THE pcb dEsign MAGAZINE

AN I-CONNECT007 PUBLICATION

December 2013

POWER INTEGRITY

isola
100 YEAR
ANNIVERSARY
1912-2012

thepcblist

THE best way to find a PCB fabricator, anywhere.

WESTAK
Sunnyvale, California, U.S.A.

[Website] [Contact Me] [RFQ]

| Overview | Contact | Specs | About | Videos | Photos | Brochures | News |

Westak is a leading manufacturer of high reliability printed circuit boards. Facilities in North America and manufacturing partners in Asia fulfill time critical prototypes through volume requirements. AS9100C, ITAR, ROHS, REACH, UL, Bellcore

Markets:	Communication, Computers, Industrial, Medical, Military/Aerospace
Board Types:	Double-sided, Multilayer
Mfg Volumes:	Prototype, Small, Medium, Large
Other Services:	Quick turn-around
Specialities:	Blind/buried vias, Carbon contacts, Controlled depth drilling, Controlled Impedance, Filled/plugged vias, Heavy copper, HDI, RF, Sequential lamination
Certifications:	AS-9100, Bellcore, ISO 9001, ITAR registered, ROHS compliant, UL

Featured Showcase

Click here to see a demo

Why YOU should Showcase:

- Capabilities listing for advanced search functionality
- Specialties and certifications listing
- Ability to upload brochures and videos
- Quick and easy "Contact" and "RFQ" buttons
- News, web and contact links

Click to see a partial list of registered OEMs!

www.thepcblist.com

A few words from our clients.

"...Not only did we gain the potential of a valued new customer, we also had the eyes of a skilled PCB expert reviewing our operations and systems providing some positive and constructive feedback."

Steve Robinson
President, APCT, Inc.

View full testimonial

" ...with Rob's years of experience performing audits and his vast knowledge, I believe Wizlogix and my end customers are benefiting. Moving forward, we will continue to explore more opportunities and collaborations with Next Level PCB services in the future."

Shawn Ng
Director/Co-Founder, Wizlogix Pte Ltd

View full testimonial

We offer a full range of auditing services for both buyers and sellers, backed by 35 years of industry experience. We'd love to talk with you about getting to the next level.

Say hello to us

NEXT LEVEL PCB
AN AUDITING COMPANY

(360) 531-3495
www.nextlevelpcb.com

FEATURED CONTENT

Designers and design engineers have focused on signal integrity for well over a decade, but now the power distribution network is taking center stage. This month, our experts take an in-depth look at power integrity analysis, as well as some common PI challenges and solutions. Don't fight the power—control it!
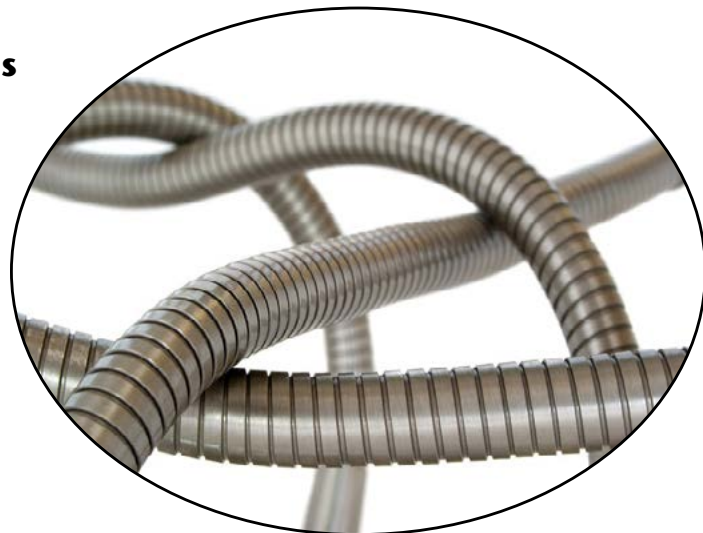
Discover the Best-in-Class Laminate for High Voltage, Tight-pitch PCB Designs
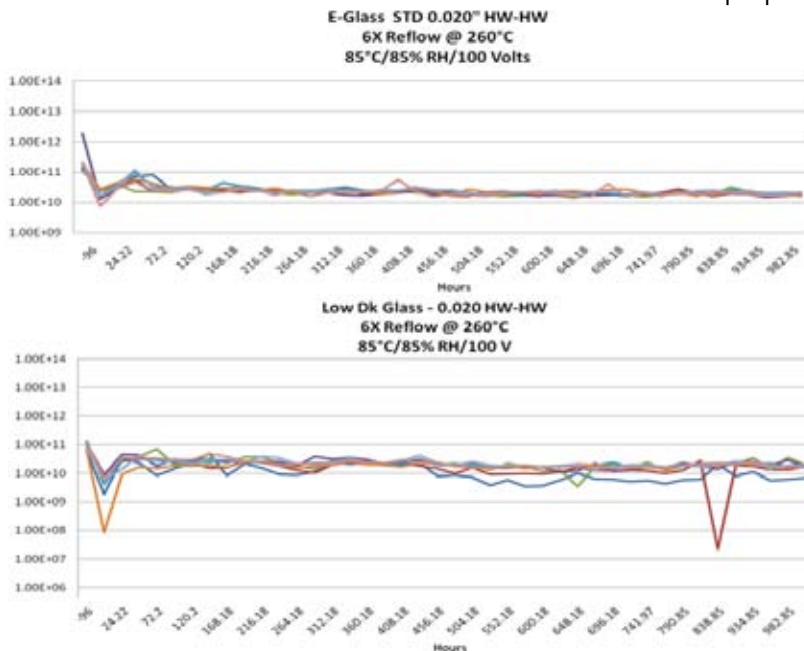
I-Speed® High Speed Digital Materials

I-Speed laminate and prepreg products are manufactured with Isola's patented high-performance multifunctional resin system, reinforced with electrical grade (E-glass) glass fabric. This system delivers a 15% improvement in Z-axis expansion and offers 25% more electrical bandwidth (lower loss) than competitive products in this space. These properties coupled with superior moisture resistance at reflow, result in a product that bridges the gap from both a thermal and electrical perspective.

I-Speed CAF Test Vehicle Results

- Passed: 85°C/85% RH/100V after 1,000 hours at 0.65 and 0.75 mm pitch
- Passed: 35°C/85% RH/10V after 500 hours at 1.0 mm pitch

I-Speed Features

- Global constructions available in all regions
- Optimized constructions to improve lead-free performance
- Improved Z-axis CTE 2.70%
- IPC 4101 Rev. C /21 /24 /121 /124 /129
- A low Df product with a low cost of ownership
- VLP-2 (2 micron Rz copper) standard offering
- Offer spread and square weave glass styles (1035, 1067, 1078, 1086, 3313) for laminates and prepregs

E-Glass STD 0.020" HW-HW
6X Reflow @ 260°C
85°C/85% RH/100 Volts

Low Dk Glass - 0.020 HW-HW
6X Reflow @ 260°C
85°C/85% RH/100 V

isola

The Base for Innovation

www.isola-group.com/i-speed

CONTENTS

Bringing Sexy Back to EDA

by Andy Shaughnessy
I-CONNECT007

Amid all of the hullabaloo in this industry, we sometimes forget one absolute truth: We're all geeks. Admit it. If you're reading this, there's no way around it: You are a geek.

Years ago, I hired an associate editor right out of college. Tracy was 22 and about as hip as 22-year-old women generally are.

After putting on my "Trainer Andy" hat, I broke down the world of electronics design for Tracy. Along the way, I mentioned that the chip designers often consider themselves to be higher up in the hierarchy of life than PCB designers. Chip designers even consider their field to be more hip and sexy than PCB design.

You sense it at shows like DesignCon and the Design Automation Conference. The IC designers treat the mere PCB designers like redheaded stepchildren. The chip guys remind me of the Prius drivers on "South Park," who cut down on smog but wind up raising the levels of "smug" to dangerously high.

Even within the chip design world, there are subdivisions of "smug." The functional verification engineers breathe rarefied air and walk on petals of lavender, while the back-end folks might as well sit at the kids' table at Thanksgiving.

We see it in the media, too. When we're all together at DesignCon or DAC, the journalists

"Geeks can be sexy."

covering chip design view PCB design editors as if we're one step above writers for *Highlights for Children.* Sometimes they wrinkle their noses as if someone is trying to mask an odor.

"Oh, you cover PCB design? I didn't know you could get into this show without an MSEE," they intone wistfully. "Isn't that just the cutest thing. Well, good for you! I'm sure it's a great little publication!"

None of them have ever pinched my cheek like a great aunt, but I wouldn't rule it out.

So, I conveyed all of this valuable information, objective and subjective, to Tracy. What did she do? She rolled her eyes.

"Come on," Tracy laughed. "You're all geeks. I don't understand the difference between ICs and PCBs yet, but their designers are all geeks, and their journalists are too. It's a difference without a distinction. You all may be a lot of things, but sexy and hip you're not. No one in this industry is."

"But we have a band," I protested. "The IC guys have a band too. We certainly can't be geeks! We play guitar!"

"Then you're slightly less geeky than the guys with pocket protectors and 14 patents," Tracy concluded. "You're the only person I know who quotes Young MC's 'Bust a Move' every single day. Please stop. It's not 1990 anymore."

And in the hallowed words of Young MC, "There it is." We're all geeks, whether we like it or not.

But there's nothing wrong with being geeks. Geeks make things work. We're always the IT guy, or gal, for our household. When something goes wrong with the computer or the Internet, we can usually fix it. We may even replace electrical outlets and the like; in my case, I draw the line at 220-volt outlets. And if we can't fix it, we do our best to diagnose the cause of the problem so we can show the electrician that we have it all figured it out.

> " *I think it's fair to say that the average person is now far more interested in innovations in electronics than he or she was even 10 years ago. We used to have to read Wired to find out about the latest in electronic gadgetry; now it's on every channel.* "

Best of all, the rest of the world is becoming geekier every day. For example, what's the biggest news this week? Amazon's helicopter drones, which may be dropping packages at your door in the next few years. This is huge news, garnering wall-to-wall coverage on the cable networks, morning chat shows and network nightly news shows.

I think it's fair to say that the average person is now far more interested in innovations in electronics than he or she was even 10 years ago. We used to have to read Wired to find out about the latest in electronic gadgetry; now it's on every channel.

We couldn't avoid hearing about Amazon's drones if we tried. All of which bodes well for electronics design. For years, much of the best and brightest young people coming out of college have gone to work in fields related to the Internet. EDA just hasn't been seen as hip or—here's that word again—sexy. But maybe, just maybe, we're all helping to change that.

It's time to let the world know that geeks can be sexy. It's a propitious time, too. The Internet is part of the background now. Consider this: Recent college grads don't remember a time without the Internet. But they remember a time without drones dropping boxes on your doorstep. Hardware design just may be the next big thing.

As we enter the holiday season, raise a toast. Here's to all of us: bringing sexy back to EDA.

Have a Happy New Year! **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 13 years. He can be reached by clicking [here](#).

It Takes a Team to Assure Power Integrity

by Brad Brim
CADENCE DESIGN SYSTEMS

SUMMARY: The proverb "It takes a village to raise a child" also applies to PCB power integrity. Multiple design team members will contribute to assuring circuit board PI as a design progresses from infancy of concept to a mature product.

It's a fact: The more effective the team, the more quickly a PCB with assured PI will result. On the front end, an electrical design engineer is responsible for the schematic, and on the back end, a layout designer is responsible for physical implementation. A PI analysis expert is typically responsible for overall PCB PI and participates early to guide the contributions of others.

In this article, we will review the current analysis approaches to PCB PI. Then, we will introduce a team-based approach to PCB PI, including a discussion of its impact on individual team members as well as the overall approach to assuring PCB PI.

Present-Day Power Integrity Analysis

There are two distinct facets of PCB PI: DC and AC. DC PI guarantees that adequate DC voltage is delivered to all active devices mounted on a PCB (often using IR drop analysis), assuring constraints are met for current density in planar metals and total current of vias, and lastly assuring temperature constraints are met for metals and substrate materials. AC PI concerns the delivery of AC current to mounted devices to support their switching activity while meet-

We Deliver...A 5-Star Performance

At U.S. Circuit, we are UL Certified to build **hybrid construction** with Rogers/FR408 family & Rogers/370HR as well as Isola I-Speed materials.
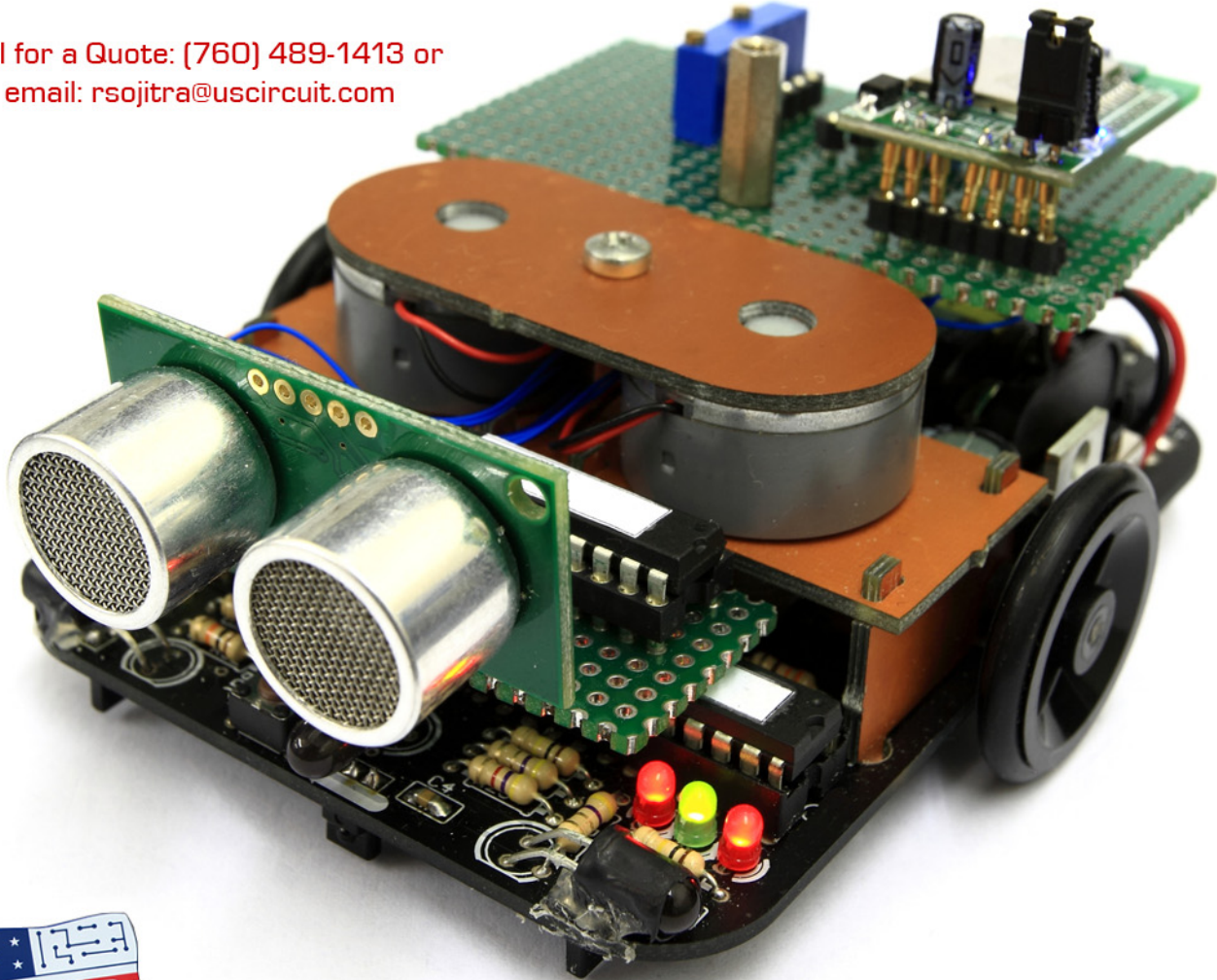
U.S. CIRCUIT
Manufacturer of
Printed Circuit Boards

U. S. Circuit, Incorporated
2071 Wineridge Place
Escondido, CA 92029
Ph: (760) 489-1413
Fax: (760) 489-2965
www.uscircuit.com

Superior Quality
Superior Service

ITAR Registered   ISO 9001:2008   MIL-PRF-55110G

IT TAKES A TEAM TO ASSURE POWER INTEGRITY *continues*

ing constraints for transient noise voltage levels within the power delivery network (PDN). The PDN noise margin (variation from nominal voltage) is a sum of DC IR drop and AC noise.

DC PI is governed by resistance of the metals and the current pulled from the PDN by each mounted device. For many years, resistive network models have been applied for approximate DC PI analysis. With recent increases of computer speeds and significantly larger addressable memory, the application of layout-driven detailed numerical analysis techniques has proliferated for DC PI. Approximation occurs less, accuracy is higher, and automation of whole-design analysis and post-processing results are available commercially. In fact, DC PI analysis for PCB designs has become a "sign-off" requirement for many OEMs. Figure 1, on the left, shows typical results for current density.

Because metal conductivity is temperature-dependent, DC IR drop is a nonlinear analysis.

Case studies for high-power design demonstrate that IR drop results vary by more than 20% when temperature effects are considered. A solution is implemented in Figure 1. A linear electrical analysis is first performed at ambient temperature and the resulting power loss is applied to perform a linear thermal analysis. Then another linear electrical analysis is performed with consideration of localized temperature-dependent conductivity. This process converges within a few iterations. The result is an accurate characterization of PCB IR drop that assures the PDN noise margin is not wasted.

AC PI is governed by voltage regulator modules, loop inductances, decoupling capacitors (decaps), and plane capacitance. AC PI effects tend to be global in nature due to plane resonances, plane-to-plane coupling, and shared reference planes. This mandates full-board analysis and precludes more resource-intensive analysis algorithms. The most commonly applied AC PI
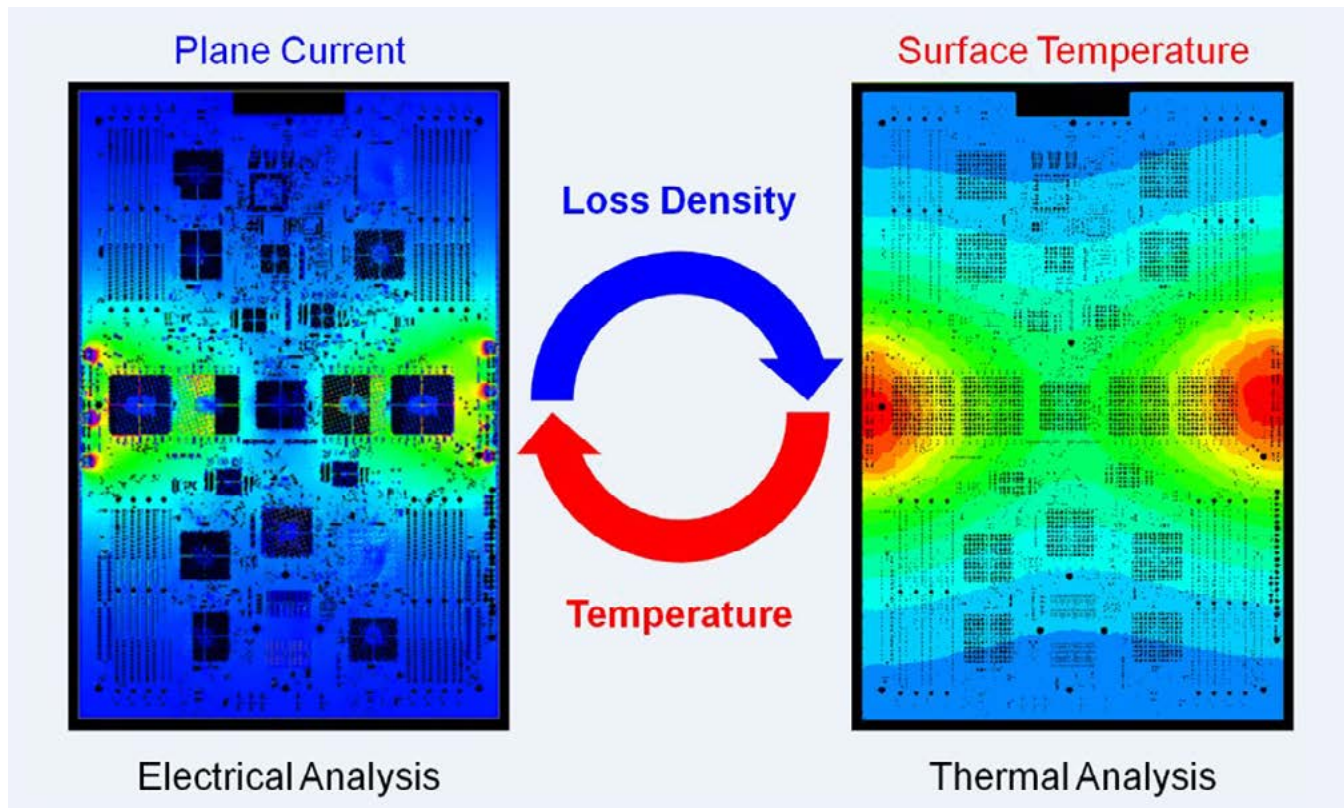

Figure 1: Current density (left) and temperature distribution (right) for a PCB design due to DC power delivery as two linear solutions are iteratively linked to address nonlinear electro-thermal analysis.

analysis for PCBs is a hybrid of circuit theory and electromagnetic (EM) analyses. This type of analysis is available in the frequency domain to extract S-parameters, or in the time domain to directly generate transient waveforms. PDN behavior of even the largest and most complex PCBs may be accurately characterized from DC to multi-gigahertz in tens of minutes using single- to low double-digit gigabytes of memory.

Though transient PI analysis may seem attractive because it directly yields noise waveforms, it is less commonly applied than frequency domain impedance analysis. "Target impedance" profiles are applied as PI constraints. Lower impedance corresponds to lower transient noise. In the absence of direct vendor specification, reasonable target impedance may be estimated based on device specifications for voltage ripple and AC switching current. Figure 2 shows a comparison of frequency domain and time domain results. Peak-to-peak PDN noise is reduced for the optimized design by 12%, while the component and manufacturing cost of the decap implementation is reduced by 21%.

A Team Approach to Power Integrity

Past contributions to DC and AC PI have focused on analysis approaches for PI experts. Pre-layout decap selections and initial IR drop analyses are typically performed by these experts. This represents an excessive time investment at the front end of a design for a back-end focused expert. A more collaborative team-based approach to PI can benefit all involved. An approach where simple analyses that yield actionable results could be set up and performed by other members of the PI team would be ideal. This PCB PI team would comprise three key members: design engineer, layout designer, and PI analysis expert, as shown in Figure 3.

Cadence's Allegro Sigrity PI illustrates the concepts of such a team-based approach to PCB PI. This team approach enables design engineers and layout designers to contribute earlier and more effectively to PCB PI.

PCB design engineers are responsible for front-end tasks. They must generate an initial bill of materials (BOM) to enable cost feasibility studies and assure electrical design intent by generating circuit schematics. Design engineers work independently of DC PI concerns, but to support AC PI, they must add decaps and include them in the BOM and the schematic. Some device vendors provide datasheet guidance for decap selection (type and/or quantity), but many do not. Even with datasheet guidance, it is tedious for design engineers to assemble and interpret the specifications for each device, instantiate all the unique components, assure they appear logically in the schematic, etc. No mechanism has existed for physical placement guidance to be communicated for back-end application.
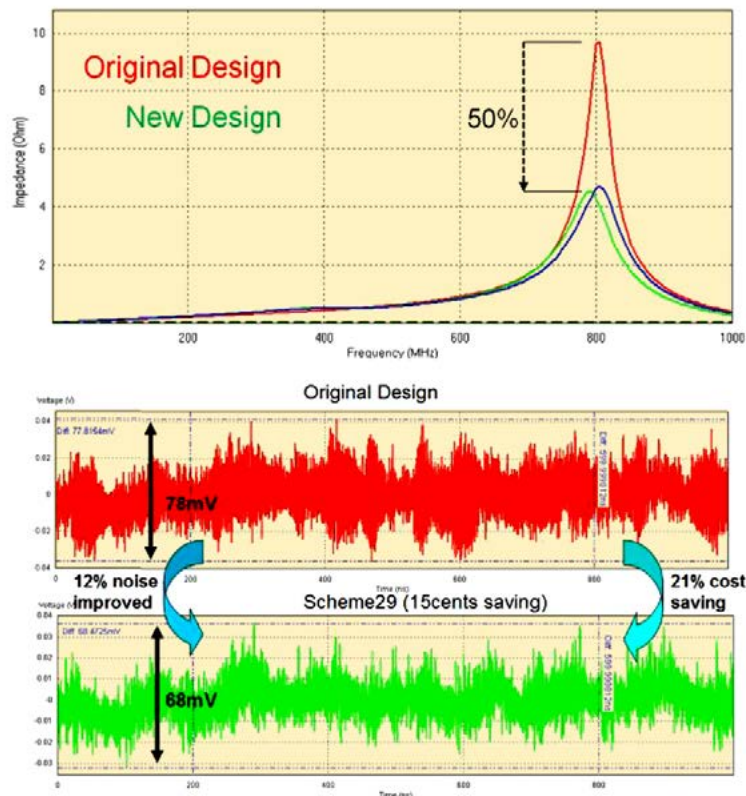

Figure 2: Impedance profile and transient PDN noise of a DIMM before and after the decap implementation was optimized.
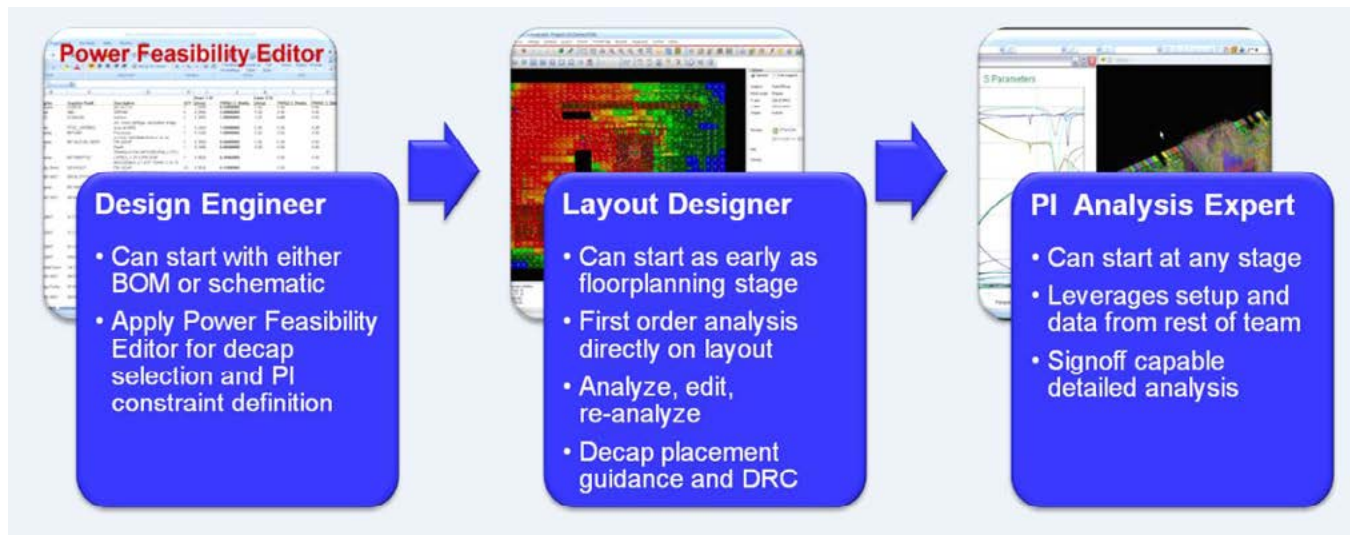
Figure 3: Roles and responsibilities of the PCB PI design team.

Figure 4: PI constraint set contents viewed from the constraint manager.

Constraint-based design methods provide a uniform interface for design intent information and enable automation of a broad class of tasks across front-to-back flows. PI (electrical) constraint sets (PI Csets) have been added to save all component-level PI information. Design engineers may apply PI Csets to quickly and completely define PI design intent for all mounted components. PI Csets also automate instantiation of components and inclusion in the BOM.

An example of a PI Cset is shown in Figure 4. PI Csets contain information for each power rail, such as decap component names, quantity of each component, package type, and physical placement guidance.

PI Cset creation is automated by a Power Feasibility Editor (PFE). It provides a mechanism to enter datasheet decap selection and physical placement guidance. A view of the PFE is shown in Figure 5. In addition to placement guidance,
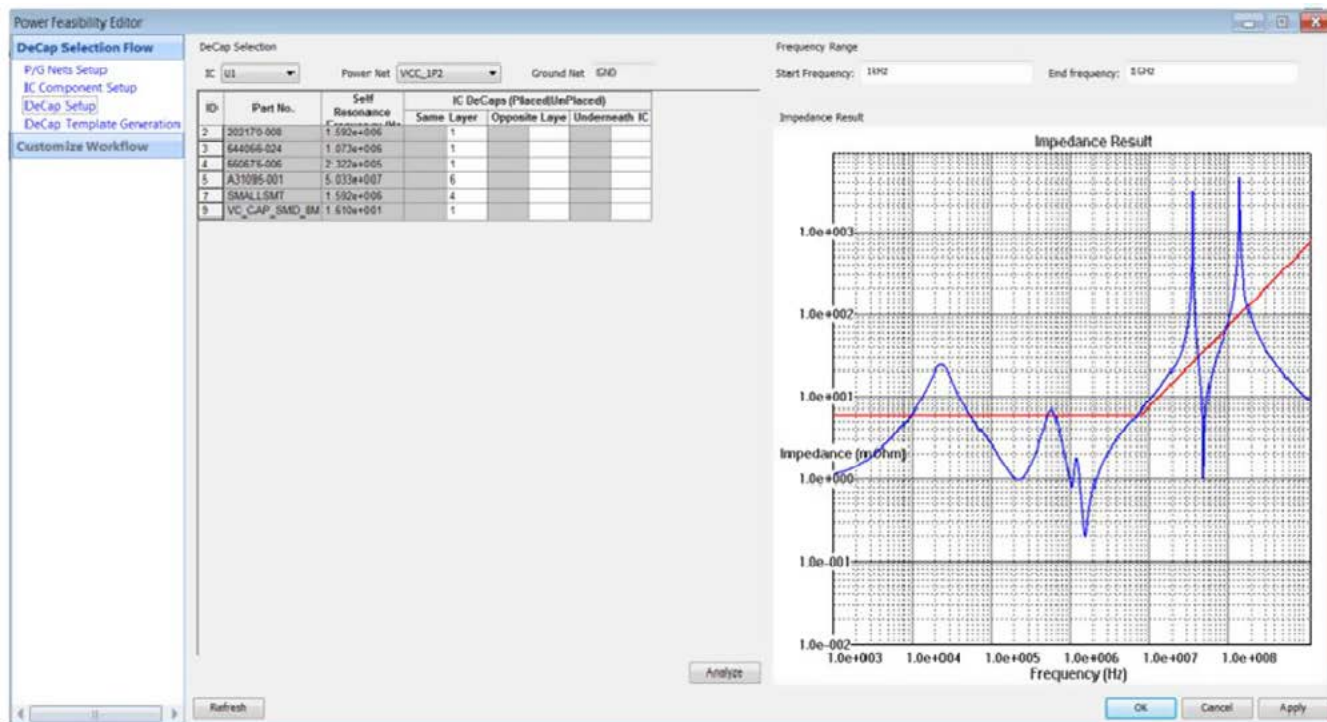
Figure 5: Single-point analysis results in the Power Feasibility Editor.

a PI Cset communicates to the layout designer component and power rail association for decaps to enable more reliable placement.

PFE also provides access to approximate and detailed pre-layout analysis for selection and placement of decaps. High-level specifications are made to generate target impedance profiles when device vendors do not provide them. An approximate PI analysis called "single-point" is provided for interactive decap selection. PI Csets are generated at the click of a button from within PFE.

Unlike design engineers, layout designers are concerned with DC PI issues. Layout designers control metal shapes and vias and these, in turn, control PI behaviors for DC IR drop and current flow. Layout designers are able to intuitively understand and act upon analysis results for these DC PI effects. DC analysis is fast but not in real time to enable dynamic updating of analysis results as layout updates are made.

A split-screen view is provided, as shown in Figure 6, to support a fixed view of analysis results as layout designers dynamically make up-

dates to address IR drop or current constraint issues. The two views are synchronized for operations that affect the display, such as layer changes, zoom, and pan. This split-screen view of DC analysis results may be applied by layout designers as they craft an initial layout before involvement of the PI analysis expert. It may also be applied with detailed analysis results performed separately by PI analysis experts as a more effective method to communicate where PI issues exist in the design. In fact, the same detailed analysis performed by the PI analyst may be launched by the layout designer to more quickly verify improved PI performance.

Layout designers strongly influence AC PI success with their placement of decaps. Decaps placed close to a device generally benefit PI, but they also restrict routing channels due to decap mounting vias. Decaps placed too far from a device will be ineffective at providing switching current to the device and negatively affect PI. Present design methods do not typically provide decap placement guidance, including information as simple as which device is associ-

ated with a decap. PI Csets enable more effective placement of decaps by layout designers by conveying design intent. The associated device and power rail and placement guidance are all specified in the PI Cset.

A decap placement mode is implemented to support layout designers, as shown in Figure 7. Simply select a mounted component, select a power rail, and cycle through a point-and-click placement process. The selected device is highlighted and three optional visual placement guidance displays are available: device to decap distance for top layer, device to decap distance for bottom layer, and decap effective radius. The first two are defined in the PI Cset and conceptually familiar. The decap effective radius is the maximum distance at which the decap will be maximally effective. It is a function of the stack-up and decap mounting parasitics as well as the decap value and its intrinsic parasitics. It is dynamically computed as the cursor moves

due to local availability of metal shapes on the associated power and ground layers.

Design intent and analysis setup information specified by design engineers and layout designers are available to PI analysis experts to ease setup for detailed PI analysis. PI Csets serve as a convenient mechanism to communicate updated placement guidance or requirements for updates on decap selection (either type or quantity) for a specific device instance or all devices to which a PI Cset is applied. Changes to PI Csets also convey information back to the design engineer and enable automated update of schematic and BOM.

Summary

Presently available analysis tools for PCB PI continue to serve the design community well. They are more effective when combined with a front-to-back, constraint-based approach. Each member of the team is able to more efficiently
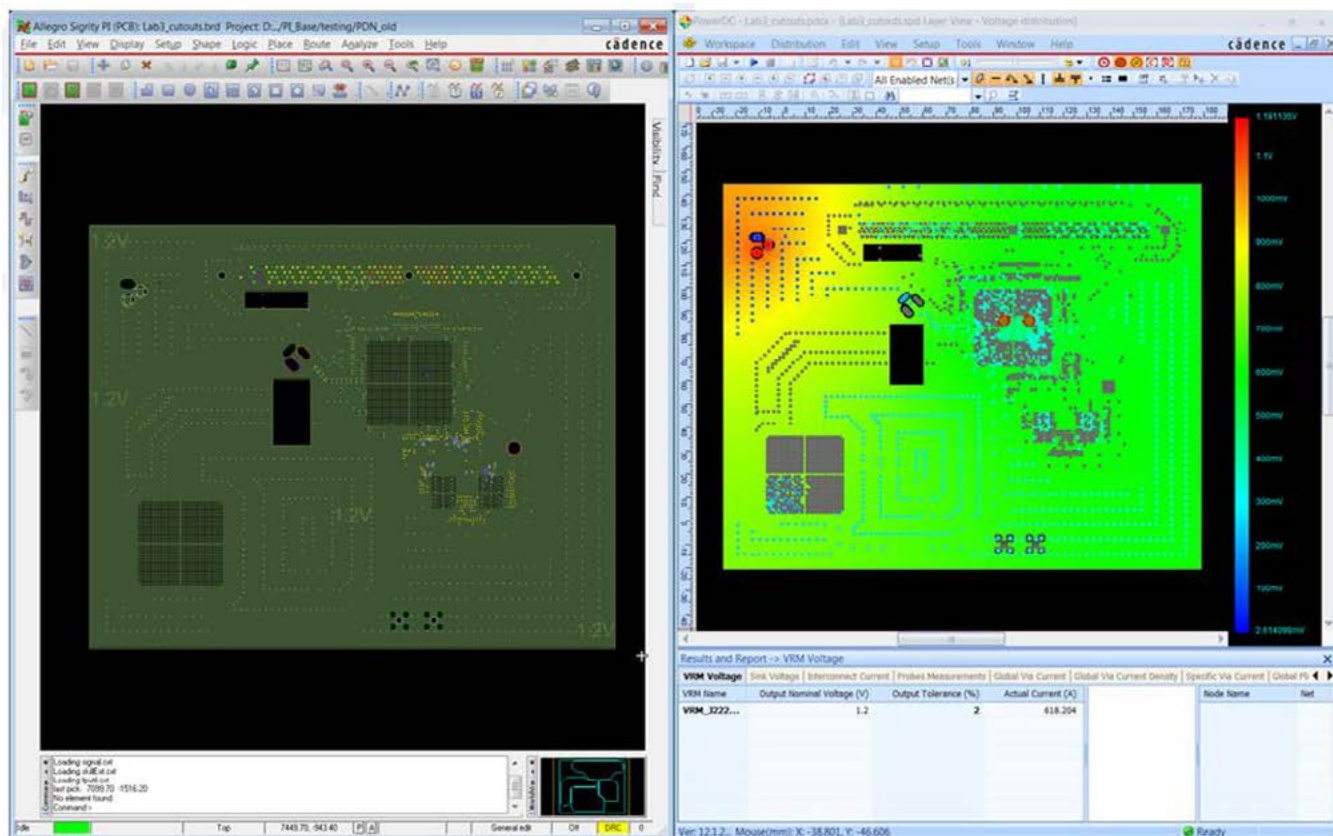

Figure 6: Split-screen view of layout (left) and IR drop analysis results (right).
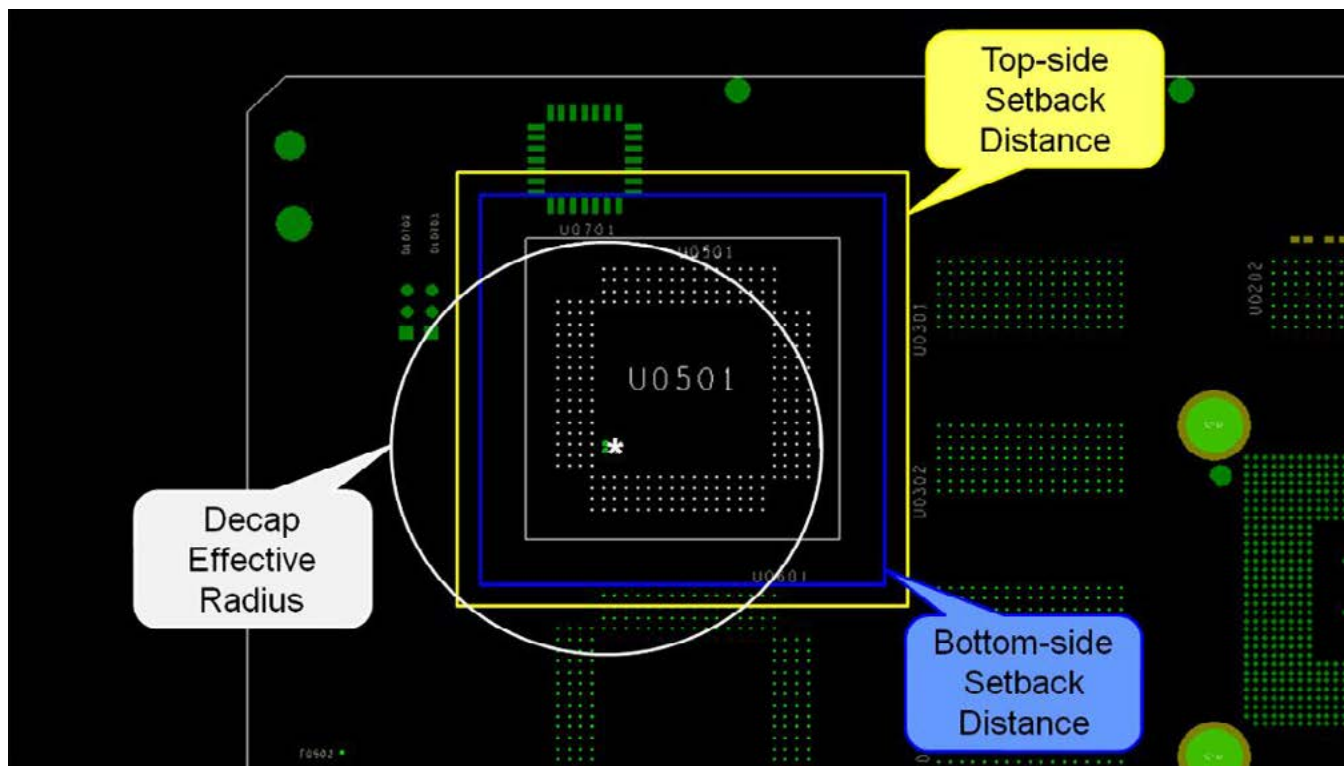
Figure 7: Layout view during decap placement for device U0501 with top (yellow) and bottom (blue) setback distances and decap effective radius (white circle) displayed.

accomplish their individual tasks and communicate design intent information to colleagues for increased efficiency of the overall PCB design flow. This approach provides access to actionable analysis results where they are most impactful. It also leverages earlier defined analysis setup information for the PI expert, and eases communication of design changes from his back-end role to his colleagues who are on the front end. **PCBDESIGN**

Brad Brim is senior staff product engineer with Cadence Design Systems. His responsibilities concern SI/PI applications for boards, packages and chip/package/ board systems. For over 20 years he has contributed to high-speed and high-frequency design solutions via development, applications engineering and marketing roles.

Invisible Printed Electronics Using Carbon Nanotubes

Researchers at the UCLA startup Aneeve Nanotechnologies have demonstrated the first fully printed and invisible electronics using carbon nanotubes.

Researchers built the electronics made of thin film transistors to be invisible to the naked eye by incorporating devices made solely using carbon nanotubes (CNT) materials that are inherently transparent. In addition to being printable, CNT materials are able to operate at faster processing data speeds.

"This is the first practical demonstration of carbon nanotube-based printed circuits for transparent applications," said Kos Galatsis, an associate adjunct professor of materials science at UCLA Engineering and a co-founder of Aneeve.

Comparing Cable Shields

by Istvan Novak
ORACLE
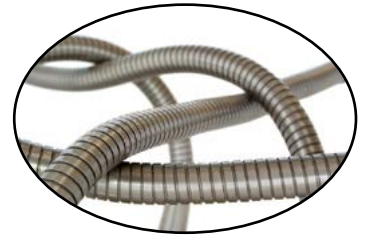
In my October column, we looked at the importance of properly terminating cables even at low frequencies and also showed how much detail we can lose in PDN measurements when we use bad-quality cables[1]. In this column we will analyze a step further the shield in our cables.

As a reminder, Figure 1 shows the noise pickup through the shield of two different cables. Data was captured with a 1-GHz bandwidth oscilloscope. Both cables had 50-ohm factory-mounted BNC connectors at their ends. The oscilloscope input was switched to 50-ohm input impedance and the cables were attached to a DUT with a BNC connector. The DUT (a small DC-DC converter evaluation board) was turned off, generating no signal on its own. The noise we see on the oscilloscope is the signal pickup of the cable from the air.

The signal of more than 8 mVpp that we see with one of the cables was consistent, not only occasional short bursts. I live in a residential area in the woods, with no visible industrial plant or antenna tower nearby. It might be interesting to track down the source of the noise, but from my perspective it is more useful to look at the differences in the cable braid constructions.

Flexible coaxial cables have conductive foil, braided wire or a combination of these serving as the outer conductor, which also serves as shield in single-ended cables. Braided shields come in single or multiple layers of wire mesh. The cables used for Figure 1 have single-braided shield with no foil. Figure 2 shows close-up photos of two cable braids, taken with a small USB-powered microscope camera.

Figure 1: Voltage measured at the DUT BNC connector with two different cables, with the DUT turned off.

8 1/2

Reasons You WIN with Ventec

ventec

Show Me

#1

#2

#3

#4

#5

#6

#7

#8

#8½

Choose Your Reason

Ventec Europe
ventec-europe.com

Ventec USA
ventec-usa.com

Ventec International Group
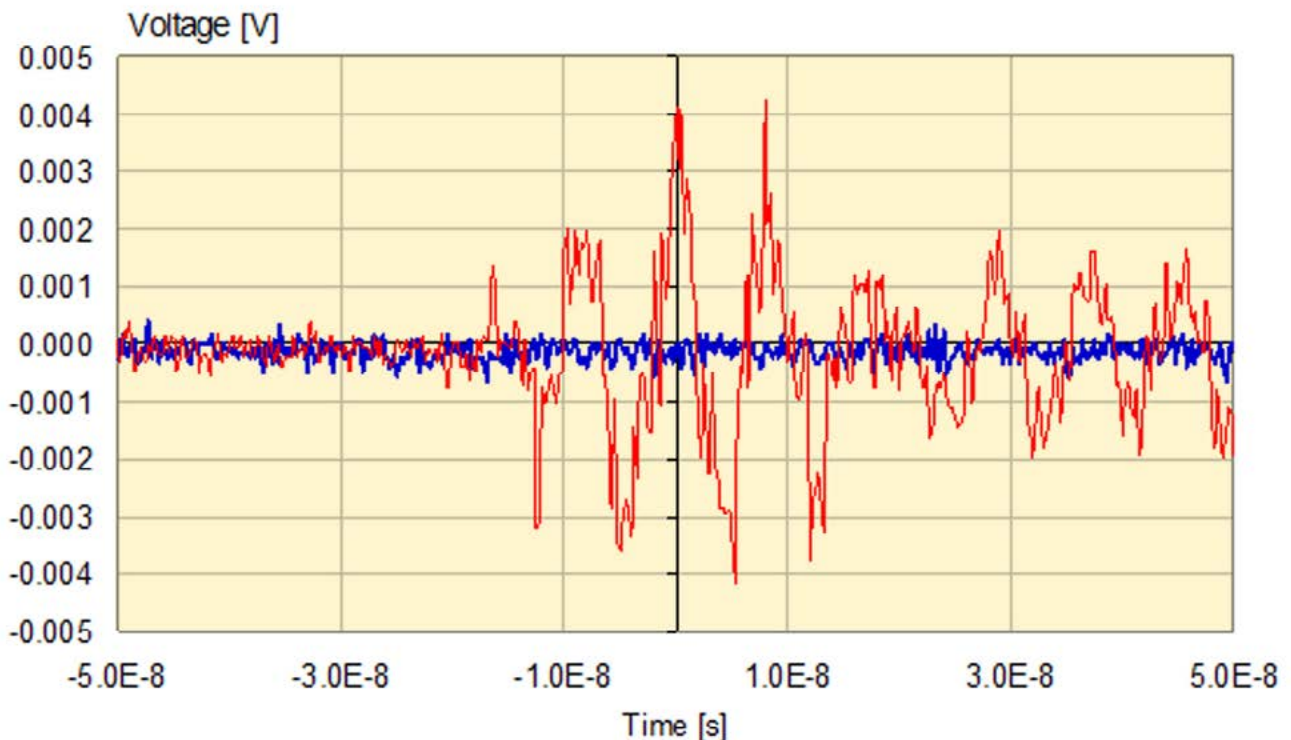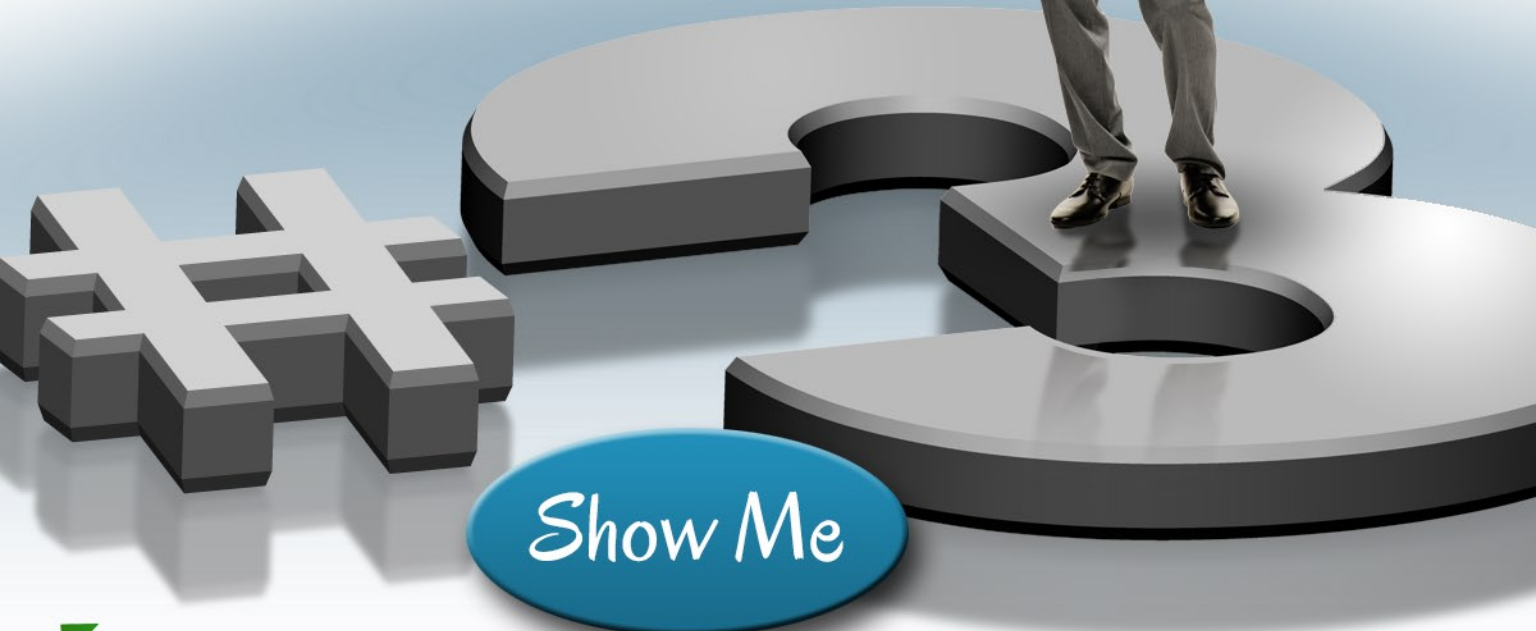venteclaminates.com

COMPARING CABLE SHIELDS *continues*

Low-cost RG174 cable   Raw RG178 cable
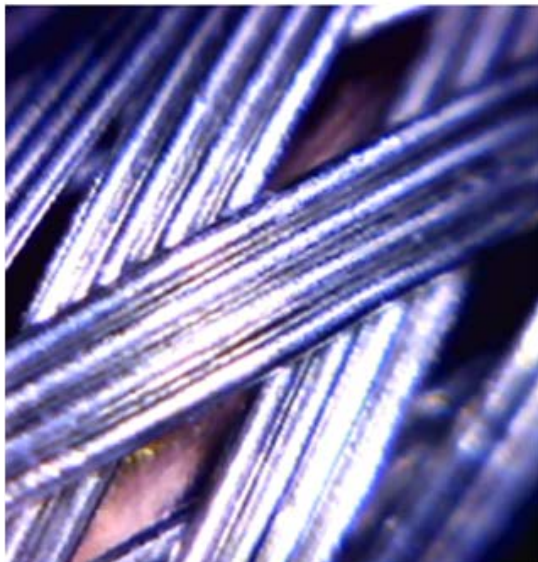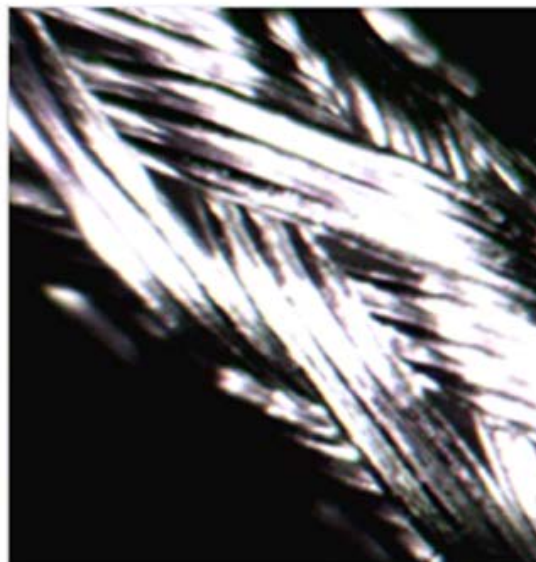
Figure 2: Close-up photos of different cable braids.

The photo on the left shows the braid construction of the coaxial cable used for the red trace in Figure 1. There are strips of wires, loosely braided around the dielectric insulation surrounding the center conductor. There are rhomboid-shaped openings, where the orange-pink color of the dielectric insulator shows through. To give you a sense of scale: The diameter of the cable, 80 mils or about 2 mm, fills the diagonal of the photo. These little openings on the braid create the transparency of the cable at high frequencies, where otherwise the skin depth is less than the braid thickness, so we could expect low surface transfer impedance and therefore good shielding. The photo on the right shows a better-quality braid from a spool of RG178 coaxial cable I bought from a different source. Note that this is not the cable that produced the blue trace in Figure 1; that cable was too expensive for me to cut it up. Nevertheless, this photo illustrates that a good quality braid does not exhibit openings of the size we see in the left photo.

To check further the differences in cable braids, I used the signal-generator function of a small pocket-size vector network analyzer (VNA) that was developed by radio amateurs primarily for ham-radio measurements[2]. The unit has a synthesized RF source, with an adjustable frequency in the 0.1–200 MHz range. The source has 50-ohm internal impedance, which terminates the cable at the driver side. I attached the cables used for Figure 1 and measured the leakage through the cable braid by a small pickup loop connected to my Tektronix TDS540 oscilloscope. The setup is shown in Figure 3.
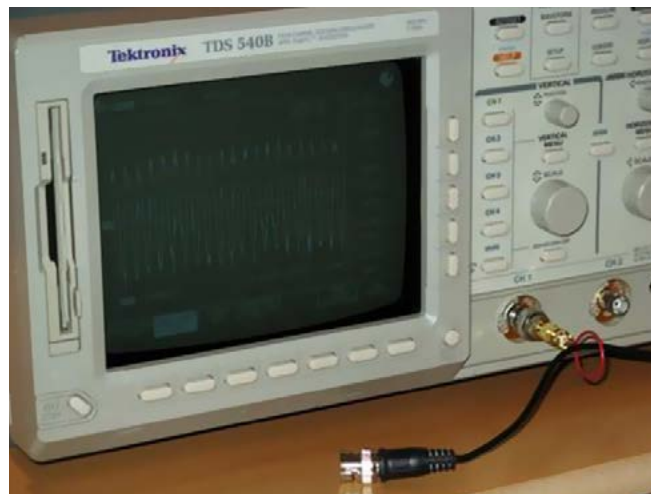
Figure 3: A small pickup loop (red wire) connected to CH1 of the oscilloscope detects the field leaking through the shield of the coaxial cable.
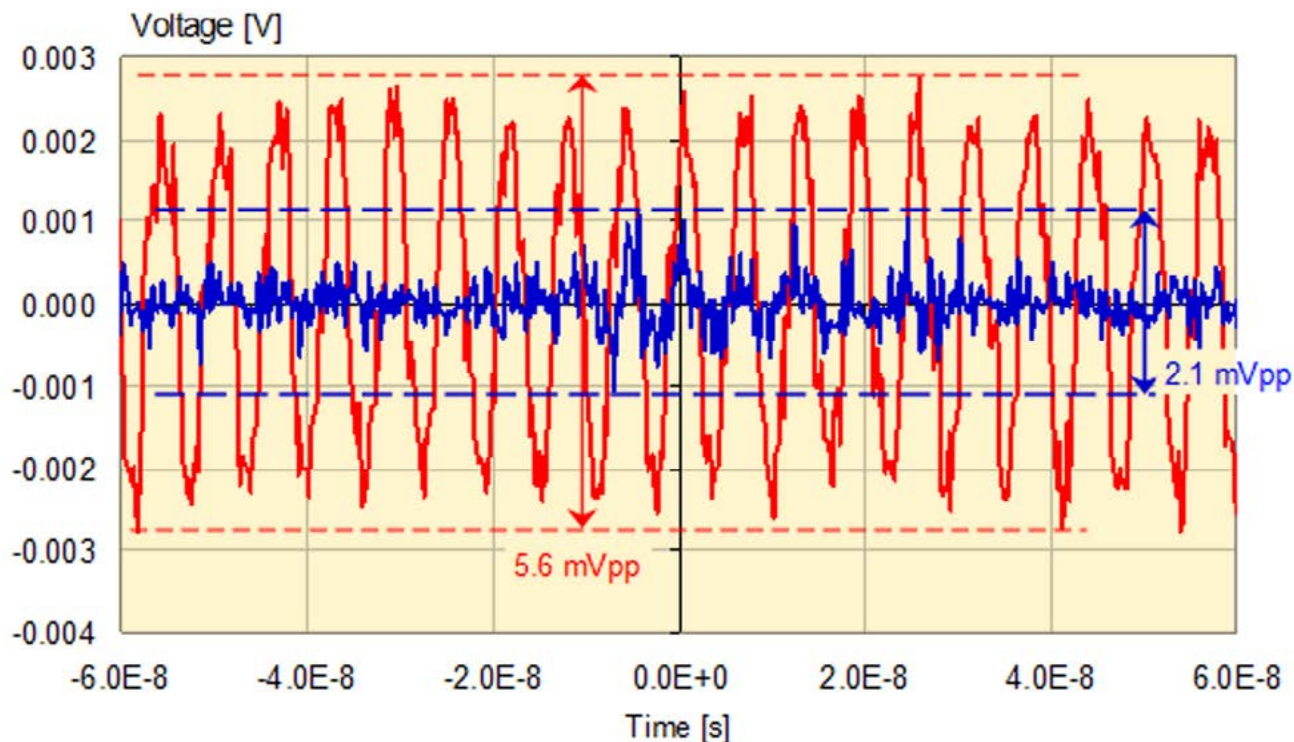
Figure 4: Signal pickup from a poorly shielded cable (red trace) and well-shielded cable (blue trace) measured with the setup shown in Figure 3.

The frequency of the source was manually changed to find the peak reading on the oscilloscope. In the case of the cable that produced the red trace in Figure 1, this happened to be around 160 MHz.

The drive strength was set to 0 dBm and, to suppress resonances in the detector loop, the oscilloscope input was switched to 50-ohm input impedance. The signals picked up by the loop for the two cables of different shielding quality are shown in Figure 4. For the more poorly shielded cable, the resulting waveform (red trace in Figure 4) shows a large sinusoidal component way above the noise floor of the oscilloscope. For the better shielded cable (blue trace in Figure 4), the maximum signal pickup across a range of frequencies is much smaller: mostly random noise with little sinusoidal component.

Of course this crude illustration does not represent a systematic quality measurement: it is rather a simple comparison showing big differences in the quality of cable shields. In the next column, we will use the pocket-size VNA to measure the approximate frequency-dependent transfer function through the cable braids under various conditions. Stay tuned. **PCBDESIGN**

References

1. QuietPower column "Cable Quality Matters," also available here.
2. MiniVNA-Pro, available here.
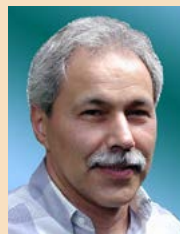
Dr. Istvan Novak is a distinguished engineer at Oracle, working on signal and power integrity designs of mid-range servers and new technology developments. With 25 patents to his name, Novak is co-author of "Frequency-Domain Characterization of Power Distribution Networks." To read past columns, or contact Novak, click here.

PCB007 News Highlights

Schweizer Electronic Reappoints Board Members

The Supervisory Board of Schweizer Electronic AG has reappointed Board Members Dr. Marc Schweizer and Nicolas Schweizer until 2018. Their contracts were previously ending in July 2015 and March 2016, respectively.

Endicott Interconnect Now i3 Electronics

The company has completed a successful transition to i3 Electronics, Inc. from Endicott Interconnect Technologies. The sale to i3 Electronics closed October 31, 2013. The company appreciates the patience and the support that employees, customers, and suppliers have provided during a challenging 2013.

IPC: PCB Book-to-Bill Ratio Falls Due to Sluggish Growth

"A combination of slower order growth and shipments that exceeded bookings in August and September brought the book-to-bill ratio below parity to 0.98," said IPC's Director of Market Research Sharon Starr. "Although year-on-year shipment growth in the North American PCB industry is still negative, it has been moving in the right direction."

Multilayer Technology Named Jacobs' 2013 Subcontractor of the Year

Multilayer Technology has been selected as the 2013 Subcontractor of the year by Jacobs Technology. This award from is the result of a partnership between Jacobs Engineering, NASA-JSC, and Multilayer Technology.

Despite Regulations, Lead Usage Continues to Grow

Companies in the electronics industry have spent billions in recent years to remove lead from solder, ensuring that the few ounces of this toxic metal on a printed board don't leach into water supplies. Though regulators are attempting to curtail lead usage, it's growing by approximately 5% per year.

Viasystems Upgrades, Opens New Facility in Anaheim, CA

Viasystems Group, Inc., a leading provider of complex multilayer PCBs and electromechanical solutions, has announced the opening of its new North American PCB Technology and Manufacturing Center in Anaheim, California.

IPC: Printed Electronics Gains Momentum

The PE industry continues to expand rapidly. Nearly every week, companies are announcing positive steps that demonstrate solid growth. For example, Optomec, a global supplier of additive manufacturing systems for 3D printed metals and PE, reported a 100% increase in bookings compared to the first half of last year.

TTM Announces Retirement of Kent Alder; Posts Q3 Loss

The company has announced that Kenton K. Alder, TTM's CEO, will retire effective January 1, 2014 and that its Board of Directors will appoint Thomas T. Edman, currently the company's president, as its next chief executive officer.

Dragon Circuits: Old Company; New Name & Ideas

Raj and Gunny Babaria acquired North Texas Circuit Boards and began rebuilding the failing company. After shedding a few long-time employees and investing in new equipment, the two say they are ready to make Dragon Circuits into a twenty-first century technology company.

Kyocera Raises Forecasts Amid PCB Firm Acquisition

Kyocera Corporation has reported net sales of 699.66 billion yen ($7.14 billion) for the first half of fiscal year 2014, up by 15% from the same period last year. Profit from operations reached 58.2 billion yen ($594 million), up by 124.8% from the first half of fiscal year 2013.

Our family is over **250** strong ...and growing.

We have more than 250 active customers, and we give each and every one industry-leading service and support. They are like family to us. In addition to delivering quality and reliability, we take the time to provide the service and support that makes each job a great experience for every member of our (growing) family.

| Learn more about Dragon Circuits | Sounds great! Let's start a quote. |

DRA ON
CIRCUITS

Legendary manufacturing, service and engineering.
www.dragoncircuits.com | info@dragoncircuits.com | 972.790.7610

Thermal Management of High-Frequency PCBs

by John Coonrod
ROGERS CORPORATION

Thermodynamics can be a difficult enough subject to understand. But when combined with high-frequency PCB design and fabrication, it can really get complicated. Thermal management of PCBs has received a lot of attention over the past few years and it will probably continue as new technology pushes the limits of this issue.

For simplicity purposes, we will only discuss two sources of heat generation. One source of heat on the PCB is an active device or chip generating heat. The other source occurs when RF power applied to the circuit causes the heat. Of course there can be a combination of these sources, but to keep this column simple, the individual sources will be addressed independently. And for simplicity, examples will be given for

a double-sided (microstrip) circuit, with a heat sink attached to the ground plane side of the circuit.

The basic concept of thermodynamics related to PCBs is concerned with thermal conductivity, heat flow and thickness of the circuit. In the case of a double-sided circuit, the copper has extremely high (good) thermal conductivity, but the substrate is typically in the range of a thermal insulator with very low conductivity. Having a high heat flow is good for keeping the circuit cooler by more efficient heat transfer from the heat source to the heat sink. The heat sink is designed to dissipate the heat away from the circuit and is typically a large metal plate bonded to the PCB with some cooling functionality.

THERMAL MANAGEMENT OF HIGH-FREQUENCY PCBS *continues*

As mentioned, most substrates used in the high-frequency PCB industry have low thermal conductivity and are in the range of 0.2–0.3 W/m/K. A common tradeoff to improve heat flow and ultimately thermal management is to use a thinner substrate, which gives a shorter heat flow path and enables more efficient transfer of heat to the heat sink. If the heat source is a chip mounted on the circuit, this is sometimes helpful and often copper-plated vias are placed beneath the chip to act as thermal channels to the heat sink.

In the case of a high-frequency circuit with PCB circuit traces that heat up due to RF heating, the selection of thinner substrates may be troublesome because it can generate even more heat. The heat generated by RF heating is from insertion loss, and a circuit with more loss will generate more heat. Typical high-frequency RF circuits are of the controlled impedance variety, and a thicker substrate will require a wider conductor to maintain this impedance. A thicker substrate and wider conductor will generally have lower insertion loss, which means there will be less RF heat generated. Unfortunately, a thicker substrate will have a longer heat flow path from the RF heat generated on the signal plane to the heat sink on the ground plane.

There are some tricks that can be beneficial for using thin, low-loss, high-frequency laminates. When a laminate is relatively thin, the conductor surface roughness will contribute to the insertion loss to a greater extent than a thick laminate. A thin laminate using copper with a smooth surface will have less conductor loss, which in turn will cause lower insertion loss and a smaller amount of heat generated. Additionally, the thinner laminate will be a shorter heat flow path, so thermal management issues will benefit.

The selection of material becomes more important for high-frequency, high-power PCB ap-

> *A thin laminate using copper with a smooth surface will have less conductor loss, which in turn will cause lower insertion loss and a smaller amount of heat generated. Additionally, the thinner laminate will be a shorter heat flow path, so thermal management issues will benefit.*

plications. Even though a thicker substrate will have a longer heat flow path, it can be less of an issue if the substrate has a very low dissipation factor. The lower dissipation factor will reduce the insertion loss and cause less RF heat generation. Ideally it would be good to have a substrate with very low dissipation factor and a high thermal conductivity; however, that is an extremely unusual combination of properties for high-frequency laminates. The substrates that typically offer the lowest loss are the PTFE-based laminates, and most of them have thermal conductivity numbers in the range of 0.2 W/m/K–0.3 W/m/K.

Recently, there has been several laminates brought to the market claiming high thermal conductivity and low loss. Many of these laminates, depending on how they were tested, do not have as high thermal conductivity in actual use as one might expect. There are exceptions, though, including RT/Duroid 6035HTC, which has a very low dissipation factor (0.0013 @ 10 GHz) and extremely high thermal conductivity at 1.44 W/m/K.

The general desired properties of circuit materials for thermal management of high frequency PCBs are low dissipation factor, high thermal conductivity and smooth copper for thin constructions. However, there are typically some tradeoffs, so it is recommended that you contact your material supplier when designing a new PCB application where thermal management is a concern. **PCBDESIGN**

John Coonrod is a market development engineer for Rogers Corporation, Advance Circuit Materials Division. To read past columns, or to contact Coonrod, click here.

The 10 Deadly Sins of Electronics Manufacturing

**by Real Time with...
SMTAI**

Jim Hall, principal of ITM Consulting, discusses his SMTAI workshop that focused on the 10 deadly sins he's found while auditing manufacturers. Lust, ignorance...it's all there!

RealTime with...
VIDEO PRESENTATION

PRESENTED BY I-CONNECT007

CLICK
TO VIEW

realtimewith.com

Magnets End Era of Computer Transistors

New work by researchers at UC Berkeley could soon transform the building blocks of modern electronics by making nanomagnetic switches a viable replacement for the conventional transistors found in all computers.

For more than a decade, researchers have been pursuing magnets as an alternative to transistors because they require far less energy needs when switching. However, until now, the power needed to generate the magnetic field to orient the magnets so they can easily clock on and off has negated much of the energy savings that would have been gained by moving away from transistors.

UC Berkeley researchers overcame this limitation by exploiting the special properties of tantalum.

In a paper published online in the journal Nature Nanotechnology, the researchers describe how

they created a so-called Spin Hall effect by using nanomagnets placed on top of tantalum wire and then sending a current through the metal. Electrons in the current will randomly spin in either a clockwise or counterclockwise direction. When the current is sent through tantalum's atomic core, the metal's physical properties naturally sort the electrons to opposing sides based on their direction of spin. This creates the polarization researchers exploited to switch magnets in a logic circuit without the need for a magnetic field.

"This is a breakthrough in the push for low-powered computing," said study principal investigator Sayeef Salahuddin, UC Berkeley assistant professor of electrical engineering and computer sciences.

Other co-authors of the study are graduate student and lead author Debanjan Bhowmik, and Long You, a research scholar.

DARPA, Semiconductor Research Corporation and the National Science Foundation helped support this work.
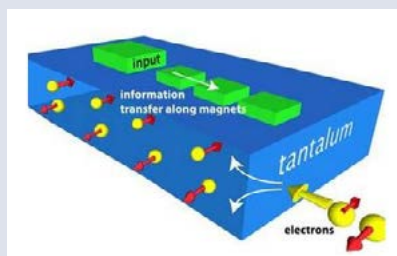
The Intersection of Unmanned Vehicle Systems and Electronics Technology

by **John Vaughan**
CIRCUIT SOLUTIONS, LLC.

This article originally appeared in the November issue of *The PCB Magazine.*

SUMMARY: The attributes of flex and rigid-flex circuit technologies uniquely mesh with the size, weight and power (SWaP) and electronics packaging requirements and challenges of unmanned vehicle systems and robotics industries, which begs the question asked by AUVSI 2013: When the world of unmanned systems comes together, where will you be?

Widely recognized as the premier event for unmanned systems and robotics in the very near future, it was with great anticipation that I attended this year's Association for Unmanned Vehicle Systems International (AUVSI) 2013 event at the Walter E. Washington Convention Center in Washington, D.C.

With over 600 highly innovative companies exhibiting, it was an eye-opening view into an industry that is rapidly morphing and poised for tremendous growth. The technology being created, the potential markets, the myriad of applications and the momentum are all undeniable.

When most people think of unmanned systems, they think only of UAVs. The market is extraordinarily broader in scope than just UAVs, with a very large contingent of air, land and sea systems all on display at AUVSI, including: underwater vehicles and systems; unmanned ground cargo transport; snake cameras; robotic surveillance fish; bomb and mine defuse systems; shipwreck exploration systems; agricultural systems for crop surveillance; and

STEP into OrCAD 16.6

View, Verify, and Share in 3D

Cadence® OrCAD® 16.6 allows product development to bridge electrical and mechanical design with bi-directional 3D capabilities. Import 3D mechanical elements such as the board enclosure directly into the PCB environment in order to ensure an accurate fit. Export a 3D model of your circuit board for use in mechanical and thermal design software. Increase productivity and decrease time to market with the advanced features of OrCAD 16.6.

To learn more about the 3D capabilities of OrCAD 16.6 visit www.ema-eda.com/OrCAD166.

cādence®

EMA | Design Automation™
ema-eda.com

search-and-rescue systems, among a multitude of other applications.

Leveraging existing technologies heavily, there is a very close and necessary marriage between unmanned systems and robotics, meaning the robotic paradigm of perception, processing and action is fully applied. This translates to a very high content of electronics being used not only in command and control of the unmanned systems, but also in: actuators; motors; sensors; vision systems; manipulation controllers; data acquisition cards; GPS systems; radar; LI-DAR; video capture and processing; and inertial guidance systems. This is just a small sampling.

The question posed by AUVSI in their event advertising headline read, "When the world of unmanned systems comes together, where will you be?"

This is a very fitting question for manufacturers of flexible circuits, flexible heaters, rigid-flex circuitry, and electronics contract manufacturers. The attributes of flex and rigid-flex circuit technologies uniquely mesh with the size, weight and power (SWaP) and electronics packaging requirements and challenges of the unmanned systems and robotics industries:

> " *Leveraging existing technologies heavily, there is a very close and necessary marriage between unmanned systems and robotics, meaning the robotic paradigm of perception, processing and action is fully applied.* "

• Flexible circuits and rigid-flex circuits allow unique designs which solve interconnect challenges
• The ability to fold and form flex and rigid-flex circuits enables a package size reduction
• Flex and rigid-flex circuits make installation and repair both practical and cost effective
• The number of levels of interconnection required in an electronics package is greatly reduced by utilizing flexible circuits and/or rigid-flex circuits
• A considerable weight reduction is achieved over wire harnesses and rigid circuit assemblies

• Flexible circuits dissipate heat at a better rate than any other dielectric materials
• The reduction in connectors and solder joints lowers costs and flexible circuits can be tested prior to assembly of components

The market potential for flex and rigid-flex circuit manufacturers to provide their products and services to the unmanned systems and robotics market was clearly noted by flex circuit and rigid-flex circuit industry leaders at the event, including: All Flex, Cirexx International, Eltek USA, PFC Flexible Circuits and Printed Circuits Inc. (PCI). All had a major presence at the event. Many of the event attendees were not familiar with flex and rigid-flex circuit technology, so there was a very steady stream of engineers asking detailed questions about the technology and expressing excitement at both the application potential and the extreme packaging configurations that could be attained with flexible and rigid-flex circuitry. (Note: Circuit Solutions, LLC. represents All Flex and PCI in the Washington Military Market.)

Equally impressive from my viewpoint is that the unmanned systems market is both invigorated and vibrant with youthful enthusiasm and entrepreneurship. I have been in the printed circuit board industry for more than 30 years and witnessed the decimation of the industry first-hand as U.S. shop after U.S shop closed due to the offshoring of electronics manufacturing. This has all been well documented and I believe the cause and effect is well understood at this point. What is less well recognized is that with the offshoring of manufacturing (and subsequently much of the R&D), coupled with the closures, our industry has lost at least an entire generation of technologists, product development and new domestic manufacturing opportunities. Manufacturing

lost both opportunity and its cool factor with our youth.

Helping to get the cool factor back into the equation, The AUVSI Foundation Student Competition Pavilion showcased student teams who compete in the Foundation's autonomous robotic competitions, including the International Aerial Robotics Competition (IARC), International Ground Vehicle Competition (IGVC), RoboBoat Competition, RoboSub competition, and the Student Unmanned Air Systems Competition (SUAS). This was a very high energy area and the technologies being developed and integrated by the student teams provided a further glimpse into the future of unmanned systems product development.

The pavilion also hosted a live demonstration of SeaPerch, the AUVSI Foundation's Science, Technology, Engineering and Math (STEM) outreach program for middle and high school students. Sponsored by the Office of Naval Research and managed by the AUVSI Foundation, the SeaPerch Underwater Remote Operated Vehicle Program is a fun and educational toolset for stimulating young minds about STEM through hands-on activities. Including a standard build curriculum for the vehicle and all necessary parts to fabricate the ROV, small underwater cameras and sensor suites may be integrated to capture video, measure and report underwater.

One perfect example of the potential resurgence in product development and manufacturing that exists in the unmanned systems market is embodied in three young men from North Carolina whom I met at AUVSI. Their company is Bird Aerospace and their product is the "Bird's Eye." Trevor Vita, 23; Matthew Most, 23; and the old man of the group, David Sanders, 24; have been friends since middle school. After high school, Vita and Sanders graduated from the University of California, Santa Barbara, with respective degrees in environmental science and software engineering. Most graduated from the University of California Los Angeles with a degree in mechanical engineering. These are bright young men with many career options. They are also young men who had an early interest in electronics and spent many hours as hobbyists tinkering with remote con-

Figure 1: Bird's Eye launch.

Figure 2: Bird's Eye unmanned aerial system.

trol aircraft, constructing and deconstructing the crafts and their electronics, and like most young men of the era, at the joystick controls of PlayStation and X-Box.

Their background, education and entrepreneurial spirit create the perfect storm for prod-uct development in the unmanned systems arena. After college, they also spent a combined seven years working hands-on in the military unmanned aerial systems (UAS) industry and realized that the existing systems were cumber-some to launch, difficult to maintain and in-
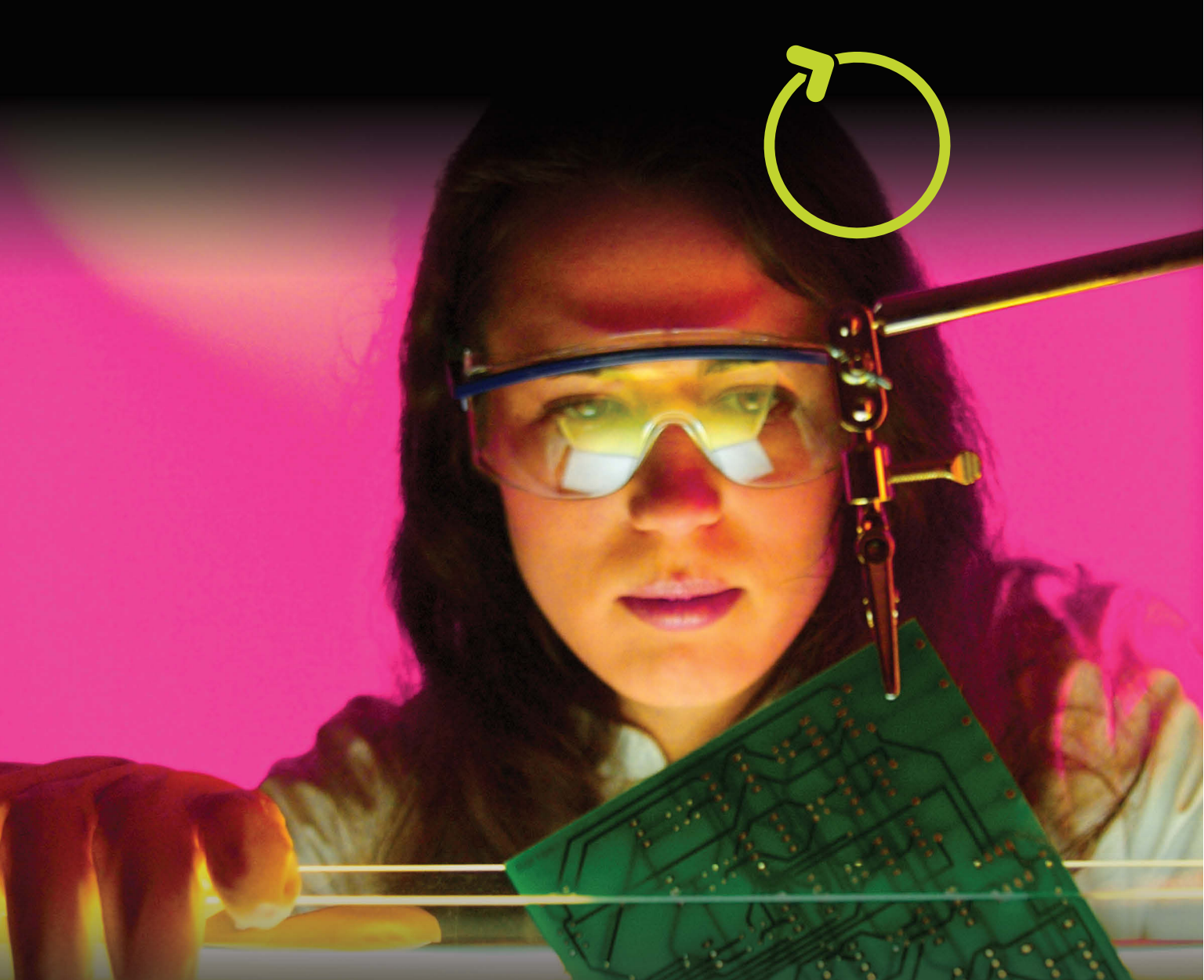
WHEREVER THE NEXT DESIGN CHALLENGE TAKES YOU, OUR LIGHT CURE TECHNOLOGY IS ALREADY THERE.

The Electronics Market continues to evolve at a faster rate than ever before. Today's complex designs, innovative materials, and increased focus on the environment can present challenges to manufacturers. Whatever demands you face, Dymax has you covered. From conformal coatings to encapsulants to edge bonding materials, we provide solvent-free, light curing technology that's truly game changing. Cost-reducing solutions that turn problems like shadowed areas, cure confirmation, and production throughput into non-issues. And, they're backed by the Dymax Edge… an integrated offering of oligomers, customized adhesives and coatings, cure and dispense equipment, and application expertise that enables Dymax to deliver the best solution to the customer. **Visit dymax.com/electronics**.

877-396-2988

DYMAX®

DYMAX.COM

THE INTERSECTION OF UNMANNED VEHICLE SYSTEMS AND ELECTRONICS TECHNOLOGY *continues*

sanely expensive. They set out to change all of that.

Their Bird's Eye UAS (Figure 1) is a revolutionary system that potentially puts very powerful technology into anyone's hands at an affordable cost. A, lightweight carbon fiber canister 12" in diameter and 2' in length houses the entire system. The Bird's Eye features a OneTouch deployment system which activates a small pyrotechnic charge that lifts the system to an altitude of 200–300 feet, where the canister splits in half and a 56" wing unfolds locking into a rigid airframe. Autonomously flowing, the operator simply uses a map/terrain overlay on a tablet or laptop to direct the aircraft on its mission. The total deployment time is 30 seconds and the operator needs only a clear view to the sky to launch. The Bird's Eye is deployable anywhere: forest, urban environment, at sea, from the air, from the desert, from high elevation and uneven terrain. With a set-up and deployment time of less than 30 seconds and a top speed of 120 mph, the Bird's Eye is potentially on the scene faster than any other small UAV to-date. Bird Aerospace's initial target markets are search and rescue operations, border patrol surveillance, agricultural surveys, forest fire management, polar ice research/reconnaissance.

As with any emerging industry there are regulatory challenges. Setting aside the privacy issue for now, the UAS industry's key challenge is the integration of UAS technology into the National Airspace System (NAS). The Federal Aviation Administration (FAA) was tasked with solving this challenge in 2012.

To better understand the regulatory challenges, the timing, the wide variety of unmanned systems applications, the markets and the economic impact of UAS, I would suggest

> *"The total deployment time is 30 seconds and the operator needs only a clear view to the sky to launch. The Bird's Eye is deployable anywhere: forest, urban environment, at sea, from the air, from the desert, from high elevation and uneven terrain."*

downloading the AUVSI's March 2013 report, titled The Economic Impact of Unmanned Aircraft Systems Integration in the United States.

Clearly, the unmanned systems and robotics market provides an excellent business opportunity for manufacturers of flexible circuits, rigid-flex circuitry and electronic contract manufacturers for the foreseeable future. There is already wide-scale adoption of some of the unmanned ground and sea systems and the robotics. As regards the integration of the UASs into the NAS, the issue is not whether these products will be adopted, but simply at what rates they will be adopted.

Just as importantly, as the care holders of the industry that has perfected these amazing circuit fabrication technologies, we have an outstanding opportunity and a responsibility to both guide and contribute to its rapid growth. Through sharing our acquired knowledge with the new generation of technologists that is evolving in concert with the development of many of the unmanned platforms, we can provide interconnect and packaging solutions, provide a manufacturing knowledge base, grow our own businesses, and most importantly, support job growth and economic growth in the USA. **PCBDESIGN**

John Vaughan is president of Circuit Solutions LLC., based in the Washington D.C. metro military market and provider of integrated supply chain and program management solutions to the military C4ISR, Unmanned Systems and IED detect and defeat communities. Vaughan may be reached at john@circuit-solutions.com.

GET YOUR PRODUCTS TO MARKET FASTER

When it comes to looking for a competitive advantage,
your PCB design strategy can ultimately prove to be your secret weapon
as you move into an uncertain future.

*Are you providing your design teams
with access to the right technology to make that happen?*

Do you know the six keys to PCB excellence? FIND OUT NOW!

Speed time-to-market today

with the PCB technology of tomorrow

LET US SHOW YOU HOW

VIRTUAL PROTOTYPING

DESIGN FLOW CONCURRENCY

DESIGN THROUGH MANUFACTURING

Follow us

BEYOND DESIGN

· ·

PDN Planning and Capacitor Selection, Part 1

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD | AUSTRALIA

In my first column on power distribution network (PDN) planning, Beyond Design: Power Distribution Network Planning, I described the basics of planning for low AC impedance between the planes, in order to reduce supply noise and provide reliable performance. I recommend that you read that column first to get the required background knowledge.

This column will focus on capacitor selection and three alternative approaches to analyzing the PDN:

1. Target frequency
2. One value capacitor per decade
3. Optimized value capacitor

Traditionally, the target frequency approach has been used. This method targets a precise frequency and is used to reduce AC impedance and can also be used to reduce EMI within a specific band. The alternatives of using either one value capacitor per decade or many opti-

mized capacitors, is an attempt to level out the AC impedance, at the desired impedance, over a broad frequency band.

The latest high-performance processors, with sub-nanosecond switching times, use low DC voltages with high transient currents and high clock frequencies to minimize the power consumption and hence, heat dissipated. Fast rise times, low output buffer impedance and the simultaneous switching of busses create high transient currents in the power and ground planes degrading performance and reliability of the product.

Poor PDN design can result in unusual, intermittent signal integrity issues including high crosstalk and excessive emission of radiation. It can be extremely difficult to track down the cause of such issues, so my recommendation is to plan the PDN design prior to place and route in a pre-layout analysis of the design.

The integrity of the PCB stackup and the PDN are the basis for a stable product. Multi-
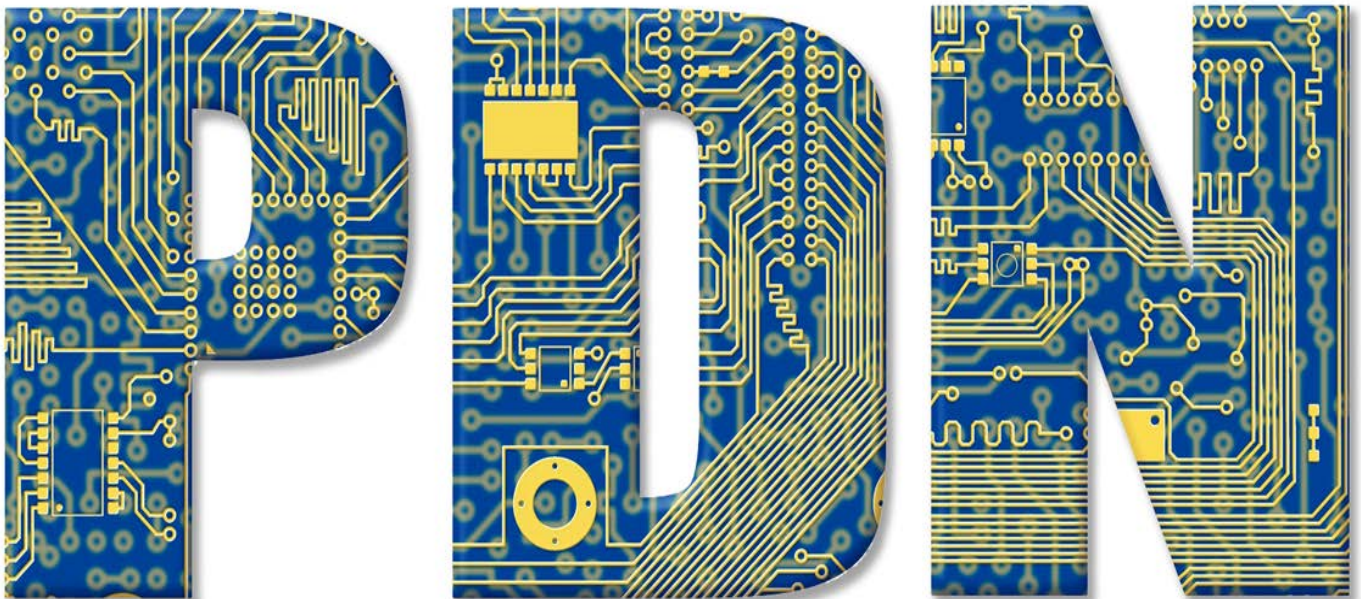
We are Commited to Delivering Outstanding Quality and Service, On-Time.

AND OUR CUSTOMERS AGREE!

Dear Prototron Team

Thanks for your continued performance and quality!! We have had 35 engineering designs fabricated by Prototron since 2012 and we are very happy. Your personal contact, knowledgeable staff and commitment to on time delivery continues to allow us to meet our commitments to our customers. Prototron's engineering department has been extremely helpful on recommending improvements to new PCB designs. You guys are great!!

Thanks,

Fred Sievert
Aeroflex Colorado Springs

Click to Learn More

Prototron Circuits
Quality printed circuit boards

America's *FASTEST* Board Shop
www.prototron.com

PDN PLANNING AND CAPACITOR SELECTION, PART 1 *continues*

layer PCB design is becoming more complex and less forgiving—it's not just about signal integrity, crosstalk and EMI. The substrate and the power delivery system are extremely critical and if they should fail then the whole system can go down or worse case, may just work intermittently.

Choosing the Right Capacitors

Many application notes say all we need to do is add three capacitors per power pin. Some recommend using three different values; others say they should all be the same value. But which is right, or are they both wrong? Decoupling is not the process of placing a capacitor adjacent to the IC power pin, but rather it is the process of placing an L-C network adjacent to the IC to supply the high transient switching current. The inductance comes from the capacitor itself, the lands, the interconnecting traces and vias and the lead frame of the IC—collectively—the loop inductance. It is this inductance that limits the effectiveness of the decoupling network.

Decoupling capacitors supply instantaneous current, at different frequencies, to the drivers until the power supply can respond. In other words, it takes a finite time for current to flow from the power supply circuit, whether onboard or remote, due to the inductance of the traces and/or leads to the drivers. Each capacitor added to the board lowers the impedance of the PDN at a particular frequency. Bulk bypass capacitance—typically provided by tantalum capacitors—provide low impedance up to 10MHz. High-frequency decoupling is provid-

ed by ceramic capacitors up to several 100MHz. Above 200MHz, high-quality, low-inductance capacitance is necessary to support the very fast switching transients associated with driving single ended transmission lines and rapidly-changing IC core-supply currents. This is provided by the on-die capacitors or capacitance formed by adjacent power and ground layers.

For bulk decoupling at the supply level, tantalum is usually preferred, due to the availability of high capacitance ratings. At the IC level, and sometimes at the power supply, ceramic may be preferred due to its low equivalent series resistance (ESR) and excellent high frequency response. Design characteristics of the ceramic also allow low-inductance designs that reduce noise generated at the initial di/dt energy transfers.

Large capacitance value ceramics provide effective decoupling at about 25% of the nominal capacitance value compared to standard tantalums. This is because the capacitance of the ceramic is more stable with increasing frequency, while that of the tantalum and aluminum electrolytics tend to roll off, making them respond as much smaller capacitance values than the nominal rating. In addition, the lower ESR of the ceramics reduces the total capacitance required to maintain the desired voltage. Ceramics range in capacitance from 12pF to ~10uF.

New types of polymer tantalum and aluminum capacitors also have better capacitance stability and lower ESR than do older types, which permit the user to substitute lower nominal capacitance values in the circuits. There are

Tantalum	
Capacitance (high)	0.1uF – 680uF
SRF (low)	127KHz – 12MHz
Voltage (low)	3V – 50V

Ceramic	
Capacitance (low)	0.75pF – 100uF
SRF (high)	490KHz – 8.3GHz
Voltage (high)	5V – 200V

Figure 1: Examples of tantalum and ceramic capacitors.

Material	Dielectric Constant	% Capacitance Change	Df %
NP0	15–100	< 0.4	0.1
X7R	2,000–4,000	+/- 15	3.5
Y5V	> 16,000	< 82	9

Table 1: Critical specifications of MLCCs.

also applications where the bulk capacitance requirements are so high that the volumetric efficiency of the tantalum makes it the preferred type.

Over the years, capacitor sizes have shrunk dramatically. Multilayer ceramic capacitors (MLCCs) are the most commonly used decoupling capacitors for high-speed design as they are small and have relatively high capacitance values for their size. MLCCs are produced from alternating layers of ceramic and metal to produce a multilayer capacitor.

The capacitance value of a capacitor is determined by three factors: the number of layers in the part, the dielectric constant, and the active area. The dielectric constant is determined by the ceramic material (NP0, X7R, X5R, or Y5V). The active area is the overlap between two opposing electrodes.

The dielectric thickness is inversely related to the capacitance value, so the thicker the dielectric, the lower the capacitance value. This also determines the voltage rating of the part, with the thicker dielectric having a higher voltage rating that the thinner one. This is why the basic trade-off in MLCCs is between voltage and capacitance.

The rating compared to working voltage for MLCCs is 2:1. This means that, for a rail voltage of 1.8V as used for DDR2, the voltage rating needs to be 3.6V. So a standard 6.3V capacitor can be used with most processors.

The dielectric constant depends on the ceramic material used. Table 1 shows different dielectrics and some of their specifications. As you can see, NP0 has the lowest dielectric constant, followed by X7R which has a significantly higher constant, and Y5V which is higher still. This is why the capacitance values for X7R capacitors are much higher than NP0 capacitors, and Y5V has higher capacitance than X7R. The capacitance change vs. temperature is very small for NP0 parts from -55°C–125°C, and gets larger for X7R, then even larger for Y5V. So the more capacitance a material provides, the lower the stability of capacitance over temperature.

Dissipation factor (Df) is the percentage of energy radiated as heat in the capacitor. As you
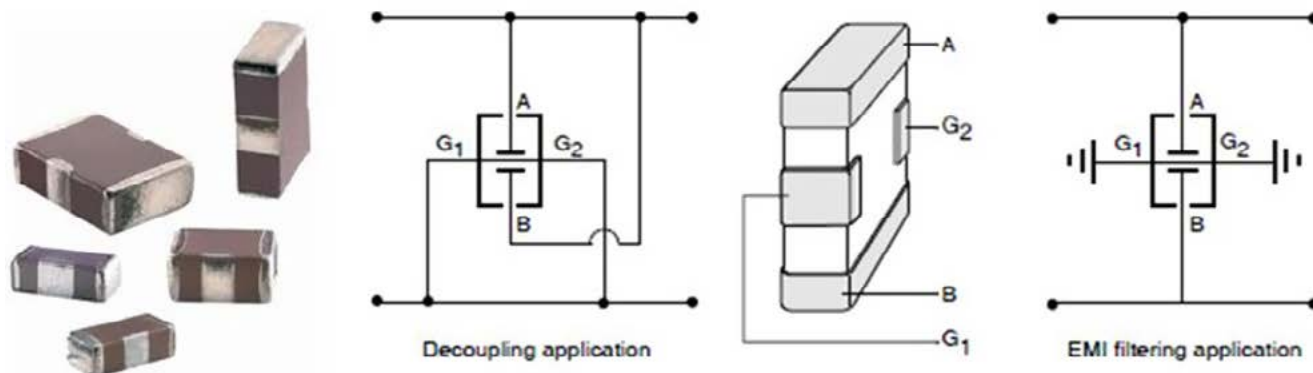

Figure 2: X2Y capacitor and equivalent circuit. (courtesy Yageo)

can see, NP0 material is very efficient, followed by X7R, then Y5V which is the least efficient of the three materials.

The capacitance of all ceramic capacitors changes with temperature, voltage, frequency and over time. C0G (aka NP0) capacitors are very stable and are manufactured in sizes up to 10nF, while X7R capacitors are less stable, and manufactured in sizes up to 1uF. A third common type is Z5U, which is of very low grade, and not recommended.

Another type of MLCC is the X2Y series. They are comprised of two identical Y-capacitors and one X-capacitor, integrated into a four-terminal device, and are available in standard MLCC sizes (0603, 0805, 1206, etc.).

X2Y filter capacitors employ a low inductance design featuring two balanced capacitors that are immune to temperature, voltage and aging performance differences. These components offer superior decoupling and EMI filtering performance and virtually eliminate parasitics. When used in EMI filtering configuration, the X2Y capacitor is connected across two signal lines. Differential-mode noise is filtered to ground by the two Y capacitors, A and B. Common-mode noise is cancelled within the device. A and B capacitors are placed in parallel, in the decoupling application, effectively doubling the capacitance while maintaining an ultra-low inductance. While X2Y MLCCs offer superior performance and are better space-wise (four X2Ys are equivalent in size to six 0402s), they are about five times the price of a standard 0402.

Tantalum capacitors that lower the impedance at the low-frequency end of the scale are less critical. Tantalums come in larger packages, from the 0805 and 1206 region to 2917, and they range from 0.1 to 680uF. Obviously, it is best to choose a low ESR and low equivalent series inductance (ESL) for the same capacitance value.

A capacitor's equivalent circuit is basically a series capacitor,

resistor and inductor. These are referred to as the capacitance value, ESR and ESL respectively. Generally, the ESR and ESL are not listed in datasheets but rather are extracted by a SPICE simulator. This is because the ESL of the capacitor is rather meaningless as the bulk of the inductance is attributed to the loop inductance due to mounting the capacitor. The capacitor's self-resonant frequency (SRF) can be calculated by:

$$SRF = \frac{1}{2\pi\sqrt{LC}}$$

Looking at Figure 3, we can see that the downward slope of the capacitor is capacitive, then as the capacitor approaches its SRF it becomes resistive and as the frequency increases the inductance takes over raising the impedance again. So basically, the capacitor only has low impedance for a very small bandwidth about the resonant frequency—and high either side of this frequency band. But the goal of PDN planning is to make the AC impedance, of the entire PDN, look like a resistor, flat from zero to infinity, but in reality this does not happen.
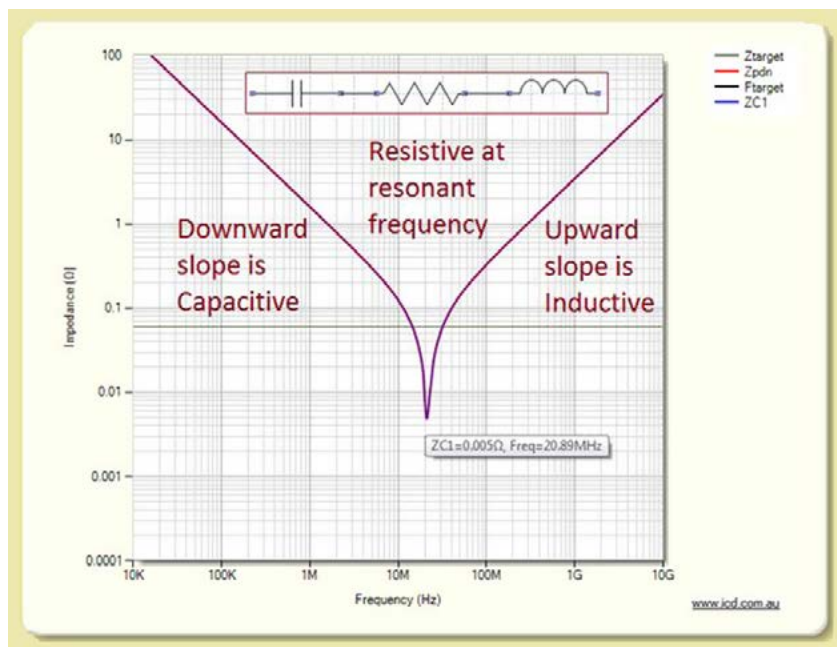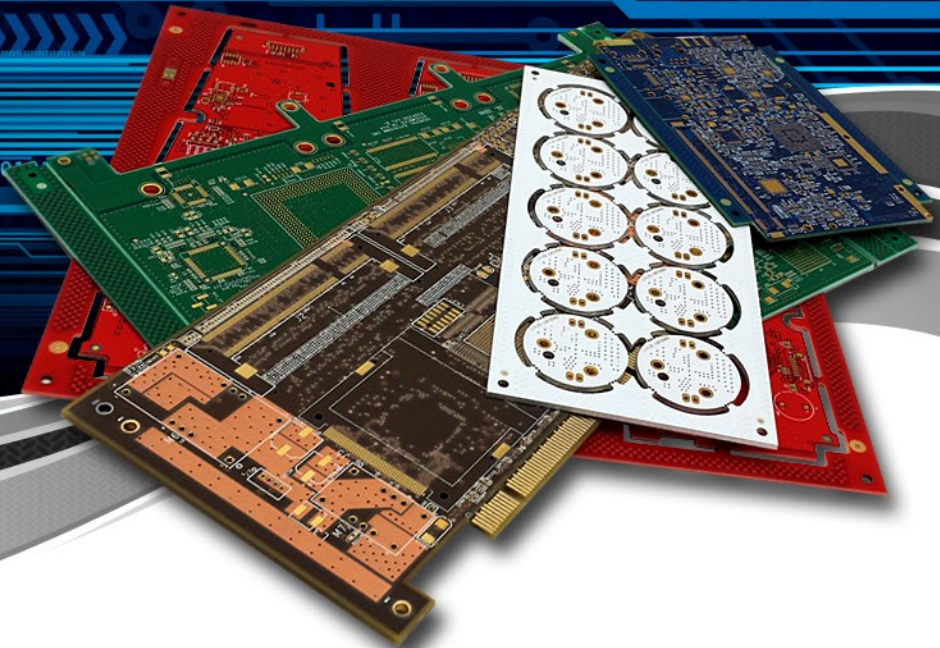

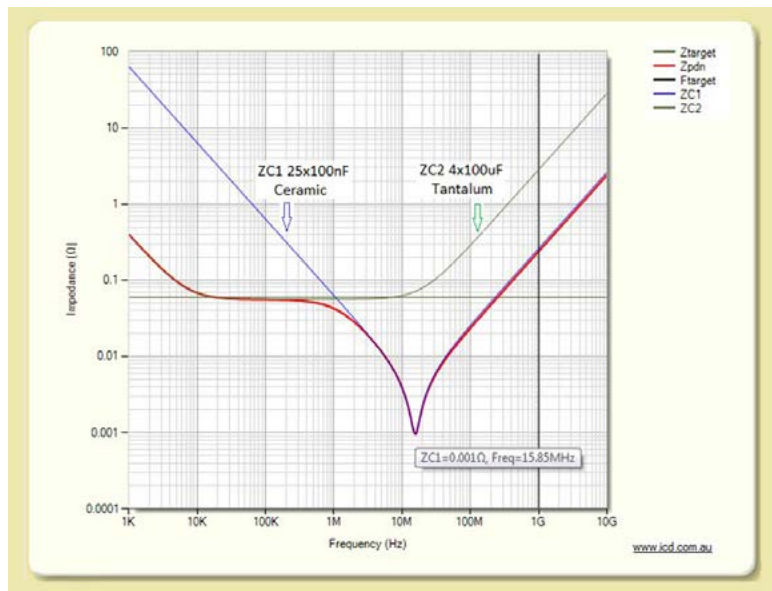Figure 3: A capacitor has series capacitance, resistance and inductance.

PDN PLANNING AND CAPACITOR SELECTION, PART 1 *continues*

Figure 4: The target frequency approach.

To meet the target (low) impedance at a particular frequency, a capacitance value is chosen so that when mounted on the PCB, it will resonate at the desired frequency, and have an impedance that is equal to its ESR. Then a sufficient number of those capacitors are placed in parallel so that the parallel ESRs approach the desired target impedance.

When N equal L-C networks are placed in parallel:

Total capacitance = N x C | Total Inductance = L/N

$$Z = \sqrt{\frac{L}{C}}$$

Both work in our favor, and for a fixed PDN inductance, the effectiveness is solely dependent on the number of capacitors (N).

• The more capacitors (N) the lower the total inductance, and the better the high-frequency decoupling
• Typical "N" values range from 4–25 decaps, though it varies by application
• When a large number of capacitors are used, their placement becomes less critical than

when only 1-2 caps are used—spread them out around the IC, and try to place them symmetrically (and evenly) with respect to the IC

In Figure 4, the ICD PDN planner, available from www.icd.com.au, illustrates 25 x 100nF 0402 ceramic and 4 x 100uF 1210 tantalum capacitors in parallel to achieve the desire target impedance from 20KHz to 250MHz for a particular PDN. But, the impedance increases rapidly at the top end above 250MHz. This may seem OK if you are using a clock frequency of 200MHz, for instance, but as mentioned in previous columns, the impedance needs to be low up to the 5th harmonic, which is 1GHz in this case.

In Part 2, we will continue looking at the alternate approaches of analyzing the PDN. **PCBDESIGN**

References
1. Barry Olney, Beyond Design: Power Distribution Network Planning and
2. Material Selection for SERDES Design
3. Henry Ott, Electromagnetic Compatibility Engineering
4. Istvan Novak, Quiet Power: Resonances in Power Planes
5. Eric Bogatin, Signal and Power Integrity - Simplified
6. Johanson Dielectrics, Basics of Ceramic Chip Capacitors
7. Kemet, SMT Capacitor Comparison
8. X2Y, Understanding capacitor inductance
9. The ICD PDN Planner is available at www.icd.com.au
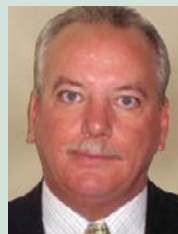
Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. ICD is a PCB design service bureau and specializing in board-level simulation. The company developed the ICD Stackup Planner and the ICD PDN Planner software. To read past columns or contact Olney, click here.

We Have a Better Way to Predict

PCB MANUFACTURING SUCCESS!

Your PCB Design is Ready to Go!

Netlist errors are quickly validated in DFMStream

DFMStream™

DFMStream provides powerful DFM capabilities in an easy-to-use tool suite designed to help engineers and designers verify design and manufacturing rules on PCB design databases, Gerber and NC data any time during the PCB design cycle. DFMStream bridges the gap between engineering and fabrication, helps save valuable time and reduces new product introduction bottle necks.

- Provides powerful DFM functionality
- Easy to learn, even for infrequent users
- Easy to implement as part of the everyday design flow
- Saves time and increases productivity

For more information visit downstreamtech.com or call 800-535-3226

Define DFM checks by area so components such as BGAs can be verified with unique rules different from rest of design

DownStream Technologies

Flex Design: Should You Do It Yourself?

Figure 1: What's the worst thing that could happen if you design your product badly?

by Tom Woznicki
FLEX CIRCUIT DESIGN COMPANY

SUMMARY: The urge to do it yourself is strong, whether fixing a faucet, cutting your kid's hair or designing a flex circuit. After all, how hard can it be? Here are four situations that might necessitate the skills of a dedicated flex designer.

Should you design your own flex circuits? I say, come on in—the water's warm! The more flex applications the better! The industry has an army of very sharp CAM operators that turn bad designs into something manufacturable. In most cases, they catch the things that could cause trouble down the road.

That said, recently I've worked with three companies that had real problems with flex cir-

cuit designs that they did themselves. Two were rigid-flex designs and the other was a dynamic flex; all three were flex applications that the customer had never tried before. The rigid-flex programs had unacceptable failures after first production runs. The dynamic flex application was a train wreck—it shut down production of a high-profile product.

This is just my opinion, and it's worth the price you're paying for it, but I'd like to propose four applications or situations where it might not be a good idea to do it yourself—especially if it's your first flex design or you have limited experience designing this type of flex. At the very least, get another set of eyes to review your design before having circuits built. Here are the four situations:

1. Dynamic Circuits

Does your flex circuit have to move as part of your product's function? Designing a dynamic circuit, especially a multilayer dynamic flex, is much trickier than a flex-to-install and also more prone to field failures. I have rarely seen enough life testing of prototypes to be statistically significant—sometimes these circuits can work fine at the prototype stage but have an unacceptable failure rate in production.

2. Rigid-flex

These circuits can be expensive to build. It's one thing to scrap out a single-layer ZIF connector flex, but if your large eight-layer rigid-flex fails and you have to pay for another batch of expedited prototypes, it will cost you plenty.

3. An Adventurous Purchasing Department

Does your purchasing department often pick vendors you've never heard of from faraway places? Let's face it: In today's economy, every board shop's webpage proclaims, "We can build flex circuits!" So your purchasing folks may be tempted by very low pricing. In this case, you need complete data and very detailed fab drawings down to a gnat's eyebrow to make sure the flex is built properly. Anything unspecified will be done in a way that is easiest for the vendor. For example, the material stocked on the shelf might not be the best for your application. A corollary issue: After prototyping, will the whole project be given to a contract manufacturer in Asia? The flex could be redesigned and by someone with no experience with flex circuits. If the flex circuit is a critical part of your product the design needs to be bulletproof and very well documented.
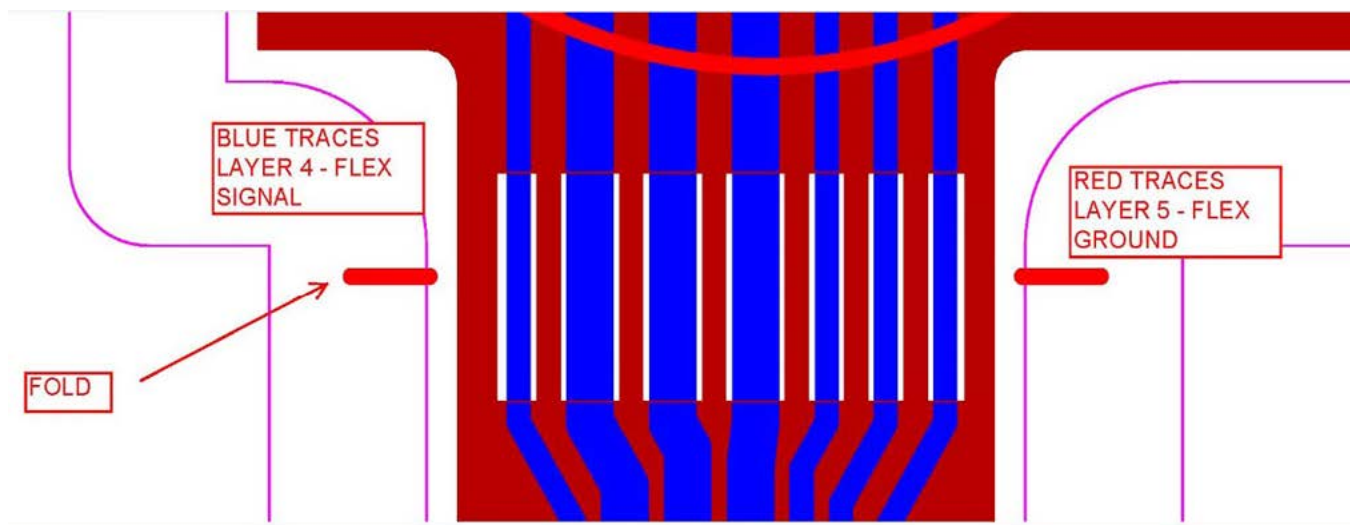

Figure 2: Tight folding areas can be tricky for novice flex designers. It may be best to get help for advanced flex circuits.

4. A Tight Time Schedule

Is there time for a two-putt? Unfortunately, flex circuits are often the last thing designed in a product and they have to take care of every leftover design issue. More than once I've heard "Don't worry; it's only for prototypes" lead to a crisis in production when the product ramped and the flex design was never revisited for DFM. If your schedule is tight, especially if it's expedited, the design package has to be like making instant soup—pour in the water and it's ready. If your data isn't ready to go to the floor and the salesperson and/or CAM guy needs to ask you questions, it chews into lead time.

Let me give you a closer look at one of the rigid-flex projects I referenced earlier: an eight-layer rigid-flex circuit with several tight folds. It was the company's first product with a rigid-flex circuit and they were blessed with an adventurous purchasing department. Purchasing found a small board shop in California that said they could do rigid-flex, and they gave them the order.

Turns out the fab drawing didn't specify rolled-annealed copper, so the vendor used flex base material with cheaper ED copper. Unfortunately, the tightest fold had the signal traces on the outside of the fold and a solid ground plane on the inside so when they folded the rigid-flex the signal traces naturally cracked.

I recommended specifying rolled-annealed copper in the next revision and modifying the ground plane to reduce the stress on the signal traces in the tight folding area (Figure 2). These two very small details made a huge difference. The second batch of protos had no cracked traces after installation!

Flex circuit design rules are not rocket science; just lots of little dos and don'ts that add up to a reliable circuit with good yields. This doesn't mean you can't bend some rules and get

Figure 3: A second set of eyes can pull your flex project back from the edge and onto the right track.

a flex circuit that works. They're kinda like wearing seat belts. Many times, you can get to where you're going without them, but sometimes you get an expensive ticket or worse.

So, if you have a two-layer flex-to-install application, there is time in the schedule and you want to give flex design a try, great. But if it's a dynamic flex or rigid-flex circuit and you're on a tight schedule with an adventurous buyer, perhaps it's not the right time to try it yourself. At the very least get someone with flex experience to review the design before you release the order. It will be cheap insurance! **PCBDESIGN**

Tom Woznicki is the president of Flex Circuit Design Co., a consulting company in San Jose, California. The company specializes in designing flexible printed circuits for OEMs and flex circuit manufacturers. Visit www.flexdude.com.

Mil/Aero007 News Highlights

Issues Continue to Plague RoHS Revision

Last week, IPC attended the EU Commission's final stakeholder meeting on the revision of the hazardous substance list under the EU RoHS Directive. As a result of the lack of consensus, the Commission will set up a working group to refine the methodology proposed to identify and assess the substances for potential restriction in electrical and electronic equipment.

Calumet Earns Zero Non-conformance Nadcap Certification

The certification recognizes the company's world-class capabilities and focus on meeting the highest levels of quality assurance for products developed for the aerospace industry. Of the 290 PCB manufacturers in North America, Calumet Electronics is one of only 16 companies to meet the stringent requirements for Nadcap accreditation.

Murrietta Earns MIL-PRF-50884 for Flex & Rigid-flex PCBs

Albert Murrietta, COO and co-owner, announces that his company has achieved full qualification for military flex and rigid-flex boards by achieving certification to the MIL-PRF-50884 standard. The company is now one of a few in the nation offering a full turnkey solution, from design through final assembly, for military-certified PCBs of all types.

Global Man-Portable Military Electronics Market 2013 - 2023

This report is the result of SDI's extensive market and company research covering the global man-portable military electronics industry. It provides detailed analysis of both historic and forecast global industry values, factors influencing demand, the challenges faced by industry participants, analysis of the leading companies in the industry, and key news.

Viasystems' Shanghai Facility Earns AS9100 Certification

"The AS9100 certification is evidence of our commitment to ensure that our quality and manufacturing systems are equipped to provide the high-quality products demanded by our customers," said David M. Sindelar, CEO.

Stress is the Culprit in Tin Whisker Growth

"We're convinced it's got to be stress from the intermetallics that causes them to form," said Eric Chason, professor of engineering at Brown University. "When you put tin on copper, there's a reaction when copper is shoved into the tin, which causes whiskers to pop out."

Robotics Industry Set for Strong Growth

"The robotics industry is looking into a bright future," stated Dr. Shinsuke Sakakibara, IFR president, on the occasion of the publication of the study World Robotics 2013: Industrial Robots. "In 2013, global robot sales will increase by about 2% to 162,000 units.

3D Printing: The New Frontier?

3D printing is ready to revolutionize space travel. ESA is paving the way for 3D-printed metals to build high-quality, intricate shapes with massive cost savings.

Next-Generation Robotics Program Secures $38M in Funds

The National Science Foundation, in partnership with the National Institutes of Health, U.S. Department of Agriculture, and NASA, has announced new investments totaling approximately $38 million for the development and use of robots that cooperatively work with people to enhance individual human capabilities, performance, and safety.

Global Markets for Satellite Technology

Satellites are self-driven objects or vehicles placed in predefined orbits around the earth for communication and monitoring purposes. This report identifies and forecasts the potential for telecommunication components, modules, and devices in satellite technologies.
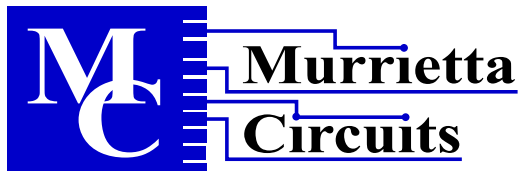
Rooting out the Root Cause

by Martyn Gaudion
POLAR INSTRUMENTS, LTD.

When your measured trace impedance is significantly different from the calculated/modeled trace impedance, be careful before jumping to conclusions.

Sometimes, your intuition can lead you astray—especially when analysing engineering problems. This makes it worth taking a step back to consider possible alternatives. Maybe, as my colleague Neil Chamberlain puts it, "That came from left field!"

I'll set the scene for this month's column topic with a non-electronics experience of my own. Polar Instruments is based on a small island with tiny roads lined with unforgiving stone walls that make driving an interesting challenge. Because I need to take equipment to shows and visit customers occasionally, I use a minivan for my commute—despite its unsuitability in local traffic. Recently, my wife persuaded me to look for an alternate vehicle—something that is small, economical, reliable, and practical. After several weekends of hunting the new and used car lots, we came to the conclusion that although there were plenty of possibilities, nothing had leapt out and said "Buy me!"

The cars we were seeing only fulfilled one of the criteria each. Being an engineer at heart I suggested to my wife that we replace "and" with "or" and run the math again in our heads: small or economical or reliable or practical. With an "or" function, only one criteria has to be true for a "Yes!" outcome. We found that car, and I asked my wife, "Shall I buy it?" She replied, "I am not saying yes and I am not saying no," which I took as a maybe, and I bought it for myself on impulse. It didn't really help that it happened to be her birthday, but it was pure coincidence; and I wasn't going to lose the car to another buyer.

Again, my wife gently reminded me that the last time I bought a 10-year old car on impulse it ended badly with a burst transmission intercooler filling the gearbox with rusty water at 3 a.m. with two young children asleep in the car in the middle of nowhere. "Lightning doesn't strike twice," said my internal logic. Needless to say, when I arrived at the office with my new toy I suffered endless "mid-life crisis" and "hairdresser's car" jokes, but it seemed like a good investment to me.

ROOTING OUT THE ROOT CAUSE *continues*

When the next day dawned, a cold spring morning, I sparked up my new investment, only to see a plume of white smoke from just one exhaust in the rear view mirror. My heart sank. After all, the dealer had been honest with me and said the previous owner was only selling the car because of the horrendous repair bills. I started to run through the possible (expensive) consequences…

In Asia, I often field questions from customers and prospective customers who say things like, "My impedance model doesn't match my measurement!" They are often armed with one or two powerful, accurate field solvers plus a measurement system that the vendor specifies as giving traceable results, calibrated against national standards. Why, oh why, is the calculated trace impedance significantly different from the measured one? Something must be wrong! The answer is, maybe and maybe not. If the contact is convinced that measurement and modeling tools are both trustworthy, then the finger of suspicion points at the dielectric constant—even though logic says that impedance only varies as the root of ε_r so it really is only a second-order effect. Often, it is assumed that because of the cost and the traceable capability of the measurement system, the measurement must be correct and the error lies elsewhere. A little thought from left field might be worth pausing for here, before putting too much blame on our old friend ε_r. Most impedance controlled PCB specs assume lossless traces, and even if the trace is only specified at moderate speeds long before dielectric loss comes into play, another factor has crept in, primarily driven by the reducing geometries being used and thinner boards and/or more layers in a given overall thickness; the result of this is that the DC resistance of the PCB trace, which could reasonably be ignored with the geometries and copper weights in use five to ten years ago, has crept up on us and is interfering with the measurement of instantaneous impedance.

It is quite possible that the impedance trace has developed a significant upward slope, and when the average impedance is taken after the initial aberrations have been allowed to settle, the impedance reading is composed of the instantaneous impedance, plus a slug of DC resis-

tance. (Hint: Design the coupon with probe access at both ends and measure the DC resistance with a precision meter and you will get an idea of how much resistance per inch is being added as an error component on top of the instantaneous impedance; on differential traces the value is doubled.) At Polar we notice this—especially on flex coupons. Some board shops have got into the habit of measuring the impedance, ignoring the DC resistance component, and then sectioning the sample and using a solver to "goal seek" for ε_r. While ε_r may be a partial contributor, it could be a fallacy to blame ε_r for all observed mismatches, which takes me back to the original story. Here, ε_r may be innocent but because it is relatively hard to measure it is used as a convenient adjustment factor to null out measured and modeled accuracy. If you are doing this it might be worth taking a casual look at the DC trace resistance before you draw an incorrect or partially incorrect conclusion.

So the smoke coming from one exhaust? Was it a head gasket on one bank of cylinders? Here comes the repair bill my wife cautioned me about…or maybe not, upon closer inspection. When cold, a valve seals off the right-hand exhaust to allow the catalyst to reach operating temperature, but also, under the close supervision of the engine management system, opens in spirited driving, but shuts off in traffic to meet noise regulations. Just as well, I looked a bit deeper before deploying the tool box to fix something that was never to blame in the first place. **PCBDESIGN**

References
1. Polar app note AP156
2. Istvan Novak, Senior Principle Engineer at Oracle, et al. "Determining PCB Trace Impedance by TDR: Challenges and Possible Solutions," DesignCon 2013.
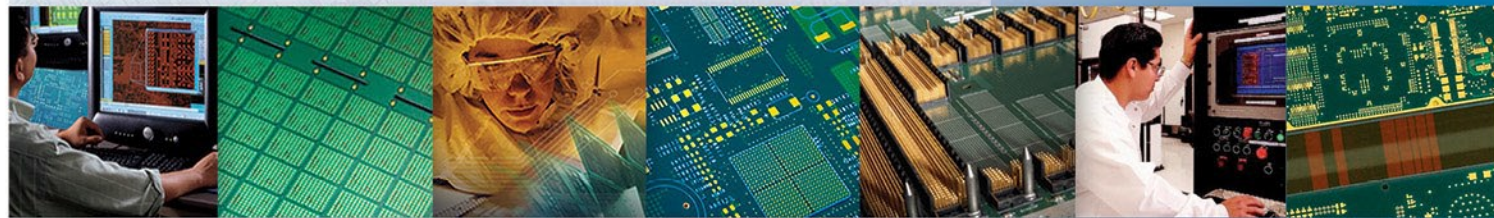
Martyn Gaudion is CEO of Polar Instruments Ltd., and a regular participant in IPC high-speed, high-frequency standards development activities. To read past columns, or to contact Gaudion, click here.

A Few Notes about TDR

by Amit Bahl
SIERRA CIRCUITS

I recently called Ken Taylor, the president of US operations for Polar Instruments, with a question from a customer about a time-domain reflectometer my company uses for impedance tests. Not only was the conversation very helpful, but almost immediately after we spoke, Ken sent me a detailed e-mail, and then a second e-mail, that are well worth repeating. So, with his kind permission, here is Ken's brief but educational lesson on TDR.

From Ken Taylor:

"Let me follow up with a few notes about your customer's question, 'What is the rise time of Polar's TDR?' It is a common question based mostly on misunderstanding. From the question, one may infer that the customer wants to know what will be the impedance at a certain frequency. Here's some background.

The TDR is a time domain reflectometer. It does not operate in the frequency domain. The high-frequency harmonics present in a pulse are mainly evident in the speed of the rising (or falling) edge. However, impedance is measured on the flat top of the pulse, not on an edge measurement.

So, what is the relevance of the edge speed? Edge speed does determine measurement reso-lution: i.e., a fast edge will reveal a short discontinuity; slower edges can see only longer discontinuities. Yet, because fast edges do respond to short discontinuities, they react greatly to the discontinuity of the probe tip, the signal injection pads and vias, and the discontinuity (typically) of the test trace at the injection point – for example, where a differential pair spreads out to reach the probe pads. This results in waveform aberrations that will typically mask or distort the test region of the measurement waveform.

For a frequency test, you must use a frequency-domain tester, e.g., a VNA, which will sweep a sine wave through a range of frequencies and thus make tests at specific frequencies. This is usually to ascertain signal loss at those frequencies. Board fabs typically don't use a VNA because of all the disadvantages. Namely, the front end is delicate and easily damaged; it requires manual intervention by a skilled operator; results vary from one user to the next; and the time involved is usually seconds to minutes. A TDR, on the other hand, can be made robust, used by an unskilled operator, measures and computes in a fraction of a second, gives repeatable results from one user to the next, and test parameters can be easily programmed and don't require user intervention.

APEX EXPO® IPC

CONFERENCE & EXHIBITION › March 25-27, 2014
MEETINGS & EDUCATION › March 23-27, 2014

MANDALAY BAY RESORT AND CONVENTION CENTER
LAS VEGAS, NEVADA

WWW.IPCAPEXEXPO.ORG

Design-Focused Education
March 21–24, 2014

NEW IDEAS...FOR NEW HORIZONS

› **DESIGN FORUM** — Educational program featuring presentations by experts in design

› **PROFESSIONAL DEVELOPMENT COURSES** — Three-hour classes led by subject-matter experts

› **DESIGNER CERTIFICATION PROGRAM** — Basic (CID) and advanced (CID+)

› **EXHIBITION** — More than 400 exhibitors displaying technology equipment and products.

For more information on design-focused programs,
visit WWW.IPCAPEXEXPO.ORG/DESIGN.

DESIGN | PRINTED BOARDS | ELECTRONICS ASSEMBLY | TEST

A FEW NOTES ABOUT TDR *continues*
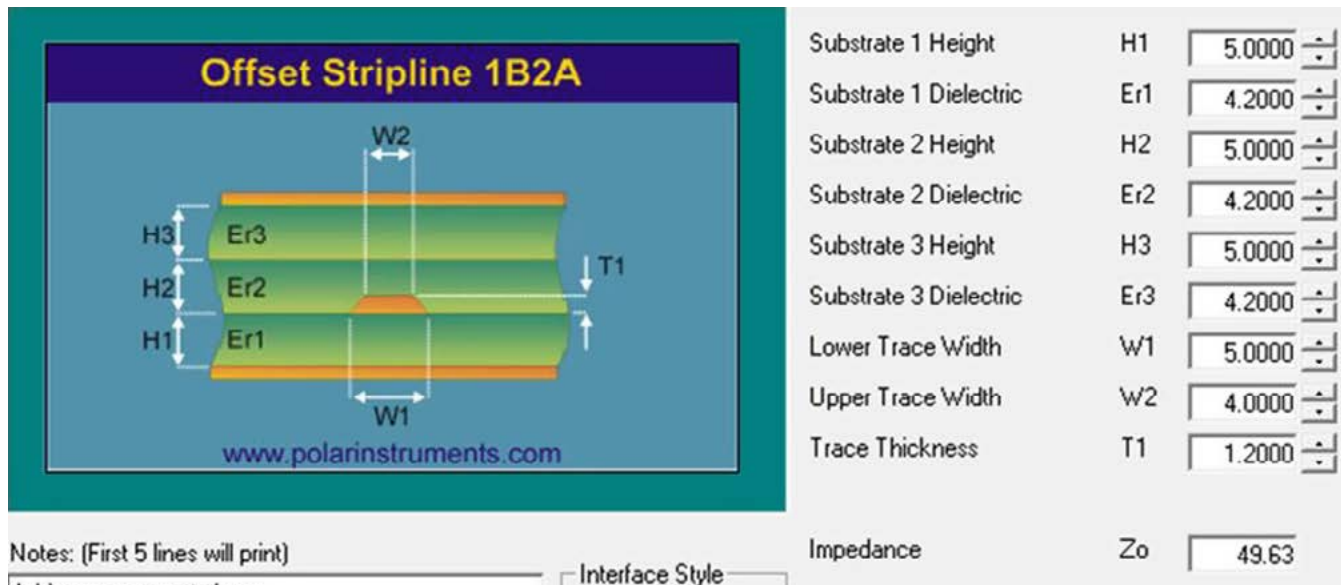
Figure 1: A single-ended, offset, 50-ohm dual stripline.

Eric Bogatin, during his days as CTO at Gigatest Labs, compared Polar TDR and VNA measurements over a range of frequencies up to around 6 or 7 GHz, and demonstrated agreement throughout the range that was well within the limits of accuracy of the two instruments. The frequency limit was the result of connector limitations. Eric didn't document this, but he does recall it along these lines.

In theory, line impedance quickly drops to a stable level, as shown in the following images. Er may decrease with frequency; see the table of frequency-dependent parameters in Figure 2.

The dielectric constant Er de-rates a little with increasing frequency as suggested in the table below, but since Zo is inversely proportional to the square root of Er, that has very little effect on impedance. This is just a typical table for a no-name product. The root of 4.2 = 2.0494, and the root of 3.98 = 1.995, a change of only 2.7%.

Using these data in a frequency-dependent solver, the impedance of the trace looks like Figure 3 (note the additional 1.5 ohms and the fact that it's essentially flat above about 800 kHz).

You may wonder why impedance dips initially. That's because the current distribution in the trace cross-section begins to favor the trace side that faces the reference plane(s), instead of being more uniformly distributed around the
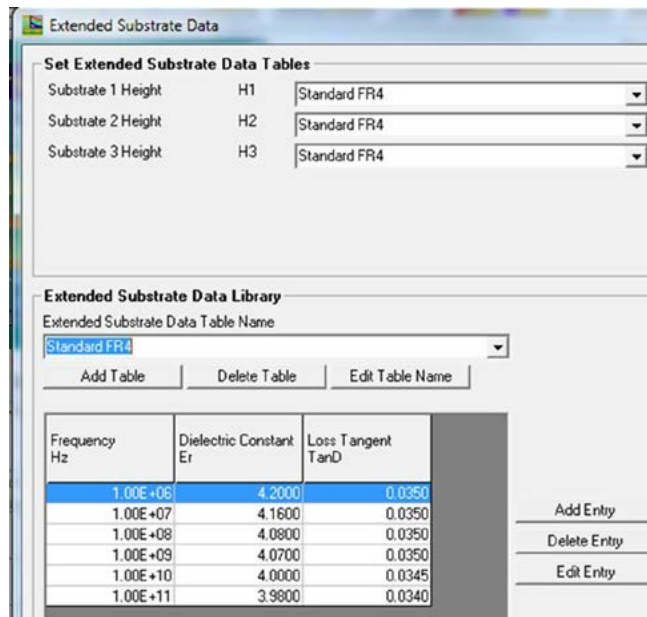

Figure 2: Table showing frequency-dependent parameters.

four surfaces. Thus, moving close to the reference plane reduces loop inductance and increases apparent capacitance, both tending to reduce impedance.

The extra 1.5 ohms is due to the copper conductivity—resistivity, if you prefer—and skin

the pcblist

THE best way to find a PCB fabricator, anywhere.

Saturn Electronics Corporation
Romulus, Michigan, U.S.A.

SEC

[Website] [Contact Me] [$ RFQ]

| Overview | Contact | Specs | About | Videos | Photos | Brochures | News |

Saturn Electronic Corp's commitment to quality extends to our technology, pricing, flexibility, and lean manufacturing. We are always conscious of our role in the PCB supply chain

Markets: Automotive, Communication, Computers, Consumer, Industrial, Medical, Military/Aerospace

Board Types: Single-sided, Double-sided, Multilayer, Flex, Rigid-Flex

Mfg Volumes: Prototype, Small, Medium, Large

Other Services: Quick turn-around

Specialities: Blind/buried vias, Controlled depth drilling, Controlled Impedance, Filled/plugged vias, Heavy copper, Printed Electronics, Sequential lamination

Certifications: AS-9100, ISO 9001, ISO 14000, TO/TS 16949, ITAR registered, QS 9000, ROHS compliant

Featured Showcase

Click here to see a demo

Why YOU should Showcase:

- Capabilities listing for advanced search functionality
- Specialties and certifications listing
- Ability to upload brochures and videos
- Quick and easy "Contact" and "RFQ" buttons
- News, web and contact links

Click to see a partial list of registered OEMs!
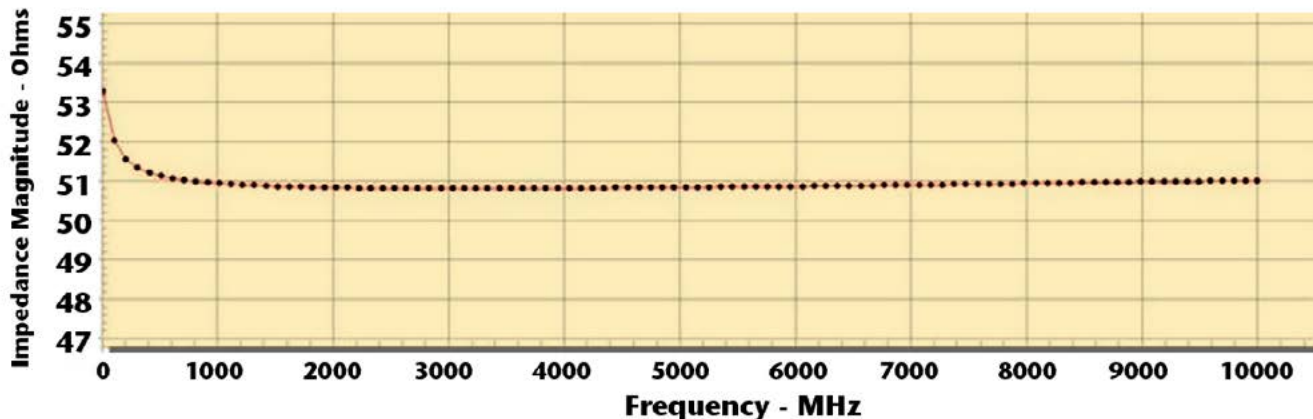
www.thepcblist.com

A FEW NOTES ABOUT TDR *continues*

Figure 3: Impedance of the example trace when using a frequency-dependent solver.
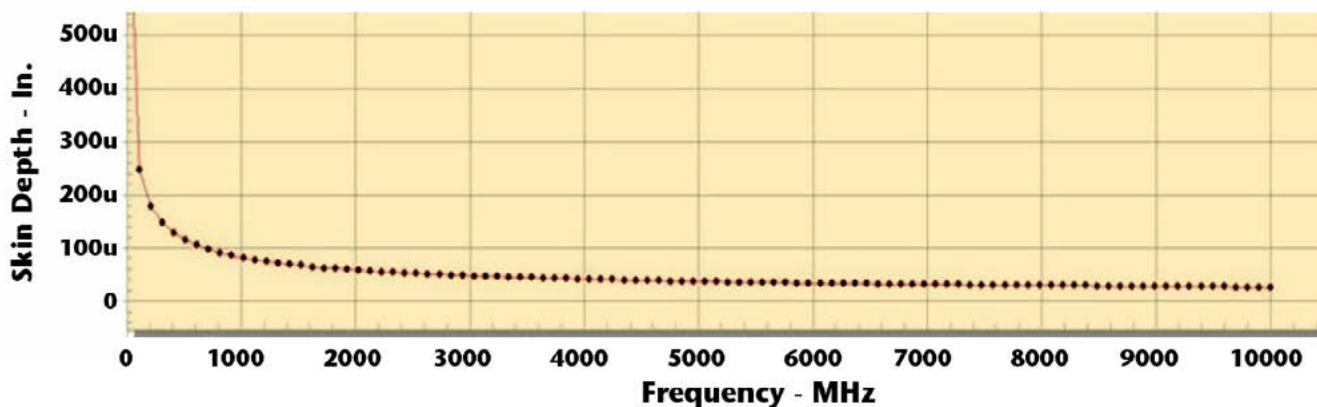

Figure 4: Resistance appears as an upward slope.

depth at frequencies above a few kilohertz.

This resistance shows on the TDR trace as an upward slope along the length of the display (the longer the trace, the greater the resistance.)

As I mentioned regarding coupons, some OEMs have discussed with me the inclusion of dedicated test or "dummy" traces into completed bare circuit boards for the purpose of on-board measurement of impedance. They wanted to do this out of concern that the panel edge coupons might not sufficiently accurately represent on-board trace conditions due to the coupon's physical placement on the panels. Dummy traces can more accurately represent on-board dimensions and environment due to their co-location, and they do have other po-

tential advantages, but have problems of their own.

Consider these issues:
• How can you tie together the reference planes without affecting the rest of the board? In use, boards carry coupling capacitors and are connected to very-low-impedance power supplies.
• We must use valuable board real estate for traces and test points on every board, thus increasing manufacturing cost.
• Testing the trace on every board (what is the point of having per-board test traces if you aren't going to test every one?) results in another cost increase.

• This is not so easily handled in the test area.

• Using a "real" trace is possible, but highly impractical for all of these same reasons.

• Trace configuration (spurs, etc.) are likely to introduce unwanted and misleading waveform artifacts.

• Appropriate probe access to the trace and reference planes is practically impossible.

In a nutshell, board stripline traces are intended to achieve target impedances when loaded and powered. These conditions don't prevail on a bare board, so on-board measurements are very probably misleading (read: impedance higher than target) unless extensive thought goes into the design of the test traces for the purpose. Hence the use of coupons.

Board manufacturers are in a better position to test striplines during the build process because at some stage in the build process, every stripline is a microstrip (before lamination). At

that point in the process, traces and the single reference plane are more easily accessible to test. A field solver can predict the impedance of the trace at this interim stage of the build. If subsequent laminations are completed accurately, as designed, then the target finished impedance will be achieved.

You pay your money and you take your chance, but it's easy to see why coupons remain the favorites."

Again, I'd like to offer a special thanks to Polar's Ken Taylor for sharing his insight into time domain reflectometry, and for helping me help my customer. **PCBDESIGN**

Amit Bahl directs sales and marketing at Sierra Circuits, a PCB manufacturer in Sunnyvale, CA. He can be reached by clicking here.

video interview

Solving Substrate Challenges and High Reliability Needs

by Real Time with... productronica

Dyconex R&D Manager Dr. Marc Hauer touches on the specific challenges and reliability requirements related to substrates for conductive medical devices.

RealTimewith...
VIDEO PRESENTATION
PRESENTED BY I-CONNECT007

CLICK
TO VIEW

realtimewith.com

TOP TEN

News Highlights from PCBDesign007 this Month

① Mentor Posts $275.6 Million in 3Q Revenue

"Third-quarter results substantially exceeded our guidance and reflect the continuing strength in our business," said Walden C. Rhines, chairman and CEO. "Core EDA business such as design to silicon and scalable verification, along with strength in transportation, drove business."

② Zuken Unveils First EDM System for Electrical & Fluid Design

The company has introduced the first data management solution specifically designed to manage E3.series design data in its native format. E3.EDM (Engineering Data Management) builds on Zuken's E3.series and CONTACT Software's CIM DATABASE EDM platform to provide data and process management integrated into E3.series for wire, harness, cable, control system, and fluid design.

③ Azitech to Hold HDI Seminar with Happy Holden

In this two-day event, Happy Holden will take attendees step-by-step through the universe of progressing HDI. He will introduce HDI and its unique design opportunities and, with his vast experience from Foxconn, he will teach how to use HDI correctly and efficiently in products.

④ CadSoft Computer Releases Global Survey Results

The PCB design software vendor marks its 25th anniversary by revealing the findings of its global survey of PCB designers. Ed Robledo, general manager, says, "The huge explosion of development boards, which our survey suggests is reducing the need for custom PCB design, is actually proving to be a big opportunity for us."

⑤ Altium, FTDI Partner to Provide HMI Solution Support

Altium Limited, a global leader in smart system design automation and provider of solutions for 3D PCB design (Altium Designer) and embedded software development (TASKING), has released PCB design content for Altium Designer users supporting the FTDI FT800 family of HMI solutions.

⑥ Mentor Graphics Launches Next-generation FloTHERM

Mentor Graphics has released its next-generation FloTHERM product featuring a new native Windows GUI to handle pre-processing and large models with ease, targeting today's most advanced electronic designs.

⑦ Ucamco Enhances Gerber File Format Specification

The Gerber file format is the bare board industry's CAD-to-CAM data transfer standard. Ucamco, its long-standing custodian and developer, has updated the file specification.

⑧ PCB Solutions Creates Engineering, Design, & Layout Division

The company is pleased to announce the ability to provide engineering services available to customers looking for assistance with engineering, designing, and laying out products that require PCBs.

⑨ Altium Launches New Vault Server and Team Configuration Center

Based on Vault technology, Altium's new Team Configuration Center (TC2) helps organizations centralize and standardize their design environment. Everything from design tool setup and configuration to document templates and manufacturing file formats can be set up and automatically deployed to each engineer's desktop.

⑩ Zuken Innovation World 2014 Issues Call for Papers

The dates for the annual Zuken Innovation World (ZIW) conferences in North America and Europe have been set. A call for papers has been issued for North America and Northern Europe; the deadline for submission for the Dearborn, Michigan event is December 31, 2013.

events

ELE EXPO
January 15–17, 2014
Tokyo, Japan

Electronix R&D Japan
January 15–17, 2014
Tokyo, Japan

Electrotest Japan
January 15–17, 2014
Tokyo, Japan

Material Japan
January 15–17, 2014
Tokyo, Japan

NEPCON Japan
January 15–17, 2014
Tokyo, Japan

CAR-ELE Japan
January 15–17, 2014
Tokyo, Japan

DesignCon 2014
January 28–31, 2014
Santa Clara, California, USA

ADVERTISER INDEX

Next Month in *The PCB Design Magazine:*

A Glimpse into 2014 Technology

What does the future hold for PCB design? What sort of advances are we likely to see in technology? Find out next month! In the January issue of *The PCB Design Magazine,* our clairvoyant contributors whip out their crystal balls and give us a glimpse into 2014.

Enjoy the holidays, and we'll see you in 2014!