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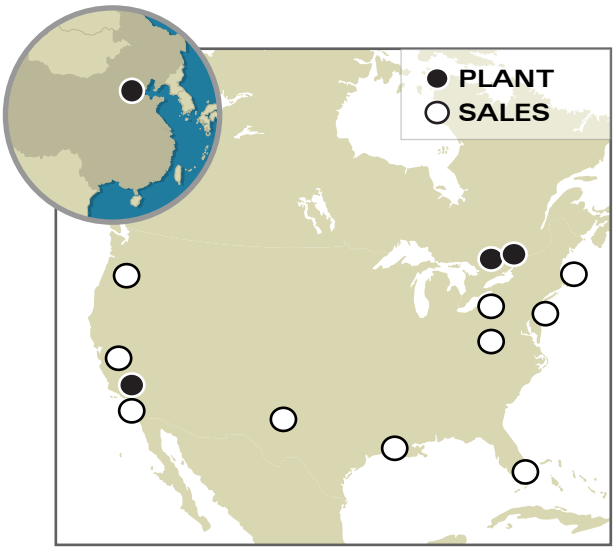

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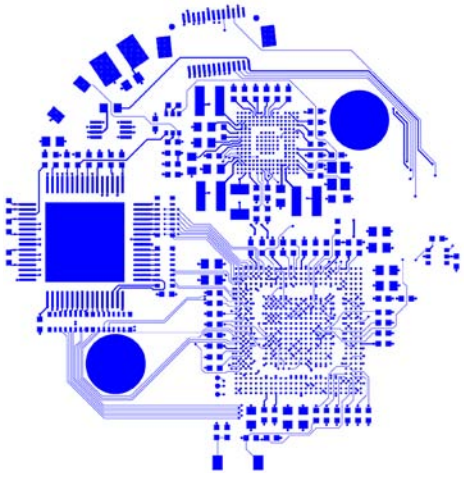
November 2012

PREMIER ISSUE: *HIGH-SPEED DESIGN*

FEATURED CONTENT

THE NEED FOR SPEED – There's no escaping the challenges of high-speed design. After all, no design exists in a vacuum. No matter what type of board you're designing, whether it's a single-sided commercial board or a 24-layer backplane, high-speed design issues are likely to wreak havoc. But we have the cure for your high-speed blues, right here in the inaugural issue of *The PCB Design Magazine!*



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I had mentioned to you upon your last visit that Prototron should feel free to use SelfCharge Inc. as a reference. I believe I speak for everyone in our organization when I say that Prototron has been and continues to be an integral part of SelfCharge's product development. Prototron has had an impeccable ability to meet our high quality standards, on-time delivery performance and price targets.

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Brady L. Boyd, C.P.M.
Materials Supervisor
SelfCharge Inc.

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CONTENTS

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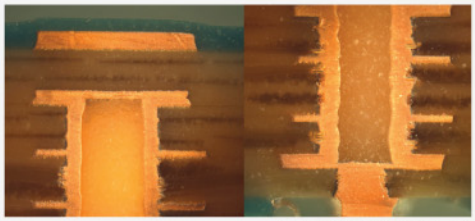

(Magnified @ 100x)

18 layer, .085" thick (2.16 mm), buried and single stack vias.
2 lamination cycles (1+N+1)
This design has passed:

- 10x solder floats @ 288°C (unconditioned)
- 10x reflow @ 260°C (JEDEC std. lead-free cycle) ,
- 6x 260°C preconditioning before 1000 cycles IST @ 150°C followed by 100 cycles @ 190°C
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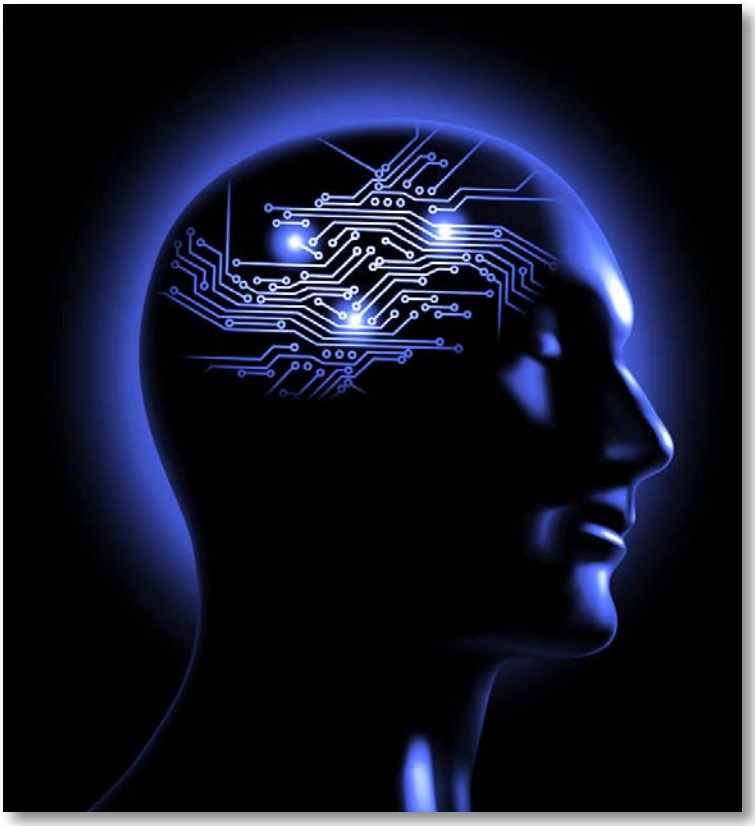
THE SHAUGHNESSY REPORT

Welcome to *The PCB Design Magazine*

by Andy Shaughnessy
I-CONNECT007

SUMMARY: If you're reading this, you've made it – to the introductory issue of The PCB Design Magazine, the only magazine of its kind devoted entirely to PCB design. So, PCB designers and design engineers, this is your magazine. Welcome home!

Welcome to the first issue of *The PCB Design Magazine* – the only magazine dedicated solely to PCB design. If you're a PCB designer or design engineer, this is your magazine. Some of you are no doubt thinking, "It's about time we had our own publication!"



Through the years, I've asked myself why there are no magazines focused specifically on PCB design and design issues. Why indeed?

So, we at I-Connect007 saw a need for a new PCB design publication, and decided to take action. The result is *The PCB Design Magazine,* a monthly, subscription-based magazine in the style of our sister publications, *SMT Magazine* and *The PCB Magazine*. Readers can expect exhaustive coverage of the issues that are important to the PCB design community, in a digital format that allows live-action animation, like the super cool cover of this issue. And because we're a green publication, we're not killing any trees.

As an I-Connect007 publication, *The PCB Design Magazine* will take full advantage of our video and audio technology. We'll be bringing you complete video coverage of DesignCon, as well as the Designers Forum at IPC APEX EXPO, with guest editors you've come to know and trust like Mark Thompson and Kelly Dack, and more. PCB designers are anything but boring, and it's my job to make every issue more exciting than the last. Each issue will be packed with the news and technological information you need, and, almost as importantly, each issue will be fun.

The response from the design community has been overwhelming. Since we broke the news, designers and engineers have been sending me articles and columns from around the world. I field calls almost every day from designers who are interested in writing for the magazine. I haven't had to resort to the usual arm-twisting to get good content. I can't think of a better way to launch a PCB design magazine than with feature articles by longtime industry gurus like Lee Ritchey and Happy Holden. *The PCB Design Magazine* definitely has quite a buzz going now.

I think we're on the right track. I'm fortunate to have quite a stable of fantastic columnists and contributors, and together we're going to make this magazine the "go-to" place for PCB designers. We do what we can to support

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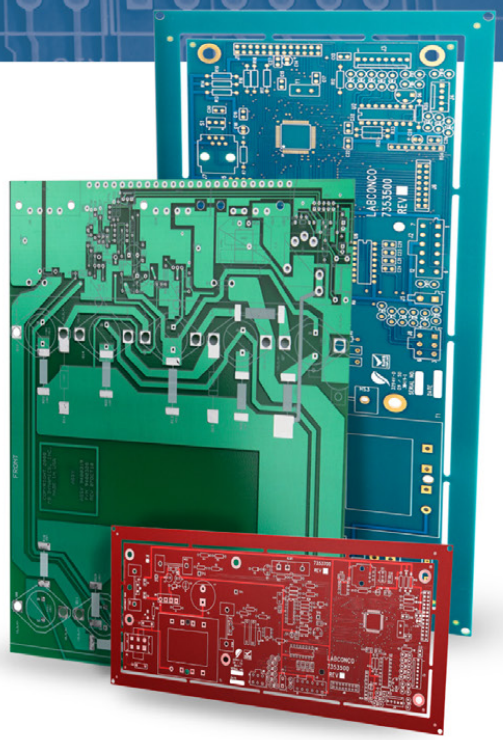

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WELCOME TO THE PCB DESIGN MAGAZINE *continues*

the industry, and I appreciate all of your support in return. You can be sure that we won't take this responsibility lightly.

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If you buy fabricated boards and you haven't already checked out *The PCB List*, now is the time. The PCB List is the single biggest database of fabricators anywhere, and there are enough search options that buyers can find exactly what they need, from the part of the world where they want to do business.

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The PCB List is just one more service that we provide to help make designers' jobs a little easier. Isn't it time someone made your job easier?

Thanks for reading our first issue of *The PCB Design Magazine*. If you haven't subscribed yet, you can do so by clicking here.

Welcome home. **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 13 years. He can be reached by clicking here.

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Designing a PCB Stackup, Part 1

by Lee W. Ritchey
SPEEDING EDGE

SUMMARY: The challenge in designing a PCB stackup is to satisfy its many demands. Information in this document is drawn from experience gained designing more than 2,000 PCB stackups for products as simple as video games and as complex as the highest-performance backplanes used in supercomputers and routers.

The practice that has worked in the past of allowing the fabricator to design a PCB stackup no longer works. Speeds have increased to the point where signal integrity and power delivery considerations make it necessary to employ far more discipline in the choice of materials and arrangement of the layers in the stackup – both of which are outside the skill set of virtually all PCB fabricators. A common part of the vendor selection process has been to submit each design for a quote to several fabricators and make the choice based on price only. This is very often a fatal method of vendor selection because the lowest bidder often takes shortcuts in order to achieve the lowest price and/or may not possess the skills necessary to manufacture quality PCBs of the given complexity.

Among the demands placed on stackup design are:

- Providing enough signal layers to allow successful routing of all signals to signal integrity rules.
- Creating copper thickness in planes and signal layers that meets the conductivity demands of signals and power and, at the same time, be reasonable to manufacture.
- Providing enough power and ground layers to meet the needs of the power delivery system.
- Specifying dimension trace widths and dielectric thicknesses that allow impedance targets to be met.
- Ensuring that the spacing between signal layers and their adjacent planes is thin enough to satisfy crosstalk needs.
- Specifying dielectric materials that are economical to manufacture and readily available.
- Avoiding the use of expensive techniques such as blind and buried vias and build up processing if possible.
- Providing for prototype manufacture in one factory or country and production manufacture in another factory or country.

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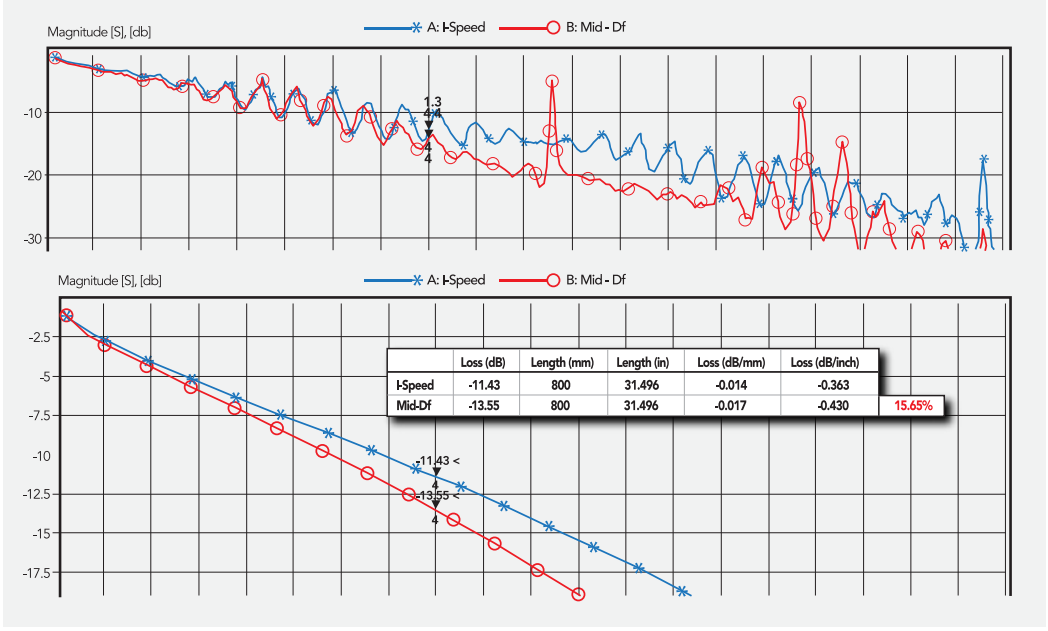

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DESIGNING A PCB STACKUP, PART 1 *continues*

Information needed to design a successful PCB stackup is scattered among many documents and specifications, many of which are not in the public domain. This document is intended to bring all of the necessary information into one document to improve the design process.

How a Typical Multilayer PCB is Built

In order to understand the choices that must be made when designing a PCB stackup, it is useful to review how a typical multilayer PCB is fabricated. Figure 1 is a diagram showing the components that make up a six-layer PCB. The manufacturing method shown in the figure is referred to as foil lamination. This refers to the fact that the two outer layers begin as sheets of foil copper with no images etched into them. This is the most cost-effective way there is to manufacture a multilayer PCB and should be the objective of the stackup design process. There are other methods available, such as cap lamination, that forms the outer layers as part of a two-sided piece of laminate and build up processing that involves blind and buried vias. These choices always result in more expensive PCBs and should be considered only as a last resort.

It should be noted that PCB layers are built in pairs. Therefore, PCBs normally have an even number of layers. As a result, when additional layers are needed they will be added one pair at a time along with an additional pre-preg layer. Designing a stackup with an odd number of layers when only one additional layer is needed does not result in a PCB that is cheaper than if a pair of layers had been added. The reason for this is that the fabricator will need to purchase a piece of laminate for the added layer that has copper foil on both sides. The copper foil that is not needed will be etched away when the necessary foil side is etched.

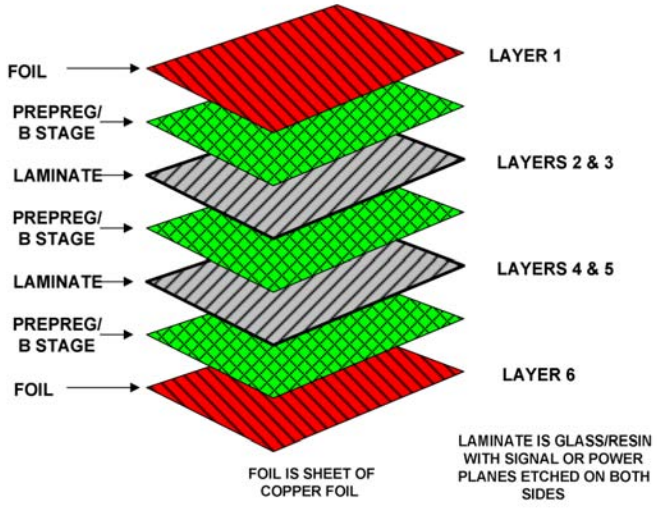

Figure 1: A typical six-layer PCB stackup using foil lamination.

As can be seen from Figure 1, three main components make up a multilayer PCB. These are:

• Sheets of laminate that have a sheet of copper foil bonded to each side which have the patterns for either signal layers or plane layers etched into the copper foils. These are often referred to as details. (Laminate is a combination of woven glass cloth and a resin system such as epoxy or polyimide.) The thickness of the copper on each side of this laminate can vary from ½ ounce to 2 ounces. (Copper foil thickness is specified in ounces per square foot of surface area. 1 ounce is approximately 1.4 mil or 36 microns thick.)

• Sheets of uncured laminate called pre-preg placed between the details and between details and the outer foil sheets. This pre-preg is a woven glass material coated with the same resin system that is used in the laminates. Unlike the laminates, the resin is only partially cured. During lamination heat will cause this resin to melt and flow into the voids in the adjacent copper layers, serving as the glue to bond the layers together and then cure it to the same rigid state as the resin in the laminate. After lamination prepreg is indistinguishable from laminate.

• Sheets of copper foil to form the outer layers. The reason the two outer layers are solid copper at this stage instead of etched with the outer layer patterns is to provide a path for the current required to plate copper into the holes drilled through the PCB for vias and component leads. The task of the stackup designer is to select combinations of pre-preg, laminate and foils that provide the desired electrical charac-

teristics while satisfying cost and manufacturability goals.

Alternative PCB Fabrication Methods

Figure 2 is an illustration of the cap lamination method of manufacturing a multilayer PCB. As can be seen, there are three pieces of laminate each with two conductor layers in this version of a six-layer PCB. The most obvious difference between this and foil lamination for this six-layer PCB is that only two pieces of laminate or details must be processed using foil lamination while three are required with cap lamination. This represents a cost increase over foil lamination. This was the method used to fabricate PCBs in the early days of multilayer fabrication.

A third method for creating a multilayer PCB is by the use of buried and blind vias. In one version of this method, the internal n-2 layers are fabricated using either of the two methods shown above, resulting in a complete sub-PCB with plated through holes running from layer 2 to layer n-1. Then, a piece of pre-preg and a piece of foil are added to each side and the combination is laminated into a final PCB of n layers. After this second lamination step, holes are drilled through the entire stackup and plated.

It is also common to drill blind vias from layer 1 to layer 2 and layer n to layer n-1 as well. It is easy to see that this method will result in a significantly more expensive PCB that takes longer to manufacture than either of the above choices. (In some cases PCBs designed to use buried vias can cost as much as twice what the same number of layers would cost using only through-hole vias.)

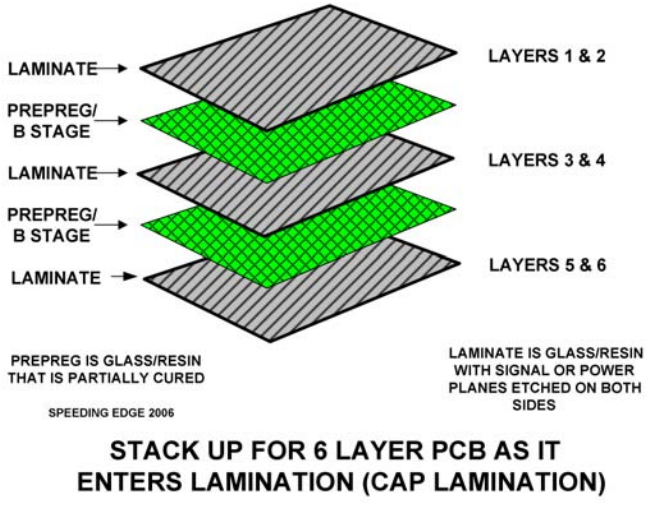

Figure 2: Typical six-layer PCB using cap lamination.

Choosing a Fabricator as a Design Partner

One of the secrets to creating PCB stackups that are right the first time is to select a PCB fabricator to work with while trading off manufacturability of the final PCB stackup against signal integrity and cost goals. The right fabrication engineer can provide valuable insight into the manufacturability of proposed stackups as well as advice on how to improve a stackup. Clearly, for this to work, the fabricator must have experience manufacturing PCBs of the complexity being designed. The design engineering department must have a clear, direct path to the engineering department of the fabricator. The classic method of allowing the purchasing or materials department to select fabricators based on cost does not work well with modern designs.

My first criterion in choosing fabricators is "Are they building PCBs like mine every day or will my design represent a stretch for them?" As always, selecting fabricators that demonstrate recent capability with the class of PCB being designed goes a long way toward ensuring success on the first try. The best way to determine that there is a match is to conduct a vendor survey by visiting the factory and viewing the production line itself. Look for PCBs of your complexity being manufactured in real time. (It is common for fabricators to display complex PCBs in conference rooms that do not represent the actual capability of the fabrication process as a way to impress customers.)

This is the standard method used by companies such as Cisco to ensure suppliers are matched to the need. These visits are conducted by a team of people who represent manufacturing, engineering and purchasing, to make sure all areas are covered. Failing that, the next best way is by checking references to see how satisfied current customers are; ask for references who are willing to discuss their experiences with the supplier. If no references are forthcoming, it is well to beware.

DESIGNING A PCB STACKUP, PART 1 *continues*

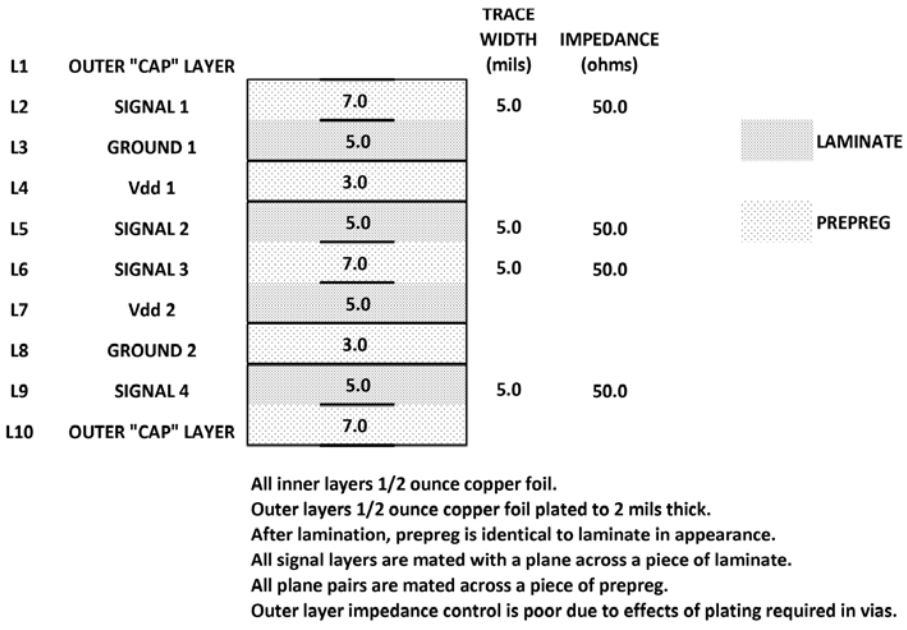

Figure 3: A typical 10-layer PCB stackup.

Types of Signal Layers

Figure 3 is a typical 10-layer PCB stackup. This example has three types of signal layers: surface microstrip (L1 & L10), buried microstrip (L2 and L9) and off-center or dual stripline (L5 & L6).

There is a fourth type of signal layer-centered or symmetrical stripline: a single stripline layer centered between two planes. The reason that dual stripline is used more often than single stripline is that each time a single stripline layer is added to a stackup, a plane must also be added to isolate signal layers from each other, resulting in higher layer counts for a given number of signal layers. The method used to keep the two signal layers in the dual stripline configuration from interfering with each other (crosstalk) is to route signals on one layer horizontal and on the other vertical.

In this example, the two outer layers are not used for signals. The reason is impedance uniformity on these layers is difficult to control accurately due to the uneven plating of copper that often results when plating is done to plate copper in the holes that conduct current such as vias and power leads.

Alternate Ways to Stack Layers

Figure 4 shows two different ways to arrange the layers in a ten-layer PCB. The short bars represent signal layers and the long bars represent planes. The stacking on the left appears to have two more signal layers than the one on the right due to the fact that the top and bottom layers on the right are not available for signals and this is true. The disadvantages of the stackup on the left are power delivery related. Most high-speed designs require plane capacitance to support fast switching edges. In order to create plane capacitance, pairs of planes must be close to each other (less than 4 mils, 100 microns). The stackup shown in Figure 4 has only one plane pair close together while the stackup on the right has two plane pairs.

A second benefit of the stackup on the right in Figure 4 is that the plane pairs are separated by pre-preg which can be made very thin, less than 3 mils, as shown in Figure 3. This is of significant value when designing a power delivery system.

A third benefit of the stackup on the right is that each signal layer is paired with a power plane across a piece of laminate. The benefit here is that during lamination, the thickness of the laminate does not change and this makes it possible to achieve tightly controlled impedances on the transmission lines. When a signal layer is mated with a plane across a piece of prepreg, impedance control is more difficult as the pre-preg thickness can change significantly during the press cycle.

For all the reasons given above, the layer stacking on the right in Figure 4 represents the best compromise between power delivery and impedance accuracy. If two more signal layers are needed, they would be added along with two more planes resulting in a 14-layer PCB. If four more signal layers are needed then four

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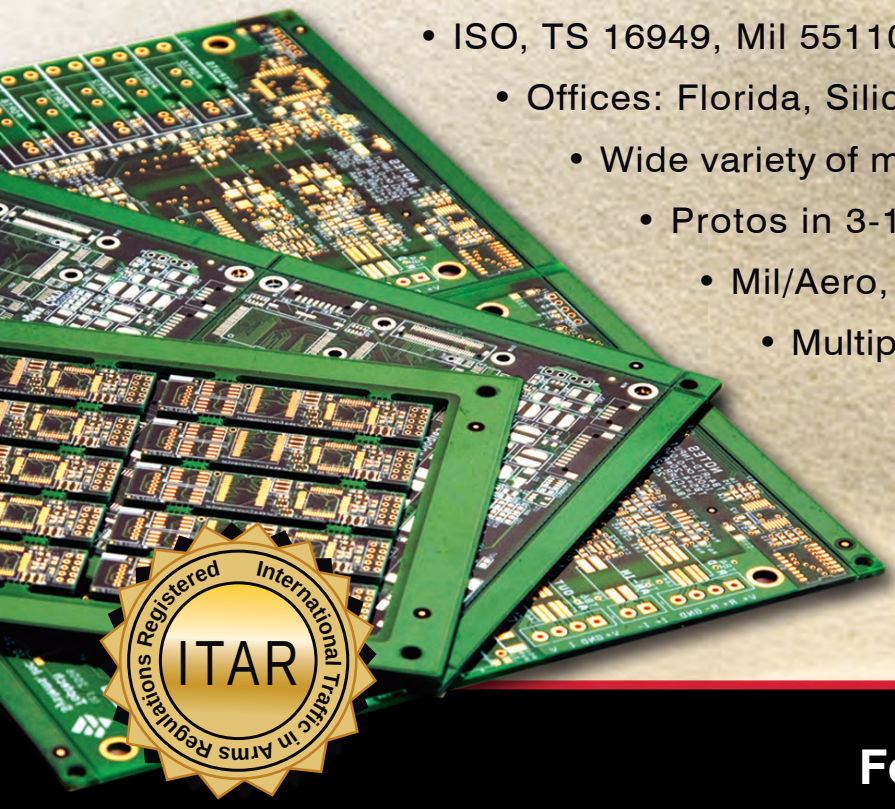

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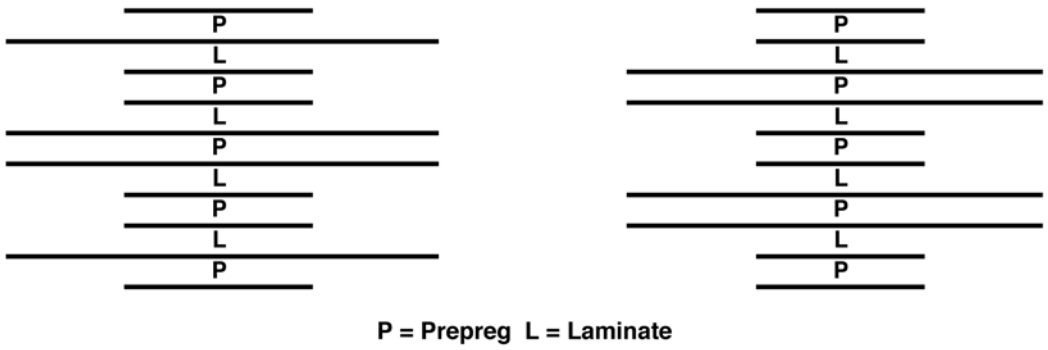

Figure 4: Two ways to arrange plane and signal layers in a 10-layer PCB.

more signal and four more plane layers would be added, resulting in an 18-layer PCB and so on for 22 and 26 layers.

Selecting an Impedance

The starting point for most PCB stackup design is determining what impedance or impedances to use in each signal layer. A number of impedances have been used for controlled impedance PCBs. Among these are 62 or 65 ohms for PCI buses, 72 or 75 ohms for video signals, 50 ohms for ECL and high-speed CMOS, 28 ohms for Rambus and an assortment of differential impedances for various differential signaling protocols.

Attempting to design stackups that accommodate more than one impedance value has proven to be difficult. A reasonable question to ask is whether or not multiple impedances are really necessary. The most common impedance found in multilayer PCBs is 50 ohms. It turns out that this impedance represents a happy medium between impedance value and ease of manufacture when more than two controlled impedance signal layers are needed. Therefore, it is worth examining the protocols that specify other impedance values to see if they will operate successfully with a 50-ohm transmission line.

The most common PCB impedance is 50 ohms. This impedance is achieved on stripline layers with a trace width that is about the same as the dielectric thickness. In order to make a 62-ohm line for the PCI bus, the trace width has to be made very narrow in stripline layers. Reference 1 explains how this impedance came into existence and demonstrates that the PCI bus works properly with 50-ohm transmission lines. A similar analysis will show that the Rambus protocol also works properly with 50-ohm transmission lines. (To make a 28-ohm line, the trace width must be so wide that it will not fit between pins on a BGA.)

This leaves 72-ohm video and the various differential protocols. In almost all cases, the 72-ohm video requirement is to match 72-ohm coaxial cable bringing a signal onto a PCB or taking it off the PCB. Building a stackup that allows both 50 ohms and 72 ohms in the same signal layer is very difficult, if not impossible. Is that really necessary? I have found that if the IC using the video signal is located close to the edge of the PCB, as most are, a very short trace of 50 ohms is not going to significantly degrade the video signal. This can be easily validated using any good SI simulator.

The 100-ohm differential impedance requirement is an artifact of the need to provide two 50-ohm lines each parallel terminated in 50 ohms[2]. It can be seen that the optimum way to route differential signals in a PCB is so that neither member of a pair interacts with the other. This is achieved by separating them from each other far enough so that one does not drive down the impedance of the other. When this is done, it is no longer necessary to specify differential impedance. As a result, all of the signals that need controlled impedance can be routed with the same impedance. The question is, what impedance?

From all of this, it can be seen that 50 ohms is a very good compromise impedance. It also happens to be in the sweet spot of the PCB fabrication process as well as of all the tools used to measure impedance and other characteristics of transmission lines. Therefore, it is wise to construct stackups that have a nominal impedance of 50 ohms.

In spite of what might be called out in some applications notes, every modern logic family fast enough to require controlled impedance and terminations is capable of driving a 50-ohm transmission line so there is no need to design complex stackups that require complex routing rules in order to make all of the nets fit into the space available in the signal layers.

Making All Layers the Same Impedance

Sometimes, in an attempt to provide more than one impedance on the same PCB, there is the temptation to make some layers of the stackup one impedance and others a different impedance. Examples of this are to make the PCI bus at 65 ohms and other signals 50 ohms. If this is done it is likely that the layers containing one impedance may be used sparsely while layers containing the other impedance may be overcrowded. Therefore, it is wise to make all layers the same impedance so the task of routing is easy.

Selecting Laminates

PCB material systems are defined by the resin systems used to make the laminate and prepreg. To a lesser extent, the type of glass is also part of how a laminate system is differentiated from its competition. For the most part, a glass composition known as "E" glass is used.

Resin systems used to manufacture laminate include:

- Epoxy-based systems (sometimes called FR-4)
- Polyimide
- PPO-polyphenylene oxide
- PPE-polyphenylene ester
- BT-bismalamine triazine
- CE-cyanate ester
- Phenolic cured epoxy
- Cyanate ester modified epoxy
- Filled phenolic cured epoxy

For a detailed discussion of the merits and drawbacks of each of these resin systems, see Chapter 5[2].

In the early years of PCB manufacture the resin system choices were epoxy and polyimide. Polyimide has very good high temperature characteristics, but is very difficult to process and absorbs moisture to a level that causes it to fail leakage tests unless it is baked dry and then waterproofed. Epoxy-based systems are very easy to process and do not fail leakage tests, but don't tolerate the temperatures required to solder well. All of the other resin systems on the above list were developed in the hopes of achieving the ease of processing of epoxy and withstanding the high temperatures associated with soldering and rework achieved with polyimide. The results have been mixed. The work horses of PCB fabrication are still variations of epoxy and polyimide.

In the United States, the resin systems of choice have been Isola Corporation's FR406 and FR408 and Nelco Corporation's N4000 series. When selecting a resin system for a project it is advisable to check with the probable fabricators and determine which laminate system in their production inventory works best. It is also advisable to choose a resin system that has an equivalent with both suppliers in order to avoid creating a single-source situation.

Most projects designed in the U.S. are destined for volume manufacture off shore in China, Taiwan, Japan or South Korea. The resins systems listed above are available in all of those countries. However, there are laminate manufacturers in all four countries that manufacture laminate locally. Among these are Mitsubishi, Panasonic, Matsushita and TUC. All of these suppliers have laminates that are equivalent to the main stream laminates used in the U.S. When designing a stackup that will be prototyped in the U.S. and manufactured in volume offshore it is advisable to obtain the materials information from the offshore supplier and make sure the materials needed are available off shore.

Laminate systems are created in two parts. These are the cured laminate with copper foil on each side and partially cured laminate (prepreg) that will serve as the glue layers during

DESIGNING A PCB STACKUP, PART 1 *continues*

lamination. When creating a stackup, it is necessary to get the specifications for both types of material in order to create a stackup that can be built with available materials. Figure 5 is this information for Isola's IS620i. Notice that each thickness of laminate is made with woven glass cloth and resin. The standard construction column specifies what type of glass cloth is used for each thickness. These numbers refer to a particular glass weave with precisely specified numbers of threads per inch and thread diameter. For more details on each glass style see Chapter 5[4].

Notice that the relative dielectric constant (e_r) varies in two ways. First, it varies with the ratio of glass to resin. Second, it varies with frequency. Therefore, it is necessary to specify both in order to achieve accurate impedance calculations. It is easy to determine which e_r to use based on ratio of glass to resin. The big question is what frequency should be used for a given design. Virtually all modern designs will have components on them with 200 pSec or faster edges that must be properly controlled. It has been shown that the equivalent frequency for this rise time is approximately 2 GHz. Therefore, using the e_r value at 2-2.5 GHz will result in accurate impedance calculations.

As can be seen in the above tables, a wide variety of glass styles are used to manufacture laminate and pre-preg. Prior to the advent of multigigabit differential signaling protocols, the glass style had little effect on signal quality. Since then, it has been shown that certain glass

Core Thickness	Standard Constructions	Resin Content	Dk at 100 MHz	Dk at 500 MHz	Dk at 1 GHz	Dk at 2.0 GHz	Dk at 5.0 GHz	Dk at 10.0 GHz
0.0020	1-106	70	3.30	3.29	3.29	3.28	3.24	3.24
0.0027	1-1080	60	3.52	3.51	3.51	3.51	3.47	3.47
0.0030	1-1080	63	3.45	3.45	3.44	3.44	3.40	3.40
0.0035	2-106	66	3.39	3.38	3.38	3.37	3.33	3.33
0.0035	1-2113	51	3.74	3.74	3.73	3.73	3.70	3.70
0.0040	2-106	70	3.30	3.29	3.29	3.28	3.24	3.24
0.0040	1-3070	49	3.80	3.79	3.79	3.78	3.75	3.75
0.0040	1 - 3313	55	3.64	3.64	3.63	3.63	3.59	3.59
0.0043	106/1080	62	3.48	3.47	3.47	3.46	3.42	3.42
0.0045	106/1080	63	3.45	3.45	3.44	3.44	3.40	3.40
0.0050	2-1080	57	3.59	3.59	3.58	3.58	3.54	3.54
0.0050	106/2113	55	3.64	3.64	3.63	3.63	3.59	3.59
0.0050	1-1652	43	3.96	3.95	3.93	3.94	3.92	3.92
0.0055	1-1652	47	3.85	3.84	3.84	3.84	3.81	3.81
0.0060	1080/2113	54	3.67	3.66	3.66	3.65	3.62	3.62
0.0060	106/ 1080	70	3.30	3.29	3.29	3.28	3.24	3.24
0.0065	1080/2113	57	3.59	3.59	3.58	3.58	3.54	3.54
0.0070	1080/2116	58	3.57	3.56	3.56	3.55	3.52	3.52
0.0070	2-2113	52	3.72	3.72	3.71	3.70	3.67	3.67
0.0075	2 - 3313	52	3.72	3.72	3.72	3.71	3.70	3.67	3.67
0.0080	2-3070	49	3.80	3.79	3.79	3.78	3.75	3.75
0.0100	2-1652	43	3.96	3.95	3.93	3.94	3.92	3.92
0.0100	3-1080	66	3.39	3.38	3.38	3.37	3.33	3.33
0.0100	2-2116	54	3.67	3.66	3.66	3.65	3.62	3.62
0.0120	2-2113/ 1652	48	3.82	3.82	3.81	3.81	3.78	3.78
0.0140	2-2116/1652	47	3.85	3.84	3.84	3.84	3.81	3.81
0.0160	3-1652	46	3.88	3.87	3.87	3.86	3.83	3.83
0.0180	2-3070/2-1652	46	3.88	3.87	3.87	3.86	3.83	3.83
0.0210	2-2116/2-1652	50	3.77	3.76	3.76	3.76	3.72	3.72

ISOLA IS 620I LAMINATE INFORMATION

Prepreg	Resin Content	Thickness (in)	Dk at 100 MHz	Dk at 500 MHz	Dk at 1 GHz	Dk at 2.0 GHz	Dk at 5.0 GHz	Dk at 10.0 GHz
106	75	0.0025	3.20	3.19	3.19	3.18	3.14	3.14
1080	65	0.0033	3.41	3.40	3.40	3.39	3.35	3.35
2113	58	0.0042	3.57	3.56	3.56	3.55	3.52	3.52
3313	54	0.0036	3.67	3.66	3.66	3.65	3.62	3.62
3070	55	0.0046	3.64	3.64	3.63	3.63	3.59	3.59
2116	55	0.0052	3.64	3.64	3.63	3.63	3.59	3.59
1652	51	0.0061	3.74	3.74	3.73	3.73	3.70	3.70

Prepreg	Resin Content	Thickness (in)	Df at 100 MHz	Df at 500 MHz	Df at 1 GHz	Df at 2.0 GHz	Df at 5.0 GHz	Df at 10.0 GHz
106	75	0.0025	0.0046	0.0050	0.0056	0.0058	0.0066	0.0073
1080	65	0.0033	0.0049	0.0052	0.0057	0.0059	0.0066	0.0072
2113	58	0.0042	0.0051	0.0054	0.0058	0.0060	0.0066	0.0071
3313	54	0.0036	0.0052	0.0055	0.0059	0.0060	0.0066	0.0071
3070	55	0.0046	0.0051	0.0055	0.0059	0.0060	0.0066	0.0071
2116	55	0.0052	0.0051	0.0055	0.0059	0.0060	0.0066	0.0071
1652	51	0.0061	0.0053	0.0055	0.0059	0.0060	0.0066	0.0070

ISOLA IS 620I PREPREG INFORMATION

Figure 5: Typical resin information.

weaves can result in differential skew and excessive jitter in differential signal paths operating at or above 2.4 Gb/S[5].

It has since been shown that three weaves which exhibit this problem are 106, 1080 and 7628. Avoiding the use of these weaves in a high-speed design obviates this problem. Of all those listed, 3313 has been shown to be the most uniform weave. For this reason, I use this weave between all my signal layers and their nearest planes.

As mentioned earlier, all of the common laminates use a glass known as "E" glass formulated to spin well and allow good adherence of resin. This glass happens to have a relatively high loss tangent. There is an alternate glass referred to as "S" glass that has a lower loss tangent. At least one laminate supplier, Nelco, uses this glass to create a low-loss laminate known as N4000-13SI. This material does have a low loss, but at the expense of creating a single-sourced PCB design. The Isola IS620i shown here has proven to be a drop-in replacement for N4000-13SI if the need for lower-loss laminate is encountered.

Considerations When Selecting a Laminate System

There are a number of properties of laminates that must be taken into account when selecting a laminate system. Among these are:

- Does the PCB require lead free assembly?
- Does the PCB require a high T_g (ability to withstand high temperatures)?
- Does the design require a low-loss laminate?
- Can the program tolerate a single-source laminate?
- Will production volumes be manufactured in a different shop or country than the prototypes?

When most of these conditions must be met, many of the laminate types listed above will be eliminated from consideration.

Obtaining Laminate Information

In order to properly design a PCB stackup it is necessary to obtain laminate information of the quality shown in Figure 5. There are two places to get this information. These are the fabricator and the laminate manufacturer. My first choice is to ask the fabricator for this data. Often, the engineering departments of fabricators do not have it. This is a sign that the fabricator is not up to the skill level required to successfully participate in designs of this complexity.

In the event the fabricator does not possess this information, the second choice is to contact the materials manufacturer directly. Laminate manufacturers accustomed to supplying materials to the high performance market will have their materials characterized in this manner and will openly share the data. There are laminate manufacturers who do not have this data. They have been supplying materials to the low-performance market and should be avoided.

In Part 2, we will investigate methods for calculating and testing impedance, and discuss the steps required for proper PCB stackup. **PCBDESIGN**

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Lee Ritchey is founder and president of Speeding Edge. A longtime PCB design instructor and consultant, Ritchey is the author of "Right the First Time: A Practical Handbook of High-Speed PCB and System Design."

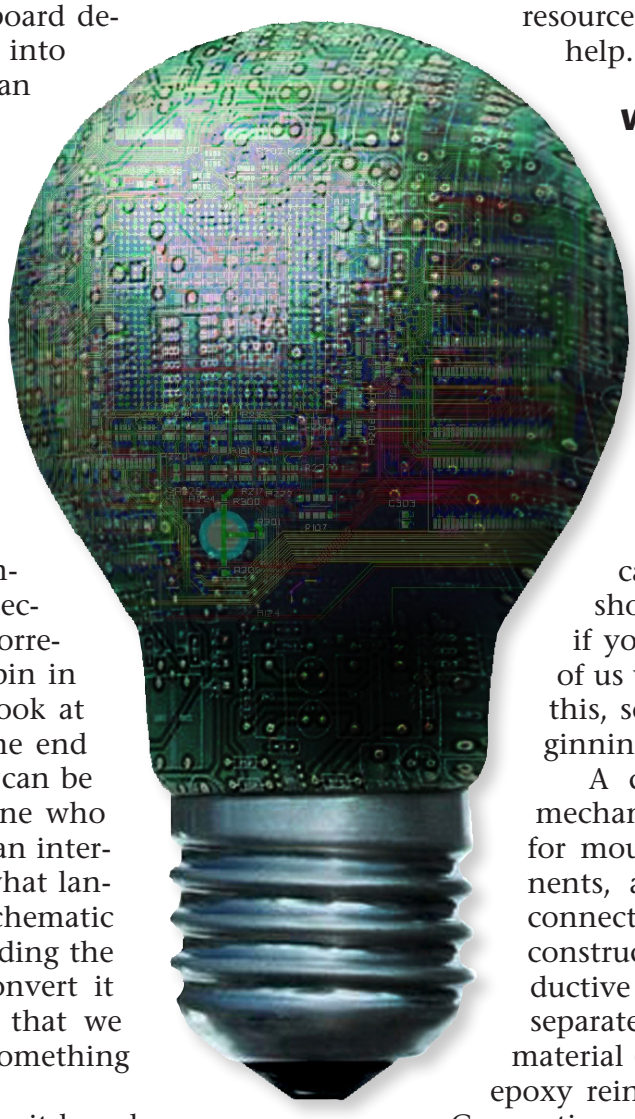
So You Want to be a Designer?

by Jack Olson

SUMMARY: Welcome to the first in a series of short tutorials on becoming a circuit board designer. If you're new, there's a lot to learn. We'll explore the PCB design process one step at a time, explaining the terminology and adding more pieces to the puzzle from month to month.

Your job as a circuit board designer is to convert ideas into reality. How's that for an opening statement?

Maybe it sounds too philosophical for a technical tutorial, but think about it. An engineer records ideas in the form of a schematic. He does this by placing symbols (which represent electronic components) and connecting the symbols together with lines (which represent conductive wires). Each connection point on the page corresponds to a component pin in the real world. We will look at this in detail later, but the end result is a schematic that can be shared with others; anyone who understands electronics can interpret the idea no matter what language he speaks. But a schematic is only a method of recording the idea. Someone has to convert it into something physical that we can hold in our hands – something we can test.



The end result is a circuit board assembly, and if you want to learn how to create one from a schematic, you've come to the right place!

Welcome to the first in a series of short tutorials on becoming a circuit board designer. If you're new, there's a lot to learn. We'll explore the PCB design process one step at a time, explaining the terminology and adding more pieces to the puzzle from month to month. As we go through it, I'll try to provide other resources where you can get more help. So, let's get started…

What is a Circuit Board?

Most of you probably wouldn't be reading this if you didn't already know what a circuit board is, but my goal is to teach the basics, and assume you know nothing. Many costly mistakes in this industry can be traced back to incorrect assumptions and poor communication, and one habit you should develop early is that if you don't know, ask! None of us was born knowing any of this, so we'll start from the beginning.

A circuit board provides a mechanically stable substrate for mounting electronic components, and provides conductive connections between them. It is constructed with layers of conductive material (usually copper) separated by layers of insulating material (usually a flame-retardant epoxy reinforced with glass fibers). Connections between conductive layers are made through plated holes.

If I had to describe the job of a circuit board designer in a single sentence, it would look

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SO YOU WANT TO BE A DESIGNER? *continues*

like this: Circuit board designers create a board shape that fits the physical size requirements, position the mounting and tooling features, determine the number of conductive layers (cost vs. performance), logically arrange circuits into functional areas (floor-planning), populate each area with appropriate land patterns (placement), add planes and traces to connect everything together (routing), and generate data to fabricate, assemble and test the product.

Beyond that, if the design is to eventually become part of a product, it needs to be manufacturable in some quantity. Feature sizes are selected to be compatible with bare board fabrication and test processes. Decisions are made with automated assembly and soldering methods in mind. There might be cost constraints involved, and environmental factors, and the final product needs to be robust enough to survive the customer's use and expected reliability.

Good design involves juggling many factors, and we'll look at each of these in detail in future columns. **PCBDESIGN**

Jack Olson, CID+, has been designing circuit boards full-time for over 20 years. He would like to thank Laser Precision Analytical for giving him his first design job.

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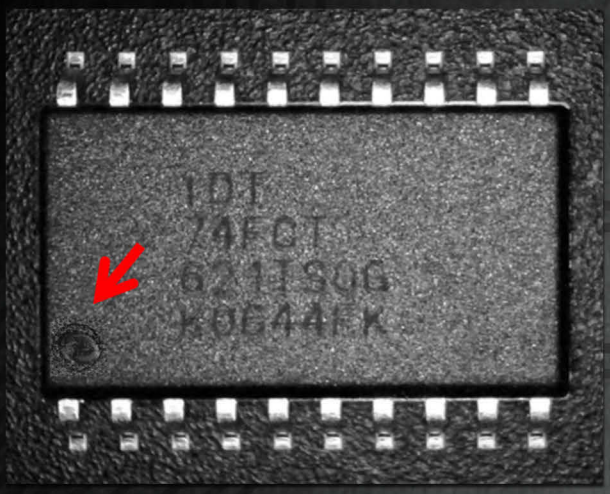

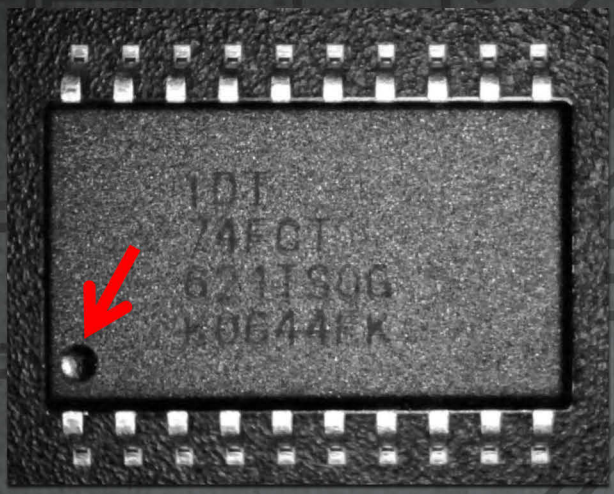

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Partner Early for HDI Board Design

by John Levreault

SUMMARY: When customers want to design boards that are as compact as possible, there is often very little reliable guidance from the chip vendors. Heed the warnings of Texas Instruments: Consult board manufacturers from the start of any projects involving BGAs with a pin pitch of 0.4 mm and smaller.

To preface this story about the design of my first HDI boards, let me point out I'm primarily an analog design engineer who's been designing mixed-signal boards for well beyond 25 years. There's nothing better than starting with a fresh sheet of paper, or more recently a blank screen, and developing a schematic that leads to a board that performs exactly as intended.

I think in terms of schematics. Over the years, by the way, I've designed many high-power class-D amplifiers that are in wide use, with varying amounts of logic to support or control that function. Today, though, chip vendors have made custom design unnecessary, for the most part, for amplifiers with outputs up to 250 W or so. More power to them (!) and hats off, but I do have a bone to pick with them in another regard. I'll get to that soon.

The first project I was contracted to design, which led, inevitably, to an HDI board architecture, was a multimedia processor based on a Texas Instruments OMAP. It was an upgrade of a product for which there was a lot of existing hardware and legacy peripherals, and my customer wanted to move to a new processor for improved audio and video performance and

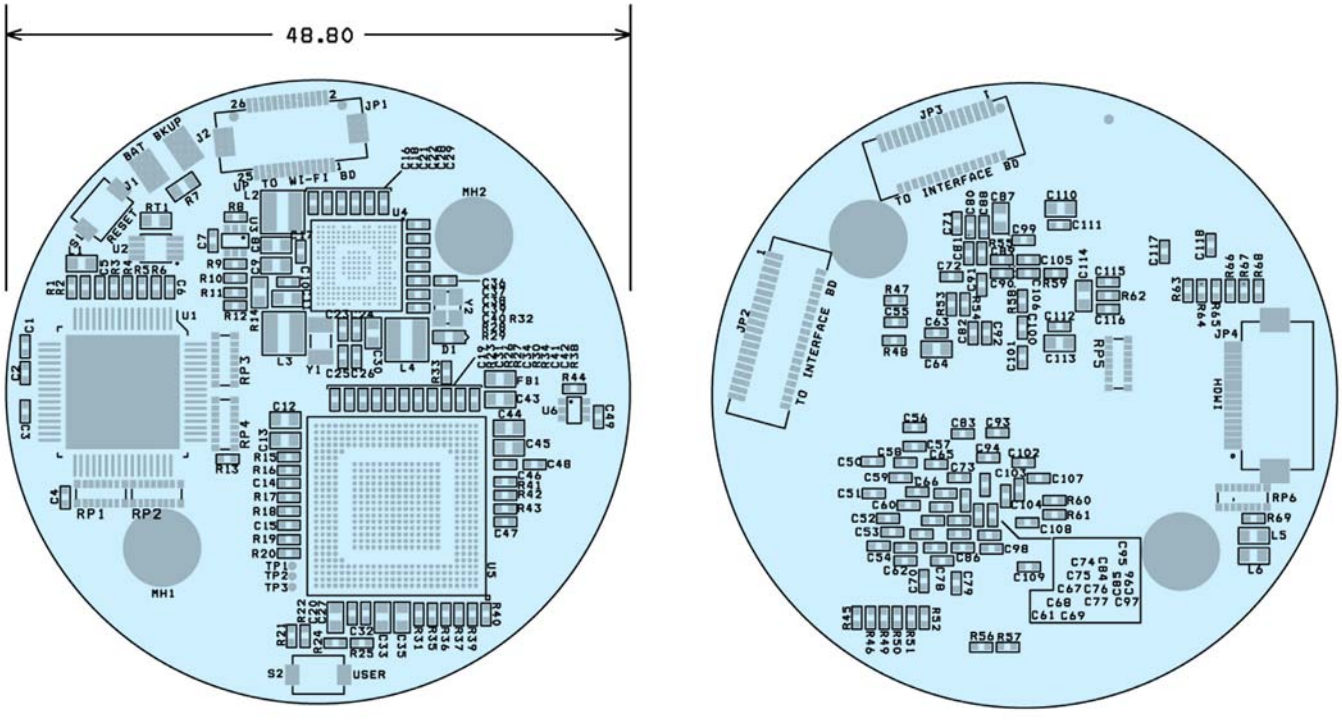

Figure 1: The tiny (less than 2 in. diameter) six-layer board for multimedia processing holds the TI OMAP processor (lower right quadrant), its companion power-management chip (upper right quadrant) that drove the stackup, and a video-processing device on one side (a) with connectors and many of the passive components on the other side (b).

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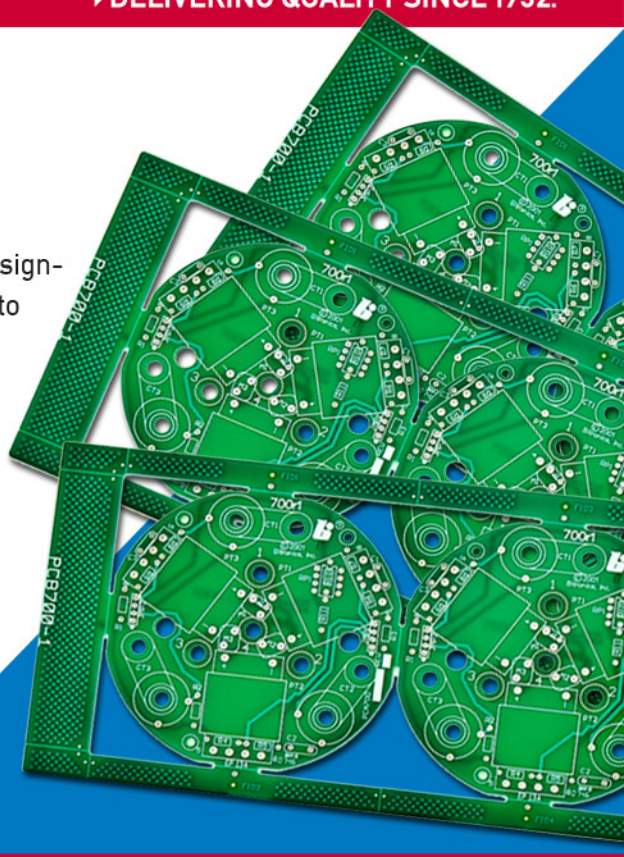

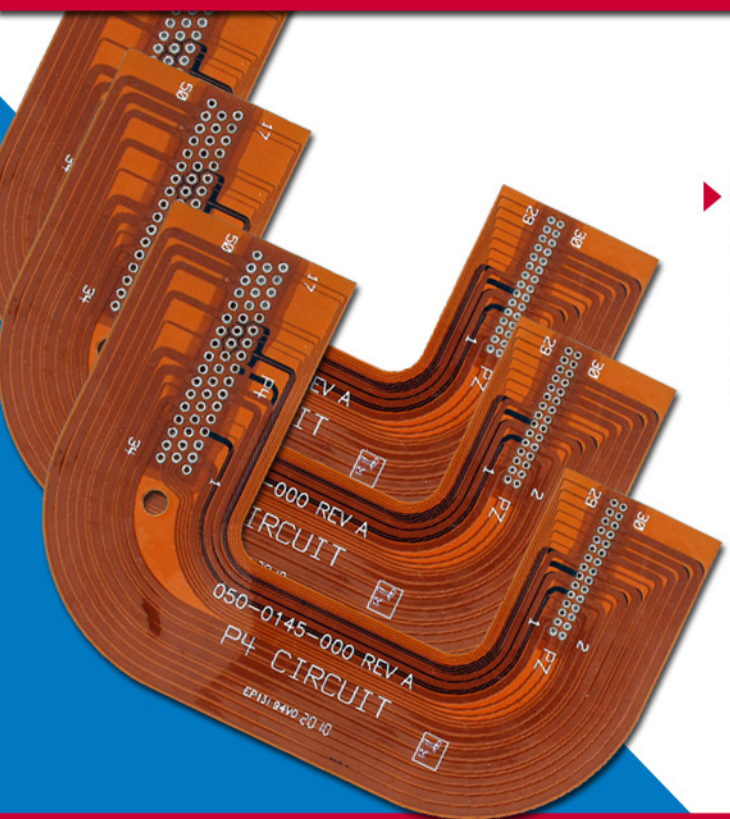

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PARTNER EARLY FOR HDI BOARD DESIGN *continues*

speed, but still use the peripherals that had been designed generations ago. There was a great deal of I/O: multiple USBs, WiFi, and much more. It was, in simple terms, a hub.

The form factor was very small, only two inches in diameter. Implementing all the required functions involved several boards in a stack spaced just 1 mm or so apart. Some of the

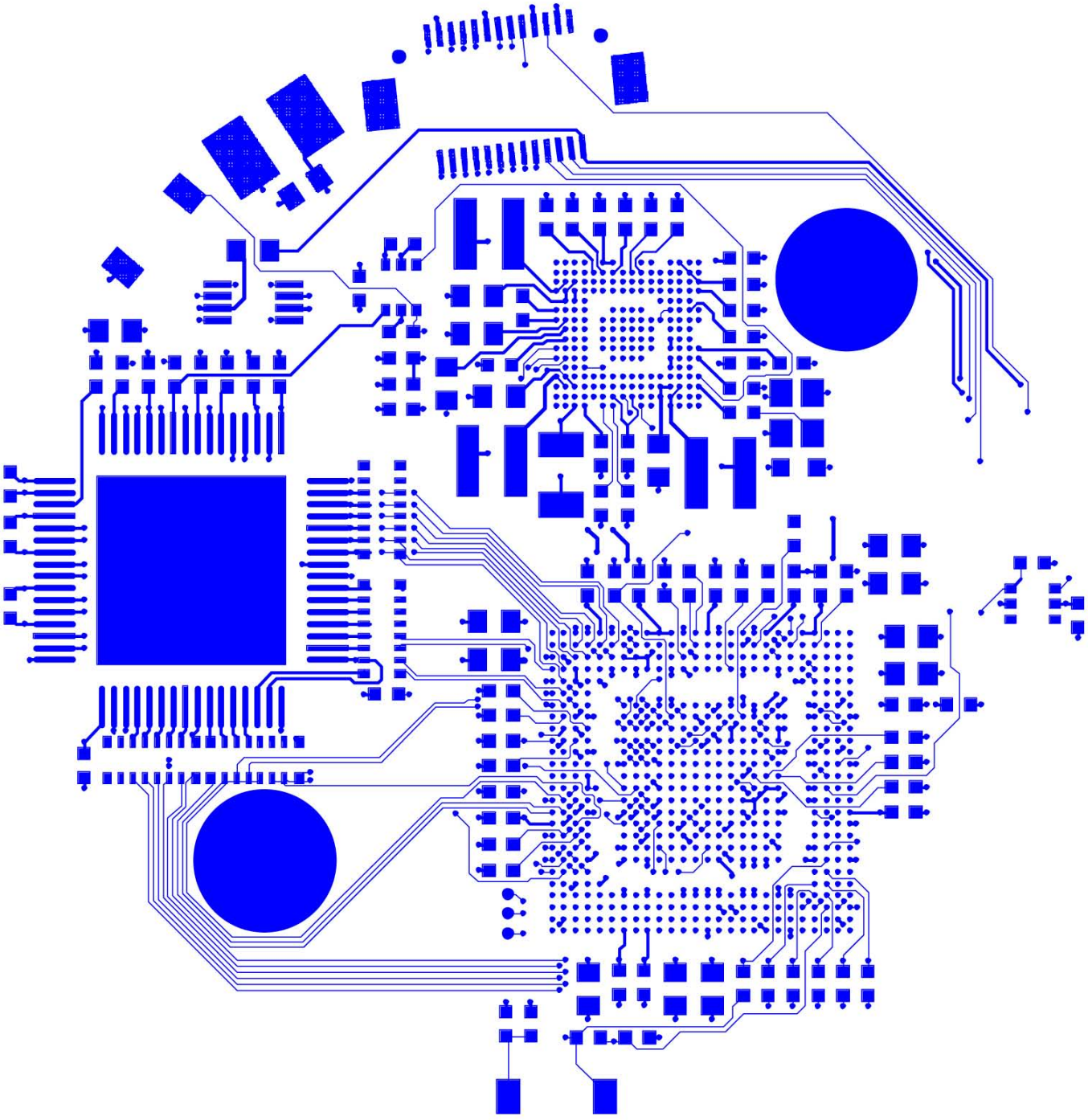

Figure 2: Routing to the inner pins of the TI PMIC could be accomplished only through microvias in the pads for the device, which has a 0.4-mm pin pitch, though top-layer traces were navigated to a few pins at the matrix perimeter.

cards were joined by board-to-board connectors; others that had tall components required a flex connection. There was an audio board, an interface board, a WiFi board – which were fairly conventional four-layer boards – and a central board designated the DSP board, incorporating the OMAP and its companion power-management chip (TPS65950), as well as a video processor.

The OMAP in this case is packaged in a BGA with pins on a 0.5-mm pitch, yet there was a more difficult routing challenge. I knew no tactics to navigate traces from inside the pin matrix of the power-management chip, which has 209 pins on a 0.4-mm pitch. Clearly, this board layout would be an education. There's no way to fan out from the center clusters of pins on such a tight pitch without resorting to vias in pads.

There are gaps among some of the pins along the matrix outer periphery through which I could fan out from some of the pins in the second row, and there is also a moat in the middle of the matrix that could have permitted me to use conventional vias for routing to some of the pins along its edges, but basically there is no practical way to get to most of the pins and route the board except for blind vias in pads. Texas Instruments agrees.

I had the advantage of an open-source design, the BeagleBoard, whose documentation includes Gerbers and the Allegro file, so I could study the via stackup stemming from an OMAP and other devices packaged in BGAs with a 0.4-mm pin pitch. And TI has some white papers with recommendations about what kind of board designs might work with this pin geometry, which describe a couple of options. But I suspect those responsible for the white papers didn't actually design such boards. It's what I call "armchair engineering." However, they do make good points:

1. The standard rules of thumb for board design do not apply when ball pitches of 0.4 mm or less are involved.
2. "Close coordination and communication between the device supplier, the PCB designer, the board fabricator, and the assembly shop is mandatory" because "fine-pitch board design is a team effort." (Reference 1)

Fortunately, I could learn a lot by essentially reverse-engineering an open-source design by which I was able to develop my via stack. Even so, that was no picnic. While I was designing the DSP board, which was eventually routed in six layers with microvias, buried vias and therefore multiple laminations, I didn't know who would build it. I took to heart the admonition from TI and other quarters to immediately open a dialog with a manufacturer. Several shops said they could fab the board, but as discussions progressed, they either couldn't do it or the way they planned to do it was too complicated. A diligent search led me to partner with Sierra Circuits, who built the board and along the way advised me how to architect it to achieve the most efficient, manufacturable design. The decision to use microvias in 10-mil pads resolved my routing issues for both the PMIC and the OMAP for that board.

The next project I landed that would involve a BGA on a 0.4-mm pin pitch progressed more easily. I sought advice from my contact at Sierra Circuits who had helped me architect the first HDI board. This project, a wearable personal communication device, was less than half the size of the other board. The prototype had to be about 1 inch by 1.25 inch and include debugging and programmer ports, but the production version would be only 0.7 inch by 1 inch. My design was consolidated in six chips, so clearly the board had to be double-sided to contain those as well as a USB interface, all the passives, and some additional elements. This was a battery-powered system, so it also needed a charger interface.

Obviously, I had to find the smallest packages available. For the MCU, my options included QFNs and the BGA I selected, whose 80 pins have a 0.5-mm pitch. The available BGAs for another device, which has only 51 pins, include one with a 0.65-inch pin pitch and a smaller one with a 0.4-mm pitch. The one with the looser pitch would not fit on the board, so I had no choice but to use the BGA with the 0.4-mm pitch, and it was that package that drove my stackup. There is a third

PARTNER EARLY FOR HDI BOARD DESIGN *continues*

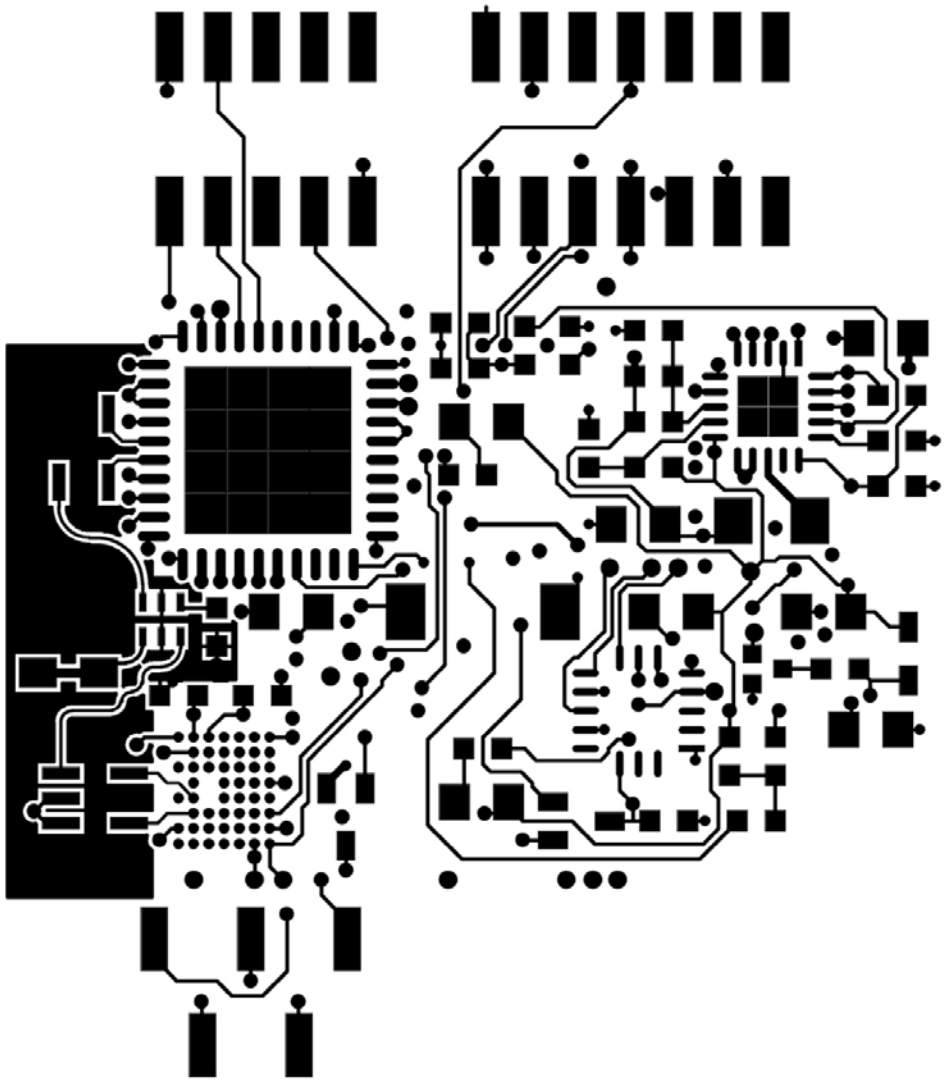

Figure 3: HDI architecture made possible squeezing six ICs – one with a 0.4-mm pad pitch – onto a double-sided board whose long dimension is just 1.25 in. The top signal layer is shown.

major component in a QFN, and I also used a QFN for my power-management device. The board also carries some flash memory in a really big package. Most of the passives are 0402 capacitors and there are two 0603 bulk capacitors.

My contact and I worked out a routing strategy resulting in a six-layer, double-sided board – signal, ground, signal, signal, power, and ground – with microvias from layer 1 to 2, 1 to 3, 6 to 4, and 6 to 5, and a standard via from layer 1 to 6. I embedded local copper pours into the inner routing layers to aid power distribution. It was manually routed, using Cadence OrCAD Layout Plus.

The scheme enabled me to put the two BGAs on opposite sides of the board: the MCU on the backside, center top, and the BGA with the 0.4-mm pitch on the topside, lower left. For the most part, I was able to keep the chips on one side of the board from overlapping those on the flip side. There was a Bluetooth chip, which made sense to locate next to the antenna along a board edge. There was a requirement to put the USB interface, which is also the charger port, in a particular spot, so that told me where to put the power-management chip.

I needed five or six different supply values for the digital devices and a supply for an analog device. Everything has a common ground. Rarely do I split planes for ground. I use ferrites and bulk capacitors for isolating the Vcc or Vdd supplies from the bulk supply running through my power plane. I prefer to route power nets last and route the top signal layer first, which completes much of the job. It's easier, I find, to nudge a signal trace to make room for a power via rather than the other way around. But if you ask 10 other people you'll get a dozen other opinions. The trick is placing components to minimize the rats' nests of routing.

Though the BGA with the 0.4-mm pitch has 51 pins, I needed only 26 of them, five of which are connected to the debug port in the proto-

type. Regarding the 80-pin MCU, six pins had no function but I routed them to a debug port just in case. The project was designed for a customer offshore who is still in development, so having those available should be handy.

Permit me to return to my issue with chip vendors. The use of HDI board architecture in my experience is driven by the presence of BGAs with a 0.4-mm pin pitch. Even tighter pitches are soon to follow. I think the companies that build the dense chips that need such packaging should have real documentation about real things that have been built with those products.

Certainly, the designers who create those chips with internal clock rates in the hundreds of MHz want to avoid compromising signals, so things are not necessarily placed in locations on the die that would result in the most convenient pinouts for customers. The evaluation boards that are provided are not usually architected for very tight packing; they're designed so customers can easily get to test and debug points.

But at the end of the day, when customers complete development and want to design boards that are as compact as possible, there is very little reliable guidance from the chip vendors. Take my advice and the recommendation from TI: Early in the HDI design process, partner with a board manufacturer who knows what to do. **PCBDESIGN**

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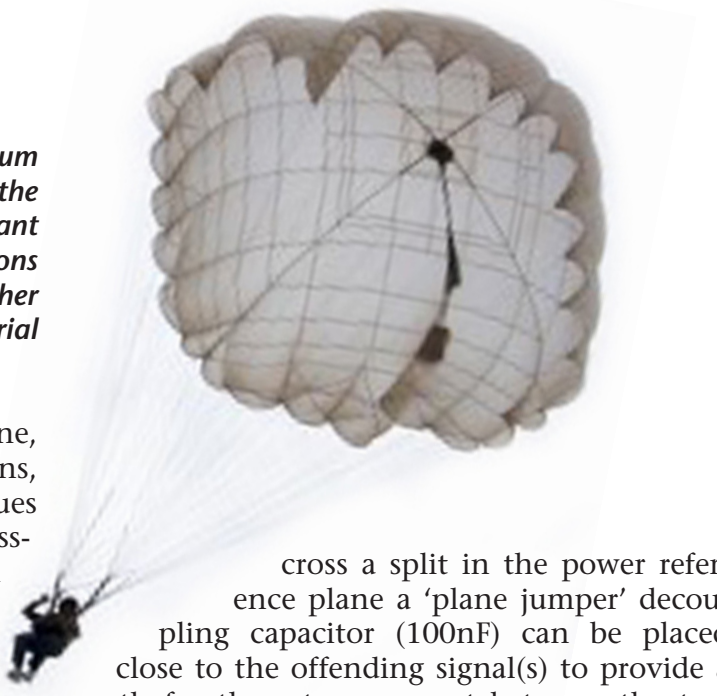
John Levreault is the president of Orvelle Technologies in Boxford, Massachusetts. He specializes in the design, development, and production of custom analog and mixed-signal products for OEMs. He can be reached via john@orvelle.com and 978-352-8235.

The Plain Truth About Plane Jumpers

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD, AUSTRALIA

***SUMMARY:** The key to building the optimum board stackup is determining how and where the return currents flow. But it is also just as important to have the board constructed to your specifications – having engineering drive fabrication – rather than delegating impedance control and material selection to the fab shop.*



Moats, islands, cut-outs in the ground plane, isolated power planes, floating ground regions, and a host of other intricate layout techniques are often used by PCB designers to reduce crosstalk, EMI, and to otherwise improve overall system performance.

But a high-speed signal crossing a split in the plane causes problems along at least three dimensions, including signal quality, crosstalk, and EMI. The problem is the impedance discontinuity in the signal path crossing the split. The discontinuity reflects energy back toward the source – particularly the higher-frequency components of the signal. At high frequencies, the return current follows the path of least inductance – which is directly below the signal trace – but that path is broken by the split. The reason for this discontinuity is the fact that the return current has to find an alternate path back to the source, creating a large loop area and a nice little antenna for differential-mode radiation.

It is important to keep in mind that both ground and power planes (any plane) can be used as the reference plane and return current path for a signal.

The key to a successful mixed digital/analog design is functional partitioning, understanding the current return path, and routing control and management – not carving up ground planes. It is always better to have just one single reference (ground) plane for a system.

I mentioned "plane jumpers" briefly in my recent column Mixed Digital Analog Technologies, where I said: "If a digital signal(s) must cross a split in the power reference plane a 'plane jumper' decoupling capacitor (100nF) can be placed close to the offending signal(s) to provide a path for the return current between the two supplies (e.g., 3.3V —||— 1.5V)."

In Figure 1, the gap totally isolates the power reference planes, so a plane jumper capacitor is used to allow the return current to bridge the gap in the planes from 3.3V to 1.5V. This is quite effective, but should be only used as a last resort, if you cannot avoid routing such a signal across the gap. I must say that it does look weird – having a decap on the schematic between 3.3V and 1.5V, where decaps are normally placed between power and ground.

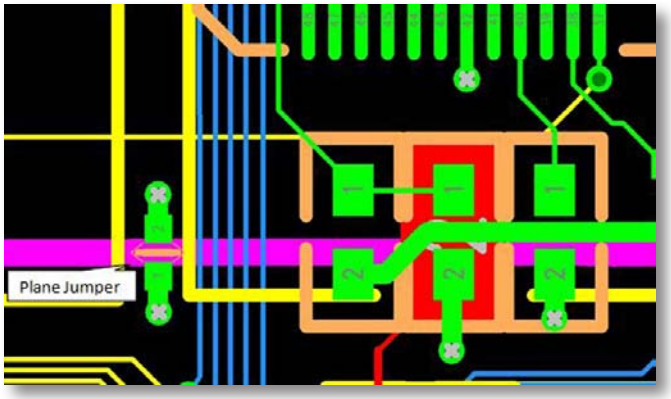


Figure 1: The return current path uses the capacitor to bridge power reference planes.

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THE PLAIN TRUTH ABOUT PLANE JUMPERS *continues*

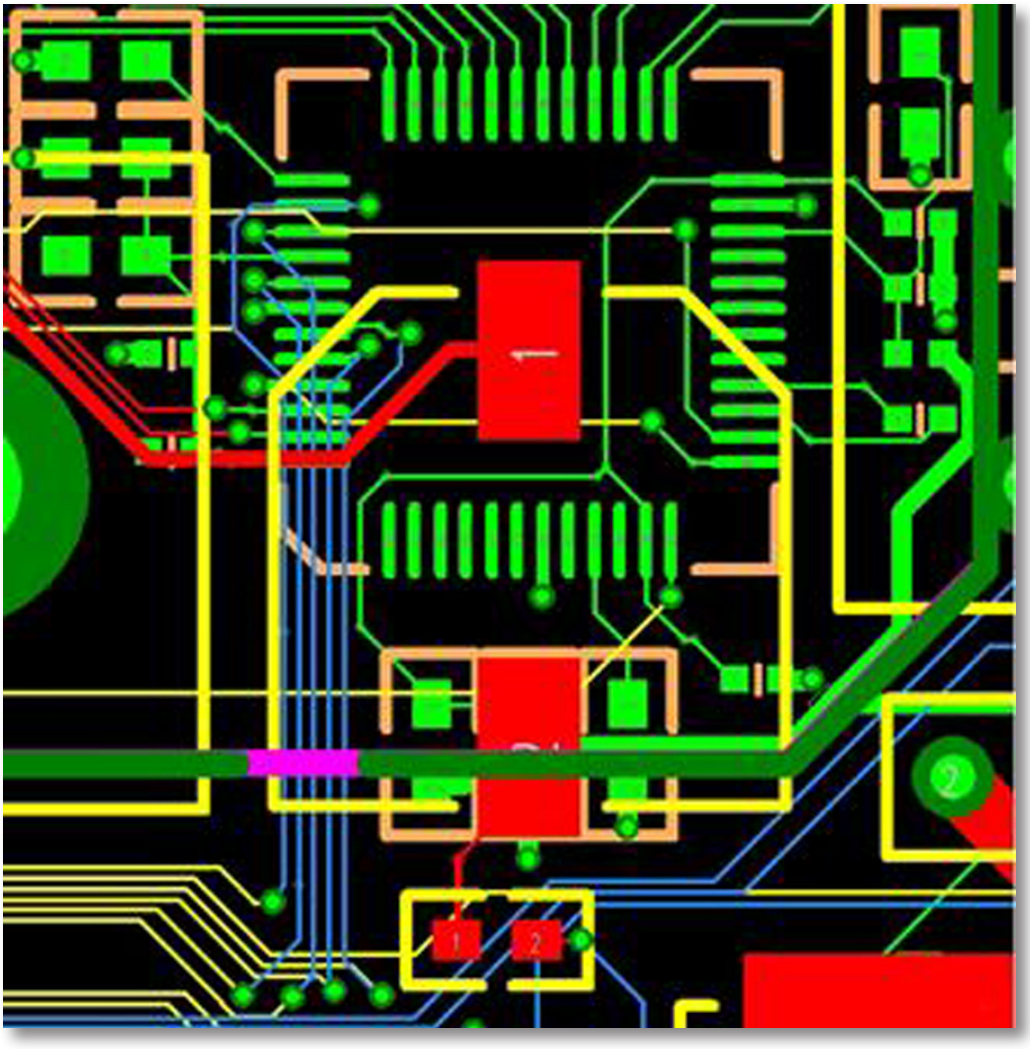

Figure 2: Control signals cross over the "bridge" of a split GND plane.

Figure 2 illustrates the correct way to tackle this situation – control signals crossing over the "bridge" of a split plane. The (blue) traces are grouped together, with a continuous ground plane beneath, providing a reliable return path for these signals. The trick is to always reference a signal to a solid plane – not to split the reference plane. The power plane can be split providing it is not used as a reference plane.

But that is the most basic use of a plane jumper. Let's look at where else in the design these magic jumpers can be employed.

ICD recently simulated a board whose

UNITS: mil — ICD STACKUP PLANNER FX – www.icd.com.au — 10/14/2012 — Total Board

Differential Pairs > SATA

Layer No	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Impedance Characteristic(Zo)	Edge Coupled Differential(Zdiff)
	Soldermask		Dielectric	3.3	0.5						
1	Signal	Top	Conductive			1.7	25	14	0.89	51.46	98.67
	Prepreg		IS FR408 ; 2116 ; Rc=56% (1 GHz)	3.7	3.8						
	Prepreg		IS FR408 ; 2116 ; Rc=56% (1 GHz)	3.7	3.8						
2	Plane	GND	Conductive			1.4					
	Core		IS FR408 ; 2-7628 ; Rc=40% (1 GHz)	3.7	14.0						
3	Signal	Inner 3	Conductive			1.4	25	7	0.47	50.78	100.61
	Prepreg		IS FR408 ; 2116 ; Rc=56% (1 GHz)	3.7	3.8						
	Prepreg		IS FR408 ; 2116 ; Rc=56% (1 GHz)	3.7	3.8						
4	Plane	VCC	Conductive			1.4					
	Core		IS FR408 ; 2-7628 ; Rc=40% (1 GHz)	3.7	14.0						
5	Plane	VDD	Conductive			1.4					
	Prepreg		IS FR408 ; 2116 ; Rc=56% (1 GHz)	3.7	3.8						
	Prepreg		IS FR408 ; 2116 ; Rc=56% (1 GHz)	3.7	3.8						
6	Signal	Bottom	Conductive			1.7	25	14	0.89	51.46	98.67
	Soldermask		Dielectric	3.3	0.5						

Plane Jumper

Figure 3: Signal current flow (red) and return current flow (blue).

designers intended to route high-speed signals from a chip to a connector on top of the board. The routing fanned out from the BGA, went directly to layer 3, then popped back up through a via to a connector on the top layer. This seems perfectly reasonable.

But looking at the stackup in more detail, the signal was first referenced to the GND plane on layer 2; then, as it transitioned to layer 3, its reference plane changed to VCC (layer 4) due to proximity. There is, in this case, only one way for the return current to "jump" planes, and that is by finding the nearest VCC to GND decoupling capacitor – which may be a long distance (relatively) from the signal transient, creating a large loop area and undesirable common-mode currents. This can all be avoided by placing a plane jumper (decap), close to the signal-via transition, between VCC and GND.

In the case, where there are multiple ground planes on a PCB, we cannot simply assume that "ground is ground" and be sure that the return current will find its way back to the source. GND stitching vias should be placed next to each signal-via transition to stitch the GND planes together, providing a clear return path.

Now, the designer had good intentions: using the GND plane on layer 2 as the common reference plane. Everything would be fine, until a lack of communication (and understanding of the design parameters) led the CAM engineer at the fabricator to change the thickness of the core and pre-preg materials to suit the dielectric materials they had in stock.

This is a classic case that we see all the time. It is the point where our design crosses over into the real world – manufacturing. It represents a point beyond which many designers rarely dare to venture, due to their lack of understanding of PCB fabrication processes. But, it is a fact that the more awareness we have surrounding the fabrication processes, the better our designs become, and the better designers we become.

The CAM professional looks at your board in purely physical terms. He, most likely, has no understanding of which signals are critical, and your current return paths. His window to your world consists of layers of dielectric materials, copper foils, PTH vias, and soldermasks. The standard Gerber file format – transferred from layout to fab – is a rather primitive (based on the old X,Y plotters) but highly effective format for describing two-dimensional graphical information. It is well suited for representing the two major components of a PCB image: lines and dots. But this is all they are to the CAM engineer.

The proverbial "left shift" in the design process is to put control of the stackup build back into the hands of engineers and PCB designers – enabling them to collaborate with, if not control, the outcome of the fabrication. To do this, designers need a comprehensive list of standard

UNITS: mil — ICD STACKUP PLANNER FX – www.icd.com.au — 10/15/2012 — Total Board Thickness: 60.5

Differential Pairs > SATA

Layer No.	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Impedance Characteristic(Zo)	Edge Coupled Differential(Zdiff)
	Soldermask		Dielectric	3.3	0.5						
1	Signal	Top	Conductive			1.7	15	10	0.7	53.85	100.91
	Prepreg		IS FR408 ; 1080 ; Rc=65% (1 GHz)	3.47	2.9						
	Prepreg		IS FR408 ; 1080 ; Rc=65% (1 GHz)	3.47	2.9						
2	Plane	GND	Conductive			1.4					
	Core		IS FR408 ; 2-1652 ; Rc=42% (1 GHz)	4.01	10.0						
3	Signal	Inner 3	Conductive			1.4	20	10	0.61	52.55	99.85
	Prepreg		IS FR408 ; 7628 ; Rc=44% (1 GHz)	3.96	7.1						
	Prepreg		IS FR408 ; 7628 ; Rc=44% (1 GHz)	3.96	7.1						
	Prepreg		IS FR408 ; 7628 ; Rc=44% (1 GHz)	3.96	7.1						
4	Plane	VCC	Conductive			1.4					
	Core		IS FR408 ; 2-1652 ; Rc=42% (1 GHz)	4.01	10.0						
5	Plane	VDD	Conductive			1.4					
	Prepreg		IS FR408 ; 1080 ; Rc=65% (1 GHz)	3.47	2.9						
	Prepreg		IS FR408 ; 1080 ; Rc=65% (1 GHz)	3.47	2.9						
6	Signal	Bottom	Conductive			1.7	15	10	0.7	53.85	100.91
	Soldermask		Dielectric	3.3	0.5						

Figure 4: The return current path now uses a common GND plane (layer 2).

dielectric materials from popular manufacturers like Isola, Nelco, Rogers, etc., and the ability to insert these into a prototype stackup, determining the single-ended and differential impedances of these materials combined with PCB layout design rules. The ICD Stackup Planner, shown in Figures 3 and 4 (available for download at www.icd.com.au) handles these tasks quite well, in fact, providing an interface between CAM, signal-integrity simulation, and PCB layout.

Since layer 3 is now closer to the GND plane on layer 2 in Figure 4, it will be used for the current return path, rather than VCC, as before. And, there is no need for plane jumpers in this case. This is by far the best scenario. The PCB designer can pass this information on to fabrication with confidence that his intended stackup build will be manufactured to suit the design's electrical needs.

Plane jumpers can be used to easily resolve a return-current issue, but they are best avoided by taking control of the stackup back into the hands of the hardware engineer and PCB designer, while streamlining communication between the hardware-engineering team and fabrication.

Points to Remember

- A split in a plane causes an impedance discontinuity in the signal path crossing the split, creating signal reflections, crosstalk, and unwanted common-mode currents that can lead to EMI problems.
- Both ground and power planes (any plane) can be used as a reference plane and return current-return path for a signal.
- It is always better to have only one single reference (ground) plane for a system.
- Plane jumpers (ceramic decaps) can provide a path for the return current between the two supply planes.
- A bridge, provided by an adjacent plane, is best used for control signals to cross a split plane.
- Plane jumpers (decaps) can be placed close to a via to allow the flow of return current from plane to plane.
- Where there are multiple ground planes, ground-stitching vias should be placed next to each signal-via transition.
- The more knowledge PCB designers have of the fabrication processes, the better the outcome of our design, and the better designers we become.
- The "left shift" in the design process is to put control of the stackup back into the hands of hardware designer so that electrical design parameters don't get pushed to the side. **PCBDESIGN**

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5. PCB Design Techniques for DDR, DDR2 & DDR3, Part 2 – Barry Olney
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7. High-Speed Digital Design – Howard Johnson
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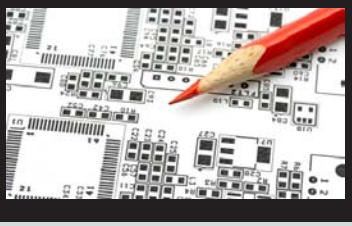
Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. The company developed the ICD Stackup Planner and ICD PDN Planner software, is a PCB Design Service Bureau, and specializes in signal integrity, crosstalk, and timing simulation, as well as EMC analysis.

Most-Read Design News Highlights



Mentor Graphics Announces TLA Program Winners

Mentor Graphics Corporation has announced winners of its 24th annual PCB Technology Leadership Awards. The Best Overall Design award went to Simon Hawkes, Mark Butt, and Kelly Perryman of UK-based Selex Galileo. Judge Rick Hartley said, "I have never given a score to a design as high as the one I ranked as the overall winner; it's just unheard of, how good that design is!"

Sunstone Launches "Share Your Story" Contest

Sunstone Circuits has launched the "Share Your Story" contest for design engineers. The contest will run through December 16, 2012, giving engineers a chance to share their PCB-related design successes online with their peers.

Intercept's Pantheon Wins NPI Award

Intercept Technology won the 2012 New Product Introduction Award at PCB West in Santa Clara, California. Intercept's Pantheon suite took home the award for the PCB Design Tools category.

DownStream Updates Post-Processing Solutions

DownStream Technologies has announced new versions of their industry-leading PCB post-processing solutions: DFMStream, CAM350, and BluePrint-PCB. The new releases will be available in Q4.

Zuken's PCB Design Suites Add Support for Xilinx Zynq-7000

Zuken now supports the Xilinx Zynq-7000 All Programmable SoCs within its CR-8000 and CR-5000 PCB design suites.

Mentor Graphics Unveils Next-Generation PADS Flow

The scalable PADS 9.5 flow enables users to cost-effectively design their products, from standard PCBs to the industry's most complex, highest performance, and densest PCBs. Enhancements in the PADS 9.5 release include the ability to switch to bottom view so the design can be viewed and modified from the bottom or top side.

ICD Releases Japanese Version of Stackup Planner

ICD Managing Director Barry Olney said, "Due to the popularity of the Stackup Planner, ICD has released a Japanese version to respond to the huge CAM market in Japan." The new release of ICD integrates the latest Boundary Element Method (BEM) 2D field solver technology into the impedance planning software to deliver the best functionality in its class.

Allegro 16.6 Addresses Need for Streamlined Solution

Allegro 16.6 accelerates timing closure for high-speed interfaces by 30-50%, through timing-aware physical implementation and verification delivered in the industry's first ECAD team collaboration environment for PCB design using Microsoft's SharePoint.

SiSoft Releases Channel Designer Kits for Intel 89xx Series

Signal Integrity Software (SiSoft) announced the availability of three Quantum Channel Designer design implementation kits for the Intel platform for communications infrastructure with the Intel Communications Chipset 89xx Series.

As a member of the Intel Intelligent Systems Alliance, SiSoft has worked closely with Intel to develop these design kits which offer ready-to-run setups, allowing designers to perform pre-route design space exploration and verify their PCB designs prior to fab-out, a huge advantage over testing physical prototypes. Quantum Channel Designer enables designers to perform post-layout analysis on all serial links, allowing designers to quickly analyze every link for voltage and timing margins.

A Chronicle of Speed and Density: The TLA Design Winners Through the Years

by Happy Holden
GENTEX CORPORATION

SUMMARY: Since 1988, Mentor's Technology Leadership Awards have honored the PCB designers working on the veritable edge of the cutting edge. Happy Holden tracks some of the trends he's seen in 12 years judging TLA designs.

Printed circuit design is a complex, challenging endeavor that often goes unrecognized. There are no university degrees in PCB design, but the skills required for modern, high-speed electronics layout and design require just as much study and lab work as a university degree. Fortunately, Mentor Graphics sponsors an ongoing program to recognize the best efforts by printed circuit board designers and organizations: the Technology Leadership Awards (TLA).

The TLA was created in 1988 by Russ Henke, then GM of Mentor's Board Station Division. For 24 years, Mentor has asked companies and individuals to submit entries that they feel are examples of the best in technology of PCB design. The electronics world has responded with some of the most challenging PCBs ever seen.

The TLA entries offer a unique look at the evolution of PCB designs over nearly a quarter century, particularly in the ever-changing areas of speed and density.

Entries are accepted for six categories of applications. This is a fluid definition that can change if new applications develop or existing categories are extinguished. The categories are:

- Computers, Blade & Servers, Memory Systems
- Consumer Electronics & Handheld
- Industrial Controls, Instrumentation & Medical
- Military & Aerospace
- Telecom, Network Controllers & Line Cards
- Transportation & Automotive

The most hotly contested categories are usually Industrial Controls, Instrumentation & Medical, Military & Aerospace, and Telecom. The majority comes from the U.S., the UK, China, and India. But 31 countries have submitted entries including Germany, South Africa, Finland, Israel, Hungary, Canada, Turkey, Singapore, Austria, Poland, Belgium, Spain, Norway, Sweden, Slovakia, France, the Russian Federation, Japan, South Korea, Taiwan, Pakistan, Italy, the Netherlands, Poland, Switzerland, Mexico, Egypt, Italy and Portugal. This list includes entries from universities in those countries.

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A CHRONICLE OF SPEED AND DENSITY *continues*

A Brief History of TLA Entries

I have been a judge for TLA since 2001, and in that time I have seen enormous changes in design complexity. Figure 1 tracks the TLA designs over this period. Each point was an entry from 2001 through 2012, with the larger triangles and squares showing the average for that year. The two diagonal dashed lines are the minimum HDI entries and the maximum through-hole multilayer entries. This is a logarithmic chart, with dispersal showing the enormous variety of entries over the years.

Figure 2 offers another way to look at these entries. I have plotted the average number of pins per square inch of substrate over the years for through-hole multilayers and microvia HDI. There has been a steady growth in the density of components from 52 (TH) and 173 (HDI) average connections per square inch in 2001 to the peak occurring in 2010 at 187 (TH) and 413 (HDI) average connections per square inch. And 2012 follows the general trend, with 180 (TH) and 330 (HDI) average connections per square inch.

The wide variations of MAX and MIN are due to the diversity of designs; typical entries range from single-sided boards to 42-layer telecom backplanes with only connectors. In 2001, only 18% of entries were HDI, but there was a steady increase of HDI entries to a level of over 40% for the last three years. HDI is also increasingly represented among the winning design, with 30% in 2001 to greater than 70% by 2010.

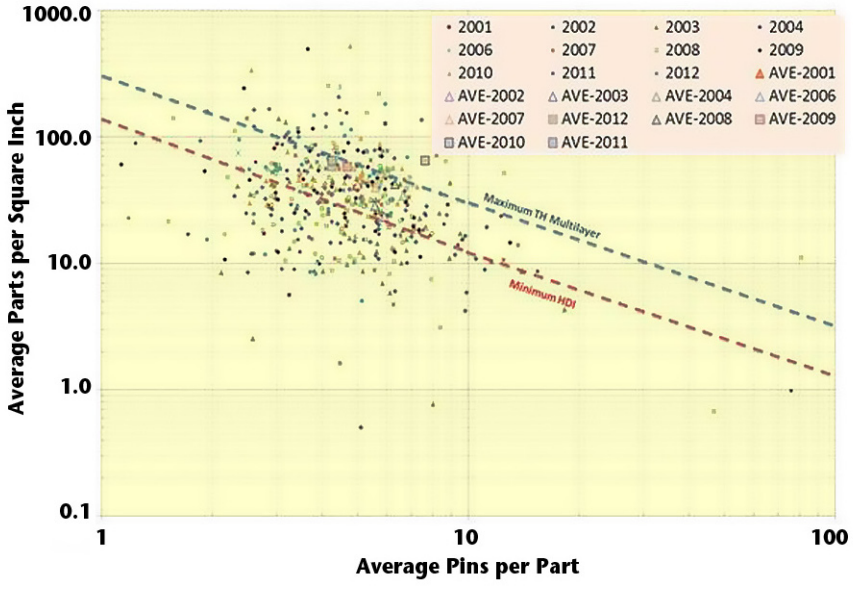

Figure 1: Individual board entries for the TLA from 2001 through 2012, with averages for each year. Shown are minimums for HDI and maximum for TH.

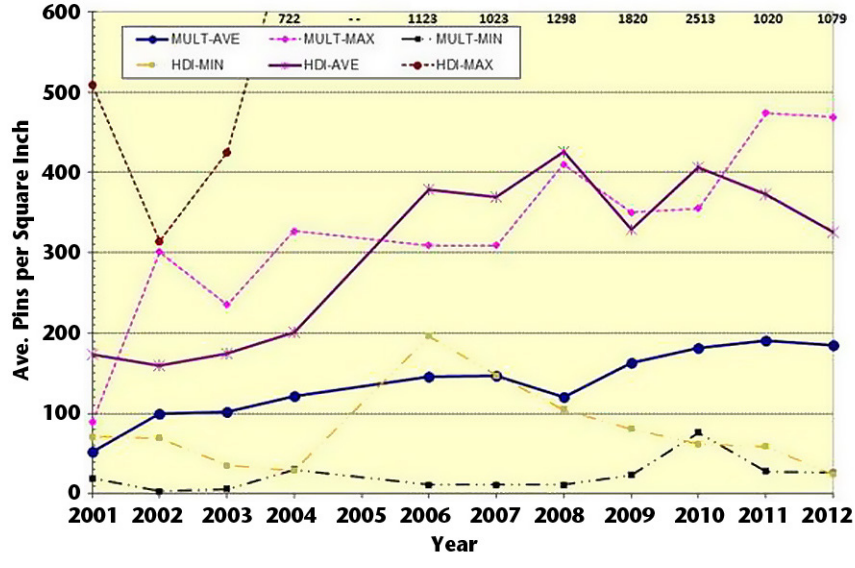

Figure 2: Average board density (in connections per square inch) for entries to the TLA from 2001 through 2012, separated for TH multilayers and microvia HDI (solid lines) with dashed lines marking MAX entries and dash-dot lines being the MIN entries.

Mentor has automated much of the technical data for submission with EDA tool scripts. These scripts collect the physical information from the design database much like a standard design report would do. Information such as size, thickness, layers, number of nets, design rules, vias, routing distances, etc., provide data needed for Mentor to create a large spreadsheet of these technical details for the judges.

Design Trend	17 years ago	12 years ago	2007	2012
Min. trace/spacing (th)	6.5/6.4	5/5	4.7/4.4	2.5/2.5
Total metal layers	8	10	16	14.3
Total area (in^2)	101	76	90	58
# Nets	1465	1544	3559	1913
# Pin-to-pin connections	5190	7661	10939	6717
# Components	649	1120	2711	2217
# Component pins	4214	5790	14666	9093
Average leads / part	18	5	5	4.2
Average leads / in^2		89	212	244

Figure 3: Entry averages from 2007 and 2012 are compared to averages from 2000 and 1995.

When screen captures of layers routed, 3D images, thermal maps, SI and PI simulations, and photos of the finished board or assembly are provided, the judges have a much clearer understanding of the challenges the designers and engineers faced, as well as their solutions. These are important parts of an entry that cannot be found in the design tool database – the problems that this team faced in terms of high-speed logic, critical nets, placement issues, signal integrity and noise challenges, as well as power integrity, PDN, thermal, manufacturing and cost issues.

The entry statistics for the 2012 TLA program are typical:

- Biggest board: 16.75" x 14.0"
- Smallest board: 2.67" x 2.11"
- Most layers: 28 HDI (5+16+5)
- Average traces/spaces: 4/4
- Most vias: 45,673
- Most nets: 8,057
- Most connections: 23,316
- Most components: 8,635
- Most FPGAs: 45
- Largest percentage of high-speed nets: 88%
- Highest passive/active ratio: 205:1

To better view some of the average characteristics, Figure 3 compares some averages of 2012 and 2007 with 2000 and 1995 entries. In 1995, clocks were around 66MHz and signals had nanosecond edge rates, and RAM averaged 64MB. DIP through-hole still predominated, but SMT was increasing. Mobile phones were just coming out and there were no HDI entries. By 2000, there were 750MHz processors with 100MHz clocks and rise times at 0.5ns. BGAs were small at 100-200 pins, and 18% were HDI.

To make the judging as unbiased as possible, Mentor removes the identity of each entry's designers. Each design is given an entry number, and until the winners are announced, judges have no idea who is responsible for the design, or even where it originated. We are, however, provided with the designers' written explanations of challenges they faced, which can be very interesting when dealing with non-English speaking design teams.

Figure 4 is typical of the drawings, figures and photos attached to a design entry. A verbal

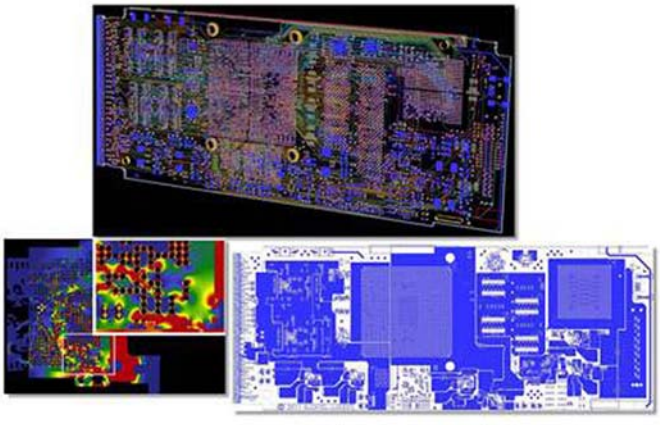

Figure 4: One of the 2012 TLA submissions featuring additional details about the power integrity of the design.

A CHRONICLE OF SPEED AND DENSITY *continues*

description is essential, as well as all the technical data and layer routings, but a finished board and a 3D image can be very helpful in putting it all into perspective!

Recent TLA Winners

To help us better gauge the caliber and trend lines of the winning designs over the years, Figures 5-10 offer a summary of the winners of the Best Overall Design awards for the last six years, followed by each team's details of the challenges associated with that design.

The 2012 Best Overall Design winner (Figure 5): Selex-Galileo's semi-active laser system:

- Complex due to unique shape and reliability concerns during use.
- Connecting two fine-pitch parts (LQFP @ 0.4 mm) without the use of microvias and large power module.
- Plated-through and cap-plated via-in-pad employed with close fabricator involvement.
- Placement and routing was done in an orthogonal fashion, then rotated to the proper 3D angle.
- EDA Tools: Expedition PCB, Dx Designer, DMS, IO Designer & Valor NPI.

The 2011 Best Overall Design winner (Figure 6): Wipro Technologies, for its single-box BTS housing transport, baseband and RF circuits:

- Digital & RF circuits – tight constraints; managed within limited board space.
- High-speed routing is done using HDI and needed strict length matching and verified using SI and timing (pre- and post-layout) simulations.
- 210 diff pairs.
- Multiple DDR3 devices.
- Serial interfaces: SGMII, SRIO-II, RP3, USB2.0.
- Power integrity: 12 major rails; 20 minor rails (lots of split planes).
- Dissipate 280W – temperature-sensitive

Figure 5: The 2012 TLA Best Overall Design from UK-based Selex-Galileo.

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A CHRONICLE OF SPEED AND DENSITY *continues*

Figure 6: The 2011 TLA Best Overall Design from India-based Wipro Technologies.

devices – resolved using heat towers & thermal ground vias
- Managed tight component & routing density while minimizing crosstalk.
- Tight DFx constraints – broad test coverage required.
- SI and timing analysis on parallel buses; SI/timing and channel analysis on SERDES/differential lines
- Power integrity on power distribution planes.
- EDA Tools: Agilent ADS – RF circuit analysis and simulations; Ansoft HFSS – 3D EM simulation for RF resonance analysis; Flotherm – board-level and system-level thermal simulations; Valor – DFx review; XtremePCB – Concurrent PCB layout work.
- Concurrently, designers were working on the single database across different locations. We were able to change/modify the constraints online and work on different sections. Since the data is updated dynamically, all the designers were able to see the progress and plan accordingly.

The 2010 Best Overall Design winner (Figure 7): General Electric Intelligent Platforms' SBC612 rugged 6U VPX single-board computer:

- Aimed at high-performance mil/aero applications. 6U form factor.
- Complexity: 3,500+ nets; 20,000+ connections; 11,600+ vias; total 20 BGAs placed on both sides – several quad flat packs with 0.4mm pitch also used.
- Thermal management: Processor was low power (30W), but still needed to be placed close to a cold wall due to operation at temperatures up to 85°C. All components had to be rated for -45°C to 85°C for ruggedization.
- Mechanical: Mezzanine plug-in cards dictated low profile placement regions.
- Buried vias: Reduced buried via pairs to cut costs, which increased routing challenge.
- High-speed signaling: Serial Rapid I/O, PCI-X, DDR3 – significant constraints with tight tolerances. Placed solid continuous ground layers on either side of over 500 diff pairs to minimize impedance discontinuities.

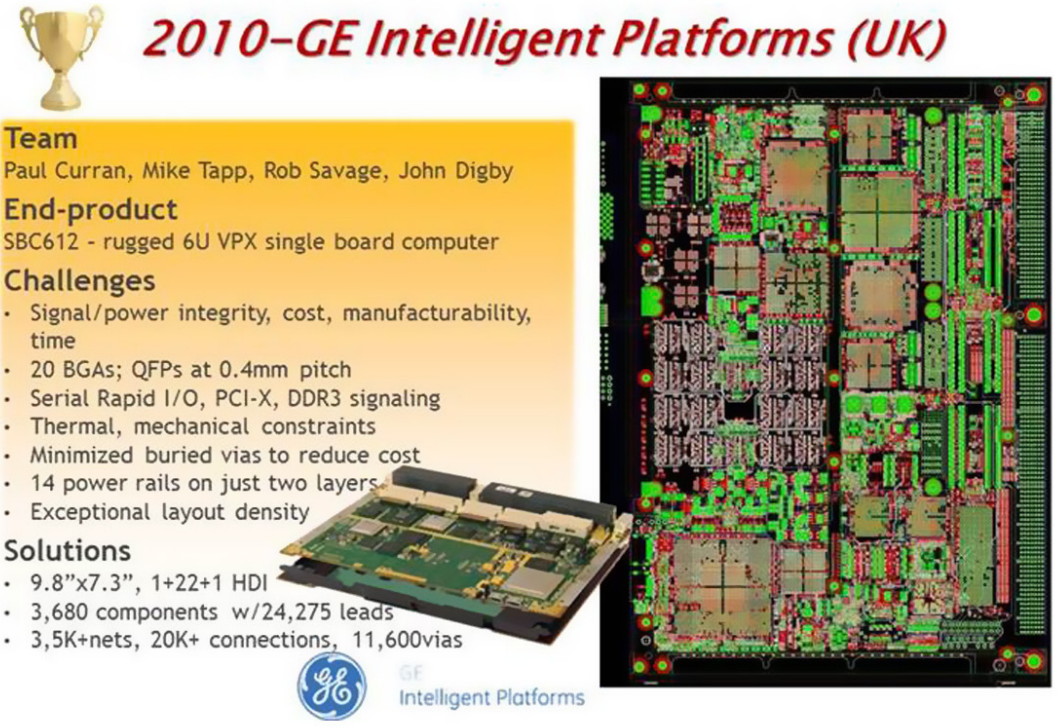


Figure 7: 2010 TLA Best Overall Design, UK-based GE Intelligent Platforms.

- Power: Managed trade-offs between power consumption and thermal management. Ensured that the PCB could deliver the required 30A current.
- Significant effort taken in placement to ensure thermal efficiency, effective power delivery, and sufficient routing channels including tuning space.
- 14 power rails placed on two internal layers shielded signals from power noise with ground plane on either side. Manually increased power trace widths wherever possible to increase current capacity for critical devices.
- The stackup created for this design has been successfully used for other designs and has become the new standard. Design was completed two weeks under schedule.
- EDA tools: Expedition PCB; I/O Designer: The major design challenge was routing the processor and connecting components. Because the number of routing channels and layers was limited, it was important to reduce the number of crossover connections between the devices. I/O Designer was used extensively to manage the unraveling of these connections. By maintaining consistency between the PCB and schematic data the team could quickly perform the necessary pin-swaps to optimize the routing without compromising the FPGA internal design.

The 2009 Best Overall Design winner (Figure 8): Tellabs Operations, for its sonnet switch module for an optical transport product:

- Tight timing margins requiring extensive constraint formulas – with tons of diff pairs, ground shielding and curved traces.
- Constraints evolved as the layout was underway.
- 120+ power rails supplying filtered power throughout the design.
- Time constraints, so two layout designers worked simultaneously with XtremePCB. Also worked concurrently with engineering.
- EDA tools: ExpeditionPCB, XtremePCB, CES, DXDesigner, FablinkXE. The use of XtremePCB and cluster attributes to group

A CHRONICLE OF SPEED AND DENSITY *continues*

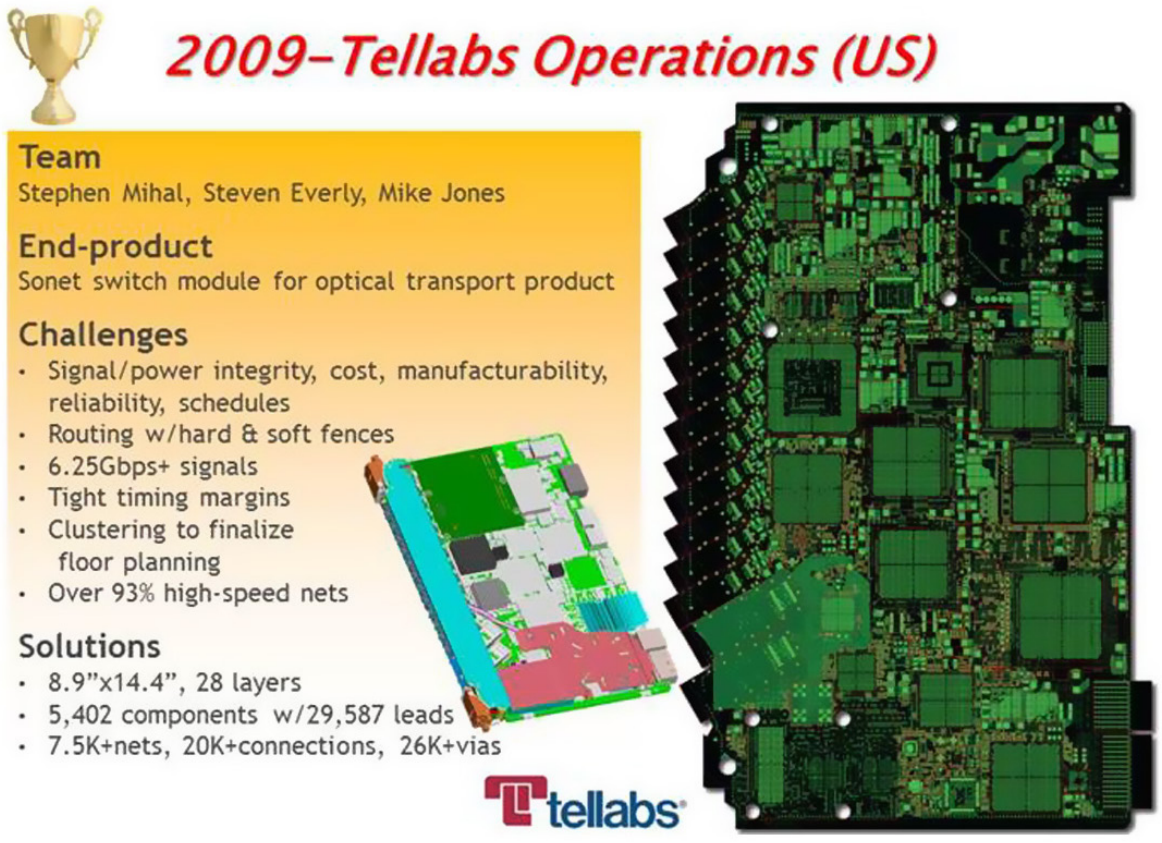


Figure 8: 2009 TLA Best Overall Design, U.S.-based Tellabs Operations.

components quickly to finalize the design floorplan, and the ability to cross-probe between the design and schematic or CES database was crucial to our success. We utilized XtremePCB to double-team during the entire layout design phase, including floorplan, placement, fanout, defining power layers, routing and trace tuning. During the layout phase we maintained a design source for engineering changes, and if running XtremePCB was not feasible we worked through design copies and utilized the export/import functions to work in tandem throughout the floorplan and placement phase. This was instrumental in reducing the time-to-market of this product. Concurrent design techniques were followed which allowed for seamless engineer changes to the design; HyperLynx Simulation was run to model design considerations. Static signals were autorouted using both hard and soft routing fences.

The 2008 Best Overall Design winner (Figure 9): Alcatel-Lucent, for its optical router telecom switch module:

- Blind vias, eight power planes, two 4-layer TH MULT laminated to a 10-layer.
- 4/4 geometry, 0.010" FHS with 18:1 AR.
- Signal and noise problems for 1,900 high-speed nets.

The 2007 Best Overall Design winner (Figure 10): Siemens, for its reconfigurable FPGA-based signal processing platform on PCI-X (1.5 TeraMAC/s):

- According to Xilinx, this is the most powerful signal processing board in the world. With 16 Virtex 4 SX55 (BGA 1148 pins), DDR2-533 DRAM (BGA 0.8 mm pitch).

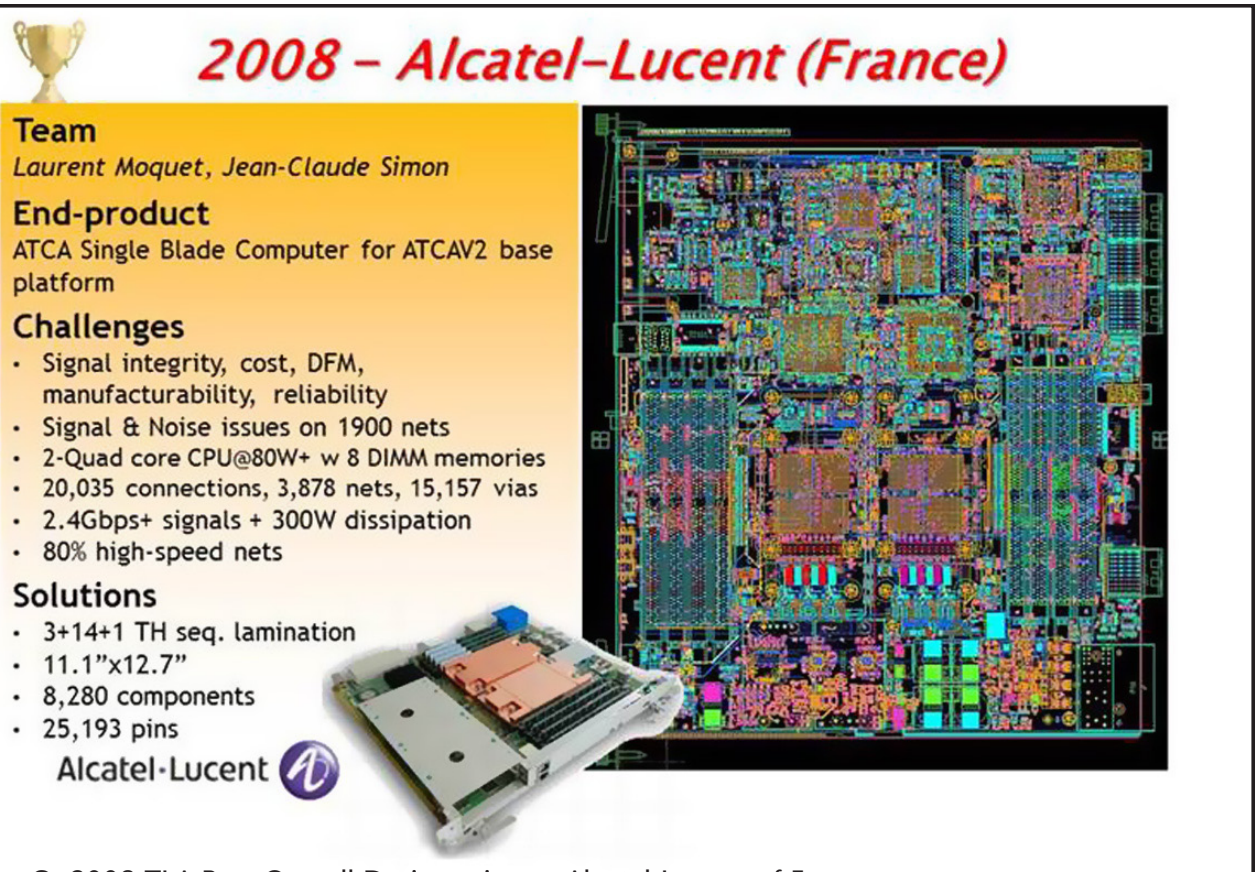


Figure 9: 2008 TLA Best Overall Design winner, Alcatel-Lucent of France.

- Board dimensions and board thickness is limited to the PCI-X standard. The manufacturer was undefined at project start, so we needed a very common PCB technology definition. Huge estimated power dissipation (220W, 100A@1.2V, 30A transients) requires thermo simulations.
- One of the challenges was the time schedule; we had only 10 weeks for the first layout.
- All 16 FPGAs on the board had to be connected to the 128-bit cascade bus and each FPGA had its own DDR2 memory bus.
- PCI specification allows a maximum of 1.6 mm board thickness, and it was very difficult to keep the layers low! Each FPGA also has to be connected to four DDR2-533 DRAMs. Each section of the buss had 3,406 high-speed nets.
- The system performance went down badly when we added the power layers and area fills, so we decided to switch from Solaris to Linux computers and to use a faster HW platform.
- When we started our design, the Mentor I/O-Designer did not support the Xilinx Virtex-4, so an experimental patch was added. To avoid voids during the soldering process, we found a completely new solution to via-in-pads by placing the microvias concentric to the BGA pads.
- EDA Tools: Boardstation, HiSpeed Option, Boardstation RE (partially autorouting, fanout generation), HyperLynx; AutoTherm, 3D Thermal analysis (FloTherm/Flomerics); Power integrity (PowerSI/Sigrity).

Challenges of the Future

A study of TLA design winners reveals several trends. More functionality is being supplied by semiconductor integration, with ever-in-

A CHRONICLE OF SPEED AND DENSITY *continues*

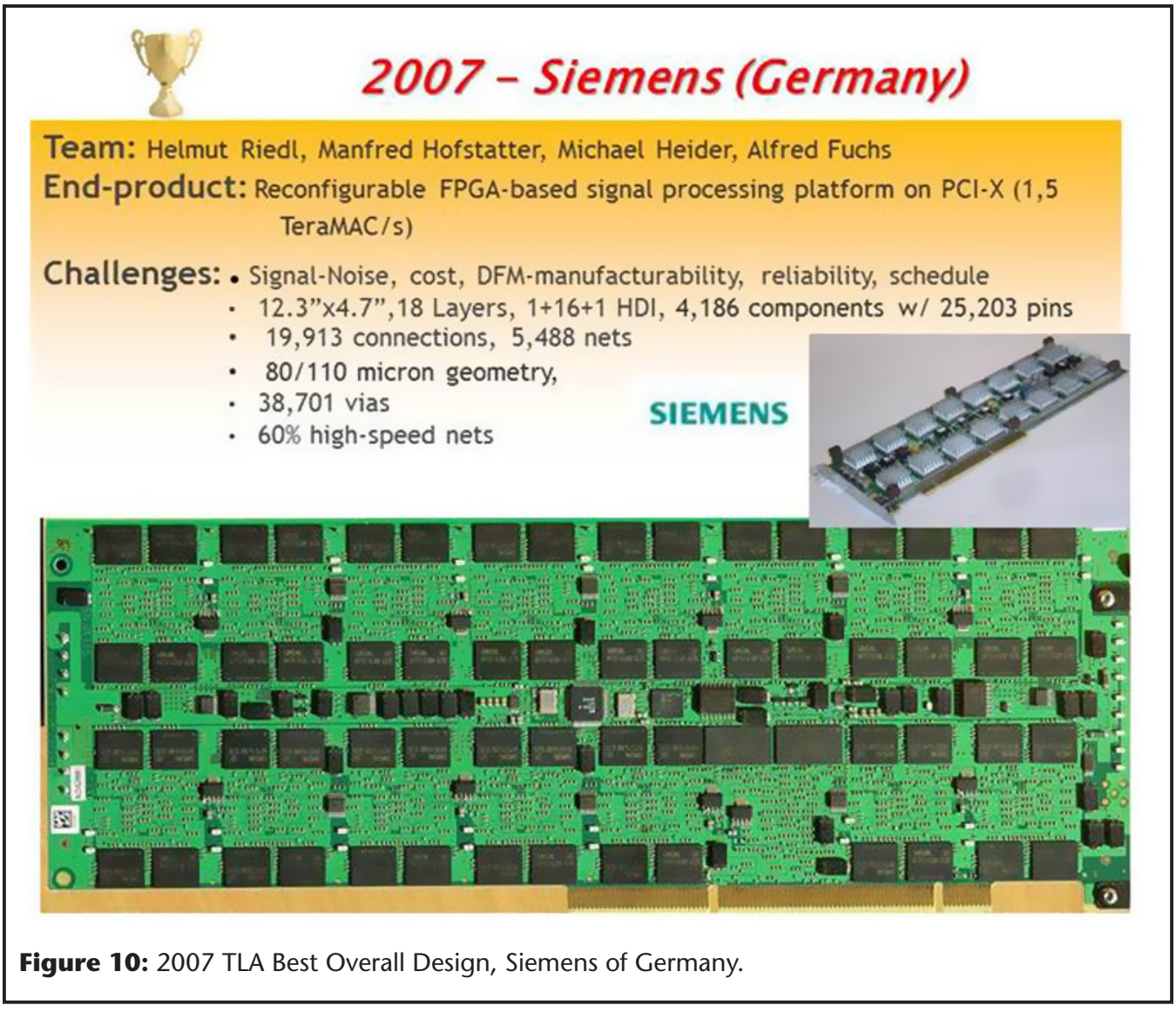


Figure 10: 2007 TLA Best Overall Design, Siemens of Germany.

creasing finer-pitch BGAs featuring more pins, busses and memory channels with their associated problems of signal and power integrity, and more passives, with thermal and manufacturing issues. Time-to-market pushes schedules, while cost controls are driving more design planning and DFM. Fortunately, there seem to be more simulation tools being used to optimize designs and solve tricky problems.

How does your work compare? If your designs are challenging, or if you have a more innovative solution to these design challenges, then you should enter the Technology Leadership Awards next year. There are few programs that show the work of our best PCB designers and engineers, while recognizing the best designers for that work. For information about the 2013 program, click here.

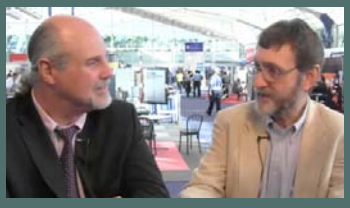
I hope to see one of your designs next year! **PCBDESIGN**

Happy Holden, "Mr. HDI," is Director of Electronics Engineering and Innovations at Gentex Corporation and a veteran PCB technologist and author. He can be reached at happy.holden@gentex.com.

video interview

Hartley: Design Education is Your Responsibility

by Real Time with... Designers Forum



Guest Editors Kelly Dack and Rick Hartley go over Rick's Designers Forum message regarding who is responsible for a designer's education. Rick makes a great point: Education is empowerment, but it is up to you, not your company or anyone else, to make sure you are educated! Like many successful designers, Rick has never allowed his education to be snuffed by a company's lack of training budget and he minces no words when explaining why.

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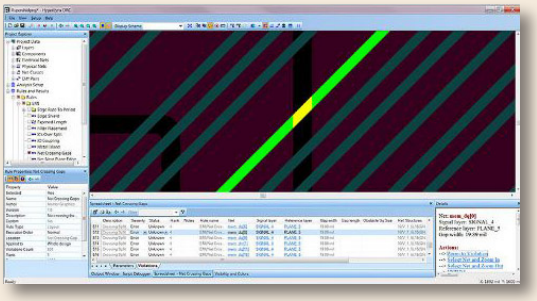
Mentor Graphics Expands HyperLynx Suite

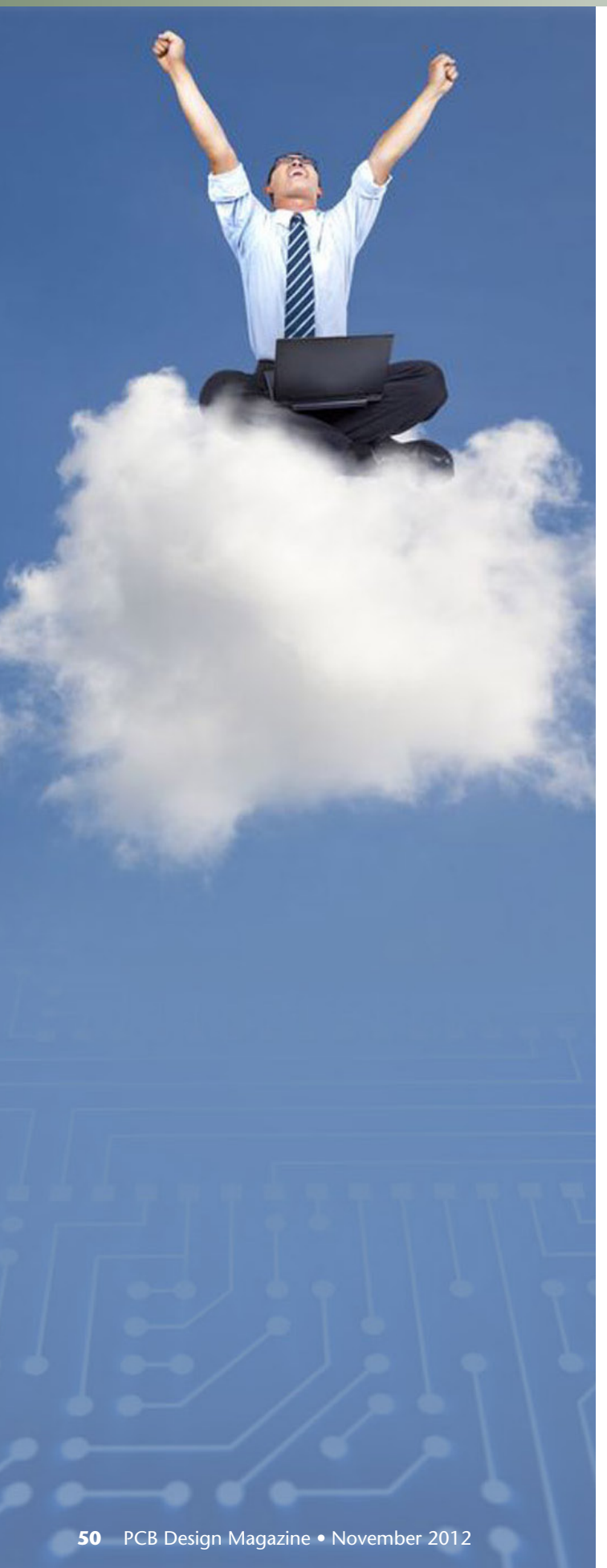
Mentor Graphics Corporation has released a major new product in the HyperLynx suite, the market-leading, high-speed analysis product line.

HyperLynx DRC efficiently performs best practice design rule checking (DRC) on PCB layout databases. Driven by customizable rules, the HyperLynx DRC product can be executed by engineers and designers during the PCB layout process to quickly highlight potential high-speed design issues pertaining to signal integrity, power integrity, and EMI, without running detailed, time-consuming analysis. Not only will designs be of improved quality, but correcting problems earlier in the design process can avoid re-design and shorten time-to-market.



One example: Sony Mobile, based in Lund, Sweden, is faced with very compressed engineering schedules to reach time-to-market windows in the mobile phone market. To ensure design quality, Sony Mobile performs design reviews to identify electrical issues related to signal integrity, EMC, and power integrity prior to building a board; however, these review meetings can be very time consuming.

"By using HyperLynx DRC we get a structured approach where all nets are equally checked by the tool. We can then focus the review meeting on the critical nets where the tool finds the violations," said Anders Olsson, senior manager, Lund Development–Electronics System Design at Sony Mobile. "Valuable time can thus be spent on problem solving instead of problem finding. This makes us more efficient in our design process, extending our review coverage, and ensures higher design quality for our customers."



Leveraging the Cloud for Automated DFM

by Iain Wilson
IRON ATOM

SUMMARY: ***Significant advances in PCB pre-CAM with automated DFM solutions now offer unprecedented levels of automation and advanced features. Cloud computing is an enabling technology offering a new way for users to access business-critical processes like DFM. In 10 years, users will be accessing business-critical applications on a browser via a Cloud-based provider.***

We know that optimizing a PCB design prior to manufacturing speeds time to market and minimizes time-consuming and costly rework cycles. With the advent of Cloud computing, powerful pre-CAM solutions can be leveraged in a new way to provide a quicker, easier and more cost-effective way to ensure designs are ready for the manufacturers. This article will explain how Cloud computing and pre-CAM software have been married and are now accessible to everyone, regardless of company size or capital.

DFM: What's Not Working Today

At PCB West 2012, I attended a seminar titled "A CAM Engineer's Perspective on Improving the CAD-to-CAM Flow." The presenter made a sincere effort to educate the audience on making the CAD-to-CAM (or design-to-manufacturing) flow smoother, quicker and with minimal errors. A significant portion of the seminar was dedicated to the topic of DFM.

The speaker offered numerous tips and advice on typical DFM issues that caused delays prior to manufacture. These issues required the job to be put on hold while the issues were resolved and often required some design rework. While listening, I reflected that these were the same issues I dealt with as a PCB CAM engineer 20 years ago.

In short, nothing has changed.

That begs the question: If it's to everyone's advantage to have the DFM bugs ironed out first, how come we, as an industry, still have to hear tips on how to prevent issues that should not, by now, be an afterthought? Shouldn't there be a solution that becomes part of the natural flow and can be adopted by anybody, regardless of the size of the company and their financial means?

Certainly, there are numerous DFM products available today. Most are very good at what they do. They range from relatively affordable, downloadable desktop applications to high-end, sophisticated (but expensive) solutions integrated with CAD tools.

Yet, the majority (if not all) of these products suffer from these problems:

- The implicit approach that designers will actually run DFM tools. Some will and some won't.
- Designers will focus on completing the design. This is rather obvious, of course, but it needs to be stated.
- Manual DFM tools are only as good as the user. They require product knowledge to get the best out of them. Unless used frequently, time will be required to refamiliarize with the product.
- Manual DFM takes time, which designers don't necessarily have. I'm sure they are itching to get working on the next design.
- Effective interpretation of the DFM results requires manufacturing knowledge.
- The automation provided by the more expensive tools is unavailable in the cheaper ones. The less you spend, the less you get.

A new breed of DFM solutions in the form of pre-CAM and recent advances in worldwide IT infrastructure (specifically, the Cloud) has opened the door to improvements that were impossible, until now.

The Emergence of Pre-CAM

Fabricators' need to get design files loaded and checked as quickly as possible has driven CAM vendors to develop a dedicated solution: Pre-CAM. You've likely heard of CAM, but these pre-CAM tools offer the following key features:

- Automated input, using some method to automatically load multiple file sets.
- Automated file recognition of PCB CAD system outputs, e.g., Gerber files, ODB++, drill files, netlists drawings, etc.
- Automated layer ordering. The correct sequencing of all the various PCB layers including pastes, legends, masks and the copper layers, of course.
- A CAM system engine.
- Automated DFM processing.
- Automated CAM tasks. The ability to perform standard CAM tasks, like unused pad removal, increasing soldermask clearances to minimums.

These tools crunch through design files like there is no tomorrow. Most file sets pass through completely automatically, or require just a nudge of information confirmation. Fabricators can use these types of tools up front at the quotation process. It's hugely advantageous for them to know critical manufacturing criteria: layer & drilling structures; minimum lines, spaces, annular ring; SMD pad density…these are the factors that drive the cost of the PCB and can determine the required tooling and manufacturing processes. If the quote is won, a significant amount of the front-end work is already done, reducing the load on the engineering

team and total engineering time required, thus getting the board into manufacturing quicker.

You may be thinking, "Where can I get my hands on one of these things?" Notice the word "automated" in my bullet list above. These tools are highly sophisticated, incorporating years, even decades, of industry knowledge translated into algorithms and computing processes. This kind of technology doesn't come cheap. Further, these tools required processing power – a high-end workstation or server – which means $$$.

> ***To us, Cloud computing is a new way to look at hardware, network and software resources that lets people develop, or use, better and more scalable software for significantly less money.***

The Traditional (On-Premises) Software Business Model

Certainly those who can afford pre-CAM will buy it. But what about light-to-medium users, smaller fabricators, and designers? The traditional model for business or engineering solution of buying the software and hardware is not a good fit for pre-CAM or other sophisticated (read expensive) solutions. Here's why:

- The up-front cost can simply go beyond the budget.
- Inevitable software maintenance fees add recurring cost.
- Pay-as-you-go schemes cost less to get going but cost the same long-term, and can ultimately cost more.
- Hardware and associated IT support add more cost.
- Users need to be trained, costing more time and money.

So, what to do? Let's look to the skies…

Cloud Computing

The ubiquitous Cloud is the software industry's latest big thing. In software, anyone who is anyone is either heading to the Cloud, or wants to (because they need to). If not, someone's going to take their place. Cloud computing offers a financially compelling model for access to computing power, software applications and data storage. There are many well established companies offering pure Cloud computing today.

You've likely heard of Salesforce.com, a venture that initially provided a Cloud CRM (customer relationship management) offering (notably, their slogan is "No Software!"). They have since gone on to expand into services, marketing, social networking and HR. They also offer a platform where a user can build custom applications to ensure a good fit into a particular market. There are many other companies offering Cloud solutions: SAP, Oracle, Google, and Microsoft, to name a few. Perhaps surprisingly, Amazon.com is considered the world's most important Cloud company today.

So what is Cloud computing exactly? I'll start by saying what it's not: 1) The Internet, and 2) A website. Certainly, the term Cloud is being bandied about all over the place. Many companies are misusing the term by slapping Cloud onto their Internet product offering. OK, I suppose it doesn't really matter for all intents and purposes – the Cloud is the catchword of the day and most end-users don't really care.

Wikipedia describes Cloud computing as follows: "Cloud computing is the use of computing resources (hardware and software) that are delivered as a service over a network (typically the Internet)."

To us, Cloud computing is a new way to look at hardware, network and software resources that lets people develop, or use, better and more scalable software for significantly less money. How is this possible? Well, if you look at an Amazon Web Services (AWS) proposal, you will see that they offer computing power for rent and many other products that tie into this. Specifically, they rent the use of one, 10, or 100 servers, that they own and maintain, for a certain per-hour cost which depends on the hardware specs required by the user.

For instance, a dual-core, 4GB server will

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LEVERAGING THE CLOUD FOR AUTOMATED DFM *continues*

cost a few cents per hour while an 8-core, 16GB server will cost a few cents more. For this fee, you get premium hardware, patched OS, and the ability to run in a highly secure environment for which you had to do precisely nothing. No up-front costs, no IT personnel, and no continuous maintenance: Nothing.

Users get load balancers, firewalls, message queuing software as part of the per-hour cost and, in practical terms, an infrastructure that lets you build software that can scale massively, without prior investment.

Cloud software takes advantage of all these new capabilities and makes all those hardware and software infrastructure parts cooperate. This new type of software is engineered to run in the Cloud and is not the old website-based or browser-based app. It's way more: Cloud software runs with an infinitely scalable backend, and it was designed to take advantage of all those elements. Very little software is specifically designed for the Cloud today.

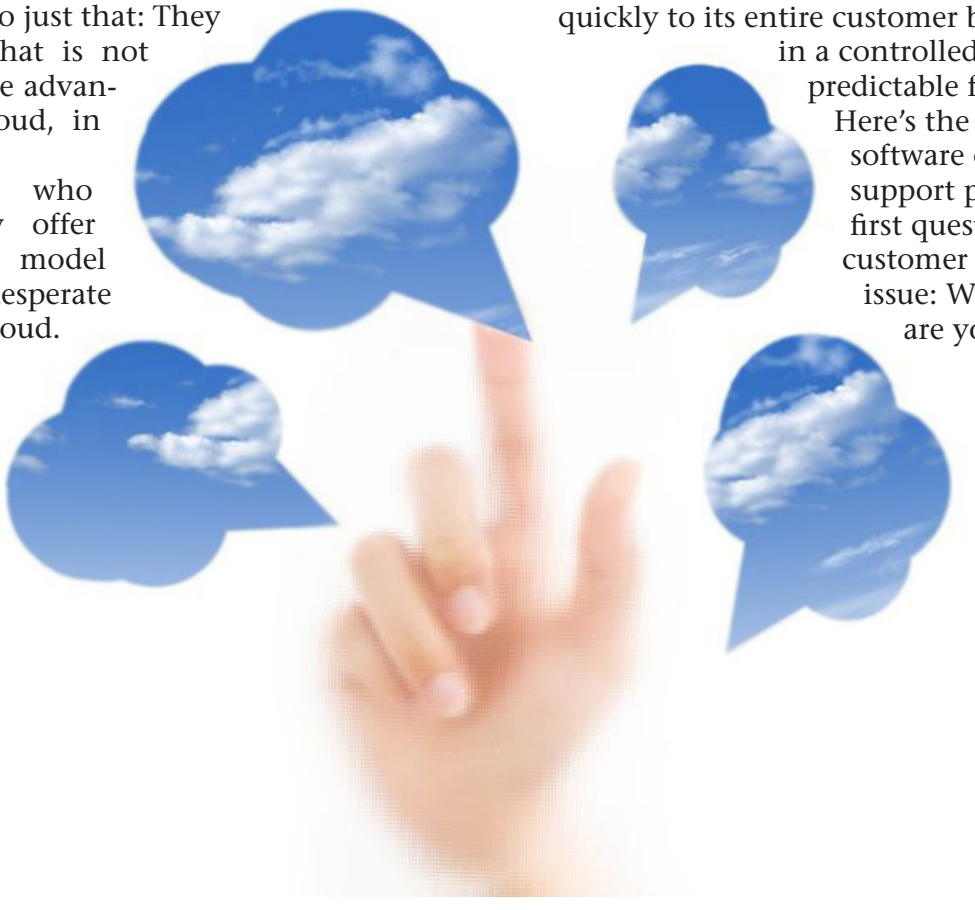
While many vendors stamp their software with the label "runs in the Cloud," most of them do just that: They run software that is not designed to take advantage of the cloud, in the cloud.

Companies who currently only offer the traditional model solutions are desperate to get to the Cloud. If you ask them if it's on their roadmap, most will assure you it is. Or if it's not in the roadmap, then they will likely espouse "security concerns" (more on that later) or some other excuse.

Here's a question to consider: "Do organizations want to spend any time, money and resources maintaining software, hardware and networks to support business-critical applications, or just have users access them with a browser?"

So, why are business-software companies so eager to migrate their traditional, on-premises product to the cloud? Here's three key items:

- Instant customer access to their product.
- Customers don't require new hardware, OS licenses and all the associated IT time and costs – it's cheap and easy to begin.
- The software company can maintain its software; new patches, service packs, new releases, new modules and new features can be applied easily and quickly to its entire customer base in a controlled and predictable fashion. Here's the de-facto software company support person's first question to a customer with an issue: What version are you on?



Traditional software companies can only make fixes available to their customers. Most software users do not run the latest and greatest, and some even neglect to apply critical patches. I don't have a concrete figure at hand, but after working for a traditional software company for 16 years, I can say that supporting multiple versions of a product was probably our single biggest workload. Software upgrades put a burden on the end-user too, of course.

Cloud Security

A very common reaction to a discussion on Cloud computing is, "Is it secure?" My perhaps trite response is usually, "It's at least as secure as your e-mail server or FTP site, but likely several orders of magnitude greater."

Cloud providers are, of course, extremely conscious of security concerns. It's fundamental to their success. There have been many news stories during the last few years about companies suffering from data breaches and having critical information stolen. Some of these stories related to poor software implementation (e.g., clear text passwords sent over the network) while others could be linked to an improper infrastructure setup (e.g., firewalls not in place or not restrictive enough, unpatched SSL implementations, missing OS patches).

While the Cloud provider cannot help a user write better software, it can certainly ensure that the software platform is rock solid. In other words, more than half the equation about security (the more complex and ever-changing part) is handled; the user need only focus on software.

For instance, Amazon's internal security policies could be seen as straight from a sci-fi movie. Employees cannot access any of the AWS servers without authentication, and the authentication is always bound to a real person. Logging-on goes from the server they work on to the office door they opened. User names and passwords are never shared. And when I say "the server they work on," I mean one of their servers, for their jobs. They cannot ever log onto a rented server without permission, since they have no way to access passwords. Only you have that information. When a computer is thrown away, the hard disks are demagnetized and shredded to pieces so that none of your data can ever be recovered.

While the Cloud provider cannot help a user write better software, it can certainly ensure that the software platform is rock solid. In other words, more than half the equation about security (the more complex and ever-changing part) is handled; the user need only focus on software.

For more information on security, Amazon.com AWS outlines its multipoint security strategy, click here. Amazon also features a special zone that meets the requirements for ITAR-controlled data, available here.

Cloud Computing Meets Pre-CAM DFM

Significant advances in PCB pre-CAM with automated DFM solutions now offer unprecedented levels of automation and advanced features. Cloud computing is an enabling technology that offers a new way for users to access business-critical processes like DFM and new markets are opening up for software vendors who can offer on-demand usage of their sophisticated and expensive products to those who can't afford to buy them or only need ad-hoc or light-medium usage.

There are, in fact, already Cloud-based pre-CAM applications available today, so go check them out. Stick around another 10 years and you will likely be accessing most, if not all, of your business-critical applications on your browser via a Cloud-based provider. **PCBDESIGN**

Iain Wilson is a co-founder and president of Iron Atom. He and Alessandro Federici founded Iron Atom in 2011 after seeing an opportunity to utilize Cloud computing to offer on-demand usage of highly automated, expensive software applications to the mass market.

Trace Currents and Temperature, Part 1: The Basic Model

by Douglas Brooks, Ph.D.
ULTRACAD DESIGN INC.

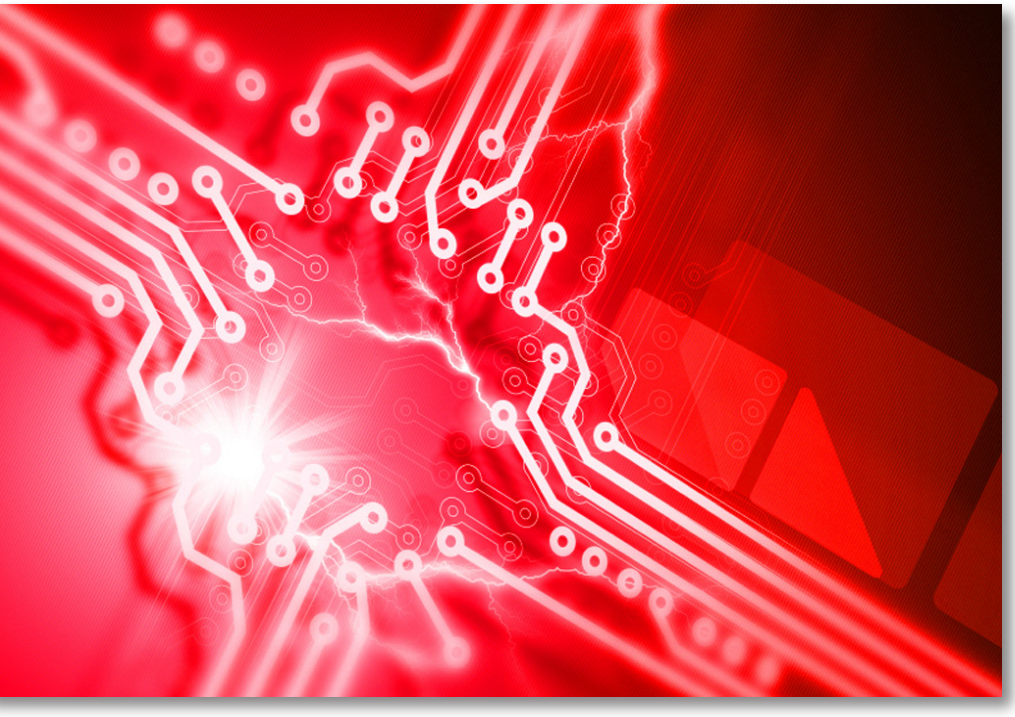
SUMMARY: *This first of a four-part series on trace currents and temperature covers the role of resistance and then formulates a basic model for analysis. Subsequent parts will explore various results that have been empirically obtained, how we can use the melting temperature of a trace to our advantage, and how to deal with vias.*

Role of Resistance

Traces heat up (increase temperature) because of power dissipation within the trace itself. If no current flows, there is no heating. If current does flow, then the power dissipated in the trace is equal to i^2R, where i is the current down the trace and R is the resistance of the conductor.

In my column "What Is Current And Why Do We Care," I provide the fundamental definition in electronics: Current is the flow of electrons. I develop that definition in that column and in more detail in an article on our website[1]. Individual electrons really flow very slowly down a copper conductor. More accurately, they *jump* from one atom to another, displacing an electron in that atom. That electron then jumps to another atom, displacing an electron in that atom, and so on. The individual electrons *do not* travel at the speed of light, but the displacement of electrons from one atom to another does progress at the speed of light.

Heat (or temperature) is movement[2]. As the temperature of a material increases, atomic and molecular motion within that material speeds up. In particular, there is random motion at the electron level, which also speeds up with temperature. This results in random collisions between electrons in conductors. If we try to push a signal down a conductor with many such collisions going on, we must overcome (at least to some extent) the effects of the collisions. We do that with a force that, in our world, equates to voltage. It is the effect of these collisions, impeding the flow of the electrons, that we call *resistance*.



The resistance that a signal sees as it propagates down a conductor is primarily the result of these collisions. There are fewer collisions at lower temperatures than at higher temperatures, and therefore the resistance of a conductor is smaller at lower temperatures and increases with temperature. The number of available electrons for current flow increases with cross-sectional area, making it easier for a signal to find a path through the collisions (i.e., there are more paths

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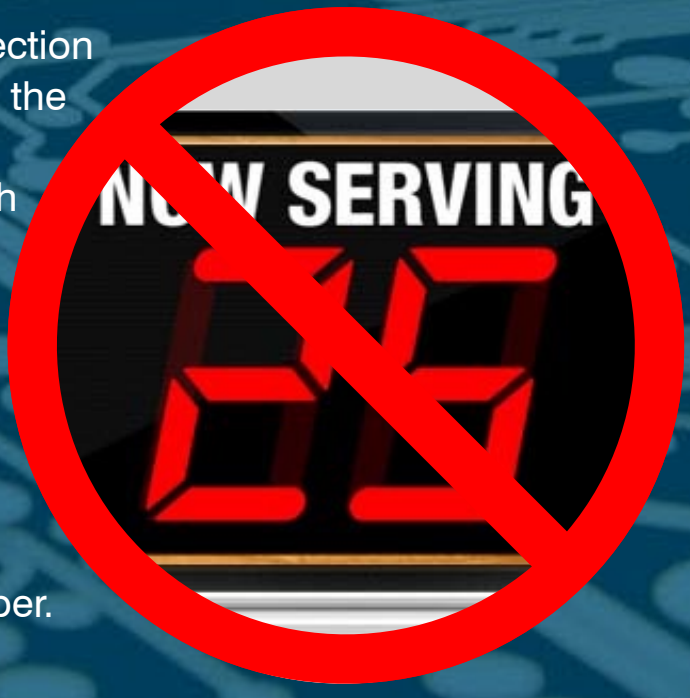

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available with bigger cross-sectional areas). Therefore, as a general rule, the resistance of a conductor decreases with increasing cross-sectional area and increases with increasing temperature.

So as we pass a signal down a conductor, a small amount of the energy in the signal is dissipated within the conductor as power dissipation: i^2R. It is this power dissipation that heats up the conductor. There is generally higher energy lost at higher temperatures, and lower energy lost with larger conductors (i.e., those with larger cross-sectional areas).

Resistivity

The characteristic of a material that reflects its electrical resistance is a property called *resistivity*. All materials have resistivity and there are numerous tables in printed media and on the Web that provide resistivity information for various materials. Silver, copper, and gold, respectively, have the lowest resistivity of all elements. It is typically given by the values:

Silver	1.6×10^{-8} ohm*m
Copper	1.7×10^{-8} ohm*m
Gold	2.2×10^{-8} ohm*m

Note: Units are ohm-meters.

Since resistivity increases with temperature (see discussion above), electrical resistivity *must be specified at a particular temperature*. This is usually specified as ambient, or room temperature, at 20°C.

As noted, the units of resistivity are ohms-length. If we divide resistivity by the cross-sectional area of a conductor, we get units of:

Ohms-length/area = ohms/unit length.

Now, if we multiply that by the length of the conductor, the units become:

Ohms/unit length X length = ohms
(or, simply, resistance).

So, the standard formula for the resistance of a conductor, based on its resistivity, is[3]:

[Eq. 1] $R = (\rho/A) * L$

Where:
ρ (rho) is the resistivity of the conductor
A is the cross-sectional area of the conductor
L is the length of the conductor.

And since resistivity is given relative to a specific temperature, then the resistance of a trace calculated with Equation 1 applies *at a specific temperature.*

Thermal Coefficient of Resistivity

The thermal coefficient of resistivity is usually represented by the symbol alpha, α. It is the factor that resistance increases with increasing temperature. Its usage is shown in Equation 2. Take the resistance of a conductor at some reference temperature (usually, but not necessarily 20°C) and multiply it by one plus alpha, times the change in temperature from the reference:

[Eq. 2] $R = R_{ref}(1+ \alpha*\Delta T)$

Where:
R = Resistance at the desired temperature
R_{ref} = Resistance at the reference temperature
α = thermal coefficient of resistivity, and
ΔT = desired temperature – reference temperature (°C).

The thermal coefficient of resistivity for silver, copper, and gold is[4]:

Silver	0.003819 per degree C
Copper	0.004041 per degree C
Gold	0.003715 per degree C

The thermal coefficient of resistivity is very roughly 0.4% per degree C.

Resistance of Copper Wires and Traces

The resistance of copper wires of arbitrary size is readily available in standard texts and Web pages. The standard table of resistance is usually based on the American Wire Gauge table which itself is based on what was known as the Brown and Sharpe Wire Gauge table first formulated in 1857[5]. While these types of tables readily equate resistance and wire size for some 44 different wire sizes (gauges) they are not

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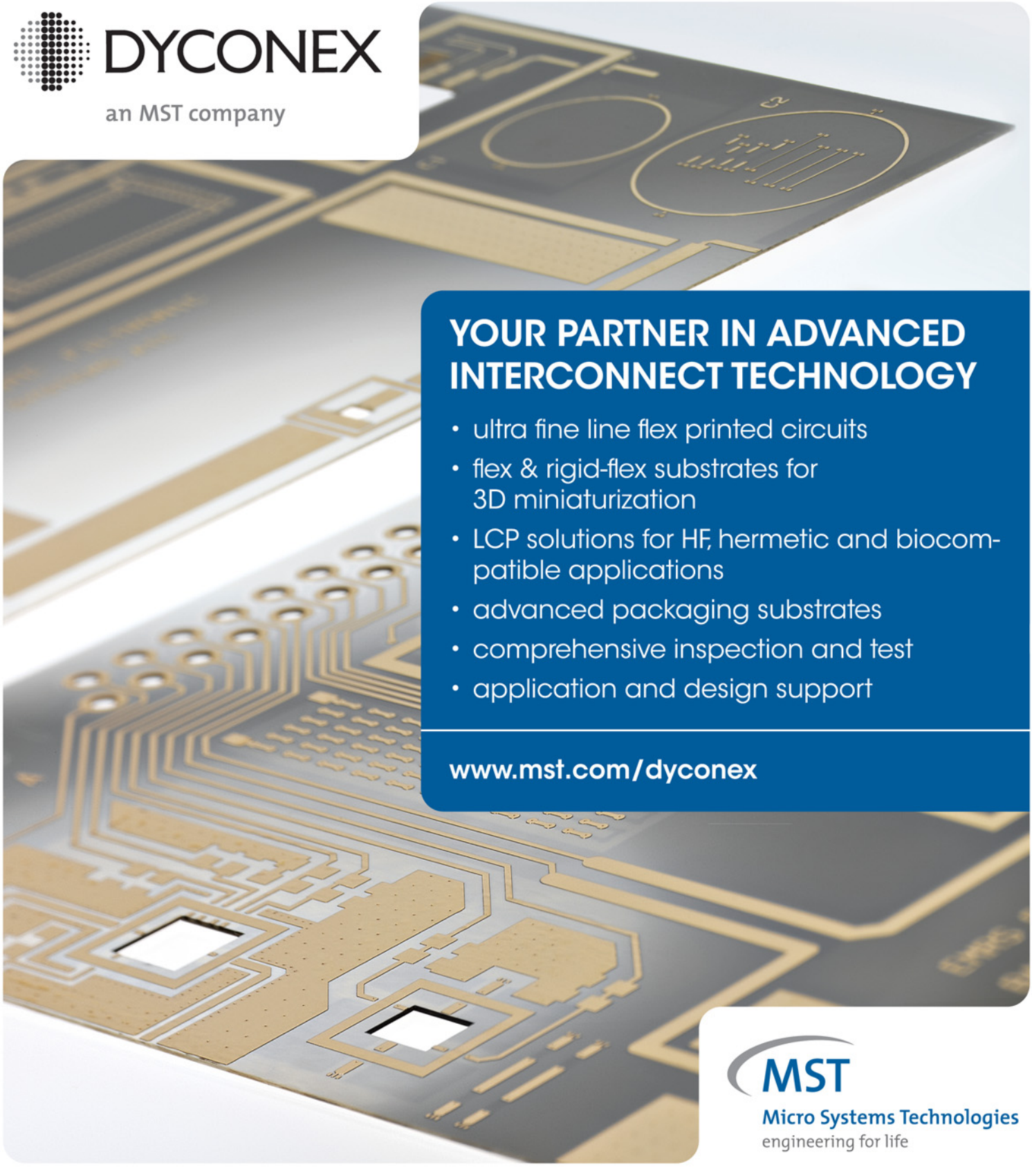

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TRACE CURRENTS AND TEMPERATURE, PART 1: THE BASIC MODEL *continues*

particularly useful for determining resistance vs. size for PCB traces. UltraCAD has created a freeware calculator for conveniently converting between trace size and wire gauge, available on our website[6].

An illustration of this calculator is shown in Figure 1.

The top portion of the calculator allows the user to enter any two of three parameters (wire gauge, trace thickness, and trace width) and solve for the third. Then if the user enters a trace length and a specific environmental temperature, the calculator will solve for the trace resistance at that temperature. Finally, if the user enters the current flowing down the trace, the calculator provides the voltage drop across the trace (a simple Ohm's Law calculation).

Model for Trace Temperatures

We now have everything we need to develop a model for trace current/temperature relationships. Such a model is shown in Figure 2.

Figure 2 illustrates a trace on a substrate. The trace is subjected to heating as a result of the power dissipated in the trace (i.e., the i^2R loss). The trace will cool as a result of conduction and convection. A stable temperature is reached when the heating effect and the cooling effect are equal and cancel. Therefore, we can start with the idea that the change in temperature (of the trace) is proportional to i^2R, or:

[Eq. 3] $$\Delta T \approx i^2 R$$

Since R is inversely proportional to the area, A, we can rewrite this as:

[Eq. 4] $$\Delta T \approx i^2 / A$$

And rearranging terms leads to:

[Eq. 5] $$I \approx \sqrt{\Delta T * A}$$

[Eq. 6] $$I \approx \Delta T^{.5} * A^{.5}$$

[Eq. 7] $$I \approx \Delta T^{\beta 1} * A^{\beta 2}$$

Note that each successive equation (Equations 6 and 7) gets progressively more general.

There are two reasons for the more general

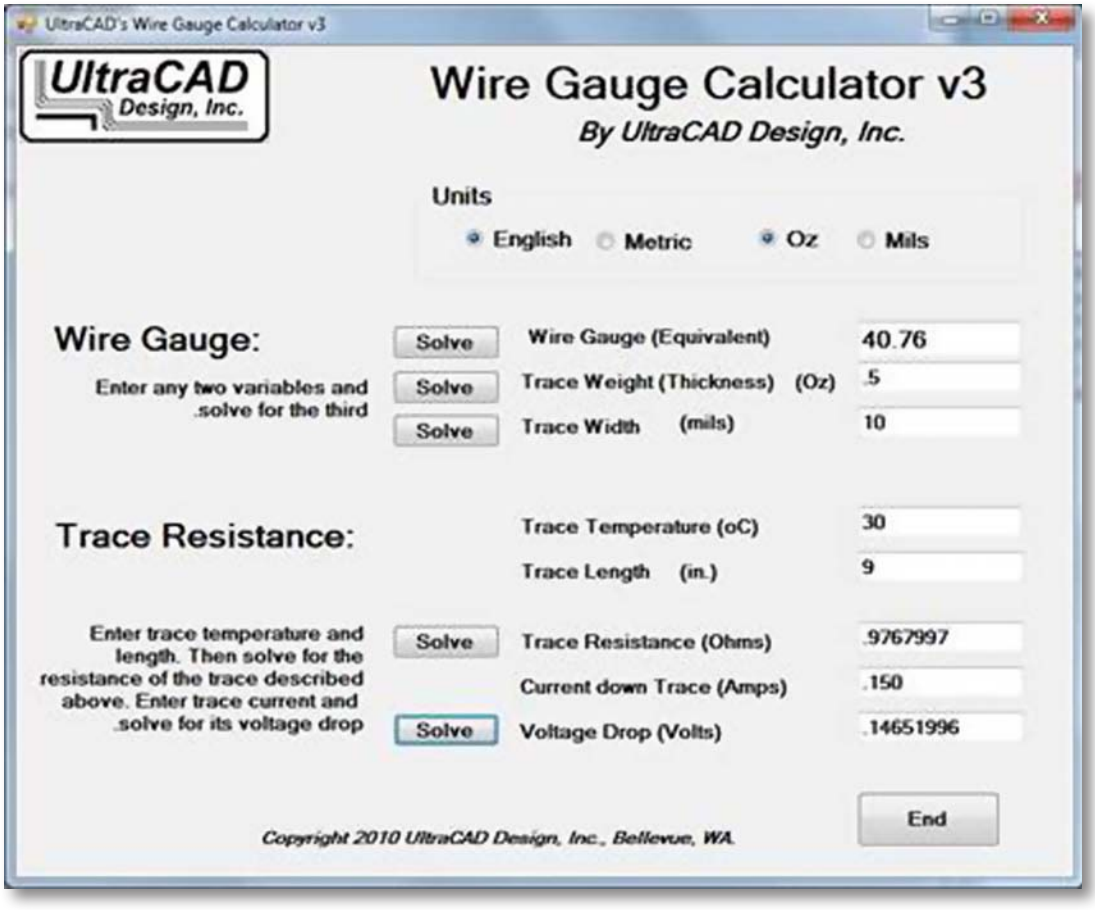

Figure 1: UltraCAD's Wire Gauge Calculator, v3.

equation. The first is that the area of the trace is involved in both the heating of the trace and the cooling of the trace. Therefore, one would expect it to have a different exponent than the ΔT term. The other reason for a more general approach is because the resistivity changes with temperature. Assume the only important factor is power dissipation. Then it would intuitively seem that 0.5 would be the correct exponent for ΔT. But as the trace heats up the resistivity changes. Therefore, for a given current, there is more heating at higher temperatures than there is at lower temperatures. Consequently, we would expect the exponent of ΔT to be slightly different from 0.5.

In an article in 1997, McHardy and Gandhi[7] attempted to fit Equation 7 to the original IPC data we all know and love; more on that in Part 2 of this series. They concluded that the form factor of a trace may be important in the relationship. That is, the temperature rise may be different for a wide, relatively skinny trace than it would be for a narrow, thicker one of the same cross-sectional area. This would be because a wider trace may cool better than a narrow trace would. Thermal stability would occur when the heating of the trace (caused by i^2R) equaled the cooling of the trace (related to the surface area, or more directly to the width, W). We may be able to improve the model in Equation 7, therefore, by looking at the form factor of the trace (i.e., the width and the thickness) instead of just the cross-sectional area. We can modify the model in Equation 7 to adjust for this by breaking the area term into its width and thickness components, as in Equation 8:

[Eq. 8] $$I \approx \Delta T^{\beta 1} * W^{\beta 2} * Th^{\beta 3}$$

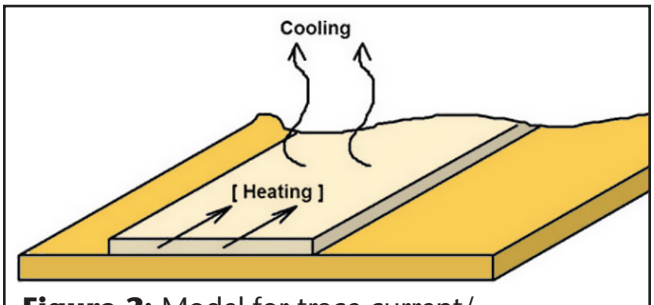

Figure 2: Model for trace current/ temperature effects.

Equation 8, then, becomes an appropriate model for investigation of the relationship between trace currents and trace temperatures. We will look at some empirical results of this model in Part 2 of this series. **PCBDESIGN**

References

1. For a more extensive discussion of current and its relationship to Maxwell's Equations, see my article "What is This Thing Called Current: Electrons, Displacement, Light, or What?"

2. For example, the definition of absolute zero temperature is when ALL motion at the atomic level stops.

3. It is really easy to mix up units when using this formula. Make sure that resistivity, area, and length are all expressed in the same length units or errors will result!

4. The thermal coefficient of resistivity is very sensitive to a particular alloy. Therefore different sources may give different values, based on different alloy assumptions.

5. For a good discussion of this, as well as a complete table, visit Wikipedia.

6. See www.ultracad.com.

7. "Empirical Equation for Sizing PWB Traces," John McHardy, Mahendra Gandhi. Presented at IPC Works '97 October 5 - 9, 1997, IPC Technical Paper S06-2.

Douglas Brooks has an MS/EE from Stanford University and a Ph.D. from the University of Washington. He has spent most of his career in the electronics industry in positions of engineering, marketing, general management, and as CEO of several companies. He has owned UltraCAD Design Inc. since 1992. He is the author of numerous articles in several disciplines, and has written articles and given seminars all over the world on signal integrity issues since founding UltraCAD. His book, Printed Circuit Board Design and Signal Integrity Issues was published by Prentice Hall in 2003. Visit his website at www.ultracad.com.

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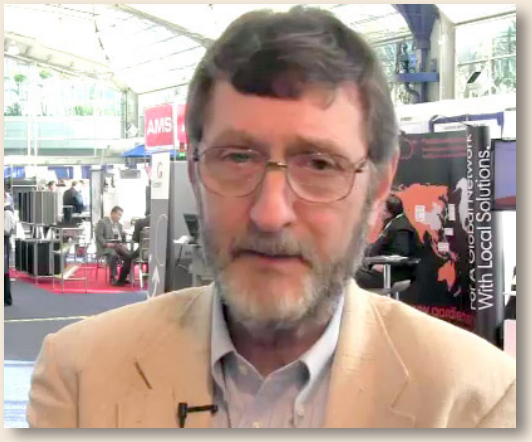
IPC APEX EXPO 2013 to Hold Design-Focused Activities

With expertise on the latest design technologies, techniques and roadmapping efforts, the IPC Designers Forum, design-focused courses and Designer Certification sessions will be held at IPC APEX EXPO, February 15-18, 2013, at the San Diego Convention Center. Leaders in design from L-3 Avionics Systems, Plexus, Gentex, and other leading companies will share insights on design challenges and processes for the next generation of electronics.

For engineering staff and managers in design, sales, purchasing and quality, the IPC Designers Forum on February 18 is a full-day educational and technical exchange program focused on critical design issues. Dieter Bergman, IPC, will kick off the Forum with a discussion on roadmapping efforts in the area of design.



Other subject matter experts presenting at the Designers Forum include: Edward Acheson, Cadence Design Systems Inc., who will discuss efficient design data transfer to manufacturing using IPC-2581; Daniel DiTuro, DiTuro Consulting, will cover design for high-reliability applications; Happy Holden, Gentex Corporation, will review the increasing complexity of PCB designs; Vern Solberg, Solberg Technical Consulting, will tackle embedded circuits; and Rick Hartley, L-3 Avionics Systems, will cover professional design technology and techniques. Mark Finstad, Flexible Circuit Technologies and Mark Verbrugge, Pica Manufacturing Solutions, will host the popular "Ask the Flexperts" session.

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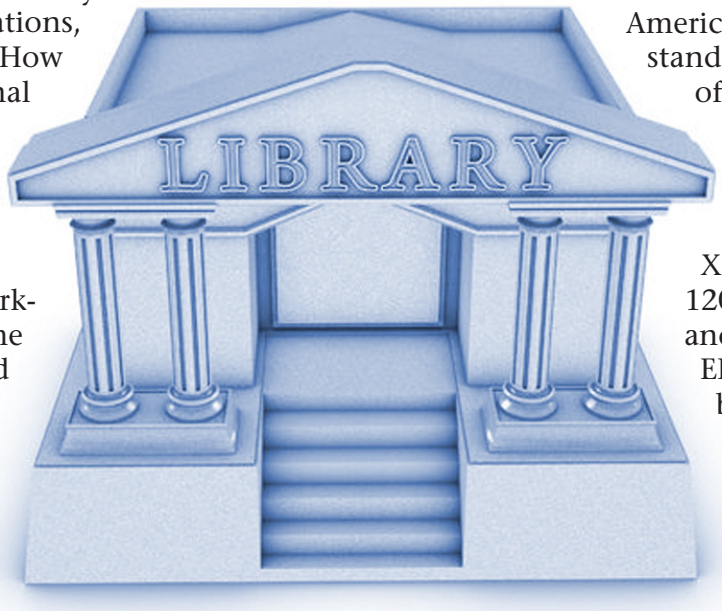
The Elements of PCB Library Construction

by Tom Hausherr
PCB LIBRARIES INC.

SUMMARY: There are many elements of PCB library construction. Measurement units, pad shapes, terms, rotations, line widths, text height, IPC's three-tier environment, manufacturers' recommended patterns, and many other issues can quickly become confusing, even for experienced designers. The good news: It doesn't have to be this way.

There are many elements of PCB library construction. Measurement units, pad shapes, terms, rotations, line widths, text height, IPC 3-Tier environment, manufacturers' recommended patterns, and many other issues can quickly become confusing, even for experienced designers. The purpose of this article is to help clear up confusion about why these features exist. At the end, a short survey will help identify how prevalent these features are in the design community. The results of the survey will be published next month in this magazine and at PCBLibraries.com, so you can see how commonly used your PCB library construction preferences are.

This information will empower designers with the information needed to make sure designs use the best construction. Are the features being used driven by standards organizations, or by CAD vendors? How do these affect the final design? Read on to find out.



Measurement Units

Let's look at working units first. Some PCB designers build all their CAD libraries in metric units, but do the PCB layout in inches. Is this you? Some still cling strictly to mil units for all PCB library creation and layout, but I find this scenario primarily in the U.S. Others use millimeters for CAD library construction, part placement, via fanout, and trace routing; even their mechanical data for the board outline, mounting and tooling holes, text heights, title blocks, drill chart and dimensions are based in metric units.

In order for the PCB designer to completely transition to metric units, the EE, mechanical drafters, component manufacturers, fabricators and assembly shops must all transition together. Component manufacturers have done an outstanding job at transitioning to the metric system. However, there is one issue regarding chip component names that I don't see changing in the near future.

When EIAJ in Japan introduced the standard dimensioning for chip components in the 1980s, in the PDP-100 publication, every component dimension and name was in metric units. The most popular resistors and capacitors were dimensioned 3.2 mm X 1.6 mm and rightfully named 3216. Under the pressure of the American imperial unit system, it didn't take long for the American-based EIA PDP-100 to be converted to inch units so that Americans could better understand the sizes and names of all chip components. Therefore, the 3.2 mm X 1.6 mm discrete components were changed to 0.125" X 0.062" and renamed 1206. Note that the "5" and "2" were dropped. EIA did not round numbers when creating footprint naming conventions, but rather they dropped numbers.

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THE ELEMENTS OF PCB LIBRARY CONSTRUCTION *continues*

the 2.0 mm X 1.2 mm chip component was introduced and quickly changed by EIA to 0.078" X 0.047", but in this case they rounded the numbers to create the 0805. Next came the 1.6 mm X 0.8 mm component, which was changed to 0.062" X 0.031", and the 0603 was born. The 1.0 mm X 0.5 mm component became 0.039" X 0.019", and the 0402 was created.

Terms and Definitions

There is enough history and facts surrounding terms and definitions to write an entire article. In brief, IPC has used the term "land pattern" to describe CAD library parts since the introduction of the IPC-SM-782 in March 1987. But during that same time period, OrCAD Capture introduced "footprint" to describe a CAD library part. The IPC-T-50 Terms and Definitions included footprint, and for 20 years the definition was "See Land Pattern." Just recently, the IPC-T-50 committee redefined the term "footprint" as "The area projected onto the printed board, described by the component body, including the lead terminations." So IPC now describes the footprint as the component package outline that attaches to a land pattern. Depending on the CAD software you use, you may have also become familiar with CAD vendor-specific terms such as "cell" and "decal."

The terms "pad" and "land" have also been used interchangeably. The IPC-7351 standard refers to a PCB library part solder area as a land, but CAD vendors refer this as a pad. In your everyday communication with other PCB designers and EE, what term do you use?

Pad/Land Shape

Since the introduction of the IPC-SM-782 in 1987, IPC has always promoted the oblong (full radius) pad (or land) shape. However, an industry poll indicates that 70% of PCB designers use a rectangle pad shape. The D-shaped pad shape has been a CAD tool option in enterprise CAD tools but rarely used in PCB library construction. The rounded rectangle is a new concept in pad shape and has not been adopted by most PCB designers due to the lack of guidance from standards organizations regarding the corner radius values. And the CAD vendor libraries and component manufacturers who provide recommended solder patterns always use a rectangular pad shape.

Figure 1 illustrates the pad shape variations for a standard quad flat no-lead (QFN) package, but note that even though the terminal leads are both rectangle and D-shaped, the component manufacturers' recommendations are rectangle pad shape. I have never seen a component manufacturer recommend oblong or D-shaped pad shape for the terminal leads. And even though component manufacturers form the thermal tab with a corner chamfer by Pin 1 and radius corners in the other three corners, the recommended thermal pad is usually sharp corners with no chamfers or radius. If the physical component thermal tab has a chamfer, I personally prefer to add a chamfered corner in the thermal pad as a visible Pin 1 indicator in copper etch.

Most CAD tools now support the rounded rectangle pad shape. The rounded rectangle

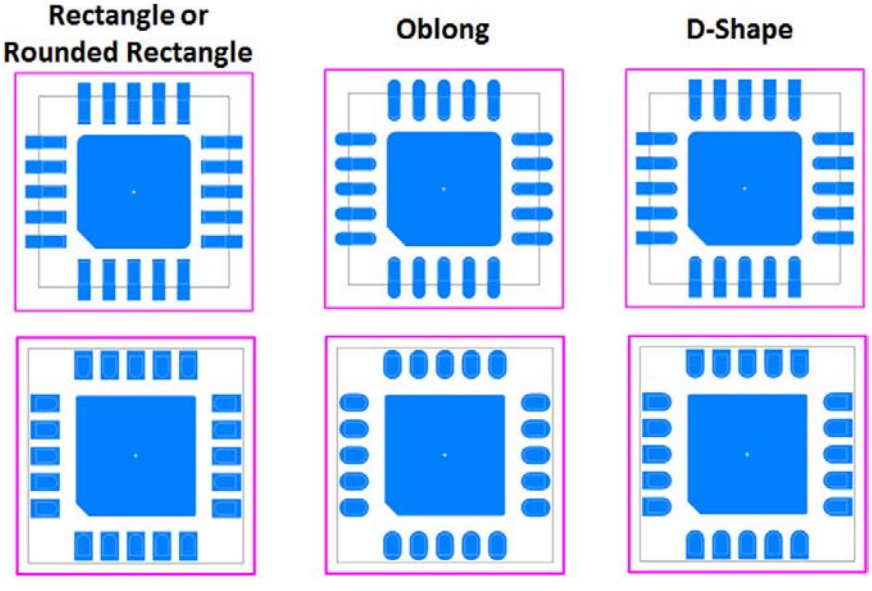

Figure 1: Pad shape variations for a standard QFN package.

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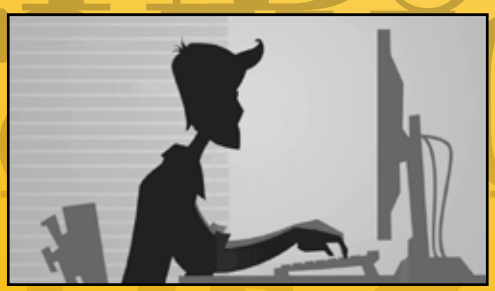

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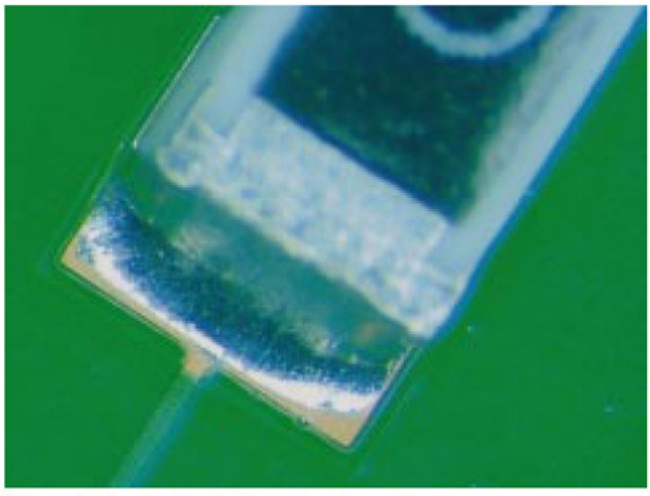

Figure E-1 SnPb Solder; No Clean Process

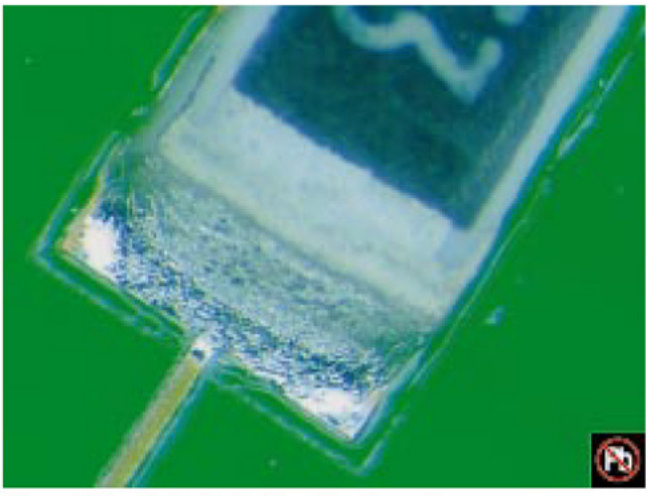

Figure E-2 SnAgCu Solder; No Clean Process

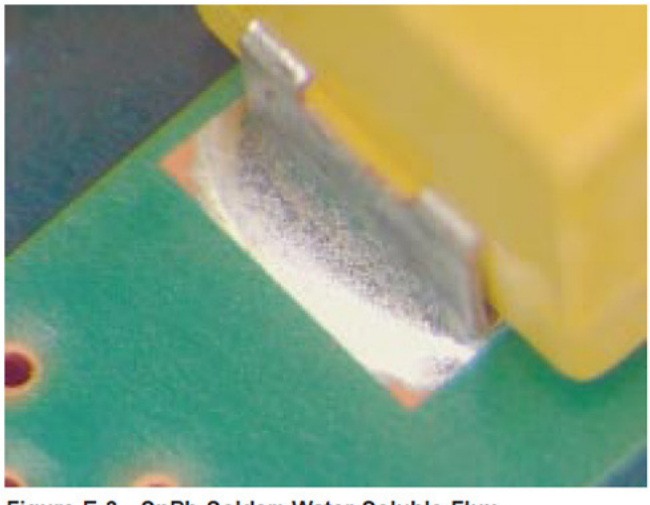

Figure E-3 SnPb Solder; Water Soluble Flux

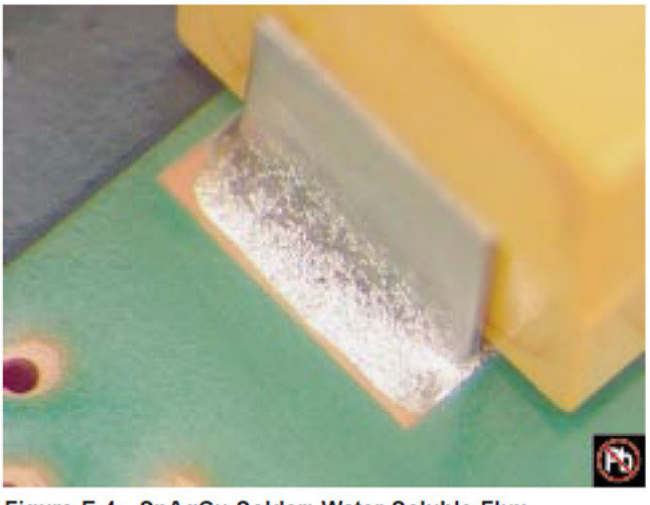

Figure E-4 SnAgCu Solder; Water Soluble Flux

Figure 2: Solder rounded off at corners.

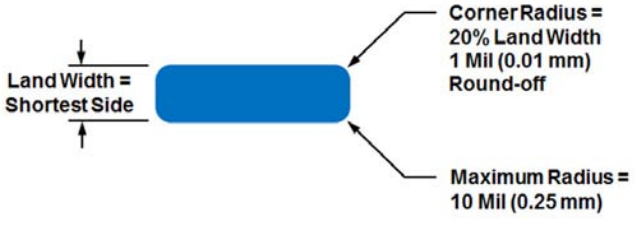

Figure 3: Rounded rectangle.

could become the universal pad shape of the future as a 100% replacement for oblong, rectangle and D-shape. Some CAD vendors claim that the rounded rectangle is the best option for lead-free solder, and others claim it improves fabrication and assembly. See Figure 2 (from the IPC J-STD-001 assembly standard), which illustrates assembled parts after reflow. Notice that the lead and lead-free solder move away from the corners of the pad, therefore creating useless copper on the PCB. In this case, a rounded rectangle pad shape would conform closer to the final solder joint than the rectangle shape.

Figure 3 is a rounded rectangle concept of how the rounded corners are calculated using the pad width and a known percentage of the width to determine the corner radius. Also, the calculation includes a round-off factor for the radius and a maximum radius. The calculation is automated by free tools such as the PCB Footprint Expert from PCB Libraries. This method

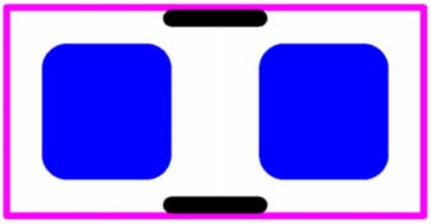

Figure 4: (left) Rounded rectangle for a chip capacitor.

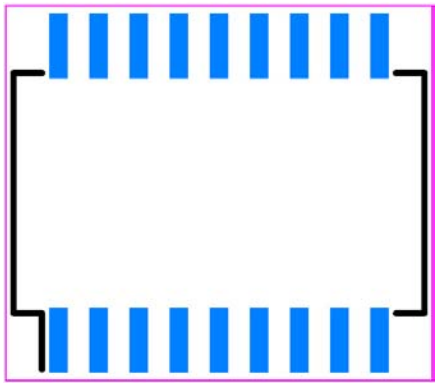

Figure 5: (middle) IPC-7351 rotation.

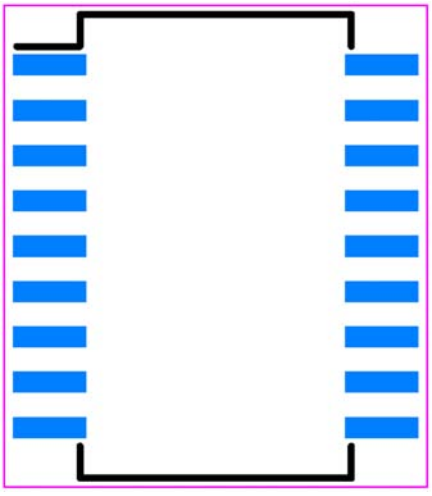

Figure 6: (right) IEC 61188-7 rotation.

of calculation creates a consistent "known" pattern throughout the entire CAD library.

The rounded rectangle shape can be used for every surface-mounted component package with the exception of bottom-only terminations such as the ball grid array (BGA), land grid array (LGA) and column grid array (CGA) due to the round component lead shape. The rounded rectangle shape is even acceptable for chip capacitors and resistors as shown in Figure 4.

Zero Component Orientation

The world standards organizations know that one of the key elements in electronic product development automation is the implementation of a single zero component orientation for all CAD library parts. IPC introduced zero component orientation in 2007 with the IPC-7351A in Figure 5, as Pin 1 left or upper left for all PCB library parts. Then in 2009, IEC introduced zero component orientation in the IEC 61188-7 in Figure 6 as Pin 1 left or lower left for all PCB library parts.

Table 1 illustrates various component families and the various rotations recommended for PCB library construction. Also included is the EIA-481D which publishes the recommended rotation of the component in the tape and reel, tube, or tray. However, not all component manufacturers adhere to the EIA-481D standard.

The primary purpose of creating all of your PCB library parts with a known zero component orientation is to easily alert your assembly shop which rotation you used by identifying the standard your PCB library was built to.

To solve this issue, the IPC-2581 CAD tool export format is designed to replace Gerber data. IPC-2581 supports fabrication and assembly. In the future, if you use IPC-2581 to provide your assembly shop with pick-and-place data, your assembly drawing should indicate zero component orientation "Level A" or "Level B," which will provide valuable information to accelerate the assembly process and reduce errors. Until everyone uses this standard terminology and orientation technique for their PCB libraries, assembly shops are forced to check and double-check every rotation to verify the rotation accuracy.

Silkscreen Outlines

Silkscreen outlines continue to be debated as everybody seems to have different ideas and recommendations regarding them. Should the silkscreen outline be outside the component package as represented in Figure 7 or under the component package as shown in Figure 8? Should the silkscreen outline perform any useful function or simply represent a box to define where each component is assembled? Here are some basic silkscreen guidelines that should be used for all PCB library construction:

1. No silkscreen outline under the component; these are covered up during assembly, don't provide any useful purpose, and are a waste of expensive inkjet cartridges.
2. All silkscreen outlines visible after assem-

THE ELEMENTS OF PCB LIBRARY CONSTRUCTION *continues*

Component Family	IPC-7x51 (Level A)	IEC 61188-7 (Level B)	EIA-481-D
Chip (All Families)	Polarization On Left	Polarization On Left	Polarization On Left
Tantalum Capacitor	Polarization On Left	Polarization On Left	Polarization On Right
Molded Body Diode	Polarization On Left	Polarization On Left	Polarization On Left
SODFL	Polarization On Left	Polarization On Left	Polarization On Left
MELF	Polarization On Left	Polarization On Left	Polarization On Left
Aluminum Capacitor	Polarization On Left	Polarization On Left	Polarization On Left
Precision Inductors	Left	Left	Left
PLCC Square	Upper Center	Left Center	Left Center
PLCC Rectangle	Upper Center	Left Center	Left Center
LCC	Upper Center	Left Center	Left Center
QFP Square	Upper Left	Lower Left	Upper Left
QFP Rectangle	Upper Left	Lower Left	Lower Left
Bump QFP Side	Upper Left	Lower Left	Upper Left
Bump QFP Center	Upper Center	Left Center	Left Center
Ceramic QFP	Upper Left	Lower Left	Upper Left
SOIC	Upper Left	Lower Left	Lower Left
TSOP	Upper Left	Lower Left	Lower Left
TSSOP & SSOP	Upper Left	Lower Left	Upper Left
TSO8 (Mini US8)	Upper Left	Lower Left	Lower Right
BGA Square	Upper Left	Lower Left	Lower Left
BGA Rectangle	Upper Left	Lower Left	Lower Left
SOJ	Upper Left	Lower Left	Lower Left
CFP	Upper Left	Lower Left	Lower Left
QFN Square	Upper Left	Lower Left	Upper Left
QFN Rectangle	Upper Left	Lower Left	Lower Left
Chip Array	Upper Left	Lower Left	Lower Left
DFN	Upper Left	Lower Left	Lower Right

Note: The EIA-481-D rotations marked in Red conflict with both IPC and IEC

Table 1: Rotation by standard note: The EIA-481-D rotations marked in red conflict with both IPC and IEC.

bly provide a functional use as alignment marking for assembly registration accuracy.

3. All silkscreen outlines must be inside placement courtyard.

4. All silkscreen outlines are mapped to the maximum component body with one exception, the silkscreen-to-pad spacing rule "overrides" the component body mapping.

5. Silkscreen outlines should map the component body and not go around pads. Excess silkscreen outlines should be avoided to make room for ref des locations. Silkscreen outlines should perform a "hatch" outline along the component package body.

6. Pin 1 is identified by extending the silkscreen along Pin 1 length to indicate polarity when the package cannot be placed inverted (the only components that can be inverted are non-polarized 2-pin parts).

7. No silkscreen on any exposed pad (land). The ideal pad/silkscreen gap should be 0.05 mm (2 mils) + solder mask annular ring. So if your solder mask annular ring is 0.07 mm (3 mils) + 0.05 (2 mils) = 1.2 mm (5 mils) minimum silkscreen to pad gap.

Some companies do not use silkscreen outlines when creating the PCB library. Others put a silkscreen outline in the PCB library part to aid part placement, but do not include it in the Gerber output data for the board fabrication. Others put the silkscreen outline only on the prototype boards but not in production, while others use silkscreen outlines on every board. Silkscreen outline line widths are also a

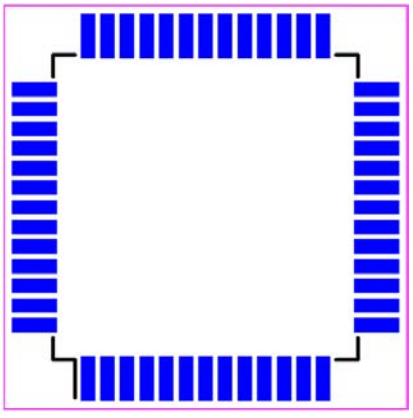

Figure 7: Silkscreen outside component body.

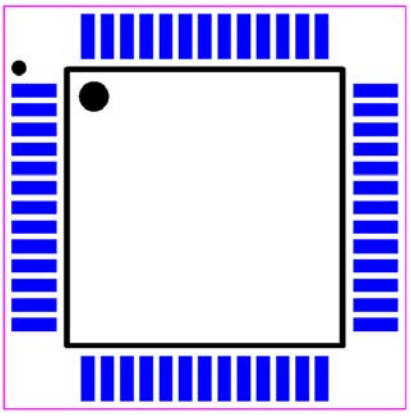

Figure 8: Silkscreen under component body.

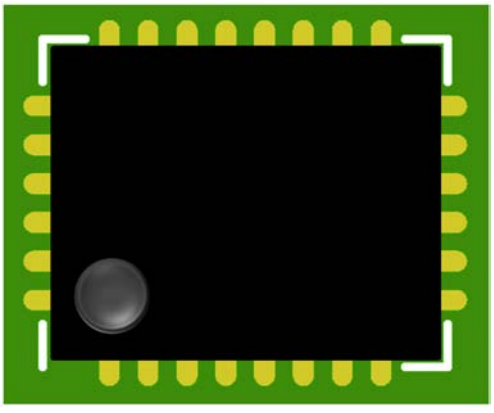

Figure 9: Missing polarity marker.

user preference, ranging from 0.1 mm (4 mils) to 0.25 mm (10 mils).

On components with bottom-only terminals, it's difficult to meet the silkscreen rules to keep the silkscreen and polarity marking outside the component and inside the placement courtyard. In these cases, the lack of silkscreen outlines indicates the polarity. Figure 9 shows the three distinct silkscreen outline corners; note the silkscreen corner by Pin 1 has a missing silkscreen outline to clearly indicate the location of Pin 1. The surface mount component families affected are DFN, QFN, SON, BGA, LGA, and CGA.

Courtyard

The IPC-7351 standard features a three-tier library system: "least" for handheld devices, "nominal" for desktop or controlled environment, and "most" for ruggedized military, space, and medical devices. Sometimes, the component manufacturers' datasheets also offer recommended solder patterns. Another option is the user preference, where neither the IPC-7351 nor the manufacturers' recommendation is used, and the PCB designer invents a unique solder pattern based on experience.

IPC-7351 promotes the use of placement courtyard boundaries to guide part placement, to aid the assembly process and also rework for unsoldering bad components. This boundary as seen in Figure 10 is referred to as the courtyard excess. In IPC-7351, there are three tiers for the gap between the outer perimeter of the library part and the placement courtyard. The least courtyard excess is 0.12 mm (5 mils) and the nominal is 0.25 mm (10 mils), while the most is 0.50 mm (20 mils). There is also a manufacturing zone to allow additional clearance if the assembly shop requires it. If your assembly shop requests an additional manufacturing zone, then the PCB designer sets a component body space rule to define the clearance between the placement courtyards. If no manufacturing zone is required by your assembly shop, then you can place the library parts bumper-to-bumper against each court-

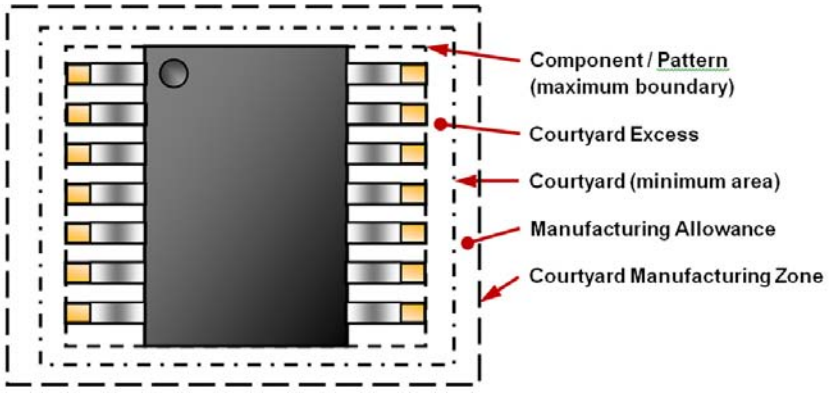

Figure 10: Courtyard boundaries.

THE ELEMENTS OF PCB LIBRARY CONSTRUCTION *continues*

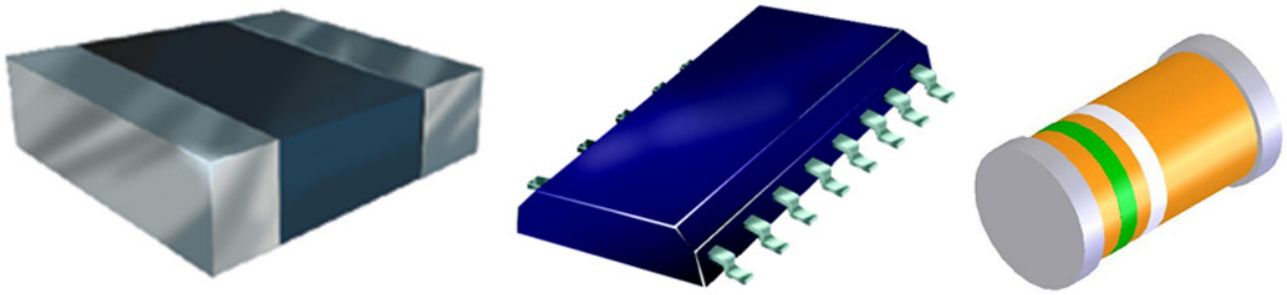

Figure11: 3D models.

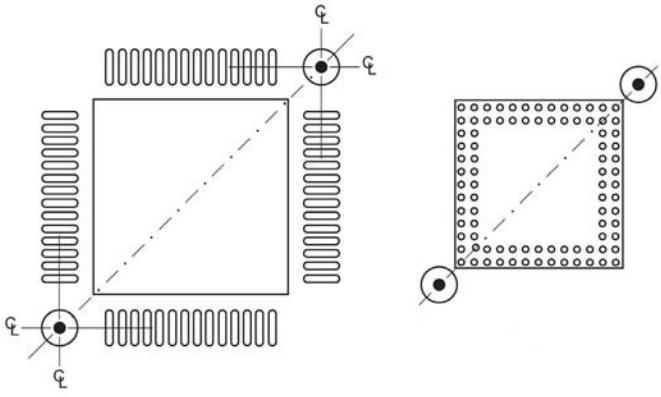

Figure 12: Fiducial placement.

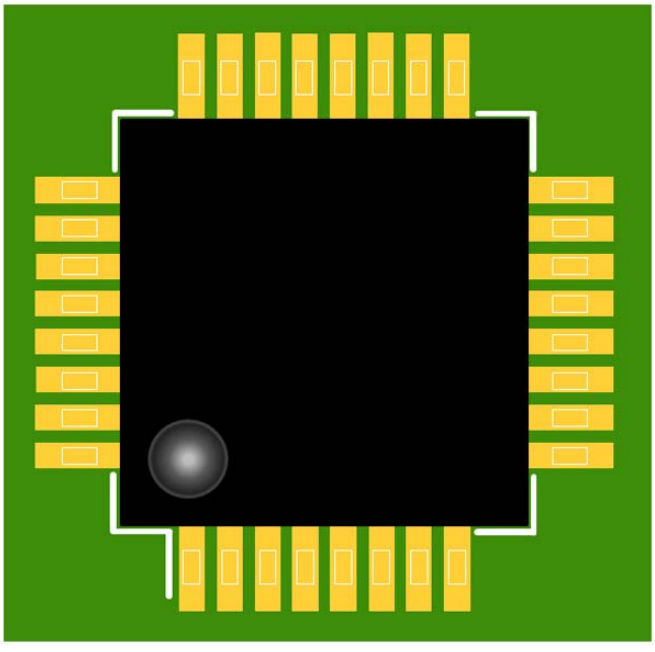

Figure 13: Post-assembly inspection line or dot.

yard boundary, but the boundaries should never overlap each other. Overlapping courtyard boundaries could compromise the assembly process.

3D modeling is an upcoming technology that many companies are adding to their PCB design flow. It used to be that PCB design tools had to export IDF data and import IDF data into 3D mechanical drafting tools like PRO-E or SolidWorks. But now, CAD vendors such as Altium are adding 3D modeling directly into their CAD tool software. Eventually 3D modeling will be a must-have feature in the PCB design flow, but no one knows when that will happen. Many people say they can't live without it, while others are asking, "Why do I need it?" I believe the industry will adapt to 3D modeling concepts as seen in Figure 11 when 3D model libraries become abundant and affordable.

Some assembly shops require local fiducials on fine-pitch quad flat packages and ball grid arrays as seen in Figure 12. Local fiducials are used by assembly to optically bombsite (locate) the center of the fiducial in each corner of the component to compensate for any skew or misalignment in the panel as it travels down the assembly conveyor belt. This improves pick-and-place accuracy for fine-pitch components that require special handling during assembly. If there is no room in the corners of the component to place two fiducials, one fiducial in the center of the part is a second option. But as assembly technology improves, the need for local fiducials could diminish.

Post-Assembly Inspection Dots

Finally, we'll take a look at the post-assembly inspection dots or lines. These are intended

Most-Read Mil/Aero007 News Highlights

AT&S Certified for EN9100/AS9100

AT&S Hinterberg has successfully passed the certification audit for the EN9100/AS9100 standard. After having successfully implemented the management system requirements for ISO 9001, ISO/TS 16949 and ISO 13485, AT&S Hinterberg has achieved another landmark in certification process.

Viasystems Boosts Military Offerings with AS9100C Cert

Viasystems Group, Inc., a leading provider of complex multilayer PCBs and electromechanical solutions, today announced the achievement of AS9100C certification at its Denver, Colorado and North Jackson, Ohio facilities. AS9100C certification is an internationally recognized aerospace industry standard for the development and production of aviation, space and defense products. Viasystems' facilities in Forest Grove, Oregon; Milpitas, California; Sterling, Virginia; and Toronto, Canada attained their re-certification to the AS9100C standards in 2011.

DOD Set to Update Component Acquisition Rules

Reported incidents of counterfeit electronic component parts this year are maintaining the record pace set in 2011, highlighting the need for continued vigilance and improved detection and avoidance measures at a time when U.S. defense representatives are scheduled to update acquisition rules, according to information and analytics provider IHS.

Report: Global Aerospace and Defense Market 2011-2015

Commenting on the report, an analyst from TechNavio's Automotive team said: "The Civil Aviation industry in the U.S. has recorded significant growth over the past few years. The Aerospace industry in the U.S. has emerged as an industry with high potential across the world, despite the negative impact of the global financial crisis. The aerospace industry in the US is showing an uptrend in line with strong market developments. It is expected that the U.S. will buy a huge amount of airplanes by 2028."

Military Fighter Aircraft Market at $34.37B in 2012

The Military Fighter Aircraft Market 2012-2022, Visiongain's latest defence report, values the market for fighter jets at $34.37bn in 2012. Major programme developments are expected over the coming decade, with the F-35 joint strike fighter (JSF) leading a host of influential procurement projects, spanning both Western and emerging nations such as India, Saudi Arabia, and China.

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for the EE or bench technician to visually see the location of Pin 1 after assembly to verify if any components were inverted during the assembly process. Using the silkscreen marking located by Pin 1 and the polarity marking on the physical package, the inspector should be able to visually verify if the Pin 1 silkscreen mark and component polarity marking match up. A good example of this is the QFP in Figure 13, where there are four different assembly rotations to attach the component to the board.

I hope you found this article useful in identifying various parts of PCB library development. This is the first article of a series that is intended to identify how your requirements for a PCB library compare to other designers' requirements. I think many PCB designers will benefit from knowing how other designers create their libraries.

Toward this end, I urge you to consider taking this three-minute survey to voice your opinion about PCB library issues. My next article will show the results of this survey.

See you next month. **PCBDESIGN**

Tom Hausherr, CID+, is president of PCB Libraries Inc. He can be reached at Tom.Hausherr@pcblibraries.com.

How to Read the ESR Curve

by Istvan Novak
ORACLE

SUMMARY: To use bypass capacitors properly, any designer must understand ESR – effective series resistance. A designer must understand what it means and how to read the ESR curve in measured or simulated plots.

The most widely used power distribution component is undoubtedly the bypass capacitor. After the nominal capacitance, its next most important parameter is its effective series resistance, or ESR. To use bypass capacitors properly, designers must need to understand exactly what ESR means and how to read the ESR curve in measured or simulated plots. That is the focus of this column.

A real-world capacitor, whether it is a discrete capacitor or the capacitance of a power-ground plane pair, is never ideal. It always has parasitic resistance and inductance. The inductance is associated with the shape and size of the capacitor electrodes as well as the shape and size of external connections – the pads, vias and planes closing the current loop around the capacitor. The size of the current loop, which determines the inductance, depends only partly on the capacitor itself. It is a widely recognized

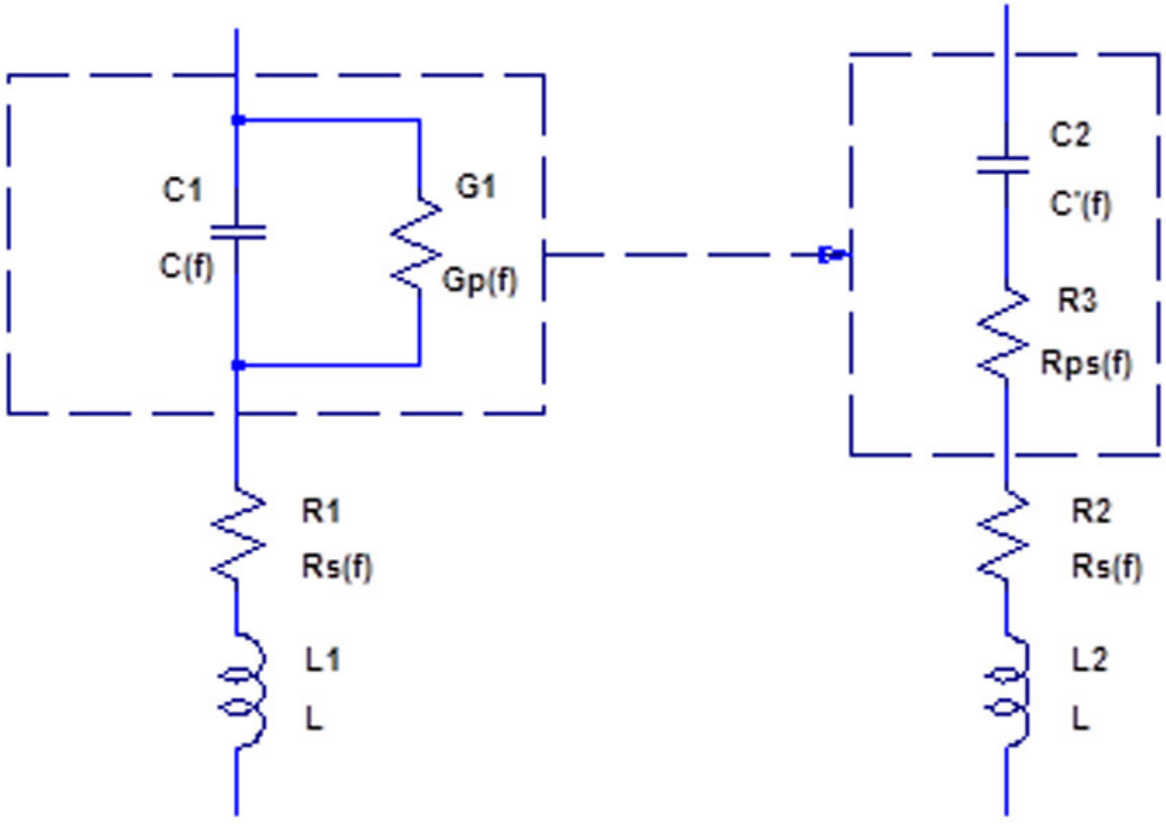

Figure 1: Equivalent circuit of a capacitor with separate conductive and dielectric losses on the left and combined effective series losses on the right. ESR is the sum of the Rs(f) conductive and Rps(f) dielectric losses.

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HOW TO READ THE ESR CURVE *continues*

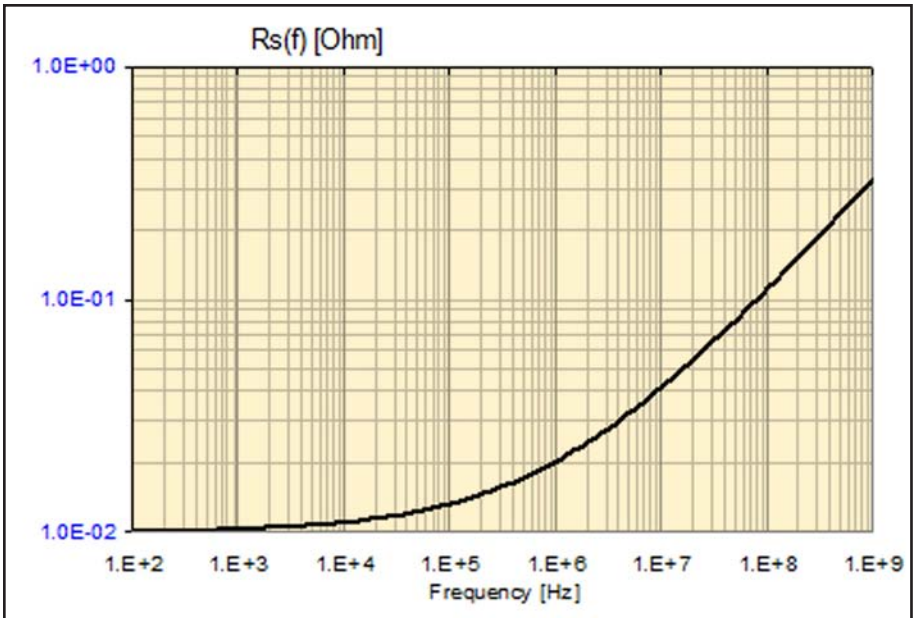

Figure 2: Typical frequency dependence of conductive losses in a ceramic capacitor.

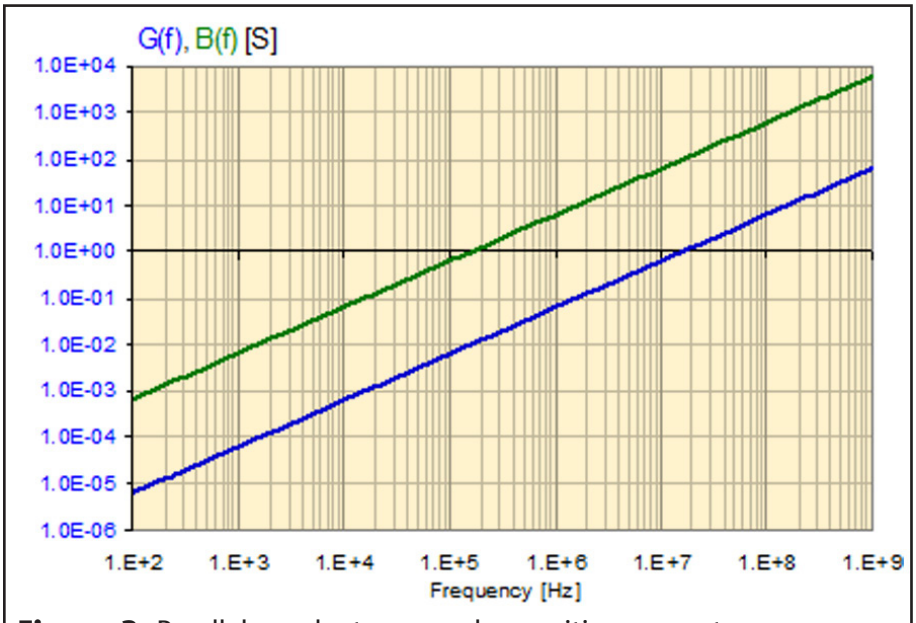

Figure 3: Parallel conductance and capacitive susceptance as a function of frequency.

and accepted fact that the loop inductance of a capacitor also depends on how we connect it to our board.

In contrast, we tend to assume that the ESR of the capacitor depends only on the capacitor, and not on its external connections. While this may be true for many applications, there are cases (to be shown in a future column) where even the ESR of a capacitor depends on the external connection geometry. To get to that interesting case, we need first to understand the contributors to ESR.

The resistance of a capacitor comes from two sources: conductor losses and dielectric losses. For instance, in a multilayer ceramic capacitor, the capacitor plates and the connecting terminals have finite resistance and they make up the series losses. The dielectric layers, especially if we have high dielectric constant materials, have a finite loss tangent and will create a parallel loss conductance. When we use a series C-R-L equivalent circuit for the capacitor, the series and parallel losses combine into a single series resistance, called effective series resistance, or ESR. This is shown in the equivalent circuits of Figure 1.

The conductive loss follows the frequency dependence of skin loss: Starting from a DC resistance value, the resistance rises with the square root of frequency. In some cases, it may be important that different contributors of conductive losses, such as terminal and capacitor-plate losses have different DC resistances and knee frequencies. Figure 2 shows a simple example: the Rs(f) conductive resistance with 10 mOhm DC resistance and 1 MHz knee frequency.

The parallel losses are described by a DC leakage current and a dielectric loss tangent, D(f). For AC modeling, we can usually ignore

the DC leakage. In a simplified model we can also assume that the dielectric loss tangent is frequency-independent; therefore, the parallel conductance is G = wC Df. If we want a causal model, the slight frequency dependence of C and Df has to be taken into account. Figure 3 shows the conductance (G) and the capacitive susceptance (B) for a 1 uF capacitor with 1% Df using the causal wideband Debye model. Figure 4 shows the series equivalent of the same lossy capacitance.

We notice that the two contributors of the equivalent series resistance vary with frequency the opposite way: The resistance of conductor losses increases, and the resistance of the dielectric losses decreases with increasing frequency. The sum of the two creates a typical basin-like plot (Figure 5). With reasonably low Df values and at low frequencies, the ratio of the magnitude of capacitive reactance |X(f)| and ESR(f) is constant and equals the (approximately frequency independent) loss tangent. We can see that in Figure 5, in the 100 Hz to 10 kHz frequency range, the red ESR curve is approximately 100 times smaller than the green |X(f)| curve, which corresponds to a 1% Df loss.

You can try different input numbers, plot the result and see all the expressions behind these calculations in the bypass capacitor model, available at www.electrical-integrity.com. **PCBDESIGN**

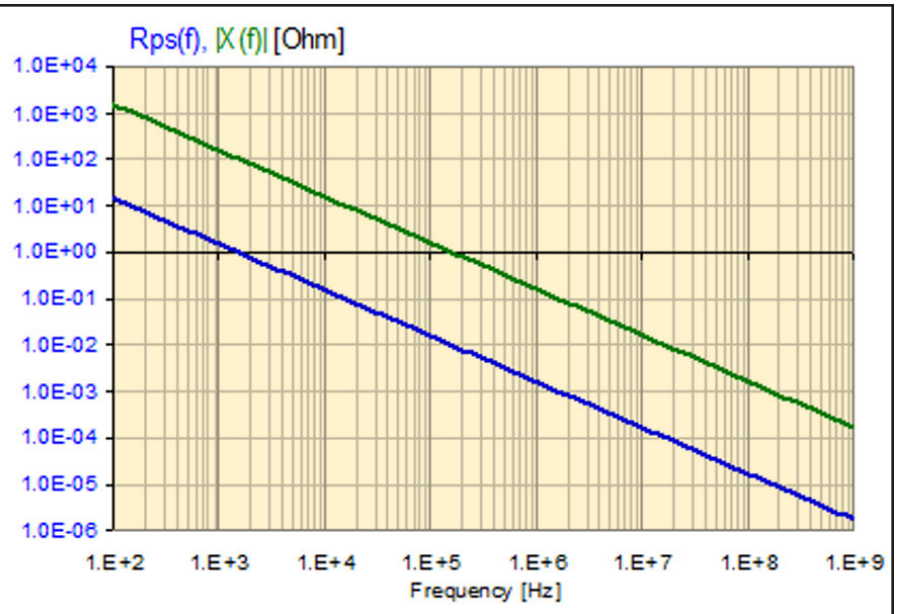

Figure 4: Series equivalent of the parallel conductance and series capacitive reactance for the capacitor from Figure 3.

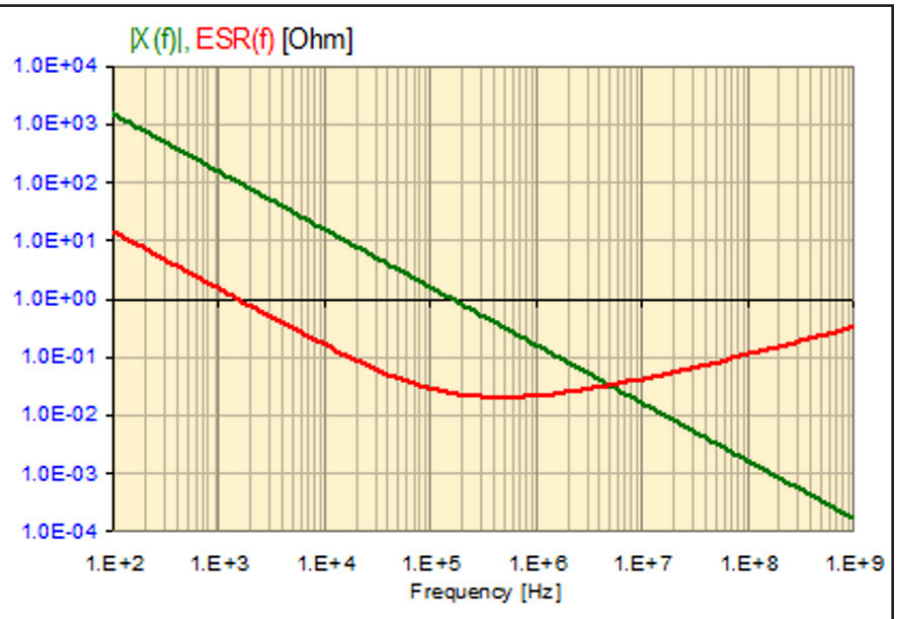

Figure 5: Capacitive reactance and effective series resistance (ESR) of a 1 uF capacitor with 1% Df and 10 mOhm DC series resistance.

Dr. Istvan Novak is a distinguished engineer at Oracle, working on signal and power integrity designs of mid-range servers and new technology developments. Novak received his M.S. degree from the Technical University of Budapest, Hungary and his Ph.D. degree from the Hungarian Academy of Sciences in 1976 and 1989, respectively. With 25 patents to his name, Novak is co-author of "Frequency-Domain Characterization of Power Distribution Networks." To contact Istvan, click here.

The Wrap Crack

by Paul Reid
PWB INTERCONNECT SOLUTIONS

SUMMARY: In the process of plating copper on the initial core, we produce a wrap of copper that goes through the barrel of the hole, and over the copper foil on its surface, producing what is called the wrap. A wrap crack is similar to a corner crack in a plated through-hole, and the focus of this column.

Buried vias and microvias are created by a sequential lamination process, which is the number of lamination steps that the board is exposed to during fabrication. The first lamination is used to make the core that includes the buried via. It is processed just like a normal circuit board, by making internal layers with discreet innerlayer circuits, laminating the stack together, and drilling the laminated stack. The board is then subjected to desmear and hole preparation, electroless and electrolytic copper plating in the hole and etching to produce discreet circuits. After that, the board is subjected to one or more lamination steps in which other structures, like microvias, are formed.

In the process of plating copper on the initial core, we produce a wrap of copper that goes through the barrel of the hole, and over the copper foil on the surface around the hole. This copper produces what is called the wrap. A wrap crack is similar to a corner crack in a PTH.

There are two styles of microvias or buried vias: those with copper caps and those without copper caps. If there is no need for a copper cap, say with staggered microvias, the core is ready to have the holes filled with epoxy or have the B-stage epoxy fill the hole during lamination. Frequently, the B-stage epoxy is used to automatically fill the microvia or buried via. There are occasions when the buried via is too large or too long for the B-stage epoxy to adequately fill the buried via during the lamination process. In those cases, a third-party epoxy may be used to fill the drilled holes. The third-party fill may be conductive epoxy or not, as the electrical current is carried by the copper plating in the wall of the buried via.

If a copper cap is required, as in stacked microvias, then the core may be put through a process called planarization or skiving. Sometimes the copper on the surface of the core is so thick that, with the copper cap, the dielectric spacing between the top of the buried via and the layer above is reduced. With ½-ounce copper foil, the thickness is typically 15.2 µm (.0006″) of copper, 30.5 µm (.0012″) of plating in the hole on the surface of the plated hole

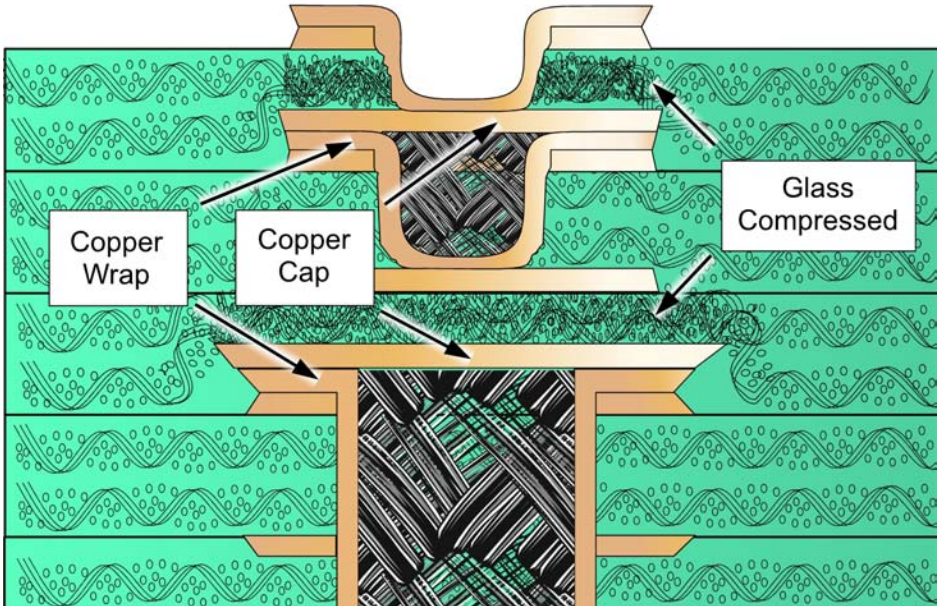

Figure 1: Planarization of the cap, wrap and glass compression.

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THE WRAP CRACK *continues*

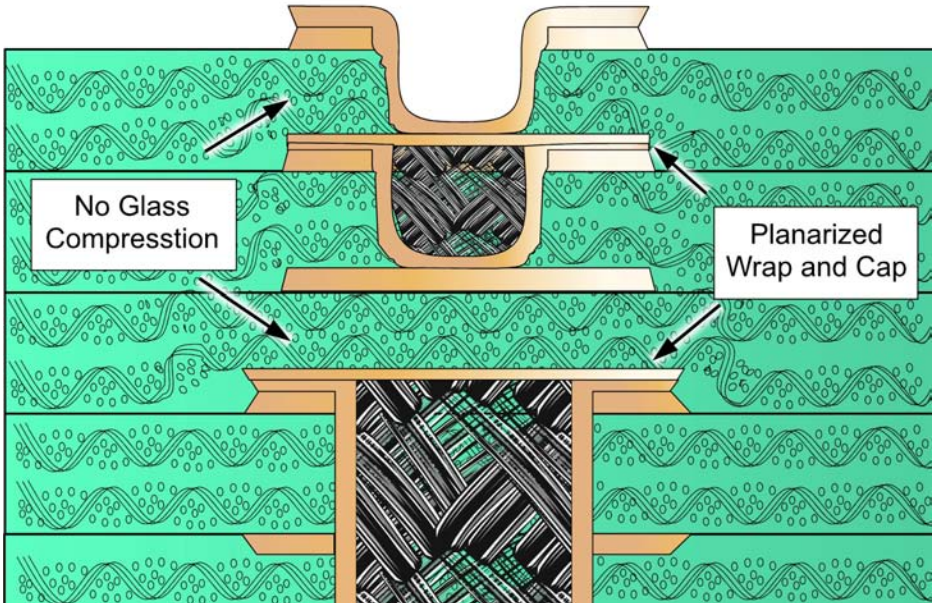


Figure 2: Planarization of the cap and wrap.

and 30.5 µm of copper for the copper cap. In this case, we have a total of 76.2 µm (.003″) of copper sticking up into the dielectric. If we use 127 µm (.005″) of dielectric after lamination, a post of copper sticks up into the dielectric 76.2 µm, thus reducing the dielectric spacing down to 50.8 µm (.002″). This means that the glass in the dielectric will be compressed during the lamination step. The compression of the glass fibers makes an area between layers that has reduced amount of resin. This compression of the glass fibers can be described as glass lock or in extreme cases can produce a glass crack.

To eliminate this condition of glass lock or glass crack, the fabricator frequently planarizes, or skives, the copper circuits before the cap is plated. This is done to reduce the copper thickness of the wrap and produce a smooth surface. Planarization is done on both sides of the core. The problem is that the core may have variation in the copper plating thicknesses due to current distribution problems. Although the copper is supposed to be 30.5 µm (.0012″) thick, it may be as low as 20.3 µm (.00079″) thick in some areas or on the opposite site of the board. So the planarization step needs to be controlled to skive aggressively on the 30.5 µm (.0012″) circuit and less aggressively on the circuit that has 17.8 µm (.0007″) of copper plating.

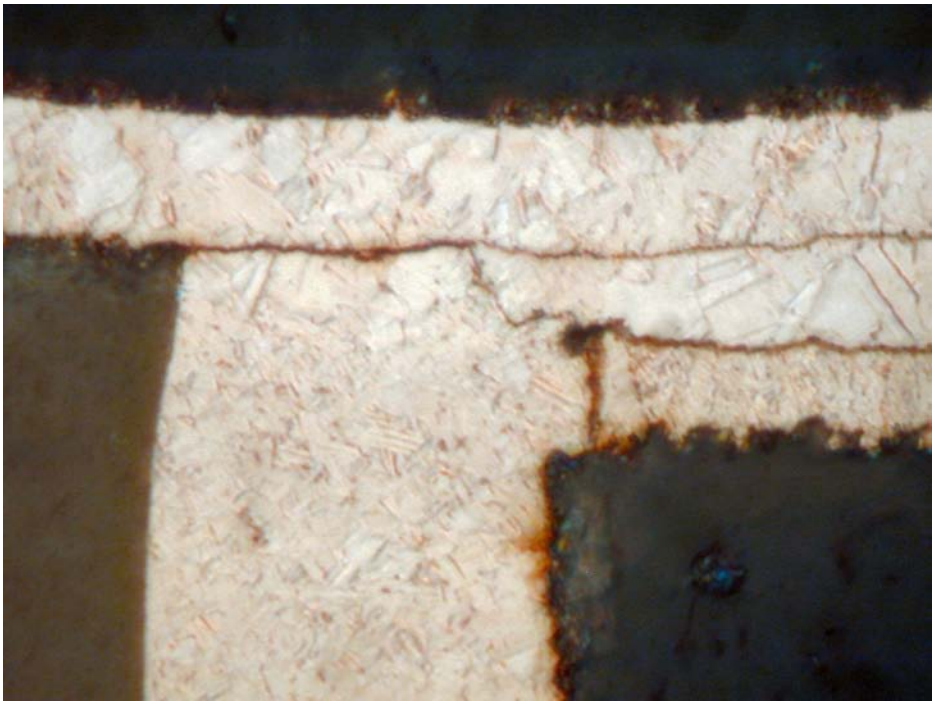


Figure 3: Photo showing wrap crack.

Next, the core is subjected to electroless and electrolytic copper plating and the cap is produced. After etching, the core may be planarized or skived again to produce a smooth surface and reduce the thickness of the cap.

One study showed that a wrap that is 5.0 µm (.0002″) thick is robust where as a wrap of less than 5.0 µm is prone to early failure. Based on this, I think a wrap of 10.1 µm (.0004″) is adequate to provide a guard band. The same is true for the cap. A

cap of 5.0 µm seems to be robust in most applications, so I would make the requirement to be 10.1 µm as a guard band. IPC-6012 specifies that the wrap and cap will be a minimum of 12 µm (.00047") and the cap will be 12 µm. Add to that the thickness of the foil, in this case 15.2 µm (.0006"). This makes the minimum copper sticking up into the dielectric a total of 38.1 µm (.0015").

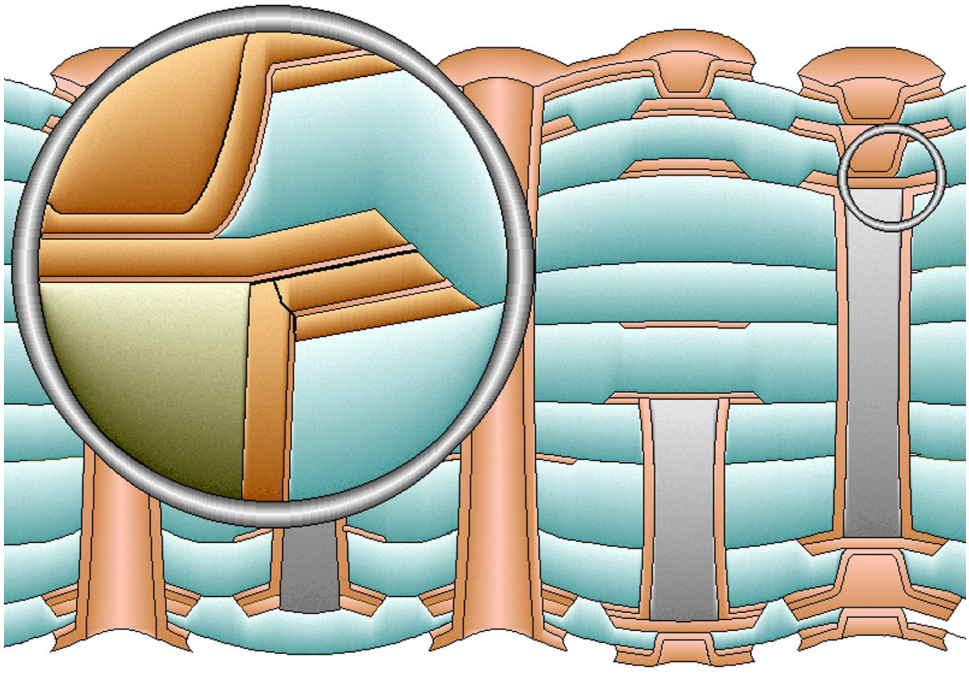


Figure 4: Animation of a wrap crack. Click **here** for animation.

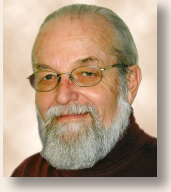
To understand the role of the cap in circuits we have to understand how the electricity flow through the buried via (see Reid on Reliability: Lifted Pad Stacked Microvia Failure). What we find is that if the cap forms the target pad for a microvia, it becomes an integral part of the circuit and a crack between the cap and the wrap will produce an open. A cap that is not part of a stacked microvia can have a crack and it will not cause an open. If the cap is not part of a stacked structure it can come completely off of the microvia or buried via and the electrical path will still be intact.

A microvia or buried via which has a wrap crack type of failure presents itself as an accelerated or a wear out type damage accumulation. Usually the cycles to failure are reduced to between 100 to 200 cycles. This failure mode starts with a crack from the corner of the dielectric. The crack progresses up the face of the copper foil and then across the knee of the wrap, usually at a 45° angle. The crack can then propagate horizontally between the wrap and the cap. In Figure 4, note that the crack has trapped moisture, resulting in oxidation between the cap and the wrap.

The fill in the buried or microvia is very important. The cap on top of the buried via produces what can be best described as a "pipe bomb." The cap traps the fill inside the buried via. Unlike the dielectric the fill is not constrained with X- or Y-axis glass fibers. The fill is expanding to all directions, X, Y and Z. Because there is more dielectric in the Z-axis the amount of pressure pushing up on the cap is greater than the X- and Y-axis pressure.

One of the factors of concern is the coefficient of thermal expansion of the fill as compared to the dielectric. While this is an important factor I believe the T_g of the fill is a bigger factor. With a T_g mismatch, the dielectric in the hole of the buried via can expand at a significantly higher rate than the surrounding dielectric until the T_g of the surrounding dielectric is reached.

The best fill is the A-stage fill of the dielectric. If one can get the A-stage dielectric and use this as the fill, the T_g will be matched and the whole buried via will have the same thermal expansion at a given temperature. **PCBDESIGN**



Paul Reid is program coordinator at PWB Interconnect Solutions, where his duties include reliability testing, failure analysis material analysis and PWB reliability consulting.

TOP TEN

Most-Read News Highlights from PCB007 this Month

① Basista Banks on Continuous Capability Enhancements

Basista Leiterplatten GmbH, based in Bottrop, Germany, specializes in the production of circuit board prototypes and small production runs of the highest quality. The circuit board manufacturer enjoys an outstanding reputation among its large client base. With the continual modernization of his company, Peter Basista not only guides the development of the market, he anticipates it.

② Italy's Somacis Buys San Diego's Hallmark Circuits

"Hallmark has outstanding employees and with our plans to make further investments, we will be expanding Hallmark's capability and capacity to meet our customers' growing requirement," said Giovanti Tridenti, Somacis Spa CEO.

③ Fire at Viasystems Guangzhou China Facility

Early on the morning of September 5, 2012, Viasystems experienced a fire contained in part of one building on the campus of its PCB manufacturing facility in Guangzhou City, China.

④ TTM Technologies Becomes First Certified Zeta Fabricator

PCB manufacturer TTM Technologies of Santa Ana, California, will be the first factory certified to produce PCBs using Integral Technology's revolutionary Zeta dielectric films.

5 AT&S to Build New Factory in Chongqing, China

China and coastal industries globally are rapidly developing their businesses in inland China, with Chongqing Liangjiang New Area – one of three national developments – becoming an investment highland for European enterprises.

6 Graphic Plc Acquires Printca Denmark

This acquisition will reinforce the position of Graphic Plc as a global leader in manufacturing complex advanced technology PCBs in the high-reliability segment of defence, aerospace, medical, industrial, telecommunications, and other special markets.

7 Invotec Achieves Record Sales in July

Sales output figures for Invotec reached a record high of over €2.7 million in July. New Managing Director Tim Tatton said, "These figures are great news and they demonstrate our proven ability in supplying time critical, high-technology PCBs. This is very encouraging against the back-drop of pessimism and uncertainty that continues to weigh heavily on the global economy."

8 Advanced Circuits Expands Colorado Facility

The additional space will provide for the introduction of additional capital equipment investment and not only provide for cost efficiencies, but also enable the expansion of current capabilities at the Aurora location which is well-known in the industry for its expedited turn-time capabilities and reliable early and on-time shipments.

9 Schweizer's PCB Segment Sees 41% Growth in 1H

Schweizer Electronic AG announced its financial figures for the first half of 2012. Within this period the company could achieve sales revenues of €53.7 million, compared to €58 million the previous year. The EBIT margin amounted to 6.9% (previous year 9.8%). Hence Schweizer confirms the revised forecast for the full financial year published on July 5 and, in view of the economic framework conditions, considers themselves well on target.

10 eXception Strengthens Capabilities, Boosts Investments

Despite evidence that the UK manufacturing sector is shrinking, eXception Group, a UK-based PCB and contract electronic manufacturer, is seeing continued growth. Increased investment in staff, processes, and equipment is allowing the company to weather the eurozone crisis, and buck the downward trend that has blighted the manufacturing sector to date.

Increasing Efficiency with PCB Design-Through-Manufacturing Automation

by John Isaac
MENTOR GRAPHICS CORP.

SUMMARY: ***Many companies are struggling to keep up while using traditional PCB design and manufacturing techniques, and treating PCB design and manufacturing as two separate entities. But the design-through-manufacturing process, when automated properly, can increase efficiency and cut waste throughout the product development cycle.***

The high-tech world is under increasing pressure to deliver more differentiated products faster, and at reduced cost. Many companies are struggling to keep up while using traditional PCB design and manufacturing techniques. And I mean this as two separate entities, PCB design and PCB manufacturing, because they often seem to be completely disconnected. Instead, the design-through-manufacturing process should be thought of as a continuum, because that's exactly what it is. Only by changing thinking to see this as a continuum with feedback can companies compete in the near future.

The typical electronics company is not organized as a continuum. Rather, there is often a mysterious chasm between design and manufacturing, as illustrated in Figure 1. PCB design is performed following basic manufacturing rules and then the data is passed to the target manufacturer. The design may have followed these basic rules but may not be ready for high-volume, high-yield production. The manufacturer will test the design data and if they identify changes that could improve the yields or the cost of fabrication/assembly, they may request the designer to re-design. This process costs time and money.

Lack of automated production line optimization and real-time management of the assembly line is another problem in today's design-through-manufacturing continuum. Without automation, you will likely see higher-cost products and lower profits because of excess material inventories and inefficient production-line equipment utilization.

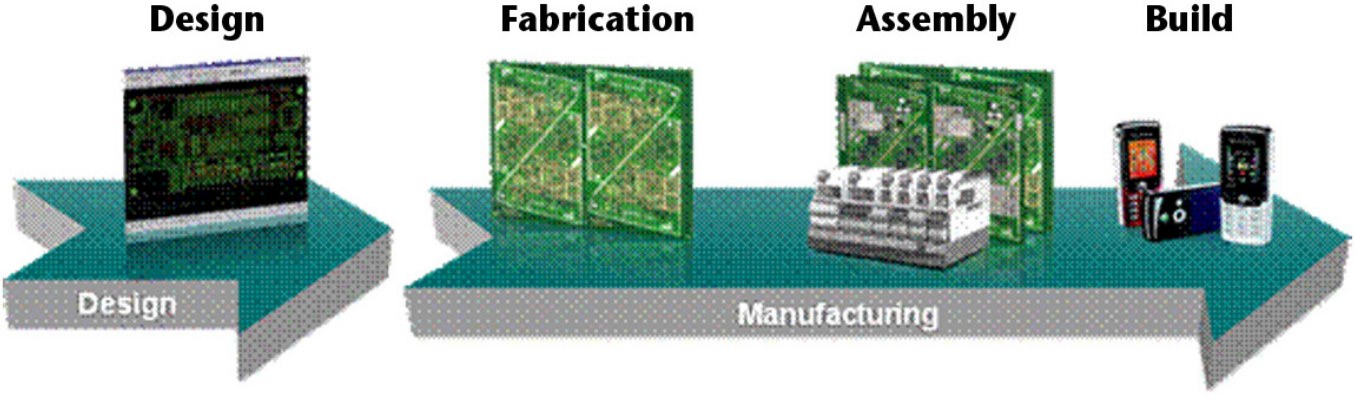


Figure 1: Lack of a continuum between design and manufacturing can lead to higher costs and longer time-to-market volumes.

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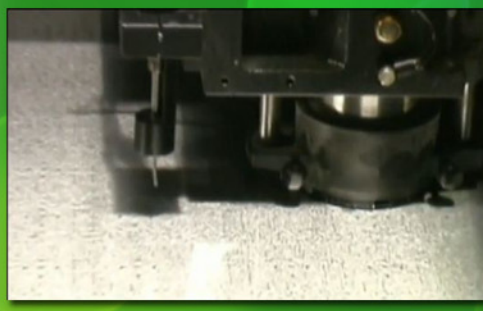

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Design-Through-Manufacturing Automation

The first opportunity for automation should start with design for manufacturability (DFM) analysis right at schematic entry and continue through the entire design process. During schematic entry, DFM requires communication with procurement and manufacturing organizations. As the schematic is created and parts are chosen, a bill of material (BOM) is generated from the design system and passed to procurement and manufacturing. Procurement then analyzes the BOM to make sure that the parts used can be procured in the volumes necessary and at the target costs. Likewise, manufacturing can assure that the chosen parts can be efficiently assembled and tested on the production line, thus reducing the cost of the product.

The next step is to ensure that the PCB can be fabricated, assembled and tested with high yields. The goal is to perform extensive checking during the PCB design process that not only highlights manufacturing violations that will cause hard failures, but also employs the manufacturer's best practices to ensure that the design data passed to the manufacturer will result in high yields without the need for design re-spins or significant changes by the manufacturer. Figure 2 illustrates this.

Design Transfer to Manufacturing

DFM checking during the design process should have taken us a long way to accelerating the setup for short time to volume production levels. Design now passes the data to manufacturing. In the past, the only method for passing this data was in the form of several separate files like Gerber, Excellon drill, NC routing, assembly drawings, etc. This method took the intelligent CAD data, where all of the inter-relationships were intact, and transformed it into disjointed segments, thus losing all of the intelligence. If the manufacturer wanted to optimize their manufacturing process for higher yields, they had to reverse engineer the data, and add the intelligence back in prior to any changes. This is an expensive and time-consuming process.

But intelligent data transfer protocols such as ODB++ maintain the inter-relationships of the data as it existed in the PCB CAD system. The manufacturer no longer has to reverse-engineer the data to reinstate the intelligence.

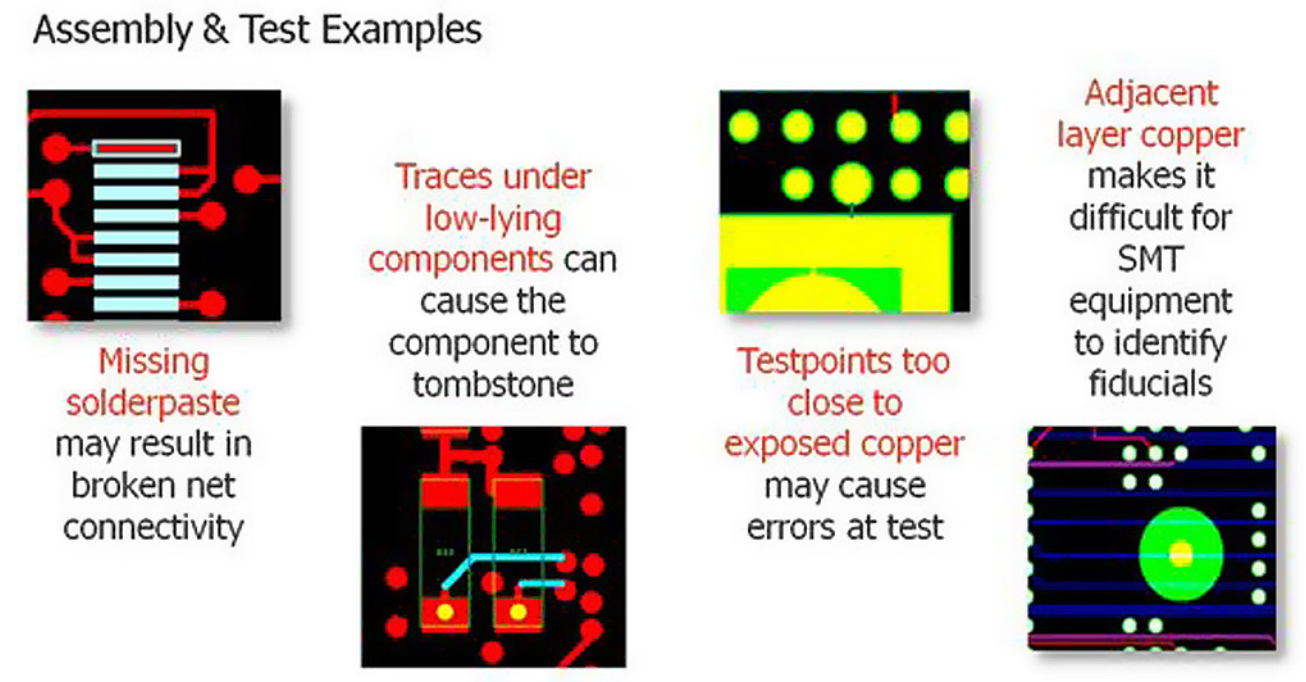

Figure 2: DFM checks can discover a variety of possible problems. These are just a few examples.

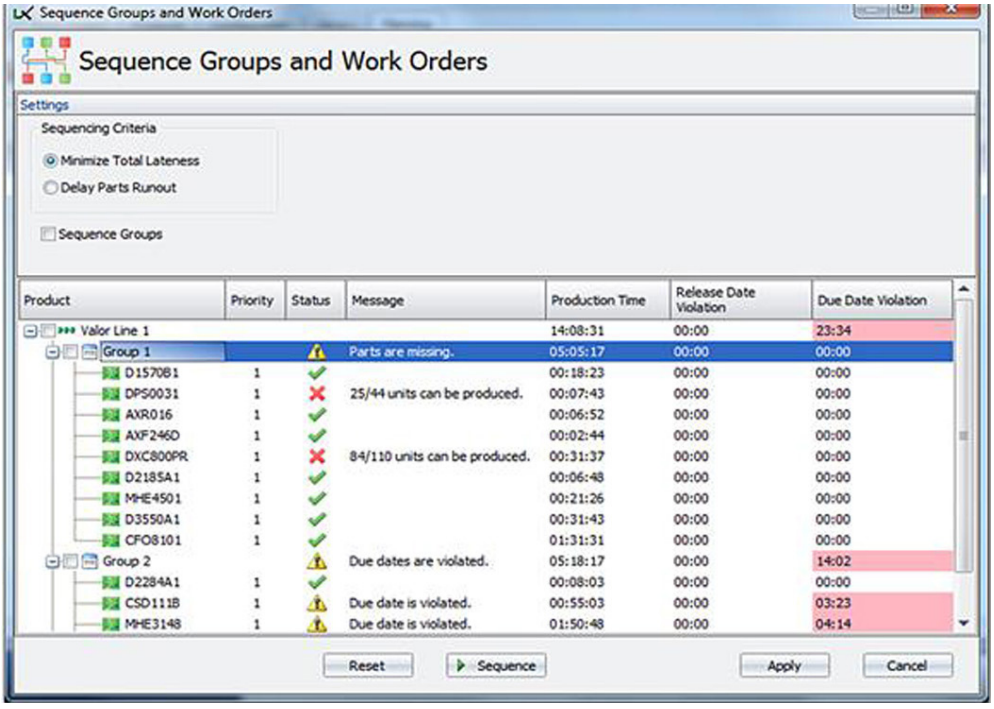

Figure 3: Optimizing the production line means most effective use of production machines and increased revenue.

Planning the Assembly Process

As a new assembly line is being configured in preparation for future cost-efficient production – for either high mix, high volume or both – simulation software (Figure 3) can aid in this process. This software can be utilized to simulate various line configurations combined with different product volumes and/or product mixes. The result is an accurate "what if?" simulation that lets process engineers try various machine types, feeder capacities and line configurations to find the best machine mix and utilization to meet their needs. Using line configuration tools, line balancers, and cycle time simulators, they can try a variety of machine platforms before deciding on the best line configurations to target for the specific product or family of products to be assembled. Once the line is set up, this same software maintains an internal model of each line for future design-specific or process-specific assembly operations.

The Production Line

Configuring and monitoring the running assembly line is a complex process but can be greatly improved with the right software support. Many elements of this complex process can be managed in real time by MES (manufacturing execution system) software.

Some parts will fail, and by capturing and analyzing this data, we can determine and correct the causes, thus increasing the line efficiency and product quality. One of the key benefits of this type of software is the ability to relate, in real time, the test and/or inspection failures with the specific machine(s) and process parameters used in assembly and the specific material vendors and lot codes used in the exact failure locations on the PCB. This data correlation and real-time visibility is crucial to maintaining a finely tuned manufacturing flow.

Feedback

At the beginning of this article we alluded to feedback being critical to the design-through-manufacturing automation process. Operating in a design-through-manufacturing continuum is a learning process. We can learn by actually manufacturing this or similar designs, and determine what additional best practices we might apply to DFM that could incrementally improve our process with increased yields or more optimum use of our manufacturing assets.

Data captured during the manufacturing process and during product failure analysis can be translated into improved best practices (Figure 4) and used to improve the effectiveness of DFM rules used by the designer. Continuous improvement of the DFM rule set based on real-world results can positively influence the design of the next product or, if the cost

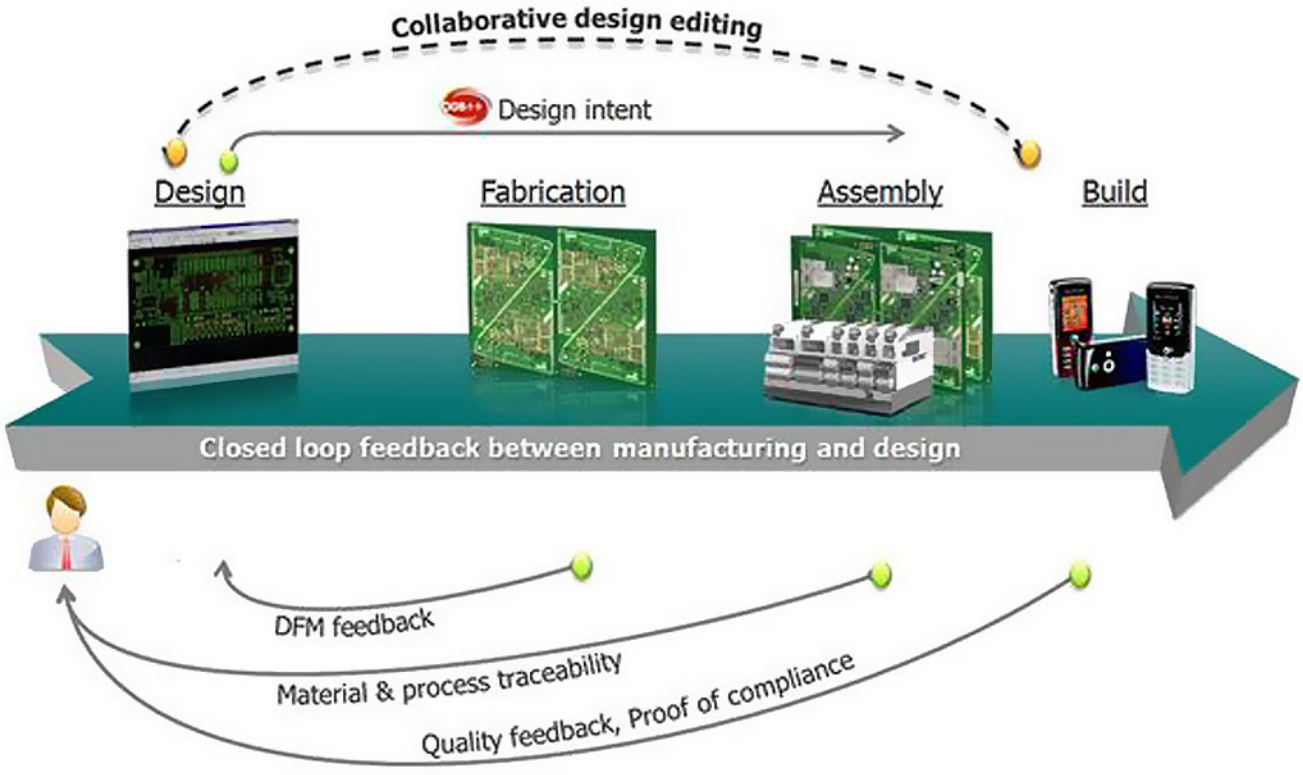

Figure 4: A design-through-manufacturing continuum, with the ability for improvement, can help an electronics company meet their goals.

change is significant enough, the yields of the current product.

The Design-Through-Manufacturing Continuum

Design-through-manufacturing should be treated as a continuum and supported with integrated manufacturing execution software. Start with the manufacturer's DFM rules, followed and checked by the designer's software, followed in turn by the transfer of data in intelligent form to the manufacturer. Then come the automated setup and optimization of the production line; the real-time monitoring and visibility of equipment; process and material performance; and finally, the capture, analysis and correlation of all failure data.

But the process does not end with product delivery, or even after the sale support. The idea of continuum is that there is no end. By capturing information from the shop floor, we can feed that back to previous steps (including design) to further cut unnecessary costs and produce more competitive products and enable a culture of real, continuous improvement. **PCBDESIGN**

John Isaac is director of market development. He has worked in the EDA industry with PCB and IC technology for more than 40 years. His career started with IBM where he managed the development of EDA systems for IBM's internal design of their high-end ICs and PCBs. He then joined Mentor Graphics where he has held marketing positions in both PCB and IC product areas. Isaac is currently responsible for worldwide market development for the Systems Design Division.

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Non-Contact Interconnect: When Crosstalk is Your Friend

by Bert Simonovich

SUMMARY: ***In normal PCB designs, crosstalk is due to electromagnetic coupling of two or more traces routed in close proximity to one another. We usually consider crosstalk to be our enemy in any high-speed design, and go to great lengths to avoid it. So how, you may ask, can crosstalk ever be your friend?***

In normal PCB designs, crosstalk is due to electromagnetic coupling of two or more traces routed in close proximity to one another. We usually consider crosstalk to be our enemy in any high-speed design, and go to great lengths to avoid it. So how, you may ask, can crosstalk ever be your friend?

To answer that question, I would like to start by taking you back to the fall of 1994. This was the era of wide parallel busses running up to 33 MHz across backplanes. High-speed serial, point-point interfaces, and SERDES technology, as we know and love today, were just a twinkle in some bright young engineer's eye.

Nortel, a.k.a. Northern Telecom, at the time, was looking to replace the computing module shelf of the DMS Supernode platform because it was projected to run out of steam a few years later. In order to address the issue, the system architects decided that a scalable, multiprocessing, shared memory computing architecture was needed to replace it.

My job was to develop a concept to package all these cards in a shelf, and then design a backplane to interconnect everything. It quickly became evident that a single shared bus could not support the bandwidth required for multiprocessing. Nor could multiple parallel buses solve the problem, because of the lack of high-density backplane connector technology needed for all the I/O. Even if we had a suitable connector, and it could magically fit within the confines of the card slot, then the layer count of the backplane would have to grow exponentially.

No, something else was definitely needed. Fortunately, Bell Northern Research (BNR), the R&D lab of Nortel where I was working at the time, had an advanced technology group that liked to play in the sand. I remember going to a meeting to see some presentations on the neat technology they were playing with.

One particular presentation they gave was of a unique non-contact interconnect technology. I immediately saw the practical application that technology offered for our architecture; it instantly became my friend. It allowed us to eventually invent a patented, proprietary point

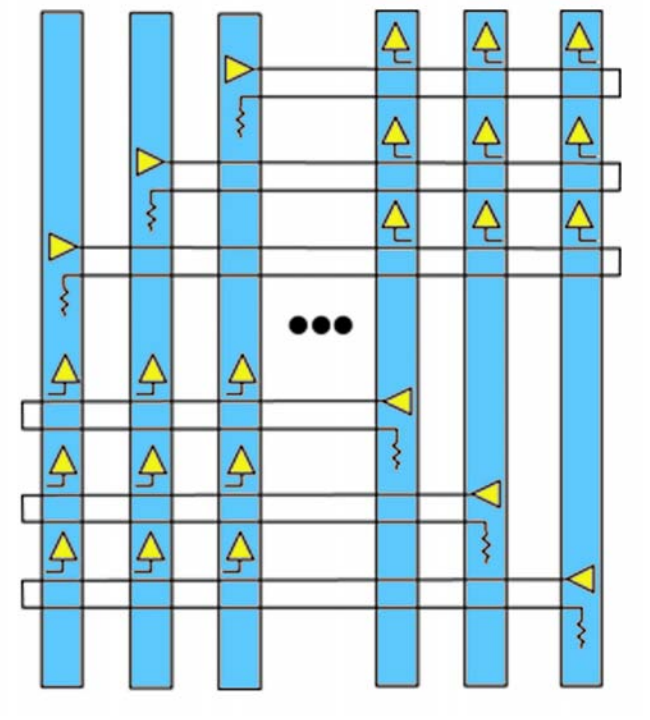

Figure 1: High-level block diagram illustrating the non-contact, point-to-multipoint interconnect concept.

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NON-CONTACT INTERCONNECT: WHEN CROSSTALK IS YOUR FRIEND *continues*

to multipoint interconnect solution, running at 1 GB/s per pair .

The non-contact technology actually relied on controlled electro-magnetic coupling, or simply, crosstalk (Figure 1). In this simple high-level block diagram example, each card on the shelf would transmit their data differentially across the backplane. As the differential pairs traversed through the connector fields of the card slots, the transmit signal was edge-coupled to adjacent small traces called couplers, which were about three quarters of an inch long. They were connected to their respective receiver pins on the plug-in cards. After the last card slot, they switched layers and returned back to the originating plug-in card, where they were terminated.

The beauty of this architecture was that each card only needed one transmitter to broadcast its data to all the other cards. Since each card had enough receivers to listen to the other cards, the point-to-multipoint interconnect achieved the equivalent of a multipoint-to-multipoint architecture, but without the overhead of additional pins and PCB layers. Furthermore, an effective line rate of 1 GB/s was achieved using simple, inexpensive 2 mm connectors; the same ones chosen for compact PCI standard.

Figure 2 is a photograph of an innerlayer, double-sided core of the backplane, prior to lamination and drilling. It shows the couplers in more detail. The round pads are for the connector vias, and are used to attach the coupler traces to the connector pins. Differential receivers are connected to these pins on a plug-in card. The rows of pads on the left are for one card slot, while the rows of pads on the right are for another.

If we look at the two traces, entering the picture from the bottom, left side, they are part of a differential pair, connected to a transmitter. Each pair was routed using single-ended traces (i.e., with no coupling to one another). As these traces approach the first row of pads, they jog down to ensure close coupling to the coupler traces attached to the pads. The close coupling continues to the next set of pads, and the pattern starts all over again, as the pair exits the picture at the bottom right (Figure 2). This pattern repeats all the way up the photo for each differential pair.

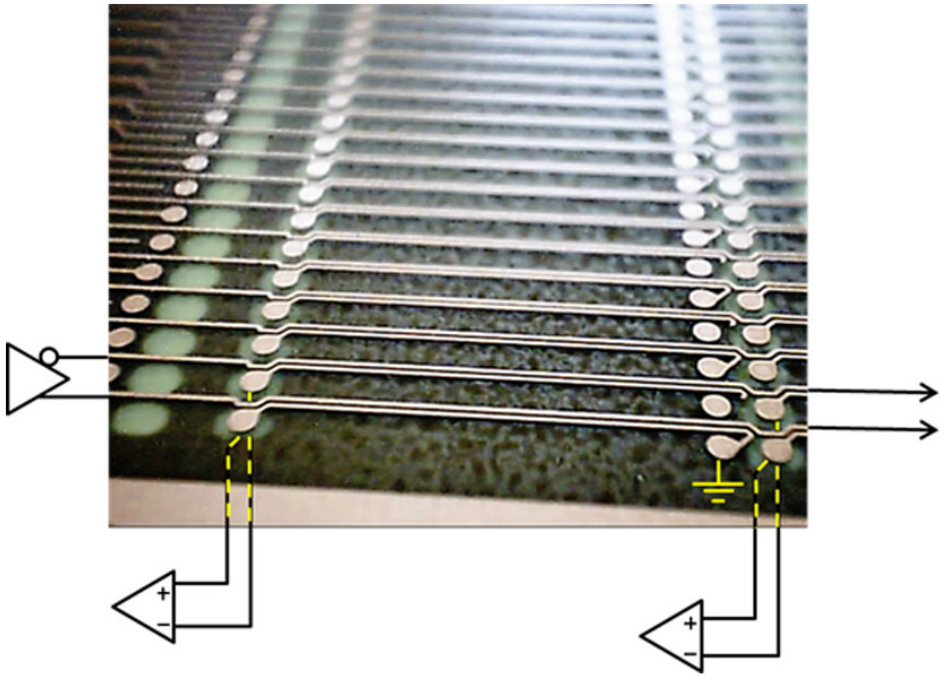

Figure 2: Photograph of an innerlayer, double-sided core of the backplane, prior to lamination and drilling showing the routing of the couplers.

You may be astute enough to notice that the bottom coupler trace connects to a grounded pad at the farend, while the mate coupler above it does not. Obviously this was intentional, but why was it done? The following explains some of the physics behind this patented technology .

When two coplanar parallel traces are in close proximity to one another, there are two types of crosstalk generated: backward, or near-end crosstalk (NEXT), and forward, or far-end crosstalk (FEXT). Generally speaking, traces routed in stripline are only susceptible to

NEXT, while in microstrip, they are susceptible to both. Since non-contact technology relies on NEXT, all routing was done in stripline.

As the transmit signal propagates, from left to right in Figure 2, the rising and falling edges of the transmit signal initiates NEXT at the beginning of the coupled length (near-end). The NEXT voltage saturates after a critical length equal to the risetime (tr) divided by twice the propagation delay (2tpd), where the rise time is in seconds, and propagation delay is in seconds per unit length. It stays saturated for twice the time delay (2TD) of the coupled length. Because of differential signalling, NEXT voltages have opposite phase on the respective couplers (odd-mode).

At the coupler via, there is a reflection caused by the impedance discontinuity of the via and connector pin. This reflection propagates towards the far end of the coupler (left to right). If both couplers at the far end are left open, any secondary reflections reflect back towards the receiver again in odd-mode. When both reflections arrive back at the receiver, they will add together and combine with the received signal. This causes inter-symbol interference, as seen by the shoulder on the trailing edges, on the eye waveform in Figure 3A.

By leaving one far-end coupler open, and shorting the other one to ground, any secondary noise that is reflected will have the same phase (even-mode). When they arrive back at the receiver, they will cancel, thereby eliminating the inter-symbol interference, and increasing the eye amplitude, as shown in Figure 3B.

You will notice that the eye waveforms do not resemble the traditional eye diagram we are used to seeing. Instead we observe a typical NEXT eye, when the coupled length is short, compared to the bit time. There is also a line right in the middle.

Figure 4 can help to explain the reason. The blue waveform is the NEXT voltage, seen at the near-end of the coupler, in response to the red transmitted waveform. Notice that there are only pulses at an edge transition of the transmitted waveform. A rising edge creates a positive pulse, and a falling edge generates a negative pulse. The duration of each pulse is twice the time delay of the coupler length.

The receiver uses simple peak-detectors and latch to regenerate the signal back to the original waveform. A positive going pulse is detected by the positive peak-detector. When it crosses the positive voltage threshold ($+V_{th}$), it sets the latch output to logic high. The output remains

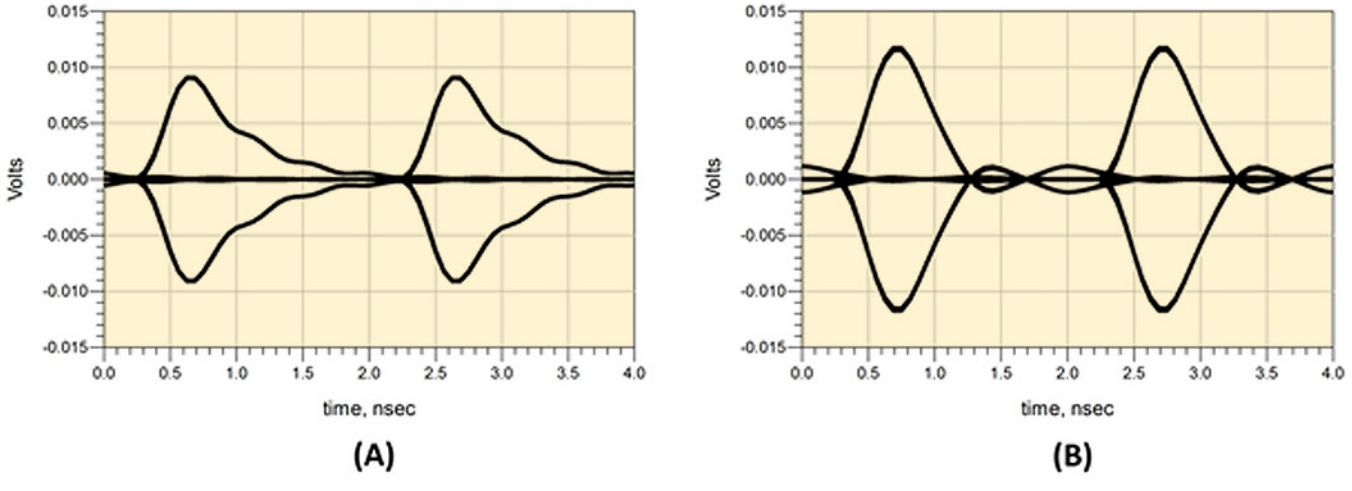

Figure 3: Simulated PRBS eye diagrams at the receiver when both couplers are left open at the end (A), vs. one coupler being shorted to ground and the other left floating (B). Reflections from the coupler via cause the inter-symbol interference and reduced amplitude in (A) compared to (B). Simulated and plotted with Agilent ADS.

NON-CONTACT INTERCONNECT: WHEN CROSSTALK IS YOUR FRIEND *continues*

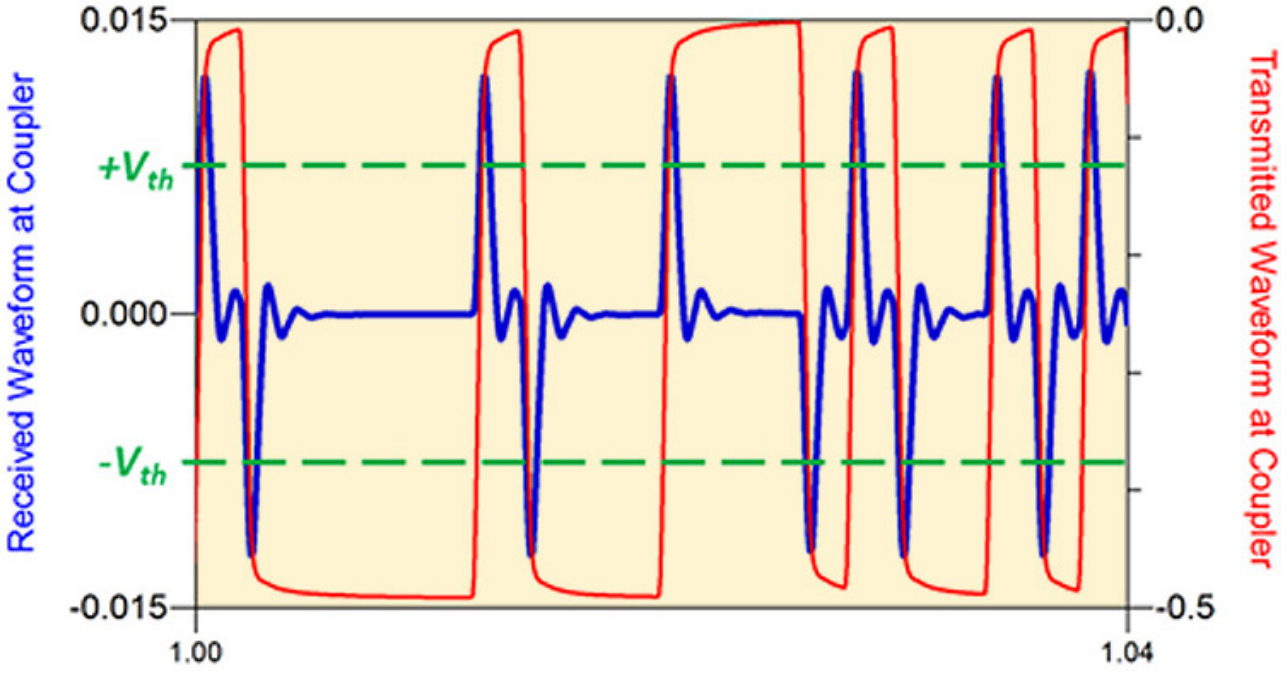

Figure 4: Near-end coupled waveform (blue) in response to the transmitted waveform (red) at the coupler. The green dashed markers are the positive and negative voltage thresholds of the respective peak detectors in the receiver. Simulated and plotted with Agilent ADS.

high until a negative pulse crosses the negative threshold ($-V_{th}$), of the negative peak-detector, and resets the latch to logic low.

And that is how crosstalk can be your friend!

Of course the small coupled crosstalk signal means we have to guard against crosstalk from other digital signals on board. But that's nothing that mixed-signal layout design rules can't solve.

Wait a minute! We both share the same enemy? Who would have thought the old Proverb "The enemy of my enemy is my friend" [sic], would apply here too? **PCBDESIGN**

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Bert Simonovich is the founder of Lamsim Enterprises Inc., where he continues to provide innovative signal integrity and backplane solutions to clients as a consultant. With three patent applications and two patent grants to his name, he has also (co)authored several publications, including an award-winning DesignCon2009 paper related to PCB via modeling. His current research interests include signal integrity, high-speed characterization, and modeling of high-speed serial links associated with backplane interconnects.

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Sunstone Highlights Expansion With Open House

Sunstone Circuits celebrated the completion of a new administration and office building by hosting an open house on October 25, 2012. The festivities were held at the company's corporate headquarters just south of Portland, Oregon.

The new building, which houses Customer Service, Finance, Marketing, Human Resources and Executive Management, represents Sunstone's continued growth and commitment to serving customers 24/7/365. Sunstone is not only improving the facilities and the work environment for the Sunstone staff, but also providing jobs and community development within Sunstone's local area.

For the estimated 80 guests on hand, Sunstone offered food and refreshments, live guitar music, tours of the manufacturing campus, and an opportunity for customers and vendors to meet employees from all departments across the Sunstone team. On the plant tours, visitors were impressed by the high level of personal human touch Sunstone employs alongside all of the automated manufacturing processes.

Visitors to the open house toured the manufacturing plant to see how printed circuit boards are made.

Ethology's Kent Schnepp and Amy Simpson visit with Sunstone President and CEO Terry Heilman (right) during the open house.

Longtime Sunstone customer Allen Siefken (left) visits with David Warren of Sunstone's Sales & Business development department.

Attendees included customers from the region, including Electro Scientific Industries, ECD, GEKCO, Maxcess, and Coherent, among others. Staff from Portland State University and Clackamas Community College, both active participants in Sunstone's educational sponsorship programs, also paid a visit. Some of the other leading businesses in the area attended, including Columbia Helicopters, IEC, Technica, UPS and FedEx. A number of local vendors and key agency partners, including Copious, Xenium, ethology, ServiceMaster, Molalla Telecommunications, Arrowhead Golf Club and law firm Tonkon Corp. rounded out the guest list.

events

For the IPC's Calendar of Events, click here.

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For the iNEMI Calendar, click here.

For a complete listing of events, check out *PCB007* full events calendar here.

Defence IQ's Military Radar Conference
November 27-29, 2012
Portland Place, London, UK

6th International Symposium on Tin Whiskers
Novermber 27-28, 2012
Ford College, Loughborough University
Leicestershire, UK

HKPCA Show 2012
November 28-30, 2012
Shenzen Convention & Exhibition Center,
Shenzen, China

2012 International Printed Circuit & Electronics Assembly Fair
November 28-30, 2012
Shenzhen, China

NCEDAR 2012: National Conference on Electronics Design, Assembly and Reliability
December 4-6, 2012
Bangalore, India

BIOMEDevice
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San Jose, California, USA

Printed Electronics USA 2012
December 5-6, 2012
Santa Clara, California, USA

Renewable Energy World Conference & Exhibition North America
December 11-13, 2012
Orlando, Florida, USA

DesignCon 2013
January 28-31, 2013
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Next Month in *The PCB Design Magazine*

The best route for placement and routing information runs through the December issue of *The PCB Design Magazine,* with feature articles by Barry Olney and Scott Fillebrown. And we'll take a look back at some of the biggest PCB design news of 2012, while looking forward to 2013 and beyond.

See you in December!