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September 2013

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MATERIALS

Key Factors Influencing Laminate Material Selection for Today's PCBs

by Steve Iketani and Brian Nelson

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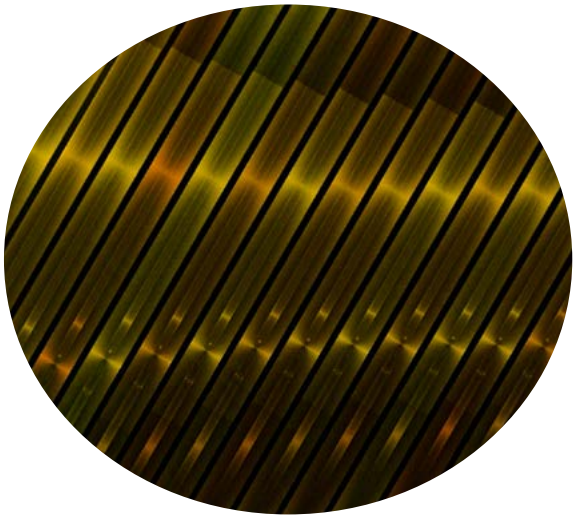
This Issue: MATERIALS

FEATURED CONTENT

Matching the right PCB material for your board's requirements can be a daunting task, especially when designing high-speed PCBs. In this issue of *The PCB Design Magazine,* our experts make sense of the myriad of materials available today, describing various techniques for making the most of your substrate.



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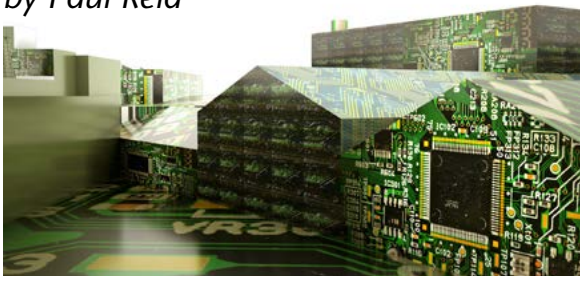

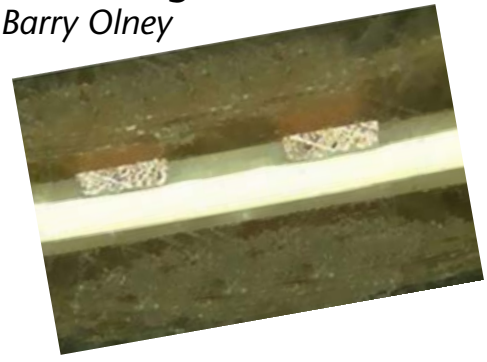

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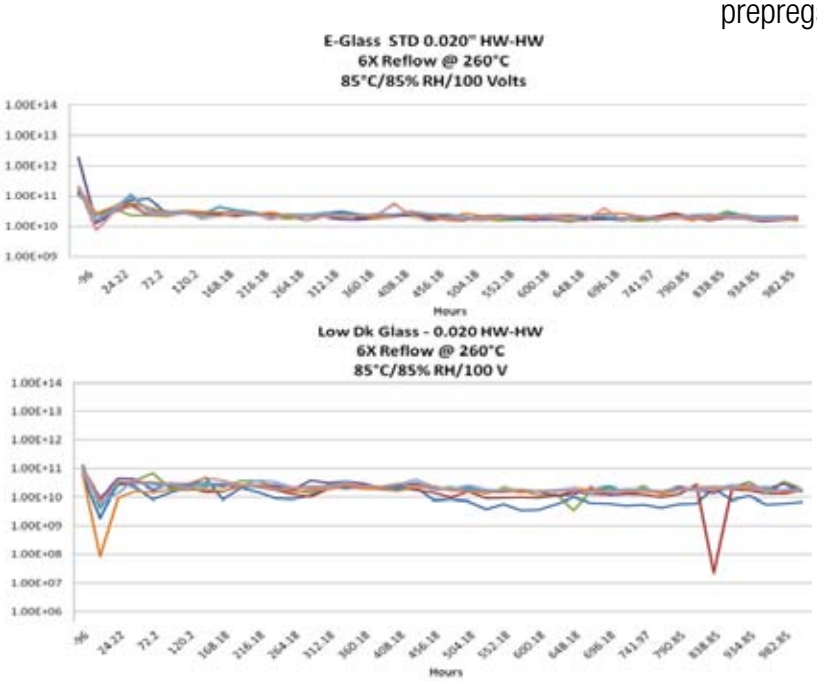

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THE SHAUGHNESSY REPORT

A Time for New Ideas

by Andy Shaughnessy
I-CONNECT007

Usually, I hate to see the end of summer, but this year I'm ready for fall. This summer it rained just about every day in Atlanta. My basement flooded; it wasn't much water, but it still smells like mildew down there.

I'm just sick of rain. At this point, I'd almost rather have snow.

And I just turned 50, so I'm anxious to get started on my second half-century. My girlfriend and I went zip-lining and we survived. If you get the chance to go zip-lining, do it. The thousand-foot runs are insane!

Years ago, I thought 50 was old, but now I think it's just right. I guess 50 is a little past middle age, unless I live to be 100. They say your body starts to fall apart around 50, and I'm anxious to see which parts go first. I should be OK for a decade or two. I exercise fairly regularly, and I've just about quit eating fried foods, which is tough in the South. I never saw deep-fried pimento cheese until I moved to Atlanta.

But if we mature folks don't take care of ourselves, we won't be around long. The same holds true for this mature industry of ours. Companies that don't evolve and adapt won't be around long.

At this rate, there won't be anyone left in this industry in 30 years. We have to attract more young people to the world of PCB design, fabrication and assembly. I may be 50, but odds are I'm still younger than just about anyone reading this. That's nice for me, but it's bad for the future.

I'm heading to PCB Design Conference West, and I guarantee I'll be one of the youngest attendees, just like I was at my first design show in the 1990s. How often do you see recent grads at any of the trade shows in our industry? You might see a handful of marketing folks who were born in the '80s, but most trade shows that focus on the PCB industry (design, fab or assembly) could be mistaken for AARP meetings.

Have you heard of such drastic "graybearding" in any other segments of the electronics industry? What can we do to start attracting bright, young talent? I wish I knew.

Like me, our industry is mature. Not that there's anything wrong

with being mature. We middle-aged folks have a lot of experience, and plenty of stories to tell. I remember when the biggest exhibitors at DAC used to brag about spending nearly $1 million on their booth and travel expenses. Does anyone believe we'll ever see spending like that again? I bet Synopsys has filed that under the heading, "It seemed like a good idea at the time."

Changing Things Up

It's popular to bash trade show managers when they have crazy ideas, but to be intellectually honest, we have to hand out "atta boys" when they're due. One good example is PCB West. Just a few years ago, PCB West seemed to be in dire straits. Down to about 30 exhibitors, things were not looking good. But this year, the expo boasts 75 exhibitors. UP Media Group is clearly doing something right.

"You rarely see one-day expos, with the exception of SMTA's regional one-day tabletop shows. Conventional wisdom has long held that no company would ship their booths, equipment and people across the country for an expo that lasted just one day. Hell, it takes a whole day just to set up an expo."

It may be due to their decision to embrace the one-day expo format, an idea that goes against all the "expert" research on trade shows that I've ever read. You rarely see one-day expos, with the exception of SMTA's regional one-day tabletop shows. Conventional wisdom has long held that no company would ship their booths, equipment and people across the country for an expo that lasted just one day. Hell, it takes a whole day just to set up an expo.

But the conventional wisdom was wrong. Ever since the one-day format was introduced, more exhibitors have been signing on at PCB West. The Santa Clara Convention Center added on a space that's perfect for smaller (i.e., not DesignCon) shows, and PCB West fills it up. It doesn't hurt that the show is anchored by a three-day technical design conference; some of these attendees have said that they'd attend this conference in Alaska if they had to.

It's good to see shows in our industry growing. The big question: Is PCB West big enough to bring back the Porch Dawgs blues band?

I also have to give IPC and SMTA credit for changing things up. Last year, the leaders of IPC and SMTA met and found common ground, as they should have years ago. They decided to hold IPC's midyear meetings, normally held at IPC Midwest, at SMTA International, and IPC Midwest was eliminated. This was great news for exhibitors who have grumbled that they couldn't afford to attend APEX, IPC Midwest and SMTAI. In October, we'll get to see the fruits of this merger at SMTAI in Ft. Worth.

And IPC has brought back the Technology Market Research Conference & IPC Management Meetings (TMRC). I don't know of any other event that provides so much current information about PCB manufacturing. When I first started covering fabrication, TMRC was a lifesaver. I felt like I was drinking water out of a fire hose. TMRC takes place the same week as PCB West, the week of September 23. Funny how that worked out.

Finally, DesignCon and APEX are right around the corner. This year, APEX returns to Las Vegas. I think people are split on the Vegas location—you either love it or you hate it. All I remember is having sore feet from walking, walking, and more walking.

So, take care of yourself, and try to think of ways we can improve our industry and make it attractive to "new blood." I've met some brilliant young people lately, but most of them have never heard of a PCB. We need to change that, and soon. **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 13 years. He can be reached by clicking here.

Key Factors Influencing Laminate Material Selection for Today's PCBs

by Steve Iketani and Brian Nelson
SANMINA

SUMMARY: Recently, there has been a flurry of new and promising laminate materials entering the market, coming from the four corners of the world. Sanmina's Steve Iketani and Brian Nelson offer their take on materials, from FR-4 to low-Df/Dk laminates, and much more.

Ever greater miniaturization of electronic equipment and its circuitry, along with increasing data traffic rates, continuously pushes the PCB industry to improve performance. The compression of development cycle times has been ongoing for some time, but recently this has created a tsunami-like impact on PCB fabrication, especially in laminate materials. In order for design engineers to find solutions for increasing speed and signal integrity management in PCBs, they must keep up with the constant evolution of laminate materials, primarily on their loss performance attributes.

Today, we are seeing wave after wave of new materials that target improved cost as well as improved performance. Some efforts are in cost reductions at the current performance levels (Figure 1), and other entries are designed to improve performance while attempting to stay at par with existing price levels (Figure 2). These performance-enhanced issuances tend to fall into the spaces between traditional class groupings, creating a more continuous suite of laminate offerings. As a result, there are more tailored choice options for any specific design application, rather than having to select either an over or under laminate available for specification.

The source area for higher-speed materials has been rapidly widening. In the early 2000s, most higher-speed materials came from the US and Japan. Today, materials are being sourced from Taiwan, Korea, Singapore, Hong Kong, and China. The companies and materials may not have the same maturity and application knowledge that the industry is accustomed to, depending upon the manufacturer, its experience, and the duration an offering has been in the market. Despite this general disadvantage, new laminate players continue to charge into the market, providing many materials of lim-

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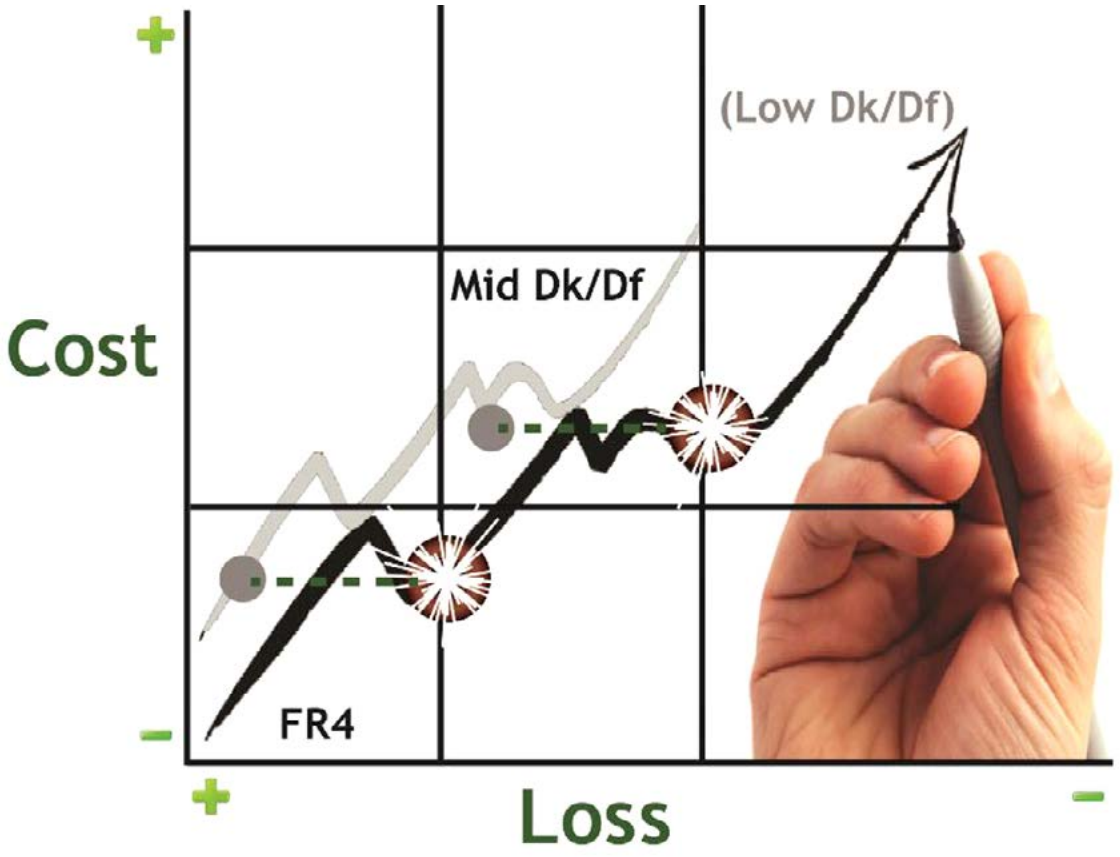

Figure 1. Some efforts address reducing costs at current performance levels.

ited data and background. A large sampling of laminates are plotted for S21 loss at 10GHz in Figure 3, which shows there are many competitive materials available with only incremental performance differences, and a nearly linear slope of options from top to bottom.

FR-4 Class Laminates

PCB material discussions often use FR-4 as a baseline for comparison of material behaviors and, especially, processability. FR-4 will continue to persist in product builds for both its thermal-mechanical strength (a valuable attribute for HDI fabs) and, of course, for its relative low cost. To continue to be in play, FR-4 also needs to provide at least acceptable limits of electrical performance coherent with transmission rates of interest. This has not been a great attribute of FR-4 historically, and our experience points to a maximum usable data rate of around 5–6 Gbps, depending on the design trace widths and routing lengths. The major impediment of using FR-4 is usually its loss tangent (Df). Yet, there have been some industry trends mitigating the loss aspect of FR-4, extending its potential use.

OEM pressure on laminate manufacturers, which began around the time of the then-new requirement to withstand leadfree assembly solder excursions, lead to some other concurrent enhancements and opened up a sub-class within a class: FR-4 resins modified and/or blended in a manner that resulted in some achieving as much as 1/3 reductions in rated Df compared to traditional FR-4s. These select offerings continue in the market, as they present Df improvements at measurably less cost than mid-Dk/Df class entrants, although these modified FR-4s do not enjoy much, if any, of the dielectric constant enhancements of the mid-Dk/Df class.

Even more to this point is the impact of halogen-free on the Df of FR-4. The change is from brominated flame retardants to non-brominated replacements that incidentally require lower content within the resin for effectiveness,

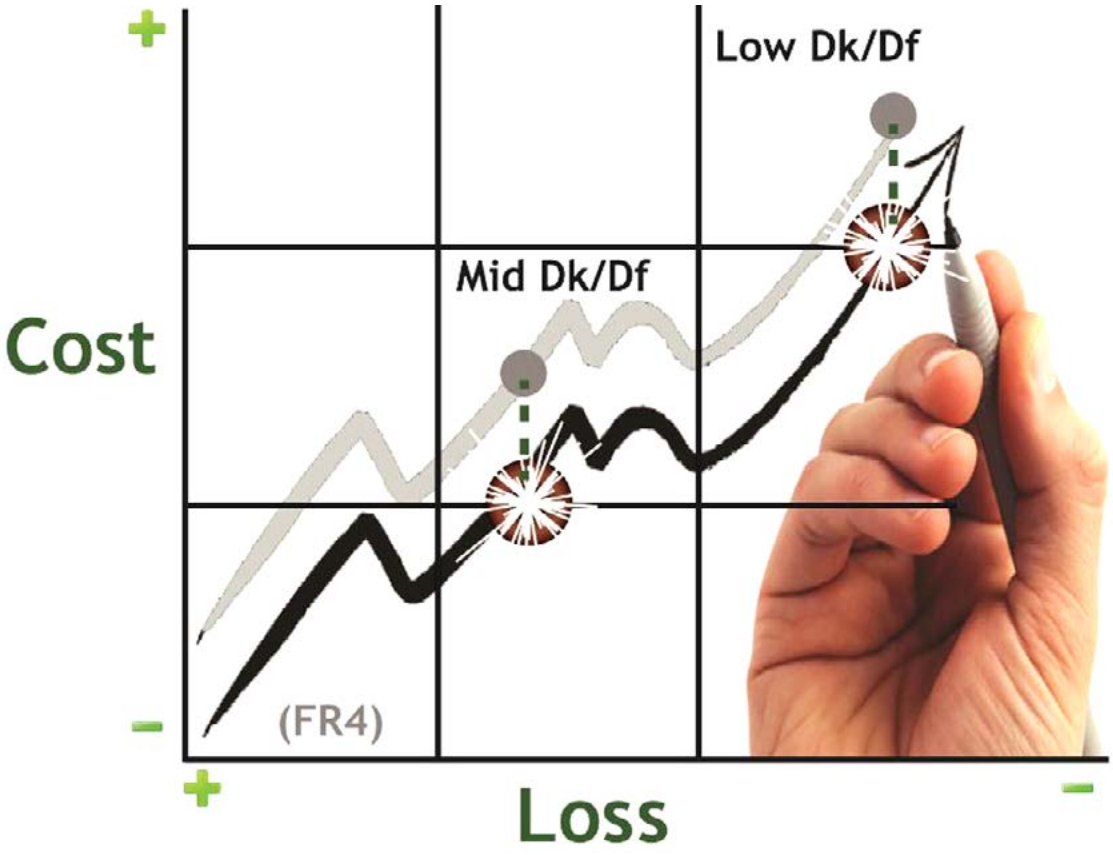

Figure 2. Other efforts focus on increasing performance while staying at today's price point.

that being the ability to conform and certify to UL94VO flame. This flame-retardant change has a measurable impact on Df. Many have taken note of halogen-free FR-4s, with Df ratings in the range of 0.010– 0.016 and at measurably lower cost than many of the mid-Dk/Df class materials. Ultimately, the mid-Dk/Df materials have loss tangents available that are lower still, well down into the 0.008 range, but at an appreciable cost premium.

Financial budgets, as well as loss budgets, tend to dictate the want and feasibility of using lowered Df FR-4s as opposed to opting into a mid Dk/Df material. As cost is always a focal point, most designs opt for the least costly laminate that will deliver the performance attributes needed for that design application. Using over-engineered material for a design application is more often the fault of market offerings forcing designs to over-buy on unneeded attributes in order to acquire the needed ones. As the material market continues to fatten out its class offerings, using over-engineered materials becomes less necessary. This is further demonstrated by the limited but available option of acquiring select lead-free FR-4 items on spread weave glass styles. As the primary benefit of these styles has been mitigation of differential impedance timing skew, these FR-4 offerings are targeting a specific performance aspect, whereas before these premium glass styles were only available bundled with higher performance resin systems.

Lower-profile copper options, those smoother than reverse-treated foil (RTF), have not really appeared in FR-4s. We believe this is because greater trace loss benefit can be realized by investing in other lower-Df resin systems rather than using cost premiums to clad relatively lossy FR-4 with finely surfaced coppers. Leadfree FR-4s also enjoy regular use in high-speed applications as part of stackup hybridization, reducing cost by being relegated to power, ground, analog and other non-critical layers, while often improving the overall thermal-mechanical

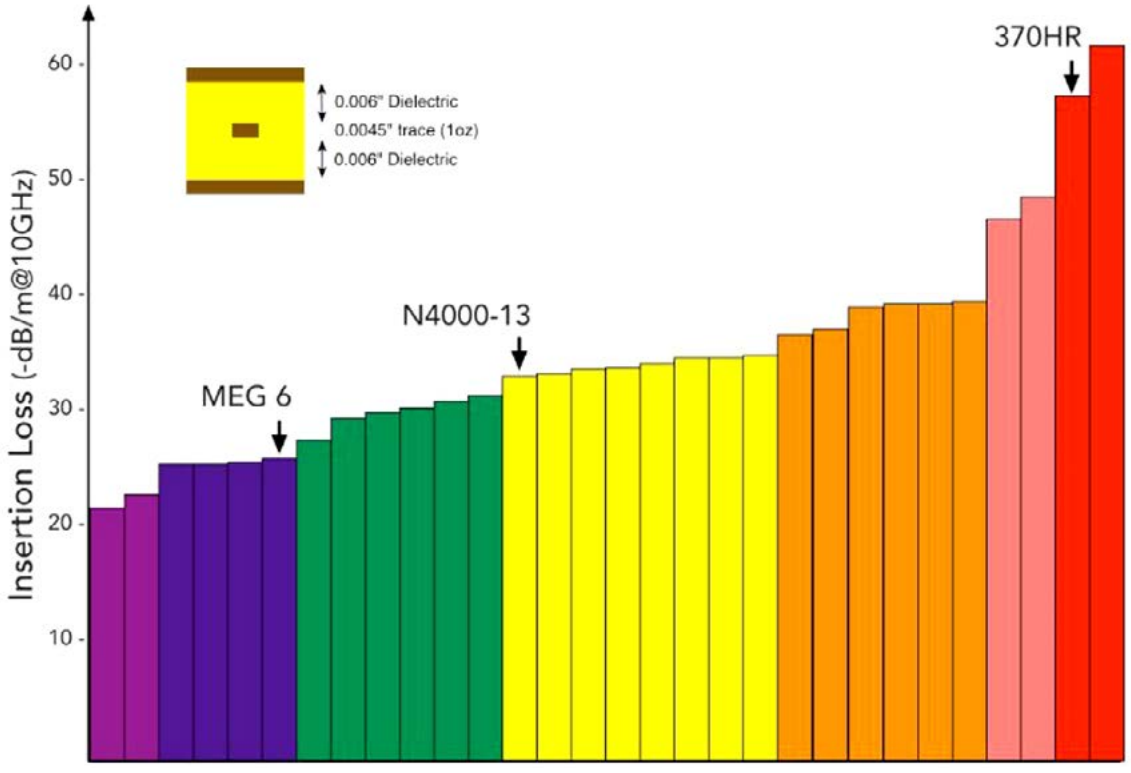

Figure 3. A variety of competitive materials are available, with only incremental differences.

performance compared to all high-performance material stackups.

Mid-Dk/Df Class Laminates

There is even a more dynamic mid-Dk/Df market at present. Mid-Dk/Df is defined here as having a dielectric constant measurably lower than FR-4, meaning at or below 4.0 and a Df rating in the range of 0.007–0.013, with a number of entries rated at or below 0.010. This class of materials has existed since the issuance of GE's Getek circa 1988, which was followed by Park-Nelco's N4000-13 and its equivalent competitor materials. Nelco also added low-Dk/Df options to N4000-13, as did several of its competitors over time.

Changes to this class came fast once RoHS dictates were being adopted. These are highly modified epoxy-based systems, some blended with cyanate esters, PPEs, PPOs and other proprietary content to achieve their performance targets. These now long, complex molecules were not proving very adaptable to the elevated temperatures of lead-free assembly and their impact on CTE-Z. Modifications were again needed and established mid Dk/Df players did just that, but only incrementally to protect their existing resin UL qualifications, which would be lost and require a new qualification cycle if UL Labs were to determine that a resin had changed to the degree of designating it as a new system.

In many ways, this hamstrings the laminators in industry-critical efforts to improve resin systems. Once a resin system formula has been locked down, it takes about a year for a laminator to get that new product through laminate UL, and the multi-months-long fabricator UL qualification extends that time even further. So, pressures of time-to-market and return on investment can run very counter to the need to advance a resin system beyond some limited scope despite the need for a fuller reinvention.

The market was able to manage for a few years, but HDI has become more complicated, BGA pitches smaller, and plated over via-in-pad and sequentially laminated build-up boards designs are much more prevalent today. The need to cross that UL line has been made evident and

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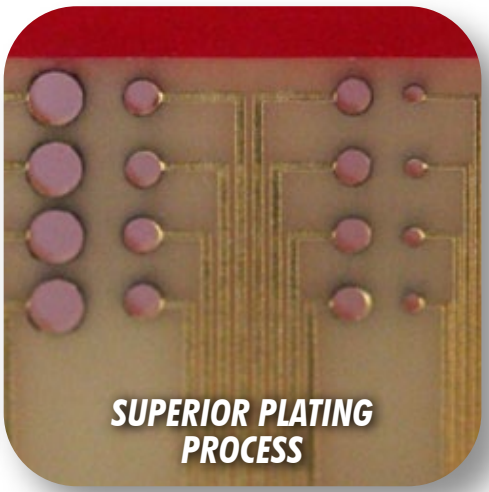

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several laminate suppliers have responded with new, more robust and performance-improved systems. Not only have they been addressing the thermal-mechanical requirements, but they have also been able to chip away at bettering Df values and have moved into more expansive options of spread weaves and copper smoothness offerings, as well as leveraging new supplier sources for lower Dk/Df glass types.

All these changes have enabled new class within a class, a spate of mid-Dk/Df materials measurably above the traditional ones but still situated below the cost and performance absolutes of the ultra-premium low-Dk/Df class. The traditional mid-Dk/Df materials were showing some good use in the 5–10 Gbps space, but running short of really supporting the upper end of that range, forcing some designs into over-specifying of materials until these new issues started appearing. The new mid-Dk/Df+ class is targeting use as fast as 12.5 Gbps depending on trace widths and routing lengths. This in turn has put pressure on the low-Dk/Df class of materials to either reduce their cost as-is or create better performance versions to satisfy the ramping development of 20–25 Gbps and faster designs. Not surprisingly, both actions are taking place now.

Low-Dk/Df Class Laminates

To better understand the low-Dk/Df class of materials, we define them as having Dk values at or below 3.7 and Df ratings at or below 0.005. A number of the mid-Dk/Df materials can easily make this Dk range if enhanced with low-Dk glass, but not while also in the range of Df. These two values together then define a distinct class. The present standard bearers are Panasonic's Megtron-6 and, to a lesser extent, the Rogers 4000 series of ceramic hydrocarbons. But there are more players today and many more in the queue and coming.

The thermal-mechanical behavior of these materials is always important as they are often relegated to very complex, HDI designs and so must be able to endure multiple lamination cycles at lead-free temperatures, which is quite challenging; it is very difficult for laminators to concoct complex molecules that deliver very high electrical performance while remaining mechanically stable and robust. All the materials of this class have proprietary resin formulations, so it is not possible for us to know their entire makeup, although at the farthest end, most have measurable content of PTFE (e.g., Rogers Duroids, Taconic, etc.).

Cost always plays a big part in any product design, so the PTFE-laden materials are still limited players, although we're seeing some very large platform boards experimenting with PTFE-based laminates for the sake of mitigating attenuation over traces on the order of about a meter. But these are 25+ Gbps R&D designs and not what is being built regularly today. Product in the 8–12.5 Gbps space has given Megtron-6 much of its market. Targeted transmission rates have been increasing toward 20–25+Gbps, thus driving the need for even lower-loss materials, most preferably ones that do not have the high cost and processing challenges of PTFEs.

A number of these have been introduced in recent quarters and are under evaluation. Performance claims are just that, always warranting independent testing and measurement. We are especially interested in seeing how any high-end materials behave, as testing clicks through frequencies of, 5, 10, 12.5 GHz or more and how well they survive the rigors of modern HDI fabrication and assembly processes. Also, former background testing is often front and center today, with requirements of CAF, insulation resistance and the like being demand items and significant filters of acceptance for a number of OEM industries.

Overall, as a fabricator, we are very encouraged to see such a huge flurry of new and promising laminates entering the market and are optimistic laminators will continue providing answers to our most pressing needs and demands of signal integrity and speed. **PCBDESIGN**

Steve Iketani is the manager of strategic technology development for the PCB Operations Division of Sanmina.

Brian Nelson is manager of new product introduction for PCB fabrication operations at Sanmina.

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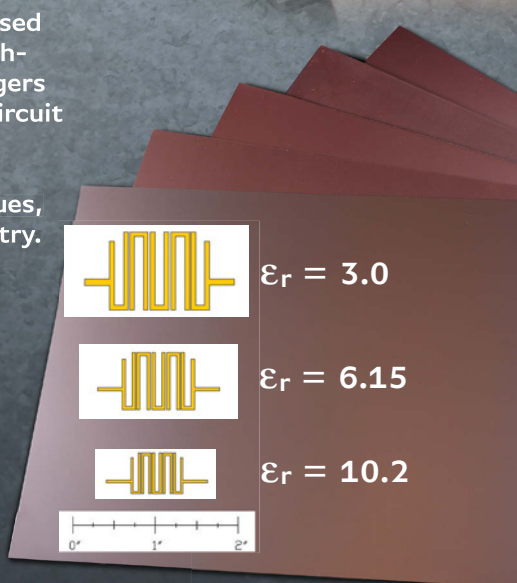

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Construction Profiles and Material Decomposition

by Paul Reid
PWB INC.

This month, we'll review the use of as-received capacitance data to produce a construction profile and a type of material damage that is called material decomposition.

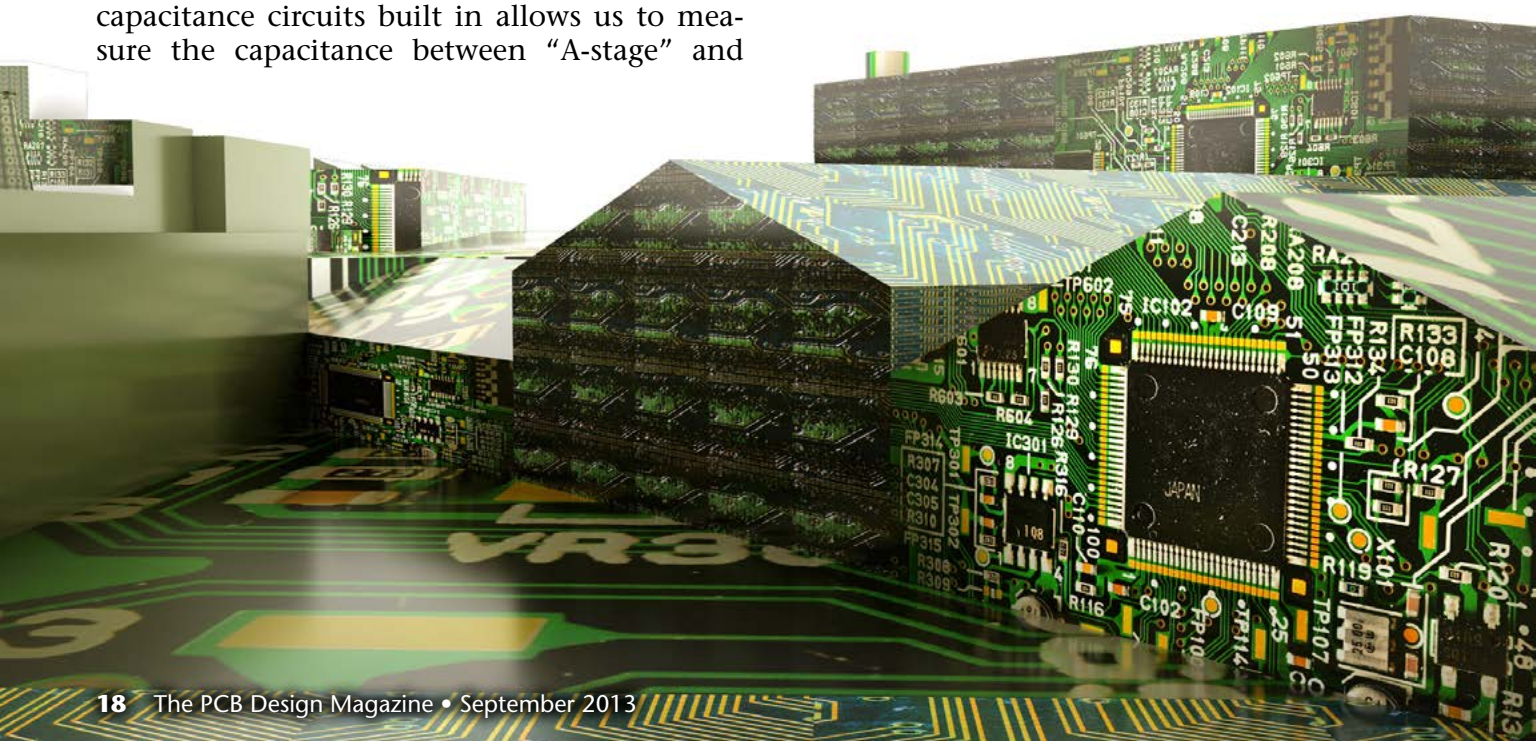
The construction profile is useful when comparing different types of board constructions. We measure the capacitance data on the as-received coupons and produce a construction profile by plotting the capacitance in picofarads. Using this method we can see variations in construction of boards like a missing layer of "B-stage" material or reversed order in lay-up.

Material decomposition is a rare type of material damage that occurs most often when low-grade materials are used in a lead-free application. With material decomposition, the assembly and rework temperatures are too high and the dielectric material epoxy system becomes carbonized.

Construction Profile

Using IST coupons with DELAM (Dielectric Estimation Laminate Assessment Method) capacitance circuits built in allows us to measure the capacitance between "A-stage" and "B-stage" dielectric layers. These DELAM circuits are layers that are flooded with copper in the coupon wherever there is a corresponding ground plane in the associated board. We are able to measure and record the capacitance between those layers. The capacitance varies due to the dielectric thickness, glass style, the Dk of the material and the amount of moisture in the material. The capacitance is usually, by design with IST coupons, 30-400 picofarads between flooded layers. For example, let's look at the coupon profile of a group of coupons in Graph 1. In this case, the flooded ground planes are measured between layers 2, 4, 6, 8, 10, 11, 13, 15, 17 and 19.

What we can do is measure the capacitance between two DELAM circuits on all incoming coupons in the "as received" state and plot those capacitances in a graph. By doing this we then can easily see if there is a difference in the construction of the coupons. Maybe one coupon is supposed to have a construction of two sheets of material 1080, but through an error



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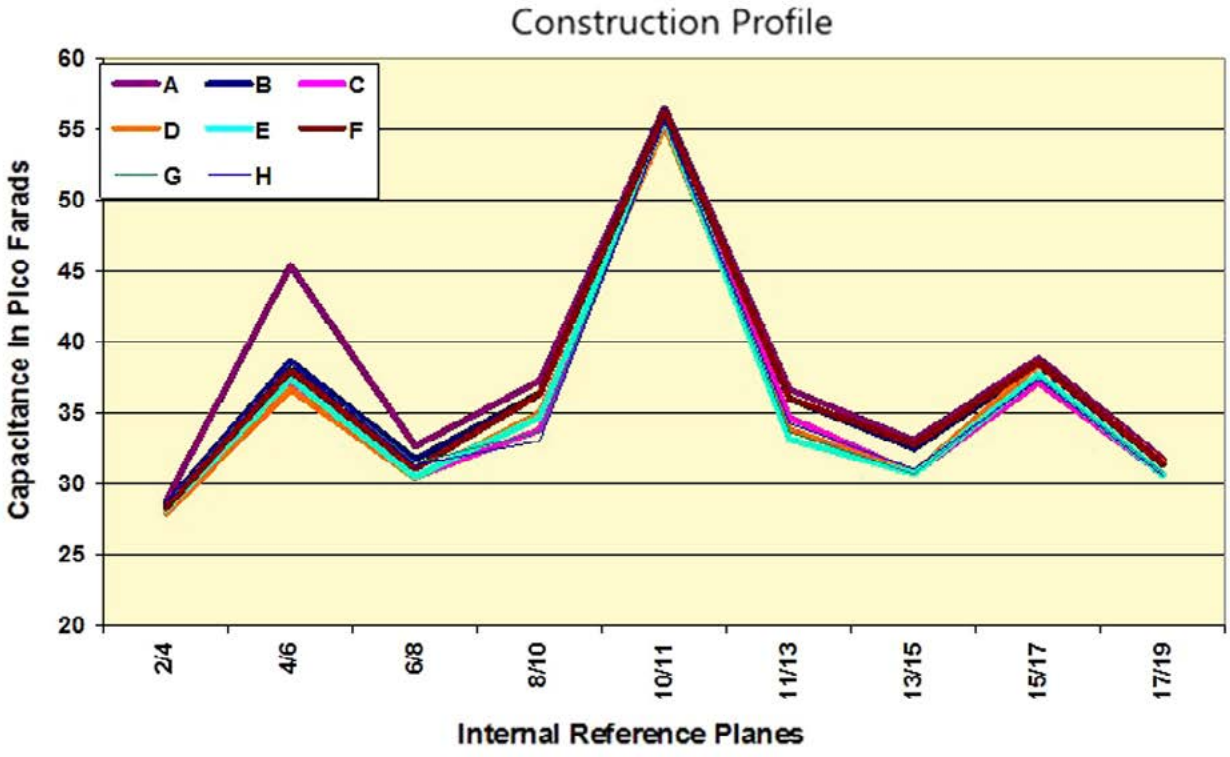
only one sheet of the 1080 is laid up on one layer. What we see is an obvious discrepancy in the construction profile. In Graph 1, notice that coupon "A" has a different capacitance profile at layer 4/6. Coupon "A" has 45 picofarads at layer 4/6 while the balance of the coupons measures 37–38 picofarads between those two layers. This discrepancy may be due to missing a layer of 1080. It is obvious that there is a difference in the construction of coupon "A" between layers 4/6 and the rest of the coupons. The rest of the variations appear normal in the graph. What one could do is to remove coupon "A" from the test set, microsection and measure the dielectric thicknesses, and if a layer is confirmed to be missing, reject the associated PWBs.

Another application of the as-received capacitance data is to see how different vendors construct their product. In Graph 2, we see the variation in the construction profiles between three vendors. The problem was that this was the exact same board built by three different vendors. The same blue print was used to specify the product. The variations in production profiles came about because of how the three vendors constructed the product. Vendor "B" may have used a core construction between layers 13/14 while vendors "A" and "C "may use a "B-stage" for the same layer. Probably the biggest cause for variations in the production profile is lay-up. The glass style, press setting, variation in process, moisture absorbed between layers and variations in the lemmatization cycles could also produce variations between construction profiles.

Just because a construction profile is different does not reflect a variation in reliability, per se. If the construction profiles are similar it does reflect on the consistency of processing. If there are differences in construction profiles those coupons with the largest variations may be selected for thermal cycle testing (IST) and DELAM evaluations. The data could then be analyzed and conclusions drawn. There could be occasions when large variations in construction profiles would indicate which boards are more vulnerable to fail for reliability or material testing.



Graph 1. Capacitance profile.

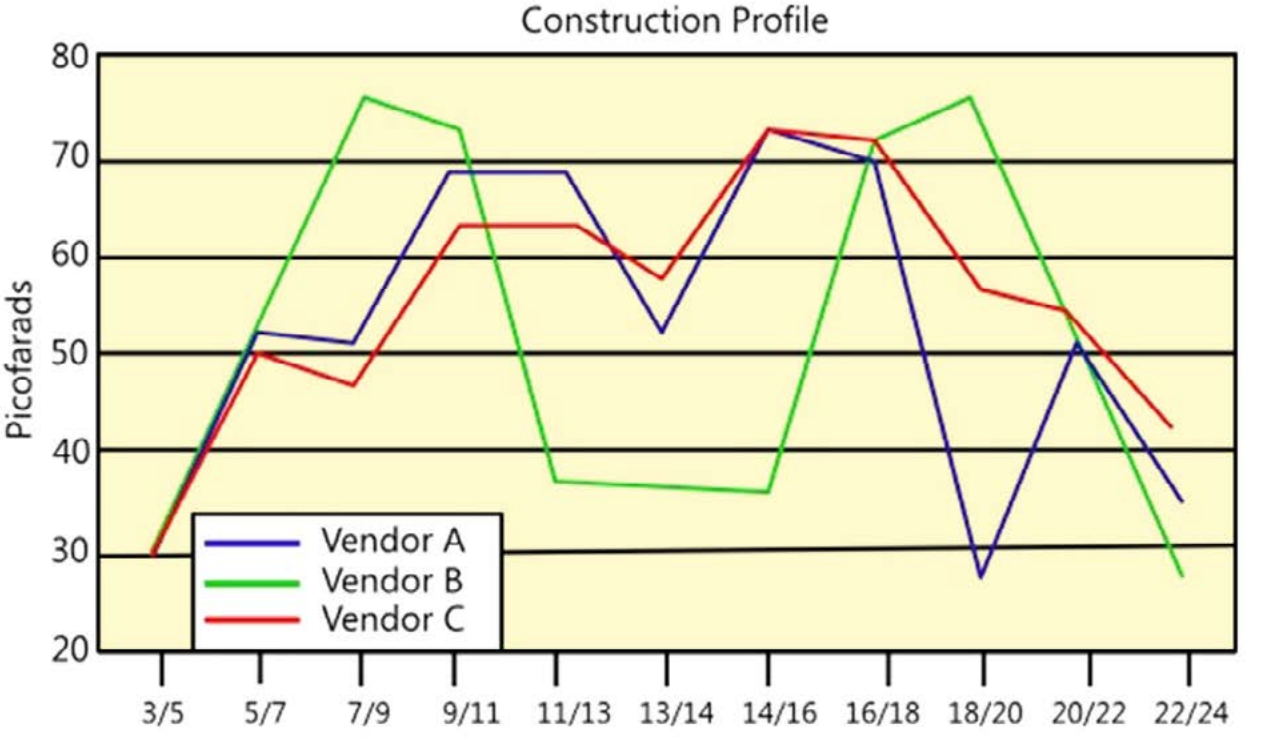
Material Decomposition

Material decomposition is a rare type of material damage. It is the frank decomposition of the dielectric material's epoxy system, due to processing the material at too high a temperature for that epoxy system. What we found was that during the beginning of the advent of lead-free processing some fabricators would just use their low T_g, dicy-cured material in the lead free application. The result, although rare, was a decomposition of the material to a degree that the material boiled and produced a carbon residue. There was one set of coupons that produced a carbon ball beside each PTH. The lead-free process temperature of 260°C was just too high for that epoxy system.

The effect on cycles to failure on the coupons with material decomposition was that there were no thermal cycling failures. There was no damage to copper interconnections in those coupons. The coupons were totally degraded but they would not fail the thermal cycle testing even though the coupon had been destroyed from a dielectric point of view. It appears that destroying the epoxy produces a stress free environment that does not put strain on the copper interconnections. The decomposition of the material produced no significant stress due to Z-axis expansion on the copper in PTHs and, if the interconnections survived the extreme pad rotation, there were no failures found.

This condition is found with capacitance measurements after preconditioning. What we see is a capacitance change of greater than -4%. Most of the time the damage is visible upon macroscopic examination as a darkening of the coupons and possible carbon balls next to interconnections. What we do is measure a change in capacitance of greater than -4%. When we complete the microsection of the worst coupon for capacitance change, in the case of material decomposition we see the characteristic black bubbles in the dielectric material. Also, there is usually pad rotation where the dielectric material has undergone plastic deformation.

In Figure 1 you will note that the material is black, there is great pad rotation and bubbles are evident in the material, suggesting the dielectric



Graph 2. Construction profile: same coupons, three vendors.

CONSTRUCTION PROFILES AND MATERIAL DECOMPOSITION *continues*

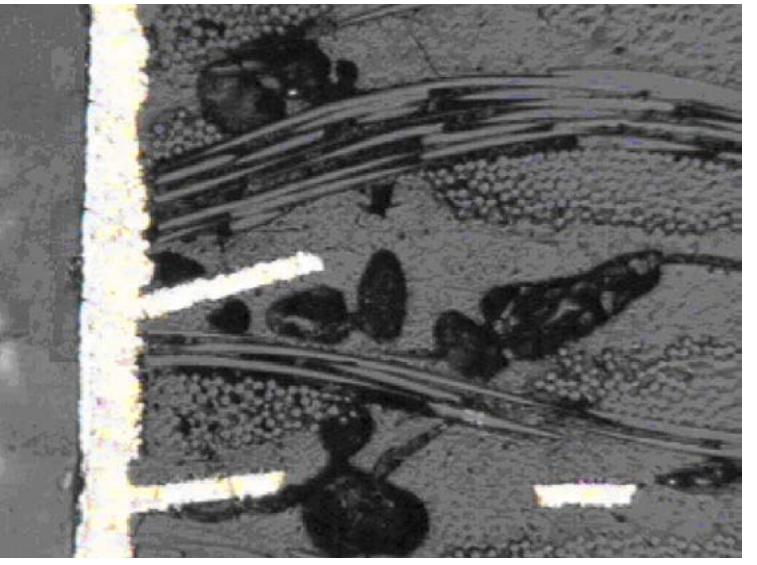


Figure 1. Cross-section of a coupon with material decomposition.

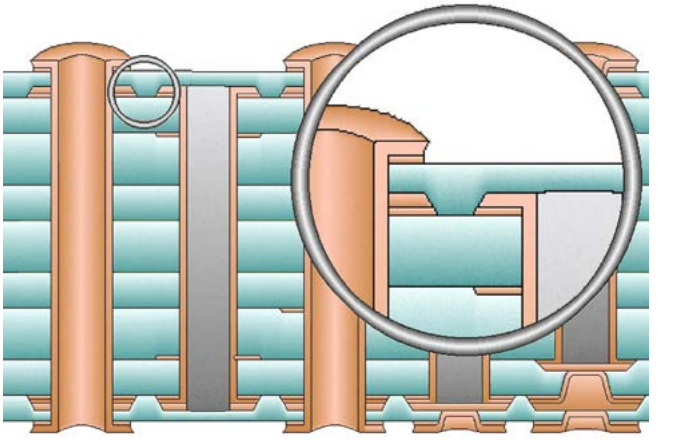
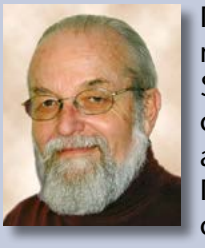


Figure 2. For animation showing material decomposition click here.

boiled at one point during heating to 260°C. Surprisingly, there was no resistance increases in the copper interconnection seen at the end of 500 thermal cycles.

The animation is my interpretation of how this material decomposition must propagate. I have never been able to catch this condition in the process of occurring, however, so this is my attempt to show how it would look based on the microsection of the coupon at ambient. **PCBDESIGN**



Paul Reid is program coordinator at PWB Interconnect Solutions, where his duties include reliability testing, failure analysis, material analysis, and PWB reliability consulting. To contact Reid, or to read past columns, click here.

"Groovy" Hologram Creates Strange State of Light

Applied physicists at the Harvard School of Engineering and Applied Sciences (SEAS) have demonstrated that they can change the intensity, phase, and polarization of light rays using a hologram-like design decorated with nanoscale structures.

As a proof of principle, the researchers have used it to create an unusual state of light called a radially polarized beam, which, because it can be focused very tightly, is important for applications like high-resolution lithography and for trapping and manipulating tiny particles like viruses.

This is the first time a single, simple device has been designed to control these three major properties of light at once.

"Our lab works on using nanotechnology to play with light," says Patrice Genevet, a research associate at Harvard SEAS and co-lead author of a paper published this month in Nano Letters.

Genevet works in the laboratory of Federico Capasso, Robert L. Wallace Professor of Applied Physics and Vinton Hayes Senior Research Fellow in Electrical Engineering at Harvard SEAS. Capasso's research group in recent years has focused on nanophotonics, the manipulation of light at the nanometer scale, with the goal of creating new light beams and special effects that arise from the interaction of light with nanostructured materials.

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Improved Thin-Film Resistor Material

by Bruce P. Mahler
OHMEGA TECHNOLOGIES

SUMMARY: Improvements in resistive alloys now allow for the creation of very small resistor elements that can be built within a logic trace. This results in improved electrical performance, improved reliability, more routing area and greater flexibility for PCB designers.

Embedded resistors have been used for many years as replacements for discrete surface devices in order to increase circuit density, improve reliability and enhance electrical performance. For many of those years, circuit designs were able to accommodate embedded resistor footprints that were relatively large, typically with line widths greater than 250 microns (Figure 1).

The evolution to greater I/O densities and routing constrictions made it very difficult, if not impossible, to embed resistors with footprints of these dimensions, especially terminating resistors within the high-density routing area of BGA devices.

This lead to the development of a 10 ohm per square sheet resistivity "resistor built in-trace" technology, OhmegaPly ORBIT, that allowed termination resistors to be built within traces and eliminated the requirement for designing

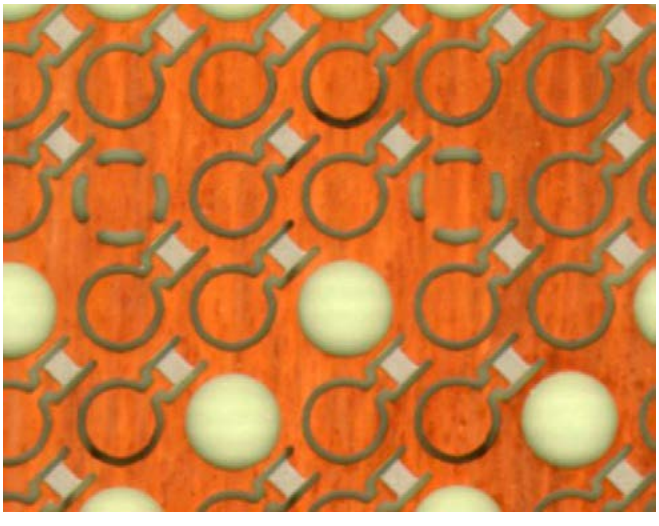

Figure 1. Parallel termination resistors.

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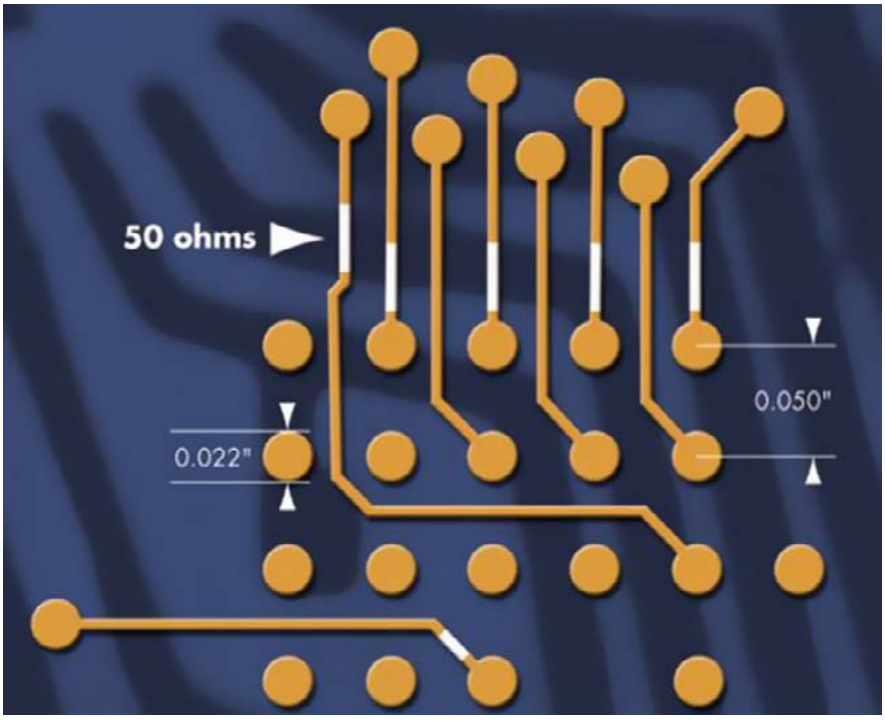

Figure 2. Resistor built-in trace.

resistor footprints by placing them within the circuit layout (Figure 2). These resistors are typically about 125 microns wide.

With increasing I/O densities, there has been a new need for embedded resistors that could fit within uBGA footprints with pad pitches of less than 500 microns. Resistors with line widths of less than 100 microns are necessary to accommodate these new requirements.

In order to achieve good tolerance and fine line resistors with line widths less than 100 microns, Ohmega Technologies began development work to enhance the standard OhmegaPly nickel-phosphorous resistive alloy. This effort focused on improving the chemical and physical stability of the resistive alloy. Success in this effort led to the creation of the patent-pending OhmegaPly Micro Trace Resistor (MTR) technology.

In addition to an improved resistive material, it is suggested that board shop processing include the use of laser direct imaging (LDI) for both the primary and secondary print operations. LDI has the advantage of greater precision, straight sidewalls and near perfect registration for the second imaging that defines the resistor length. This means that the overlap of the photoresist-defined window over the resistor element needed for the second print and etch operation can be smaller and becomes critical when working with lines and spaces of 100 microns or less using conventional print and etch processes.

Another key aspect to the creation of micro trace resistors is the use of a unique NiP differential etch technology. As line widths become narrower, the effect of undercut on the circuit becomes more pronounced, resulting in more line variation and larger resistor value tolerances. Over-etched line edges become ragged or uneven. This contributes to wider tolerances and degrades electrical performance in high frequency applications. When micro trace resistors of 100 microns or less are etched in the primary

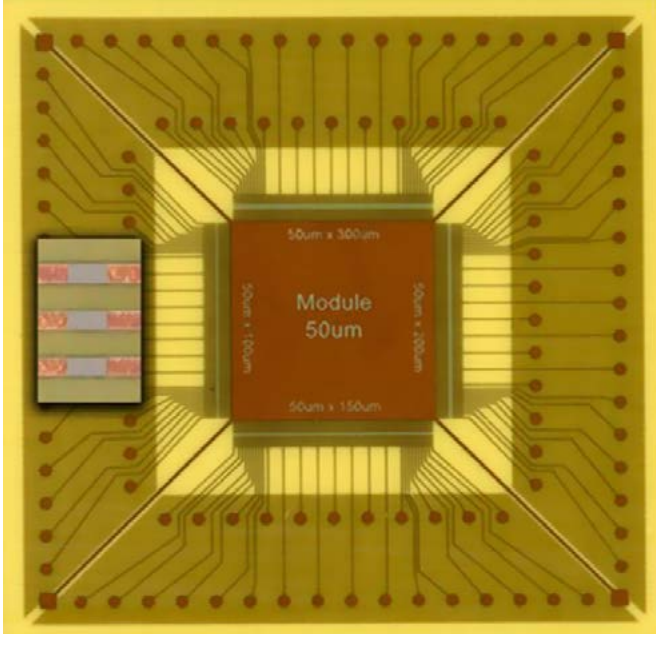

Figure 3. Example of Micro Trace Resistors.

	Standard OhmegaPly®		OhmegaPly® MTR®	
	25 ohm/sq	50 ohm/sq	25 ohm/sq	50 ohm/sq
Sheet Resistivity (after final alkaline etch)	28	50	25	50
Tolerance for a 100µ wide resistor	15%	15%	10%	10%
Micro Etch Exposure ΔR%	10%	4%	1%	1%
240 Hours 95% RH/40C ΔR%	2%	2%	1%	1%

Table 1. Comparison of Standard OhmegaPly and OhmegaPly MTR.

copper etchant, whether acid or alkaline, the dwell time is especially critical because the narrower the resistor element, the greater the variation in width has on the ohmic value of the resistor.

After primary copper etching, the exposed NiP layer must be stripped to limit the resistive layer to the boundaries of the etched copper features. The NiP differential etch is a selective copper sulfate solution that will strip the exposed resistive material without etching the copper features. In addition, it is a self-limiting bath that ceases to work after all of the exposed NiP resistive material is stripped away. It does not undercut copper to etch any underlying NiP resistive material. The importance of the congruence of the resistive trace to the copper trace is that as the resistor widths become narrower, the width variation has a greater effect on the resulting percent tolerance in ohmic values. After the differential strip, the use of LDI for the second print enables precision copper etching and tight tolerance miniature resistor elements (Figure 3).

Improvements in the chemical and physical stability of the NiP resistive alloy resulted in improved properties of the embedded resistor when compared to standard NiP resistive films (Table 1).

With greater material stability in the PCB chemical processes, a significant improvement in the final resistor tolerance is achievable with MTR.

Another concern with very small Micro Trace Resistor footprints is the power carrying capability of such small size elements. The power dis-

OHMEGAPLY MTR® MICRO TRACE RESISTOR® TEST RESULTS

Resistivity	Resistor Width	TWO SQUARES		FOUR SQUARES		SIX SQUARES	
		Resistance (Ohm)	Power rating (mW)	Resistance (Ohm)	Power rating (mW)	Resistance (Ohm)	Power rating (mW)
25 ohm/sq.	50 Micron	50	40	100	50	150	55
	75 Micron	50	60	100	80	150	80
	100 Micron	50	70	100	100	150	125
	125 Micron	50	90	100	125	150	165
50 ohm/sq.	50 Micron	100	30	200	45	300	55
	75 Micron	100	45	200	65	300	80
	100 Micron	100	60	200	85	300	115
	125 Micron	100	80	200	100	300	120

Table 2. Power ratings of Micro Trace Resistors at 25°C.

sipation of the resistor is a function of thermal management, film thickness and element size. The NiP resistive alloy, both the standard and improved MTR versions, have a relative alloy thickness of approximately 0.4 microns for the 25 ohm per square product and 0.2 microns for 50 ohm per square sheet resistivity product, respectively. This is approximately twice the film thickness of other thin film alloy materials that are commercially available. This added thickness results in a lower temperature rise for a NiP resistive alloy when compared to other resistive alloys of the same sheet resistivity.

Testing of MTR resistors resulted in very good power ratings for such small element sizes, more than sufficient for most uBGA termination applications (Table 2).

Conclusion

Improvements in the basic OhmegaPly NiP resistive alloy has resulted in an enhanced version of the product that is especially suited for the high-density footprints of uBGA modules. These improvements allow for the creation of very small resistor elements less than 100 microns wide that can be built within the logic trace, resulting in improved electrical performance, improved reliability, more routing area and greater flexibility for the PCB designer. **PCBDESIGN**

OhmegaPly®, OhmegaPly RCM®, OhmegaPly ORBIT®, OhmegaPly MTR® and Micro Trace Resistor® are all registered trademarks of Ohmega Technologies, Inc. Culver City, CA, USA.

Bruce P. Mahler is vice president of Ohmega Technologies. He has been awarded four patents for improvements in embedded resistive materials and other packaging technologies over the past 35 years.

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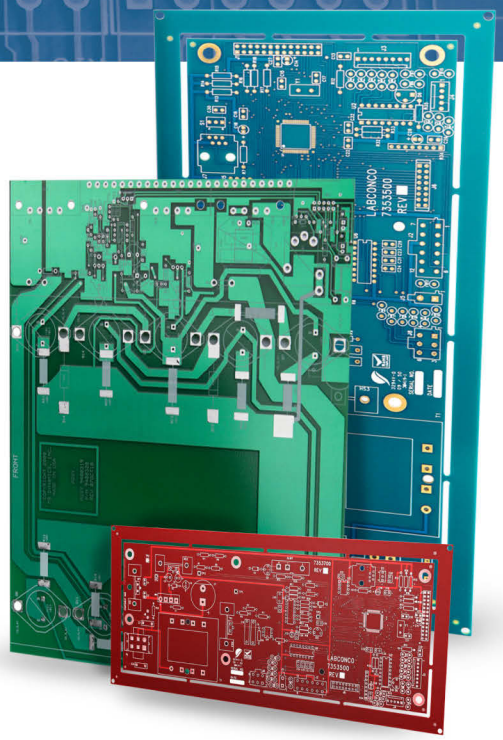

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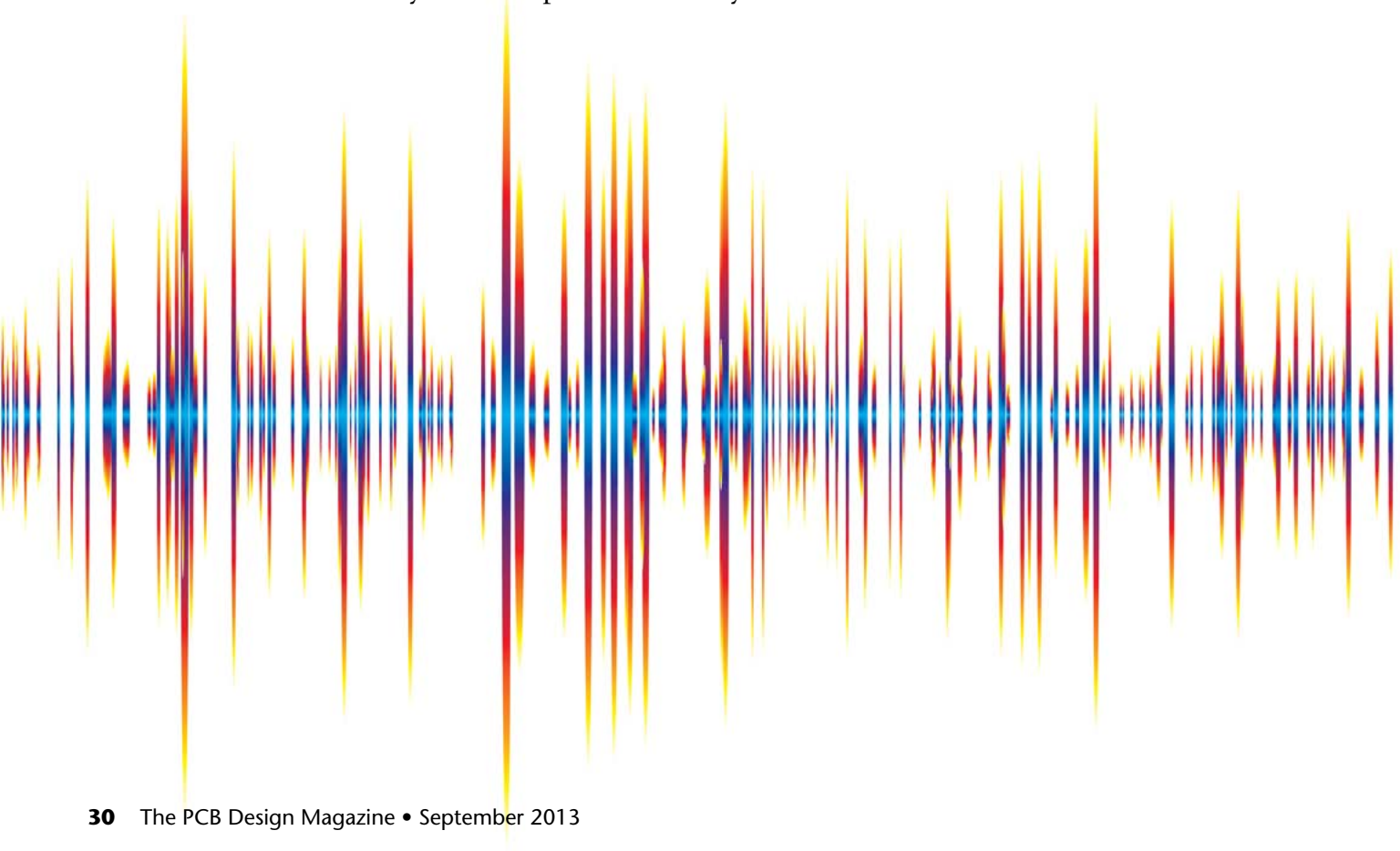
High-Frequency Laminates for Hybrid Multilayer PCBs

by John Coonrod
Rogers Corporation,
Advanced Circuit Materials Division

A hybrid multilayer is a PCB construction that uses dissimilar materials. Reasons for using dissimilar materials include: improving reliability, reducing cost, optimizing electrical performance, and improving manufacturability. For the past several years, hybrid multilayer PCB construction has flourished in the arena of high-frequency RF applications.

Multilayer reliability concerns are often related to the coefficient of thermal expansion (CTE) of the circuit material. Some laminates that display excellent electrical performance at high frequencies also have high CTE values. These laminates are often non-filled PTFE-based substrates that have a very low dissipation factor (tangent delta), low dielectric constant, and very good electrical performance at microwave and millimeter-wave frequencies. However, the high CTE of these laminates can cause problems when the PCB undergoes thermal cycling, such as soldering.

A high-CTE laminate grows at a different rate than the copper during elevated thermal exposure, and this difference can cause delamination of the copper-to-substrate interfaces. Also, when a PTFE-based circuit reaches elevated temperatures, it will expand and put stress on the plated through-hole (PTH) vias, which may in turn cause them to fracture. It is typically desired to have a substrate with a CTE simi-



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HIGH-FREQUENCY LAMINATES FOR HYBRID MULTILAYER PCBS *continues*

lar to that of copper, which is approximately 17 ppm/°C. But some PTFE substrates have a CTE in the range of 200 ppm/°C or more.

Nowadays, most multilayer constructions perform multiple electrical functions. With some multilayer circuits, only a few copper layers are considered electrically critical for high-frequency performance, while the rest are not critical. These circuits could use PTFE-based laminates for high-performance layers, and a low-CTE material in the remainder of the board. Combining the high-CTE and low-CTE materials will yield a hybrid multilayer with a composite CTE that can be acceptable for thermal reliability and good electrical performance.

Some hybrid multilayer PCBs use dissimilar materials specifically for cost reasons. Most high-frequency laminates cost more than FR-4; however, they are typically compatible for circuit fabrication. A word of caution regarding using hybrids for cost reduction: Even though the material costs are very different, if fabrication is made more difficult due to the combination of these dissimilar materials, some cost savings may be mitigated. The supplier of high-frequency materials should be involved in planning these hybrids, because these companies typically know which materials are compatible.

Hybrids are often used in coupler applications; they help improve the performance of the coupler. High-frequency materials with very different dielectric constant (Dk) values can be used to improve the coupling coefficient. A quick example is a four-layer stripline broadside coupler, with the same low-Dk laminate type used for the top and bottom layers. The circuit uses a material with a high Dk value for the layer that separates the coupling elements of layers 2 and 3. This combination can help tune the design for specific coupling values as well as other enhanced coupler properties.

A word of caution regarding using hybrids for cost reduction: Even though the material costs are very different, if fabrication is made more difficult due to the combination of these dissimilar materials, some cost savings may be mitigated. The supplier of high-frequency materials should be involved in planning these hybrids, because these companies typically know which materials are compatible.

The combination laminates with different Dk values have been used in antenna multilayer hybrids in order to optimize the performance of the antenna. Typically, a thick laminate with a low Dk is used for the radiating element of a PCB antenna. It is often not optimum for the feed line that transfers energy to the antenna radiating element to use this same material because the feed line will lose some energy due to radiation loss before it reaches the antenna elements. In this case, a multilayer hybrid is used where the feed line is a buried signal layer in a stripline configuration using a low-loss material. The stripline configuration will not allow radiation loss. A PTH via is used to get the energy from the feed line to the antenna element on the outside layer of the hybrid. Many times the outside layer for the antenna radiating element will be of a different Dk than the inner layer feed line to optimize each circuit feature's performance.

Hybrid multilayer PCBs can offer improved manufacturability, because certain materials offer better drill life, simpler processing for PTH preparation, and shorter lamination cycles, as well as causing less debris during laser ablation, etc. When the desire is to improve manufacturing by using hybrids, there are many issues to consider for each material. Typically, a very thorough study is needed to assess compatibility issues and yields, as well as true improvements to the fabrication process. **PCBDESIGN**

John Coonrod is a market development engineer for Rogers Corporation, Advance Circuit Materials Division. To contact Coonrod, click here.

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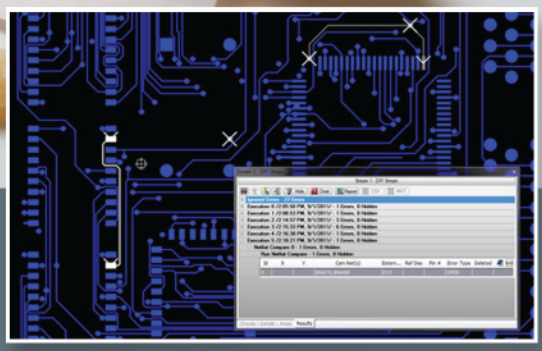

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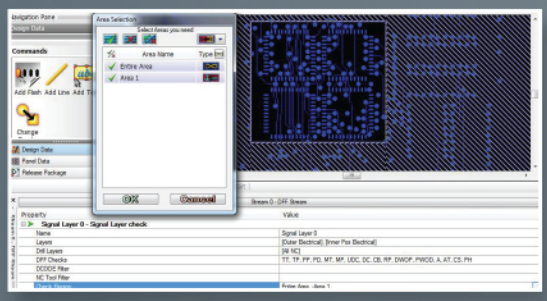

Define DFM checks by area so components such as BGAs can be verified with unique rules different from rest of design

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PCB007 News Highlights

Omni Circuit Boards Develops Aluminium Trace Circuit Board

Omni Circuit Boards has announced the successful development of an aluminium, monometal wire-bonded circuit board. The prototype, designed and manufactured for use in a D-Wave systems quantum supercomputer, allows for superconductivity and operation in low temperatures just above absolute zero.

IPC, JPCA: New Design Guidelines for Printed Electronics

"IPC will continue its work on the design guidelines, in collaboration with JPCA, to secure additional companies' experiences. We encourage companies with expertise in this area to help by participating in the continuing international consensus-building committee process," said IPC Director of Technology Transfer Marc Carter.

The PCB List Celebrates Anniversary

"The participation of fabricators in claiming and populating their listing is directly proportionate to how beneficial The PCB List is. It's simple and only takes a few minutes to get your company up and searchable to an expansive list of registered buyers," noted Patty Goldman, sales director for The PCB List.

MFLEX Reports 20% Q3 Decline in Net Sales

"We believe our third quarter results will serve as an inflection point as we anticipate a meaningful sequential improvement in revenue in the fourth quarter, with continued momentum into fiscal 2014. As a result, we expect to return to profitability in the first quarter of fiscal 2014, as well as on a full year basis in fiscal 2014," said Reza Meshgin, CEO.

IPC N.A. PCB Industry Study Forecasts Growth by Year End

North American PCB production should see a return to modest growth by the end of 2013. The growth is expected to continue through 2016, not just for North America, but also for world PCB production as a whole. Recently released by IPC, the annual survey-based study provides a comprehensive overview of the market and business of PCB manufacturing.

German PCB Market Continues Growth in May

Despite May 2013 having only 19 working days, total turnover for the month was still 5.6% higher from April, and 3.3% higher from the same period last year.

Viasystems in Line with Expectations; Q2 Sales Nearly Flat

Net sales and operating income in the company's PCB segment for 2Q13 were $240.7 million and $4.7 million, respectively, compared with PCB segment net sales and operating income of $240.4 million and $15.1 million, respectively, for 2Q12.

IPC Trims PCB Sales Forecast; June Bookings Down 6%

"Until this June, monthly PCB orders outpaced sales every month since January, which has produced positive book-to-bill ratios for the past six months," said Sharon Starr, director of market research.

TTM Technologies Q2 Net Sales Up 4%

"Overall results for the second quarter were in line with our guidance," said Kent Alder, CEO. "During the quarter, we experienced broad-based strength in our networking and communications end market in both Asia Pacific and North America…"

AT&S Begins FY 2013/14 on Positive Note

"Despite the challenging market environment, both mobile devices and automotive and industrial segments reported significant year-on-year improvements in revenue and capacity utilisation. We have good reason to be satisfied with how the financial year 2013/14 has started, and have laid a solid foundation for the year to come," explained CEO Andreas Gerstenmayer.

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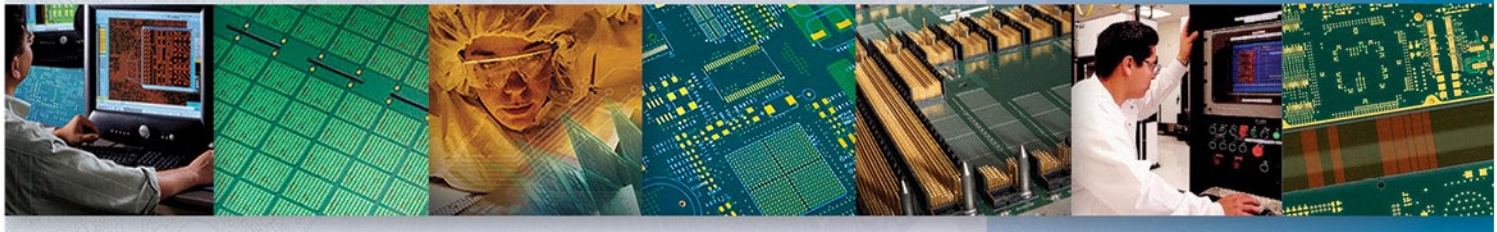

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Material Selection for SERDES Design

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD | AUSTRALIA

Many challenges face the engineer and PCB designer working with new technologies. For SERDES—high-speed serial links—loss, in the transmission lines, is a major cause of signal integrity issues. Reducing that loss, in its many forms, is not just a matter of reducing jitter, bit error rate (BER) or inter-symbol interference (ISI). Materials used for the fabrication of the multilayer PCB absorb high frequencies and reduce edge rates thus putting the materials selection process under tighter scrutiny. This column will look at the factors that must be taken into account, in the selection process, and provides some options for PCB designers.

The ideal transmission line model has properties distributed along its length. A physical transmission line can be approximated by describing sections of signal and return path as a loop inductance along its length. The simplest equivalent circuit model, in Figure 1, has a series of capacitors separated by loop inductors. There are also small series resistors with the inductors and shunt resistors across the capacitors which we assume are negligible. If I recall from Circuit Theory 101, this looks very similar to a low-pass filter, which of course attenuates high frequencies.

The Fourier Theorem states that every function can be completely expressed as the sum of sine and cosine of various amplitudes and frequencies. The Fourier series expansion of a square wave is made up of a sum of odd harmonics. If the waveform has an even mark to space ratio then the even harmonics cancel. Also, as the frequency increases, the amplitude decreases.

A square wave can be expressed as:

$$F(t) = \cos(\omega t) - \cos(3\omega t)/3 + \cos(5\omega t)/5 - \cos(7\omega t)/7 + \cos(9\omega t)/9 \ldots\ldots$$

It can be observed in Figure 2, that the 9th harmonic (pink waveform) has the steepest slope. It is this component, of the square wave, that gives the overall square wave its fastest rise time.

A square wave is made up of a number of sinusoid waveforms of different frequencies. However, only the lower frequency components can transverse the transmission line reducing the rise time at the output. This rise time degradation is due to the losses in the transmission line (dielectric loss), which is frequency dependent, and is the main source of Inter-symbol In-

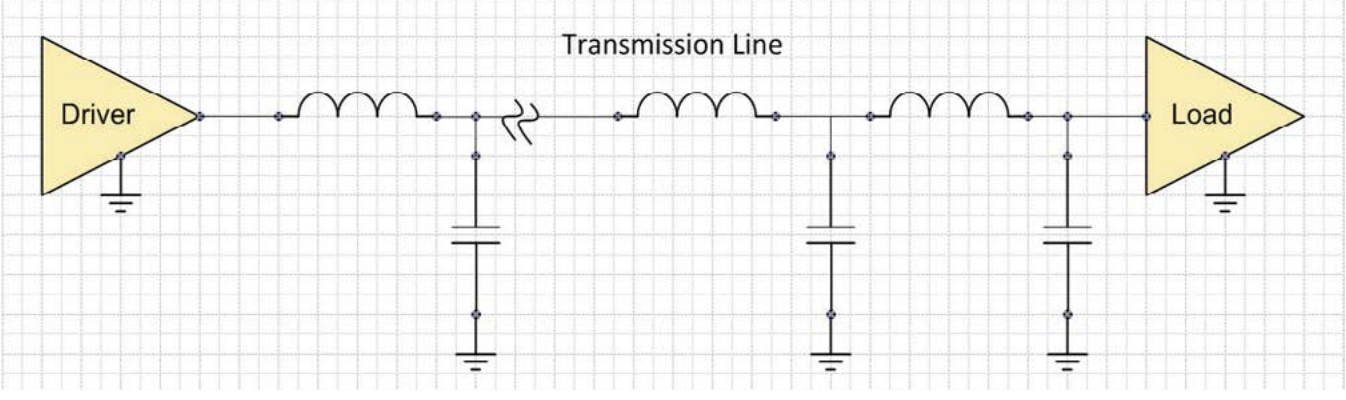

Figure 1. Ideal transmission line model.

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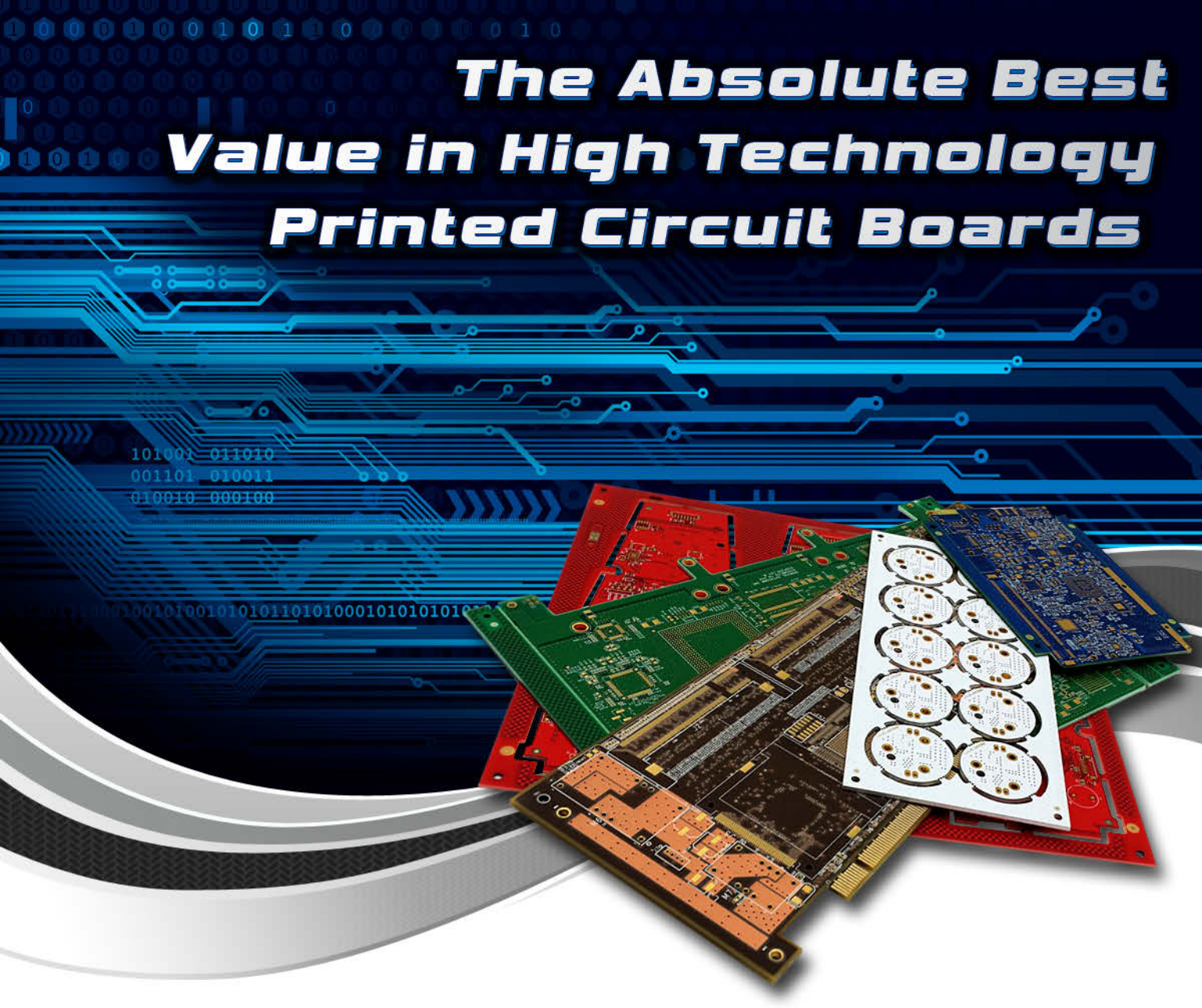

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terference (ISI). ISI is a significant contributor to jitter.

Analog designers, on the other hand, must be concerned about dielectric loss at low frequencies when constructing high-Q circuits intended to ring, without loss of signal amplitude, for recurring cycles.

FR-4, the glass epoxy material commonly used for multilayer printed circuit fabrication, has negligible loss at frequencies below 1GHz. But since the dielectric loss is frequency-dependent, at higher frequencies, the dielectric loss of FR-4 increases. So, for higher frequency digital, RF and microwave design alternative materials that exhibit lower losses need to be considered.

Designed for use in high density multilayer boards, FR-4 is suitable for surface mount components, multi-chip modules, direct chip attachment, automotive and wireless communications. FR-4 (flame retardant) has a low glass transition temperature (Tg) ~135°C and is mostly used for thin PCBs of 62 mil. FR-4 is also available with a high Tg > 170°C and is used on thicker PCB > 62 mils. The characteristics of FR-4 also make it particularly beneficial in high volume, fine-line, multilayer applications.

For digital applications below 1GHz, the losses can be ignored. But what is the highest frequency that needs to be considered? The maximum bandwidth of a signal is not determined by the fundamental frequency but rather by the rise time of the signal. Since the harmonics of the fundamental signal determine the rise time of the signal, then it is the maximum frequency harmonic that must be considered. I typically use the 5th harmonic but it may be the 7th if the rise time is extremely fast. So, for a 400MHz, fundamental frequency, the 5th harmonic is 2GHz.

At frequencies above 1GHz, the main selection criteria for PCB fabrication material is dielectric Loss or loss tangent (Df) and glass transition temperature (T_g). Df is a parameter of a dielectric material that quantifies its inherent dissipation of electromagnetic energy. The term refers to the tangent of the angle in a complex plane between the resistive (lossy) component of an electromagnetic field and its reactive (lossless) component. Standard FR-4 has a Df of 0.02 whereas a low loss dielectric may have < 0.001 at 10GHz.

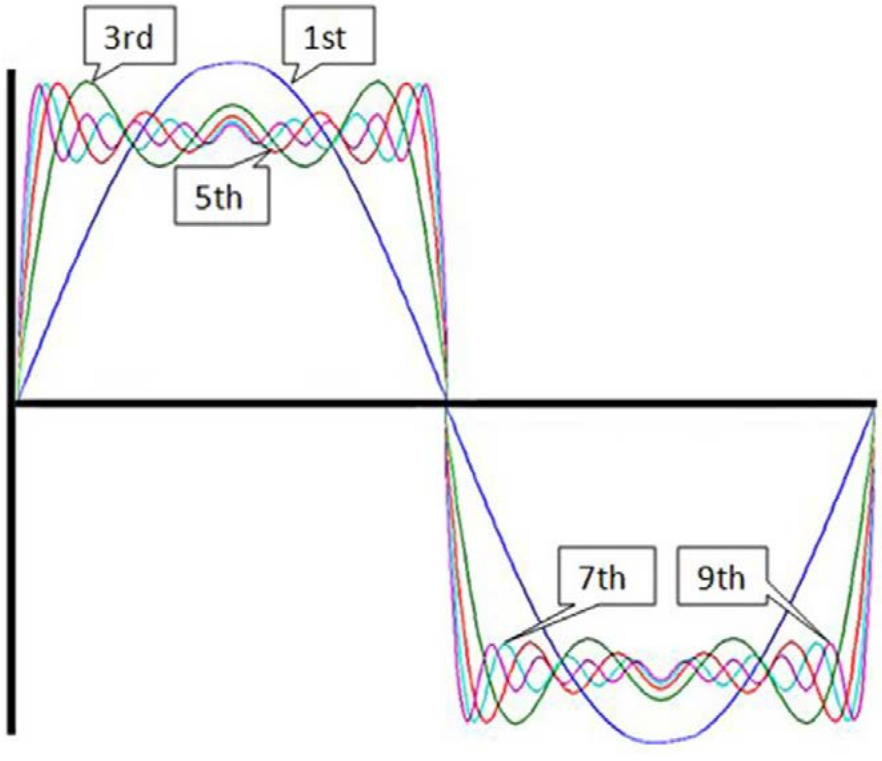


Figure 2. Reconstruction of a square wave using the odd harmonics.

The glass transition temperature is the point at which a glassy solid changes to an amorphous resin/epoxy. If the temperature exceeds the T_g, the material rapidly expands in the Z-axis. Plus, mechanical material properties degrade rapidly—strength and bonds in the material. A high T_g guards against barrel cracking and pad fracture during reflow. Standard FR-4 has a T_g of 135-170°C whereas the high-speed materials are generally over 200°C.

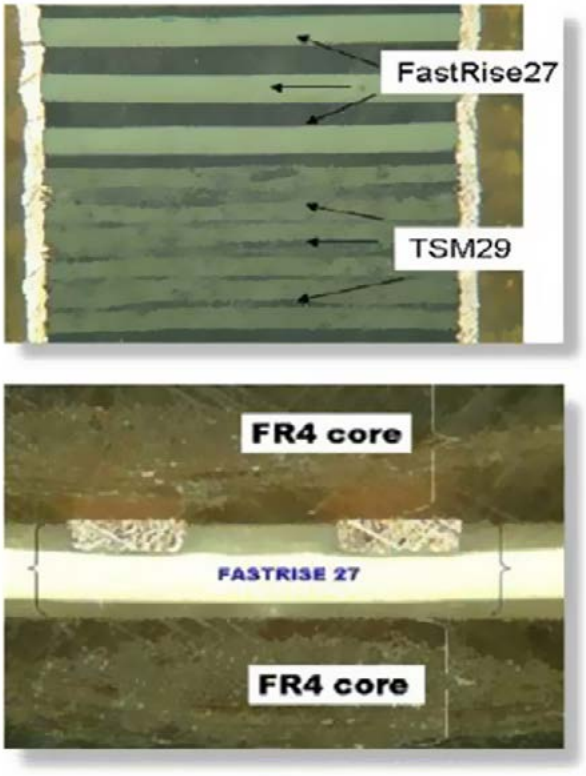
Also, at high frequencies, a non-uniform dielectric in the substrate can cause skew in differential signals. The inconsistency of the dielectric material comes from that fact that

the fiberglass and the epoxy resin, that make up PCB core (laminate) and prepreg materials, have a different dielectric constant. And, because the fabricator cannot guarantee the placement of the fiberglass with respect to the location of the traces, this results is uncontrolled differential skew. One way to avoid this is to always route differential pairs diagonally, across the board, as the fiberglass matting is laid in the X, Y direction. Or, zigzag diagonally across the board. Alternatively, a fiberglass-free material, such as fastRise™27, can be used to eliminate differential skew. However, fiberglass free materials come at a price.

The Taconic TSM-DS family of cores combined with fastRise27 (Df: 0.0014 @ 10 GHz) prepreg is an industry leading solution for the lowest possible dielectric losses that can be attained at epoxy-like (200 - 215°C) fabrication temperatures. For high-speed multilayer PCBs, the price of poor yield drives up the final material cost. fastRise27 enables the sequential lamination of TSM-DS, at low temperature, with consistency and predictability that reduces cost according to Taconic.

Another attribute of dielectric materials is the dielectric constant or relative permittivity (E_r or Dk) that reflects the extent to which it concentrates electrostatic lines of flux. It is the ratio of the amount of electrical energy stored in a material by an applied voltage, relative to that stored in a vacuum. If a material with a high dielectric constant is placed in an electric field, the magnitude of that field will be measurably reduced within the volume of the dielectric. Therefore, a lower E_r is desirable for high-frequency design.

Park Electrochemical Corporation, for instance, produces Nelco 4000-13 laminates that use NE-glass rather than the default E-glass. The dielectric constant for NE-glass is lower than E-glass—hence, the difference in E_r between resin and glass is low, which leads to less skew. NE-glass shows better temperature stability, lower E_r, and lower loss than the equivalent E-glass. The reduced E_r and dissipation factor yields important signal integrity benefits in high-speed signaling applications.



Multiple plies of *fast*Rise™27 form flat planar structures. This photo shows the contrast between fiberglass reinforced TSM-29 and non-reinforced *fast*Rise™27.

***fast*Rise™27 fiberglass free prepreg eliminates skew in differential traces. Here the contrast between the black FR-4 layer with a high glass content and the fiberglass free *fast*Rise™ prepreg is shown.**

Figure 3. Image of fastRise27 fiberglass-free prepreg eliminates differential skew. (Courtesy of Taconic)

MATERIAL SELECTION FOR SERDES DESIGN *continues*

Close attention should also be paid to the skew associated with the fiber weave effect. For high-speed data rates of 5 Gbps and above, this skew significantly cuts into the available jitter unit interval (UI) budget and leads to a reduction in the observed eye width at the receiver. If the flexibility exists, specify a denser weave material (2113, 2116, 1652 or 7628) compared to a sparse weave (106 and 1080). Figure 4 compares the different types of fiberglass weaves to a 4/4 mil differential pair. Notice that one side of the pair can be routed over the fiberglass and the other over the gap (resin), depending on the placement. The different dielectric constants create skew. Routing the differential signals diagonally across the weave can reduce this skew considerably.

DC blocking capacitors are common sources of impedance discontinuities in high-speed serial channels. Typically, narrow trace width and narrow trace spacing are used to construct the 100 ohm differential transmission line pair. However, as these narrow trace pairs are routed into the surface mount pads of a DC blocking capacitor, the sudden widening of the controlled impedance traces as they join with the capacitor pads can cause an abrupt impedance discontinuity. The effect of this discontinuity appears as excess capacitance because the surface mount pads of the DC blocking capacitors act as a parallel plate with the reference plane underneath.

To remove the excess parasitic capacitance associated with surface mount pads, remove a portion of the reference plane that is directly beneath the surface mount pads. This allows the signal that traverses through the DC blocking capacitor to reference a lower plane (further away) and reduces the parasitic capacitance, thereby minimizing the impedance mismatch. The optimum routing structure has a 20–25 mil wide cutout, under the capacitor lands, depending on the distance to the lower plane.

With so many materials to choose from which are the best for your specific product? Low cost generally means low quality. But the price of poor yield drives up the final material cost. And different materials are available locally compared to offshore. Typically, prototype boards are fabricated locally whereas for mass production, Asia is more economical.

The ICD Dielectric Material Library in Figure 5 has recently been upgraded to include over 5,650 materials many of which are suitable for high-speed, RF and microwave design up to 40GHz.

With the continuous trend to smaller feature sizes and faster signal speeds, planar capacitor laminate or embedded capacitance materials (ECM) are becoming a cost-effective solution for improved power integrity. This technology provides an effective approach for decoupling high-performance ICs whilst also reducing electromagnetic interference.

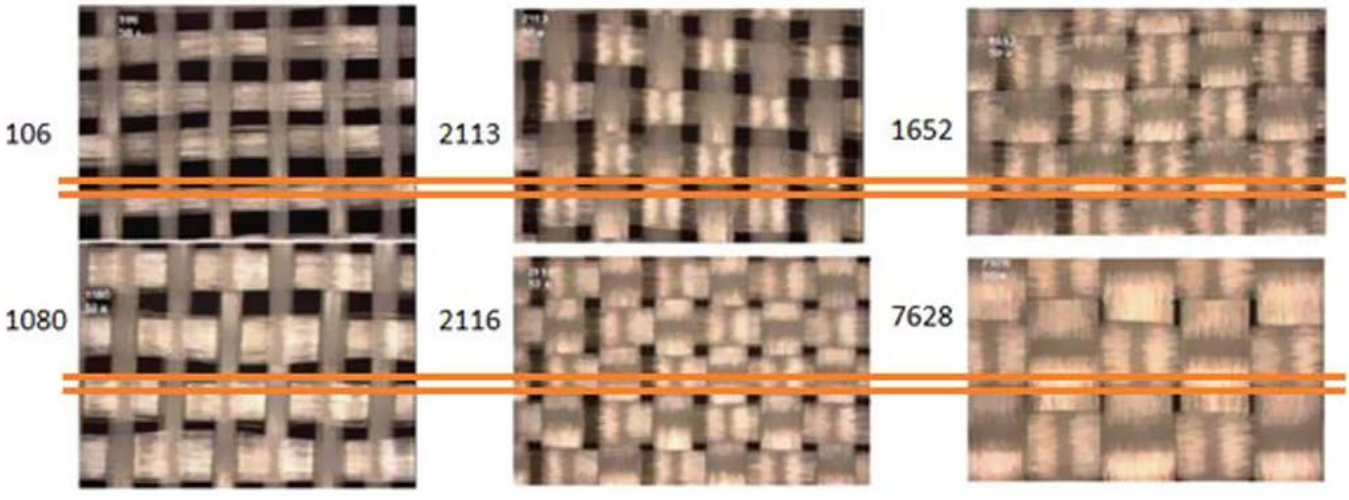


Figure 4. Different types of fiberglass weaves compared to a differential pair. (Courtesy of Altera)

Standard	Df	High-speed	Df	Ultra high-speed	Df
Panasonic Hiper V	0.0240	Isola FR408	0.0090	Isola I-Speed	0.0065
Isola IS415	0.0230	Isola FR408HR	0.0086	Nelco N4800-20SI	0.0060
Isola 370HR	0.0210	Nelco N4000-13	0.0080	Nelco Meteorwave 1000	0.0055
Panasonic FR-4	0.0190	EMC EM-888 *	0.0080	Nelco Meteorwave 2000	0.0040
ITEQ IT-180A *	0.0170	Panasonic Megtron 4	0.0080	Rogers RO4450B	0.0040
Isola FR406	0.0163	Ventec VT-464(LK)	0.0080	Rogers RO4350B	0.0037
Nelco N4000-29	0.0160	Nelco N4000-13SI	0.0070	Rogers RO3001	0.0030
EMC EM-355(D) *	0.0150	Nelco N4800-20	0.0070	Isola I-Tera	0.0028
Panasonic Hiper F	0.0150	Isola IS620i	0.0070	Panasonic Megtron 6	0.0020
Doosan DS-7809	0.0150			Taconic fastRise27	0.0014
Doosan DS-7408	0.0140			Taconic TSM-26	0.0014
Technolam FR-4 86UV *	0.0130			Taconic TSM-30	0.0013
EMC EM-828 *	0.0120			Rogers RT/Duriod 5870	0.0012
NanYa Plastics NP-175TL *	0.0120			Taconic TSM-DS/DS3	0.0010
Panasonic Megtron 2	0.0100			Rogers RT/Duriod 5880	0.0009
Ventec VT-464	0.0100				

Table 1. Materials available in the ICD Dielectric Materials Library—Dielectric Loss @ ≤ 10GHz
(A full list of materials and properties is available from www.icd.com.au).
* Taiwanese materials available in Asia

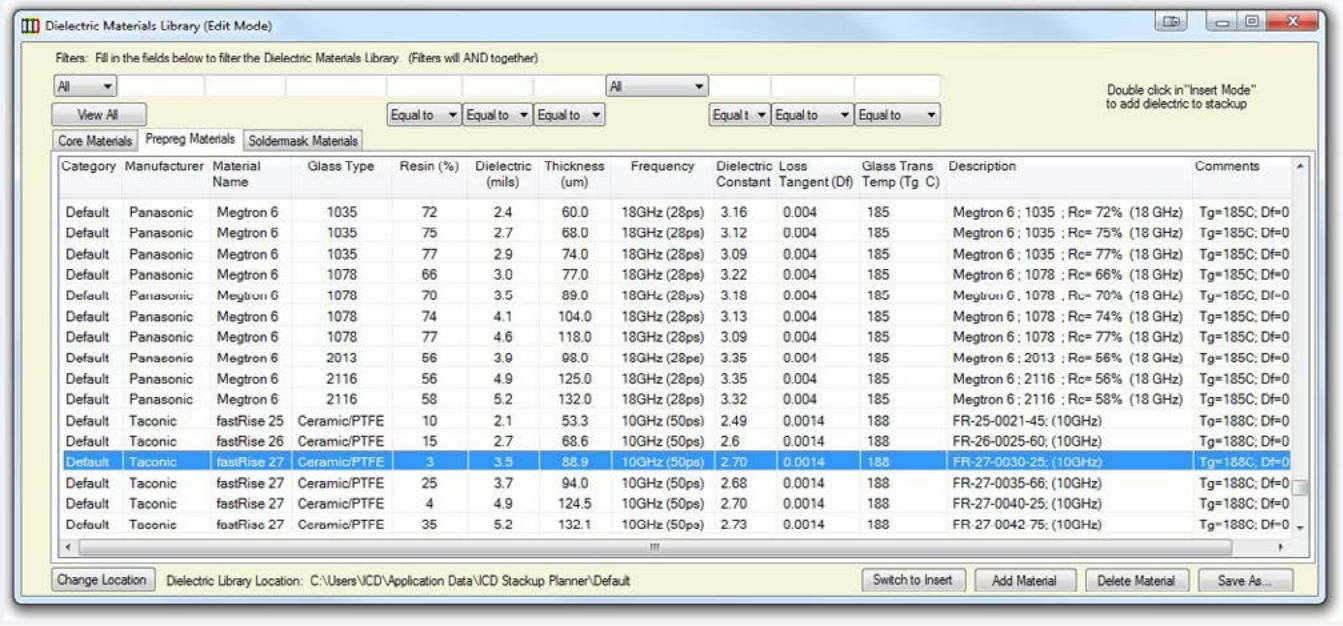


Figure 5. ICD Stackup Planner—Dielectric Materials Library with over 5,650 materials up to 40GHz.

Embedded capacitance technology allows for a very thin dielectric layer (0.24–2.0 mil) that provides distributive decoupling capacitance and takes the place of conventional discrete decoupling capacitors over 1GHz. Unfortunately, standard decoupling capacitors have little effect over 1GHz and the only way to reduce the AC impedance of the power distribution network above this frequency is to use ECM or alternatively die capacitance. These ultra-thin laminates replace the conventional power and ground planes and have excellent stability of dielectric constant and loss up to 15GHz.

The ZBC-2000 laminate is constructed using a single ply of either 106 or 6060 style prepreg, yielding a dielectric thickness after lamination of 2 mil, when measured by cross-sectioning. The ZBC-1000 technology results in a 1 mil dielectric distributed capacitance material. FaradFlex™ and Interra™ buried capacitance products utilize a durable resin system for non-reinforced dielectrics for 1 mil thickness and below. Also with a product range up to 20nF per square inch in capacitance density, 3M ECM is the highest capacitance density embedded capacitance material on the market.

Zeta Lam allows significant layer count reduction in PCBs with better signal performance. Having a low dielectric constant combined with very high withstanding voltage, these glass free films change the design rules for via diameter and trace width, while still conforming to the manufacturing needs of the PCB shop. Three traces between vias at a 0.4 mm pitch is not only possible but very manufacturable according to Integral Technology.

For high-speed serial link performance, reliability and production yields are of greater importance than cost. But unless you are pushing limits of the technology, then a dielectric material of Df < 0.01 will most likely suffice.

Points to remember

- A transmission line looks very similar to a low-pass filter—which of course attenuates high frequencies
- A square wave is made up of a number of sinusoid waveforms, of different frequencies, however only the lower frequencies components can transverse the transmission line
- FR-4 has negligible loss at frequencies below 1GHz. But since the dielectric loss is frequency-dependent, at higher frequencies the dielectric loss of FR-4 increases
- The maximum bandwidth of a signal is not determined by the fundamental frequency but rather by the rise time of the signal—5th harmonic
- At high frequencies, a non-uniform dielectric in the substrate can cause skew in differential signals
- A fiberglass-free material such as fastRise27 can be used to eliminate differential skew

Manufacturer	Material	Description	Thickness (mil)
3M	ECM	Embedded capacitance material	0.24, 0.47, 0.55
DuPont	Interra HK04	Ultra thin laminate	0.5, 1.0
Integral Technology	Zeta Bond	High T_g epoxy based adhesive film	1.0, 1.5, 2.0
Integral Technology	Zeta Lam SE	Low CTE C-stage dielectric with a Hi T_g	1.0
Integral Technology	Zeta Cap	Hi performance polymer coated copper	1.0
Oak-Matsui Technology	FaradFlex	Planar capacitor	0.31,0.47,0.63,0.94
Sanmina	ZBC1000	Buried cap, hi performance decoupling	1.0
Sanmina	ZBC2000	Buried cap, hi performance decoupling	2.0

Table 2. Embedded capacitor materials available in the ICD Dielectric Materials Library.

• Close attention should be paid to the skew associated with the fiber weave effect

• Specify a denser weave material (2113, 2116, 1652 and 7628) compared to a sparse weave (106 and 1080)

• DC blocking capacitors are common sources of impedance discontinuities in high-speed serial channels. The optimum routing structure has a 20–25 mil wide cutout, under the capacitor lands, depending on the distance to the lower plane.

• Planar capacitor laminate or embedded capacitor materials are becoming a cost-effective solution for improved power integrity. **PCBDESIGN**

References

1. Intro to Board-Level Simulation and the PCB Design Process, Barry Olney

2. Board Level Simulation and the Design Process: Plan B: Post Layout Simulation, Barry Olney

3. Practical Signal Integrity, Barry Olney

4. Altera Application Note AN528

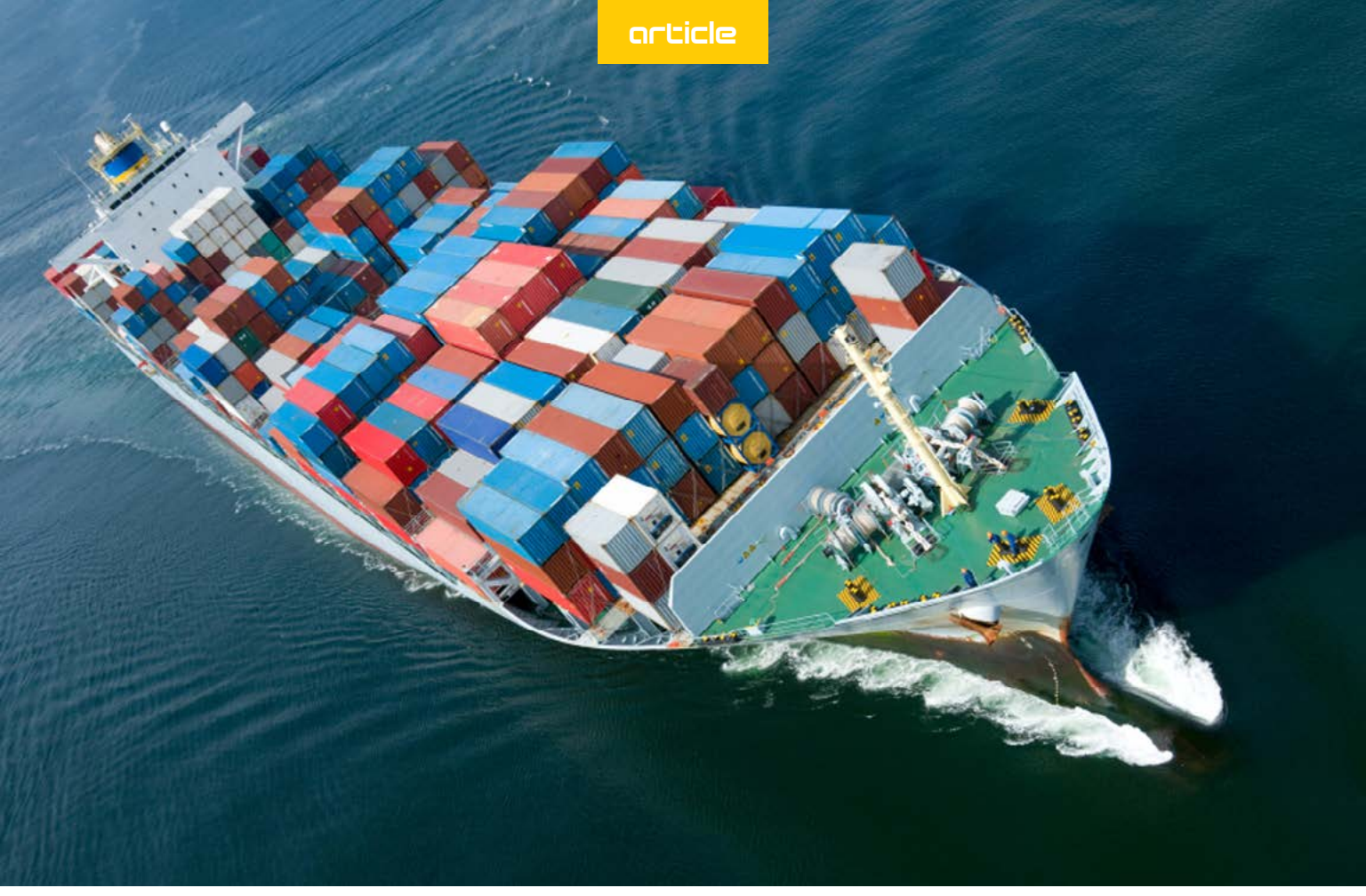
5. Samina, 3M, Integral Technology, Dupont Nelco, Isola laminate datasheets

6. Signal and Power integrity Simplified, Eric Bogatin

7. High Speed Digital Design, Howard Johnson

The ICD Stackup and PDN Planner can be downloaded from www.icd.com.au

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. ICD is a PCB design service bureau and specializing in board-level simulation. The company developed the ICD Stackup Planner and the ICD PDN Planner software. To read past columns or contact Olney, click here.



Domestic vs. Offshore PCB Manufacturing

by Nolan Johnson
SUNSTONE CIRCUITS

SUMMARY: ***If you are sending your PCB manufacturing offshore, what factors weighed heaviest in your decision-making? How do you know if offshore manufacturing still makes sense for you? This article considers both simple and complex ideas for cost-benefit analysis to help guide your decision process.***

Larger manufacturing industry trends are taking hold in the PCB world. With high-volume manufacturers like General Electric profitably reshoring large-scale production, PCB manufacturers are taking note and challenging old paradigms. PCB design complexity is increasing and production volumes are dropping, and many manufacturers are finding that the realized savings from offshoring may not offset the risks associated with it.

A growing list of factors is tipping the scales back in favor of domestic PCB manufacturing. Three basic elements from this list underpin a simple cost-benefit analysis. They are:

- Rising wages abroad
- Persistent high overseas transportation costs
- Limited improvement of speed to market

The Trend Away From Offshore PCB Manufacturing

In the case of low-volume, single-run PCB manufacturing, a simple measure of the cost delta between domestic and offshore production illustrates dwindling savings. The average manufacturing wage abroad is increasing 18–20% per year while domestic worker productivity continues to improve, adding to the appeal of home grown manufacturing. Overseas shipping remains expensive just as cheaper domestic energy is lowering the cost of production in the

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U.S. Delays have always cost money, so the additional time still required for an offshore vendor to manufacture and deliver a PCB becomes a bigger issue. As the cost differentiators narrow or even reverse with changing conditions both here and abroad, the trend toward reshoring is gaining momentum.

Problems with quality assurance (QA) are helping to accelerate this reshoring trend. Quality issues occur frequently and are usually preceded by an absence of transparency. Collaboration with offshore manufacturers is inherently limited, and the loosely-coupled relationships foster a 'take what you get' transactional paradigm. This leaves the product manager to hope and assume his PCB is properly manufactured to design while offshore.

Offshore quality control issues are expected to fuel the return of at least $2.5 billion in electronics manufacturing to the U.S. over the next three years. PCBs represent a significant portion of that amount, meaning projects requiring small to mid-level PCB volumes can no longer settle for offshored product that almost meets—or fails to meet—design requirements.

Your IP is at Risk

The same PCB designs not being manufactured to spec are increasingly at risk of piracy. GE reshored its Geospring water heater in 2012, even though they had already initiated production abroad. The move was motivated by the need to protect the company's intellectual property. If the intellectual property of one of the world's largest corporations is fair game, what is the risk to a PCB design from a company with fewer legal resources?

Online PCB chatter about reverse-engineering in Chinese facilities illustrates the frustration felt by product managers who send production abroad to save money. The money saved offshore is promptly lost if you suddenly find yourself competing with a cheaper version of your own design.

Domestic PCB Manufacturing: The Benefits

We have found that asking the right questions leads to the best outcomes when considering offshore versus domestic PCB manufacturing. Lower-volume PCBs face greater relative risk to the bottom line, so risks of offshoring can help make domestic manufacture more appealing for this type of product.

Reshoring may even be the preferable—though not obvious—choice for higher-volume PCB manufacturers. With larger production volumes, even modest per-unit savings can appear attractive on the surface, suggesting that offshoring is the right choice. However, those savings paint only half the picture. Our experience tells us that less easily quantifiable factors pose greater obstacles to offshoring than rising Chinese wages or high crude oil prices.

When you weigh the pros and cons of offshore manufacture, we advise two critical actions:

- Carefully consider the less apparent problems associated with offshoring
- Ask questions aimed at challenging both options

Offshoring Production, Onboarding Problems

As easily identifiable costs associated with overseas PCB manufacturing rise and gain media attention, you should also consider less apparent complications. If you plan to offshore PCB manufacturing, carefully examine the impact to your domestic operations.

We encourage our customers to avoid evaluating the potential costs of offshore PCB manufacturing along only two dimensions. Rising transportation fees and overseas wages tell an incomplete story. There are real, indirect costs that may be minimizing or even eliminating savings from offshore manufacturing.

If you carry more inventory than necessary to optimize your transportation buy, the real expense of overseas shipping also includes the costs to store, handle, and insure excess supply. An offshore supplier unable to support your just-in-time (JIT) inventory requirements translates into unfulfilled orders and lost business. When offshore PCBs come close—but fail to meet—design specifications, the resources required to re-tool the boards or adapt the product to accommodate them masks the real cost of low yield.

Once these potential hidden costs are con-

sidered, the net savings from offshoring may not justify the risk to your overall operation.

Risk Can Unleash Additional Costs

Offshore PCB manufacturing does incur risk, and mitigation of that risk places a burden on your domestic team. This creates additional hidden costs that can quickly add up to offshore manufacture actually being more expensive than domestic. How much time and effort do you spend coordinating and policing offshore PCB manufacturing?

An overseas manufacturer in a time zone ten to fourteen hours different from yours literally builds your board while you sleep. Unfortunately, if you need to collaborate about the project with someone on the offshore team, one of you will be getting up in the middle of the night to do so. Disruptions to routine like this come with a cost. Cultural differences can lead to miscommunications, misunderstandings, and expensive mistakes.

In order to ensure an offshore PCB build is properly executed, some measure of domestic resource must be diverted to focus on it. The critical question is, "How much?" To be fair, offshoring can also save significant amounts of money if it is a good fit for your needs. From our experience, once you measure the true cost drivers of offshore production and identify its impact on domestic operations, the answers to a few more key questions will illuminate the best choice for you.

Does Your Volume Justify the Journey?

Volume is one critical factor in determining whether to use a domestic or offshore manufacturer. Offshoring favors established PCB designs requiring high-volume runs with long lead times. The larger potential aggregate savings better insulates your bottom line against less apparent offshore manufacturing costs.

The return on offshore manufacturing investment diminishes quickly when dealing with lower volume or prototyping production. Offshore production manufacturers are optimized for large runs and will not deviate from process to devote additional attention to nonconforming projects. This QA risk alone should give lower-volume producers pause. A domestic resource offers more transparency to the manufacturing process, and collaboration happens faster and with less effort. Issues resolve quickly, which minimizes risk to yield and PCB quality.

Depending on your annual volume, even one trip to Shanghai or Chennai to address quality issues could reduce or eliminate savings from offshoring. Overseas site visits really guarantee nothing. If your product requires a more agile process that includes design conception or prototyping, you make yourself vulnerable to a wide range of new variables and pain points.

> ***Depending on your annual volume, even one trip to Shanghai or Chennai to address quality issues could reduce or eliminate savings from offshoring. Overseas site visits really guarantee nothing.***

During prototype design, you need effective communication and coordinated effort to succeed. Transition plans, phase-ins, phase-outs, and revision control demand immediate attention that is sometimes unavailable because of time zone differences or language barriers. Respected PCB fabricators in the U.S. build their businesses by excelling in these areas, while offshore vendors simply aren't structured to provide the responsive support often required in such situations.

Even if you have an established PCB design to manufacture, unless you are prepared to overstock to accommodate your offshore vendor, larger production runs will take precedent over yours. This widely accepted practice impacts scheduling and can ripple through your supply chain, adding up to significant delays in getting the finished product out the door. Domestic manufacturers are structured for better flexibility, able to provide real time support, and more likely to better meet the needs of low volume production. If you operate on a JIT basis, fabricators located in your hemisphere also pose less of a scheduling risk.

DOMESTIC VS. OFFSHORE PCB MANUFACTURING *continues*

In cases where offshoring fits volume and scheduling needs, be prepared to deal with cultural differences in business paradigms. What you may consider a problem with scheduling or quality may be your offshore vendor's idea of premium service and products. Does your offshore supplier share your vision of good customer service? If your foreign PCB supplier does not buy into or understand your expectations, no amount of intercontinental oversight will bridge that chasm.

Are You Getting What You Paid For?

Once your boards arrive from the offshore fabricator, yields become your next concern. We again encourage multi-dimensional analysis of the production. Instead of targeting a percentage yield and checking a box, also consider consistency of yields over time along with the board's functional reliability in the end product.

Long-term reliability is a key measure. Counterfeit components routinely find their way into PCBs manufactured offshore. Some substandard parts are easy to spot, others not so much. A Rolex knock-off purchased from a Hong Kong street vendor requires some time before the cheap internal parts fail and the faux precious metal tarnishes. Likewise, counterfeit components in your offshore PCB may stand up to initial testing, then fail after your product is in use. Counterfeit components impact product performance, end customer satisfaction and eventually your reputation in the marketplace. This makes for a high price to pay, but a difficult cost to measure

Your intellectual property is at greater risk once it moves offshore. The threats to your IP are complex, vary from country to country, and require substantial financial commitment to combat. Domestic patent, trade secret, and mask work laws are antiquated and provide minimal protection. Little or no motivation exists in places like China to protect U.S. corporate intellectual property. Their laws aimed at protecting foreign IP are mostly toothless and carry limited enforcement effort with them.

As we pointed out, even GE chose to reshore its product rather than spend financial resources battling the threat to their IP in China. Smaller companies realistically have few options for securing their IP. Thoroughly vetting partners to determine reliability can help, but most companies are making a leap of faith when they send their IP offshore.

> ***Offshoring no longer guarantees a lower cost of production. Threats to intellectual property in countries like China have heightened interest in reshoring. As a result, trends indicate PCB manufacturing is returning home.***

Conclusions

Offshoring no longer guarantees a lower cost of production. Threats to intellectual property in countries like China have heightened interest in reshoring. As a result, trends indicate PCB manufacturing is returning home.

Making the right decision about domestic versus offshore PCB manufacturing depends on a thorough cost benefit analysis. Your results will vary depending on volume and design requirements. We encourage our customers to look for hidden costs of offshoring and seriously consider its less quantifiable pain points, like the impact on inventory management and burden on the domestic operation.

When you remove hidden assumptions and question offshoring paradigms, the answers you find will guide you toward better outcomes. You might find that a domestic manufacturer that specializes in low-volume, high-mix manufacturing provides a viable alternative to offshoring your project. **PCBDESIGN**

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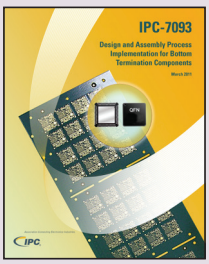
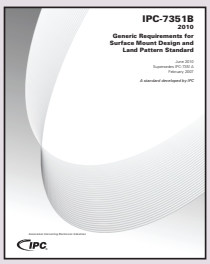
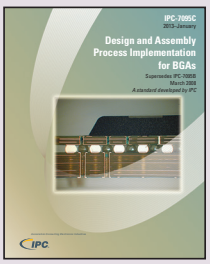
- IPC-2226, *Sectional Design Standard for High Density Interconnect (HDI) Printed Boards*



IPC-7093, *Design and Assembly Process Implementation for Bottom Termination Components*



IPC-7351B, *Generic Requirements for Surface Mount Design and Land Pattern Standard*



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Mil/Aero007 News Highlights

PCB Sales to Mil/Aero Market Remains Positive

Despite cutbacks in the U.S. military budget, cumulative rigid PCB sales to the military market from January through May this year were up 3.4% compared to the same period in 2012, while rigid PCB sales to other markets were down 9.1% year-to-date.

IPC DVD Helps Industry Understand Conflict Minerals Regs

"The proceedings DVD gives those who could not attend the summer conflict minerals conference the opportunity to benefit from the knowledge shared by industry experts and the experiences of those in the trenches…" said Fern Abrams, director of government relations and environmental policy.

Endicott Interconnect Secures Re-certifications

Endicott Interconnect Technologies, Inc. recently announced the completion and passing of several critical re-certifications including AS/EN/JISQ9100:2009—Revision C, ISO 9001:2008, and ISO 13485:2003.

Micropack Achieves AS9100 ANAB Accreditation

"Micropack Limited has always focused on meeting the stringent challenges of the industry and AS9100 certification is a major step in our endeavor to achieve excellence and to meet the exacting demands of the aerospace and defence industries. Nadcap certification is next in our road map," said CEO Sreekar Reedy.

Invotec Develops PCBs for European Comm Satellite

Invotec Group took a keen interest in the launch of Inmarsat's latest satellite, Alphasat, in July. The most sophisticated commercial communications satellite ever launched, Alphasat features an advanced digital integrated processor system built by Astrium in the UK and incorporating PCBs manufactured by Invotec Group.

SOMACIS Earns Nadcap Merit Status for Electronics

The company has been awarded Nadcap Merit status for Electronics at its Italian facilities, covering rigid and HDI PCBs. The very first European PCB manufacturer to achieve the Nadcap accreditation, SOMACIS has held the accreditation since 2005.

Multilayer Technology Earns AS9100C Re-certification

The company has announced completion of and passing the AS9100C re-certification audits. The re-certification consisted of three full days of intense auditing of all departments by a registrar. This audit marks the three-year anniversary that the company has achieved and maintained this certification.

Park Electrochemical Unveils Very Low-Loss RF Material

Park Electrochemical's NL9000 RF/microwave electronics materials products feature very low-loss, high-frequency transmission and exceptional antenna gain and directivity performance.

HEI Q2 Sales Up 35%

"Our Victoria operation continues to grow with the large contracts relating to the military radio systems and other customer demand. We are also seeing operational improvements in the Victoria and Tempe plants with better flow and improving yields," said HEI CEO, Mark B. Thomas.

Rogers Introduces Improved Antenna Grade Laminates

The company's Advanced Circuit Materials Division introduced improved high-frequency materials to address several market needs. The RO4700JXR Series antenna-grade laminates were designed for use in base station, RFID, and other antenna designs and combine low-loss dielectric with low-profile copper foil for reduced passive intermodulation (PIM) and low insertion loss.

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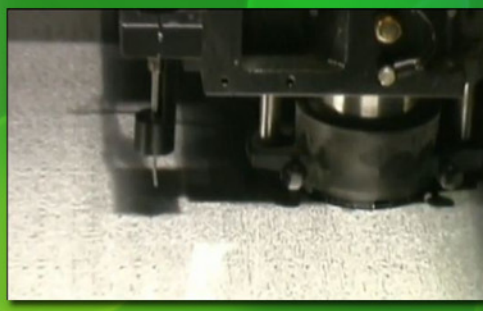

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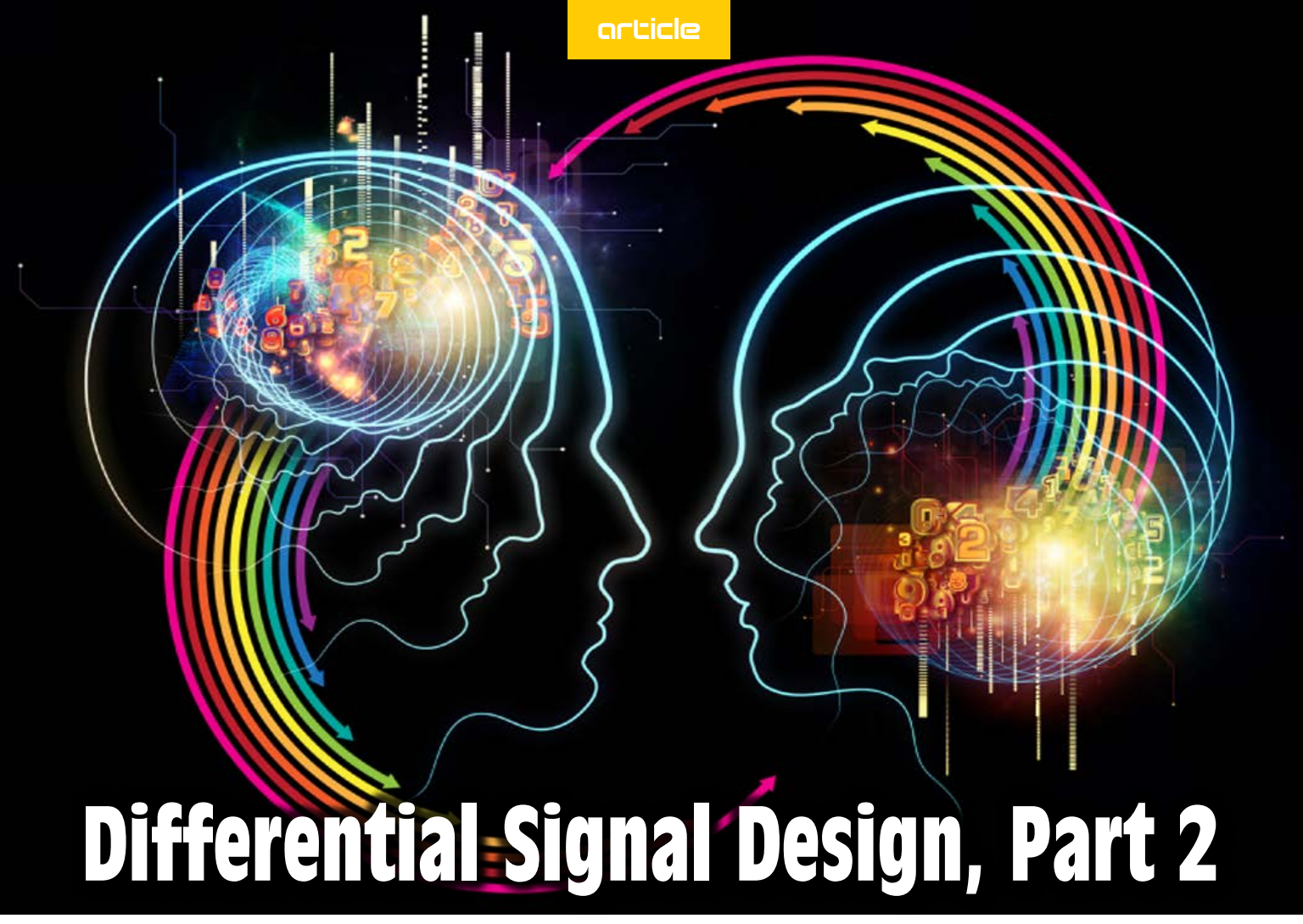

Differential Signal Design, Part 2

by Lee W. Ritchey
SPEEDING EDGE

SUMMARY: This month, Lee Ritchey concludes his two-part series on differential signal design and design rules, and he addresses some of the many misconceptions surrounding diff pair design.

How should differential pairs be routed?

From the discussion in Part 1 of this series, it can be concluded that tightly coupled differential pairs carry two handicaps. The first is that for a given impedance the traces will have to be narrowed in order to maintain the desired differential impedance. Second, the differential pair must remain tightly coupled along its entire length resulting in routing restrictions that can prove to be a problem. As a result, it is advisable to design a stackup and trace width that meets both the skin effect loss requirements and achieves differential impedance that results in only minor changes in impedance when the pair must be separated to pass through a tight pin field.

The design rule that satisfies the above conditions is a "not closer than" spacing that results in no routing restrictions. The loosely coupled example above is such a "not closer than" case.

A big advantage of routing using the "not closer than" rules for differential pairs is that both single-ended traces that are meant to be 50 ohms can use the same trace width as the differential pairs with a differential impedance specification of 100 ohms.

Determining what the "not closer than" spacing must be involves deciding how much impedance variation when differential pairs are separated is acceptable. There isn't any hard answer, but a rule that is couched in terms of 2H or 3H, with H being the height above the plane, is arbitrary. A precise method for arriving at an answer involves using a 2D field solver to calculate the impedance change as the space between the two traces is decreased. I have set a limit of 5% impedance change as acceptable. This is half of the ±10% that the PCB impedance can be expected to vary. I have designed

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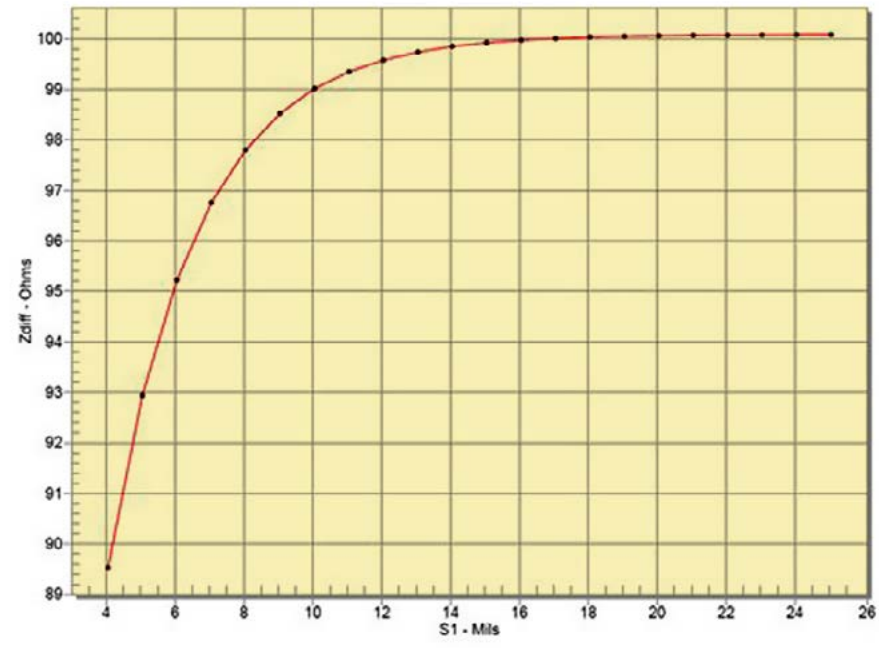


Figure 10. Differential impedance vs. separation.

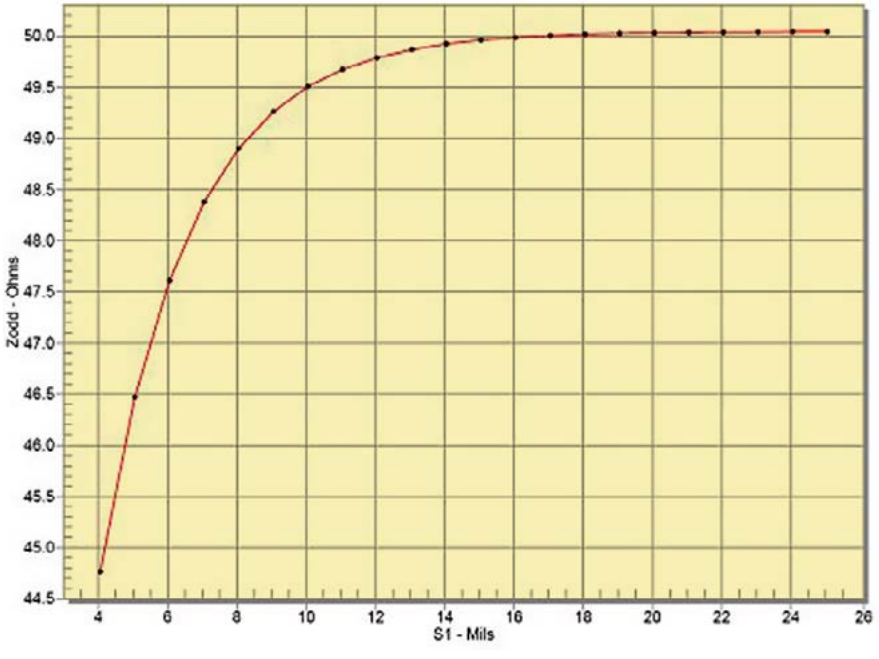


Figure 11. Single-ended impedance vs. separation.

in excess of 100 PCBs using this method, with excellent results.

Figure 10 shows how differential impedance goes down as the two traces in a pair are moved closer together. Notice that at 10 mil separation the impedance has dropped only 1 ohm or 1%. Figure 11 shows the single-ended impedance of one of the traces in the pair as the two traces are moved close to each other. Notice that with wide separation the impedance is 50 ohms and drops to only 49.5 ohms at 10 mils separation. This why it is reasonable to route single-ended and differential traces using the same trace width so long as separation is maintained. It is also why it is not necessary to measure differential impedance when the "not closer than" rule is followed.

The differential pairs in this study are centered stripline spaced 4 mils from either plane using 3313 laminate and prepreg.

Is a differential impedance specification necessary?

Nearly all specifications for impedance of differential pairs are for the impedance across the pair. The discussion above of how a differential pair works shows that the circuit does not depend on a differential impedance. Why, then, is differential impedance always specified? The reason that differential impedance is almost always specified rather than single-ended impedance is that it is thought that differential impedance is different than the sum of the two impedances when the individual impedance is measured from "ground" to either of the two traces. It turns out that it is possible to measure either side of the pair and look for 50 ohms if the differential impedance has been specified at 100 ohms.

If the routing instructions are given as "not closer than" as described earlier, it is not even necessary to build a test structure that is a differential pair to get accurate results.

Where do return currents flow?

Much has been written about where the return currents for a differential pair flow. There is even one textbook on high-speed design that pictures such a current flow in a differential pair on its cover with current flowing out one side and back in the other. A common assumption is that the return current for one member of the pair flows in the other member. This assumption is based on the fact that the two currents are equal and opposite. This is just a happy coincidence.

Referring back to the schematic in Figure 1, seen in Part 1 of this article, it can be seen that each transmission line is a standalone transmission line that operates independently from the other. They happen to be the same impedance and are terminated in the same impedance, so their currents happen to be equal and opposite. They do not have to be the same impedance for the circuit to work; they just have to be properly terminated.

If the two currents are independent of each other, where do their return currents flow? It is useful to understand why the currents flow in the first place. The signal integrity issue is concerned with what happens as the logic states change or the transient behavior of the circuits. When a transmission line changes logic states, a current needs to flow to charge up or discharge the parasitic capacitance of the transmission line to alter its voltage. It is reasonable to expect that the two currents, the outbound current and the return current, will flow in the two sides of this parasitic capacitance.

When the transmission line is routed by itself this parasitic capacitance exists between the transmission line and the planes over which or between which it travels. If a second transmission line, such as the other member of the differential pair, is routed close to the first one, a small amount of parasitic capacitance will exist between the two lines. For even the tightest routing that is manufacturable, this capacitance is a very small fraction of what exists between the line and the planes, so a tiny amount of the return current would flow in the second transmission line or the partner line.

Figure 10 shows the E fields on the top half of the diagram and the current distribution in the traces and planes in the bottom half immediately after the logic state has changed. This is a simulation that shows where the currents are flowing in a differential pair routed between two planes (stripline). Notice that the current distribution in the two traces is crowded near the surface with none flowing in the center of the conductor. This is what is known as skin effect. At very high frequencies the current is crowded near the surface of the conductor due to the rapidly changing magnetic field surrounding the conductor.

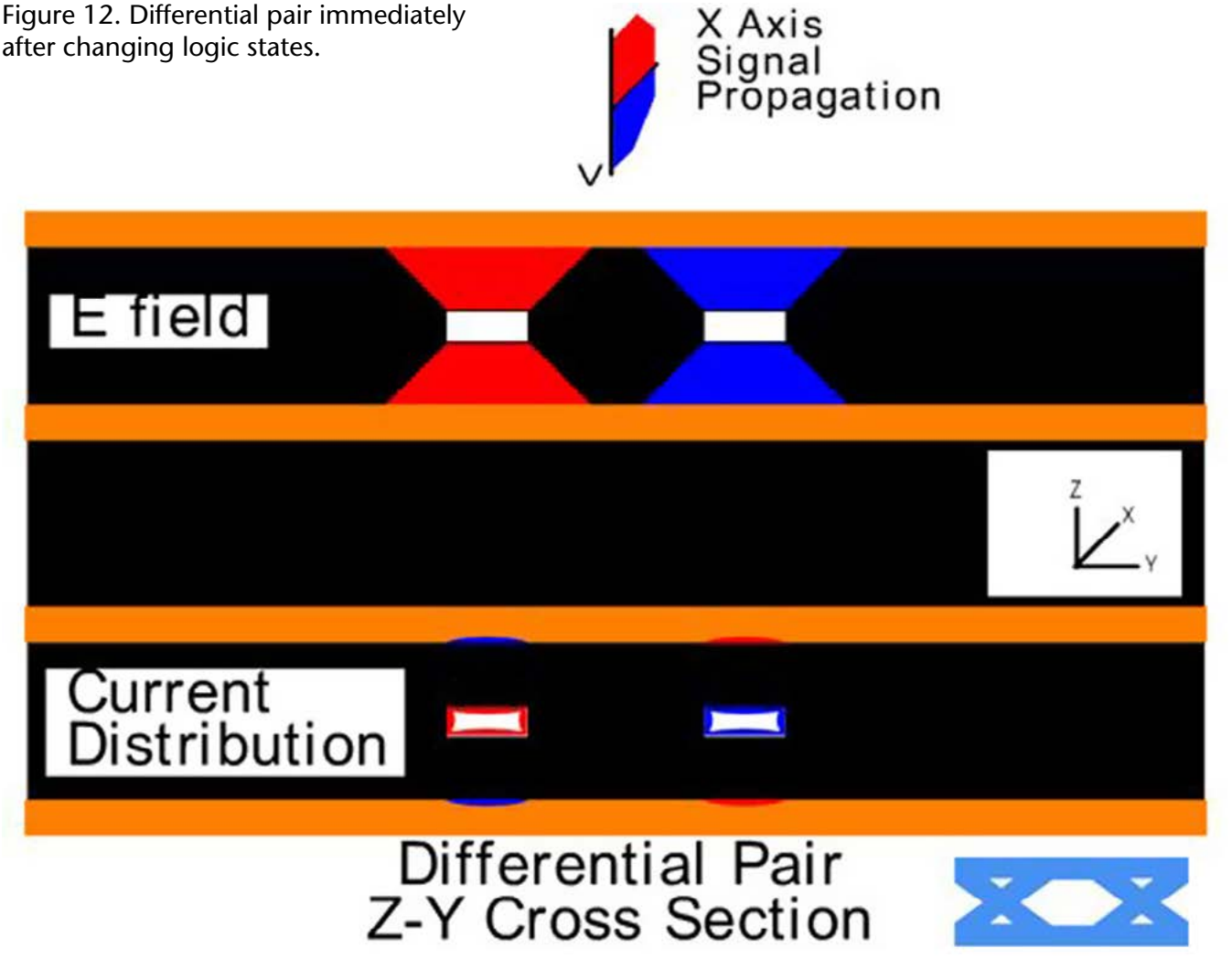
Also notice that there is an opposite current under each trace in both planes. (Red represents flow in one direction and blue in the other.) These are the return currents for each of the transmission lines. It is flowing there to charge up or discharge the parasitic capacitance between each trace and its plane partners.

This simulation was done by Teraspeed Consulting using a 2D field solver. It is an animation from which one frame has been taken during the switching event. When the animation is allowed to run to steady state, the currents flow evenly throughout each trace and evenly throughout each plane. This is the "low-frequency" behavior of any transmission line. The high-frequency behavior shows that the currents crowd near the surface of any conductor and the return currents flow in the "partner" of the transmission line. In this case, the partners are the planes, not the other traces.

Does tight coupling eliminate or reduce crosstalk into a differential pair from an aggressor signal?

One of the alleged advantages of routing differential pairs with tight coupling is that it eliminates crosstalk from nearby aggressor signals. The underlying assumption is that noise from the aggressor is coupled into both members of the differential pair in equal amounts producing what is called "common-mode" noise. Since differential pairs are known for their ability to ignore or reject common-mode noise, this is a noble objective.

Figure 12. Differential pair immediately after changing logic states.



For common-mode noise rejection to be effective, the magnitude of the offending noise source must be equal as it intercepts both members of a pair. Figure 13 illustrates worst-case cross talk for off center stripline transmission lines when the height above the nearest plane varies from 5 mils to 15 mils and the separation varies from 5 mils to 100 mils. The most striking characteristic of coupled lines traveling over a plane is how rapidly the crosstalk drops off as the separation is increased. This crosstalk is a direct indication of the strength of the EM field as the distance from the transmission line is increased.

Figure 14 shows two methods for routing a differential pair. The upper diagram shows routing one trace over the other in adjacent signal layers or "broadside" routing and the lower diagram shows side-by-side routing in the same layer as the aggressor. In each case, the routing is 5 mil lines and 5 mil spacing. Looking at the H = 5 mils curve in Figure 13, one can estimate the magnitude of the crosstalk into each of the two members of the pair when routed side by side (coplanar). It can be seen that the crosstalk into the near member of the pair (DIFF A) is 12% and the crosstalk into the far member (DIFF B) is 2%. Cleary, this is not common-mode coupling since the magnitude of the induced noise is much larger in the near line than the far line.

If one examines the broadside structure, it can be seen that the noise induced in the member of the pair in the same plane as the aggressor (DIFF A) is 12%. The chart does not show the magnitude of the crosstalk into the trace in the other signal layer (DIFF B), but with a good

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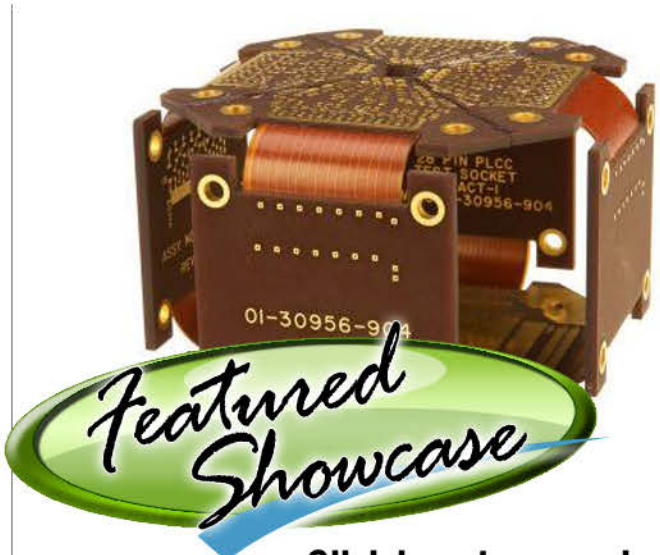

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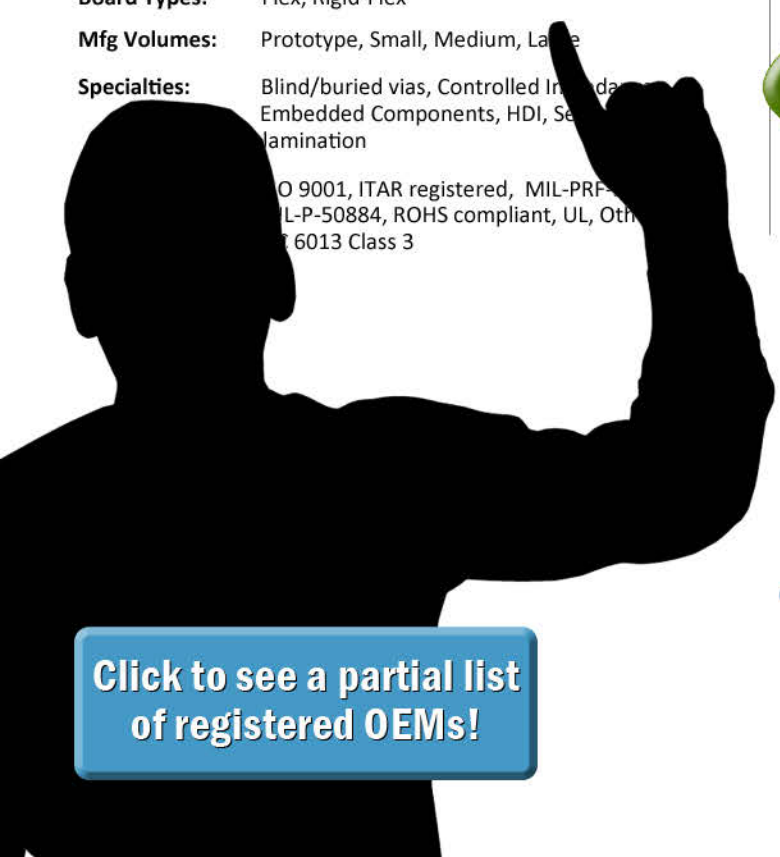

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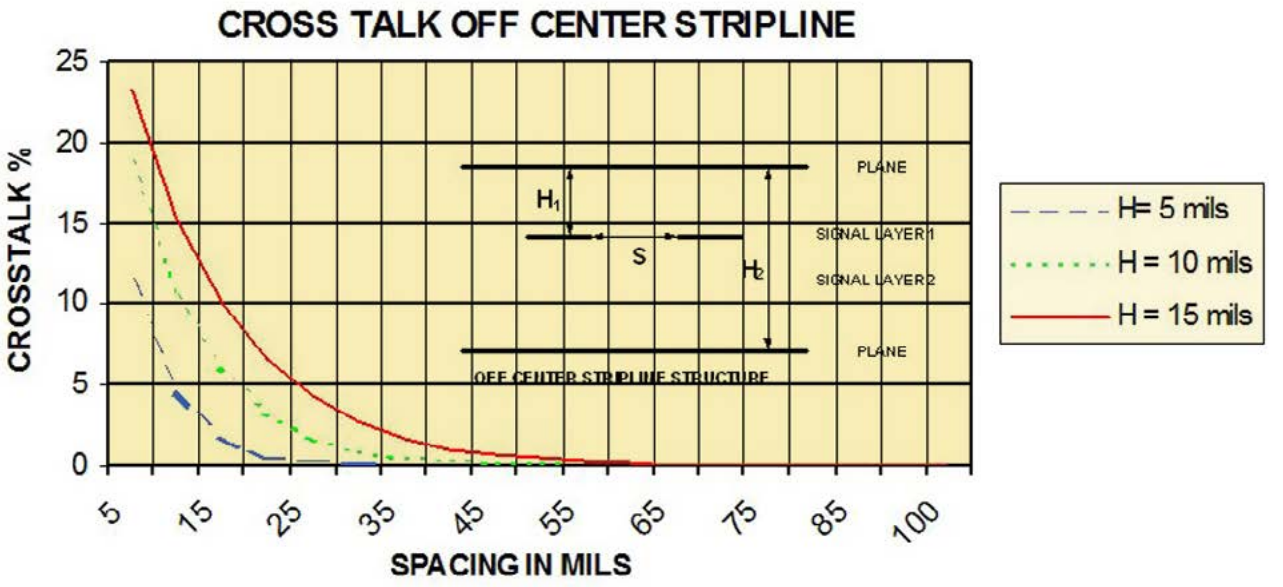

Figure 13. Worst-case crosstalk, off-center stripline.

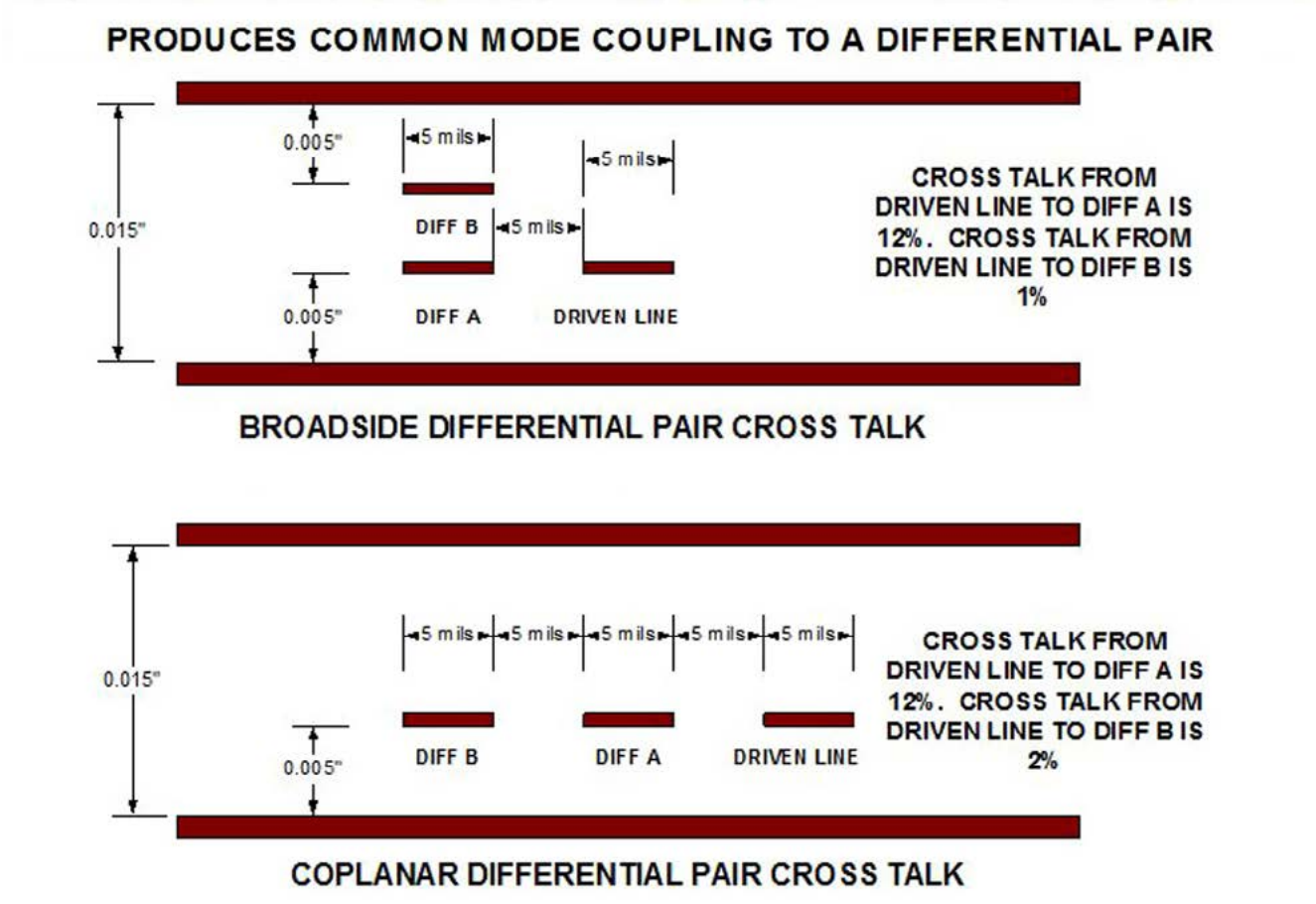

Figure 14. Possible ways to route differential pairs near an aggressor.

2D field solver can be shown that the magnitude of the crosstalk is on the order of 1%.

Clearly, neither method of routing is capable of creating common-mode coupling or crosstalk.

If tight coupling between members of a differential pair does not protect them from crosstalk, what should the routing rules be to avoid crosstalk problems? The only reliable method for controlling crosstalk into a differential pair is to do analysis that establishes the maximum allowable crosstalk into either side of the pair and impose a spacing rule that guarantees this limit is not violated.

Is broadside routing of differential pairs beneficial?

There are design guidelines that recommend routing differential pairs broadside or one over the other in adjacent signal layers. The usual reasons given for doing this are that tight coupling is good and that common-mode noise rejection is better when the pair is routed this way. The benefit of tight coupling was discounted earlier in this paper.

From Figure 1, it can be seen that there is no beneficial relationship between the pair of transmission lines. Their only relationship is equal and opposite signal amplitudes and tight timing to each other. From Figure 14 it can be seen that neither coplanar routing nor broadside routing of a differential pair results in common-mode noise rejection due to crosstalk from an aggressor signal. In fact, if the broadside pair is routed between a Vdd and Vss plane, as is usually the case, there will be differential noise injected into the member of the pair that is routed next to the Vdd layer due to ripple or power supply noise on the power plane. The only way to prevent this is by surrounding the broadside pair with ground layers on both sides which either adds extra layers to the PCB stackup or compromises the PDS system.

In addition to the above considerations, broadside routing complicates PCB layout by blocking routing channels in both layers of an adjacent signal layer pair, often forcing the use of more signal layers and increasing the cost of the PCB more than would otherwise be needed. Insuring that the adjacent signal layers are precisely aligned at the PCB fabrication shop is also made more difficult when broadside routing is done.

Is there a situation where common-mode coupling into a differential pair exists?

There must be a case where common-mode noise coupling into a differential pair is possible, since so many engineers believe it is possible. Such a case exists. One example is the unshielded twisted pair (UTP) used for virtually all phone wiring as well as for most wired Ethernet. Figure 15 shows a differential pair with the EM fields surrounding each member of the pair. Notice that outside the pair the EM field lines area equal and opposite. As a result, there is no detectable field outside the pair when differential signals are traveling on it.

When a source of EM noise is located above or below the pair, the field strength of the EM field is the same amplitude as it intercepts both wires. Any noise coupled into the wires is equal in amplitude and the same polarity. This is the "common-mode" noise that is referred to when tight coupling is said to result in common-mode noise. When the noise source is located to the right or left of the pair, the strength of the field is slightly less in the member of the pair that is in the shadow of the other member and, as a result, the magnitude of the noise induced into

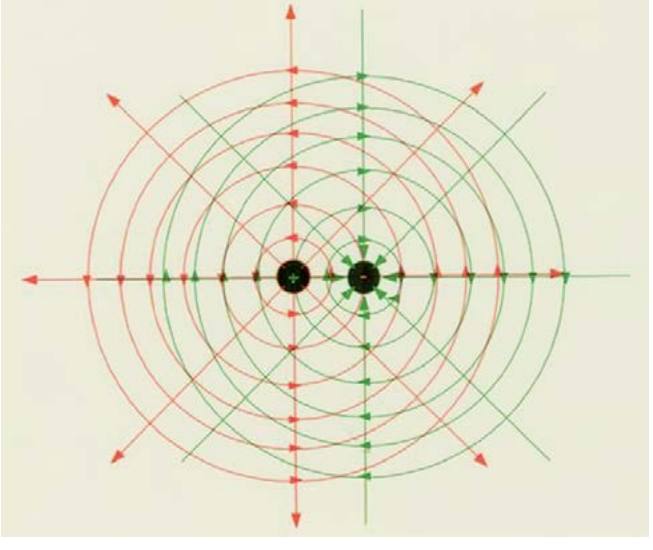

Figure 15. An unshielded differential pair showing field lines.

the near wire is larger than the far wire resulting in "differential noise" coupling. True, the difference is not large, but it is measurable. To avoid this problem, the wires are twisted so that one wire is near the noise source for a while and then the other one is (the unshielded twisted pair, or UTP).

Even with the tight coupling of a differential pair suspended in space it is difficult to maintain common-mode rejection without twisting the pair. What chance is there to achieve common-mode rejection in a PCB when the members of the pair travel over a plane? None.

What are the power delivery requirements of differential pairs?

A close examination of the circuit in Figure 2 reveals that the current consumed by both the driver and receiver circuits is constant. All than happens when the circuit is active is that the current in either box is simply switched from one side of a circuit to the other as the logic state changes. As a result, the current demand from the power delivery system is constant or "DC." This means that the power delivery circuit does not need to be very complex if the only circuits being powered are differential drivers and receivers. The power supply could be a simple battery and these circuits would function correctly.

Most simple differential driver receiver pairs are relatively insensitive to ripple on Vdd. However, due to often poor advice about how to design the PDS, large amounts of ripple can be present on Vdd. A common type of ripple or noise on Vdd is switching voltage transients that are generated by DC-DC converters. These voltage spikes often exceed the ratings of the differential circuits, resulting in poor signal quality. A common solution has been to insert a ferrite bead in the Vdd lead of the differential driver circuit. As long as the driver is a simple one, as shown in Figure 1, this remedy appears to work. As a result, the kneejerk solution to poor PDS design is to insert ferrite beads and other components into the power lead of each driver. This has resulted in excessively complex layout problems around FPGAs and other circuits with many differential drivers.

A far easier solution to this problem is to design the PDS in such a manner that the noise transients are not present. The methods for doing this level of design are well documented in the design handbooks mentioned earlier.

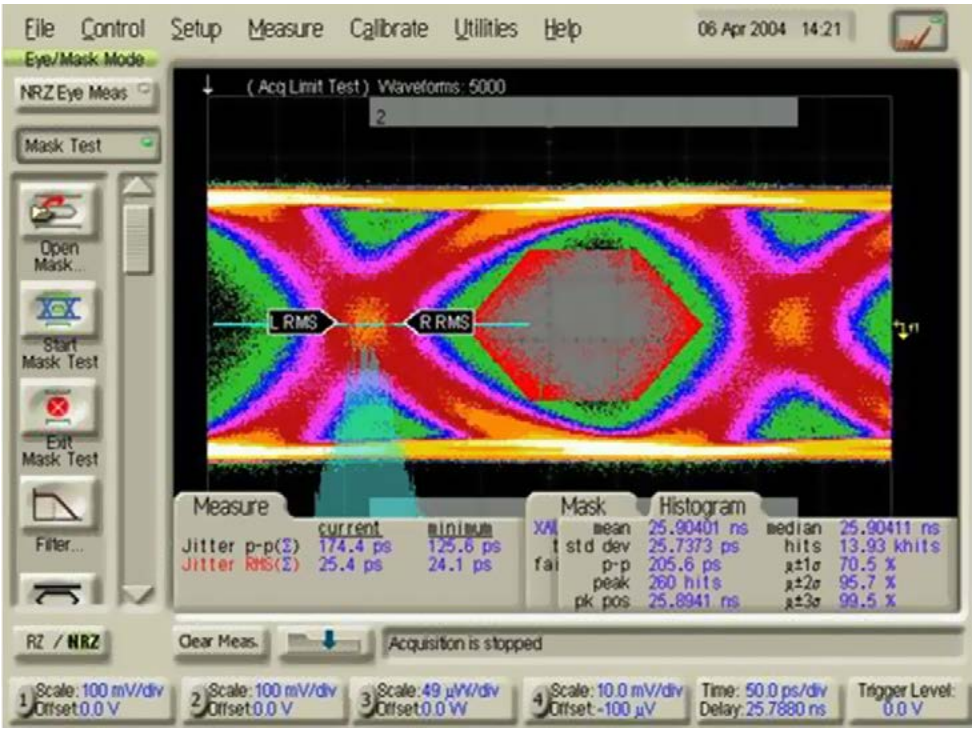

Figure 16. 3.125 Gb/S eye with ferrite.

Most differential drivers used for gigabit and higher differential signaling circuits are not as simple as that shown in Figure 1. They often contain encoding circuits as well as pre-emphasis or de-emphasis circuits in the drivers that are single-ended. These circuits require varying current at very high frequencies. Placing ferrite beads in series with their Vdd leads results in severe signal degradation. Figure 16 is the eye diagram mea-

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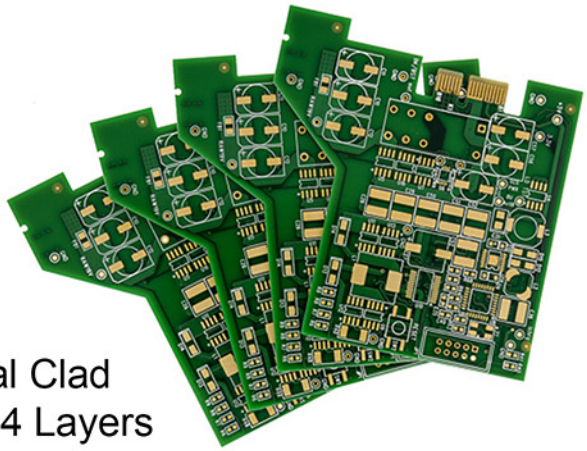

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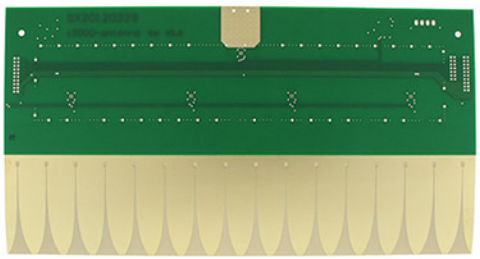

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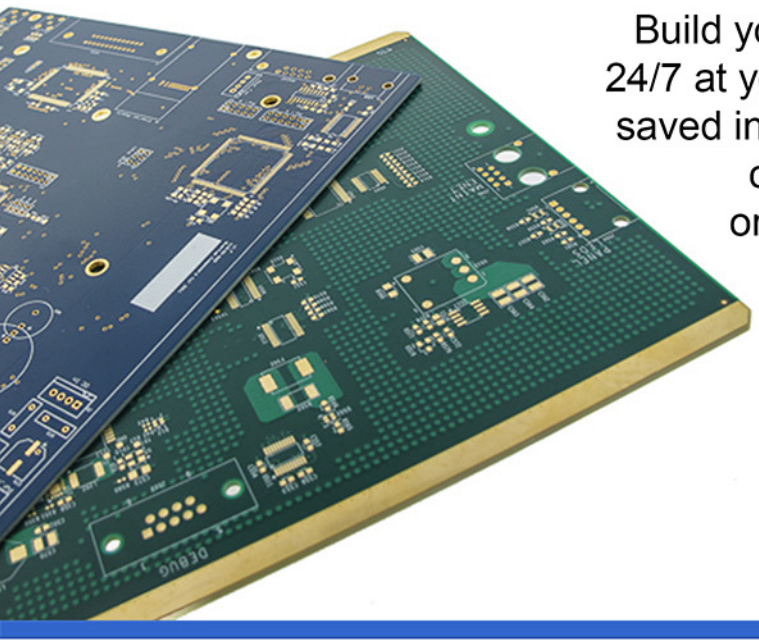

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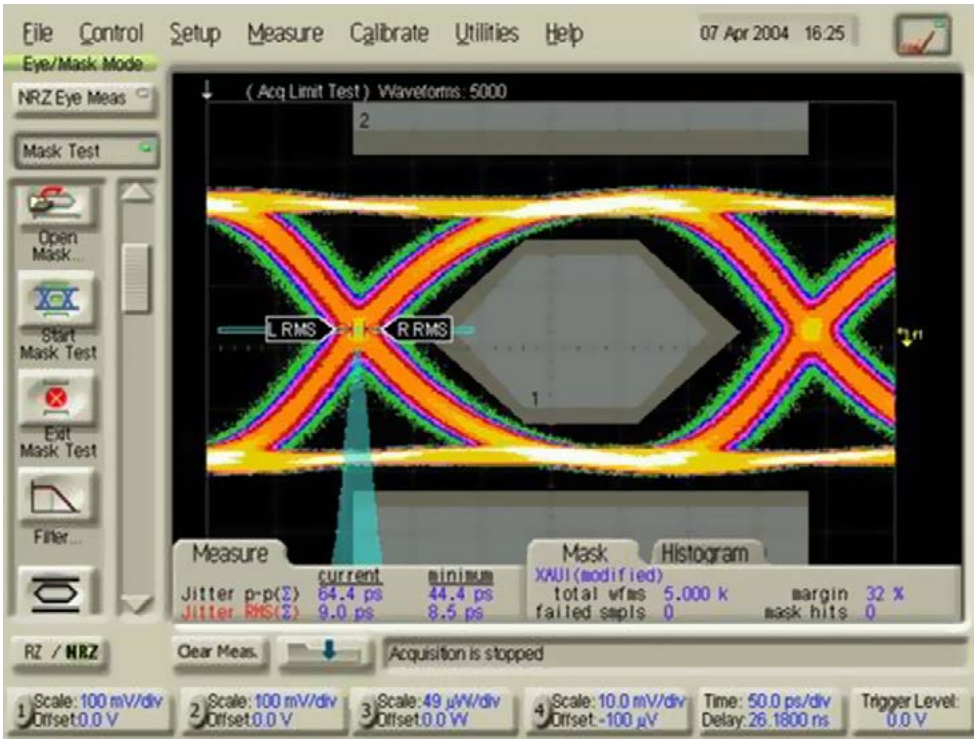

Figure 17. 3.125 Gb/S eye without ferrite.

sured on a 3.125 Gb/S serial link with a ferrite bead inserted in the Vdd lead of the driver. As can be seen, the eye is severely degraded. This degradation was caused by inserting the ferrite bead in the power lead resulting in a very poor quality source of current for the driver. Figure 17 is the same circuit with the ferrite bead removed. The improvement is dramatic. When the engineer who inserted the ferrite bead was asked why he did it, his answer was that there was excessive noise on Vdd and he hoped the ferrite bead would remove it. It did so, but at the peril of the driver circuit operation.

This is an example of treating a symptom rather than the problem. In most cases, as in this one, the use of ferrite beads in power leads treats a symptom. The symptom in this case is there is too much ripple on Vdd. The cause is a poorly designed PDS. In the first example presented here, the ferrite bead cured the symptom without generating an undesirable side effect. The second example treated only the symptom and introduced a bigger problem.

In summary, simple differential driver receivers can tolerate a relatively poor power delivery system due to the constant current nature of their circuits. Gigabit and higher differential signaling protocols commonly have varying current demands that will be as high in frequency as the signals involved in the signal path. As a result, a PDS design that will supply all of these frequencies is required. Since surface mount bypass capacitors are effective only up to a little more than 100 MHz, it is necessary to have some amount of inter plane capacitance as well.

Linear vs. Switching Power Supplies

Most FPGA vendors require the use of linear supplies for the high speed serial links that are often a part of their high performance offerings. The reason these are specified is that the authors of the applications notes in which this requirement is contained do not realize that the switching spikes that commonly are part of the output from switching supplies are rather easily suppressed. Many of the switching power supply vendors have applications notes that describe how to deal with these switching transients.

Separate SERDES Supplies

The same vendors that specify linear-only supplies for their SERDES also require a separate supply voltage for them even though other parts of the FPGA use the same voltage. The reason for doing this is to prevent "noise" from other parts of the design from coupling into the SERDES. The solution to this problem is to design a single supply that has ripple or noise which is within the tolerance of all the circuits being powered. Most vendors do not know the noise tolerance of their SERDES so this complicates doing an adequate design. From experience it can be said

that virtually all SERDES currently on the market are capable of withstanding as much as 50 mV of ripple without noticeable degradation. This is a target that is readily obtainable with standard capacitors.

Figure 18 is a 22-layer PCB with one 1152-pin FPGA in the center that has all of its SERDES used, as well as 200+ single-ended I/O. It also has two 10 Gb/S ports in the lower right corner and two 1 Gb/S ports in the upper right-hand corner. It has no ferrite beads in any supply and the SERDES supply voltage is shared with other parts of the FPGA. Each supply voltage impedance was designed to be 10 mOhms or less from DC to 150 MHz with 10 or more nF of plane capacitance for each supply. When the system is running at full traffic, there is no measurable ripple on any of the seven supplies.

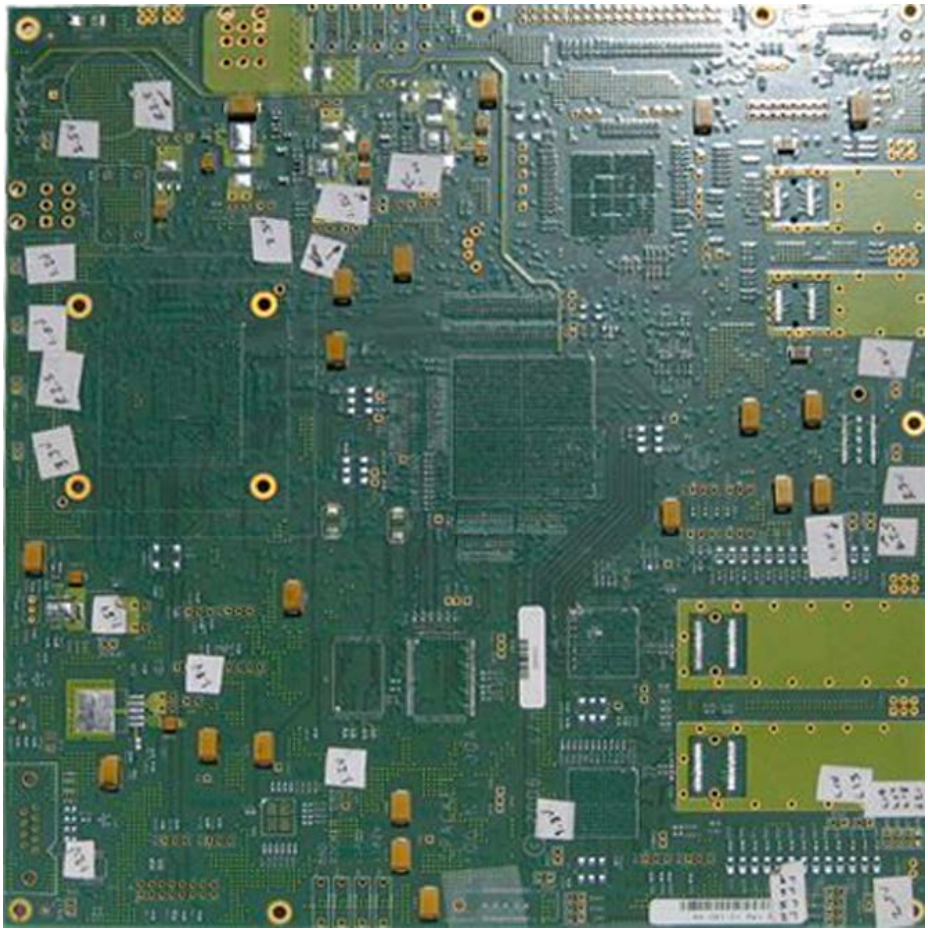

Figure 18. PCB with seven ps voltages, no ferrite beads.

Do routing vias cause signal degradation in differential signals?

In the context of this question, a routing via is any via used to connect a component lead to an internal layer or to allow a signal to change layers. These vias usually have a drill diameter of 12 mils and add a parasitic capacitance of about 0.5 pF to the trace where they connect in a PCB that is 100 mils thick.

A common restriction placed on routing high-speed traces is that no vias are allowed for fear that they will degrade the signal. This has the effect of constraining routing to a single layer of the PCB, often a severe restriction that forces the use of more signal layers than might actually be needed. The signals in Figure 6 have two or four vias along their length. As can be seen, the loss vs. frequency of the two paths is virtually the same and linear indicating that adding routing vias does not have a notable effect on the signal path. (The plated through-holes required by press-fit connectors are much larger and, as a result, have substantially more parasitic capacitance and can have an adverse effect on the signals at high frequencies.)

One exception to the above explanation is the case of a four-layer PCB such as a PCB used for a PC motherboard. In this case, when the via is used to transition from the top signal layer to the bottom signal layer, there is no easy path for the return current and there will be signal degradation. The degradation does not stem from the via itself, but from the act of layer changing. To avoid this problem on a four-layer PCB, the signals must start and end on the same signal layer and not pass through to the other signal layer.

Do right-angle bends cause SI problems in high-speed differential pairs?

This is another of the many issues that worry design engineers. Many of the applications notes and design guides for differential signaling, as well as single-ended signaling, prohibit the use of right angle bends for fear they will degrade the signals. The origin of the rule prohibiting the use of right angle bends is covered in Chapter 25 of Volume 1 of my book Right the First Time, along with measurements that show right angles in traces to be invisible to at least 20 GHz. References 16 and 20 at the end of this article are additional studies that show right-angle bends are not to be feared in logic designs.

Are there other advantages of differential signaling?

As noted earlier, the equal and opposite nature of the differential pair means that demands on the PDS are less than for a similar single-ended data path. This has a significant benefit when passing signals into and out of IC packages. Much has been written about simultaneous switching noise (SSN) of wide, single-ended buses and the signal integrity problems associated with Vdd and ground bounce in IC packages. Often, this limits the width of parallel data buses or forces the total redesign of IC packages to reduce SSN as the rise and fall times of the signal get faster. Replacing wide, parallel buses with high data rate differential links solves this problem.

Another benefit of differential signaling, again, because of the equal and opposite nature of the two signals, is the reduction or elimination of EMI when signals must travel on cables or flexible circuits. This is the fundamental reason that fast Ethernet does not cause an EMI problem even though the signals are traveling on an unshielded twisted pair. The connection between a laptop motherboard and the display is another place where this property is used, as are differential connections between PC mother boards and disc drives.

“Another benefit of differential signaling, again, because of the equal and opposite nature of the two signals, is the reduction or elimination of EMI when signals must travel on cables or flexible circuits. This is the fundamental reason that fast Ethernet does not cause an EMI problem even though the signals are traveling on an unshielded twisted pair.”

Where will differential pairs appear in the future?

DDR memory buses have become quite large; often as many as 130+ single-ended address and data paths are used. Simultaneously, these paths have increased in speed and their rise and fall times have become very small (less than 200 pS). This has resulted in severe problems with SSN. The current speeds of DDR2 are reaching the limits of what can be done to increase bandwidth of the memory subsystem to keep pace with the increase in CPU speeds.

The DDR standards body is working on a memory architecture that is based on converting the wide parallel data buses to very high speed differential paths. This is possible at a reasonable cost due to the reduction in the cost of creating serdes to get back and forth between serial and parallel data streams. This new memory architecture is in the prototype stages at the present time.

Are new sources of SI problems emerging for diff signals as speed increases?

In addition to signal degradation from reflection and crosstalk, there can be signal attenuation stemming from skin effect losses and losses in the dielectric used to fabricate the PCB. The frequency or data rate at which these losses become a factor depend on the highest frequency in the data stream, the length of the path and the type of dielectric material used.

There is a desire in some quarters to have a simple rule of thumb that allows easy determi-

nation of when the speed is fast enough that these losses need to be accounted for. This would certainly be handy. Unfortunately, the problem is too complex for such an easy solution. The only way to be certain that these two sources of degradation are not going to be a problem is by using a good signal integrity analysis tool to simulate the actual proposed path with the materials and signals to be used. This analysis is not difficult to perform and is an integral part of good systems engineering.

As speeds exceed 2 Gb/S there is another potential source of signal degradation that is difficult to isolate. This degradation shows up as excessive jitter on the receive signal and skew between the two sides of the differential pair. The source of this degradation is the irregular weave of the glass used in the laminate. There are at least two weaves, 106 and 1080 that cause this problem. This is discussed at length in Volume 2 of the book set mentioned at the start of this document and in reference 18 in the bibliography at the end of the document.

Summary of design rules for differential signals routed in a PCB

- Members of a differential pair do not have to be routed together
- Members of a differential pair should be routed to a "not closer than" rule
- Vias in differential pairs are not harmful
- Right angle bends in differential pairs are not harmful
- AC coupling capacitors may be placed anywhere along the length of the pair
- Length matching tolerance of a differential pair is determined using rise time at the receiver
- Specifying the single-ended impedance of each member of a differential pair is acceptable
- Parallel terminations of differential pairs should be sized on the high side of the PCB trace impedance tolerance
- Crosstalk spacing rules must account for the fact that there is no common-mode noise rejection in a PCB
- Broadside routing of differential pairs makes PCB layout more difficult than coplanar routing
- Broadside routing of differential pairs makes PCB fabrication more difficult than coplanar routing

Summary of rules that do not apply to differential signals routed in a PCB

- The return current for one member of a differential pair flows in the other member
- Ferrite beads should be placed in the Vdd leads of differential drivers
- Differential impedance is a necessary requirement for differential signaling
- Broadside routing of differential pairs results in signal integrity improvements

Tight Routing Hazards to Single-Ended Traces

While this topic is not directly related to differential signaling it is useful to examine how single-ended traces interact when routed tightly. All transmission lines interact with each other when they are placed close to each other whether they are on the same plane or an adjacent plane. In few, if any, cases including differential signaling discussed in this paper, is this interaction beneficial. Two effects of interaction that are not beneficial are crosstalk and reduction in impedance.

A common routing density left over from the time when impedance and crosstalk were unimportant due to the relatively slow rise times of signals produced by such logic at TTL or slow CMOS circuits is 5 mil lines and 5 mil spaces. Figure 13 shows how crosstalk increases as traces are routed ever closer together. For a 5 mil line 5 mil space routing strategy in a stripline layer with a height above the plane of 5 mils, the cross talk is 12%. Few logic families have enough noise margin to tolerate the level of crosstalk.

Another potentially damaging side effect of this routing density is shown in Figure 11, depicting single-ended impedance vs. separation to other traces routed in the same layer. Notice for a 50 ohm trace when the separation is 10 mils or more, the single-ended impedance of a trace is little affected by neighboring traces. When the spacing is reduced to 5 mils, the impedance drops to 46.5 ohms a 7% drop from what was expected. The reason that this hap-

pens is related to the fact that any metal introduced into the near field of a transmission line increases the parasitic capacitance per unit length of that transmission line. Increased parasitic capacitance on a transmission line results in a powered impedance.

When a second transmission line is added to the other side of this pair, the impedance of the line in the center is driven to about 42 ohms or an error of almost 16%, much larger than the tolerance specification placed on the PCB manufacturer. Such large changes in impedance compromise the entire reflection budget of most logic families.

The effects of this impedance variation is most visible when a trace is routed for part of its length parallel to one or more traces and then travels by itself for some distance. The 50 ohms measured on a stand-alone test trace can be reduced to a far lower value on signal traces.

From the above, it follows that routing rules for single ended traces should be similar to those for differential signals. A "not closer than" routing specification must be imposed to insure that impedance variations along the length of a routed trace are within signal integrity limits. **PCBDESIGN**

References

1. Child, Jeff, "Low-Voltage Differential Signaling (LVDS) Reports for Duty." Electronic Design. May 25, 1998.

2. Ritchey, Lee W, "How to Design a Differential Signaling Circuit." Printed Circuit Design, March 1999.

3. Crisafulli, Kellee & Kaufer, Steve, "Terminating Differential Signals on PCBs." Printed Circuit Design, March 1999.

4. EDN Staff, "Line Drivers/Receivers Conform to New LVDS Standards." EDN, June 10, 1999.

5. Johnson, Howard, "Differential Termination." EDN, June 5, 2000.

6. Desposito, Joseph, "Transceiver Chip Replaces Parallel Backplanes with High-Speed Serial Links." Electronic Design, February 7, 2000.

7. Goldie, John & Nicholson, Guy, "A Case for Low Voltage Differential Signaling as the Ubiquitous Interconnect Technology." Electronic Systems, March 1999.

8. Rothermel, Brent R, etal, "Practical Guidelines for Implementing 5 GB/S in Copper Today, and a Roadmap to 10 GB/S." DesignCon2000.

9. Cohen, Tom, et al., "Design Considerations for Gigabit Backplane Systems." DesignCon2000.

10. Patel, Guatam, et al., "Gigabit Backplane Design, Simulation and Measurement." DesignCon2001.

11. Bogatin, Eric, "The Return Current in a Transmission Line." Printed Circuit Design, Aug. 2002.

12. Bogatin, Eric, "When Should I Worry About Lossy Lines?" Printed Circuit Design and Manufacture, March 2005.

13. Bogatin, Eric, "A Designer's Guide to High Speed Serial Links." Printed Circuit Design, June 2005.

14. Clink, James, "Maximizing 10 GB/S Transmission Paths in Copper Backplanes." DesignCon 2003, January 2003.

15. Johnson, Howard, "Modeling Skin Effect Loss." EDN, April 2001.

16. Johnson, Howard, "Who's Afraid of the Big, Bad Bend? Right Angle Turns." EDN, May 2000.

17. Johnson, Howard, "Differential Signaling, Measuring Differential Impedance." EDN, January 2000.

18. Bogatin, Eric, "Skewering Skew, Laminate Weave Induces Skew." Printed Circuit Design and Manufacture, April 2005.

19. Theorin, et al., "Differential TDR Testing Techniques." W. L. Gore, March 1998.

20. Brooks, Douglas. "90 Degree Corners, The Final Turn." Printed Circuit Design, January 1998.

21. Brist, Gary et al., "Non-classical conductor Losses Due to Copper Foil Treatment." CircuiTree, May 2005.

Lee Ritchey is founder and president of Speeding Edge. A longtime PCB design instructor and consultant, Ritchey is the author of *Right the First Time: A Practical Handbook of High-Speed PCB and System Design.*

video interview

Ventec Repositions its Business for High Reliability

by Real Time with... CPCA

Mark Goodwin, general manager for Ventec's European operations, sits down with Marcy LaRont talk about market and products trends. Ventec is about to reposition its business to address the needs of the high-reliability market.

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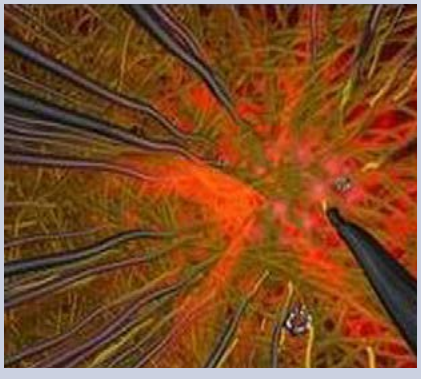
Scientists Develop Innovative Sensor for SERS

Scientists at ETH Zurich and the Lawrence Livermore National Laboratory (LLNL) in California have developed an innovative sensor for surface-enhanced Raman spectroscopy (SERS). Thanks to its unique surface properties at nanoscale, the method can be used to perform analyses that are more reliable, sensitive, and cost-effective.

Until now, the detection limit of common SERS systems was in the nanomolar range, i.e. one billionth of a mole. The results of a study conducted by Hyung Gyu Park, Professor of Energy Technology at ETH Zurich, and Tiziana Bond, Capability Leader at LLNL, were published this week as a cover article in the scientific journal Advanced Materials.



Raman spectroscopy takes advantage of the fact that molecules illuminated by fixed-frequency light exhibit "inelastic" scattering closely related to the vibrational and rotational modes excited in the molecules.

The key to the successful development of the sensor was therefore twofold: on the one hand, it was their decision to continue using CNTs, whose morphology is essential for maximising the number of "hot spots," and on the other hand, it was the fact that these nanotubes were double-coated.

Park envisions installation of the technology in portable devices. He stresses that invention of a new device is not necessary; it is simple to install the sensor in a suitable way.

Other potential applications include forensic investigations or military applications for early detection of chemical or biological weapons, biomedical application for real-time point-of-care monitoring of physiological levels, and fast screening of drugs and toxins in the area of law enforcement.

Electromagnetic Fields, Part 2: How They Impact Propagation Speed

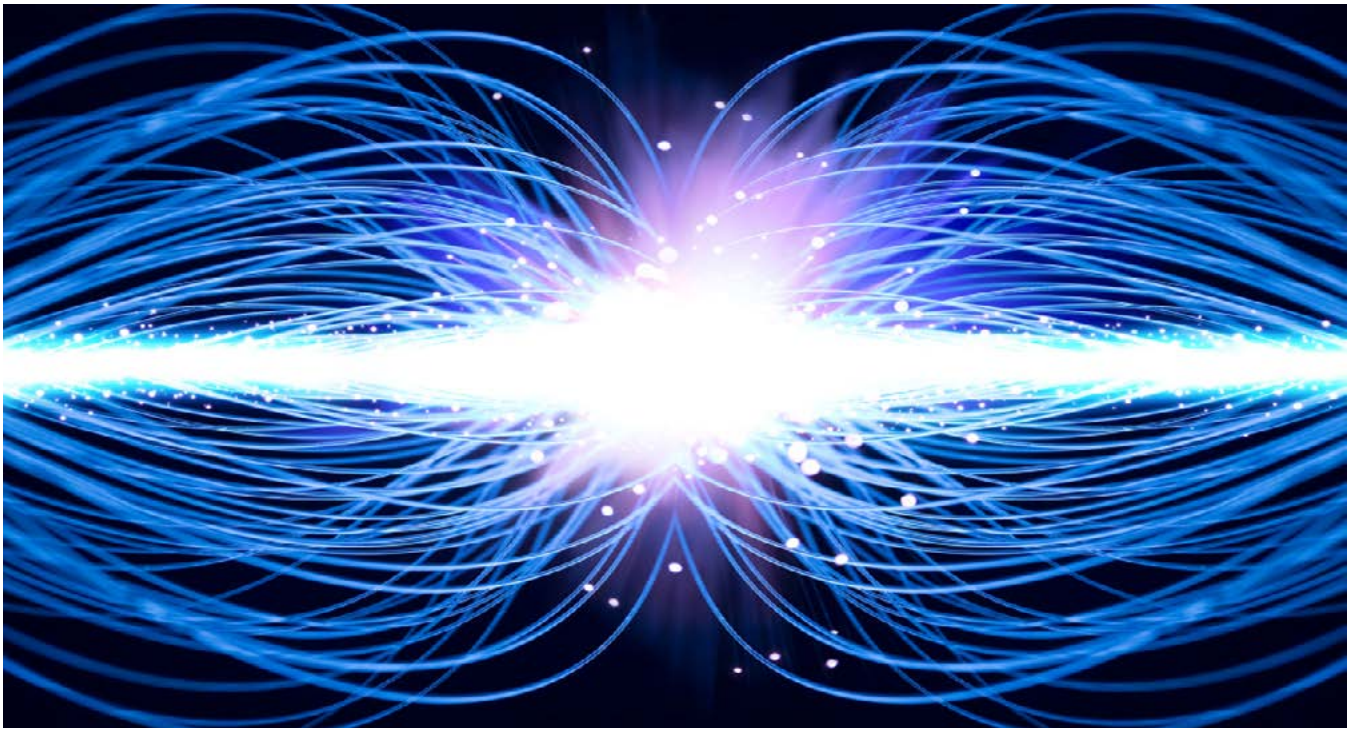
Douglas Brooks, Ph.D.
ULTRACAD DESIGN

In my August 2013 column in *The PCB Design Magazine,* I suggested that thinking in terms of what the electromagnetic field looks like around our traces might offer significant insight into how our circuits might be performing. In that column, I pointed out that the electromagnetic field had more to do with trace impedance than the specific trace dimensions did. That is, a trace can be "scaled" without changing the impedance (or the shape of the field.) But if the field distribution changes, then the impedance will change.

In this column, I am going to make similar observations about signal propagation speed. Recall that electronic signals travel at the speed of light, or 186,282 miles per second[1]. This equates to 11.8 inches/ns (or what we sometimes round off to a foot per nanosecond.) In any other material, the speed of light slows down. It slows down by the square root of the relative dielectric coefficient[2], Equation 1.

$$Speed = \frac{11.8}{\sqrt{\varepsilon_r}}\ in/ns \qquad \text{Equation 1}$$

Consider the situation shown in Figure 1. This is derived from a HyperLynx simulation. Here we have a trace in a stripline environment, surrounded by a dielectric. If we assume the relative dielectric coefficient of the dielectric is 4.0, then the propagation speed of the signal will be 11.8/2 = 5.9 in/ns (we sometimes round this off to 6"/ns.) Note the electromagnetic field in this figure. It is completely contained within the dielectric between the two planes on either side of the trace.



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ELECTROMAGNETIC FIELDS, PART 2: HOW THEY IMPACT PROPAGATION SPEED *continues*

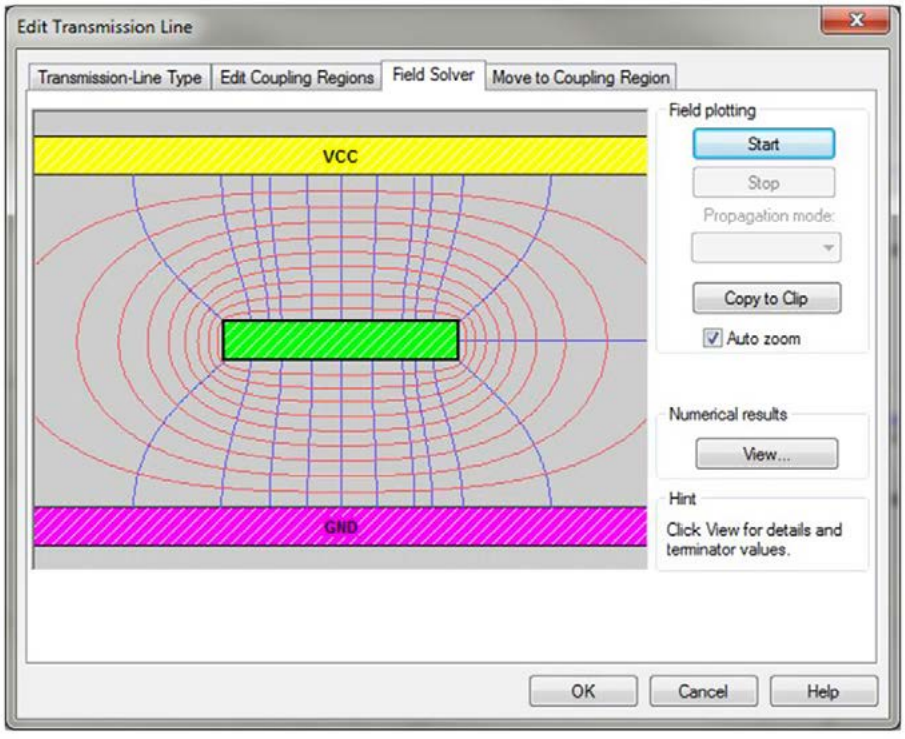

Figure 1. HyperLynx simulation showing an 8 mil trace spaced 5 mils from each plane.

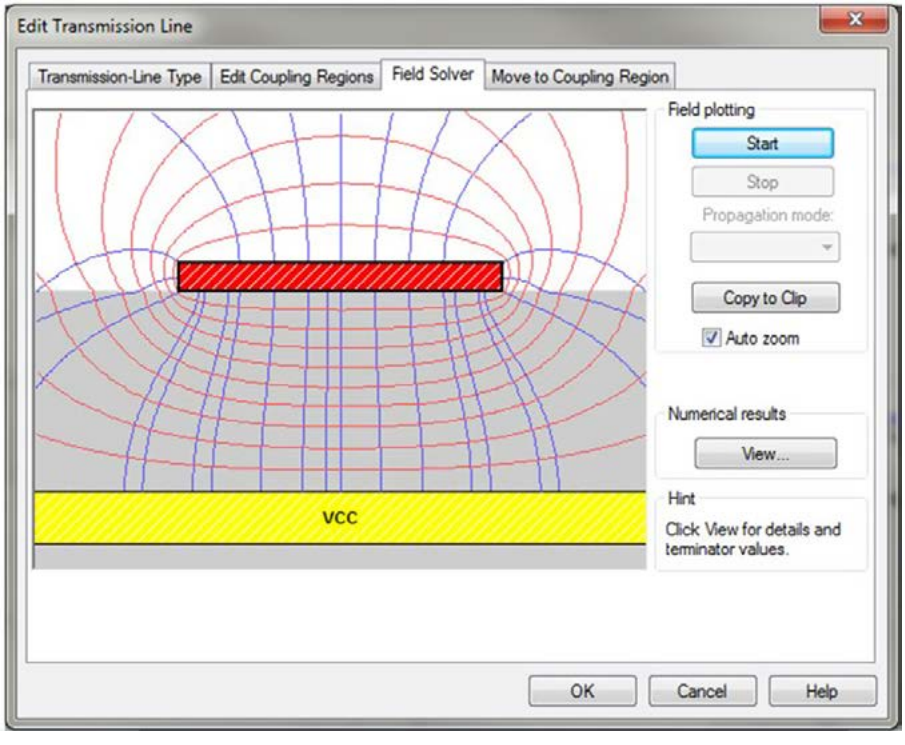

Figure 2. An 8 mil trace, 5 mils from a plane in a microstrip environment.

Now consider Figure 2. It shows the same 8 mil wide trace separated from a plane by 5 mils in a microstrip environment. By simply looking at the electromagnetic field distribution we can make a couple of observations. Part of the field is in the same environment as in the Stripline situation, so that part will want to travel at the same speed as above (5.9 in/ns). But part of the field is in the air. It will want to travel at the speed of light in the air, 11.8 in/ns. The fields cannot travel at different speeds than the current. The electric field cannot travel at a different speed than the magnetic field. They all have to travel together at the same speed. In a 2011 column, I showed how to calculate the propagation speed in such a situation, an admittedly complicated problem. But we can intuitively guess that the speed will be somewhere in between the stripline case and pure air.

This illustrates an important point:

Propagation speed does not depend on how fast the current can flow through a conductor. It depends on how fast the electromagnetic field can flow through the material it is flowing through.

Now, to illustrate this final point with more emphasis, consider Figure 3. It shows a 30 mil wide trace, 5 mils from a plane in a Microstrip situation. This is the same environment as in Figure 2, but with a much wider

trace. In this situation, a significantly greater portion of the electromagnetic field is captured between the trace and the plane, with a much smaller portion of the field in the air. We can intuitively infer that the signal will slow down, compared to that in Figure 2, because more of the electromagnetic field is contained within the slower dielectric. In the limit, for an infinitely wide trace, all the electromagnetic field will be in the slower dielectric and the propagation speed will be the same as in the stripline situation.

Just for interest, Table 1 shows what happens to propagation speed as the width increases in the example above. In every case, distance to any plane is 5 mils, relative dielectric coefficient of the dielectric is 4.0, and trace thickness is 0.5 oz.

The trend for the speed in microstrip to approach the speed in stripline as the trace width increases is clear.

1. This is the speed of light in a vacuum. The speed of light in air is almost the same; you need to be an astronomer to care about the difference.

2. All materials have a relative dielectric coefficient, which can be looked up in many different handbooks or on the web. FR-4, a common PCB dielectric, has a relative dielectric coefficient that is often given as 4.0, but might range between 3.5 to 4.5 or so. **PCBDESIGN**

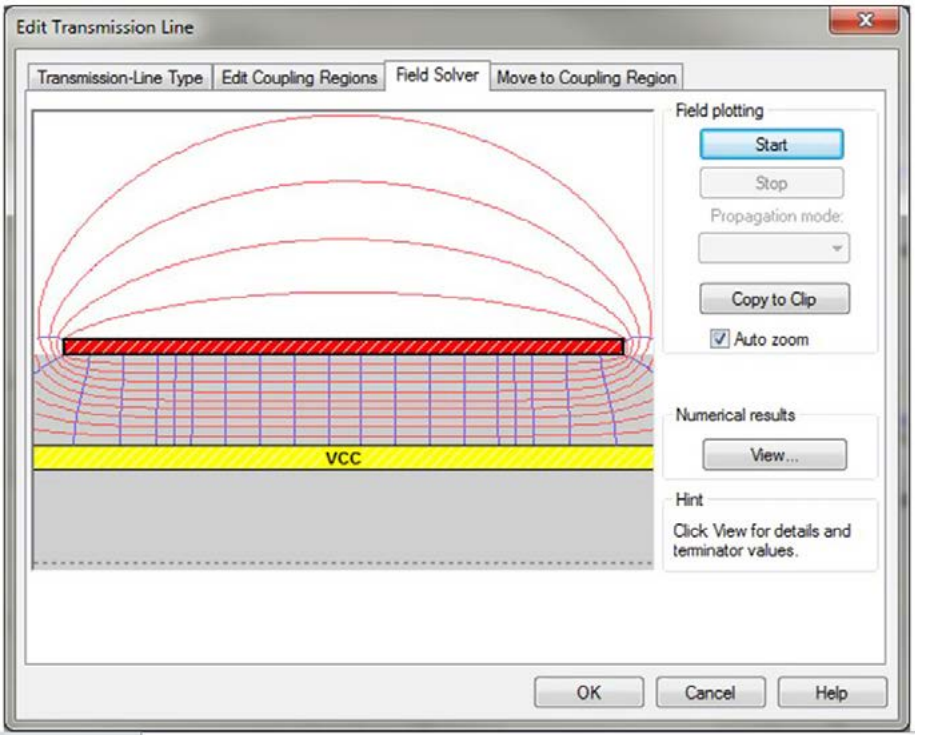

Figure 3. A trace 30 mils wide, 5 mils from a plane.

Width of trace (mil), microstrip	Propagation speed (in/ns)
Stripline (for reference)	5.9
8	6.9
30	6.5
100	6.2
500	6.0

Table 1. Propagation speed as width increases in Figure 3.

Douglas Brooks, Ph.D., is the founder of UltraCAD Design Inc. He has written numerous articles in several disciplines and held signal integrity seminars around the world. He has spent most of his career in the electronics industry in positions of engineering, marketing, management, and as CEO of several companies. Prentice Hall recently published Brooks' latest book, PCB Currents: How They Flow, How They React. Visit his website at www.ultracad.com.

TOP TEN

News Highlights from PCBDesign007 this Month

① Zuken to Invest $30-50 Million in U.S. Expansion

Zuken, a global leader in electronic design automation software, will invest $30 to $50 million in its U.S. based operation over the next three years. The Americas expansion will be anchored by a new Zuken innovation center located in Silicon Valley.

② DownStream Discounts Available Until September 30

Summer is winding down, but DownStream Technologies is offering a new seat of BluePrint-PCB 1000 or 2000 at 15% savings through September 30, 2013. Users who already have CAM350 can take advantage of this special offer and upgrade to DFMStream at savings of 25%.

③ Mentor Announces Agenda for IESF 2013

Mentor Graphics has announced the agenda for its thirteenth annual Integrated Electrical Solutions Forum. IESF 2013 is a day-long, free conference on September 19 which covers all aspects of electrical and electronic design/simulation within the automotive, commercial vehicle, and off-highway industries.

④ EDA Consortium Presents Export Seminar

The EDA Consortium is presenting a seminar on U.S. export regulations at its San Jose, California headquarters on September 18, 2013. Larry Disenhof, group director, Export Compliance and Government Relations at Cadence Design Systems, and the chairman of the EDAC Export Committee, will share his knowledge of the current state of U.S. export regulations.

5 AWR Names Winners of IMS2013 Student Design Contest

AWR Corporation, the innovation leader in high-frequency EDA software, gifted its software to the winners of the High Efficiency Power Amplifier and Software Defined Radio Student Design Contests offered at the 2013 International Microwave Symposium Microwave Theory and Techniques Society Conference.

6 Optimum Design Associates Passes SSQA Audit

Optimum Design Associates, an ISO 9001:2000 industry leader in the design, engineering, layout and assembly of PCB and turnkey EMS, recently passed the rigorous requirements of a standardized supplier quality assessment (SSQA) conducted by Applied Materials.

7 IPC and JPCA Release Design Guideline for PEC

One of the more important documents for the nascent printed electronics industry was completed early this month. IPC/JPCA-2291, Design Guideline for Printed Electronics, will help design teams use additive manufacturing processes to make electronic circuits.

8 Altium, Desktop EDA Partner on ECAD & MCAD Integration

"By partnering with Desktop EDA, we're extending Altium's market-leading position as a native 3D PCB design system provider," said Daniel Fernsebner, director of technical partnerships for Altium. "Desktop EDA apps for Altium Designer focus on bringing greater productivity to mechanical designers working with PCB designs."

9 Mentor Posts Record Results; Exceeds Guidance by 50%

Mentor Graphics Corporation announced revenues of $253.2 million for the company's fiscal second quarter ended July 31, 2013. For the third quarter of fiscal 2014, the company expects revenues of about $260 million, and maintains revenue expectations of about $1.155 billion for FY 2014.

10 Zuken Releases CR-5000 Enterprise PCB Design Software

CR-5000 Version 15 features enhanced collaboration with EMS and simplified implementation of high-speed interfaces. Other new functionality includes routing with impedance control for improved signal integrity management, and day-to-day productivity enhancements.

events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out *The PCB Design Magazine's* event calendar.

NEXTGEN AHEAD
September 9–11, 2013
Washington, D.C., USA

International Test Conference 2013
September 10–12, 2013
Anaheim, California, USA

Capital Expo & Tech Forum
September 10, 2013
Laurel, Maryland, USA

2013 MEPTEC
September 17–18, 2013
Tempe, Arizona, USA

Failure Analysis of Electronics Short Course
September 17–20, 2013
University of Maryland, Maryland, USA

Electronics Operating in Harsh Environments Workshop
September 17, 2013
Cork, Ireland

IESF 2013: Integrated Electrical Solutions Forum
September 19, 2013
Dearborn, Michigan, USA

MRO EUROPE 2013
September 24–26, 2013
London, UK

PCB West 2013
September 24–26, 2013
Santa Clara, California USA

ID WORLD Rio de Janeiro 2013
September 26–27, 2013
Rio de Janeiro, Brazil

SAE 2013 Counterfeit Parts Avoidance Symposium
September 27, 2013
Montreal, Quebec, Canada

2013 SMART Group European Conference
October 2–3, 2013
Oxfordshire, UK

RFID in High-Tech
October 2–3, 2013
Santa Clara, California, USA

Long Island SMTA Expo and Technical Forum
October 9, 2013
Islandia, New York, USA

IEEE SMC 2013
October 13–16, 2013
Manchester, UK

electronicAsia
October 13–16, 2013
Hong Kong, China

SMTA International
October 13–17, 2013
Fort Worth, Texas, USA

SMTA Harsh Environments Symposium
October 15, 2013
Fort Worth, Texas, USA

SMC 2013
October 16–17, 2013
Santa Clara, California, USA

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Next Month in *The PCB Design Magazine:*

Design for Assembly

In the rush of meeting time-to-market deadlines, it's easy for PCB designers and design engineers to overlook issues related to assembly. But processes that take place downstream can still have an effect on your job on the front end. In next month's DFA issue, our EMS contributors provide a rundown of some assembly trends—good and bad—that designers need to be aware of, and they offer valuable tips on design for assembly as well.