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AN I-CONNECT⁰⁰⁷ PUBLICATION

AUGUST 2011

Counterfeit Products: Strategies for Military Systems p.14

FOD Can Cause High-Reliability FUD p.24

Step Stencils: A Powerful Tool for Special Applications p.34

Conformal Coating: The Key to Reliability p.46

HIGH-RELIABILITY ELECTRONICS

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HIGH-RELIABILITY ELECTRONICS

Welcome to the August 2011 issue of SMT Magazine

This month we focus on the assembly of high-reliability electronics. Manufacturers of mission-critical PCBs face a plethora of challenges—technological, administrative, legislative and logistical. And your customers (and their end-users) are counting on you to navigate this maelstrom. If you're assembling high-reliability PCBs, this edition of SMT is required reading.

The war on counterfeit parts continues. In **Counterfeit Products: Strategies for Military Systems**, Sanjay Tiku of Microsoft and Michael Pecht of the CALCE Electronic Products and Systems Center offer a variety of solutions for eliminating knock-off parts from your final product. They also address the burning question: What's the most risk-free way to acquire genuine parts?

Even if you manage to keep counterfeits at bay, a single speck of dirt can lead to disaster, at test or in the field. CEO Zulki Khan of Nexlogic explains how **FOD Can Cause High-Reliability FUD**. He explains how foreign object debris (FOD), often undetected by the naked eye, can lead to a bad case of fear, uncertainty and doubt (FUD), and provides a methodology for keeping debris out of your assembly process.

In **Conformal Coating: The Key to Reliability**, Dr. Helmut Schweigart and Umut Tosun of Zestron discuss the use of these coatings on high-rel boards and the need for optimum surface cleanliness before conformal coatings are applied.

Craig Hunter of Vishay Intertechnology delves into **Thermal Simulation of SMT Components in High-Temperature Applications**. One of the most common harsh environments that PCB assemblies face is

extreme heat. Craig breaks down the influx of new components that can survive (and function effectively) at temps above 200 degrees Celsius.

Feeling fatigued? In **Reliability of the Lead-Free System: Part 1: Solder Joint Fatigue**, Dr. Jennie S. Hwang of H-Technologies Group expands her series on reliability in the age of RoHS. She discusses the causes of solder fatigue and the ways it manifests itself, and she takes a microstructural peek inside a case of solder joint fatigue.

In this month's columns:

In **Printed Electronics in the Middle**, Ray Rasmussen takes a look at the convergence taking place in the printed electronics industry. Find out what a heavy hitter like Foxconn may have planned regarding PEC, and what it means to traditional PCB makers.

Agilent's Jun Balangue gives us some pointers on **Minimizing Measurement Errors Caused by Parallel Impedance Paths**. What is G bus guarding, and how can it help you make sense of parallel impedance paths?




Ray Prasad of Ray Prasad Consultancy Group continues with his series in **Auditing PCB Assembly Capability of OEMs or EMS Companies: Asking the Right Questions, Part 2 – Manufacturing & Technology Questions**. How do you assess the true manufacturing capability of a company?

And Barry Matties, who's flown to China more times than he can count, shines a light on our relationship with our No. 1 trade partner in China...**It's Not a War, Just a Battle**. Remember—we can lose the battle and still win the war.

See you in September at IPC Midwest!

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Printed Electronics in the Middle

by Ray Rasmussen

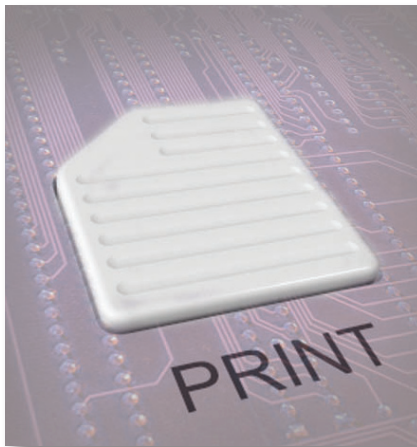
I-CONNECT007

Last month I attended the SGIA show in San Jose, (Silicon Valley). In the past, the IDtechEx shows have almost exclusively provided me with my printed electronics (PE) fix and I saw little need to add SGIA to my already long list of trade shows and conferences I attend each year. However, this year, I was intrigued when I learned that the keynote was our own Joe Fjelstad.

Although I'd heard of the SGIA in the past, they always seemed to be outside of our space, focused on graphics and printing. Well, that's starting to change.

Joe gave the audience a history lesson on printed electronics technologies, which have been around for decades. For an audience of mostly graphics folks, Joe's talk was well received and some were surprised to learn about the long-ago beginnings of this "new" technology.

The SGIA represents the graphics companies. Their members print brochures, magazines, labels, etc. SGIA stands for: Specialty Graphic Imaging Association. The title of their conference, "[Printed Electronics and Membrane Switch Symposium](#)," gives you an indication of what they think is important. Over the last decade, their members have been blind-sided by the Internet and are scrambling to find other markets for their services. SGIA members



know how to print millions of "multilayer" images on all kinds of surfaces, usually with very fine registration. At the show, they were learning about new conductive ink technologies, waterproof coverlays and more. They don't know much about electronics yet, but there seems to be a serious interest in it based on the conference and exhibition. I wouldn't say the show was bustling, but it was well attended and probably

met the expectations of the organizers and the exhibitors.

PE in the middle

There's a really interesting convergence happening. I've been writing about it for years, but the SGIA show, along with some other recent news, has illustrated to me where we are in the convergence process.

The way I see it, a show like IDtechEx looks at technologies, which move typical electronics applications into printed electronics. This is where we see traditional electronics components (like PCBs) being bypassed with PE technologies. On the other end of this convergence are the printing companies looking to integrate electronics into their offerings. Most printing companies already produce "dumb," visually pleasing (usually) products for packaging or media. Marketers are looking for ways to "smarten" up their product packages, which is the entry into

IN SUMMARY

There's an interesting convergence happening in the printed electronics industry, and the 2011 SGIA show in May, along with other recent news, illustrates where we are, and more importantly, where we're headed.

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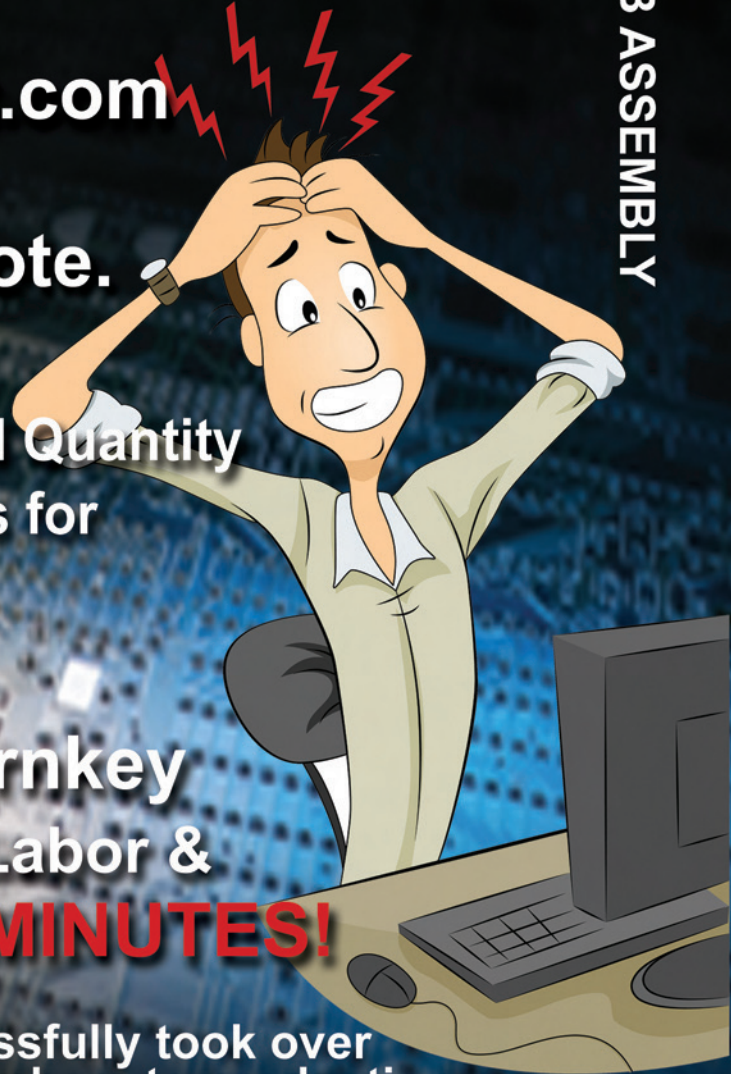
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the world of electronics for the printers. In the middle of both these efforts is where printed electronics lies.

Something happened last month, which to me was quite telling. Not much was made of it in the mainstream press and virtually no mention in the trade press. There was, however, an article that appeared in El Paso Inc. titled, "[Foxconn plans to expand: new maquila to go in next to electronics giant.](#)" The article explains Foxconn's plans to relocate most of its North American operations to its San Jeronimo, Mexico, plant that is located in the middle of a Mexican desert, south of Santa Teresa, New Mexico. This was according to Francisco Uranga, Foxconn's VP for Latin America. It seems that Foxconn believes it can gain additional efficiencies by consolidating other Mexican operations into one, huge factory in this underdeveloped, low-cost region. However, here's what really caught my attention: In this isolated area with only one company (Foxconn), guess who's setting up shop right next door? The article notes that another maquila, RR Donnelley & Sons, one of the largest printing companies in the U.S., will set up operations adjacent to Foxconn. If you Google the company news, you'll see that Donnelley recently shuttered several U.S. printing plants and raised \$600 million from the market. Interesting. There's more.

In the article, Foxconn's Uranga is quoted as saying that this new plant will be making some kind of "high-tech labeling" for Dell Computer, one of Foxconn's customers. Now, why would the largest printer in North America set up shop right next to the largest electronics contract manufacturer? It can't just be to create some high-tech labeling for Dell.

There has to be more to it than that.

In a press release issued on May 19, the story unfolds a bit more. It seems that Donnelley has taken an equity position in a PE company called [Solicore](#), which sells a host of PE products. The news release says, "In addition to this equity investment, RR Donnelley and Solicore have entered into a commercial agreement to develop the next generation of integrated power solution products. The joint development agreement will leverage RR Donnelley's proprietary imaging technologies and Solicore's patented embedded power solutions to deliver products using a combination of gravure, offset, flexographic, and digital printing processes." Here's the kicker, from Solicore CEO David B. Corey: "We believe that applying printing technology to the production of fully integrated electronic products can fundamentally change the economics of the industry."

I don't think I'm making too much of a stretch, here. The convergence I've been talking about for years is really starting to happen. Now, add in Happy Holden's comments about PE being the "number one" R&D effort at Foxconn and it all starts to make sense. Here we go! **SMT**



Ray Rasmussen is the publisher and chief editor for I-Connect007 publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuitTree Magazine*. Ray can be contacted at: ray@iconnect007.com

HansaMatrix Earns Medical Certificate ISO 13485:2003

HansaMatrix recently received Medical Certification ISO 13485:2003 which demonstrates high manufacturing quality and allows the manufacturing of medical devices and providing related services.

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Reliability of the Lead-Free System

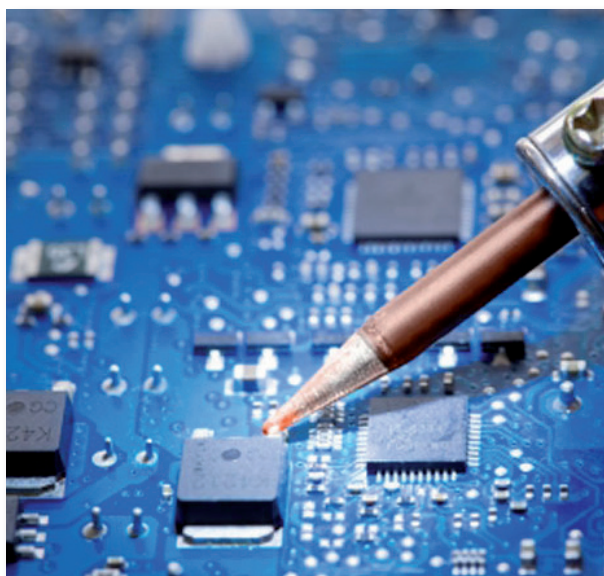
Part 1: Solder Joint Fatigue

by Dr. Jennie S. Hwang, CEO
H-TECHNOLOGIES GROUP

IN SUMMARY

Industry expert Dr. Jennie S. Hwang continues her look at the reliability of the lead-free system this month with a closer examination of solder joint fatigue. Fatigue is one of the most likely culprits for material failure—regardless of metals, polymers or ceramics.

Fatigue is one of the most likely culprits for material failure under cyclic or repeated stress conditions—regardless of metals, polymers or ceramics—due to the cumulative fatigue damage. Soft solder material, which has a low melting temperature customarily recognized as below 400°C (752°F), is particularly susceptible to fatigue.



When soft solder, tin-lead or lead-free are used as solder joints in electronic circuits, absent of any other failure causes, solder joint failure is often attributed to fatigue. In electronic applications, the solder fatigue damage may not be caused by mechanical loads, but rather by the temperature fluctuation as the result of in-circuit functions, power on-and-off and/or external environmental temperature exposure. These temperature changes inevitably generate cyclic thermal stresses in a thermal-expansion-coefficient mismatched system during the service life of electronic packages and assemblies, causing thermal fatigue (as opposed to mechanical fatigue).

Fatigue is a progressive and localized structural damage (atomic- and larger-scale

levels) which occurs when the solder joint is subject to cyclic stresses (loads and unloads). When the stress exceeds a certain threshold, microscopic cracks will begin to form. This localized damage mechanism separates fatigue from creep behavior.

As the cyclic stress continues, a crack will propagate and eventually reach a critical size, and the solder joint will fracture. Generally, the fatigue process undergoes three stages: Crack initiation, crack propagation and fracture. For solder joints functioning as the electrical, thermal and mechanical interconnections in a circuitry, a mechanical fracture is generally not a practical criterion of failure. The electrical performance, as measured by resistance increase due to cracks, is used as a failure criterion. Electrical failure often precedes mechanical fracture. When in the presence of corrosive elements, a corrosion-enhanced fatigue could also occur.

Fatigue strength, correlating to fatigue life, is defined as the stress value at which a failure occurs after a given number of cycles. The fatigue strength depends not only on the specific solder alloy material, the extreme high temperature and the extreme low

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RELIABILITY OF THE LEAD-FREE SYSTEM—PART 1: SOLDER JOINT FATIGUE *continues*

temperature, but also other factors: Surface defects, notches, holes, residual stress, voids, gas porosity and inclusions. All of these “imperfections or defects” could act as the stress concentration sites to initiate the localized damage under the fatigue environment. This is the reason why defects, such as voids or surface cracks, should not be categorically dismissed even when some test results do not reveal the performance difference between the presence and absence of such defects.

At the atomic level, the solder joint fatigue mechanism starts with dislocation movement and then forms slip bands that nucleate short cracks. Micro-structurally, grain coarsening is often a result as observed under the SEM examination. Grain size is important to fatigue—the smaller, the better. When other defects exist, such as a surface defect, a defect rules.

Comparing a SAC lead-free solder joint with a SnPb solder joint, distinct intrinsic differences in their respective metallurgy determines their dislocation systems, microstructures and metallurgical phases, which, in turn, dominate the fatigue behavior and degradation mechanism in response to various service conditions and, thus, the fatigue life.

It should be noted that stresses acting upon solder joints in real-world applications are usually random in nature rather than “regularly” cyclic as the commonly used parameters in an accelerated temperature cycling (ATC) test. One challenge is to extrapolate from cyclic test data to the behavior under actual random stresses. Based on the underlying metallurgy, this challenge escalates in an SAC lead-free system in comparison with tin-lead eutectic. (Note: The SAC is a lead-free system and the lead-free is not always necessarily an SAC.)

In practical terms, a fatigue phenomenon involves chance, randomness and probability. This is why one simple ATC test is hardly able to lead to a conclusion. And it stands to reason that the test data should be in congruence with the principles of science and needs to be checked and balanced

with the underlying scientific principles—in this case, the fundamental metallurgy and fracture mechanics. Yet that knowledge is not often exercised. (More discussion will be forthcoming in future publications of this column.)

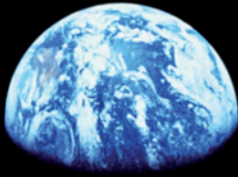
Additionally, most soft solders, even under ambient temperatures ($298 \pm 5^\circ\text{K}$), reach a homologous temperature well beyond 0.5. Therefore, creep behavior is also expected to occur, which complicates the overall degradation behavior and failure mechanism as the creep and fatigue processes operate interactively. **SMT**



Dr. Hwang, a pioneer and long-standing contributor to SMT manufacturing since its inception as well as to the lead-free development, has helped improve production yield and solved challenging reliability issues. Among her many awards and honors, she has been inducted into the WIT International Hall of Fame, elected to the National Academy of Engineering and named an R&D-Stars-to-Watch. Having held senior executive positions with Lockheed Martin Corporation, Sherwin Williams Co., SCM Corporation and IEM Corporation, she is currently CEO of H-Technologies Group providing business, technology and manufacturing solutions. She is a member of the U.S. Commerce Department's Export Council, and serves on the board of Fortune 500 NYSE companies and civic and university boards. She is the author of 300+ publications and several textbooks and an international speaker and author on trade, business, education and social issues. Contact her at (216) 577-3284; e-mail JennieHwang@aol.com.

Dr. Hwang will present two workshops, “BTC Assembly – Material, Process, Reliability” and “BGA/CSP/WLP Reliability in Packaging and Assembly,” at the SMTA International Conference, October 17, 2011, in Fort Worth, Texas.

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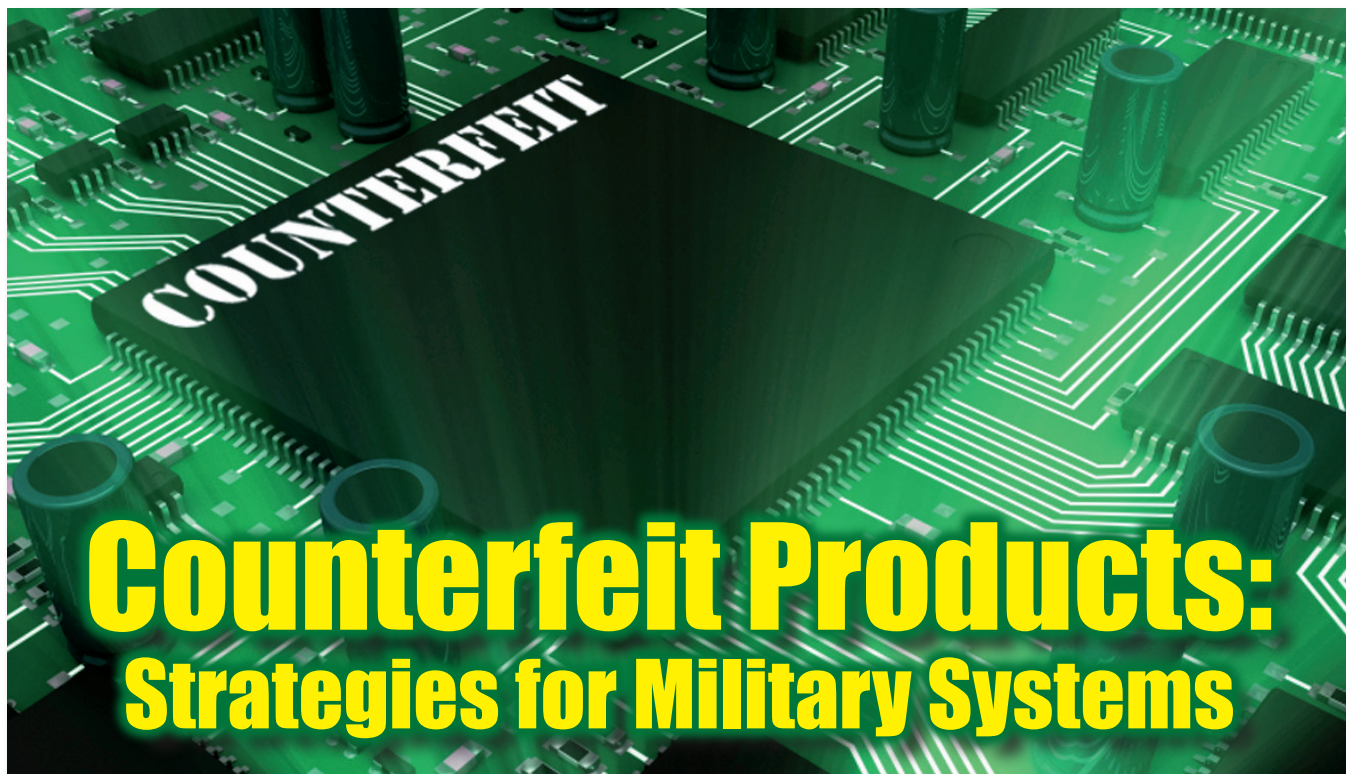
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by **Sanjay Tikku**

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CALCE ELECTRONIC PRODUCTS AND SYSTEMS CENTER

IN SUMMARY

An electronic component that may be worth only \$2 can cost as much as \$20 to replace if it is detected to be counterfeit after it is mounted onto a PCB. Failures of systems that use counterfeit electronics can cause loss of mission, significant maintenance and logistics costs and safety problems—leading to injuries and potentially loss of life.

Counterfeit products, also called knock-offs, bogus or imitation products, are products whose identity has been deliberately misrepresented and are offered for sale as if they were authentic. Counterfeit goods mean any goods, including packaging, bearing

without authorization a trademark which is identical to the trademark validly registered in respect of such goods, or which cannot be distinguished in its essential aspects from such a trademark, and which thereby infringes the rights of the owner of the trademark in question under the law of the country (of importation) [1]. Counterfeiting is an infringement of the legal rights of the owner of intellectual property [2].

According to the Organization of Economic Co-operation and Development (OECD), the estimate of the total value of counterfeit and pirated products in 2008 was between US \$450-650 billion, which is estimated to grow up to US \$1.2-1.7 trillion by 2015 [3]. OECD found that the magnitude and scope of counterfeiting activities is larger than the national GDPs of 150 economies and affects nearly all product sectors, from luxury items to items that have an impact on personal health and safety. These figures only take into account the revenue that counterfeiters siphon off from manufacturers; it does not include safety-related costs, which repair and maintain systems using the counterfeit products, or liability costs.

Electronics parts and assemblies are also prone to counterfeiting due to luring monetary benefits facilitated by the complex nature of the supply chain that makes introduction easier and detection difficult. Besides loss of revenue for the manufacturers, the economic repercussions of unwanted counterfeit electronics products reach far beyond the cost of merely replacing the counterfeit. For example, an electronic component that may be worth only \$2 can cost as much as \$20 to replace if it is detected to be counterfeit after it is mounted onto a circuit board [4]. Also, failures of systems that use counterfeit electronics can cause loss of mission, significant maintenance and logistics costs and safety problems—leading to injuries and potentially loss of life.

Benign and Harmful Counterfeit Products

There are many reasons why people indulge in, produce and sell counterfeit products, but the primary reason is to make money. Most often, items having ready demand, mass market appeal and large margins like bags, watches, clothing, cell phones and pharmaceuticals are targeted. Sometimes people buy counterfeit products knowingly. In some cases, such as music, they don't even buy the product, they just copy it themselves. Some people like the "real" product or the brand name, but believe that they are overpriced or beyond the price they can afford. So they are willing to purchase a "similar" product at a significantly reduced price, which is usually counterfeit. This type of counterfeiting is culturally accepted in certain places, or at least openly tolerated.

For example, Canal Street in New York City and an area across the street from the Rosslyn Metro in Washington, D.C., are two well-known places to obtain counterfeit handbags and accessories. It is anybody's guess whether

the reason for acceptability for such markets is lack of government resources, lack of a comprehensive plan of action, lack of interest or some combination of reasons.

To fight the purchase of "wanted counterfeit products," companies typically rely on brand protection methodologies through intellectual property (IP) laws and enforcement. However, this is not a major disincentive for criminals. This is also not a deterrent for cultures that don't really understand or agree with such laws. For example, U.S. teenagers may think that music should be free and the Chinese under communism believed that people should not own IP.

In some cases, the purchase of a counterfeit product is made unknowingly and deception is involved. This is often the case with electronic components (as opposed to final consumer products), which do not have mass market appeal. For electronic systems with long service life, like military systems

such as airplanes, the main risk arises due to unavailability of obsolete or out-of-production parts. There have been several reports of counterfeit electronic components turning up in military weapons, airplane flight management systems and cars.

There have been several reports of counterfeit electronic components turning up in military weapons, airplane flight management systems and cars.

For example, it was recently reported that substandard parts had ended up in global positioning system (GPS) oscillators used for navigation on more than 4,000 U.S. Air Force and Navy systems [5]. Some other examples of counterfeit parts from past safety and mission critical systems have been presented in the IEEE Spectrum article "Bogus: Electronic Manufacturing and Consumers Confront a Rising Tide of Counterfeit Electronics" [6].

Risks for Military Systems

In the last two decades, civil and military systems have gotten increasingly networked in

**COUNTERFEIT PRODUCTS: STRATEGIES FOR MILITARY SYSTEMS** *continues*

the United States. This network is threatened not only by conventional disruption threats, but also by counterfeit parts. Introduction of counterfeit parts channeled through a legitimate or partially illegitimate supply into assemblies that comprise electronic equipment and systems can cause mission disruptions. Because of the complexity of today's electronic parts supply chains and reliance on supply chains outside the U.S., the potential for counterfeit parts being introduced cannot be overlooked. The breakdown of procurement quality assurance and supplier vetting by customers has further improved the odds for counterfeiters to slip their parts into this complex supply chain.

Apart from the possibility of counterfeit parts being responsible for failure during the operation of mission critical electronic assemblies, a deliberate revelation of any such supply after the parts have been assembled can be used to trigger a grounding of a number of suspect assemblies and a wave of warranted and unwarranted recalls. This can result in widespread disruption in functioning of a large variety of diverse security-related systems, where the parts may have been used, even though no system would have failed functionally.

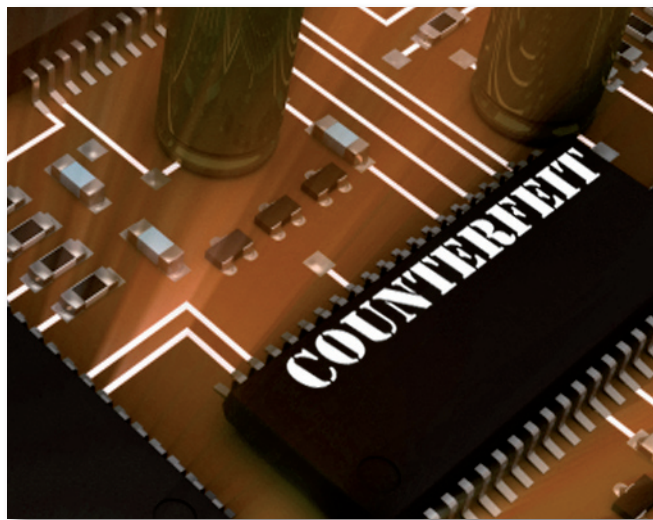
The counterfeit parts problem is made worse due to the low probability of detection. More often than not, the company or agency which finally purchases a counterfeit part (which may be contractual agencies for the

government or the military) is not even aware that it has done so. This is because the fraud has been perpetrated several steps earlier in the supply chain. Since most of these government or military contractors do not determine the origins of parts, the possibility for counterfeit parts being included in electronic products and systems increases. Reduction in the focus of parts selection and management through stringent component, distributor and supplier qualifications has facilitated this as well. Moreover, counterfeit parts are not easy to detect because those who manufacture and distribute them go to great lengths to duplicate materials, part numbers and serial numbers to coincide with the authentic parts.

The different levels of sophistication in part defectiveness that can be used to introduce disruptive electronics into military systems include parts with defects and so-called "Trojan horse" parts. Parts with defects include counterfeit parts from an entirely different manufacturer than the original manufacturer, scrapped parts of original manufacturers introduced into the supply chain through back channels and failed parts recirculated for use. A Trojan horse part is a distant possibility because such items require technical expertise and sophistication of design. A typical example is for a part to cause faulty information to be transmitted; e.g., initiate faulty GPS or altimeter readings in aircrafts affecting operational decisions.

Causes and Potential Solutions

The most risk-free way to purchase a non-counterfeit product is to buy directly from the manufacturer, the manufacturer's authorized distributor or an authorized after-market distributor. If we want a real Gucci bag we go to the Gucci store. If we want a counterfeit product, we go to Canal Street in New York City. The same principle holds true for electronics components. If you go anywhere but to the manufacturer or an authorized distributor, you are looking for trouble. And even if you find a real product from some third party, you cannot be confident that the product wasn't previously scrapped and refurbished.



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**COUNTERFEIT PRODUCTS: STRATEGIES FOR MILITARY SYSTEMS** *continues*

Even if you buy a product directly from the manufacturer or the manufacturer's authorized distributor, this doesn't completely ensure that the product is defect-free. This is because the product you buy can be considered a system, made up of various components and processes often from a large number of suppliers. Examples of a manufacturer selling a defective product due to inadvertent inclusion of counterfeit materials includes the supplier that introduced lead into the Mattel toys, or the supplier that added improper grapes to a certain French wine. Fortunately, the manufacturer directly feels the repercussions of this deception and corrects the problems. However, proactive monitoring of material quality and sources by higher-order supply chain members can prevent a costly reactive response.

So one may ask if it is so simple to buy the "real products," why do counterfeits enter into so many high-technology systems such as military systems? Counterfeit parts get into military systems because the military systems need components that are most often obsolete, thus creating distress buying and a high profit margin product; not because there are so many customers, but because there is no alternative. The parts may be made outside the U.S. (e.g., China); but they are essentially requested by a broker in the U.S., who in turn was solicited by some defense contractor because the parts they wanted were obsolete. The activity is rarely, if ever, a deliberate attempt to infiltrate the U.S. military with counterfeit parts, but simply a response to a business opportunity when the buyer is desperate enough to be much less careful while buying these parts.

Counterfeiters have not been known to make electronic components for U.S. military systems in advance, because there is normally no market. Instead, middlemen directly or indirectly "consign" people to make these

products. The middleman may actually know that the products he consigns out will not be legitimate, but pleads ignorance. The actual "makers" of the counterfeit parts are looking at any way possible to make some money. This leads to the various ways (e.g., changing labels, repackaging, refurbishing scrap) in which counterfeit products have been known to become incorporated into military and avionics systems. Thus, unlike the consumer product counterfeiter, the "military" counterfeiter only makes his counterfeits when "asked" by the middleman.

Planning for life cycle availability of electronic parts, along with planning for appropriate design refresh with parts from their active procurement life, can mitigate this situation significantly. The goal is to not get

into a situation where you are desperate for a part that is no longer available. You have to make sure that you have adequate supplies of parts and second sources. This, however, is made difficult by the fact that product lifecycles are difficult to predict accurately, and we have examples

like the B-52s, for which the lifecycles have prolonged way beyond what was intended at original design [7].

Current U.S. Government and Military Policies

A number of treaties and legislations have been enacted internationally and in the U.S., respectively, to penalize counterfeit activities and other intellectual property violations. However, legislative action has not proven effective because of the huge profit incentive for illegitimate businesses, and the legal difficulties in affixing counterfeiting charges on the primary perpetrators in the global supply chain as and when such events are detected.

Besides legislative actions, several private and public organized activities have also

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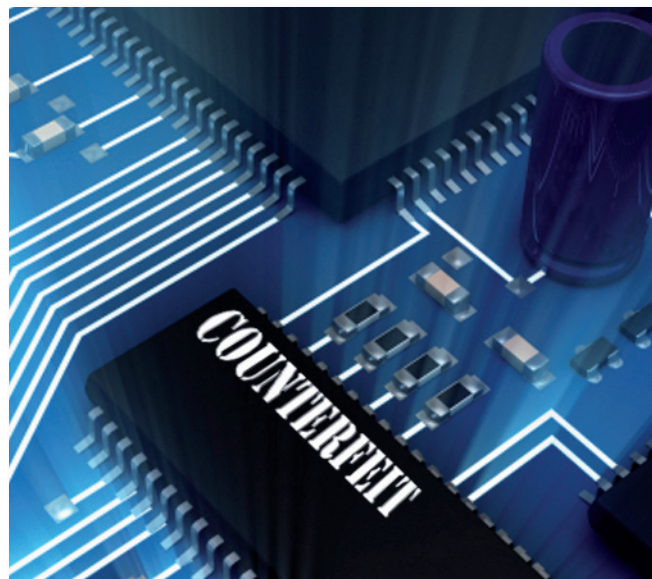
**COUNTERFEIT PRODUCTS: STRATEGIES FOR MILITARY SYSTEMS** *continues*

taken notice and created information-sharing tools to help the industry avoid the use of counterfeit parts. The International Anti-Counterfeiting Coalition (IACC) is a non-profit trade association devoted to combating product counterfeiting and piracy. In the U.S., the Department of Defense's Diminishing Manufacturing Sources and Material Shortages (DMSMS) database described in GIDEP, the Department of Energy (DOE) Lessons Learned Program, the Lockheed Martin Idaho Technologies Company (LMITCO), the Defense Industrial Supply Center (DISC), the Naval Supply Systems Command (NAVSUP) and the Electronic Resellers Association International (ERAI) are all involved with this activity. However, these are mostly post-facto counterfeit part reporting agencies that do not do preemptive prevention and avoidance.

For example, the U.S. Army's Brilliant Anti-Armor Submunition (BAT) program experienced numerous failures of Cypress SRAMs, and failure analysis revealed a number of anomalies including memory, timing and parametric failures. Raytheon, which built the circuit card assemblies for the BAT program had apparently purchased the parts. Cypress was apparently aware of such counterfeit problems as far back as January of 1999, but the problem was announced through GIDEP in May 2002.

Knowledge concerning counterfeit products is not well shared amongst the government agencies and industry organizations in the U.S. In fact, even the various law enforcement agencies do not appropriately share data. Most of the issues are caught not by the government, but by contractors who have varying policies on information sharing and often don't want to acknowledge that they are purchasing from poor sources.

Another government program, called the Trusted Foundry Program, was initiated in 2004 to ensure that mission-critical national defense systems have access to leading-edge integrated circuits from secure, domestic sources. This is a very limited solution with a large number of significant drawbacks. First, the most state-of-the-art electronics are no longer made in the U.S. For example,



the best memory devices today are made by Korean companies. There is no way that a U.S. foundry can compete with them on performance, quality and reliability. For affordable, leading-edge technologies, the U.S. military should purchase products from such sources. The Trusted Foundry Program cannot be competitive in price (design, die, package or test), does not have enough volume to enable best practices and state-of-the-art development and lags behind the state of the art. It is neither affordable nor leading edge.

The inability (or unwillingness) of the DoD to act "strategically" when managing electronic systems that depend on the commercial supply chain is costing large amounts of money and putting system sustainment and security at risk. This is reflected in how the DoD manages systems directly and how they manage subcontractors who design, build and sustain those systems. Performance based logistics (PBL) and similar outcome-based contracting approaches are the right idea in theory. However, they force the DoD subcontractors to take responsibility for the entire life cycle of a system and thereby think and manage electronic parts strategically for the good of everyone. Nevertheless, today's PBL contracts are in many cases too short (only five to seven years), or they specifically exclude the difficult key supply chain management activities, e.g., obsolescence management.

The Art of Fume Extraction



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The part of the DoD (the Defense Logistics Agency) that does worry about key part procurement issues, such as counterfeit parts and obsolete parts, is primarily “piece-part” centric. While piece-part management has unquestionable value, lots of DoD systems are not managed at the piece-part level. All the part-level supply chain problems exist or are moving to the COTS (commercial off-the-shelf) assembly level; e.g., counterfeit batteries for laptops. The government must expand its thinking to COTS assemblies and software. Hardware and software represent a “co-sustainment” problem—ultimately they have to be managed together.

Summary and Conclusions

The increasing use of electronics in all key areas of national security infrastructure and the sophistication of counterfeiters makes the introduction of electronic parts into the supply chain a distinct possibility. High profits, low risk of detection and weak prosecution further contribute to the supply of counterfeit products. Counterfeiting of electronic parts causes potential hazards, including safety and loss of profits to companies, as well as maligning the reputation of manufacturers and distributors. A number of laws have been enacted in the U.S. to penalize counterfeit activities and other IP violations. Several private and public organized groups have also taken notice and created technological and information-sharing tools to help the industry detect and avoid the use of counterfeit parts. But these measures do not solve the cause of the problem. There are also some new documents to address counterfeit products, such as SAE AS5553, “Counterfeit Electronic Parts; Avoidance, Detection, Mitigation and Disposition.” However, this is only a high-level guide that will have little effect on the current problems.

To combat counterfeit products, it will be necessary to get at the heart of the reasons that counterfeit products are procured. Factors that contribute to the targeting of electronic products include: Obsolescence; lead time (manufacturer or an authorized distributor unable to supply products within the lead time requirement of customer); price issues (parts available at lower prices from independent distributors and brokers); absence of due diligence and verification tools in the electronics part supply chain; availability of inexpensive means to create counterfeits; and the high cost of procedures to detect incoming counterfeit parts. Recently, CALCE has uncovered counterfeit products that appear to be the result of shortages in the supply chain due to the earthquake followed by a tsunami in Japan. This is affecting a range of components, including capacitors.

To reduce the reliance of military electronic equipment on less reliable sources for part replacements, creating obsolescence mitigation and avoidance solutions during the design of the equipment can address the problem to some extent for the military.

However, considering the dynamic nature of technology updates and the ever-changing landscape of the supply chain marketplace, this approach cannot be a do-all and end-all to solve the problem.

Although electronic manufacturing business is growing in East Asia, the regulatory controls, business ethics and long-term corporate checks on product integrity are not yet mature there. In this evolutionary business environment, chances for foul play through external intervention remains a high possibility. The solution is not to have a total exclusion of electronics parts manufactured outside the U.S., but to create a controlled flow of verified and verifiable electronic technologies and parts through a symbiotic

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Although electronic manufacturing business is growing in East Asia, the regulatory controls, business ethics and long-term corporate checks on product integrity are not yet mature there.

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partnership. The U.S. has to integrate the developing countries into the mainstream of international trade and commerce. Business, corporate laws and business ethics in these nations must be brought on par with international requirements. Confidence needs to be generated that a part bought from authorized indigenous manufacturing facilities in these countries is as good as a part bought from anywhere in the U.S. or Western Europe. This can also help solve obsolescence issues since a number of small electronics industries in these developing countries would be willing to manufacture obsolete parts.

At the time of this writing, Senator John McCain and others were trying to investigate counterfeiting in Shenzhen, China, under the pretense that they will undercover counterfeits that could get into U.S. government and military systems. It will be very difficult for them to find these counterfeiters in China. It may be much easier to find counterfeit Gucci bags and Rolex watches just down the road from the Senate in Washington, D.C. Where Senator McCain needs to focus his attention is on the military contractors that are "consigning" middlemen to find parts they all know may be counterfeit. These contractors and middlemen are equally culpable as the counterfeiters (whether in China or elsewhere) who make these parts. **SMT**

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Sanjay Tiku has a MS and Ph.D. degree in Mechanical Engineering from the University of Maryland, College Park. He currently works for Microsoft Corporation and leads a team of engineers and researchers who use advanced computer-aided design analysis tools, experimental techniques and other numerical and statistical methods to ensure reliability and drive qualification of complex electromechanical products at Microsoft. He is a member of the IEEE, and an invited member of academic honor society Phi Kappa Phi.



Professor Michael Pecht has an MS in Electrical Engineering and an MS and Ph.D. in Engineering Mechanics from the University of Wisconsin at Madison. He is a Professional Engineer, an IEEE Fellow, an ASME Fellow, an SAE Fellow and an IMAPS Fellow. He is the founder of Center for Advanced Life Cycle Engineering (CALCE) at the University of Maryland, which is funded by over 150 of the world's leading electronics companies. He is also a Chair Professor in Mechanical Engineering and a Professor in Applied Mathematics at the University of Maryland.

FOD CAN CAUSE HIGH-RELIABILITY FUD

by **Zulki Khan**, *President and Founder*,
NEXLOGIC TECHNOLOGIES INC.

IN SUMMARY

Unless foreign object debris-free PCB assembly is rigorously practiced, the military/aerospace, high-reliability OEM is inviting fear, uncertainty and doubt (FUD). The mil/aero OEM or contractor must cast a wary eye on the assembly floor to catch the most innocent-looking to the most blatant FOD violations.

Yet another acronym is rapidly making its way to the PCB assembly floor: FOD, or foreign object debris (sometimes called foreign object damage). FOD is closely associated with aviation runway accidents given recent, widely-publicized events. However, FOD has far-ranging effects down to the PCB level.

It doesn't take a rocket scientist to figure out that FOD can have devastating effects on a PCB project. That's because board real estate has shrunk dramatically. Components

are so small, such as the micro BGA and CSP devices shown in Figure 1, that many of them can barely be seen with the naked eye. The tiniest amount of debris on the assembly floor can find its way into your PCB, hide in a tiny crevice on the board and have an adverse effect on PCB reliability and especially high-reliability products.

High-reliability devices are highly sophisticated and particularly FOD-susceptible. Sometimes a speck of dirt can cause an issue. At worst, it can cause a system or end equipment to not perform at an optimal level; at the least, it can consume inordinate time

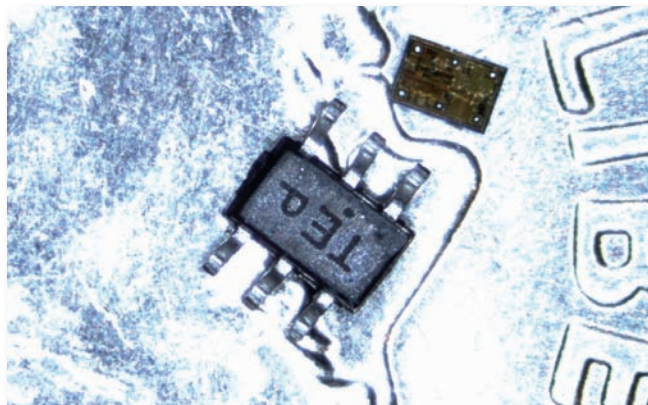


Figure 1: FOD can have especially adverse effects on advanced packaging like microCSPs.

to debug and uncover the root cause. And, somewhere in between, while FOD may not immediately cause damage, it could pose a latent issue constantly degrading performance and causing economical damage.

FOD encompasses a myriad of damaging objects at varying manufacturing levels, from the PCB to the system level and on to field-use of those systems. The debris runs a wide spectrum from tiny bits of dirt on to non-ferrous substances, electromagnetic radiation and on to many larger objects like pieces of pavement or other damaging objects on a runway. This wide scope of FOD is increasingly drawing the attention of mil/aero OEMs and contractors. They are demanding contract manufacturers (CMs) and EMS providers to pay even closer attention to FOD, as well as have their personnel properly trained and certified and apply well-disciplined measures on the assembly floor to eliminate FOD problems.

FOD on the Assembly Floor

The mil/aero OEM or contractor must cast a wary eye on the assembly floor to catch the most innocent-looking to the most blatant FOD violations. The worst-case scenario that violates all FOD-free assembly rules is a cluttered work area with extraneous items not related to a given mil/aero PCB project.

But there can also be literally hundreds of pieces of debris, carelessly or inadvertently placed items, and an array of objects that violate FOD rules, regulations and guidelines. A majority of FOD is virtually invisible to the human naked eye, therefore careful and disciplined practices must be applied, constantly practiced and adhered to vigorously on the assembly floor to minimize or eliminate FOD.

In particular, due to intense manufacturing steps, there can be pieces of metal or wire clippings, displaced solder balls, FR-4 material residue, residue from various manufacturing processes, pieces of solder wire, fluxes, as well as by-products of the manufacturing process, also known as solder dross. This is caused by oxidation of alloys such as tin, lead, zinc or aluminum, while the board goes through wave soldering, as shown in Figure 2. At the extreme, FOD can be insects, dead or alive, such as

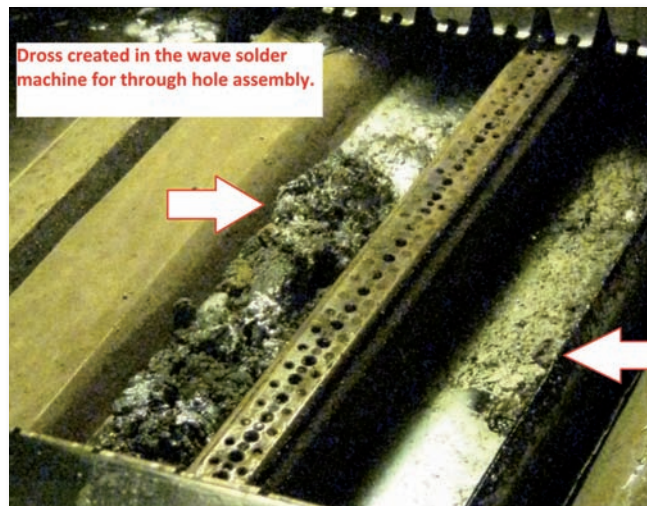


Figure 2: Solder dross or by-products of the manufacturing process is another source of FOD.

flies, that accidentally get into manufacturing areas. Or, during inclement weather, specks of mud or water on shoes can be inadvertently introduced into manufacturing.

As mentioned above, components and boards have shrunk so much that it is difficult to monitor FOD on the manufacturing floor unless you have proven and well-disciplined measures to guard against it. An example is FR-4 residue, which may contain glass debris and dust, as shown in Figure 3. This debris or dust can stay underneath a 0.3-millimeter (mm) pitch micro CSP when that board is scored, while de-panelizing it from a bigger panel. The savvy CM or EMS provider knows ahead of time this might occur and executes the proper methodologies and strategies to eliminate that problem.

FOD on the assembly floor also encompasses unneeded tools that are not related to the project at hand. These can be wrenches, torque meters, screwdrivers—unwanted objects which are in the vicinity of a particular project or in its migration path from one department to another. Consumable items like cotton swabs, washers, brushes, tie-ups, industrial wipes and others are a third category of FOD on the assembly floor.

FOD Champion, Guidelines and Programs

CMs and EMS providers seriously abiding

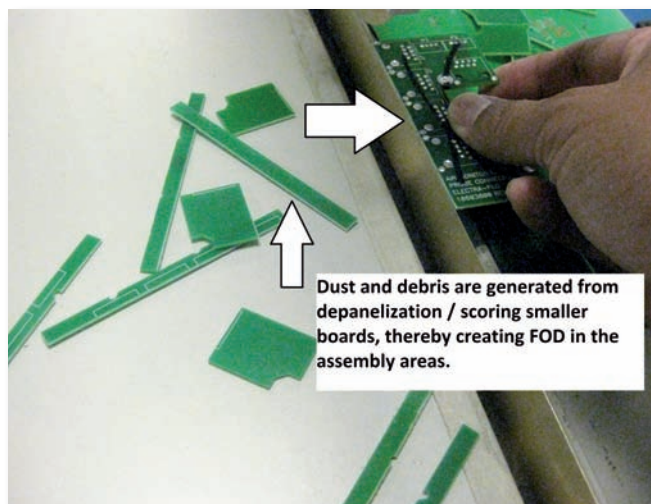


Figure 3: FR-4 residue can be in the form of dust or debris and is another form of FOD.

by FOD prevention rules and regulations have a so-called FOD Champion on the assembly floor to assure PCB projects are FOD-free. In effect, he or she is an internal auditor who daily visits critical FOD-free assembly areas and has the authority to correct or improve any related shortcomings.

Also, there are several FOD prevention programs the mil/aero OEM and contractor should become familiar with to acquire assurances their CMs or EMS providers are following the right paths toward FOD-free PCB projects. Those are FOD General Guidelines, Awareness, Control, Training and Elimination. The guidelines are not part of a specific standard like AS9100, but are more related to plain, old-fashioned cleanliness or general housekeeping. The rule of thumb is a “clean as you go” process. This includes:

- Keeping the immediate area clean when work cannot continue.
- Cleaning the immediate area when work debris has the possibility of migrating in or out of the site or inaccessible area.
- Cleaning the immediate work area after the work is completed, but prior to inspection.
- Cleaning before extended period breaks like meetings or lunch.
- If an object from the work site is dropped, it should be picked up immediately.

FOD Awareness involves several aspects. One is to store non-critical equipment required for use on a particular project in an FOD Awareness area. This selected equipment can be calibration, test or lab gear, which is normally not in the immediate work area, but readily accessible for use on the given PCB project. This also applies to the test area where PCB projects are packaged, tested and shipped. Here, associated tools, materials and supplies are kept separate to avoid inadvertent movement into the FOD control and sensitive area. Guarding individual work areas is critical to protect against FOD, especially when an operator is not present.

Not wearing jewelry or loose objects at FOD prevention assembly sites is another aspect of FOD Awareness. The precaution here is that these items can accidentally fall and damage the product, like causing a short between different IC pins. The only exception to the rule is medical ID bracelets or wedding rings, which are too tight to remove. In cases like these, a too-tight ring on a finger must be taped with approved tape.

The FOD Control area has the highest levels of emphasis and ensures that such PCBs associated with flight or mission control equipment are securely controlled against any FOD risk. This includes securely sealing any PCB or associated part to avoid any contamination. Here, the FOD Champion makes sure an increased level of control is maintained to ensure export hardware and mission control equipment are protected from FOD at all times.

The kinds of things prohibited in a FOD Control area with a placard displayed in the controlled area (Figure 4) includes drinks, food, gum, tobacco, lead pencils, two-piece ink pens, jewelry, staples and staplers, unsealed or damaged card board, particle or debris like Styrofoam, pins attached to badges or coats and a long list of other similar items.

There's also a tool control plan as part of the FOD Control area. This procedure is defined for generating the specific assembly and manufacturing for a given PCB job that is to be completed in a FOD-free area. An example of a FOD-free manufacturing



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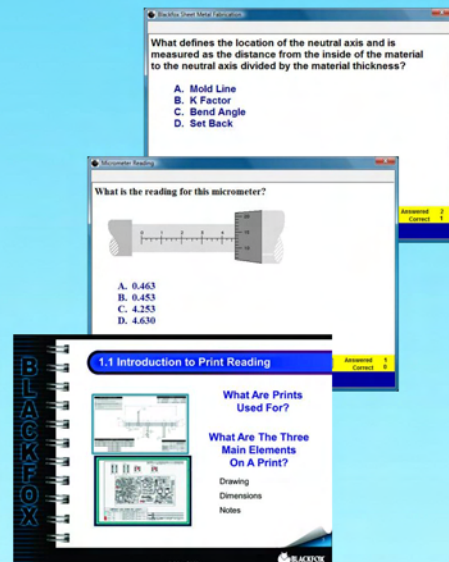
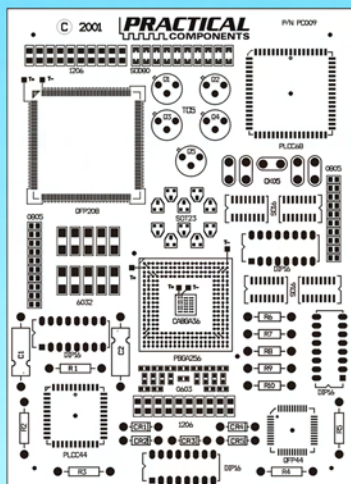
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**FOD
CONTROL
AREA**

Figure 4: Placard warns employees to keep the area free of objects that aren't associated with the current project.

technician's bench is shown in Figure 5. It also calls for cleaning all support equipment like tools, soldering irons and others when a task is completed and no later than the end of a shift. Again, here like in most FOD-free instances, the basic principle to follow is good housekeeping practices. These procedures prevent any and every type of contamination or possibility of migrating, entrapping, damaging or failing a PCB project.

Tool Control is yet another aspect of FOD Control area, not to be confused with the tool control plan. The procedure requires that all tools used for the assembly and production of a FOD-free PCB project cannot be moved in or out of the immediate work area without proper

supervision. Tools used on a given PCB project must be inspected and calibrated as required by the CM or EMS provider. Personnel are not allowed to bring in their own hand tools for the job without a manager or supervisor's approval. The FOD Champion plays a vital role here by authorizing any exceptions.

As far as FOD Control training, it is critical that assembly floor personnel have IPC610 training at the bare minimum. However, training in both J-STD-001E and J-STD-001ES is critical for maintaining a FOD-free assembly floor. The "E" version supports military gear, while the "ES" targets space application control. Each standard requires formal training in some cases 8:00 a.m. to 5:00 p.m. daily classes for a week and sometimes two weeks. The 40-hour training involves classroom discussion, but the majority goes to on-the-job assembly floor work where technicians solder, de-solder or rework components, as well as other related tasks to get acquainted and well-versed in these standards.

Lastly, foreign object elimination (FOE) identifies organizational and procedure responsibility. It applies not only to all employees of a CM or EMS provider company, but also to subcontractors, vendors and visitors who are around FOD-free manufacturing areas. That includes assembly, installation, testing, operation, modification, storage and delivery process areas. More specific to PCB assembly and manufacturing, FOE regulates the disposal of such consumable supplies as cotton swabs, industrial wipes, tie-ups and assorted items regularly used as part of a given PCB project—all of which should be immediately disposed of to keep a FOD-free workplace.

Audit

Auditors can come to a CM's or EMS provider's location from a variety of agencies, depending on the PCB project being either designed or manufactured. Audit inspections can come from JPL, NASA, contractors or from an independent audit party called Defense Contractor Management Association (DCMA).

Auditors are quick to inspect a technician's bench to make sure that he or she has the proper documents, is following the right



Figure 5: FOD-free technician workbench.

Video Interview

Reliability Testing for Long Life Cycles

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Reliability expert Vicka White, principal engineer at Honeywell Air Transport Systems, is Chair of the IPC D-30 Rigid Printed Board Committee and Vice Chair of the IPC Terms and Definitions Committee. She explains how Honeywell conducts reliability testing on PCBs that must survive 20 years in the field and how reliability needs will likely influence IPC's requirements.



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procedures, is trained and correctly certified and their workstations are free of everything but the items and tools related to a particular job. For example, if the technician is using a solder wire for a lead-free project, auditors want to ensure that he or she has the flux and solder required for that project and nothing else. Auditors want to ensure non-related objects do not mix with those things that are project-specific.

Also, as part of an in-depth audit, inspection personnel have the right to remove non-related materials and objects from a technician's workstation, tag them, bag them and ship those non-relevant items to the OEM or contractor customer. Those items can be multiple soldering tips, device removal tools, cleaning supplies and other such objects. However, when the project is completed, they can be shipped back to the CM or EMS provider. This means during the course of a particular build, a designated assembly workstation(s) must be FOD-free, with the removal of all extraneous materials and objects.

Lastly, auditors are authorized to come into

a CM's or EMS provider's manufacturing site at any time without advance notice. This gives them the latitude and freedom to conduct a detailed audit on the spot to assure that FOD is being prevented during the build of a project. It also gives auditors the proof that all procedures and processes are in place and FOD is seriously regarded. **SMT**



Zulki Khan is the Founder and President of NexLogic Technologies, Inc., in San Jose, California, an ISO 9001:2008 Certified Company, ISO 13485 certified for manufacturing medical devices and a RoHS compliant EMS provider. Prior to NexLogic, Khan was General Manager for Imagineering, Inc., in Schaumburg, Illinois. He has also worked on high-speed PCB designs with signal integrity analysis. He holds a B.S. in EE from NED University in Karachi, Pakistan, and an M.B.A. from the University of Iowa. He is a frequent author of contributed articles to EMS industry publications.

Minimizing Measurement Errors Caused by Parallel Impedance Paths

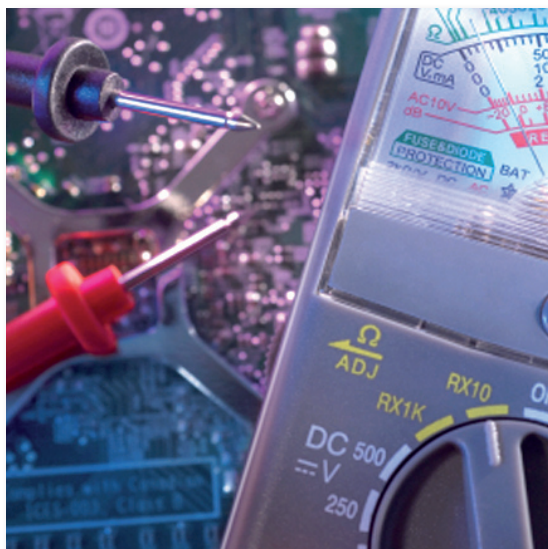
by Jun Balangue

AGILENT TECHNOLOGIES

How can we minimize measurement errors caused by parallel impedance paths with analog measurement using G Bus guarding?

Measurement on a single device—such as a resistor, capacitor or inductor, etc.—will result in an accurate measurement even if you are just using a simple multimeter. However, measurement on a device on a PCB assembly (PCBA) along with other devices presents an entirely different scenario as the device may be subject to one or more parallel impedance paths.

These parallel impedance paths cause measurement errors by providing current



paths around the device under test (DUT). For instance, Z_{sg} and Z_{ig} , in Figure 1, represent parallel impedance paths around the DUT, which is R_x . Using an in-circuit test (ICT) system, when such parallel paths are formed, a parallel current (I_p) flows around R_x and through the measurement operational amplifier (MOA) feedback path. The added current through the feedback paths cause R_x to appear as smaller

impedance than it actually is.

The analog stimulus/response unit (ASRU) of an ICT system has a G Bus that can be used as a guard by breaking the parallel impedance path. Figure 2 shows the scenario where the

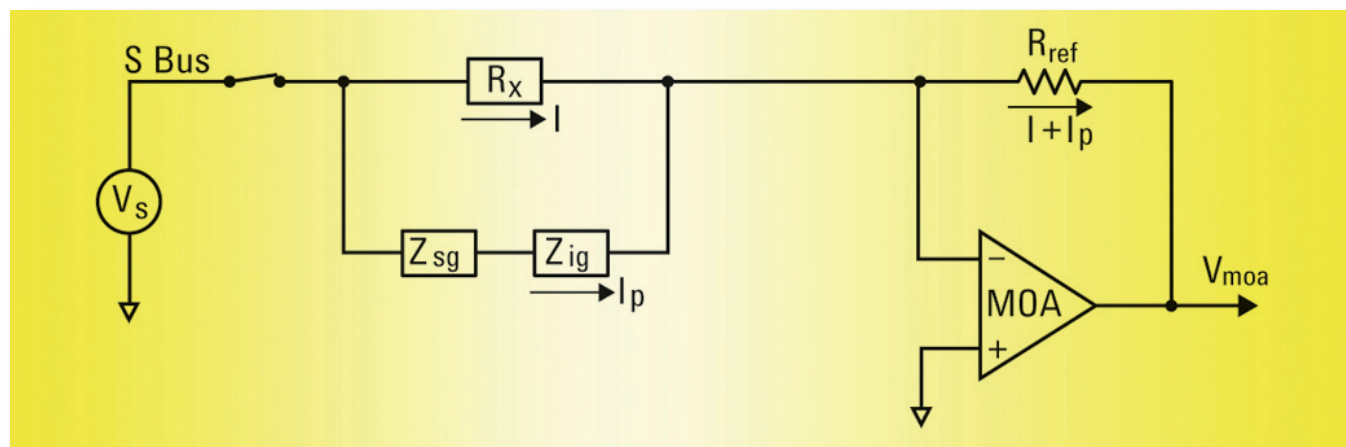


Figure 1: Parallel resistance paths cause measurement errors.

IN SUMMARY

Author Jun Balangue takes a look at ways to reduce measurement errors on a PCBA caused by parallel impedance paths using G Bus guarding.



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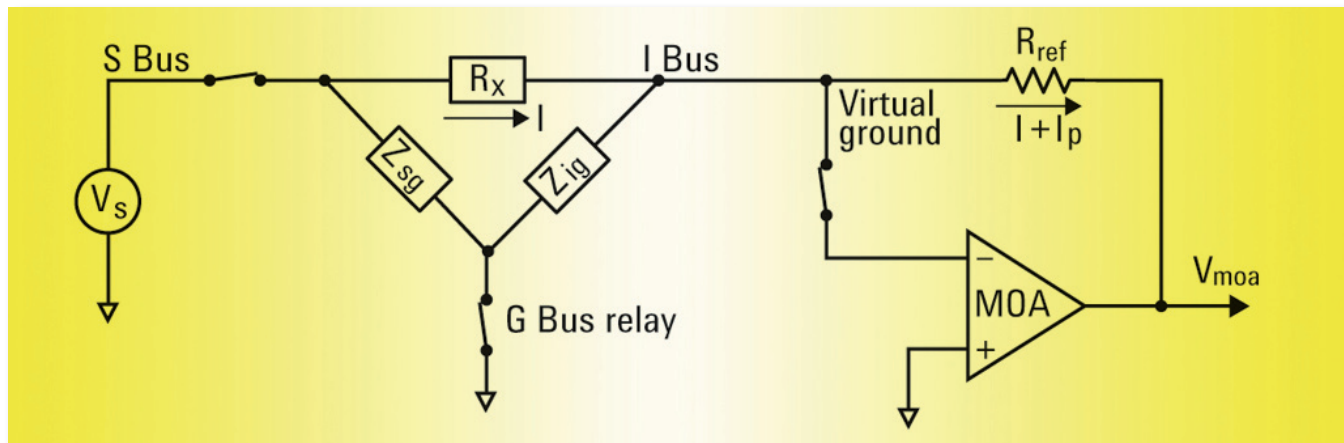


Figure 2: The G Bus breaks parallel resistance paths.

G Bus is connected in the circuit when the DUT has a parallel impedance path. By connecting the G Bus as shown in Figure 2, the current that would flow through both Z_{sg} and Z_{ig} becomes insignificant. Also, when the non-inverting input (positive pin) to the MOA is grounded as shown in Figure 2, the inverting input (negative pin) becomes a virtual ground due to characteristics of the measuring operational amplifier (MOA).

This also places the I bus connection at virtual ground. With the G Bus also at ground potential, there will be no difference of potential existing across Z_{ig} , and no current flows through the parallel path around R_x and through the MOA feedback path. V_s does, however, supply current to Z_{sg} . This current

does not affect the measurement as long as the V_s output impedance is very low compared to Z_{sg} . If there is more than one parallel path around the DUT, multiple G Bus connections are possible. **SMT**



Jun Balangue is a Technical Marketing Engineer at Agilent Technologies. He holds a Bachelor of Science in Electronics and Communication Engineering and has 19 years of industry experience ranging from semiconductor manufacturing to PCB manufacturing. Balangue has been with Agilent for the last 10 years.

SMTA to Feature Lead-Free Soldering Tech Symposium

The SMTA announced that the renamed Lead-Free Soldering Technology Symposium will be held on October 20, 2011 as a focused symposium at SMTA International in Ft. Worth, Texas. The scope of this year's symposium is the reliability of interconnections, particularly those studied in the second phase of the NASA-DoD Pb-Free Consortium project. The project is providing unprecedented data on the long-term performance of lead-free interconnections addressing alternative surface finishes, as well as the performance of mixed SnPb/Pb-free solder joints and the effects of rework activities.

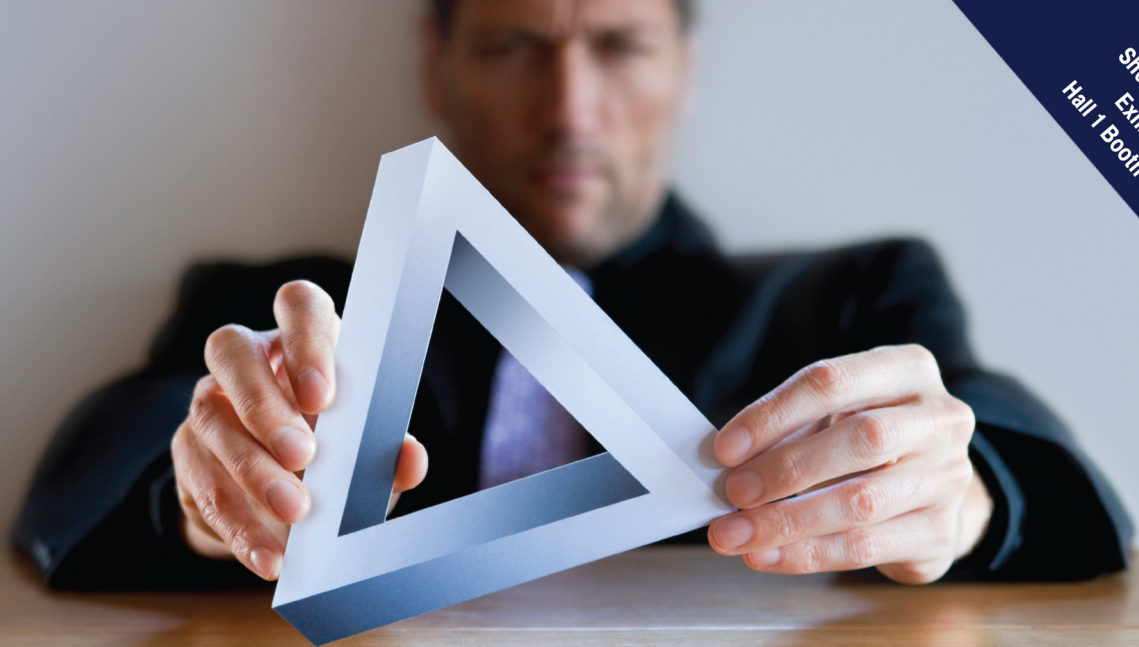
Session topics include an Overview and Update

of the NASA-DoD Lead-Free Electronics Project, Investigating the Edges of Lead-Free Assembly Processes, Mechanical Reliability Performance of Lead-Free Solder Alloys and the Impact of Alloy Composition, Design and Load Parameters in Lead-Free Solder Joint Reliability.

Programmatic Challenges of Pb-Free Technology for the High-Reliability Electronics Industry is the title of the keynote address given by Paul Vianco, Ph.D., Sandia National Laboratories and symposium chair and co-organizer.

Details can be found [here](#) or by contacting SMTA administrator [JoAnn Stromberg](#) at 952-920-7682.

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STEP STENCILS: A Powerful Tool for Special Applications

by **William E. Coleman**
PHOTO STENCIL

IN SUMMARY

Mixed-technology applications of solder paste printing for through-hole/SMT, as well as solder paste/flux printing for flip-chip/SMT, require special step stencil designs. Several applications and the stencil design to achieve a solution are discussed in detail in this paper.

Abstract

In the early days of SMT assembly, step stencils were used to reduce the stencil thickness for 25-mil-pitch leaded device apertures. However, as SMT requirements became more complex and, consequently, more demanding, so did the requirements for complex step stencils. Mixed-technology applications of solder paste printing for through-hole/SMT, as well as solder paste/

flux printing for flip-chip/SMT, require special step stencil designs. Thick metal stencils that have both relief etch pockets and reservoir-step pockets are very useful for glue and paste reservoir printing.

Electroform and laser-cut step-up stencils for ceramic BGAs and RF shields are a good solution to achieve additional solder paste height on the pads of these components. Special 3-D electroform stencils are an excellent solution for odd PCBs having some raised areas on the board (up to 0.090" high). The two-print stencil printing process is useful in dealing with the problem of small and large components coexisting on the same PCB. These applications and the stencil design to achieve a solution are discussed in detail in this paper.

Introduction

Eight different applications for step stencils will be described. These include the following:

1. Step-up stencils for ceramic BGAs.
2. Step-up stencils for intrusive reflow of through-hole components.



The two-print stencil printing process is useful in dealing with the problem of small and large components coexisting on the same PCB.



3. Step stencils with a relief etch pocket on the contact side (board side) for:
 - a. Raised vias
 - b. Bar codes
 - c. Board hold-down clips
 - d. Additive traces
4. Step stencils for two-print applications for mixed technology:
 - a. SMT/through-hole
 - b. Flip-chip/SMT
5. Thick stencils with etched reservoir pockets for printing glue for a variety of components with different stand-off heights.
6. Two-print stencil, with etched relief pockets, for printing glue for component attachment after SMT solder paste has been printed.
7. Three dimensional electroform stencils with a formed relief pocket for a high flex connector that connects two PCBs.
8. Two-print stencils for printing small devices like 0.3-mm-pitch uBGAs and 01005s at the same time as printing large devices like RF shields, SMT connectors, QFPs and other chip components.

Step Stencil Applications and Solutions

1. Ceramic BGAs

Ceramic BGAs present a challenge to the SMT assembly process. Since the high melting temperature prevents the solder balls from melting at normal reflow temperatures, any slight coplanarity problem can result in an open contact to the CBGA balls. It is desirable to print higher solder bricks on the CBGA pads to prevent this problem. Normally, a solder paste brick height of 7 to 8 mils is desirable. On the other hand, SMT components like 0.5-mm-pitch QFPs, 0402 chip components and R-packs will not tolerate an 8-mil-thick stencil. Their aperture sizes are too small to achieve good paste release with a stencil this thick. Therefore, a step-up stencil is required for this application.

An example of this stencil is shown in Figure 1. This stencil starts out as an 8-mil-thick foil and the foil is etched back to 5 mils

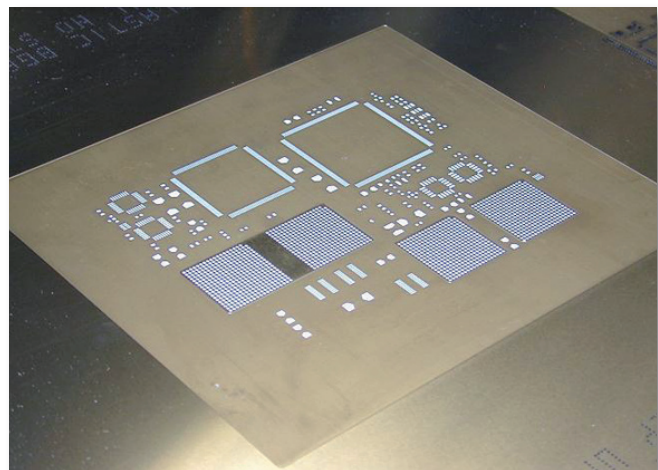


Figure 1: Step-up laser-cut stencil for CBGAs.

in all areas except in the CBGA area. The foil then has all the apertures, including the CBGA apertures, laser-cut into the foil. Electropolish and nickel plating are recommended for this stencil to achieve good paste release for the small apertures.

In cases where 0201 chip components and 0.5 mm pitch uBGAs are present, a stepped electroform stencil is recommended to achieve good paste release for these small apertures. A picture of a step-up electroform stencil is shown in Figure 2. The stencil is made by plating up to 5 mils in all areas and then continuing to plate up to 8 mils in the CBGA areas. Customers usually prefer the step on

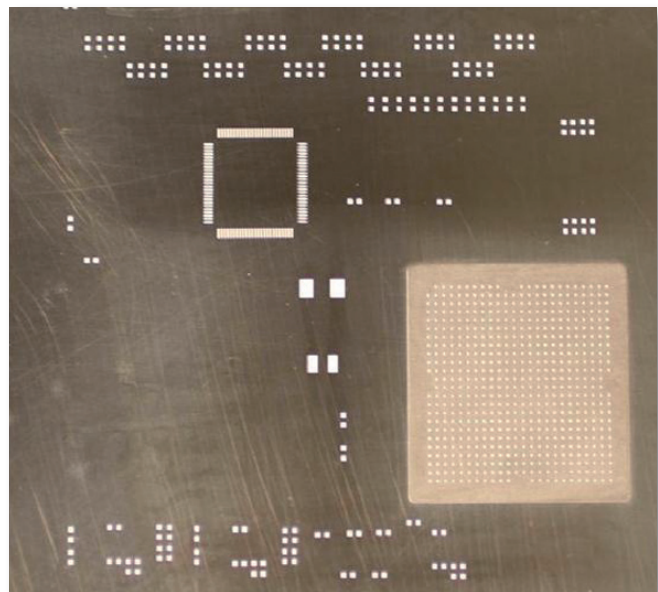


Figure 2: Step-up electroform stencil for CBGA.

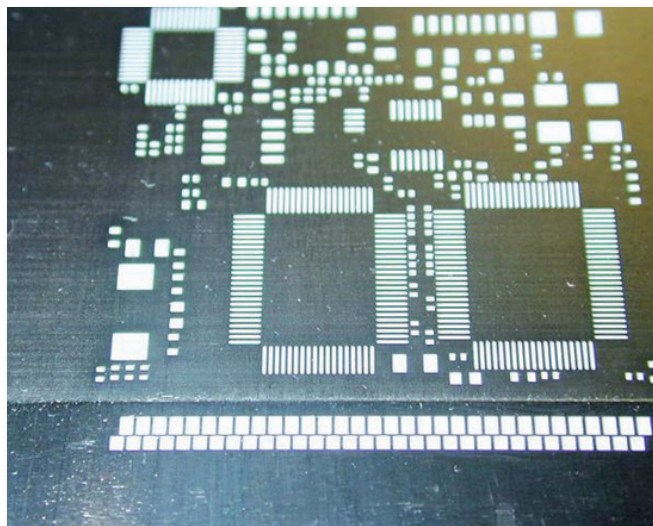


Figure 3: Step-up laser-cut stencil for through-hole connector.

the squeegee side of the stencil, and this is the case for the prior two examples. A general rule for spacing between the step ledge and first aperture in the lower thickness area (keep-out design) is 0.035 to 0.050" per 0.001" of step (IPC 7525 Stencil Design Guidelines). User feedback indicates that metal squeegee blades work fine with step-up stencils as long as these keep-out designs are followed.

2. Step-Up Stencil for Through-Hole Intrusive Reflow

An increasing trend has emerged to reflow through-hole components, rather than using wave soldering, along with the SMT components [1]. To achieve this, solder paste is printed on, in and around the through-hole hole and pad (annular ring). Three stencil alternatives can achieve sufficient solder paste for this application:

1. Overprint the hole/annular ring with an oversized stencil aperture.
2. Step-up and overprint the hole/annular ring with an oversized stencil aperture.
3. Two-print stencil where the second print stencil is very thick and provides more solder paste for the requirement. (This is described in the "Step Stencil for Two-Print Operation for Mixed Technology" section below.)

Figure 3 shows a step-up stencil with the step on the squeegee side for a through-hole edge connector. The stencil is 10 mils thick in the through-hole area and 5 mils thick elsewhere. The squeegee stroke is parallel to the step-down ledge so the entire length of the blade drops down to 5 mils during the squeegee stroke.

3. Relief Step Stencil with Relief Etch Pockets on Contact Side of Stencil

1. Raised via pads on the PCB. If a board has raised via pads, they will prevent the stencil from gasketing to the PCB. To achieve good stencil/board contact a relief pocket is etched on the contact side of the stencil wherever there is a raised via. Typically, the relief pocket depth is half of the stencil thickness, which is usually enough to clear the raised via. A picture of this stencil is seen in Figure 4.

2. Bar code on the PCB. Many PCBs have bar code identifiers attached to the board surface. If it gets too close to board pads it can prevent the stencil from gasketing to these pads during printing. A simple solution is to use a stencil that has a relief pocket etched in the area of the bar code. This allows the stencil to sit flat on the PCB during printing.

3. Board hold-down clips. Some stencil printers have edge clips which hold the PCB down during the print operation. If there are component pads close to the edge of the board, the stencil may not be able to gasket to

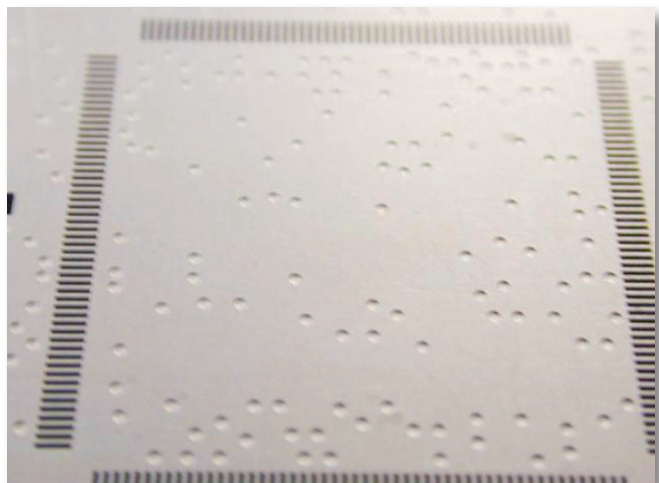


Figure 4: Raised via pad relief step stencil.

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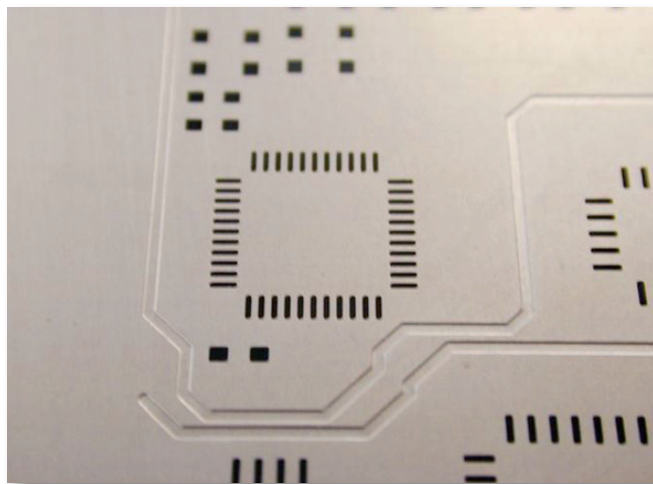


Figure 5: Additive trace relief pocket stencil.

the board on the edge. Again, a stencil solution is to provide a relief etch pocket in the area of the hold-down clips.

4. PCB with additive traces. Additive traces are added to the surface of the PCB to correct a design problem by altering the lead wiring. Unfortunately, this trace adds height to the board surface. A stencil solution is to provide a relief pocket around the additive trace. An example of this stencil is shown in Figure 5.

4. Step Stencil for Two-Print Operation for Mixed Technology

1. SMT/through-hole mixed technologies. When overprint (oversized apertures for the through-hole) with a normal step-up stencil does not provide enough solder paste volume for proper intrusive reflow a thicker stencil must be used. However, the normal SMT components will not tolerate a thick stencil (15 to 20 mils thick) and a step down (20 mils down to 5 mils) is impractical. The two-print stencil operation is a viable solution. Consider a PCB that has a fully-populated pin grid array (PGA). Overprint is limited because of the fully-populated geometry. The only alternative to providing more solder paste is to make the stencil thicker. In this case, a stencil 15 mils thick was required. In the two-print operation all the surface mount solder paste is printed with a normal SMT stencil of 5 or 6 mils thick. The second print stencil is 15 mils thick with

relief etch pockets etched on the contact side of the stencil any place that SMT solder paste was printed during the first print. As a rule of thumb, the relief pocket depth should be 4 mils deeper than the SMT first print stencil [2].

2. Flip-chip/SMT mixed technologies.

There are applications when it is desirable to print flux or solder paste for a flip-chip component and solder paste for normal SMT devices. Both are then placed and run through the reflow cycle. Normally, the stencil thickness for the flip-chip printing is 1 to 2 mils thick; much too thin for normal SMT printing. Two-print stencils are ideal for this application. A thin (1- to 2-mil-thick) electroform is used to print either flux or solder paste on the flip-chip pad sites on the PCB. Then a SMT stencil (5 mils thick) is used to print solder paste on all SMT pads. This stencil has relief pockets formed on the contact side anywhere flip-chip flux or paste was previously printed. Figure 6 shows a 3-D AMTX electroform stencil that is 5 mils thick with 3-mil relief pockets formed on the contact side which is ideal for this application. This stencil has a formed step-up relief pocket. The height of the stencil in the flip-chip area is 8 mils (5 mil stencil thickness and 3 mil relief pocket).

5. Thick Stencil with Deep-Etched Reservoirs for Printing Glue for Component Attachment

Advantages exist to printing glue rather than dispensing it. Set-up time is reduced and

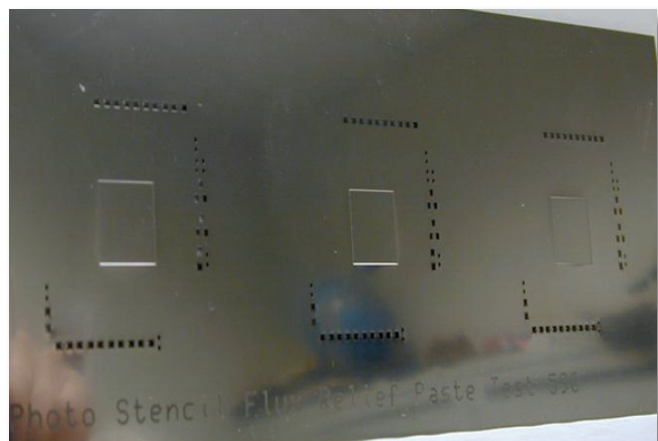


Figure 6: 3-D electroform stencil for paste printing with flux relief.

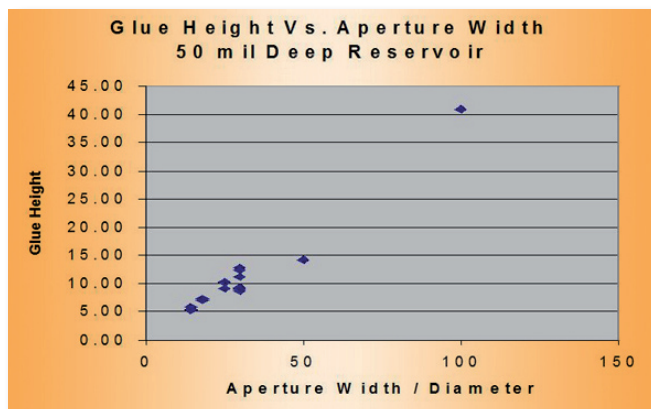


Figure 7: Glue height versus aperture size.

process time is shortened since glue bricks are deposited in parallel rather than one dot at a time. Glue does not print the same way solder paste does and it is acceptable, as well as useful, to leave glue remaining inside the stencil aperture. As a benefit, this allows different heights of glue to be printed using the same stencil thickness. Large apertures will release all the glue while small apertures will release only a portion of the glue. Glue height versus aperture size for a 50-mil-deep reservoir pocket is shown in Figure 7. This is very useful when the PCB contains components with different stand-off heights.

An example of an application is a PCB with chip components with a stand-off of 4 mils and an SOIC with a stand-off of 15 mils. This is shown as a schematic in Figure 8. By using a 15-mil-thick stencil the aperture sizes can be adjusted to provide 6 mils of glue height for the chip components and 15 mils high for the SOIC component.

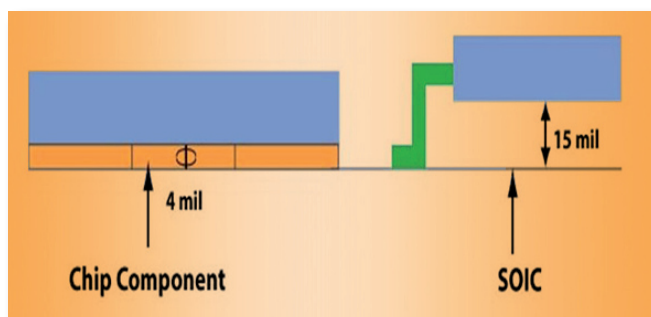


Figure 8: Chip component and SOIC with different stand-offs.

6. Two-Print Stencil for Printing Glue After Paste

It was reported that printing glue compared to dispensing glue resulted in lower defect rates for large and complex server type PCBs [3]. The process used is to print solder paste first for the back side components then print glue, with a 20-mil-thick stencil with 15-mil-deep relief pockets for the back side component solder bricks. The next three figures are courtesy of Mike Kochanowski: Figure 9 shows a schematic

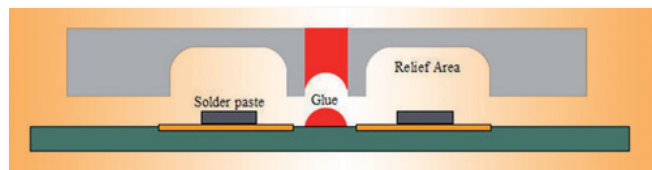


Figure 9: Glue two-print stencil 20 mil thick with 15 mil relief pockets.

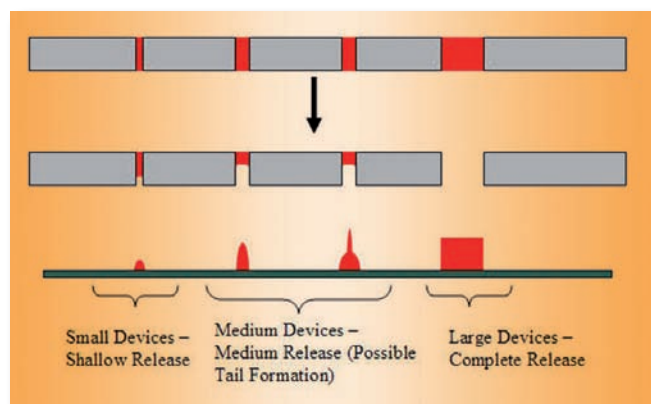


Figure 10: Different glue heights for different aperture sizes.

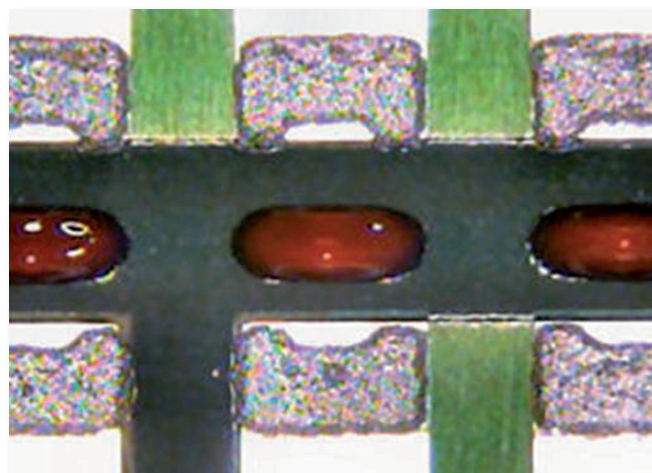


Figure 11: Glue and paste bricks for 0805 device.

cross section of the glue two-print stencil; Figure 10 illustrates the fact that some glue remains in the glue aperture depending on the size of the glue aperture; and glue and paste for a 0805 chip component is shown in Figure 11.

7. 3-D AMTX Electroform Stencil for Special PCBs Connected with High-Profile Flex Connector

Two PCBs are connected with a flexible connector, which rises up 90 mils above the board surface. The challenge was to be able to print solder paste on the SMT pads with the flexible connector obstructing a normal stencil from making contact with the board. The solution to this problem is a 3-D Electroform stencil, which is 5 mils thick, but has a 95-mil-high relief pocket formed in the stencil. Figure 12 shows a picture of the stencil. Figure 13 shows the squeegee side of the stencil along with the special E-Blade that has a notch formed in the blade for clearance of the relief pocket.

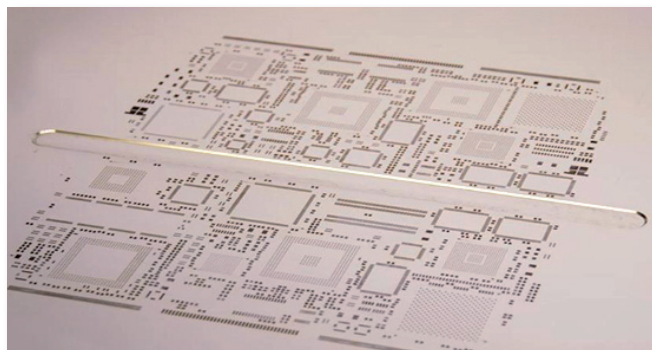


Figure 12: 3-D electroform stencil with 90-mil-high relief pocket.



Figure 13: 3-D electroform stencil with notched e-blade.

8. Two-Print Stencils When Very Small and Large Devices are Present on PCB

A problem exists when printing small devices like 0.3-mm-pitch uBGAs and 01005s at the same time as printing large devices such as RF shields, SMT connectors, QFPs and other chip components [4]. This problem is illustrated in Figures 14 and 15. If a thick stencil is used, good paste release is realized for the large apertures resulting in good solder fillets. However, small apertures have incomplete paste transfer because of low area ratios, resulting in dry solder joints for the small components.

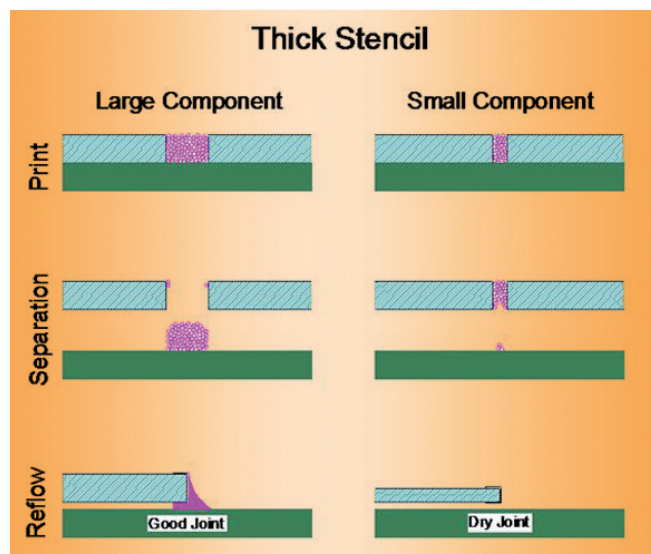


Figure 14: Print sequence for thick stencil.

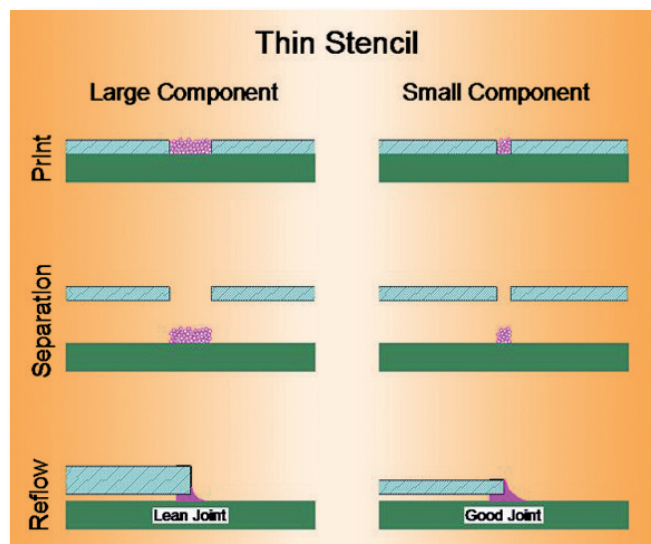


Figure 15: Print sequence for thin stencil.

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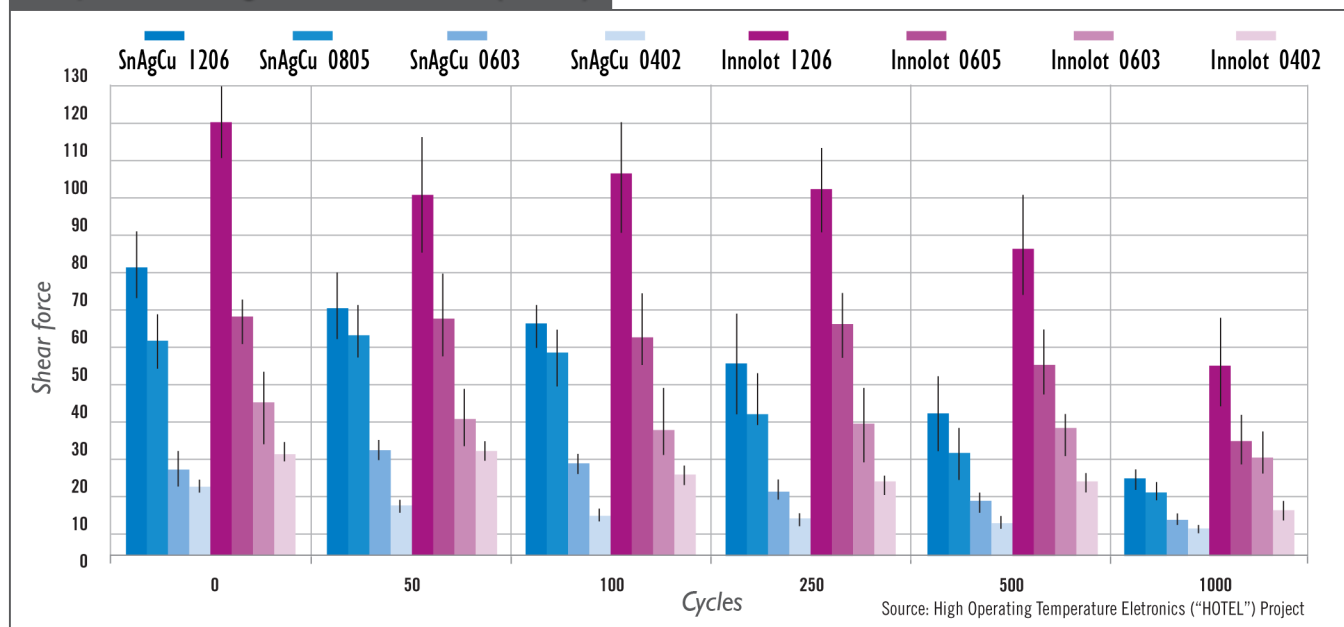
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Component and typical Aperture Size	Stencil Thickness →					
	2 mil 50u	2.5 mil 62u	3 mil 75u	3.5 mil 87u	4 mil 100u	5 mil 125u
01005						
6 mil (150u)	0.75	0.60	0.50	0.43	0.38	0.30
7 mil (175u)	0.88	0.70	0.58	0.50	0.44	0.35
.4mm CSP						
6 mil (150u)	0.75	0.60	0.50	0.43	0.38	0.30
7 mil (175u)	0.88	0.70	0.58	0.50	0.44	0.35
8 mil (200u)	1.00	0.80	0.67	0.57	0.50	0.40

Green = OK Orange = Warning Red = Stop

Figure 16: Area ratio matrix.

On the other hand, a thin stencil provides good paste release for both large and small components, but too little paste for the large components results in lean solder joints. The area ratio matrix, shown in Figure 16, illustrates acceptable stencil thickness and aperture sizes for 01005 and 0.4 mm uBGA devices. One possible solution to this problem is a two-print stencil process, where the small component's solder paste bricks are printed first with a thin stencil.

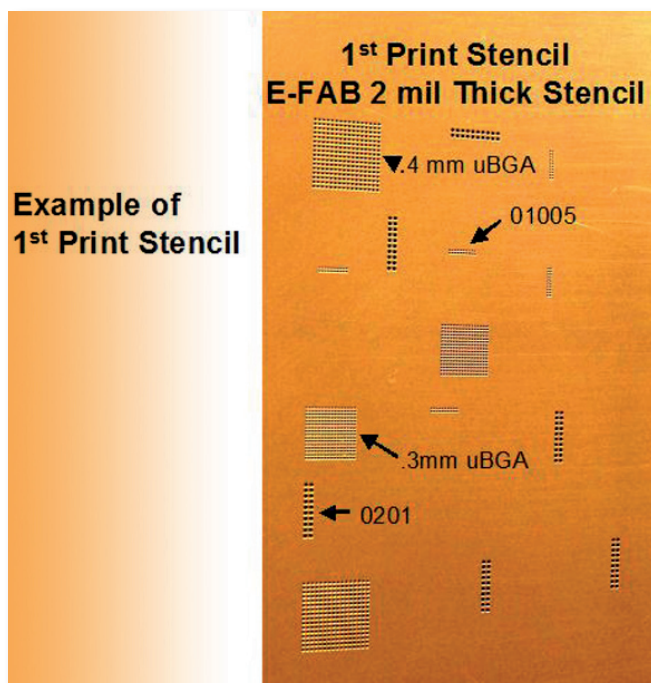


Figure 17: First print electroform stencil.

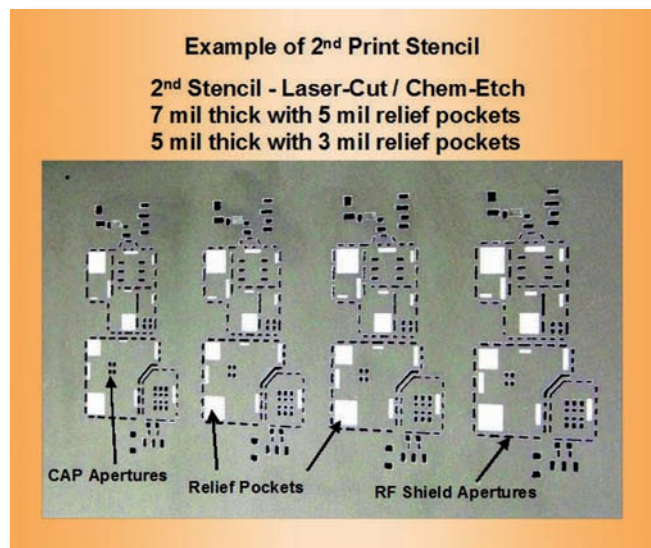


Figure 18: Second print chem-etch relief/laser-cut apertures.

Next, a second in-line screen printer prints solder paste for the large components. This stencil has relief pockets etched on the board side of the stencil anywhere solder paste was printed with the first stencil. This process is illustrated for a cell phone application in Figures 17 and 18. Figure 17 shows a 2-mil-thick electroformed stencil for printing 0.3 and 0.4 mm uBGAs and 01005 and 0201 chip components. Figure 18 shows the second print stencil with relief pockets for the first print stencil solder paste bricks.

The design question that needs to be

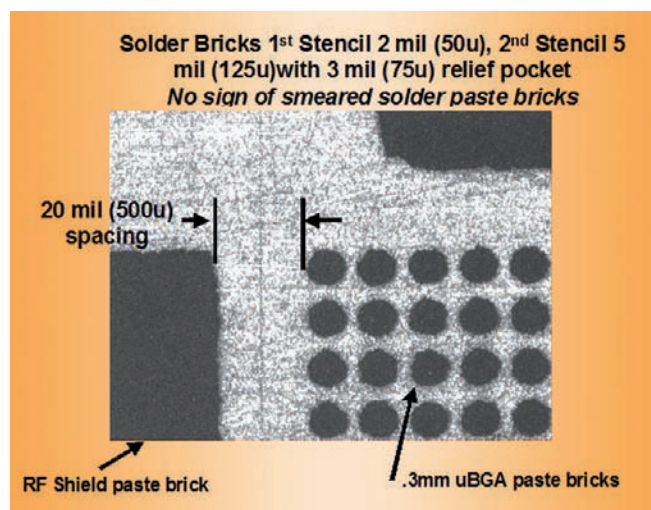


Figure 19: Solder bricks showing no smearing.

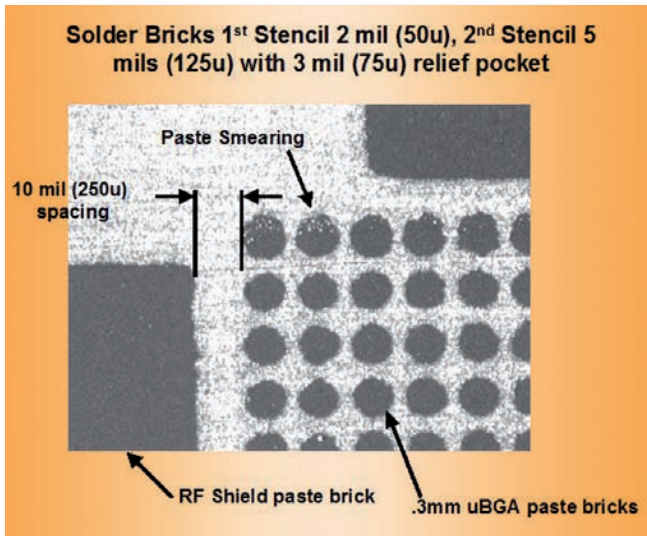


Figure 20: Solder bricks showing smearing.

answered is: What is the smallest spacing between apertures in the first and second print? Figure 19 shows that 20-mil spacing between apertures with a 3-mil-deep relief pocket works very well with no smearing of the solder paste bricks, in this case the 0.3mm uBGA bricks. Figure 20 shows smearing when the spacing is 10 mils. This suggests that somewhere around 15 mils between apertures is a workable spacing for this process.

Conclusion

Step stencil technology offers unique solutions for various printing applications. Step-up stencils offer printing solutions for CBGA and through-hole paste volume/height requirements. Step-up electroform stencils not only offer solutions for higher solder volume/height for the above applications, but also provide excellent paste transfer for 0.5 mm uBGAs and 0201 devices. Two-print stencils, including a thick second print stencil with deep relief step pockets, offer solutions for both glue-attach printing and intrusive reflow printing. Normal SMT stencils 5 to 6 mils thick with relief step pockets on the contact side of the stencil offer solutions when there are raised areas on the PCB that would prevent a normal stencil from gasketing to the board.

3-D AMTX electroform stencils provide an excellent solution for two-print stencil

operations when printing flux/paste for flip-chip and paste for SMT in a mixed technology application flip-chip/SMT. 3-D AMTX electroform stencils with formed-relief pockets are excellent for printing on boards when high protrusions exist on the board surface. Two-print stencils are also a viable solution for printing very small components along with large components on PCBs as in cell phone applications. **SMT**

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Dr. William E. Coleman earned his Ph.D. in Physics from West Virginia University. His early career was spent with NCR developing memory and visual display devices. Dr. Coleman has spent the past 23 years at

Photo Stencil as Vice President of Technology working closely with customers to understand their SMT printing requirements. At Photo Stencil he has developed several innovative solutions for these requirements. Dr. Coleman has published over 20 papers in this field and is presently Co-Chair of IPC 5-21e committee, which produced IPC 7525 "Stencil Design Guidelines." He is on the Editorial Advisory Board for *SMT Magazine* and the Advisory Board for West Virginia University.

MilAero007 Highlights



SEC Authority to Phase-In Conflict Minerals Regulations

IPC — Association Connecting Electronics Industries recently submitted comments to the U.S. Securities and Exchange Commission (SEC) regarding the legal basis for a phase-in of the conflict minerals regulatory requirements. Submitted in early June, the comments were prepared by SEC expert Thomas White of WilmerHale.

PPI Time Zero Receives AS9100 Certification

Becoming AS9100 certified demonstrates PPI Time Zero, Inc.'s continued commitment to provide quality services to customers and to meet the special needs of aerospace business activities. Although the company has operated to ISO9001 standards for many years, the changes in its organization required to reach the AS9100 level have required a personal commitment from each and every employee.

Kitron, Prevas Enter Strategic Partnership

Through the cooperation between Prevas and Kitron, customers get the opportunity of market leading support throughout their entire value chain including product and test development, industrialization, sourcing, manufacturing, logistics, redesign and other after sales services.

LaBarge Stockholders Approve Acquisition by Ducommun

LaBarge, Inc. announced that at a special meeting, the company's stockholders voted to approve and adopt the Agreement and Plan of Merger under which LaBarge will be acquired by Ducommun Incorporated. Under the terms of the merger agreement, each outstanding share of LaBarge common stock will be cancelled and converted into the right to receive \$19.25 in cash.

SMTA Announces AIMS Harsh Environments Symposium

The AIMS Harsh Environments Symposium, to be held October 17, 2011, as a focused symposium at SMTAI in Ft. Worth, Texas, will address concerns related to harsh environment electronics and the challenges within the electronics community, with an added emphasis on military and space.

API Technologies Achieves New AS9100 Rev C Certifications

API Technologies Corporation, a provider of electronic systems, subsystems, RF and secure systems for defense, aerospace and commercial applications, has achieved AS9100 Rev C certification, the quality standard for the aerospace and defense industries, for its Windber and Alum Bank, Pennsylvania locations. These locations mark the company's fifth and sixth such facilities to achieve the designation.

OSI Systems Receives \$248 Million IDIQ Contract

OSI Systems, Inc., a vertically-integrated provider of specialized electronic products for critical applications in the security and healthcare industries, has announced that its Security division, Rapiscan Systems, has been awarded a three-year Indefinite Delivery, Indefinite Quantity (IDIQ) contract valued at up to \$248 million from the U.S. Army for Entry Control Point Non-Intrusive Inspection systems.

High-Reliability Suppliers Benefit from New Cleaning Tests

The drive to cut costs has prompted many companies to eliminate cleaning steps by shifting to no-clean fluxes. However, printed board users in high reliability fields like aerospace and automotive have found that residues can remain, prompting an industry-wide effort to improve the tests used to determine cleanliness.

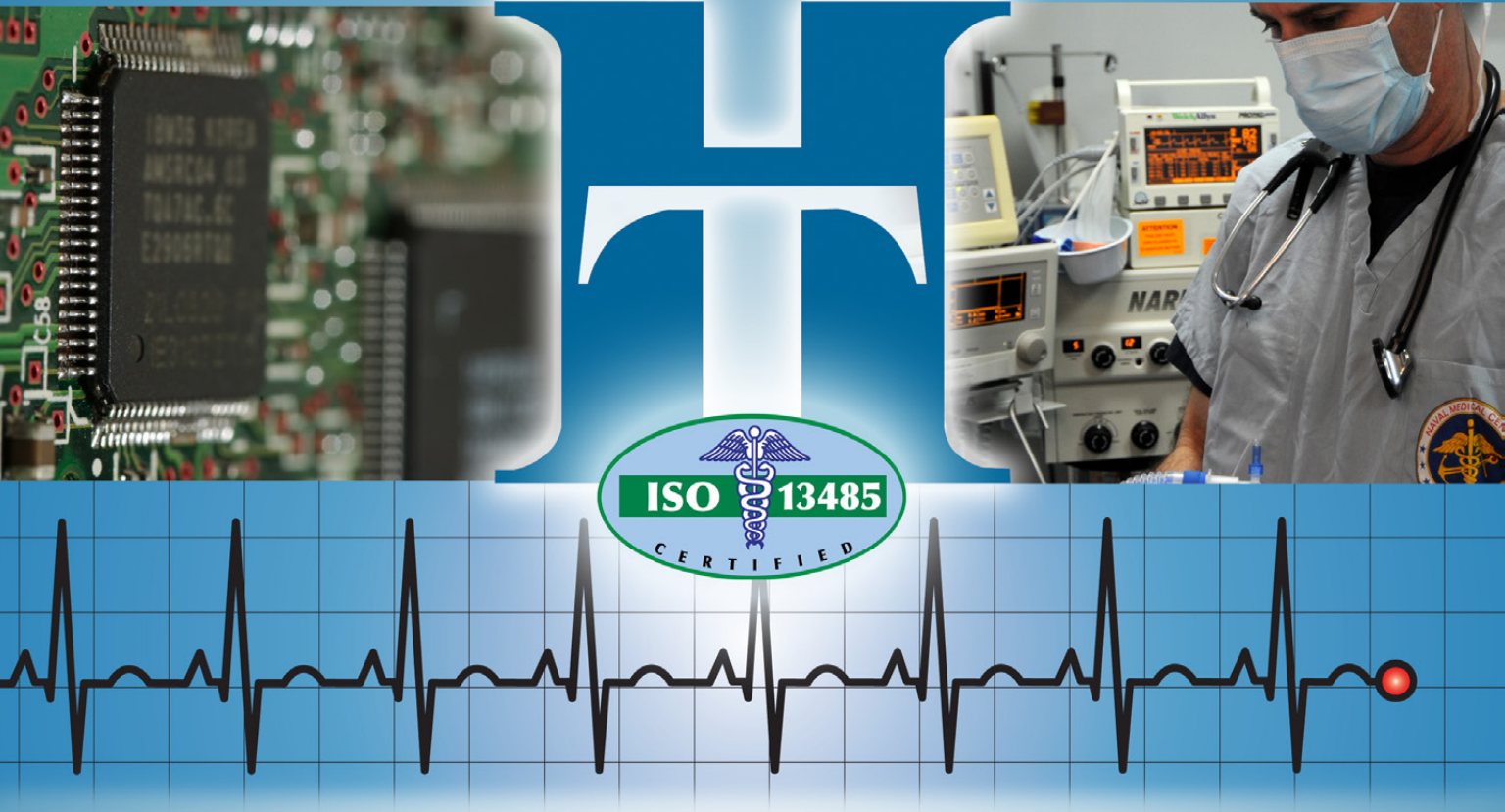
Harris, Tektronix Component Enter Partnership Agreement

Harris Corporation and Tektronix Component Solutions have announced the strengthening of their long-standing relationship via the establishment of a strategic partnership agreement. The mutually-beneficial relationship is intended to enhance both organizations' ability to deliver greater value to mutual customers in the defense industry and aid in the innovation of next-generation products.

AWS Group Earns Nadcap Accreditation

AWS Group has received notice of accreditation by Nadcap, the body which aims to provide continual improvement within the aerospace, defense, automotive and related industries. Together with ISO 9001 (2000), AS/EN 9100 and ISO 14001 plus Silver status for supply chain excellence in the ADS SC21 programme, this most-recent and challenging approval means that AWS Group has "the full set" of quality and process certification.

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by Dr. Helmut Schweigart

ZESTRON EUROPE

and Umut Tosun

ZESTRON AMERICA

IN SUMMARY

Circuit boards in ordinary consumer products are not intended to last, but high-reliability applications in the military, aerospace, communication, medical and automotive industries demand a guaranteed, long-term product life. The application of a conformal coating is one way to ensure product reliability.

Effectively removing contamination is one step toward guaranteeing the long-term reliability of mission-critical circuit assemblies. While circuit boards in ordinary consumer products are not intended to last, high-reliability applications in the military, aerospace, communication, medical and automotive industries demand a guaranteed, long-term product life. The application of a conformal coating is one way to ensure product reliability.

However, proper functioning of electronic

assemblies under the most stringent and adverse conditions can only be guaranteed when conformal coatings properly adhere to board surfaces. The usual requirement for effective adhesion is best assured through the highest cleanliness level of the assembly surface. Cleanliness assessments can now be performed by implementing quick, innovative and economical analytical test methods.

In the automotive, military and aerospace related industries, electronic assembly requirements have been steadily increasing over the years. With rising package densities and complexities, higher assembly cleanliness standards are required during the manufacturing and assembly process.

The use of assemblies under harsh climatic conditions, such as temperature fluctuations and moisture exposure, has increased the risk of malfunctions. Thus, failure mechanisms such as leakage currents, electrochemical migration and dendrite growth are initiated through environmental influences (Figures 1 and 2).

With the introduction of lead-free solder pastes, the increased amount of rosin and activator content must also be taken into consideration. The latter is responsible for an increase in corrosion-related malfunctions and therefore a reduction in the reliability and life expectancy of electronic assemblies.

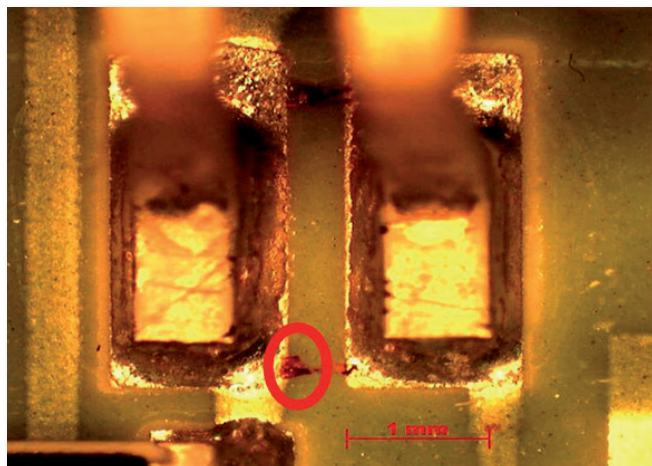


Figure 1: Dendrite growth between solder joints.

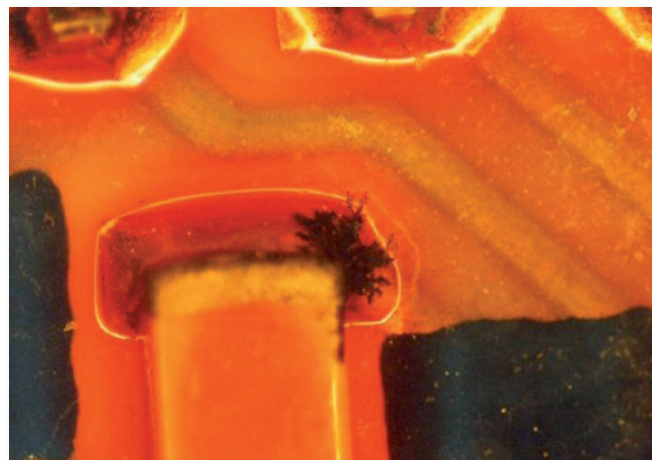


Figure 2: Electrochemical migration even under conformal coating.

Coating as a Reliable Protective Measure

To ensure the reliability of electronic products, protecting assemblies with conformal coatings is an important and necessary measure. As conformal coating is usually the last step in the manufacturing process, application failures may have drastic effects on production costs and can lead to unavoidable field failures. To guarantee the optimum adhesion of the protective coating and prevent subsequent formations of cracks or delamination, it is of utmost importance to ensure the highest cleanliness level of the assemblies prior to coating.

Minimum Surface Cleanliness Before Conformal Coating

The minimum cleanliness requirement prior to conformal coating applications is specified in the latest standard, J-STD 001E. Accordingly, the following methods are required for proper qualification (see Table 1).

Visual inspection can be performed with a microscope. No visual impurities should be observed.

The amount of rosin on assemblies plays a significant role as it directly influences adhesion of conformal coating. Rosin residues can lead to insufficient adhesion and can result in coating delamination. Acknowledging the threshold for Class 3 assemblies with a set limit of $40\mu\text{g}/\text{cm}^2$, one has to be aware that this value is equivalent to the amount of rosin

that can be found around a single solder joint. Furthermore, the amount of rosin left by lead-free solder pastes has increased tremendously due to changes in their composition. Over the years, rosin residues have been detected by means of extensive and lengthy procedures such as HPLC (high-pressure liquid chromatography). However, they can now be easily analyzed through a quick chemical test such as a resin test. This innovative test method ensures that residual resin can be easily identified and subsequently removed to ensure proper adhesion of conformal coating.

While assessing the surface's cleanliness according to the J-STD 001E, the ion equivalent represents an important test method as well. A high ionic equivalent value indicates the existence of a large amount of hygroscopic impurities. Over time, these impurities might lead to coating delamination and ultimately result in failure of the assembly (Figure 3).

J-STD 001E QUALIFICATION REQUIREMENTS
Visual inspection with 20x or 40x magnification (according to IPC A610E)
Measurement of rosin residues ($<40\mu\text{g}/\text{cm}^2$ for Class 3 assemblies)
Measurement of ionic contamination ($<1.56\mu\text{g}/\text{cm}^2$ eq. NaCl)
Evidence of other organic impurities
SIR measurement after or during climatic storage

Table 1: J-STD 001E Qualification Requirements.

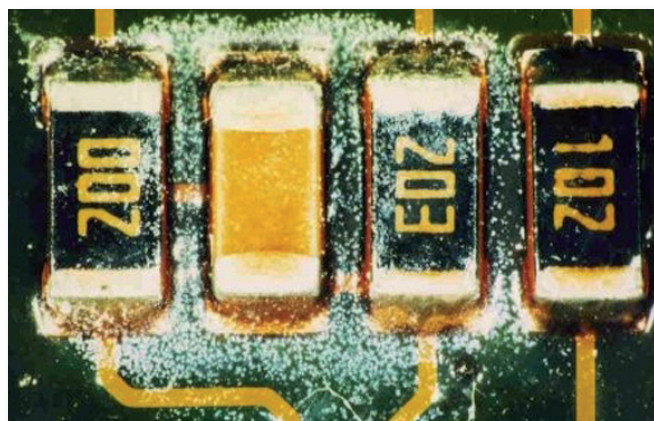


Figure 3: Coating delamination.

Other organic impurities such as flux residues can clearly influence the quality of the coating and trigger failure mechanisms underneath the conformal layer. In accordance with J-STD 001E, the presence of organic impurities can either be tested with infrared spectroscopy or detected with a quick and easy-to-use discoloration method such as the flux test. By means of a color reaction, the flux test specifically reveals organic acids used as activators. In addition, this innovative and non-destructive test method provides a visual distribution of the critical residues on the board surface.

SIR measurements demonstrate surface insulation resistance. A high degree of insulation ensures that electrical signals on the assembly are not distorted. Flux residues and conductive impurities may cause leakage current bridges and can thereby lead to malfunctions. While performing SIR measurements, a comb structure is stored in a climatic exposure test cabinet and the surface resistance between the individual comb structures is measured. All previously mentioned methods ensure the detection of the various impurities.

Nevertheless, the integration of a cleaning process is usually required to be able to maintain all of the production thresholds set by J-STD 001E. The cleaning process should not only remove impurities, but also guarantee the proper adhesion of the conformal coating to minimize long-term risk of future crack formation and delamination.

Conclusion

Coupling an appropriate cleaning process with innovative surface cleanliness tests will yield an economical and cost-effective solution and result in a proper coating process while enhancing the process and operational reliability of the coated assemblies. The German Society for Corrosion Protection (GfKORR)—a federation of corrosion experts from industry and academia working in all fields of corrosion science with the goal of avoiding corrosion and its negative consequences—is endorsing this statement in its latest “Use and Processing of Conformal Coatings for Electronics Assemblies” guideline. Authored by a consortium of leading coating manufacturers, this guideline provides a selection of reliable and economical process solutions. When using optimized cleaning and qualification test methods during the production steps preceding the coating process, coating adhesion is ensured and the long-term reliability of the assemblies is guaranteed. **SMT**



Helmut Schweigart, Ph.D., is head of the Application and Process Technology Department of ZESTRON Europe, located in Ingolstadt, Germany. Dr. Schweigart holds a Ph.D. in mechanical

engineering and completed his theses in the area of “Reliability of Electronic Assemblies” at the Technical University of Munich, Germany. Apart from being a chair of several task groups related to corrosion and reliability aspects, Dr. Schweigart has published numerous technical articles in leading electric manufacturing magazines.



Umut Tosun, M.S.Chem.Eng., is the Application Technology Manager at ZESTRON America and is also the manager of the Global Task Group. As an active member of the SMTA and IPC organizations,

Tosun has presented a variety of technical papers and studies. He is also a member of the “Ask the Experts” Panel from Circuitnet, where, on a regular basis, he shares his expertise and knowledge with others.

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Micro Access Technologies on PCB Assemblies

by Anthony J. Suto
TERADYNE INC.

IN SUMMARY

As successful as ICT has been over the years in finding potentially costly manufacturing defects early on the production line where it is less expensive to repair, a substantial change has occurred in the characteristics of the tested board assemblies that challenge the continued use of ICT within certain market segments.

In-circuit test has been instrumental in identifying process defects on countless varieties of populated PCB assemblies for over four decades. In-circuit test (ICT) operates by gaining electrical access to the board under test through a bed-of-nails test fixture. The PCB is designed to support this level of testability by incorporating test pads on each net that can be contacted by the bed-of-nails fixture.

When performing component tests, each component is typically isolated from the surrounding components and is tested on an individual basis. This divide-and-conquer strategy allows the system to test virtually any complex PCB without the need for

detailed knowledge of the overall assembly's functionality.

As successful as ICT has been over the years in finding potentially costly manufacturing defects early on the production line where it is less expensive to repair, a substantial change has occurred in the characteristics of the tested board assemblies that challenge the continued use of ICT within certain market segments.

Technology Trends Threatening ICT

High density interconnect (HDI), increasingly higher data rates and miniaturization of PCBs are all trends that limit the widespread use of conventional test pads. With PCB line widths of less than 4 mils and spacing of less than 4 mils on HDI assemblies, it is virtually impossible to place a 35-mil-diameter test pad, or even one that is only 20 mils across.

The increased use of area array packaging, such as ball grid arrays (BGA) and the use of blind and buried vias, also makes it difficult to gain electrical access to signals because the signal trace may be buried in an inner layer, with no available surface access for a test pad. Finally, customers are constantly demanding higher product functionality in either the same or smaller footprint, and this miniaturization trend is also placing pressures on the design community to eliminate conventional test point access.



For these high-speed signals, changes in the path impedance can cause reflections or other undesirable effects that interfere with reliable signal transmission.



Even if it were possible to place test points on a PCB assembly, the added capacitance at the access point location would lower the characteristic impedance of a high-speed, multi-gigabit transmission line at that particular location. For these high-speed signals, changes in the path impedance can cause reflections or other undesirable effects that interfere with reliable signal transmission. As a result, test points may limit the signaling speed that may be reliably achieved on a compromised transmission path and therefore disrupt the target operation of a printed circuit board that has been designed to operate at high speeds.

Fortunately, a variety of micro access technologies are available, including Agilent's bead probe technology [1], Rex Waygood's solder bump [2], Prasad's solder bump [3], Vaucher's access technique [4] and the Test Access Component (TAC) [5], that all offer a means of retaining electrical access on today's complex PCB assemblies.

These techniques, some dating back to the 1980s and 1990s, are in the process of being re-discovered and re-deployed in high-volume production as a means of gaining electrical access on HDI PCB assemblies and on high-speed signal nets. These micro access objects are geometrically small enough to have minimal to no impact on PCB signal routing and minimal impact on high-speed signal integrity.

Changing the Paradigm

Gaining electrical access to PCB nets traditionally involved targeting a large test point or test pad on the PCB under test with a small diameter test probe. This concept alleviated the need to have highly-accurate and expensive fixturing technologies because any mechanical alignment inaccuracies between the test probe and the test pad can be accommodated by using a relatively large test target on the board. Micro access techniques have reversed this paradigm by placing a small test point on the PCB assembly that is targeted by a large flat head or micro-serrated probe. A small feature size object is still contacting a large feature size object in order to resolve

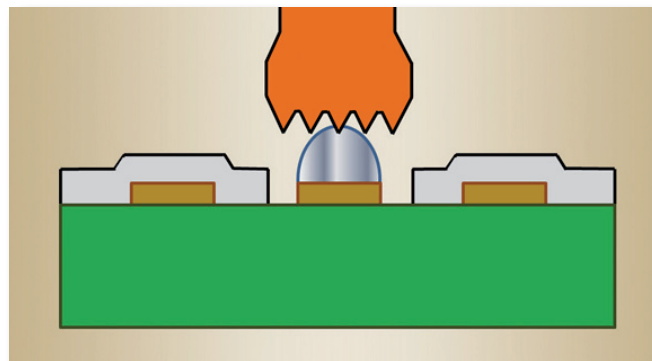


Figure 1: Waygood solder bump, targeted with a large, serrated fixture probe.

targeting inaccuracy, but the locations of the objects have been effectively swapped.

A Technology Ahead of its Time

One of the earliest micro access technology dates back to the year 1990 and is cited in Reference 2. This reference describes the concept of using a small solder bump on a PCB to gain electrical access to on-board signals. Specifically, this technique involves printing a sufficient amount of solder paste on a test point location to form a solder bump after reflow that rises above the solder mask. A significantly larger serrated or flat-headed test probe can then be used to contact the solder bump for the purposes of electrical testing of the PCB assembly (see Figure 1).

A second micro access technology published in 1997 (Reference 3), essentially bolsters the earlier teachings of using a solder bump on a PCB as an access point, but discusses placing a solder bump on test point locations that are smaller than 30 mils in feature size.

As interesting as tiny solder bumps are for gaining electrical access to signals on PCB assemblies, there are at least two additional micro access techniques that diverge from this concept.

Getting the Bump Out

An early, non-solder bump micro access technique was disclosed in 1996 at a technology conference (Reference 4). The concept disclosed opening a small aperture in the solder mask directly above a signal trace.

The exposed conductor is contacted by a large diameter, deformable Z-axis conductor tipped probe. The Z-axis anisotropic conducting probe tip material is comprised of a deformable insulating material (similar to an eraser tip) that is loaded with small diameter metal wires that enable electrical conduction in the Z plane (Figure 2). In practice, enough probe force is exerted upon the probe tip to partially deform, enter the aperture opening and make electrical contact with the exposed etch below. The other side of the probe tip is connected to the spring-loaded test probe to maintain the electrical path.

The probe tip geometry is large as compared to the solder mask aperture opening to ease the test fixture's targeting accuracy and repeatability. In practice, the exposed etch is typically HASL finished to eliminate oxidation of the copper etch. The interesting part of this board probing technique is that the PCB signal traces can be laid out without the need to re-route around traditional test points. Needless to say, only signal traces that reside partially or completely on the outer PCB layers can be accessed. This is a common trait of many micro access techniques.

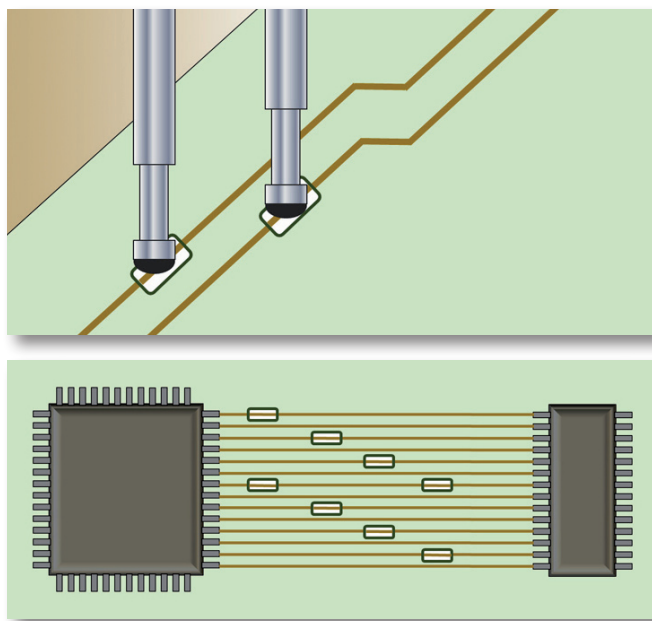


Figure 2: Vaucher concept of using a deformable Z-axis anisotropic conducting material on probe tips to gain electrical access on signal nets through small solder mask openings.

The next non-solder bump micro access technique is called the Test Access Component, or TAC [5]. With this technology, a small surface mount component is mounted directly on top of the signal trace to gain electrical access. The part that is being used as an access point is typically an inexpensive 0402, 0201 or even a 01005 resistor component. Ideally, the part chosen has a body width that is nearly the same width of the signal etch so as to add a negligible amount of additional per-unit-length capacitance to the trace. The signal trace runs directly under the component, effectively shorting out the end caps. As a result, the specific value of the component does not matter in this application.

The TAC device supplies two access locations on the end caps for increased electrical and mechanical reliability. The small component is typically contacted by a large flat head or micro-serrated probe in the test fixture, thereby minimizing the need for highly-accurate fixturing technologies. In practice, a small amount of solder wicks up to the top of the end caps and it is this material that the large fixture probe contacts (Figure 3).

The insertion loss of a 2.5 inch length of 8-mil-wide etch with a 0201 TAC mounted in the center of the trace has been characterized. The insertion loss, or S21 loss of 6dbV at 20GHz, is due almost entirely to the dielectric loss of the FR-4 material and not the test access component itself.

The test access component was additionally tested for mechanical robustness. With this test case, a 0201 TAC was repeatedly contacted with a large 0.060 inch diameter flat headed probe with a spring force of 5 oz. Kelvin resistance measurements were made on each contact cycle and the minimum and maximum values for every group of 100 readings were charted. The results showed that the contact resistance is very low and repeatable at 12 milli-ohms with no open or high-resistance cycles for 100,000 cycles.

Finally, Figure 4 shows a section of the test board and the corresponding TDR measurements for the signal etch and the TAC. As shown in this illustration, the impedance is nominally 50 ohms and dips slightly by less

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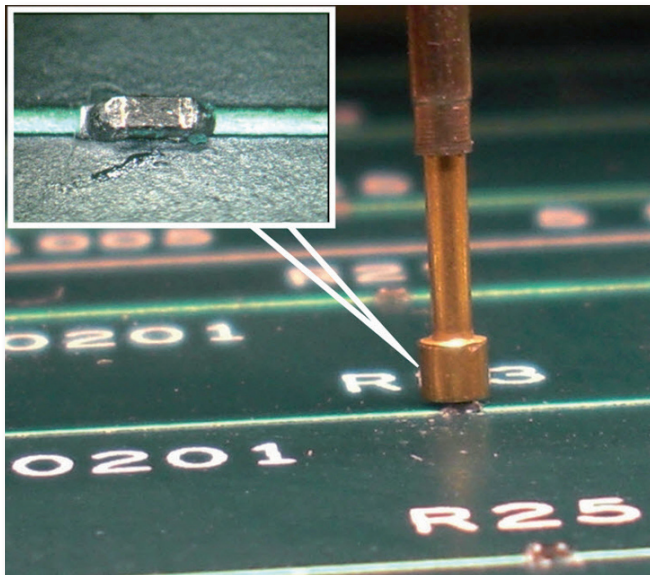


Figure 3: Test Access Component (TAC) used to electrical gain access on PCB trace.

than an ohm at the TAC location. This slight dip is far less than the normal tolerance of a controlled impedance PCB, which is usually specified as $\pm 10\%$ of the desired characteristic impedance. As a result, a small test access component can be used on gigabit signal traces with negligible signal integrity impact.

A World of Compensation

Although some signal integrity engineers may try to dissuade board designers and test engineers from placing test pads on high-speed signals, there are ways that the board designer can compensate for the added capacitance of such a structure and create a more uniform transmission line. This technique can also be applied to TAC components that are physically much wider than the signal trace width and add unwanted capacitance and corresponding impedance discontinuity on the line.

Compensating a test pad or a large TAC can be accomplished by removing sections of the reference plane that lies directly below the surface signal trace. In essence, the anti-pad structure in the reference plane effectively removes some parallel plate capacitance and fringing capacitance to best match the nominal per-unit length capacitance between the line and the reference plane. The specific

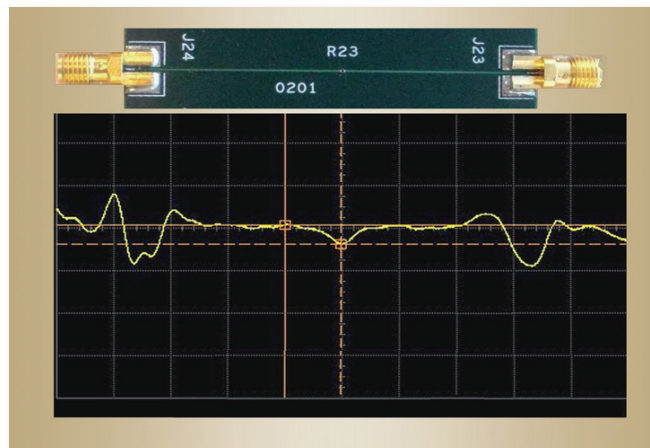


Figure 4: Section of a test board and corresponding TDR of trace with 0201 TAC in the center of 2.5 inch long, 8-mil-wide, 50 Ohm trace.

geometry of the anti-pad structure depends upon a number of parameters, including the dielectric constant of the PCB medium, the trace width, height and distance from the reference plane, as well as the solder mask thickness and material. As a result, it is best to model the structure with a 3-D electromagnetic field solver to validate the optimal anti-pad dimensions.

Knowing that the instantaneous return current from an initial wave front propagates in the opposite direction in the reference plane, it is good practice to give the return current a low inductance path to travel. As a result, the compensating anti-etch structure in the reference plane should allow for a return current path directly underneath the test pad or large TAC. Figure 5 shows an example of how a test point can be compensated.

What to Use

Micro access techniques involving solder bumps have been validated as a viable test access vehicle in high-volume manufacturing environments [6]. These structures can be used with HDI PCB assemblies and on high-speed signal traces without negative impact to signal integrity. It is recommended that the solder bump structures be implemented in the manner cited in the published references and to assess any potential intellectual

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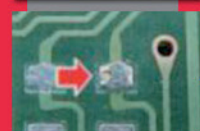
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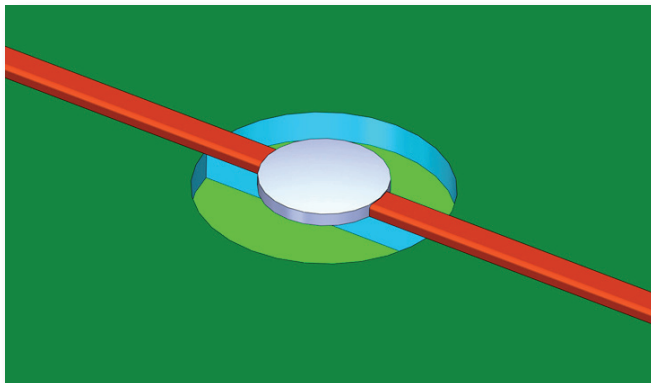


Figure 5: Compensation of conventional test pad's additional capacitance by voiding out two crescent-shaped portions in the reference plane. Note that there is a strip of the reference plane under the test pad for the wave-front return current.

property issues associated with a particular implementation. The other two, non-solder bump access technologies are also viable alternatives that support HDI and high-speed signaling. In the end, it is recommended that all micro access techniques be evaluated to determine which technique yields the best results for a given test application.

In-circuit testing is still viewed by many to be the most economical test method of obtaining the best overall test coverage and diagnostic resolution on contemporary PCB assemblies. PCB trends that involve miniaturization, HDI and high-speed signaling have all threatened the continued use of ICT because of the diminishing use of conventional test pads. Employing micro access technologies on circuit assemblies will help extend electrical access and allow the continued use of in-circuit test platforms to support mission-level testing, as well as future test technologies. **SMT**

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Anthony Suto is a Senior Staff Scientist for Teradyne's systems test group and has worked at Teradyne for over 27 years. In this role, he has contributed in the in-circuit, automated X-ray inspection, semiconductor test and functional test domains. Suto earned his electrical engineering degree from Union College in New York and has authored a variety of patents and technical papers.

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Video Interview

Condensation Soldering in High-Reliability Applications

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John Bashe, general manager of Rehm Thermal Systems, meets with Editor Pete Starkey at APEX to explain the principles and benefits of condensation soldering in high-reliability applications.



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Henkel Achieves Silver Sintering Technology Success

Henkel Electronic Materials has announced its success with a revolutionary silver (Ag) sintering technology that enables high-volume production of modern power packages in a process that does not require pressure. In its market debut, Henkel's Ag sintering capability has been designed into Ablestik SSP2000, a high-reliability die attach material well-suited for use with power modules such as IGBTs and high power LED products.

With Ablestik SSP2000, because the silver particles are joined via a unique surface tension mechanism, the pressure requirement is eliminated and the material can be cured in a standard batch oven at a temperature as low as 200°C. In addition, Ablestik SSP2000 can be processed on standard die bonding systems, eliminating the need to reinvest in specialist equipment and making the transition from existing materials simple, fast and cost-effective.

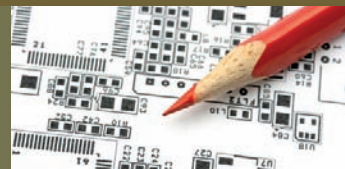
While high UPH is a central advantage of

Ablestik SSP2000, even more notable is the material's thermal resistance and reliability. When compared to high-lead soft solders, which are the current material of choice for power semiconductor devices, Ablestik SSP2000 has far superior power cycling reliability. In power cycle testing where solder failed at 200 cycles, the Ag sintering technology was able to reach more than 2,000 cycles before the first failure.

Not only do semiconductor packaging specialists want higher throughput, higher performance materials, but are also actively seeking viable replacements to high-lead solders--particularly in the power device segment. The RoHS deadline for the elimination of lead-based materials from the power device market is currently set for 2014, which means that in less than three years suitable alternatives must be in place.

For more information, visit:
www.henkel.com/electronics.

PCBDesign007 Highlights



Happy Holden Keynote Q&A: Asia Driving HDI

"Asian companies have government-backed loan guarantees, so banks are willing to finance all of this growth: New plants, equipment and processes. And PCBs create a lot of jobs," Happy Holden explains. "So industry gets the focus from government that it needs, as well as access to government research and tax-free export zones where manufacturing costs are significantly reduced."

Cadence Acquires Azuro Inc.

Cadence Design Systems has acquired Azuro Inc., a company that offers a unique clock concurrent optimization technology, also known as ccopt. Terms of the acquisition were not disclosed. The acquisition is not expected to have a material effect on the Cadence's results of operation for fiscal 2011.

Register Now for Z-DAC Americas in San Antonio

Registration is now open for Zuken's Z-DAC Americas, set for November 8-9, 2011, in San Antonio, Texas. The Early Bird price of \$275 is available until midnight on September 23, 2011. After that, the standard price of \$450 applies, so don't miss out on the savings.

LeCroy Corporation Acquires Bogatin Enterprises

LeCroy Corporation has acquired Bogatin Enterprises, a training company founded by "Signal Integrity Evangelist" Dr. Eric Bogatin. "A key ingredient in our training is leveraging commercially available tools to achieve an acceptable solution faster. LeCroy's signal integrity measurement and analysis products offer a rich source of practical examples," said Bogatin.

Sierra Circuits Exhibits HDI Stackup Planner at Semicon West

Sierra Circuits announced that it demonstrated the latest version of its HDI Stackup Planner software at the Semicon West trade show at the Moscone Center in San Francisco, California last month.

PCB Planet Appoints Parry as North American Sales Rep

Parry commented, "I would not take on an assignment such as this one if I did not believe in it wholeheartedly. I have investigated a lot engineering companies in my career and I can honestly say that PCB Planet is, without a doubt, the best of them all. I am proud to be working with this fine company."

PCI-SIG Developers Conference Wrap-Up

The 2011 PCI-SIG Developers Conference (DevCon) was well attended by representatives of companies developing products with PCI technology, including the latest PCI Express (PCIe) 3.0 architecture, and by the companies servicing these companies as well. This year marked SiSoft's inaugural year as an exhibitor at DevCon.

ASQED Held July 19-20 in Malaysia

ASQED was held on July 19-20, 2011, in Kuala Lumpur, Malaysia. ASQED plays a critical role in promoting quality-based electronic design and manufacturing in Asia. Keynote speakers included Chief Technology Officer Happy Holden of Foxconn Advanced Technology.

AWR Opens Registration for Asian AWR Design Forum

AWR Corporation has finalized event agendas and opened registration for its Asia Pacific 2011 AWR Design Forum. ADF is an open event at which designers of microwave and RF circuit and systems such as MMIC, RF PCB and LTE communication systems can network and share useful information and resources pertinent to high-frequency design.

ANSYS to Acquire Apache Design Solutions

ANSYS will acquire Apache Design Solutions for a purchase price of approximately \$310 million in cash, which includes an estimated \$29 million in cash on Apache's balance sheet. This merger brings a variety of signal integrity tools under one roof; Apache purchased Optimal Corporation in 2007 and ANSYS acquired Ansoft Corporation in 2008.

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Neuralynx looks forward to a continued long and prosperous business relationship with Prototron for years to come.

Barbara Lincoln
Materials Manager
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Bozeman, MT

...and of course the customer is always right!



productronica 2011:

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IN SUMMARY

productronica offers an ideal platform to present products and solutions and to learn about others. The trade fair is also an industry meeting point for acquiring new customers and exchanging information with existing business partners.

productronica is the leading trade fair for innovative electronics production and will be the gathering point for top-tier professionals and specialists from all over the world, November 15-18, 2011, at the New Munich Trade Fair Center. It is the only trade fair in

the world that showcases the entire value chain for electronics manufacturing—from software to process control, from technology to applications and from products to system solutions—under a single roof.

productronica offers an ideal platform to present products and solutions and to learn about others. The trade fair is also an industry meeting point for acquiring new customers and exchanging information with existing business partners.

Statistics and the show's global presence prove its success: productronica 2011 already shows a growth of 15% in exhibition space compared to productronica 2009. The numbers of exhibitors has increased by 15% in comparison to the trade fair in 2009. More than 1,200 exhibitors are anticipated to cover more than 830,000 square feet of exhibition space in seven halls. Forty percent of the exhibitors come from outside Germany. All the

global key players like Nordson Asymtek, DEK Printing Machines, Juki Automation Systems, Speedline and Universal have already signed up, as well as Fuji Machine, Panasonic, Yamaha Motors, Sony, Hitachi and many more. To see a full list of international exhibitors, visit the productronica [Web site](#).

productronica 2011 revolves around newly-developed products, as well as the latest manufacturing technologies and system solutions. It is a unique platform and the perfect place to discover innovative process technologies, as well as important developments in automation, manufacturing technology for PCBs and the sectors for measuring, testing and inspection technology and quality control.

In addition to the full, value-added chain of electronics production, the show will focus on the following highlights:

- **Battery and energy-storage manufacturing and power electronics:**

productronica has extended its product index in 2011 to include the areas of battery production and power electronics. These areas are playing a very important role primarily in the topic of electromobility. In particular, a large number of production engineering challenges still remain unsolved. This topic will be highlighted during the trade fair and will take up a [special show](#) organized in close cooperation with the Productronics Association in the German Engineering Federation (VDMA).

- **Efficient production management:** Efficiency in manufacturing, improved quality and traceability are just a few examples of things that have become possible thanks to efficient production management such as MES, ERP, etc.

- **Electronic manufacturing services (EMS):** Outsourcing in times of anticipated bottlenecks and promising new branches of business are increasing the demands the EMS industry places on productronica. To learn more about these themes, click [here](#).

- **Organic and printed electronics:** This is a developing industry with growth that will become noticeable in the production sector in the future, which is why it needs its own platform at the leading trade show for electronics production.

productronica 2011 is also the perfect meeting place for the PCB industry. As a result, exhibitors and visitors can come together in the redesigned Hall B1, where the [PCB Community Area](#) will be the central hub. The Community Area, which was created especially for the show, is divided into three areas: A speaker's corner, a poster show illustrating the sectors that create added value and a meeting place for discussions at the heart of the industry. productronica's objective is to bring the industry together. As a result, productronica is living up to its reputation as an independent, innovative platform that promotes the success of all market participants.



The show will present everything that sets standards in electronics production in 2011: The sessions in the [productronica Forum](#) and the [Innovation Forum](#) deal with topics that pertain to current market situations and technologies.

For more information, visit the [related-events program online](#).

If you are interested in exhibiting, some space is still available. For details, visit the exhibitor information page [online](#) or contact [Anika Niebuhr](#) at (646) 437-1014.

Planning to visit the show? Get your tickets online and save time when you arrive at the trade fair grounds and avoid lines. Tickets may be purchased by clicking [here](#).

Subscribe to the [productronica newsletter](#) and receive a free day pass. The newsletter will keep you updated about the latest industry news and practical tips to ensure your personal success.

If you are looking for a travel opportunity, an all-inclusive trip is being offered to visit productronica 2011 and the city of Munich, Germany. From November 14 to 17, 2011, we are taking care of everything and offer advantages such as:

- A four-star hotel;
- Admission to productronica and the conference program;
- Dinner at the famous Hofbräuhaus;
- A guided tour through Siemens' production facility; and
- [Business Partner Match-Making](#).

For more information about the trip, click [here](#). For visitor information, call [Sabrina Weimer](#) at (646) 437-1016.

productronica is the leading world trade fair for innovative electronics production and is supported by the Productronics Association



in the German Engineering Federation (VDMA) as a conceptual partner. The event has taken place in Munich, Germany, every two years since 1975 and is a core element of the electronics trade fair network of Munich International Trade Fair. This network includes the leading global trade fairs, electronica and productronica, held in Munich, as well as leading regional trade fairs in Brazil, Hong Kong, China and India. With over 8,000 exhibitors and more than 280,000 visitors, the Munich International Trade Fair is one of the internationally leading trade fair organizers in this segment. For more information, visit [productronica.com/en/home](#).

Messe München International (MMI) is one of the world's leading trade fair companies. The company organizes around 40 trade fairs for capital and consumer goods and key high-tech industries. Each year over 30,000 exhibitors from more than 100 countries, and over two million visitors from more than 200 countries, take part in the events in Munich. In addition, MMI organizes trade fairs in Asia, Russia, the Middle East and South America. With six subsidiaries abroad, in Europe and in Asia, and with 66 foreign representatives serving 89 countries, MMI has a truly global network. For more information, visit [www.messe-muenchen.de/en/Home](#). **SMT**

Video Interview

Critical Cleaning Explained

by Real Time with...IPC APEX EXPO 2011



Barbara Kanegsberg, president of BFK Solutions, discusses key challenges in the cleaning of electronics assemblies. She explains to Editor Pete Starkey the principles of critical cleaning and introduces her latest publications.



www.realtimewith.com

Updated Guidelines for Cleaning of Printed Boards & Assemblies

To help the process engineering community deal with these difficulties, IPC has released the B revision of IPC-CH-65, Guidelines for Cleaning of Printed Boards & Assemblies. With guidance from industry experts, the cleaning guidelines have been completely rewritten and address all facets of cleaning, including material selection, process considerations, equipment selection, as well as the environmental impact of cleaning. The document not only brings cleaning requirements up to date, it also combines multiple documents into a single, comprehensive guideline. IPC-CH-65B explains the interactions between materials and processes and outlines the sources and types of contamination found on today's circuit card assemblies.

The cleaning of printed boards and assemblies has undergone a significant transformation in two decades, due in large part to environmental regulations which are cross-referenced in the document. No-clean fluxes and lead-free solder are among the technical mainstays.

In the coming months, IPC will host two

educational sessions covering IPC-CH-65B. On August 17, 2011, IPC will host a 30-minute Webinar, "How Clean is Clean Enough? Overview of the IPC-CH-65B Cleaning Handbook," at 10:00 a.m. Central time. To register, click [here](#). In addition, a three-hour course, "PD-01 Cleaning Guidelines for Boards and Assemblies: Developing a Successful Process with the NEW IPC-CH-65B," will be held on September 22, 2011 at 1:30 p.m., in conjunction with IPC Midwest Conference & Exhibition, Renaissance Schaumburg Hotel & Convention Center, Schaumburg, Illinois. For more information and to register, visit www.IPCMidwestShow.org.

IPC members may request a free single-user download of IPC-CH-65B, Guidelines for Cleaning of Printed Boards & Assemblies, by sending an e-mail to MemberTechRequests@ipc.org within 90 days of the document's publication date. After that date, IPC members may purchase the standard for \$50. The nonmember price is \$100. For more information or to purchase IPC-CH-65, visit www.ipc.org/CH-65.

Supplier Highlights



Numerical Innovations Releases DFM Now!

DFM Now! allows PCB designers and engineers to verify that their Gerber and Drill files are ready for PCB manufacturing. It also facilitates PCB quotation and has many other high-end CAM features. The product is being offered completely free.

Photo Stencil Introduces New Stencil Technology

Photo Stencil, LLC introduces a new stencil technology, called NicAlloy-XT, for printing solder paste on PCBs. NicAlloy-XT brings to market the best of NicAlloy and electroform stencils. It bridges the gap between traditional laser cut stencils and higher-end electroformed stencils.

Ellsworth Adhesives Names New Engineering Sales Rep

Ellsworth Adhesives is pleased to announce the addition of Sergio Patricio as an Engineering Sales Representative for Ellsworth Latin America Adhesives LTDA. In his new role, Patricio will focus on field sales and technical support to existing and new development businesses in the São Paulo, Southeast and Southern regions of Brazil.

ITW Acquires Teknek

Illinois Tool Works Inc. has acquired Teknek, a world leader in manufacturing contact sheet cleaning and Web cleaning solutions for the electronic and industrial markets. Teknek will be a wholly-owned subsidiary of ITW and will become a part of the company's existing Electrostatics business platform, within the Electronics Group.

Techspray Unveils Eco-Stencil AQ Batch Stencil Cleaner

Designed for ultrasonic and spray-in-air systems, Eco-Stencil AQ batch stencil cleaner offers great cleaning performance with much lower environmental impact. The cleaner effectively removes all types of solder paste (e.g. water-based, RMA, no-clean and lead-free) and uncured adhesives from stencils and misprinted boards.

A-Tek Systems Releases Kolb PSB500 PCB Batch Cleaner

The Kolb PSB500 is a four-step, closed-loop, fully-automatic batch cleaning system and includes both cleaning and rinsing (tap water and DI-water) for ultrafine cleaning tasks, such as PCBs, ceramic substrates, hybrids and misprints in a compact, space saving design.

Electrolube Develops LED Product for European Market

SC3001 is a silicone resin, developed specifically to meet the needs of the LED industry. Currently only available in Australia and China, the product will be officially launched to the rest of the world at productronica, along with the 2000 silicone resin range which includes SC2001, a general potting and encapsulating compound, SC2001FD, a fast cure compound, and SC2003, a thixotropic compound.

Manncorp Unveils BR-810 Split-Vision Rework

The premier model in Manncorp's line of surface mount rework systems, the BR810, is designed for safe removal, precise placement and reliable soldering of the most delicate and sensitive SMD packages found in the industry's most challenging board repair applications.

KEMET Acquires Cornell Dubilier Foil

"This acquisition is a first step in the strategic direction we outlined recently to find opportunities to vertically integrate our operations to better control our supply sources and our cost structure," said Per Loof, Chief Executive Officer of KEMET.

tbp electronics Invests in DEK Horizon 03iX Screen Printers

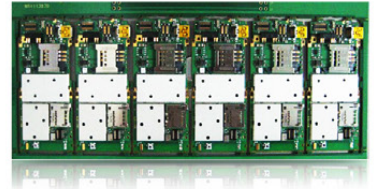
DEK has confirmed that tbp electronics has purchased three of its Horizon 03iX screen printing platforms to drive progressive manufacturing processes for high-end customers. As a leading supplier of EMS in the Benelux region, tbp electronics has adopted DEK mass imaging technologies to help deliver EMS solutions for key industries including medical, petrochemical, safety and test.

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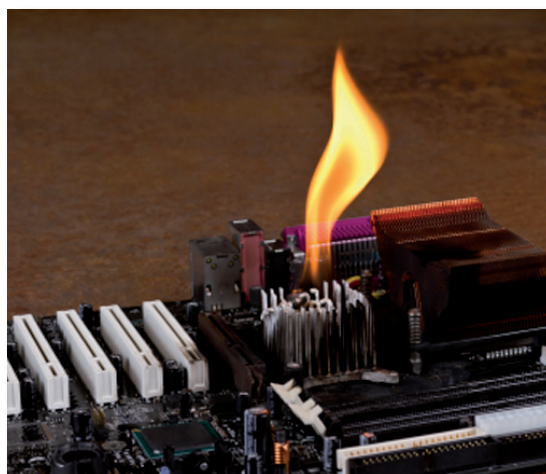
Thermal Simulation of SMT Components in High-Temperature Applications

by Craig Hunter

VISHAY INTERTECHNOLOGY

Surface-mount components are used in every environment imaginable and are exposed to many different extreme elements that can impact their performance, from high vibrations to moisture. But the most common extreme they encounter is high temperature. This “harsh environment” is often in remote locations or critical applications where reliability is critical. Good examples are oil exploration and drilling sensing systems, mining, automotive and aerospace electronic systems. But elevated temperatures are also seen in other applications like industrial control systems and equipment which may be exposed to direct sunlight like smart meters. In these applications, component failure or even the failure to achieve required performance levels can be extremely costly, and in some cases very dangerous as well. Fortunately, the industry has responded with a wide variety of surface-mount components that not only operate at higher temperatures, but also perform effectively and reliably.

Under-the-hood automotive electronics reliability is one significant market expansion. Customers (and, therefore, car manufacturers) demand high quality levels, which have become a key metric for prospective purchasers



IN SUMMARY

In high-temperature applications, component failure or even the failure to achieve required performance levels can be extremely costly, and in some cases very dangerous as well. Fortunately, the industry has responded with a wide variety of surface-mount components that not only operate at higher temperatures, but also perform effectively and reliably.

of vehicles. Component manufacturers have developed parts for use in ECUs and other control and sensing systems. For example, AEC-Q101 qualified n- and p-channel power MOSFETs are available for automotive applications with maximum junction temperatures to + 175°C and thermal resistance as low as 1.5°C/W. For voltage regulator module

(VRM) and DC-to-DC applications, SMD power inductors have been introduced that combine high operating temperatures to + 200°C with very high current ratings.

For a wide range of operating conditions, these devices also handle high transient current spikes without hard saturation and offer high resistance to thermal shock, moisture, mechanical shock and vibration. Inductors combining these attributes with torroidal designs are available for applications where EMI is also a concern.

Typically, tantalum molded chip capacitors are only available with standard operating temperatures of + 150°C or + 175°C. However, to provide designers with a less expensive and more reliable option for high-temperature applications, devices have been recently introduced that offer 500 hours of continuous operation at + 200°C, without the need for voltage derating. For even higher

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temperatures, where wet tantalum capacitor assemblies or arrays are required, the industry offers operating temperatures to + 220°C.

Ideal for oil exploration and drilling systems, thin and thick film chip resistors and networks feature operating temperatures to + 230°C. For increased reliability in these applications, such devices provide load-life stability as low as < 1% after 1,000 hours at + 220°C, and storage temperatures as high as + 245°C. Solid aluminum capacitors are also available with high-temperature ranges to + 175°C and very long useful life of 20,000 hours at + 125°C.

For accurate surface temperature measurement over a wide temperature range from -40°C to +125°C, negative temperature coefficient (NTC) thermistors are offered with a tiny mounting space of 65 mm²/0.1 in², and ultra-fast response time of < 4 s. Select thermistors offer designers a choice of electrical resistance values at + 25°C (R_{25}) to meet the self-heating, voltage output or noise suppression needs of their particular application.

It's clear that there's no shortage of components that meet the stringent requirements of high-temperature applications. However, designers also need help in understanding how these components will hold up in their actual application. Here,

again, the industry has responded with several useful tools. One such example is the free ThermaSim online thermal simulation tool on Vishay's [Web site](#). ThermaSim helps designers speed time to market by allowing detailed thermal simulations to be performed before prototyping. ThermaSim allows designers to define other heat-dissipating components and simulate their effect on the MOSFET's thermal operation. Simulating these components ensures optimum device selection for application specifications and eliminates fallouts during thermal-performance line testing. For increased accuracy, the simulations use structurally detailed power MOSFET models created using finite element analysis (FEA) techniques.

With such tools at their disposal, designers have everything they need to ensure the best design and reliability for their high-temperature application. **SMT**



Craig Hunter is Director, Global Internet Marketing at Vishay Intertechnology Inc. He may be contacted at craig.hunter@vishay.com.

Nordson Enters Agreement to Acquire Value Plastics

Nordson Corporation has entered into a definitive agreement to acquire Value Plastics, Inc., a leading designer and manufacturer of precision engineered, plastic molded, single-use fluid connection components used primarily in critical flow control applications for healthcare and medical device markets. Headquartered in Fort Collins, Colorado, Value Plastics employs approximately 75 people. The transaction is expected to close during Nordson's fourth fiscal quarter.

Nordson President and CEO Michael F. Hilton said, "Value Plastics supports Nordson's strategic objective of building upon our medical and life sciences platform and complements our existing growing positions in biomaterial delivery devices

and medical device assembly. Value Plastics is an ideal addition to the Nordson portfolio, where our global reach and infrastructure will provide opportunities to leverage the business' profitable growth beyond its primary domestic markets served and into general industrial markets."

The \$250 million purchase price, subject to adjustment as provided in the purchase agreement, will be financed with availability under an existing \$400 million revolving credit facility. The transaction is expected to be accretive to Nordson's earnings in the first full year of acquisition.

Additional information can be found at www.nordson.com.



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Auditing PCB Assembly Capability of OEMs or EMS Companies: Asking the Right Questions, Part 2 – Manufacturing & Technology Questions

by Ray Prasad

RAY PRASAD CONSULTANCY GROUP

In my [July column](#), I discussed the overview of an audit process to assess the manufacturing capability of OEMs or EMS companies. In this column, I'll focus on the technology and manufacturing capabilities of the supplier. I will conclude this series with questions on quality and RoHS compliance in an August column.

Even though I am dividing the questions into various areas, namely technology, manufacturing, quality and RoHS compliance, overlaps will occur. However, it is not important which category these questions fall into, but rather the fact that they should be asked. These questions are intended to help generate discussions that are relevant to your product and the manufacturing site you plan to audit.

Manufacturing-Related Questions

Many business-related questions are aimed at determining the supplier's financial stability, long-term viability as a business, pricing policy and quality standard to be used. These questions should be asked. You should also ask about the production capacity of the line and the percentage of that capacity available for your products to see if there is a match. We are not covering these areas in this series

IN SUMMARY

How do you go about assessing the manufacturing capability of a company? In Part II of his column, industry expert Ray Prasad continues his overview of a detailed audit process.



of columns, but for some ideas on questions in this area, see Reference 1.

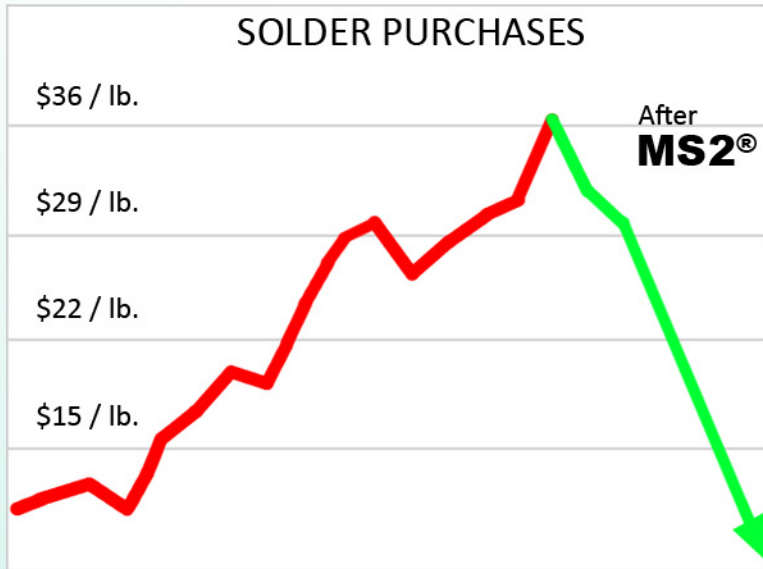
Begin by asking about the types of components used in various products being built by the company today and the level of defects (PPMO and First Pass % Yield) in those products. The answer to just this one question will give a good general overview of the assembler's capability.

Ask the supplier to check the types of packages and their pitch being used in the products they are currently building. Here are some examples:

- Types of through-hole components being used;
- Smallest components 0402, 0201, 1005;
- Resistor Networks with fine-pitch pads (0.4 mm pitch);
- BTCs such as QFN, DFN, LGA;
- QFP with 0.4 mm and 0.3 mm pitches;
- CSP/BGA with 0.5 mm pitch;
- CSP/BGA with lower than 0.5 mm pitch;
- Maximum BGA I/O count;
- Package-on-package (PoP);
- Others (make a list).

The type of package and their pitches play a key role in the level of defects. For example, based on a recent study (Reference 2), here is

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a brief summary of defects you can expect for different types of packages:

- Plated through-hole (PTH) – 4,000 PPM;
- Gull wing – 1,400 PPM;
- Chips, BGA, J-lead – Around 600 PPM; and
- Average of all types – 1,079 PPM.

What is noteworthy in this study is that through-hole components caused the highest level of defects. This should not be a surprise since the most common process for soldering through-hole components is wave soldering, which has too many variables to control. Since through-hole is not going away for a long time, even though their number has dwindled drastically, you or your supplier may want to consider automated selective soldering for PTH to reduce PTH defects.

In the same study, the author found that the type of lead and their pitch plays an important role in defects:

- 16 mil pitch (0.4 mm) – 13,088 PPM;
- 20 mil pitch (0.5 mm) – 1,878 PPM;
- 25 mil pitch – 950 PPM; and
- 50 mil pitch – 650 PPM.

When pitches get below 0.5 mm, the defect levels really skyrocket. So if you cannot avoid 0.4 mm pitch, you need to really focus on the manufacturing capability of your supplier to successfully deal with fragile leads of ultra-fine-pitch packages. Put another way, if your product contains pitches below 0.5 mm, there are very few companies who can build them with good quality on a consistent basis. So your audit process needs to be much more rigorous if you need to assemble ultra-fine-pitch components.

There is no such thing as a perfect PCB

surface finish. All surface finishes, such as HASL, OSP, ENIG, immersion silver and immersion tin, have their pros and cons. In most cases, the assembler does not make his own PCB. He orders them from a PCB supplier. An assembler who is a turn-key supplier is responsible for selecting his own PCB supplier. On the other hand, if you specify the surface finish, you should be asking the same questions from the PCB supplier.

Here are some examples of questions that should be asked about different surface finishes being used on your product:

For ENIG surface finish: Did you ever have black pad incidence? How was it resolved? Very few suppliers are willing to admit the problem, but black pad is a potential problem with ENIG and you should ask about it.

For immersion silver: Ever had champagne microvoid incidence? If so, how was that resolved?

For OSP: Ever had BGA ball drop incidence? Any issue with via fill during wave soldering of mixed assembly? Did you have to use a more active flux or nitrogen to achieve 100% via fill? Even though only 75% via fill is required, if you always get that minimum (75%), it is not an acceptable quality.

For HASL: Since the inherent problem with this finish is uneven surface finish, it is really worth asking if the supplier has successfully used HASL for BTC, BGA or fine-pitch packages. Very few people can make that claim and that was the reason for moving away from

HASL in the first place. It was not too long ago that the predominant surface finish was HASL. In addition to getting uniform solder coating with HASL, board warpage may also be an issue. For most companies using finer pitches, BGAs and BTCs, HASL is really not an option.

There is no such thing as a perfect PCB surface finish. All surface finishes, such as HASL, OSP, ENIG, immersion silver and immersion tin, have their pros and cons.

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TECHNOLOGY

Test, Assembly & Packaging TIMES

Because of availability constraints, many companies end up using both tin-lead and lead-free components on the same board. Such assemblies fall into what is commonly known as “forward” or “backward” compatibility scenarios. The key concern is selection of the right peak reflow temperature since the tin-lead and lead-free components require very different peak reflow temperatures for proper reflow. So the key question is how does the assembler deal with tin-lead and lead-free BGAs on the same board? What peak temperature is used to prevent over heating of tin-lead BGAs/QFPs without compromising proper reflow of lead-free BGAs? What reflow peak and TAL do you use when most of your components are tin-lead, but the BGAs are lead free?

Handling and control of moisture-sensitive components and tracking of their exposure times is another issue that is worth digging into since very few companies do it correctly. What is the handling procedure to prevent baking (when exposure time has expired) of moisture-sensitive BGAs? How many times do you bake moisture-sensitive components? (Note: Only once is allowed.)

It is not easy to detect the seriousness of defects in a company during the course of a short audit. But finding the ratio of bridging to opens over last six months can give you a good idea about the extent of field failures you may see. About six times more shorts than opens is a good sign since there is practically zero chance that shorts would escape any inspection or test. Opens, on the other hand, can easily escape the inspection and test and will come back to haunt you after a relatively short time in the field.

It is also important to ask about the test strategy (ICT, flying probe, functional, etc.) used on the product, especially when you see

a large bone pile on the shop floor. Large bone piles are common in companies that do not use ICT and have high defect rates.

Technology Questions

The types of machines used by a company are important. The existence of a detailed and formal design and process document, and an extensive training program for operators, technicians and engineers, are the key

elements of a strong SMT infrastructure. You should ask about the number of engineers working on manufacturing process development and on the production floor and their qualifications.

The same questions should be intended to assess their understanding

of the technology. For example, you should ask about the properties of solder paste (compositions, metal content, particle size range, etc.) to see if they have been selected for a reason. What is the solder application method (stencil or screen)? Why was this method chosen? What is the paste deposit thickness? Does this thickness requirement change if fine pitch is used on the same board? What is the approach (differential stencil thickness versus micro modification of stencil aperture) for applying paste on a board with standard surface mount and fine pitch? Have they looked into the implications of each approach? Do they get heel fillet in fine pitch without getting insufficient fillets in standard components?

What is the reflow soldering method used (vapor phase, infrared, convection or combinations thereof)? What are the typical thermal profiles on the board surface and at a solder joint? Do they develop a unique profile for each board? How and where are the thermocouples attached? Are they attached on surface or on the solder joints? Is the board drilled to attach thermocouples to the BGA

“It is not easy to detect the seriousness of defects in a company during the course of a short audit. But finding the ratio of bridging to opens over last six months can give you a good idea about the extent of field failures you may see.”

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balls on the outer and inner layers? If not, how do they know if the BGA balls really reflow? Have the reflow processes been compared for manufacturing yields?

What cleaning method and solvents are used? How is the cleanliness of product board monitored? What sort of repair/rework equipment is used and what are the thermal profiles for repairing each surface-mount device type?

To determine if the company has any experience or plans to develop capabilities for newer technologies, such as BTC, BGA and ultra-fine-pitch packages (if your product requires them now or in the future), you should ask detailed questions related to that technology. For example, are you planning to achieve toe/side fillets in BTCs? How? How to do you ensure you get sufficient paste thickness to prevent potential opens without getting too many voids? How do you prevent paste dripping into via holes in thermal pads?

What do you see as the major concerns in PBGA and how do they compare to PQFP? What is their experience with head-in-pillow? If you are doing all you can about paste height, reflow profile, and do you think component supplier is responsible for head-in-pillow?

Do you prefer copper-defined pads or solder mask defined pads? Why? What do you think of approach used by some companies where solder mask is sprayed up to the edge of the pad with zero clearance? Do you prefer via-in-pad or tear-drop design? Why? Did you conduct any evaluation on PCB routing for different pitch, pad sizes, line width/space, etc., and their impact on layer count? Did you experiment with different sizes of pads and their impact on process yield?

The idea behind these questions is to establish whether the company has performed extensive process evaluation and whether or not the company understands the importance of critical materials and process variables on product quality and reliability. It will be obvious within a very short time during the visit if there is someone in the company who understands these issues or if they are just following the recommendations of component and material suppliers. How many suppliers

do you know who build PCBAs? How useful would their recommendations be?

The intent of these questions is not to dictate the process to the company, but to assess its understanding and capability. You should focus mainly on end requirements. Let the assembler worry about how best to meet those requirements—you are simply trying to establish whether they can meet your requirements. **SMT**

References

1. Ray Prasad, "Surface Mount Technology: Principles and Practice," 2nd Edition, Chapter 2.
2. Stig Oresjo, Agilent Corporation, "Year 1999 Defect Level and Fault Spectrum Study," SMTAI 2001 proceedings.



Ray Prasad is the founder of Ray Prasad Consultancy Group which provides education, consulting and technical expert services in tin-lead and lead-free technologies using SMT, BGA, BTC, fine-pitch and through-hole components. He provides factory and process audits, including RoHS compliance services, and also offers SMT and lead-free/RoHS training courses in Beaverton, Oregon, and at client sites around the globe.

Author of the textbook "Surface Mount Technology: Principles and Practice" and over 100 papers, Prasad holds two patents in BGA and is a popular workshop leader for in-depth SMT, BGA/CSP and lead-free professional courses.

Prasad will be teaching "Design and Manufacturing with SMT-BGA-BTC in a Sn-Pb & LF World" on October 10-12, and "Auditing PCB Assembly Capability & RoHS Compliance of OEMs and EMS Companies" on October 13. For details, click [here](#).



IPC EXECUTIVE SUMMIT: Management Meetings and Market & Technology Conference

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- How to prepare for supply chain disruptions
- How the ban on conflict minerals will impact the industry
- What trends in the global business outlook mean for your company
- How the semiconductor industry is driving new OEM requirements for interconnect suppliers
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China... It's Not a War, Just a Battle

by Barry Matties
I-CONNECT007

Some say we are at war, an economic war, with China. Because they feel we are at war, some critics are very angry that American engineers are over there training the “enemy” to take technology, jobs and the economy away from the U.S. Others would say that is not a war, but rather more of a battle where no human lives are lost—a battle of economic consequences. Certainly many lives have been impacted as a result of this economic battle.

It seems to me that there is a natural order of things and the rise and fall of nations is all part of the order. There is no doubt that America has gone backward on many fronts. Our deficit spending is out of control, the job situation continues to be weak, housing markets are still down, salaries are down and there's no real solution in sight. More taxes, less taxes, hard cuts, soft cuts, new leadership, old leadership—these are just some of the ongoing conversations in the nightly news. The result of all this uncertainty is that it makes it hard for business leaders to hire, or even invest, for the future.

During our turmoil we hear about the steady rise in China's prosperity. Once again, many will say the prosperity is through theft,



IN SUMMARY

Some viewing our current job situation would say that it not a war, but, rather, more of a battle where no human lives are lost—a battle of economic consequences. Certainly many lives have been impacted as a result of our economic battle we have with China.

imitation, patent infringement and the willing transfer of knowledge from American and other country's engineers and managers. Of course, a low wage-earning nation does not necessarily start out with the management or engineering skills, so the foreigners relocate, buy houses and start training their new work force. The core of this is the consumer's desire

for the highest quality products at the lowest possible cost. It's a trap.

If we want to pay less we must lower the cost of producing the product. To do that, our answer was to go find cheap labor and set up factories to take advantage of such labor. The result is lower prices to the consumer. While consumers are enjoying lower prices, they are also losing their jobs. Not in an instant, but over the course of years. Couple all this with America's voracious appetite for short-term profit, at any cost, and you find America sitting exactly where it is, stuck in deficit spending, a weak job market, equity stripped out of the housing market and a slow and questionable recovery from a recession of historical impact. So are we just hanging on to the crumbs?

One thing that is surprising is how fast solar manufacturing has been moving to China. With a core central strategy of



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education and manufacturing, China is the world's largest supplier of solar panels. So does this mean our dependence on foreign oil from the Middle East will be supplanted by a new dependence on green energy from China? They are, after all, the largest consumer of energy and the low-cost producer of manufactured goods.

So what does all this mean? Well, if you are an engineer looking for a job, but discovering that no one in America is willing to hire you or that your industry has moved to China, should you retrain and find a new job managing a restaurant, or do you move abroad and continue work in your chosen field? Many U.S. workers don't even have that choice. When we look at our unemployment numbers here in America, it is clear to see that getting a job can be difficult at best right now.

In fact, some people have been unemployed for so long that their only hope of getting a job is to retrain, and even then there are still no guarantees. Should we be angry at the engineers for being overseas, or should we wake up and realize we are in a global market with more advanced nations than ever before? Not only are there more of them, but emerging nations are transforming at a historic, rapid pace. In a global market you have to be willing to take a global job. For the ones that are angry at the engineers, stop complaining and realize that these people are trying to take care of their families and are still contributing to world

development. If an equal job was available in America, my guess is they would take it.

I think if I were to be angry at anything, it would be the lack of importance America places on education and infrastructure. The greatest national resource we have is our people and their bright minds. We must change the educational system here in America. More of our graduates, at all levels, need a higher level of knowledge. That is where the power of change, growth and prosperity is. We may be a generation away from the results of a new educational standard, but it will be worth it.

In conjunction with education we must focus on infrastructure. The need to smartly modernize our power grids, transportation, communication and other systems are at a peak. When kids come out of college in China there are jobs waiting for them; when kids come out of school in America, finding a job is proving to be very difficult.

We have all heard or discussed the issues I've mentioned here, but now we must act on it. It is time to get rid of politicians, bureaucrats and any other obstacles that stand in the way of rebuilding our nation from the ground up. It took us many years to get where we are and it will take many years to rebuild, but it can be done. **SMT**



Barry Matties started in PCB manufacturing in the early 80s. In 1987, he co-founded *CircuiTree Magazine*. Nearly 13 years later, *CircuiTree* was sold as the leading publication in the industry. In the early 2000s Barry and his former *CircuiTree* partner, Ray Rasmussen, joined forces again and acquired PCB007. Over the years, PCB007 has grown and continues to thrive. In July 2010, Barry and Ray acquired *SMT Magazine*. With his many years of business leadership skills, Barry now produces this column for anyone who has a desire for success. The column relates 25 years of successful business leadership, including marketing and selling strategies that really work. Read a few and decide for yourself.



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TOP TEN

SMTonline
News

Most-Read News Highlights from SMTonline this Month

① **Revised EU RoHS Directive Published**

"IPC has advocated over the past two years that any changes to the RoHS Directive be underpinned by a solid scientific examination," says Fern Abrams, IPC Director, Government Relations and Environmental Policy. "Due to IPC's aggressive lobbying efforts, the revised RoHS Directive does not restrict any additional substances."

② **IPC Midwest to Focus on Solutions to Industry's Challenges**

IPC Midwest will feature an exhibition with the industry's top suppliers, showcasing the newest products, processes and emerging technologies in all major categories. Admission to the exhibit floor is free to all who register by September 16, 2011. Attendees can shop and compare equipment and processes for their unique needs all under one roof, saving time and travel expenses.

③ **Even with Fine Pitch, Rework Can Keep Production Running**

The wide diversity in package types can often mean that companies end up with components that don't have the right type of solder balls. Problems arise when purchasers can't get the desired parts in packages that contain the type of solder they need: Lead-based for military applications or lead-free for consumer products.

④ **Flextronics, Sanmina-SCI Tap Into Clean Energy**

Flextronics and MEMC Electronics Inc. have extended their agreement to continue making solar panels for an MEMC subsidiary. Sanmina recently announced a partnership with Sparq Systems Inc. to manufacture micro-inverters and communications hubs for solar photovoltaic systems.

5 IPC Midwest to Hold First Annual Hand-Soldering Competition

IPC announces the first annual IPC Midwest Hand Soldering Competition, September 21-22, 2011, at the Renaissance Schaumburg Hotel and Convention Center, Schaumburg, Illinois. The contest will pit competitors against each other to build a functional electronics assembly within a 30-minute time limit.

6 iNEMI: Book on Lead-Free Solder Process Development

The International Electronics Manufacturing Initiative (iNEMI) is pleased to announce the recent publication of Lead-free Solder Process Development, by Wiley-IEEE Press. Several iNEMI project leaders and participants were involved with this book, which is an important reference guide for engineers in the electronics manufacturing industry that are, or will be, migrating to lead-free soldering.

7 NEPCON South China Highlights Entire Manufacturing Chain

NEPCON South China 2011, August 30-September 1, 2011, will give trade professionals numerous opportunities to find new manufacturing solutions and assess the latest technologies. Attendees also will be able to expand their networks onsite with new and existing suppliers to maintain a competitive edge.

8 Jabil's Q3 Revenue Growth Exceeds Expectations

"Revenue growth was stronger than expected for our third quarter," said Timothy L. Main, President and CEO. "We are pleased to demonstrate continued growth above our long-term targets. As a result, Jabil is poised to deliver record revenue and earnings in fiscal 2011."

9 Indium's Bastow to Host Webinar on Flux Reliability

Indium Corporation Senior Technical Support Engineer Eric Bastow will present his IPC APEX Expo 2010 and 2011 technical papers as part of IPC's Summer School Webinar series on Wednesday, August 10, 2011, 10:00 to 11:00 a.m. CST. Barstow will present "Effects of Flux Residues on Reliability" and "Understanding SIR."

10 Photo Stencil Introduces New Stencil Technology

Photo Stencil, LLC introduces a new stencil technology, called NicAlloy-XT, for printing solder paste on PCBs. NicAlloy-XT brings to market the best of NicAlloy and electroform stencils. It bridges the gap between traditional laser cut stencils and higher-end electroformed stencils.



SMTonline.com

EVENTS

For the IPC's Complete Calendar of Events, click [here](#).

For the SMTA Calendar of Events, click [here](#).

For the iNEMI Calendar, click [here](#).

For a complete listing of events, check out SMT Magazine's full events calendar [here](#).



IPCA Expo 2011

August 3-5, 2011
KTPO Trade Centre, Bangalore, India

NEPCON South China

August 30-September 1, 2011
Shenzhen Convention & Exhibition Center,
Shenzhen China

EMPC 2011— European Microelectronics & Packaging Conference

September 12-15, 2011
Brighton Metropole, Sussex, England

Capital Expo & Tech Forum

September 13, 2011
Laurel, Maryland

electronica & productronica India

September 13-16, 2011
Bangalore, India

Advancements in Thermal Management 2011: A Symposium for Design Engineers and Product Developers

September 20-21, 2011
Nashville, Tennessee

IPC Midwest Conference & Exhibition

September 20-22, 2011
Schaumburg (Chicago), Illinois

AeroCon

September 20-22, 2011
McCormick Place North, Hall B, Chicago, Illinois

Long Island SMTA Expo and Technical Forum

September 21, 2011
Islandia, New York

RFID Europe 2011

September 27-28, 2011
Cambridge, UK

MD&M Online West

September 28-29, 2011
Online



PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

PUBLISHER: **RAY RASMUSSEN**
(916) 294-7147; ray@iconnect007.com

SALES MANAGER: **BARB HOCKADAY**
(916) 608-0660; barb@iconnect007.com

EDITORIAL:
GROUP EDITORIAL DIRECTOR: **RAY RASMUSSEN**
(916) 294-7147; ray@iconnect007.com

MANAGING EDITOR: **HOLLY COLLINS**
(252) 288-5118; holly@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

EDITORIAL ADVISORY BOARD:
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MAGAZINE PRODUCTION CREW:

PRODUCTION MANAGER: **SHELLY STEIN**

shelly@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **SHELLY STEIN, BRYSON MATTIES**

INNOVATIVE TECHNOLOGY: **BRYSON MATTIES**

COVER ART: **SHELLY STEIN, BRYSON MATTIES**

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Next Month in SMT Magazine

The supply chain is the life force of the industry. Managed properly, the supply chain can help a company reduce costs, streamline organization and efficiently manage materials. The September issue of SMT Magazine will highlight all aspects of the supply chain: Management, MRP, supplier selection, total cost of ownership and more.

We'll feature articles from these industry experts: Susan Mucha of Powell-Mucha Consulting; Mark Medlen of Riverwood Solutions; Sjef van Gastel of Assembleon; Ray Prasad of Ray Prasad Consultancy Group; John Mayes of Paragon; an interview with Della Systems; and many, many more.

If you're not yet a subscriber, don't miss out! Click [here](#) to receive SMT Magazine in your inbox each month.

See you in September!