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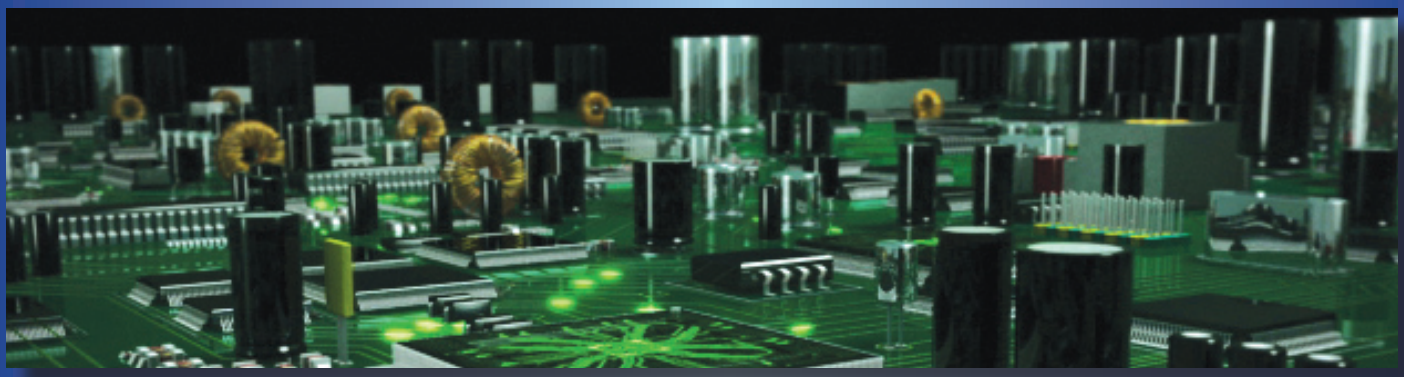

ADVANCED PACKAGING TECHNOLOGY

Welcome to the June 2011 issue of SMT Magazine

This mid-year edition of SMT focuses on advanced packaging technology. Once only found in the most bleeding-edge assemblies, stacked packages, WLCSPs, SiPs and FBGAs are finding their way onto an ever-increasing number of mainstream applications.

If you're not working with these packages yet, you will be soon. As you'll see, demand for some of these packaging systems is expected to double over the next few years, so now is the time to double down and learn everything you can about these tricky little devices.

Sandra Winkler of New Venture Research gives us a glimpse of the future of advanced packaging in the feature article IC Packaging Continues to Blossom. This feature breaks down each of the newest packaging types, and details the effects that smart phones, tablets and DVD drives may have on packaging technology.

Nothing in electronics assembly happens in a vacuum. In Advanced Packages Change PCB Landscape, Zulki Khan of Nexlogic Technologies explores the difficulty of using traditional inspection and testing methods with advanced packages that are nearly impossible to detect and often lack gull wings or leads for testing.

Lead-free usually means higher temps and greater stress on the PCB. But Brook Sandy, Edward Briggs and Dr. Ronald Lasky of Indium believe bismuth is a viable, low-cost, low-temp alloying option. In the Bismuth-Based Alloys for Low-Temp Lead-Free Soldering and Rework, these experts walk us through the results of a Hewlett Packard test study.

In JISSO International Council Celebrates Global Standardization Progress, industry veterans Dennis Fritz and Joe Fjelstad provide an update on the Jisso International Council's 12th annual meeting.

Publisher Ray Rasmussen's column Rare Earth Metals—What's Going On? discusses these not-so-rare metals that are vital to electronics manufacturing. With the Chinese monopoly of these metals driving up prices, what's to stop us from reopening old mines in the Western US, or seeking alternative metals?

And in his column NEPCON China Review, Barry Matties gives us a first-person look back at one of the biggest assembly shows of the year, as well as a rundown of the SMT China Vision Award winners. Find out why the deals on the show floor were non-stop and the energy palpable—and loud.

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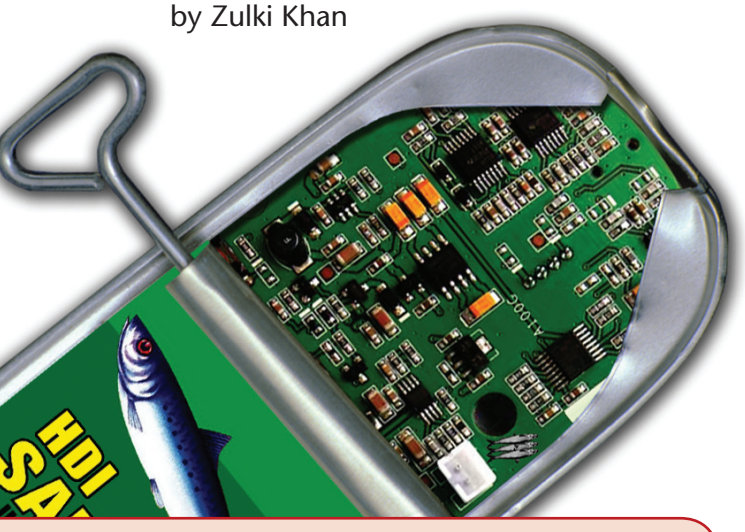

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Rare Earth Metals—What's Going On?

IN SUMMARY

Rare earth elements or metals (REMs) aren't rare, just difficult to obtain due to governmental restrictions and environmental and cost concerns. Ray Rasmussen takes a look at China's restrictions, new mining efforts underway in the U.S. and possible alternatives to REMs.

by Ray Rasmussen
I-CONNECT007

In a nutshell, rare earth elements or metals (REMs) aren't rare. They're actually abundant and found all over the earth in just about every country. The term "rare-earth" is a hangover from the 19th century. Here's a better explanation.

From Wikipedia

The International Union of Pure and Applied Chemistry (IUPAC) defines rare earth elements or rare earth metals as a set of seventeen chemical elements in the periodic table, specifically the 15 lanthanoids plus scandium and yttrium. Scandium and yttrium are considered rare earth elements since they tend to occur in the same ore deposits as the lanthanoids and exhibit similar chemical properties.

Despite their name, rare earth elements (with the exception of the radioactive promethium) are relatively plentiful in the Earth's crust, with cerium being the 25th most abundant element at 68 parts per million (similar to copper). However, because of their geochemical properties rare earth elements are typically dispersed and not often found in concentrated and economically exploitable forms known as rare earth minerals. It was the very scarcity of these minerals (previously called "earths") that led to the term "rare earth." The first such mineral discovered was gadolinite, a compound of cerium, yttrium, iron, silicon and other elements. This mineral was extracted from a mine in the village of Ytterby in Sweden; many of the rare earth elements bear names derived from this location.

From an IEEE Spectrum interview on rare earth metals/minerals, Steven Cherry talks with Thomas Graedel about a paper he recently presented on the subject. Graedel, a geology professor at Yale, said the following when asked why we don't just mine more of these metals, since they aren't so rare:

"The first problem, I think, is that nature is a bit whimsical in how it has deposited the materials, and we have some that are deposited in minable form only in one or two or three places worldwide. Platinum, for example, is essentially only available from South Africa and much smaller amounts in Russia and much smaller amounts again in Canada, and no other country has minable deposits. So, basically, the deposits are one limitation. Another is that many of the elements—indium and tellurium, for example—are minor trace constituents of the actual metals that are

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mined. We don't mine indium. We mine zinc and hope that we can recover the indium as a low concentration by-product."

As mentioned above, if you can't find significant "pockets" of these elements, the cost of mining smaller quantities, which includes typical environmental concerns around mining metals and separating them from other materials, becomes cost-prohibitive.

Of course, many national security issues surround these metals. Since not all metals are found in every part of the world, countries have to cooperate, which could be a good thing on one hand; but, as we saw recently with China's restrictions on the export of their REMs, countries don't always want to work together. And, since 95% of the REMs come from China (they have 36% of the world's known reserves, the U.S. only 13%), the U.S. Congress is working to reinvigorate U.S. efforts to expand our reserves of these metals.

What do we use REMs for? *Popular Mechanics* published a piece on 4 Rare Earth Elements That Will Only Get More Important. The article will help you gain a better understanding of the importance of these metals. The metals of concern are used in electronic products, PV solar and batteries. Lithium is one of the popular ones we hear about used in batteries to power our mobile devices.

So, where does the U.S. stand with regard to REM deposits? According to the U.S. Geological Survey, the United States has 12 million metric tons located in significant deposits in 14 states. There's actually more than that, but it's harder to obtain for the reasons mentioned earlier.

Why is China Restricting Exports?

China claims it's just doing what other nations have already done, which is to develop a strategic reserve of these hard-to-find metals. And, since much of the developed world has opted to purchase their rare elements from China over the last decade, China thinks it's time for those countries to step up and produce their fair share. To develop its industry, China has been selling REMs at bargain-basement prices, which has shuttered most U.S. operations. Now, that's about to change.

Alternatives to Rare-Earths?

China's monopoly of REMs and export restrictions has fired up labs all over the globe as governments, universities and industries work to create new materials with similar properties. An article in MIT's *Technology Review* looks at a few of the efforts underway to develop alternatives. In the long run, it looks like these efforts, along with renewed mining, will be able to replace most of the REMs from China and possibly lead to new discoveries going forward.

It would seem that market forces are more in play here than natural forces. Since the Chinese announcement that they would restrict exports last year the price of REMs has skyrocketed, creating a new interest in mining. Since we have significant reserves, the laws of supply and demand will take over. We do hear and read about new mining efforts underway in the Western U.S. to revive old mines and exploit new discoveries. I would say, from what I've been reading, the concern over these metals is short-lived as government and industry tackle this problem. In the long run, the rest of the world will continue to develop their own REMs, or, alternatives leading to a more diverse and stable supply of these not-so-rare metals. **SMT**

Visit the links below for the latest news on REMs from SMTOnline:

Defense Bill Calls for a Competitive, Multi-Source Rare Earth Inventory Plan

iNEMI: Rare Earth Metals Assessment, Supply Chain Action

China Announces New Caps on Rare Earth Production

Ray Rasmussen is the publisher and chief editor for I-Connect007 publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuiTree Magazine*. Ray can be contacted at: ray@iconnect007.com

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IC Packaging Continues to *Blossom*

by Sandra Winkler
NEW VENTURE RESEARCH

IN SUMMARY

IC shipments grew 28.9% from 2009 to 2010. The prevalence of ICs in our daily lives, keeping us connected all the time, will continue to show an annual increase, but a slower growth, of 7.52% CAGR from 2010 through 2015. Unit shipments of ICs will be 267,811 million in 2015. Sandra Winkler takes a look at the future of ICs.

The year 2010 was a banner year for the semiconductor industry, pulling out of the Great Recession of late 2008 to early 2009 much faster than other industries. Hand-held gadgets, from smart cell phones to tablets, are the primary drivers behind this recovery; the auto industry is also on an uptick. A few select end products are listed in Table 1.

Tablets are new to the market and, thus, have low unit figures. However, the compound annual growth rate (CAGR) of 59.8% is impressive enough to make one take notice. Smart phones also have an impressive growth rate of 15.2% for the years 2011 through 2015. And the hard disk drives, CD/DVD drives and flash drives are just simply large markets. All this information points to a healthy market for ICs in the future.

IC shipments grew 28.9% from 2009 to 2010. The prevalence of ICs in our daily lives, keeping us connected all the time, will continue to show an annual increase, but a slower growth, of 7.52% CAGR from 2010 through 2015. Unit shipments of ICs will be 267,811 million in 2015. Approximately 68% of these shipments are leadframe-based throughout the forecast period.

With this industry having its cycles every four years (a downturn or softening of the market the first year of a new president in the United States), 2013 will see a tapering of growth rates to only 4.8% that year.

	2010 Units (M)	2015 Units (M)	CAGR
Notebook PCs	200	300	8.4%
Tablets	12	125	59.8%
Hard disk drives	450.6	645.9	7.5%
CD/DVD Drives	361.3	440.6	4.0%
Flash Drives	400	535	6.0%
Cell phones	1,302	1,954	8.5%
- Smart phones	205	416	15.2%
- Dumb phones	1,097	1,538	7.0%

Table 1.

After a revenue growth of 31.3% from 2009 to 2010, the CAGR for IC revenue will be 7.42% for the years 2011 through 2015. Revenue for these chips will grow from $249,911 million in 2010 to $357,413 million in 2015. This is still quite healthy, although slightly behind unit growth.

The total package assembly revenue was approximately $38.5 billion in 2010, which is predicted to expand to $57.1 billion by 2015. Package assembly revenue growth will be at an 8.18% CAGR through 2015, ever so slightly ahead of the total IC revenue growth of 7.42%.

The Role of Packaging

Packaging of these ICs is important, as the package holds the footprint to the PCB, and can either facilitate or hamper the speed and performance of the chip. Attachments to the package, such as heat sinks, must also dissipate the heat coming from the chip; failure to remove excess heat can cause device failure. Thus the right package, made of the right materials, is critical.

The change in the unit percentages in the IC package mix is displayed in Figure 1. Array packages, QFNs and WLPs are on the rise as a percentage, while TSOPs are showing a decline as a percentage. While the largest market for TSOPs, standard logic, is holding relatively even, the package is losing ground in the large memory market sector.

So what are the largest growth areas for IC packages?

- Stacked packages and SiPs, which largely are packaged in FBGA solutions, are both growing in the vicinity of 16% compound annual growth through 2014.

- QFNs and inner-row QFNs, which allow for a great expanse of I/O counts, are edging in on territories previously held by SOs and QFPs. QFNs are growing at 10.45% CAGR through 2015, while the newly-introduced inner-row QFN will grow at a staggering 107% through 2014.

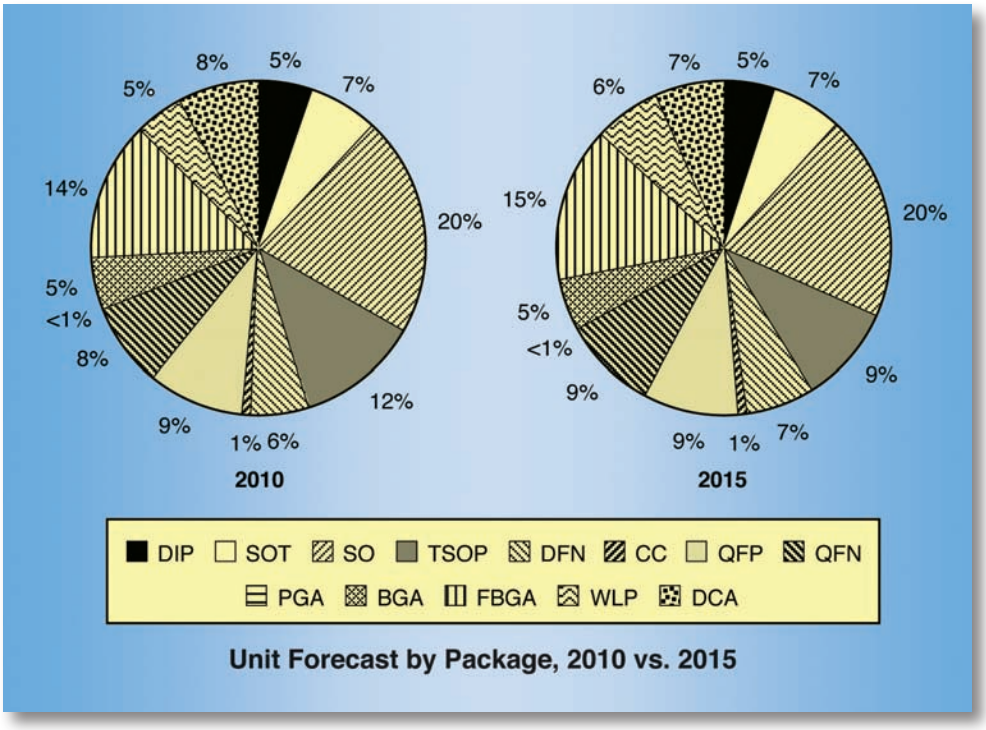

Figure 1: Change in unit percentages in the IC package mix.

- Wafer-level packages (WLPS), which capture the very low end of the market, will broaden their reach with the adoption of fan-out WLPs. Fan-out WLPs have an added overmold which expands beyond the edge of the chip, allowing for a larger surface for electrical traces beyond what is capable with traditional WLPs, which allow for considerably higher I/O counts. WLPs are growing at 13.85% CAGR through 2015, while fan-out WLPs are growing at 38.4% CAGR through 2014.

- Flip chip interconnection, which can be incorporated into a variety of package solutions, is growing at a CAGR of 31.3% through 2014 for in-package solutions. While PGA, BGA and FBGA package solutions are obvious selections for a flip chip interconnection style, flip chip can also be utilized on leadframe packages as well, such as the DFN and QFN package solutions.

Stacked Package

Stacked packages are a special form of a multi-chip package, one which places the die vertically on top of one another. The stacked package and SiP markets are being driven by the wireless communication and digital data storage markets. High-density memory for data and image storage, as well as higher speeds for reading and writing, are required to meet the needs of the marketplace. The complexity and number of features in handheld products such as cell phones continue to increase, while pressure for small and lightweight products also persists. Stacked packages are useful in meeting both of these conflicting needs.

Speed, performance, signal integrity and package density are key drivers of this technology. Many of these devices are placed in portable devices and, by increasing the density of the packaged devices, can reduce the size of the end products. This both reduces the cost of the final product (system cost), as less material is used, and increases the desirability of the final product in the eyes of the consumer.

Stacked package options include:

- Die Stack—die within a single FBGA;
- Package on package (PoP);
- Package in package (PiP);
- Stacked TSOPs or within a TSOP;
- Stacked QFN or within a QFN;
- Stacked MCMs; and
- Stacked WLPs.

A total of 50% of all stacked packages are die stack packages. This technology keeps all die stacked on a single substrate. PoP solutions comprise 36%. This package solution places one technology, such as memory, on one substrate, and another technology, such as logic, on a separate substrate. This allows for each of the device types to be tested separately and then stacked after testing. Both die stacks and PoP solutions will be reduced as a percentage of the total over time, as PiP, stacked QFN and WLPs gain ground. PiPs also allow for dissimilar technologies, but with the top device inverted or upside down and all devices on a common substrate and overmold. A total of 74% of stacked packages will find themselves in cell phones ultimately.

> ***Speed, performance, signal integrity and package density are key drivers of this technology.***

System in Package

A system in package (SiP) is a customized package, with multiple elements inside, in a standard JEDEC footprint. A SiP can be one or more semiconductor die and passives (resistors and/or capacitors), or two or more chips that form a system, such as a processor plus memory, integrated into a single packaged unit. Die embedded within the substrate with other devices on top of the substrate qualify.

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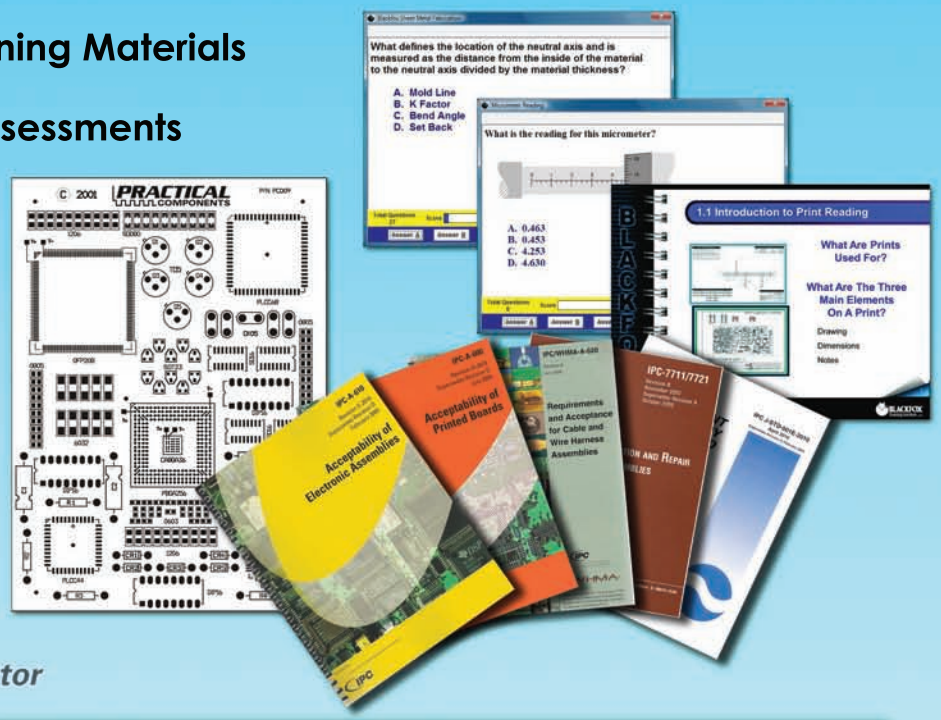

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However, one die plus a decoupling capacitor does not qualify. A SiP can be thought of as a functional block. It operates as a system to achieve a level of performance beyond what can be accomplished by placing the components into individual packages. Like an MCM, because more activity is happening within the package, fewer leads are required in and out of the package in relation to other large and complex devices.

The die within a SiP can either be placed next to each other horizontally or stacked vertically, blurring the definition between stacked packages and SiPs. When a stacked package contains enough elements to be a system, then it is placed in this category.

> ***The goal is to create a packaged part that costs less than an MCM and can fit into a greater number of everyday end products.***

A SiP attempts to fill the need for a semi-custom package with not-so-exotic parts, thus differentiating it from the more complex and customized MCM. The goal is to create a packaged part that costs less than an MCM and can fit into a greater number of everyday end products. An individual SiP should be easily modifiable so as to go into different products than the one for which it was originally created, and have some degree of scalability to upgrade the device.

A common package platform such as a BGA, with a JEDEC footprint, would also distinguish a SiP from the more customized MCM. A standard package format also makes the part transparent to the user for ease of assembly.

The end result of both a SiP and an MCM is that the individual pieces of a unit are in close proximity and, thus, can operate at higher speeds and with lower power consumption than if the individual pieces were farther apart in separate packages. The number of I/Os on the package is reduced in comparison to separately packaged parts due to the functional block nature of the package, in which many functions are being handled within the package with fewer connections needed outside the package.

If discrete devices are incorporated within the SiP, then these do not require tracing on the PCB. In addition, less space is consumed on the PCB, allowing for shrinkage of the final product. Any number of end applications can benefit from these dynamics. Certain medical devices, such as hearing aids, and cameras that are swallowed to provide images of the intestinal tract, require this small form factor. Any hand-held, battery-operated device, such as a cellular telephone, can benefit.

Cell phones, again, are the largest market for SiPs, with approximately 69% of all SiPs going into these products. Another 10% will be captured to the base stations that serve the cell phones.

QFNs and Staggered Inner-Row QFNs

QFN, or quad flat pack no-lead, packages are a more recent package introduction than the more established packages such as the SO, but they have quickly attained popularity. The QFN is in the chip scale package (CSP) category, being close to die sized. It has leads on four sides of the package, which are encapsulated within the mold compound so that the package rides flat on the PCB. The lack of visible leads protruding from the bottom gives this package the name “no lead.”

The shortened lead length increases the speed of devices, as the electron does not travel quite as far to reach the PCB from the die. The entire leadframe is reduced in size due to the closely cropped nature of the package in relation to the die, and to the shortened lead length, which does not have the external gullwing leads.

The QFN offers thermal performance superior to that of leaded packages of similar body size and I/O count. The leadframe is on the bottom of the package; thus the die attach pad is exposed, allowing it to be easily soldered directly to the board and allowing heat to

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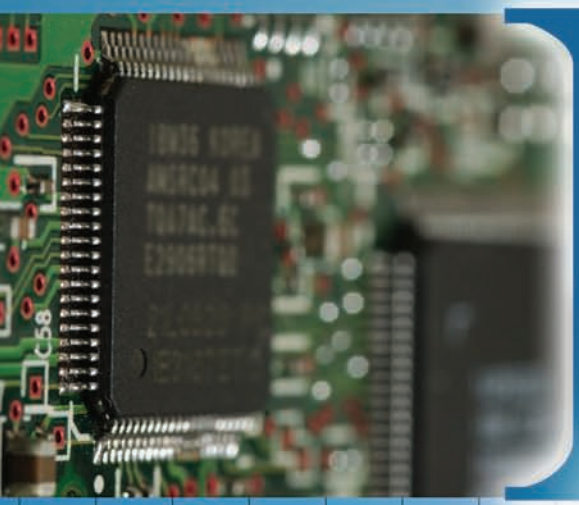

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dissipate into the PCB. Heat transfers faster into solid material than into ambient.

QFNs currently house a large number of devices; the largest markets include 8-bit MCUs, standard logic, voltage regulators and references, and both special-purpose logic and analog communications chips.

Extending the Lead Count

To further increase the reach of this package, the latest development in QFN packages is to extend the number of rows of leads from the usual one row, to two or three rows of leads. The leadframe is stamped or etched as in any other leadframe solution, but the leads are of various lengths, either two or three different lengths. When bent downward for connection to the PCB by trim and form equipment, the result is a staggered-row, array-patterned package solution with a hole in the center. This allows the number of package leads to extend into the hundreds, up from generally fewer than 50 with a traditional QFN. The resulting package is a high-density, leadframe array package.

> ***"The result is that the final packaged product is the same size as the die itself."***

The staggered inner-lead QFN has the ability to capture the lower-end of the quad flat pack (QFP) market. This includes extending its reach to higher-bit MCUs and both logic and analog communications chips, largely bound for handheld gadgets that require a small form factor package.

Wafer-Level Packages (WLP) and Fan Out Overmolded WLPs

Wafer-level packages (WLPs) are formed on the die while they are still on the uncut wafer. The process can be thought of as an extension of front-end manufacturing in that it involves the entire wafer, but it is more similar to bumping for flip chip and TAB operations. The result is that the final packaged product is the same size as the die itself. Singulation of the device occurs after the device is fully packaged, unlike traditional forms of packaging.

Most WLP designs place the active circuits face down for the shortest electrical path. The active circuits can also be face up, with electrical connections either through the silicon or wrapping around the silicon. Through-silicon designs allow for wafer stacking, such as in the Tru-Si model. Face-up WLPs can be used for signal-sensitive devices and fine-pitch interconnections as well.

Fan-Out Overmolded WLPs

Reconfigured or fan-out overmold wafer-level packages were introduced in 2006. After devices are manufactured on a wafer, the devices are sawn and transferred on a carrier to another larger wafer that has gaps between die, which are filled with overmold material that also coats the back side of the devices for protection. This allows for a larger surface on which to extend a redistribution layer, thus allowing for far more I/Os than would be possible on the original smaller surface. Solder balls or bumps can be added to this surface for interconnection to a printed circuit board.

The WLP Market

While WLPs are used for logic, memory and analog devices, it is the analog market that is the largest for WLPs. Voltage regulators and references, found in all electronics, are a large market for WLPs. WLPs are quite suitable for these devices, as WLPs are traditionally a low-I/O package, which match the I/O demand of voltage regulators and references.

Fan-Out Overmolded WLPs extend the I/O count beyond just the number of I/O which can fit on the face of a small IC. Fan-out overmold WLPs are utilized to package baseband processors, RF and analog, power management and analog and logic ASICs, including application processors, power amplifiers and within MCMs to create a

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radio-in-package (RiP) device. More applications will be found for these packages subsequently.

Flip Chip Interconnection

Flip chip interconnection places the die flipped face down (or active side down) so that the circuitry faces the substrate. Unlike wire bonding, in which the connections are made at the periphery, flip chip connections are in an area array covering all or part of the face of the die. Flip chip is almost always performed on packages with substrates, although a few designs utilize leadframes. The die does not have to be face down with leadframe designs; the leadframe can be designed to reach over the top of the die in a face-up position for interconnection, as in the case with Carsem's FCOL. This maintains the face-up position away from the PCB, preventing crosstalk with the PCB, which is important with RF chips.

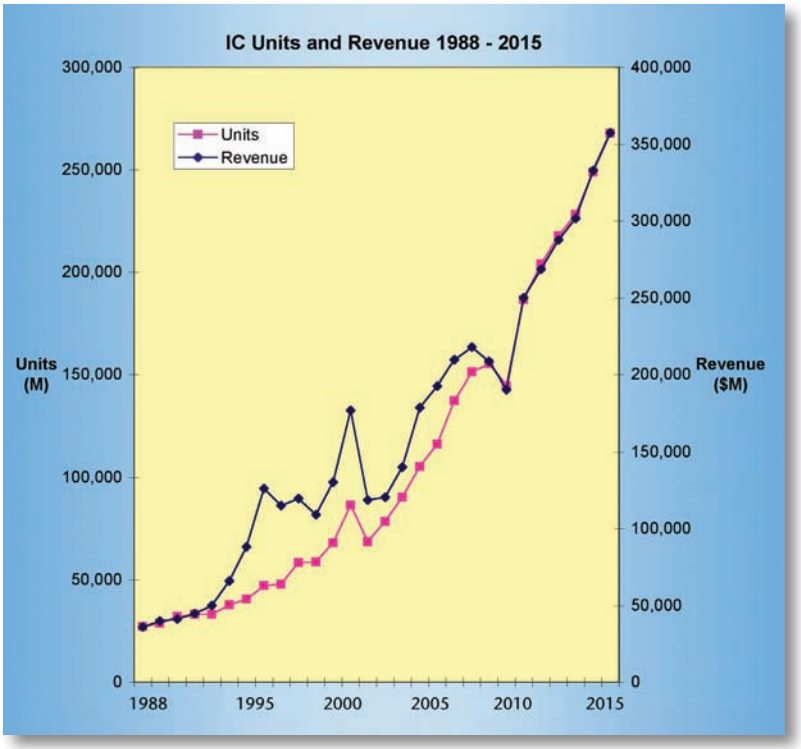

Figure 2: ICs continue on an upward trend.

The electrical connection is made through bumps on the face of the die, which then connect directly to the substrate below. The bumps are in an array pattern on the face of the die, and are placed on the surface of the die while the die are still on the uncut wafer. Individual die can also be bumped, but this is not a cost-effective solution.

The processes involved with flip chip technology tend to be expensive and sometimes difficult, although less expensive than wire bonding when I/O numbers are high. Flip chip is not suitable for every application and tends to be used for high-performance, high-I/O devices and low-I/O devices in space-constrained areas. Flip chip allows for a higher density of interconnection points than does wire bonding, as the array pattern of bumps on the die surface allows for a greater percentage of the total device surface to be used for interconnect. This is in contrast to just the periphery being used, as in the case of wire bonding. Because the interconnection to the substrate is made beneath the die, not out to the periphery of the die as in wire bonding, a smaller form factor is achieved in the overall package size; hence the use of this technology in space-constrained areas. Given the shortened electrical distance to the board, flip chip also offers greater speed with less parasitics.

The use of flip chip becomes mandatory on any die with an I/O count so high that the pads cannot fit around the die perimeter. Though this number is die specific, it almost certainly applies at I/O counts above 700. Due to the shorter length in the interconnection, flip chip also has lower signal transmission losses in relation to wire bonding. High clock speeds and increasing functionality of the chip drive the need for higher I/O counts and faster package performance than what is obtained through the use of wire bonding. Most microprocessors switch to flip chip when their clock speeds reach 400 MHz. Flip chip is also used for some high-frequency RF devices.

Flip chip is used for a number of applications, including computers and game consoles, networks and communications and mobile platforms. Frequency, battery life and miniaturization are all issues for mobile

Video Interview

Endicott Interconnect Still On the Leading Edge

by Real Time with...IPC APEX EXPO 2011

Jim Fuller, the company's Vice President of Manufacturing Programs, sits down with Guest Editor Joe Fjelstad and shares a bit of history and provides a sense of direction for one the most fully-integrated and advanced circuit manufacturing and assembly companies in the industry.

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applications. Typical devices utilizing flip chip include chips at the high end such as MPUs, graphics chips, field programmable gate arrays (FPGAs) and programmable logic devices (PLDs). Flip chip also has a niche at the bottom of the market, with low I/Os in space constrained products. Devices with flip chip with low I/O generally do not require underfill beneath the die to accommodate the CTE mismatch, although it is often used on handheld devices anyway to assist with the "oops" factor.

Smaller, Faster, Cheaper Still the Theme

The fastest growing packages and technologies are well suited for space-constrained locations and will find themselves in handheld items purchased by average consumers. Long gone are the days when military and space applications dominated the demand for ICs, individual consumers now control much of the market. Consumer items costing $400 and under still sold well during the Great Recession. Demand for cell phones, particularly smart phones, tablets, digital cameras, automobiles laden with ICs and more will continue to keep demand for ICs on an upward trend, as shown in Figure 2. SMT

Sandra Winkler has been an industry analyst since 1988, and since 1995, a staff member of Electronic Trend Publications, currently New Venture Research. She has produced numerous off-the-shelf and custom reports. Winkler began her analyst career in the telecommunications industry. Since 1995, she has focused on the semiconductor packaging industry and has authored more than 30 widely cited reports on the topic, including "The Worldwide IC Packaging Market," "Advanced IC Packaging Markets" and "Trends and IC Packaging Materials." Winkler has an M.B.A. from Santa Clara University. She is on the executive planning committee of IEEE-CPMT, Santa Clara Valley Chapter.

Advanced Packages Change PCB Landscape

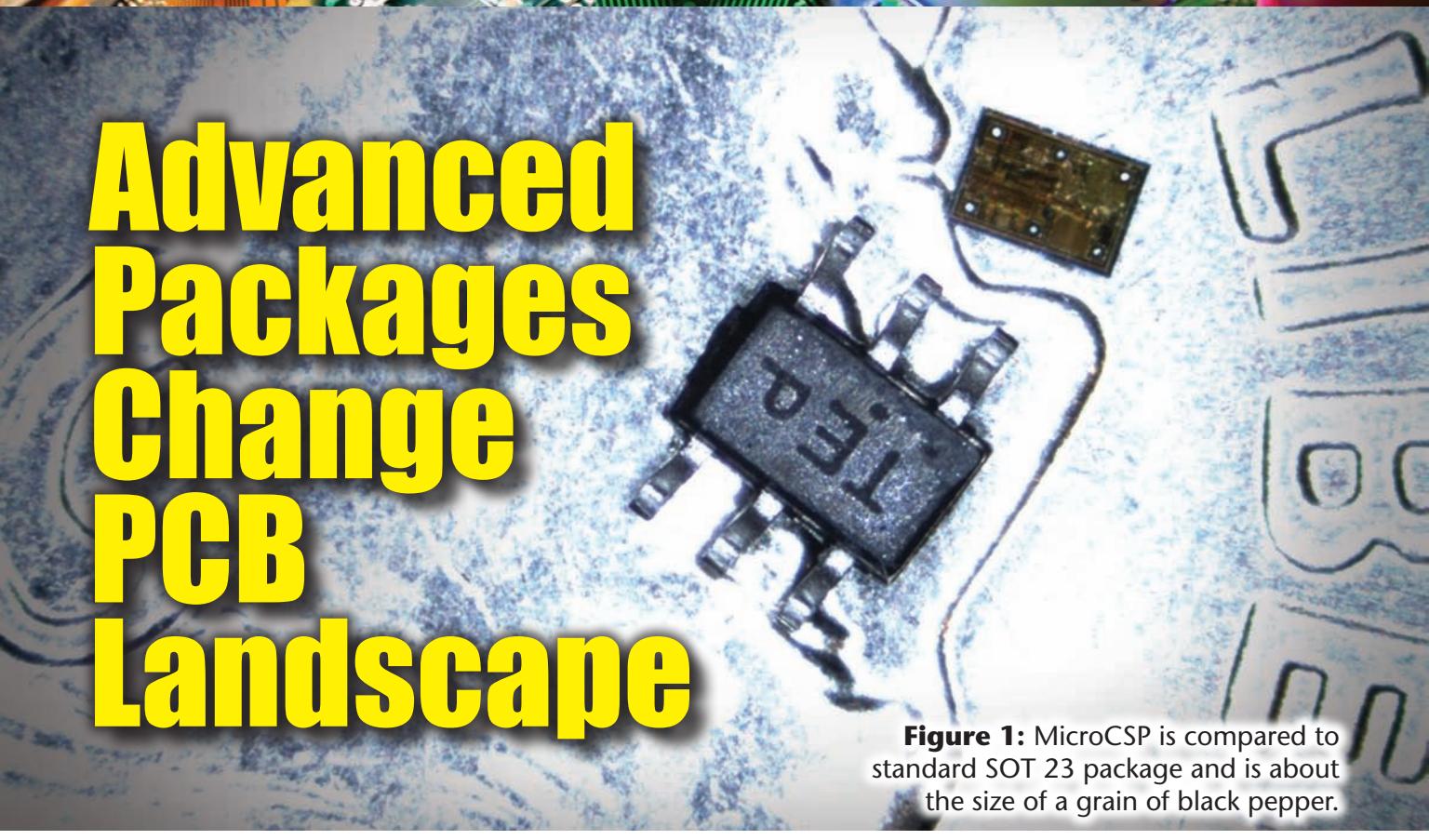

Figure 1: MicroCSP is compared to standard SOT 23 package and is about the size of a grain of black pepper.

by Zulki Khan, *President and Founder*
NEXLOGIC TECHNOLOGIES, INC.

IN SUMMARY

Ever-shrinking advanced packaging technology falls on the shoulders of automated optical inspection (AOI) machine manufacturers and spurs them to develop new solutions to meet inspection challenges.

When it comes to advanced packaging, inspection is the key challenge that immediately springs to mind from a PCB assembly perspective. Figure 1 shows how miniscule advanced packaging is becoming. In this case, a microCSP is about the size of the letter "L" in the word "Liberty" on the face of a dime and is compared to a standard SOT 23 package. Other packages, such as microBGAs and smaller passives like 0201s and 01005s, are also continuing to dramatically increase in usage, posing major challenges to PCB assembly. Additionally, package-on-package (PoP) is making inroads into PCB assembly, thus posing another new and unique set of issues and challenges for both EMS providers and OEMs.

Ever-shrinking advanced packaging technology falls on the shoulders of automated optical inspection (AOI) machine manufacturers and spurs them to develop new solutions to meet these issues. Basically, AOI inspects the image of a component and recognizes letters and numbers written on a package to confirm verification of the package and its value. Currently, small packages like 0603s and 0402s can be read via AOI without any issues.

However, smaller packages like 0201s and 01005s are virtually impossible to inspect. That's because there's no room for numbers and, hence, no numbers and letters to be inscribed on the package to review or verify. Consequently, it becomes questionable

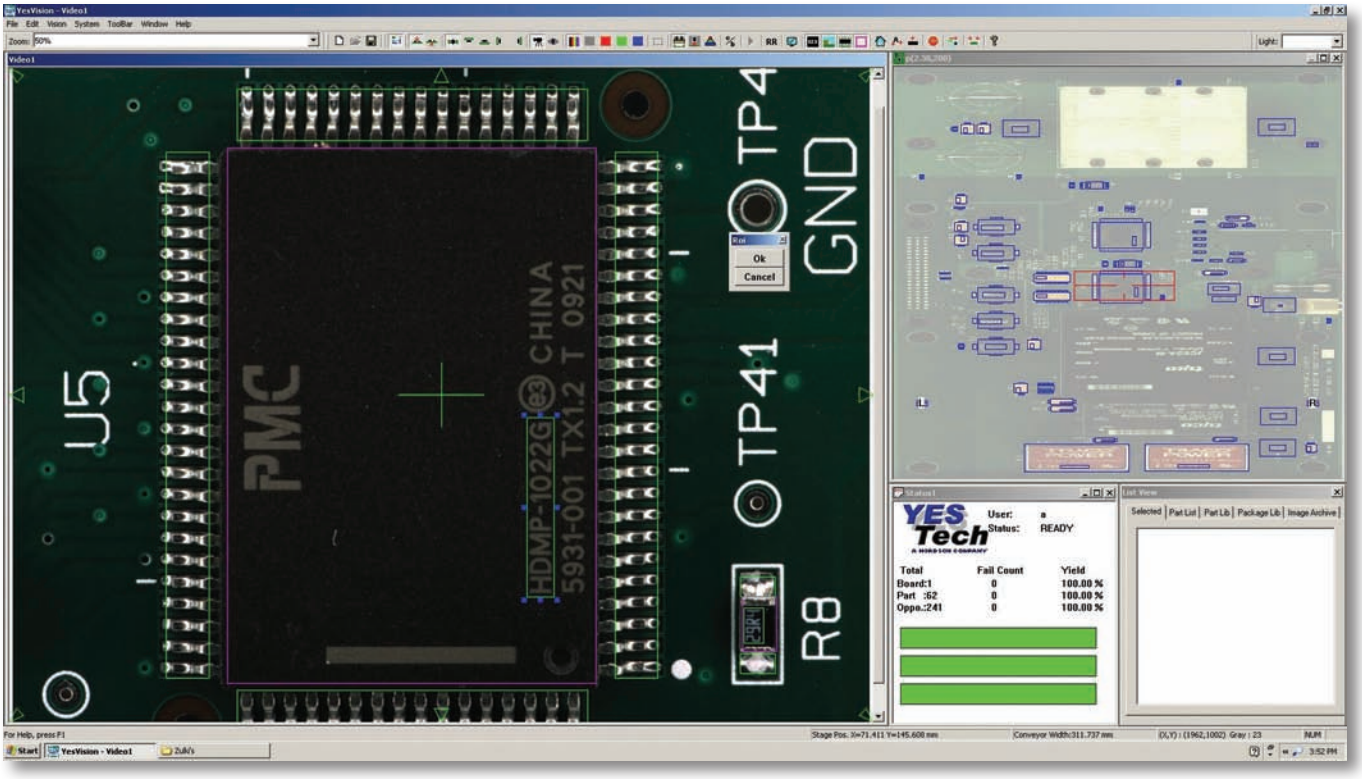

Figure 2: A 0603 package under AOI inspection process used to train the AOI machine. Image also shows difficulty of inspecting this small device.

whether or not the right component is used. Figure 2 shows a 0603 package under the AOI inspection process used to train the AOI machine, but this image also indicates the difficulty of inspecting such a small device. Advanced AOI machines have anywhere from five to 10 megapixel cameras which can capture the minute details on the components. There are at least four side-view cameras along with a top-view camera to give exceptional inspection and defect coverage. High-end AOI machines have complex algorithms, normalized correlation, as well as advanced color inspection techniques to detect the letters and numbers on the advanced packages.

Some EMS companies rely on manual inspection using quality control personnel, but, in this day and age, it is definitely not a great procedure; not only because those important device images cannot be seen clearly, but also from a dollars and cents and time-to-market loss perspective. This is a tedious and laborious process, which consumes considerable time, is subject to human interpretation and is prone to errors. There are no ifs, ands or buts. You've got to have the most advanced inspection systems available today to meet the advanced packaging challenges and maintain a high-level of assembly efficiency.

Why? From a cost perspective, the reason is there is virtually no possibility of re-work involving these small packages. If a microCSP or microBGA is damaged in any way, chances are about zero that it can be re-worked, meaning extra costs and production time for a new substitution. For instance, a microBGA is extremely difficult to re-ball since there is not enough surface tension on the BGA balls and PCB surface, or even enough room to manually do the re-work. The bottom line is there is no room for error when dealing with the advanced packages. Put another way, the best trained, most experienced technicians and engineers are required on the SMT line to make certain no mistakes occur, and that the job is performed correctly the first time.

Ultimate Goal: Process Control

In effect, the message is clear for any contract manufacturer (CM) or EMS provider involved with advanced packaging requirements. The ultimate goal is to develop and maintain stringent manufacturing process control that includes not only state-of-the-art AOI, but also thermal profiling, advanced paste height inspection techniques, printing and, most importantly, first article inspection (FAI).

FAI is normally performed at the end of the process. However, to close the loop earlier and thus shorten the correction cycle, FAI provides the highly-critical instant feedback right after a component is placed on the board. FAI checks at SMT placements with two associated functions. First, before components are placed, SMT QC ensures all feeder checks, polarity and component values are accurate. Secondly, as soon as components are placed and before the board goes to reflow, FAI assures placement is correct to include orientation and pin numbering sequence and so on.

As for paste height inspection, this step has always been important, but now it is especially critical because an advanced package's land pattern on the surface mount pad is extremely small and tight. Paste height inspection provides the crucial information to verify paste distribution on the surface mount pad, as shown in Figure 3.

The more advanced printers with vision systems also join in to inspect the presence or absence of paste on the pad. However, they are not as critical and accurate as laser paste height inspection systems. Here, stencil design is extremely important; it must be perfectly made so paste is dispensed as accurately as possible. Sometimes it's vital to open a bigger stencil's window compared to the surface mount pad. At times, it can be 0.9:1 or 1.1:1, depending on the application and stencil thickness and the amount of paste that is required. Figure 4 shows how insufficient solder can result in a head-in-pillow defect.

Figure 3: Paste height inspection verifies paste distribution on SM pad.

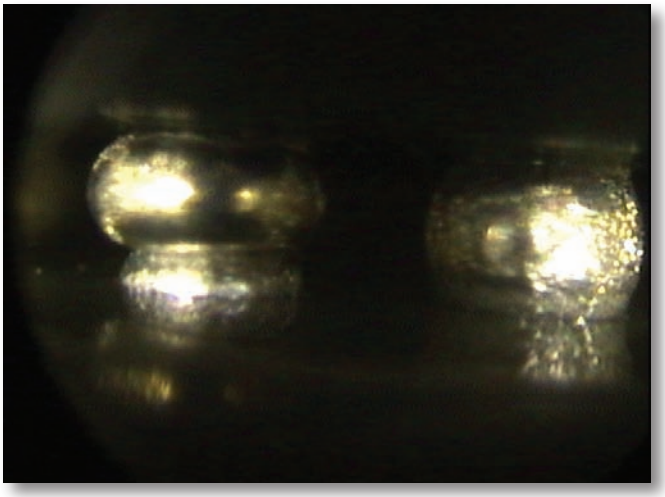

Figure 4: Insufficient solder results in head-in-pillow defect.

So, at all times, paste dispensing must be precise—not too much and not too little. And, as an added note, inkjet technology is considerably more desirable than other printing techniques for its greater accuracy. With an inkjet process, you can adjust the amount of paste on the same board for analog components, which require more paste when compared to digital components, and require less paste for perfect printing.

Thermal Profiling and Reflow

Like the other critical steps in the SMT line, thermal profiling takes on a greater importance due to the fact the land pattern and surface mount area is very limited. The tolerance also needs to be very tight not only for paste printing, but also in creating this profile. Experienced manufacturing engineers are mindful of this fact with small land

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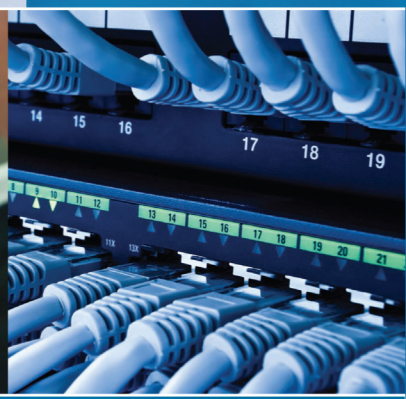

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patterns because, even when off by a few mils, it could dispense the paste outside the SMT component, thereby creating the possibility of opens and cold solders.

Also, in some cases, advanced packaging vapor phase reflow is being substituted for conventional convection reflow, especially for mil/aero PCBs and other applications demanding extreme high-reliability and quality. In the vapor phase technique, heat is transferred to the PCB surface from a source to the gaseous mass, creating a huge vapor blanket which acts as a reservoir of thermal energy. This energy is then used to reflow the solder on the board. The challenge, which is not too difficult to overcome, is creating a three-stage thermal profile for vapor phase technology which could deter many EMS companies or OEMs from using the process.

Cleaning is another challenging area. With packages continuing to shrink, cleaning underneath is becoming more and more difficult. These packages are so small that proper cleaning is virtually impossible. There's not enough room, and too much air pressure, to remove the solder. Flux residues underneath the board cannot be used because these tiny components can get damaged or they might just fly off the board.

The next best thing is a so-called batch cleaning process with saponifiers or other cleaning chemistry. This process has the ability to go into tight spots underneath a microCSP or microBGA device and perform the cleaning when no-clean flux is used. This type of cleaning is required for high-reliability mil/aero applications and is becoming more popular compared to de-ionized, water-only cleaning.

Testing

Advanced packaging offers no gull-wings or leads for testing purposes. Although 0201s and 01005s have tiny pads, they are too small to be used effectively as test points. Packages like 0603s or 0402s have pads that can be used as test points for flying probe testing, as shown in Figure 5. But for advanced packages, conventional test points are lacking. In these cases, modular, bus or batch testing must be used. As the name implies, different components are put together and tested in a modular batch fashion rather than using stand-alone test points or the surface mount pads as test points.

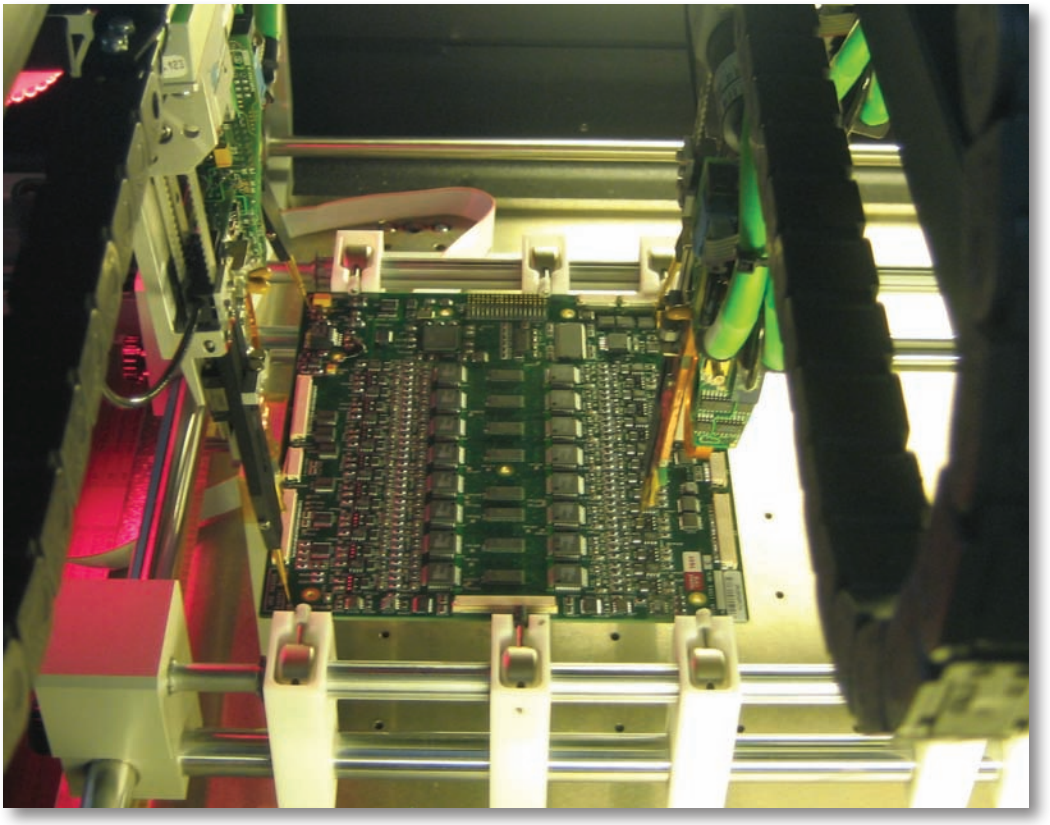

Figure 5: Packages like 0603s and 0402s have pads used as test points for flying probe testing.

This has another effect on a board's real estate due to having more test points than usual to check for 100% functionality. Since surface mount pads cannot be used, separate test points

Video Interview

Novel Z-Axis Interconnection Technology

by Real Time with...IPC APEX EXPO 2011

Guest Editor Joe Fjelstad meets with Steve Garcia, President of Medallion Technology, on the APEX show floor to discuss the company's unusual interconnection technology used to make vertical interconnections between two or more substrates.

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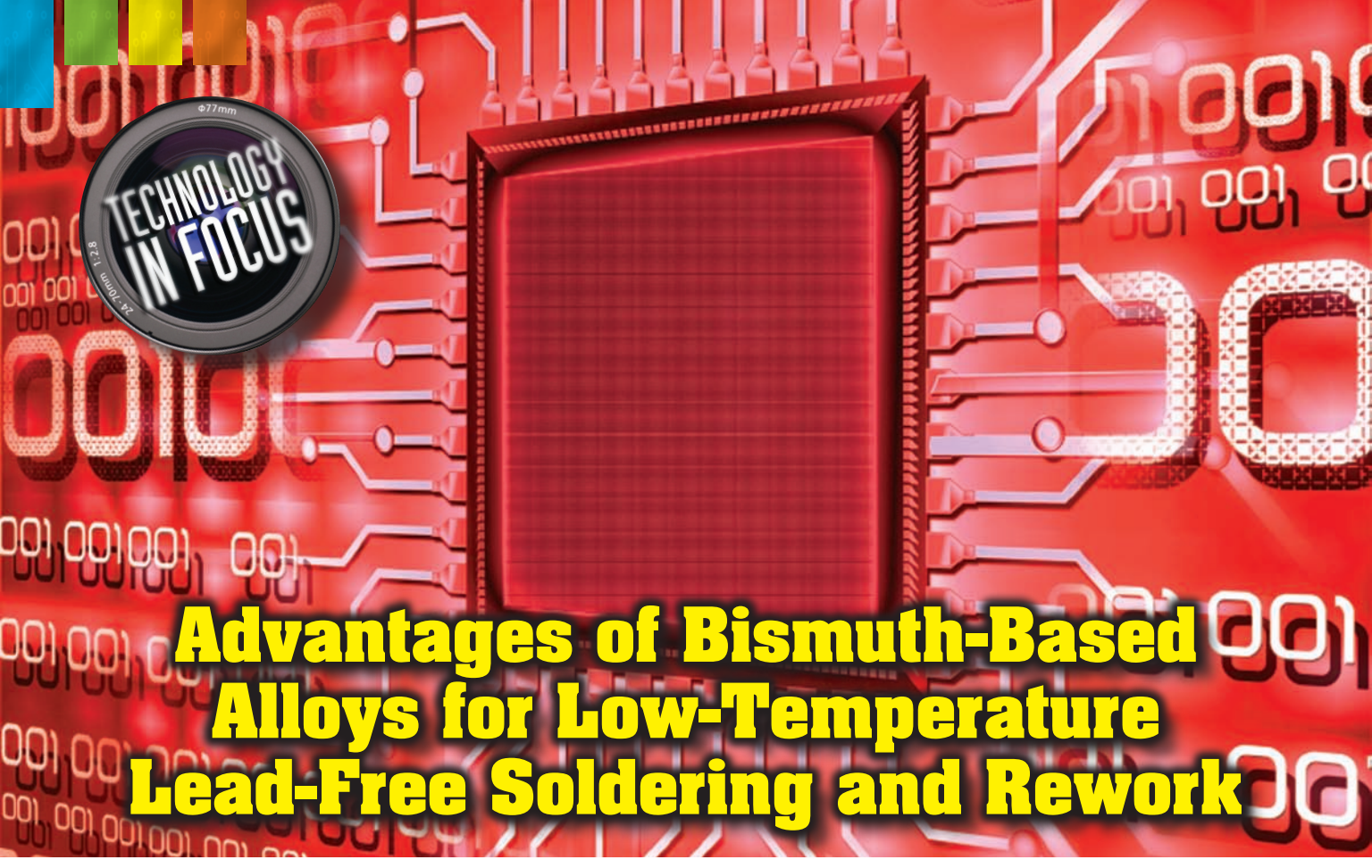
are needed on the top or bottom side of the board for flying probe testing.

Lastly, PoP is gaining popularity and creating concerns among PCB assemblers. In effect, PoP is stacking one advanced package device on top of another with special glue to hold them together. The CM has to make sure the first component is assembled correctly and that the second one is properly stacked on the first. Then, a special thermal profile must be developed and specifically tailored for that PoP stack.

Thermal profiling takes on a special meaning here because now we are not only considering the surface of the board for calculating the heat flow, but also considering the heat flow between the stacked components. Not all pick-and-place machines can handle PoP, so a special module has to be used. This module can control the placement of the component height using programmable z-axis control. Basically, the SMT programmer can define the height of the placement of the component, which would virtually be sitting on top of the other component. However, some CMs and EMS providers have this capability with existing pick-and-place machines on the assembly floor so that a multitude of customers can be served. SMT

Zulki Khan is the Founder and President of NexLogic Technologies, Inc., in San Jose, California, an ISO 9001:2008 Certified Company, ISO 13485 certified for manufacturing medical devices and a RoHS compliant EMS provider. Prior to NexLogic, Khan was General Manager for Imagineering, Inc., in Schaumburg, Illinois. He has also worked on high-speed PCB designs with signal integrity analysis. He holds a B.S. in EE from NED University in Karachi, Pakistan, and an M.B.A. from the University of Iowa. He is a frequent author of contributed articles to EMS industry publications.



Advantages of Bismuth-Based Alloys for Low-Temperature Lead-Free Soldering and Rework

by Brook Sandy, Edward Briggs and Ronald Lasky, *Ph.D.*
INDIUM CORPORATION

IN SUMMARY

A trend toward miniaturization, occurring at the same time as the conversion to RoHS-compliant lead-free assembly, has been a considerable challenge to the electronics assembly industry due to the higher reflow process temperatures required for lead-free assembly. Bismuth is a low-cost alloying option, especially in light of rising metals costs, and will be considered in this paper.

The increased function of personal electronic devices, such as mobile phones and personal music devices, has driven the need for smaller and smaller active and passive components. This trend toward miniaturization, occurring at the same time as the conversion to RoHS-compliant lead-free assembly, has been a considerable challenge to the electronics assembly industry. The main reason for this is the higher reflow process temperatures required for lead-free assembly. These higher temperatures can thermally damage the PCB and the components. In addition, the higher reflow temperatures can negatively affect the solder joint quality, especially when coupled with the smaller paste deposits required for these smaller components. If additional thermal processing is required, the risk increases even more.

A low-temperature solder is advantageous in this process in that its lower temperature thermal processing requirements can reduce the total thermal damage caused by using higher melting temperature alloys. Defects, such as delamination or "popcorning" of moisture sensitive devices (MSD), could be minimized or eliminated by using lower temperature solders. Delamination or popcorning failure modes occur when moisture diffuses into plastic components that rapidly expand upon heating. These lower

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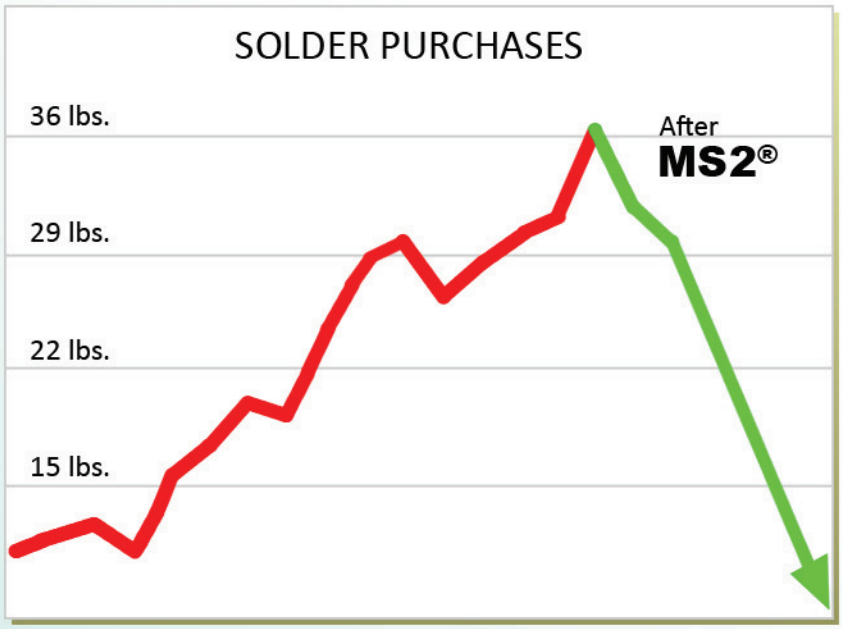

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temperature alloys may also be considered for use with temperature sensitive components, the step soldering process or rework.

The base metal for most solders is tin, which melts at 232°C. In low-temperature soldering a number of alloying elements can be used to reduce tin's melting temperature. Ga, In, Bi and Cd are effective in reducing the melting temperature of solder alloys, although Cd is not often considered due to its toxicity. Gallium-containing alloys are not practical as they are typically liquidus at room temperature or slightly above. This leaves bismuth and indium as alloying candidates for a low-temperature tin-based solder alloy. Indium has some unique properties, but it is much more costly than other alloying elements, which are generally used in solders. Bismuth is a low-cost alloying option, especially in light of rising metals costs, and will be considered in this paper. More specifically, we will investigate the BiSnAg alloy with a composition of 57Bi/42Sn/1Ag. Many companies have evaluated this alloy, with much of work done by Hewlett Packard (HP). Some of this work will be re-visited in this paper.

This BiSnAg alloy has a lower melting temperature than eutectic tin-lead solder's ($Sn_{63}Pb_{37}$ or Sn63) 183°C, yet it is high enough for most soldering applications. In addition, its mechanical properties are similar to Sn63, but contain no lead. The alloy is near eutectic at 137 to 139°C. Although a reflow temperature of 20 to 40°C above liquidus is typically recommended, the BiSnAg alloy still only requires a maximum reflow processing temperature of about 180°C. Sn63 assembly generally requires 205 to 215°C (or higher if reflowing lead-free BGAs -225 to 230°C) and process temperatures of 240 to 245°C are common for lead-free assembly. Work performed by HP on shear strength, creep resistance, fatigue resistance and other mechanical testing showed BiSnAg to have properties approaching or surpassing Sn63 under most conditions, including reasonable strength up to 90°C [1].

Concerns remain with bismuth-containing alloys, as Bi tends to be fairly brittle. Bismuth (and many bismuth alloys) are unique in the sense that they expand upon cooling, which can cause issues, such as fillet lifting, with through-hole components and, if used in an application where lead is present, can form a low-melting eutectic at 96°C. This concern was a real issue when the industry was first transitioning into the lead-free arena because most assemblies were only partially lead-free and lead contamination was a real concern. As the transition has progressed, this situation has become much less an issue.

In addition to reviewing the work HP has done with this alloy, new work on stencil printing characteristics, reflow profile optimization and solder joint quality will be presented.

The Hewlett Packard Work

Wetting

A number of factors affect wetting behavior, such as the surface tension of the solder, PCB pad metallization and flux activity. Early work by HP [1] showed that the flux activity of the materials that were tested was vital to the results, but once the proper flux chemistry was achieved, the results (spread test and wetting angle as shown in Figure 2)

Metal	Source	Price/lb.	
Bismuth	Metal Bulletin	$11.45	Avg.
Copper	Metal Bulletin	$4.37	4/27/2011
Indium	Metal Bulletin	$343.00	Avg.
Lead	Metals Week	$1.27	Avg.
Silver	NYMEX	$674.00	4/27/2011
Tin	Metals Week	$14.63	4/27/2011

Figure 1: Metals chart.

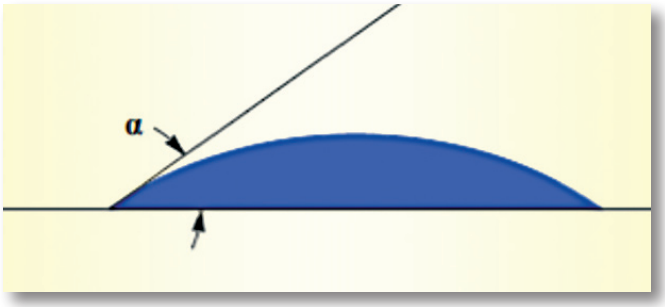

Figure 2: Wetting Angle α on CuOSP [1].

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were near those of Sn63. The lower melting temperature BiSnAg alloy requires a flux with a lower activation temperature. Most tin-lead fluxes activate at 160 to 170°C and are not optimal for the BiSnAg process.

Shear

Solder joints experience shear stress caused by differences in coefficient thermal expansion (CTE) mismatch in temperature cycling. The HP study found that the BiSnAg alloy had a higher shear strength than Sn63 at 20°C, a comparable shear strength at 65°C and lower (but comparable) shear strength than Sn63 at 110°C. For more detail on the test procedure and results please refer to 57Bi-42Sn-1Ag: A Lead Free, Low Temperature Solder for the Electronic Industry [2].

Creep

Creep is defined as a constant load applied at an elevated temperature causing deformation or flow over time. Results from the HP study are shown in Figure 3. The steady-state strain rates as a function of shear stress are plotted at 25°C, 65°C and 90°C (for BiSn and Sn63, no data were available for the BiSnAg). Creep resistance of BiSn exceeds Sn63 at 25-65°C [1].

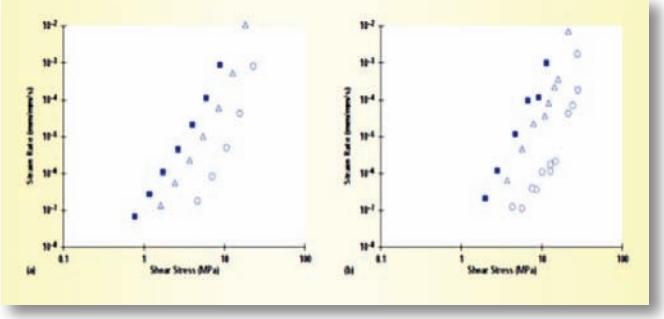

Figure 3: Strain Rate versus Shear (a) Sn63 (b) SnBi [1].

Thermal Fatigue

An interesting finding occurred during HP's thermal fatigue testing. Twenty boards were assembled with Sn63 and 58Bi/42Sn using PCBs with CuOSP and Sn63 HASL finish on the pads. All passed visual and functional testing, but during thermal cycling (-20°C to 110°C) a thermal failure was observed with

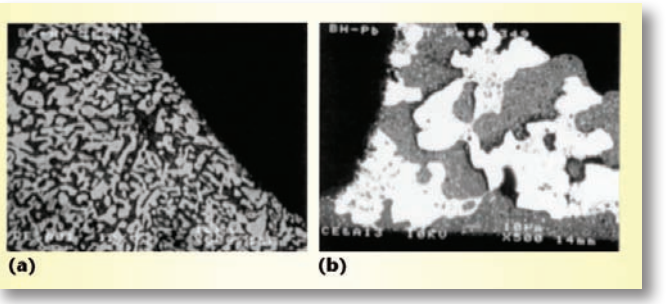

Figure 4: SEM cross section of solder Joints the same magnification after thermal cycling (a) BiSn on CuOSP (b) BiSn on Sn63 HASL [3]. (Note the large grain structure.)

the BiSn solder on the SnPb HASL-finished PCB pads when some of the components fell off after approximately 500 cycles (whereas the Sn63 failed after 900 cycles.) It was noted before testing that the solder joint surfaces of the SnBi on CuOSP and Sn63 HASL were smooth, but afterward the SnBi on SnPb HASL was grainy, while the BiSn on CuOSP was still smooth. This roughness was due to large grain growth (Figure 4). HP concluded that the grain growth was due to lead from the surface finish dissolving into the BiSn solder, forming a low melting eutectic at 96°C. Since each cycle reached 100°C, that phase became liquid at the grain boundaries, accelerating the formation of the large grains [1].

Due to the concern with this low melting point phase, lead contamination studies found that the lead content of <0.3% wt. does not significantly degrade the mechanical properties of BiSnAg even when aged at 100°C. However, it was suggested that the maximum allowable target should be 0.1% wt. lead.

In later work, HP observed that small additions of Ag (or Au) increased the thermal fatigue life of the BiSn alloy. At -25° to 75°C (BiSnAg), all assemblies survived 7,000 cycles, and actually outperformed Sn63. BiSnAg thermal fatigue is comparable or superior to Sn63 (even in range of 0 to 100°C and in the absence of lead contamination). It was suggested by HP that the Ag may decrease the grain size and stabilize the microstructure (a finer microstructure typically is ideal for better mechanical properties) [4].

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Bend Test BGAs

In this test, HP incorporated three PCB pad surface finishes, CuOSP, ENIG and ImSn, and a plastic ball grid array (PBGA) with the following solder spheres: 96.5Sn/3.5Ag, Sn95.8/Ag3.5/0.7Cu, 99.3Sn/0.7Cu and Sn63. A four-point bend test was performed on assembled boards after aging them isothermally at 90°C for one, three and 10 days.

It was found that the high tin-containing solder spheres (with liquidus ≥217°C) did not melt/collapse using the low-temperature profile required for the SnBi solder paste. It was also found that, when dealing with the SnBi solder paste,the volume of paste deposited on the pad is vital. When the volume was insufficient, all solder joints failed in the solder between the PCB and the BGA ball. However, with adequate paste volume, the SnBi solder joint strength improved enough to force failure by pullout of the Cu pad. Joint strength was about 65% of Sn63 [4].

> *To approach Sn63 solder paste performance, more paste is required than current stencil designs for Sn63 or lead-free processes deliver.*

Summary of HP Testing

BGAs: It was recommended to use SnBi or SnBiAg solder spheres so that the solder joints will collapse and improve the joint microstructure, thus improving the mechanical properties. Current Sn63 or SAC stencil aperture designs can be used. As mentioned, SAC alloy balls will not collapse due to the lower reflow process associated with SnBi or SnBiAg alloys. Therefore, to get the best properties when using the higher melting SAC solder balls, the correct volume of SnBiAg paste is vital. To approach Sn63 solder paste performance, more paste is required than current stencil designs for Sn63 or lead-free processes deliver. In HP's study for a 30mil solder sphere where 4000 to 4500mil^3 was sufficient, 8000 to 9000mil^3 of SnBi/SnBiAg solder paste was required. The appearance of the reflowed solder joint changed from an hourglass shape to a barrel-like shape. One approach to optimize this issue is to use square versus circle apertures. For the same area ratio, a square aperture will provide more volume.

Backside components: The SnBi and SnBiAg alloys have a lower surface tension than either Sn63 or lead-free alloys. This lower surface tension may be problematic in double-sided reflow for heavier components on the underside. The lower surface tension of bismuth solder may not hold components in place during the second reflow.

Surface finishes: HP concluded that CuOSP PCB pad surface finishes consistently showed the best mechanical and process results. ImAg, ENIG and ImSn all produce acceptable wetting and subsequent performance. Thick coatings of Ag or Au should be avoided, as with any Sn-bearing solder, due to embrittlement issues.

Bake out: Post-baking procedures (if a bake is required) may need to be altered. Twelve hours at 125°C is too harsh for this low melting alloy. A maximum temperature of 90°C for 12 to 15 hours should be sufficient.

Component placement: Because of the lower surface tension of the SnBi and SnBiAg alloys, the registration of the solder paste deposit to the PCB pad and component placement may be more critical as less self-alignment may occur.

Depanelization: Use adequate fixturing and board support, as the BiSnAg has a more sensitive strain rate [2].

New Study Results

Printing

The focus of this printing experiment was to observe the transfer efficiency of the SnBiAg solder paste to note any discernable difference in process parameters from the typical Sn63 or lead-free solder pastes. Therefore, in an

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effort to minimize the number of variables, the same stencil, squeegee blades and printer parameters were utilized as in previous experiments with the Sn63 and lead-free solder pastes.

A 4-mil laser-cut/electro-polished stencil, 250mm squeegee with edge guards, foiless clamps and landscape vacuum support blocks were used on the stencil printer. The solder paste was printed at 50mm/second squeegee speed with a blade pressure of 4kg.

A test board with 16, 14, 12mil circular and square (and 11-mil squares), was evaluated. 0201, land grid array (LGA) and various rectangles in both solder mask defined (SMD) and non-solder mask defined (NSMD) pads, were evaluated. A no-clean solder paste with Type 3 particle size of 57Bi/42Sn/1Ag was chosen. Eight PCBs were printed with no stencil wipe performed and data collected via a Koh Young KY-3020T laser scanning system to measure the volume of the stencil printed deposits.

Area Ratio

The stencil aperture area ratio (AR) is a critical metric in successful stencil printing. It is the area of the stencil aperture opening divided by the area of the aperture side walls. Figure X shows a schematic for a circular aperture. A simple derivation shows that the AR is simplified to the diameter (D) of the circle divided by 4 times the stencil thickness (t), or AR = D/4t. Somewhat surprisingly, the results are the same for square apertures, with D now equal to the side of the square. For the AR of a rectangular aperture, the formula is a little more complicated: ab/2(a+b)t, where a and b are the sides of the rectangle.

It is widely accepted in the industry that to get good stencil printing the AR must be greater than 0.66. Experience has shown that if the AR < 0.66, the transfer efficiency will be low and erratic. Transfer efficiency, another important stencil printing metric, is defined as the volume of the solder paste deposit divided by the volume of the aperture [5].

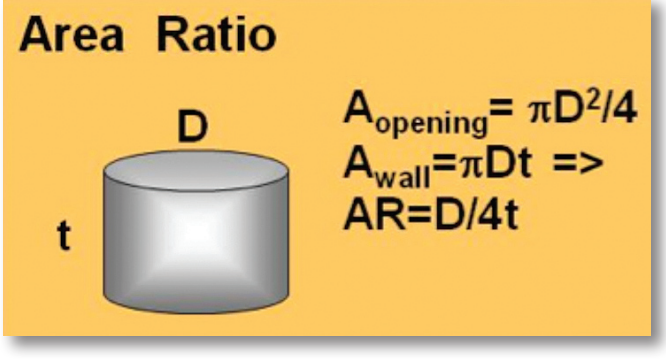


Figure 5: A schematic showing the definition of the area ratio for a circular stencil.

Stencil Printing Results

The transfer efficiency of the LGA pad, 12mil CSP and 0201, as shown in Figure 6, was excellent. The 0201 area ratio of 0.67 was the greatest challenge and included 6,400 data points for reference in this test. With the exception of a couple of outliers, the transfer efficiency was very good.

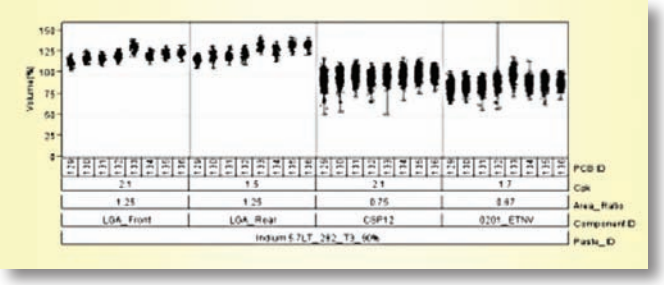


Figure 6: Stencil printing results.

Circles Versus Squares

For the larger apertures, circles provided a bit better Cpk, but as the apertures became smaller the squares began to outperform the circles (Figure 7). The smaller apertures are more challenging in regards to transfer efficiency, and the paste volume becomes

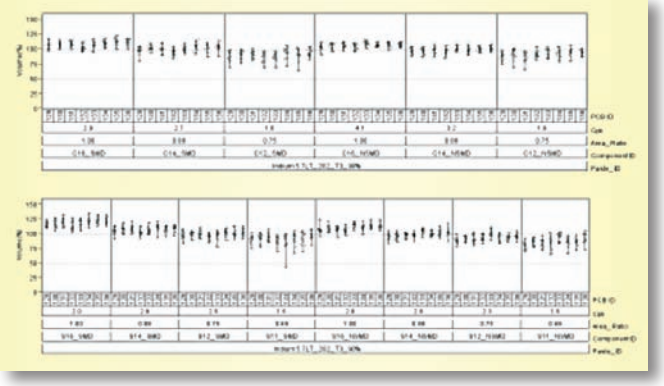
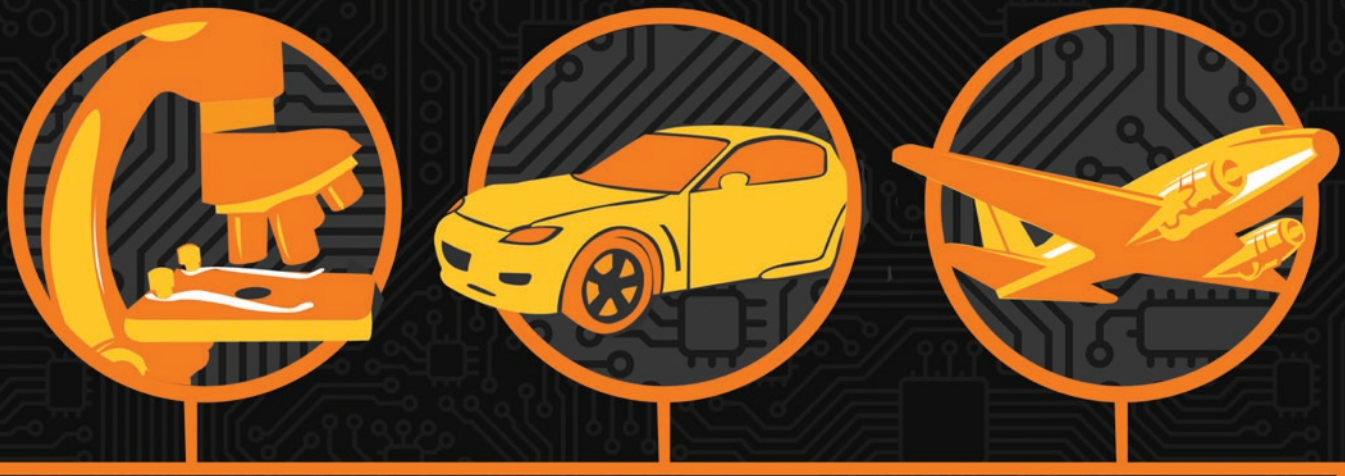


Figure 7: Circles versus squares.



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critical. It's important to note that for a circular and square stencil aperture of the same area ratio, the square (radius corners recommended) aperture delivers more paste volume. The increased volume for these smaller area ratios increases the transfer efficiency as evidenced in the test data.

SMD Versus NSMD

For larger apertures (>14mil), the non-solder mask defined (or pad-defined) PCB pads provided better transfer efficiency than the solder mask defined. For the larger pads, the non-solder mask defined pads provide a better stencil to PCB gasket. However, as the PCB pads become smaller (<14mil), the data shows that the mask defined pads provided better transfer efficiency. Paste release from the stencil aperture relies partially on the adhesion of the solder paste to the PCB pad. As the PCB is lowered from the stencil aperture, adhesion of the solder paste to the PCB helps the paste to "pull" out of the stencil aperture. With the smaller pad there is little surface area for adhesion; the wall of the solder mask (mask defined pad) may increase the surface area for adhesion improving paste release.

In summary, the printing process for SnBiAg solder paste was very similar, if not identical, to the Sn63 or lead-free process.

Reflow Profile Results

In our reflow experiments, a ramp-to-peak profile (Figure 8), with a peak temperature of 170 to 180°C and time above liquidus (TAL) of 70 to 80 seconds was used. Due to the lower processing temperature, a longer TAL is often necessary to allow for intermetallic formation. A common test vehicle having apertures of 38.5mil x 390mil with pitch size 90mil was used. The paste was first printed and reflowed on CuOSP finished PCB pads immediately after printing and the solder joints were then evaluated (Figure 9). Additional samples were then printed on ENIG, CuOSP and ImAg PCB pads and placed in humidity chambers—the first sample for three hours at 76% RH and the second sample for three hours at 90% RH. The samples were then reflowed to observe the humidity resistance in the solder joint formation (Figures 10 and 11).

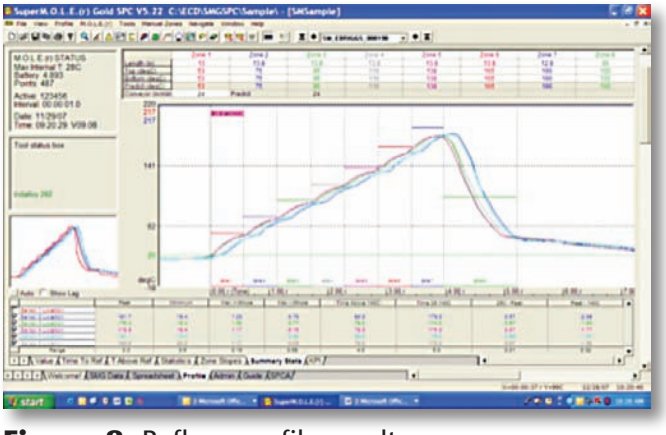

Figure 8: Reflow profile results.

Results

Wetting

Figure 9: Printed and immediately reflowed.

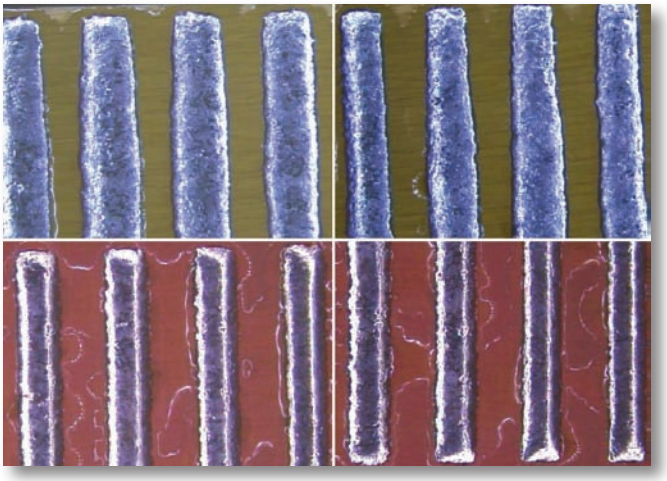

Figure 10: ENIG on top, CuOSP on bottom: 3 hours 76% RH, 3 hours 90% RH, 3 hours 76% RH and 3 hours 90% RH.

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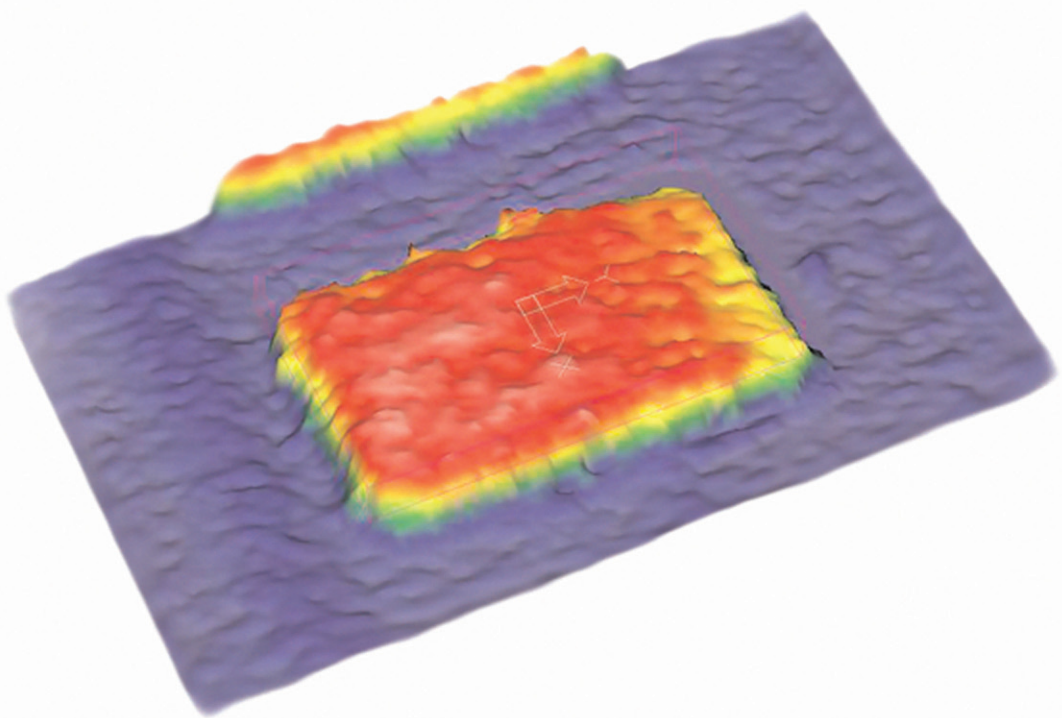

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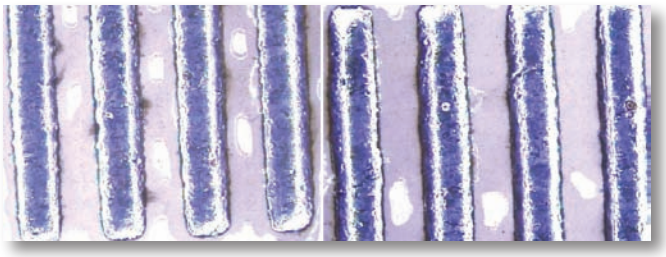

Figure 11: ImAg: 3 hours 76% RH and 3 hours 90% RH.

Solder Ball

A test vehicle with 100mm CuOSP pads was selected. Solder balls are typically increased if the printed solder paste deposit infringes onto the solder mask. To challenge the solder paste, stencil apertures were also incorporated to purposely overprint onto the solder mask. Stencil apertures for the experiment were 75, 100, 125, 175, 225 and 275mm so that the later aperture openings overprinted the 100mm pads (Figure 12).

The results were very favorable with only one solder ball at 225mm stencil aperture (ratio 1.0/2.25) and two solder balls on the largest overprint 275mm stencil aperture (ratio 1.0/2.75).

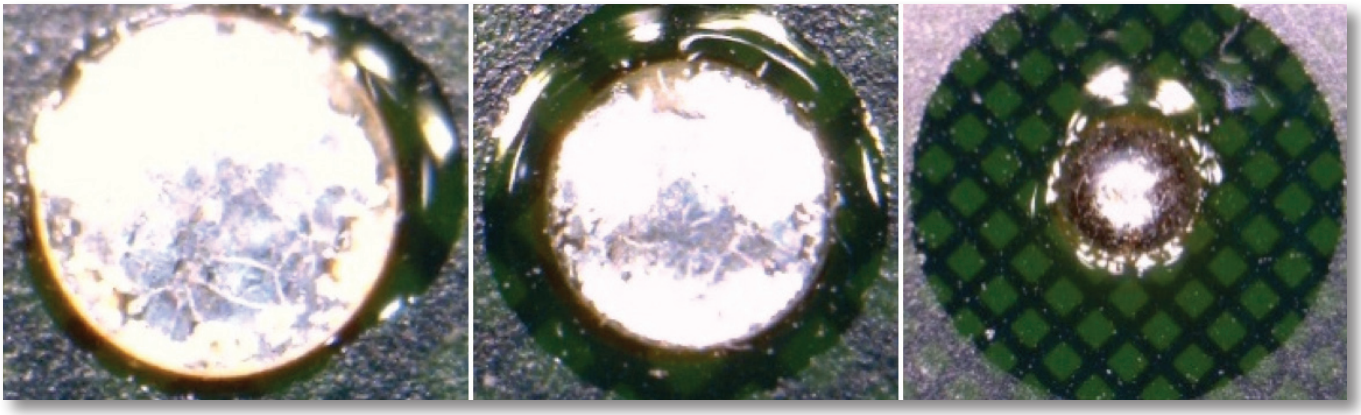

Figure 12: 100mm (1.0/1.0) on left, 175mm (1.0/1.75) in middle and 225mm (1.0/2.75) on right.

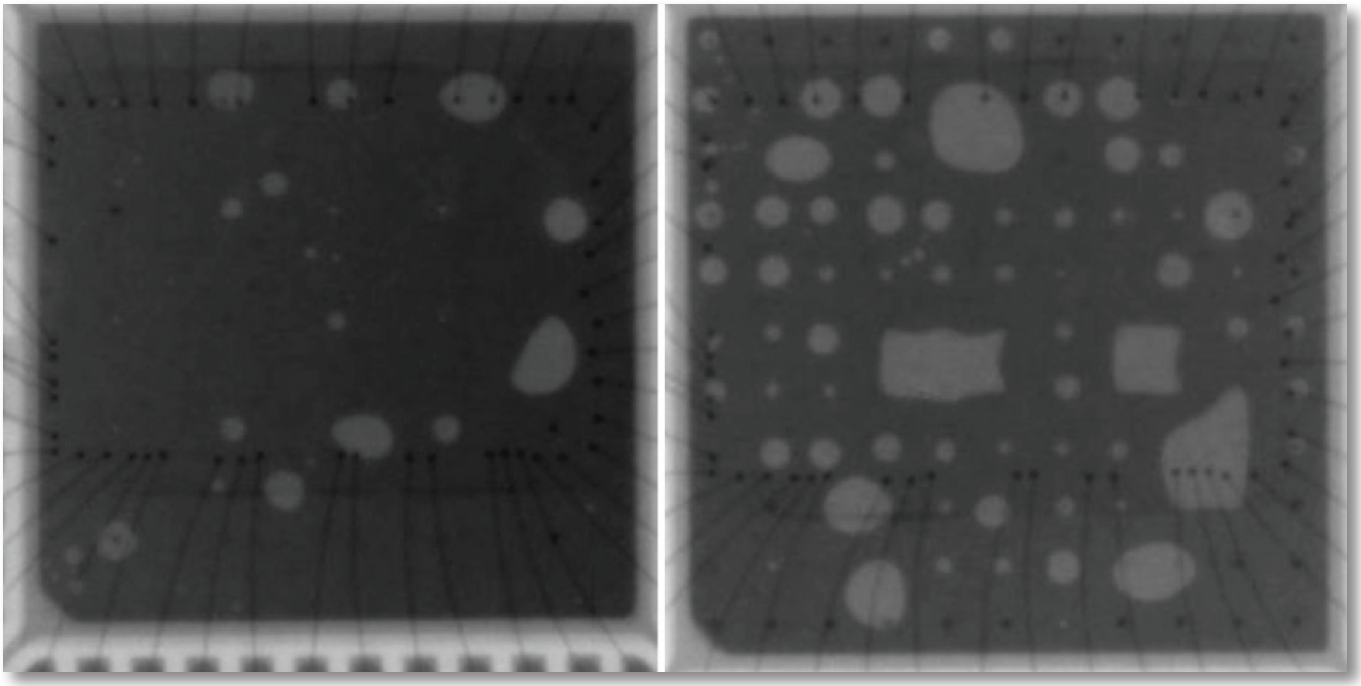

Figure 13: Pattern 1 - 5 x 5 via pattern on left. Pattern 2 - 11 x 11 via pattern on right.

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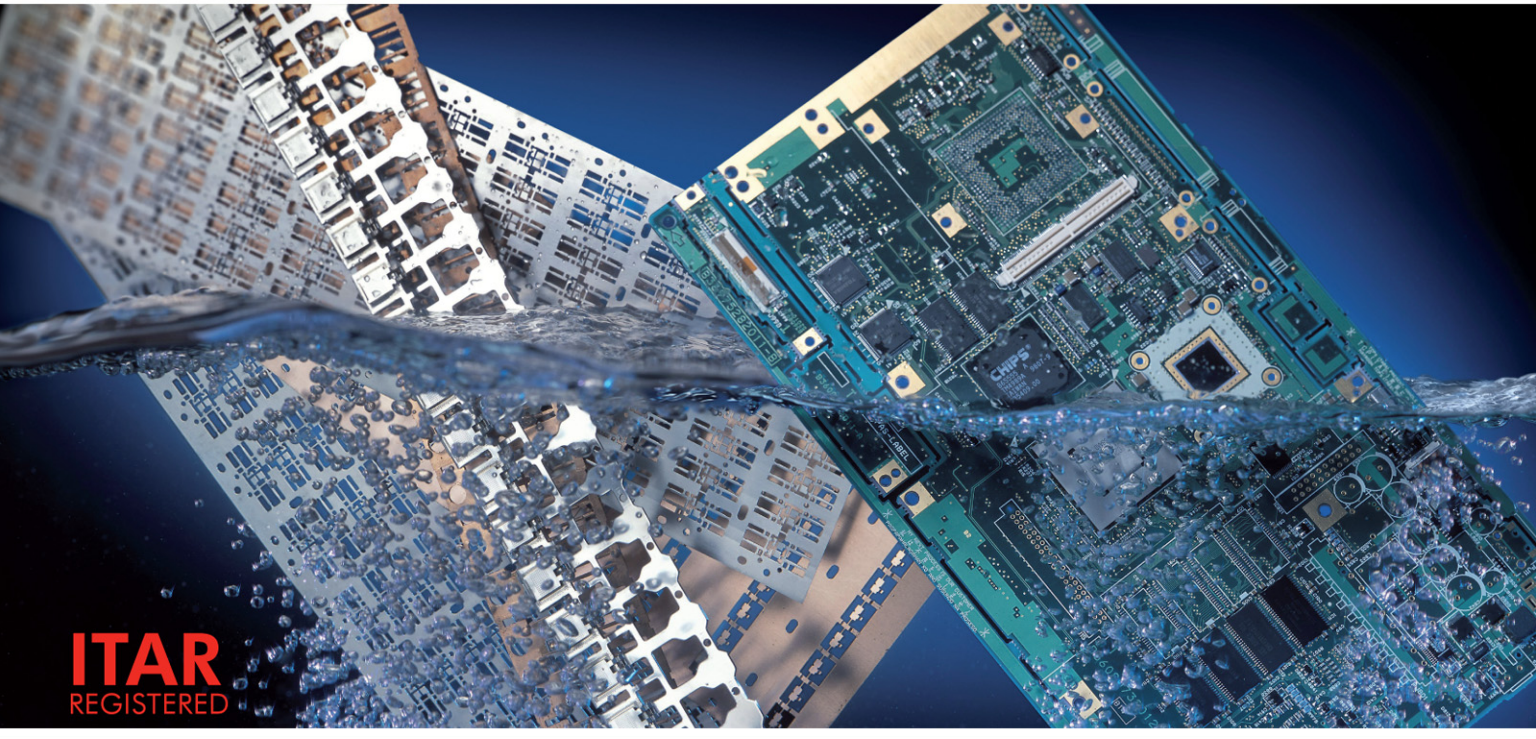

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Voiding

The test vehicle utilized 6mm x 6mm QFNs, ImAg finish, with via-on-pad. The solder paste was printed 1:1 to observe the worst-case scenario in regard to voiding. The components were then reflowed and X-rayed to observe the voiding. Examples of the results are shown in Figure 13. The results were actually quite good on the 5 x 5 pattern of vias, the 11 x 11, though not as good, was typical compared to lead-free SAC alloys. SMT

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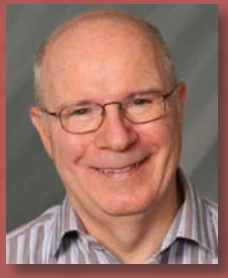
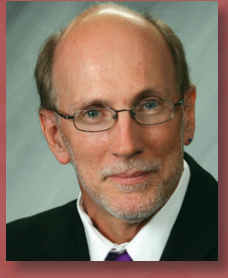
3. ASME Technical Paper 95-WA/EEP-4.

4. "Strength and Fatigue Behavior of Joints Made With Bi-42Sn-1Ag Solder Paste: An Alternative to Sn-3.5Ag-0.7Cu for Low Cost Consumer Products," Valeska Schroeder, Fay Hua and J. Gleason.

5. "Fine Powder Solder Pastes: Stencil Printing and Reflow in Lead-Free Assembly," Chris Anglin, Ed Briggs, Tim Jensen and Ron Lasky.



Dr. Ron Lasky is a Senior Technologist at Indium Corporation and a Visiting Professor at Dartmouth College. Additionally, he has over 20 years experience in electronic and optoelectronic packaging at IBM, Universal Instruments and Cookson Electronics. Dr. Lasky has authored or edited five books on science, electronics and optoelectronics and numerous technical papers. He has also been an adjunct professor at several colleges and has taught over 20 different courses on topics ranging from electronic packaging, materials science, physics, mechanical engineering and science and religion.



Ed Briggs is a Technical Support Engineer with Indium Corporation where he has worked for over 19 years. He has an AS Degree in Chemical Technology from Mohawk Valley Community College where he won the Douglas J. Bauer Award for Excellence in Chemistry. He is an SMTA-certified engineer and has earned a Green Belt Six-Sigma Certification from Dartmouth College for demonstrated proficiency in developing and executing design experiments to support continuous process improvement. Briggs is also certified as an IPC-A-600 and IPC-A-610D specialist.

Brook Sandy is a Product Support Specialist for PCB Assembly Materials in Indium Corporation's Solder Products Business Unit. She acts as a technical liaison between customers and internal departments, such as R&D and production, to insure the best quality and selection of products. She also provides support in improving informational materials to assist PCB assembly materials customers. She previously worked in R&D, developing conductive adhesives for die- and strap-attach, as well as conductive inks for RFID applications. Her areas of expertise include analytical testing of conductive materials, applications such as screen printing and jet dispensing (jetting), as well as scale-up and pre-production of developmental materials.

Video Interview

Novel BGA Technology from Molex

by Real Time with...IPC APEX EXPO 2011

Molex Process Engineer Jim Hines describes a novel approach to creating improved solder connections for BGAs. Hines tells Guest Editor Joe Fjelstad about the paper he presented at APEX which compares solder charge to BGA and other reflow technologies.

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Delta's Florida Facility Earns AS9100 Certification

Delta Group Electronics, Inc. announced today that its Florida facility has received the highly-regarded AS9100 quality designation by Underwriters Laboratories, Inc. (UL). With this certification, Delta Group has earned AS9100 certification at four of the company's five operations. All facilities are also ISO9001:2008 certified.

The ISO 9000 Series Standard is an internationally-recognized quality management system developed by the International Organization for Standardization (ISO). The ISO 9001:2008 registration defines the quality system requirements for a company to achieve the expectations of its customers and to provide a culture focused on continued quality improvement. Developed in 1997 by the American Aerospace Quality Group to promote quality standards across all aspects of air transportation, the AS9100 standard is directly aligned with the ISO 9001 requirements. The AS9100 registration contains additional requirements, clarification and interpretation of a company's quality system.

Delta Group Electronics initiated its quality certification process in 2000 and completed this first stage in 2001 by receiving ISO 9001:2000 designations at each of its then three facilities in New Mexico, California and Florida. To meet the needs of its customers and to enhance its overall quality system, Delta Group pursued the AS9100 upgrade such that the California, New Mexico, Arkansas and Florida facilities are now operating under this registration, with and Texas operating under the ISO 9001:2008 registration.

Founded in 1987, Delta Group Electronics, Inc. is a full-service EMS company offering turnkey services for its customers in the aerospace, defense and commercial industries. For more information, visit www.deltagroupinc.com.

JISSO INTERNATIONAL COUNCIL Celebrates Global Standardization Progress

by Dennis Fritz and Joseph Fjelstad

IN SUMMARY

The JIC has redefined the electronic interconnection hierarchy in terms of Jisso levels. Providing a universally agreed-upon set of terms and definitions and approaches will allow for seamless pathways to technological solutions between users and suppliers relative to the interconnecting, assembling, packaging, mounting and integrating of system designs for all manner of electronic products.

The Jisso International Council (JIC)—comprised of Asian, European and North American Jisso councils and supported by all major electronics industry trade and technology associations, including IPC, JEITA, iNEMI, JEDEC, EIPC, JPCA and others—recently completed its 12th annual meeting. The major council, co-chaired by Masahide Okamoto of Hitachi representing the Jisso Japan Council, consists of Bernd Roemer of Infineon, representing the Jisso European Council, and Denny Fritz of McDermid representing the Jisso North America Council. The meeting was held in College Park, Maryland, at the University of Maryland CALCE Center. Mike Osterman of CALCE was the host. Now, after 12 years of a quiet behind-the-scenes effort, this group of highly-dedicated engineers and managers, representing electronic companies from around the world and who make up the JIC, is poised to pay important dividends to the electronics industry.

The mission of the JIC is to promote a strategic partnership among organizations interested in the total solution for interconnecting, assembling, packaging, mounting and integrating system design. This is accomplished, in part, by providing a universally agreed-upon set of terms and definitions and approaches to allow for seamless interfaces and pathways to technological solutions between users and

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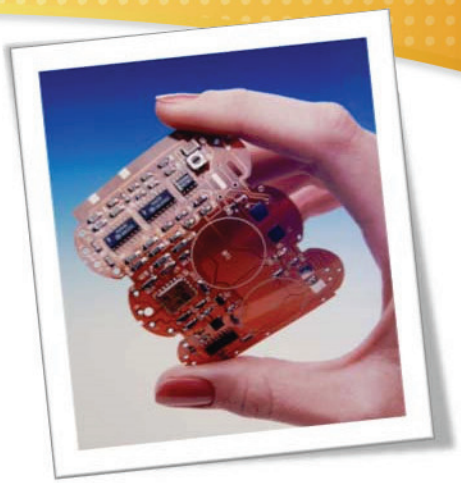

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suppliers relative to the interconnecting, assembling, packaging, mounting and integrating of system designs for all manner of electronic products. It has not been a simple task reaching the agreements that have been made to date, and there are still rough edges that will require polishing, but the concepts are key in helping the electronics industry navigate a less turbulent course to the future.

For any such effort to meet with success requires a lot of communication and cooperation. It also involves the knocking down and rebuilding of some "older" conventions. One of them is the redefining of the hierarchy of interconnections. A debt of gratitude is owed to those who clearly defined interconnection hierarchy of the past, but the terms are no longer sufficient to embrace the changes of the last decade. As a result, the JIC redefined the electronic interconnection hierarchy in terms of Jisso levels. The term "jisso" is a Japanese word which roughly translates to "mounting," but has been adopted in Japan for use in describing electronics manufacturing because electronics are commonly produced through a sequence or series of mounting and interconnecting steps, thus the term is an apt and useful one in any language.

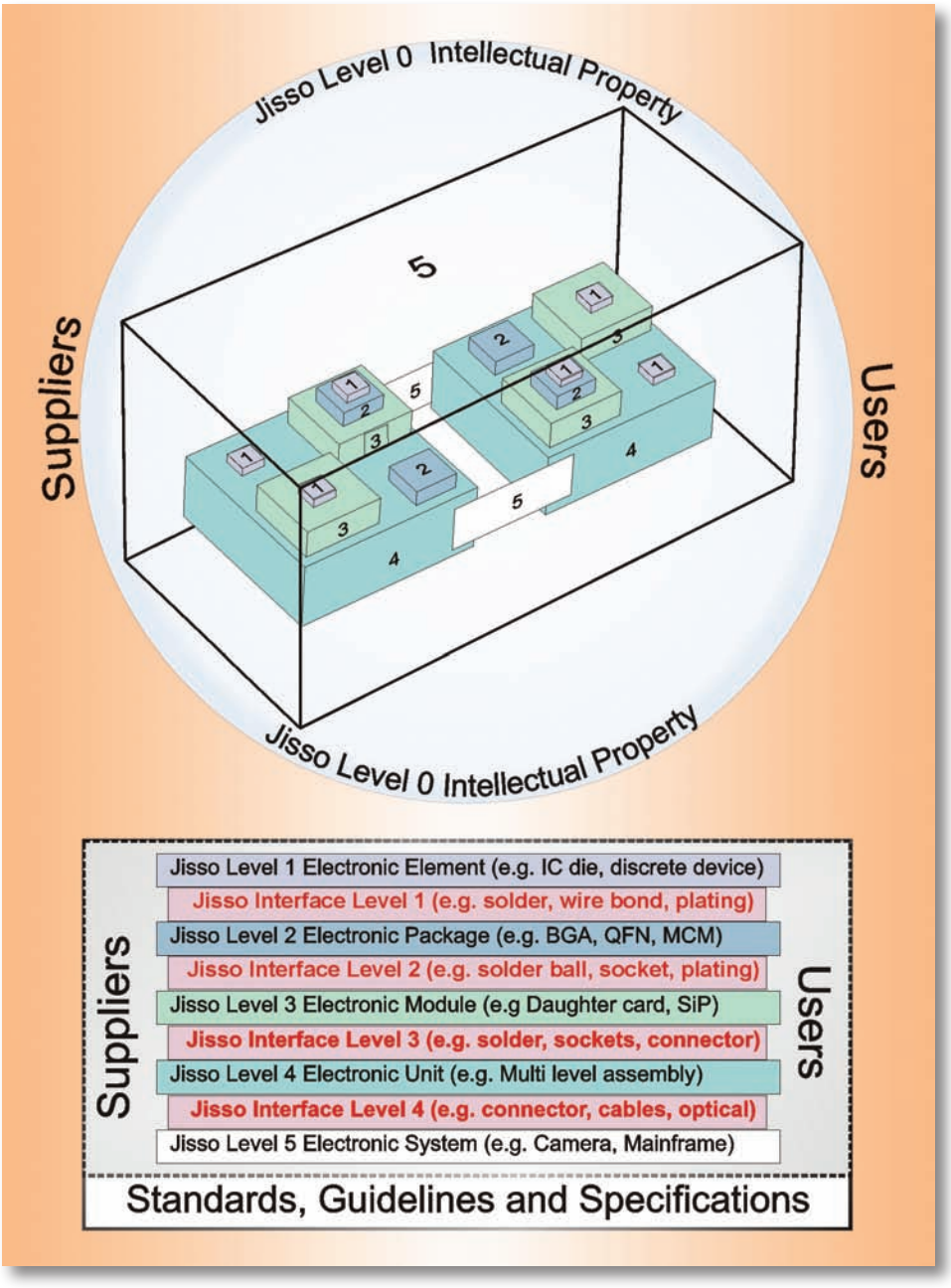

Figure 1: The Jisso concept embraces all aspects of electronic interconnections and seeks to harmonize standards and communications between supplier and users. Beginning at Jisso Level 0, Intellectual Property, which encompasses all other Jisso levels 1 through 5, including both structures and interconnection technologies, the Jisso International Council hopes to improve understanding between and among the global electronics interconnection industry participants.

The JIC plans to promote the basic concepts and secure global participation in use of JIC structures. The intent is to start with industry, but then to also reach out to those in education and to those reporting

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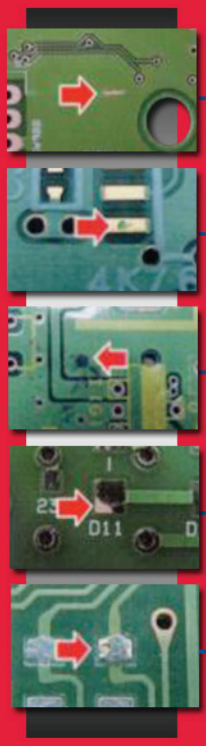

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on the industry. This will allow the industry to communicate with clarity presently missing, especially given the explosion of interconnection solutions. The reader is invited to read and begin to make use of the following terms and definitions.

Level 0 — Intellectual Property

The intellectual property of an item pertains to the idea or intelligence imported or described in a formal document (protocol, standards and/or specifications), design entity or patent disclosure.

- The information may be in hard or soft copy and can include computer code or data format as a part of the descriptive analysis.
- The characteristics are described as to their physical, chemical, electrical, mechanical, electromechanical, environmental and/or hazardous properties.

Level 1 — Electronic Element

Uncased bare die or discrete components (e.g., resistor, capacitor, diode, transistor, inductor or fuse), with metallization or termination ready for mounting.

- This can be an IC or discrete electrical, optical or MEMS element.
- Individual elements cannot be further reduced without destroying their stated function.

Level 2 — Electronic Package

A container for an Individual Electronic Element or Elements which protects the contents and provides terminals for making connections to the rest of the circuit.

- The Package outline is generally standardized or meets guideline standards.
- The Package may function as electronic, optoelectronic or MicroElectroMechanical Systems (MEMS), or System in Package (SiP) and may in the future include Bio-electronic sensors.

Level 3 — Electronic Module

An electronic sub-assembly with functional blocks, which is comprised of Individual Electronic Elements and/or Component Packages.

- An individual module having an application specific purpose including Electronic, (including SiP), Optoelectronic or Mechanical (MEMS).
- The module generally provides protection of its elements and packages, depending on the application to assure the required level of reliability. The Module may be a Company standard (catalog item) or Custom (OEM specific).

Note: There will likely be some subdivisions of Level 2 and Level 3's descriptions to increase the granularity and clarity relative to what is included within each of these levels.

Level 4 — Electronic Unit

Any group of functional blocks that have been designed to provide a single or complex function needed by a system in order for the system to serve a specific purpose. The Electronic Unit may be comprised of Electronic Elements, Component Packages and/or Application Specific Modules. The function of the Electronic Unit may be electronic, optoelectronic, electromechanical or mechanical, or any combination thereof. The function may in the future include bio-electronic applications.

Level 5 — Electronic System

A completed, market-ready unit dedicated to combining and interconnecting functional blocks. The functional blocks are generally comprised of Electronic Units, but may also include Electronic Modules, Electronic Packages or Electronic Elements. The Electronic System Product can include the cabinetry, a backplane or motherboard into which the Assemblies, Modules, Packages or Elements are inserted and the cabling (electrical, optical or mechanical) needed to interconnect the total functional block(s) into a configured system. The electronic system can vary in complexity


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from very simple to highly complex.

In summary, the JIC, after seven years of discussions, has defined a comprehensive framework and structure for harmonizing the global electronics manufacturing industry infrastructure. These concepts have been met with the approval of standards bodies such as the IPC, JEDEC and JEITA and numerous companies in Asia, Europe and the Americas; however, ultimate success will depend heavily on the participation, beginning on a grass-roots level, of everyone in the global electronics industry. It is hoped that the reader will actively embrace these concepts. Comments and suggestions on Jisso are solicited and welcomed by the JIC. A Web site sponsored by the IPC is up and more information will be added on a regular basis to keep the industry informed. Reports from the meeting in Berlin, Germany, will be circulated shortly so keep your eyes on the Web site. **SMT**

Joe Fjelstad, a founder of Silicon Pipe Inc., is an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 150 U.S. patents issued or pending. He is the author of "Flexible Circuit Technology" and author, co-author or editor of several other books including "Chip Scale Packaging for Modern Electronics." He has also authored numerous technical papers and articles. He frequently presents seminars on PCB, flex circuit and chip scale packaging technologies at industry conferences.

Dennis Fritz is a part-time Senior Engineer with SAIC, Inc. in Merrillville, Indiana where he deals with the impact of lead-free electronics on DoD electronics. He also interfaces with Purdue University at both the Lafayette and Hammond campuses as they assist in this lead-free research with graduate student projects. Technical direction for the SAIC work comes from Naval Surface Warfare Center, Crane, Indiana.

ZESTRON Wins Best Paper Award at SMTA China

ZESTRON North Asia's Process Engineer Jerry Ji was awarded the Best Paper of Technology Conference One (CE11) for his presentation of the technical study titled "pH-Neutral vs. Alkaline Cleaning Agents" at the SMTA China East Technical Conference during NEPCON Shanghai.

This collaborative study, conducted by ZESTRON's worldwide engineering team, was prompted by recent industry trends and conducted to compare the cleaning effectiveness of pH-neutral and alkaline technologies at low operating concentrations as well as their effects on material compatibility.

During the past few years, significant changes in solder paste formulations and assembly processes have occurred. Post reflow residues of tin-lead and newer lead-free soldering materials are more difficult to remove due to increases in component density, larger component packages, higher lead counts, finer lead spacing and lower standoffs. While modern aqueous alkaline cleaning agents effectively remove these flux residues, achieving satisfactory results often requires an increase in temperature, exposure time, chemical concentration, and mechanical energy. This often presents a new set of challenges in the area of material compatibility.

With the emergence of pH-neutral defluxing technologies in early 2009, these formulations promised to set a new standard for material compatibility, while proving valuable to those who worked toward environmentally sound processes. As a result, potential users are very interested in assessing the differences between alkaline cleaning agents and the newer pH-neutral products, with regard to both, cleaning performance and material compatibility.

"This award demonstrates that ZESTRON's continuous research work meets current industry demands." says Dr. Harald Wack, President of ZESTRON worldwide.

If you would like to review this paper or have any questions on "pH neutral vs. alkaline," please contact Jerry Ji at: j.ji@zestronchina.com.

Headquartered in Manassas, Virginia and operating in over 35 countries, ZESTRON is the leading global provider of precision cleaning products and services. For additional information visit www.zestron.com.

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- 80% go to see new products and find new suppliers
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- 76% report that the show influences their buying decisions

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Randy Cherry, principal engineer, Tellabs, Inc.

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Source: Embassy Suites Hotels' Third Annual Business Travel Survey

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Bob Black, president & CEO, Juki.

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The Value of JIT-Structured On-the-Job Training

Courtesy of Blackfox

IN SUMMARY

Companies are discovering that "structured" on-the-job training provides many benefits for short- and long-term success. Such training is designed to prepare employees for job performance through task-oriented training conducted by qualified instructors in the actual work environment. By using a just-in-time approach, employees receive the knowledge and skills required to be productive their very first day.

To be competitive in today's manufacturing environment, assembly accuracy, consistency and flexibility are more important than ever. You need to train your employees, and train them quickly, and you need to find a low-cost, yet effective way to offer such training. You also need to improve morale and develop responsible, loyal, high-performing employees. Plus, you know that the old way of training people on the job, i.e., the buddy system, "follow Joe around" or unstructured on-the-job training (OJT), simply does not work.

Companies are discovering that "structured" OJT provides many benefits for short- and long-term success. OJT is designed to prepare employees for job performance through task-oriented training conducted by qualified OJT instructors in the actual work environment. By using a just-in-time (JIT) approach, employees receive the knowledge and skills required to be productive their very first day.

Structured Versus Informal OJT Systems

For some, OJT is defined as a "buddy" assigned to the employee to mentor them during the first few days on the job. In many insistences, the buddy has not received adequate training himself and is required to produce product before being fully

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- The Prototron employees I have come in contact with are very professional and considerate.

We continue to work with other vendors for pricing, etc., but remain a loyal Prototron customer.

John Martin
Electronics Lab Manager
Badger Meter, Inc.

...and of course the customer is always right!

competent. This often leads to the transfer of bad habits and a trial-by-fire method of job training where employees are forced to learn a job on their own, receiving guidance only when they make a mistake. Learning is less effective and the transfer of knowledge is only temporary or incorrect when employees learn by observing another employee or through informal instruction, leading to sub-standard quality and frustration.

A "structured" OJT training method includes experienced trainers taking new employees under their wings, instructing and coaching them JIT on how to perform their job, giving them the benefit of years of experience using a documented, consistent training system. Instruction plans and job aids provide a road map for repeatable, sustained knowledge creation and learning.

A planned and documented approach to implement an OJT system will provide designated OJT specialists the tools to become successful trainers and leaders on the plant floor. When properly trained and supported, an OJT specialist can reduce training times and learning curves in excess of 50%.

Elements of Successful OJT Systems

Structured OJT programs, over time, will lead to the creation of permanent organizational knowledge. This is accomplished when all job functions are included as part of the OJT system. Included in the OJT program is a clear understanding of the criteria for success in the processes, procedures, troubleshooting and problem solving and quality inspection.

Some of the key OJT system goals include repeatable and sustainable performance, reduced learning curves, measurable and sustainable results, longer retention of knowledge and skill and continual and effective change.

All training topics or elements are linked systematically with feedback loops to evaluate conditions for success. Updates to training material or job-aids and frequent coaching and mentoring sessions for employees on the plant floor will also enhance the learning effectiveness.

Implementation of OJT System

In order to implement a successful OJT system, standards of performance must be developed that clearly link back to the employee job location. These standards must be validated with a job analysis processes, including the use of a detailed functional position descriptions.

Effective standards of performance and related materials for use by the OJT specialist are also developed to ensure consistent delivery/transfer of information by all trainers.

JIT System Benefits

The Blackfox JIT system is a team-driven model for developing a structured OJT program that meets or exceeds quality management system requirements. The model empowers all employees to work together to determine training needs and agree on the best way to perform their jobs. They design, develop, implement and evaluate the training. Employees participate as members of design teams, approval teams, design team facilitators, OJT trainers, administrators and in-house advocates.

Studies show that adults will not learn unless they are highly motivated, and they are not motivated if they think they will not need the information.

By targeting the "need to know" training to motivate people, the quality of learning can be improved. This idea is called JIT training as opposed to "just-in-case" training, which, until now, has been the traditional method of classroom training. The methodology is to

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coach our customers' team how to implement, maintain and deliver a targeted, low-cost, high-impact, results-oriented program.

The approach:

- Involves and empowers employees;
- Improves teamwork;
- Improves attitude;
- Improves communication;
- Improves decision-making;
- Creates a true workplace learning environment;
- Creates the capability for future problem solving;
- Ensures employee buy-in to processes and procedures;
- Improves employee job satisfaction;
- Shortens development time by spreading a lot of work over several people; and
- Improves workload management.

Summary

The structured JIT System has been proven to be the most effective, efficient method of learning job skills to increase productivity and quality:

- **Implemented by Your Team** – You will learn how to build the JIT infrastructure. It draws on the power of the team to deliver targeted, low-cost, high-impact results.
- **Studies indicate** that approximately 90% of employee knowledge is learned on the job.
- **Learning is immediately** relevant to the work, whether it deals with materials, information or services.
- **Systematic** – Planned, prioritized, and documented. It is always compliant with ISO requirements.
- **Progressive Investment Structure** – Invest only in what you want and need. It costs time and effort, but "if you think training is expensive, try not training."
- **Versatile** – Can be successfully implemented in any job function, in any industry. SMT

IPC Capitol Hill Day to Discuss Key Industry Issues

Government over-regulation, export controls and maintaining the military and aerospace sectors' use of U.S. electronic interconnect manufacturing capacity are just some of the key issues that will be addressed at the IPC Summit on American Competitiveness and Capitol Hill Day, June 15-16, 2011, in Washington, D.C. Electronics manufacturers will hear from Washington insiders such as former U.S. Representative David McIntosh, a leader in efforts to address government over-regulation, as well as industry leaders on critical issues that directly impact the U.S. electronics industry's ability to compete globally.

Burdensome regulations issued by the U.S. EPA, OSHA and the Securities and Exchange Commission (SEC) are impeding electronics companies' competitiveness by imposing costly and unnecessary regulatory burdens. Rep. McIntosh will discuss how Congress can address government over-regulation to make businesses more competitive.

Other regulatory briefings will include presentations on the impact of the conflict minerals regulation and export control regulations. Ben Cohen, chief counsel of Litigation and Washington D.C. Operations for The Boeing Company, will discuss the complexities of implementing Section 1502 of the Dodd-Frank Wall Street Reform and Consumer Protection Act of 2010.

Attendees will also hear from an expert industry representative on how the U.S. government's reform of the export control system will affect U.S. electronics manufacturers' global competitiveness. The reform process is ongoing but should be finalized by the end of the year. It is critical for legislators to understand the importance of protecting the information contained in printed board assemblies that are specifically designed for items listed in the International Traffic in Arms Regulations (ITAR).

Participants will be able to immediately take action to address these issues by visiting their legislators in meetings set up by IPC staff. These face-to-face meetings enable participants to establish valuable relationships with their representatives, educate them on the issues that directly impact the U.S. electronics industry's ability to compete globally and gain their support.

For more information or to register for IPC Capitol Hill Day, click this link. Due to scheduling deadlines for special luncheon and reception events held in conjunction with NAM, IPC cannot accept registrations after June 9, 2011.

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NEPCON China Review

IN SUMMARY

In addition to show floor activities, a number of technical sessions were offered at NEPCON China. Organized in cooperation with the SMTAI, the conference program provided attendees a wide range of topics. The 5th annual SMT China Vision Awards were also presented.

by Barry Matties
I-CONNECT007

More booths, larger footprints and happy exhibitors were the overall themes for this year's NEPCON China. Held at the Everbright Convention center in Shanghai, China, this year's show was another success for the Reed Group. Though Reed was hoping to be in a new venue this year, they were stuck at the Everbright for this year's show.

The show is scheduled for a new venue located in Pudong next year. The exhibitors I spoke with are really looking forward to the new venue, as the Everbright is an older complex with an awkward floor plan. Despite these issues, this year's show was bursting at the seams. With more than 500 exhibitors, it seemed that every available booth space was utilized; even the breezeways between halls had booths lining the edges.

The first day of the show was very busy, but the second day was packed. The last day landed on a Friday this year and the attendance drooped precipitously. Even though the last days of shows are typically slower, it seems that the change from previous years, ending on a Thursday instead of Friday, had many departing for the airports Friday morning. Despite that, most attendees felt the show was a success.

The show floor offered plenty to see. The mega booths were packed with equipment and armies of sales and technical staff. The smaller booths were busting with equipment, too. With the continued labor and capacity pressure in China, throughput was the theme of the showcased technology. On the main floor, a new live demo would take place every few minutes. Even if you were at the other end of the large show you could hear their sales pitches, as there didn't seem to be any rule in place for decibels reached on the show floor. They really had to be very loud as they were competing with all of the other noise on the show floor—machines running, video monitors blaring marketing messages, music playing, air compressors and people talking—yet the battle of decibels raged on. Despite it all, the messages seemed to get through as equipment deals were made. I don't think I have ever attended a show louder than this one.

Aside from the show floor activities, there were a number of technical sessions taking place. Organized in cooperation with the SMTAI, the conference program provided attendees a wide range of topics. The 5th annual SMT China Vision Awards were also presented.

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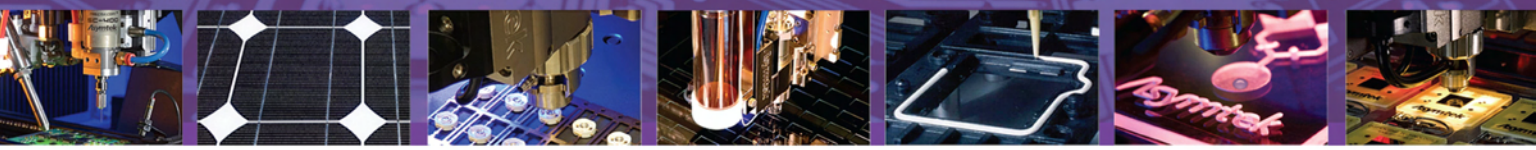

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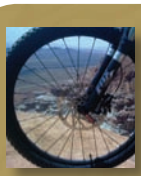
Shenzhen Desen Precision Machine Co., Ltd.	DSP-3008 Semiconductor-Level, Full-Auto Solder Paste Printer
Nordson ASYMTEK	Nordson ASYMTEK Jet Dispenser for Side-View LED Manufacturing
Micronic Mydata (Shanghai) Co., Ltd.	MY100HXe with MY100DXe solution
Speedline Technologies Asia PTE Ltd.	OmniES Reflow Soldering
Sun East Electronic Technology (ShenZhen) Co., Ltd.	IPC-8 (Genesis 8) Series Reflow Soldering
Sun East Electronic Technology (ShenZhen) Co., Ltd.	Peak Series Lead-free Wave Soldering
Speedline Technologies Asia PTE Ltd.	Aquastorm® 200 Stainless Steel In-line Cleaning
Machine Vision Products, Inc.	Spectra
ZhenHuaXing Technology (Shenzhen) Co., Ltd.	In-line VCTA-A586 AOI
ALeader Vision Technology Co., Ltd.	ALD700DL
Nordson DAGE	XD7600NT Diamond FP X-ray Inspection System
Shenzhen Unicomp Technology Co., Ltd.	UNICOMP AX8200 Inspection Machine
Agilent Technologies	Agilent M9186A PXI-based Versatile Voltage/Current Source Measurement Module
DEK International	ProActiv
SITECH Electronics Technology Co., Ltd.	Intelligent Management System
Micronic Mydata (Shanghai) Co., Ltd.	MYCenter
Cookson Electronics - ALPHA	ALPHA®EF-6850HF Soldering Flux
Cookson Electronics - ALPHA	ALPHA® Telecore XL-825 Lead-Free Cored Solder Wire
Henkel Adhesive Technologies-Electronics	Macromelt® OM341
DEK International	Nano-Protek
Sun East Electronic Technology (ShenZhen) Co., Ltd.	IPC-8 (Genesis 8) Series Reflow Soldering
DEK International	DEK Horizon 03iX

It is clear to see why trade shows are an important part of any industry. There really is no substitute for the business conducted, in person, at the event. Congratulations to all the winners of the SMT China Vision Awards, we look forward to visiting NEPCON China next year at the new venue. **SMT**

Visit RealTime with...Nepcon 2011 for our coverage of this year's event.



Barry Matties started in PCB manufacturing in the early 80s. In 1987, he co-founded *CircuiTree Magazine*. Nearly 13 years later, *CircuiTree* was sold as the leading publication in the industry. In the early 2000s Barry and his former *CircuiTree* partner, Ray Rasmussen, joined forces again and acquired PCB007. Over the years, PCB007 has grown and continues to thrive. In July of this year, Barry and Ray acquired *SMT Magazine*. With his many years of business leadership skills, Barry now produces this column for anyone who has a desire for success. The column relates 25 years of successful business leadership, including marketing and selling strategies that really work. Read a few and decide for yourself.

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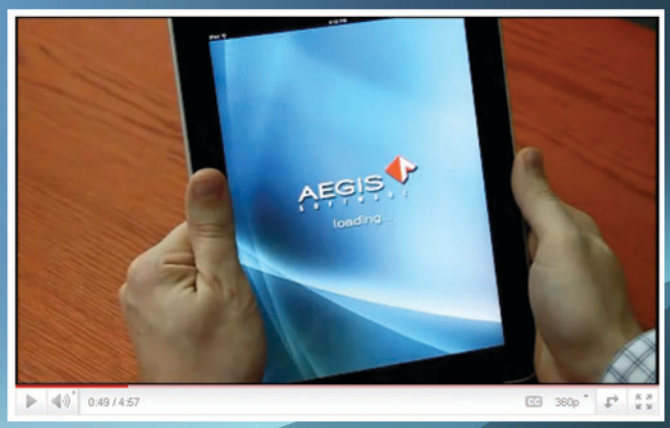

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Most-Read News Highlights from SMTonline this Month

1 IPC: Guidelines for Design, Assembly Process for BTCs

Assemblers who have tried to resolve problems that stem from the rapidly growing array of advanced packages are getting help from IPC with the newly released IPC-7093, Design and Assembly Process Implementation for Bottom Termination Components.

2 Aegis Unveils iPhone/iPad Offerings at APEX

Aegis Software unveils its next industry-first technology in the form of the only iPad- and iPhone-integrated manufacturing software system for electronics assemblers.

3 IPC Honors Best Technical Papers at APEX

IPC has announced the winners of this year's Best U.S. and International Papers at IPC APEX Expo, held April 12-14, 2011, in Las Vegas, Nevada. The event's Technical Program Committee selected the winners through a ballot process.

4 Plexus Demonstrates Excellence in Lean Sigma

"We recognize that continuous improvement will play a key role in Plexus' ongoing success and, as such, it is an integral part of our strategy. Hosting the Best Practice Event enables Plexus to share our global expertise in lean sigma with other companies," said Willie Mackinnon, Senior Director of Operations - EMEA.

5 Sanmina-SCI Reports Revenue of $1.57 Billion for Q2

Revenue for the second quarter was up 2.7% to $1.57 billion, compared to $1.53 billion for the same period of fiscal 2010. "We believe demand is improving and the second half of fiscal 2011 will be stronger than the first half," stated Jure Sola, Chairman and CEO.

6 Celestica to Boost Toronto Workforce by 40%

Celestica Inc. plans to increase its Toronto workforce by 40% as demand for the company's diversified manufacturing services picks up, Chief Executive Craig Muhlhauser told reporters.

7 Molex Reports Q3 Results, Dividend Increase

Revenue for the March 2011 quarter of $874.5 million increased 16% from the March 2010 quarter and declined 3% from the December 2010 quarter.

8 Sparton's EMS Segment Suffers Sales Drop for Q3

EMS sales for the three months ended March 31, 2011 decreased approximately $0.8 million as compared with the same quarter last year. This decrease primarily reflects certain program losses, primarily with two customers, partially offset by increased inter-company sales.

9 Plexus Reports Record Revenue of $568 Million

"Fiscal second quarter revenues were a record $568 million with EPS of $0.59. Both revenue and EPS were consistent with the high-end of the guidance range we provided last quarter," said Dean Foate, President and CEO.

10 New No-Clean Flux from Henkel

Designed with modern manufacturing requirements in mind, Henkel Electronic Materials has formulated Multicore MF210, a no-clean sustained activity flux that is compatible with both lead-free and tin-lead processes. The halide-free, resin-free material is effective with a wide range of solder resists, as well as rosin and OSP-based protectants for maximum adaptability.

SMTonline

EVENTS

For the IPC's Complete Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar, click here.

For a complete listing of events, check out SMT Magazine's full events calendar here.

MILESTONE
June 2011
Baltimore, New England, Los Angeles

JPCA Show
June 1-3, 2011
Tokyo Big Sight, Japan

Space Coast Chapter Expo, Technical Forum and Barbeque
June 9, 2011
Melbourne Auditorium, Melbourne, Florida

IPC Summit on American Competitiveness
June 15-16, 2011
Washington, D.C.

IPC International Conference on Flexible Circuits
June 21-23, 2011
Minneapolis, Minnesota

Energy Harvesting & Storage Europe 2011
June 21-22, 2011
Munich, Germany

Wireless Sensor Networks & RTLS Europe 2011
June 21-22, 2011
Munich, Germany

NEPCON Thailand
Jun 23-26, 2011
BITEC, Bangkok, Thailand

Assembly Technology 2011
June 23-26, 2011
BITEC, Bangkok, Thailand

LEDforum Shanghai 2011
July 6-7, 2011
Jumeirah Himalayas Hotel Shanghai, 1108 Meihua Road, Pudong Xinqu

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Ad Index

Next Month in SMT Magazine

Don't miss the July issue of SMT Magazine: ***Thermal Management: Beat the Heat,*** featuring articles to help you design and manufacture with heat in mind, offering new strategies for heat management and materials for heat dissipation.

Look for articles on thermal stress from Henkel, the Rochester Institute of Technology, columnist Karl Dietz and more, which round out our feature coverage. Also on deck, we bring you a Green Guides article, part one of a two-part article from Vern Solberg's ***PCB Designer's Notebook,*** offerings from Saturn Electronics, Zestron and more. Great summertime reading is coming your way this July!

Don't miss an issue; be sure to subscribe to SMT Magazine today if you haven't already done so. It's easy, it's free and the link is right here.