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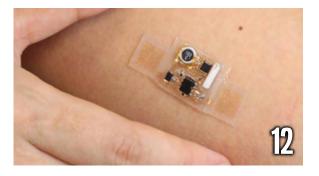




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FEBRUARY 2019 • FEATURED CONTENT

DESIGNOOT



Everything is a **Substrate**

Technological advances have made it possible to print circuits on all sorts of traditional and non-traditional substrates, and even materials not considered substrates. What does a PCB designer need to know in order to design circuits on these alternative materials? We asked our expert contributors to share their insights into printing circuits on some non-traditional materials.

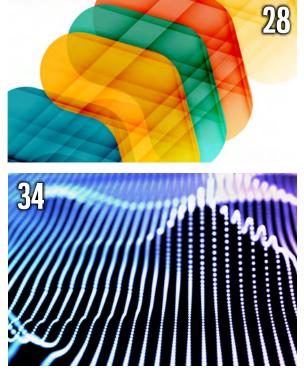
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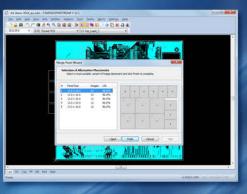
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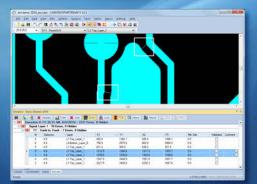


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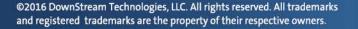


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The Future on Display at DesignCon

The Shaughnessy Report by Andy Shaughnessy, I-CONNECTO07

It's always nice to get out of the wintry East Coast in January, and once again, DesignCon was calling my name. Every year, 5,000 or so engineers descend on the Santa Clara Convention Center for this signature industry event.

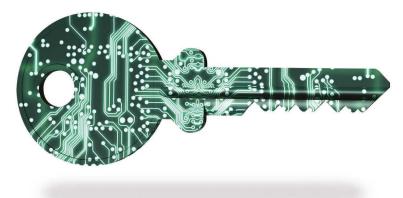
This may have been the biggest show yet; there were packed aisles for much of the show with very few down times, even on the afternoon of the second day. Show managers UBM put on an ambitious event with over 100 sessions in the 15-track conference program as well as almost 200 exhibitors.

Every DesignCon has an unofficial theme; a few years ago, it was the "Jitter Show." This year may have been the year for PAM4, fourlevel pulse amplitude modulation, which was the topic of a variety of presentations and one panel discussion. Used by the SerDes engineers who dwell in the 112 Gb/s arena, PAM4 data has three separate eyes and four levels, so it's a whole different ballgame. There's currently a back-and-forth discussion between design engineers about whether PAM4 is even necessary.

Another big topic at DesignCon was 5G—one of the main components of IoT. Some engineers I spoke with said they were still searching for the perfect laminate for 5G, which is up to 1,000 times faster than 4G and features super-high bandwidth and low latency. There are still a lot more questions than answers regarding 5G. There was a little bit of political talk with engineers worrying about Huawei's dominance of the 5G equipment market. The



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U.S. government has ruled out using Huawei systems in its 5G networks, fearing that Huawei equipment could be used to spy on Americans.

This marked the first year that I can remember where DesignCon and IPC APEX EXPO took place during the same week. It was a fairly constant topic of conversation at Design-Con. Having been involved in planning a trade



show, I understand how it is; sometimes, you don't get much of a choice of dates, and you take what you can get. IPC and UBM certainly didn't want their shows to run opposite each other. I ran into a half dozen "road warriors" on the second day of

DesignCon—engineers who had just flown in after attending the first few days of IPC APEX EXPO in San Diego.

The mood at DesignCon was upbeat. Company owners and managers were optimistic about the industry and the future and excited about the possibilities this new technology may bring. Quite a few managers said their companies were doing better than ever. I met some new graduates and a few other new hires; several companies predicted they would be hiring this year or in 2020.

All of this brings us to the current issue of *Design007 Magazine*. With all of these technological advances, OEMs are now putting printed circuits on all kinds of substrates including materials not even considered substrates. We

asked our expert contributors to share their insight into printing circuits on alternative materials.

In our lead feature article, columnist Barry Olney of iCD explains why all PCB substrates are not created equal, and why designers need to avoid "flat-earth thinking." Next, Dan Gamota of Jabil discusses some of the off-thewall substrates he has worked with over the years, and why materials such as toughened glass could be great substrates.

Columnists Anaya Vardya and John Bushie of American Standard Circuits discuss microwave bonding methods and their various effects on loss and dielectric constant. Next, John Coonrod of Rogers Corporation explains how designers are moving past microwave frequencies to millimeter-wave frequency ranges of 30–300 GHz, and why flexible circuits may be the answer. And we have a great article by CF Yee of Keysight Technologies that focuses on the influence of metal plating on PCB channel loss and impedance.

We also bring you columns from our regular contributors such as Mark Thompson of Prototron Circuits, Stephen Chavez with the IPC Designers Council, Bob Tise and Dave Baker of Sunstone Circuits, and Jade Bridges of Electrolube.

As always, we'd love to hear from you. Shoot us an email by clicking here and let us know what you think. Until next month, have a good one! **DESIGN007**



Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 18 years. He can be reached by clicking here. Powerful Schematic Capture and PCB Design Software



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Not All PCB Substrates Are Created Equal

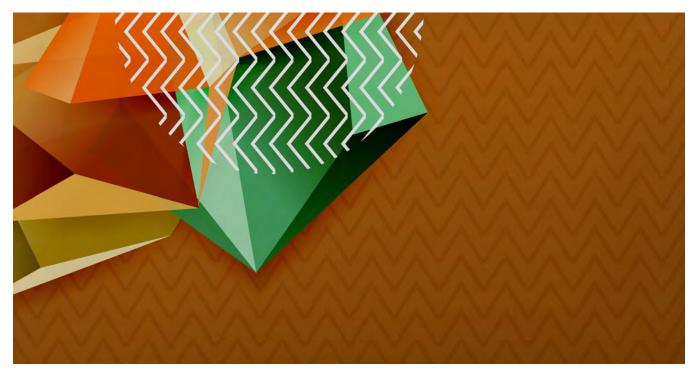
Beyond Design

Feature Column by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

PCB substrates are all around us in every gadget we use whether it's a computer, smartphone, or simple child's toy. The substrate may be rigid or flexible, or a combination of both. It is a carrier for the electronic devices and the signal and power interconnects and is usually planar in structure with conductors separated by insulating dielectric materials. However, each product has a specific performance requirement and may need a distinct type of substrate to comply with the product's specifications—particularly for high-speed designs.

Because the impedance of transmission lines is a function of substrate dielectric constant, essential requirements for a multilayer PCB dielectric material is extremely tight tolerance and consistency in the dielectric constant and thermal coefficient of dielectric constant (the amount of change in the dielectric constant as a function of temperature). In addition, the coefficient of thermal expansion (CTE)—especially in the z-axis (through the thickness of the material)—is of particular importance in multilayer designs because plated through-holes (PTHs) are used to make connections between different layers of the stackup. The CTE is a yardstick for expected PTH barrel reliability.

A wire suspended in free air has impedance in the order of 330 ohms. This impedance may have been viable in the old vacuum tube days but is not a good starting point for any digital design. A twisted pair cable with an outer shield has 100 ohms differential impedance. A coax cable with an inner wire surrounded by dielectric material and an outer shield is typically 50–75 ohms. As we add a coupled return path close to the signal conductor in the presence of a dielectric, the impedance reduces.



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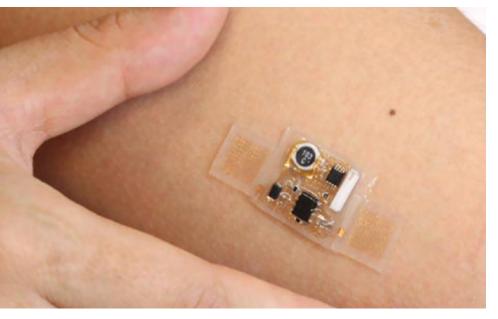


Figure 1: Biosensor patch worn on the skin. (Source: CBS News ^[1])

Typically, for a digital design, a characteristic impedance of 40–60 ohms and differential impedance of 80–120 ohms are used. This becomes more important as the edge rates become faster. Also, different technologies have their specific requirements. For instance, USB requires 90 ohms differential impedance, and DDR3/4 require 40/80 ohms single-ended/differential impedance. For perfect energy transfer, the impedance of the driver must match the impedance of the transmission line. A good transmission line is one that has constant impedance along the entire length of the line so that there are no mismatches resulting in reflections.

Technology is advancing rapidly in the field of medical electronics, providing doctors with more efficient ways to gather information. Figure 1 shows an ultra-thin and wireless adhesive biosensor that is stuck to the skin. This device can monitor a person's heart rate and other vitals and transmit the data in real time to a smartphone or computer. In this case, there appears to be no reference plane, but the impedance of the critical RF traces can still be managed by the careful planning of coplanar structures on the surface of the flexible substrate. The coplanar impedance is determined by the ratio of trace width to clearance, so size reduction is possible without limit—the only penalty being higher losses. In addition, a virtual ground plane exists between any two adjacent traces, as there is no field at that point. Hence, crosstalk effects are very weak between adjacent traces.

There is a common misconception that digital signals are transferred in the copper conductors of a multilayer PCB substrate, which is flat-earth thinking. A transmission line does not carry the signal itself but guides electromagnetic energy from one point to another through the substrate. Voltage and current do exist in the conductor, but only as a conse-

quence of the field being present as it moves past. The path should also control the characteristic impedance, so there are minimal reflections. What we really need to do is to provide a smooth, consistent path for the flow of electromagnetic energy.

The speed of a computer does not depend intrinsically on the speed of electrons but on the speed of energy transfer between electronic components. The dielectric material determines the velocity (v) of propagation of the electromagnetic (EM) energy (where the speed of light (c) is $3x10^{8}$ m/s):

$$v = \frac{c}{\sqrt{Er}}$$

With a typical Er (Dk) of four for FR-4 material, the signal will travel at approximately half the speed of light (c/2) through the substrate regardless of the clock frequency. The lower the Er, the faster the speed. With their relative timing requirements, the signals essentially ride the EM carrier wave. So, matching the propagation speed between signals on different stackup layers is crucial to ensure the correct timing margin at the receiver.

A stripline is any trace sandwiched between reference planes on both sides (Figure 2). The

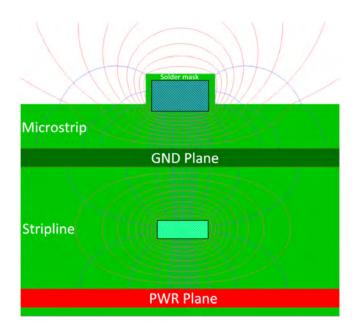


Figure 2: Microstrip and stripline electromagnetic fields (simulated in HyperLynx).

electric fields (blue) of a stripline are totally contained between the two solid planes, so the speed of propagation for signals guided by the trace is entirely determined by the dielectric constant of the surrounding materials.

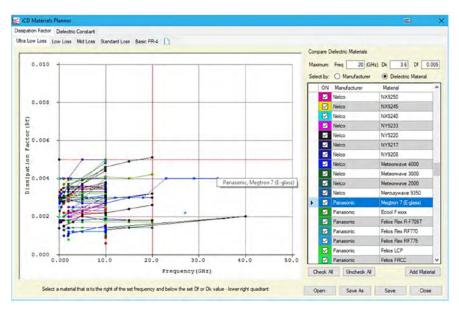
On the other hand, a microstrip is any trace fabricated on the outer layers of a PCB. A microstrip has dielectric material, a plane on one side, and air on the other. An embedded mi-

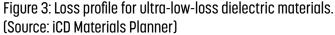
crostrip is similar but covered in a conformal coating such as solder mask or another dielectric material. In this case, the effective dielectric constant should be calculated by a field solver and represents a combination of the surrounding materials. There are also other variants of microstrip and stripline such as build-up microstrip, coplanar waveguides, and dual (a)symmetric stripline.

The electromagnetic fields surrounding the microstrip exist partially within the dielectric material(s) and partially within the surrounding air. Since air has a dielectric constant of one, which is always lower than that of FR-4 and solder mask, mixing a little air into the equation will speed up the signal propagation. Even if the trace widths are adjusted on each layer, so that the impedance is identical, the propagation speed of microstrip is always faster than stripline—typically, by 13–17%.

At frequencies above 1 GHz the dissipation factor (Df), another selection criteria for high-speed PCB substrate material, comes into play. Df is a parameter of a dielectric material that quantifies its inherent dissipation (loss) of electromagnetic energy. It refers to the tangent of the angle in a complex plane between the resistive (lossy) component of an electromagnetic field and its reactive (lossless) component. Standard FR-4 has a Df of ~0.02 whereas an ultra-low-loss dielectric may have <0.005 at 10 GHz.

Dielectric constant and dissipation factor contribute to the frequency dependent loss and to degrade the bandwidth and speed of the signal. The signal quality transmitted through the medium and picked up at the receiver will be affected by any impedance discontinuities and the losses of the dielectric materials. Fortunately, high-frequency dielectric materials generally have low Er and Df, enabling the signals to propagate faster, have less loss, and therefore, higher bandwidth. Figure 3 shows the loss profile of selected dielectric materials.





When we design a transmission line, as part of a multilayer stackup, we are not just defining the copper traces but also specifying the dielectric to transfer the electromagnetic energy. The traces and vias guide the energy through the substrate. A field solver uses the combined effects of trace width, clearance, and thickness plus the dielectric constant and material thickness to determine the impedance of the trace. However, the speed of propagation is independent of trace geometry and is totally determined by the dielectric material. All dielectric materials that compose a substrate have different properties, so one needs to select the optimal materials for the required purpose carefully.

Key Points:

- The impedance of transmission lines is a function of substrate dielectric constant
- The CTE is a yardstick for expected PTH barrel reliability
- Adding a coupled return path close to the signal conductor in the presence of a dielectric reduces the impedance
- Typically, for a digital design, a characteristic impedance of 40–60 ohms and differential impedance of 80–120 ohms are used
- A good transmission line is one that has constant impedance along the entire length of the line, so that there are no mismatches resulting in reflections
- Coplanar impedance is determined by the ratio of trace width to clearance, so size reduction is possible without limit—the only penalty being higher losses
- A transmission line does not carry the signal itself but guides electromagnetic energy from one point to another through the substrate
- With their relative timing requirements, the signals essentially ride the EM carrier wave
- The speed of a computer does not depend intrinsically on the speed of electrons but on the speed of energy transfer between electronic components

- The propagation speed of microstrip is always faster than stripline—typically, by 13-17%
- Dissipation factor is a parameter of a dielectric material that quantifies its inherent dissipation (loss) of electromagnetic energy
- Dielectric constant and dissipation factor contribute to the frequency dependent loss and to degrade the bandwidth and speed of the signal
- High-frequency dielectric materials generally have low Er and Df, enabling the signals to propagate faster, have less loss, and therefore, higher bandwidth **DESIGN007**

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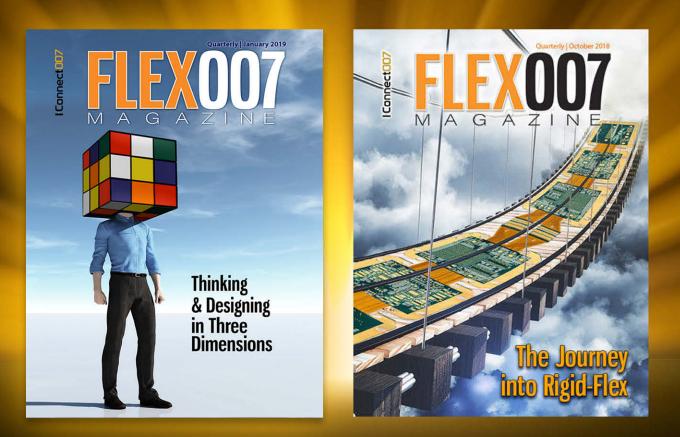
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Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in boardlevel simulation. The company developed the iCD Design Integrity software incorporating the iCD

Stackup, PDN, and CPW Planner. The software can be downloaded from www.icd.com.au. To read past columns or contact Olney, click here.



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Feature Interview by Patty Goldman and Andy Shaughnessy I-CONNECT007

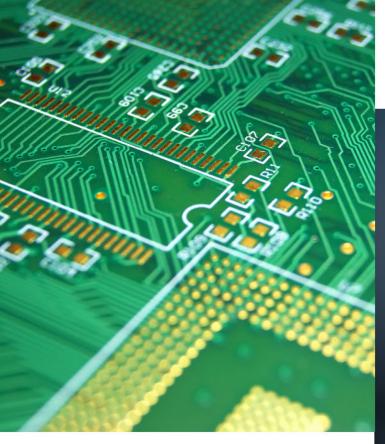
Dan Gamota has spent his career in electronics manufacturing. Dan has been at the forefront of some of the most cutting-edge processes and technologies since he started at Motorola decades ago. Now as the VP of manufacturing technology and innovation for Jabil, Dan gave us his take on the current state of flex and alternative substrates and explained why modeling, automation, and process controls are likely to be key ingredients in the recipe for manufacturing non-FR-4 boards in the future.

Patty Goldman: Dan, tell us a little bit more about yourself and your background.

Dan Gamota: I've spent 25 years in manufacturing and innovation. I started at Motorola when cellular phone commercial adoption was ramping up. I was on a team tasked with developing a scalable manufacturing process for an elegant microelectronics technology—bare die assembly (e.g., flip chip, C4)—which IBM had licensed to Motorola. Motorola was seeking to take that technology, which was developed and commercialized within a vertically integrated company (IBM), and prepare it for mass adoption by OSATs and PCBA services suppliers. Motorola was tasked with establishing the industry supply chain while moving from an elegant, well-controlled, low-volume product process that had to be closely monitored (multiple in-line testing platforms) to ensure high yield to one that was compatible with high volume SMT manufacturing (few testing steps) for mobile devices (i.e., cellular phones, pagers, two-way radios).

Early on, that gave me an appreciation for electronics manufacturing, automation, and process control. In the early days of SMT, you had to ensure that there was a significant amount of discipline on the design side: DFM, process guidelines, and material selection.

My active involvement with SMT and advanced microelectronics manufacturing lasted until about 2001. I was fortunate to have experienced the critical operational facets for







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about seven years of a well-controlled and well-established manufacturing environment. In 2001, the Motorola CTO Dennis Roberson was seeking to disrupt the way that we assembled electronics and the products that we could design. With his sponsorship and my direct boss, Dr. Iwona Turlik, we started on this path of manufacturing innovation. We thought, "Instead of having a rigid circuit board, could we use other materials for the circuit board? Could we use flexible materials such as textiles, polyesters, and paper, or stretchable materials such as silicones and polyurethane based soft materials? Could we use toughened glass that we could bend and form to any desired shape?"

Could we use toughened glass that we could bend and form to any desired shape?

The search for the new FR-4 started my second stage of manufacturing innovation. From 2001–2010, we experienced a significant drive to integrate electronics into products that historically had no electronic content, which opened up people's imagination to where electronics ultimately would be placed. That vision has driven the design of wearables and other types of on-body systems that we're starting to see today including those products providing physiological monitoring of athletes and individuals who want to understand how their body performs. Also, other types of new systems requiring non-FR-4 substrates are being driven by the healthcare and medical fields offering point-of-care diagnostics functionality. You're going to continue seeing the introduction of new materials (soft, stretchable, flexible, conformal, etc.) that historically had no presence in the electronics industry.

Goldman: What was it like learning that you could basically do whatever you want to do? Was it harder, easier, or just liberating?

Gamota: I would say all three. Motorola was seeking to identify what was the next great innovation to differentiate our wireless products portfolio. And the first thing when you think about flex and conformal is larger displays to enhance the mobile devices experience. The market seemed committed to helping realize a new technology that would allow people to have large 19-inch diagonal screens on their mobile devices that they could open up, roll up and put in their pocket.

Motorola fostered an environment that allowed people to fail while innovating, but fail fast and make changes quickly. They promoted an environment that had individuals trying to do things that had never been done before, so there probably wasn't as much anxiety as you might see elsewhere in a VC-backed startup. Also, at this point, I was involved in an entrepreneurial activity within Motorola where there was a sense of urgency to commercialize a product; the team worked 24/7 driven by enthusiasm rather than threat of venture closure. We were competing against the likes of Plastic Logic, Organic ID, and Poly IC-the darlings of the venture capital world in terms of startups. However, we didn't have that do-or-die ultimatum hanging over our heads since Motorola was supporting us.

We had access to large teams of engineers across the Motorola enterprise (semiconductor, cell phone, pagers, 2-way radios, automotive, etc.). Also, we were able to partner with other large companies like Xerox (XRCC and PARC), DuPont, and Dow, to establish the best team. Further, because Motorola was a large vertically integrated electronics company, we were able to seek support from individuals that had experienced the early days of semiconductors and mobile electronics products.

For instance, when we were trying to design circuitry using printing methods and inks, we went to Barry Herold, a 30-year veteran at Motorola who was known for his early IC innovations. Barry is credited with many innovations that contributed to the success of ICs as far back as the two-inch wafer. We had these wonderful mentors who kind of had a second coming; they were rejuvenated. Our team was called the "Dream Team." We combined a veteran group of experienced talent with a rookie group of individuals who did not know the technology barriers of the past. The team believed that we were going to launch a multibillion-dollar business based on novel products realized by a portfolio of innovations designs materials, processes, manufacturing equipment.

Goldman: When you were designing some of those early flexible or rigid-flex boards, there must have been a lot of failures and having to do it over again until you caught on to it such as the direction of the copper grain at flex points and things like that. Am I right?

Gamota: You're right. It was the days of Mac-Gyver because people were fabricating a bottom-gate transistor using any materials you had available. We had people using a Juicy Fruit gum wrapper, paperclip, and semiconductor ink to make a transistor. They looked at everything in an open transistor and IC design world where you simply required a conductive material for the gate, dielectric material for the gate insulator, another conductive material for the source and drain, and a material that had semiconductor-like properties.

When we would visit printing services companies-because ultimately, we were going to use printing equipment such as a screen printer, gravure, or flexography-we would go to their shelf of inks that they were using for graphic arts printing, and we would look at the ink chemical compositions. We learned that in graphic arts printing (e.g., a magazine) several of the inks used have electrical properties. Some inks are great conductors while others are great insulators. Except for not having a semiconductor ink, the printers had all the necessary materials to print transistors as well as the process know-how to align and print very fine features necessary for electronics. They knew how to ensure that transistor structure layers were pinhole-free and how to achieve sub-50 micron registration from printed layer to printed layer.

It seemed like everything was going to align



perfectly, and the only thing that was a potential concern for us was the semiconductor material. The advancements in semiconductor material electrical mobility were a little bit tempered and the materials weren't as high performing once you took them out of a well-controlled environment—a chemistry lab. Once you moved the material into a manufacturing or NPI environment, you lost a couple orders of magnitude in mobility performance. You still have these issues today when transitioning technologies from lab to fab. Also, we lack the ability to consistently print 1,000 transistors and ensure that all 1,000 provide the same electrical performance.

That's where the deficiency of printed transistors lies—robust high mobility semiconductor inks. Printed transistors would have a very difficult time replacing silicon based transistors. Once we realized that printing 1,000 transistors that all worked within a certain operation window would be very difficult and we observed the cost coming down quickly for silicon-based ICs, an all-printed transistor-based circuit was no longer an option. This was the start of flexible hybrid electronics (FHE).

Today you see flexible hybrid electronics (printed electronic devices combined with silicon-based devices assembled on a flexible substrate)—enabling the design and manufacture of products having unique form factors. The form factor is enabled because the substrate is no longer rigid but can be flexible, stretchable, and conformal. The use of FHE building blocks also enables flexibility in the design layout itself—you can still have one component or a few components that are silicon-based that provide the necessary functionality (e.g., computation speed or TX/RX performance for communications) while integrating printed elements to build your product.

Another critical set of design rules which were established for FHE was related to the copper traces on the substrate. These stringent design rules did not allow us to realize some of the products that we wanted in the past. Today, there are new materials (e.g., inks) that are being developed that may expand the product opportunities. These materials can conform to rough surfaces and planarize them to achieve the necessary flatness. For a long time, we were limited in the number of different products that we could develop because we were constrained by the lack of a smooth base conductive trace surface.

> For a long time, we were limited in the number of different products that we could develop because we were constrained by the lack of a smooth base conductive trace surface.

Andy Shaughnessy: What are some of the more interesting substrates and surfaces that you're working with or that you see coming online in the future? Futuristic types always talk about putting printed electronics on every cereal box, which would light up when you walked by on the grocery aisle.

Gamota: All of that is doable. The packaging materials that are used, whether it's the materials for candy wrappers or materials that are used for cereal boxes have surfaces that are pristine and perfect for electronics integration. But to me, for the most part, those are not the ones that are going to take us to the next realm. What I see moving us forward are stretchables.

When you talk about silicone materials which can deform in millions of directions, that's where the excitement lies. Many of these stretchable substrates are being investigated for digital tattoos that we put on our arms for perhaps monitoring our body's core temperature. That's great, but just wait until you can build a suite of sensors that you can place inside a person's body to monitor their heart rate or the stresses on their organs or artery walls.

That's the electronics journey that we are experiencing. There are some hurdles associated with it, but people are establishing guidelines to identify the substrates and their critical properties such as biocompatibility and stretchability. Now, we just need to appreciate the other criteria that are necessary to insert these products into our body to achieve the desired functionality and long-term performance.

Shaughnessy: We always thought that copper was going to hit the wall before now, and we keep seeming to be able to make FR-4 do more and more. Do you think it will get to the point where we finally run out of a use for FR-4, or we have to start using some of these boutique materials or others?

Gamota: I have history on my side, right? If I go back to my experience developing flip chip technologies at Motorola, everybody was predicting that flip chip was the future because wire bonding technology was reaching its limit. I wouldn't say it happened overnight, but in two years, I went from thinking wire bonding was dead to the introduction of ball-grid arrays (BGAs), micro BGAs, and chip-scale packages. What I learned is that you never can say a technology is going to go away with a high level of

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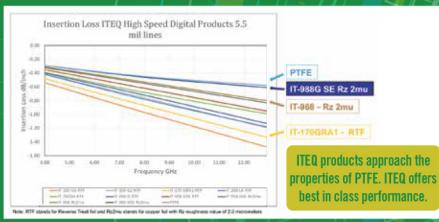
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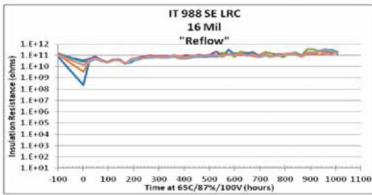
Sequential Lamination

7	Lamination	cycle	data

Lamination	DMA	DSC	TMA	T300 with CU	Solder Dip PCT: 1h @ 121°C	Td 2wt%/5wt%
1	213	187/187	182	> 60	> 60	408 / 435
2	216	194/199	193	> 60	> 60	41 7/ 438
3	214	186/192	185	> 60	> 60	417/442
4	216	193 / 194	184	> 60	> 60	424/443
5	217	194 / 199	190	> 60	> 60	418/442
6	218	191/197	188	> 60	> 60	405/436
7	218	190/197	194	> 60	>60	425/444

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confidence unless you amass a large volume of data to support the prediction. Although wellrespected technology thought leaders were making these predictions, the data they were using did not include input from all the industry stakeholders.

Also, I observed firsthand the commitment and drive of engineers. Engineers like challenges. If you tell an engineer that their future is quickly disappearing and that they need to find something else, they will innovate and extend the applicability of the technology. I feel that the introduction of new substrate materials with unique properties is fueling innovation and expanding the electronic product landscape. At this time, we are not replacing FR-4; it still has a significant amount of life.

Goldman: I've seen that in basic circuit boards where it was said that we'd never see another single-sided board.

Gamota: I agree. Never say never. If you look at the wearables industry, most products today are single-sided. Single-sided is mandated because the biggest pain point for designers is the connector and its durability when the substrate to which it is attached is deformed. No one has developed a connector that can withstand the strain experienced by wearable electronics, limiting designs to a single-side topology. It is suggested that double-sided topologies will not be realized until connectors are developed that use self-healing materials that relax to their initial state after being subjected to multi-axis deformation. Although single-sided is the standard today double-sided should be available in the future if history is repeated. There hasn't been enough focused innovation around the connector. Today, engineers are trying to leverage well-established connectors like buttons (e.g., conductive materials) and other types of known connectors. Many in the industry are predicting the introduction of novel connectors to address the gaps based on public reports of R&D efforts.

Shaughnessy: Flex manufacturers have told me that the only problems designers usually have is with the simple stuff. They get all the SI right, but then they put the connectors in the wrong spot on the bend of the flex or too close to the edge. Some say that the assembly for flex or rigid-flex is the worst part.

Gamota: Exactly, and that is the area where I think leveraging the digital twin tools that we're starting to see will help designers overcome these common problems. As the digital twin tools ingest larger product data sets, the designers will have the ability to simulate the product design, product manufacturing process, and product in-field performance in the virtual world. In the future designers will be able to identify potential failures using a digital twin provided they have access to the data. The development of an accurate digital twin could have a significant impact—the number of physical products built for the design, engineering, and product validation testing could be drastically reduced (reducing indirect and direct labor time and cost). There would be no need for the building of tens, hundreds, and even thousands of physical products to test under different environmental and mechanical conditions. Once we can collect accurate representative data sets and feed it back into the digital twin tools we will be able to optimize the design, process, and performance of the product. With the adoption and enhancement of digital twin tools you're going to start seeing improvements in those simple things such as product failures due to connector location.

Shaughnessy: Have you done a lot of work with ceramic substrates?

Gamota: Yes, but that work has been mostly for photonics modules. It's interesting that you ask because we're updating the iNEMI Roadmap chapter on flexible hybrid electronics, and there was a comment regarding the inclusion of ceramic substrates in the chapter. We originally included ceramics in the roadmap because if you go back in time, ceramics were the preferred substrate for the first generation of printed electronics. Ceramic and metal inks were screen printed on a ceramic substrate and subsequently fired. Ultimately, a decision was made to remove the established ceramic substrates from the next edition of the roadmap chapter and instead focus on novel flexible glass substrates and glass/polymer composite substrates.

I'm intrigued by the potential of these materials to withstand high dynamic loading in aggressive temperature, humidity and liquid environments. These substrates will provide designers with new product opportunities.

Shaughnessy: I remember right after 9/11, we started seeing a lot more of these round designs on ceramic, and they couldn't tell us what it was for because it was for a Tomahawk missile that had to withstand Mach 2. Do you know of any other material that is that durable?

Gamota: I have to admit that the answer is no. I sometimes am concerned that we may not be as open to trying new things as we once were. Today we are limited by how much time we are given to succeed due to the shorter product commercialization cycles, and therefore, we haven't tried to exercise the limits that have been placed on some of the materials we use. I'm not sure who's actually responsible for leading the development of those high performance materials outside of the traditional defense and aerospace suppliers. I believe that IMRE in Singapore at one time included the development of these materials in its R&D project roadmap. In the United States, perhaps the national manufacturing innovation institutes such as NextFlex may be investigating potential material compositions to provide the necessary durability.

A possible catalyst to accelerate the development of these substrates is the desire for space exploration. I don't know how long it's going to take, but we've already started hearing about the supply chain to Mars and what that supply chain will require. People are debating questions such as "Are you going to build products here on Earth and ship them up to Mars? Or will you ship the BOM to Mars and build the product there?"

Are you going to build products here on Earth and ship them up to Mars? Or will you ship the BOM to Mars and build the product there?

That's going to be a game changer. I don't know when that's going to happen, but if we continue to have visionaries such as Elon Musk and Jeff Bezos, we are going to see more challenges placed on the materials that we use for electronics. Perhaps most of the R&D activity will be performed by companies such as Boeing, Rockwell, and the other large companies that provide electronic systems to go into space. However, limited information has been discussed regarding the advancement of these high performance materials.

Goldman: That's a relatively small market.

Gamota: Agree. Today it is a very small market, but everybody says, "Don't look at the acorn today; look at the oak tree tomorrow. The oak

tree is civilization in space." I don't know what the timing will be, but the opportunity is massive.

Shaughnessy: Dan, is there anything else you want to mention?

Gamota: I truly believe we are in a situation where we will see significant growth in electronics manufacturing innovation. Presently, it's being slightly tempered because of the shortened timelines that we are given for transitioning ideas to product realization. We may see an increase in the diversity of available substrates and the functionality that those materials give us to realize some of the products, but it's all going to have to wait until we can accelerate the industrialization process and leverage digital building blocks such as digital twin tools.

Things are good, but they could be better, and they're only going to get better if we have the appropriate digital tools with accurate data sets for us to build models and simulations in a virtual environment before investing in the prototyping and manufacturing of physical products.

Do you feel that electronics manufacturing has deviated from encouraging only revolutionary technologies to accepting evolutionary technologies?

I have a question for you both. Do you feel that electronics manufacturing has deviated from encouraging only revolutionary technologies to accepting evolutionary technologies?

Shaughnessy: It does seem that way, and some analysts are saying it's about time for a quan-

tum leap like we saw with EDA tools for SMT— something game-changing.

Gamota: You said the magic word—SMT! Two months ago, I met with an executive at an SMT equipment supplier, and we had a similar conversation about SMT. For 20+ years in SMT, components and devices for pick & place assembly have gotten bigger and smaller, but the fundamental process has not changed. Is SMT ready for a disruption? The executive stated that it appears that no one is thinking about it. He remembers a time when vertically integrated companies like Motorola and IBM had the bandwidth and assets to drive manufacturing innovation in search of what's next. They had teams of engineers seeking novel assembly processes. He felt that once those companies stopped having dedicated advanced manufacturing technology groups that designed and built equipment to support internal manufacturing of products, manufacturing innovation kind of stopped.

Perhaps it is time to revisit existing manufacturing technologies such as SMT. How would you go about bringing together the appropriate people to start the dialogue? It doesn't have to be a major disruption in SMT manufacturing. However, at some point, you should see a jog in the SMT road.

That is the kind of dialogue we should have with Happy Holden as he is the type of person with the experience to lead the conversation. He is known as an expert on manufacturing innovation. Happy is credited with introducing several broad industry adopted revolutionary manufacturing technologies. He could facilitate the discussion for why we continue to use established manufacturing processes with little interest in change.

Shaughnessy: Dan, I really appreciate you taking the time to talk to us today.

Goldman: This is thought-provoking information. Thank you.

Gamota: Thank you. DESIGN007





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Microwave PCB Bonding Methods: What Designers Need to Know

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Feature Column by Anaya Vardya and John Bushie, AMERICAN STANDARD CIRCUITS

There are three methods commonly used for bonding multiple layers of RF and microwave PCB laminates such as PTFE (Teflon) materials like Rogers duroid. These three methods are thermoplastic films, thermoset prepregs, and direct bonding (often called fusion bonding). Each has their own pros and cons that PCB designers need to understand to balance cost and performance.

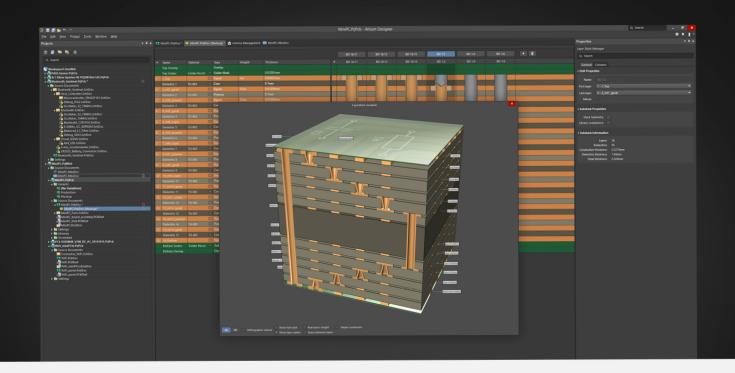
Thermoplastic Film Bonding

Bonding films are designed to flow into the laminate stackup under heat and pressure to encapsulate the traces left on the surface of the inner layers after the etching process. This means that the bond is primarily mechanical in nature. Several thermoplastic bond films are available for use in PCB applications including polyethylene (PE), chlorotrifluoroethylene (CTFE), fluorinated ethylene propylene (FEP), and polytetrafluoroethylene (PTFE). Major suppliers of this material over the past 40 years include Rogers, Taconic, and Arlon. Thermoplastic bonding films are not well suited for use in hybrid multilayers due to the temperature required to melt these materials. The lower thermal degradation point of thermosetting materials may cause these materials to oxidize and decompose.



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The transition (melting) temperature of these films must be considered to assure the right material match to the application. Polyethylene has the lowest melt temperature from approximately 190–250°F (88–121°C), depending on the density of the resin and degree of molecular cross-linking. CTFE is about 380°F (193°C), which is prohibitive for PCBs that will see manufacturing processes with higher temperatures such as hot air solder leveling (HASL). FEP has a transition point of 500°F (260°C) and is capable of handling HASL temperatures. PTFE has the highest transition temperature above 630°F (332°C), so it will survive subsequent high-temperature processes.

The primary advantage of using thermoplastic films is their low electrical loss factor. PTFE multilayer boards are well known for their excellent electrical properties, but using a hybrid construction of a high-loss epoxy-based prepreg would defeat the purpose of the PTFE. While a particular bonding film may not exactly match the dielectric constants of the laminate, the effect of any difference is typically negligible, or if not, the board can be designed to allow for the difference. The downside is that thermoplastic film bonding is typically limited to low layer PCBs and not suited for sequential lamination.

Thermoset Prepreg Bonding

Thermoset prepregs harden and cure as a result of a thermochemical reaction such as the reaction that hardens the two components of epoxy when mixed together that you can buy at the hardware store. Thermoset prepregs can also be reinforced with fillers to improve the stability of the final product. Once hardened or cured, thermoset materials are typically harder than their thermoplastic counterparts. Unlike thermoplastic materials, thermoset materials go through the thermochemical reaction only once, and cannot be re-melted like a thermoplastic. Before the cure of thermoset prepregs, they have a limited shelf life compared to thermoplastic films.

The primary advantages of thermoset prepregs are the ability to manufacture sequentially laminated PCBs and produce higher layer count stackups, and a closer match to traditional laminate properties in hybrid constructions. The primary disadvantage is a high electrical loss factor.

Fusion Bonding

The first two methods require additional films or prepreg materials, which function like glue to keep the multiple layers in one piece. The third approach for forming RF and microwave PCBs, fusion bonding, uses heat and pressure to direct bond the material substrate layers into one piece. The layers are joined together through extremely high temperature and precisely controlled pressure without the addition of any bonding materials.

This method has its challenges such as the additional control over the lamination fixture, pressure, and elevated temperature. But the increased performance over thermoplastic and thermoset bonding are significant in the right application. The fusion bonding results yield a fully homogeneous dielectric constant structure with no mismatch of properties from different films or prepregs. Fusion bonding produces a single, uniform dielectric constant value throughout the PCB package, which can instrumental for high-frequency applications that must meet critical performance requirements.

Comparison of Pros and Cons

Thermoplastic Films

Pros

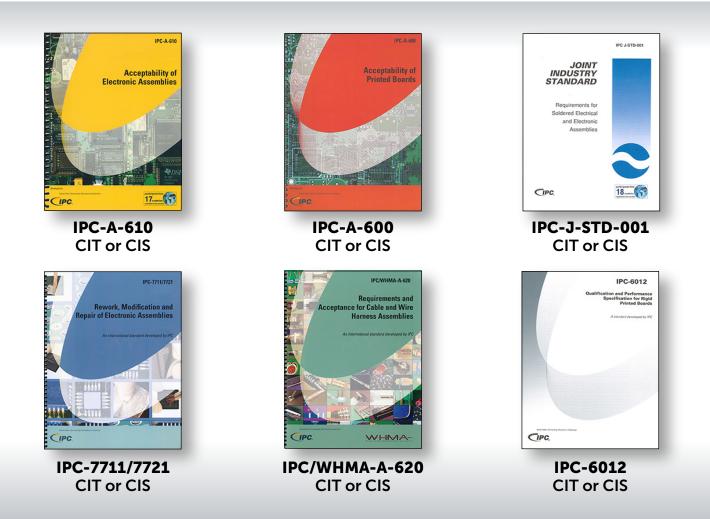
- Good to excellent loss characteristics
- Lower dielectric constant (E_r) than most thermosetting prepregs (close to pure PTFE)
- Pure isotropic material

Cons

- Not a good choice for sequential lamination
- Lamination temperature unsuitable for many thermosetting prepregs
- Poor drilling performance with potential for smearing
- Cannot be desmeared or etched back



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Thermosetting Prepregs

Pros

- Possible to match resin system and electrical properties of thermosetting laminates with an E_r of 2.95 and above
- Superior CTE to thermoplastic bond films
- Can be desmeared and typically etched back

Cons

- Anisotropic material
- Not available with an $E_r \le 2.94$
- Traditionally higher loss than thermoplastic resin systems

Fusion Bonding

Pros

- Best electrical performance
- E_r is almost perfectly matched to adjacent laminate materials
- May be sequentially laminated depending on copper thickness

Cons

- Not typically suited for bonding plated subassemblies unless PTFE bond-ply is used
- Long lamination cycle
- Extremely high lamination temperature required ≥700°F (371°C)
- Not compatible with thermosetting resin systems

Conclusion

As you can see, each of the discussed microwave bonding methods has distinct advantages and disadvantages that must be considered when choosing which method will be the right one for a specific application. PCB designers need to fully understand these characteristics to balance cost and performance when selecting the optimum bonding method. **DESIGN007**

Visit I-007eBooks to download your copies of American Standard Circuits' books today: The Printed Circuit Designer's Guide to... Fundamentals of RF/Microwave PCBs and Flex and Rigid-Flex.



Anaya Vardya is president and CEO of American Standard Circuits.



John Bushie is ASC's application engineering manager and a process engineering specialist.

To read past columns or contact the authors, click here.

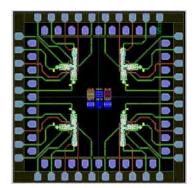
Circuit Design May Boost Memory Storage

Scientists at Oak Ridge National Laboratory and Hypres, a digital superconductor company, have tested a novel cryogenic—or low-temperature—memory cell circuit design that may boost memory storage while using

less energy in future exascale and quantum computing applications.

The team used Josephson junctions made from niobium- and aluminumbased materials fabricated at Hypres for the single-bit memory design on a chip and demonstrated write, read, and reset memory operations occurring on the same circuit.

"The test showed the viability of



memory processing functions to operate faster and more efficiently," said Yehuda Braiman, a distinguished scientist in the computer science and mathematics division at ORNL. "This could lead to substantially

> decreased access energies and times and allow for more circuits to occupy less space."

> Building on an initial design, ORNL's Braiman, Niketh Nair, and Neena Imam continue working on multi-valued memory cell circuits and large arrays of memory cells. Their first step was a ternary memory cell circuit design.

(Source: Oak Ridge National Laboratory)

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Higher Frequencies Pave Way for Flexible Circuit Materials

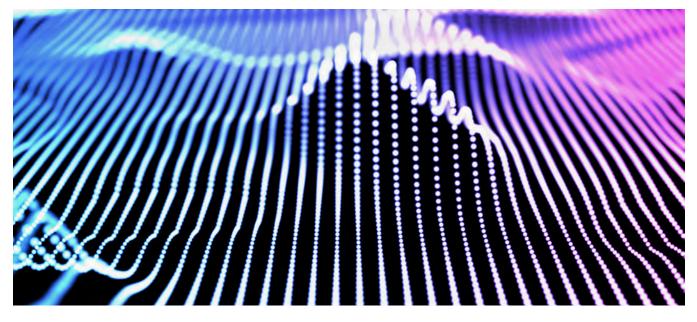
Lightning Speed Laminates Feature Column by John Coonrod, ROGERS CORPORATION

The frequency spectrum is being consumed quickly for many wireless applications from popular cellular communications systems to more esoteric safety and medical systems. For the available spectrum, circuit designers are reaching beyond traditional microwave frequencies and into the millimeter-wave (mmWave) frequency ranges from 30–300 GHz. Those designers often look to a relatively mature technology, flexible circuit technology as the PCB materials for those high-frequency circuits. Although such materials may not typically be a first substrate choice for high-speed, high-frequency circuits, the thinner, flexible circuit materials are well suited for the shorter wavelengths at mmWave frequencies.

Such high-frequency signals are being planned for global communications in fifth-generation (5G) wireless systems, automotive driver assistance system (ADAS), and self-driving autonomous vehicle systems, among other

applications. Thinner substrate materials have several advantages for high-frequency circuits. For example, thinner dielectric materials between copper circuit planes can help minimize internal resonances in the circuits. Thicker circuit materials can suffer higher electromagnetic (EM) radiation losses to neighboring circuits and can lose energy as EM interference (EMI) at higher frequencies where signal wavelengths are smaller and signal power can be harder to come by. Circuits designed for mmWave frequencies usually start with thinner circuit materials for optimum performance.

The smaller wavelengths of mmWave frequencies tend to highlight circuit material anomalies at those higher frequencies—anomalies that can also influence the radio frequency (RF) performance of the circuit. Such material anomalies include variations in dielectric thickness, dielectric constant (Dk), copper conductor width and spacing, and copper con-



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ductor plated thickness. For mmWave circuits, even small variations in these key material properties can impact electrical performance. Fortunately, flexible circuit technology is typically well controlled for thickness compared to thicker, more rigid circuit board materials.

As a simple example, a microstrip circuit using 5-mil circuit material with a Dk of about 3 and a thickness variation of 1 mil will exhibit an impedance difference of about 6Ω at microwave frequencies. A 6Ω impedance difference may impact some applications; however, at mmWave frequencies, even small thickness variations can cause impedance differences that cause more reflections and many related issues. The 1-mil difference could be from a material with a thickness tolerance of only ± 0.5 mil $(\pm 10\%$ thickness tolerance). This is considered a very tight tolerance for a rigid circuit material; however, the thickness tolerance of flexible circuit materials can be much better controlled. Flexible circuit materials tend to provide highly consistent Dk that is nearly isotropic, as a function of the material formulation. This is generally true, although exceptions do exist.

While flexible circuit materials offer many advantages for mmWave frequency designs, it should also be noted that they can suffer higher loss, dissipation factor (Df), and moisture absorption than more traditional, rigid circuit materials. The Df for many flexible circuit materials is in the range of 0.015–0.030 at 10 GHz, which is considered high. The Df of circuit materials for mmWave frequencies usually needs to be less than about 0.003 because of the oftenlimited signal power at those high frequencies. Moisture absorption can also affect the electrical performance of a circuit material. Water vapor is polar in nature and can increase the Dk of the dielectric material that absorbs it. Still, as some circuit designers may not be aware, some circuit materials that can be used in flexible circuit applications also provide very good Df and moisture absorption characteristics, making them well suited for mmWave applications.

An example of flexible circuit material for mmWave applications is the 5-mil RO3003 circuit material. It provides material properties for mmWave circuit applications such as 77-GHz automotive radar sensors, and it is not a woven glass-reinforced material. The glass reinforcement provides strength, but it can also limit circuit flexibility. RO3003 materials have an extremely low Df of 0.001 when tested at 10 GHz with low moisture absorption of 0.05%. The material's thickness is also tightly controlled, held to a tolerance of $\pm 10\%$.

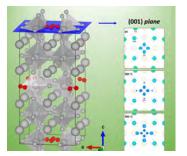
As always, it's best to communicate with your material supplier well before beginning the design cycle. **DESIGN007**



John Coonrod is technical marketing manager at Rogers Corporation. To read past columns or contact Coonrod, click here.

Neutrons: Fueling Better Power

A University of South Carolina research team is investigating the oxygen reduction performance of energy conversion materials called perovskites by using neu-



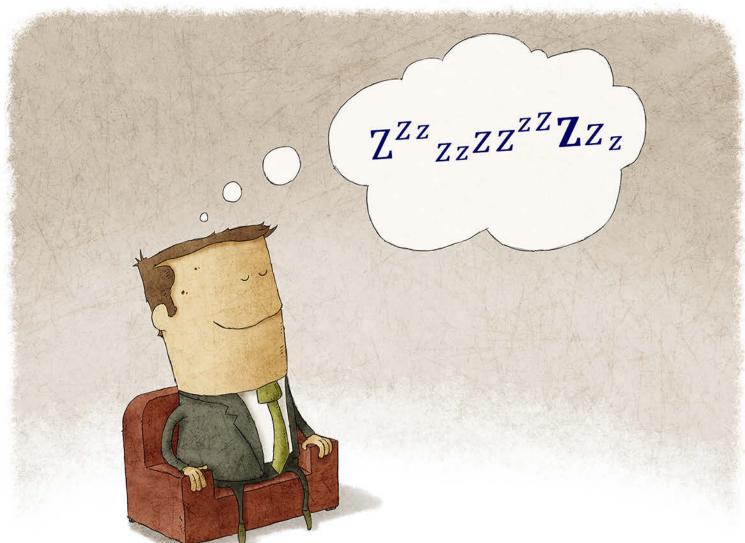
tron diffraction at Oak Ridge National Laboratory's Spallation Neutron Source.

Perovskites are core components of solid oxide fuel cells, which can be utilized for distributed power generation in remote areas or for backup power at data centers. Neutrons' sensitivity to light elements allows them to accurately probe the perovskites' structures and reveal how they influence the fuel cell's performance. Using a furnace in the VULCAN beamline, the team mimicked a fuel cell's typical environmental conditions.

"VULCAN's unique high-temperature capability allowed us to see the perovskites' structures in their operating conditions," said USC's Kevin Huang, the corresponding author.

(Source: Oak Ridge National Laboratory)

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PCB007 Highlights



Better to Light a Candle: Chapter One— Prepping the Next Generation ►

There has been a considerable amount of (electronic) ink and words shared in our industry bemoaning the graying-out of our industry and the growing shortage of skilled people at all levels. (See the May 2017 *PCB007 Magazine* column "Help Wanted—and How!" for just one example). As is usually the case, though, when all is said and done, more has been said than done.

Itronics Starts R&D to Recover Tin and Copper from Its "Breakthrough Technology" PCB Refining Pilot Plant ►

Itronics Inc., a "creative green technology company" that produces GOLD'n GRO fertilizers and silver products, has started research and development to recover tin and copper from the silver bullion being produced by its "breakthrough technology" PCB refining pilot plant.

It's Only Common Sense: A Word From the Future—CES 2019 ►

If only we could invent something that would stop hunger and poverty, give us world peace, or stop us from being so angry with each other all the time—something we desperately need and could use right now. That would be something, wouldn't it? It's only common sense.

CES 2019: More Show Floor Favorites >

This final piece covering CES 2019 reviews more automotive technology, updates on 3D printing, and some trending devices such as smartwatches and new computer components for those that either need or just want to have extremely powerful and impressive-looking computers.

ESI's Chris Ryder: There's More to Choosing a Laser Than You Think >

At the recent HKPCA show, Barry Matties sat down with ESI's Chris Ryder, director of product management—HDI—to discuss considerations for choosing a new laser system, and how ESI uses its decades of flex and rigid-flex drilling experience to help guide customers in their decision-making process.

Standard of Excellence: Keep Your PCB Supplier Sharp >

The best way to create a solid and productive partnership with your PCB supplier—and all of your suppliers for that matter—is to keep an open line of communication with them. No matter what kind of relationship you currently have with your suppliers, you can never communicate enough. Let them know at all times what you need from them.

Flex Time: Pointers for Your First Rigid-Flex Design ►

If you are new to rigid-flex designs—or have never done a rigid-flex PWB layout—you might wonder how it is similar to and different from hardboard design. In this column, I'll address critical items you need to know to successfully create a stable and robust rigid-flex design.

Mr. Laminate Tells All: Good Morning, Vietnam! ►

Many electronics-based OEMs and their supply chains are looking for China alternatives in the current economic and political landscape. Of all the remaining locations possible in Southeast Asia, Vietnam is coming to the forefront as a viable choice for successful export manufacturing. Every day, we see evidence of large OEMs shifting their focus to Vietnam.



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Eliminate Confusion

The Bare (Board) Truth by Mark Thompson, CID+, PROTOTRON CIRCUITS

This column will address eliminating confusion that creates remakes both from the enduser/designer and the fabrication house. First, let's talk about being clear about your intentions. What are some of the things that create miscommunication, lost time, and sometimes even remakes at the fabrication house of your choice? The first thing is querying the fabrication house for impedance numbers.

Let's say you've asked for a material type on your drawing that is neither readily available or used by your fabricator. Here, you should expect the fabrication house to respond quickly and have all the deviations at once for you to review. This includes any impedance width changes, material types, or copper weights to produce the part. Any deviations regarding drawing notes such as wrap plate requirements that cannot be incorporated due to insufficient space or the extra etch compensation to meet the wrap plate requirement should also be addressed.

If your chosen fabricator comes back and says the material you have called out is not a standard stocked material for them, you are asking for a three-day turn. Giving you an alternative is great, but if by changing to the material they suggest your trace widths or spaces change to the point the part has to be laid out again, this can be very frustrating for the board designer.

To mitigate this from happening, give yourself an additional mil or two of space. This will allow the fabricator to resize the traces to meet your impedance and adjust dielectrics. For example, if you have designed the part as a 0.1mm trace and space, this does not allow the fabricator to resize the traces without affecting



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the spaces. It may even require the fabricator to ask for a lighter starting copper weight to allow for a 0.5-mil change in trace width to still make the part producible.

This is where the etch compensation based on starting copper weight is key to remember when designing the part to allow for slight changes to either dielectric distance, starting copper weight, or trace width changes to meet your impedances. Having gone through all this, if the fabrication house does not state additional deviations due to the color of solder mask, material finish type, or even the material UL rating required, this is also frustrating for the designer. You should communicate with an engineering person at the fabrication house ahead of time to preclude these deviations from slowing down the part.

The second thing is being clear on what you need. If you initially ask for half-an-ounce starting copper and the copper weight needs to be increased due to voltage or EMI issues, this loses time in laying out the design again to accommodate a larger space to deal with the higher copper weight. If you've stated one copper weight only to change it, expect you may have to change trace widths or spaces to

If you've stated one copper weight only to change it, expect you may have to change trace widths or spaces to accommodate these changes.

accommodate these changes. Likewise, changing a mask color form from green to red may require a complete re-layout due to the slightly thicker red or other colored mask change. Thus, what you ask for should not change from your original request, or you should expect to have to re-lay out the design to increase space or trace widths. Again, with the example used previously of a 0.1-mm trace and space, if all the variables don't remain the same as what was asked for, the fabricator only has a few deviations that can be made on their end. All of these negotiations should be made before the release of the dataset. Frustrations can occur on both sides (the end user and the fabricator) when things change based on the information they have received versus what they get once the dataset has been released.

The two main delays we see at the fabrication level are:

1. Deviations that require re-lay outs due to changes being added to the drawing or RE-ADME file that were not previously negotiated and need a new layout from the designer

2. If your chosen fabricator does not identify all of the deviations at the quote stage, which requires more back-and-forth communication between the board designer and the fabricator, delaying the parts

Much of this was never an issue 0.008"/0.008", and designers know that those numbers correspond roughly to the dielectrics needed to meet said impedances. However, with trace and space routinely at 0.004"/0.004" today, the deviations from copper weights or mask colors can and will affect the ability to produce your part as you wish it.

Remember the things that a fabricator can change to meet your desired impedances, such as:

- **Trace widths** if space allows based on copper weights. Remember, all copper is typically compensated at the CAM stage to deal with the known loss at the fabricator's etcher
- **Dielectrics** if overall thickness can be met by adjusting the dielectrics and copper weights can be reduced on interface layers. For example, if all plane layers are called out as one ounce but the trace widths on the surface layers are 0.004" or below to meet the impedance, you may have some pushback asking to reduce the copper

weight on the plane layer due to having to go to a single-ply prepreg construction. As evidence of this for internal planes larger than a half ounce or three-eighths of an ounce, fabricators like to use a minimum of two plies of prepreg. Bear in mind that even the thinnest preg ply used as two-ply may be too thick to deal with the 0.004" or below trace widths called out on the surface for impedances requiring a relayout to increase the space on the surface and the trace widths, and still meet a twoply construction to keep your planes at one ounce

- Material type to get closer to the Dk you were modeling the trace and space at so no changes or very few changes need to be made to the trace widths, which may also require a new layout
- **Copper weight reductions** if a given trace has to be increased, digging into your available usable space

These are really the only things a fabricator can do to get close to your desired impedances on their end without requesting a new design with wider spaces, material deviations, and the overall thickness and tolerance requirements. But what are some things a designer can do to help the fabricator if those changes are needed?

One thing is to not use the same trace width for different scenarios on the part (i.e., using a 0.004" trace for single-sided at 50 ohms, and part of a 100- or 90-ohm differential pair). Differentiating them by a tenth or even a thousandth of a mil will allow the fabricator to uniquely pick out those structures that need to resized and not affect the others of the same width. This has been a practice known to designers for years. Additionally, using the same trace width for copper fill area as the impedance traces is not a good idea because if one needs to change to meet the desired impedances, the fill area will also be affected.

Now, let's talk about mask color changes from what was initially negotiated based on the same 0.004"/0.004" design rules for trace and space. If the original request calls for red solder mask and the part dataset is received with it changed to green mask, red mask is thicker. Thus, impedances are based on the red mask are calculated, so changing to a green mask may mean the 0.004" traces would have to increase due to the thinner mask color. Even as little as a half-mil change may throw out your ability to increase the trace as a true 0.004" trace and space design. Further, going with a lighter copper weight to start to not have to re-lay out the design with wider space will not work because reducing the copper weight means increasing the trace width to get the desired impedance.

Even as little as a half-mil change may throw out your ability to increase the trace as a true 0.004" trace and space design.

What is the bottom line of this column? Similar to ISO—where we must do what we say and do what we do—as a board designer, you need to make sure all changes (e.g., material type, trace widths or spaces, mask colors, or even surface finish) from what was originally negotiated with the fabrication house before asking them to calculate impedances not to have to re-layout the design. Save yourself some grief by having a conversation with the fabricator about all of the variables so you will not be asked to re-lay out the design, taking additional time.

As always, thank you for reading. DESIGN007



Mark Thompson is in engineering support at Prototron Circuits. To read past columns or contact Thompson, click here. To download your copy of Thompson's eBook, The Printed Circuit Designer's Guide to... Producing the

Perfect Data Package, click here.

Greater Phoenix Chapter Revived

The Digital Layout

by Stephen Chavez, CIT, CID/CID+, IPC DESIGNERS COUNCIL

This month's column highlights the Greater Phoenix Chapter in Arizona.

The IPC Designers Council is an international network of designers. Its mission is to promote printed circuit board design as a profession and to encourage, facilitate, and promote the exchange of information and integration of new design concepts through communications, seminars, workshops, and professional certification through a network of local chapters.

Chapter Spotlight by Stephen Chavez

The Greater Phoenix chapter was revived in late 2018 after being largely dormant over the past few years. It has also undergone some leadership changes. As the former president, I have taken on a more active global role at the executive level of the IPC Executive DC Board as the communications officer at large. I will stay on the leadership committee for the Greater Phoenix Chapter as the VP at the request of the newly elected president, Randy



Paul Fleming

Kumagai. Randy and I have already started to brainstorm with ways to kickstart the chapter's activity in 2019.

Former VP Paul Fleming will step down and assist the leadership team as needed, becoming a regular member. Tom Reilly will remain the communications officer. Also, we have a recent addition to the leadership team of Dave Baldwin, our longtime past chapter president. Dave will be a great addition to the chapter's future as well.



Tom Reilly

Meet Randy Kumagai

Here are a few words from the newly elected chapter president:

"I am pleased to have been elected as the new president of the Greater Phoenix IPC Designers Council. I have been involved with rigid and flex PCBs for over 25 years. As the president and owner of Silver Mountain Design, a manufacturer's rep company, we have represented companies in the past such as Minco, Advanced Quick Circuits, Tyco Printed Circuits, and TTM. Currently, we represent Summit Interconnect and Flexible Circuit Technologies. We have offices in Phoenix and Tucson. The mission of the DC is to facilitate the orderly

exchange of design concepts concerning printed boards and related technologies. I will support this on a local level providing design-related events, programs, and communications with the help of our other officers, Stephen and Tom, and the resurgence of Dave back



Randy Kumagai

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Figure 1: SkySong, the ASU Scottsdale Innovation Center.

into the mix. I am very excited to work with them to get this chapter active again and work with other active global DC chapters."

To contact Randy, you can email him at rkumagai@silvermountaindesign.com.

History

The Greater Phoenix Chapter has been in existence for over 20 years. One of the former presidents still has his membership card from 1997 where they used to meet at Motorola on Scottsdale Road and McDowell. More recently, meetings have typically been held every quarter at the ASU SkySong located in Scottsdale, Arizona (Figure 1). Like many of the other global chapters, this chapter started with a small group of designers many years ago with past leaders such as Cyrus Ringle, Dave Bald-



Figure 3: April 2013 Phoenix chapter meeting.



Figure 2: January 2011 Phoenix chapter presentation.

win, Jim Gazia, and Paul Fleming.

At its peak, the chapter had meetings with 20–30 regularly attending members and an executive board consisting of roughly six members (Figures 2 and 3). We have had many great speakers and presenters over the years, including Dieter Bergman, Gary Ferrari, and Rick Hartley to say the least. We also had many of the industry PCB design tool vendors come out, presented, and sponsored meetings such as Mentor, Cadence, and Altium, as well as several local and global suppliers.

After the economy went downhill, for several years, this chapter saw its attendance slowly drop to a point where we had more chapter leadership members and sponsoring suppliers in attendance at quarterly meetings than general members. As chapter leadership roles

decreased and changed from one person to another, each executive member gave more than 110% effort trying all that was in their power to jump-start the chapter activity.

Unfortunately, in late 2017, it was decided by the remaining four-member executive leadership team of the chapter to simply take a break and allow the chapter to lay dormant simply due to the overall lack of attendance. However, the core chapter leadership team kept meeting regularly. At these regular meetings, we continued to collaborate and looked to find others willing to be a part of the chapter's executive board and step up to an active role in the chapter.

In late 2018, Paul introduced Randy to the executive team. After several follow-up meetings that Randy attended, he agreed to take up the reins as the chapter president. Randy was voted in, and it was finally decided that it was time to get busy again getting this chapter back on its feet.

The Future

The future looks bright for this chapter. We have several major tool vendors and local and global suppliers already primed to sponsor our meetings. Under Mike Creeden's leadership, San Diego PCB has agreed to be as actively involved with the Greater Phoenix Chapter as they are with the San Diego Chapter by hosting chapter meeting at their Chandler satellite office. This is something that this chapter has never had—a regular home to host meetings.

As 2019 unfolds, we hope to take advantage of all of the opportunities that present themselves such as coming together, learning, and networking. We, like many other chapters, would like to have more people to participate in the Arizona area-current designers, engineers, manufacturers, software vendors, and those interested in PCB design. Arizona has become a great melting pot of engineering! If you are ever in our area, please look us up, and hopefully, you can time it just right to attend one of our meetings. Our 2019 meetings schedule has not been finalized yet, but will soon be published through LinkedIn since we don't have a chapter website at this time. Always feel free to reach out to me as well. We'd love for you to visit or join our chapter!

2019 Training and Certification Schedule: Updated IPC Certified Interconnect Designer (CID)

- February 26–March 1: Manchester, NH
- March 5–8: Santa Clara, CA

- March 19–22: Kirkland, WA
- April 22–25: Schaumburg, IL
- May 21–24: Pittsburgh, PA
- June 18–21: Kirkland, WA
- August 6–9: Baltimore, MD
- August 26–29: Markham, ON
- September 6–9: Santa Clara, CA
- September 19–22: Schaumburg, IL
- October 21–24: Anaheim, CA
- November 2–5: Raleigh, NC
- November 5–8: Dallas, TX

IPC Advanced Certified Interconnect Designer CID+

- April 16–19: Markham, ON
- September 6–9: Santa Clara, CA
- September 10–13: Kirkland, WA
- September 19–22: Schaumburg, IL
- October 21–24: Anaheim, CA
- November 2–5: Raleigh, NC
- December 3–6: Manchester, NH

Note: Dates and locations are subject to change. Contact EPTAC Corporation to check current dates and availability. A minimum enrollment of seven students is required for a class to be held.

PCB Design Events

- PCB2Day
- Controlling noise, EMI, and signal integrity in high-speed circuits and PCBs
- April 17–18: Seattle, WA
- June 13–14: Boston (Chelmsford), MA
- pcb2day.com

PCB West 2019

- September 9–11: Santa Clara, CA
- pcbwest.com



Stephen Chavez is a member of the IPC Designers Council Executive Board and chairman of the communications subcommittee. To read past columns or contact Chavez, click here.

Exploding PCBS: Don't Lose Track of Voltage in Your Design

Connect the Dots by Bob Tise and Dave Baker SUNSTONE CIRCUITS



Managing split planes? Your CAM tool will not do it for you. We see this almost every day—not exploding PCBs, which pretty rare but rather problems created by having more than one voltage on a power plane layer. From where we sit, this is one of the more insidious and costly challenges facing PCB designers.

Losing an entire lot of boards to spontaneous combustion offers an immediate, measurable cost, but the less noticeable anomalies can eventually cost even more once you add up production delays and resources directed at solving the problem. Worse yet, malfunctioning boards can make it into the field and create even bigger headaches.

The severity of the PCB failure seems to have an inverse relationship to the amount of effort required to fix it. When there's smoke coming out of your PCB, it's relatively easy to find out why. Digital glitches and signal anomalies are more subtle issues that can take many hours of tedious detective work to solve. We'll explain why managing split planes can be so challenging and take a look at some best practices for avoiding this common issue.

Why Does This Happen?

PCB design tools offer the ability to assign voltage amounts to the entire plane, but that can lead to problems if your design assigns multiple voltages to the same plane. You can divide the plane into separate, electrically isolated areas using a split plane—an enclosed region on an internal plane layer. But when you have more than one voltage assigned to a power plane layer, your CAM tool does not check whether you have a 12-V via going into a 3-V section of the board. In this situation, the board will fail.

Another example is the mixing of digital and analog signals. Analog ground is noisy, and it fluctuates. Digital ground needs to be quiet. Connecting digital and analog planes together probably won't result in a smoking board. There will, however, be anomalies from the noisy analog ground interfering with signals



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Checking this box will result in 2 different nets assigned to the Inner 1 layer. If two or more nets are to share the same plane layer but still be isolated from each other (called a split plane) then the isolation needs to be manually drawn and maintained by you on that plane layer.

Figure 1: Our CAD tool gives a loud warning, but some CAD tools assume that you are aware of this limitation and don't give any warning when you apply multiple nets to a layer.

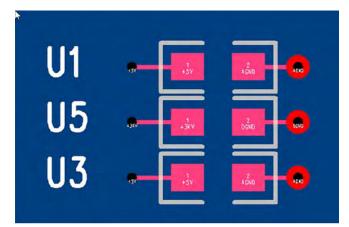


Figure 2: Notice how +5V and +3KV are both tied automatically to this plane and will not generate any error; however, it will let all of the magic smoke out of your PCB.

DRC Summary	? 💌
Uncheck error types you wish to ignor	re
✓ 2 Plane layer has multiple net as	ssignments warnings

Figure 3: Our CAM tool simply tells you that you have a split plane; it does not analyze the connections to that plane.

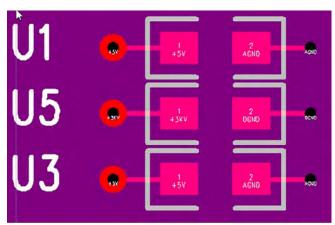


Figure 4: DGND and AGND are tied to the same area of the ground plane, which will cause noise on your analog ground and is not a lot of fun to troubleshoot; again, no error will be generated in the design tool.

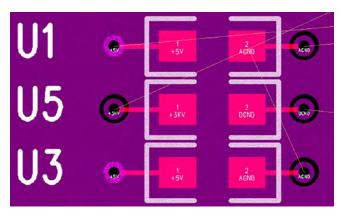


Figure 5: The drawn polygon assigned to +5V will not connect to any other vias, shorts will be avoided, and +3KV net will show up as open; you will get a warning that U5 is in the wrong space. Also, notice the guide wires from unconnected pins.

on digital pins. If you are relying on manual oversight to discover these issues before production, it's easy to lose track of individual connections, especially on a complex board design with hundreds of vias.

Best Practices for Managing Mixed-signal Output

For simpler designs, when you need to assign one or more power nets to a layer, it makes sense to apply plane splits and segregate areas containing each voltage. This is an efficient way to distribute power, but it relies on human input to ensure accuracy and gets risky for more complex boards. We think a better method is to use polygon area fills to make connections. With polygon area fills, when you name each, net connections on all layers become visible and vias of different nets will not connect. This enables your CAM tool to perform error checking on your separate area fills automatically.

As you design, there are steps you can take to prevent problems with mixed signal output. First, partition your PCB with separate digital and analog areas:

- Make sure digital and analog components are assigned to their respective areas
- Never route digital signals through analog territory and vice versa

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- Straddle analog to digital converters along the border of the two territories
- Use a single, solid ground plane
- If you have to route a signal trace from one area to the other, place it entirely over the PCB's ground plane

Second, keep the power ground and control ground separate for each power supply stage. Also, to keep your digital and analog grounds separate, build in a small impedance path. This will limit power circuit interference and help protect your control signals.

Finally, pay attention to routing. For example, you want your analog grounds crossed only by analog lines. This will reduce capacitive coupling on a large ground plane with lines routed above and under it.

Prevention Begins With Awareness

Knowing what the error checker will and will not catch regarding connections to split planes is the first and most important step to preventing exploding PCBs. We believe that the best method for dealing with complex power plane schemes is one that can rely on automated error checking. **DESIGN007**

Bob Tise and **Dave Baker** are engineers at Sunstone Circuits. To read past columns or contact Tise and Baker, click here.



Bob Tise



Fraunhofer and Forming Technology IWU Develop Interactive Control for Industrial Robots

The Fraunhofer Institute for Machine Tools and Forming Technology IWU has developed an unprecedented technology to make human-machine teamwork more efficient, benefiting the entire manufacturing workflow.

"We have added effective, secure, and flexible interaction to legacy technology. This is the first time humans can communicate and collaborate directly with heavyduty robots based on hand gesture in the industry," says Dr.-Ing. Mohamad Bdiwi, head of the department for robotics at Fraunhofer IWU. For collaboration on the shop floor, the machine recognizes human gestures, faces, and postures when a person enters the robot's work zone. This data serves to make the teamwork safe and control the robot. Humans can gesture, using hands and arms to instruct the mechanized coworker to perform a task. The robot can interpret even complex movements.

The robot not only tracks hands but also scans faces. For example, if the human glances sideways or rearward to talk to another coworker, the machine knows to ignore



gestures meant for others.

Humans and the robot can work together directly and even pass parts and tools back and forth. The robot sees when a hand is too close to the worker's face and waits for it to be extended out of the danger zone before handing the object over. This human-robot interaction comes courtesy of smart algorithms and 3D cameras that lend the robot the power of sight.

(Source: Fraunhofer Institute)



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Thermal Management Materials: Golden Rules for Product Selection

Sensible Design by Jade Bridges, ELECTROLUBE

Electrolube's Jade Bridges offers more advice about which product type you should select and use based on a thorough appraisal of the assembly, its application and environmental limitations, and the problems that are likely to arise during production. She also offers two golden rules to help you avoid those costly mistakes.

Selecting the right type of thermal management method that will suit a particular electronic assembly and its predicted operating conditions is far from easy. There are a number of stages in the selection process that you should consider taking before you decide upon a particular material or material format, whether paste or pad. In this column on achieving effective thermal management of electronic assemblies, I will revisit our trusted question-and-answer format to bring you some essential pointers, beginning with a few cautionary notes on pain points—the occasional pangs of agony you will have to face during the decision-making process.

1. What key pain points are associated with thermal management products?

Well, where do I begin? There are a host of materials and methods out there to choose from, and they serve a variety of purposes depending upon the physical constraints of the application, its environmental considerations, the severity of duty, component layout, assembly geometry, etc.

When choosing an appropriate product, a first question to ask yourself is, "What data can be relied upon?" Certainly, there are some excellent technical data sheets out there that any self-respecting supplier will have taken great care to produce accurately and in good faith. But do you really know what thermal conductivity you will need, for example? And do you know how much material will be needed in the interface between component and heat sink to achieve a thermally stable assembly?

Think about the practicalities and how you intend to apply the material. Will it be manual

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or automated? And don't forget those niggling details that tend to get overlooked such as the conditions of the operating environment, which might cause pump-out, for example); migration of the interface material and its effects on the surrounding components or the materials used in the construction of the assembly, which are likely to include sensitive plastics; and special coatings. For guidance on all of this, read on.

2. How do I avoid these pain points?

To answer this and the questions raised in the previous paragraphs, let me give you two golden rules that should at least get you on the right path to making informed choices.

Rule 1

By all means, read through the technical data sheets, but don't just compare the values on paper. Get some product samples and see how they behave in a real application. A good supplier will be more than happy to accommodate this type of request, and some may even offer in-house test facilities to help you make the right decision. I cannot stress enough the importance of this test-before-you-buy approach. If a thermal management product is not tested before use, the end performance of your product might be very different to what

If a thermal management product is not tested before use, the end performance of your product might be very different to what you expected.

you expected. If you value your reputation in the market, it is vital to ensure that the desired efficiency of heat transfer can be achieved and retained over the expected lifetime of your product.

Rule 2

Taking a cue from the property market, it's all about application, application, application! Make sure the product chosen matches your production needs, and don't forget those rework requirements, which will slant your choices towards specific material chemistries. Also, don't be reticent in seeking advice. Speak to your thermal management materials supplier about your key requirements both in the application and final use to ensure the best combination of properties are present in your final material choice.

3. How do I know that my thermal management choice is the best solution for the job?

The most common way to evaluate the performance of a thermal management product is to check the thermal resistance between the component and heat sink with and without the thermal management product applied. Another common method is to measure the device or component operating temperature with and without the thermal management product applied.

As previously mentioned, it is vitally important to ensure that the thermal management product applied continues to perform satisfactorily throughout the expected lifetime of the product. To ascertain this, the performance of the device or the thermal resistance between it and the heat sink need to be measured again after accelerated aging or environmental tests that simulate the real-world application conditions. This is the only way you be sure that the thermal management product chosen is really suitable for the job.

Don't forget, whatever your choice is, you need to consider the application of the thermal management product and the volumes that will be needed for production. Make sure the chosen product also meets your needs in terms of ease of application, and that its dispensing/application rate is compatible with production line speeds.

4. How do I apply a thermal paste?

Thermal pastes are designed to be applied as thin, uniform films. They should cover the

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entire surface area of the mating contact with no excess. Any excess that is pushed out from the interface when, for example, the component to be thermally managed is brought together with its heat sink, should be removed. Apply too much thermal paste, and it may cause issues with extrusion outside the interface boundaries, oil bleed, and most importantly, increased thermal resistance, resulting in reduced heat transfer efficiency. Thermal pastes can be applied via screen or stencil printing or by using specially designed dispensing equipment. In all cases, the correct amount of thermal paste should be calculated to ensure only the minimum thermal paste required is deposited at the interface.

5. Why would I choose a gap pad over traditional thermal paste?

So far, I've concentrated on thermal pastes, which are essentially liquids of varying viscosities and supplied in several chemical types. Another method is to use gaps pads—sheet materials that can be pre-cut to the size and shape that is required. They are simple and easy to use and typically being applied manually to the surface, so there's no requirement for mixing, preparation, or curing stages. The answer is that gap pads can be a viable solution, particularly for low-volume, hand-assembly operations.

Conclusion

Hopefully, I have suggested some easier routes through the minefield of thermal management material choices! Look out for my next column where I will shed more light on thermal management issues. **DESIGN007**



Jade Bridges is global technical support manager at Electrolube. To read past columns from Electrolube, click here. To download your copy of Electrolube's micro eBook, The Printed Circuit Assembler's Guide to...

Conformal Coatings for Harsh Environments, click here.

AI Instantly Captures Materials' Properties

Researchers at Aalto University and the Technical University of Denmark have developed an AI to seriously accelerate the development of new technologies from wearable electronics to flexible solar panels. Artificial intelligence for spectroscopy (ARTIST) instantly determines how a molecule will react to light, which is clinchpin knowledge for creating the designer materials needed for tomorrow's technology.

With ARTIST, the research team offers a paradigm shift how we determine the spectra—or response to light—of

individual molecules. ARTIST has the potential to speed up the development of flexible electronics including lightemitting diodes (LEDs) or paper with screen-like abilities. Complementing basic research and characterization in the lab, ARTIST may also hold the key to producing better batteries and catalysts as well as creating new compounds with carefully selected colors.

The multidisciplinary team trained the AI in just a few weeks with a dataset of more than 132,000 organic molecules. ARTIST can predict with exceptional accuracy how

> those molecules—and others similar in nature—will react to a stream of light. The team now hopes to expand its abilities by training ARTIST with even more data to make a more powerful tool.

> The researchers aim to release ARTIST on an open science platform this year. It is currently available for use and further training upon request.

(Source: Aalto University)

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Nano Dimension Expands EMEA Presence >

Nano Dimension Ltd. has signed contracts with two EMEA-based resellers to market Nano Dimension's award-winning DragonFly Pro additive manufacturing platform for printed electronics in Belgium, the Netherlands, Luxemburg (the Benelux region), and Israel.

National Circuit Assembly Renews AS9100D Certification >

National Circuit Assembly—a provider of PCB, cable, and electromechanical manufacturing and test services to leading OEMs—announced that it successfully completed the recertification audit for its AS9100D certification.

Ventec Recertified to AS9100 Revision D and IATF 16949 ►

Both Ventec's China and U.K. facilities are certified to AS9100 Revision D quality standard, providing OEM's and PCB fabrication customers servicing the aviation, space, and defense industries access to a fully accredited supply chain for high-reliability laminates and prepregs.

All Flex Partners with Minnesota Wire for Stretch Flex Technology >

All Flex is proud to assist Minnesota Wire with several new exciting technologies expanding their iSTRETCH product line using innovative stretch flex technology.

Eltek Reports Revenues of \$8.5 Million in 3Q18 ►

The third quarter of 2018 was the first quarter for Eli Yaffe as Eltek's CEO. Revenues were \$8.5 million—up 10% from Q3 of 2017—and the net loss decreased to \$463,000 from a net loss of \$1.2 million in Q3 of 2017.

ILFA Takes Off as Certified Aerospace Supplier >

ILFA is a high-tech PCB manufacturer located in Hanover, Germany, for 39 years, and has been working with well-known customers from the aviation and aerospace industry for a long time.

Amphenol Invotec Secures Nadcap Approval for its Telford Site >

Amphenol Invotec's Telford site has been awarded Nadcap accreditation. This achievement complements the Nadcap Merit status already awarded to its Tamworth site and represents a clear demonstration of the company's commitment to the highest standards of reliability and quality.

Defense Speak Interpreted: PERM–Pb-free Electronics Risk Management >

This column explores PERM—the Pb-free Electronics Risk Management Consortium. The name was chosen around 2008 by a group of engineers from aerospace, defense, and harsh environment (ADHE) organizations.

NASA to Develop Reusable Systems for Moon Landing >

As the next major step to return astronauts to the Moon, NASA announced plans to work with American companies to design and develop new reusable systems for astronauts to land on the lunar surface. The plan is to test new human-class landers with the goal of sending crew to the surface in 2028.

China Set to Impose Stricter Regulations on PCB Industry ►

China will implement a new set of strict regulations on the operations of the PCB industry on February 1, which may threaten the survival of small- to medium-size makers.



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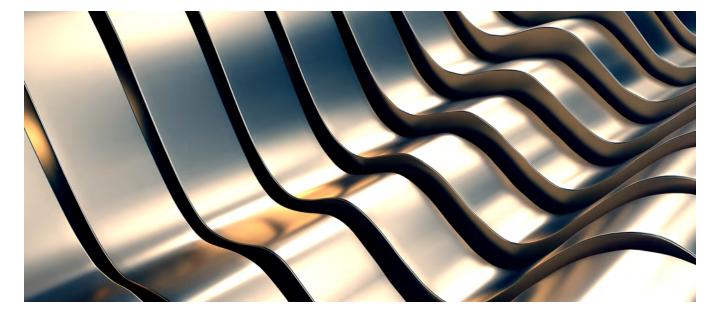
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3DEM Modeling: Influence of Metal Plating on PCB Channel Loss and Impedance

Article by Chang Fei Yee

KEYSIGHT TECHNOLOGIES

This article briefly introduces different types of metal plating commonly used in PCB fabrication. Subsequently, the influence of metal plating on PCB channel loss (i.e., insertion loss or S21) and impedance (i.e., time domain reflectometry or TDR) is studied with 3DEM modeling using Keysight EMPro.

Introduction

Metal plating that serves as a protective layer is applied on top of the copper traces during PCB fabrication, thus alleviating the oxidation process of the copper. Common finishes include immersion silver (IAg), electroless nickel immersion gold (ENIG), etc. With immersion silver, nearly pure silver (i.e., ~0.02 mils in thickness) is coated over the copper traces on a PCB. Meanwhile, with ENIG, nickel (i.e., ~0.2 mils in thickness) is deposited on the copper trace followed by a coating of gold (i.e., ~0.01 mils in thickness) on top. Nickel serves as a barrier layer to prevent the migration of gold into the base copper. However, metal plating comes with disadvantages. On a PCB, the current of the signal tends to propagate more closely to the surface of the trace when the frequency of the signal becomes higher. Skin depth is the parameter that determines how extensive the current of signal travels with reference to the surface of the transmission channel. The relationship between skin depth and signal frequency is governed by Equation 1. For instance, at frequency 10 GHz, skin depth becomes 0.026 mils.

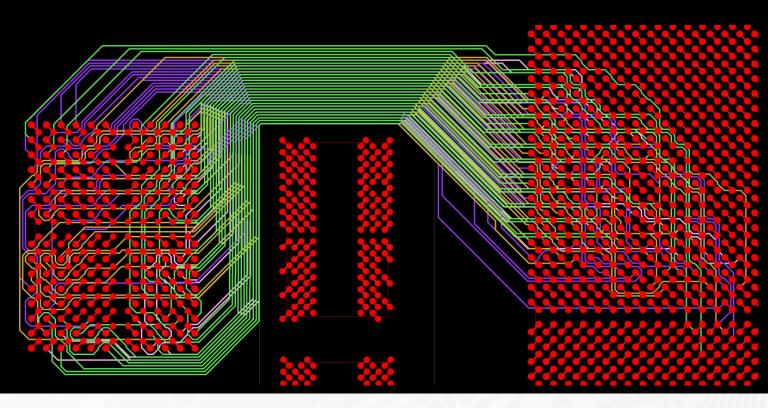
Equation 1.

$$\sigma \approx 66 \times \sqrt{\frac{1}{f}}$$

 σ = skin depth in microns f = frequency of the signal in MHz

Equations 2, 3, and 4 indicate that attenuation of the signal is inversely proportional to the metal conductivity. Once metal with lower conductivity is coated over a copper trace, the signal experiences a larger amount of attenuation. For instance, skin depth becomes 0.026 mils at a signal frequency of 10 GHz. If ENIG

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plating (i.e., base copper 1.09 mils, nickel 0.2 mils in the mid layer, and gold 0.01 mils on top) is applied, the high-frequency signal will propagate on the gold and nickel-plated layers. This signal will encounter a larger magnitude of attenuation due to the lower conductivity of nickel.

Equation 2.

Equation 3.

 $\alpha_{c} = 8.686 \times \frac{R^{1}}{2 \cdot Z_{0}}$ $\rho = R \frac{A}{l}$ $\sigma = \frac{1}{\rho}$

Equation 4.

 $\begin{array}{l} \alpha_{c} = \text{attenuation due to metal conductivity in dB/meter} \\ R = \text{series resistance of metal trace in ohm/meter} \\ Z_{0} = \text{trace impedance in ohm} \\ \rho = \text{resistivity in ohm-meters} \\ \sigma = \text{conductivity in Siemens/meter} \\ l = \text{trace length in meters} \\ A = \text{cross-sectional area of the trace in meters}^{2} \end{array}$

Referring to Table 1, silver has the best conductivity, followed by copper, gold, and nickel. Nickel's conductivity is less than half that of gold. A thicker layer of gold or a better conductor on top (i.e., one that is enough to cover the skin depth) alleviates the attenuation. This phenomenon is proven in simulated cases to be discussed in the following section.

Metal	Conductivity (x10 ⁷ Siemens/m)
Copper	5.8
Silver	6.3
Gold	4.5
Nickel	1.5

Table 1: List of metal conductivity.

Model	Nominal single- ended impedance (ohms)	Description
А	50	Bare copper 1.3 mils, no plating Bare copper 1.3 mils, no plating
В	50	Base copper 1.28 mils, plating silver 0.02 mils on top
С	50	Base copper 1.09 mils, plating nickel 0.19 mils in the mid layer and gold 0.02 mils on top
D	50	Base copper 1.09 mils, plating nickel 0.2 mils in the mid layer and gold 0.01 mils on top

Table 2: List of models for metal plating on PCB microstrip.

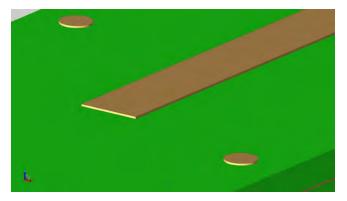


Figure 1: Microstrip Model A in Keysight EMPro.

Analysis and Results

To study the influence of metal plating on PCB channel loss (i.e., insertion loss or S21) and impedance (i.e., time domain reflectometry or TDR), four models of a one-inch long microstrip are constructed and listed in Table 2. For Model A as depicted in Figure 1, bare copper trace (i.e., 38 mils wide and 1.3 mils thick) without plating is laid out 17.5 mils above the reference plane and insulated by low-loss dielectric substrate material. Model B mimics immersion silver plating with 0.02mil silver on top. Meanwhile, Model C mimics ENIG plating with nickel and gold on top. Model D has slightly thicker nickel but thinner gold versus Model C. All four models have the same overall trace thickness and width and dielectric substrate material and thickness but without solder mask.

With reference to S21 plots depicted in Figure 2, Models A and B experience almost the similar insertion loss due to slightly higher conductivity for silver versus copper. Meanwhile, Model C with 0.19-mil thick nickel (i.e.,

much lower conductivity) in the mid layer and 0.02 mils of gold on top encounters an additional 0.06 dB attenuation at 10 GHz versus Models A and B, created by overlapping between skin depth with the mid nickel layer. Further decreasing the top gold coating and increasing the mid nickel layer intensifies the attenuation, resulting in extra 0.04 dB PCB loss for Model D versus Model C. Meanwhile, the TDR plots

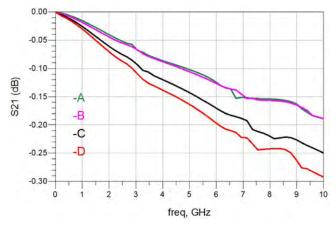


Figure 2: S21 plots for models listed in Table 2.

depicted in Figure 3 indicate that metal plating or coating on top of the copper trace reduces the single-ended characteristic impedance by 1 ohm versus Model A (i.e., bare copper without plating).

Summary

For the fabrication of PCBs with high-frequency signal routing beyond 5 GHz, the selection of metal plating is very important. Besides degradation due to oxidation, hardware designers should also consider the skin effect and attenuation contributed by the conductivity of the plating material. **DESIGN007**

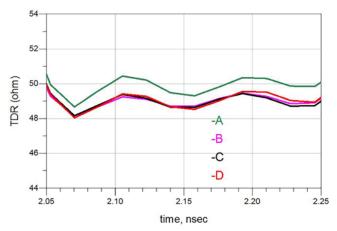


Figure 3: TDR plots for models listed in Table 2.

Further Reading

1. Coonrod, J. "Circuit materials and high-frequency losses of PCBs," *The PCB Magazine*, February 2012.

2. Henninger, T. "PCB Surface Finishes," Viasystems presentation.

3. Olney, B. "Effects of Surface Roughness on High-speed PCBs," *The PCB Design Magazine*, February 2015.



Chang Fei Yee is a hardware engineer with Keysight Technologies. His responsibilities include embedded system hardware development, and signal and power integrity analysis.

Robert Art on the Importance of Thermal Management



In an interview with I-Connect007 Technical Editor Pete Starkey, Robert Art, global account manager for IMS materials at Ventec International Group, discusses future market requirements for thermal management materials, and the need for a better

understanding of the concept of thermal impedance.

"The market is looking for what it has always looked for—better thermal performance. In every sales meeting and discussion with customers and at trade show events, the engineering community is always looking for better thermal performance. We continue to push the envelope when it comes to developing stronger, more reliable robust dielectrics that can be thinner to reduce thermal impedance and resistance values," says Art.

Another topic in discussion was solder joint reliability. Art noted that solder joint reliability is a big concern today for many customers, and not exclusive to the automotive electronics market. "If you look at our roadmaps, some of the product offerings we're pursuing not only improve the thermal performance or peel strength but also the modulus of the dielectric to make it more conducive to providing a solid solder joint. Solder joint fatigue is a big issue in our marketplace today, and that's an area of focus for our future development," said Art.

To read the full interview, click here. (Source: I-Connect007)



Editor Picks from PCBDesign007

CES 2019 Showstoppers, the Show Floor, and Some Neat Stuff >

CES 2019 is over, and those of us who spent four to five days trying to see and hear as much as possible are in recovery mode. There were over



FOP

182,000 attendees, and 6,600 of us were media all trying to get to as much of the 2.9-millionsquare-feet exhibit space as possible.

AltiumLive Munich: 🕘 Day 1 Keynotes 🕨

AltiumLive brought together a family of over 220 electronics engineers and designers eager to learn from top industry experts and applications specialists who were equally eager to share their



knowledge and experience freely.



AltiumLive Munich Draws Designers from Around Europe 🕨

Andy Shaughnessy spoke with designers from Germany, Austria, the Netherlands, and Belgium, just to name a few countries. Many of them were involved in the automotive segment but some were in medical and industrial controls as well. It's great to be at an event that is full of PCB designers, because designers are few and far between at most PCB industry events.



Happy Anniversary, Gerber Format: Looking Ahead to Digital Innovation >

We can thank H. Joseph Gerber, the man who took manual PCB design to the next level with the automated photoplotter, for giving us this format in 1964. Gerber started Gerber Scientific Instrument



Company in 1948 to commercialize his first patented invention—the variable scale.

5 The Digital Layout: Chapter Highlights and Certification Successes ►

This month's column highlights the San Diego chapter, which is also where IPC APEX EXPO 2019 will be held at the end of January. You will also find updates on recent CID and CID+ certification success



stories, a recap of the PCB Carolina event from the Research Triangle Park (RTP) North Carolina chapter, and upcoming events, so mark your calendars for next year.

6 Arlon EMD Accelerates Investments in Operations ►

Arlon EMD, a veteran-owned manufacturer of high-performance polyimide and other specialty resin materials based in Rancho Cucamonga, California, has completed another phase of facility improvements targeting enhanced cleanliness of laminate and prepreg. This investment in operational improvements is the third in the past 18 months and the fifth capital investment over the past 36 months focused on material cleanliness.

7 RTW IPC APEX EXPO 2019: Oren Manor Details New Camstar Electronics Suite ►

Nolan Johnson meets with Oren Manor—director of business development for Mentor, a Siemens Business—to discuss the introduction of their new Camstar Electronics Suite soft-



ware, an innovative manufacturing execution system (MES) for electronics.

8 TUM Hyperloop Team Learns PCB Design on Way to Setting World Speed Record ►

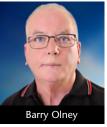
At AltiumLive Munich, Andy Shaughnessy met with Tobias Bobrzik, a Technical University of Munich student and member of the TUM Hyperloop team. In 2018, the TUM Hyper-



loop team's prototype pod set the world speed record of 290 miles per hour, which lead to their meeting with Musk. Tobias designed some of the PCBs used in that vehicle, so I asked him to tell us more about this experience, and what he hopes to do after graduation.

9 10 Fundamental Rules of High-speed PCB Design, Part 5 >

The final part of the 10 fundamental rules of high-speed PCB design focuses on boardlevel simulation encompassing signal integrity, crosstalk, and electromagnetic compliancy. Typically, a high-speed



digital design takes three iterations to develop a working product. However, today, the product life cycle is very short, and therefore, time to market is of the essence. The cost per iteration should not only include engineering time but also consider the cost of delaying the products market launch.



Mentor, a Siemens business held a webinar on "Correct Model Assignments for SI (Full Flow)" on February 21, 2019, 8:30 a.m. to 9:30 a.m. U.S. Pacific.

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Sales Development Representative (SDR)

The sales development representative is responsible for initiating contact with potential customers generated through a variety of marketing efforts. The goal of this position is to identify customer needs, qualify their interest and viability, and create a relationship that will help drive sales by ultimately moving these leads through the sales funnel to deliver a highly qualified lead to Sunstone's customer support team.

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Marketing Customer Loyalty and Insight Manager

The marketing customer loyalty and insight manager is responsible for proactive relationship building with Sunstone's current customers. This position coordinates, executes, and manages outbound call programs built to effectively retain customers through positive relationship building, listening to concerns, addressing issues, and educating on available products and services. A customer-orientated focus is necessary to preserve long-term customer satisfaction. This position requires someone that is highly organized, has excellent communication skills, and displays good-judgment.

Essential Duties and Responsibilities (Other Duties as Assigned)

- Displays excellent communication skills including presentation, persuasion, and negotiation skills often required in working with customers and colleagues, including the ability to communicate effectively and remain calm and courteous under pressure
- Directly support the marketing department by focusing on outreach activities to create, build, maintain, and rebuild customer relationships
- Provide and report to the marketing team all valuable feedback, market intelligence, and statistics obtained by you from our customers
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- Salary: \$16.00 to \$24.00 /hour
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The role will develop practical, scalable 3D machine learning solutions to solve complex challenges that detect, recognize, classify, and track medical imagery. Additional focus on the design, implementation, and deployment of full-stack computer vision and machine learning solutions.

The ideal candidates will hold a master's (doctorate preferred) in computer science or electrical engineering with at least three years of relevant experience. We desire a strong understanding of machine learning and computer vision algorithm application within embedded systems, plus significant vision expertise in multi-view geometry, 3D vision, SFM/SAM, and activity recognition.

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- High willingness to travel and have flexible employment
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- Create and conduct customer technical presentations.
- Develop technical strategy for customers.
- Possess the ability to calm difficult situations with customers, initiate a step-by-step plan, and involve other technical help quickly to find resolution.

Hiring Profile

- Bachelor's Degree or 5-7 years' job related experience.
- Strong understanding of chemistry and chemical interaction within PCB manufacturing.
- Excellent written and oral communication skills.
- Strong track record of navigating technically through complex organizations.
- Extensive experience in all aspects of Customer Relationship Management.
- Willingness to travel.



Service Engineer USA

Limata GmbH, a provider of direct imaging system solutions for the global PCB manufacturing industry and adjacent markets, is looking for qualified candidates to fulfill the role of service engineer in the United States.

Duties:

- Assemble, install, service, and maintain our products
- Inspect the unit towards operating conditions
- Solve technical problems on-site
- Resolve problems with our customers and technical department
- Ability to support our customers in all technical questions

Qualifications:

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- Willingness to travel
- Strong verbal and written communication skills

To be part of our team, please click below and send your resume to karriere@limata.de.



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Manncorp, a leader in the electronics assembly industry, is looking for a technician to operate our new in-house SMT LED assembly lines.

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- Set up and operate automated SMT assembly equipment
- Prepare component kits for manufacturing
- Perform visual inspection of SMT assembly
- Participate in directing the expansion and further development of our SMT capabilities

Requirements and Qualifications:

- Prior experience with SMT equipment, or equivalent technical degree preferred
- Basic computer knowledge
- Proven strong mechanical and electrical troubleshooting skills
- Experience programming machinery or demonstrated willingness to learn
- Positive self-starter attitude with a good work ethic
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We Offer:

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Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

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- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:

- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
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- Health and dental insurance
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Skills and abilities required for the role:

- Scientific and technical educational background
- Experience in the PCB industry in engineering and/or manufacturing
- Strong communications skills (German and English) with the ability to write full technical reports for group or customer distribution
- Ability to work in an organized, proactive, and enthusiastic way
- Ability to work well both in a team as well as an individual
- Good user knowledge of common Microsoft Office programs
- A full driving license is essential
- Willingness to travel regularly throughout Europe and occasionally to Asia

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Skills and abilities required for the role:

- Seven to 10 years of experience in the PCB industry in engineering and/or manufacturing
- Strong communications skills (German and English)
- Project management experience
- Detail-oriented approach to tasks
- Ability to manage tasks and set goals independently as well as part of a team
- Knowledge of Microsoft Office products
- A full driving license is essential.
- Willingness to travel regularly throughout Europe and occasionally to Asia

We offer:

• Excellent salary and benefits commensurate with experience

This is a fantastic opportunity to become part of a successful brand and leading team with excellent benefits.

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Field Service Engineer West Coast

Pluritec North America, ltd., An innovative leader in drilling, routing and Automated Inspection in the Printed Circuit Board industry, is seeking a full-time Field Service Engineer, located on the West Coast.

This individual will support service for North America in Equipment installation, training, maintenance and repair. Candidate must be able to handle trouble shooting electronic and mechanical issue's as well customer applications in the field. A technical degree is preferred, along with strong verbal and written communication skills. The position requires the ability to travel 2-3 weeks per month.

> Please send your resume to: Carolina.zeppieri@pluritec.org

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Sales Personnel, Japan

The Gardien Group is looking to expand the sales team in Tokyo, Japan, and seeking highly motivated team players with a positive attitude. Prior experience in the PCB industry is an advantage but not necessary for the right candidate.

The role involves working closely with the customer to identify their needs and deliver the right solution. The candidate should be able to offer a high level of customer satisfaction to ensure ongoing sales.

Training will be provided along with a competitive benefits package, excellent growth opportunities, and periodic bonuses.

Interested candidates, please contact us at careers.jp@gardien.com with your resume.

Kindly note only shortlisted candidates will be notified.



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Escondido-based printed circuit fabricator U.S. Circuit is looking to hire sales representatives in the following territories:

- Florida
- Denver
- Washington
- Los Angeles

Experience:

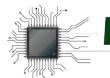
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Multiple Positions Available

Want to work for a fast-growing company? MivaTek Global may be the place for your next career move. 2018 has brought significant growth, increasing sales and revenue. And, we are just getting started! To support the current customer base and fuel further expansion, we are looking for bright and talented people who are energized by hard work in a supportive and flexible environment.

Open Positions:

- Technical Service Technicians
- Regional Sales Representatives
- Regional Leader for Asia Sales and Support

Proven experience in either PCB or Microelectronics and willingness to travel required for all positions.

More About Us

MivaTek Global is a distributor of manufacturing equipment with an emphasis of Miva Technologies' Direct Imager, Mask Writer, Flatbed Photoplotter imaging systems and Mach3 Labs X-Ray Drills. We currently have 45 installations in the Americas. Expansion into Asia during 2018 has led to machine installations in China, Singapore, Korea, and India.

To be part of our team, send your resume to n.hogan@kupertek.com for consideration of current and future opportunities.



We Are Recruiting!

A fantastic opportunity has arisen within Electrolube, a progressive global electrochemicals manufacturer. This prestigious new role is for a sales development manager with a strong technical sales background (electro-chemicals industry desirable) and great commercial awareness. The key focus of this role is to increase profitable sales of the Electrolube brand within the Midwest area of the United States; this is to be achieved via a strategic program of major account development and progression of new accounts/ projects. Monitoring of competitor activity and recognition of new opportunities are also integral to this challenging role. Full product training to be provided.

The successful candidate will benefit from a generous package and report directly to the U.S. general manager.

Applicants should apply with their CV to melanie.latham@hkw.co.uk (agencies welcome)



Zentech Manufacturing: Hiring Multiple Positions

Are you looking to excel in your career and grow professionally in a thriving business? Zentech, established in Baltimore, Maryland, in 1998, has proven to be one of the premier electronics contract manufacturers in the U.S.

Zentech is rapidly growing and seeking to add Manufacturing Engineers, Program Managers, and Sr. Test Technicians. Offering an excellent benefit package including health/dental insurance and an employer-matched 401k program, Zentech holds the ultimate set of certifications relating to the manufacture of missioncritical printed circuit card assemblies, including: ISO:9001, AS9100, DD2345, and ISO 13485.

Zentech is an IPC Trusted Source QML and ITAR registered. U.S. citizens only need apply.

Please email resume below.



PCB Manufacturing, Marketing Engineer

Use your knowledge of PCB assembly and process engineering to promote Mentor's Valor digital manufacturing solutions via industry articles, industry events, blogs, and relevant social networking sites. The Valor division is seeking a seasoned professional who has operated within the PCB manufacturing industry to be a leading voice in advocating our solutions through a variety of marketing platforms including digital, media, trade show, conferences, and forums.

The successful candidate is expected to have solid experience within the PCB assembly industry and the ability to represent the Valor solutions with authority and credibility. A solid background in PCB Process Engineering or Quality management to leverage in day-to-day activities is preferred. The candidate should be a good "storyteller" who can develop relatable content in an interesting and compelling manner, and who is comfortable in presenting in public as well as engaging in on-line forums; should have solid experience with professional social platforms such as LinkedIn.

Success will be measured quantitatively in terms of number of interactions, increase in digital engagements, measurement of sentiment, article placements, presentations delivered. Qualitatively, success will be measured by feedback from colleagues and relevant industry players.

This is an excellent opportunity for an industry professional who has a passion for marketing and public presentation.

Location flexible: Israel, UK or US

apply now



IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.



For information, please contact: BARB HOCKADAY barb@iconnect007.com +1 916.365.1727 (PACFIC)



2019 Programs

NORTH AMERICA

IPC TECH ED

April 2

King of Prussia, PA

Process and Acceptability Requirements: Utilizing J-STD-001 and IPC-A-610 Together

May 7

Milwaukee, WI (in conjunction with Electrical Wire Processing Technology Expo)

The Evolution of IPC's Cable & Harness Documents — IPC-D-620, IPC/WHMA-A-620 and IPC-HDBK-620

September 10

Huntsville, AL Process and Acceptability Requirements: Utilizing J-STD-001 and IPC-A-610 Together

November 12 Raleigh, NC (in conjunction with PCB Carolina) Topic Coming Soon

December 3

Anaheim, CA Process and Acceptability Requirements: Utilizing J-STD-001 and IPC-A-610 Together

MEETINGS

March 5–7 Raytheon in Huntsville, Alabama PERM Meeting

May 21 Washington, D.C. IPC IMPACT Washington, D.C.

June 15–20 Raleigh, NC IPC SummerCom: IPC Committee Meetings

CONFERENCES

February 19–22 Dallas, TX 2019 WHMA 26th Annual Wire Harness Conference

May 14–16 Baltimore (Hanover), MD IPC High Reliability Forum

June 3

Boston, MA ITI & IPC Conference on Emerging & Critical Environmental Product Requirements

June 5

Chicago, IL ITI & IPC Conference on Emerging & Critical Environmental Product Requirements

June 7 San Jose, CA

ITI & IPC Conference on Emerging & Critical Environmental Product Requirements

June 18–19

Raleigh, NC IPC SummerCom: Materials Conference

September San Jose, CA i4.0 Connect Forum in cooperation with IPC and i4.0 Today

September 11 Philadelphia, PA IPC E-Textiles 2019

EUROPE

April 1–2

Ingolstadt, Germany IPC Tech Ed – Cleaning Forum (in partnership with Zestron) May 6–7

Nuremberg, Germany IPC Automotive Electronics High Reliability Forum

September 23–24 Prague, Czech Republic IPC Wire Innovation Conference

September 26 Paris, France IPC Transportation Electronics Reliability Council Annual Meeting (ITERC)

November Brussels, Belgium IPC IMPACT Europe

November 11–12 Munich, Germany IPC E-Textiles Symposium

ASIA

June 25 Suzhou, Greater China IPC WorksAsia Automotive Electronics Forum

September 3 Beijing, Greater China IPC WorksAsia Aerospace & Aviation Forum

Oct 10–11 Shenzhen, Greater China HSRC South – PCB Design Seminar & Competition Productronica China 2019

December 18

Find more events in Asia on www.ipc.org/events

WISDOM	WEDNESDAY	WEBINARS	- Exclusive for	Members
February 20 March 20	April 17 May 22	June 26 July 17	August 21 September 18	October 16 November 2

For more information, visit www.IPC.org/events



Events Calendar

China International PCB & Assembly Show (CPCA Show 2019) >

March 19–21, 2019 Shanghai, China

MicroTech 2019 >

April 4, 2019 Cambridge, U.K.

SMTA Atlanta Expo >

April 11, 2019 Peachtree Corners, Georgia, USA

Medical Electronics Symposium 2019 >

May 21–22, 2019 Elyria, Ohio, USA

PCB Pavilion @ LCD EXPO Thailand >

June 27–29, 2019 Bangkok, Thailand

PCB West 2019 ► September 9–11, 2019 Santa Clara, California, USA

Medical Electronics Symposium 2019 ►

May 21–22, 2019 Elyria, Ohio, U.S.

PCB Pavilion @ LCD EXPO Thailand >

June 27–29, 2019 Bangkok, Thailand

Additional Event Calendars



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