I-Connect007

JANUARY 2018

DESIGN007 MAGAZINE

WHAT'S NEW IN EDA?

“This micro eBook should be required reading for every PCB designer or design engineer, whether novice or veteran.”

Andy Shaughnessy
Managing Editor, The PCB Design Magazine

In this second micro eBook from Mentor, A Siemens Business, written by signal integrity engineer, Fadi Deek, provides a thorough investigation of power distribution network performance and will help PCB designers and engineers of all experience levels make better design decisions.

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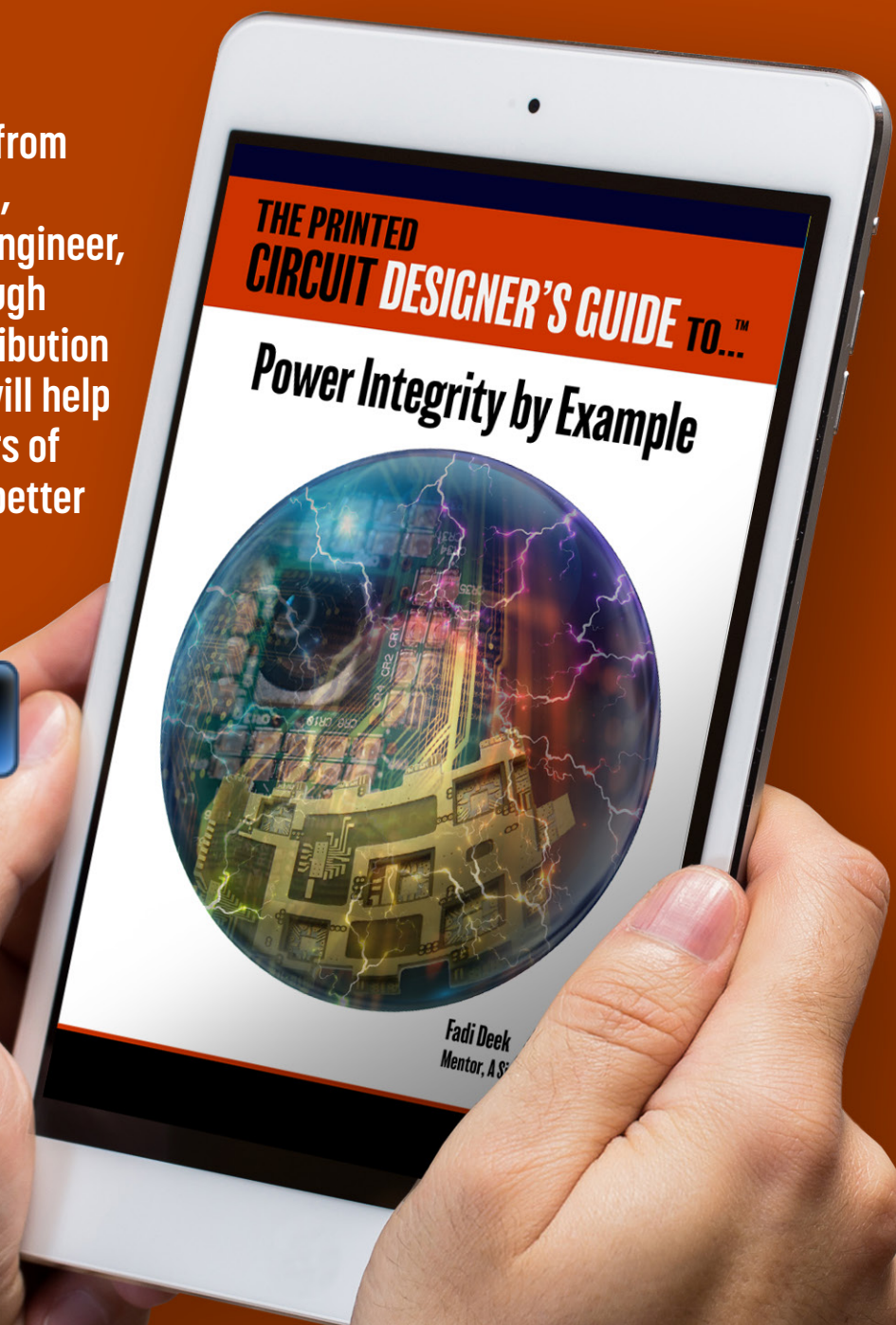
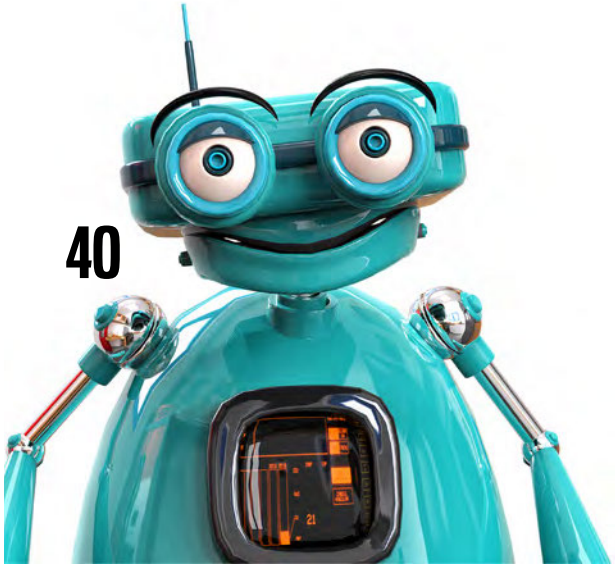


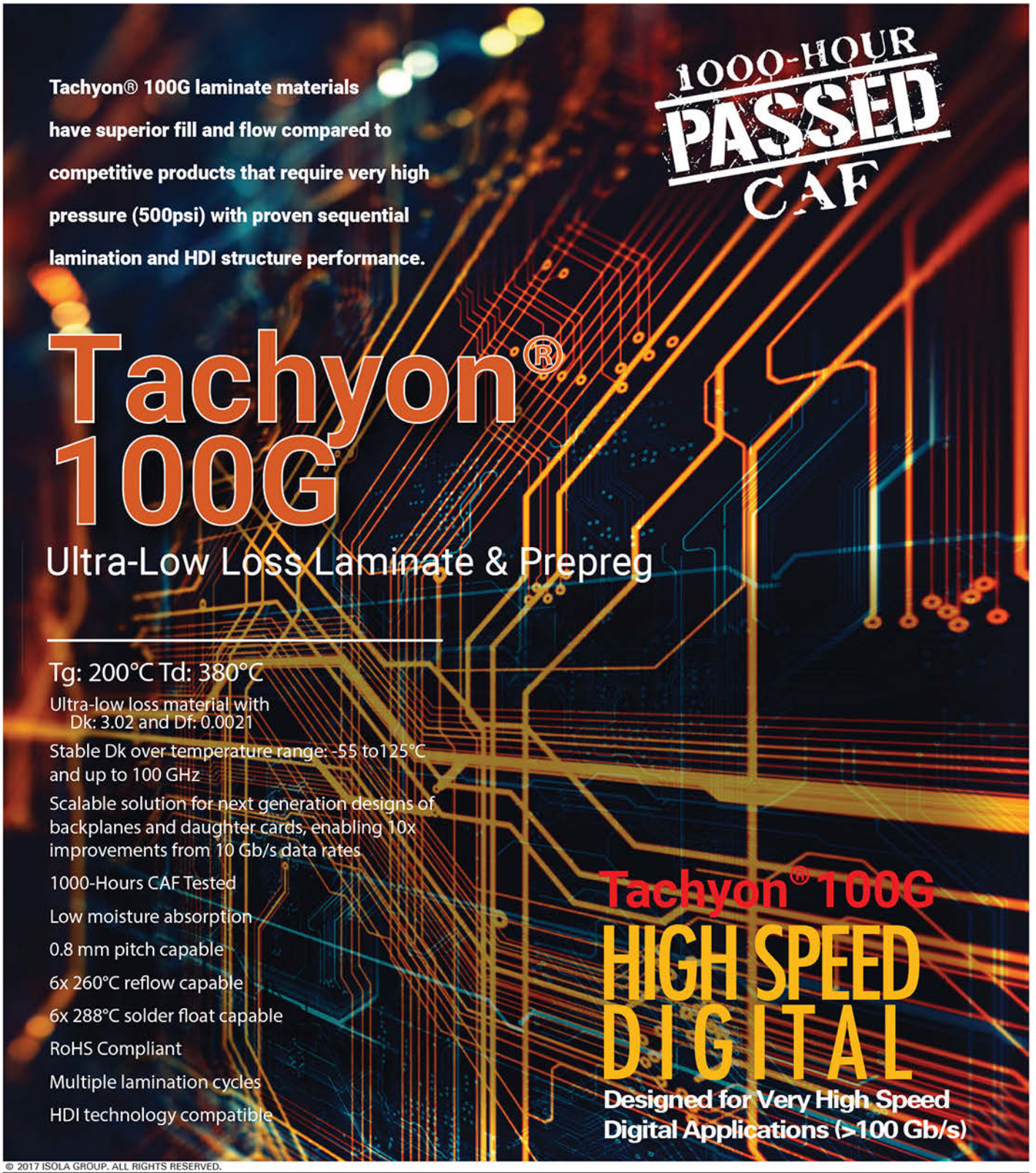
I·007e Books

DESIGN007 MAGAZINE

What's New?

It's a brand-new year, and the magazine has a fresh new look and title. So, to ring in the new year with this first issue of *Design007 Magazine*, we asked representatives from a variety of PCB design-related companies to answer the question, "What's New?"





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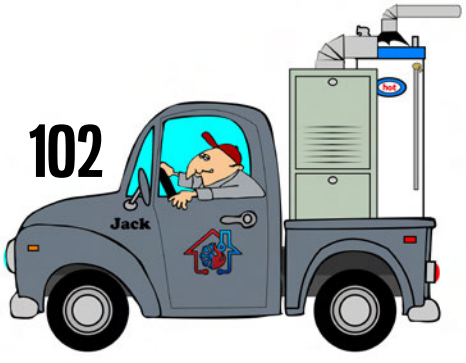

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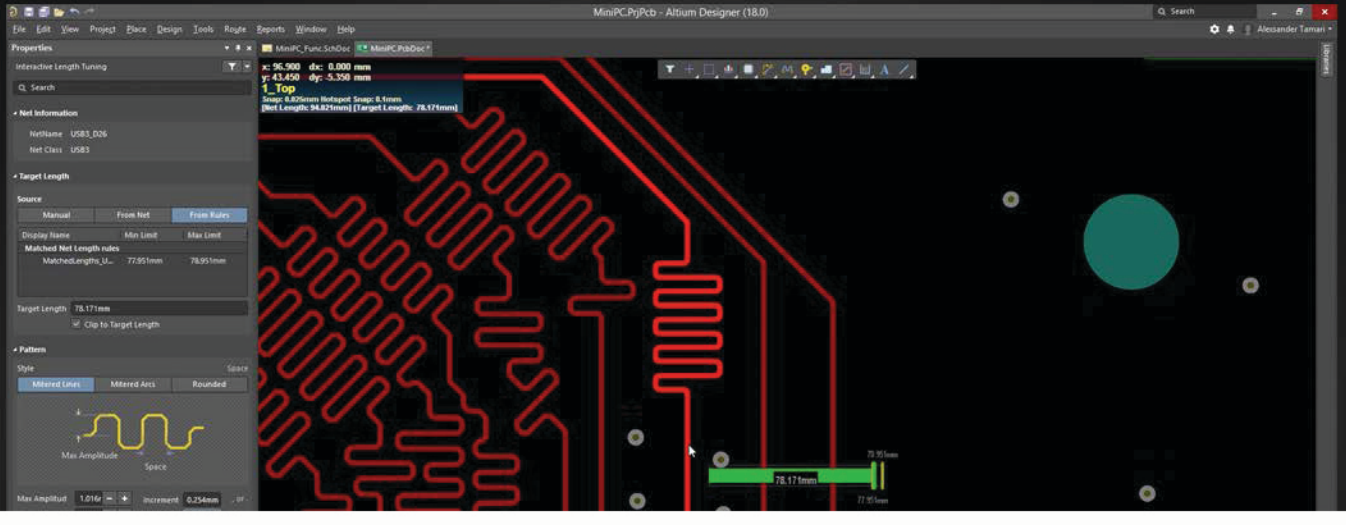

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New Year, New Title, and New Look

The Shaughnessy Report
by Andy Shaughnessy, I-CONNECT007

I can't believe it's 2018. When you were a kid and you imagined 2018, did you ever dream that we'd have autonomous vehicles, or artificial intelligence in so many new products?

Yes, it's a new year, and you may have noticed that the magazine has a new name, and a new look. Welcome to the premier issue of *Design007.* We have now unified all of our magazine titles under the I-Connect007 name, starting with *PCB007 China Magazine* in 2017, and now with *SMT007 Magazine, PCB007 Magazine,* and *Design007 Magazine.*

This will make things a lot simpler for all of us. And let's face it: many people in the industry still calls us 007, so it makes sense to have 007 in our titles. As the old saying goes, "Keep it simple, stupid."

You'll also notice that *Design007 Magazine* features a completely different layout now. It's much more open, and it feels less crowded. There's more white space, and the text and images have much more room to "breathe," as I like to say. It's very slick and uncluttered, and the images have more "pop" now.

I think you'll really enjoy the new *Design007 Magazine.* Our production department colleagues really outdid themselves this time; I don't know how they managed to design three new magazines while still working on everything else on their plates. Kudos to Shelly Stein and Ron Meogrossi for making this redesign a reality.

To ring in the new year with this first issue of *Design007 Magazine,* we asked representatives from a variety of PCB design-related companies to answer the question, "What's New?" For our first feature, we assembled a solid group of design veterans to take part in our expert discussion: Martyn Gaudion of Polar Instruments, Rick Almeida of DownStream Technologies, and Hemant Shah and Mark Hepburn, both with Cadence Design Systems. In a wide-ranging interview, they discuss everything from their companies' newest and coolest technologies to the slight uptick in new PCB designers recently.

Several of our contributors focus on improving automation this month. Ben Jordan of Altium explores the future of EDA and IoT,

and predicts that EDA tool companies will need to "put the 'A' back in EDA." Craig Armenti of Mentor is also bullish on automation, making the case for fully automated schematic verification in PCB design tools. In an interview, Karel Tavernier of Ucamco discusses his plans to enhance the automation of his company's CAM tools, as well as the venerable Gerber standard, and why he's such an advocate for artificial intelligence in the design process. And Ty Stephens of UK-based Pulsonix explains in an interview how his company plans to become a greater presence in the U.S., starting with their new component search engine that lets users bring in verified parts in one click. We also have great columns from our regular contributors Barry Olney of iCD, Jade Bridges of Electrolube, and consultant Tim Haag.

We're also including an IPC APEX EXPO 2018 pre-show supplement, featuring interviews with the IPC managers who put this show together each year. Designers shouldn't miss our interview with Nancy Jaster, manager of design programs at IPC, who has news about the speakers and events planned for this year's Design Forum during IPC APEX EXPO.

Yes, it's show time! Are you going to DesignCon, IPC APEX EXPO, or CPCA? If you are, we'd love for you to stop by our booth and chat about what's new in your neck of the woods. But if you can't make it to Santa Clara, San Diego or Shanghai, you can still keep up to date with our coverage of each show, from start to finish.

Let me know what you think about our new look. Now, we have a lot to do, so let's get cracking. See you next month!

DESIGN007

Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 18 years. He can be reached by clicking here.

Mysteries of a Promising Spintronic Material Revealed

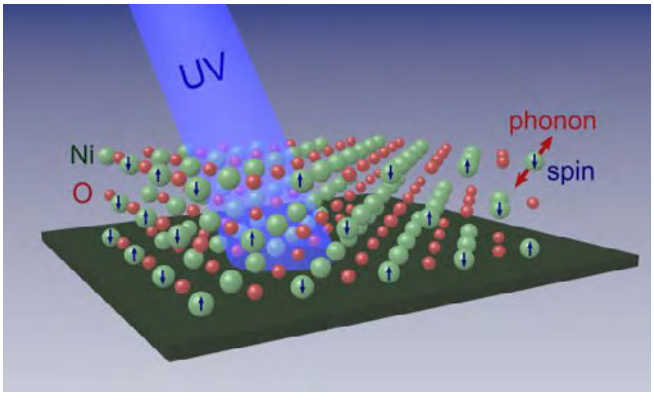
Researchers at UC Riverside used an unconventional approach to determine the strength of the electron spin interactions with the optical phonons in antiferromagnetic nickel oxide (NiO) crystals.

The interdisciplinary team of researchers, led by Alexander Balandin, distinguished professor of electrical and computer engineering, used ultraviolet Raman spectroscopy to investigate how spin ordering affects the energies of phonons in these materials. Practical applications of spintronic devices in information processing require accurate knowledge of the strength of the electron spin interaction with phonons.

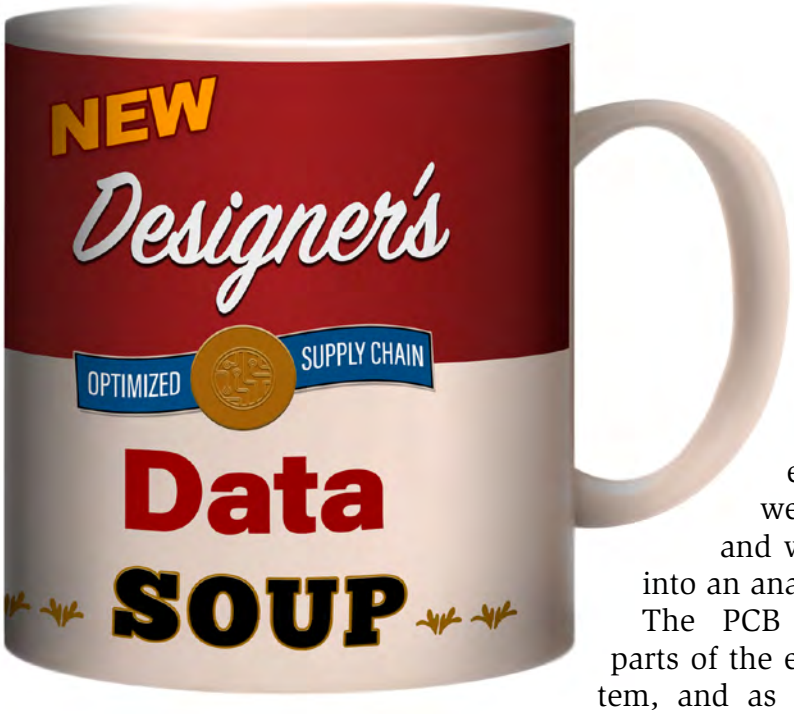
"Our results shed light on some of the long-standing puzzles surrounding this material, reveling unusual spin-phonon coupling," said Balandin.

The UC Riverside team also included Jing Shi, professor of physics, and Roger Lake, professor of electrical and computer engineering, in addition to members of their research groups, graduate students, and postdoctoral researchers.

The investigation of the spin-phonon interaction will have important implications for development of spintronic devices. By avoiding electrical currents, spintronic devices have a potential for ultra-fast and low-energy-dissipation operation. Interaction with phonons is one of the energy dissipation mechanisms in spintronics. The data reported by the UCR researchers may help in optimizing the design of spintronic devices by altering phonon properties and the way phonons interact with electron spins.



What's New in EDA:
The Experts Discussion



Feature Article by Andy Shaughnessy
I-CONNECT007

To ring in the new year with this month's issue, we wanted to find out what's new in the world of EDA software. Joining us on our experts conference call were Polar Instruments Managing Director Martyn Gaudion, DownStream Technologies founder Rick Almeida, and Director of Product Management Mark Hepburn and Product Management Group Director of Allegro Enterprise Products Hemant Shah, both with Cadence Design Systems. In a lively conversation, the group discussed the challenges and opportunities they see in our industry, as well as the need to bring new blood into the PCB design community.

Andy Shaughnessy: Thank you all for joining us during this short holiday work month. Basically, tell us what's new with your companies for the next year or so. Do you want to start with Cadence, Mark?

Mark Hepburn: Sure. One of the things that we're working on is driving the need for moving the industry from more of an authoring-centric world, especially how we capture designs and work with them, into an analytic space.

The PCB touches many parts of the extended ecosystem, and as an industry we need to get a lot of information to the engineers, at their fingertips. We can't stop there, and the converse of that is that we need to get information about the design and design process back out to the enterprise. What we're doing is bringing in capabilities that enterprise has dealt with for a long time, technologies like data marts, business intelligence, analytics and predictive analytics, making that accessible to our customer base.

The way that formalizes is around our new product, Allegro Pulse. Essentially, it's a data mart that collects information about all the design data that's managed in an environment; whether it be the work-in-process design data management, or information about the library, we characterize all that information into a datamart behind the scenes in near-real time, and then present it back out in many different actionable forms such as dashboards, KPIs, reports and notifications.

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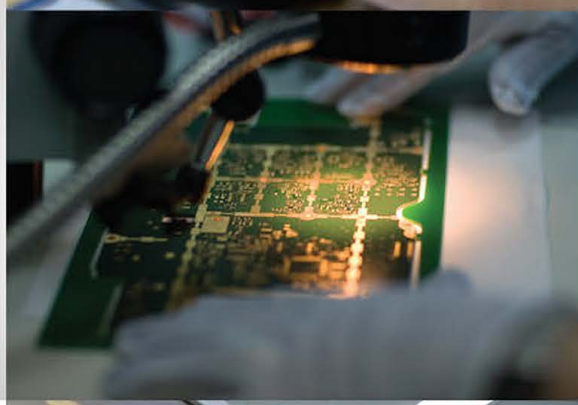

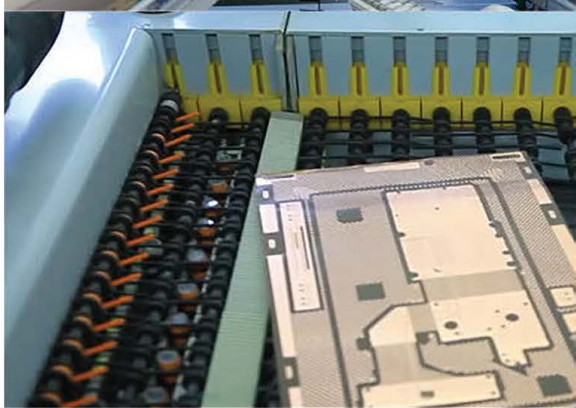

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For example, we can provide different dashboards for management to look at, to see how a project is progressing. We can look at the library content and help people optimize what's in their library, what parts are obsolete, what parts are being requested by engineers—information critical to other domains such as supply chain. Then we bring that all together, and present that back out to the enterprise, and that's important, when you're trying to link in supply chain and manufacturing in real time with a need to get your design out quickly.

Mark Hepburn, Cadence Design Systems

So that's the front end, Pulse. The other component of this is, how do we manage that data? For us to capture that data, we must bring in a holistic way of managing the work-in-process data, so we're actually driving into the work in process and native design data management within our applications to capture that data. We can do this transparently and in near real time, because we have the work in process BOM, design and library data.

What we are doing differently is pushing data management under the surface. Historically, it's been hard for our industry to adopt design data management, because it changes the design methodology too much, and engineers have enough on their plate, let alone doing some logistics around "How do I check in and version a file?" So, we're pushing that below the surface, and making that transparent for the engineer, so it's as simple as a "save." It's at that point we use our knowledge of the tools and data extract and characterize the information. This is what allows us to get all that great metrics data that we can use to promote back out to the enterprise for collaboration.

Shaughnessy: Martyn, what's new at Polar?

Martyn Gaudion: Thanks for having me, Andy. It's very appropriate that the guys from Cadence are here. A lot of the focus on our tools outside of fabrication is in pre-layout. A lot of people use our tools prior to layout to set the stack-ups they're going to use, and once they've worked on a series of different technologies and stack-ups for different types of technology, they need to feed that information into the CAD system.

Now we've been working with Cadence, and we're doing a new project now to smooth the path of our data into the layout of those other systems. We find that people work on stack-up long before they've committed pen to paper, and certainly the linking to other systems is an area we particularly want to focus on. Following the meeting we had at PCB West with Cadence, we're looking at doing that in even more detail.

So that's a key area we're working on, smoothing the pre-layout path into layout. The other area we're working on is, we've been doing a lot of focus on copper roughness modeling for insertion loss, and we've been improving the tools to do this. The more recent techniques we've put in have been somewhat academic, especially Huray, and a lot of feedback from our customers was that this method required input from scanning electron microscopes and some quite complex data to feed in which isn't easily accessible. We've worked very closely with Bert Simonovich, who I think you know well, and Bert has helped us provide a method "cannonball stack" to take the RZ roughness data from the copper foil, and feed that in and reduce numbers which we can feed into Huray methods making a much more realistic approach for the average PCB specialist.

From the first quarter of next year, we're incorporating cannonball stack both into Speedstack and Si9000 the ability to put RZ, and use that for insertion loss modeling. So, for people who want to get a first pass on insertion loss, that should make life a lot easier, and require a much less expensive kit. But we're also, also educating people that you need to make sure that the foil surface you're modeling is the real surface that gets used, so it's important for designers to understand where the drill

ends are, which are the plated-up layers, where you can use the roughness data from the core supplier and where you need to talk to the fabricator about roughness data. So yes, talking to other CAD systems, and making life easier in terms of modeling copper roughness are two primaries of focus now, and that's the areas we'll be pushing into the first quarter of 2018.

Shaughnessy: Thanks, Martyn. Rick, do you want to chime in about DownStream?

Rick Almeida: So, for us, we're working on a big release right now, bringing our CAM products and our documentation product more in line with one another, for post-processing. But there are two areas we're working on now. One is with the IPC-2581 Consortium, to build a stack-up visualizer that allows us to do a couple of things. One is to visualize stack-up data that we use in CAM350 to model the PCB, and in BluePrint for layer stack-up details in the documentation, as well as sharing information between the designer and the fabricator using an incremental 2581 format to go back and forth.

There's one other area that we're working on. For a while now, the EDA companies, Cadence, Mentor, Altium, and Zuken and so forth, have been introducing a lot of 3D design capability into the front end of the process—the front end for us. What we're looking to do is bring that 3D information into the back end of the process. We've got some unique challenges to do that, particularly being unable to extract 3D data intelligently from the CAD systems, but the area we'd be working on is visualization of the bare board in 3D, doing some facsimile of component rendering because we don't feel that users will want it to redesign models at the back end.

We're doing more of a 3D rendering STEP model import for the purpose of viewing the PCB in 3D, viewing the PCB panel in 3D, to understand where you might have conflicts between components and mill cutouts and so forth, especially on assembly panels, and then 3D documentation to augment 2D documentation that engineers are producing now. Those are the two areas that we are pretty much focused on for the next nine months, until we get this release out the door.

Shah: So, along the lines of what Rick is talking about, as you know, we partner with DownStream. We actually OEM their technology and sell it as Allegro Manufacturing Option. Three years ago, we started collaborating, building the products together, and what customers were asking for was to have approval sign-off technology like DownStream has, and we created the Allegro Manufacturing Option product that works very closely with Allegro PCB Editor. Customers wanted a way to check their designs before going to manufacturing, that it's fabricatable, number one. Number two, what they wanted was an easy way to create documentation to hand off to manufacturers, and this is where the blueprint technology comes into play, and it's one of its kind in the industry.

Now what we hear from customers is that this is good and many of our customers have adopted the Manufacturing Option, but they asked us to do these manufacturing checks during the design process. So as the design is being created, they wanted us to do DFM checks, so that they don't go through the design, do all the work, and have to redo some of the work because of the problems found at the tail end of the process. So we built the industry's first and unique CAM-ready, built-in DFM rules that are checked in real time without any performance issues.

So we built the industry's first and unique CAM-ready, built-in DFM rules that are checked in real time without any performance issues.

As you're placing a component, you can find out if it is too close to the board edge, which is

a very common occurrence with PCB designers, and they need to know if they're too close to the board edge, or even a slot. , If you don't detect it early enough, you'll place other circuitry around it, and then when you find the problem later in the cycle, then you have to move a lot more of your circuitry to fix that one problem. There are more than 2,000 rules in Allegro PCB Editor, to enable this DFM technology. The announcement for this was done around PCB West, but we continue to enhance it, and our focus will stay on this technology, expanding this technology in other areas for manufacturing.

Shaughnessy: OK. Now I'd like to open it up to everybody. What do you see as the biggest challenges? For your own company or for the industry? What do you guys worry about?

Almeida: I'll jump back on the 3D. The biggest challenge we see is that you've got a lot of 3D definition going on in the design world, but there's really no vehicle to get that data out of the design world into downstream processes, no pun intended. Typically, you can export in ODB++ or IPC-2581, and you get all the design intelligence, but any of the 3D definition as far as model assignment and component rendering is still contained within the CAD system. You use Gerber, you get no intelligence and no component information.

Rick Almeida, DownStream Technologies

The only other real option would be to use a STEP file import, which we're looking at and have actually started implementing, but STEP has its own shortcomings. You get a better rendering of the PCB assembly with more realistic components, but you lose a lot of intelligence that's tied into the board, like for layers and nets and so forth, and being able to interrogate the various individual pieces. And for me, as an industry we're continuing to see the design community embrace 3D for design.

I think that's just a natural evolution. I think that's going to be a key area, and how do you take that 3D and bring it further into DownStream? Not just into fabrication, but all the way into production and rework and so forth, where 3D can have a big impact, and right now there's really no vehicle between the design side of the chain and the manufacturing side of the chain.

Shah: On the design side, the challenge is with availability of STEP models that are accurate and realistic, and so customers struggle with trying to get 3D models. Now there are tools out there that allow you to create these 3D models, so we introduced Allegro ECAD-MCAD Library Creator. It enables quick creation of 3D models as you create a 2D footprint. You can also create a 2D footprint from the 3D model, so now they are synchronized. The challenge of synchronizing these libraries between ECAD and MCAD is addressed through ECAD-MCAD Library Creator.

Now, Rick's right that now you've got to have intelligence in these models, as well as the assembly, so you can't just go into the STEP world and lose all the intelligence. That's one challenge we have, and we believe that's a challenge industry should tackle in short order. And then the last piece, of course, passing the data to manufacturing, you have all the 3D data in the design. How do you pass it to manufacturing in an intelligent manner? That's the challenge.

Shaughnessy: Interesting. Martyn, what keeps you awake at night?

Gaudion: Well, it doesn't keep me awake, but we see our customers now being faced with such a huge range of options and material choices. Whereas a designer may have previously had the opportunity to select a generic FR-4 or a high-speed material, now all the material suppliers have a huge range of materials for heat

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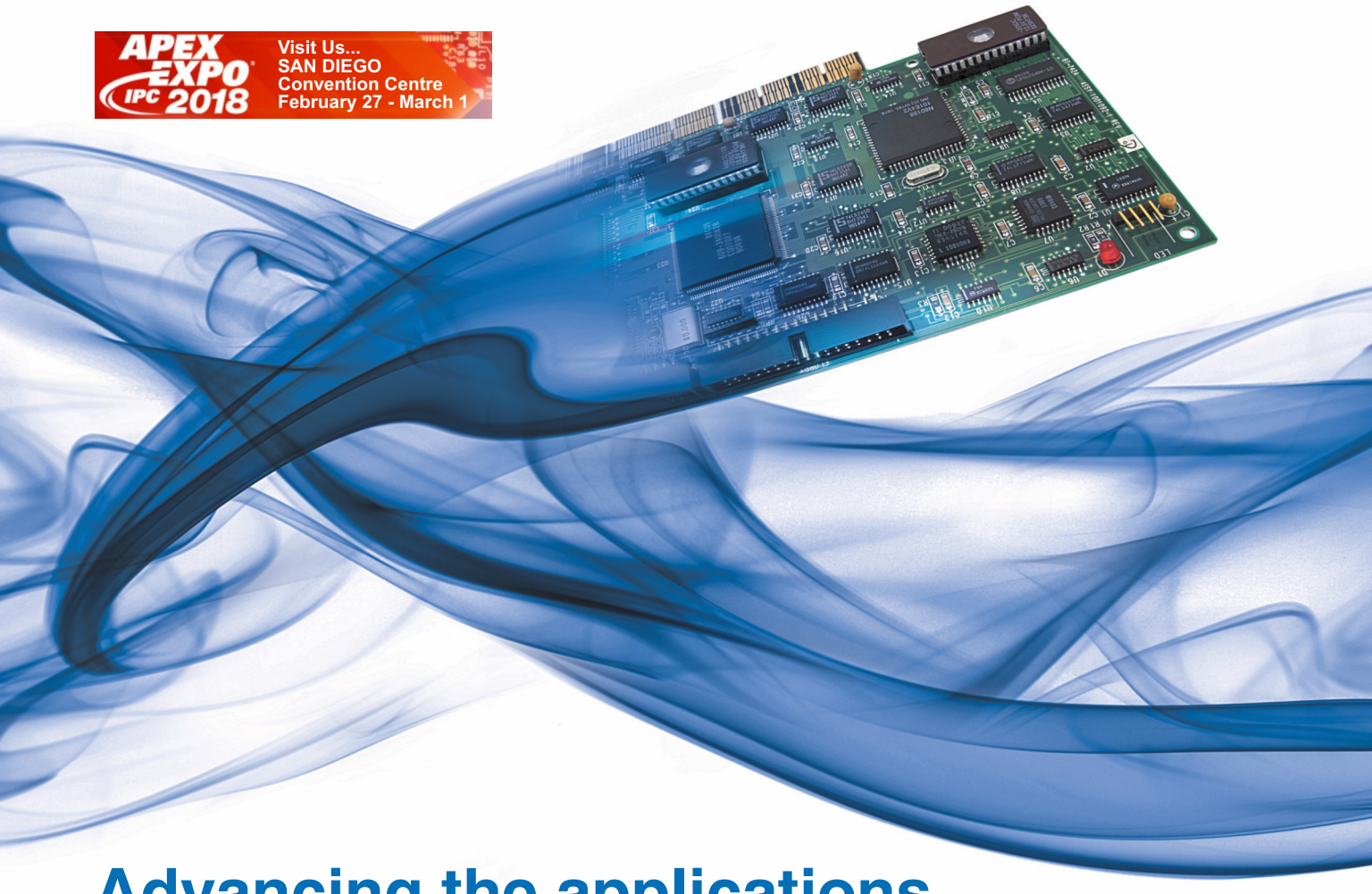

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dissipation, reliability, high speed, and some are focused on automotive, aerospace, consumer, and there's a huge, huge range in material choice.

Trying to help our customers navigate through that choice of materials, we try to work very closely with all the material suppliers who are material partners with us. This ensures that designers and pre-layout people, PCB technologists, have a good informative background in terms of how they're going to choose the right material for their design. And once they lock the material in, that's done at an early stage, so it's critical to get that right the first time. We work with that community to make sure that customers are well-informed about what's important for their design and what's maybe less important.

Shaughnessy: This is a question for everybody. How much of what you do focuses on education, and educating your customers?

Hepburn: I think we have a unique challenge here with moving an industry expert in traditional authoring tools into more enterprise-grade analytics and intelligence applications; there's some education that has to occur there.

One of the things that we're doing is trying to focus on the result of the data. For an engineer, it's not a very exciting problem to manage data, right?

One of the things that we're doing is trying to focus on the result of the data. For an engineer, it's not a very exciting problem to manage data, right? But the insights, productivity are very interesting to the company and the engineer. However, the education process for data management can't be done without huge methodology changes and articulating the benefit you get by having access to all this data from you, your colleagues, and across your organization. So that's the challenge that we're working through. It's the messaging of how do you link the value of what this data can do for the engineer, and link that back to what does it do for the enterprise and the company at the same time? It's a learning experience; however, we are finding enterprise customers have bought into the business value, so we are making some good progress.

Gaudion: Just to focus on the education front, I was just looking at our website. It's been 21 years since we launched the Polar website, and now there are over 900 pages for the industry to dip into. We've been updating it, and it's about the third time we've had a major refurbishment on our site. We started the site about two years before Google even came into existence.

Shaughnessy: You all have a pretty good idea who's using your tools. Are you seeing more young people coming in as designers and EEs?

Shah: Well, obviously in India and China, you see many more younger designers than you see in North America and Europe, and the industry is struggling with trying to get the younger people into the industry here. And it's a problem; the industry needs to create some program that allows and influences younger people to get into the trade, and smaller mom-and-pop shops obviously cannot afford to invest in it, although they need to because they have a graying population as well. They have a real chicken-and-egg problem. Larger companies, though, will tend to go to younger populations and solve that problem first. But Europe and North America are lagging and that's a problem.

Almeida: I almost disagree with you. I don't think you're seeing young designers come in. I think if you're seeing any young designers, they're coming in as EEs. Because I think that that the traditional, dyed-in-the-wool PCB

designer is going to be a thing of the past. Surveys show that about 50% of board designers plan on retiring in the next 10 years. And there's really nobody coming up behind them. When I was young, there were all kinds of programs for drafting and electromechanical design. Now, designers are being replaced with EEs who need to know everything about the circuit, the performance, the layout. And the problem they're going to have is really understanding things that are further downstream. How do you design for manufacturing? How do you know that what you design matches what your fabricator can build? There are still a lot of PCBs being designed, but you have a different skill set, and the skill set is geared more towards performance, not manufacturability.

Shaughnessy: Right. Susy Webb's PCB Basics class at PCB West was almost entirely made up of EEs. Most of the young designers I meet now are electrical or mechanical engineers.

Almeida: Well, simulation has always been important, but it's becoming a bigger factor tied to the board, and the analysis part, and a lot of times it just is outside of the skill set of your traditional printed circuit board designer, no matter how well they can route a tight dense board and eliminate cross talk that goes with that, they just don't understand the electrical issues that are associated with it, and you need that EE discipline to do that. The other big problem PCB has is this: When was the last big breakthrough we ever saw in PCB technologies? The last one I can think of is surface mount, and that was in the early '90s. That forced a lot of companies to retool their CAD systems, because the gridded systems didn't work anymore. The PCB problem has pretty much been solved a long time ago. You don't see any more disruptive technologies being introduced into the marketplace. Where's the next CCT? Where's the next P-CAD or PADS, or PSpice, for that matter?

Shah: There are a couple of things that are on the horizon, not quite there yet, but after surface mount we had HDI and embedded.

Almeida: Sure, but it didn't really take off as a mainstream technology, and it certainly has been there for a while. It's been slow to be embraced.

Shah: We see a lot more customers doing HDI and embedded. And HDI is really driven by the finer-pitch BGAs that customers are faced with. In fact, there's a trend going on where customers are forced to go to an interposer, because the BGA pin pitches that are coming out for the next generation of BGAs is even smaller than what they could do with HDI. But you know, the next set of things that are coming out there are still in a proof-of-concept stage. One is the VECS technology, which is the vertical connect system which allows you to have a via which is not round but flat. It's a 2D trace going from the top of the board to the bottom of the board. So that's a new technology that's in a proof-of-concept stage right now.

Hemant Shah, Cadence Design Systems

Hepburn: Something else, just a little different perspective on all this is, the disruption here, we're looking at it right now as where does it come from a pure technology or tools perspective? But especially with the younger generation that's coming in, they're looking for completely different ways of designing. For example, agile development methodologies which are now taking half of a development organization because of the software content, are driving into even the hardware design, and there's a bit of an impedance mismatch there. How do you make that work? And the younger generation, that's what they're looking for. They're looking for that highly-collaborative, very iterative-type design, and frankly a lot of our tool sets today are not organized for that.

When they look at that, they're like, "I'm kind of in this more regimented phase-gate process." For very good reasons, but nonetheless, the disruption we see could come from more how we design, and a process around designing, as opposed to purely the tools and the technology.

Shaughnessy: Shifting gears, how much does flex drive what you all are doing?

Gaudion: What we've seen with flex is that where people used to use it just for interconnects at low speeds, they seem to be going straight to high-speed designs with flex, and that means that people are going in with quite complex designs straight-away. Whereas with the more traditional builds, people gradually ramp up the speed, now people want to go fast from the get-go, and that's you know, dealing with the different dimensions and the material properties of flex brings in some extra things into the equation there. Certainly, we see flex being a significant percentage on all our tools and that's interesting for us to keeping developing in that area.

Martyn Gaudion, Polar Instruments

Shah: We see a lot of our customers pushing the boundaries on flex and especially rigid-flex. They're really pushing the boundary, not only in terms of the number of layers in flex with multilayers, but they're also looking at, "How do I figure out if the bending of my flex is going to work, not only in the mechanical stage, but electrically?" Imagine a rigid-flex rigid, and the second rigid board is flexed and bent over the first one. You want to make sure the crosstalk doesn't prevent the circuitry from functioning in the field. So that's another capability. Bringing the multiple domains—manufacturing, mechanical, and electrical—all together is an important concern that our customers have that PCB design tools need to address.

Gaudion: I think one area we also find on flex is, we often get asked to model and measure flex, but then when we ask our customers for samples, they say, "We can't, it's confidential, our clients won't let us share that information." Then we get kind of stuck in a loop where people would like us to help them, but they won't give us the samples to test out the tools, and that's something I've heard is common with other EDA vendors. It's become this world of where information is tightly legally controlled and manufacturers aren't always allowed to disclose things to their suppliers, compared to when we first started working on impedance controlled boards, where you had coupons and test pieces freely available and people would share the information. The supply chain seems a bit more cautious about supplying test vehicles out to people like us and to our competitors.

What they would be sharing is nothing that's particularly confidential, but without the ability for us to get hold of test vehicles, it's very hard for us to design something, because we'd have to guess what the client's doing. So, they'll say, "I've got this particular structure I'd like you to model," and we say, "Can you send us some samples?" And they say, "I'm sorry, but legal won't let us do that." I certainly would appreciate some more openness in the supply chain, where it's not mission-critical; it's everyone trying to help each other.

Shaughnessy: It seems like the industry is getting a little bit less paranoid about sharing. But traditionally, PCB people have been leery of sharing anything, even if it might be for the greater good.

Shah: Well, that big paranoia is with the 2581 spec, and even ODB, sharing that with fabricators. "Am I actually giving away intellectual property here, now that 2581 is really an intelligent database of the CAD system?" And then,

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"Well, we want to use Gerber because it's unintelligent." Gerber wasn't made as a security method protocol for passing information. It was just what was around at the time in the late '80s to get something from the computer out into a physical board. But there is a paranoia about data being stolen, because it's a reality now that we're using more Asian resources. They have a piracy problem there, and not just with designs, but even, I'm sure every one of the people here today have had their software ripped off in Asia somewhere, us included. It's probably well-warranted, but it gets to the point where it starts to overshadow developmental stuff. And Martyn's right, we've had the same issue with customers. You've got to kind of guess what the problem is based on a description, because they're not going to show you what it really is, and it puts you at a loss with just trial and error basically. Am I solving the right thing for this guy?

Am I solving the right thing for this guy?

Shaughnessy: But do you all support ODB++ and IPC-2581? I know Cadence and DownStream do. Martyn, what do you think about IPC-2581 and ODB?

Gaudion: We support 2581, but because most of our clients are pre-layout, then they're using our tools before there's too much data available. The data we can put in 2581 is thin by nature, but we can. We have both links directly into the tools and via 2581, so there's two different routes in. But there's not, from our perspective, that much of it available to feed in, other than the stack-up information into 2581.

Shah: Andy, one of the things that you cannot use earlier in the process is ODB++ for exchanging the stack-up data that Martyn talked about. Only 2581 allows you to do that. And I know that the adoption of 2581 is really gaining momentum. At the consortium update session at PCB West, Axiom Electronics talked about how they have standardized on 2581 and if anybody gives them Gerbers, they have to pay more, because it's an inefficient data format. Aegis supports 2581, so a lot of fabrication companies out there and manufacturing companies out there support it.

Shaughnessy: How about printed electronics? Is printed electronics making a dent in your customers' jobs? Are you all seeing any of that?

Shah: We do get regular inquiries from customers whether we support that or not. We support some outputs that support the printers. But you know, there's no industry standard, so there are multiple different languages that are consumed by the 3D printers. But it's an emerging industry right now, and people are prototyping with smaller boards, simpler technologies and so on. Many companies are using 3D printers for developing prototypes.

Shaughnessy: But you're not going to print 100,000 of them.

Shah: Yeah, exactly. They aren't manufacturing in high volume at this point.

Shaughnessy: It's a very cheap way to do certain prototypes.

Almeida: Right. That was the same experience almost everybody had when everyone was talking about "system on a chip." It was like, "Oh, well, you can put the whole thing on a chip, it's going to make PCBs obsolete." Well, you've got to walk that all the way through, what are you going to put the chip on? It's got to go somewhere! And what's interesting is we've seen for a while electronics shrinking down, and they've gotten to a point where they can only shrink so far without some level of voice recognition. You can only take a cell phone and make it so small because at some point, your fingers aren't going to work on the device. There's a human limitation that we have with miniaturization, and what you're

seeing is the other way, they start to go wider but they start to become more functional.

Gaudion: I guess a slightly different take on printed electronics is that, rather than a pure print approach where you're looking at printing everything, you can certainly see parts of the process being picked away, like looking at a resist being printed on, where you've got particular processes where an additive technology works well with the existing PCB manufacturing technology. Whereas the full prototyping, yeah, it's great for prototyping, but the lack of reinforcement's always going to be a bit of a barrier there unless there's a way of printing with reinforcement.

Shaughnessy: This has been good. Is there anything you all would like to add?

Shah: No, I think we're good for now.

Shaughnessy: OK, thank you gentlemen.

Gaudion: Thanks, Andy.

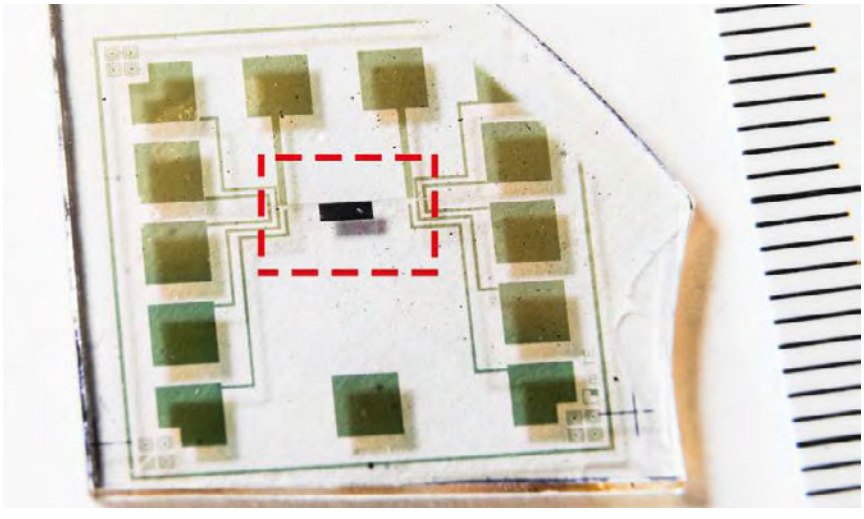
Rick: Good talking with all of you. **DESIGN007**

A Major Step Forward in Organic Electronics

Researchers at the Laboratory of Organic Electronics have developed the world's first complementary electrochemical logic circuits that can function stably for long periods in water. This is a highly significant breakthrough in the development of bioelectronics.

The first printable organic electrochemical transistors were presented by researchers at LiU as early as 2002, and research since then has progressed rapidly. Several organic electronic components, such as light-emitting diodes and electrochromic displays, are already commercially available.

The dominating material used until now has been PEDOT:PSS, which is a p-type material, in which the charge carriers are holes. In order to construct effective electron components, a complementary material, n-type, is required, in which the charge carriers are electrons.



In an article in Advanced Materials, Simone Fabiano, head of research in the Organic Nanoelectronics group at the Laboratory of Organic Electronics, presents, together with his colleagues, results from an n-type conducting material in which the ladder-type structure of the polymer backbone favours ambient stability and high current when doped. One example is BBL (polybenzimidazobenzophenanthroline), a material often used in solar cell research.

Postdoctoral researcher Hengda Sun has found a method to create thick films of the material. The thicker the film, the greater the conductivity.

"We have used spray-coating to produce films up to 200 nm thick. These can reach extremely high conductivities," says Simone Fabiano.

The method can also be successfully used together with printed electronics across large surfaces.

Hengda Sun has also shown that the circuits function for long periods, both in the presence of oxygen and water.

"This may appear at first glance to be a small advance in a specialised field, but what is great about it is that it has major consequences for many applications. We can now construct complementary logic circuits - inverters, sensors and other components - that function in moist surroundings," says Simone Fabiano.

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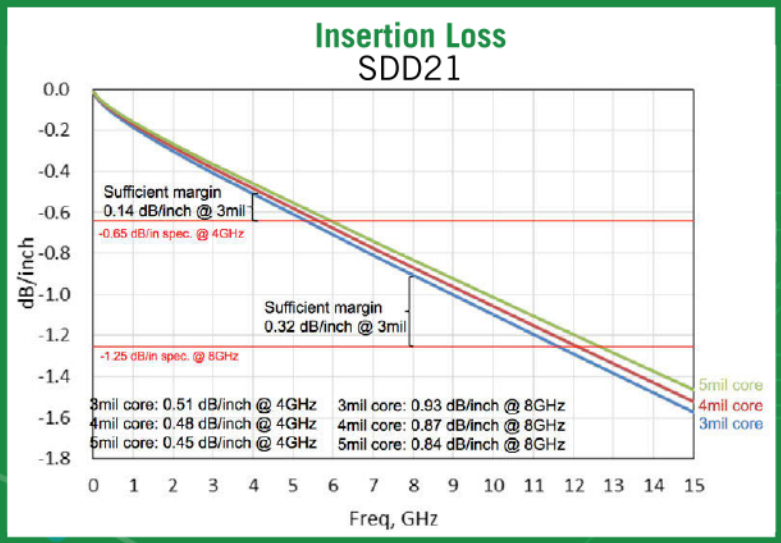

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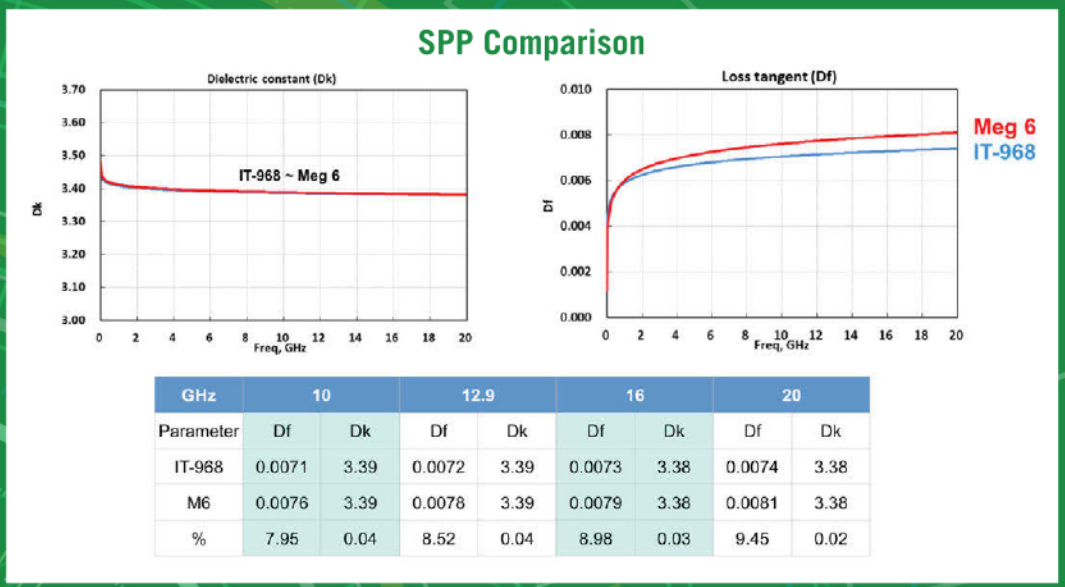

GHz	10		12.9		16		20	
Parameter	Df	Dk	Df	Dk	Df	Dk	Df	Dk
IT-968	0.0071	3.39	0.0072	3.39	0.0073	3.38	0.0074	3.38
M6	0.0076	3.39	0.0078	3.39	0.0079	3.38	0.0081	3.38
%	7.95	0.04	8.52	0.04	8.98	0.03	9.45	0.02

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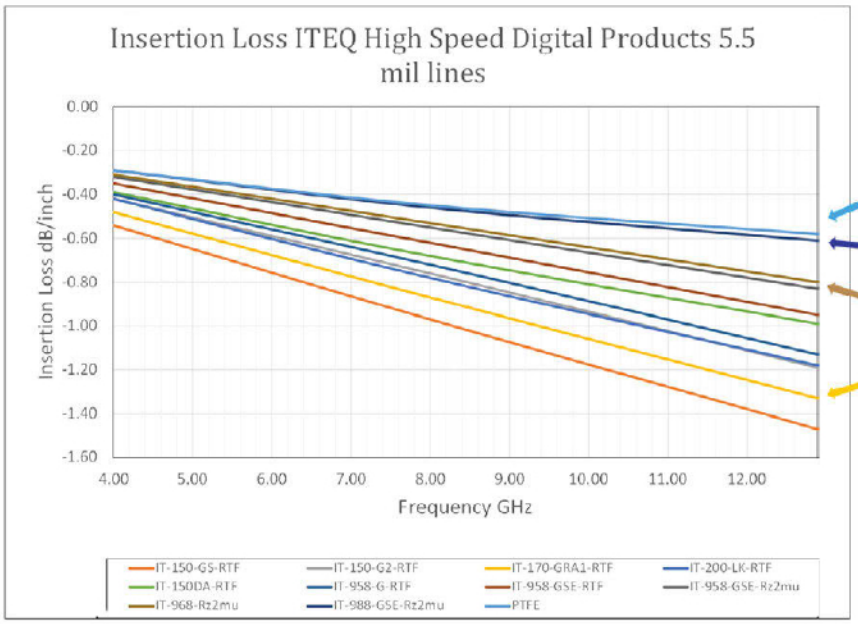

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IoT: Let's Put the "A" Back into EDA

Feature Article by Ben Jordan
ALTIUM

If I say IoT, most people today will immediately conjure up some notion in their mind. This is especially true in the engineering community, where many of us are hanging the future of our careers on the Utopian vision of a clean, beautiful environment with hidden networks and sensors everywhere. A future where our communication devices, personal gadgets, homes, kitchens, transportation and more will be smarter (whatever that means), and we will be watched over by electronic guardian angels. Maybe it will not be so nice, or maybe it will be greater than we can currently imagine, but whatever your viewpoint is, two things are abundantly clear: There are going to be lots of PCBs made, and IoT will require EDA tools with even greater levels of automation. It's time to put the "A" back in EDA.

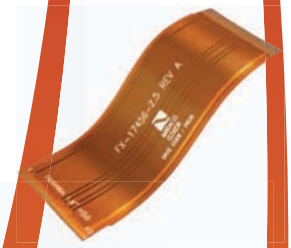
IoT: More Boards and Fewer Designers

Predictions earlier in this decade made by Hans Vestberg (Ericsson)[1], Jon Iwata (IBM)[2], and Dave Evans (Cisco)[3], were all bullish, typically estimating that more than 50 billion connected devices would be in use by 2020. Since then, real numbers have been crunched and these estimates have become more realistic[4]. But even the most conservative predictions today of what the Internet of Things becomes within the next few years are quite staggering. It's clear that there will be more than 20 billion connected devices (there may already be, if we include personal communications) by 2020.

Please indulge me while I ruminate on this a bit, with what I believe to be fair and reasonable assumptions about designs, based on my empirical observations. Twenty billion devices obviously do not mean 20 billion unique designs, but let's say for argument's sake that these devices will equate to 200,000 new designs by 2020. In other words, I'm assuming there will be, on average, 100,000 instances of each type of connected device. Well, that may seem ridiculous, but as we know, some devices will sell only 1,000 units and others will sell in the tens of millions.

If there are 200,000 unique designs and each one takes on average five design spins to get

Engineering And Providing Balanced Interconnect Solutions



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to the final production revision (and I'm being optimistic here; some will take more, others less), then we are facing a million designs. Who will design those boards? There are lots of PCB designs to be done, and yet in North America, we see an aging of the PCB designer community and slowly declining numbers of those in the dedicated job. At this point, there appears to be not enough new dedicated designers entering the job market to meet the need.

At the same time, we can observe more and more electronics and electrical engineers bridging the roles of circuit and PCB design, rather than having dedicated engineering and PCB design roles working separately. Evidence of this has been everywhere for more than a decade. Today, you could look at nearly any crowd-funding campaign for an electronic device, and the same inventor or engineer who came up with the idea did the electrical engineering, PCB layout and firmware development. We're increasingly wearing all the hats; it's not intentional, but the natural outcome for startups to save money and time, enabled by tools.

What do IoT PCB designs look like?

What kind of boards go into IoT devices anyway? I look at the current generation of connected devices for example, and it's a mixed bag. The smart thermostat in my home has two PCBs inside: one is a double-sided relay, power and connector block for wiring into the air conditioning system, and the other is the board with all the "smarts" on it. Without destructively taking a microsection, I can tell that board is at least four layers of copper, probably six, since it has a decent sized SoC chip and some DDR memory on it.

I've also done destructive analysis of smart health monitoring wearables from well-known manufacturers. In those designs, I typically see a single board that's rigid-flex, likely with a minimum of six layers in the rigid parts, with mixed signal sections on the flex for RF connectivity (Bluetooth, Wi-Fi). In one case, there were two separate PCBs with a flex circuit connector (FPC) linking them.

Figure 1: Fitness tracker (Source: Altium LLC, PCB2020 Roadmap Presentation 2017).

Surveys show that the most frequently designed boards still have between two and six layers, but there has been a marked increase (>10%) over the past five years of boards in the seven-to-10 layers category. This is reflective of the kinds of components needed for IoT and smart, connected products. User interfaces with capacitive touch and high-resolution displays require multimedia processing, upping the pin counts and memory amounts and speeds used. Naturally having to add powerful SoC chips and DDR3/4 memory along with high-speed wireless makes the boards more complex as time marches on.

There are a lot of sensor and power and connectivity boards, and a lot of main boards with complex compute power, to design. For reliable production, cost savings, reuse and supply chain flexibility, a lot of these products will naturally need to be divided into multiboard systems. And the amount of time available to a comparatively diminished workforce for designing these boards right keeps getting shorter.

IoT Design Bottlenecks

It's hard to design boards right the first time in every respect. Thanks to great teachers in our industry, along with IPC designer certification and training, we are constantly improving

our game and getting better at the core skills of PCB design for manufacturing, test and assembly. And despite the increasing difficulty with cluttered channel space in the wireless spectrum, we're pretty good at designing for electromagnetic compatibility and signal integrity as well. Yet, board designers still must fight to reduce design time and re-spins due to other pesky problems. The real bottlenecks in the process of getting an electronic product to market are exacerbated by the nature of IoT devices: mechanical form and fit, extended production runs and parts availability, as well as increasing complexity and density.

On the product form and fit side, there's the obvious issue that the PCB assembly must fit within the designed structure of the overall product. And for a long time, EDA vendors have been aware of the need for proper collaboration between the PCB designer and the MCAD flow. Most designers even to this day are relying on transfer of mechanical CAD data between the ECAD and MCAD tools for synchronizing the physical aspects from mechanical CAD to PCB design and back. While these formats such as IDF/IDX and STEP have gone a long way to improving the fortunes of product designers, they are still intermediary formats and suffer loss of fidelity.

With regards to production run extension and parts availability, there can be serious show-stoppers. Most IoT devices that are accepted by their markets will experience demand surges. This is a delight to manufacturers and designers, yet poses significant supply chain problems that often lead to design re-spins. Most seasoned designers have experienced this, having had to modify a product simply because one obscure component is not available in time for the second production batch. No serious business can tolerate the opportunity cost of waiting for that part to become available again.

Then there's the age-old issue of "smaller, faster, better" marketing requirements putting pressure on designers to squeeze more into less space, without neglecting signal integrity and compliance with FCC, CE, C-Tick, UL, and other EMC and safety regulations.

What can we do to increase design throughput, allow busier people to design more boards and get them right first time more often to meet the looming demands? The short answer is to provide and improve user-guided automation.

Multi-Board Design & Collaboration

Given that at least half the IoT products have or will have multiple PCBs within the assembly, designers need multi-board design automation in their tools. This automation enables rapid design without unnecessary re-spins by allowing the PCB designer in a native PCB environment to combine multiple PCB assemblies into a multi-board assembly. In the multi-board assembly, the PCB substrates can be aligned correctly using planes, edges and axes. Mounting holes and critical components such as board-to-board connectors can be moved into alignment with each other and with mechanical features of the overall enclosure assembly, as shown in Figure 2. This physical virtual prototyping allows for finding show-stopping problems. For example, Figure 2 also shows the main power connector in the design interfering with the rear shell of the plastic enclosure of this touch-sensor based light dimmer. We can also see board interferences with the front side

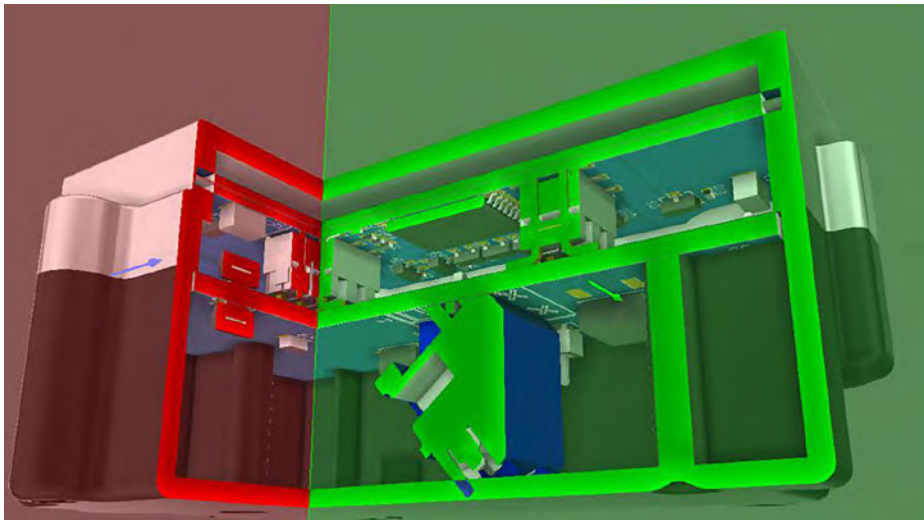

Figure 2: Multi-board clearance visualization (Source: Altium LLC, 2017).

of the enclosure on the face panel PCB, with the board edge penetrating the plastic shell.

The critical aspect of connection management and board-to-board signals is also automated for the user in proper multi-board system design tools. A Connection Manager coupled with a unified engineering change order process allows omni-directional synchronization of connector pinouts from one board to another, and the user can easily highlight signal paths throughout the assembly to guarantee no mistakes are made on signal assignments.

It's easy to overlook the collaborative aspect of this. Many new products being developed for smart home, automotive and other IoT applications rely on reusing known-good modules. Startups with a great idea often cannot spend time re-designing their boards for the compute section of the product. Instead, during the bootstrap phase, they often opt for combining low-cost open source COTS modules with their own interfaces and software to reduce spin-up time. Having proper multi-board capabilities allows them to bring in those externally developed modules quickly without running into connectivity or mechanical interference errors.

Real-time collaboration with MCAD is also key for product development teams who are centered on the aesthetics and outward design. Having ECO automation between ECAD and MCAD is necessary to achieve maximum productivity in that environment.

Supply Chain Automation

A successful product launch can have a certain sting in the tail: demand surge. Demand surge is when, after initial trial of a new product, the market acceptance of the new product spreads rapidly and demand increases sharply. Sometimes this can also happen due to unforeseen events: for example, earthquakes taking down a competitor's factory. In any case, any reasonable business needs to be able to respond rapidly or risk losing their market share. The problem is, how can you be sure your supply chain, particularly for the components in your design, has everything you need to ramp up additional production runs?

Additionally, it's all too easy for inexperienced designers to utilize components which electronically would be suitable for their product, but which have unstable supply. This often is manifested painfully through the ability to get the parts easily in small quantities, which gives engineers a false sense of security about the part's availability, during successful prototyping phases of the design process. Once the design progresses past prototype and test to scale up and then to production, you discover the hard way that those new-fangled engineering samples you were sold during the design of the board are still not in full scale production and you have to wait!

What is needed is bill of materials (BOM) automation, that allows designers to check the list of components used in the design against live supply chain data, and allows alternative suppliers and drop-in replacements to be found quickly before generating outputs and wasting time on outdated production data. Figure 3 shows this in principle: The list of BOM checks

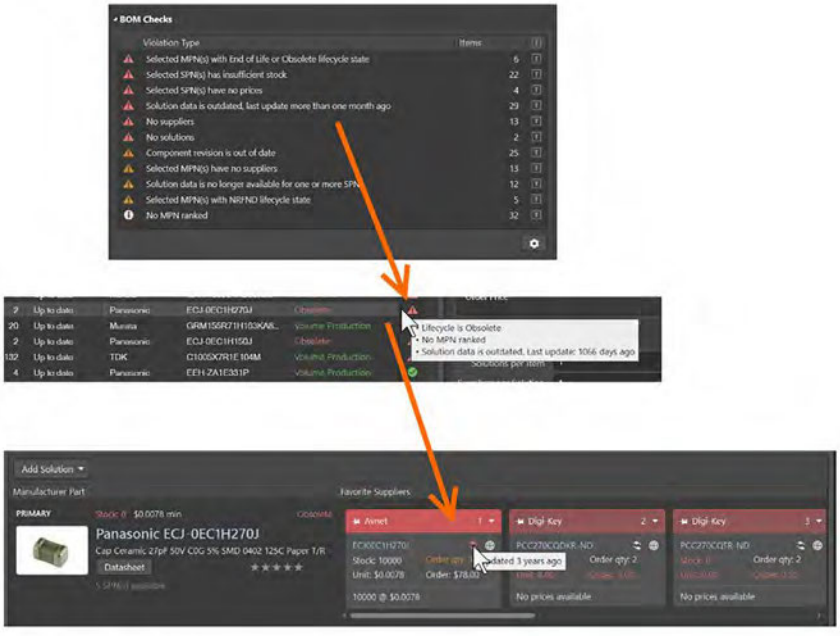

Figure 3: BOM scrubbing and rules checking (Source: Altium LLC 2017).

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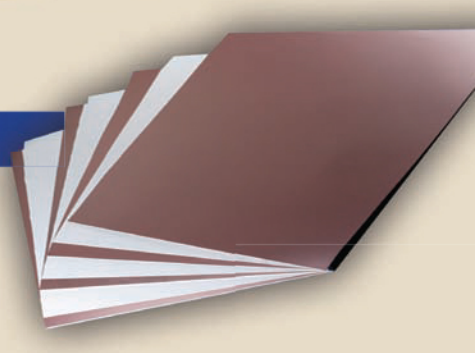

Heat can be damaging, especially when it is not managed. That's why Rogers Corporation invested so much time and energy into creating an array of material-based thermal management solutions to keep heat rise to a minimum in printed circuits. From automotive circuits to LED modules to power supplies, ML Series laminates and prepregs effectively conduct heat away from the source, while COOLSPAN thermally & electrically conductive adhesive (TECA) materials enhance the thermal management of new and existing designs. And for that extra cooling edge, 92ML StaCool laminates feature a thermally conductive metal bottom plate to enhance the heat dissipation.

Product	Thickness	Thermal Conductivity (Z-Axis), W/mK	Thermal Impedance, C-cm2/W	Tg, C	CTE (Z-Axis), ppm/C		Dk, 1MHz	Df, 1MHz	Breakdown Voltage, kVAC	Flammability
					<Tg	>Tg				
92ML	8mils	2.0	0.52	160	22	175	5.2	0.013	>50	HF V-0

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is applied real-time to the BOM document in the design project, and warnings and errors are shown automatically for each line item. In the example shown here, the selected component is obsolete, has outdated supplier links and no user preference rank for any given supplier. This lets the user know they need to find a drop-in alternative to this 56pF 0402 capacitor, which would not require a physical change to the PCB itself.

Of course, sometimes the component that is no longer available is more complex, like a microcontroller, and it would trigger a new revision of the PCB to replace with an alternative that's not a drop-in replacement. However, the BOM rule checking and live supply chain links make this scenario far less likely.

Deep Learning (Applied Artificial Intelligence)

PCB designers and engineers who I talk to (including myself) will always say the same thing: "An autorouter makes a mess and cannot do what I can do. I will never use an autorouter!" And fair enough, too! For all but the simplest designs that have no impedance control, no sensitive analogue circuits and no high-speed topology requirements, our experience of routing automation in times past has been less than stellar to put it mildly.

From my own point of view, what's around the corner with AI and deep learning is the crux of this matter. With all those complex boards to design, we need automation to help with component placement and routing of the PCB. We need it whether we want it or not. But it must work.

I mention AI and deep learning because we are finally at a point in time where we have technology that can rapidly accelerate the learning of routing and placement algorithms. Yes, it's been tried several times before. Neural nets, for example, have been used extensively in the development of 1990s era autorouting tools, such as Neuroroute. Just a layman's recap here: A neural net is a connectivity or relationship graph that is "trained" by first feeding in examples of what it should do with human generated results. The idea is that the neural net "learns" the human way of routing PCBs and creates a set of parameters that cause it to mimic how a human would do the routing.

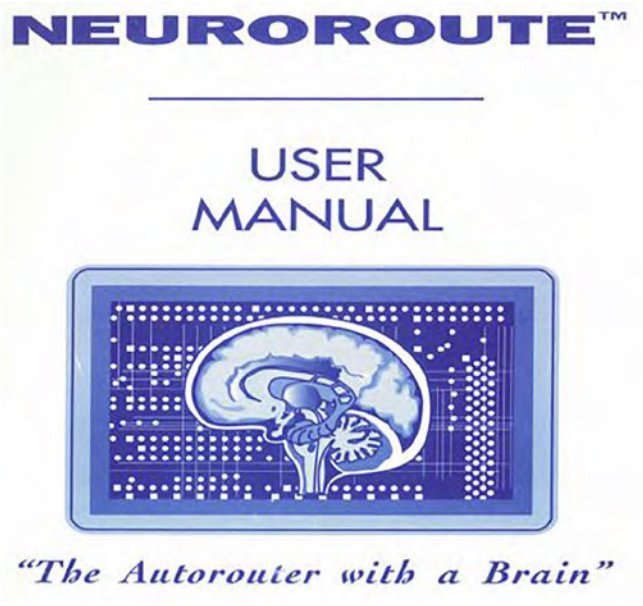

Figure 4: Neuroroute user manual front page (Source: Altium LLC 2017).

Neuroroute (Figure 4) was arguably the first ever neural-net based topological autorouter ever developed. It was acquired by Protel (now Altium) in the late 1990s and formed the base engine of what became the Situs autorouter that is in all Altium PCB tools to this day. I say it had great promise, but for early-'90s PCB designs (two-to-four layers, 15 mil track-space ratio, 1 mm pitch QFP and 0805 chip components), it actually did a pretty decent job. The problem is that it was not able to adapt to the much finer package pitches and BGAs that hit PCB designers in the early 2000s, and the basic set of PCBs used to "train" it was very limited.

The principle was sound, but lack of ongoing training data set availability makes it hard to update. Since then, many largely improved routing tools have been developed. The topological router can be compared with traditional shape-based routers (Figure 5) such as SPECCTRA by mapping the board space and obstacles using polygons, and applying different path costs (for example, adding vias versus going the long way around the board), to

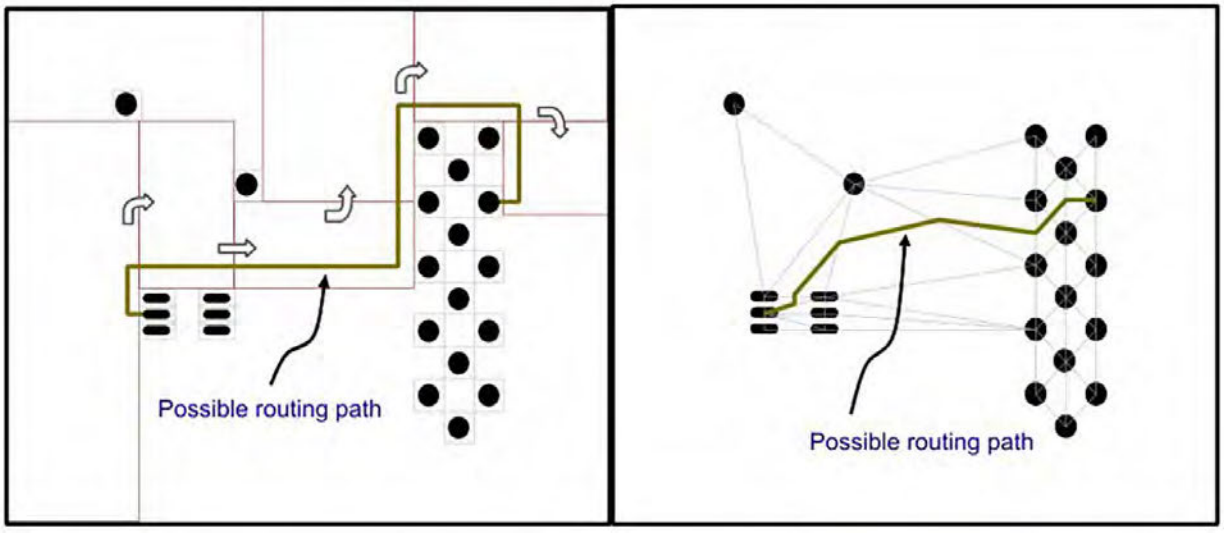

Figure 5: Rectilinear vs. topological routing (Source: Altium LLC 2017).

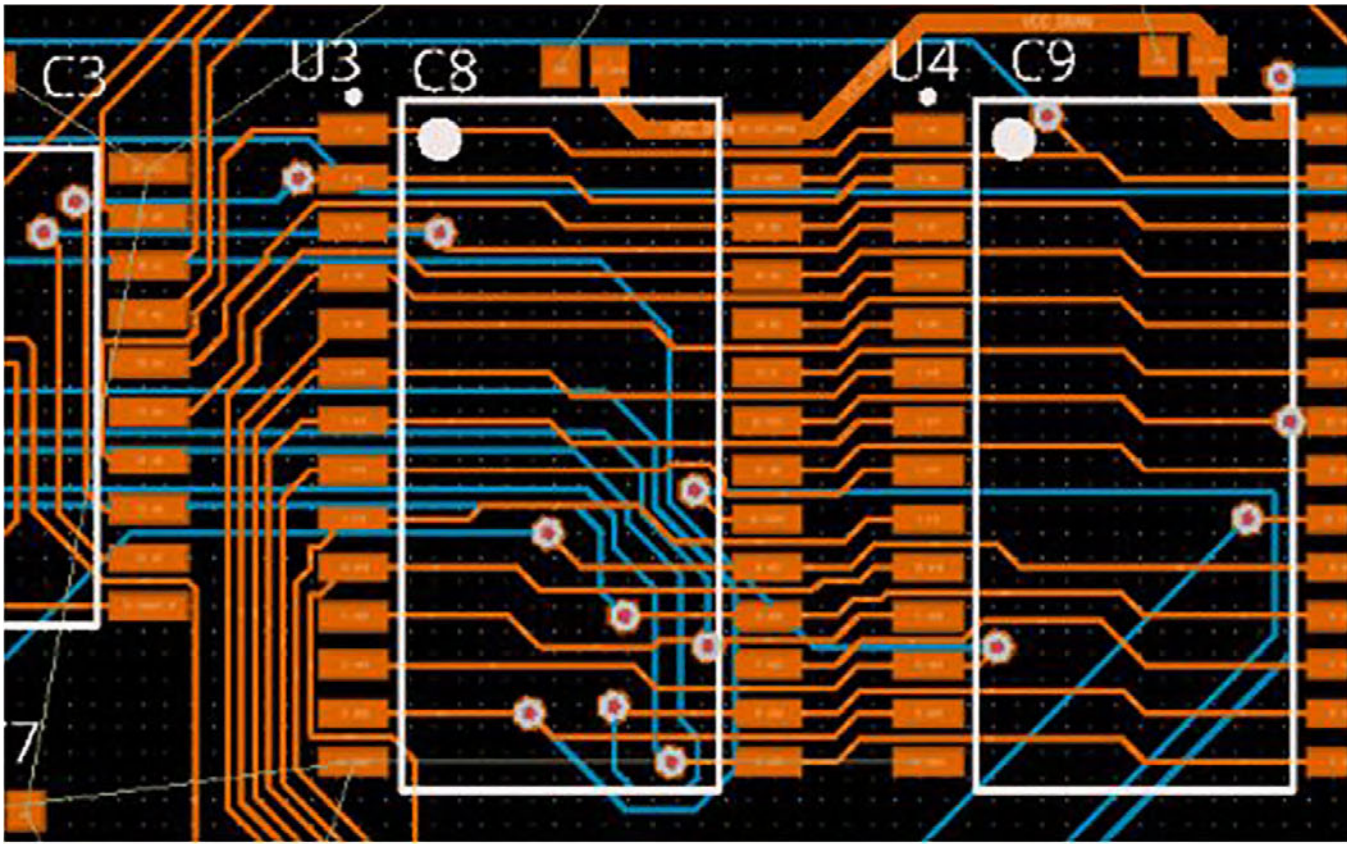

Figure 6: Situs results with 2-layer SMT board (Source: Altium LLC 2016).

optimize the routing while obeying the design rules. This is how Situs works, with an additional path to straighten traces for 90°/45° angles.

Still, for simple boards like the one shown in Figure 6, and for users who take the time to learn how to correctly set up the PCB rules and constraints along with different routing strategies, it does do a decent job.

The current generation of routing automation recognizes the need to have more interactive user input to determine paths. The ActiveRoute tool in Altium Designer uses path-cost optimized topological routing driven by user

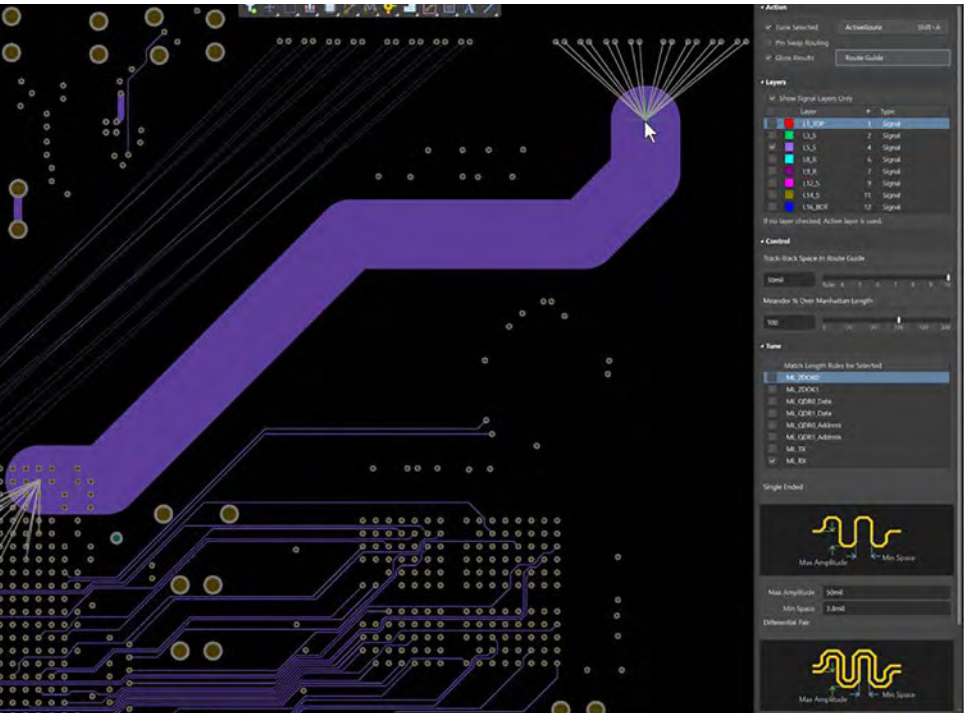

Figure 7: User-guided routing automation (Source: Altium LLC 2017).

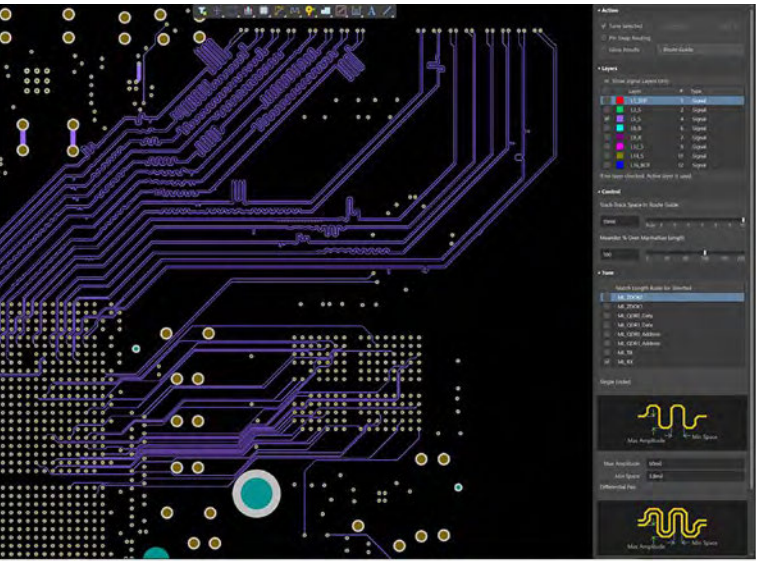

Figure 8: User-guided automation results (Source: Altium LLC 2017).

selection and guidance. The results are far more amenable to professional PCB designers and engineers (Figures 7 and 8).

This current generation of routing automation is a great step forward, providing speed for designers while allowing them to maintain quality and control of routing. But in my opinion, it won't be enough to carry us into the future of IoT.

Neural net-based topological routing engines need to be way more powerful. But the only way we can improve them to the point of useful results for every desktop, is through deep learning.

Again, coming from a complete layman, deep learning is a fancy term for expanding the data set that teaches the artificial intelligence engine called a deep neural network, and applying that expansive set of stimuli and responses to develop the software (or machine's) behavior.

The real question here is, what if the neural net routing automation had a practically unlimited set of PCB designs to train it? What if, each time you design a new PCB in your EDA tool, the EDA tool could learn your moves and begin to help you by anticipating how the board could be routed, or even how moving some parts on the board (within your constraints, of course) could drastically reduce routing time and layer count? What if you could leverage and contribute (voluntarily) to a hive-mind of engineers and PCB designers anonymously to train the world's greatest routing engine?

There'd be no excuse left for not designing the next imperative device! **DESIGN007**

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Ben Jordan is senior manager of product and persona marketing. He is a computer systems and PCB engineer with over 20 years of experience in embedded systems, FPGA, and PCB design.

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Fully Automated Schematic Verification

by Craig Armenti
MENTOR

The Challenge: Eliminate Schematic Design Errors

The schematic is the controlling document for every PCB design. It captures the design intent and drives all downstream processes including simulation, analysis, layout, fabrication, and assembly. As such, it is critical that the schematic accurately reflects the product's electronic requirements and specifications.

Historically, the all-important task of verifying that the schematic is properly conveying design intent has been a manual process conducted by one or more hardware engineers. This verification is usually performed one sheet or one block at a time, with some automation used to assist in the process such as exporting the bill-of-materials and/or the netlist to text files or spreadsheets.

Schematic verification is an accepted part of the hardware engineer's responsibility just as PCB layout verification is an accepted part of the PCB designer's responsibility. However, with today's circuit designs becoming more and more complex, time-consuming manual schematic verification is no longer an option. Manual verification of a complex circuit introduces significant risk by not identifying schematic design errors that are, in turn, passed to the downstream processes and ultimately to the fabricated board. This results in costly respins and increased time to market.

In a recent study conducted by the Aberdeen Group, 65% of the companies surveyed cited increasing product complexity as their top PCB design challenge (Figure 1).

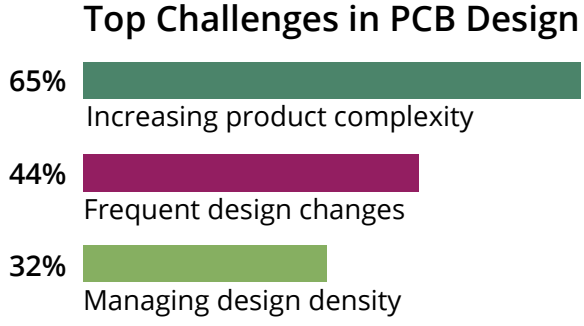

Figure 1: The top challenges in PCB design. (Source: Aberdeen Group)

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The Aberdeen Group's findings reinforce the criticality of ensuring that the schematic design is error-free throughout the product development process. This article discusses how an efficient, fully automated, schematic review process can be an enabler for design teams to eliminate schematic design errors, thereby reducing costly respins and improving time to market.

Manual Schematic Review: No Longer an Option

Schematic capture is certainly not the most exciting or glamorous task within the product development process. In fact, many hardware engineers delegate the task to technicians within the team, providing hand drawings or PowerPoint representations of the circuit for the technician to interpret and enter. This delegation allows the hardware engineer to focus on other tasks, such as circuit optimization or lab testing, but it also increases the importance of properly verifying that the schematic has been captured correctly.

Just as a great building cannot be built on a weak foundation, a great product cannot be designed on a weak schematic. As design complexity increases and product development time decreases, the need for fully automated schematic verification becomes more important. Without proper schematic verification, there is significant potential for additional hardware respins, slower time to market, increased field returns, and poor product quality (Figure 2).

During manual schematic review, teams typically focus on only the most common design issues including:

- Components not properly connected to power and/or ground
- Missing power
- Diodes oriented incorrectly
- Nets missing receiver
- Pin voltage mismatch (different voltage thresholds)
- Wrong board-to-board connectors
- Minor issues resulting in unnecessary delays, cost, and risk

While these are not complex issues, it is difficult, if not impossible, to visually find all occurrences of these issues in a complex design. And these are just the most common schematic issues. There are many more potential issues that a manual review simply cannot find.

Fully Automated Schematic Verification

ECAD verification tools have historically focused on the layout and manufacturing aspects

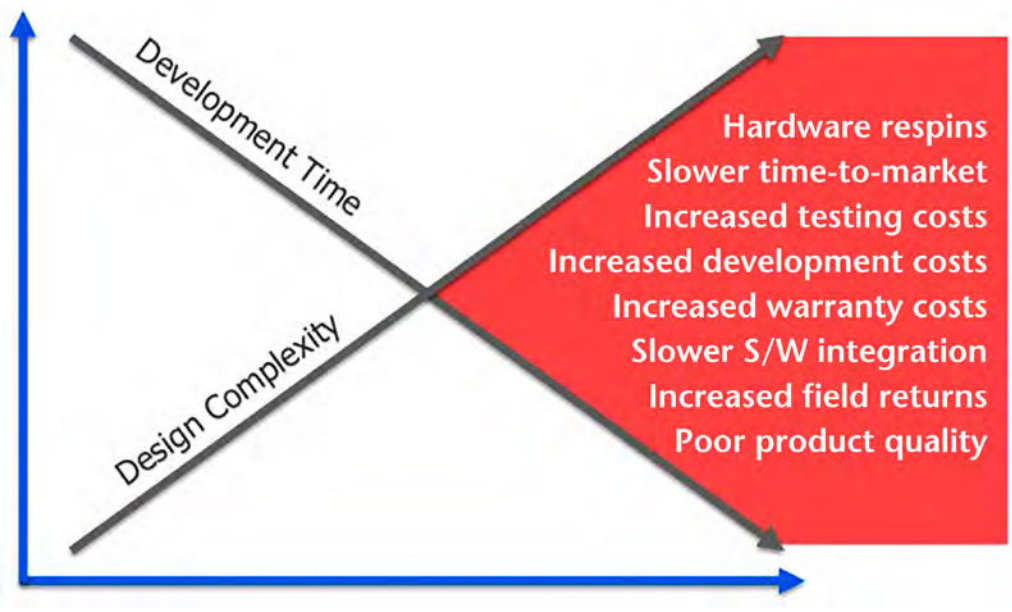


Figure 2: Impact of poor schematic verification as design complexity increases.

of the design, not the schematic. Given that 78% of all projects experience two or more respins, and that the root cause for many of the respins can be traced back to schematic design errors, the time has come for fully automated schematic verification. Eliminating schematic errors can result in significant cost- and time-savings, resulting in faster time-to-market, improved product quality, and lower risk (Figure 3).

By fully automating schematic verification to occur during schematic capture, rather than after, the development process shifts to the left, resulting in proven benefits such as reduced cycle time, lower costs, and the elimination of design spins (Figure 4).

Using Xpedition schematic integrity analysis, engineers can fully inspect all nets on a schematic using pre-defined checks and an extensive intelligent model component library. This automated schematic analysis can save design teams hundreds of hours of visual inspection and lab debug time. The checks

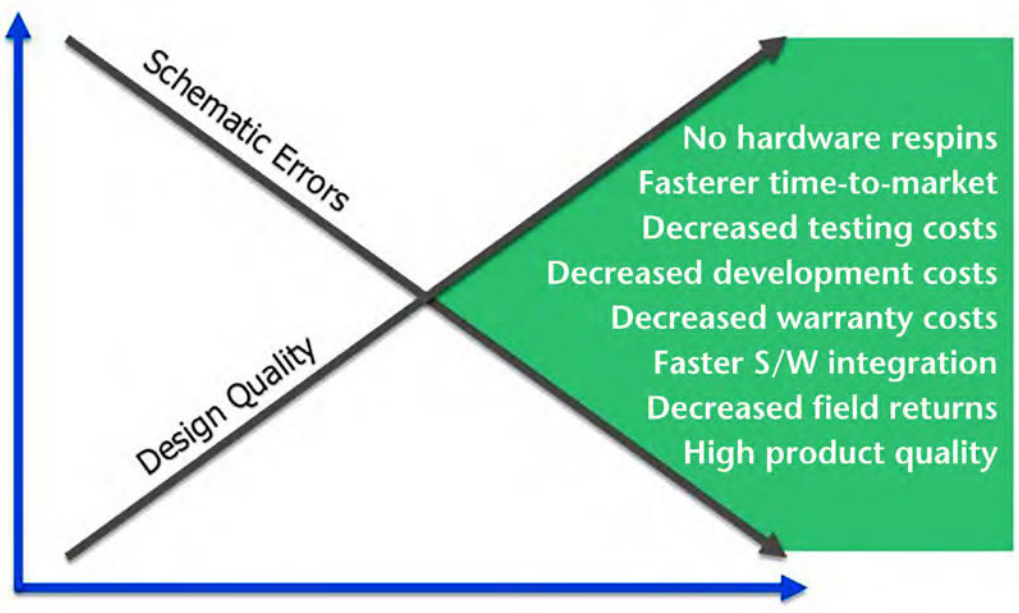


Figure 3: Benefits from fewer schematic errors.

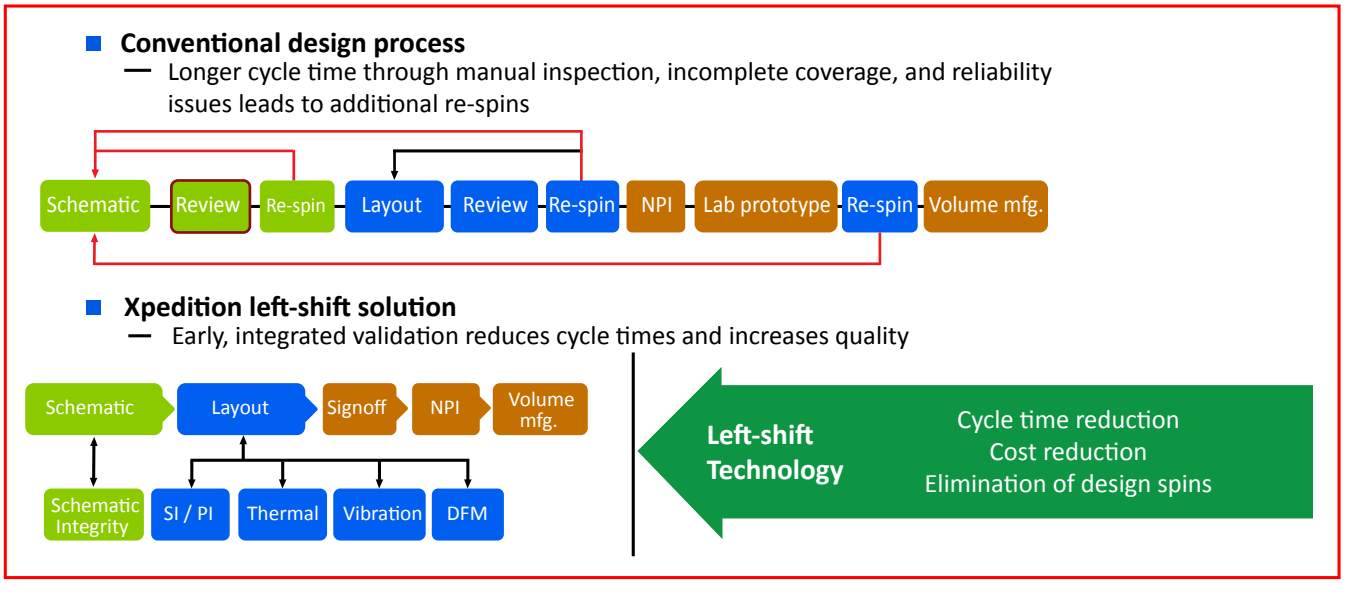


Figure 4: Left-shift of schematic technology.

execute rapidly in parallel with schematic capture, such that layout can commence with the highest confidence for first-pass success. More than 125 proprietary schematic integrity analysis checks are exhaustive, rapid, and power- and technology-aware. They are designed to identify both parametric errors and poor design practice and work with all major PCB design tools.

On average, Xpedition schematic integrity analysis performs 400,000 checks per design. An example of the results after performing Xpedition schematic integrity analysis on a schematic are show in Figure 5.

Applications

Xpedition's schematic analysis technology is applicable to multiple needs within an engineering team's design operations. While most of this article emphasizes the importance of schematic verification during new product design, other applications include:

- Existing product design: Sustaining existing electronic designs can create a significant burden upon product design teams, particularly when field performance does not match expectations and business intent. Schematic integrity analysis can be performed on electronic designs after they have been released into the market to improve the quality of the electronic design, increase yield, and decrease product returns. Schematic analysis can rapidly assess problematic products that are exhibiting less-than-ideal behavior that negative impacts production yields, in-warranty failure rates (MBTF), no-fault-found rates, and install/commissioning success rates. The presence of latent design defects and marginalities in field-released products can produce degradation of operating performance, causing the design team to be distracted from isolating the hidden root cause of problems. It is common for such diagnoses to consume multiple weeks of investigation, much of which is avoidable via screening of the design's integrity. By modeling problematic products, schematic analysis can systemically identify latent defects and marginalities providing design teams with a comprehensive overview of where to look to diagnose any performance-limiting problems, in a fraction of the time and effort normally required.
- Original design & manufacturing layout: The application of schematic integrity model-

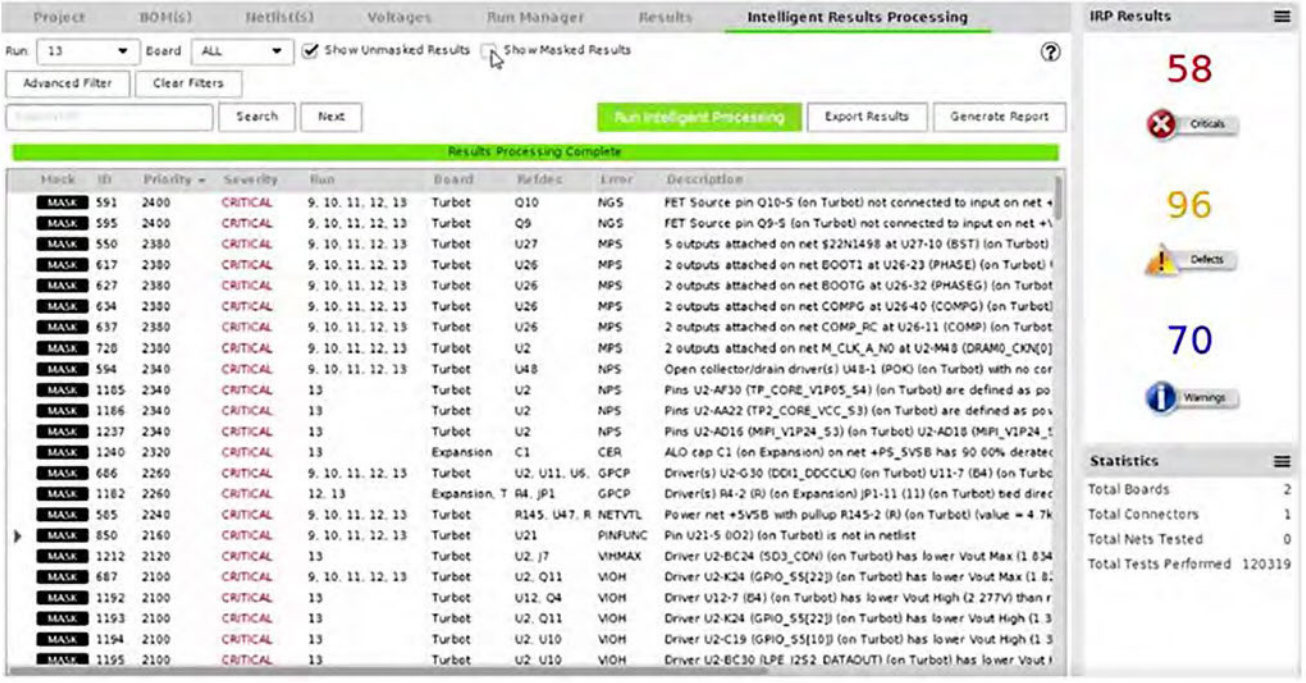


Figure 5: In this example, Xpedition schematic integrity analysis found 58 critical issues, 96 defects, and provided 70 warnings, far more than could ever be found with manual checking.

ing as a screen for a new design's acceptance can provide time-to-market-sensitive OEMs with a rapid and cost-effective means to assure consistent, reliable design from their ODM and design services partners. The systemic reveal of defects and marginalities presents an objective, thorough and measured indicator of the new design's ability to meet performance targets. The CAD-agnostic capability can work directly with clients' ODM partners to establish in-process analysis support, fully compatible with their unique design processes, which ensures optimized first pass design success.

Summary

One of the primary goals of any product development team is to reduce the number of design respins before releasing a product to market. Given that the root cause of design respins is often schematic design errors, a process that includes fully automated schematic verification can significantly mitigate the incidence of this costly issue. Xpedition schematic integrity analysis enables full inspection of all nets on a schematic using pre-defined checks and an extensive intelligent model component library.

New designs can be modeled and continually analyzed to assure that last-minute design changes are fully assessed. Data from multiple board designs can also be integrated to perform system-level validation. Furthermore, schematic integrity analysis can be performed on designs after they have been released into the market to improve the quality of the electronic design, increase yield, and decrease product returns.

Today's complex designs no longer allow for manual schematic review and verification. **DESIGN007**

Craig Armenti is a PCB marketing engineer for the Board Systems Division of Mentor. Armenti has more than 25 years of experience in the EDA industry. He has held marketing and application engineering positions with several major telecommunication and software companies.

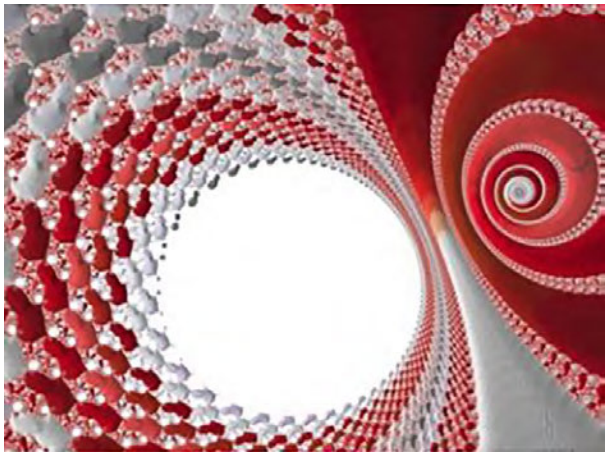
Developing a Secure, Un-Hackable Net

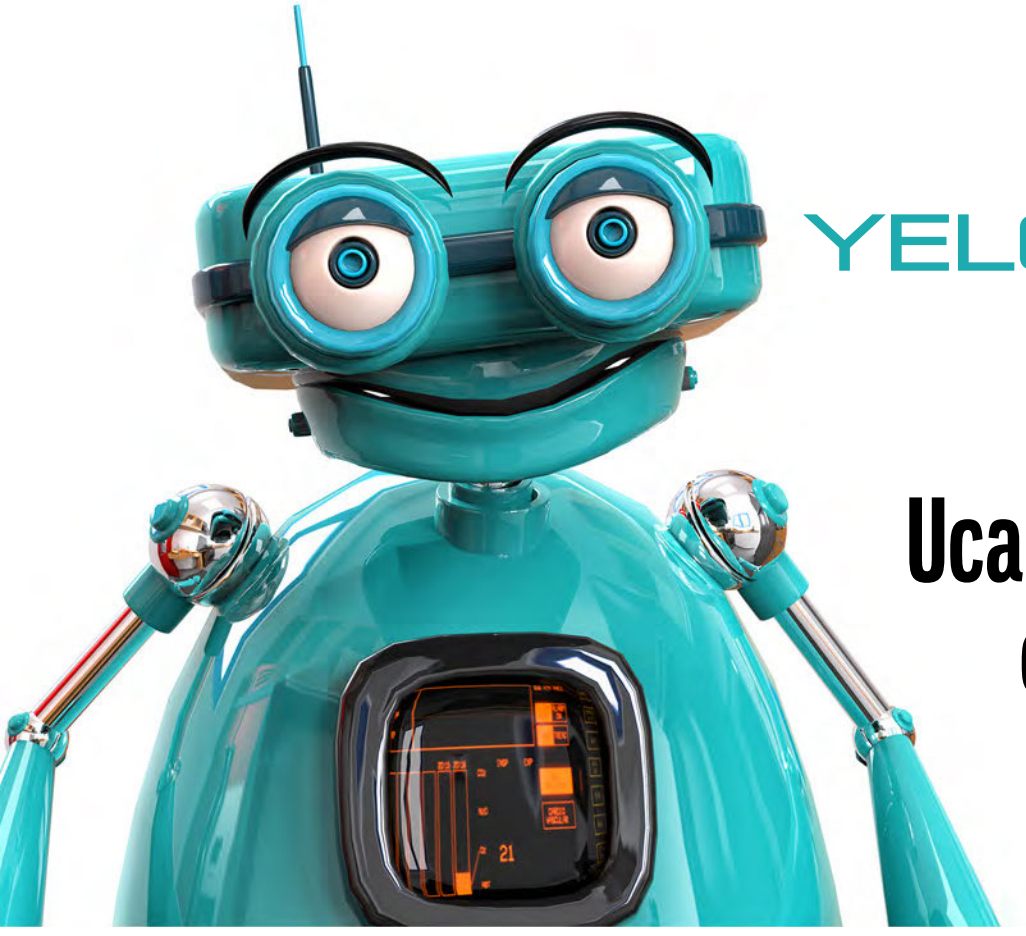
With the EU and UK committing €1 billion and £270 million respectively into funding quantum technology research, a race is on to develop the first truly secure, large-scale network between cities that works for any quantum device.

"When quantum computers are fully developed, they will break much of today's encryption whose security is only based on mathematical assumptions. To pre-emptively solve this, we are working on new ways of communicating through large networks that don't rely on assumptions, but instead use the quantum laws of physics to ensure security, which would need to be broken to hack the encryption," explained lead author Dr. Ciarán Lee (UCL Physics & Astronomy).

"Our approach works for a general network where you don't need to trust the manufacturer of the device or network for secrecy to be guaranteed. Our method works by using the network's structure to limit what an eavesdropper can learn," said Dr. Matty Hoban (University of Oxford).

The team used two methods–machine learning and causal inference–to develop the test for the un-hackable communications system. This approach distributes secret keys in a way that cannot be effectively intercepted, because through quantum mechanics their secrecy can be tested and guaranteed.





YELO!

Ucamco Focuses on Improving Gerber, CAM Automation

Feature Interview by Andy Shaughnessy
I-CONNECT007

Ucamco has launched quite a few new CAM tools over the past few years, as well as updates for the venerable Gerber data transfer format, which the firm owns. For our "What's New?" issue, I caught up with Ucamco Managing Director Karel Tavernier and asked him about the company's latest efforts. He discussed their newest CAM tools, recent enhancements to Gerber, and the role artificial intelligence plays in automating the company's technologies.

Andy Shaughnessy: Karel, what's new at Ucamco?

Karel Tavernier: Our latest releases were driven by one of our cleverest customers, who challenged us to speed up the processing of routine jobs by making it possible to CAM 50% of standard jobs automatically. This makes a lot of sense: CAM takes up a significant proportion of the time it takes to make short run products, and yet the marketplace expects ever shorter delivery times. The more we looked at the proposition, the more we realised that 50% must indeed be achievable with current AI technologies; after all, with Integr8tor, we are already enabling our clients to input around 80% of their incoming jobs automatically. And at the other end, once the single PCB is final, panelization and output of the digital tools is largely automated using standard tools or can be automated using Hypertools—custom scripts within automation programs.

Our challenge, to close the gap between the original job and the finished single PCB, has largely been achieved with our Yield Enhancing Layout Optimizer (YELO). YELO is a set of AI algorithms that automatically adjust designs to fit given goal capability classes, and they do this incredibly well, automating the boring, routine part of CAM work, thus freeing CAM engineers to focus their skills on the more complex designs that can't be handled automatically.

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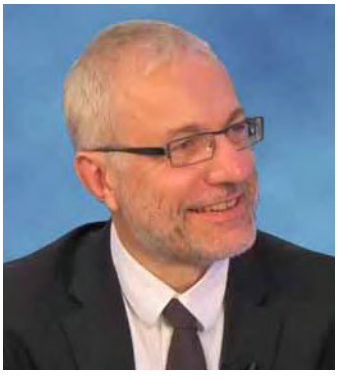
Another time-waster is the way in which CAM and CAD professionals typically communicate with each other about design issues. Today's methods are to my mind quite medieval and utterly confusing, including screen shots pasted in Word or Excel document with comments batting to and fro across the ether. The problem with screen shots is that they offer no context—you cannot zoom or see other layers—and the whole workflow lacks traceability: What was approved when and by whom? And precious time drains away while waiting for approval.

Enter our new Communic8tor, announced at the recent productronica.This can be likened to Adobe Acrobat, but where Acrobat is excellent for annotating, proposing changes and giving approval on PDF documents, Communic8tor is designed specifically to handle the resolutions, precision and complexity of PCBs, making it possible to annotate issues or classes of issues, give or decline approval and so on. It does this within the context of the PCB, showing multiple layers and enabling high zoom levels, making it possible for the parties to measure what they are seeing with near infinite precision. And traceability and workflow control is built into the system. Even better, Communicat8tor is not confined to our installed base, any system that can output our DPF format, Gerber or ODB + + can handle it.



Karel Tavernier, Ucamco

Shaughnessy: What are you working on for the next year or so?

Tavernier: YELO and Communic8tor are totally new, and to be absolutely frank most of our R&D effort will be spent on enhancing them and handling incoming customer requests.

Shaughnessy: What would you say are the biggest drivers of your decisions regarding new products and upgrades?

Tavernier: By nature, we are all techies rather than commercial people, so for us, setting R&D priorities involves heart-wrenching choices. By nature we are drawn to develop new, innovative stuff. However, we have an incredibly loyal customer base, many of whom have been with us for decades. It is our duty to protect their investments in software, automation and operator training. We must keep a balance between improving existing products and developing new ones. And I think we do. We have continued to develop Ucam, starting from a pure 32-bit single processor system, running native under Unix, to a native Windows system, to today's UcamX, 64 bit, multi-processing and a state-of-the art workspace GUI. While innovating and developing the platform, we worked incredibly hard to maintain broad compatibility so that our maintenance contract customers could come with us without being forced to buy new software. Not that we supply all new options for free under maintenance—we don't—but as part of our maintenance agreement, we protect our customers' investment and take them with us as technology changes.

While we were developing Ucam, we also spent time innovating in other areas. With Integr8tor we were the first to bring automated data input and a workflow server system to the fabrication industry, and we are still the best at it. Now with Communic8tor we bring a totally new concept to the conundrum of communication between fabrication, assembly and design.

Shaughnessy: What technologies at Ucamco are really exciting to you?

Tavernier: Personally, I am really excited by the AI technologies we have started to use in recent years. A PCB contains lots of data, but in a restricted and defined field. This makes it an ideal target for AI technologies. From the application point of view Communic8tor is the most exciting. It is a totally new concept, at least in our industry. It addresses a need which currently lacks structured solutions.

Shaughnessy: We see several other data transfer formats getting a lot of attention, but most PCB designs are still created in Gerber. Why do you think PCB designers are still using Gerber after so many decades?

Tavernier: Maybe the question is why one would stop using Gerber. Especially if you go beyond the generalities of data format to look at the specific question of CAD to bare board CAM data transfer. But before we do that, let's get specific about Gerber too: there's the traditional Extended Gerber (X1), and the latest generation Gerber X2 format. There are things that Extended Gerber does not do. It doesn't contain the netlist, nor where the vias are, nor what the layer structure is—important information, admittedly. But it does the most important job of all exceedingly well: It describes the most complex part of bare PCB data, the layer images and drill data, in clear, reliable and simple terms.

And implementations are thoroughly debugged, so there are very few problems with images in Gerber. This should not be taken for granted: geometric software is easy enough to create, but debugging it and making it truly reliable takes years. Attempts to replace Gerber have until now been idealistic and impractical, because instead of adding the information that was lacking, they proposed to replace Gerber's image transfer format, which works so well, with another image format that is incredibly difficult to get right, and then add the missing information, which is actually the most straightforward part to add. It's a bit like using a sledgehammer to swat a fly and of course the market has not followed.

And so we come on to Gerber X2, which does what those other formats might have done well to do: it's a compatible extension of Gerber X1. It leaves in place what works—the image—and adds the information that is missing: the layer structure, the netlist, and where the vias are.

It's simple and it takes what works and builds on it, and it is gaining market share very rapidly. ODB++ has achieved a modest market share after 25 years of ceaseless marketing, and all other attempts at radically new formats have failed up to now. X2 has achieved over 10% of market in our installed base in just two years, and its use is increasing month by month. The reason? Simplicity and compatibility. People stick with Gerber because Gerber is simple, and replacing it is complicated and not worth the bother. And they will continue to use Gerber in the coming 50 years, albeit an evolved Gerber, with new capabilities added in a compatible way.

Shaughnessy: Thanks for your time, Karel.

Tavernier: Thank you, Andy. **DESIGN007**

Researchers Develop World's Smallest Wearable Device

A Northwestern engineering professor, working in conjunction with the global beauty company L'Oréal, has developed the smallest wearable device in the world. The wafer-thin, feather-light sensor can fit on a fingernail and precisely measures a person's exposure to UV light from the sun.

The device, as light as a raindrop and smaller in circumference than an M&M, is powered by the sun and contains the world's most sophisticated and accurate UV dosimeter. It was unveiled at CES in Las Vegas and will be called UV Sense.

UV Sense has no moving parts, no battery, is waterproof and can be attached to almost any part of the body or clothing, where it continuously measures UV exposure in a unique accumulation mode.

Rogers said the device, created in a partnership with L'Oréal, is meant to stick on a thumbnail – a stable, rigid surface that ensures robust device adherence. It's also an optimal location to measure exposure to the sun.

Pulsonix Ready for 2018

Feature Interview by Andy Shaughnessy
I-CONNECT007

Pulsonix has been developing PCB design software for almost 20 years, establishing a reputation for its full-featured, low-cost design tools. Now, the UK-based company wants to break into the U.S. market, and recently showcased its latest tools at PCB West. During the show, I-Connect007's Angela Alexander and I spoke with Business Development Manager Ty Stephens about the company's latest tools and plans to become a major player in the U.S. market in 2018 and beyond.

Andy Shaughnessy: I'm here with Ty Stephens of Pulsonix. For some people who may not be aware, give us a brief background of Pulsonix.

Ty Stephens: The company was founded in 1997. At that time there were no noticeably unified products in the market. By this, I mean all the tools you would expect to take an idea from concept to realization, for example schematic capture, Spice simulation, PCB layout and manufacturing preparation in one product environment. Most of the EDA products around were generally formed through mergers and acquisitions, so they ended up all being bolted together. We noticed there was an opportunity to have one unified product where it was schematic capture, simulation, PCB design, and now the 3D element, all within one system. This is where we started when the product was released in 2001, and now we've grown to the size that we are today, with household names using our software throughout the world every day to create their products.

Shaughnessy: Pulsonix seems to have a niche—robust tools at a low price point.

Stephens: Yes, I suppose for us it came from a point of view as a startup company, but with considerable experience gained at our previous company, we understood the need for a very stable product offering, high quality support, and very fast turnaround on software fixes. This was and still is our unique selling point. Functionality was equally important, so

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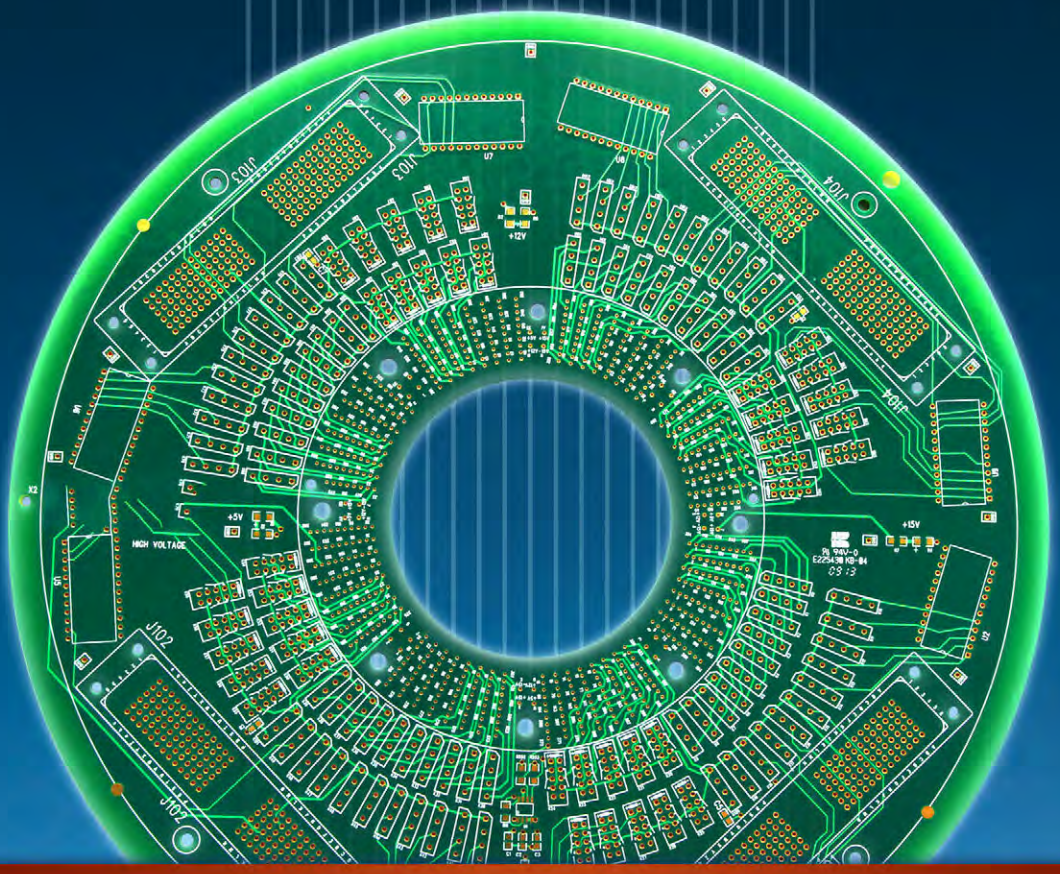

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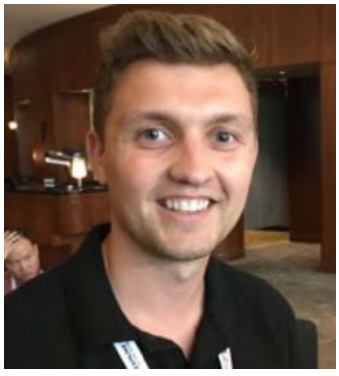
we set out to create a great tool that met the needs of all users—large companies, small companies and individual users alike, each of which wants to be able to design comprehensive products without large overhead. We coupled this with an aggressive price point that instantly made us attractive in the market when you also consider the performance and functionality being offered. We've built on that, and now we've reached the size where we can maintain this price point.



Ty Stephens, Pulsonix

Shaughnessy: Tell us about the new tools that you recently released.

Stephens: One of the exciting features we're showcasing here today at the PCB West show is the Component Search Engine. This tool has been developed by a UK-based company called Samacsys and together we have worked to integrate their component search engine into Pulsonix.

The website itself allows Pulsonix users to search over 11 million parts, view datasheets, pricing information from various suppliers, and most importantly, download verified Parts and their STEP models directly into Pulsonix with click of a button.

I don't just mean download from a website, then manually import them; I mean one click and it's physically on the end of your cursor in either the schematic or PCB design environments and saved into the Pulsonix libraries automatically. I remember speaking to Alex McDougal, the managing director of Samacsys, recently and he mentioned that engineers can spend up to half their design time working on component creation activities. Can you imagine just how much time this is going to save our users?

Angela Alexander: This sounds very interesting and something I can imagine many of your customers are excited about.

Stephens: Yes, very excited. We have trialed it across a selection of customers in Europe and the response has been tremendous. We are very pleased to be rolling it out to all the Pulsonix user base. As a no-cost option, it endorses the value our users receive for their investment in the product purchase and the annual maintenance charge.

Alexander: So this is your first venture out here to sell in the marketplace?

Stephens: Not quite; this is the first time we have been here as a company showcasing Pulsonix at a major tradeshow. We've been selling Pulsonix here since 2001 through reselling partners who have attended various shows, but now we are here in our own right exhibiting our products.

Alexander: And how have you found the show? Does it seem to be going well?

Stephens: Very successful so far; we've met lots of interesting people and have been discussing their needs and issues. Their challenges are very well addressed in the Pulsonix tool, so that has been a very positive aspect for us. The feedback we have had is that our technology meets their requirements and the product is also a good price point for them.

Alexander: That's good.

Shaughnessy: Great. Is there anything we missed?

Stephens: No, I think that's it for now. We have had a good response from the show and will build on this success in the coming months.

Shaughnessy: Thanks for speaking with us today, Ty.

Stephens: My pleasure. **DESIGN007**

I-Connect007

EXCLUSIVE IPC APEX EXPO 2018 PRE-SHOW COVERAGE

A Sneak-Peek at IPC APEX EXPO 2018

IPC President and CEO John Mitchell gave I-Connect007 a sneak-peek at the upcoming IPC APEX EXPO, happening in February in San Diego. Mitchell provides a description of this year's keynote, as well as a few new additions and areas of emphasis. It looks like it will be another packed house, with plenty to see, do, and learn about.


John Mitchell

Patty Goldman: John, what can you tell us about the upcoming show, and keynote speaker, which I understand is expected to be quite a draw?

John Mitchell: Jared Cohen is our Tuesday keynote. He is now the CEO of Jigsaw, which is a part of Google. He's the former advisor to two U.S. Secretaries of State and the author and member of the Council on Foreign Relations. The title of his speech is, "Game changers, Technology, and the Next Big Disruptions." He travels a lot, so he'll be drawing on his travel and first-hand accounts of some of the various important and emerging trends in technology, and then reveal how some of those will matter to the electronics industry.

Goldman: That should be very interesting and appropriate.

Mitchell: Yes, we're looking forward to Mr. Cohen's insights into the complex world of technology. In addition to this opening keynote on February 27, I will give a keynote on 'Educating a 21st Century Workforce," and cover how understanding the challenges and solutions in educating a 21st century workforce, is critical to businesses and leaders around the globe.

Goldman: Sounds good. What else will be going on at APEX?

Mitchell: Our theme this year is "Succeed at the Velocity of Technology." We are more than 95% sold out for the show floor, which is great, and we're anticipating more than 450 suppliers to showcase their products and services. In addition to the exhibition, we of course have our educational offerings, the professional development courses, which include subjects like PCB fabrication troubleshooting, printing, dispensing, jetting, manufacturing yield, reliability, and DFX. We really try to provide things that are driven by real-world application of what's happening right now, so the attendees can apply it later. We're trying to help them access new research on materials and processes and learn about trending materials or applications and processes, such as Industry 4.0 and wearables. We'll address real-world problems and teach the practical way that people can be

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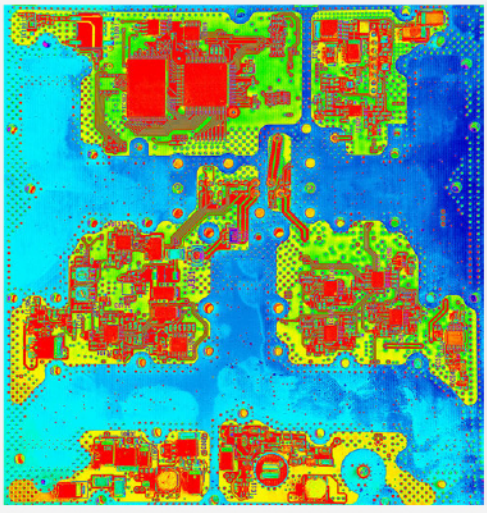

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successful at their jobs. So, flex circuit design, signal integrity issues, wearables, printed electronics, impedance and tools that merge electrical and physical design are just a few of the areas that the programming will cover.

Then, we have the technical conference, which offers the industry's most stringently-vetted program available. We have more than 80 papers this year, and they're measured against strict requirements by a panel of industry experts. We want to make sure we have the latest research and innovation available from the subject matter experts in the areas of board fabrication, design and electronics assembly.

The content that the attendees will be experiencing at this show is completely unique to IPC APEX EXPO. We've been careful to craft the conference so that similar topics don't overlap to help attendees maximize their time and effort. A few of the highlights include PCB fabrication reliability, assembly reliability, and then voiding and developments in the assembly of bottom termination components.

The Design Forum will be going on concurrently and will feature distinguished experts from the design community. They'll be delivering design-focused education on some topics, as well as sharing priceless and timeless lessons learned. They'll be presenting practices in Industry 4.0, including IPC-2581, emerging ECAD and MCAD, designing for flexible circuits, as well as circuit board design and mistakes you can avoid. Those are some of the topics that will be presented there. We will have buzz sessions again, with a market outlook buzz session, as well as IPC standards updates and environmental legislation updates.

We're trying to make sure that people in every stage of their career can be successful by coming to IPC APEX EXPO. There will be sessions for early career that we would recommend, things like PCB fabrication, voiding, bottom termination components, PCB surface finish reliability, things like that. Then, for those in mid or later career, some of the sessions they might benefit from would be the wearables, printed electronics, emerging technology, SIR corrosion, and some of the reliability issues with dispensing jetting, etc.

The whole show continues to grow every year, which I'm very pleased with. Frankly, the industry's been doing very well this past year. We're excited about that because typically the show follows the viability of the industry. We expect the show to grow right along with it this year. One of the two annual IPC board of directors' meetings will be held right before APEX EXPO, so you should see the majority of the IPC board members in attendance.

Goldman: Will there also be award ceremonies?

Mitchell: Yes. At the Tuesday luncheon we will have the official IPC annual meeting, and then for the Monday and Wednesday luncheons we will have the industry awards ceremonies. We just can't get them all done in one lunch. When you have thousands of volunteers, it's a good problem to have, right?

Goldman: Exactly. At the Tuesday annual meeting, will we be electing any board members?

Mitchell: A new member of the executive committee—a new secretary/treasurer—will be put forward at that time. Actually, all of the executive positions will be renewed because Joe O'Neill will just have finished his two-year term as chairman. He would move to immediate past chair and there would be subsequent shifts in the other positions, if tradition follows.

Those positions are being vetted by the board and we'll have that approved for general voting, as well, once the board approves. Also, there will be at least one board member renewal, and there may be one slot available, or not. We'll see. Right now, we're completely full at the maximum number of board members. If one of those people moves onto the executive committee, then there's a possibility that there may be another slot available, but it won't be a necessity to fill it. We have five on the executive committee, and then the elected board members range anywhere from seven to 14 members at any time. Right now, we're at 19, which is the max.

Goldman: Okay, what else? Anything more to add on the keynote speaker?

Mitchell: I think people will be very excited to hear from him. We've had really good fortune most of the years I've been here in having keynotes that people are pretty gung-ho about, so I expect this will be no exception.

And one other thing. In an effort to engage people earlier on understanding the industry and what IPC does for it, we're bringing in some high school groups that will be touring and will be privileged to hear some panels. I understand one of the schools, a San Diego school, has already accepted, and we've put the invitation out to a couple others.

Goldman: Any news on the standards front?

Mitchell: In addition to our standards, education, advocacy, and solutions areas, there are a few initiatives that we're going to focus on for the next two or three years. You'll see some of this coming out at the show. One of those initiatives is what we're calling the transportation initiative. As you've noticed, we've recently had a lot of standards in the automotive arena. We're going to be looking at the heavy trucking, rail, and shipping, etc. as well. Since electronics is proliferating into the transportation space, we want to make sure that we can leverage the industry's expertise to those verticals, as well. You'll see a lot of effort on the transportation initiative.

On the education initiative, we're looking to do a lot more and that will be discussed at APEX EXPO as well as workforce development. There are still a lot of jobs that aren't being filled and we're trying to work with the industry to understand exactly what the skill sets are that we could help develop in individuals so there can be more people available to be hired, as well as reaching out to schools and doing some academic work there.

We'll continue to improve our systems to be better and more consistent with our offerings to the industry, on a global basis.

Andy Shaughnessy: You mentioned the design forum. My focus is design, so I'll be covering that. Sounds like you have a pretty good program.

Mitchell: There's the standard information that everybody's used to, that will of course, always be there, but the team just continues to reach out to the industry to understand the latest, newest, hottest issues that we need to be covering. They're striving to make sure that it's out there so people can get that information.

Goldman: John, how much interchange is there between the people out on the show floor and the people in the conferences and committee

meetings? Sometimes I feel like for the people on the show floor, all they know is the show, and they never see that other half, which is the conference and the committee meetings. Do you get that feeling?

Mitchell: I'm sure that happens for some people, but I know there are other people that are experiencing all the show has to offer. It just depends. For instance, if you're a sales person and you're there, guess what? You're not going to leave the show floor, and that's where you ought to be because I know people there last year who said, "Hey, in the first day I met my entire annual quota." That person really ought to be on the show floor, doing the selling. That's what their role is. That's where they're going to be the most effective they can be.

For other people, they're going to spend time at committee meetings, standards meetings, and learning events, etc., and the show floor. That will be the guy that gets caught Wednesday afternoon and buys something on the show floor from somebody else because they were tied up all day Tuesday, and that's why people have three days to check out the exhibits.

Some instructors are going to be teaching the entire time and they may not even make it to the show floor. That's why we try to have the big food event one evening so people have a good motivation to go down to the show where we do the burgers, the dogs, and the brats and stuff. We pull everybody out on the show floor at 5 pm on Tuesday for the reception, then on Wednesday we're having the ice cream social from 2–4 pm on the show floor.

Goldman: One of the good parts about San Diego is the fact that the meeting rooms and the show floor are so close together, right?

Mitchell: Yes. Just down the escalator and you're right there. It's all a good thing.

Goldman: Yes, it is. Thank you so much, John. We'll see you soon.

Mitchell: Thank you, Patty. ■

Philip Carmichael, IPC President, Asia on the Changes in PCB Value Chain

During the 2017 International Printed Circuit & APEX South China Fair (HKPCA & IPC Show 2017) in Shenzhen, China, IPC Asia President Philip S. Carmichael speaks with I-Connect007 Managing Editor Stephen Las Marias about the move in the value chain that's driving the electronics manufacturing industry forward. He discusses the new market trends that will further the growth of the PCB industry, and how new manufacturing technologies will help bring the industry toward the vision of a lights-out factory. Carmichael also explains the need for knowledge transfer, education, and standards, in the industry.

Watch the interview here ▶

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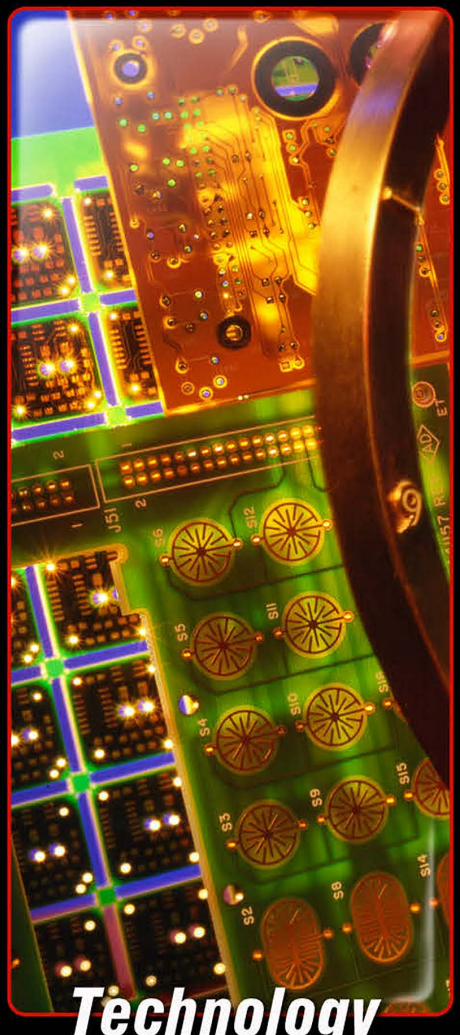

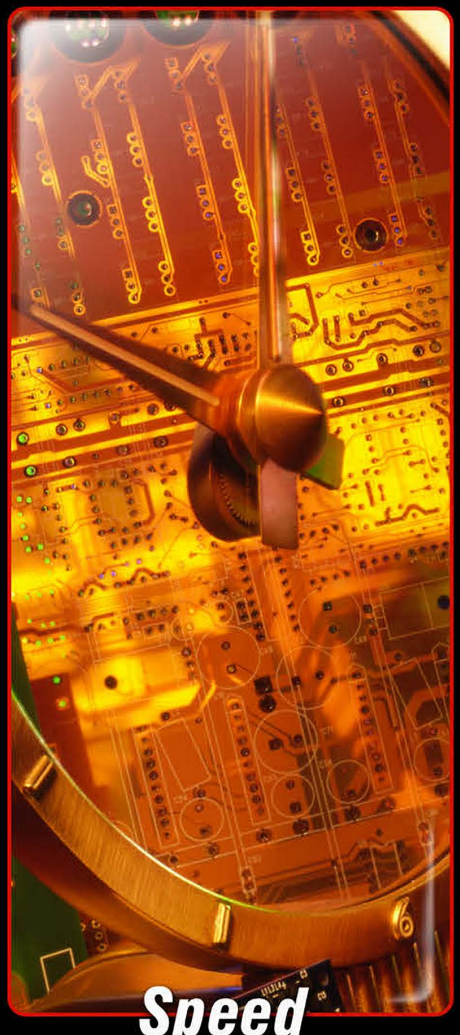

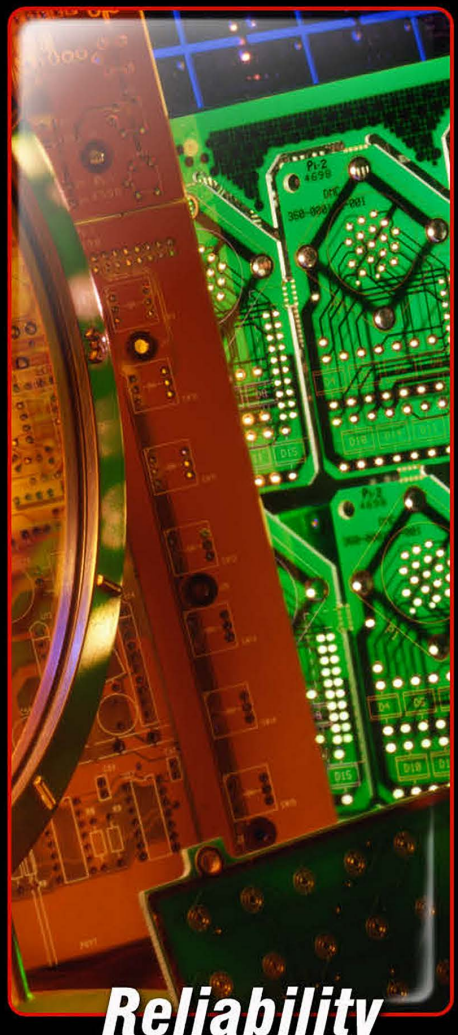

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Keeping it New, Current and Relevant: IPC Conference Director Jasbir Bath

Jasbir Bath, technical conference director for IPC APEX EXPO, has been coordinating IPC's technical program for several years now, but his interest and excitement for the event continues to expand. It's clear that Jasbir and his team take great pains to create a fresh, exciting menu of sessions, development courses and more, full of potential learning experiences, year after year. It looks like 2018 will be no exception.


Jasbir Bath

Patty Goldman: Hi Jasbir, please begin by telling me what your position at IPC entails.

Jasbir Bath: I'm the conference director for the IPC APEX EXPO conference. I've been doing it for the last four or five years. My responsibility is to help organize the conference, solicit papers, and then put together a technical program committee to solicit papers and review the abstracts coming in, and then select papers for the conference. We're at the stage now where we're putting papers into sessions. We're writing session descriptions and we're receiving papers and presentations for each of the sessions to review for the conference. That's the job that I'm responsible for. We may have some drops, we may have some additions, but we're in the middle of the review process for papers and presentations now.

Goldman: How many tracks should there be?

Bath: There should be 32 sessions. We're doing about five tracks in parallel from Tuesday afternoon, Wednesday all day, and then Thursday morning. We're trying to make sure that the tracks have assembly, PCB fabrication, and reliability tracks, as well as some others. We're trying to keep the fabrication and the reliability in one track, the assembly in one track, etc., so that two fabrication sessions aren't going at the same time. It's always tricky. We try not to clash with the standards committee meetings. That gets interesting, because some of the people who chair the paper sessions may also be involved in standards meetings. We want to make sure, for example, if there's a PCB assembly track that it doesn't overlap with a PCB assembly standards committee meeting.There has been feedback on that, so we're putting in a renewed effort to make sure we don't have any overlaps. At the same time, if there's a potential clash on Thursday morning with the professional development (PD) courses that are going on, we're also trying to make sure we don't have a PD course on one subject coinciding with a technical session in the same area.

Goldman: Do the professional development courses run on the weekend and during the week too?

Bath: They run on Sunday all day, Monday all day, and then Thursday morning. It's not a big overlap. There maybe last-minute changes that we can't account for, but generally we're in good shape.

Goldman: It's hard to make everyone happy.

Bath: Exactly. The chair of a standards committee session may also be chairing a technical

conference session we have, so we give priority in some ways to someone who's chairing a standards meetingand chairing a session. We'll give them the power to move things around.

Goldman: Continuing with the conference, are there any new tracksor hot topics this time around?

Bath: We have some that are generally considered hot topic sessions. There will be sessions on bottom termination components, which is a growing technology. We have the emerging technology session where we cover wearables, printed electronics, and emerging technologies like stretchable applications, wash-ability of materials for e-textiles, and an overview of XR virtual reality or augmented reality. That's a nice session. We have the traditional PCB fabrication and assembly sessions and component reliability. We have voiding sessions, which is a hot topic in terms of voiding areas for BGAs and components and how to minimize voids. We have a session on jetting, which is a newer technology where people are looking at non-contact dispensing for solder paste.

Then we have the traditional sessions, but some of those like surface insulation resistance (SIR) are still continuing issues. There are still challenges in terms of not just existing materials, but developing materials, masking materials, flux residue issues, etc. We'll have session(s) on reliability of plated through-hole materials, issues with reliability in terms of degradation and glass epoxy degradation. We're trying to cover things that are challenging, or issues that are coming up in the industry.

Goldman: Of course, all the papers are fresh and dealing with the latest technology.

Bath: Exactly. We also have a session on creep corrosion, where we have experts from IBM talking about the new developments in corrosion testing. Typically, you've got your alloy sessions, your high-speed/ high-frequency sessions, and where we're going on that. Then surface finish reliability, where we'll talk about recommendations for increasing shelf life with PCB finishes. A paper we have for the cleaning session is looking at cleaning challenges when we get to very fine powder sizes for solder paste.

Goldman: How clean is clean, right?

Bath: How clean is clean, and how clean can you get it? What are the challenges of removing flux residue? We have solder paste testing development on where we are in terms of the test technologies and J-standard 005, what test vehicles you can use for solder paste evaluations, and paste development for laser soldering applications. It's the kind of things that discuss new applications coming up, like miniaturization. We're getting smaller and smaller paste deposits. Some of the components to assemble are temperature-sensitive so reflow ovens can't be used so you may have to use laser or other non-contact applications to reflow those locations.

We've got rework application sessions. Rework is still interesting and still coming up. Session speakers will talk about the challenges for big board rework and optimizing bottom heat for manual rework applications. Then there are the typical copper foil issues, alloy reliability, and test/X-ray inspection issues. For instance, the impact of X-ray on preprogrammed managed NAND devices and understanding if the X-ray is causing any radiation damage to thedevices with best practices.

We have a design session looking at different redesigns and how to do it the right way, ECAD/MCAD tools, etc. We have a session on flex with areas covered including minimizing signal degradation for flex PCBs. We have sessions on conformal coatings covering issues on high temperature protective coatings, and nano coatings, etc. We are also looking at reliability modeling and reliability of adhesives. That pretty much covers the conference. We have some new sessions, some sessions on existing material developments, where we're going, and then test and papers to cover some of the challenges and development that we need for new technologies.

Goldman: How many papers total for the 32 sessions?

Bath: Approximately 75. The sessions are either two-or three-paper sessions running from Tuesday afternoon, Wednesday all day, and then Thursday morning.

Stephen Las Marias: Compared to last year, do you have more papers for 2018?

Bath: It's about the same. If the paper is being presented in another conference we don't accept it. Basically, we want what is new. We set a higher bar for our criteria for acceptance. Our philosophy is not quantity, but quality. If it doesn't add value we won't include it within the technical conference. Our review process is such that, when we're reviewing papers and presentations, we're reviewing for technical content, as well as grammatical issues, and making sure that the paper is a good read for the audience. We're reviewing papers to make sure they read well. That's something that I don't think other conferences do as well. Our process for review can take 2–6 weeks because of the back and forth with the authors. When we do reviews on the papers or presentations, we generally get good feedback. Some people don't like some aspects when we ask them to update them. But, in general, we get a lot of feedback that says, "Thank you for helping me to provide a better paper and presentation." Because, at the end of the day, we're trying to enhance the informationvalue to the audience. That's the idea.

Goldman: Do you also put together the buzz sessions?

Bath: The buzz sessions come in with industry challenges. Typically, we ask within IPC, "What sessions do you think would be of use to the industry?" The sessions typically are presented by IPC staff, but buzz sessions could be from somebody who comes to IPC and says, "We would like a session in this area." These are free sessions which are giving the status of some area of interest. For example, the first buzz session this year is a politics and policy roundtable. What's going on in government relations? What are the issues? Your typical technical conference session may not have this kind of discussion. These usually have two or three speakers, a panel, a short presentation, and then question and answer with the audience, and more interaction. The second buzz session will be a standards update. Three is on printed electronics. Where are we going? Where do we need to go to get to the next level? These are things that someone who is a chair of a standard committee, or an IPC staff standard commitee liaison, has been talking within their committees, and is saying, "Couldn't we have a buzz session on this area?" Maybe it's not fully developed, but it's developing, and they can give a status of where they are at and say, "Here's where we need to go to." It should be of interest to the audience.

Goldman: I see there's also one called "Student Presentations," although there's nothing listed yet.

Bath: Yes. The suggestion came during the Technical Program

Committee discussions, "Should we just open up a buzz session to universities or students who have an area of interest?" Maybe they're doing a six-month project or MS project and could come to the buzz session and present on this area. We're asking around for students who do work in electronics manufacturing if they might be willing to come and present. We would look to get an IPC emerging engineer to chair that session because we're trying to encourage students to participate in these kinds of events. That's the idea. We haven't got it dialed in, in terms of speakers yet, but we're looking. And because it's a presentation, it doesn't need to have a paper with it. In terms of getting this session done, it wouldn't be that hard. We've asked around a little bit and we're just waiting. As of now, it's just a place holder we have for student presentations.

Goldman: I hope that works out, because that could be very interesting.

Bath: It would be nice to have but if doesn't happen in 2018, we'll revisit that session for 2019. We're trying to encourage the students who wouldn't get the opportunity to present in a technical session to use this session, and get them involved a little bit more. That would be good for them and for the industry.

For other buzz sessions, you've got the typical ones: the pulse of the industry, China/environmental issues, and new areas such as e-textiles. This is a developing standards group; this is what we're doing and some of the questions/areas around that. Where are we in terms of standards development? Buzz sessions can be kickoffs to discussions on where the industry should go.

Buzz session seven is on the the PCQR squared database. What are the updates? Then, the pulse of the electronics and the business outlook with roadmaps and things, and where we're going. Buzz session 11 is something that we got from Brooke Sandy-Smith at Indium Corp. on IPC J-STD 001 standard and the ROSE testing requirements in the standard being discontinued. What are we going to do? Let's have a panel discussion on this. This was from a user. Someone out there saying, "We would like to have this." Then we checked within IPC and there were people in the industry who were willing to be on the panel for this. We don't have to go out and pull people. They want to be involved. We just ask them and they say, "Yes, sign me up." This is an ongoing issue. This is something they've got to deal with, so you'll get feedback in the

industry on where we are and the status of the emerging methods to reach the level of industry standardization. What should we be doing? We're trying to get these types of discussions moving in the industry.

Goldman: Let's talk about the professional development courses, the PDs, of which I see there are 30 being offered. They're usually about half a day, right?

Bath: Yes, there are 30 half-day sessions, with classes on things like non-contact/jet dispensing and other focused technologies. They can encompass what we currently know about a subject, and things on the horizon. As we get into more and more miniaturization, we learn about new technologies and people need to know where the state-of-the-art is. This is going to cater to that, which we hope will be of use. We believe it will be.

There are the regular courses too, like the design analysis courses. I think quite a lot of them have been around before, but there are updates from each of the authors on those. We're trying to make sure we cover all the

bases. We cover the ESD program. It's not something that maybe has a massive audience, but it's something that we think could be of use. We've got design for testability and boundary scan.

There's something for everybody here. We've got the cleaning and coating. We have a couple of sessions on reliability from Dock Brown of DfR, discussing physics of failure. Let's give the audience something that they don't normally get when they come to the technical sessions with a more in-depth discussion on certain areas. We have Jean-Paul Clech at EPSI who is will be presenting on reliability as well. We also have new developments in selective soldering.

The rest of them cover areas including PCB fabrication, PCB assembly, and the issues in those areas. How do you troubleshoot? What are the defects? How do you do failure analysis? For engineers coming in, it covers people who maybe are developing engineers, trying to learn the ropes, and then some of the courses are more advanced for those who have been around in the industry and want to learn about developments in those areas. We're covering it in both ways as best we can. We're covering a wide range of topics from intermediate to advanced levels. We're saying, "Here's the booklet, pick and choose, however you want it." We think that these are the courses that would be of most interest to the audience.

Goldman: In the past, how well attended are the PD courses?

Bath: In recent years, we haven't had to cancel any PD course for lack of interest. I don't have the figures in front of me, but at minimum maybe 10-15 people, and at maximum maybe 100 attend a PD course. Typically, we're in the 20-40 range, but for some of these courses we're getting 60, 70, and more, which is a lot. We're not upset about the attendance whatsoever. These are the areas where there's a growing need, and we're happy to oblige.

Goldman: Any last thoughts from you, Jasbir?

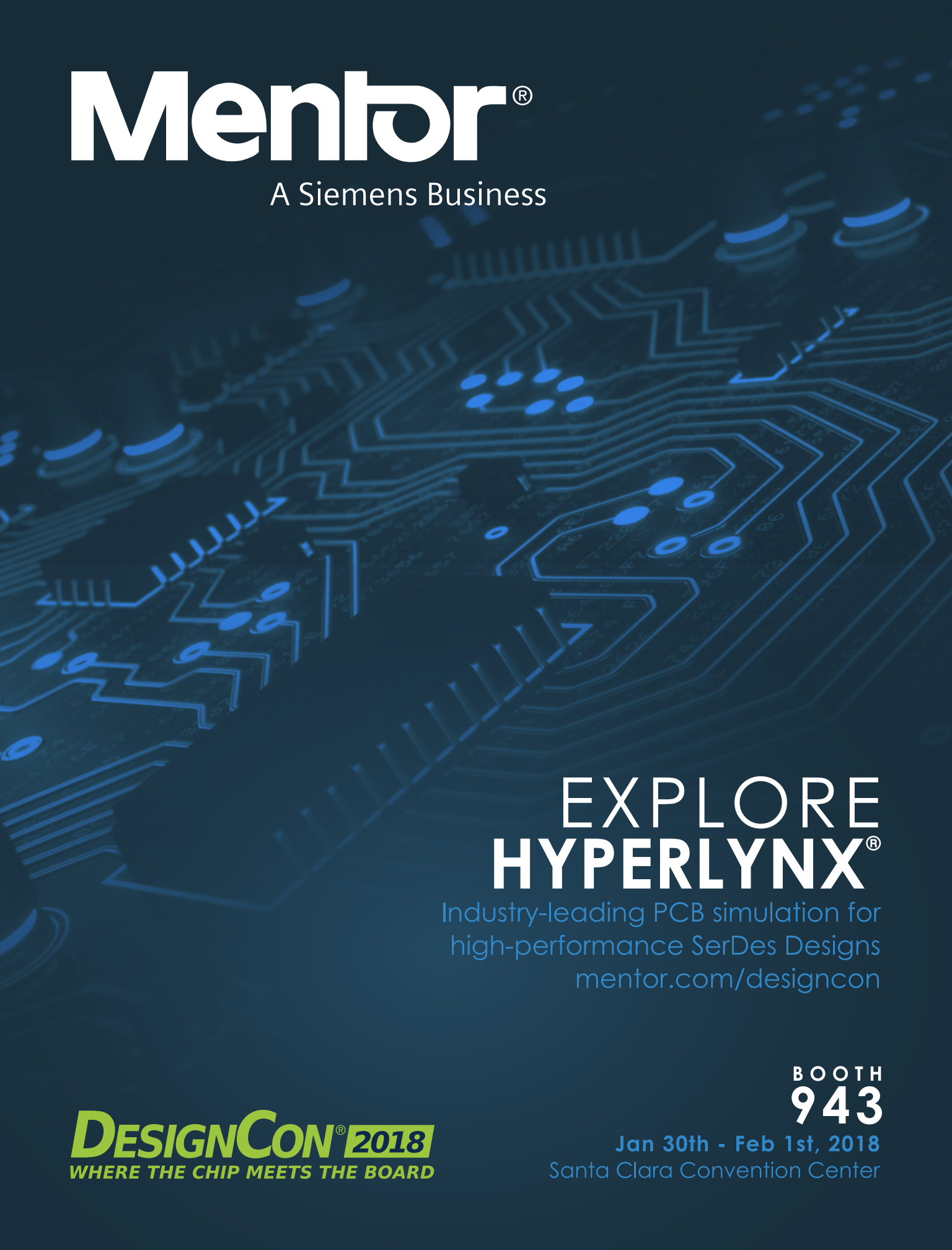
Bath: If you look at the entire technical program, you'll see different pieces that cover different areas. I look at it in terms of new developments, but also new defects or failures that people are working on. It's a nice overlap between the technical conference sessions, which give you the details of where we're going, and the PD courses, which may give you more training, and cover those aspects in more detail. The technical conference session could be on printing, but the PD printing course will cover three hours where the conference would be a half an hour, or an hour and a half. It's more in-depth. The buzz sessions are where the pulse is, the biggest issues and the emerging trends. We've got a nice balance in terms of how we do this. We've got the PD courses on the front end and on the back end, with the conference and the buzz sessions in the middle. With the exhibits on top of this and the standard committee meetings, I think it's a nice balance. It gives everybody a chance to pick and choose.

Goldman: If somebody really wants to get immersed in it, they certainly can and come home with a boatload of knowledge.

Bath: Exactly. You come in, pick and choose what you want, and you come out and hopefully apply what you learned to your work. That's how we want people to come in on Saturday and Sunday all the way through to the end of week. You have every opportunity to learn something everywhere you turn.

Goldman: Thanks so much for your time, Jasbir. We appreciate it. See you in February.

Bath: No problem. Thank you. DESIGN007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CFX: Updates and Developments


Nancy Jaster

Nancy Jaster is the manager of design process at IPC—and she has every right to be. As part of the technical staff team, she works directly with many IPC standards committees to support the industry, particularly those related to DFM and DFX guidelines, as well as those involved in data transfer. With 28 years' experience in the industry—10 years in manufacturing and 18 years in design—she understands clearly what people need on the factory floor.

In an interview with I-Connect007, she discusses the latest developments in the Connected Factory Initiative (CFX), the machine data interface standard that would enable manufacturers, equipment, device and software suppliers to achieve Industry 4.0 benefits, and CFX demos at IPC APEX EXPO 2018.

Stephen Las Marias: Nancy, what's the rationale behind the Connected Factory Initiative?

Nancy Jaster: I'm one of the fortunate ones in that I've got the experience in both design and manufacture. I already have the IPC-2581, which is the standard to get design data to manufacturers. The wonderful thing about 2581 is that it is intelligent data. It's no longer just a flat file. It's a model-based dataset where we can share much more information with the manufacturing floor than we ever have before because it's all bundled up in this one package.

IPC used to have CAMX, a standard for transmitting data on the shop floor. But it was tied to a message broker, which limited its usability. After talking to some of the machine vendors, my original thought was how we could take CAMX to the next level, and how do we get CAMX working with 2581? I realized that we had an issue there, and that we really needed to look at the shop floor like we looked at getting design data into manufacturing as an intelligent data model.

Data is key not only to the design process but the manufacturing process. We really need this overall data backbone to support the industry, and we want this data backbone to be smart, intelligent data. We want it to be on a standards base, so that if we're calling, say a fiducial the same thing in every standard that we have, then we can easily pass that information back and forth. We standardize how we describe it, and what it makes up from a data perspective, and then you can reuse that piece of information anywhere within the product realization process. It's critical for us to get to the standard understanding, the standard way of using data. It's critical for the industry to be looking forward, thinking about it from an intelligent data perspective. When I started in this industry, we got flat files and we got drawings, and then we would have to take those and parse those out. I actually did some machine programming on the shop floor for a while. You'd have to take that unintelligent data and put all that intelligence in there. Now, we have the ability to do that within the data.

CFX is taking that shop floor data and taking it to the next level, coming up with standard terms and definitions, and has a standard transport definition so the information

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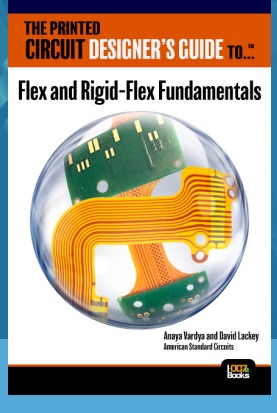

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can flow from machine to machine, no matter whose machine it is. When they get that data, they can then apply their internal algorithms, their secret sauce, shall we call it, so we're not infringing upon what the manufacturers are doing or what may make their piece of equipment special. It's just using that common

framework so we can transmit the data from machine to machine. As we gather information, like if you have a part and you must alter the placement slightly, we can seed that back upstream. You want this to be bidirectional data going back and forth, so we can learn from the shop floor and continually improve the manufacturing process.

Las Marias: Is CFX a replacement for the IPC-2541, or the CAMX, as you were mentioning earlier?

Jaster: It's kind of a replacement, but it's two-fold. One, the industry has moved ahead. When you think about how this industry started and how we used to do drawings on big drafting tables, and then photographing it down to the size we really wanted, to where we are today with data. The whole technology has changed and we're taking advantage of those advances. With the whole Internet of Things and Industry 4.0, people really want to start communicating more about the data. In the past, it's really been one way. You just keep it flowing through the factory. But we know there are so many things we can learn from the process, and we want to take that information and flow it back, not only in the manufacturing process but to design.

When I was in the development area, that was always a problem because we'd send it over to manufacturing and they may do something or tweak that data partially, not change the design, but they might adapt the data a little bit for their shop floor. Then that meant that information didn't necessarily get back into the design community. So, being able to have bi-directional data is going to move us forward. Not only can the shop floor understand what's going on in their machines and maybe tweak things a little here or there, or if they know this design in the past has had a problem, to change something to adapt to it. They can also feed information back to the design community as well because we've got this common set of terminology that we're using, so it'll be easy to transmit information back and forth.

Las Marias: How is CFX going to address all that?

Jaster: CFX is not related to any one tool. It is tool agnostic, so it is being done by the equipment manufacturers, the software vendors, and OEMs, all on the committee. We have a chair from each one of those areas to make sure that it's being looked at across the board, and that it's not one industry or one player trying to push their version of things. It is definitely a balanced committee with balanced leadership who are looking at this for the entire electronics industry.

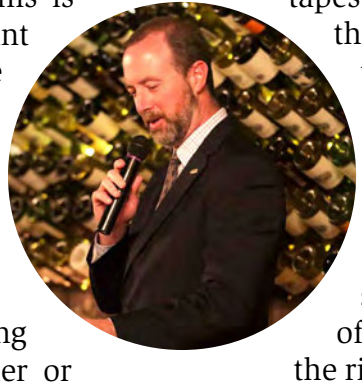
We have already agreed to a transport mechanism, and it's the AMQP 1.0 message queuing protocol. The team looked at a number of transport mechanisms, and the team decided that was the one that really had the most versatility and would serve us in the long run for this committee. Now, the next thing we're working on is standardizing the bits of information we need to share back and forth.

But instead of doing it machine by machine, like if you're a surface mount machine or an oven, we're instead doing it by function. We know that with pretty much every machine,

they've got an eye on that machine to make sure that they're looking at the fiducial. So, this is from 00, and everything is determined from this point. We know everybody has a camera that's looking for that, right? So, why reinvent that multiple times for each piece of equipment? That's going to be a building block.

We're creating all these building blocks that we can say, 'Oh, this piece of equipment needs a barcode reader. It reads barcodes, and it's looking for 00.' It's pulling those together, and now we can create the standard so that this is how we pull that information across from machine to machine. It's consistent across the board. If what we're calling a fiducial, then every piece of equipment's got to use that same terminology and the same criteria to describe that block. It's that commonality at a low level, at the right level, so we're not forcing people to tell them how necessarily to do things. So, what information needs to be portrayed? When I worked at Lucent, we used to talk about the 'whats' and the 'hows', and the whats are what you need to have at a lower level, so that you can standardize.

Everybody can agree to that, everybody knows that a product has an ID. We want to standardize on that ID and say, 'this is the ID.' Every board has the point zero, the starting place where we zero out from, so all my dimensions are from this point forward. Everybody agrees to that, so we're going to make sure that definition is the same across the board. By doing that, you can then build upon it, but you're still not inhibiting innovation on the software provider or the machine vendor to do things differently, or even the OEM. There's still an opportunity for them to make improvements or adjustments, or they can decide what information they want to maybe feed upstream to keep track of quality, production, or for whatever reason. It still allows everybody to do things differently when you get down to the 'hows.' How they do it, it may all vary, but if we're communicating the same language across the board, it's going to make life so much easier for everybody.



Las Marias: CFX aims to provide or enable true plug and play interoperability of the equipment, device, and the software.

Jaster: That is our goal.

Las Marias: So far, what have been the challenges in that aspect? We're dealing with a lot of vendors here.

Jaster: Yes, and somehow, I got lucky. I don't know what I did, but my vendor support has been great from day one. I think part of it was that I went into the very first meeting and said, 'This is for you. We want to do what is right for the industry. We've got no preconceived ideas. We want it to be not non-tool specific. It's not like you're going to have to go off and buy vendor A's product, or use a particular product.'

I think it helped because I do have manufacturing and design experience, and that helped me a bit in communicating to folks. Because I've been there, and I've actually had to run Mylar tapes to run sequencings machines for through-hole components and figure out what's the best way to lay-out and insert those parts on the board. Been there, done that, and I understand the complexities of the shop floor.

It's only gotten more and more so as the industry has evolved. Part of it was being in the right place at the right time. I had help from my chairs in pulling the right people into that room, and I cannot say enough about my three chairs: Jason Spera from Aegis Software, Mark Peo from Heller Industries Inc., and Mahi Duggirala from flex. The three of them are wonderful. They're open and they're willing to listen to all ideas. They're not there pushing an agenda.

Sometimes, we've had a meeting or two where people were kind of pushing an agenda,

and we basically said, 'No, stop it. IPC doesn't allow commercialization.' We don't want people pushing their own agendas when it's product specific or vendor specific. Some of that came up, and the wonderful thing is that a good, strong, solid team of people pushed back at the right points in time. I'm not saying it happened a lot. It really has been a very good group to work with. They're very interested. At first, there may have been a little skepticism. Could we really keep it generic enough that everybody could use this? But when we came up with the building block approach, people thought that was unique and a great idea, so let's go for it. Probably the biggest problem we have in all of standards committees is that they're made up of volunteers. Our volunteers have been great, a lot of them have given it plenty of time, but there just never seems to be enough time. You always wish you had a little more time with folks where you could maybe get a little bit farther, a little bit faster. So, you're always limited by people's time that they can commit to a project. But let me reiterate, IPC has great volunteers.

We are making great strides. We had our first meeting over in Germany at productronica. We've never done that before, but my colleague over there who runs some of the standards meetings, Andreas Ojalil, ran that meeting for me. We have a lot of our committee members over there, so they're continuing to work it. People are excited because they see where this is going, and they see that this is going to be machine to machine, it's generic, and you don't have to use a particular message broker. You're not tied to any one competitor's tools. It's going to give you what we need without forcing you to do something you don't want to do. You're not giving away the secret sauce, which is critical.

Las Marias: I think one big factor is the increasing trend towards Industry 4.0. This is a version of that when it comes to the factory floor in the electronics in the industry.

Jaster: And that was part of it, too. When we started, we said we wanted it to address Industry 4.0, and everybody in that room said, 'Well, what's the definition of Industry 4.0? Because everybody's got a different definition.' That's one of the things that this team said, 'For this team's perspective, this is what we mean by Industry 4.0, this is our interpretation, and this how we're going to address it.' People agreed, so it may not fit some other models, but it's going to work for the folks who the standard is intended for.

Las Marias: What about the legacy systems that are being used by manufacturers or electronic assemblers? Do they have to install new systems or equipment?

Jaster: They won't have to install new equipment. This is intended to work with all existing equipment, and it will, because it's at a high enough level that it will work. When it really is going to come into play is for the equipment manufacturers and the OEMs, and even the software providers. They now know if they work to this standard that it's going to be easier on implementation. With any standard, you don't have people going, 'Okay, we're going to cut it in tomorrow.' It doesn't happen that way.

It's like with a software update in the CAD world. A CAD vendor comes along with an update for their program. A company will decide when they want to implement that. They may implement it on new designs, where you still have to have things around for old

designs. With factories and producing products, even in the design community, most of our customers or our members are not consumer products. Consumer products you can do a lot of things and change over in a year, because you can change a whole product.

In the defense industry, the automotive electronics industry, we have a long-term approach to products because we must have long-term support. In telecommunications, my background, we always had to support the old as you move to the new. I believe going to the CFX standard will be a phased approach., At some point in time people on the factory floor may want to start implementing CFX even with some of their older equipment, or older programs, etc. But because it's a standard, it should be easy and adaptable to do. Once we get the tool kit available, which Aegis has just graciously signed over to IPC, we're going to put it on a public website so that people can go in and start working with it. I haven't seen it yet, but I am told it's very easy to program in this new environment using the AMQP 1.0, and it's going to be very simple for folks to make modifications and update things. Obviously, every factory and every machine vendor will have to determine when they want to start implementing this. But again, that's the wonderful thing about it being at the 'what' level, and not at the 'how' level. It allows that flexibility.

Now, what happens to the old standards? They're still going to be around. It'll take us a while before we say that we're not going to support them. We won't necessarily do any updates to them, but we don't necessarily say that you can't get the standard, because if somebody's currently using a particular standard and they want to buy a copy of it again, we can do so. You can't necessarily just throw it out just because you got something new. You always have to look back and make sure you can deal with legacy products.

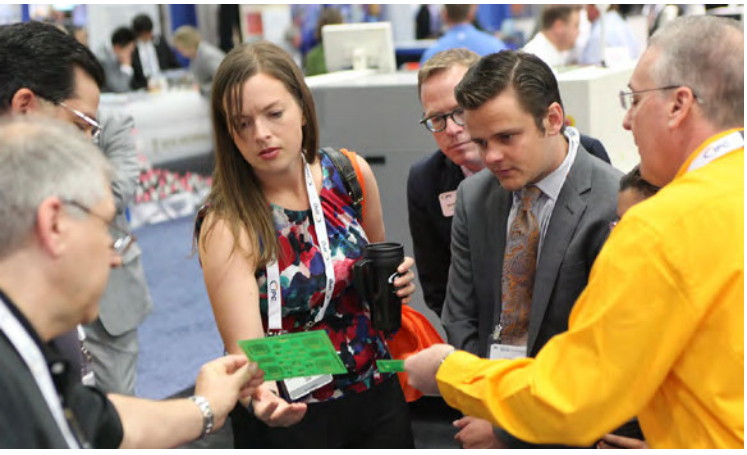
Las Marias: That's true, because a lot of manufacturers have already invested millions in them.

Jaster: Right. You always have repairs, you always have legacy issues, and you have old machines on the factory floor. My guess is, as people bring in new equipment, they'll start using the standard. They'll see how easy it is to develop and use, as well as transmit data back and forth. The bi-directional ability is going to be great. Then they may take on projects to update other programs on their floor, even for older equipment. It'll be easy enough to do moving forward, once they get used to using the new standard.

Las Marias: Right now, you have the software toolkit from Aegis, which is the CFX messaging library, and then the transport mechanism AMQP 1.0. Are there any other new developments with CFX?

Jaster: Right now, we're working on those building blocks and defining what those building blocks should be. The next step is getting those building blocks in place and getting the standard definitions there. Come APEX, we actually hope to be able to demonstrate on the show floor how simple and easy it is to use these building blocks to run the machines. I'm hoping we will have demonstrations there, but the key now is getting all those building blocks together and determining at what point we want to go ahead and actually publish the standard. It's just more work right now and getting those blocks built.

Las Marias: Apart from the demo, what should the industry expect at APEX regarding CFX?



Jaster: Well, hopefully the standard will be released next year. The standard will be released for the building blocks that we know of today, but as industry changes, we need to keep making sure that we are in tune with industry and continually look to make sure the standard stays up to date with where the industry is going.

I would love to see if we can integrate it into making sure that it's communicating well with the 2581 data. I really want to get this continuous backbone of data and expand it out. Right now, we're really focused on circuit assemblies. Can we expand this into printed wiring board assembly? I think we can, so is that the next phase we tackle? I don't know. We have a standard component traceability. We need to make sure that component traceability works well with the CFX standards so that we can make sure we're providing that information back. I'm also responsible for a number of standards related to material declarations for RoHS and REACH. I would like to get those standards connected in as well, so that they're all talking to one another. I want a set of standards to support a data backbone for the electronics industry.

As you know, when you're putting in data it is basic quality 101. Do it right the first time. If design inputs the data and it is correct, which it has to be, then it transfers automatically over to production. If they don't have to touch anything, not only do you speed up your process, you improve your quality, you have fewer errors, and you have less manual intervention. Now we don't have to worry about transmitting data from machine to machine because they can all talk to one another with CFX.

Then you worry about, how do you take this data, and move it even farther outward in through the thread? We really need this backbone of data to support manufacturing. Data has always been key, and we've gone from paper, to flat files, to somewhat intelligent files, to now extremely intelligent data, and we just need to take that and keep using the technology as it becomes available to us. The other part is making sure it's secure. You always have to make sure your data is secure.

Las Marias: The traceability, the standards, and then RoHS and REACH. They will be connected, but not really integrated into the CFX, right?

Jaster: Not yet. That's another phase. When the directives came out for RoHS, we needed things, and so standards were written. Now we're working on connecting the factory. My goal is someday to get them all talking to one another.

Las Marias: Do you think this will be able to somehow pave the way for something like the lights-out assembly factory?

Jaster: Not yet. Do I think robots are going to completely take over the factory? No, because people still add value. Will it get us to a point where you can engage your people to instead of doing busy work they are doing something of more value? Definitely. Instead of people having to manually do something over and over, or correct problems over and over, it's going to help improve the quality, improve the data, and then allow employees to spend time working on other activities and things that can help the overall manufacturing process. How can they improve the secret sauce, or what can they do differently within their factory, versus

other factories, to make their product better than somebody else's? It's going to take people away from doing that drudgery, like double checking and triple checking data all the time, into allowing for more innovation.

Las Marias: Moving forward, as new technology developments happen in the industry, how can others in the electronics assembly industry join in or contribute to the CFX?

Jaster: All they've got to do is call me, email me, talk to one of my chairs, or talk to another committee member. To participate on an IPC committee, you do not have to be an IPC member. Obviously, we would love everybody to be an IPC member, but you don't have to be. We take any and all volunteers. We are welcome to include people in the process. When this goes out for industry review, we want folks that maybe haven't been involved looking at the document and making sure that we haven't missed something. When I teach hardware methodology, I always have a section on why we need design reviews, or why you need to do a test plan review. People get so focused on what they're doing and think they've got everything covered, but you always want that fresh set of eyes to look at it to make sure that you didn't forget something.

Going out for industry review is going to be very critical on this document. I have nothing but the highest regard for this team. This team is doing an outstanding job. The comments we're going to get back are going to be for the little things we forgot, not the big things. I think the logic is strong. The way everybody on the team is approaching and looking at and agreeing to it, I know we're headed in the right direction. But you want to make sure that the little things aren't forgotten.

That's going to be where we're going to get some help, with the little tiny details. One screw used to screw up assemblies on the shop floor. Somebody forgot to add a screw to the drawing to put the faceplate on, and guess what? You can't ship product. It's the little things that can always trip you up. Again, I feel very strongly that we are totally in the right direction. This is going to be an outstanding standard that everybody's going to be able to use, but it's good to have reviews to make sure we're looking at all aspects of it.

Las Marias: Nancy, do you have anything that we haven't talked about that you would like to share?

Jaster: The one thing I just really want to stress is that it has been a pleasure working with this team. I think we will have a major impact on the industry when we finally get the work completed. The level of cooperation within the industry is just outstanding. I am extremely proud of this team and its leadership. It is a delight to go to the meetings, and they're just a great group of people that really want to do what's right for the industry.

I'm not saying that my other teams aren't great, because I love my teams, but to see the manufacturers, the equipment manufacturers, and the software guys all in the same room, and nobody's trying to protect turf, is just amazing. You have competitors in this room and yet they're all working together to do what is right for the industry. They're doing what they believe is right for the industry. When we get the standard completed it will make a significant impact on the industry, in a positive way.

Las Marias: That's true. That's also what we at I-Connect007 strive towards—to be good for the industry. Nancy, thank you very much for your time.

Jaster: Thank you. **DESIGN007**

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All the Details on IPC's Emerging Engineer Program

Teresa Rowe and Nancy Jaster, in charge of IPC's Emerging Engineer Program, explain to I-Connect007's Patty Goldman and Jonathan Zinski how this novel approach to attracting and supporting young people works.


Teresa Rowe

Patty Goldman: Teresa and Nancy, let's start by having you tell us a little about what each of you does at IPC.

Teresa Rowe: I am a senior director of assembly and standards technology. I work with a technical team, as a staff liaison to the industry preparing IPC standards. My focus is in the assembly area. I'm also one of the leads for the emerging engineer program that we're going to be discussing today.

Nancy Jaster: I am also in the technical department as a staff liaison. My focus is more on IPC's design standards, and I assist Teresa with the emerging engineers program.

Goldman: Teresa, can you please describe the emerging engineers program and fill us in on this IPC program?

Rowe: The emerging engineer program started about three years ago. At IPC APEX EXPO 2018, it will have reached its third year. It was developed out of a conversation we had about attracting the younger generation to join our standards activities and to be more interested in our efforts as a global association for the electronics industry. We are attempting to pair emerging engineers, or individuals, who are in the early part of their career in electronics with someone who has been part of a task group or subcommittee, and part of our standards development processes, for a longer period of time. We like to think of it as a way to bring the two generations together to introduce our older generation to the newer technologies and newer thoughts, but also for our emerging engineers to gain the knowledge and exposure that they need to develop their careers.

We started very small and we have grown the program; we have tried to tailor it each year to not only have our engineers grow in the program, but also to introduce them to more detailed projects as the years develop. Nancy came on board at the tail end of the first year.

Jaster: The program is to help these young people develop leadership skills as well, because it gives them an opportunity to explore other areas, and to understand everything about the association. We've had real success in having some of our mentors take our emerging engineers and make them co-chairs of teams, so they can start learning the leadership skills that they need. It's an excellent program for people who are new in the industry or who haven't been there very long to get some leadership ability, as well as learn more about IPC and the standards development process. It really helps IPC out because it gives us some fresher views…not that we don't love our members who have been with us for a long time, but it gets us some newer people involved and starts expanding things, so we can be ready for the future as well.

Goldman: How many engineers, or how many sets of mentors and engineers are there right now?

Rowe: We have two that will be in their third year with us, and we have three in their second year. We are now looking at our applicants for our first-year group starting in 2018. The interesting part of this is that for our second-year group we actually have a university student who is one of our emerging engineers. We were excited in our second year to bring an individual on board who is a student, as opposed to actually working in the industry at the current time. He has developed a real interest in IPC and he's taking on a larger role, too, with some activities that Nancy has been working on.

Goldman: You said you have applicants. How does that part work? Who applies and how do you determine who you accept?

Rowe: There is an application process. We ask applicants to complete a benefits and commitments paper or page, which is on our website for the emerging engineer program[1]. That explains the commitment for three years; as we both said, it is a three-year commitment for this program. We ask the individual to acknowledge that and for their supervisor, or the person they report to, to acknowledge that this is a three-year commitment on their part. We have had requests for additional information such as 'What do I do beyond the events?' for example. We've been able to work with each individual to understand their concerns as they're worried about that three-year time commitment. It does take that paper and it also takes a copy of their resumé. When that information comes to Nancy and me, we sit down together and review it to determine if that person meets the qualifications and requirements, and then we fill our slots accordingly.

We do have situations where organizations have asked for the person's mentor to be from their company, as well. We've been able to match those individuals up, where the mentor is someone who may be mentoring that individual at their company now. In other cases, it's someone from their organization, but maybe from a different site or a different location around the world. We've also had companies come to us and say, 'I have an emerging engineer candidate, and I would truly like to have someone mentor them who is not part of our organization to give them a broader knowledge base of other organizations and the way to rest of the world works.'

Jonathan Zinski: When you go through the application process, how many slots do you have to fill?

Rowe: We have been talking about five for our current year, plus a university student.

Goldman: I guess you need to have mentors, which I presume are mostly committee chairmen? Would that be accurate?

Jaster: We do have chairs that have been mentors, but the key is really that they're an active member on a committee. We want somebody who can work with the emerging engineer and direct them to the right standards committees that they may be interested and want to participate in. They don't necessarily have to be a chair, but it does have to be somebody who has been involved in the standards activities.

Rowe: Patty, we've seen TAEC lifetime members come forward and ask to be mentors.

Goldman: The mentors must have to make a three-year commitment too. What all is involved in that commitment?

Rowe: We certainly expect before the first meeting for our mentor and our emerging engineer to discuss the emerging engineer's interests. We encourage them to do that by teleconference, although email is fine. The emerging engineers discuss what their interests are, as far as professional development. In the first year, as they attend APEX EXPO, we require them to attend professional development courses and they have to attend standards committee meetings. They have to attend a series of other receptions and events. They have to acknowledge that they've attended all of these things. We ask them to keep notes. They do a report at the end of the event that shows us what they've done. The fun part is we ask them to take selfies when they meet individuals. We may send them off to meet someone, or a person that meets a certain set of criteria. We ask them to take a selfie and show us they've met the person and started to network and have a conversation. Then it's up to the mentor to follow up on activities for the remainder of that year.

Jaster: One of the things we have them do is go to the show floor. They have to meet with a number of exhibitors, because we want them to get down on the show floor and see all that equipment and talk to some of the vendors on the show floor. It's really an opportunity for them to start networking and understanding the benefit of being at IPC APEX EXPO and getting the most out of it, because we really encourage them to do all the activities that are available to them. They basically get a one-of-a-kind opportunity for three years and we encourage them to take as many of the classes as they can, and to go to as many of the activities as possible, so that they can not only learn, but network and really get a full feeling of what the show and conference is all about.

IPC's emerging engineers and their mentors.

Goldman: The commitment on the part of their company, presuming they're from a company, or university, is they have to get themselves to the meetings, to the show, and then IPC sponsors them for meetings and workshops. Is that correct?

Rowe: This is true for companies, yes. The commitment from the company is they have to get the emerging engineer to the show and sponsor their travel.

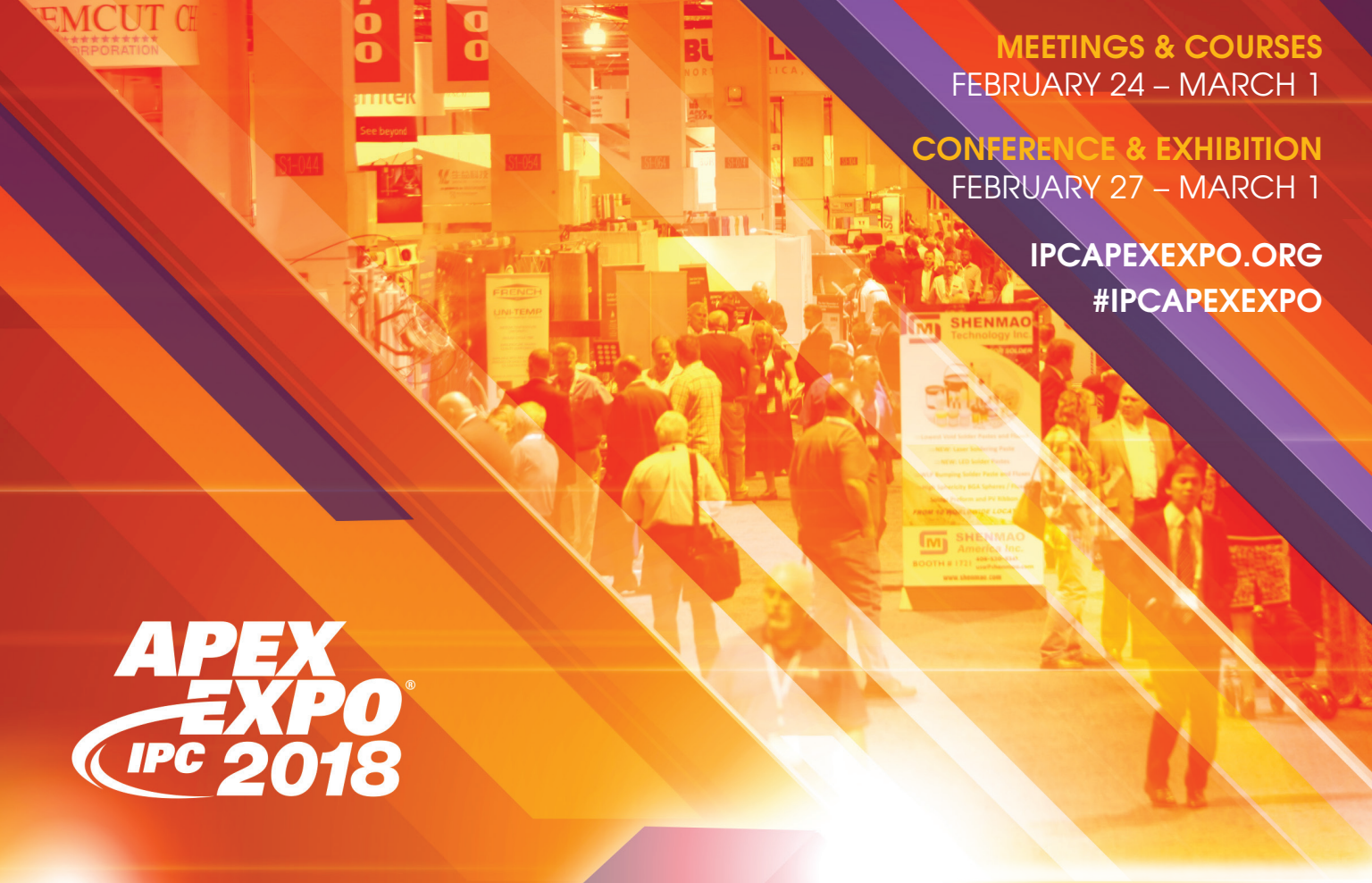
Goldman: I know there are a lot of workshops offered. Is there a requirement as to how many they should take each time, or is that open?

Jaster: The first year we said they have to take two classes.

Rowe: Then the second year we required one. We're now preparing our third-year activities. We'll be working on that. This will be our first group to reach three years.

Goldman: After this you'll see how well the first two participants, or emerging engineers, pick up on their own for next year.

Rowe: This is true. What we have noticed, to Nancy's point, is that one of our two emerging engineers has taken on a general vice chair position.



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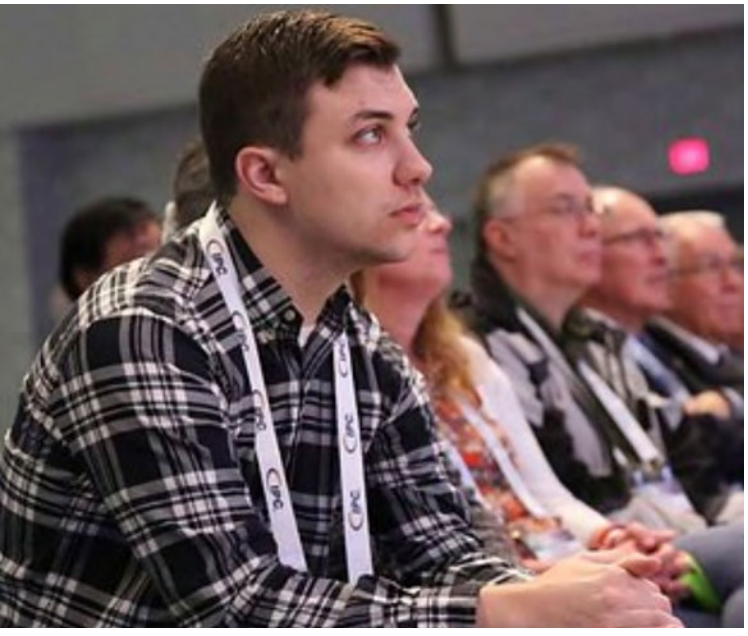

Jaster: Actually, two emerging engineers have become vice chairs.

Goldman: Fantastic. So they are delving into it. We all know how you can get really interested in this industry. Many of us kind of fell into it by chance, so it's nice that now we're making a concerted effort to bring people into the industry and not letting it happen just by chance.

Jaster: The nice thing is, because they do have the mentors, it's not like we're just saying, 'Here you go,' and they get overwhelmed by the size of APEX EXPO. They are getting some encouragement; they're getting direction from their mentors. I recall the first time I went to APEX EXPO—and I already had several years under my belt—it was almost overwhelming with the amount of choices of classes, technical sessions, and the show floor. Having somebody to help mentor them and help get them through that process and find the most benefit for them is very helpful. We owe a big thanks to our mentors for stepping up and doing that, as well.

Rowe: I second that. We have seen our mentors and our emerging engineers interacting off in a corner, or looking at the directory trying to determine where they were going. It is real-time event. It's not a mentor saying, 'I'm here to help you and you come find me.' The mentors are reaching out to the emerging engineers and really guiding them through those activities.

Goldman: They volunteered to be a mentor and so they've got a real interest, and that's good to hear.

Rowe: They've taken it to heart.

Jaster: What was really interesting last year, our second year, was watching the emerging engineers bond as well. The second-year ones kind of took the first-year engineers under their wings and tried to help them along. To me it's just been an overwhelming success at how well the folks that are involved in the program are enjoying it and taking advantage of all the opportunities that they have.

Goldman: I take it you expect to continue to expand the program?

Jaster: We do.

Rowe: As we mentioned, we have slots open for this year and we have a number of applicants. The deadline was December 15, for the 2018 class. I know that we have some individuals who've expressed interest and we're just waiting at this point in time for their paperwork to come in. We do have four that have already sent their applications in.

If someone applies, we don't automatically accept them into the program. We review the applications. We also have had individuals apply and asked to be waitlisted, just like you have a university situation with delayed admission. We've had a situation already where we were able to accommodate the individual because he couldn't attend the first year. He said, 'I'm interested in this program, I just can't come to APEX EXPO,' so we delayed his start until the following year. We do try to accom-

modate when we can, because we understand that this is a volunteer effort that their companies are allowing them to do.

Goldman: What feeling do the companies have regarding this?

Rowe: From my perspective, I don't think we'd have companies coming back and offering the second individual for the three-year program. We do have a company who has said, 'We have someone in their third year, and we'd like to have another person start this year.' We've had interest from companies that have taken the program to heart. Nancy and I talked about this just recently. They have embraced the idea of introducing these individuals to this activity. I've had feedback in another conversation from one of our mentors saying that the program has really helped the emerging engineer in that company to take on a bigger role. It's recognizing within the company that this is something that they've been selected to do and it was a choice, not only by their company, but by IPC. This is an opportunity to embrace for their career. This is my perspective from an assembly point of view. Nancy, I know you've had similar conversations with your design groups, correct?

Jaster: Yes. Again, the companies are really enthused to have people in this program. Our current emerging engineer, I don't think he's going to have any trouble whatsoever getting a job, because some of our mentor companies have already expressed an interest in him. It's giving him an opportunity to do things that he wouldn't have had the opportunity to do had this program not been there. He's already getting involved in industry and working on projects because he is an emerging engineer.

Goldman: Now, you've almost got a full slate for next year. How do people find out about this?

Rowe: Our marketing group has put out flyers on the program at various IPC events. We have posters that we post at our major events. We've also used tabletop tents in our standards committee meetings. We've done some visual information for them. We also have a webpage[1] on the IPC website.

Jaster: There's also usually a full page in our show directory as well.

Goldman: So if somebody doesn't go to the show or a standards committee meeting they might not find out about it? How does that work for university students? Just curious.

Rowe: We have spoken about the emerging engineer program at IPC Day and at some of the events on university campuses that we have attended in the past couple years.

Jaster: If you see me at any trade show, you know that I'm pretty blunt and ask young-looking people how long they have been in the industry. Then, I explain what the emerging engineer program is. I think some people wish I'd go away, but I'm out there talking all the time. I was at an event at PCB Carolina, at

North Carolina State, and there were a lot of students there. I definitely brought it up to all the students there. We're trying our best to get to the student community as well.

Goldman: Is there some place where you list the emerging engineers and their mentors, so that when people see them at the meetings and so forth the rest of us can speak to them?

Jaster: We do make them show up at the breakfast for the keynote speaker. Certain lunches we make sure we have them stand up and they get introduced along with their mentors. Wednesday evening, we have a meet-and-greet with the emerging engineers at APEX. That is one of the activities they are going to be highly encouraged to attend, so they can meet other committee members, or other IPC members. Again, they really bonded as a group, so there's no problem getting them together for opportunities like that. They like each other, which is a good thing.

Rowe: We've also put their photos on our Emerging Engineer program web page[1]. We don't have their names, but we do have their pictures that were taken at APEX EXPO 2017. We have special badge ribbons for them when they attend a meeting. Each emerging engineer gets a very unique, large pin. Patty, as you're aware, the TAEC members have pins, the Hall of Famers have pins, President's Award winners get pins, and they're a certain size. The emerging engineer pin is much larger and the mentor pin is unique as well. They are a pewter color, rather than gold. Each person is presented with one when they join the program, which they wear when participating in their events so that they can be identified.

Zinski: Are there any more specific requirements for people who are considering applying, other than being in the industry?

Rowe: We'd like for them to be interested in standards development, although we understand and we accept that at this stage in their career they may not understand what that means. This is a program for them to learn what IPC offers and an opportunity for them to be paired with someone who has been in the industry. Beyond being early in their career and having an interest in the electronics association or electronics in general, there aren't a whole lot of criteria that say they have to study this or that or whatever. Nothing like that.

Jaster: What's really been nice is we have folks that are more on the design side. We have other folks more on the manufacturing side and those who are interested more in the process-related type of standards rather than assembly standards. We've been lucky that we've gotten a nice array of people interested, not just all from one area.

Goldman: That's another good thing. Okay, I think we have covered just about everything here. Thanks so much for your time.

Rowe: Thank you very much. DESIGN007

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What to Expect at IPC APEX EXPO 2018: EXPO Veteran Alicia Balonek Shares

Alicia Balonek has seen it all. IPC's senior director of trade shows and events joined IPC during the dot-com bubble, and helped launch the first IPC APEX EXPO. Editors Andy Shaughnessy and Patty Goldman spoke with Alicia about IPC APEX EXPO 2018, what attendees can expect, and the organization's continuing efforts to attract talented young people to this industry.


Alicia Balonek

Andy Shaughnessy: Alicia, I didn't realize you've been doing this with IPC for 18 years. I'm sure you've seen a lot through the years—including substantial changes.

Alicia Balonek: Well, that's true. I started with IPC in 1999 and I was part of the launch of APEX in 2000, so this show is very dear to me and it was a great opportunity to be involved with a launch show. There's such a connection to the show, we've certainly experienced our fair share of ups and downs but for the most part it's been an extremely enjoyable experience through the years. There have been a lot of changes in the industry, especially on the board side, particularly in 2004 when IPC Printed Circuits Expo, a show produced by IPC since 1994, was co-located with APEX and IPC APEX EXPO was formed.

Every show is a new experience and we just seem to keep learning from that, and we do it for the industry. This is the largest event in North America for electronics manufacturing and it has been since its inception. Everything is under one roof, from one end of the manufacturing process to the very end of the process, and we're proud to be able to bring the industry together for this important event.

Shaughnessy: We're glad it's not in Anaheim anymore (laughing).

Balonek: Well, for a show this size, especially with the extensive electrical and plumbing requirements, there aren't many facilities throughout the country that can handle this event, especially with the long move-in time. We have almost two million pounds of freight on the show floor. It's a heavy equipment show, so not only does it take time to get that freight onto the show floor, we also must make sure that we're giving the exhibitors ample time to calibrate the machinery and their assembly lines so they're ready before the show begins.

Shaughnessy: I think everyone really likes San Diego. It's hard to have a bad time here.

Balonek: Especially when you're coming from the Midwest or the East Coast in February. Everybody enjoys that warm weather and it is a great facility. I've been in this industry for a long time and I've worked in many different convention centers, and we have great staff from the San Diego Convention Center working with us. I couldn't ask for a better team. They look forward to our show every year.

Patty Goldman: So what will be happening this year?

Balonek: Well, it's not necessarily new, but a favorite of the event, is the show floor reception on Tuesday evening which is a great gathering place for attendees to network with the exhibitors. We're introducing "Passport to Prizes" this year and we'll be giving away an iPad mini, Beats

headphones, Google Home, and lots of other useful and high-tech prizes. When attendees register they'll be given a little passport card which will have the exhibitor sponsor's booth number and name on it. They have to go to those specific booths throughout the show to get stickers from them; on Thursday, they must drop off the card at the IPC booth, where we'll announce the winners that afternoon.

Goldman: That's something new that should be fun.

Balonek: Especially with the younger audience that we're trying to attract to APEX EPXO. Of course, they come for the education, but there should be a fun aspect of it too. They've asked for more networking opportunities and just fun things to do on the show floor.

Shaughnessy: People like it when they can get a beer together at the show.

Balonek: Exactly. Our keynote speaker this year is Jared Cohen, the founder of Google Ideas and now he's with Jigsaw, the Alphabet arm. We're excited to bring him to the show, and he's equally excited to speak to this audience. I think his quote was, "Wow. This is perfect for me," when the invitation came across his desk.

Goldman: A nice technical audience.

Balonek: Yeah, and that's the one thing with the keynote speakers that we do try to recruit for this event—they love speaking to this audience because they can speak at the same level as them. For lack of a better term, they don't have to "dumb it down" for us. We get it. Mr, Cohen will present, "Game Changers: Technology and the Next Big Disruptions."

Shaughnessy: Yeah, it was great having Mayim Bialik last year. She was great discussing engineers versus scientists. That was funny.

Balonek: It was interesting the questions they were asking her. I always find that fascinating to see what kind of questions there are. I think my absolute favorite keynote speaker, though, was William Shatner.

Shaughnessy: Hard to beat that.

Balonek: I'm still trying.

Goldman: You've had some pretty good ones.

Balonek: Thank you. It's a hard industry to tap into. It's a very niche industry, so it's a long process of trying to figure out who would be the best fit. So, if you have any ideas, I'm always open to them.

Shaughnessy: I think it's good how you rotate. Instead of having all futurists or something, you kind of rotate and you even had a super famous guy like Shatner, but then the next year was Michio Kaku.

Balonek: That's an important thing when planning an event. You've got to keep it fresh every year so people keep coming back. One new initiative that we are doing this year is a STEM program for high school students, and that will take place on Thursday. We invited two high schools from Southern California that are involved in STEM programs. There's been a lot of talk in this industry about how to attract the younger employees for the industry. It's great to recruit at the college level, but

there's such an initiative for STEM now that we really need to start reaching out to people at the high school level before they even enter college so they can consider this industry as a career choice.

David Bergman, our vice president of standards and training is doing a cool presentation, "How to Make a Circuit Board out of Peanut Butter," for the students and then we'll take them on the show floor. Hopefully, after they see the peanut butter presentation, they'll see the equipment and the technology that makes the circuit boards and it will all come together for a better understanding of the industry. Then we have a lunch scheduled with a panel discussion with some industry leaders so they can ask questions about our industry. We hope that it will be well-received by the students and that we'll be able to recruit the next generation for this industry.

Shaughnessy: That's one of the things we constantly see: People are retiring. For some reason, especially in PCB design, there was a big flood of designers joining the industry in the '70s and '80s. We're seeing a few young people coming in, though.

Balonek: And that's good but we need to do more and that's where STEM comes in. STEM education is so important and it's nice to see schools offering these types of programs. My daughter is in middle school now and they refer to her program as STEAM in her school, she's involved in the program and goes to classes three times a week. They have afterschool workshops too, so it's a really good to start at even a younger level to start tapping into where our future engineers are coming from.

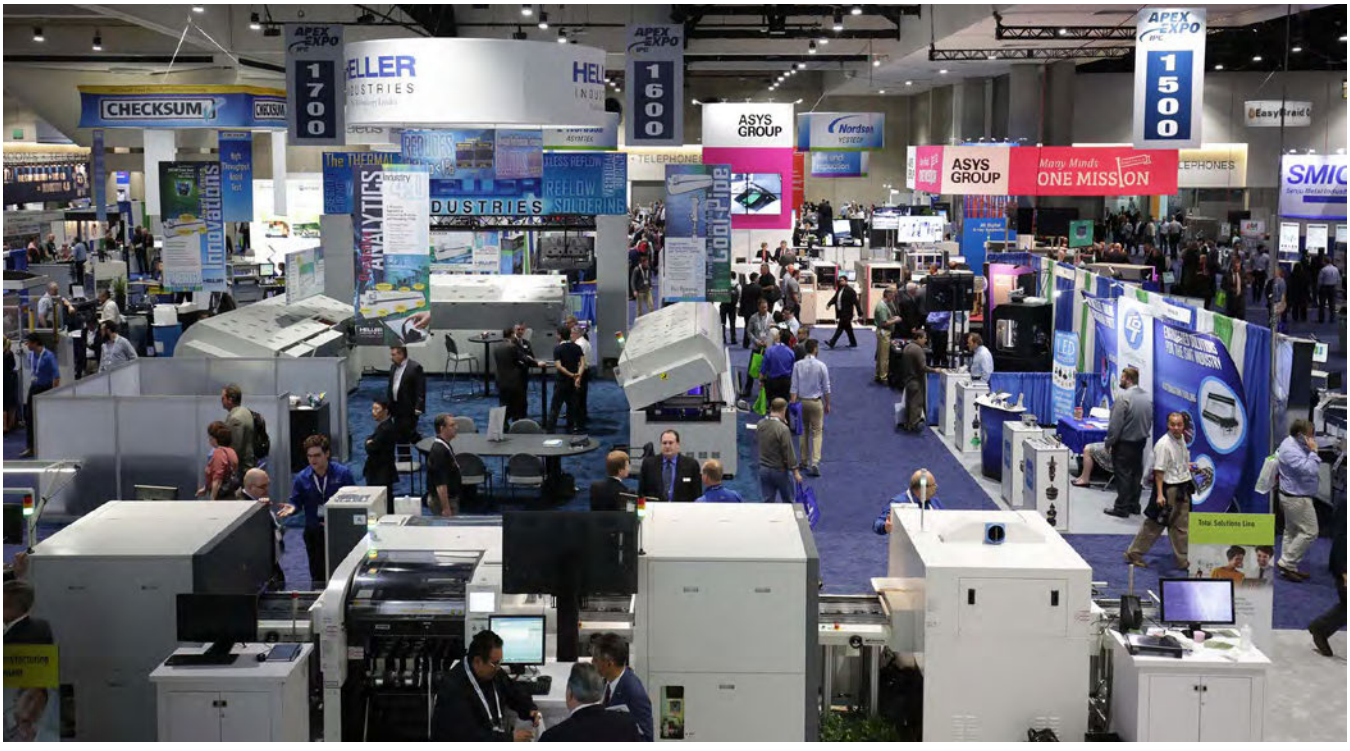
Goldman: Is your daughter finding the program interesting and intriguing?

Balonek: Oh, she absolutely loves it, and especially the part that includes making slime. I don't know if you guys have young kids, but they're making it all the time. I cannot tell you how many gallons of Elmer's Glue I have in my house right now. But even with these small experiments, they're exposing themselves to science which is beneficial for kids. But back to the STEM program at APEX EXPO, we're able to provide this program through sponsorships and I'd like to take a minute to recognize, ASM Assembly Systems, Mycronic Inc., Nordson and Panasonic Factory Solutions Company of America for sponsorships. In exchange, they'll be invited to the panel discussion and the students will be visiting their booths during a special tour of the show floor. We'll also be making a donation in their names to the STEM program for the participating schools.

Goldman: That sounds like a fantastic program. I guess the important thing is to make sure it's not a one-time thing, right?

Balonek: Right. It's a pilot program this year and we hope to be able to offer it again next year and maybe even doing things in different cities. I know a lot of our members have production plants within their facilities so we could do something in their cities if they don't have the time to coordinate a program themselves.

Goldman: We recently had our newest team members visit a PCB facility—they are editors, not really PCB people. They were absolutely astounded at what was involved in making the circuit boards, and of course they related it to



their cellphones: "Oh my gosh. Who knew all this stuff had to happen to make one?"

Balonek: Exactly. I had no idea before I joined IPC.

Shaughnessy: Where were you before you came to IPC, Alicia?

Balonek: I worked at a financial association in the banking industry, which was cool, though, because that was in the '90s, so you saw a lot of changes in banking with the ATM machines coming out, retail banking, gas stations and grocery stores. It was an exciting time there. It was right around the dotcom era too.

Shaughnessy: That was the good time.

Goldman: Not as exciting as circuit boards, though, right?

Balonek: You know what? The longer I'm at IPC, the more exciting it gets. I finally get it. It took me a long time to grasp this industry. It's exciting to see how engaged our members are too. That's what I like most about working at IPC.

Shaughnessy: Everybody you talk to in the industry will tell you about their job. They'll tell you how they love it, how they got into it. Everybody has some crazy path that led them to this industry.

Balonek: It's funny. Engineers are typically introverts until you start asking them about their work in this industry.

Goldman: Alicia, what else should our readers know about this year's show?

Balonek: I'd like to just share a few facts with you. Just the sheer buying power of our attendees that come to the show—many of them wait until they visit IPC APEX EXPO before they make their purchasing decisions for the year. In fact, through our attendee surveys, we know that 37% of our attendees indicate that they will be making a purchase within six months of the show. Then about 28% of our attendees actually make the final buying decisions for their companies, and 55% recommend or influence those buying decisions. We have the key decision-makers coming to this event.

Goldman: That's good. How about the size this year? How's that shaping up comparatively?

Balonek: We're expecting about 450 exhibitors in about 150,000 net square feet of space, and right now, the needle is pointing into the direction of selling out the show. We still have a lot to do, but that is our goal. As far as attendance-wise, we'll have total visitors of about 9,000, which encompasses about 4,600 attendees and about 4,400 booth personnel.

Shaughnessy: That's a lot of people. You do a good job just herding the cats and putting it all together.

Balonek: It's fun. We work so hard planning all year long, and, when I see it come together, I cry at every ribbon-cutting. I'm just so happy that all our plans went off without a hitch, although there are sometimes little bumps in the road. It's very fulfilling to me.

Goldman: I bet. Your baby gets born.

Balonek: Exactly.

Shaughnessy: I liked having the guitar players during the ribbon-cutting in Vegas. That was nice.

Balonek: Yeah, they were fun. My husband and I were on a trip in Vegas and we were at the Irish bar in Mandalay Bay, and that's how I found them. They were a lot of fun.

Goldman: Is that how you come up with your ideas, hmm?

Balonek: It's just amazing where you come up with ideas and what you're doing when you come up with those ideas. I also want to mention the First-Timers' Welcome Reception. We normally have a breakfast on Tuesday morning for them, but this year we're having a reception on Monday evening for the first-timers.

Goldman: You expect that to be a better time slot?

Balonek: I think it's a better time. Nobody really wants to get up for a 7:00 am breakfast meeting. And we will be holding the Women in Electronics reception on Wednesday evening.

Goldman: You have something every evening. Are those considered part of the show? Or are those separate?

Balonek: Yes. Those are free networking events and included in the exhibit hall only registration option.

Goldman: Well, we are looking forward to it. Especially after winter, we're always looking forward to San Diego. Thanks for talking with us today, Alicia.

Balonek: Thank you. DESIGN007

IPC APEX EXPO
App is Where It's At

In an interview with I-Connect007, IPC Exhibits Manager Kim DiCianni discusses the IPC APEX EXPO 2018 app and how this powerful tool will keep attendees on track. She also highlights its usefulness for exhibitors.


Kim DiCianni

Stephen Las Marias: Kim, can you please tell us more about yourself and your role at IPC?

Kim DiCianni: I am the exhibits manager at IPC. I handle all logistics, sales, operations, overall exhibitor tasks for the event as well as managing registration, the agenda planner, the app, and most things that have to do with exhibitors and attendees for IPC APEX EXPO. I've been with IPC for 12 years, and I've always worked on the show, so I've been growing with the event as IPC APEX EXPO evolves.

Las Marias: Please tell us about the app. When was it first created for the APEX show?

DiCianni: I started managing the APEX EXPO app in 2015. We created the app two years prior to that, but I don't know that it was as extensive or had the capabilities that it does now. It has come a long way from that first year.

Las Marias: How is the app helping the attendees?

DiCianni: The app provides everything that attendees could possibly want or need for the event, including being able to look up exhibitors by specific categories. If they're looking to focus on a specific category, not only can they see what exhibitors are tied to that, they can see related tech conference and PD sessions, and any event related to something they're interested in. App users could filter for "adhesives," and it will tell them what exhibitors are related to it, and what sessions might be of interest to them.

Basically, what happens is when an attendee registers, they select their demographics. Their demographics then go into our o line agenda planner, which feeds the app. It gives them suggestions of any exhibitor that would be of interest to them, any session we have, and attendees can add those things to their planner. If they add it to their schedule, they're able see what time something takes place or what exhibitor they might want to see. They can browse exhibitors by name and product categories that the exhibitor selected.

We have "What's on Now?" which shows anything that's going on at that moment or coming up soon. They can look at any speaker's profile. They can see a list of attendees, or someone that might be of interest for them to connect with, and they can request a connection to that person. We have the maps of the show floor and the meeting rooms area. Users can see virtually anything that we offer at the event right in the palm of their hand, and it's always the most up-to-date information.

We have the show directory on site as well, but, as you know, once something goes to print, if something changes, it's no longer up to date. The app is always up to date. If something gets canceled at the last minute, we can do push notifications letting people know, or if

it was replaced by something or if the speaker changes. For the Tuesday morning keynote at 9:00 a.m., we can send a push notification at 8:00 a.m. as a reminder.

Jonathan Zinski: I was looking at your app from last year, and it was very extensive. I liked how you had links to check out the local area and find restaurants.

DiCianni: Many people aren't familiar with San Diego, so it helps. The app has social media links so they can look at Facebook, LinkedIn, or anything IPC is putting out during and after the show. The app we have now is called the multi-year. We use Core-apps and have since 2015, so if you already have the app on your phone from a previous year, it'll automatically add the new show, but it keeps the apps from the previous show also. So, if you made notes last year on something, you can go back, look at your notes from last year, and see if it is going on again. You're able to go back and compare the app. It never goes away.

Las Marias: How popular was the app last year and the years before, in terms of downloads, and did the attendees find it useful? Do you have some sort of feedback mechanism that will gauge that?

DiCianni: Last year, about 20% of our attendees downloaded the app. It has increased each year since 2015, in terms of downloads and usage. Comparing 2016 to 2017, the number of people using speaker profiles, sessions, and exhibitors is growing as well as the overall use. I think every year we're seeing an increase in usage.

Zinski: Do you use analytics to see what features are being used the most and which aren't being explored as much?

DiCianni: I would say probably our largest hits are on the session views, exhibitor views and speaker views—they're all very high.

Zinski: What means are you using to advertise it? If I had seen it last year, I would have used it.

DiCianni: On the printed show directory that's given to all registrants the QR code is right on the front page of the directory. We had 8-1/2 x 11 signs across the registration counter with the QR code. It had a picture of a tablet, a phone with the logo and then the QR code to download it right there. On most of our directional signage throughout the hall upstairs in the meeting area we also had the QR code. I know we promoted it to exhibitors in newsletters, and it was promoted within the conference brochure last year that was sent to attendees in December.

Zinski: Is there a way in the app for users to leave feedback about features they'd like to see improved or that they'd like to see added?

DiCianni: Currently not in the app itself, we do not. We do send exhibitor and attendee surveys at the end of each show. I know on both the exhibitor and attendee surveys we do touch on usefulness of not only the app itself but the agenda planner and ask survey respondents to provide their ideas for suggested improvements.

Las Marias: Does the data on usage or functions and features being used by attendees help you decide what other features to include in the show next year?

DiCianni: Absolutely. For example, the app is confirming that people like to look at new products. We know speakers at a session might be important or the session itself or

certain products or new products. It helps when we see trends, what's important to attendees, what they're looking for, etc.

Zinski: You said the app is continually updating for each year, so if someone has last year's, and is interested, they could download it right now and it would update for the show?

DiCianni: The 2018 app is still being created and it has to go through the approval process from Apple, so that's where we're at right now is putting in the new graphics and getting it prepared for 2018. Before we can actually push it live, it has to go through an approval process. If you were to download it right now, you would be able to see '17, '16 and '15, and then as soon as '18 becomes available, it would come into the app as an update. It would tell you that you have an update for the app, and then '18 would become available.

Once a person registers, their information comes from our registration company, and it populates into the agenda planner. Then when the app goes live, basically everything in that agenda planner, all our sessions, everything comes into the app. We're in the process right now of actually finalizing the agenda planner itself. It should be done in the next week.

Zinski: I'm on Android, and I was looking on Google app store, and I saw two of your apps. One of them looked pretty old, and the other one was the recent one.

DiCianni: Yeah, prior to 2015, we used another company for the app, so that's probably the other one you're seeing, because I don't think they ever go away. We have requested for it to be removed, so I'll have to check that out. Another thing I wanted to mention is the operating platforms, because I know people worry about Apple having so many operating, the app is always up to date and will work with the operating systems as they update. So, there's never going to be an issue with that.

Zinski: That's good to know. It's frustrating when a phone pushes an update. Android was pushing out their latest operating system, and half my apps are just crashing because they're not ready.

DiCianni: Exactly, and that's something that is very important to us, and I have confirmed repeatedly that, no matter what updates these carriers are doing or what platform they're using, it will work with it.

Las Marias: Kim, is there a benefit to the exhibitors for using the app?

DiCianni: Yes, we offer a sponsorship opportunity for them. On last year's, we just had an IPC banner, but this year, we are offering that to exhibitors, and it would lead to their page. It could be a great promotional tool to get themselves out there.

Las Marias: Right, good exposure. Hopefully doing this preview will inform a lot of people way before the event, and come the actual event, they will know that they can download the app. Thank you very much for your time.

DiCianni: Thank you so much. **DESIGN007**

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IPC APEX EXPO Show Coverage Magazine

Special coverage of the IPC Awards and Hall of Fame Inductees

Exclusive attendee and expert Q&A with designers, fabricators, and assemblers

Our columnists put the show into perspective

Our cameras take you to the show floor and beyond

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PCB007 Highlights

One World, One Industry: Connecting the Dots Between Manufacturing and Community ▶

Across the United States, the first Friday in October represents the annual celebration of Manufacturing Day. On this date, manufacturers and supporters come together to celebrate the longevity and success of our industry. Since 2012, Manufacturing Day has served as a chance to learn about the businesses that thrive in our communities and contribute greatly to the economy.

American Standard Circuits Wins 2017 Innovator of the Year Award ▶

Anaya Vardya, CEO of American Standard Circuits, announced that his company was awarded the city of West Chicago's Brilliance in Business Award for Outstanding Achievement in Design and Innovation at the annual ceremony on Monday, December 4.

Papandrew Leads Advanced Circuits' New Offshore Division ▶

Advanced Circuits is one of the largest PCB manufacturers in the United States. Now, the company is expanding the range of its services with the launch of its new Offshore Division. Recently, the company hired PCB veteran Greg Papandrew to lead the new division and help the company meet buyers' demand for offshore PCB sourcing.

Strategies for High-Density PCBs ▶

As hand-held and portable electronic products and their circuit boards continue to shrink in size, the designer is faced with solving the physical differences between traditional printed board fabrication and what's commonly referred to as high-density interconnect (HDI) processing.

FlexFactor: Faith in the Future ▶

Take just a minute and read through this list of new product ideas. Can you identify the common thread? Yes, they are all enabled by advanced technology, but would you believe that these products were all pitched in the last year by high school students?

TTM Technologies to Acquire Anaren ▶

TTM Technologies Inc. has agreed to acquire Anaren Inc. for approximately $775 million in cash from affiliates of Veritas Capital.

It's Only Common Sense: The All-Important Intense Customer Survey ▶

Whether you are in the business of board fabrication or board assembly, the fact is that you are not building your own products. You are building your customers' products, which means that you are in the business of helping your customers be successful.

HDI: Today, Tomorrow and the Future ▶

For the November issue of *The PCB Magazine,* our editorial team interviewed some of the top HDI experts in the PCB supply chain. Joining us on the conference call were Steve Bird, PCB/flex technology manager at Finisar, and Tony Torres of APCT.

All Flex Introduces Automated Online System for Custom Flat Flex Cables ▶

All Flex, a manufacturer of flexible printed circuit boards and flexible heaters, has announced the addition of an automated tool for ordering customized polyimide flat flex cables (FFC).

Ground Bounce

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

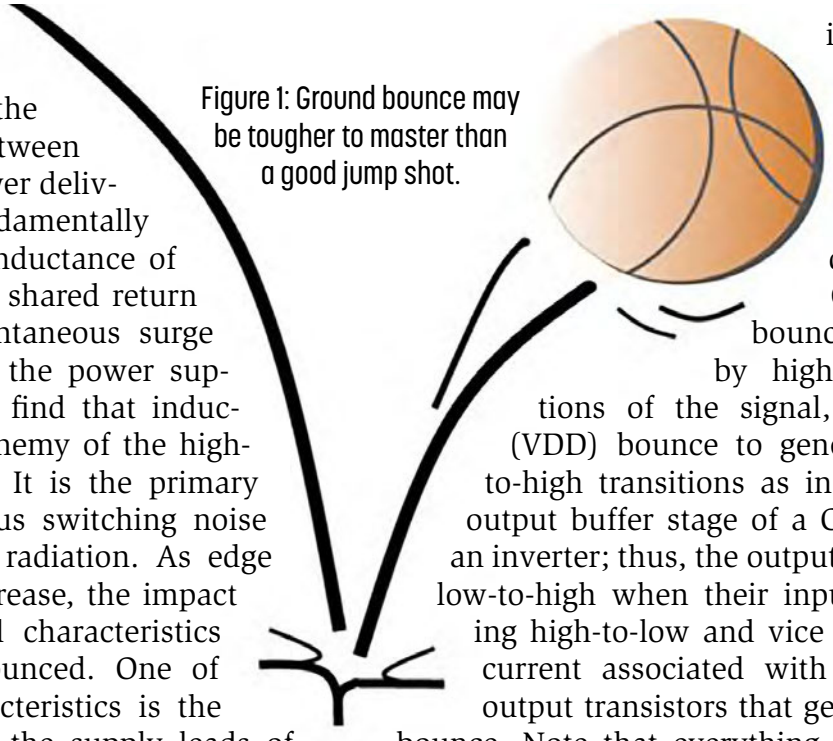

Figure 1: Ground bounce may be tougher to master than a good jump shot.

Ground bounce, or more precisely, supply bounce, is the voltage produced between two points in the power delivery path. It is fundamentally related to the total inductance of the current path and shared return paths and the instantaneous surge current delivered by the power supply. Once again, we find that inductance is the covert enemy of the high-speed PCB designer. It is the primary cause of simultaneous switching noise and electromagnetic radiation. As edge rates continue to increase, the impact of intrinsic electrical characteristics become more pronounced. One of these inherent characteristics is the inductance found in the supply leads of all ICs. In this month's column, I will look at supply bounce and how to minimise the impact on high-speed digital circuits.

Ground bounce arises from a common-mode potetial developed between an IC die substrate and the PCB ground return plane and is totally independent of the transmission line characteristics. The physical location of the device driver within the IC as well as the number of outputs that are simultaneously switched, with respect to the common power and ground connections to the die, also has an impact. In addition, ground bounce is associated with the dI/dt (change in current over time) of the output which depends on the switching speed of the driver gate.

Ground (GND) bounce is generated by high-to-low transitions of the signal, whilst power (VDD) bounce to generated by low-to-high transitions as in Figure 2. The output buffer stage of a CMOS device is an inverter; thus, the outputs are switching low-to-high when their inputs are switching high-to-low and vice versa. It is the current associated with switching the output transistors that generates ground bounce. Note that everything discussed here concerning ground bounce can equally be applied to the opposite effect: VDD bounce.

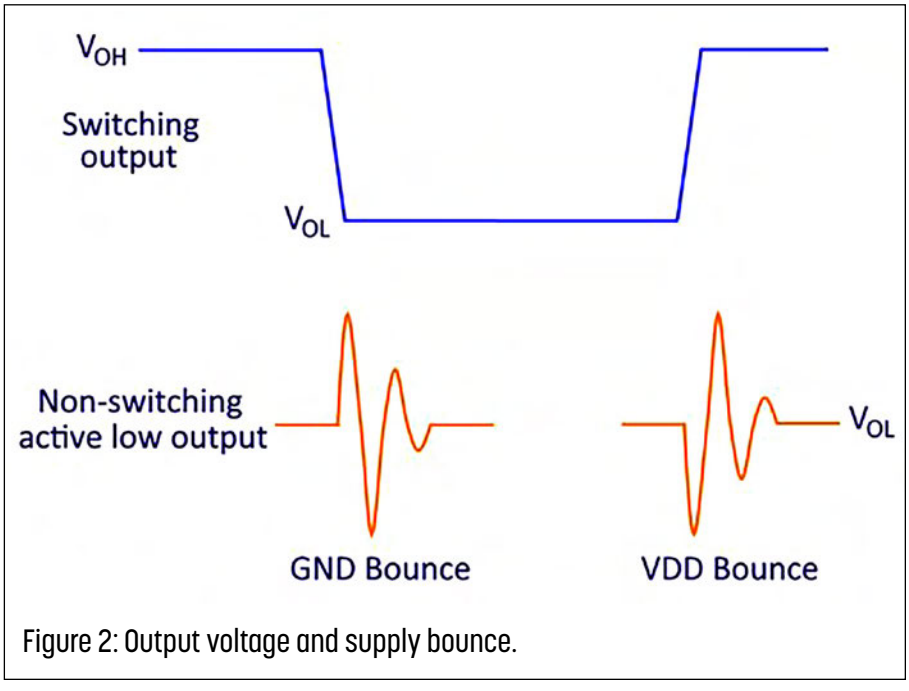

Figure 2: Output voltage and supply bounce.

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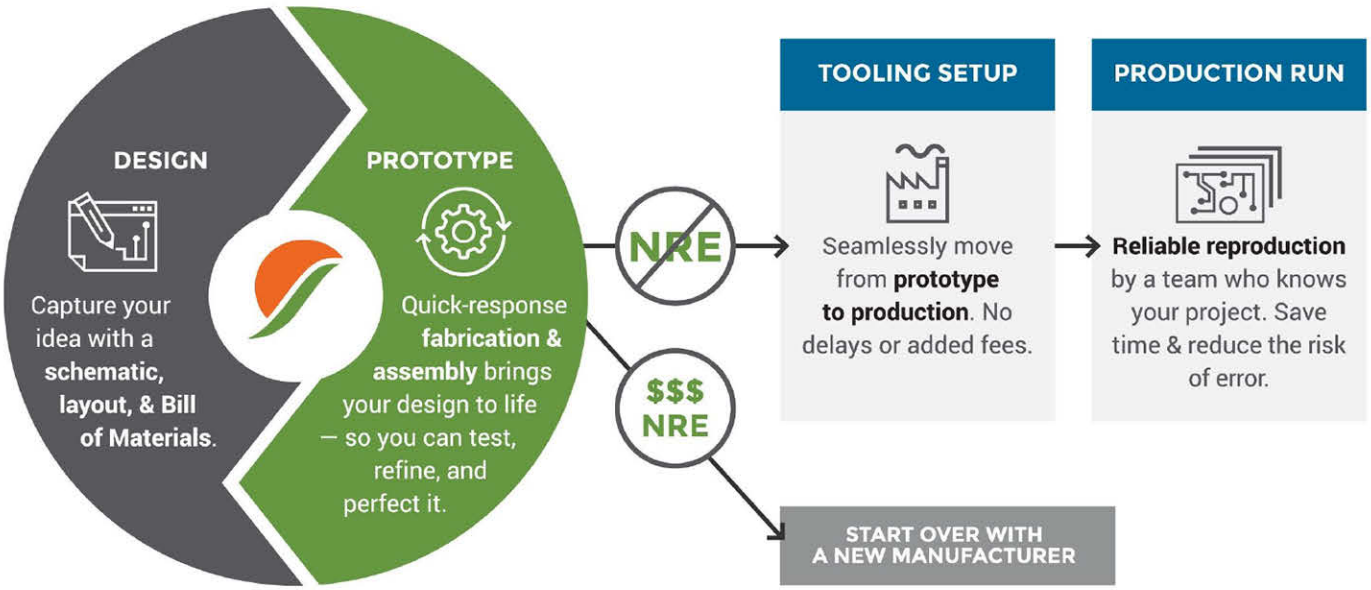

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When supply bounce occurs, the charge that is impressed across the power delivery path results in common-mode voltage. Unfortunately, it is not possible to eliminate the transfer of charge between logic transitions but the magnitude of the radiated peaks can be limited by providing a very low AC impedance path between power and ground. This is why power distribution network (PDN) planning is so important. The AC impedance of the power planes must be maintained below the target impedance up to the maximum bandwidth.

The measured supply bounce is generally very small (typically 150mV) compared to the full rail voltage swing of the output signal. So, its presence does not impact on the transmitted signal. However, it does interfere with the reception of the signal at the load, depending on the noise margin, and can cause double clocking. This is because a TTL receiver compares the input voltage against the local 0V ground reference plane. CMOS devices compare the input voltage to the weighted average of the VDD and GND while ECL compares it to VDD. Although the topology is different between logic families, the concept of supply bounce is the same. If N outputs are simultaneously switched, then there is N times as much current and therefore the supply bounce pulse is N times larger.

Figure 3 depicts the simplistic view of how supply bounce is generated. When the input to the driver transistor (right) goes high, the output goes low (V_{OL}), and a surge of current is pulled through the output ball of the BGA package from the capacitive load. This current flows through inductor L_{GND}, representing the matrix of ground balls beneath the BGA package, causing a voltage glitch on the IC die substrate. There are typically multiple GND and VDD pads, on the BGA package, so that the parallel combination reduces the overall inductance of L_{GND} and L_{VDD}, respectively. The victim, non-switching output (left), remains active low. However, the voltage glitch, on the substrate, is coupled into the output, and is transmitted out of the pin.

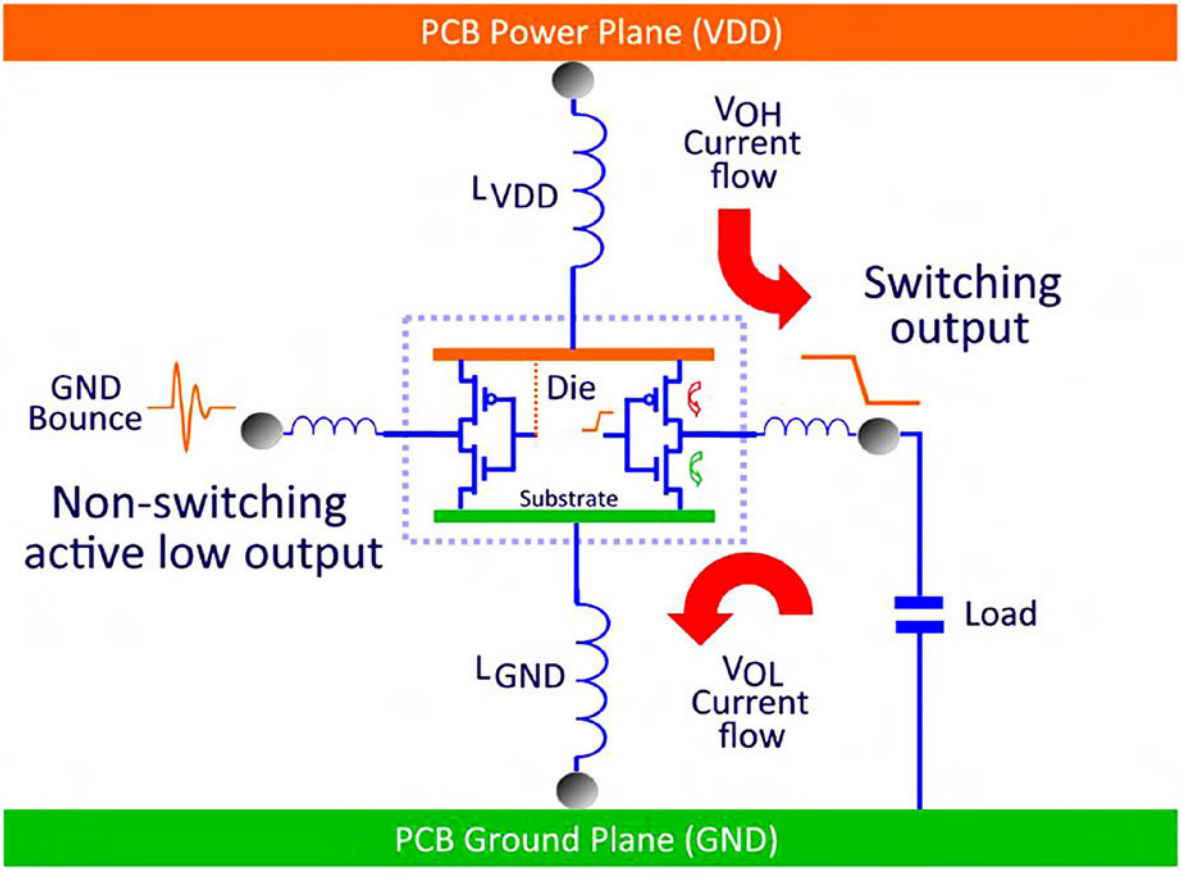

Figure 3: Generation of supply bounce in a BGA package.


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There may be hundreds of such outputs on an IC, which all simultaneously impart switching noise onto the planes. The opposite applies to VDD bounce; when the output switch pulls the output voltage high (V_{OH}), the current surges through L_{VDD} to the load.

Supply bounce gets worse as a result of the following conditions due to the increased current drawn from the PDN:

1. Capacitive load increases
2. Load resistance decreases
3. Lead and trace inductance increases
4. Multiple gates switch simultaneously

At high-speeds, the lead inductance of an IC package is critical. Larger packages tend to have more lead inductance. Wire bond, tape automated bonding (TAB) and flip-chip IC packages dramatically reduce the internal inductance by shortening the supply lead connections between the IC die substrate and the PCB planes.

Fortunately for PCB designers, there are a number of approaches that can be implemented, particularly during layout and routing of the PCB, to minimize the voltage drop, hence supply bounce, in the power delivery path:

1. Decrease the rate of change in the loop. Where possible, slow down the edge rates by employing series terminations. Also, some ICs now have clock skew adjustment to slow down the edge rate in addition to on-die terminations which are used to alleviate the need for external terminations.

2. Decrease the total loop inductance of the return path. Make the return path as short and wide as possible.

3. Bring the signal and return path closer together. This increases coupling and ensures that the return path follows the signal with a minimum loop area.

4. Limit the number of signals that share the same return path. A separate ground and VDD connection should be provide for each IC pin, directly connected to the ground or power plane, during the fanout routing of the package. Connecting two or more pins together, and then routing them through the same trace to a common grounding via, defeats the purpose of multiple ground and power pins.

5. Minimize the inductance of the planes during layout by using wide plane pours rather than thick traces.

6. Use thin (<5mil) dielectric core materials between the power and ground planes. Or better still, use embedded planar capacitance to provide additional low inductance decoupling to the IC.

7. Optimize the power distribution network by analyzing the decoupling requirements across the entire frequency bandwidth. Low AC Impedance reduces radiation.

8. Locate power and ground vias adjacent to each other, where possible, so that the magnetic flux is cancelled which minimizes common-mode currents.

9. Preferably, select IC packages that have a large central grounding pad under the package and connect it using multiple vias to reduce the inductance to ground. Also, select a package that has a high ratio of ground and power pins compared to signal pins. BGAs generally provide this but other SMT packages have limited supply pins.

10. Choose an IC with the lowest drive current output that will provide the required performance. This reduces the amount of current available to rapidly charge the system capacitance, directly reducing ground bounce.

11. Stagger the timing of output pins on a device. Spreading the switching time of many outputs over an extended period can substantially reduce ground bounce at the IC level.

12. Use differential signaling and avoid common-mode currents. Differential-mode is converted to common-mode at any imbalance in the pair. So it is best to correct any disparity as soon as it occurs by adding extra length, hence delay.

Supply bounce cannot be eliminated and problems occur when its combined amplitude becomes excessive. However, low inductance and low AC impedance of the power distribu-

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tion network reduce the impact of simultaneous switching noise and electromagnetic radiation in high-speed digital PCB designs.

Key Points

- Supply bounce is fundamentally related to the total inductance of the current path or shared return paths. It is the primary cause of simultaneous switching noise and electromagnetic radiation.
- When supply bounce occurs, the charge that is impressed across the power delivery path results in common-mode voltage. It is this common-mode voltage that creates electromagnetic emissions.
- The magnitude of the radiated peaks can be limited by providing a very low AC impedance path between power and ground.
- Supply bounce interferes with the reception of the signal at the load, depending on the noise margin, and can cause double clocking.
- Supply bounce gets worse as the result of increased lead inductance, capacitive load and simultaneously switching outputs. It also deteriorates with reduced resistive load.
- At high-speeds, the lead inductance of an IC package is critical. Larger packages tend to have more lead inductance.
- A number of approaches can be implemented during layout and routing of the PCB to minimize the voltage drop, hence supply bounce, in the power delivery path.

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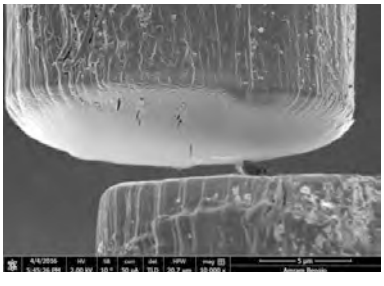
1. Barry Olney's Beyond Design column, The Dumping Ground.
2. Understanding and Minimizing Ground Bounce, Fairchild Semiconductor.
3. EMC and the Printed Circuit Board, Mark Montrose.
4. Signal and Power Integrity – Simplified, Eric Bogatin.
5. High-Speed Digital Design, Howard Johnson.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN and CPW Planner. The software can be downloaded from www.icd.com.au. To contact Olney, or read past columns, click here.

Nanotube Fibers in a Jiffy

A method developed by the Rice lab of chemist Matteo Pasquali allows researchers to make short lengths of strong, conductive fibers from small samples of bulk nanotubes in about an hour. The work complements Pasquali's pioneering 2013 method to spin full spools of thread-like nanotube fibers for aerospace, automotive, medical and smart-clothing applications. The fibers look like cotton thread but perform like metal wires and carbon fibers.

It can take grams of material and weeks of effort to optimize the process of spinning continuous fibers, but the new method cuts that down to size, even if it does require a bit of hands-on processing.



Pasquali and lead author and graduate student Robby Headrick reported in Advanced Materials that aligning and twisting the hair-like fibers is fairly simple.

First, Headrick makes films. After dissolving a small amount of nanotubes in acid, he places the solution between two glass slides. Moving them quickly past each other applies shear force that prompts the billions of nanotubes within the solution to line up. Once the resulting films are deposited onto the glass, he peels off sections and rolls them up into fibers.

Pasquali said the process reproduces the high nanotube alignment and high packing density typical of fibers produced via spinning, but at a size sufficient for strength and conductivity tests.

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MilAero Highlights

Ventec Proudly Supports 'Skate for the 22' Foundation ▶

Ventec International Group is proud to support the "Skate for the 22" Eagles vs. Boston Bruins Alumni hockey game on December 17 at the Edge Sports Center in Bedford, Massachusetts.

DARPA's Software Defined Radio Hackfest Creates Solutions for Spectrum Challenges ▶

The DARPA Bay Area Software Defined Radio (SDR) Hackfest came to a close on Friday, November 17 at the NASA Ames Conference Center in Moffett Field, California.

Global Defense Spending Forecast to Reach $1.7T in 2018 ▶

Global defense expenditure is set to increase again in 2018 to reach its highest level since the end of the Cold War, according to the annual Jane's Defense Budgets Report released today by IHS Markit.

NASA to Test Advanced Space Wireless Network and Device for Returning Small Spacecraft to Earth ▶

NASA launched the Technology Educational Satellite, or TechEdSat-6, to the International Space Station on Orbital ATK's Cygnus spacecraft from NASA's Wallops Flight Facility in Virginia on November 12.

DARPA Digging for Ideas to Revolutionize Subterranean Mapping and Navigation ▶

Request for Information seeks concepts for novel systems and component technologies to disruptively augment military and civilian operations underground.

Lockheed Martin and NEC to Enhance Satellites, Space Travel with Artificial Intelligence ▶

Lockheed Martin and NEC Corporation today announced that Lockheed Martin will use NEC's System Invariant Analysis Technology (SIAT) in the space domain.

Eltek Reports Revenues of $7.7 Million in Q3 of 2017 ▶

Revenues for the third quarter of 2017 were $7.7 million, compared to $9.3 million in the third quarter of 2016 ($8.4 million excluding Kubatronik).

Drone Race: Human Versus Artificial Intelligence ▶

Drone racing is a high-speed sport demanding instinctive reflexes, but humans won't be the only competitors for long.

European Satellite Confirms General Relativity with Unprecedented Precision ▶

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Phase Change Materials:
A Practical Addition to Thermal Management Options

Sensible Design

by Jade Bridges, ELECTROLUBE

Over the past few months, I have been exploring the subject of thermal management materials and solutions: why we use them in the first place, what materials and methods are available to us, how we apply them, and what the limitations are of these materials, as we put them to the test in real world applications.

In these columns, you may have noticed more than a passing reference to a new generation of thermal management solutions, phase change materials, which offer many advantages over more traditional, non-curing thermal pastes, such as the achievement of minimal bond line thickness with improved stability and pump out resistance. Phase change materials are also attracting the attention of specialist electronics sectors such as the LED lighting industry, where they are increasingly becoming the product of choice for larger sized assemblies destined for exterior and heavy-duty interior LED lighting applications.

So, this month, I'm going to look more closely at phase change materials and I will cite some of the "FAQs" that our customer support teams field every day on the telephone, at exhibitions and when visiting customers' premises. I've selected five of the most common questions and hope the answers offer useful guidance for those readers who are keen to find out more about these innovative new thermal management products.

Can you please explain exactly what changes take place in the properties of phase change materials during their use?

A phase change material is designed to alter its state at the phase change temperature, meaning that it will transition from a solid material to a softer material above the phase change temperature. This allows the product to 'flow' into all the voids and small gaps that are present at an interface between two substrates, just like a paste would do on application, thus

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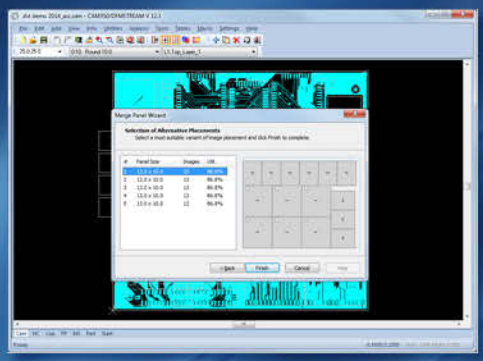

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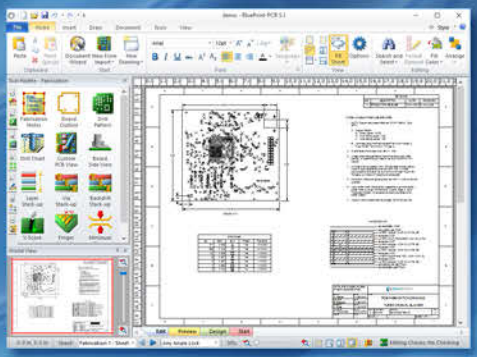

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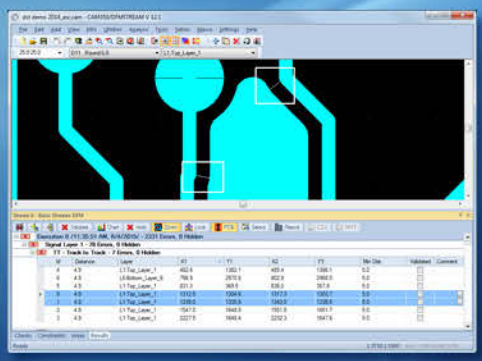

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allowing for minimal bond line thickness and minimal thermal resistance at that interface. From this it can be deduced that the best performance will only be achieved with a phase change material when it is used above its phase change temperature.

Are phase change materials restricted to a single method of application or are there more options?

There are, in fact, numerous options for applying phase change materials. Some products can be screen or stencil printed, so it is possible to apply a thin layer to many different substrates and unit designs. When considering which type of application is appropriate for a phase change material, it is essential to understand the temperatures that the device will be subjected to during operation. For example, while a device subjected to thermal cycling or operation at a continually stable temperature will dictate what type of thermal management product is likely to achieve the most efficient performance, with phase change materials there is the additional factor of the phase change temperature to consider. If the continuous operating temperature of the device is below the phase change temperature, the product will not perform at the level normally expected of it.

Why is the stability of a phase change product important?

Phase change materials provide greater stability than traditional thermal interface materials, such as thermal pastes. This is because most devices will go through some form of thermal cycle, even if it is just as simple as when the device is switched on and off.

When changes in temperature occur, all the materials in the unit will expand or contract to a certain degree, depending upon the temperature the device reaches in operation and, ultimately, the temperatures that the individual components reach. The coefficient of thermal expansion will vary from component to component due to the different materials from which they are made, so contraction and expansion can happen at different rates, and effects such as pump-out can occur as a result.

Pump-out happens at the interface where the mating substrates alter with the temperature changes, producing a shear type action at the surface that can lead to changes in the rheology of the interface material and movement of the thermal product from its original application position. Phase change materials alter their state above and below the phase-change temperature, so they can resist the effects of pump-out and remain more stable over many thermal cycles.

Are there other, more traditional thermal management solutions that feature a high level of stability?

Companies have introduced some novel products that offer the benefits of traditional thermal management solutions while combining the stability required for high thermal cycling applications. These offer a surface cure only and can be easily removed if any rework is required. Other traditional products that provide a complete cure while also featuring a high level of stability include single-part silicones or two-part epoxies, for example. However, with these products, rework is much more difficult, and they are unlikely to achieve the low thermal resistance of a traditional thermal paste.

Why would you select a phase change material over a more traditional thermal solution?

A phase change material is chosen mainly for its stability coupled with its ability to maintain a low thermal resistance. As noted above, there are other options that offer good stability in changing thermal conditions, but few provide as good a compromise as phase change materials with regards to balancing these two desirable properties. As with all new projects and applications, it is advisable to get some expert advice before you settle on any material or solution and then test it thoroughly before you commit. **DESIGN007**

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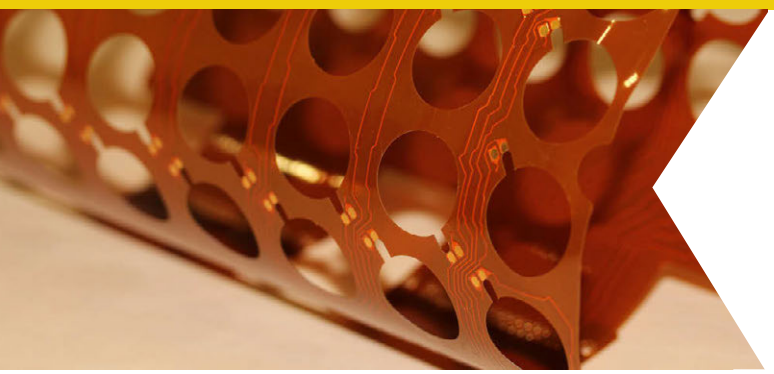

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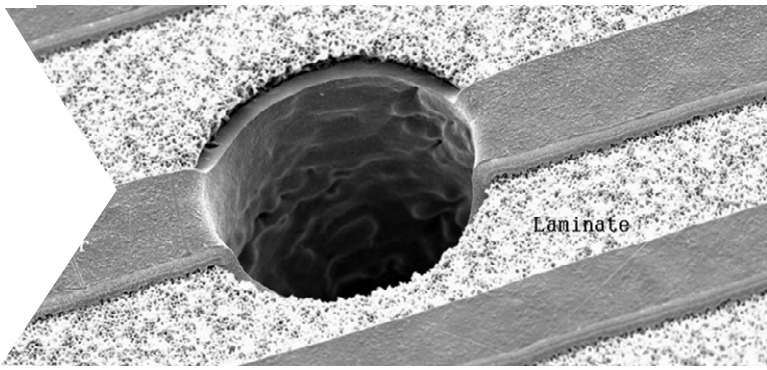

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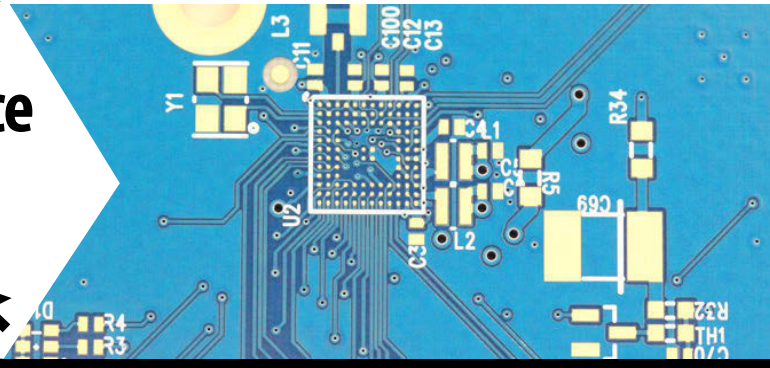

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Good Support Isn't Just for Customers

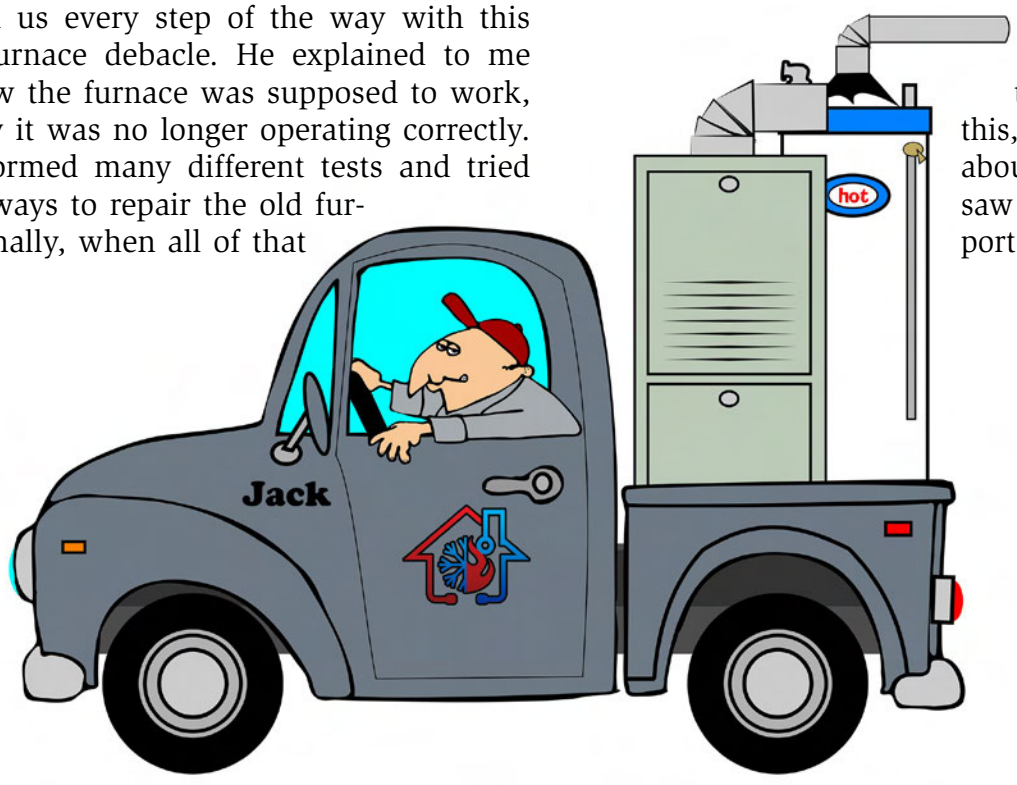
Tim's Takeaways

by Tim Haag, CONSULTANT

It is with great sadness that my wife and I are saying goodbye to a dear member of our family, but don't run for your Kleenex just yet. The dearly departed is not a person or a pet, instead it is our old furnace that has finally kicked the bucket. In fact, by the time you read this, we will have already been basking in the warm glow of a new furnace for over a month. Although I am not very happy about having to spend the money for this new mega toaster, and I am unhappier about having to wear a winter jacket while writing this, there has been one good thing about this whole frigid adventure. With the furnace on the fritz, I had the opportunity to work with a wonderful gentleman who has been helping us through this.

This man, let's call him Jack, has been working with us every step of the way with this whole furnace debacle. He explained to me fully how the furnace was supposed to work, and why it was no longer operating correctly. He performed many different tests and tried several ways to repair the old furnace. Finally, when all of that didn't correct the problem, Jack gave us some expert advice as to which type of new furnace would be best for our needs and connected me with the proper folks to install it for us. I can honestly say that I know more about furnaces now than I have ever known before, and I was completely comfortable with the final decision to replace the heater after knowing that we had done everything that we could to get the old one to work again. After all, some things just can't be fixed and need to be replaced. To quote the movie *Frozen*, "Let it go, let it go…"

I have been working in PCB CAD tools customer support for years and years, and it isn't that often that the tables are turned and I have someone who is supporting me. I've got to say, it was a pleasure being the recipient of some quality support. I learned a lot from Jack through all of this, and not just about furnaces. I saw customer support being modeled



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by someone who I consider to be an expert in the subject even though I know that he would never think of himself in that manner.

I have said in this column before that all of us are in the customer support game, even if we aren't actively supporting our company's customers.

I have said in this column before that all of us are in the customer support game, even if we aren't actively supporting our company's customers. Whether it is your co-workers, your boss, or even your family members or your extended community, we all end up supporting others somehow. Good customer support practices are important whether we are manning a support line, or if a co-worker is asking us for help with a PCB layout. And with my furnace problems, I found that Jack was a master at support. Here are some basic principles of support that I observed in him that I believe would helpful for all of us in the PCB community.

First, Jack put me at ease with the situation. He didn't try to buffalo me with technobabble, nor did he give me false hope. He patiently explained to me what was wrong at a level that I could understand, what his plan was, and how we would proceed from there. When his initial plan of attack didn't fix the furnace, he outlined a new plan making sure that I understood the change in direction. In all of this he never lied or held anything back from me. When it became apparent that the fix he planned on wasn't going to work, he admitted to it honestly and led us through to the next step.

Think about the times that you've been able to help someone. Perhaps a co-worker can't figure out how to get the layout software to add a via where they need it, or a specific net won't route to the pin that it should. The last thing that your co-worker needs at that moment is to see indifference in your eyes or to be baffled by technobabble. Depending on the gravity of the situation, they may be in a real panic. You may not have all the answers that they need, but by helping them to be at ease with the situation, often a solution will present itself that they couldn't see before.

The key here is to build trust and then not betray that trust when your co-worker needs your help. There were many times when I was supporting CAD customers that I would get a panicked call from someone who was stuck and couldn't get their layout tools to work the way that they expected them to. The first thing that I did was to make sure that they knew that I was there to help them, and that I would see them through the problem. Once they knew that someone had their back, their panic would subside and then we could get a lot more productive work done towards resolving their problem.

The next thing that I noticed is how thoroughly Jack guided me through the entire process. This is important: When all the repairs failed to fix the furnace, the only option left was to invest thousands of dollars in a new furnace. If Jack had told me, "Sorry I can't help you, just give me thousands of dollars for a new furnace" when he first showed up, I probably would have thrown him out on his ear. Instead, he educated me on how furnaces work, what was broken, and how he was attempting to repair it. When those repairs didn't work, I could clearly see why and that the only option left was to replace it.

When we are helping others with a problem, the best thing we can do is to help them to understand what is going on so that they can be part of the solution. There are some circumstances that will call for you to step in and fix the problem and then move on, this is part of regular customer support. There are many other scenarios though where it is better to guide the other person through the problem instead of taking it out of their hands. In this way, you will build trust with the other person, and they will learn more to hopefully be able to solve their own similar problems in the future.

Best of all, Jack never abandoned me during this whole process. He didn't transfer me over to someone else when he didn't know all the answers, instead he researched the issue to get me the correct information. He also stayed with me even when he could no longer help and another team had to be called in to install the new furnace. Jack has continued to check on us and has promised to come over after the installation to make sure that we have been well taken care of.

You've probably been on the phone trying to get support for a consumer product problem before, and had them transfer you from person to person to person. Well, your customers and your co-workers don't like that anymore than you do. The key is to maintain the trust that you have been building with the person that you are working with, and that trust isn't helped by dumping them over to someone else. There were many times when I was supporting an EDA customer that I wanted to give up, but I didn't because I knew that the customer might interpret this as abandonment. So I would roll up my sleeves and stick with the problem and the customer until we got it figured out and they were up and running again.

When you are working with others, whether they are customers or your co-workers, remember that they came to you for help for a reason. You may not have all the answers, but you are probably their lifeline and they need your help. So put them at ease, guide them through the problem, and don't leave them hanging. If the people that you are helping are your customers, you've just improved your odds of retaining them as customers in the future. If they are co-workers, you will help to build and maintain a solid relationship built on trust.

I would write more about this, but my fingers are freezing, so it's time to find some fat comfy gloves. See you next month! **DESIGN007**

Tim Haag is a consultant based in Portland, Oregon.

Going Organic

Organic solar cells could be an inexpensive and versatile alternative to inorganic solar cells. However, their low efficiencies and limited lifetimes currently render them impractical for commercial use.

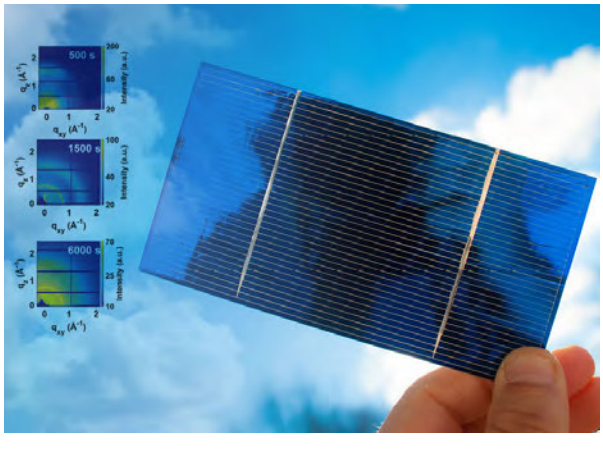
Using Argonne's Advanced Photon Source (APS), a DOE Office of Science User Facility, researchers analyzed how organic solar cells' crystal structures develop as they are produced under different conditions.

The scientists focused on the photoactive layer of the cell, built from thin films that absorb energy from sunlight and then convert that energy into electric current. The researchers produced the films via spin coating, a widely used process for film fabrication in research labs.

"It was the stability and reproducibility of this specific spin-coating setup that allowed this study to happen," said Northwestern graduate student Eric Manley, first author of the study published Oct. 9 in Advanced Materials.

The study's most significant discovery, made possible by the new experimental setup, was how certain additives can significantly affect both the time it takes for the film's structure to stop changing and the intermediate structures the film adopts during evolution.

"We hope this will pave the way to making these cells more viable for everyday applications," said Joseph Strzalka, physicist and member of the Time-Resolved Research group within Argonne's X-Ray Sciences division.



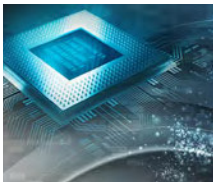
1 Top 10 Most-Read PCB Design Articles of 2017 ▶

On New Year's Day, we took a look back at the most-read PCB design articles of 2017. Here are the top 10 design articles of the last year for your enjoyment. Is it just a coincidence that two of these articles are related to HDI design techniques?

2 That's Hot: Ventec's Goodwin on Thermal Management ▶

IPC's fall committee meetings were held in conjunction with SMTA International, as has been the case for several years now. Patty Goldman sat in on some subcommittee meetings, including one on laminates, where she met up with Ventec COO Mark Goodwin for a discussion on thermal management from a laminate supplier's perspective.

3 Cadence Allegro Pulse Extends Team Collaboration ▶



Cadence Design Systems has announced Cadence Allegro Pulse, the industry's first solution to enable extended team collaboration by providing near-real-time insights into the complexities of the electronic design process. Allegro Pulse connects management, engineering, procurement and other business stakeholders to up-to-date work-in-progress design data in a single, unified web-based platform.

4 The Impact of HDI on PCB Power Distribution ▶

HDI is often used to meet the requirements of today's complex designs. Smaller component pitches, larger ASICs and FPGAs with more I/O, and higher frequencies with shrinking rise-times all require smaller PCB features, driving the need for HDI. Beyond some of the more obvious electrical effects of the microvias

used on HDI designs, there is also an impact to the power integrity the PCB.

5 Three Perspectives for HDI Design and Manufacturing Success ▶

Mike Creeden, CID+, has been in the PCB design industry for more than 40 years now. In June 2003, he founded San Diego PCB, which was acquired by Milwaukee Electronics about a year ago. Mike spoke with us about the latest HDI design techniques, as well as the pros and cons related to this cutting-edge process.

6 Who Really Owns the PCB Layout? ▶

One would think that the title of this article should be a no-brainer. The fact of the matter is that the ownership of this vital aspect of electronic design is not only cloudy, but it will become murkier in the next 10 years. This murkiness is also an opportunity for mechanical engineers who aren't afraid to expand their horizons. Paul Taubman of Nine Dot Connects has more.

7 Beyond Design: Next-Gen PCBs–Substrate Integrated Waveguides ▶

As PCB transmission frequencies head toward 100GHz, copper interconnect is reaching its performance threshold. Metallic waveguides are a better option than traditional transmission lines, but they are bulky, expensive and non-planar in nature. However, recently, substrate integrated waveguides (SIW) structures have emerged as a viable alternative.

8 Designers Notebook: Strategies for High-Density PCBs ▶

As hand-held and portable electronic products and their circuit boards continue to shrink in size, the designer is faced with solving the physical differences between traditional printed board fabrication and what's commonly referred to as HDI processing. The primary driver for HDI is the increased complexity of the more advanced semiconductor package technology.

9 PCB Libraries Rebrands Flagship Product, Library Expert Pro ▶

The Library Expert Pro, the industry's original IPC-7351-based footprint generator, has outgrown its name, and is now Library Expert Enterprise. This change better reflects the advanced features it currently has, the new features planned for 2018, and its capacity to provide enterprise-level library solutions. Some of the largest companies in the world are taking advantage of these features at the enterprise level in their organization.

10 Mentor Paper: The Benefits of Model-Based Engineering in Product Development ▶

Simulation models are often used to help develop today's system designs. Unfortunately, the typical system model is seldom fully leveraged throughout the development process. This paper by Mentor, a Siemens business, describes how model-based engineering increases the productivity of the development process and enables informed design decisions.

Career Opportunities

Pssst! Are You Looking for Someone?

Place your notice in our Help Wanted section.

For just $500, your 200 word, full-column—or, for $250, your 100 word, half-column—ad will appear in the Help Wanted section of all three of our monthly magazines, reaching circuit board designers, fabricators, assemblers, OEMs and suppliers.

Potential candidates can click on your ad and submit a résumé directly to the email address you've provided. If you wish to continue beyond the first month, the price is the same per month. No contract required. We even include your logo in the ad, which is great branding!

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Barb Hockaday at barb@iconnect007.com or +1.916.608.0660 (-7 GMT)

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GOOD FOR THE INDUSTRY

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SALESPERSON WANTED · MAINLAND SOUTH CHINA

Work where you live!

The I-Connect007 China team is seeking an experienced salesperson to generate and manage a revenue stream for our Chinese publications.

Key Responsibilities include:

- Sell advertising contracts for monthly magazine
- Develop and cultivate new business
- Keep timely and accurate records
- Generate and follow up on all leads
- Manage contract renewals
- Account management: work with local and international team to provide customer support
- Phone and email communications with prospects
- Occasional travel

Qualifications

Successful candidates should possess a university degree or equivalent, experience with managing and cultivating leads, projecting, tracking and reporting revenue. We are looking for positive, high-energy candidates who work well in a self-managed, team-based, virtual environment.

Compensation

This is a base salary-plus-commission position. Compensation commensurate with experience.

Requirements

- Must be located in China Mainland, South China area preferred
- Good command of Chinese language, proficient with English speaking and writing
- Able to follow established systems and learn quickly
- Able to maintain professional external and internal relationships reflecting the company's core values
- 2-5 years' sales experience
- Experience with Microsoft Office products
- Must be highly motivated and target-driven with a proven track record for meeting quotas
- Good prioritizing, time management and organizational skills
- Create and deliver proposals tailored to each prospect's needs
- Experience in the electronics industry desirable

QUALIFIED CANDIDATES: CLICK HERE TO APPLY

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WWW.ICONNECT007CHINA.COM

Career Opportunities

saki
The Future in Focus

Field Application Engineer

Saki America Inc., headquartered in Fremont, CA, a leader in automated inspection equipment, seeks two full-time Field Application Engineers (FAE), one in the Fremont headquarters and the other for the Eastern and Southern United States.

The FAE will support the VP of Sales and Service for North America in equipment installation, training, maintenance, and other services at field locations. The FAE will provide technical/customer support and maintain positive relationships with existing and future customers.

Strong analytic abilities and problem-solving skills are a must in order to understand customer applications and troubleshoot issues. The FAE will perform demos and presentations for customers and agents as well as assisting in trade show activities. Candidate must have a minimum of a two-year technical degree, experience in AOI, SPI, and X-ray inspection, and strong verbal and written communication skills. The position requires the ability to travel about three weeks per month. Must be a US citizen and be able to lift up to 40 lbs.

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eptac
TRAIN. WORK SMARTER. SUCCEED.

Become a Certified IPC Master Instructor at EPTAC

Job Summary:
We are growing! EPTAC, a leading provider in the electronics training industry is looking for some great people to join our team. If you love teaching people, choosing the classes and times you want to work, and basically being your own boss, this may be the career for you. We are looking for instructors that have a passion for working with people to develop their skills and knowledge. If you have a background in electronics manufacturing and an enthusiasm for education, drop us a line or send us your resume. We would love to chat with you. Opportunities available across U.S. and Canada, especially in our growing markets of California, Chicago, Minnesota and New England. Some travel involved. IPC-7711/7721 or IPC-A-620 CIT certification a big plus.

Qualifications and Skills:
- A love of teaching and an enthusiasm to help others learn new concepts and skills
- Background in electronics manufacturing
- Previous soldering and/or electronics/cable assembly experience
- Previous IPC Certification a plus, but will certify the right candidate

Benefits:
- Ability to operate from home: no required in-office schedule
- Flexible schedule: control your own time, work as often as you like
- IRA retirement matching contributions after one year of service
- Training and certifications provided and maintained by EPTAC

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Career Opportunities

ACE ACCURATE CIRCUIT ENGINEERING

PCB Assembly Supervisor—full time
Accurate Circuit Engineering—Santa Ana, CA

Position Summary: Responsible for all assembly processes to ensure continued growth as directed by management.

Essential Job Functions:
- Create, implement, and supervise in-house manufacturing facility
- Recruit, hire, train, and supervise assembly floor personnel
- Extensive hands on experience with all aspects of PCB assembly
- Understanding of IPC-A-610 standards
- Research and acquire additional assembly resources
- Gather data on product shortages, lead times, price changes, etc.
- Coordinate the assembly activities with sales to ensure 100% on-time delivery
- Create, implement, and supervise daily quality processes to ensure 100% accuracy
- Document, monitor and review progress of the business unit
- Respond to internal and external customers in a timely manner
- Coordinate walk-through, site audits, etc.

Qualifications:
- Minimum 3 years as operations supervisor of electronics assembly house
- 5+ years' experience in the electronics industry
- Previous experience as a quality or operations supervisor preferred
- Ability to solve practical problems using pre-established guidelines
- Strong facility in Microsoft Office applications
- Excellent verbal and written communication skills
- Ability to work with people of diverse backgrounds
- Highly organized/excellent time management skills
- Ability to perform at the highest level in a fast-paced environment
- Valid California driver's license

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ACE ACCURATE CIRCUIT ENGINEERING

PCB Process Planner

Accurate Circuit Engineering (ACE) is an ISO 9001:2000 certified manufacturer of high-quality PCB prototypes and low-volume production for companies who demand the highest quality in the shortest time possible. ACE is seeking a skilled individual to join our team as a PCB process planner.

Responsibilities will include:
- Planning job travelers based on job release, customer purchasing order, drawings and data files and file upon completion
- Contacting customer for any discrepancies found in data during planning and CAM stage
- Consulting with director of engineering regarding technical difficulties raised by particular jobs
- Informing production manager of special material requirements and quick-turn scheduling
- Generating job material requirement slip and verify with shear clerk materials availability
- Maintaining and updating customer revisions of specifications, drawings, etc.
- Acting as point of contact for customer technical inquiries

Candidate should have knowledge of PCB specifications and fabrication techniques. They should also possess good communication and interpersonal skills for interfacing with customers. Math and technical skills are a must as well as the ability to use office equipment including computers, printers, scanners, etc.

This position requires 3 years of experience in PCB planning and a high school level or higher education.

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Career Opportunities

CHEMCUT
BOUNDLESS INNOVATION | UNBEATABLE PRECISION

Chemical Process Engineer

Chemcut, a leading manufacturer of wet-processing equipment for the manufacture of printed circuit boards for more than 60 years, is seeking a Chemical Process Engineer. This position is located at Chemcut's main facility in State College, Pennsylvania. Applicants should have an associate degree or trade school degree, or 4 years equivalent in chemical process engineering.

Job responsibilities include:

- Developing new industrial processes
- Providing process criteria for both new equipment and modifying existing equipment
- Testing new processes and equipment
- Collecting data required to make improvements and modifications
- Assisting in investigating and trouble-shooting customer process problems
- Ensuring that equipment works to its specification and to appropriate capacities
- Assessing safety and environmental issues
- Coordinating with installation/project engineers
- Ensuring safe working conditions and compliance with health and safety legislation

Key Skills:

- Aptitude for, and interest in chemistry, IT and numeracy
- Analytical thinking
- Commercial awareness
- Ability to perform under pressure
- Communication and teamwork
- Problem-solving

Experience with circuit board processes is a plus.

Contact Arlene at 814-272-2800 or by clicking below.

apply now

CHEMCUT
BOUNDLESS INNOVATION | UNBEATABLE PRECISION

Field Service Technician

Chemcut, a leading manufacturer of wet-processing equipment for the manufacture of printed circuit boards for more than 60 years, is seeking a high-quality field service technician. This position will require extensive travel, including overseas.

Job responsibilities include:

- Installing and testing Chemcut equipment at the customer's location
- Training customers for proper operation and maintenance
- Providing technical support for problems by diagnosing and repairing mechanical and electrical malfunctions
- Filling out and submitting service call paperwork completely, accurately and in a timely fashion
- Preparing quotes to modify, rebuild, and/or repair Chemcut equipment

Requirements:

- Associates degree or trade school degree, or four years equivalent HVAC/industrial equipment technical experience
- Strong mechanical aptitude and electrical knowledge, along with the ability to troubleshoot PLC control
- Experience with single and three-phase power, low-voltage control circuits and knowledge of AC and DC drives are desirable extra skills

To apply for this position, please apply to Mike Burke, or call 814-272-2800.

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Career Opportunities

Electronics Expert Engineer

Orbotech is looking for an Electronics Expert Engineer to handle various hardware activities, including communication, data path processing, device interfaces and motion, as well as system supporting functions in a multi-disciplinary environment.

What Will Your Job Look Like?

- Providing cutting edge hardware solutions for challenging product line needs
- Developing board design and Logic in VHDL
- Defining and managing interfaces (software, algorithm, mechanics and electricity)
- Successfully integrating hardware with other product disciplines
- Supporting the product needs during and following release

What Do You Need to Succeed?

- BSc in electronics engineering
- At least 5 years of R&D experience in complex board design, mainly FPGA (communication interfaces, DDR controller, algorithm implementation)
- Experience in an Altera/Xilinx development environment
- Experience in ECAD design tools (DxDsigner, ModelSim) is an advantage
- Knowledge in laser interfaces, RF and analog is an advantage

Who We Are

Virtually every electronic device in the world is produced using Orbotech systems. For over 30 years, Orbotech has been a market leader in developing cutting edge inspection, test, repair, and production solutions for the manufacture of the world's most sophisticated consumer and industrial electronics.

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Electronics Team Leader

Orbotech is seeking an Electronics Team Leader to join our electronics team, which develops multi-disciplinary systems, including vision/laser, image processing, and control and automation missions.

What Will Your Job Look Like?

- Lead a team of electronics engineers in a multi-disciplinary environment
- Lead electronic activities from requirement phase to development, integration and transfer, to production
- Be the focal point for other disciplines and projects managers
- Maintain and improve existing electronics platforms

What Do You Need to Succeed?

- BSc/MSc in electronic engineering/ computer science from a well-recognized university
- 5+ years' experience in digital board design, high-speed links, computing embedded systems, and HW/SW integration
- 2-3 years' experience in leading a team of engineers
- Solid skills in complex FPGA design with multi-modules
- Solid skills in high-speed board design, DDR3/4, PCIE, USB, IO, and optic links
- Ability to design and execute end-to-end solutions

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Career Opportunities

ventec INTERNATIONAL GROUP 騰輝電子

Technical Sales Engineer

Positions available in the Chicago area and California

Do you want to advance your career by joining a globally successful and growing world class CCL manufacturer and help drive that success? As a California-based member of the technical sales team, your focus will be on Ventec's core market segments: mil/aero, automotive and medical, offering a full range of high-reliability materials including polyimide, IMS and thermal management products.

Skills and abilities required

Non-negotiable:
- DRIVE & TENACITY!

Required:
- 7 to 10 years of experience in the PCB industry in engineering and/or manufacturing
- Detail-oriented approach to tasks
- Ability to manage tasks and set goals independently and as part of a team
- Knowledge of MS office products

Full product training will be provided. This is a fantastic opportunity to become part of a successful brand and a leading team with excellent benefits.

Please forward your resume to:

jpattie@ventec-usa.com and mention "Technical Sales Engineer - California Based or Chicago area" in the subject line.

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ventec INTERNATIONAL GROUP 騰輝電子

Ventec Seeking U.S. Product Manager for tec-speed

Want to work for a globally successful and growing company and help drive that success? As a U.S.-based member of the product and sales team, your focus will be on Ventec's signal integrity materials, tec-speed, one of the most comprehensive range of products in high-speed/low-loss PCB material technology for high reliability and high-speed computing and storage applications. Combining your strong technical PCB manufacturing and design knowledge with commercial acumen, you will offer North American customers (OEMs, buyers, designers, reliability engineers and the people that liaise directly with the PCB manufacturers) advice and solutions for optimum performance, quality and cost.

Skills and abilities required:
- Technical background in PCB manufacturing/design
- Solid understanding of signal integrity solutions
- Direct sales knowledge and skills
- Excellent oral and written communication skills in English
- Experience in making compelling presentations to small and large audiences
- Proven relationship building skills with partners and virtual teams

This is a fantastic opportunity to become part of a leading brand and team, with excellent benefits.

Please forward your resume to jpattie@ventec-usa.com and mention "U.S. Sales Manager—tec-speed" in the subject line.

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Career Opportunities

BLACKFOX
Premier Training & Certification

IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

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Altium

Business Development Representative at Altium

New Logo Business Development representatives are highly motivated and hardworking with an upbeat can-do attitude. They work with our New Logo Sales Team to displace our competition in accounts by offering Altium's unified PCB development tools within a defined region.

The New Logo Developer's (NLD) main responsibilities will be qualifying leads and prospecting into competitive lists, searching the web, and utilizing internal sales tools (Inside View, LinkedIn, Marketo, SalesForce) to uncover and work with opportunities for the New Logo Closer to close. They are expected to meet or exceed monthly, quarterly & annual quota.

Responsibilities:

- Develop lead opportunities by collecting information that includes business pains/needs, timelines, authority and project teams, budget, competitive information, etc.
- Aggressively drive daily prospecting calls to build pipeline of prospective clients and occasionally closing smaller deals
- Develop relationships with key partners in their territory to identify new business opportunities
- Plan and prioritize personal sales activities in conjunction with the New Logo Closer, with the goal of achieving sales targets
- Work alongside inside sales teams on specialized projects such as call-out campaigns, promo drives and webinar fulfillment
- Once trained, maintain an in-depth knowledge of Altium products and technologies, competitive products, and industry trends

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Career Opportunities

IPS INTEGRATED PROCESS SYSTEMS INCORPORATED

PCB Equipment Sales

World-class manufacturer of wet process equipment for the PCB and plating industries, Integrated Process Systems Inc. (IPS) is seeking qualified candidates to fill a position in equipment sales. Potential candidates should have:

- Process engineering knowledge in PCB manufacturing
- Outside sales background
- Residency on the West Coast to manage West Coast sales
- Knowledge of wet process equipment
- Sales experience with capital equipment (preferred)

Compensation will include a base salary plus commission, dependent upon experience.

more details

Altium

Application Engineer

The application engineer is the first contact for our customers who have technical questions or issues with our product. We value our customers and wish to provide them with highest quality of technical support.

Key Responsibilities:

- Support customer base through a variety of mediums
- Log, troubleshoot, and provide overall escalation management and technical solutions
- Create various types of topic based content, such as online help, online user guides, video tutorials, knowledge base articles, quick start guides and more
- Distill complex technical information into actionable knowledge that users can understand and apply
- Continually develop and maintain product knowledge

Requirements:

- Understanding of EDA electronic design software, schematic capture and PCB layout software
- Bachelor's degree in electronics engineering or equivalent experience
- Sales engineering and/or support engineering experience
- Circuit simulation and/or signal integrity experience
- Understanding of ECAD/ MCAD market segments
- Understanding of micro controllers, SoC architecture and embedded systems market
- Database experience preferred (i.e., MySQL, PostgreSQL, Microsoft Access, SQL, Server, FileMaker, Oracle, Sybase, dBASE, Clipper, FoxPro) etc.
- Experience with PLM/PDM/MRP/ERP software (Program Lifecycle Management) preferred
- Salesforce experience a plus

Salary based upon experience. Comprehensive benefits package and 401k plan. Openings in USA, UK, and Germany.

For more information, contact Altium.

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Career Opportunities

MacDermid
PERFORMANCE SOLUTIONS

Do you have what it takes?

MacDermid Performance Solutions, a Platform Specialty Products Company, and daughter companies manufacture a broad range of specialty chemicals and materials which are used in multi-step technological processes that enhance the products people use every day. Our innovative materials and processes are creating more opportunities and efficiencies for companies across key industries – including electronics, graphic arts, metal & plastic plating, and offshore oil production. Driving sustainable success for companies around the world, and at every step of the supply chain, takes talent. Strategic thinking. Collaboration. Execution.

The people of MacDermid Performance Solutions stand united by a guiding principle: If it doesn't add value, don't do it. This belief inspires a unique culture where each team member has opportunities to imagine, create, hone and optimize. Do you have what it takes? Join our growing team of over 4,000 professionals across more than 50 countries with openings in research, finance, customer service, production and more.

MacDermid Performance Solutions and its affiliates are Equal Opportunity/ Affirmative Action Employers.

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NCAB GROUP
Integrated PCB Production

Outside Sales/ Key Account Managers

NCAB Group USA is adding to our existing outside sales team in various U.S. locations:

- Ontario, California
- Itasca, Illinois
- Vancouver, Washington

This is a sales position that requires the ability to convert those cold calls into high-value customer meetings. What we are looking for:

- A "hunter" mentality
- The ability to create solid customer relationships
- A desire to excel and not settle for mediocrity
- 5+ years of experience in the PCB or semiconductor industry
- An excellent ability to present a product and do the "deep dive" during customer visits by asking open ended questions and identifying customer pain points
- The energy to move from prospecting to cold calls to getting the win
- Knowledge of "SPIN" selling
- A college degree
- Willingness to travel, domestically and globally
- U.S. citizens with a valid U.S. passport

Interested? Send your resume.

apply now

Visit us at www.NCABGroup.com

Career Opportunities

FPGA Design Expert

Orbotech is seeking a FPGA Design Expert to join our electronics team, which develops multi-disciplinary systems including vision/laser, image processing and electro-optics.

What Will Your Job Look Like?

- Lead image acquisition and processing activities in the team
- Engage in all aspects of FPGA design activity: requirement phase, coding, synthesizing, verification support and LAB bring up
- Participate in system definitions for current and next generation products
- Collaborate with other teams: SW, algorithm and QA

What Do You Need to Succeed?

- BSc/MSc in Electrical Engineering from a well-recognized university
- Extensive knowledge of VHDL
- 5+ years of FPGA development experience (requirement, architecture, RTL coding, simulation, synthesis, timing analysis, P&R, board level integration and verification)
- Experience in designing and implementing low-latency, high-throughput FPGA designs utilizing PCIe Gen2/3, Gigabit Ethernet, SERDES, DDR3/4
- Experience in complex FPGA such as Altera Stratix-II and Arria 5&10 devices
- Authoring documentation experience such as FPGA specifications and FPGA verification plans

Who We Are

Virtually every electronic device in the world is produced using Orbotech systems. For over 30 years, Orbotech has been a market leader in developing cutting-edge inspection, test, repair, and production solutions for the manufacture of the world's most sophisticated consumer and industrial electronics.

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Arlon EMD, located in Rancho Cucamonga, California is currently interviewing candidates for **manufacturing** and **management positions.** All interested candidates should contact Arlon's HR department at 909-987-9533 or fax resumes to 866-812-5847.

Arlon is a major manufacturer of specialty high performance laminate and prepreg materials for use in a wide variety of PCB (printed circuit board) applications. Arlon specializes in thermoset resin technology including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, high density interconnect (HDI) and microvia PCBs (i.e., in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001:2008 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customer's requirements.

more details

my I-Connect007

GOOD FOR THE INDUSTRY

Account 1 — Profile 2 — Company 3

During this process please don't use your browsers back button.

Your Email *	Your Email
Confirm Email *	Confirm Email
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Events Calendar

47th NEPCON JAPAN ▶
January 17–19, 2018
Tokyo Big Sight, Japan

1st Autonomous Driving Technology Expo ▶
January 17–19, 2018
Tokyo Big Sight, Japan

DesignCon 2018 ▶
January 30–February 1, 2018
Santa Clara, California, USA

EIPC 2018 Winter Conference ▶
February 1–2, 2018
Lyon, France

MD&M West ▶
February 6–8, 2018
Anaheim, California USA

2018FLEX ▶
February 12–15, 2018
Monterey, California USA

IPC APEX EXPO 2018 Conference and Exhibition ▶
February 27–March 1, 2018
San Diego, California, USA

China International PCB and Assembly Show (CPCA) ▶
March 20–22, 2018
Shanghai, China

KPCA Show 2018 ▶
April 24–26, 2018
Kintex, South Korea

Thailand PCB Expo 2018 ▶
May 10–12, 2018
Bangkok, Thailand

Medical Electronics Symposium 2018 ▶
May 16–18, 2018
Dallas, Texas, USA

2018 EIPC's 50 Years Anniversary Conference ▶
May 31–June 1, 2018
Bonn, Germany

JPCA show 2018 ▶
June 6–8, 2018
Tokyo, Japan

IPC Calendar of Events

SMTA Calendar of Events

DESIGN007 Calendar of Events

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