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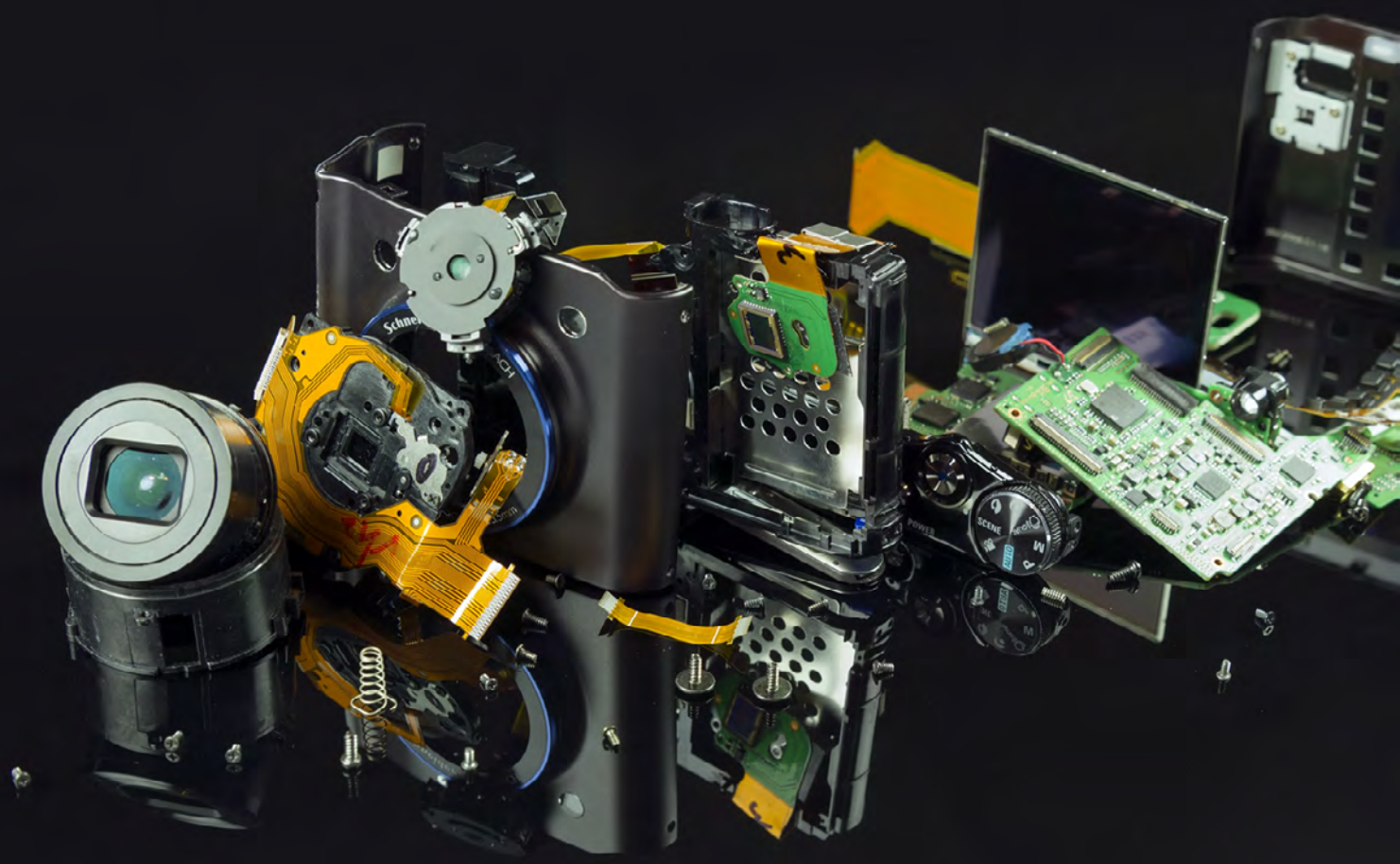

MULTI•BOARD design

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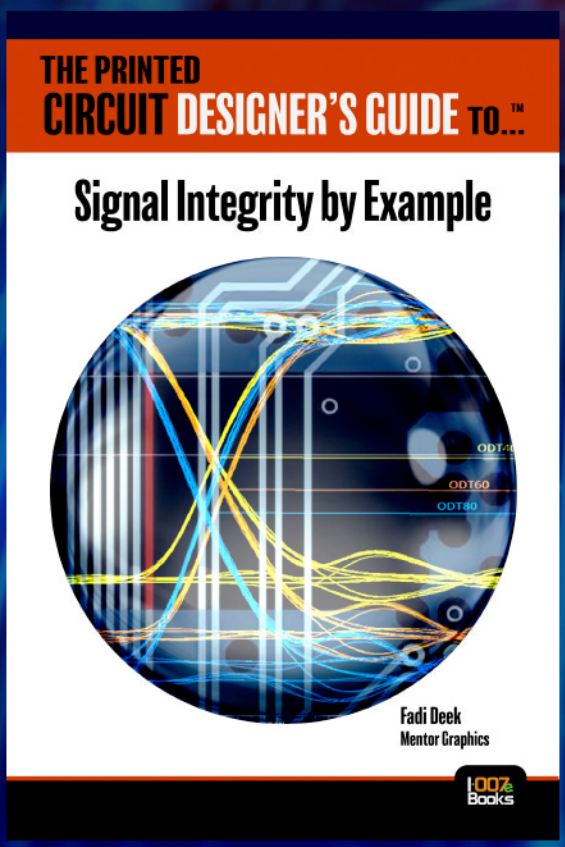

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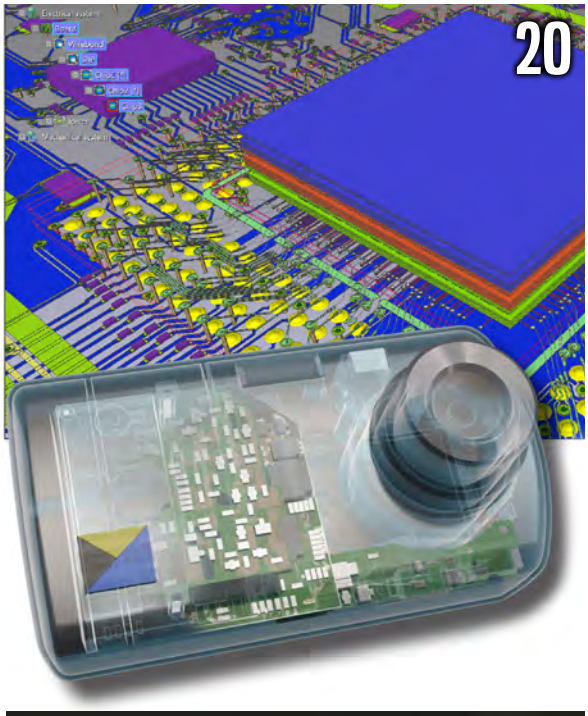
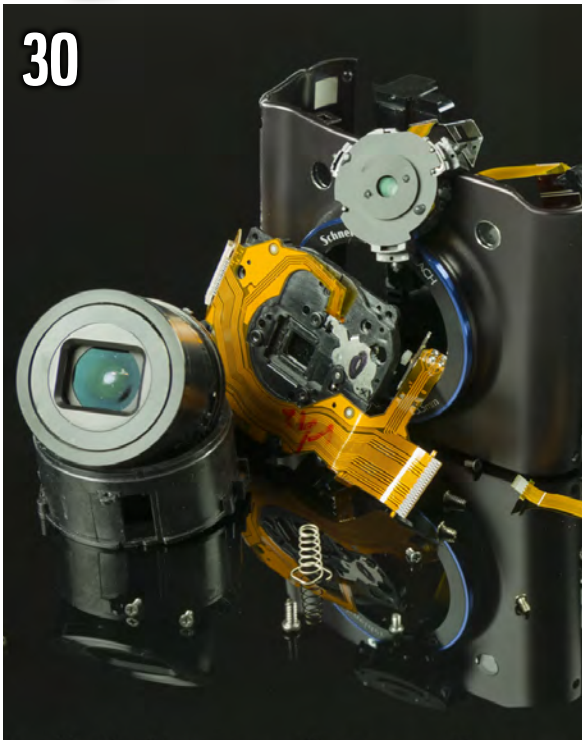


Multi-board Design

Over the past few decades, we've seen a gradual expansion of the number of multi-board electronic devices. Products are more complex now, plain and simple. There's no way that anyone could build a car, not to mention an autonomous car, with a single PCB in 2018. For our June issue, we have a variety of features that are chock-full of multi-board design information.



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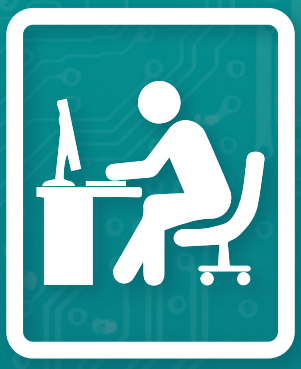

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Multi-board Design: Multiple Challenges?

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

If one PCB is good, aren't two or more boards even better? That is the question!

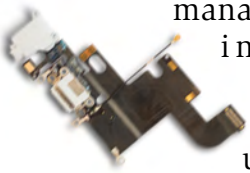
For most of the PCB's history, electronic devices contained a single circuit board. But that was back in the "olden days," and that time has passed.

Over the past few decades, we've seen a gradual expansion of the number of multi-board electronic devices. Products are more complex now, plain and simple. There's no way that anyone could build a car, not to mention an autonomous car, with a single PCB in 2018.

Multi-board devices are here to stay. But multi-board PCB design brings with it even more challenges for the designer and design engineer. It's all about management. It reminds me of a juggler trying to keep half a dozen balls in the air.

Every aspect of the design process is different, from schematic through data hand-off. Design teams, sometimes working in different time zones or countries, must become fluent in system-level management of a variety of interconnects, and ECAD and MCAD collaboration is more critical than ever with multi-board designs.

Designers are constantly making trade-off decisions throughout the multi-board design cycle, especially regarding reliability, thermal management, signal integrity and power integrity. The final product's form factor weighs heavily on the design process,



and a good 3D EDA tool is a requirement for laying out multiple PCBs today.

Fortunately, most of the EDA tools of today have multi-board design capabilities, and 3D functionality plays a big role. Interconnect management, data management, concurrent design, and ECAD-MCAD co-design functions also help bring multi-board design into the mainstream.

For our June issue, we have a variety of features that are chock-full of multi-board design information. In our first interview, Dave Wiens of Mentor discusses multi-board design techniques, from a 30,000-foot view down to a nuts-and-bolts board level, including the various trade-offs that occur throughout the design cycle. Zuken's Bob Potock provides a technical article on the 3D convergence of multi-board PCB and IC packaging design, and the importance of ECAD and MCAD collaboration. Finally, we interviewed Ben Jordan of Altium, who breaks down many of the challenges related to multi-board design, and some of the techniques that can simplify complex designs. As Ben says, "It's not a complicated concept."

From our monthly contributors, we have Barry Olney of In-Circuit Design who explains DDR3 and DDR4 fly-by topology termination and routing, while John Coonrod of Rogers Corporation discusses exceptions designers might encounter when comparing material data sheets. And Jade Bridges of Electrolube shines a spotlight on the selection of thermal management materials.

To wrap things up, we have an article from Chang Fei Yee of Keysight Technologies that outlines the best methods for achieving signal integrity during layer transition in high-speed boards.

As we head into the summer, take the time to download a PDF of *Design007 Magazine* to read on the beach. We'll keep bringing you all of the design news and technical information that you need! **DESIGN007**

Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 18 years. He can be reached by clicking here.

A Laser that Can Smell like a Hound

University of Adelaide researchers have created a laser that can "smell" different gases within a sample. Applications for the new device lie not just in environmental monitoring and detecting industrial contamination, but may eventually be used to diagnose disease by "smelling" the breath.

The researchers liken the ability of the laser to differentiate between different gas compounds in a sample to the sensitive nose of a bloodhound. But rather than smell, the device uses patterns of light absorption to measure the composition of the sample.

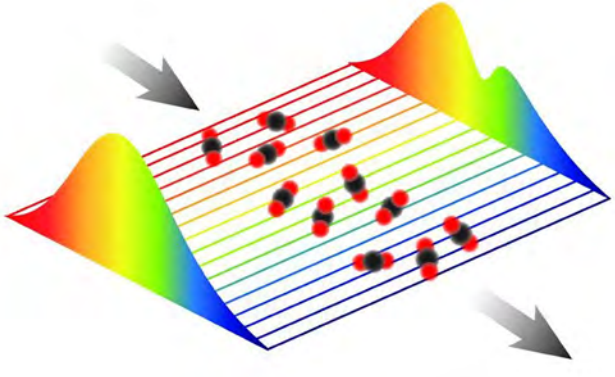
From the University's Institute for Photonics and Advanced Sensing (IPAS), the researchers report in the journal Physical Review Applied that the laser can measure the amount of carbon dioxide in a gas sample in under one second, with high accuracy and precision.

"The ability to rapidly measure gas composition to such high accuracy is cutting edge," says lead author Sarah Scholten, PhD candidate.

The device exploits a Nobel-prize winning technology, developed by US and German scientists, called an "optical frequency comb." This laser comb generates millions of different light frequencies or colours at once.

The researchers pass this special light through a sample of gas where each gas molecule absorbs a distinctive set of colours. The pattern of light absorption is a unique fingerprint of the gas composition of the sample.

"This first work aims at atmospheric monitoring, however, the technique is broadly applicable and offers an avenue for near-universal concentration measurements," says Dr. Chris Perrella, postdoctoral fellow.



Dave Wiens
Discusses Multi-board Design Techniques

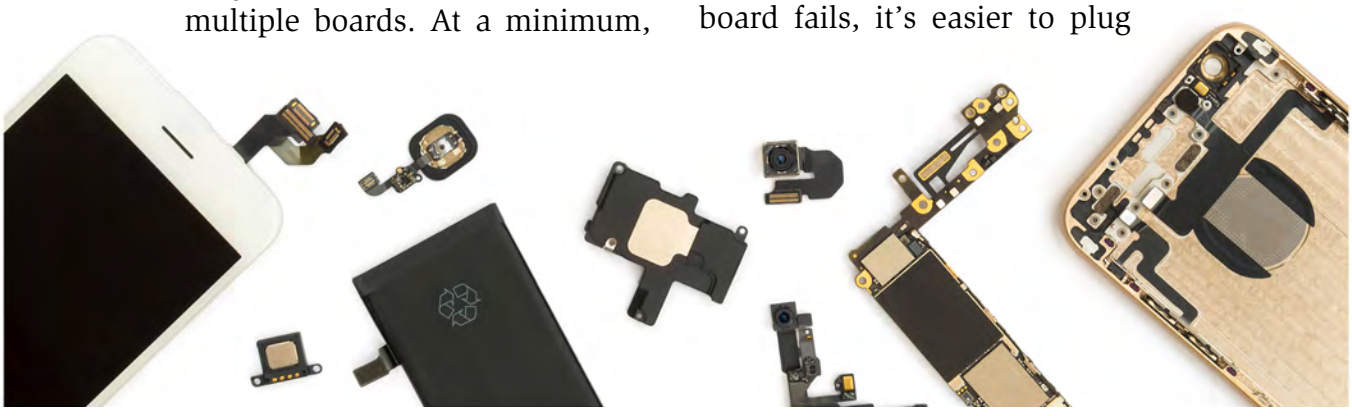
Feature by Andy Shaughnessy
I-CONNECT007

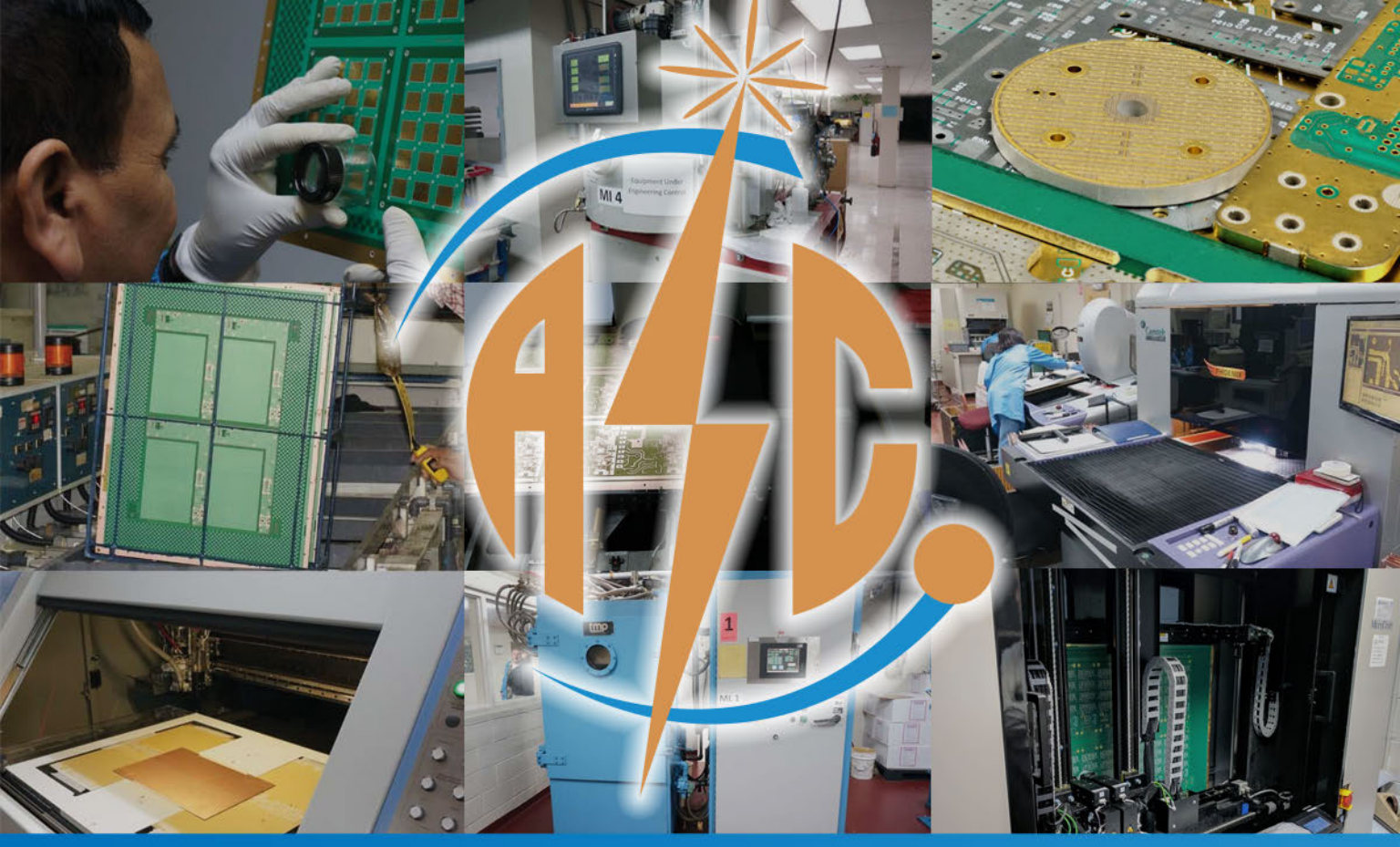
Today, many products contain two or more PCBs, and multi-board design has become the rule rather than the exception for quite a few PCB designers. For this multi-board design issue, I recently interviewed Dave Wiens, product marketing manager for Mentor, a Siemens business. We discussed how the multi-board design technique differs from laying out single boards, along with the planning, analysis and verification processes required to design multi-board systems.

Andy Shaughnessy: Dave, what are some of the typical end products that might use multiple PCBs?

Dave Wiens: The easy answer is that almost every end-product that includes electronics is a multi-board system, even small products like your mobile phone. If you look up your phone model on iFixit, you'll see a teardown that has multiple boards. At a minimum, there'll be a separate board for the camera or for the audio or for the external connections. Those are all separate functions and, in some cases, when somebody's designing they won't necessarily design all those pieces. They might, for instance, be acquiring the camera from somebody else, and that basically represents a component. It is a complete PCB, but to them it's a component because they didn't design it. We're not necessarily talking big back planes, with tons and tons of data cards on them. Certainly, that's a multi-board system, but pretty much everything you see today is multi-board.

I don't know about you, but when something in my house stops working, I tend to tear it apart. Sometimes I'm trying to figure out if I can fix it, but often I just want to see how they designed it. Really, when you're designing something and making decisions to make it into multiple boards, you start thinking about things like size and space. Should I put this all on one board? Should I break it up into multiple boards for space reasons? Should I do it because of reliability reasons? If this data board fails, it's easier to plug





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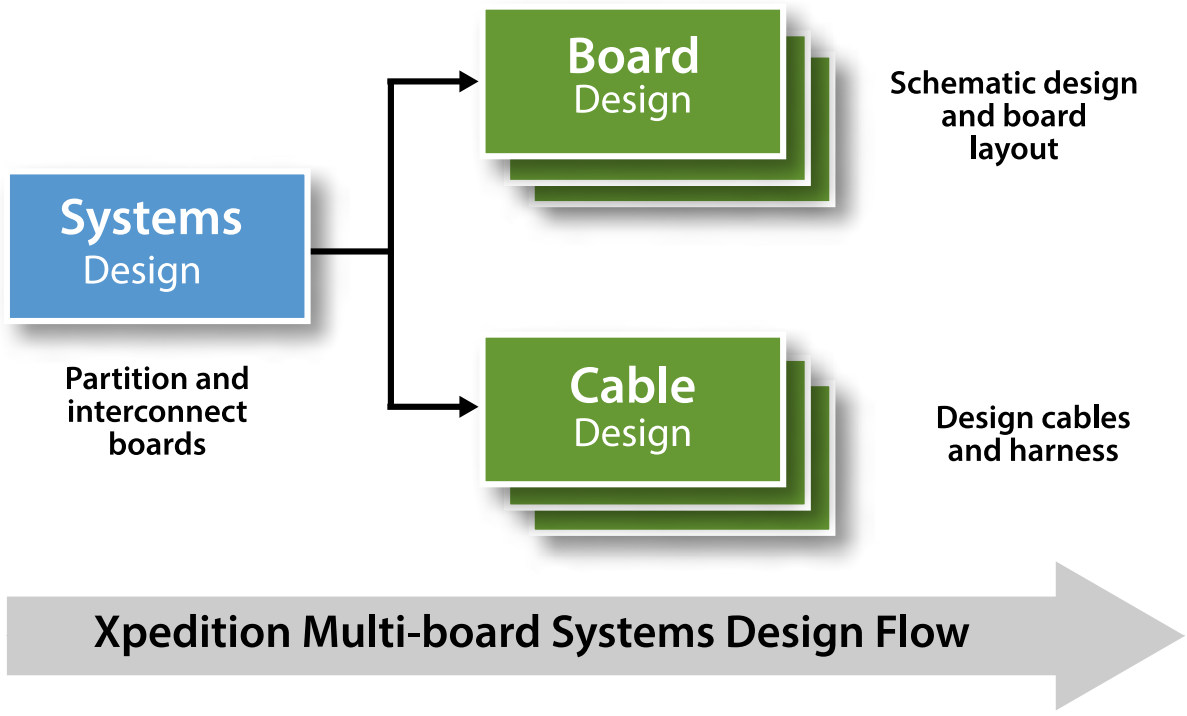

Figure 1: A fully integrated process for designing multiple PCBs and associated cables.

and play it with something else versus throwing away the whole system. Should I do it for cost reasons? Performance reasons? And then there's the make versus buy decision, right? For this function of my system, should I just buy a board and connect it to my system? Or should I design it into the system?

You see that with your home PC. It's got dedicated graphics built into it now, but you still may want to put an add-on graphics card, but those used to be things that weren't necessarily integrated into one system. They've done that over time.

Shaughnessy: It sounds like some of the biggest challenges are the trade-offs make. Like, should you add another board? What are some of those challenges?

Wiens: I'd loosely group the design challenges into four categories: managing design complexity, enabling multi-disciplinary team collaboration, optimizing product reliability, and leveraging IP across the organization. Regarding design complexity, yes, the trade-offs are a huge one and, frankly, because of that a lot of people kind of avoid it. I mean, they make decisions very early on to segment something. They take their high-level requirements, and then they start building an architecture from that. They decide what's going to be hardware, what's going to software, and how that's going to interplay with mechanical structures, cabling structures, all of that is decided way up front, and then the question is: Do they ever revisit that? If they don't revisit it, then they were either really good and they got it right up front, or as the design progressively refines itself, as the engineers refine it from that high-level architecture down into the physical implementations, they may find things.

For instance, the architecture indicates, "I decided to put these two boards over here." But maybe they don't fit. Maybe they are too far apart for those high-speed signals from the driver on one board to the receiver on another board. There are things that you don't know at that top level that as you progressively refine you get smarter and smarter, and so you want to make those trade-offs progress through the design. If you locked and loaded your design way up front, then you've lost that alternative. That's the case of most teams. Because it's so painful to make changes after that initial archi-

tecture was decided, they don't tend to do a lot of revisiting it in the form of trade-offs, in the form of any ECOs.

When the design gets bigger, it becomes nearly impossible to use that form of collaboration, so that's an impact because of complexity. Also, because of that complexity and the density of designs, the performance of designs, you've got to think about trade-offs like form factor or performance where before maybe the box was big enough. You really didn't care what went where or you were operating down at much lower speeds, and so you didn't care about performance across boards, but as those changes happen, it becomes more critical to do design trade-offs.

Regarding the second challenge, to address complexity, teams need to be able to communicate or collaborate across multiple disciplines. I was just talking about the box, and so I'm talking about the mechanical guy and the guy doing the PCB being able to collaborate. Maybe the high-speed engineers are collaborating with the PCB guys, and so this multi-discipline collaboration needs to be managed more efficiently, again, to enable them to do those trade-offs to avoid any redundant efforts. Because a lot of times when they pass data from one person to the next, they're doing it again through some manual means, maybe email. It may be a whiteboard. There are lots of ways to do it that are very inefficient, so somebody receives that data and they basically must redundantly design whatever that person communicated and, of course, that introduces lots of fun errors.

We're really trying to find ways to break down what we talked about, black box design or silo design processes. There are silos really across the spectrum. If you think about a process from left to right, on the left you've got requirements and, by the way, left to right you could think about it in terms of a V diagram, too, if you wanted. On the left, though, you've got your basic requirements. Those marketing people they come in and say, "Here's what we want to build." It has requirements, and then somebody takes those requirements and they progressively refine it down into an architecture, and then at some point it ends up as PCBs. At the back end of the left-to-right process, we at Mentor have been leveraging the Valor technology to optimize what we call the lean NPI process to handle the transfer and the collaboration between the PCB design team and the manufacturing team. There's also top to bottom, where you have the multiple disciplines. You've got hardware and inside hardware there's multiple PCBs that have packages on them, which have silicon on them, and then there is software, cabling, and maybe the networking on what's being communicated across that cabling, and the mechanical infrastructure. These are all different disciplines that, at some point, are being designed concurrently after the design has been partitioned up for those disciplines.

Those guys need to collaborate more efficiently as well, top to bottom, and we've talked in the past about things like ECAD/MCAD collaboration, right? How do you optimize those guys working across disciplines? The same thing happens between electronics and electrical. Is it in the wiring? How do I optimize?

To put on my Siemens hat now, we talk about a continuous digital thread. The idea of a digital thread is from that initial point of requirements capture, where everything is continuously created and communicated in a digital form, eliminating any redundant efforts and optimizing the communication between steps. That's the Holy Grail.

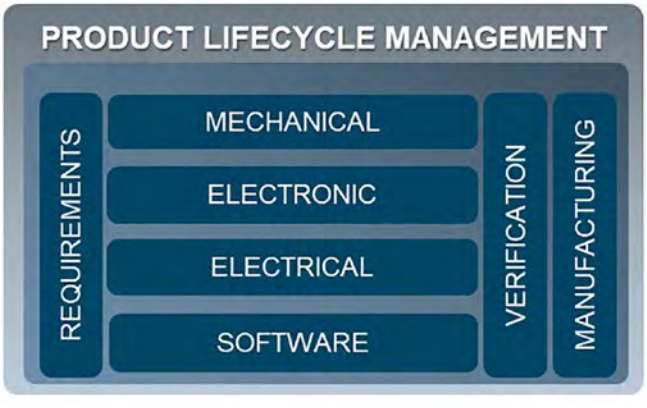

Figure 2: Optimizing electronic systems design with a continuous digital thread from requirements through manufacturing, and across multiple domains.

The third challenge is optimizing product reliability. I'm designing this system and I've worked across the teams efficiently, but I still may not be catching all the errors, and as I build larger and larger systems the chances of designing in errors increases, and so the need for technology to validate designs throughout the process increases. Validation starts with the connectivity between the multiple boards—simple things like connector pin mismatches can cost millions to identify and redesign. It also includes system-level schematic checking and system-level modeling for signal and power integrity, thermal and mechatronic behavior.

The last challenge is leveraging the IP generated during the design process across the organization, and that partly gets into that digital thread of data passing throughout the flow, but it also says, "Hey, look. If I design a piece of circuitry, I want others to be able to reuse it." At the single board level, I've seen upwards of 80% of a design reused from one generation of a product to the next. You want to enable that efficiently, but that's not multi-board design. When it comes to multi-board, people are reusing entire boards.

"Hey, look. If I design a piece of circuitry, I want others to be able to reuse it." At the single board level, I've seen upwards of 80% of a design reused from one generation of a product to the next.

Shaughnessy: Well, it sounds like there's a lot going on at the very front end.

Wiens: Yes. It's at the front end and it's also really throughout the whole process because, again, you want to enable that guy at the front end to make smart decisions, but you also want to enable progressive refinement with optimization. As the thing goes through and you realize, "Hey, this either won't work or it won't work as well as it could have. Hey, what changes can we make? Can we put this set of functionalities onto this board? You know, onto board A instead of board B?" Can we, in some cases, say, "I want a really, really fast connection; can I have a fiberoptic cable connection between these two boards instead of going through a whole bunch of physical connectors across back planes and things like that?"

Those are the kinds of decisions that somebody is going to sit there and try to think through, once they start seeing the physical incarnation of the board being built.

Shaughnessy: Speaking of the front end, I've heard of designers who want the schematic to represent multiple boards. Is a multi-board schematic that different?

Wiens: It certainly is. We certainly have had customers who started there. Most modern EDA tools have a hierarchical schematic system. That just means you have high-level blocks, you design at a high level, and then you start to poke into a block and you can see more data, and you can progressively go down multiple levels of that. Engineers naturally said, "Well, okay. So if at the top level today my high-level schematic is just one board, well, what if I go one level above that? Now, I'm looking at multiple boards." That is possible, but it gets back to the complexity of managing all that data, managing the connections, and really at that level the schematic tool is really a documentation tool, not an architecture optimization tool, if you know what I mean.

In addition, system engineers don't normally know or really use schematic capture tools. They use higher-level abstraction tools, like Visio, which is basically just a hopped-up version of PowerPoint drawing tools. I'm underselling it, but you know what I mean if you've ever used Visio. But of course, they want that high-level abstraction to transfer directly to

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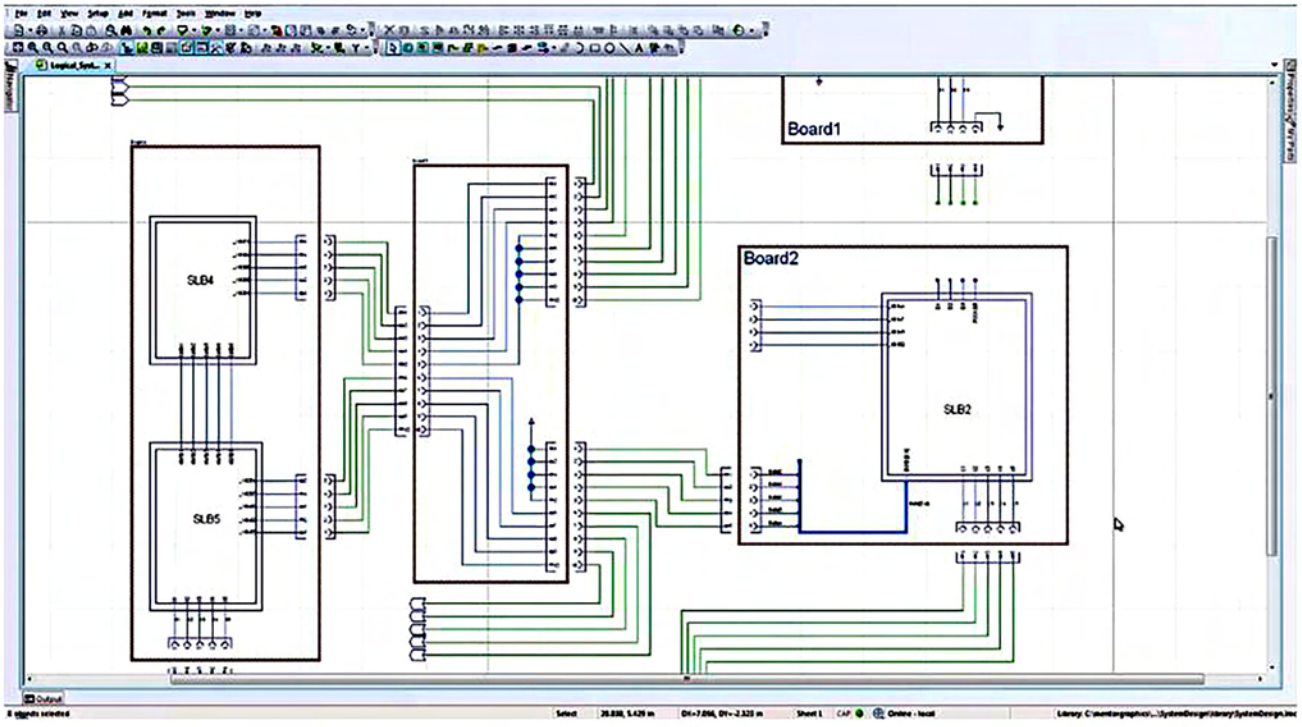


Figure 3: Connectivity defined across a multi-board system.

lower-level boards, without having to re-draw or re-design.

Shaughnessy: Well, it sounds like the multi-board is just one more option, really. Is it just another option in the toolbox?

Wiens: Yeah. I think we're talking about the same thing. In the world of EDA, the big word is automation. We try to find areas in the design process that are inefficient and optimize them and automate them as much as possible so that we improve the productivity of the overall team. That's what we're doing here.

People are designing multi-board systems today. They've just been doing it very inefficiently, and just saying, "Well, this is part of the design process. We have to suck it up." It takes longer. It produces lots of errors. It generates designs that aren't necessarily optimized, but, oh well, we don't have a better way, so we're going to keep doing it. It's kind of a new frontier for us EDA vendors to try to go after to optimize that. We're working to optimize that process from left to right. We've got technology that goes all the way back to requirements capture, and we have a lot more on the right side, too, in terms of manufacturing automation, and we're looking top to bottom, across multiple domains like ECAD, MCAD and electrical.

Shaughnessy: That's another thing I was wondering about. It seems like the MCAD side would be a little more involved than normally with multi-board. Is that accurate?

Wiens: MCAD's involvement often depends on the complexity of the enclosure the electronics are going into. If it's a simple box, with a lot of room, there's not much collaboration needed. Of course, most teams want to minimize material waste and try to optimize the enclosure. That requires close collaboration between ECAD and MCAD teams throughout the design process, not just at the beginning and end. To answer your question, regardless whether it's a single-board or multi-board system in the enclosure, the frequency of iterative collaboration depends on the complexity of the enclosure relative to the boards inside.

Shaughnessy: Is there any difference in how you run signal integrity and EMI simulation and analysis, other than having to just do it more than one time? What do you think?

Wiens: I could answer that question a couple of different ways. Let's just look at a single board scenario. I'm only designing a single board system, and let's say I have an RF section on that board. Well, suddenly, I'm putting up via arrays around that section within the board. I'm putting a metal can on top of that section. I mean, you've seen an RF board, right? They look cool, like little walled cities. That's an example of EMI control on a single board. The same thing, you can imagine, happens on a multi-board scenario. One board radiates onto another, and if you've got two boards sandwiched on top of each other, there's a lot of that going on between the two. But you use the same kind of isolation approaches to optimize it.

It's the same thing with signal integrity. Signal integrity is about a signal traversing from a driver through some kind of topology to a receiver. It's easy to think about on a single board. You've got a driver on one chip that goes through a package, comes out through the pin. It goes through traces on the board, maybe through some vias, pops up somewhere else, goes back up to another chip that receives the signal. Multi-board is just an extended topology. It starts bringing in things like connectors. That's why you have companies like Molex and Samtec selling expensive connectors that are optimized for performance, because high-speed signals traverse multiple boards. You need to be able to model that connector.

Some of that gets into 3D electromagnetics to efficiently model what the connector looks like, and maybe you've got some cabling between boards. You've got to model that as well. Engineers have been able to manually model a multi-board system for quite a while – but it meant manually re-creating the topology model in a simulation environment—again breaking the digital thread and potentially introducing errors and delays. To try to automate that process, using that 'A' word in EDA, means looking at the overall topology. We extract that topology automatically into HyperLynx and build all those topology models for them so that they don't have to do it all manually. That's something that we can do today in a multi-board environment.

You asked about EMI and SI, and thermal is another case that's very common. We've got a technology called FloTHERM that's integrated within the flow. With FloTHERM, you can model at the chip level. You can model the chip inside a package. You can model that package on a board. You can model multiple boards inside an enclosure, and all the way up to that enclosure inside a room.

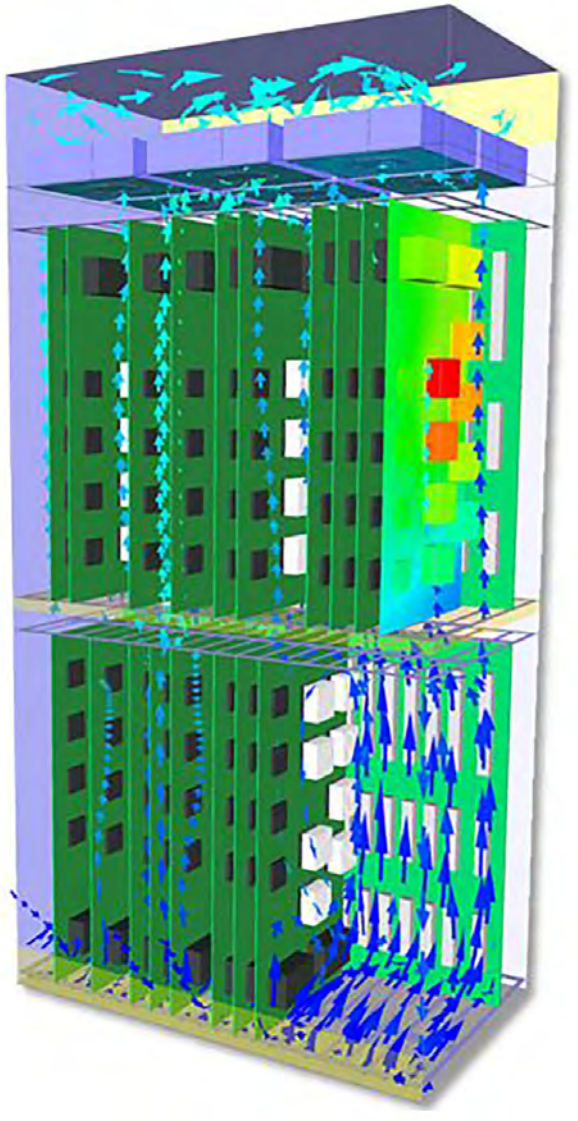


Figure 4: Virtual prototype multi-board system for mechatronic behavior, signal/power/thermal performance and manufacturability.

There are other things like schematic integrity, being able to model to do checks on schematics at the single board or multiple board level. I mean, there are just lots and lots of examples of validation that people have always thought of as a single board problem, but it naturally transfers itself up into the multi-board scenario.

Shaughnessy: On multi-board design, is it typically a team working on it? That seems like the best way to go, having a couple of guys working on it at the same time doing concurrent design.

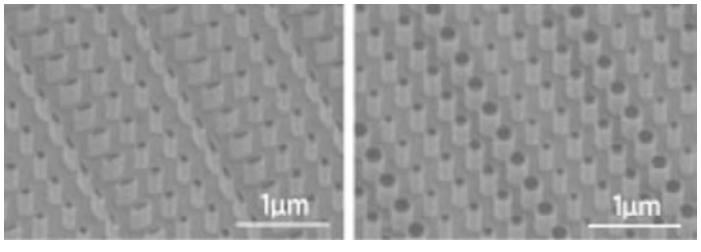
Wiens: Yep, absolutely. There is concurrency in that left to right spectrum in the sense that you might have, say, a system engineer designing multiple blocks of multiple boards, and they may say, "Okay. I think this board is pretty much locked down. Hey, you PCB design engineers. You can start working on the schematic for this one board." After those guys have started laying down the schematic, they can hand it off to the layout guy who can start doing basic layout. This is all happening concurrently, right? It's no longer a serial process, and then the big thing is if a change is needed, if an ECO is required, initiated from one side or the other, how efficiently does it pass from one person to the next?

So that's concurrency in what was traditionally a serial process from one discipline to the next, but we've also enabled concurrency within disciplines. We started with layout concurrency more than a decade ago. We've since added concurrency to the rest of the core flow of things like the schematic, so design engineers can work concurrently. They can enter constraints concurrently. They can layout concurrently. They can simulate concurrently. Then, for multi-board we added the capability for multiple system engineers to collaborate concurrently in designing that architecture as well. It's really concurrency across multiple disciplines.

Shaughnessy: It's been great talking to you, Dave. Thanks for your time.

Wiens: Thank you, Andy. **DESIGN007**

Light-bending Nano-patterns for LEDs



Nanoscale patterns designed to bend, deflect and split light can now be fabricated directly on light-emitting diode (LED) surfaces using an innovative etching method developed by A*STAR researchers. A new fabrication scheme creates new possibilities for the facile control of light output.

The light-emitting component of LEDs is a surprisingly simple structure, typically a thin layer of a dielectric material such as gallium nitride (GaN) on a crystalline sapphire substrate.

Egor Khaidarov and colleagues from A*STAR's Data Storage Institute and Nanyang Technological University have now found a way to pattern GaN with nanoscale features that can control the behavior of light.

"We have demonstrated that metasurface –surfaces patterned with features typically smaller than the wavelength of emitted light–can be fabricated directly on a standard GaN-on-sapphire platform," says Khaidarov.

Metasurface modifications of LEDs have been attempted in the past. These included patterning an additional layer with a very different refractive index than the underlying GaN-on-sapphire substrate to keep the light in the metasurface layer and enhance the light-matter interactions.

The resulting design, however, posed a major challenge for fabrication, requiring the team to develop a precise nanofabrication procedure involving electron beam lithography and fast, high-temperature reactive ion etching.

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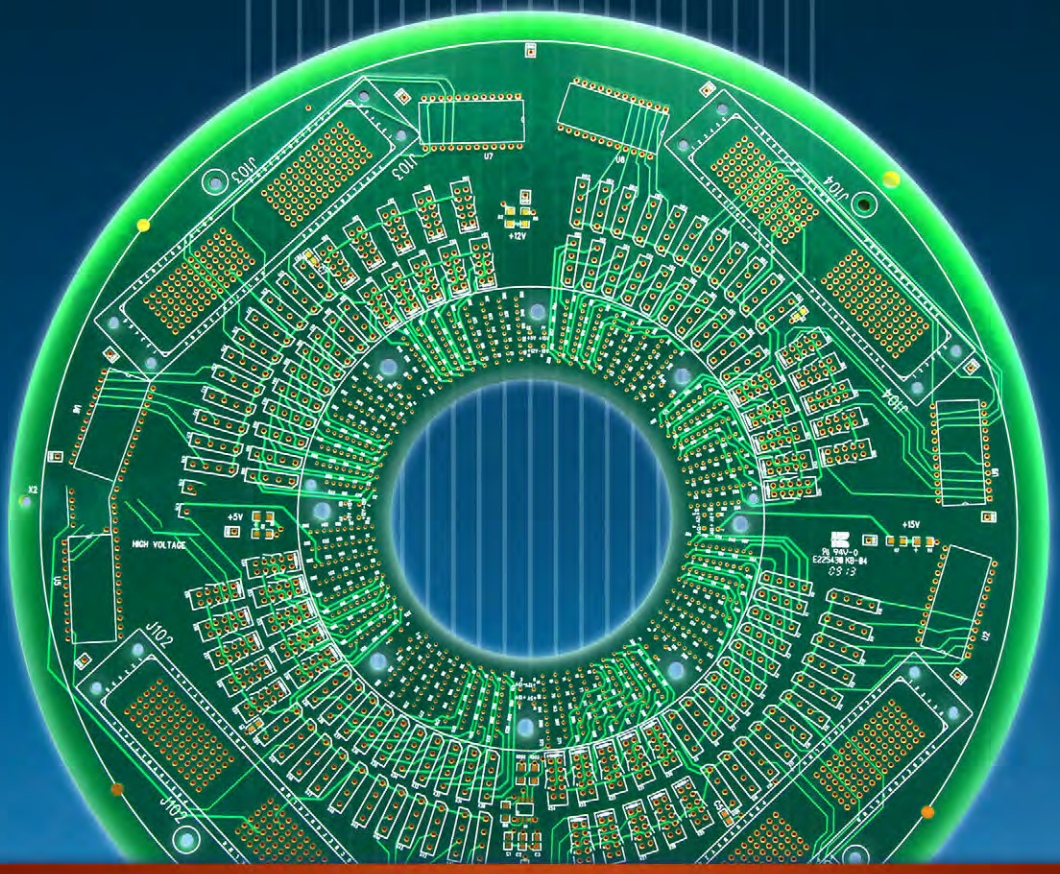

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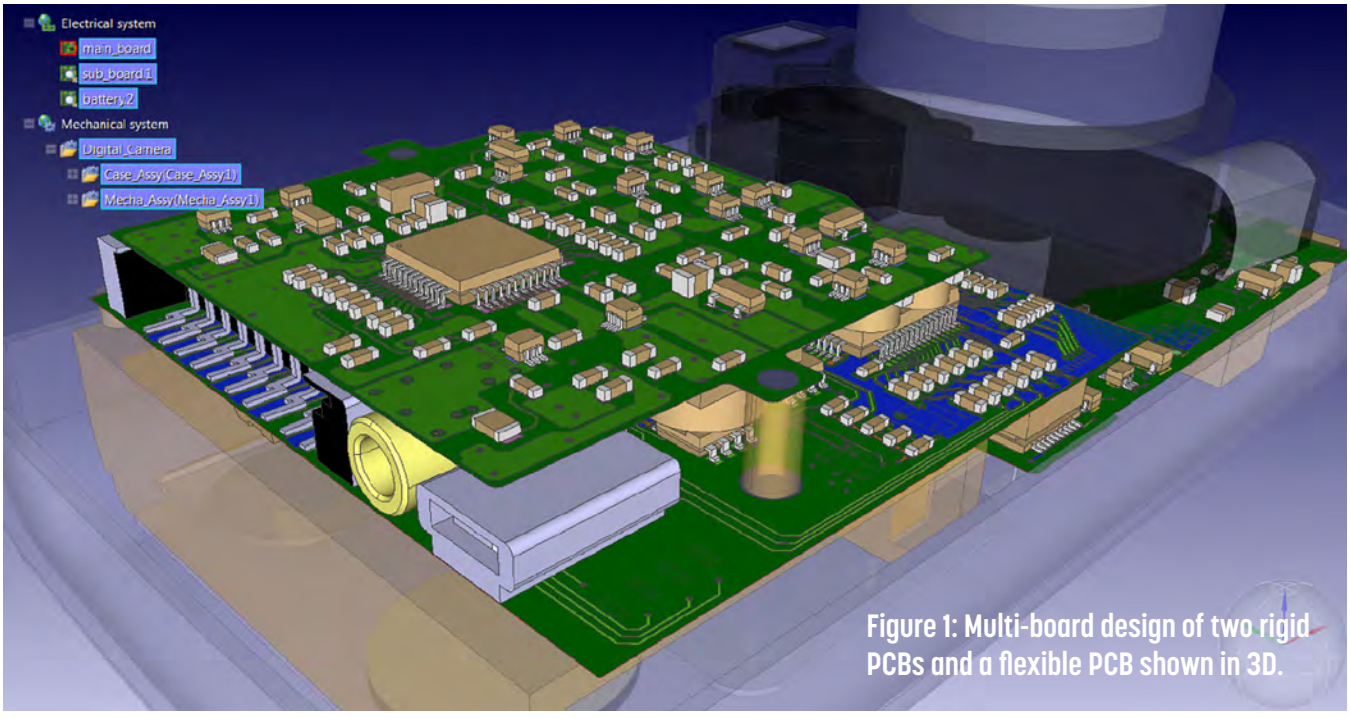

Figure 1: Multi-board design of two rigid PCBs and a flexible PCB shown in 3D.

3D Convergence of Multi-board PCB and IC Packaging Design

Feature by Bob Potock
ZUKEN USA

The electronic product design process is being challenged like never before, with the need to develop feature-rich, light, compact products at a lower cost, in less time. To address these challenges, designers are combining chips and boards in new configurations, such as complex 3D stacked structures, or new packaging technologies like package-on-package (PoP) and system-in-package (SiP). They are also embedding passive and active components on inner layers, inside cavities and within the dielectric of the board stack-up.

Traditional 2D PCB design systems are used to design one PCB at a time in isolation from the other PCBs within a product, and also in isolation from the ICs, packages, and enclosure. Validating connections between the PCBs, collision checking the boards to the enclosure, and reducing interconnection distance to the ICs requires time-consuming manual operations that are error-prone and limit the potential for reuse.

A new generation of 3D multi-board product-level design tools offer major improvements by managing multi-board placement in both 2D and 3D, and enabling co-design of the chip, package and board in a single environment. Multi-board design makes it possible to create and validate a design with any combination of system-on-chips (SOCs), packages, and PCBs as a complete system. Chip-package-board co-design enables designers to optimize routability via pin assignment and I/O placement to minimize layer counts between the package, chip and board. The new design methodology makes it possible to deliver more functional, higher performing and less expensive products to market in less time.

Multi-board Design Challenges

Today's complex multi-board electronic products create design challenges, such as planning and management of interconnects at

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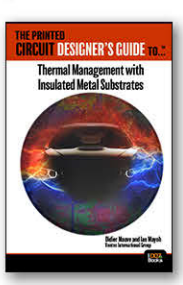

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the system level. In current-generation tools, the signal verification process for a multi-board design involves exporting pin lists that include net names for each board connector and correlating the net names to the master list of net names. In many cases, it's also necessary to manually verify each board connector's signal name. With mechanical engineers and board designers working with disconnected systems it's difficult, if not impossible, to intelligently manage connectivity and changes between boards. Using a spreadsheet or some other disconnected document to manage the large number of interconnects between the PCBs in the system is time-consuming and prone to error.

When mechanical engineers have inaccurate information on the electrical design or electrical engineers have inaccurate information on the mechanical design, the result in many cases is that batteries don't fit, mounting screws create shorts against PCBs, and connectors don't mate with packaging openings. Improper management can easily result in wasted product development time, scrapped boards and slipped schedules.

The combination of increasing capabilities, shrinking size and more complex external shapes means that electronics must increasingly consider the shape of the package while the mechanical design is more dependent than ever on the physical aspects of the internal electronics. Multi-board designs make ECAD-to-MCAD translation more difficult because of the need to communicate the position of connectors and other common points between the boards.

Yet in the current generation of tools, the collision-checking process involves exporting placement information, usually in IDF format, for each PCB to a mechanical engineer for assembly analysis. PCB design tools have continued to focus on working in 2D on one PCB at a time, with the electrical work done in 2D and then the 2D design being exported into 3D mechanical design software where the boards are positioned and checked for interference. The PCB designer is unable to, for example, position two boards on top of each other to see how they fit together. This is normally done after the board design has been exported to the mechanical design tool. Interdependencies between interlocking boards and their enclosure in complex products are critical.

The limitation of this approach is that if a problem such as an interference is identified, it's necessary to go back and forth between two different environments—PCB and mechanical design—to try and solve it. The other option is for a PCB designer to use a non-native viewer to conduct their own analysis. It is estimated that 50% of complex products require at least one additional PCB fabrication to address electro-mechanical issues. It is also very awkward to perform a high-level design study, such as

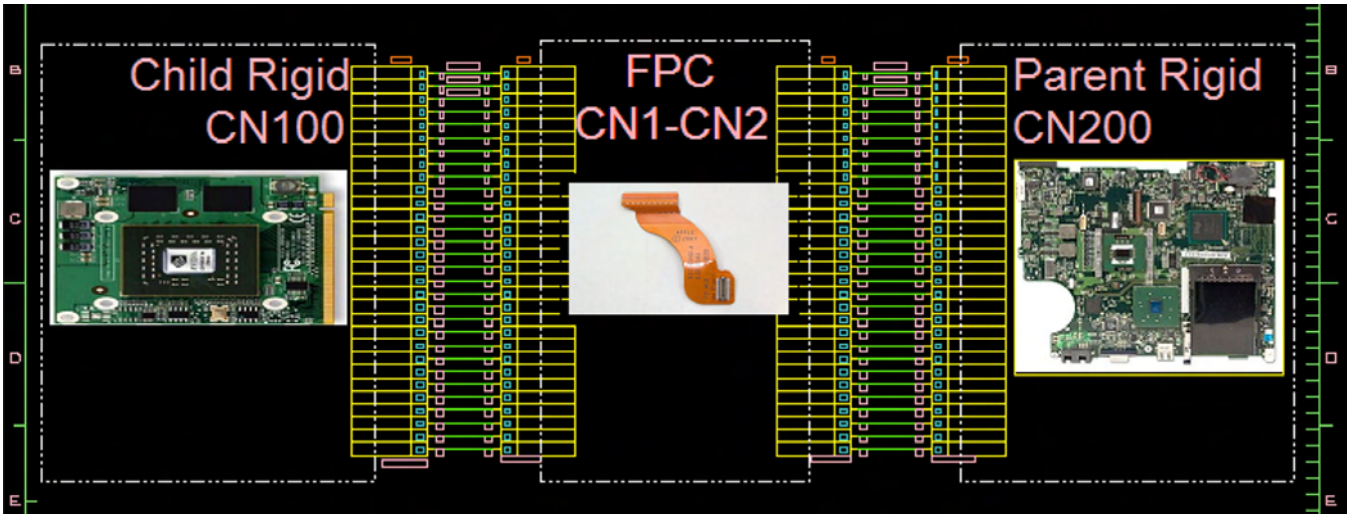

Figure 2: Today's products are competing on style, size, weight, cost, and function. A product-centric design process should be optimized for competitive factors.

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evaluating whether a two-board or three-board design is best, and which blocks should be allocated to which board.

3D Design Challenges

To compensate for increasing silicon costs, new packaging technologies have emerged to pack ICs more closely together. PoP structures are being used to connect logic and RAM ICs. SiP integration is being used to integrate multiple chips into a single package. And 3D-IC technology using through-silicon vias (TSV) is being used to reduce interconnect distance in stacked chip configurations. Meanwhile, PCB technology has evolved over the years with high density interconnect PCBs, high density packaging, embedded components and advanced I/O technology.

The greater complexity of these new packaging configurations is creating major challenges for packaging designers as well as for the PCB and IC designers who must integrate the package into their own work. Traditionally, the PCB, the IC and the package are each designed in their own stand-alone 2D environment. PCB design software has been enhanced to address technology advancements with improvements in routing, constraint management, and signal and power integrity analysis. But these improvements have largely been limited in scope to the PCB design process.

With increasing functionality, tighter cost constraints, and the decreasing form factor of today's products, such as portables, wearables and the Internet of Things (IoT), components need to be tightly coordinated with each other so that pin assignments can be optimized for small size and minimum layer count substrates. The overall goal is to align the board, package and chip so that each signal follows the shortest possible path from the chip to the board, resulting in the fewest possible layers in the package. With the lack of tool integration, but increasing design requirements, engineers have reverted to workarounds such as using spreadsheets and generic office productivity tools to perform planning and feasibility studies, and to define the tool interfaces and data transfer.

3D Design Tools Address Multi-board Design

A new generation of 3D multi-board, chip-package-board co-design tools addresses these challenges by providing an environment for system design that integrates 2D and 3D multi-board design along with the chip and package. Designers can manage all of the boards in the system in a single view to define the connections between them and then highlight the signal across each entity and analyze the entire interconnect length. The number, size, type and configuration

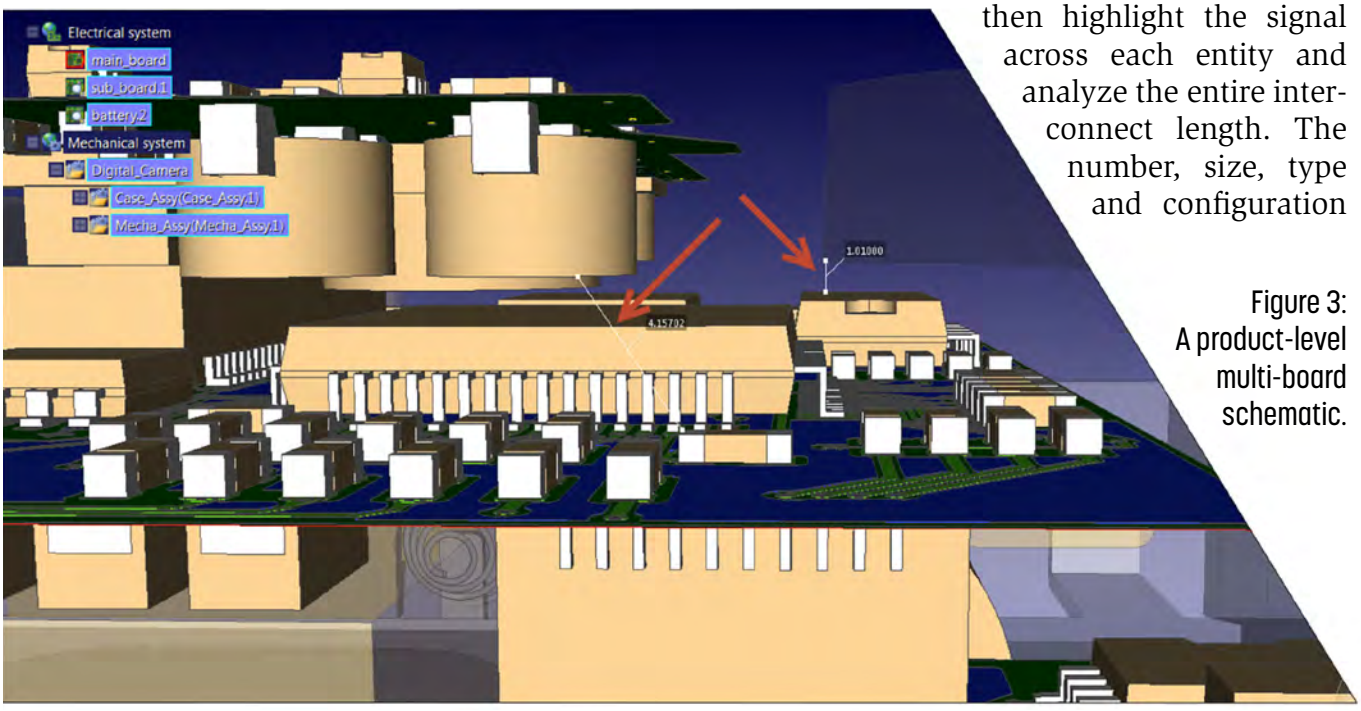

Figure 3: A product-level multi-board schematic.

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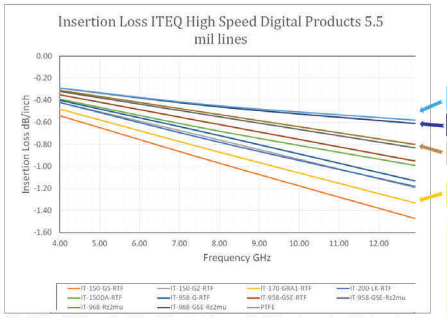

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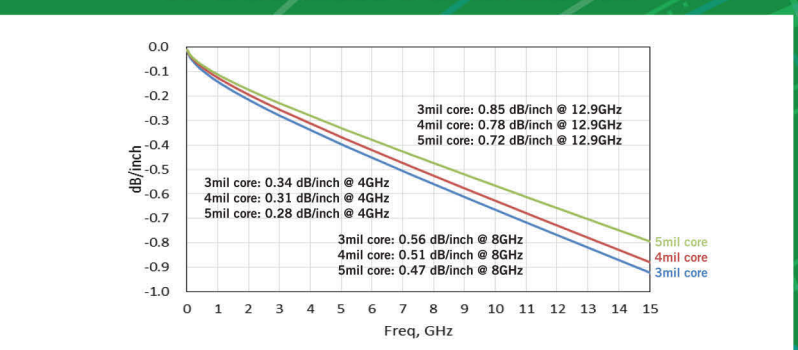
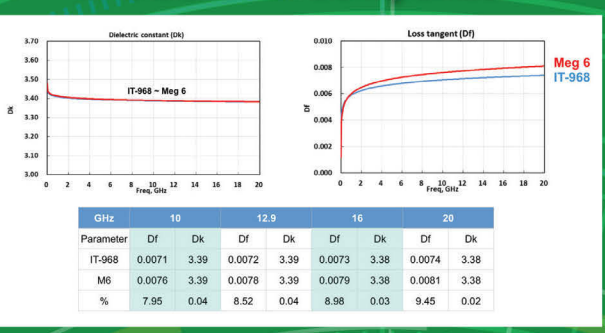


IT-968 SPP Comparison



GHz	10		12.9		16		20	
Parameter	Df	Dk	Df	Dk	Df	Dk	Df	Dk
IT-968	0.0071	3.39	0.0072	3.39	0.0073	3.38	0.0074	3.38
M6	0.0076	3.39	0.0078	3.39	0.0079	3.38	0.0081	3.38
%	7.95	0.04	8.52	0.04	8.98	0.03	9.45	0.02

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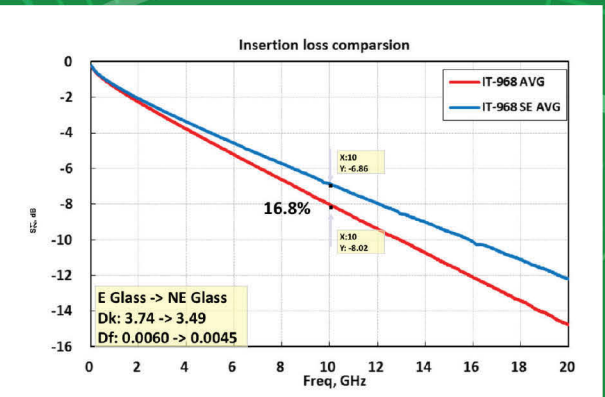
Tg (°C)	DSC	185	185
T-288 (w/ 1 Oz Cu, min)	TMA	120+	120+
Td-5%(°C)	TGA 5% loss	390+	390+
CTE (%), 50-260°C	TMA	2.2	2.2
Peel strength (lb/inch)	1 oz	6	6
Water Absorption	D-24/23	< 0.1	< 0.1
Dk , 1 GHz 2-10 GHz	IPC TM-650 2.5.5.9 IPC TM-650 2.5.5.13	3.8 3.8-3.7	3.4 3.4-3.3
Df , 1 GHz 2-10 GHz	IPC TM-650 2.5.5.9 IPC TM-650 2.5.5.13	0.0032 0.0038-0.0050	0.0028 0.0031-0.0040

E-Glass vs Low Dk Glass



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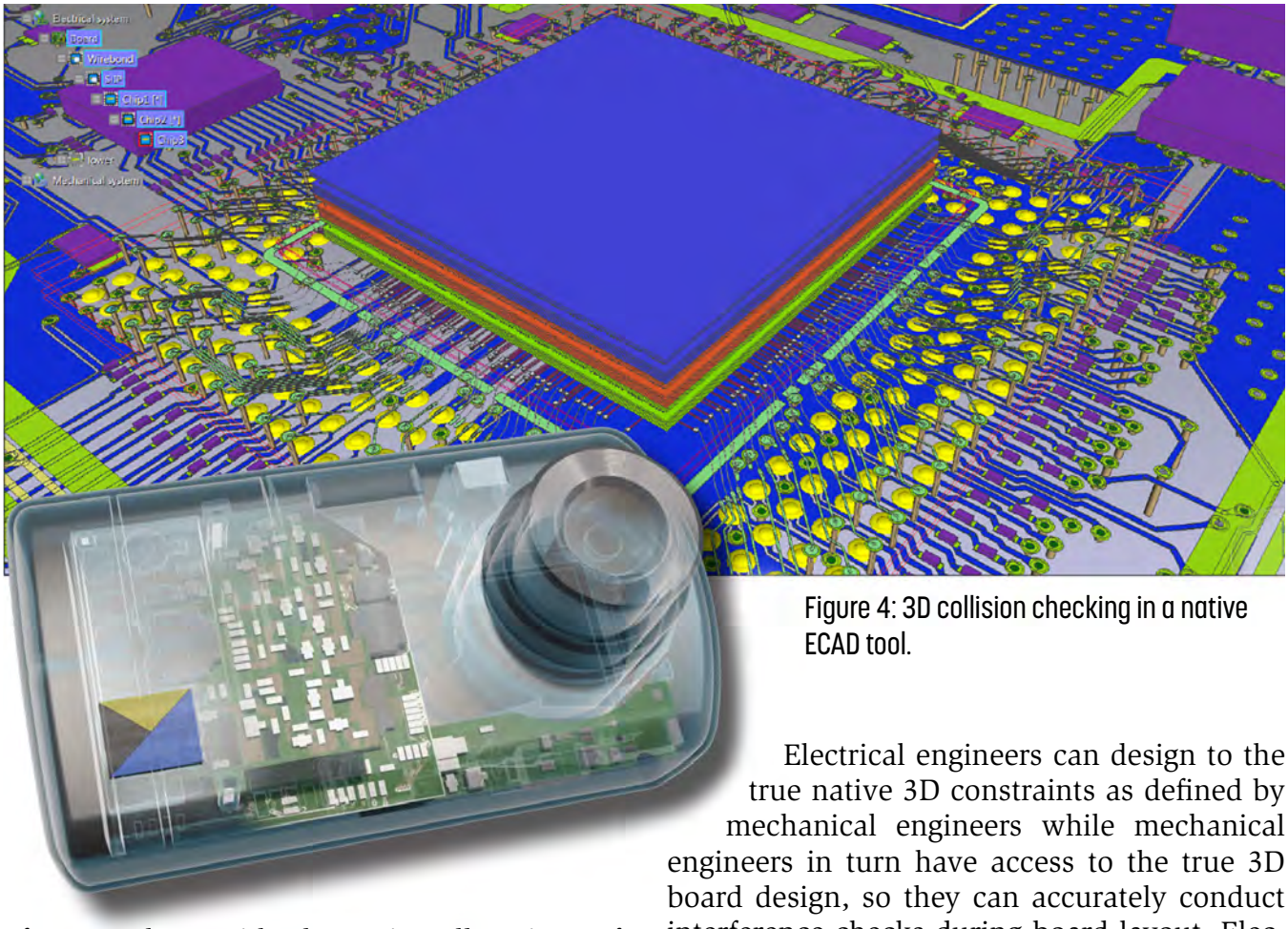


Figure 4: 3D collision checking in a native ECAD tool.

of PCBs, along with alternative allocations of functions across them, can be evaluated collaboratively with the ability to make trade-offs. Functional blocks can be assigned and moved between boards and boards can be reshaped, added and subtracted as necessary. The 3D multi-board design tool can address signal continuity at the system level while simultaneously managing multiple PCB interconnects and understanding board-to-board signal continuity.

PCB designers gain the ability to import the mechanical enclosure directly into the ECAD tool, so they can get single or multi-board designs right the first time. 3D parametric libraries are shared between the ECAD and MCAD systems. During layout, users invoke a wizard to import the 3D enclosure model and specify all the associated PCBs. They then layout the PCBs with the enclosure in real-time, optimizing placement capacity and capturing interference violations earlier in the design process.

Electrical engineers can design to the true native 3D constraints as defined by mechanical engineers while mechanical engineers in turn have access to the true 3D board design, so they can accurately conduct interference checks during board layout. Electrical engineers can design multiple boards within a single model to ensure precise positioning of angles, shapes and cuts needed to avoid interference. Working with the exact product shape makes it possible, for example, to fit more functionality into a package that is curved to conform to interior styling than could be accomplished with an orthogonal approximation. 3D ECAD design enables more accurate alignment of connectors so that they precisely fit openings on the enclosures.

Chip-Package-Board Co-Design

By integrating planning and final design for PCBs, packages and ICs in a single view, the newest generation of tools makes it possible for engineers to conduct system-level co-design of the PCB, package and chip and optimize I/O placement, pin assignments, redistribution layer (RDL) routing, and bump and ball placements. The benefits are particularly great when working with non-traditional structures

with routing complexity in both vertical directions such as PoP, SiP, chip-scale packaging and 3D-IC/3D packaging. The new tools also automate routing of the chip RDL and package escape, reducing pathfinding cycle time and making it possible to optimize die bump placement. The new approach makes it possible to study the trade-offs involved in using different numbers of package layers while simultaneously considering RDL routing on the IC side and the escape route on the PCB side in a single design view. Advantages of the new approach include lower RDL, interposer/substrate and package layer count, improved signal integrity and faster time-to-market.

Each person working on the project can see their piece of the puzzle in the context of the full product, making it easier to optimize pin assignments and avoid connectivity errors. For example, package/IC bump assignment can be performed while viewing the effects on the rats nest at the PCB level. The designer can observe the potential impact at the package and IC level of making automatic or interactive pin swaps at the board level to improve PCB routability. The pin swap operation is automatically communicated between the package and PCB databases, eliminating the need for CSV or other neutral files to communicate the change. Multiple engineers can work simultaneously on a single substrate because the tool enables engineers to lock the package design. If a designer needs to make a pin swap in a locked package design, they can send a notification that the other engineers can accept or reject as an ECO.

Simulation

The effects of changes from a signal integrity, power integrity or thermal point of view can be determined by performing multidiscipline, multi-physics analysis with solutions from providers such as Keysight Technologies, ANSYS, AWR, CST and Synopsys. The co-design environment enables signal traceability across the complete system. Signal paths can be reviewed and analyzed as they cross design and component boundaries from drivers through the system interconnect to receivers. Intelligent and integrated schematic- or layout-based simulation environments support multiple design flows.

Conclusion

The move from coplanar designs to complex 3D stacked structures and embedded devices is driving the need for tools that can accurately render and provide meaningful visual and DRC feedback to enable, rapid right-the-first-time

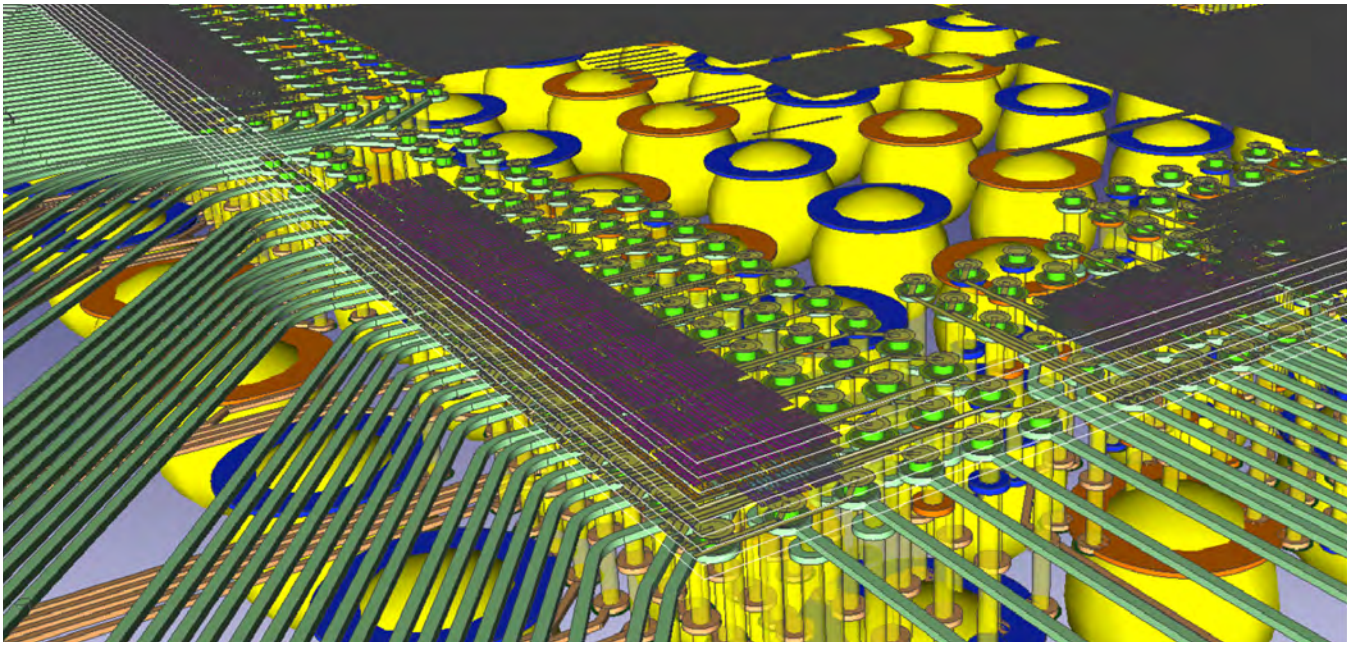
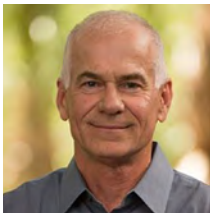


Figure 5: Co-design environment for chip, package, and board in 3D.

designs. The new generation of 3D multi-board product-level design tools enable real-time 3D hierarchical design, allowing design teams to concurrently create any combination of advanced stack dies, packages and PCBs. With a native 2D and 3D architecture, designers can effectively co-design a chip, package and board to optimize I/Os at each level, embed components in the dielectric of a stack-up intelligently, and verify manufacturing rules in real-time. Next-generation tools manage multiple boards and their associated enclosures simultaneously and provide collision checking directly in the native ECAD tool. The new integrated 3D multi-board chip-package-board co-design environment makes it possible to holistically optimize the package, board and IC design to a greater degree than was possible in the past with the end result being higher performance and lower manufacturing costs. **DESIGN007**



Bob Potock is vice president of marketing for Zuken USA.

Turbocharge for Lithium Batteries

A team of material researchers from Jülich, Munich, and Prague has succeeded in producing a composite material that is particularly suited for electrodes in lithium batteries. The nanocomposite material might help to significantly increase the storage capacity and lifetime of batteries as well as their charging speed. The researchers have published their findings in the journal Advanced Functional Materials.

Lithium-ion batteries are the ultimate benchmark when it comes to mobile phones, tablet devices, and electric cars. Their storage capacity and power density are far superior to other rechargeable battery systems. Despite all the progress that has been made, however, smartphone batteries only last a day and electric cars need hours to be recharged. Scientists are therefore working on ways to improve the power densities and charging rates of all-round batteries. "An important factor is the anode material," explains Dina Fattakhova-Rohlfing from the Institute of Energy and Climate Research (IEK-1).

One way of addressing this problem is hybrid materials or nanocomposites - composite materials that contain nanoparticles. The scientists developed a material comprising tin oxide nanoparticles enriched with antimony, on a base layer of graphene. The graphene basis aids the structural stability and conductivity of the material. The tin oxide particles are less than three nanometres in size - in other words less than three millionths of a millimetre - and are directly "grown" on the graphene. The small size of the particle and its good contact with the graphene layer also improves its tolerance to volume changes - the lithium cell becomes more stable and lasts longer.

"The nanocomposite anodes can be produced in an easy and cost-effective way. And the applied concepts can also be used for the design of other anode materials for lithium-ion batteries," explains Fattakhova-Rohlfing. "We hope that our development will pave the way for lithium-ion batteries with a significantly increased energy density and very short charging time."

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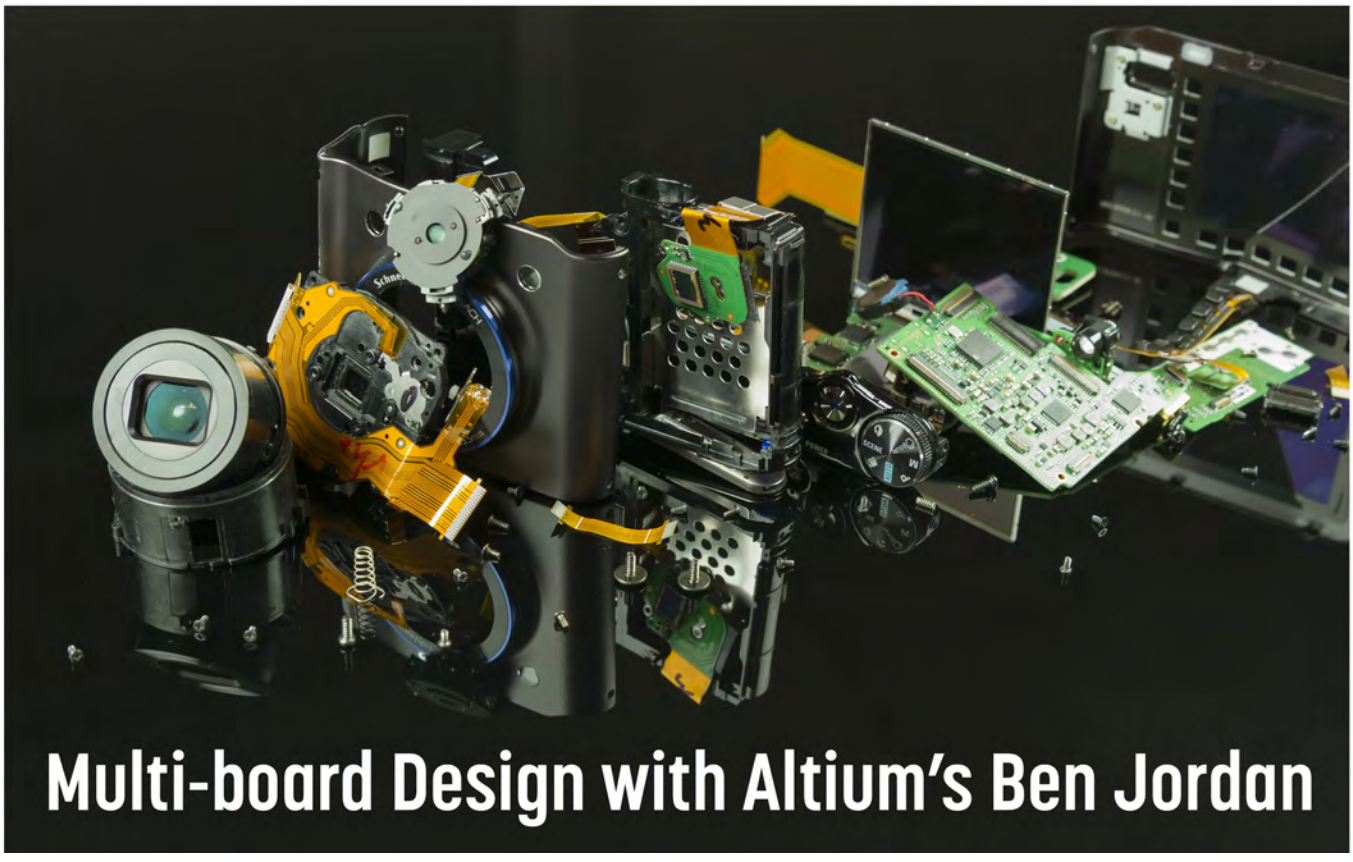

Multi-board Design with Altium's Ben Jordan

Feature Interview by Andy Shaughnessy and Stephen Las Marias
I-CONNECT007

Not too long ago, historically speaking, most electronic products contained only one PCB. But multi-board designs have become almost ubiquitous over the past decade, and EDA software companies are working to improve and simplify the multi-board design process. For this issue of *Design007 Magazine,* Editors Andy Shaughnessy and Stephen Las Marias spoke with Ben Jordan, director of product and persona marketing for Altium, about the company's multi-board design tools, the challenges that customers face, and the numerous trade-offs that designers must contend with while performing multi-board design.

Andy Shaughnessy: Ben, why don't you begin by telling us about multi-board design and multi-board EDA tools.

Ben Jordan: Multi-board design is, from my and Altium's point of view, simply the challenge of designing systems where there is more than one printed circuit board. It's not a complicated concept, and many of Altium's engineers and product managers have come from a background of designing new electronics. We even had our own internal hardware team for some time, doing the FPGA development boards. So we had some pretty high-end designers, people like Dave Jones, who runs the EEV blog now, and some of his colleagues back in Australia. We also had the team in Shanghai for a while doing IoT modular design. This all ended up being multi-board systems design.

Ben Jordan

One reason engineering firms do multi-board designs is to divide and conquer. We want to partition a bigger product into smaller modules to make the task of designing those modules and testing those modules as individual clusters of functions that sort of make sense

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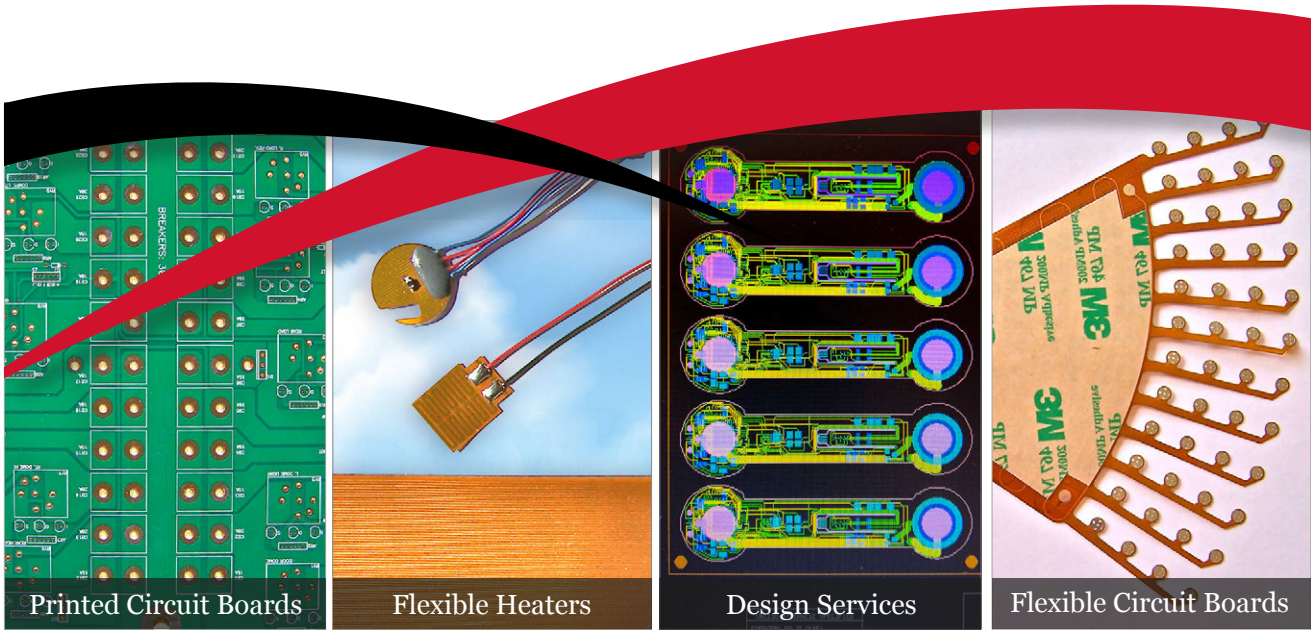

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together. You have the upside of being able to properly test and measure, and control supply chain issues, and design for fabrication and assembly if you have the ability of breaking up a large, complex product into small replaceable units.

This is not just for electronics; this is not a new concept. It's done in every other industry. We know that just about every professional PCB designer at some point is going to be designing a board, if they are not already, that's just one board in a larger system, and they may be involved in designing a larger system and integrating those modules. It makes sense that a mainstream professional development tool should have multi-board capabilities and shouldn't be considered a high-end feature.

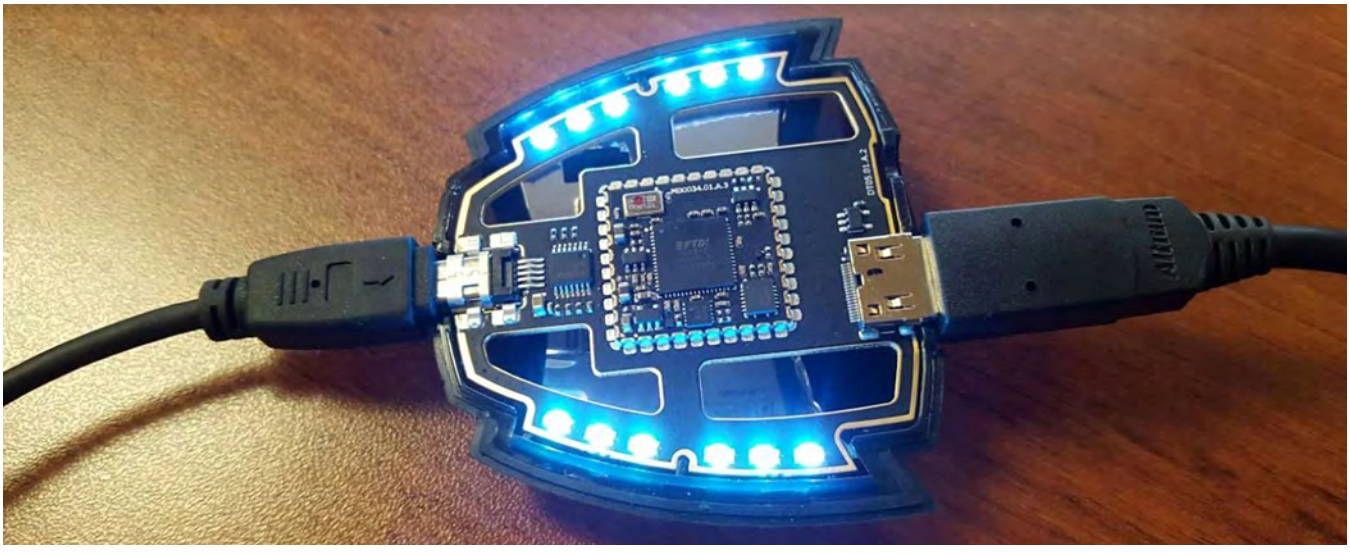
It took a while because it required a new 3D modeling engine for doing 3D properly and efficiently; bringing multiple large complex PCB designs into a single editor workspace requires a lot of memory and computing power, otherwise the whole thing becomes unusable. So that was a big challenge for us, and it took some time, but we've finally been able to release that for Altium Designer 18.

We took the company into IoT experimentation in Shanghai. We've implemented stamp-based form-factor modules, and we were doing our FPGA development boards, the NanoBoard NB1, the NanoBoard 2, and NanoBoard 3000, which were all multi-board modular systems that could reconfigure the platform. We encountered all the challenges that people have with manufacturing boards of different layer stacks, but how do you optimize that? Is there a way the tools can offer you a way of analyzing and checking layer stack compatibility, so you can consolidate and make the best use of panel space fabrication?

Shaughnessy: What are some of the challenges designers typically face in multi-board design?

Jordan: One that is a real pain in the derriere is connectivity management.

Connectivity management is a big piece of the problem, because it's so common for a component library in the CAD tool to look at the 3D model and the footprint (or decal or pattern, depending on what CAD tool you come from) with the mating face top down. The footprint for the connectors that you are using traditionally has them all numbered starting at the top left, anti-clockwise. In other words, you have a plug and you have a socket, and when the receptacle is reversed on the bottom side of one of the modules, because it's got it sandwiched down on the baseboard, your pin numbering is mirrored, and it's a problem. These cause headaches with managing pinouts. Then there's the other side of it where you want to be able to swap some things around to optimize the layout and routing on one of the modules,



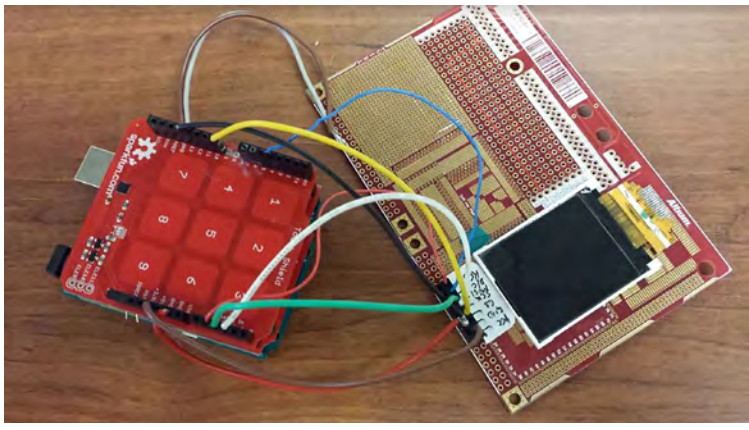
and you need to be able to propagate changes like that throughout the broader system. So, connectivity management should be a part of pin-swapping as well.

Looking into the future, we've solved the basic pin assignments, connectivity management, and synchronization of pin swaps on the schematic side. What we have not yet done, but it's on our road map, is model the cables. There's a multi-board assembly and there's cable connectivity between them. Maybe a single wire or a multi-point cable or a harness. We don't compete with the MCAD tools which do a fabulous job of modeling cable harness assemblies, and it's not in our plan to try to do what they do; SolidWorks Electrical is fantastic. But the goal is to model wire and cable to a level where a PCB designer can actually make sure they are specifying the basics of it, saying this goes to here and here and joins these boards together, and it has to sit in this kind of envelope in 3D, and it's got these connections, and these signals travel through it, and we can swap pins again.

There's a lot more we could do in this space, in this domain with problem solving, I think. We haven't done anything with power integrity or signal integrity, for example. But that is definitely something that has to be considered with multi-board design. Speaking of power integrity, it's very easy to forget that you have one PCB and if you test that one PCB, it will pass EMI requirements in isolation. You make that a part of a multi-board system where there are signals going across connectors and return paths may be forced around the design through power cables in strange ways, if you can't design your connectivity right.

Individual modules may well pass for FCC regulations or CE regulations, and then completely fail once you integrate the whole system together as a multi-board assembly. So, these are the kinds of issues we have to think about.

Shaughnessy: One of challenges that designers talk about with multi-board design is virtual prototyping. What's your take on multi-board virtual prototyping?



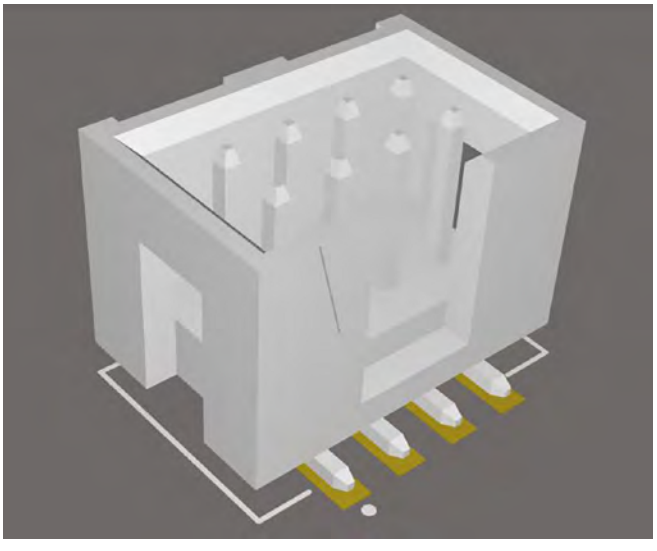
Jordan: That's kind of a buzz phrase in our industry. The first time I read that was in marketing about three years ago, and it was always related to simulation. But simulation has been around for a long time. Let's call it virtual prototyping today. Maybe it's a little more than that. It's simulating the whole system, and that's really actually very difficult to do. I think on the engineering side, people have been talking about simulation-based design. That's something that MathWorks would talk about with MATLAB and maybe PTC with Mathcad and some of those analysis simulation tools that take a high level programming language. I think there are opportunities for us to integrate that more into the front-end design process. But as a basic starting point, we really do need to consider modeling power integrity.

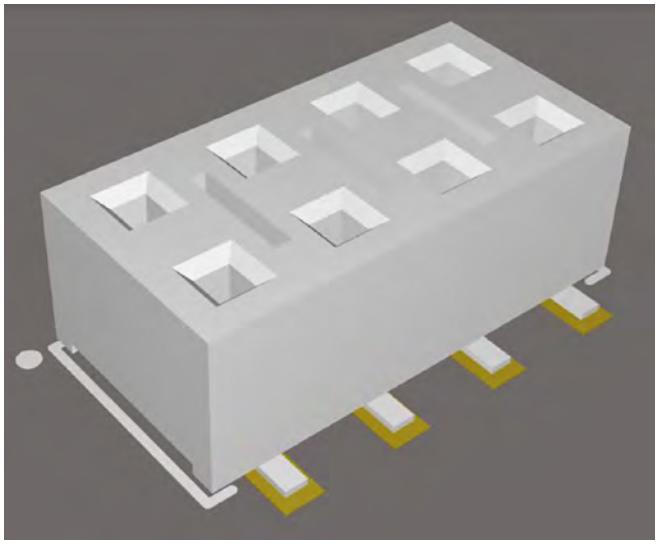
We do have tools for simulation in Altium Designer. We've had that for a long time, so you can do mixed analog and digital simulation from our regular PCB design schematic editor. It supports Spice 3F5, PSpice models, and Digital SimCode. You can do mixed-mode analysis for actual functional prototyping. Not many people know too much about those features or use them regularly, but the engineers know about it. Front-end engineers use it in small ways if they are designing a new circuit they'll simulate. Most of the time they don't bother, because they're using circuit design principles they have been using for a while, and they know it's good. Or they're just following the data sheet for a chip and hooking it up the way the application note says, and they've prototyped it on the bench and it works.

I could foresee that in the future, we should extend that capability to do DC Power Delivery network analysis across multiple boards and through connectors. That will take a fair bit of work and take us some time, and I'm not promising that that's what we are going to do, but I could foresee that we would endeavor to do that because power supplies in a multi-board assembly are critical. Sending power and having ground returns appropriately assigned to pins on connectors in multi-board assemblies is critical to even the AC function of the design.

Shaughnessy: How do designers figure out the cutoff, or the break-even point, for going the multi-board route? It seems like there would be a lot of trade-offs.

Jordan: Has anyone ever tried to draw a Venn diagram with all of the trade-offs with PCBs? I think it's impossible. You'd have so many bubbles and some of them would never overlap, so you couldn't actually find that happy medium. At the same time, I can understand why a tool you have developed for yourself would work, but also be complex. I think there's promise there. If one can make some assumptions about the kind of product that you're designing or what its target industry or position is, in the broader system, then there are certain lists of assumptions can be made about some of those trade-offs; and that can simplify the decision making.





Shaughnessy: So, how would you sum up what we've discussed regarding multi-board design?

Jordan: There are really three elements to this. One is design for proper function and that involves the latest in signal integrity, power integrity, pin assignments on connectors, and making sure you have proper return path designs so that you don't get electromagnetic radiation problems. Coupled with that, we as an industry still need to solve that problem of making sure everything works together as an integrated bundle of boards versus just the individual modules.

The second thing is the 3D assembly and making sure all the parts fit, and that's associated with the bill of materials as well. Design for assembly is an exponentially more complex thing when you're dealing with multi-board systems, because you've got to assemble the individual parts but also the overall system, and I think our industry could improve or augment our existing DFA practices. I think IPC could help with this to define DFA guidelines for multi-board assemblies so that contract manufacturers can do final module integration and test—design for excellence, basically.

And the third thing is integration of the design practice into the broader organization. PCB design is so complex that it's very easy to fall into the fissure of that narrow space of only considering the boards; it's very important to consider the broader implications: We're designing a multi-board system, and it's part

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of an overall mechanical assembly or product. We need to be able to document things property for final assembly, and being able to modify individual modules, because this is something that we tend to do now, really. You can move components on modules to interface correctly module-to-module, but you can also do it with the broader enclosure. And that's just really a starting point, but this affects the overall mechanical assembly and that has implications for PLM systems, enterprise resource planning, and production for the broader product; also, in the electronics assembly, there may be contract manufacturer's implications, mechanically. I consider things like custom plates that have to be milled to cover certain areas of the board as it's going through soldering processes, for selective conformal coatings or selective soldering, or these kinds of things. These are all issues.

Stephen Las Marias: In our experts' meetings, we often hear about the importance of fabricators and EMS companies talking to designers. It seems like communication would be even more important with multi-board designs.

Jordan: Yes. I have one great example of a power supply factory that a colleague visited, that was showing us that they were designing PC power supplies. They make hundreds of thousands of these things. And they redesigned the whole PCB just to be able to move one mounting screw and mounting hole half an inch, because it affected the assembly process, and they wanted the factory workers, or robots, to be able to screw the screw in at 90 degrees to the board instead of with a slight angle on the screwdriver.

It's sometimes impossible for the PCB designer to be aware of all the potential issues of assembly, and it has a profound impact on the industry. Having a closed loop from the CM back to the designer is absolutely necessary for improving efficiencies, and it's worth spending an extra day on design if it cumulatively saves many weeks of human labor down the line.

Shaughnessy: Well, is there anything we might have missed?

Jordan: I'm satisfied that we've covered the main boulders.

Shaughnessy: Thanks for your time, Ben. **DESIGN007**

Robots Learn by Checking in on Team Members

The software and hardware needed to coordinate a team of unmanned aerial vehicles (UAVs) that can communicate and work toward a common goal have recently been developed by KAUST researchers.

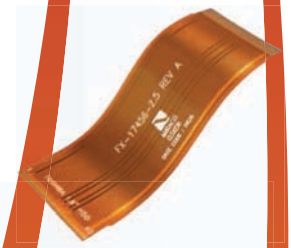
"Giving UAVs more autonomy makes them an even more valuable resource," says Mohamed Abdelkader, who worked on the project under the guidance of Jeff Shamma. "Monitoring the progress of a drone sent out on a specific task is far easier than remote-piloting one yourself. A team of drones that can communicate among themselves provides a tool that could be used widely, for example, to improve security or capture images simultaneously over a large area."

Abdelkader and the team quickly dismissed the idea of having a central base station that the drones would communicate with. Instead, they custom-built UAVs and incorporated a light weight, low-power computing and wi-fi module on each one so that they could talk to each other during flight.

"Each of our drones makes its own plan based on a forecast of optimistic views of their teammates' actions and pessimistic views of the opponent's actions," explains Abdelkader.

Their algorithm worked well in both indoor and outdoor arenas under different attack scenarios. Abdelkader hopes their software, which is now available as open-source, will provide the test-bed for multiple applications.

Engineering And Providing Balanced Interconnect Solutions



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PCB007 Highlights

Unimicron Germany Rises from the Ashes with New Smart Factory ▶

This is a review of the grand opening of Unimicron's new smart factory in Geldern, Germany. A fire in a PCB shop is an experience we all dread, but still it happens, and the consequences can be devastating. In the early hours of December 28, 2016, the innerlayer production plant at RUWEL International in Geldern caught fire and the whole factory and its contents were destroyed.

Chin-Poon PCB Plant Fire to Affect 15% of Revenues ▶

Chin-Poon Industrial, which has more than 70% of its revenues from the automotive electronics industry, has estimated that losses resulting from a deadly fire at its production site in Taoyuan, Northern Taiwan on the evening of April 28 will amount to about NT$300 million ($10.2 million).

Flex Talk: Something New for Everyone ▶

Whether you are new to single- and double-sided flex, moving into rigid-flex construction, thinking of using bookbinder technology, or investigating an additive process, working with new technology can be both exciting and challenging.

AT&S Offers a Look into the Future of Connection Technology ▶

AT&S presented innovative technologies and trends in connection solutions at the 14th AT&S Technology Forum. Numerous interested customers were able to find out about the latest developments in the electronics and printed circuit board industry for areas such as mobile devices, automotive, industrial, communications and medical technology and to exchange views with the AT&S experts.

Printed Circuits Upgrades Photo Department ▶

Flex and rigid-flex circuit board manufacturer Printed Circuits has added two new pieces of equipment to their photo department including a new Orbotech Paragon 8-watt laser direct imager and a Fusion 22 automatic optical inspection machine with laser via inspection capabilities.

It's Only Common Sense: Silence is Not Always Golden ▶

A few years ago, I worked with a client that won and then lost 30 customers all in the span of 10 months. They had bought the customer base of a company that was going out of business.

The Right Approach: the Rebirth of Made in America ▶

I have been on the record for the past 10 years saying that jobs we lost overseas may move out of China to a new low-cost country, but they were never coming back. I have never been happier to be wrong! I talk to a lot of CEOs, and the first question I ask is, "How's business?" The answers are overwhelmingly positive, and it is clear that their optimism is at a level not seen for over a decade. America as a low-cost country. Think about that.

Nano Dimension Sells Three Printers, Opens Customer Center at U.S. HQ ▶

Nano Dimension Ltd. has announced new sales of the DragonFly 2020 Pro 3D printer to three prominent American customers. Nano Dimension also announced the opening of its third Customer Experience Center co-located with the company's U.S. headquarters in Santa Clara, California.

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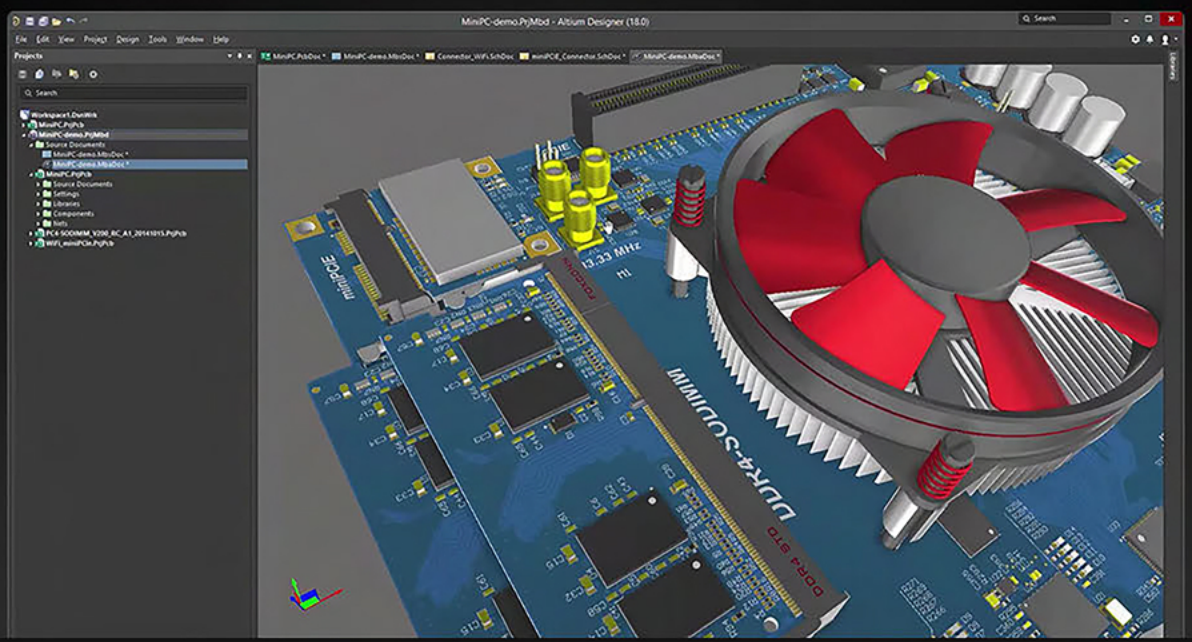

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DDR3/4 Fly-by Topology Termination and Routing

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

DDR3/4 fly-by topology is similar to daisy chain or multi-drop topology, but it includes very short stubs to each memory device in the chain to reduce the reflections. The advantage of fly-by topology is that it supports higher-frequency operation and improves signal integrity and timing on heavily loaded signals. If you are employing high-frequency DDR4, then the bandwidth of the channel needs to be as high as possible. However, with today's extremely fast edge rates, the sequencing of the stubs and the end termination, and the associate load, can make a measurable difference in signal quality. In this month's column I will look at how best to route DDR3/4 fly-by topology.

Reflections occur whenever the impedance of the transmission line changes along its length. This can be caused by unmatched drivers/loads, layer transitions, different dielectric materials, stubs, vias, connectors, terminations and IC packages. By understanding the causes of these reflections and eliminating the source of the mismatch, a design can be engineered with reliable performance. For perfect transfer of energy and to eliminate reflections, the impedance of the source must equal the impedance of the trace, as well as the impedance of the load.

As signal rise times increase, consideration should be given to the propagation time and reflections of a routed trace. If the propagation time and reflection from source to load are longer than the edge transition time, an electrically long trace will exist. If the transmission line is short, reflections still occur but will be overwhelmed by the rising or falling edge and may not pose a problem. But even if the trace is short, termination may still be required if the load is capacitive or highly inductive to prevent ringing.

Series termination is an excellent strategy for point-to-point routes, one load per net.

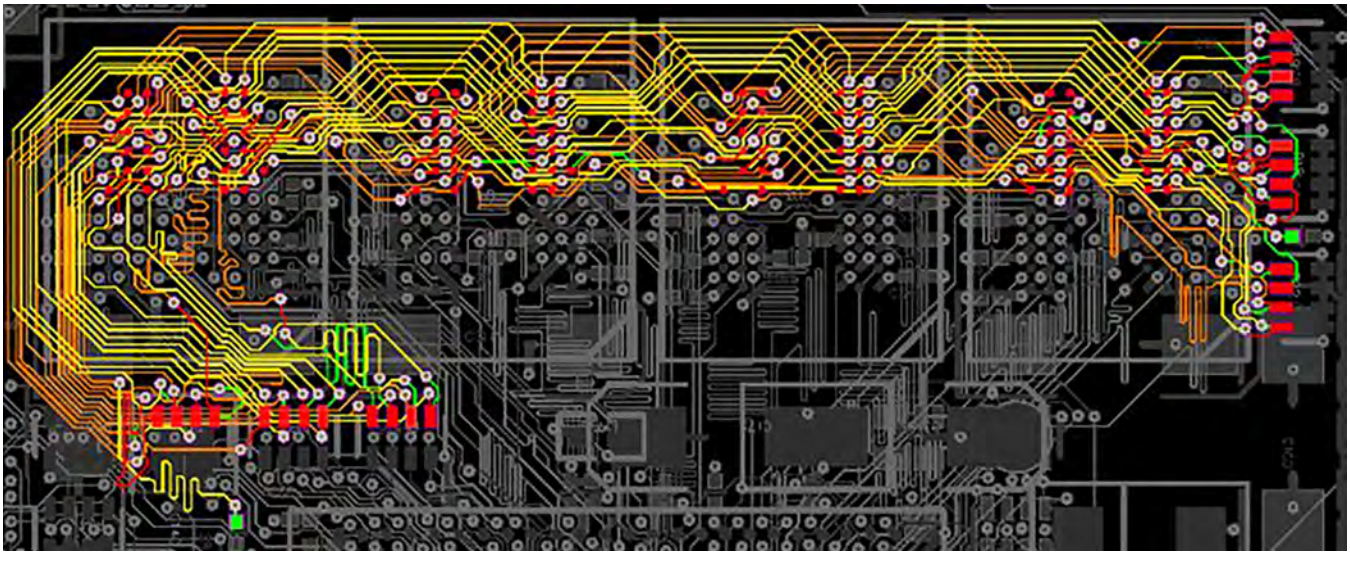
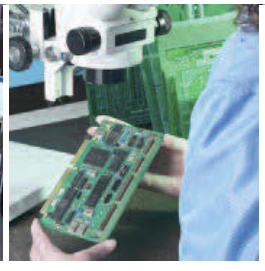


Figure 1: Fly-by topology for clock, address and command routing.



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Whereas parallel (end termination), is preferred for busses with a number of loads in a multi-drop topology. For DDR3/4 layouts, a series termination is generally not required for on-board memory devices. However, if your design has plug-in memory then the data and data mask signal length may be excessive and require a series termination.

With the fly-by address, control and command (ACC) signals, the traces should be routed as practicable as possible to the memory device pins and the parallel termination placed at the end of the line as in Figure 1. Short stubs can be used to connect the passing signal to each memory device in sequence but the longer the stubs the higher the capacitance. This stub capacitance, along with the parasitic input capacitance of the receiver pin, creates an imperfection in the termination network.

When implementing parallel terminations, it is not always possible to place the termination after the final load in a multi-drop topology due to real estate restrictions. Figure 2 shows the schematic of this configuration. If the stub is very short and the signal edge rate is not excessively fast, then this may be acceptable. However, as the edge rate increases, the extra capacitance of the stub is significant and creates reflections.

When the first incident wave arrives from the driver, part of that wave, which is a small pulse, bounces off the imperfection and returns to the driver. This pulse bounces again off the low-output impedance driver and returns one round trip later to the receiver. What we observe at the receiver is the initial rising edge, followed one round trip later by a secondary pulse. If the initial reflected pulse is sufficiently

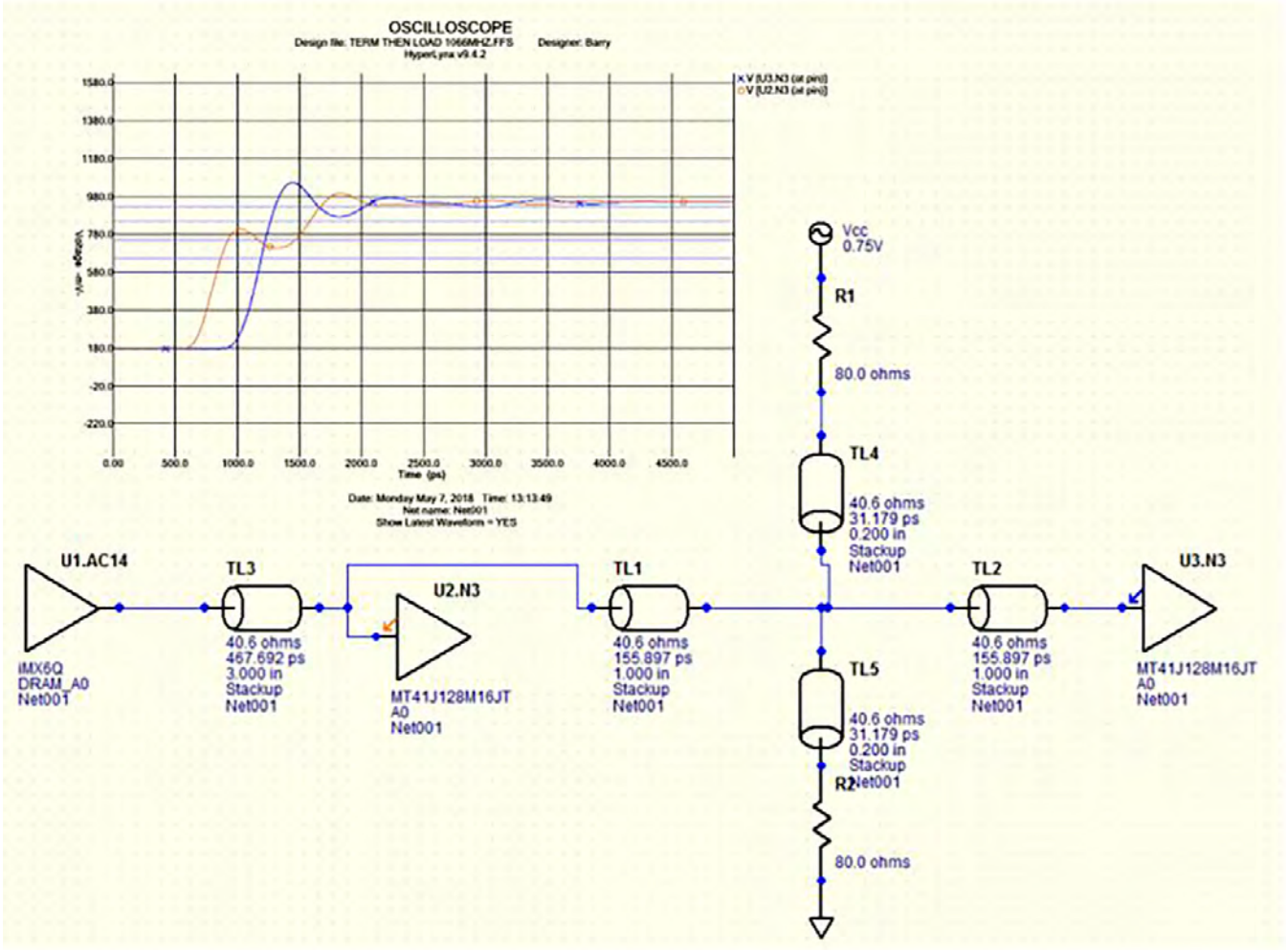


Figure 2: DDR3 address signal with termination before final load (all simulations performed in HyperLynx).

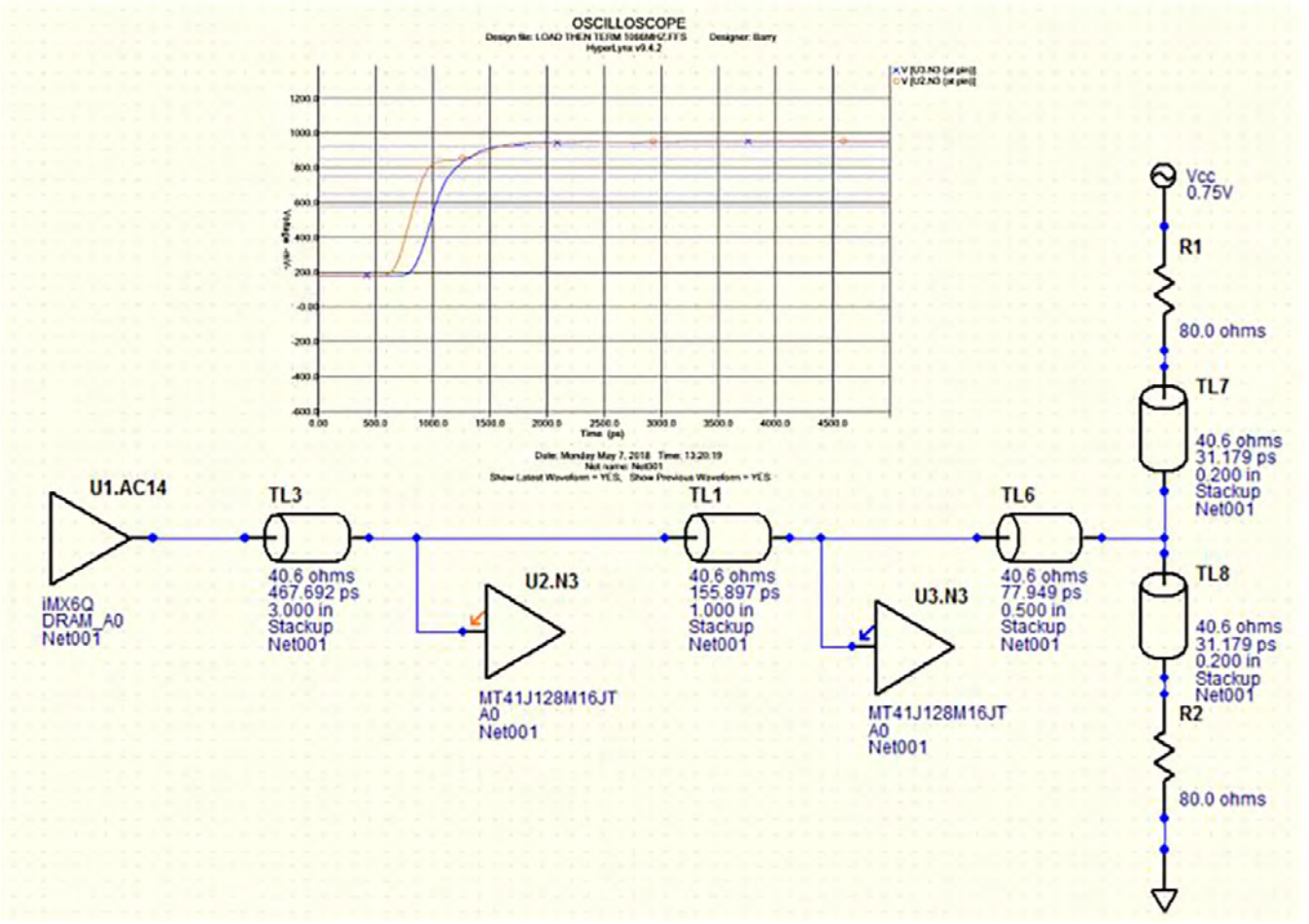


Figure 3: DDR3 fly-by topology with termination after final load.

small, all subsequent reflections will be negligible. However, in this case, the reflection causes a non-monotonic edge at the first receiver (orange waveform), which could lead to false triggering of the receiver. If for example, there are four memory chips on the address line, then this would occur on all receivers except the last to a similar extent.

Figure 3 illustrates a typical DDR3 fly-by topology with the termination at the very end of the final load. Also, the passing address signal trace goes directly to the receiver pins with no stub. This is the ideal scenario. In this case, there are no reflections, from the termination, which can be seen from the waveforms.

Now let's add a half inch stub from the passing address signal trace going to each receiver input pin, as I have seen many designers do. Figure 4 shows the schematic and the resultant waveforms. The reflections created by the additional capacitance, of the stubs, is not quite as bad as that of Figure 2, which had the termination before the final load. However, this demonstrates the impact of stubs on the ACC signals in the fly-by topology. Figure 5 shows the jitter and noise created by the half inch stubs on the signal.

After running a few more, quick simulations in HyperLynx LineSim with varying stub lengths, I found that the stub length can be no more than 200 mil, to alleviate the impact of the reflections, in this (typical) case. This results in the reasonably clear eye diagram of Figure 6.

In conclusion, DDR3/4 fly-by parallel terminations should be placed after the last receiver at the end of the transmission line and routed directly to the last receiver. Since there is no reflection from this topology, this implies that the length, from last receiver to the termina-

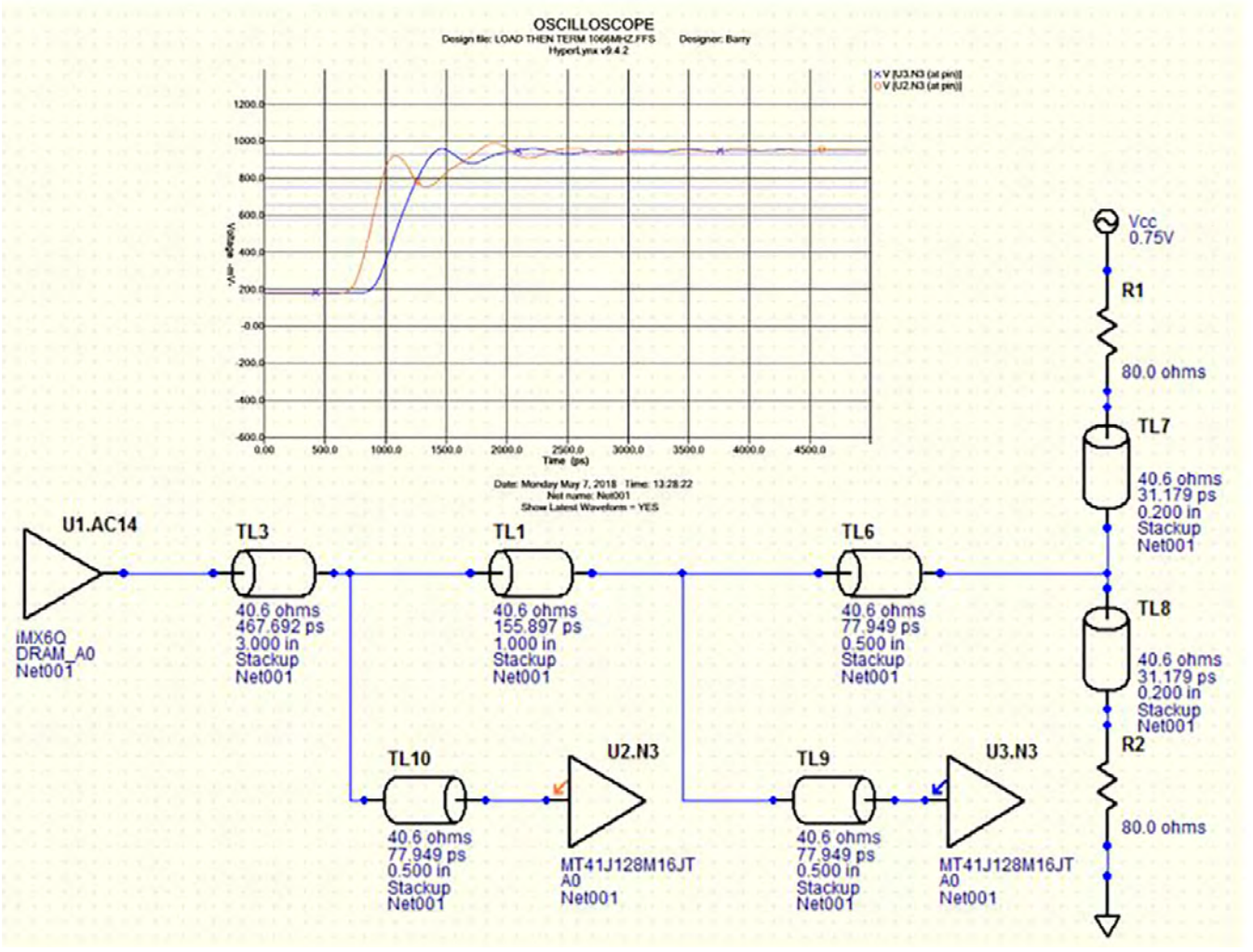


Figure 4: DDR3 fly-by topology with end termination and 500 mil stub.

tions, does not need to be matched to the delay/length of the other signals in the ACC group. Also, further simulations confirmed that the length can be rather long (up to 3 inches) without any noticeable degradation of signal quality. Stubs to each receiver input, from the passing signal, should be kept below 200mil in length to maintain a clear eye.

Key Points:

- Fly-by topology supports higher-frequency operation and improves signal integrity and timing on heavily loaded signals.
- The sequencing of the stubs and the end termination and the associate load can make a measurable difference in signal quality.
- Reflections occur whenever the impedance of the transmission line changes along its length.
- If the propagation time and reflection from source to load are longer than the edge transition time, an electrically long trace will exist.
- If the trace is short, termination may still be required if the load is capacitive to prevent ringing.
- Series termination is an excellent strategy for point to point routes, one load per net.
- Parallel (end termination) is preferred for busses with a number of loads in a multi-drop topology.
- Address, control and command (ACC) signals, traces should be routed directly to

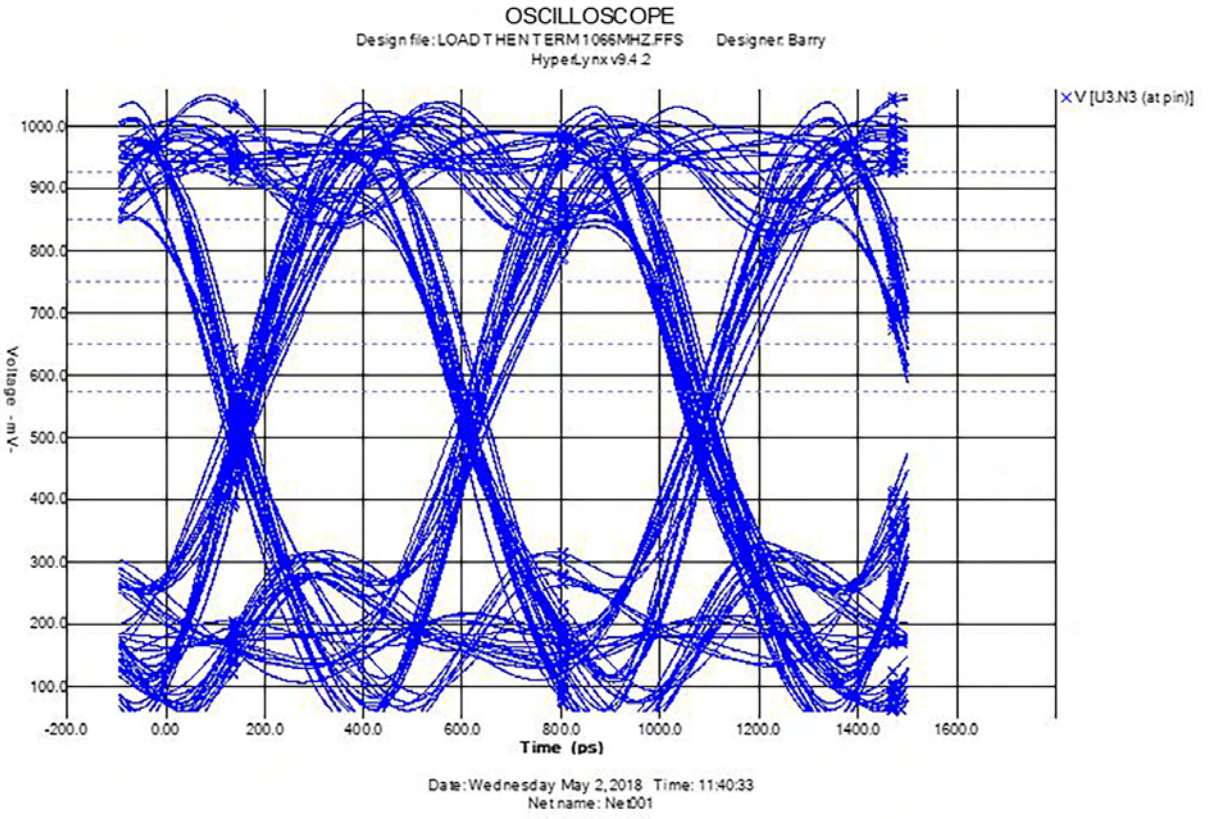


Figure 5: DDR3 fly-by topology with 500 mil stubs to receiver inputs.

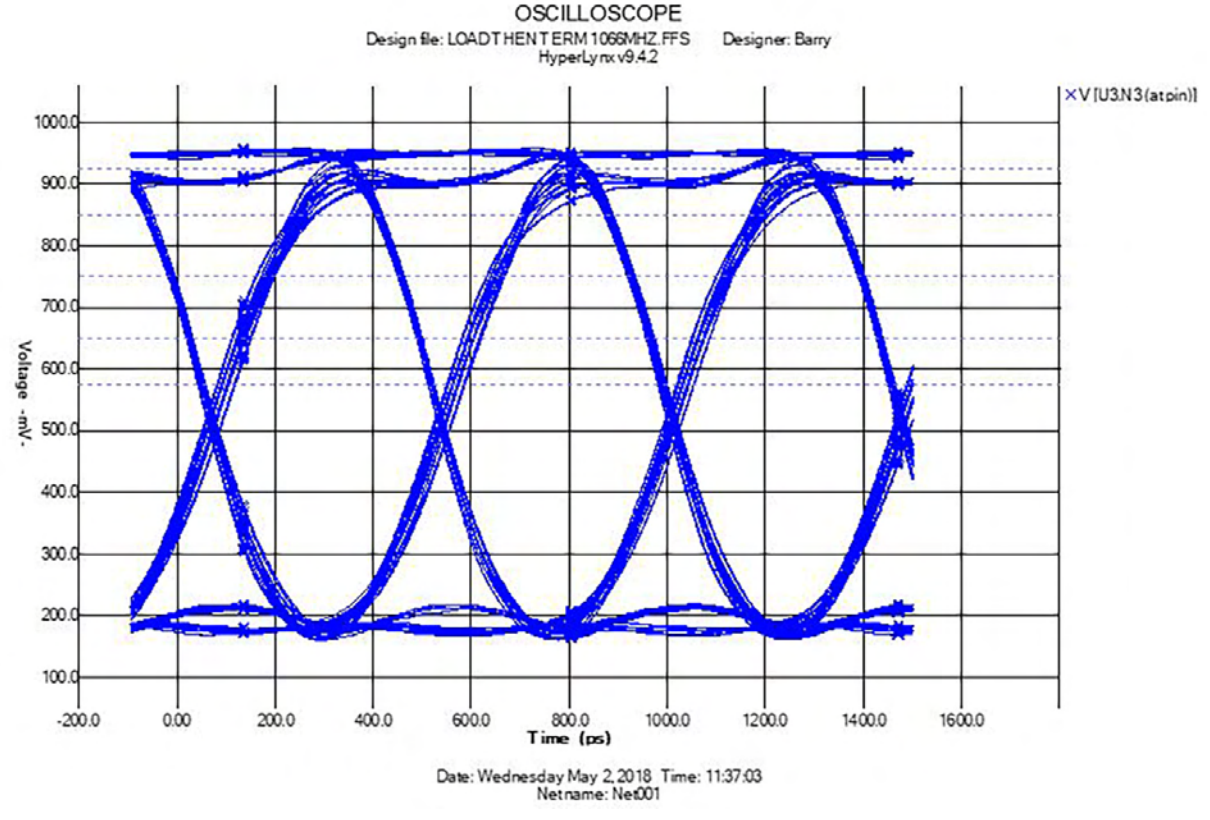


Figure 6: DDR3 fly-by topology with 200 mil stubs to receiver inputs.

the memory device pins and the parallel termination placed at the end of the transmission line.

- Stub capacitance, along with the parasitic input capacitance of the receiver pin, creates an imperfection in the termination network.
- There are no reflections when the passing address signal trace goes directly to the receiver pins with no stub and the termination is at the very end of the line.
- Stubs create reflections and have a detrimental impact on the address signal in the fly-by topology.
- Simulations suggest that the stub must be a maximum of 200mil to alleviate the impact of the reflections.

References:

1. Barry Olney's Beyond Design: DDR3/4 Fly-by vs T-topology Routing, Impedance Matching: Terminations.
2. High-Speed Signal Propagation, by Howard Johnson.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN and CPW Planner. The software can be downloaded from www.icd.com.au. To contact Olney, or read past columns, click here.

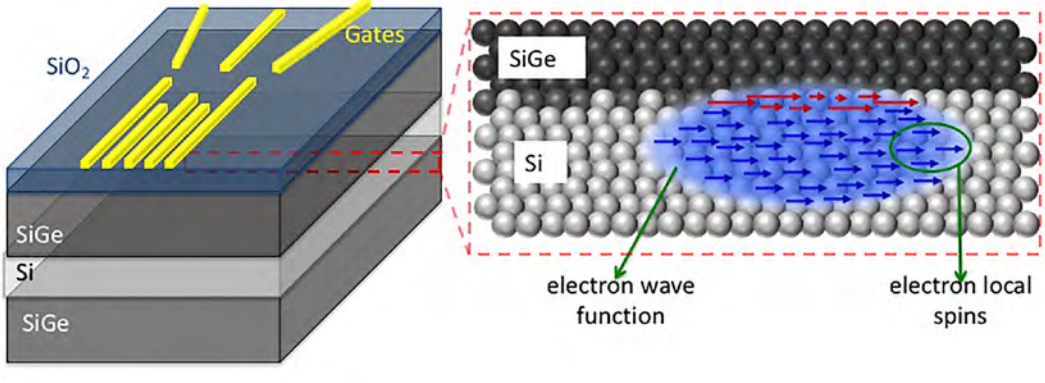
Silicon Provides Means to Control Quantum Bits for Faster Algorithms

Research groups from Purdue University, the Technological University of Delft, Netherlands and the University of Wisconsin-Madison have discovered that silicon has unique spin-orbit interactions that can enable the manipulation of qubits using electric fields, without the need for any artificial agents.

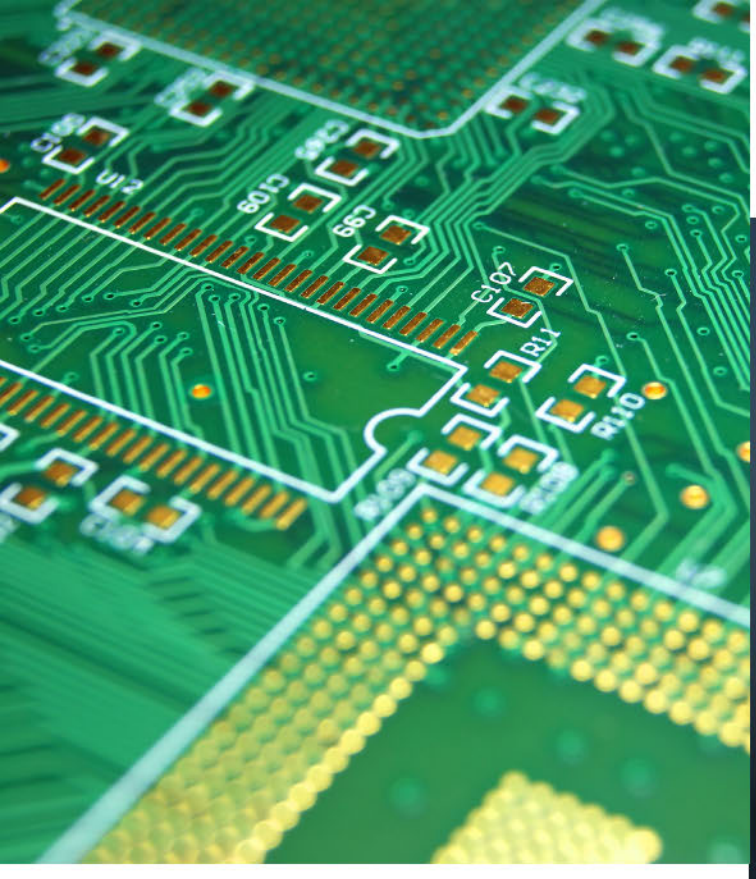
"Qubits encoded in the spins of electrons are especially long-lived in silicon, but they are difficult to control by electric fields. Spin-orbit interaction is an important knob for the design of qubits that was thought to be small in this material, traditionally," said Rajib Rahman, research assistant professor in Purdue's School of Electrical and Computer Engineering.

The strength of spin-orbit interaction, which is the interaction of an electron's spin with its motion, is an important factor for the quality of a qubit. The researchers found more prominent spin-orbit interaction than usual at the surface of silicon where qubits are located in the form of so-called quantum dots–electrons confined in three dimensions. Rahman's lab identified that this spin-orbit interaction is anisotropic in nature, meaning that it is dependent on the angle of an external magnetic field, and strongly affected by atomic details of the surface.

The researchers published their findings on June 5 in Nature Partner Journals - Quantum Information. The Wisconsin-Madison team fabricated the silicon device, the Delft team performed the experiments and the Purdue team led the theoretical investigation of the experimental observations.



Upcoming work in Rahman's lab will focus on taking advantage of the anisotropic nature of spin-orbit interactions to further enhance the coherence and control of qubits, and, therefore, the scaling up of quantum computer chips.



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Considerations for Comparing Material Data Sheets

Lightning Speed Laminates

by John Coonrod, ROGERS CORPORATION

RF and high-speed digital designers often compare data sheets from different circuit material manufacturers while seeking to find the proper material for their applications. Of course, a careful study comparing the different data sheets is highly recommended. However, when the details of circuit material data sheets are considered, several exceptions could cause confusion among those unfamiliar with this process. Understanding the test methods and their testing conditions for each property is critical in recognizing whether a direct data comparison of two different materials is valid.

To begin with, one common high-frequency circuit material property to consider in most applications is Dk (dielectric constant or relative permittivity). Many PCB designers see Dk as a straightforward property, but when you evaluate the different test methods, conditions and influence the material has on each test method, the results may not be as one would assume.

As an example, the same piece of material can be tested in two different tests and achieve two different Dk values, and both values may be correct. One reason why that statement can be true is since most materials used in the PCB industry are anisotropic, which means that the Dk is not the same on different axes. Some test methods will evaluate the material in the z-axis (thickness axis) only and other test methods will evaluate the x-y plane of the material for the Dk property. When a material is anisotropic, there should be a different Dk in the z-axis than in the x-y plane.

Another example is related to the normal frequency-dependence of the Dk in high frequency materials. As a general statement, an

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increase in frequency will cause the Dk to decrease slightly when tested within the microwave range of frequencies or within the lower millimeter-wave range of frequencies. Again, it is possible to test the same material in two different tests, which are using the same test method and get two different answers for Dk and both answers are correct. That can be true due to the frequency-dependence of materials and when using the same test method but at different frequencies, the Dk value should be different.

There are also similar accuracy concerns for comparing data sheets as it relates to dissipation factor (Df). The main concern regarding Df is typically the test methods being compared at different frequencies. Df is frequency-dependent and with an increase in frequency, the Df should increase. Sometimes data sheets will show the Df values at 2 GHz or 2.5 GHz when targeting applications in that frequency range and then other data sheets will report Df for the material when tested at 10 GHz. The Df should be higher at 10 GHz than 2 GHz, so the designer needs to make sure the frequency and test method is the same when comparing Df values for different materials.

The main concern regarding Df is typically the test methods being compared at different frequencies.

Additionally, there are other scenarios to consider for different properties and one example would be the thermal conductivity of a material. There are different test methods for determining the thermal conductivity of the material and when using the same test method, there are different sample preparations which can alter the results of this property. One noteworthy difference for testing thermal conductivity and using the same test method is whether the material is copper clad or if the copper was removed prior to testing. Most materials used in the PCB industry have relatively low thermal conductivity and copper has extremely good thermal conductivity. A common range of thermal conductivity for high-frequency materials is from 0.2 W/m·K to 0.5 W/m·K and copper has about 400 W/ m·K for thermal conductivity. When a material is tested for thermal conductivity and if copper remains on the sample being evaluated, the thermal conductivity test method will report a much higher value than if the sample has the copper removed prior to testing. Since most thermal modeling software requires thermal conductivity values of the raw substrate, it is more appropriate for the test procedure to exclude the influence of the copper during this test.

Another consideration for data sheet comparisons is peel strength and several items can be an issue for fair assessments. One issue that can be a significant concern is the use of one copper type to generate lower insertion loss and a different copper type used to report the peel strength value of the material. It is well known that a copper type which has a smooth surface (at the copper-substrate interface) will have lower insertion loss due to lower conductor loss. However, the smoother copper will typically cause the peel strength to be lower.

Some material suppliers will often use smoother copper to demonstrate better insertion loss performance, while their data sheet will have peel strength values generated from using a copper with a rougher surface. This is usually noted on the data sheet as a footnote next to the peel strength value, which cautions the reader that the peel strength testing was done with a different copper than the copper used for other test methods on the data sheet. **DESIGN007**

John Coonrod is technical marketing manager at Rogers Corporation.

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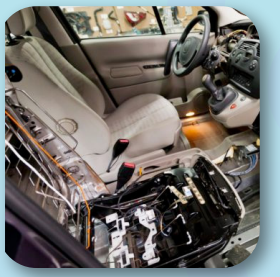

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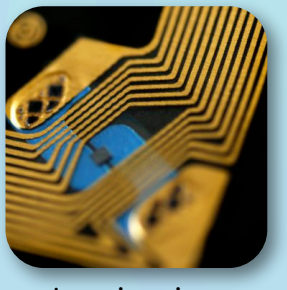

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Thermal Management Materials: Easing the Decision-Making Process

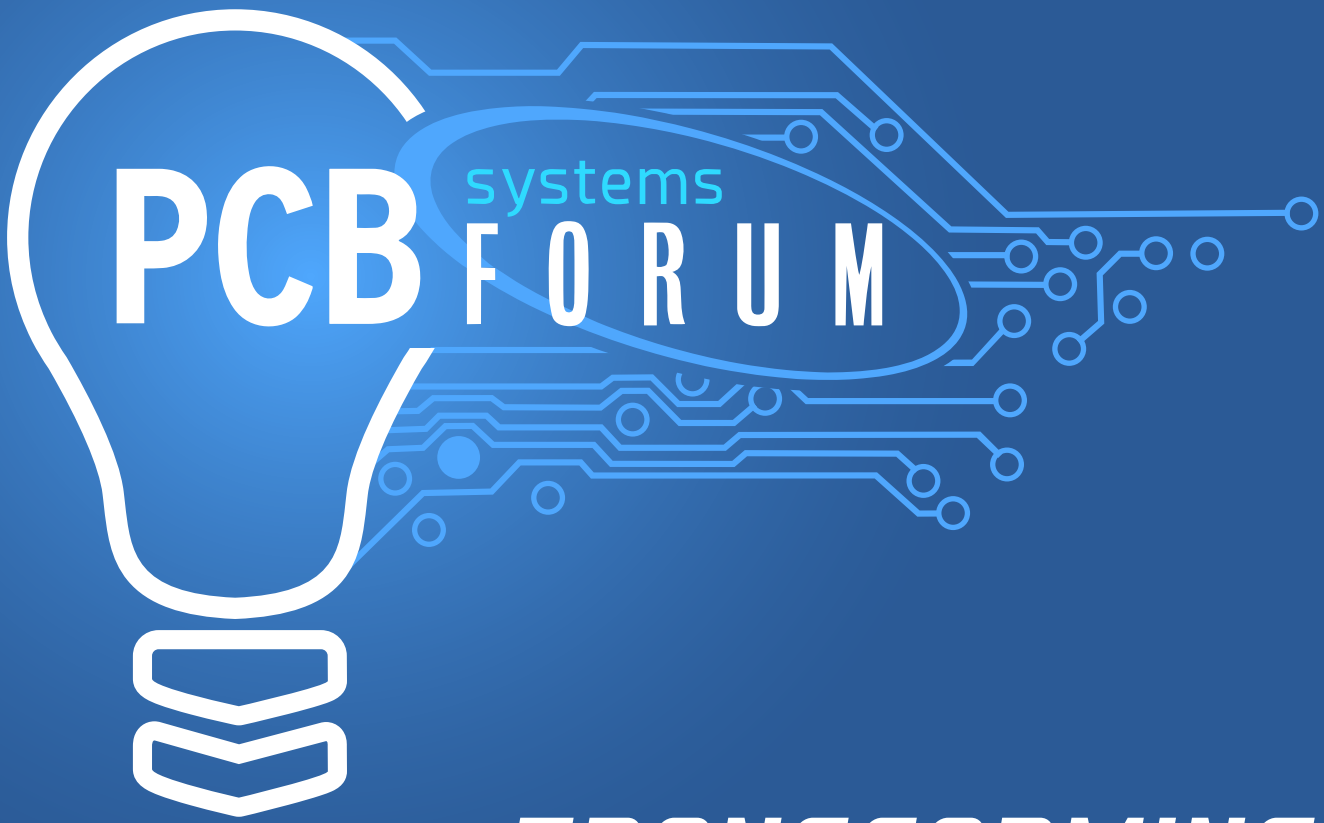
Sensible Design
by Jade Bridges, ELECTROLUBE

Last year I introduced the subject of thermal management materials—why they are necessary, what materials and methods are available to us, how best to apply them and so on—basing each column on our customers' frequently asked questions. My colleague, Alistair Little, has discussed resins in greater detail in each of his columns; now, I've been invited back to pick up from my last series, this time concentrating more closely on the practicalities of thermal management with this five-point guide to material choice and application.

01 Understanding the Dimensions: Interface or Gap Filler?

Knowledge of the dimensions of your application is critical to the selection of appropriate thermal management materials. A thermal interface is the space between a component and its heat sink, and the thermally conductive media used in this space are referred to as thermal interface materials (TIMs). This space is usually very small (i.e., on the micron scale). A gap filling application, on the other hand, is more to do with the distance between a component and the metal housing that encloses an electronics assembly and is typically measured in millimetres. In this case, a thermally conductive material is used to help minimise the chances of hot spots within the unit itself while the casing is used as the heat sink.

The difference between a few microns and a few millimetres could be critical to the performance of the thermal medium chosen. For example, if you place a TIM in a gap filling application, it is likely to be unstable in the thicker layer: with vibration, or following a period of temperature cycling, it could easily be displaced. Likewise, if a gap filling material is used in a thermal interface application, it will be very difficult to achieve a thin,



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even film, creating a higher thermal resistance at the interface and consequently reduced heat transfer efficiency.

02 Bonding or Non-Bonding: Paste or Pad?

There are many different types of thermally conductive materials and choosing between them will be dictated by production requirements and application design, as well as critical performance factors that must be achieved. For example, choosing between a bonding or non-bonding material may depend on whether the heat sink needs to be held in place by the interface material, in which case a bonding compound is the better choice. Alternatively, a compound that is fixed (does not move) may be required, in which case it may be appropriate to choose a thermal pad, which has the additional benefit of being pre-cut to size for ease of application. However, both options may result in a thicker interface layer and therefore a higher thermal resistance. The trade-off then comes from the performance requirements of the chosen compounds and understanding the conditions of the application.

03 Maximising Heat Transfer Efficiency Across a Wide Temperature Range

Thermal changes are common within heat dissipation applications because most devices are switched on and off or have varying power requirements in use. In addition, environmental temperature changes can lead to extremes within the device—automotive applications are a good example, as these must also operate after being powered down in conditions well above and below what we would consider a standard ambient temperature.

It is therefore critical that the chosen thermal dissipation media operates within the temperature limits defined for the device, while maintaining performance during changeable conditions. A typical problem is pump-out, whereby the stresses exerted by the minute changes in dimensions of the interface substrates can cause a non-curing interface material to move over time. The ability of a TIM to resist these stresses will improve the performance of the device over its lifetime and will be dependent upon the interfacial spacing, as well as the type and amount of TIM applied.

Where thermal effects are significant, it might be worth considering the use of phase change materials—non-curing, non-bonding products that change to a slightly softer material above their phase change temperature. The properties of these materials allow them to conform to the contours of the interface and provide a much lower thermal resistance than a cured product, whilst minimising the effects of pump-out, typically associated with non-curing products. However, if a phase change material is used in a device which typically operates below the phase change temperature, the material will remain in its solid form and will not provide the desired low thermal resistance.

04 Environmental Conditions: Is Protection Required?

Aside from thermal changes, there may be other environmental factors to consider. A thermal interface material or gap filler must also be resistant against other environmental conditions such as high humidity, salt mist, corrosive gases, and so on. It is important to consider at the design stage whether these external factors could impact on the performance of the thermal compound. As a TIM is usually applied in a very thin layer between two substrates, it is unlikely to be fully exposed to such conditions; however, a gap filling material could be subject to more challenging environments, in which case the better approach would be to switch from a gap filler to a full protection compound, such as a thermally conductive encapsulation resin.

05 How to Apply?

Application technique will depend upon the type of product. For both curing and non-curing products, the method of application may be screen printing or automated dispensing, the only difference being the available work-

ing time of a curing material. For example, if the product quickly becomes touch dry, it may not be suitable for stencil printing as the cured product may block the screen. In most cases, a minimum amount of material must be applied for thermal interface and gap filling applications to ensure maximum heat transfer. For a thermal interface, the layer must achieve uniform coverage over the entire interface; and when using a gap filler, the material must be applied while ensuring that all air is expelled, as air is a poor conductor of heat and may cause additional hotspots.

If an encapsulation resin is deemed to be the best choice, it is likely that the entire PCB will need to be covered. The amount of resin applied will have to strike a balance between achieving the desired protection level and minimising any weight and volume gains contributed by the resin.

Hopefully, the foregoing has provided a useful introduction to thermal management materials. Look out for my next contribution, where I will continue exploring thermal management. **DESIGN007**

Jade Bridges is global technical support manager for Electrolube Ltd.

Designing a Better Superconductor with Geometric Frustration

Superconductors contain tiny tornadoes of supercurrent, called vortex filaments, that create resistance when they move. This affects the way superconductors carry a current.

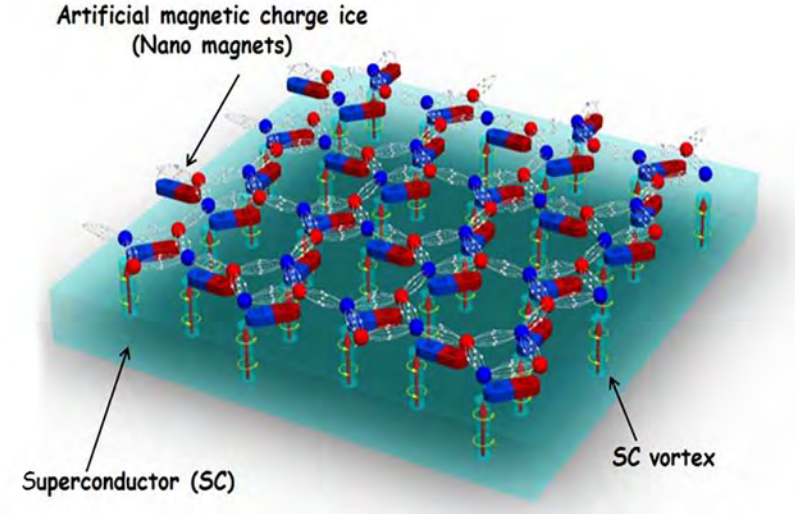
But a magnet-controlled "switch" in superconductor configuration provides unprecedented flexibility in managing the location of vortex filaments, altering the properties of the superconductor, according to a new paper in Nature Nanotechnology.

"We work on superconductors and how to make them better for applications," said Boldizsár Jankó, professor in the Department of Physics at the University of Notre Dame and co-corresponding author on the paper. "One of the major problems in superconductor technology is that most of them have these filaments, these tiny tornadoes of supercurrent. When these move, then you have resistance."

The collaborators' solution overlays the superconductor with an artificial spin ice consisting of an array of interacting nanoscale bar magnets. Rearranging the magnetic orientations of those nano-bar magnets results in a real-time rearrangement of the pinning on the superconducting site. This makes possible multiple, reversible spin cycle configurations for the vortices. Spin is a particle's natural, angular momentum.

"The main discovery here is our ability to reconfigure these spinning sites reversibly and instead of having just one spin cycle configuration for the vortices, we now have many, and we can switch them back and forth," Jankó said.

Because the control of the quantum fluxes is difficult to visualize in an experiment, simulations were required to successfully reproduce the results, said Xiaoyu Ma, a doctoral student in the Department of Physics who conducted the computer simulation in the study and is the co-first author on the paper. The simulations allowed researchers to see the detailed processes involved. "The number of vortex configurations that we can realize is huge, and we can design and locally reconfigure them site by site," Ma said. "This has never been realized before."



MilAero Highlights

It's Only Common Sense: Finally, State Dept Shows its Teeth on ITAR ▶

A good friend of mine sent me this article he received in an email from the law firm of Williams Mullins. Read it and weep, ITAR offenders! Law-abiding companies, rejoice.

Testing Todd: AVI–Your Tireless Friend in Final Inspection ▶

The "automation vs. human" debate continues. There are experts with many years of experience performing final inspection with precise detail. This is not debated. However, circumstances change with unpredictable results.

Triangle Labs: Covering the Niche Market of Large Boards ▶

I recently had the opportunity to speak with John-Michael Gray, president of Triangle Labs. We had quite a discussion on their rather unique capability of building large-format PCBs and multilayers—perhaps the largest PCBs in the world.

Tariffs on China Could Harm U.S. Electronics Companies ▶

IPC—Association Connecting Electronics Industries today warned that the Trump administrtion's plan to impose higher tariffs on goods imported from China could harm many small- and medium-sized U.S. electronics manufacturers that rely on Chinese materials, components and equipment to produce their products.

Combining Strengths Synergistically: PDS and Green Circuits ▶

Power Design Services (PDS) and Green Circuits have just announced their merger. I-Connect007 Publisher Barry Matties recently sat down with Joe O'Neil and Matthew Becker of PDS, along with Ted Park of Green Circuits, to get the full scoop.

ACT Completes Acquisition of ECT ▶

Additive Circuits Technologies LLC (ACT) is pleased to announce the conclusion of a corporate reorganization and the incorporation of assets acquired from EarthOne Circuit Technologies (ECT) and technology advancements for Autonomous Vehicles.

Solar UAV to be Developed with the Potential to Stay Airborne for a Year ▶

A new solar electric unmanned aerial vehicle (UAV), which has the potential to fly for up to a year before needing maintenance, has become a step closer to reality following a new agreement between two cutting-edge British companies, BAE Systems and Prismatic.

Lasers in Space: Earth Mission Tests New Technology ▶

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Achieving Optimum Signal Integrity

During Layer Transition on High-Speed PCBs

Article by Chang Fei Yee
KEYSIGHT TECHNOLOGIES

This article discusses the impact of stitching vias and discontinued return path or reference on signal integrity during layer transition on high-speed PCBs, particularly in terms of signal reflection and crosstalk.

Introduction

In electronic systems, signal transmission exists in a closed-loop form. The forward current propagates from transmitter to receiver through the signal trace. Meanwhile, the return current travels backward from receiver to transmitter through the power or ground plane directly underneath the signal trace that serves as the reference or return path. The path of forward current and return current forms a loop inductance.

It is important to route the high-speed signal on a continuous reference plane so that the return current can propagate on the desired path beneath the signal trace. In addition to that, whenever there is signal transition from one layer to another through a via, an extra via that connects the reference planes on different PCB layers (i.e., stitching via) must be placed near the signal via to provide a continuous return path.

If the return path is broken due to the absence of stitching via or switching of reference plane from ground to power or vice versa after layer transition on PCB, the "return current" might detour and propagate on a longer path, which causes the rise of loop inductance. This might also lead to the sharing of common return path by different signals that poses high risk of interference among the signals due to higher mutual inductance. This interference results in crosstalk that occurs on the transmitted signal [1] [2]. This phenomenon is proven in the following section with 3DEM simulation.

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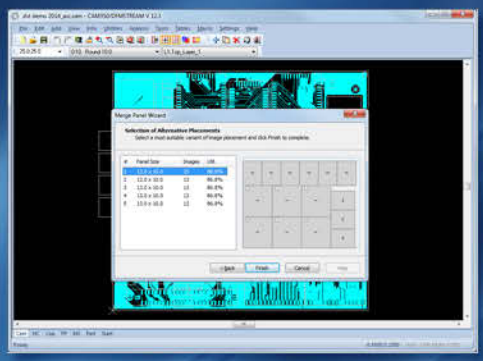

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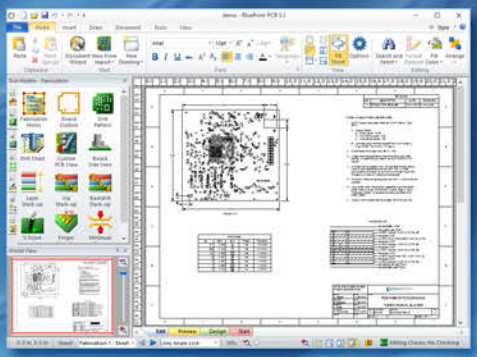

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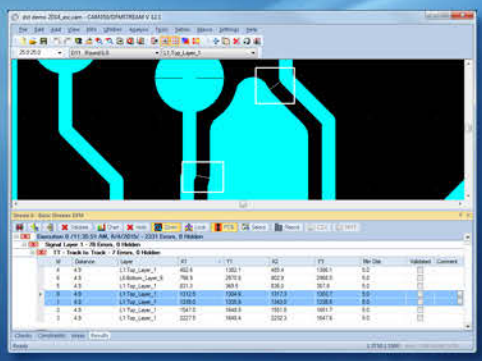

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Analysis of Signal Reflection and Crosstalk with 3DEM Modeling

To investigate the impact of stitching via and discontinued return path on high speed signal fidelity, three test models of 3DEM are constructed using Keysight EMPro. In test case 1 (the 3DEM structure in Figure 1), two signal traces with 50 ohm characteristic impedance in single ended mode on top PCB layer are transitioned to bottom layer using vias. Each segment of the signal traces on both top and bottom layers is 100 mil long and 5 mil wide. Meanwhile, the diameter of the via barrel and pad is 5 mil and 7 mil respectively.

The PCB stackup shown in Figure 2 is applied in this 3D model, where solid planes exist on layer 2 and 3. All the four copper layers have 1.2 mil thickness. FR-4 material is used as the PCB substrate. The two signal traces are separated 15 mil apart (i.e., triple the signal trace width for minimum crosstalk). A stitching via is placed 20 mil off each signal via to connect electrically the two reference planes on layer 2 and 3.

From a crosstalk perspective, port 1 and port 2 terminations are assumed to be the transmitting and receiving ends, respectively, of the aggressor line. Meanwhile, port 3 and port 4 terminations are assumed to be the transmitting and receiving end, respectively, of the victim line.

	Thickness (mil)
Solder mask top	0.5
Signal L1	1.2
Substrate	3.5
Plane L2	1.2
Substrate	10
Plane L3	1.2
Substrate	3.5
Signal L4	1.2
Solder mask bottom	0.5

Figure 2: PCB stackup similar to our first example.

In test case 2 (Figure 3), the 3DEM structure is left with only a single stitching via electrically connecting the two reference planes on layer 2 and 3. The rest of the portion is the same as test case 1.

On the other hand, in test case 3 (Figure 4), voids are placed on the layer 3 reference plane to break the electrical connectivity between the planes on layer 2 and 3 though stitching vias. This is to simulate the effect of the discontinued return path on signal reflection and cross-

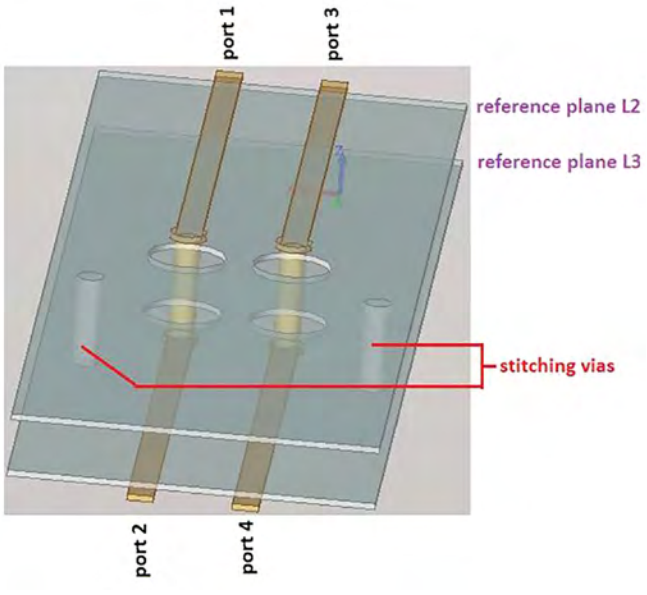

Figure 1: 3DEM structure in test case 1.

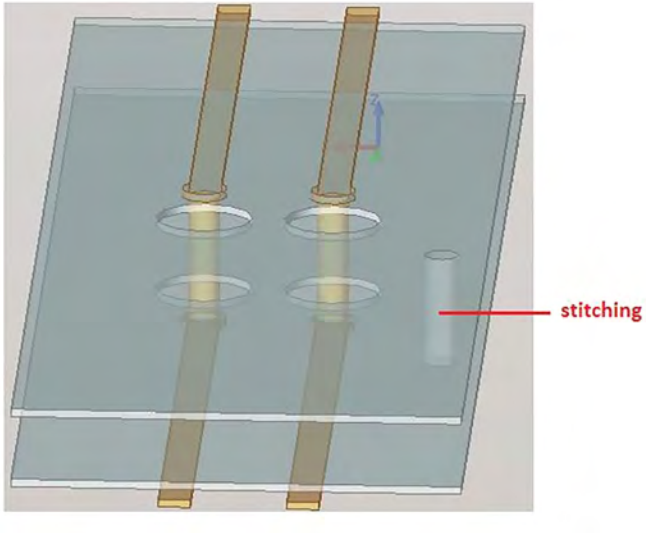

Figure 3: 3DEM structure in test case 2.

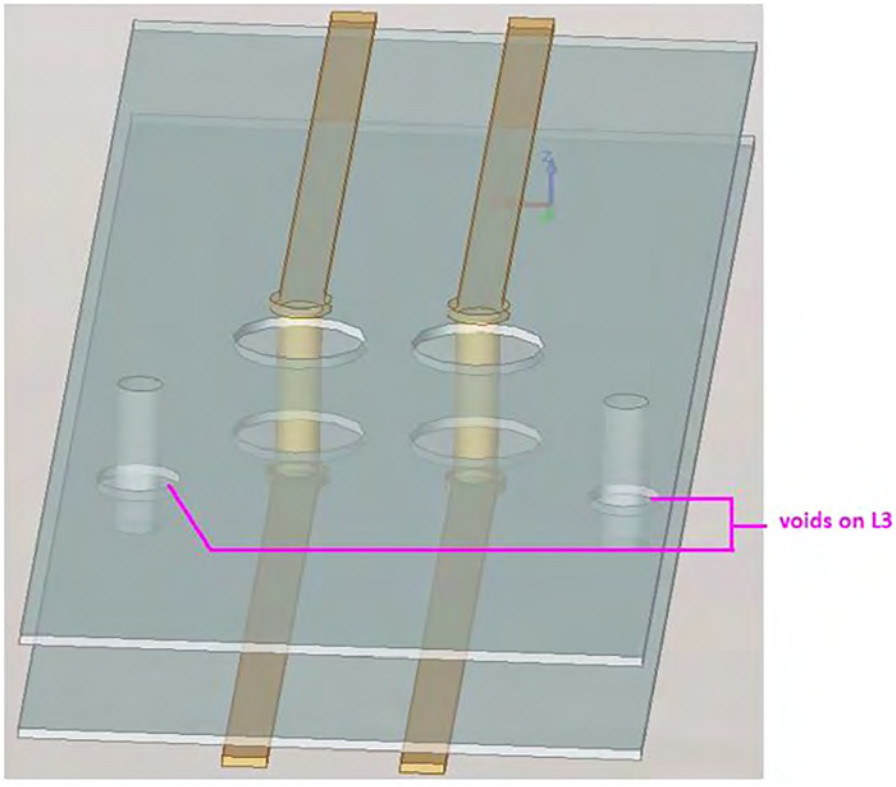

Figure 4: 3DEM structure in test case 3.

talk by switching the reference from ground to power or vice versa after the signal layer transition through via.

S-parameters of the 3DEM models in these test cases are plotted in Figure 5, from 1MHz to 20GHz as shown. The S11 parameter is meant for signal reflection while S41 is meant for far-end crosstalk (FEXT). A more severe signal reflection and crosstalk are indicated by the smaller absolute value in dB. With reference to Figure 5, in most of the frequency range, the most severe signal reflection and FEXT are experienced in test case 3, followed by case 2 and the least severe in case 1.

Subsequently, transient simulation is performed for these three test cases to observe the phenomenon of FEXT in time domain. In this transient simulation, a square wave signal with 2.6Gbps data rate, 800mVpp amplitude and 7V/ns slew rate is injected into port 1 of each test case's 3DEM model, with port 3 being pulled low (serving as the near end point of victim line), followed by probing at port 4 (i.e., serves as far end point of victim line). Referring to Figure 6, noise induced at the far end point of victim line in time domain for test case 1, 2 and 3 is 68mVpp, 75mVpp and 127mVpp respectively.

Test case 1 experienced the least severe crosstalk and signal reflection, because each signal via has its own stitching via and all segments of the signal traces are referenced to the same net, prefereably ground. This structure provides a perfect return path for high-speed signals. In test case 2, there is only a single

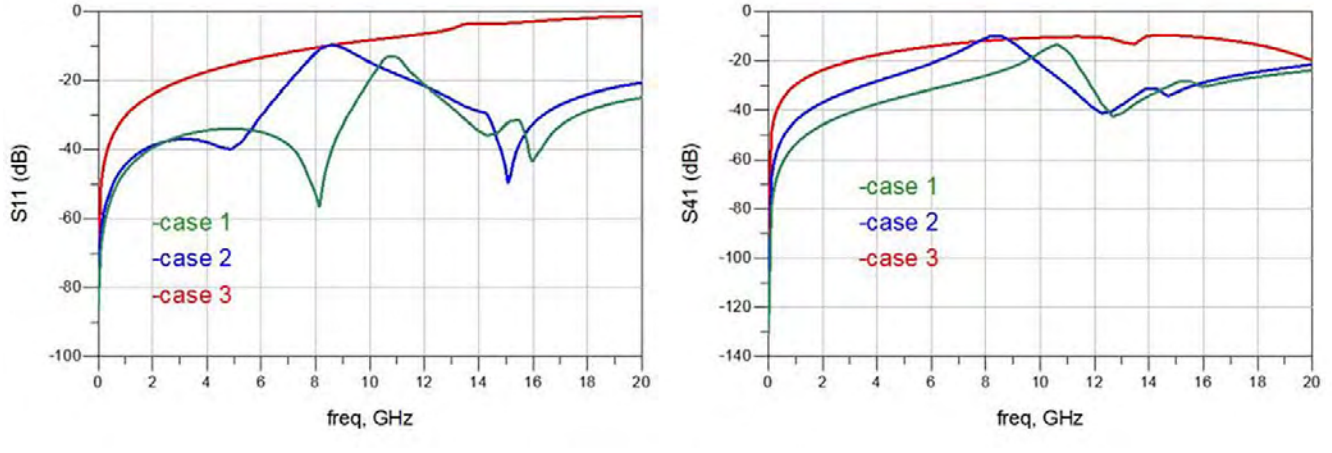

Figure 5: Simulated plots of S11 (left) and S41 (right).

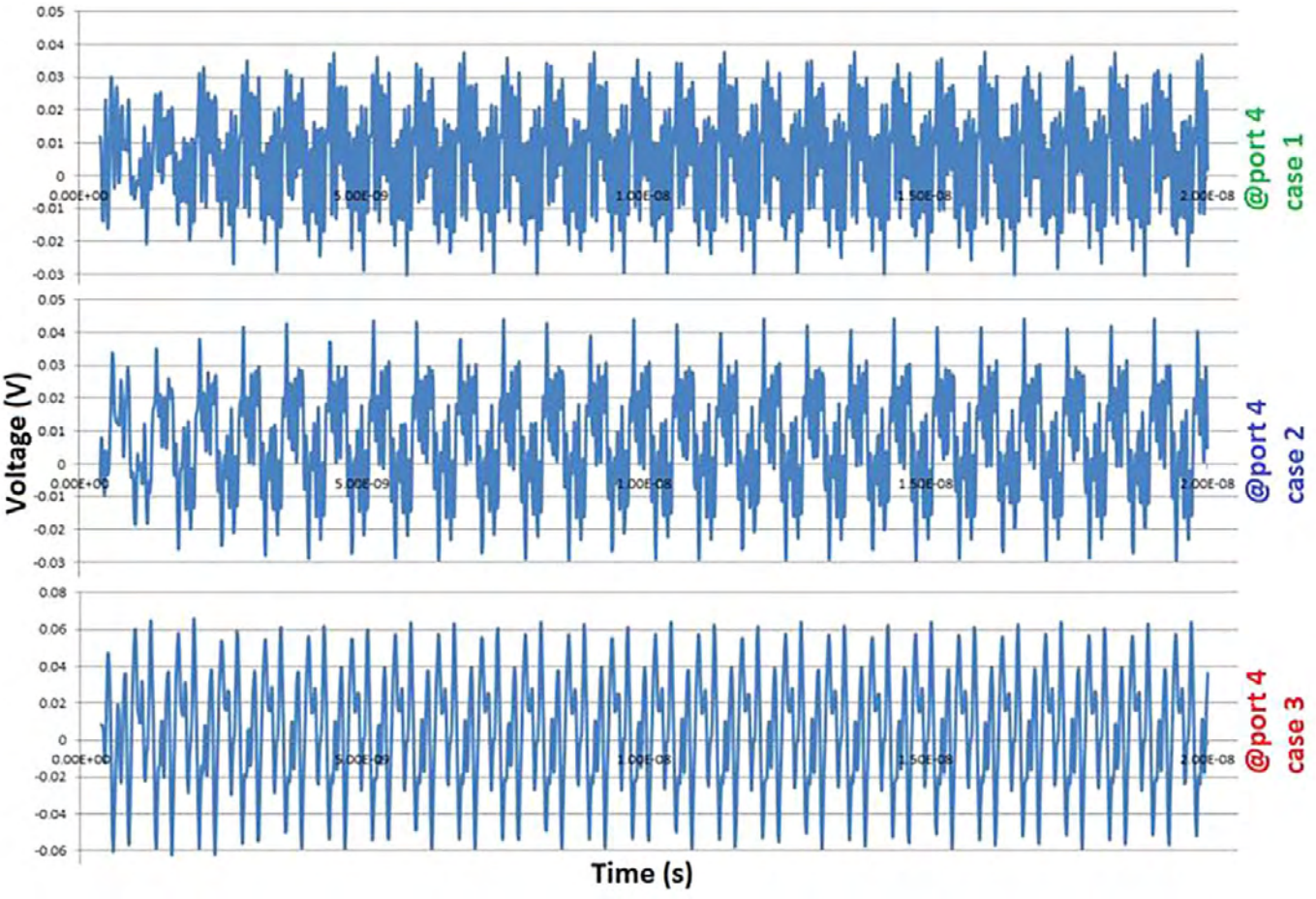

Figure 6: Noise induced at far end point for 3 test cases due to crosstalk.

stitching via connecting the reference planes. This sole stitching via becomes the return path bottleneck of the two signal traces and results in more critical crosstalk for the return current versus test case 1.

On the other hand, in test case 3, the signal trace on the top layer is referenced to ground, but the signal trace on the bottom layer is referenced to power, or vice versa, contributing to the broken or non-continuous return path after signal layer transition, thus intensifying the signal reflection and crosstalk.

Conclusion

It is crucial to provide a continuous return path for high-speed signaling during layer transition on PCB to minimize signal reflection and crosstalk. This is achievable by assigning each signal segment's reference plane to the same net (i.e., preferably ground). Additionally, stitching vias shall be placed near signal vias to electrically connect the reference planes on different PCB layers. **DESIGN007**

References

1. Tan, S., Yew, Y. and Shi, H. (2008), Crosstalk and Switching Noise Mechanism Study in High-Density Wire-bond FPGA Devices, 10th Electronics Packaging Technology Conference, Singapore, pp. 78-83

2. Barry Olney's Beyond Design column (April 2017), Return Path Discontinuities

Chang Fei Yee is a hardware engineer with Keysight Technologies. His responsibilities include embedded system hardware development, and signal and power integrity analysis.

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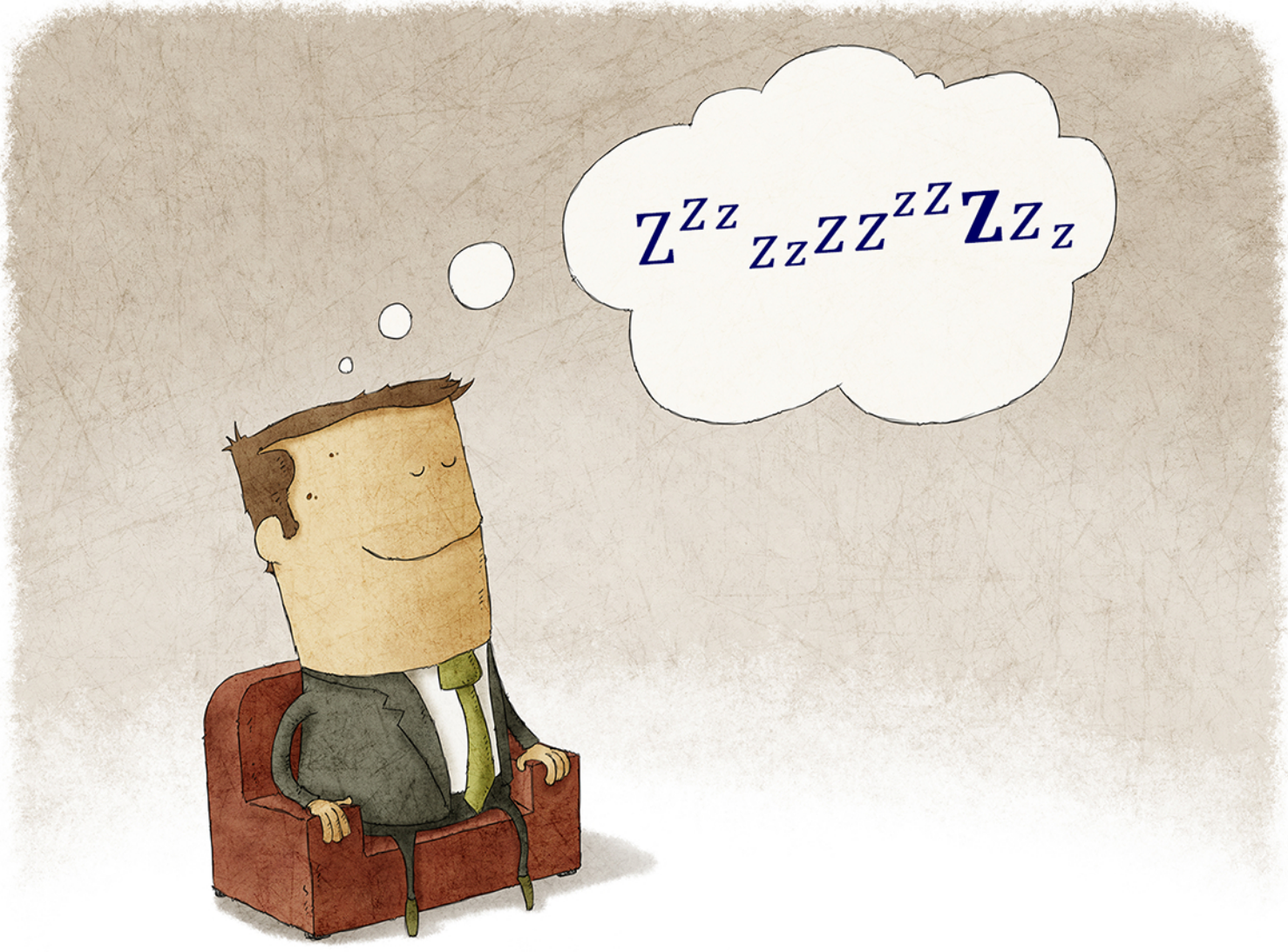

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Recent Highlights from Design007

1 Mark Thompson: What Designers Need to Know about Fab ▶

Mark Thompson wants to help PCB designers. He's seen it all in CAM support at Prototron Circuits: the incomplete or inaccurate data packages, boards that are unnecessarily complex or over-constrained, and so much more. Dan Beaulieu asked Mark to explain why it's so important for designers to communicate with their fabricators, and why they need to get out of the office and visit a board shop every now and then.

2 PCB Design Software Market to Reach $4B by 2023 ▶

The PCB design software market is expected to grow at a CAGR of around 26% from 2018 to 2023 to reach $4 billion by the end of the forecast period, according to a new report by analyst firm Market Research Future (MRFR). The European PCB design software market is estimated to grow due to the investments from automotive companies to adopt the software.

3 Beyond Design: A Review of HyperLynx DRC ▶

Free software usually comes at a price: the results might be inaccurate, the software might be time-consuming to set up and use, and the tool might overlook issues that require a revision to mitigate. But HyperLynx DRC is the exception to the rule.

4 Freedom CAD Celebrates 15th Anniversary ▶

May 16, 2018 marks the 15th anniversary of Freedom CAD Services. Freedom CAD was founded on this day by Lou and Lauren Primmer, pioneers in the PCB CAD industry. They launched Freedom CAD when Plexus decided to divest the Nashua, NH design center in 2003.

5 Field Trip: CID Class Sees How Flex is Made at Streamline Circuits ▶

While I was teaching my CID class for EPTAC in Santa Clara, I learned that we were only a block away from Streamline Circuits. Streamline does a lot of military and aerospace work, as well as communications and industrial electronics. The company manufactures quite a bit of multilayer flex and rigid-flex circuits, in addition to rigid boards. This would make a great field trip for my CID class!

6 Ucamco Updates Gerber File Specification ▶

Ucamco has released version 2018.05 of the Gerber Format Specification. The document is available on the Gerber download page on Ucamco's website.

7 Experts Discussion: What Does 5G Mean to Materials and EDA Tools? ▶

Whether we're ready for it or not, 5G technology is coming. For this issue, we decided to speak with John Hendricks, market segment manager for wireless infrastructure at Rogers Corporation, and Ben Jordan, director of product and persona marketing for Altium, about the challenges related to 5G and what this means for PCB designers and fabricators.

8 Design and Manufacturing Perspectives from DISH Technology's Les Beller ▶

I recently interviewed Les Beller, a long-time PCB designer who is now a manufacturing engineer for DISH Technology. We discussed his company's business shift towards 5G and streaming, and the stresses that puts on a design team. He also explains the greatest challenges that he's facing with HDI and higher frequencies, and the added importance for designers to understand the manufacturing process and DFM tools.

9 Global EDA Market Projected to Reach CAGR of 12.2% by 2018-2023 ▶

The EDA tools market is projected to register a CAGR of 12.2% during the forecast period 2018-2023. The demand for compact electronic devices has been increasing across several sectors, such as automotive and industrial manufacturing, and has compelled the IC manufacturers to increase investment in R&D, to reduce the size while improving the performance of ICs.

10 EDADOC: A Driving Force in China's Automotive Electronics Design ▶

EDADOC is one of the biggest providers of PCB design and manufacturing services in China, with a long history in automotive electronics design and manufacturing. I recently conducted an email interview with EDADOC R&D Technical Research Manager William Zhou and Brand Planning Specialist Wen Ling about the challenges related to designing and fabricating automotive PCBs.

Career Opportunities

Pssst! Are You Looking for Someone?

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For just $500, your 200 word, full-column—or, for $250, your 100 word, half-column—ad will appear in the Help Wanted section of all three of our monthly magazines, reaching circuit board designers, fabricators, assemblers, OEMs and suppliers.

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Barb Hockaday at barb@iconnect007.com or +1.916.608.0660 (-7 GMT)

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TAIYO KOGYO CO., LTD.

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Taiyo Kogyo is a Japanese PCB manufacturer founded in 1962. Our unique and differentiated boards are used in various industry segments, and our products are appreciated for application in power electronics. High-current and thermal solution PCBs are our strength.

Position Summary:

Responsible for creating new business and expanding business with existing customers in the U.S. Work at home, part-time (half-day/5 days a week) is okay. (Option: After six months, position can be upgraded to full-time, based on performance.)

Responsibilities:

- Develop new customers: Work closely with local sales representatives and independently in territories without sales reps
- Educate and support local sales representatives
- Operate as company's U.S. Sales office and communicate daily with Japanese headquarters for smooth and speedy communications with local sales reps and customers
- Travel and visit prospective customers with local sales reps or alone to develop new customers (about 6 to 10 times a year)
- Attend company booth at business expo (APEX) during the show
- Search for and appoint competent local sales reps in non-covered regions

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Zentech Manufacturing is Hiring!

Looking to excel in your career and grow professionally in a thriving business? Zentech, established in Baltimore, Maryland, in 1998, has proven to be one of the premier electronics contract manufacturers in the U.S.

Zentech is rapidly growing and seeking to add a circuit layout team leader with hands-on Mentor Expedition experience. We offer an excellent benefit package including health/dental insurance and an employer matched 401k program, and we hold the ultimate set of certifications relating to the manufacture of mission-critical printed circuit card assemblies, including: ISO:9001, AS9100, DD2345, and ISO 13485. Zentech is an IPC Trusted Source QML and ITAR registered.

U.S. citizens only need apply.
Please email resume to
sales@zentech.com.

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Career Opportunities

Manncorp™

SMT Field Technician
Huntingdon Valley, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to install and support our wide array of SMT equipment.

Duties and Responsibilities:
- Manage on-site installation of equipment and training of customers
- Troubleshoot and diagnose technical problems by phone, email or additional on-site visits, when necessary during post-installation service and support
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Produce service reports
- Cooperate with technical team and share information across the organization
- Assist with the crating and uncrating of equipment

Requirements and Qualifications:
- Three to five years of experience with SMT equipment, or equivalent technical degree
- Strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Organizational skills, detail orientated and capable of multitasking
- Good written and oral interpersonal skills with an ability to work under minimum supervision
- Ability to work with little supervision while traveling
- Availability for frequent travel
- Ability to arrange and schedule service trips
- USA Citizenship required

We Offer:
- Health & dental insurance
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Technology Communications Writer/Content Manager
Board Systems Division

Mentor Graphics, a Siemens business, is a global technology leader in EDA software, enabling global companies to develop new and highly innovative electronic products in the increasingly complex world of chip, board, and system design.

Job Duties:
The Mentor printed circuit board (PCB) technical writer/content manager will:

- Write and produce high-quality content for various properties (blogs, product collateral, technical white papers, case studies, industry publications, etc.).
- Gather research and data, interview subject matter experts, and transform complex information into clear, concise marketing communications.
- Manage projects across multiple PCB product teams (high-speed design/analysis, advanced packaging, board design) within a deadline-driven environment.

Job Qualifications:
The ideal candidate should possess:

- Strong writing and editing skills with experience in PCB design technologies.
- Desktop publishing skills (InDesign) using project templates and knowledge of online publications and social media.
- A technical background (B.S. in electrical engineering or computer science preferred; this role works closely with the PCB division's technical marketing engineers and managers.
- Solid project planning and management skills; appreciation for adhering to deadlines; creativity for turning technical information into compelling content; teamwork and strong interpersonal communications skills; ability to be a self-starter.

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Zentech is rapidly growing and seeking to add a Manufacturing Engineer. We offer an excellent benefit package including health/dental insurance and an employer-matched 401k program, and we hold the ultimate set of certifications relating to the manufacture of mission-critical printed circuit card assemblies, including: ISO:9001, AS9100, DD2345, and ISO 13485. Zentech is an IPC Trusted Source QML and ITAR registered.

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MacDermid Enthone
ELECTRONICS SOLUTIONS

Technical Service Rep, Northeast

Do you have what it takes? MacDermid Enthone Electronics Solutions is a leading supplier of specialty chemicals, providing application-specific solutions and unsurpassed technical support.

The position of the Technical Service Rep will be responsible for day-to-day support for fabricators using MacDermid Enthone's chemical products. The position requires a proactive self-starter who can work closely and independently with customers, sales group members and management to ensure that customer expectations and company interests are served.

- Thoroughly understand the overall PCB business, and specifics in wet processing areas
- Prepare action plans for identification of root cause of customer process issues
- Provide feedback to management regarding performance
- Create and conduct customer technical presentations
- Develop technical strategy for customers
- Possess the ability to calm difficult situations with customers, initiate a step by step plan, and involve other technical help quickly to find resolution

Hiring Profile

- Bachelor's Degree or 5-7 years' job-related experience
- Strong understanding of chemistry and chemical interaction within PCB manufacturing
- Excellent written and oral communication skills
- Strong track record of navigating technically through complex organizations
- Extensive experience in all aspects of customer relationship management
- Willingness to travel

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Career Opportunities

ventec
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騰輝電子

Ventec Seeking U.S. Product Manager for tec-speed

Want to work for a globally successful and growing company and help drive that success? As a U.S.-based member of the product and sales team, your focus will be on Ventec's signal integrity materials, tec-speed, one of the most comprehensive range of products in high-speed/low-loss PCB material technology for high reliability and high-speed computing and storage applications. Combining your strong technical PCB manufacturing and design knowledge with commercial acumen, you will offer North American customers (OEMs, buyers, designers, reliability engineers and the people that liaise directly with the PCB manufacturers) advice and solutions for optimum performance, quality and cost.

Skills and abilities required:

- Technical background in PCB manufacturing/ design
- Solid understanding of signal integrity solutions
- Direct sales knowledge and skills
- Excellent oral and written communication skills in English
- Experience in making compelling presentations to small and large audiences
- Proven relationship building skills with partners and virtual teams

This is a fantastic opportunity to become part of a leading brand and team, with excellent benefits.

Please forward your resume to jpattie@ventec-usa.com and mention "U.S. Sales Manager—tec-speed" in the subject line.

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PCB Manufacturing, Marketing Engineer

Use your knowledge of PCB assembly and process engineering to promote Mentor's Valor digital manufacturing solutions via industry articles, industry events, blogs, and relevant social networking sites. The Valor division is seeking a seasoned professional who has operated within the PCB manufacturing industry to be a leading voice in advocating our solutions through a variety of marketing platforms including digital, media, trade show, conferences, and forums.

The successful candidate is expected to have solid experience within the PCB assembly industry and the ability to represent the Valor solutions with authority and credibility. A solid background in PCB Process Engineering or Quality management to leverage in day-to-day activities is preferred. The candidate should be a good "storyteller" who can develop relatable content in an interesting and compelling manner, and who is comfortable in presenting in public as well as engaging in on-line forums; should have solid experience with professional social platforms such as LinkedIn.

Success will be measured quantitatively in terms of number of interactions, increase in digital engagements, measurement of sentiment, article placements, presentations delivered. Qualitatively, success will be measured by feedback from colleagues and relevant industry players.

This is an excellent opportunity for an industry professional who has a passion for marketing and public presentation.

Location flexible: Israel, UK or US

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Career Opportunities

ventec
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Technical Support Engineer, UK

As a UK-based Technical Support Engineer, you will help customers choose and optimize the use of Ventec materials in their Printed Circuit Board manufacturing processes. You will provide a two-way channel of technical communication between Ventec's production facilities and UK/European customers. You will be required to undertake some laboratory testing (including the use of TMA, DSC, Melt Viscometer, Gel Plate Timer, and laboratory scale multilayer presses) and provide appropriate technical support to Ventec UK and European sales personnel to maximize results.

Skills and abilities required for the role:

- Hold a HNC, HND, degree or equivalent in a technical/scientific discipline.
- Excellent communications skills and ability to write full technical reports for group or customer distribution.
- Ability to work in an organized, proactive, and enthusiastic way.
- Ability to work well, both in a team as well as an individual.
- Good user knowledge of common Microsoft Office programs.
- Full driving license essential.

Appropriate training will be given if required.

This is a fantastic opportunity to become part of a successful brand and leading team with excellent benefits. For more information, please click here.

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This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

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Events Calendar

PCB West ▶
September 11–13, 2018
Santa Clara, California, USA

IPC E-Textiles 2018 Workshop ▶
September 13, 2018
Des Plaines, Illinois, USA

electronica India productronica India ▶
September 26–28, 2018
Bengaluru, India

AltiumLive 2018: Annual PCB Design Summit ▶
October (Dates TBA)
San Diego, CA and Munich, Germany

electronicAsia 2018 ▶
October 13–16, 2018
Hong Kong

SMTA International ▶
October 16–17, 2018
Rosemont, Illinois, USA

TPCA Show 2018 ▶
October 24–26, 2018
Taipei, Taiwan

electronica 2018 ▶
November 13–16, 2018
Munich, Germany

HKPCA/IPC International Printed Circuit & South China Fair ▶
December 5–7, 2018
Shenzhen, China

Additional Event Calendars

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