MAY 2019

# DESIGN007
## MAGAZINE

**DESIGN RULES**

are like through-holes—
everybody has one!

# DESIGN007
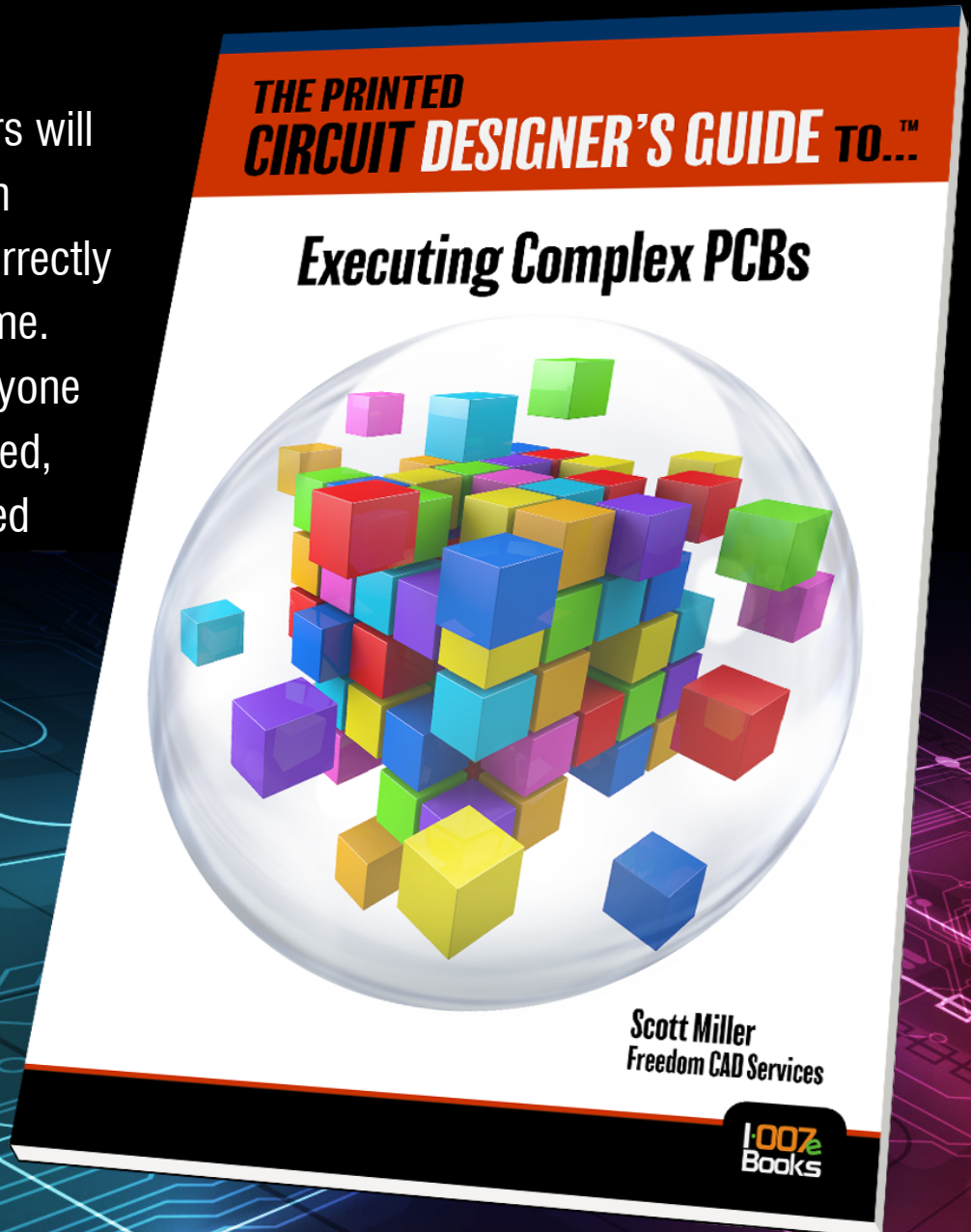## MAGAZINE

# Design Rules

We've heard a lot about design rules lately, from designers and manufacturers alike. There just doesn't seem to be much agreement about design rules: how to set them, manage them, and validate them. We've seen how the IC segment has standardized its design rules process; is this sort of alignment possible in PCB design? For this issue, we spoke with a number of design and manufacturing experts about design rules and constraints.

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# DESIGN007
## MAGAZINE

# Design Rules:
# For Your Own Good

## The Shaughnessy Report
### by Andy Shaughnessy, I-CONNECT007

Rules are a part of life, but most of us don't like following the rules; I certainly don't. But I think we can make an exception for design rules.

Many of you remember simpler times when you didn't need any stinkin' rules. Those were the good ol' days. Try to design even a simple board now without some constraints.

Like most rules, design rules came about for your own good. And no single designer could possibly remember all of the constraints required to design one of today's PCBs. But with a set of well-defined design rules, a designer can execute the most complex PCBs on the first try.

I have to admit that I had no idea that designers had to contend with so many design rules for each design. Designers tell me they routinely have to set hundreds of design rules for the more high-tech designs. How does a designer manage all of these design rules and avoid over-constraining the design, which adds unnecessary cost and complexity?

One thing that struck me while working on this issue was how little agreement exists about best practices for design rules. If you ask a half-dozen designers to explain their approach to design rules, you might get a half-dozen answers.

It reminds me of the Wild West. You may have design rules for schematic, layout, fabrication, signal and power integrity, thermal, and assembly. With high-speed boards, you may have to set up matched-length, differential pair, DDR, and spacing constraints. And that's just the tip of the iceberg.

Today's more powerful PCB design software tools all feature constraint editors that make setting and managing design rules about as simple as it's going to get. But setting up design rules is still a time-consuming part of each design cycle.

Is there a model for us to follow? Our friends in the IC arena figured out design rules years ago. Of course, that's a whole different ballgame with only a handful of manufacturers serving that market. But those manufacturers laid down the law. "If you want to work with us, here's what you're going to provide us, every time." That took care of that

problem. But that may not work for our segment with thousands of PCB fabricators worldwide.

So, we asked our expert contributors to discuss possible paths forward regarding design rules. First, we have a wide-ranging interview with Mike Creeden of San Diego PCB and Freedom CAD's Scott McCurdy, Jay Carbone, and Rich Kluever who discuss design rules from the perspectives of designers and fabricators as well as the need for a universal design data input. Next, we have a short excerpt from the new I-007eBook written by Scott Miller from Freedom CAD titled *The Printed Circuit Designer's Guide to… Executing Complex PCBs*, which focuses on using design rules.

Then, columnist Barry Olney weighs in with a feature on high-speed design constraints, explaining how to set design rules based on pre-layout simulation, and how IPC's guidelines can go a long way toward helping designers set constraints. In an interview, Altium's Craig Arcuri follows up with a look at design rules from his vantage point of running both design and manufacturing companies, and why this industry, especially design software, must evolve sooner rather than later.

We also have an interview with Dave Wiens and Mike Santarini of Mentor, a Siemens Business, who explain how design rules are part of the "shift left" movement to enable more decision-making earlier in the design process, and why PCB designers of today must have cross-domain awareness to succeed. Columnist Tim Haag explores the need for design rules and knowing when it's okay to break them. Then, columnist and author Mark Thompson highlights some of the challenges related to setting design rules for tight tolerances, and why negotiation is sometimes needed.

We also have columns from our regular contributors, including Bob Tise of Sunstone Circuits, Jade Bridges of Electrolube, and Stephen Chavez representing the IPC Designers Council. Further, we have a great article by Linda Mazzitelli of PTC that investigates the ongoing convergence of ECAD and MCAD technology.

It's a great time to be in this industry. See you next month! **DESIGN007**

**Andy Shaughnessy** is managing editor of *Design007 Magazine.* He has been covering PCB design for 19 years. He can be reached by clicking here.

# 2D Materials May Enable Electric Vehicles to Get 500 Miles on a Single Charge

Lithium-air batteries, which currently are still in the experimental stages of development, are poised to become the next revolutionary replacement for currently used lithium-ion batteries that power electric vehicles, cellphones, and computers.

Lithium-air batteries can store 10 times more energy than lithium-ion batteries and are much lighter. However, lithium-air batteries could be even more efficient and provide more charge with the incorporation of advanced catalysts made from two-dimensional materials. "We are going to need very high-energy density batteries to power new advanced technologies that are incorporated into phones, laptops, and especially electric vehicles," said

Amin Salehi-Khojin, associate professor of mechanical and industrial engineering in the University of Illinois at Chicago's (UIC's) College of Engineering.

One of the reasons the 2D TDMCs performed so well is because they help speed both charging and discharging reactions occurring in lithium-air batteries. They also synergize with the electrolyte.

Poya Yasaei, Zahra Hemmat, Pedram Abbasi, Shadi Fuladi, Xuan Hu, Robert Klie, Fatemeh Khalili-Araghi, and Baharak Sayahpour of UIC and Robert Warburton and Jeffrey Greeley of Purdue University are co-authors on the paper.

(Source: UIC)

# Design Rules Recipe:
# Solvability, Manufacturability, and Performance



## Feature Interview by The I-Connect007 Editorial Team

One thing that we've noticed lately: Each designer seems to have his or her own way of using PCB design rules. There doesn't seem to be much agreement about setting or using design rules.

So, in this true experts panel, Mike Creeden of San Diego PCB joined Freedom CAD's Scott McCurdy, Jay Carbone, and Rich Kluever to share their views on PCB design rules. This wide-ranging discussion with Andy Shaughnessy, Nolan Johnson, Barry Matties and Happy Holden covers everything from identifying the required constraints to setting electrical and manufacturing design rules and managing these often disparate requirements.

**Andy Shaughnessy:** Welcome, gentlemen. The topic of design rules keeps popping up, and there's not much agreement about best practices. Or is there? Mike, can you talk about how you go about setting up design rules?

**Mike Creeden:** Design rules help us utilize the strength of our CAD tool to make the circuit do what we want it to do, and that occurs in three areas. I always talk about what I call the "designer's triangle," which are three perspectives when we look at the layout.

The first perspective would be the layout solvability. You have to solve the layout, and your design rules enable you to do that. I'm able to pin-escape from fine-pitch parts, and at the same time, I want to balance that with DFX or DFM. Second, physically speaking, I must address the concerns for the manufacturing process and capabilities of my supply chain. I want to optimize them because the more robust I can make it, the higher producibility and reliability I would have long term and in a production volume. Third, the other perspective is performance. Performance is many things, including signal integrity, power delivery, thermal, etc., and all those things have to be met.

We don't want to over-constrain anything. And you cannot do one or two of those perspectives I just mentioned and ignore the other one. When we apply our design rules, there might be an EE as well as a layout person—sometimes, that is the same person—and then there's also design rules from the manufactur-

ing supply chain. They may be different than the physical layout rules to pin escape. All design rules should be added as early on in the layout cycle as possible. Then, it's correct by construction.

**Shaughnessy:** Scott, can you take us through your process?

**Scott McCurdy:** I approach the design industry coming from my background of running a PCB fabrication company, where half the things that came to us had to be put on hold because something was wrong in the design. Sometimes, there was

Scott McCurdy

just no adult supervision at the other end. At Freedom CAD, we are a PCB design service bureau and create hundreds of designs each year, so I'm also including Jay Carbone, one of our top designers who lives for this stuff and is one of our better "interactors" with engineers, in this conversation. We deal with a lot of different personalities and skill levels. I also brought Rich Kluever, who was at Solectron for many years at the CM level running Valor, identifying design problems at the factory that was going to have to assemble this stuff. Rich has tried to bake into our process and people more of a manufacturing perspective because every one of our designs goes through Valor twice.

**Jay Carbone:** I can identify with the "designer's triangle" concept because that's a constant battle. A schematic is a perfect world; as soon as we put a piece of etch down on a board, we've compromised that perfect circuit. With RF circuitry, assembly rules go out the window. Sometimes, RF engineers want to piggyback caps or share component pads. Various technologies dictate different sets of rules; there's no one-size-fits-all solution.

We start with a kickoff meeting with the electrical engineer to go over the circuitry and

technology. From there we start putting in the rules. We like to identify potential signal integrity issues up front. As far as spacing and line widths, this might be a little bit further down the road as you handle the placement and become more familiar with the components, etc. For example, maybe they can get away with using five or four mil traces for ease of manufacturing, or maybe they're down to a 3.5 for impedance reasons.

**Creeden:** You can only put so many rules in today's modern CAD tools. The eyeball check that designers do so often is understated and undervalued. The other thing I wanted to address is an idea for a universal output. Scott and I had this discussion earlier. We have a universal output, such as ODB++ or IPC-2581, which are intelligent data formats for output. As an industry, we do not have a universal intelligent data input. I've talked to a couple of the CAD manufacturers, and they're all thinking about it, but they want to make it their own proprietary blend. Instead, I would encourage them to have a universal input that any fabricator could use; then, it could be used by whatever CAD tool the designer uses.

**Nolan Johnson:** Scott, I was wondering if you'd be willing to drill down on that for a little bit. A universal input is a great idea. What do you envision that looking like?

**McCurdy:** At some point, it needs to be a data file, and I envision it being the same thing as an ODB++ or IPC-2581 where it's universally portable into any CAD tool. It would show the manufacturer's process constraints and capabilities matrix as well as the stackup in the usage, material, and copper weights. All of these things exist in little islands of automation, but I would like to see a fabricator create this input where any CAD tool could read it.

**Johnson:** What do you see as a mechanism for bringing better control over design rules down to the designers who work toward the bottom half of the bell curve?

**McCurdy:** The manufacturer can output at the start of the job what their capabilities matrix are. When any designer approaches a part, they're going to look at the densest BGA on the board first, the highest pin-count device, and what the pitch and feature size is. That tells them what they need to use for minimum features to pin escape and sets up a whole chain reaction of design rules for the solvability.

**Carbone:** To your point of the designer's triangle, I would look at the technology and my highest speed first. Is back-drilling allowed? How many layers am I going to need to exit that BGA? In the end, my dielectric may be so thin that I have 3.25-mil lines because I have a 28-layer card and I can only have .102" to do it in. Now, I have to go back to the manufacturer and customer and say, "This is the box you put me in. Can this be fabricated? What are the yields on this, and what can we do to mitigate loss?"

**Barry Matties:** Do designers typically know who's going to be manufacturing the board when they set out to design the board, or does that happens post-design?

**Creeden:** That's a great question, and it gives as many answers as there are designers out there. But as someone who has done some public speaking on this subject, the designer should know to seek that information right upfront. And if you do not have it, you're just doing a small run or a debug board, for example. Or your procurement people don't want to tell you who they're building with, so you have to design for the solvability portion of the triangle, such as what do you need to pin escape.

**Matties:** We were talking to some suppliers yesterday about materials and how it affects the design of PCB boards and base material laminate, and they indicated that a designer will come to a fabricator, and the fabricator will say, "This is the material that we use." Then, the designer is pretty much locked into that.

**Creeden:** That's very true, and I work a lot with Insulectro who try to bring all of the materials to the fabricators out there. Material science is becoming much more integrated into high-speed design. It has to because the material is where the electromagnetic field exists. You must involve them at the beginning, and if the fabricator is making those decisions, you have to ask the electrical engineer or understand the performance requirements.

**Shaughnessy:** Rich, you come from a manufacturing background. What are some of the things when you are setting up design rules that you look for?

**Rich Kluever:** We're unique in the sense that we listen to questions about their supplier base and who their fabricator is going to be. We're in the middle where we take requirements from a lot of different customers and engineers and funnel

Rich Kluever

them through to various suppliers. We don't have a single path of where we always use the same suppliers or rules. I have my rules set to point me to things and let me make decisions. Again, we don't always know where everything's going, so we try to use the industry standard. We're constantly updating our knowledge base with the feedback we receive from some suppliers on things that are good and things that aren't.

**Matties:** What you're describing comes down to designer knowledge and expertise. What advice would you give to a new designer?

**Kluever:** Ask a lot of questions and work with us; a lot of our designers develop this experience. In the Valor group, we act as gatekeepers. We're not going to let you send something out that isn't manufacturable. It's a matter of building that knowledge base by receiving feedback and understanding where you

may have misunderstood or made mistakes before. Understand what all of the terms are. It's tough to just say, "Here's everything you need to know," because all of us on this call probably have been doing this for 30 years, and we don't know everything we need to know.

**Matties:** Is there a design review process that a service bureau offers versus just doing the design?

**Creeden:** I deal with this a lot as a trainer, and I think your question is, "What about the EE who has now been conscripted to do PCB layout and has no design training in college?" We're looking hard at that subject. Surveys say

Mike Creeden

that 50–60% of designers will be gone in five years, so that knowledge base will be gone. But the industry thinks a MOOC (massive open online course) class can be a Band-Aid solution. It's an online course that you can take in two hours to learn how to be a designer. Anyone who has been in the business for a while laughs because it's so ineffective.

**Kluever:** And it's important to understand the "why" of the rules as much as the "what." You're going to have times that you will have to balance these things and make tradeoffs. You need to understand which one you can give more than another, and if there is a fail, is it a less serious fail than something else? For example, finding a failure in the fabrication process is better than finding one after you've soldered on a $1,000 BGA.

**Matties:** It sounds like there's no piece of software or book that will guide you to that end.

**Happy Holden:** Yes, but that's the problem. Design rules can be determined mathematically,

but unfortunately, nobody is taking the time to put down rules or write the software that essentially creates a planning tool. I've looked at this for the last 40 years, so I have a planning tool, but I can't sell it because it has no documentation and if you look at it cross-eyed, it will go apart, but I call it a virtual prototype. Our industry keeps adding new sets of rules as we come up with other devices and constraints. For example, there are requests for designers to design for recycling and being environmentally friendly.

**Matties:** With the movement to the digital factory and smart manufacturing, what impact, if any, is that playing on the design community?

**Creeden:** I'm not seeing much at all, but I'm sure hoping that universal manufacturing rules are a byproduct of it. One of the most advanced, leading factories is GreenSource Fabrication is in New Hampshire, and at some point, the industry's goal is that the automation that they have would be transferable to the layout project.

**Matties:** A whole new level of data will have to be uniform and provided.

**Kluever:** I don't see how there could be one rule that fits all because all of these manufacturers have such a wide range of capabilities.

**Creeden:** Nobody's saying that there's one rule; we're saying that there's one format whereby each factory can plug in their capabilities matrix and process allowances.

**Holden:** Yes, that's what I call the virtual prototype or the design planner, which is badly needed software. One of the things I saw while working with Freedom CAD on their eBook is that the majority of their work is in the front-end planning of the design—not operating the EDA tool.

**Johnson:** Happy, I just want to tie the thought that you just made back to something that Rich said earlier, describing your Valor model as being a user and defining your rules in

such a way that it started to flag areas that you wanted to pay attention to. Rather than just straight-up manufacturing violations, which is how everybody seems to look at how they define the rules, you have a philosophically different approach, and Happy is touching on that too. When you change to that sort of a thinking model, how did that change using the tools and results?

**Kluever:** It requires you to be a lot more interactive with the tool in making decisions and not letting the tool make the decisions for you. I'll give you a good example with solder mask clearance. Some people want the solder mask to be designed exactly as they want the end product to be, whether it's two- or three- mil clearance and some mask defined pads. There are folks that roll up all of their solder mask at one-to-one and let the fabricator modify it accordingly.

In our world, how do I set a rule for that? I have multiple rules. I set a rule very high so that all of the solder mask fails. Then, I let the tool do the math for me and segregate the results. Now, I can look at it, and say, "All of the solder mask has two-mil clearance." If 90% of it is two-mil clearance, but six parts are one-to-one, I don't like that. So, I focus on those six parts and adjust them to be two-mil clearance so that everything is the same.

**Creeden:** I think what Happy was alluding to was intelligent input for rules. When do you use your rules? When do you apply them? When do you check them? If you're doing them at the end of the design, you're going to find errors, but those are very costly. When you appropriate correct-by-construction methodologies supported by your toolset, whatever that may be, you're correct by construction.

**Matties:** Are there any housekeeping rules that we should have for managing design rules? In other words, how do we keep them organized, and what should people think about?

**Creeden:** To me, they're relative to the circuit and fabricator or manufacturing supply chain

you're using. Essentially, rules don't stand alone by themselves because there are 1,000 rules out there. I want ones that apply specifically to the circuit I'm doing, and I'm going to implement it to achieve the performance of the circuit as well as how I'm going to build it with reliability and have the circuit perform the way I want it to.

**Matties:** Do you create a new set of rules for every design that you're starting?

**Creeden:** Absolutely. They're similar, but every circuit is its own entity for rules. I may use a rule set that I used someplace else, but rules have to be assigned to parts, nets, areas, features, layers etc. I never want to assume that if a rule worked on a previous circuit, it will also work here.

**Matties:** That's great advice because, for a manufacturer, you may fall into, "I've used these rules in the past with this manufacturing and it's going to apply here again." Does that happen?

**Creeden:** Yes, because factories do have a capability matrix, and they may be the same, but how they apply them on a four-layer board is different than how they would on a 12-layer board. You have to drill down, and ask, "How does this board work in this factory?"

**Carbone:** Multiple plating cycles or a different stack-up could change the line widths or impedance of a proven circuit. There are many different factors for changing stack-ups or moving a circuit to different layers of the card.

Jay Carbone

**Kluever:** You also have to consider the conditions of your design and what you're trying to do. I've had cases where people apply a rule, such as a solder mask oversize on a BGA, and say, "Yes, but we've always used this and it

works," to which I respond, "But in the past, you didn't try to route a trace in between these paths." They've changed the condition of the design, so the rule doesn't apply anymore. You also have to understand where those rules truly apply.

**Holden:** Because semiconductors are constantly becoming more complicated, every time you start a new project, there's probably a new set of constraints that dictates that you have to come up with a new set of rules. The rules used last time, even for this company, now conflict because it doesn't meet signal integrity, cost, etc. It's something that everybody learns, which is unfortunately why we say we're concerned about experienced professionals retiring.

**Creeden:** Happy, you hit on something that I think is very important for us to touch on as a group. How do rules interact? For example, if I'm doing DDR, I'm going to match lengths on a bus. CAD tools are so powerful that I can match it to the micron and they can do it. It may not even need it, but we do it anyway because we like that power and want to match it. Often, we need to ask if there's a package delay coming off the chip and if that has been factored in. If I have two forward crosstalks and I'm external, that just made the problem worse. It's not as black and white as "I have some rules. Let's implement them." There's an environmental consideration that needs to be looked at.

**Shaughnessy:** Because it sounds like a lot of hours are being spent on setting up these design rules.

**Creeden:** Well, correct by construction—you either want it right, or you don't, so pick one.

**Matties:** There's no time to do it right but plenty of time to do it over.

**Shaughnessy:** I just want to acknowledge the wisdom and expertise that is being shared on this call. Do you have any final thoughts?

**Creeden:** My closing thought would be that a design will only be as accurate as the rules that constrain it. Those rules need to look at it from the three perspectives I mentioned: solvability, manufacturability, and performance.

**Matties:** Thanks for all of your input today. It's greatly appreciated.

**Creeden:** My pleasure.

**McCurdy:** Thank you.

Visit I-007eBooks.com to download *The Printed Circuit Designer's Guide to… Executing Complex PCBs* written by Scott Miller from Freedom CAD Services Inc. as well as other free, educational titles. **DESIGN007**

# Wrap-around Sensors for the Grid

Scientists at Oak Ridge National Laboratory have developed a low-cost, printed, flexible sensor that can wrap around power cables to precisely monitor electrical loads from household appliances to support grid operations.

Using an inkjet printer, researchers deposited wires on a flexible plastic substrate, then wove in a magnetic strip to channel the flux produced by an electric current, making the sensor suitable to install in tight spaces. When tested on conductors in the lab and on a building HVAC unit, the sensor measured responses of up to 90A of electrical current and is expected to exceed 500A in larger applications.

"These inexpensive sensors provide crucial, real-time usage data needed to monitor and control devices, such as smart HVAC and water heaters for better power grid efficiency and resilience," said Pooran Joshi, a senior scientist in the Materials Science and Technology Division at ORNL.

The team is currently testing new materials, electronics, and packaging to increase the sensor's range and applications while keeping costs low.

(Source: Oak Ridge National Laboratory)

# Design Rules, Simulations, and Analyses

GETTING IT done RIGHT the *FIRST* TIME

*Timing is everything in life and complex PCBs.*
—Anonymous

The following is an excerpt from Chapter 5 of *The Printed Circuit Designer's Guide to… Executing Complex PCBs* written by Scott Miller of Freedom CAD Services.

It is a fact that complex electronic components will not function properly unless a specific set of physical conditions is met. Active components and chipset performance requirements are presently being pushed to the edge. Their capabilities are only limited by the physical geometry and electromechanical properties of the materials that interface with them. We have come to the point where component chip makers are supplying 100-page user manuals describing not only what a chip can do, but also the layout, assembly manufacturing, and environmental operating criteria required for it to perform. Careful attention to these rules must be considered for the successful operation of the individual component within a circuit and the performance of the circuit in relation to all circuits on the PCB.

One designer said:

"Signal and power integrity analysis is a key way to ensure that the board design will meet the performance requirements on the first pass. By using software to simulate the effects on signal and power integrity, our customers spend less time in the lab trying to find out why their design isn't performing as expected. Performing in-process simulations enables problems to be identified and corrections to be made earlier in the design process, thus minimizing the collateral damage. The more items you have to move to address a problem, the more time this takes."

## Starting the Physical Design Process

The next step is entering the execution phase of the board design process, which involves implementing all of the elaborate pre-planning that has already taken place.

## Layout Processes

Many companies employ a number of specialized layout processes. One senior project engineer explained his process for very complex boards that he has refined over many years:

"I work with larger OEMs, and this is what I tell them. I go through their design and create libraries of templates to give us predictabil-

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ity and efficiency. What I do is predictive engineering, which is to reuse circuits that they've already used. If they are a repeat customer, they already know it works, and now suddenly it saves them in fabrication, assembly, tests, and debug. They save a boatload of money and end up with fewer spins.

Our process is to create reusable modules. This allows us to use parts that you've already used, and if it's a new part, we go ahead and do a module for it; just substitute the old one for the new one after we've modified it. So, from that point on, after it has been proved to work, it works for us.

First, we have them define stackups ahead of time. We sit down with the customer and their fabrication shop and determine whatever layer count they feel with this particular company works best. We build in all of the fabrication capabilities that their fabrication house has because they usually have more than one fabrication house. We're just trying to define everything ahead of time so that it now becomes predictable.

Then, you place and replicate as much as you can. That's really what it comes down to. When the placement is done, you do placement verification. Then, once that's all done, approved, and cleaned up, you route all of the differential pairs and high-speed clocks. Next, you send that to engineering for them to review and route the remaining signals, which are pretty much single-ended nets, matched groups, etc. That last step is final verification. When we get to that, we send them a final board to review. We can do it in two weeks when we have all these pieces in place because it's already designed.

"At least I know that the replication process or reuse process is very good. It works, and people that have experienced it like it. And now the tools are better."

The process is as follows, using clusters, templates, and bundles:

- Auto-cluster from schematics
- Auto-place for complex parts
- Place
- Replicate and/or reuse templates
- Placement verify (refine)
- Fabrication and assembly review
- Cluster nets into bundles and route
- Complete routing with constraints
- Engineering review for SI, PI, and power distribution network (PDN)
- Rest of routing
- Validation (DFM and DFT)
- Create a template for future use
- Customer review
- Deliverables

Visit I-007eBooks.com to download *The Printed Circuit Designer's Guide to… Executing Complex PCBs* as well as other free, educational titles. **DESIGN007**

# Words of Advice for New PCB Designers

In a recent survey, we asked the following question: What do you think is the most important thing a designer should remember when planning a new PCB design? Here are a few answers, edited slightly for clarity.

1. Have a good music selection.
2. Don't panic. It's almost always possible to complete a complicated design if you go step by step.
3. How will the board be fabricated and how will it be assembled? Both of these will affect cost and reliability.
4. Place with flow planning for routing in mind.
5. Each design has its own restriction and requirements. And each design is a new challenge. Communicate with the team and gather all information (mechanical, environmental, SI, PI).
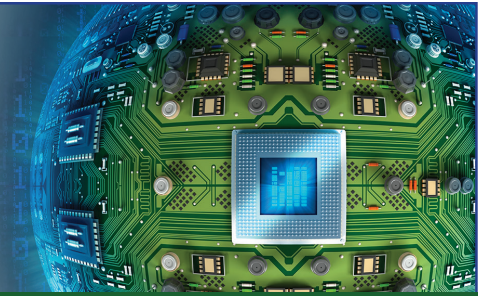
# ITI & IPC Conference on Emerging & Critical Environmental Product Requirements

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For more information, contact **Ken Schramko**, IPC senior director of North American government relations, at **KenSchramko@ipc.org**.

# High-speed PCB Design Constraints

## Beyond Design

**Feature Column by Barry Olney,** IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Digital design has entered a new realm. Modern high-speed design (HSD) not only requires the designer to continuously break new ground on a technical level but also requires the designer to account for significantly more variables associated with higher frequencies, faster transition times, and higher bandwidths. Ignoring signal and power integrity and electromagnetic compatibility invites schedule delays and increases development costs and the possibility of never succeeding to build a functional product, which is a career-limiting strategy.

The key methodology is to understand the underlying high-speed design issues and then translate these into corresponding design constraints that will be adhered to during the entire design process. It is best to develop these high-speed design constraints based on pre-layout simulation (Figure 1).

We had a few critical nets to manage in the past, but now, it seems that a significant number of interconnects are critical. Also, each design requires a specific set of constraints based on the technologies used. Sure, we can port basic design rules for trace width, clearance, etc., from a previous design to the next, but individual constraints still need to be established. Constraint reuse is also limited by net and group naming conventions. If you are consistent, then porting is much easier.



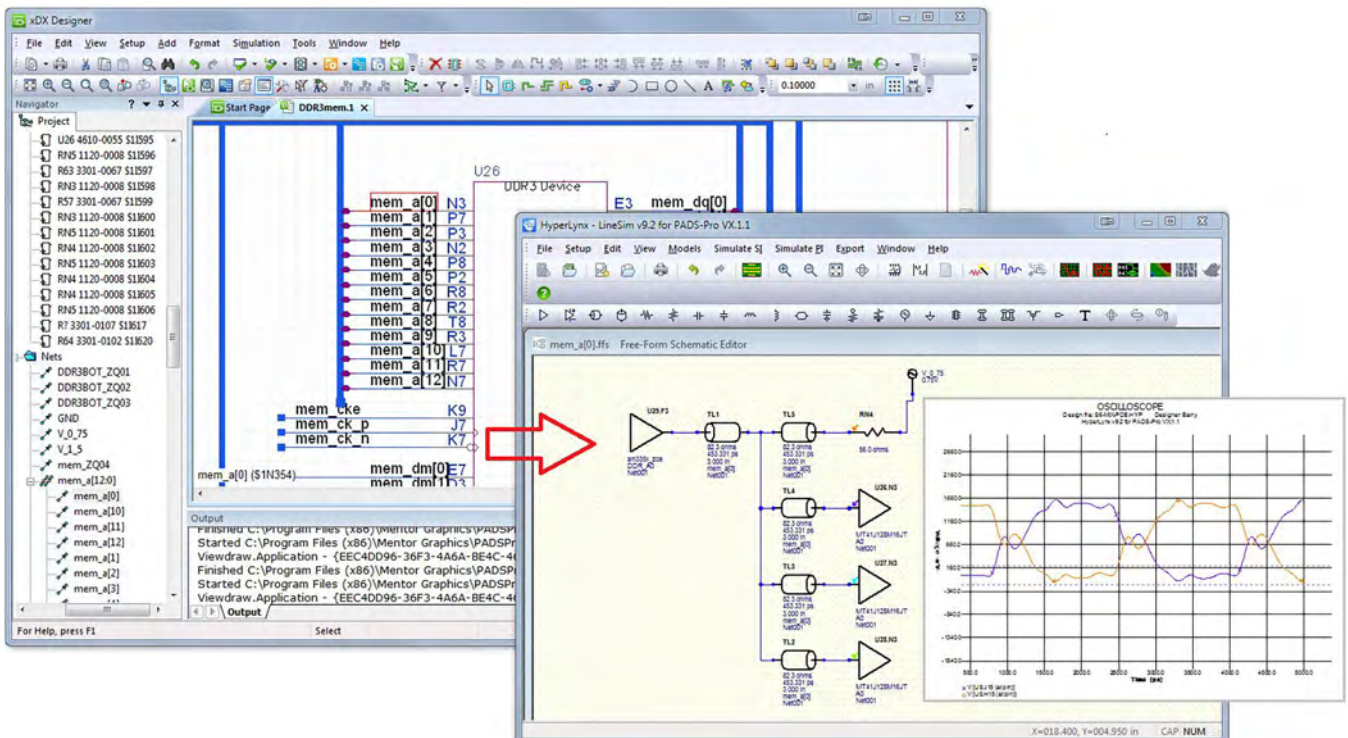Figure 1: Develop high-speed design constraints based on pre-layout simulation (xDX Designer to HyperLynx).
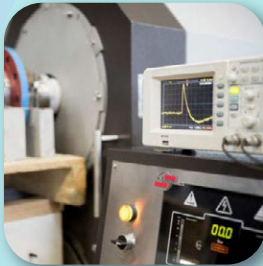
# Candor
## Circuit Boards

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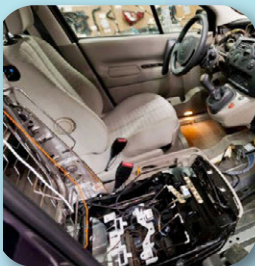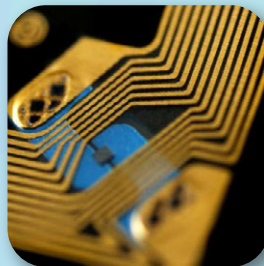Click to see what we bring to each sector of the industry:

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To begin with, every designer needs a set of well-established design rules to base the constraints on. IPC has provided the electronics industry with guidelines for designing and manufacturing PCBs compiled over the years with the support of both committee and industry members.

The IPC-2220-FAM: Design Standard for Printed Boards series is the bible for PCB designers. The series is built around IPC-2221B—the base document that covers all generic requirements for PCB regardless of materials. From here, the designer chooses the appropriate sectional standard for a specific technology.

The IPC-2220-FAM series includes:

- IPC-2221B: Generic Standard on Printed Board Design
- IPC-2222A: Sectional Design Standard for Rigid Organic Printed Boards
- IPC-2223C: Sectional Design Standard for Flexible Printed Boards
- IPC-2224: Sectional Standard for Design of PWBs for PC Cards
- IPC-2225: Sectional Design Standard for Organic Multichip Modules (MCM-L) and MCM-L Assemblies
- IPC-2226A: Sectional Design Standard for High-density Interconnect (HDI) Printed Boards

This series provides coverage on material and final finish selection, current-carrying capacity and minimum electrical clearances, test-specimen design, guidelines for V-groove scoring, dimensioning requirements, and conductor thickness requirements.

Also, several documents apply to HSD and land-pattern design:

- IPC-2141A: Design Guide for High-speed Controlled Impedance Circuit Boards
- IPC-2251: Design Guide for Electronic Packaging Utilizing High Speed Techniques
- IPC-7351B: Generic Requirements for Surface Mount Design and Land Pattern Standard

These standards (and their predecessors) have been part of a well-used section of my technical library since 1987. They provide excellent reading and reference material for all PCB designers. These documents are available for purchase from www.ipc.org.

Design rules must keep up with the latest devices and fabrication processes without losing sight of design for manufacturability (DFM). DFM is the practice of designing board products that can be produced in a cost-effective manner using existing manufacturing processes and equipment. If you follow the above IPC guidelines, you will be designing for both manufacturability and mass production. However, at times, one must stretch the rules a little to meet the specific requirements of a design. This is fine, providing you can justify the reasons and tolerate the consequence of your decision.

Entry-level EDA tools tend to rely on the skills of the PCB designer to detect possible issues as they arise during the design process. However, these days, a more constraint-driven, correct-by-construction approach is required for complex designs. Once the rules are established, they will be followed by downstream tools and validated to conform by the various design rule checkers (DRCs). A spreadsheet format is more efficient if you are dealing with a high volume of constraints, sorting, filtering, and duplicating constraints.

Constraint management:

- Enables better synchronization between schematic and layout
- Streamlines access to relevant PCB data
- Eliminates errors due to data integrity issues
- Promotes greater reuse of PCB data

Figure 2 illustrates typical constraints planning and definition for a high-speed DDR2 and DDR3 design. Constraints should be defined at the schematic level and flow through to the layout process. The advantage of this approach is that the engineer can convey their intent to the PCB designer without misinterpretation. Alternatively, the independent engineer (who does everything) can manage the constraints

File  Edit  View  Setup  Filters  Tools  Data  Output  Help

| Constraint Class/Net | # Pins | Net Class | Topology | |
|---|---|---|---|---|
| | | | Type | Ordered |
| (All) | | (Default) | MST | |
| DDR2 | | (Default) | MST | |
| DDR2_Unused | | (Default) | MST | |
| DDR3 | | (Default) | MST | |
| Address | | ddr3_address | MST | |
| clocks | | ddr3_clocks | Chained | |
| control | | ddr3_control | MST | |
| Data | | (Default) | MST | |
| Group0_1 | | (Default) | MST | |
| Group2_3 | | (Default) | MST | |
| ExpoDemoAnalog3v_(All) | | ExpoDemoAnalog3v_(... | MST | |
| ExpoDemoPower0_9_(All) | | ExpoDemoPower0_9_(... | MST | |
| ExpoDemoPower_(All) | | ExpoDemoPower_(Def... | MST | |
| fs_addr | | (Default) | MST | |
| fs_data | | (Default) | MST | |
| mictors | | (Default) | MST | |
| PCI_Express | | PCI_Diffpairs | MST | |
| Power_0_9_(All) | | (Default) | MST | |
| Power_1_5_(All) | | ExpoDemoPower_(Def... | MST | |
| Power_1_x_(All) | | (Default) | MST | |
| Power_3_0_(All) | | ExpoDemoAnalog3v_(... | MST | |
| Power_3_x_(All) | | (Default) | MST | |

Navigator

- Schemes
- Net Classes
  - (Default)
  - DDR2_Addr_Cntrl
  - DDR2_Clocks
  - DDR2_Data
  - DDR2_Strobes
  - ddr3_address
  - ddr3_clocks
  - ddr3_control
  - ddr3_extra
  - ddr3_group0
  - ddr3_group1
  - ddr3_group2
  - ddr3_group3
  - Diff
  - ExpoDemoAnalog3v_(Defa.
  - ExpoDemoPower0_9_(Defa
  - ExpoDemoPower_(Default)
  - Gnd
  - PCI_Diffpairs
  - PCI_RX_Diffpairs
  - PCI_TX_Diffpairs
  - Power
  - Special
- Clearances
- Constraint Classes
- Parts

Trace & Via Properties / Clearances / Nets / Parts /

Output

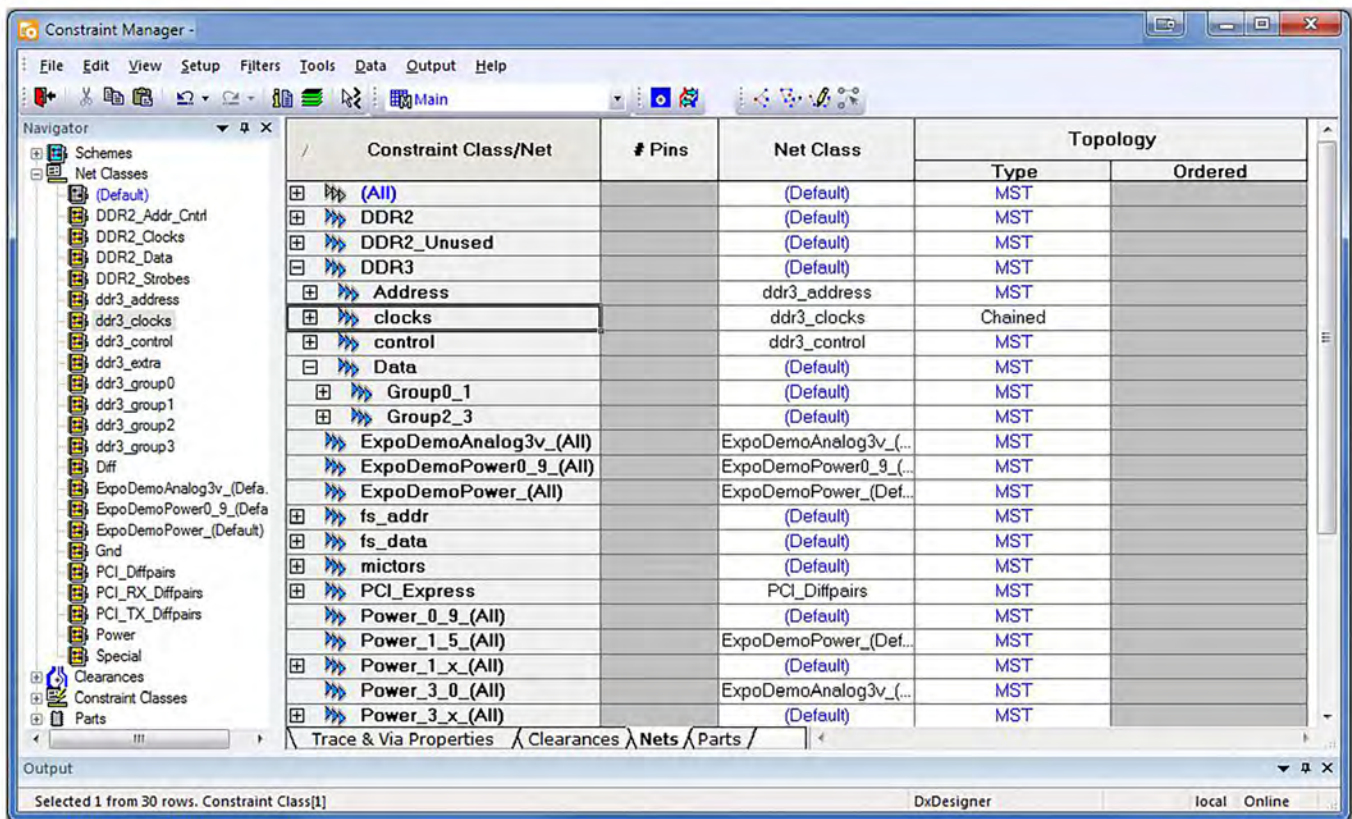Selected 1 from 30 rows. Constraint Class[1]          DxDesigner          local  Online

Figure 2: Constraints planning at the schematic level (PADS Professional).

throughout the design process using the same consistent management tool. Also, the reuse of constraints from a previous proven design not only ensures consistent rules but also minimizes the possibility of errors.

Net classes are used to organize and speed up the definition of routing constraints for nets with similar properties. For each net class, the layers allowed for routing, the corresponding trace width range for these layers, and the via types allowed can be defined. For differential pairs, a layer-dependent differential pair gap can be defined based on the calculated impedance to ensure uniform impedance across all layers.

The proper grouping and definition of net classes and constraint classes in the early stages of the design process simplifies constraint definition and management significantly. Grouped constraints can increase layout efficiency, reducing design time, and, ultimately, lower PCB design costs.

With DDRx design, it is also a requirement to assign layer sets to data lanes/strobes and ad-dress, command, and control (ACC) and their associated clocks to ensure matched propagation delay. Signals within a group should be routed on the same layer with each path having the same via count. Even if the trace widths are adjusted on each layer, so as the impedance is identical, the propagation speed of microstrip (outer layer) is always faster than stripline (inner layer), typically by 13–17% (Figure 3). The speed of propagation of digital signals is independent of trace geometry and impedance and is solely determined by the dielectric constant of the material the electromagnetic energy propagates in.

The higher the signal frequency with which the designer must contend, the more complicated will be the PCB design. Complex PCB designs require deep knowledge and experience and simulation tools. However, it is not always necessary to route traces as short as possible, differential signals as close as possible, or to avoid crosstalk as much as possible. Rather, it depends on the signal's significance. Basically, the designer must know which are the sensi-
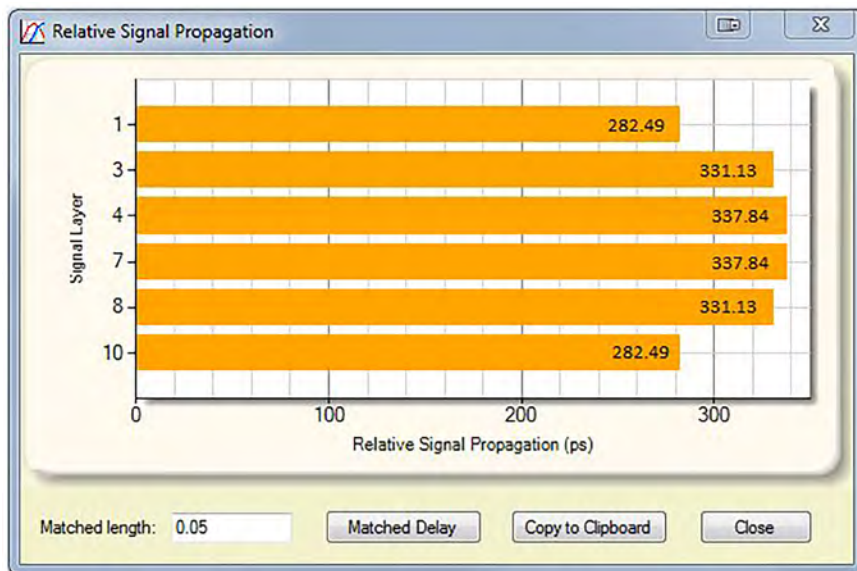
Figure 3: Relative signal propagation of microstrip and stripline (iCD Design Integrity).

tive parts in the circuit or where problems due to reflections and crosstalk can occur. With this knowledge, good placement of the devices can be made. Because placement is such an important step in high-speed design, the designer will do well always to keep it and the return current in mind.

With higher frequencies and faster transition times, the digital system timing budget is also of the utmost importance. The timing budget is the account of timing requirements necessary for a system to function properly. For synchronous systems to work, timing requirements must fit within one clock cycle. A timing budget calculation involves many factors, including setup and hold time and maximum operating frequency requirements. By calculating a timing budget, the limitations of conventional clocking methods can be seen. This data can then be translated into routing design constraints.

The first step in establishing the timing budget is to define the initial system timings. To do this, one must obtain estimates of the minimum and maximum output skew from the silicon vendors. This information is generally available in the IC datasheets. Then, define the setup and hold times for the read and write cycles. The timing budget for each component is then calculated given a certain margin. What-

ever is left over (if anything) can then be allocated to the board-level interconnect design. This is the only factor that PCB designers can influence. If there is no margin left for the interconnect, then the silicon numbers need to be retargeted, or an easier solution might be to decrease the clock speed. This is why a shoddy design may work at a low frequency but not at full speed. Timing is everything in high-speed design.
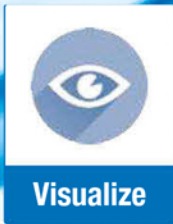
In conclusion, PCB designers need to understand the underlying high-speed design issues of the design based on simulation and then translate these into corresponding design constraints. Constraints can always be altered on the fly if a particular constraint is too tight, providing the designer can justify the easing of the specification and that the product is still manufacturable.

## Key Points:
- The key methodology is to understand the underlying high-speed design issues and then translate these into corresponding design constraints
- High-speed design constraints are based on pre-layout simulation
- Constraint reuse is limited by net and group naming conventions; if you are consistent, then porting is much easier
- IPC has provided the electronics industry with guidelines for designing and manufacturing PCBs
- Entry-level EDA tools tend to rely on the skills of the PCB designer to detect possible issues as they arise during the design process
- A constraint-driven, correct-by-construction approach is required for complex designs
- Constraints should be defined at the schematic level and flow through to the layout process

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- The proper grouping and definition of net classes and constraint classes in the early stages of the design process simplifies constraint definition and management significantly
- The propagation speed of microstrip (outer layer) is always faster than stripline (inner layer), typically by 13–17%
- The speed of propagation of digital signals is independent of trace geometry and impedance and is solely determined by the dielectric constant of the material
- The designer must know which are the sensitive parts in the circuit or where problems due to reflections and crosstalk can occur
- The timing budget is the account of timing requirements necessary for a system to function properly
- The timing budget shows the limitations of conventional clocking methods and can then be translated into routing design constraints **DESIGN007**

## Further Reading

- Olney, B. "Beyond Design: The Need for Speed–Strategies for Design Efficiency," *The PCB Design Magazine,* March 2016.

- Olney, B. "Beyond Design: Design Rules and DFM for High-speed Design," *The PCB Magazine,* June 2012.
- Olney, B. "Beyond Design: Signal Flight Time Variance in Multilayer PCBs," *The PCB Design Magazine,* December 2017.
- The IPC-2220-FAM: Design Standard for Printed Boards series, www.ipc.org.
- Hughes, S. "Why Impose Design Constraints?" Mentor, a Siemens Business.
- Martens, J. "How to Handle PCB Design Constraints Without Losing Your Mind," Mentor, a Siemens Business.
- Hall, S. W., Hall, G. W., & McCall, J. A. *High-speed Digital System Design: A Handbook of Interconnect Theory and Design Practices,* Wiley, 2000.
- Johnson, H., & Graham, M. *High-speed Signal Propagation: Advanced Black Magic,* Prentice Hall, 2003.

**Barry Olney** is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded from www.icd.com.au. To read past columns or contact Olney, click here.

# The First Walking Robot that Moves Without GPS

Researchers at CNRS and Aix-Marseille University (AMU), in the Institut des Sciences du Mouvement—Étienne Jules Marey (ISM), have designed the first walking robot that can move without GPS: AntBot.

Inspired by desert ants—which are considered extraordinary solitary navigators—AntBot can explore its environment randomly and go home automatically without GPS or mapping.

Ants use polarized light and ultraviolet radiation to locate themselves in space. Cataglyphis desert ants, in particular, can cover several hundreds of meters in direct sunlight in the desert to find food, then return in a straight line to the nest without getting lost. Distance and heading are the two fundamental pieces of information that, once combined, allow them to return smoothly to the nest.

AntBot is equipped with an optical compass used to determine its heading by means of polarized light, and an optical movement sensor directed to the sun to measure the distance covered. Armed with this information, AntBot has been shown to be able to explore its environment and to return on its own to its base with a precision of up to one cm after having covered a total distance of 14 m.

(Source: French National Centre for Scientific Research)

# Altium's Craig Arcuri on Design Rules: Past, Present, and Future

**Feature Interview by
the I-Connect007 Editorial Team**

We recently spoke with Altium's Craig Arcuri about his views on design and manufacturing rules. Craig has experience running both design and manufacturing companies, so he has a fairly circumspect view of constraints from both sides of the product realization process. In this interview, Craig details some of the challenges with setting and managing hundreds of often divergent design and manufacturing rules, and how both design and manufacturing constraints need to evolve to better serve all of the stakeholders in PCB design.

**Andy Shaughnessy:** Craig, there seems to be a lot of disagreement about design and manufacturing rules, and it seems that there's not much agreement on best practices. It's very fragmented, and everyone does design rules their own way. As an EDA tool company guy, what are users asking you all for regarding design rules?

**Craig Arcuri:** Let me give you a different perspective. Of the last three companies I ran, one was a design company that did engineering design and used CAD tools to create data that was then passed on to manufacturing. Although we tried to care, and said we cared, we really didn't worry about what happened after we sent the data out because that was somebody else's problem. Then it was poetic justice that my last two companies were manufacturing companies that had to deal with those folks who didn't really worry about what happened after the handoff to manufacturing!

You know the phrase "poop rolls downhill." Well, the manufacturing folks are pretty close to the bottom. At the end of the day, the engineer and layout person have done their job, and a big pile of data comes down and lands on manufacturing. My job is to make a physical thing in less time with less money at a higher quality than is probably reasonably possible given the pile of poop that I was given. Over the course of the last 10 years, I've seen 200–300 unique customers per quarter send the data to the manufacturing people, from the perspective of being close to the bottom.

Some of the data comes from companies like Google, Tesla, Intel, and Microsoft. You might think that those companies would provide pristine data and that the design rules would be absolutely well-defined, followed, and imple-

Craig Arcuri

mented in the design EDA tool, and translated through the software into a package where I would think, "This is going to be a piece of cake. What am I going to do with all the money I'm going to make?"

You might also assume that the little guys come across with data out of CAD tools like Eagle and KiCad where a consistent database is a thing of dreams, and it's a bunch of disconnected data that may or may not have any sanity to it. But you would be sadly mistaken. Across the board, manufacturers rarely receive a data package where manufacturing rules have been considered, adhered to, or worked around, and where the data has been presented in a way that shows that. The instructions are almost never clear and the board can't always be built.

Now, I won't put all of the blame on the designer or engineer. If you look at companies like Apple or Samsung, they expect most of the products they design to go into volume production very quickly. Regardless of their size, companies that expect a product to go in volume production clearly consider design rules and manufacturing issues during the design

process. They "design for manufacturing," as opposed to "design with manufacturing."

But everybody else typically has a designer or an engineer in front of a computer screen. And it's not that they don't want to know more about manufacturing. It's not that they want to choose components that are hard or impossible to get or will be impossible to reflow because of their mass. They're not doing that on purpose, but part of it is that they're busy. They have a job to do, and that job is to create the electronic design and capture it in a CAD tool as quickly as possible and get that prototype to a manufacturer to build so that it can be validated back in the labs.

The engineers are never going to have time to understand the nuances of why a tall electrolytic capacitor next to an 0603 is going to have a shadow effect when it gets reflowed. For decades, manufacturers have beat on customers, I've been one of them, saying, "Please involve me earlier. I can consult with you, explain what things are important, and look at the designs as you do them."

Then, commercial reality comes in. At some point, a quote is given, and generally, customers don't want to involve a manufacturer early for commercial reasons because that would mean they'd be locked in. The only way we're going to have to solve that is with smart software that aims more at designing with manufacturing in mind so that the tools evolve in a way that is far beyond where they are today.

**Shaughnessy:** We've heard that before about how software needs to evolve, and some people see a role for AI. Do you think AI will be a part of this evolution?

**Arcuri:** Absolutely. And I'll say one more thing while I'm standing on my soapbox. I think DFM is the stupidest thing ever. I know, I've just said heresy (laughs). The layout is completed by a designer and the CAD tools. Then, the data is sent to a fabricator, and while the design is being cast in concrete, fiberglass, or resin, the data is sent to an assembly shop so that they can do DFM.

Well, what good is that? All I'm going to do with the DFM is learn what problems I'm going to have to solve on the manufacturing floor because it's already baked in concrete. I can't go back and say, "Stop the fabrication and start over again. Move that BGA 300 mils to the left so that it's not right on the edge of the board and won't need fixtures to run it down the line." I don't have that option. DFM is really just a preemptive alert for the manufacturing engineers to say, "This is the pile of crap that's heading in your direction, so figure out how to build it, and you can't change anything. Too bad." We have all of these rich CAD tools with lots of information about constraints, land sizes, via holes, and annular rings, and then we reduce that rich data down to Gerber data, which is about as dumb as a post, or ODB++, which is more intelligent.

Then, we give it to a fabricator and an assembly shop. In that whole process, I don't believe the humans and business paradigms involved are going to evolve in such a way that this can be done collaboratively. Due to commercial and technical reasons and how busy everybody is, I can't make a designer understand everything a manufacturing engineer knows and vice versa. The only place left to go is the software. We can create a software paradigm where this stuff happens in parallel. We have to.

**Happy Holden:** We've had that for 20 years in integrated circuit design.

**Arcuri:** Exactly! The parallels to that are shockingly obvious. I'm in love with whoever said that (laughs).

**Nolan Johnson:** That's a good one, Craig. Happy and I have IC backgrounds too. The PCB design tool flow seems to be 10–20 years behind where IC was. IC has been driven by huge monetary constraints to getting to silicon, which then forced the discipline that isn't present in PCB right now. Instead of having three shops and a $60,000 price tag for getting your first silicon, you're looking at a few hundred bucks at any one of 800 shops.

**Arcuri:** That's a very good point. The capital requirements for an IC factory are grossly large. There are 400–500 medium to small CMs in North America alone competing for all of this business. It's such a fragmented market, and it's not driven by the turn time. The cost of spinning an IC is astronomical compared to, "If we have to relay out the board and fabricate another board and simplify it more, that's not going to kill us." We're preaching to the choir.

**Johnson:** Let's take that complexity and add another layer because there are some trends going on here. We have that sort of complexity going on plus new design constraints that are coming all the time. There are so many specialized functions. You can't expect one designer to master them all, so how do the tools help them?

**Arcuri:** I've always wanted to know so much about something that I could call myself a thought leader in a subject area without laughing at myself, and I'm still looking for that thing. I am a pilot and am pretty good at flying, but to the extent that I am old now and have a lot of experience. Globally, we are embracing more and more collaboration across all walks. With the gig economy and services like Uber where software applications connect a

## Globally, we are embracing more and more collaboration across all walks.

customer with a seller, there's a piece of technology in the middle that facilitates that. People use the Uber analogy a lot, but the idea is that the devices we have are much more powerful and portable. We are much more comfortable, although it might be scary to many of us, with our data being someplace in the Cloud. Because when it's in the Cloud, it's a lot easier to create collaborative experiences because everybody can access it.
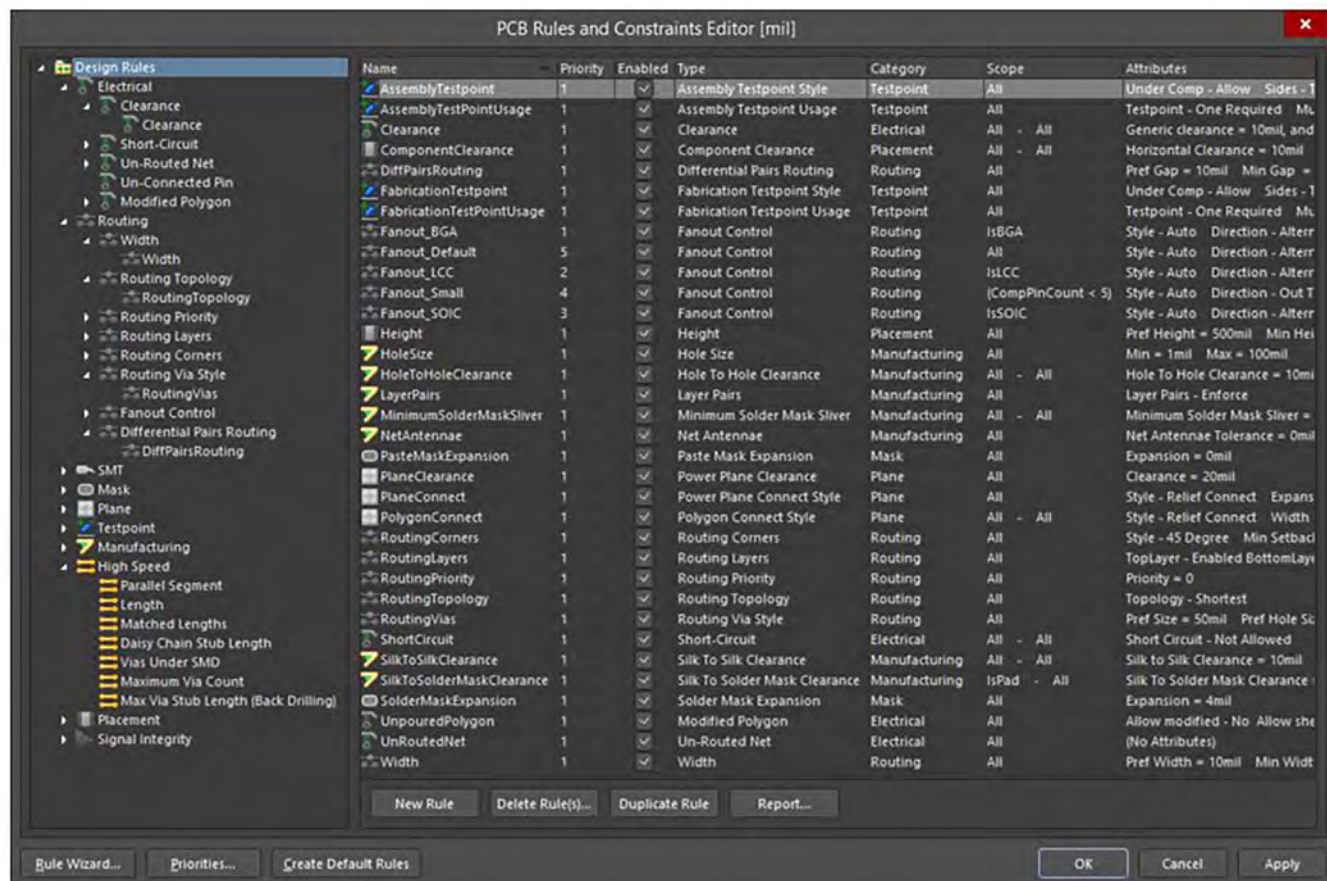
The Altium design rules editor.

It's not a case of FTPing or emailing files. We're all looking at the same thing, so that evolution is an enabler for companies like Altium to look at this very fragmented process and say, "We can't solve it all at once, but how can we start bringing pieces together?" I'm sure we're not the only ones, but we're feverishly working on things in our R&D area to create platforms that allow different functions and software tools to interact in a very agnostic way, meaning it wouldn't matter what company you chose.

**Johnson:** Where do you see Altium's vision going for how to retool all of this? Were you alluding to Altium 365 as a starting point?

**Arcuri:** I was trying not to say that, so thank you for prying that out of me. Again, being a guy who was in the trenches at the last two companies I worked at, it didn't matter what went wrong; I was blamed because I was at the bottom of the hill—the manufacturers. I'm a big believer in not letting the marketing get too far ahead of the reality. You could look at some things that Altium has today that are public information and guess what we might do with that if we thought this problem we've been talking about was a big problem. We thought that there was a great business opportunity in helping to solve it, and we are.

For example, Octopart has a huge user following, and it's absolutely not centric to Altium. Components are one of the major irritants in our life because, from a manufacturing perspective, if I don't have them, I can't put them on the board. From a customer perspective, if I go to order them and can't get them because Cisco just designed that tantalum capacitor into a product, the worldwide supply just went down to zero. Everything to do with components—physically, electrically, and related to the supply chain—causes us lots of excitement in this industry.

We have a thing called Ciiva, which is interesting and CAD-nostic. I would like to be cred-

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ited with that, by the way, unless it's already been collared by somebody else, but I'm going to call it CAD-nostic. A CAD-nostic view of manufacturing says, "Every manufacturer has certain constraints, requirements, and input data needs. If I can create something in front that gives them those things in a much more predictable way, then I will save them time and get the customer more predictable results across many manufacturers, whether that manufacturer is in New York, California, Texas, or Germany."

Altium 365 is a product we've talked about, and what's in the marketplace today is about 2% of what we envision that to be. If I look at our aspirational goals for the future, we believe that the underpinnings like Octopart and Ciiva, for instance, will be foundational pieces as well as cloud-based infrastructure. Something above that, like Altium 365, needs to truly use advanced software techniques and latest methodologies to bind all of that together. We are feverishly working on that across the globe.

**Shaughnessy:** We've had some people ask, "Why isn't there a universal input data for design rules?" We have universal output like ODB++, IPC-2581, or Gerber, but there's no universal input. It sounds like 365 is along those lines. Is that how you're looking at it?

**Arcuri:** Yes, one of the reasons that a universal input doesn't exist today is because it really is

hard. You don't have one component supplier to go to. There are hundreds of component suppliers who represent data sheets completely differently and have different equipment. How you program a JUKI machine to place parts on the board is different than how you program a Yamaha machine, etc. Within a factory, there are all kinds of different equipment, which creates various variables. Then, you have different technologies and customer demands, and they're using different CAD systems.

Some of them are experts with those CAD systems, and some of those have the iPhone approach, which is, "I opened an app and I'm now a board designer. It worked in the app. Why can't they build it?" You have to create something that people want to be part of and want to put their collective knowledge into as opposed to saying, "I've created this. Now, all of you must adopt it." That is our challenge and mission, but not only for Altium 365. In a perfect world, we would be overjoyed if a Mentor, Cadence, or Zuken user got the same benefit that an Altium user would get.

**Johnson:** How much traction do you find right now from other vendors in the marketplace to participate?

**Arcuri:** On the manufacturing side, I can't answer that question yet. Ask me in three months. On the component side, as you might expect, some are very cooperative. In other words, "This electronic data feeds of all our parametric data." Others say, "Here's a data sheet. If you want the data, scrape it off the data sheet." How would I answer that? I'm not sure I touch enough people to answer it broadly other than to say there are so many people involved. Some factories have the attitude of, "I don't want to tell you anything because if I do, that will make me the same as the next company." Other factories are very open.

I don't talk to CAD tool suppliers very often other than I have a fair amount of experience with Cadence. Again, I think the question

is premature, and I can answer it in about six months. Toward the end of this year, we're going to have some things realized that provide the opportunity for the collaboration. Then, we can say, "We've built the foundation. It's CAD-nostic and manufacturing agnostic. Is anybody going to join?"

**Johnson:** It will be interesting to see how the continued implementation of protocols like CFX and Hermes for Industry 4.0 smart factories may help turn the balance to a greater acceptance of data transferring collaboratively.

**Arcuri:** Definitely. That's another piece. I don't mean it to sound like I hate our industry, but it just hasn't evolved. It's stuck in a very siloed, monolithic paradigm and the world around us isn't. Taxi drivers resisted, and then Uber changed that landscape, like it or not. It's going to take constant pressure to change our industry because you can't change the personality of a person, a company, or an entire industry just through a speech. And in many cases, that pressure comes from the consumers of these products, components, manufacturing services, and equipment. Kicking and screaming, we are pushing the industry into submission, but I don't think it's going very willingly into the night yet.

Industry professionals understand that they have to slowly get onboard, which is a step in the right direction. The rate of change will continue to accelerate, and everybody says Industry 4.0 is needed, it's happening, and they're on board with it. But the day that I can make it possible to feed a file to something and drive a JUKI, Panasonic, Yamaha, Siemens, and a MY-DATA machine without someone having to sit there figuring out which rotation the diode has to be, I'll be a happy camper.

Another thing that drives people crazy is that Industry 4.0 is a nice phrase, but we're more like Industry 1.2. Three years ago, I was standing on my factory floor looking at $10 million worth of capital equipment, test machines, QA inspectors, and all kinds of great technicians, and once a month, we still put a diode on backward? How does that happen?

**Holden:** To bring us back to the original topic of design rules, what we're talking about is boundary conditions for many separate goals. In the electronics business, every PCB and product has something to try to differentiate it from the competitor's product. These goals to differentiate our products and support innovation drives us to a different set of design rules for every board and product.

Unfortunately, since electronics have no boundary in terms of where it's going, these goals and directions are constantly going to be manipulated, and as you said, all we can do is potentially have collaborative software or something similar. If the goal was boundary conditions of cost, supportability, distribution, or environmental, it would say, "Start with these design rules and see how far you can get with it before you have to start changing them because the design rules compete with each other."

Something has to win out. Like density, if you want to make lines smaller, that means materials have to be thinner. If you don't have the materials or if you can't stand the signal loss, then you have to use wide traces. That competes with my density and size goal. The biggest thing is that we don't have a tool that shows us or allows us to play with these trade-offs and "what ifs." Because of tight schedules, we just have to grab a number, guess, and go with it. Right or wrong, time doesn't allow us the luxury of doing it. Otherwise, you can do it over. You only have enough time to do it once and cross your fingers that we got close to the reliability, cost, or supportability goals that were set.

**Arcuri:** I envision a world where you can see real-time effects as you're doing something and your changes are captured so that you can understand the various impacts.

**Shaughnessy:** We appreciate your time, Craig.

**Arcuri:** It's my pleasure. Thank you. **DESIGN007**

# Mentor's EDA Perspective on Managing Design Rules

**Feature Interview by Andy Shaughnessy**
I-CONNECT007

I recently spoke with Dave Wiens, product manager, and Mike Santarini, EDA content director of corporate marketing, both of Mentor, a Siemens business, about design rules and constraints, and what their customers want regarding design rules. They explained how EDA companies like Mentor help designers constrain for performance while avoiding overconstraining and increasing the cost of the board and also being manufacturing-aware.

**Andy Shaughnessy:** Can you start by telling us about what your customers want in their design rules capabilities. What do you try to provide them as far as design rules?

**Dave Wiens:** Customers have to take all of the design constraints and manage what might be conflicts between those and determine what the tradeoffs are to optimize the product. From a tool perspective, we try to enable whoever is defining those constraints to do it as easily as possible within a common environment, and then pass those on to whoever is going to utilize them. Often, it's the layout designer that has to implement the constraints.

They're dealing with the physical embodiment of the product, but there are constraints on the schematic stage as well. We help them automate the definition of those constraints, simplify the entry, but it's not enough to define constraints. You also have to validate those constraints.

You must try to simplify the way it's done so that somebody can look at a design and say that it passed. It's about simplifying constraint definition as well as adherence to the constraints and verification. So, how does the designer do the design and try to adhere to constraints? Ensure that the full design verification and constraints were met and that the product is going to work. Again, the problem is constraints are coming from multiple people, for instance different requirements on performance might being at odds with each other.

**Shaughnessy:** One of the designers I talked to said that the problem is that no one person can remember all of these things simultaneously.

**Wiens:** Right. And in the old "Wild West" of design, there wasn't a constraint editor. Then, you got constraints and had an engineer talking over your shoulder, saying, "When you route these two traces, keep them this far apart." It was all digitized, and you had to use old-fashioned ways to determine whether they were far enough apart. There was no such thing as a digital constraint or something to adhere to.

Dave Wiens

The idea of becoming aware of all of them is a big thing, so from an EDA perspective, we try to automate these things. We help gather all of those constraints in one place. There are still things that can be done to improve on that. It's about having a streamlined way so that you can pass constraints from whoever defined them. If it came from the engineer at the front or the manufacturing NPI engineer at the back, the process helps define those and pass them to the person who has to implement them.

**Shaughnessy:** Many designers say they don't even know who is going to be fabricating their board or prototype, much less production. How do you figure all of that in the design rules? Do you have to re-enter it each time?

**Wiens:** In most tools you do. Not just every job, but you want to be able to design for multiple manufacturers, for instance. And you definitely want to be able to retarget, and that's one of the things that we've been able to do thanks to our Valor technology. The majority of manufacturers out there, around 80%, use Valor for their verification tool. If they're using Valor, they can pass the designer those rule decks. Then, the designer can retarget without having to reenter a bunch of constraints. They can say, "I want to go after this manufacturer instead of this one," and do it with a rule deck that the majority of manufacturers use.

To bring up a common theme, last fall, we talked to you regarding the "shift left," bringing verification earlier into the design process.

That plays into this as well. Again, it's about constraint definition, adherence, and verification, trying to bring the full board verification early on in the process so that it's not just used as a sign off tool at the end. Instead, it should be used throughout to help ensure that the designer becomes smarter and more aware of engineering and manufacturing and produces a product that can meet the constraints.

For instance, in manufacturing, there are tolerances. If you do this, it will work, but if you do this, it will be lower cost and still work. So, what are the absolute rules, and what are the gray-area rules? You have to deal with some level of tolerance; over-constraining a design is easy, and to some degree, lazy. If you talk to your average layout designers, they'll go off on this. They'll say that the engineer gave them a constraint, and there's no way to meet it. Defining hardline constraints is easy but defining constraints that work with other constraints and the tradeoffs that can be implemented within tolerances is a lot harder.

**Shaughnessy:** Meanwhile, you're pushing the envelope with the technology, and I'm sure that makes it more difficult with each revision of the tool that comes out.

**Wiens:** With increasing design complexity comes additional constraints. And there are all kinds of constraints that have to be thought of to fire a 28-Gb signal across a board. We have to continually increase the constraints that somebody can set for that; at the same time, we need to try to make it as simple as possible to do that. Defining constraints can be somewhat onerous. Great, you have an environment to define those constraints, but do I have to be a Ph.D. to do it?

**Shaughnessy:** Theoretically, there's almost no limit to the number of design rules you can have for a design.

**Wiens:** Right. Your average board has tens of thousands of connections and nets. You could constrain each one of them independently if you wanted to, but that's where reality has to

come into play. If you define rules for every single signal, you're going to spend your life defining the constraints. Again, that brings in the hierarchy, and ways to define rules ripple down to define a high-level constraint that's applied to a whole bunch of nets. If you need to tweak individual nets within a bunch of one hundred, for instance, you can do that. But you don't want to have to individually define the constraint for every one of them, and then find out that you messed something up and have to go back to all of them.

**Shaughnessy:** So many of these things are on the edge. Some fabricators say that they receive boards that are listed as Class 2, but they push it so much that they call it Class 2.5.

**Wiens:** Yes. How can we do it cost-effectively is the other side? And from a performance perspective, you can over-constrain a design. You can say, "I need an extra 10 layers to shield all of the signals," but that's not cost-effective, and the only way to determine the appropriate constraints is to run an analysis up front. How loose can you make the constraints so that you can still achieve the performance you're looking for at the cost target?

**Shaughnessy:** That's what your co-worker Todd Westerhoff once said: "What's the dirtiest I can make my signal and have it still work (laughs)?"

**Wiens:** Exactly. In this case, being a purist is easy. I want my digital signal to look like digital signals. You have to have some degree of attenuation or noisiness on the signal; that's going to happen.

**Shaughnessy:** From what I've seen with the IC world, it seems like they solved the design rule problem 20 years ago in their segment. I guess it was out of necessity because if you have a re-spin of a chip, that costs hundreds of thousands of dollars. Plus, there were only a handful of foundries compared to the number of PCB fabricators, so it would be simpler to set up manufacturing rules, right?

**Wiens:** I'm not an IC expert by any means, and I'll let Mike speak to that, but I can tell you a few things that they've hit. Number one, the IC vendors hammered home the golden verifier approach. They said, "We're not going to even accept a design from you unless we know that you adhere to these rules. There's no point because of the cost associated with it." And that concept that everybody has to validate something using one tool drove those rules into the design process. You had to use those rules.

Another thing they did was go to a block-based design approach that said there are reusable blocks of IP from one design to the next. First, it gives you immediate quality. You designed and verified that IP once, so it's a known good IP. Second, it accelerates the design process because you're reusing stuff—not just redoing stuff. Now, the idea of buying IP from somebody else and reusing it hasn't caught on with the PCB side, but it has with the IC side. Synopsys has made good money off of that. Do you have anything to add from an IC perspective, Mike?

**Mike Santarini:** Another thing in the IC space is that fewer companies are manufacturing the chips now. Silicon foundries have more control of their particular processes because they make their money by producing massive amounts of silicon and

Mike Santarini

getting a good yield. The goal is to get it right the first time. At some point, they tell customers, "This is what the process is. You must use this vendor's specific tool to ensure that what you've designed conforms to what will be manufactured." The other thing is all of the equipment; they standardize on the kind of equipment they're going to use at each process node. What does it look like in the PCB space, Dave? Are there still a lot of people mixing and matching what equipment they use?

**Wiens:** Absolutely. There are many more manufacturers and a lot of variability in equip-

ment. They're driving all the way down to the lot size of one—a customizable manufacturing process that can cost-effectively produce one board. Again, a lot of that has to be optimized like IC, but the cost associated with failure and implementation is lower.

**Shaughnessy:** One of the overarching themes here seems to be the management of all these rules. You may have rules for signal integrity, power integrity, and the fabricator's etch-back rules, etc., but how does anyone manage all of this?

**Wiens:** It requires cross-domain awareness. The engineer defining the rules for signal integrity has to be aware of the manufacturing process that's going to be used. Are they going to be doing microvias or back drills on through-hole vias? They could define a constraint that says every via has to be back drilled because everybody knows that unused vias are noisy, so back-drill every via. There's a cost associated

with that, and is that necessary? Also, if you're drilling vias, the deeper the via, the more the bit is going to wobble. That's a tolerance issue.

**Shaughnessy:** A fabricator might say, "Here's how we do stackups," and the EDA company has to turn that into a constraint.

**Wiens:** Stackups are another item that can be defined in a variety of tools from the manufacturing side. Of course, they can put them in Valor. That's a direct transfer back to the designer. They might send them to us in other formats or tools, so we've had to add capabilities to import that into our constraint environment to avoid having to re-enter rules like that. The stackup that you're using absolutely impacts the performance; it changes every single performance constraint. That's where reuse comes in, knowing what their most cost-effective stackups look like and picking from those when you define your constraints up front for performance.



The Mentor Xpedition constraint editor.

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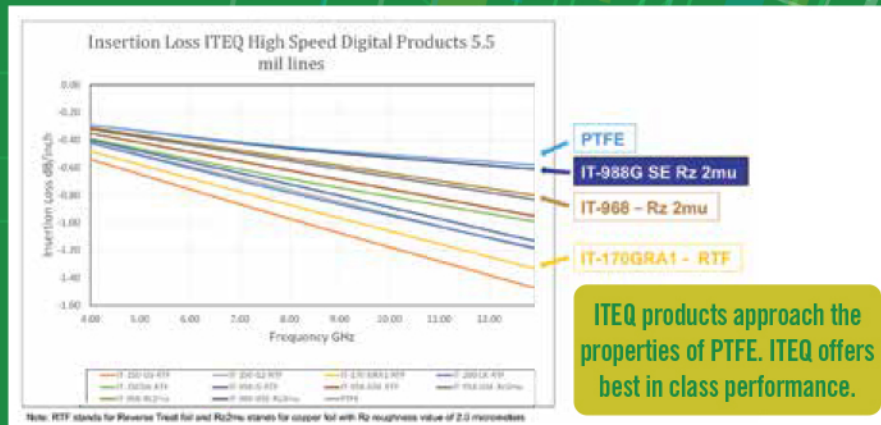
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- Very Stable Dk-Df across frequency
- HDPUG MRT-6 - LRC and HRC passed all thermal requirements
- HDPUG MRT-6 - LRC and HRC passed CAF requirements
- Proven thermal stability beyond 7 lamination cycles and suitable for HDI applications

## Sequential Lamination

### 7 Lamination cycle data

| Lamination | DMA | DSC | TMA | T300 with CU | Solder Dip PCT: 1h @ 121℃ | Td 2wt% / 5wt% |
|---|---|---|---|---|---|---|
| 1 | 213 | 187 / 187 | 182 | > 60 | > 60 | 408 / 435 |
| 2 | 216 | 194 / 199 | 193 | > 60 | > 60 | 41 7/ 438 |
| 3 | 214 | 186 / 192 | 185 | > 60 | > 60 | 417 / 442 |
| 4 | 216 | 193 / 194 | 184 | > 60 | > 60 | 424 / 443 |
| 5 | 217 | 194 / 199 | 190 | > 60 | > 60 | 418 / 442 |
| 6 | 218 | 191 / 197 | 188 | > 60 | > 60 | 405 / 436 |
| 7 | 218 | 190 / 197 | 194 | > 60 | > 60 | 425 / 444 |

No thermal degradation observable after 7 lamination cycles

## HDPUG MRT-6 LRC CAF Data



IT 988 SE LRC 16 Mil "Reflow"
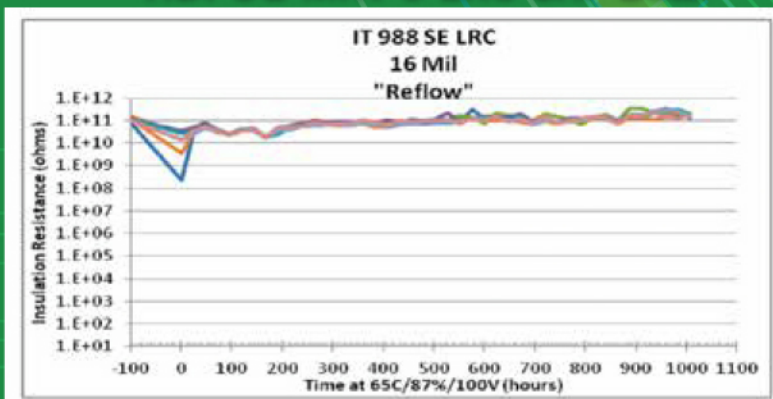
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**Shaughnessy:** If you're a designer and use design rules all the time, do you have to go back to validate them after each couple of projects?

**Wiens:** Yes. What was that rule based on? Was it based on a manufacturing process? Does that manufacturing process still exist? Is it still the same cost? Are there alternatives? Was it based on a certain performance in terms of the data rate, DDR4 versus DDR5? What was that based on? So, yes, that comes into play when you think about whether or not you can reuse it. Again, it's a moving target.

**Shaughnessy:** Is there anything that you would recommend to one of your designer users or anything that you wish that they would understand regarding setting up and using design rules?

**Wiens:** If they know what their tool is capable of, then they're more likely to leverage that, and be more productive. One of the problems with having a tool with a lot of horsepower like Xpedition is that customers don't always know what's under the covers, and constraint management is a big area of that.

**Shaughnessy:** The more I find out about design rules, the more I'm surprised that we get it right so often. There are so many potential screw-ups.

**Wiens:** There's a margin for error, and that's a good thing. Unfortunately, that margin usually comes at a cost. Everybody thinks, "At the end of the day, I'll manufacture it, boot it up, and if it works, I'm successful." But they might have had to do it with a higher-cost manufacturing process, components, or complex stack-ups. What does success look like, and what's the best practice?

**Shaughnessy:** I know some designers over-constrain just to be thorough, and it costs more to manufacture.

**Wiens:** Exactly. If that is baked into the process, meaning everybody knows that it cost this much to manufacture the last one, and nobody raised an eyebrow when they did that, I'm going to do it again. Designers and engineers are incredibly smart people; it's not like they're incapable of multidomain awareness, but there are a lot of moving pieces. So, you try to control as many of them as possible to minimize the tradeoffs and options to be considered.

**Shaughnessy:** I appreciate you both taking the time out to talk with me.

**Wiens:** Thanks for the opportunity.

**Santarini:** It's always good talking with you.

Visit I-007eBooks.com to download *The Printed Circuit Designer's Guide to… Signal Integrity by Example* and *Power Integrity by Example* written by Fadi Deek from Mentor, a Siemens Business, as well as other free, educational titles. **DESIGN007**

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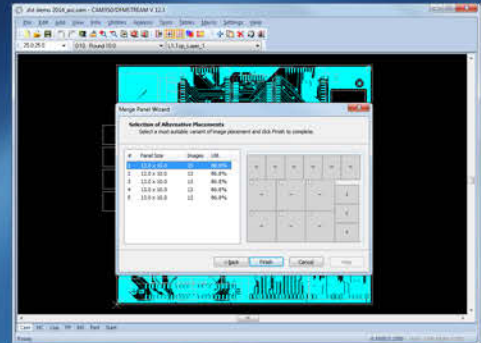
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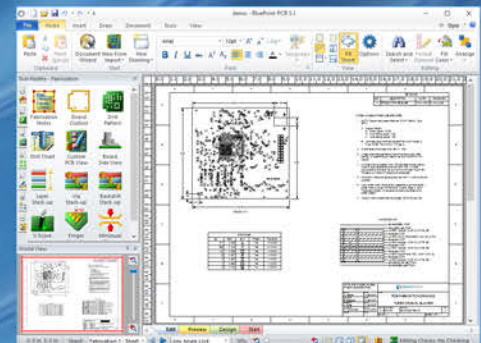
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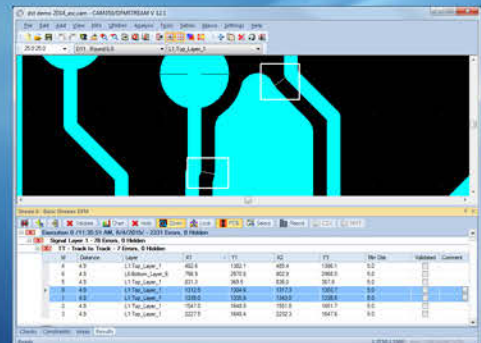
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# Rules Keep You From <span style="color:red">Crossing</span> the Line

## Tim's Takeaways
### Feature Column by Tim Haag, CONSULTANT

I have the privilege of living in a neighborhood along with a lot of other families. In the winter, we enjoy indoor holiday celebrations, and during the warmer months, we enjoy outdoor potluck dinners. We help each other out with various chores, and routinely celebrate our triumphs and victories together. No, this isn't the fictional TV town of Mayberry, but at times, it almost seems like it. And one of the greatest joys of living here is all of the children. These little ones laugh and play and want to tell me all about their day at school. While waiting for their parents to finish barbequing the hot dogs, they ride their bikes, trikes, and scooters all over our cul-de-sac. It really is perfect.

In 10 years though, this story will be a little different. All of these little ones will have grown into teenagers, and they're going to exchange their bikes, trikes, and scooters for cars, trucks, and motorcycles. You can bet that these same parents who take delight in sneaking their kids an extra cookie during the potluck dinner will be creating detailed lists of rules and constraints to keep their teen drivers safe. These rules won't be limited to just attending driver's education and successfully passing their driving test though. I'm sure that school grades will also have to be maintained, curfews will be in effect, and of course, their driving skills will be monitored. There will be a zero-tolerance policy regarding unsafe driving practices or breaking the rules of the road.

## Driving Rules

Strict regulations like these demonstrate how much parents truly love and care for their kids by trying to keep them safe, even if the kids don't really believe it themselves. Driving rules are designed to keep drivers between the lines of traffic instead of crossing over those lines into dangerous situations. Similarly, design rules are also intended to keep PCB trace

routing between the lines instead of crossing over them as well. But you might be surprised how many people refuse to use the full potential of their DRCs to protect themselves, and in some cases, refuse to use them at all.

When online design rule checking first appeared in PCB design tools many, many years ago, there were a lot of problems associated with them. At first, they only had a few (if that many) clearance settings, and those didn't always work as they should. I remember being warned of clearance errors on some tools that actually weren't errors at all; the tools just weren't reporting them correctly. This would happen more often if you were using oddly angled traces on too fine of a grid. It was not unexpected then that PCB designers back then were sometimes leery of using or relying on DRCs.

> ## When online design rule checking first appeared in PCB design tools many, many years ago, there were a lot of problems associated with them.

Another problem during that time was PCB design was largely converting over from hand-taped designs to computer-aided design tools. If you aren't familiar with the process of hand-taping a design, PCBs were laid out at two, four, or even 10 times the actual size working on a transparent grid over a light table. The designer would apply opaque tape and dots to create the traces and vias of the layout using the grid for a reference. The grid, plus the designer's experience, was the only clearance checking available, and designers would maintain the correct trace to via spacing by eyeballing it. If something was too close together, an X-Acto knife would be used to trim the tape or dot down a bit.

For PCB designers that were artists with tape and dots, the transition to CAD was sometimes difficult. To gain freedom with their work

the way that they were used to, they would often disable the grids and online DRCs. Although this would give them a design environment that they were more comfortable with, it would make a mess of the job because of all the DRC errors. I used to spend days repairing designs like these because I would first have to move all of the existing routing onto a grid to clean up the DRC errors. Once everything was back on a grid, it was a lot easier to edit the placement and routing for modifications. However, many of these designs took a lot more effort than I expected because when I did bump every trace and via to get the correct spacing, there was no longer enough room for all of the traces. Those were the times my mood would get really bad for a while.

So, yes; it was understandable why design rules were ignored in the past, but that still didn't make it right. I know first-hand the cost of not using the available DRCs because of all the heroics that I had to go through to fix them. If turning off the DRCs wasn't the right thing to do back then, it certainly isn't these days either.

Last fall, while driving I-5 from California to Oregon, I had the misfortune of getting caught up in the forest fire that ravaged the beautiful scenery of the Mount Shasta area (Figure 1). Shortly before I arrived there, the safety officials decided to close the freeway at a specific point due to concern that the fire was about to jump the road. If I had been just 10 minutes earlier, I probably would have beat the road closure, but as it was, I had to retrace my route and take the long way around Mt. Shasta to the east.

I don't want to bore you with the details, but let's just say that four extra hours of slow, bumper-to-bumper traffic on winding backroads without adequate rest areas was not fun. But my point is that someone made the right call when the fire exceeded specific safety rules that were created for the protection of the public. Although my extended detour wasn't fun, I was very happy with the safety those rules afforded.

## PCB Design Rules

Just as traffic rules are intended to keep us safe and out of trouble on the road, PCB design rules are also intended to keep our designs

Figure 1: Driver's view of the Mt. Shasta forest fire in the fall of 2018.

safely out of trouble. Yet, even today, some designers won't use their design rules and constraints to their fullest extent. I wonder if some designers don't want to take the time to fill out all of those annoying DRC details. It is true that you can jump right in and start routing traces that way, but at what cost? Having to re-spin a design because of manufacturing errors that could have been avoided by using your design rules can be an expensive mistake.

Maybe some designers don't understand how incredibly helpful these rules can be. I think that most everyone would agree that setting up the basic trace width and clearance rules can make our job as PCB designers much easier. But with all of the DRC capabilities that are in most PCB design systems, you can set up all kinds of rules and constraints for many different objects beside standard trace and space rules. There are rules for text, holes, and different kinds of inclusion or keepout zones. You can also set up specialized constraints for microvias, power plane connections, and component heights. Then, there are whole realms of advanced rules and constraints, including high-speed design rules, manufacturing rules, and much, much more.

Setting up the rules will take some time; that is true. Fortunately, many PCB design systems feature helpful tools, such as spreadsheet style design rules and constraints menus that allow you to import and export your rules from either the schematic or the layout with ease.

Many design departments store their design rules like library parts so that their designers can quickly import a basic set of rules that have been saved for specific design technology. Once in place, those basic rules can then be modified and enhanced for the particular design, and then saved out again for the next person to use. Pay it forward. Anything that we can do to help reduce design time is well worth it.

## Conclusion

The bottom line is this; just as traffic rules are in place to protect us, so are PCB design rules. For those who ignore any of these rules, there could be some expensive consequences waiting for them at the end of the road. On the flip side, there are enormous benefits when working within rules and constraints. Teenage drivers will certainly enjoy the privileges of driving, I enjoyed avoiding the flames of the Mt. Shasta fire, and PCB designers will enjoy designing the latest technologies, knowing that the full range of their online DRCs will keep them from making time-consuming and costly mistakes. **DESIGN007**

**Tim Haag** is a PCB design consultant based in Portland, Oregon. To read past columns or contact Haag, click here.

# Board Negotiations: Design Rules and Tolerances

## The Bare (Board) Truth
### Feature Column by Mark Thompson, CID+, PROTOTRON CIRCUITS

In this column, I explore design rules and the constraints they put on the PCB fabricator. As you will see (and may have experienced), some work, but others do not.

## 1. Applications

Depending on the board application, you may need tighter tolerances. For example, with aerospace, automotive, and medical boards, the tolerances must be tighter. So, how do we get there?

## 2. Designing With Specific Tolerances

Here are several examples of how a PCB fabricator can deal with various tolerances. Let's look at "press fit" applications for tool sizes. Typically, a given plated hole or slot is ± 0.003″ and a typical non-plated hole or slot is ± 0.002″. So, what does the fabricator do when a plated hole is called out as ± 0.002″?

The simple answer is to calculate how much plating there will be in the hole barrel, and then over-drill to accommodate the ± 0.002 tolerance. Typically, this is done by labeling the ± 0.002″ hole as *plus 0.004″ minus zero* in the CAM system. End-users on RF applications, such as antennas and phased arrays, have precalculated the copper in the hole barrel for many years. Often, end users will stipulate the drilled hole size (not the finished hole size as most designers call out) here so that they can pre-calculate how much plating will be in the hole barrel based on the PCB fabricators capabilities.

## 3. Don't Be a Violator

For instance, we may receive an IPC callout for a 0.002″ annular ring minimum. But what happens when the end user does not allow for that, creating gap violations? Or worse, what if they don't understand that a PCB fabricator drills approximately 0.004–0.005″ over the finished hole size as expressed on the drill drawing to meet the nominal hole size? Making the pads on a signal layer or the anti-pads (relief pads) 0.004″ over the finished hole size without accounting for the additional plating to meet the IPC minimum of 0.002″ per side annular ring does *not* work.

In a perfect world, the machine tolerances and true position are both ± 0.000″, but that is just not the case in practice. It used to be said that if you added up all the tolerances needed to manufacture a given board, nothing would be possible. As an example, let's add a ± 0.003″ true position tolerance to a ± 0.003″ machine

**APPLICATIONS**

**TOLERANCES**

**NO VIOLATIONS**

**LINE EDGES**

**UNIFORM PLATING**

**NEGOTIATIONS**

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tolerance. This would mean that +0.006″/- 0.000″ could occur at some point. I can assure you this would not work for a ±0.002″ annular ring if the signal pads were only increased by 0.004″ to meet an IPC ±0.002″ minimum annular ring, and the over-drill for plating was not considered.

What about plating tolerances and fabrication route dimensional tolerances, layer-to-layer registration tolerances during lamination, or signal integrity tolerances? Again, If we add up all of the accumulative tolerances to build a board, the boards might *never* get built. So, what is the good news?

Some tolerances negate one another, so use true position versus machine tolerance. If *both* were stated to be ±0.003″, we move the furthest plus extent on the true position, but we go the other direction on machine tolerance at the minus extent of ±0.003″, the two will balance each other out. Add tolerances of ±0.002″ layer-to-layer misregistration potential, for instance.

So, how does the fabricator mitigate the known expansion and contraction based on thin materials? Again, the good news is that most fabricators use a post-etch punch technology. This is where the inner layer cores do not get punched before imaging in a dry-film department. What does this gain us? When the layers are etched and stripped in plating, we have already gone through some of the aqueous processes that contribute to the expansion and contraction of the core materials, and they get punched after those aqueous processes.

In conjunction with that, a scale factor based on the known expansion or contraction of the thickness of the core and material type being used is associated at the CAM department, further mitigating the movement and keeping them within tolerance.

## 4. Line Edge Acuity

In addition, most fabricators utilize a direct image device that helps with line edge acuity. Back in the day, a silver film was produced and plotted with the opposite emulsion. Then, a Diazo film was produced to be used in manufacturing, and all of these copies produced a poorer and poorer line edge quality. Add to that the fact that the old raster plotters had lines of rasterization or a stair-stepped look that also produced poor quality line edges. Today's plotters do not do this, and the use of a direct image device where the sensitized core is directly imaged with light produces fewer line edge issues and better positional accuracy. Typically, these direct image devices even have their own de-ionizing and scavenging systems fully enclosed in the machine, so class 1,000, 10,000, or 100,000 cleanrooms are not needed anymore to reduce the amount of particulate in a given dry-film department.

## 5. Plating Processes

Plating processes have also come a long way from balancing the front to the back of a given panel to achieve the same copper area to allow for more uniform plating. Today, most shops have dual rectification on their plating tanks to allow dialing in the plating distribution. Again, years ago, if you hit a given panel with too much current, you could conceivably plate more in the hole barrels than on the surface, making "hourglasses" of the holes to check that the current was proper. Now, not only are the plating tanks dual rectified (allowing for better plate distribution) but the panels are also periodically pulled from the tanks and checked with a pin gage to ensure the proper plating on the surface and in the barrel of the holes.

## 6. Negotiations

If the tolerance is too tight, often, negotiation is needed. One such negotiation might be warranted for vias. For example, if the via tolerance is called out as ±.003″ for plated vias, and we run into space violations at etch or drill compensation, what can be done? In this case, we ask to change the vias from ±0.003″ to +0.003″ minus the entire hole size. This allows the fabricator to drill the vias smaller, allowing for both annular ring and space violations caused by attempting to increase the pad size to keep the vias at ±0.003″. In most cases, this is acceptable to the end user, as they are true vias and only really require electrical continuity.

Another example of a negotiation would be maintaining controlled impedances since there are hundreds of different materials and all of them have slightly different Dk and Df values. If a given customer just calls out FR-4, the shop will invariably choose their most commonly used "flavor" of FR-4 materials. Sometimes, that can result in small tweaks of the trace width or spaces to achieve the controlled impedance. Again, the good news is that typically, a drawing will specify that up to 20% of trace width or space is acceptable to achieve impedances; anything more than 20% will require buy-in from the customer. Thus, there are many ways to skin a cat to be able to produce a given PCB.

As always, thank you for your time. If you have any questions about this column, please feel free to email me at markt@prototron.com. **DESIGN007**

**Mark Thompson** is in engineering support at Prototron Circuits. To read past columns or contact Thompson, click here. Thompson is also the author of *The Printed Circuit Designer's Guide to… Producing the Perfect Data Package.* Visit I-007eBooks.com to download this book and other free, educational titles.

# Quantum Sensors Improve Sensitivity of Magnetic Resonance

The Quantum Technologies for Information Science (QUTIS) group of the UPV/EHU (University of the Basque Country) has participated in an international investigation together with the CSIC and the University of Ulm (Germany) that has given rise to a series of protocols for quantum sensors that would allow obtaining magnetic resonance imaging of biomolecules using a minimum amount of radiation.

Nuclear magnetic resonance (NMR) is a technique behind many applications such as medical imaging, neuro-



science, or the detection of drugs and explosives. With the help of quantum sensors, nuclear magnetic resonance has been adapted to work in the nanoscale regime, which has given it the potential to have an impact on various disciplines including life sciences, biology, or medicine, and provides measurements of incomparable precision and sensitivity.

"We hope that the combination of quantum sensors and dynamic decoupling techniques will allow us to obtain nuclear magnetic resonance imaging of individual biomolecules," commented the authors, including Dr. Jorge Casanova and Dr. Enrique Solano, both Ikerbasque researchers.

Their protocol is robust and requires less energy than conventional techniques. This not only extends the operating regime of the sensor to stronger magnetic fields but also avoids the heating of the biological samples that would occur when using other protocols with high radiation intensity. As a result, this work opens a new line of research and paves the way for the safe use of nuclear magnetic resonance at the nanoscale.

(Source: UPV/EHU)
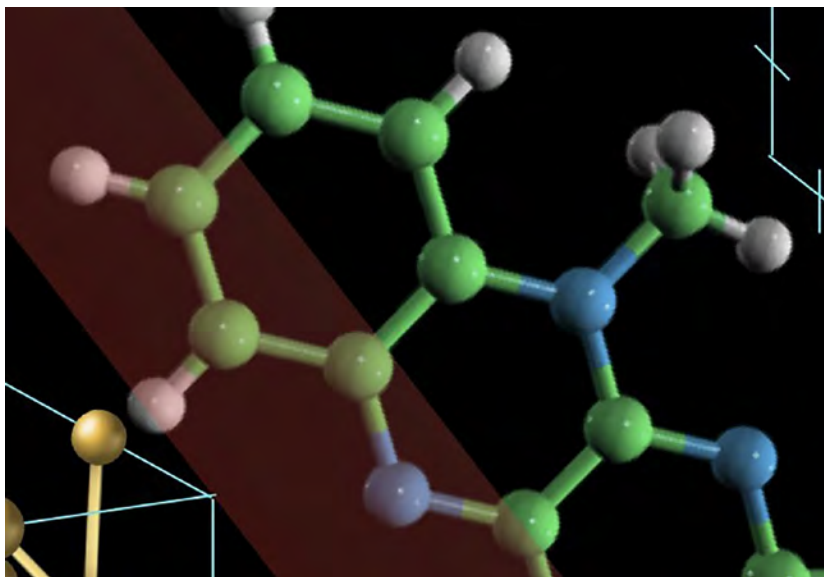
# PCB007 Highlights

## Creating Smart Surfaces with Electronic Functionality ▶

Of all of the technical user presentations I attended at the AltiumLive design summit in Munich, the one I found most fascinating introduced an innovative technology that encouraged a bit of lateral thinking and appealed to my creative side.

## ITEQ's Tarun Amla Discusses 5G Inflection Points ▶

ITEQ Corporation Executive VP and CTO Tarun Amla discusses effects of 5G on materials and shares general observations on the 5G rollout at DesignCon. He also talks about the challenges for their customers, and how they help them address their issues.

## Punching Out! Getting to a Signed Letter of Intent ▶

The letter of intent (LOI) serves as a roadmap for the buyer's attorney to begin drafting the purchase agreement, so it is important that there are enough details in the agreement. Any major terms that are important to the parties should be included. Here's a list of the very important items in the LOI.

## MacDermid Alpha Opens Tech and Applications Center in Taiwan ▶

MacDermid Alpha Electronics Solutions officially opened a Global Development Application Center on March 19, 2019. The advanced technology and application center will house sales, technical service, customer service, and office personnel alongside the laboratory staff.

## Reliable 3D Flex ▶

We all have a tendency to stick close to the familiar and use the tools we know to create solutions to problems confronting us; we're only human. Unfortunately, using only familiar tools limits our ability to come up with optimal or even superior solutions. This article will help you avoid some of the traps conventional wisdom doesn't always give guidance on.

## Standard of Excellence: Buy Based on Value, Not Price ▶

There are only two ways to buy PCBs; the first is based on price, which is the wrong way because it encourages a very shallow relationship based on just one thing—the price of the boards; and the second, and right, is based on value. A great company should understand what it means to buy value.

## Ventec Focuses on High-mix Manufacturing ▶

The I-Connect007 team recently toured Ventec International Group's Suzhou factory where a modern, flexible manufacturing concept designed for fast delivery is enhancing their established volume manufacturing of specialty, high-reliability epoxy laminates and prepregs. Read on to know more about Ventec's ongoing investment in the facility to offer flexible world-class high-mix manufacturing capabilities for polyimide, thermal management, low-loss, and signal integrity material solutions.

## The PCB Norsemen: A PCB Broker's Guide Through the Galaxy of Automation ▶

A smart factory is defined by its ability to harness manufacturing data flowing throughout the enterprise and then convert that data into intelligent information that can be used to create improvements in productivity, efficiency, savings, yields, automation, enabled traceability, compliance, and reduced risk of errors and rework. All crucial factors when manufacturing printed circuits.

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# Spotlight on the Orange County Chapter

## The Digital Layout
### by Stephen Chavez, CIT, CID/CID+, IPC DESIGNERS COUNCIL

This month's column highlights the Orange County Chapter, which is the largest IPC Designers Council (DC) chapter and one of the most active and thriving. Scott McCurdy, Orange County Chapter president, describes the successful format the chapter follows to reach local designers and PCB professionals. You'll also find an update from the IPC DC Executive Board as their collaboration with the new IPC Education Foundation continues.

## Chapter Spotlight
### by Scott McCurdy
ORANGE COUNTY CHAPTER PRESIDENT

The IPC Designers Council is alive and well in Southern California. The Orange County Chapter has been active since long before I took over as president in 2003 nearly 16 years ago. We are proudly the largest active chapter in existence based on the attendance at our quarterly meetings. We average 50–65 attendees at our meetings, and occasionally have 80+ people in attendance.

So, what's so special about the Orange County Chapter? For starters, we're fortunate that a large number of electronics companies are located in Southern California, so there are many PCB designers in our area who are thirsty for knowledge. We are also lucky to have many local PCB fabrication and assembly companies from which we draw attendees and speakers. All of the major CAE vendors have offices and technical field personnel here and have been very supportive of our chapter in hosting lunches to help us keep our costs down.

Another factor in our success is our timing. We hold "lunch 'n learn" events (Figure 1). It's much easier to draw a crowd for a long educational lunch when the traffic is lighter rather than holding meetings after working hours when rush hour is a nightmare. It can also be easier to tell your boss you're taking a long



Figure 1: Orange County Chapter "lunch 'n learn" event.

lunch to attend an educational event than to tell your family that you won't be home for dinner.

But the key reason that our chapter thrives is that we cover interesting topics with engaging speakers who share their knowledge and consistently delight our audience. Some of our biggest crowds were a result of the following topics:

- Flex and rigid-flex overview and design considerations
- PCB cost adders
- PCB routing guidelines for signal integrity and power integrity
- PCB-enabling technologies
- Embedded passives
- PCB design optimization starts in the CAD library
- HDI technology

Our meeting agenda has other elements too. I usually speak for about 10 minutes about upcoming PCB-related events, such as trade shows and conferences, as well as upcoming IPC designer certification workshops (Figure 2). I also let members know about the various publications, newsletters, and podcasts geared to the PCB design professional. And I always ask the audience if anyone is looking for a new job or if anyone's company is looking for designers. You can't beat the networking that is a byproduct of bringing together a room full of designers. Then, I introduce our featured speaker(s), and the learning begins. And to make things fun, we always have a raffle drawing at the end of a meeting with a couple of hundred dollars in prizes graciously donated by our speakers, sponsors, and others.

I won't say that's it's easy to put these events together, but since I've been president, we've done 64 events. But believe me, it's not all me. Our other officers, including Terri Kleekamp of Mentor, a Siemens Business, and Kathy Palumbo of Production Analysis and Learning Services have been active in our chapter longer than I have. We're also blessed with other faithful volunteers, such as Judy Warner of Altium, Marty Grasso of Advanced Circuits, and a few others who show up early and give us a hand setting up the room, greeting our attendees, giving them a name badge, hooking up computers and speakers to the projector, setting up the PA system, etc.

Lately, we've been putting my iPhone on a tripod to record the presentations. We always send out an email a few days after each event to provide links to download slideshow presentations from the speakers and to watch the presentations. Further, we print out a "cheat sheet" with all of the URL links so that our attendees don't have to take notes. We also have a "bingo card" to capture contact information to keep our database current and get audience suggestions for topics they'd like to hear about in the future.

In summary, we have a great bunch of designers and PCB professionals who come to our meetings. And I believe that this format



Figure 2: Scott McCurdy speaking at an Orange County Chapter event.

for learning more about the PCB interconnect industry from design through manufacturing is helping designers by igniting their passion for learning and expanding their knowledge and skills to keep current in this challenging, ever-changing profession.

**Scott McCurdy** is the director of sales and marketing at Freedom CAD Services Inc. Visit I-007eBooks.com to download *The Printed Circuit Designer's Guide to... Executing Complex PCBs* written by Scott Miller from Freedom CAD Services as well as other free, educational titles.

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## IPC DC Executive Board

The IPC DC Executive Board and the IPC Education Foundation met March 28 to continue to integrate and work toward common goals. Several topics were discussed, including:

- Local IPC DC chapter activities
- Updating the current IPC DC webpage
- Expanding IPC College Chapters and the Education Foundation's role in increasing the education sector of IPC
- The new online PCB design course class being offered by IPC

Stay tuned for more updates as we continue to collaborate for the betterment of our industry.

## 2019 Training and Certification Schedule

### IPC Certified Interconnect Designer (CID)
- May 21–24: Pittsburgh, PA
- June 18–21: Kirkland, WA
- August 6–9: Baltimore, MD
- August 26–29: Markham, ON
- September 6–9: Santa Clara, CA
- September 19–22: Schaumburg, IL
- October 21–24: Anaheim, CA
- November 2–5: Raleigh, NC
- November 5–8: Dallas, TX

### IPC Advanced Certified Interconnect Designer CID+
- September 6–9: Santa Clara, CA
- September 10–13: Kirkland, WA
- September 19–22: Schaumburg, IL
- October 21–24: Anaheim, CA
- November 2–5: Raleigh, NC
- December 3–6: Manchester, NH

*Note: Dates and locations are subject to change. Contact EPTAC Corporation to check current dates and availability. A minimum enrollment of seven students is required for a class to be held.*

## PCB Design Events

### Realize LIVE
- June 10–13, 2019: Detroit, MI

### PCB2Day
- Controlling noise, EMI, and signal integrity in high-speed circuits and PCBs
- June 13–14: Boston (Chelmsford), MA

### IPC SummerCom
- Standards development committee meetings featuring Panelpalooza
- June 15–20: Raleigh, NC

### PCB West 2019
- September 9–11: Santa Clara, CA

### AltiumLive 2019
- October 9–11: San Diego, CA

The IPC Designers Council is an international network of designers. Its mission is to promote printed circuit board design as a profession and to encourage, facilitate, and promote the exchange of information and integration of new design concepts through communications, seminars, workshops, and professional certification through a network of local chapters. **DESIGN007**

**Stephen Chavez** is a member of the IPC Designers Council Executive Board and chairman of the communications subcommittee. To read past columns or contact Chavez, click here.

# Accurate Gerber Files Are Mission Critical for Smooth PCB Manufacturing

### Connect the Dots
#### by Bob Tise, SUNSTONE CIRCUITS

Gerber files can reveal design issues ahead of the quote process and ensure your manufacturer has everything needed to produce your boards correctly. After consulting with Engineering Support Specialist Eric Haugen, we explored some best practices for making sure that Gerber files are accurate.

Speed is a critical component of the PCB manufacturing process. I spend the bulk of my day receiving files from customers and giving them backquotes in return. Rare is the day when a customer finishes off a quote request with, "Hey, take your time. I'm in no hurry."

Sunstone Circuits processes dozens of rush quote requests every day, and I can assure you that we do not like sending them back for more information from the client because crucial information is missing. And I'm pretty certain our customers don't like getting their quote requests sent back, or worse yet, producing boards that don't work because a key design element was not relayed to us.

Sometimes, this happens for an unavoidable or unforeseeable reason. Other times, it's purely a function of being in too much of a hurry to measure twice and cut once. We get it; it's hard to take your foot off the gas when your production lead or your boss is tapping their fingers on your desk.

An important thing to remember when you're deciding whether or not to hit the pause button is that your fabricator cannot read your mind (Figure 1). Before you hit send on a quote request, take five minutes and be sure you are sending something that's usable for your manufacturer.

Especially if you've been working on it for a long time, viewing your design in the native CAD tool can be overwhelming. You have been zoomed in, looking at tiny details for days or weeks. It seems so close to finished, but this is exactly when you should lean back and look at the big picture.

Converting to Gerber provides you with an uncluttered view of your board design. You can see each layer lined up. This can reveal all sorts of issues that will slow the quote process, such as one layer being scaled while others are not or one layer being metric and one not. Converting to Gerber also offers a double check that can pre-solve problems related to an esoteric



Figure 1: Your fabricator cannot read your mind.

naming convention, text on silkscreen layer showing up on the copper layer, tolerance issues with traces, and misaligned drill holes.

## Perform A Design Rule Check Before You Convert

You can prevent many issues by using the design rule check (DRC) tool in your CAD software. If you've properly configured the DRC tool, questions that often send a quote request back for more information can be answered. Are the layers all there? Are the spaces big enough? Do you have more drill files than copper layers? How are your tolerances?

These answers provide a good foundation for manufacturability, but you still have one very critical job with regard to the DRC. Ask yourself, "Can my fabricator make this design?" Remember, just because your software will let you design a board in a certain way, that doesn't mean we can build it. Think about manufacturability as you perform your DRC before converting to Gerber.

## Check Your Gerber Files

Once you've converted to Gerber format, you'll gain a more holistic, simplified view of what's really going on with your design (Figure 2). Here are some categorized items you can more easily check for and make changes where needed when viewing Gerber files.

### Minimum Feature Size

When you carefully scrutinize minimum features size and question what the DRC permits, you can:

- Find unintentional neckdowns
- Locate places where traces just barely touch pins
- Discover breaks in traces or where ends just barely touch
- See where pads are too small
- Eliminate small traces or features that can be a needless and major cost drivers
- Validate minimum drill size, more easily locating unnecessarily small drill holes that can also significantly drive up costs

### Feature Spacing

Solve clearance problems before they occur. Upon viewing the Gerber file, you'll have a sharper view of spacing types and be better able to recognize clearance problems for:

- Trace/trace
- Pad/pad
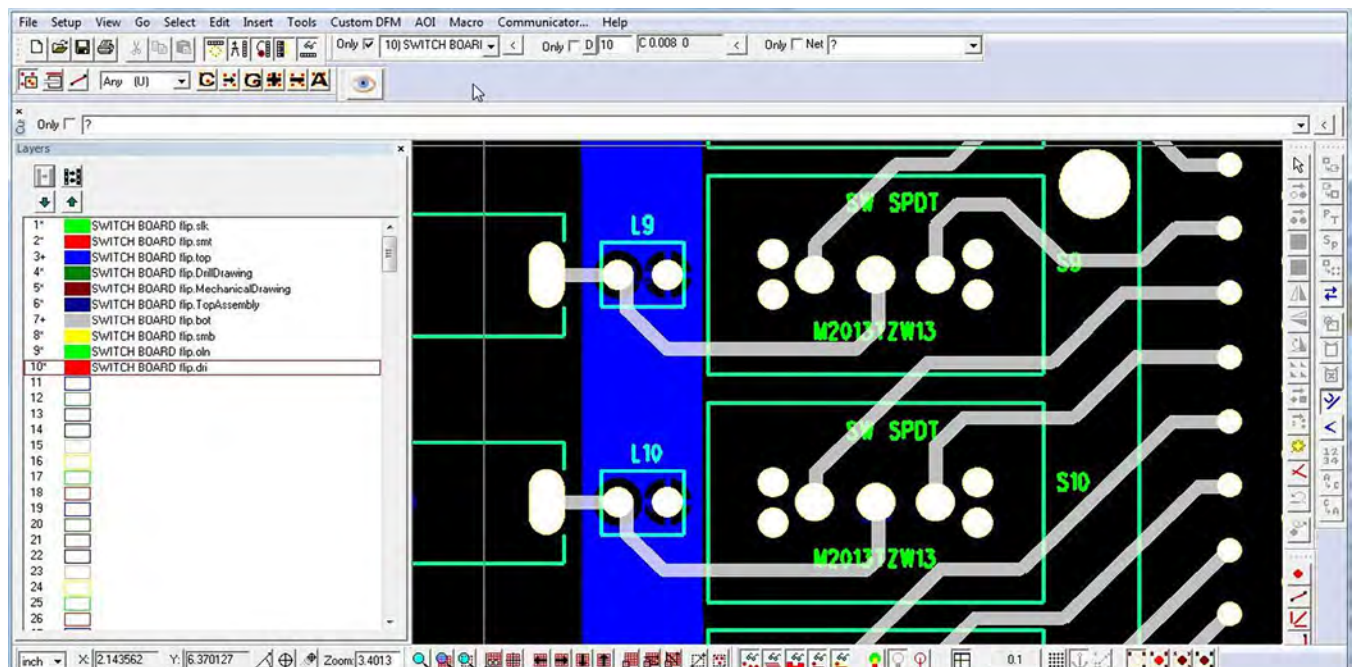


Figure 2: Many Gerber viewers are available online.

- Copper/copper
- Drill/drill
- Drill/copper
- Pad/pad

### Look at Each Layer

This is really the only way to visually confirm each is correct. And by doing so, you accelerate the quote process and avoid cost overruns during the production of the boards. Before submitting your quote request, consider:

- Does each layer import at the correct scale and size?
- Are the number of copper layers correct?
- Are the silkscreen and solder mask layer counts accurate?
- Did the drill file read as intended, as a single file or multiple files? If not, why?
- Was the drill file updated at the same time as Gerber files?
- Do drill holes line up with artwork?
- Were all area fills refreshed just prior to generating Gerber files?
- Did you intend to have potentially expensive blind vias or buried vias?
- Even one misstep in this category can create problems down the road. Though the list may seem long, the potential return on investment of a few minutes can be significant.

### Check Solder Mask Layers

When you are double-checking each board layer, pay careful attention to solder mask layers. Oversights here cannot only cause delays but result in boards that do not function properly or at all. Ask yourself:

- Do all pins have mask openings?
- Vias under components should not have mask openings. Do they?
- Are solder mask openings slightly larger—at least 0.004″—than component pads?
- Are plated through-hole pads 0.015″ larger than the drill, and therefore, large enough to avoid breakout?

### Leave Plenty of Breadcrumbs for Your Fabricator

As I said, we can't read your mind. Fabricator notes can make the difference between a quick turn and a protracted delay. If filenames are just a jumble of numbers or we have questions about what services you want us to perform, the notes are where we can go for guidance. Consider the following questions:

- Will the fabrication notes conflict with your order form?
- Do notes call for unnecessary services?
- Do you reference documents that we do not have access to?
- Does the design service you selected include a technician checking your notes?

Not all quick-turn prototyping services offer human intervention. So, if you're relying on a technician for review of your design files ahead of the quote and production process, be sure to choose a service level that includes it.

## Not all quick-turn prototyping services offer human intervention.

Finally, and this may seem obvious, make sure you are sending your fabricator the correct file. You would be surprised how often we receive the wrong files and discover it after production of the PCBs is complete.

So, please invest a few minutes in your design and check your Gerber files before you hit send. We want to help your rush job and keep your boss from tapping their fingers impatiently on your desk. **DESIGN007**

**Bob Tise** is an engineer at Sunstone Circuits. To read past columns or contact, click here.

# Thermal Management:
## Why It Should Be High on Your Circuit Protection Agenda

### Sensible Design
**by Jade Bridges,** ELECTROLUBE

In my previous column, I highlighted a few cautionary notes on the pain points associated with thermal management products, particularly the choices that you will be confronted with, such as which material or product type (i.e., pad or paste) is best suited to your application. In this column, I will underline the importance of getting it right, and touch on the consequences if you don't.

There are a variety of materials and methods to choose from, and they serve different purposes depending upon the physical constraints of the application, component layout and assembly geometry, the environment in which the assembly will be placed, the severity of duty, etc. Then, there are some more specific questions to ask, such as: what thermal conductivity do I require, or how much material will be needed in the interface between component and heat sink to achieve a thermally stable assembly?

Overlook the slightest detail, and you could compromise the performance of your electronic assembly. Clearly, poor thermal management practice will affect the efficiency of dissipating heat away from components and safely out of the assembly. As the temperature of a component increases and reaches its equilibrium temperature, the rate of heat loss per second will equate to the heat produced per second within the component. This temperature may be high enough to significantly shorten the life of the component or even cause the device to fail unless adequate thermal management measures are taken.

Of course, the same applies to a complete circuit or device, which has individual heat producing components within it. In this case,
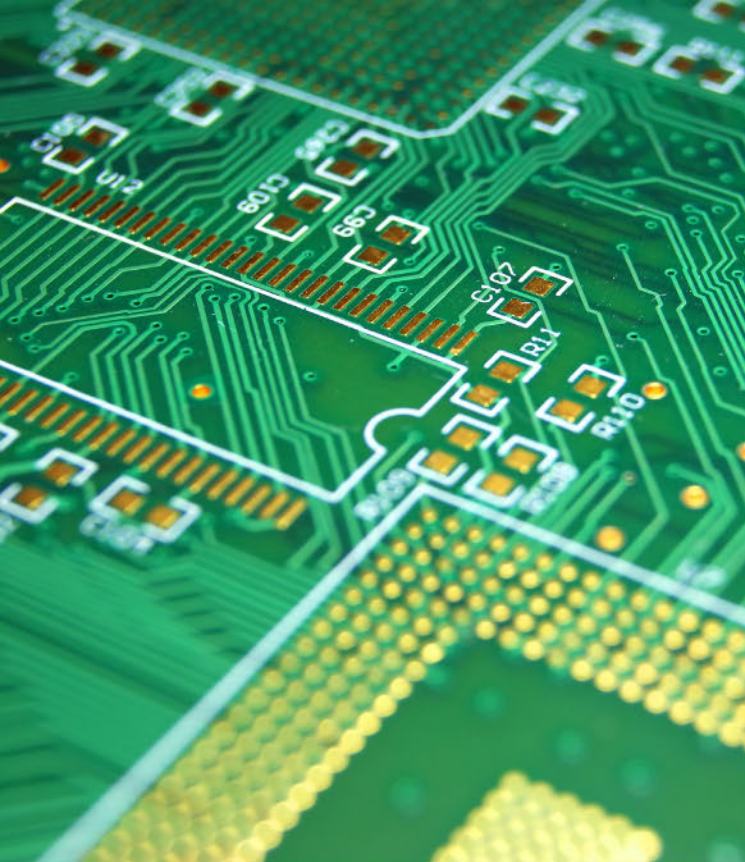
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inadequately thermally managed components will almost certainly overheat, which will negatively impact the surrounding components and lead to reduced life expectancy for those components or even their complete failure in service.

Poor reliability arising from thermally induced circuit failures might prove detrimental to brand reputation, but what if the application served a critical role? Applications might include the following:

- A safety-critical device upon which the safety of personnel working in a hazardous environment might depend
- A device that simply would not function without proper thermal management procedures in place
- A device with a defined working temperature range when in use
- A piece of equipment designed to work in harsh or extreme conditions, which must work reliably regardless of those conditions

## Silicone or Non-silicone?

Traditionally, silicones have always provided the higher temperature option, offering greater stability at temperatures in excess of 150°C compared with other chemistries. However, recent advances have seen the gap between the thermal performance of silicone and some non-silicone materials narrow slightly with new non-silicone market entrants now offering excellent stability at temperatures up to 180°C.

As well as providing excellent high-temperature performance, silicones offer very good environmental stability, particularly where electronic devices are operated in areas of high humidity. Their very low viscosity ensures fast flow and thorough coverage during application, and also makes them an excellent choice for application via screen/stencil printing.

Whilst possessing some clear thermal advantages over non-silicone technologies, silicones do have some negative issues, including a phenomenon called migration. Migration occurs when volatile low molecular weight siloxanes are released from the silicone, caus-

ing problems in the surrounding environment. Where electronics are concerned, migration results in the formation of silicon carbide on PCB surfaces, leading to failures.

In the wider production environment, deposits of low molecular weight siloxanes on surfaces in other parts of the factory can also lead to problems with the adhesion of surface finishes, particularly paint, the quality of which may be compromised. Such siloxanes can also find their way around factories through ventilation and extraction systems, causing even wider spread problems, and in some incidences, a total ban on silicone containing materials may be in place at certain production plants.

Thus, there is an increasing demand for non-silicone products. One contributing factor is the global shortage of silicone, which is forcing suppliers to pass on price increases to customers. Indeed, some manufacturers of silicone-based thermal management products are warning about hefty price increases of up to 25%.

It is also perhaps the escalating growth of the global LED market that is fuelling the move towards non-silicone solutions as the long-term reliability of silicones in LED applications is now in question [1]. Non-silicone thermal management solutions now deliver a high-performance alternative to silicone materials and provide manufacturers, such as those involved in the LED lighting industry, with an immediate drop-in solution.

## The New Kids on the Block

Thermal pastes are at the forefront of thermal management applications and are expected to remain so for some years to come. They are easy to apply and rework whilst providing a cost-effective alternative to thermally conductive bonding products, such as RTVs and two component epoxies, for example.

Thermal pastes have offered some of the lowest thermal resistance values available in the market for thermal interface applications, but in recent years, a new rival to this material technology has appeared on the scene—phase-change materials. Like pastes, phase-change materials can also be applied very thin-

ly, therefore offering exceptionally low thermal resistance. With phase-change technology, a key benefit is the greatly reduced effects of pump out, making phase-change materials an excellent choice for applications that undergo widely varying temperatures.

With thermal management playing more and more of a crucial role in electronics, it is likely that the stability of these new phase-change materials will see them take an overwhelming lead in thermal management technology. And as this technology rapidly develops, this will take effect sooner rather than later. **DESIGN007**

**References**
1. "Electrolube Addresses Major Market Changes to Thermal Management of LEDs," SMT007 Online.

**Jade Bridges** is global technical support manager at Electrolube. To read past columns from Electrolube, click here. Also, visit I-007eBooks.com to download your copy of Electrolube's book, *The Printed Circuit Assembler's Guide to... Conformal Coatings for Harsh Environments*, as well as other free, educational titles.

# KAIST Technology Controls Near-field Thermal Radiation

In the nanoscale gaps, thermal radiation between objects increases greatly with closer distances. The amount of heat transfer in this scale was found to be from 1,000 to 10,000 times greater than the blackbody radiation heat transfer, which was once considered the theoretical maximum for the rate of thermal radiation. This phenomenon is called near-field thermal radiation. With recent developments in nanotechnology, research into near-field thermal radiation between various materials has been actively carried out.

Surface polariton coupling generated from nanostructures has been of particular interest because it enhances the amount of near-field thermal radiation between two objects, and allows the spectral control of near-field thermal radiation. This advantage has motivated much of the recent theoretical research on the application of near-field thermal radiation using nanostructures such as thin films, multilayer nanostructures, and nanowires. Thus far, most of the studies have focused on measuring near-field thermal radiation between isotropic materials.

A joint team led by Professor Bong Jae Lee and Professor Seung Seob Lee from the department of mechanical engineering at KAIST succeeded in measuring near-field thermal radiation according to the vacuum distance between metallo-dielectric (MD) multilayer nanostructures by using a custom MEMS (microelectromechanical systems) device integrated platform with a three-axis nanopositioner.

By measuring the near-field thermal radiation with a varying number of unit cells and the fill factor of the multilayer nanostructures, the team demonstrated that the surface plasmon polariton coupling enhances near-field thermal radiation greatly and allows spectral control over the heat transfer.

The researcher's thermal radiation control technology can be applied to next-generation semiconductor packaging, thermophotovoltaic cells, and thermal management systems. It also has the potential to be applied to a sustainable energy source for IoT sensors.

This research, led by Ph.D. Mikyung Lim and Ph.D. candidate Jaeman Song, was published in Nature Communications.

(Source: KAIST)
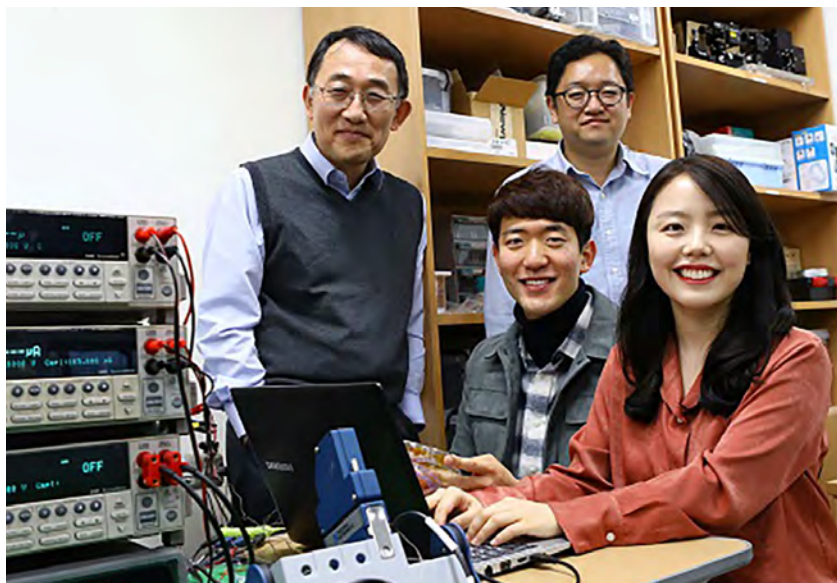
# MilAero007 Highlights

## FTG to Acquire U.S.-based Circuit Board Company ▶

Firan Technology Group Corporation has entered into an agreement to acquire a U.S.-based circuit board manufacturing company focused on the aerospace and defense markets.

## IPC's U.S. Export Control Compliance Workshops ▶

To help the electronics industry stay abreast of U.S export control obligations, IPC is hosting training workshops the week of April 29, 2019, in California, Illinois, and Virginia.

## NASA 'Nose' Importance of Humans, Robots Exploring Together ▶

NASA is sending humans forward to the Moon, this time to stay. Upcoming expeditions to the Moon will require making every moment of astronaut time outside the safety of the Gateway in orbit and lunar lander system on the surface count. Robotics will enable lunar crews to do more while minimizing their risk.

## World's First Flight of Pioneering 'Lighter Than Air' UAV ▶

A new type of unmanned aerial vehicle (UAV) has made a successful maiden flight thanks, in part, to the expertise of engineers from the University of Southampton.

## PCB Design Is All in the Family With Nicole Pacino ▶

I shared a flight with Nicole Pacino on the way to Altium Live in Munich, and she mentioned that her father was speaking at the show. I went down the list of speakers, and it turned out that her dad is Mike Creeden of San Diego PCB. In Germany, I asked Nicole to tell us

about how she got into this industry, and what we could do to draw more young people into this career.

## DARPA Seeks to Make Scalable On-chip Security Pervasive ▶

Program to focus on addressing the economic and technical challenges associated with incorporating scalable defense mechanisms into chip designs.

## NASA's Mars Helicopter Completes Flight Tests ▶

Weighing in at no more than 4 pounds (1.8 kilograms), the helicopter is a technology demonstration project currently going through the rigorous verification process certifying it for Mars.

## TTM Invests in Two Nano Dimension Additive Manufacturing Systems ▶

Nano Dimension Ltd. announced that TTM Technologies has expanded its relationship with Nano Dimension by purchasing two additional DragonFly Pro systems, to complement the existing single unit at the facility.

## University Students Point to the Future in their Research ▶

Cutting-edge automation, AI, machine learning, and Industry 4.0 are all part of the response to the increasing demands for printed circuit boards that are not only faster, smaller, and cheaper but also higher-frequency, lower-loss, more temperature tolerant, and higher reliability. In many cases, it will be unique and advanced research coming out of the university system that will help move the industry forward.

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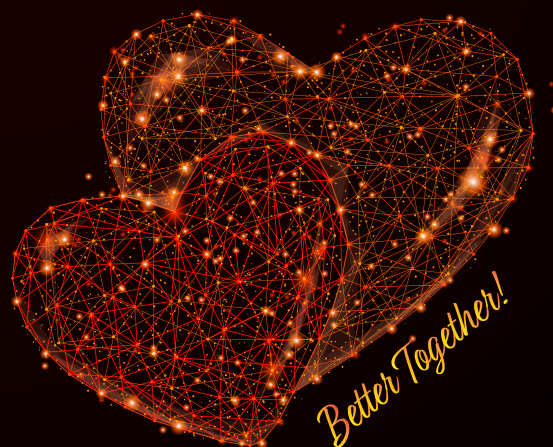
# MCAD Is From Mars, ECAD Is From Venus

**Article by Linda Mazzitelli**
PTC

The ability to clearly communicate design intent from ECAD to MCAD is fraught with complexities and is a primary contributor towards missing key project milestones.

"Product development now requires electromechanical collaboration with teams that not only work locally, but more often work across multiple states, countries, and continents, which presents a unique challenge when communicating between the different design and engineering domains," said Alex Grange, technical marketing engineer at Mentor, a Siemens Business.

While collaboration is essential for ensuring ECAD designs and MCAD assemblies are in sync, the process itself can be time-consuming and error-prone, and as a result, issues can (and do) occur.

In addition to the obvious technology gap between ECAD and MCAD, there is also a terminology gap. Terms, such as "layers" and "parts," have a slightly different connotation in each domain. Also, since work typically continues after updates are sent, ensuring that the data is in sync creates its own set of challenges, leading to potentially more confusion and missed changes. Plus, the more popular formats (STEP/IDF) require supporting documentation to communicate their intent, and trying to find a methodology that will consistently work for you can be downright frustrating!

Ron Sutherland, CAD/simulation administrator at Intel, added, "At Intel, we are examining our ECAD/MCAD collaboration processes more closely now than ever. The interaction and collaboration between these two engineering disciplines have grown more and more vital to the successful design of electromechanical products. Close collaboration between ECAD and MCAD design engineers enables a higher-quality product with less need for rework, which decreases time to market and costs."

## It's All in the Numbers

Statistics show that design verification is 60–80% of the overall design cycle time due to the manual communication of engineering changes during the design review process. In addition, more than half of today's complex

designs must be redesigned because of functional errors found after prototype designs are built and verified. Of those errors, over 44% are related to electrical problems (EMC/SI) not being verified and communicated to the physical design team due to the lack of intelligent browse, query, and communication capabilities for engineers, test, and manufacturing.

## How We Do It Today

In the past, options for collaboration were pretty limited to DXF, which required extensive manual file mapping. Today, there are multiple choices, each with their own pros and cons.

In the case of IDF or STEP, both require that the entire database is exchanged each time. This generally entails sending a detailed README file along with marked-up PPT and/or PDF files to explain what was being changed, where the changes occurred, and why they were done, as it is virtually impossible to tell simply by importing the file.

While those two formats are the most popular method of data exchange and the methodology still works, it is truly a static way of communicating because:

- Once the changes are passed to the other domain, the design process does not stop while waiting for a response
- If there are any questions regarding the updates, they are typically resolved via a face-to-face discussion, phone, or email (i.e., it's hard to communicate the acceptance or rejection of proposed changes)
- Conversations are generally not documented or retained, leading to lack of traceability regarding who, what, why, and when the changes were done

Also, to implement the changes, constraints are often turned off, resulting in interference issues and potential re-spins.

## What Are the Options?

While all file format transfers generally have the same inherent issue—the files need to be created and managed—as the industry evolves, so does the collaboration process. Now, the emerging standard is moving towards EDMD, which uses the incremental data exchange (IDX) file format.

What is the difference, you might ask? Is it just another format that follows the same mold as the others? For those of you who are not familiar with it, the EDMD format is based on the ProSTEP iViP format, which is:

- Standards-based
- Process-oriented
- STEP-affiliated

In addition, it is supported by almost all of the major ECAD and MCAD vendors on the market today as the "go-forward" form of collaboration.

What sets it apart from the other formats, is that it enables incremental data exchange (i.e., the IDX file only contains items that have been added, deleted, or updated from the last data exchange). To do this, it assigns a unique identifier to each item associated with the design including components, holes, keep-in/-out areas, and the board itself.

It also allows you to:

- Evaluate updates before incorporating them into the design
- Propose new updates without sending the entire database
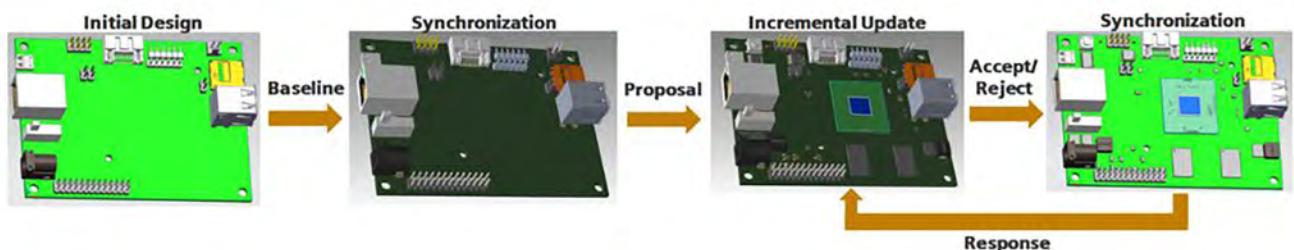


Figure 1: The IDX format flow, which allows incremental data exchange.

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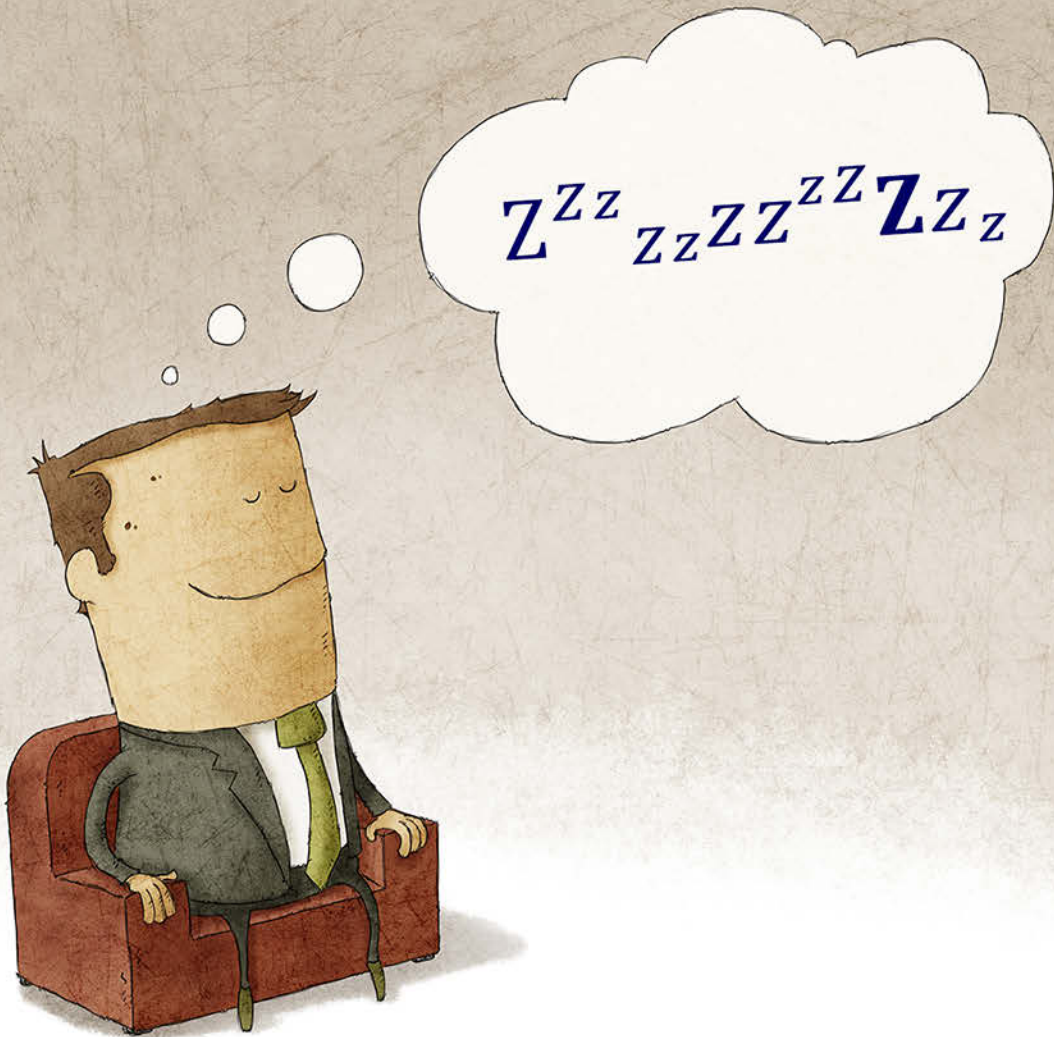
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- Electronically accept or reject proposed changes
- Electronically add notes to the collaboration file regarding design intent
- Retain change history regarding who did what, why, and when

The IDX files generated from either the ECAD or MCAD tools are then managed in a "collaboration" folder located on either a local or shared drive.

"IDF was a good step in the right direction. We were able to pre-locate components, represent holes and transfer keep-in/-out information," stated Shawn Larson, senior technical fellow at Zuken. "Today with IDX, we have a much more robust model of the PCB and its structure. Board-level components, traces, pads, copper, component heights, rigid/flex support, and more can be passed. We even have the ability to accept or reject changes electronically. The word 'collaboration' fits much better with the way we want to work, and the day-to-day data flow between the mechanical and electronic teams is cleaner and clearer."

While IDX may not be perfect, it does provide a better way to more accurately and clearly communicate design intent between domains and achieve business goals.

"Companies today are striving to streamline their design process and reduce the oppor-

tunity for introducing errors throughout the product life cycle," said Sandra Humphrey, senior consultant at Archer Grey. "Utilizing IDX allows companies to introduce products to market faster and with higher quality by enabling interdisciplinary collaboration, which provides an efficient method to communicate design intent, initiate change proposals, and ensure these work items are completed in a timely manner irrespective of geographic location."

## How Does IDX Data Exchange Work?

You can think of IDX as a way to initiate and perpetuate a virtual "conversation" with the person you are collaborating with. Whoever initiates that conversation must also be the one that receives the final acknowledgment. Let's take a look at two scenarios:

### 1. Initial "Baseline" Data Exchange
- "Discussion" is initiated by either ECAD or MCAD and sent to the other domain as a "baseline" file that contains all of the data in an initial exchange
- The received file is then imported and previewed
- A response is sent to initiator acknowledging the successful baseline import
- The databases are now in sync, and either side is free to make additional updates
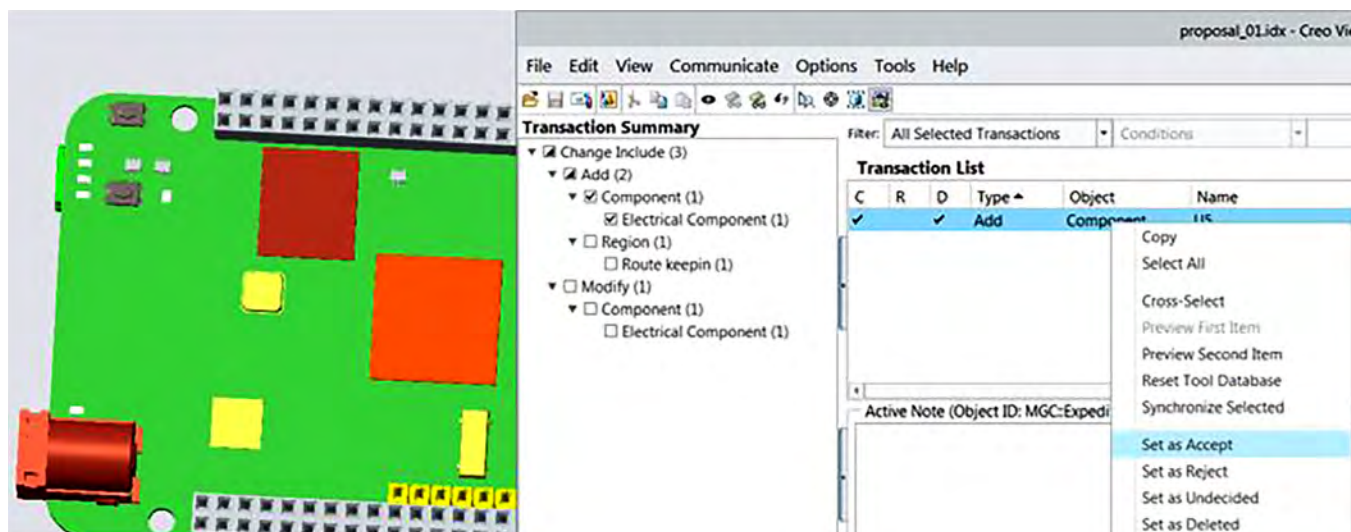


Figure 2: Typical ECAD/MCAD collaboration flow diagram.
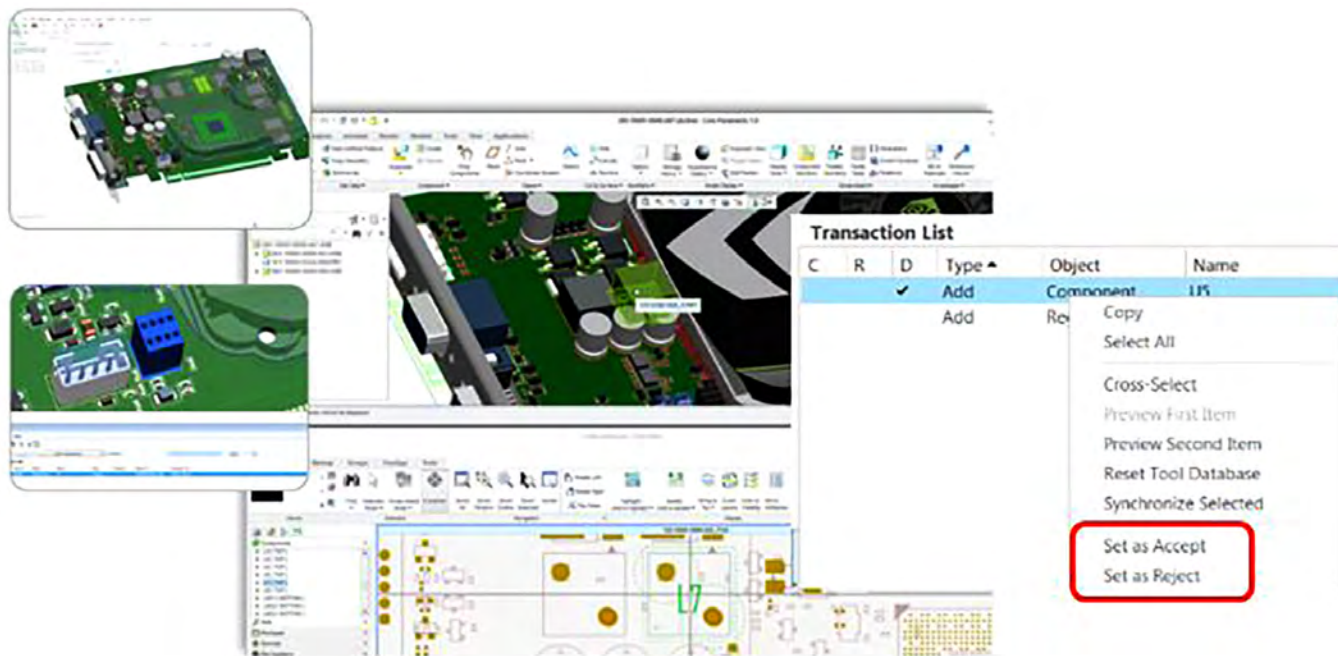
Figure 3: Collaboration integration.

## 2. Incremental Exchange

- "Discussion" is initiated by either ECAD or MCAD and sent to the other domain as a "proposal" file that contains only items that have been added, deleted, or changed
- The received file is then imported and visually previewed
- Updates are accepted or rejected, and notes are added to each item as needed
- A response is sent to initiator with included annotations
- The databases are now in sync, and either side is free to make additional updates

For final validation, you can create a baseline IDX from both the ECAD database and MCAD assembly and run a comparison between the two to ensure there are no discrepancies.

## Part Mapping

As with any collaboration, ensuring data integrity is paramount, and nowhere is that more important than ensuring ECAD/MCAD part models are aligned correctly. Ideally, a
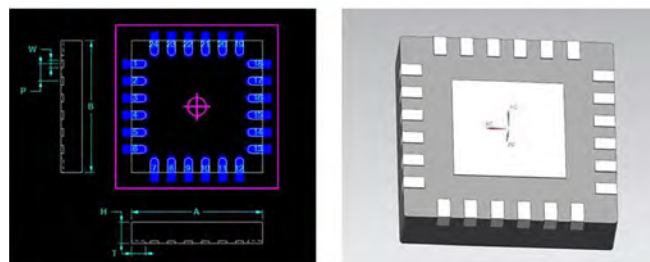


Figure 4: Aligning part models is critical to ECAD/MCAD collaboration.

new part introduction process will ensure that when a new request is submitted, the logical symbol, physical footprint, and MCAD part model are all associated with the correct origins, orientations, and pin alignments during development.

To ensure the parts are aligned correctly, they can either be associated through their part names or via a mapping file that tells the system which part name on the ECAD side aligns with its mechanical counterpart (e.g., ECAD = part_abc, MCAD = part_123).

There are several ways that ECAD and MCAD part data can be associated and displayed. The three typical scenarios are:

- No detailed models have been developed (IDX will take the x, y, and z dimensions of the ECAD parts and use those as a reference on the MCAD side)
- Some detailed parts have been developed (mechanical parts that interact with the housing, including connectors, switches, LEDs, etc.)
- All parts have detailed models

Please note that detailed models are not required to take full advantage of the benefits of IDX, but it does make for a more accurate picture.

## IDX Considerations

Probably the most important thing to remember is that unlike current "throw-it-over-the-wall" methodologies for ECAD/MCAD data exchange, IDX data exchange is a process. Because you are no longer sending the entire database to and fro, it is critical that there is a clearly defined and understood methodology to ensure that the data remains in sync.

The ProSTEP iVip association is continuing to evolve the methodology and include new updates to the standard on regular intervals. New members are always welcome and can contact the organization at prostep.org.

## Future/Extended Collaboration Methodologies

While using file formats for managing data exchange will continue to be with us for the foreseeable future, other collaboration methods are being explored and deployed to enable a more seamless and consistent collaboration methodology.
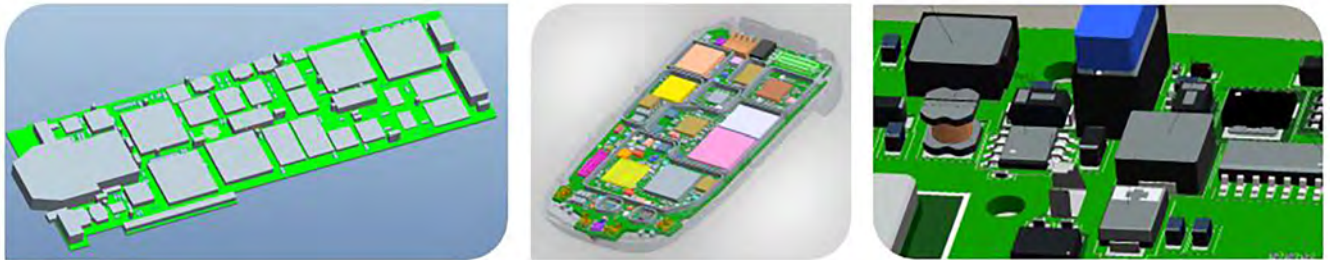


Figure 5: Example of part-mapping options.
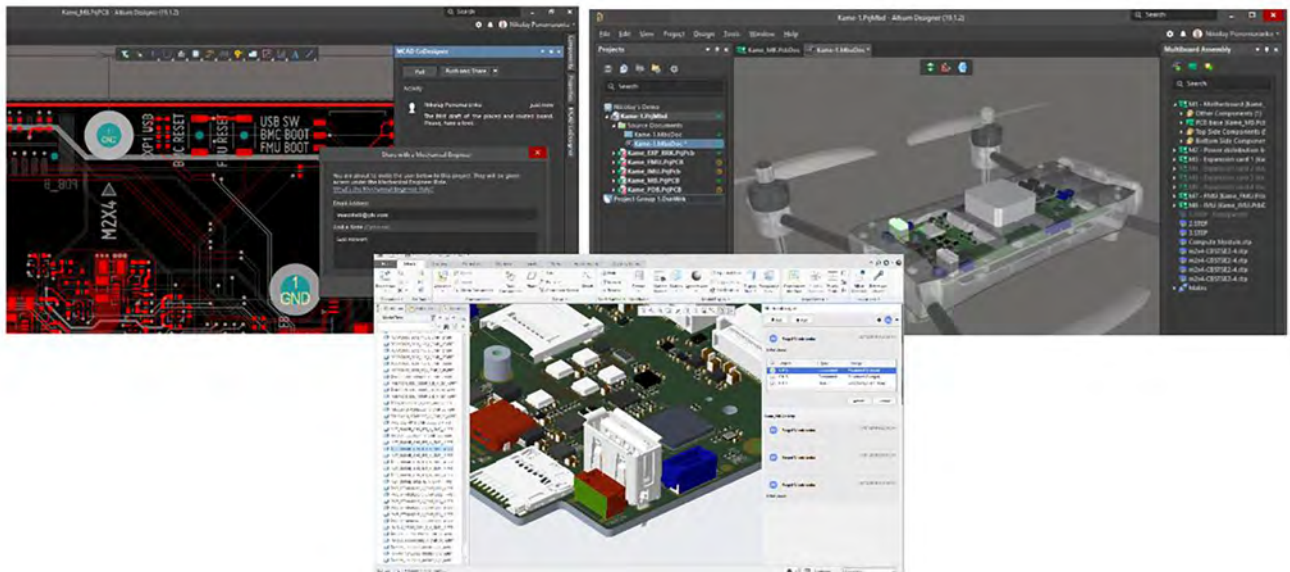


Figure 6: Exchange interface with "push and share" interface.

"File-based methods of ECAD/MCAD collaboration are reaching their limits, and the negative effects on the product development process are growing," said Nikolay Ponomarenko, director of product management for Altium. "PCBs are core components of mechatronic assemblies and design teams can no longer afford to have them designed outside of the whole product context."

Ponomarenko continued, "By enabling a direct integration between the ECAD and MCAD domains through a dedicated extension that lives and operates within the MCAD environment, designers and engineers can seamlessly collaborate through a simple 'push-and-pull' operation. This eliminates the need to manage and exchange data via external files, such as IDF, IDX, or STEP to accurately communicate updates from one domain to another."

## How to Proceed

First and foremost, take a look at your options and decide what is best for you. The format and process that works well for one organization might not for another. Also, be assured that the existing data exchange file formats are not going away anytime soon, so there is no need to rush your decision regarding what to do next. Once you've finally settled on what format you're going to use, you need to figure out your evaluation and implementation strategy. To ensure success, document the process and educate the design teams to ensure everyone in your organization understands the methodology. **DESIGN007**

**Linda Mazzitelli** is the product management director at PTC responsible for ECAD design data management, visualization, and ECAD partner management.

# Viennese Scientists Develop Promising New Type of Polymers

Organic polymers can be found in solar cells, sensors, LEDs, and many other technical applications today. One specific type–S-PPVs–were previously regarded as promising, but were almost impossible to produce until recently. Now, a team from Technische Universität Wien has managed to identify a new chemical synthesis process for the production of S-PPVs.

PPV polymers have a long, solid hydrocarbon structure to which certain side groups are attached. By choosing different side groups, it is possible to set the electronic properties of the material. Until now, O-PPVs have been used for this.

"If it is possible to replace oxygen side groups with sulphur side groups, this creates a new polymer–an S-PPV–which has significantly improved properties," says Florian Glöcklhofer from the Institute of Applied Synthetic Chemistry at TU Wien. "We knew that this could lead to improvements in the transport of electrical current and would significantly improve the overall stability of the polymer."

After four years of work and numerous bitter setbacks, the team finally succeeded in discovering a reliable, straightforward method for producing S-PPVs. Suitable monomers are manufactured with the help of microwave radiation, which are polymerized, and the side groups can then be further modified.

The new synthesis method has now been patented with the help of TU Wien's Research and Transfer Support. According to Glöcklhofer, the synthesis uses inexpensive base materials and does not require any palladium catalysts or similar expensive interim steps.

(Source: Technische Universität Wien)

## Editor Picks from PCBDesign007

### 1 New eBook Explores Tips for Executing Complex PCB Designs ▶

Written by Scott Miller, COO of Freedom CAD Services, *The Printed Circuit Designer's Guide to… Executing Complex PCBs* provides a set of guidelines for designing the most complex, high-speed circuit boards. This book is a must-read for anyone designing high-speed, sophisticated PCBs.
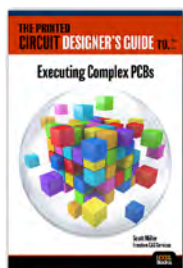
### 2 Nano Dimension Offers Update on Dragonfly 3D Printer a Year After Launch ▶

The Nano Dimension Dragonfly 3D printer arrived in much fanfare a little over a year ago. Customers around the world are using them to print antennas, sensors, and PCBs. At Altium-Live in Munich, I asked Product Manager Robert Even to discuss what they've learned in the year since the Dragonfly debuted, and some potential uses for 3D printing technology.

### 3 Lightning Speed Laminates: Higher Frequencies Pave Way for Flexible Circuit Materials ▶

The smaller wavelengths of mmWave frequencies tend to highlight circuit material anomalies at those higher frequencies—anomalies that can also influence the radio frequency (RF) performance of the circuit. Such material anomalies include variations in dielectric thickness, dielectric constant (Dk), copper conductor width and spacing.
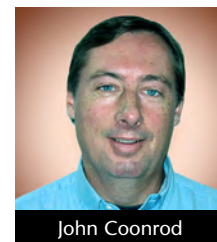
John Coonrod

### 4 Beyond Design: The Proximity Effect ▶

Skin effect and the proximity effect are manifestations of the same principle—magnetic lines of flux cannot penetrate a good conductor. The difference between them is that skin effect is a reaction to the magnetic fields generated by current flowing within a conductor.

## 5 PCB Design Is All in the Family With Nicole Pacino ▶

I shared a flight with Nicole Pacino on the way to Altium Live in Munich, and she mentioned that her father was speaking at the show. I went down the list of speakers, and it turned out that her dad is


Nicole Pacino

Mike Creeden of San Diego PCB. In Germany, I asked Nicole to tell us about how she got into this industry, and what we could do to draw more young people into this career.
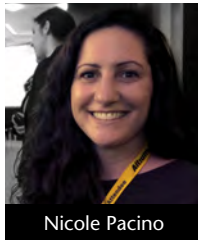
## 6 DAIKIN Adopts Mentor's Xpedition PCB Design Platform for Global Design and Data Management ▶

Mentor, a Siemens business, today announced that DAIKIN, one of the world's leading air conditioning manufacturers, selected Mentor's Xpedition printed circuit board (PCB) design flow software as their global design environment.

## 7 George Fox University: Teaching PCB Design to EE Students ▶

Gary Spivey is director of engineering projects at George Fox University, a Christian college in the Pacific Northwest, and his students learn to design and fabricate a PCB while also giving back to the com-


Gary Spivey

munity. Not surprisingly, these graduates get snapped up quickly. In this wide-ranging interview, Spivey discusses GFU's engineering curriculum, their cutting-edge lab facilities, and the need to teach students to think critically.

## 8 SimplifyDA: Time for a New Autorouter Paradigm? ▶

At DesignCon, I spoke with SimplifyDA CEO Zen Liao and Director of Sales and Marketing Dale Hanzelka. Simplify-DA is putting a new twist


Zen Liao & Dale Hanzelka

on the old autorouter by utilizing topological technology. I asked them to discuss their approach to autorouting, and how they plan to entice more PCB designers to use routers. Is it time for a paradigm shift in autorouting?
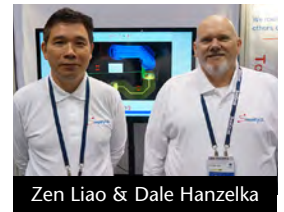
## 9 The Shaughnessy Report: The Youth of the Industry ▶

When was the last time your company hired someone straight out of school, or even under 40? Until recently, I would have guessed



1985. But there's something happening, and I hope it's the beginning of a trend. Young people are once again entering the PCB design community workforce, and the overall PCB manufacturing industry as well.

## 10 EMA Partners with Berkeley SkyDeck ▶

EMA Design Automation has announced a partnership with Berkeley SkyDeck. This partnership provides Or-



CAD software to SkyDeck startups for use in the design and development of printed circuit board (PCB) electronics within their innovative products.

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# Career Opportunities



## Analyst Programmer, Hong Kong

We believe in caring about our people because they are our greatest asset. CML works with multicultural stakeholders daily to achieve more and bring them the best solutions. That's why we continuously invest in optimizing our culture and focus on providing our team with opportunities to develop their skills (e.g., through professional coaching to achieve their highest potential).

The analyst programmer will assist the IT and ERP manager in Hong Kong to support the company's BI systems, ERP systems, and other related IT-landscape applications.

In addition, this post will participate in system development projects and provide support including, but not limited to, user requirement collection and analysis, user training, system documentation, system support and maintenance, enhancement, and programming.

- Develop and enhance related IT systems and applications
- Prepare functional specifications
- Transfer the relevant business and interface processes into IT systems and other applications to get a maximum automation degree and prepare all required business reports
- Conduct function testing and prepare documentation
- Manage help desk/hotline service

CML is a leading provider of printed circuit boards. We develop tailor-made sourcing and manufacturing solutions for our customers worldwide with strong partnerships and reliable connections.



## APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

# Career Opportunities

# Career Opportunities

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# Career Opportunities

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### Huntingdon Valley, PA

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- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

**Requirements and Qualifications:**
- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
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**We Offer:**
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- Retirement fund matching
- Continuing training as the industry develops

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## Gardien

### Sales Personnel, Japan

The Gardien Group is looking to expand the sales team in Tokyo, Japan, and seeking highly motivated team players with a positive attitude. Prior experience in the PCB industry is an advantage but not necessary for the right candidate.

The role involves working closely with the customer to identify their needs and deliver the right solution. The candidate should be able to offer a high level of customer satisfaction to ensure ongoing sales.

Training will be provided along with a competitive benefits package, excellent growth opportunities, and periodic bonuses.

Interested candidates, please contact us at careers.jp@gardien.com with your resume.

*Kindly note only shortlisted candidates will be notified.*

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# Career Opportunities

## U.S. CIRCUIT

### Sales Representatives (Specific Territories)

Escondido-based printed circuit fabricator U.S. Circuit is looking to hire sales representatives in the following territories:

- Florida
- Denver
- Washington
- Los Angeles

**Experience:**
- Candidates must have previous PCB sales experience.

**Compensation:**
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Contact Mike Fariba for more information.

mfariba@uscircuit.com

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## ELECTROLUBE
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The successful candidate will benefit from a generous package and report directly to the U.S. general manager.

Applicants should apply with their CV to melanie.latham@hkw.co.uk (agencies welcome)

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# Career Opportunities

# Events Calendar

**IPC High-Reliability and Microvia Summit** ▶
May 14–16, 2019
Hanover (Baltimore), Maryland, USA

**Design & Manufacturing New England** ▶
May 15–16, 2019
Boston, Massachusetts, USA

**Maker Faire Bay Area** ▶
May 17–19, 2019
San Mateo, California, USA

**Medical Electronics Symposium 2019** ▶
May 21–22, 2019
Elyria, Ohio, USA

**IMS 2019** ▶
June 2–7, 2019
Boston, Massachusetts, USA

**MD&M Medical Design East** ▶
June 11–13, 2019
New York, New York, USA

**PCB West 2019** ▶
September 9–11, 2019
Santa Clara, California, USA

**SMTA International** ▶
September 22–26, 2019
Rosemont, Illinois, USA

# Additional Event Calendars

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**EDITORIAL CONTACT**
**Andy Shaughnessy**
andy@iconnect007.com
+1 404.806.0508 GMT-5

**SALES CONTACT**
**Barb Hockaday**
barb@iconnect007.com
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