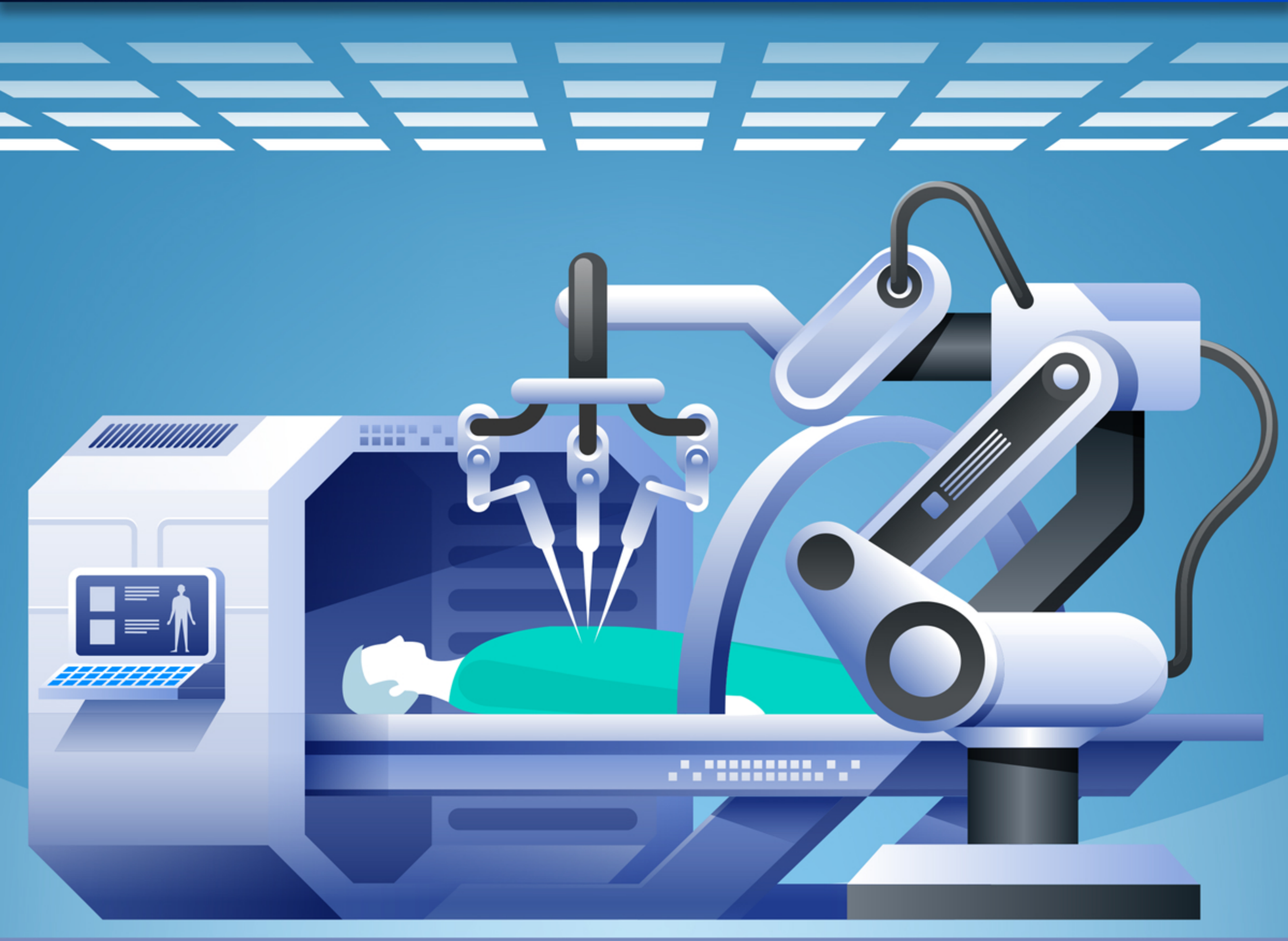
I-Connect007

NOVEMBER 2018

DESIGN007 MAGAZINE



Designing for the Future of Medicine

DESIGN007 MAGAZINE

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The medical electronics market is blowing up, and there doesn't seem to be a ceiling. A recent report estimates that the global medical device market will reach $409.5 billion by 2023, expanding at a CAGR of 4.5% from 2018 to 2023. All of this bodes well for PCB designers and design engineers. We asked our expert contributors to give us their prescription for best practices in the medical PCB design segment.

NOVEMBER 2018 • ADDITIONAL CONTENT

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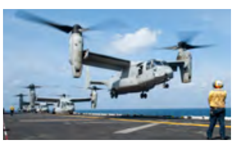

Medical Electronics: Vital Signs Are Good

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

When Marcus Welby, M.D. premiered in 1969 with Robert Young in the starring role, the good doctor usually had everything he needed in his trusty doctor bag. And if Dr. Welby couldn't fix you with his stethoscope and sphygmomanometer, the local hospital was up to the task with its EKG, EEG, and heart rate monitors beepin' away, and ready cure you before the end of the episode.

Now, the newest Apple Watch features a titanium electrode built into the digital crown that allows the wearer to give himself or herself an electrocardiogram. Devices like the Fitbit let the user track pulse rate, blood pressure, and body temperature. Marketing these devices under the "fitness" umbrella was a stroke of genius that capitalizes on the current fitness trend.

Call it the democratization of medical care, if you will. But whatever the name, the medical electronics market is blowing up, and there doesn't seem to be a ceiling.

A recent report by Research and Markets estimates that the global medical device market will reach $409.5 billion by 2023, expanding at a CAGR of 4.5% from 2018 to 2023. The same group predicts that the world's market for wearable medical devices will hit $12.1 billion by 2021.

It was inevitable, really. Every part of our lives—registering to vote, making an offer on a house, driving your car—is becoming more automated. If this rate of medical innovation continues, visits to the doctor and hospital may become increasingly rare in the near future.

As a male, this is good news for me. Men are preternaturally predisposed to avoiding the doctor until a wound becomes infected or we're at death's door. Because men love gadgets, many of us would be happy to monitor our vital signs, especially if the devices have that necessary "cool" factor.

I really don't mind wearing my CPAP mask because the technology is so cool. It's IoT-ready and capable of sending a daily report of my nocturnal breathing activities to my doctor. It uses an encrypted cellular Internet connection, so my neighbors can't hack into it. When I talk to other CPAP-wearers (primarily at PCB trade shows), we talk smack about who has the coolest CPAP machine like we're comparing motorcycles, cars, or sailboats.

All of this bodes well for PCB designers and design engineers. Medical is one segment that just keeps growing, and more people in our industry are moving into medical every year. IoT and 5G are going to make the medical PCB designer's job that much more interesting—and complicated.

For this month's medical issue of *Design007 Magazine,* we asked our expert contributors to give us their prescription for best practices in the medical PCB design segment. In our cover story, StarFish Medical's Kenneth MacCallum discusses some of the trends he sees in medical electronics, and some of the challenges designers face in this evolving market. Next, we have an interview with DfR Solutions' Dock Brown fresh from his SMTAI keynote on medical hardware. Dock explains how predictive engineering software can be used early in the design cycle to spot component failures and drive costs down.

Consultant Tim Haag has a great feature column about how electronic medical devices are playing a lifesaving role in his family right now, and why your job matters—even if it doesn't always seem that way. Then, we have an interview with Tamara Jovanovic—a recent graduate and PCB designer at Happiest Baby, a Los Angeles company that makes smart baby beds that can sense when an infant is about to suffocate and alert the parents. Finally, we have an interview with Dr. Titu Botos of NeuronicWorks who discusses IoT and why he believes that the Internet of Body (IoB) could be the "next big thing."

We also have columns by our regular contributors Steph Chavez, Barry Olney, Vern Solberg, Doug Brooks (with special guest Dr. Johannes Adam of ADAM Research), Istvan Novak, Alistair Little, and Bob Tise and Dave Baker. Further, we have an article on the effects of fiber weave on high-speed signal integrity by CF Yee of Keysight Technologies.

If you don't already subscribe to *Design007 Magazine,* I won't tell anyone. Click here to subscribe to our magazine and newsletters. See you next month! **DESIGN007**

Andy Shaughnessy is managing editor of *Design007 Magazine.* He has been covering PCB design for 18 years. He can be reached by clicking here.

Electronic Tattoos Add Power to Wearable Computing

Associate Professor of Mechanical Engineering Carmel Majidi discusses electronic tattoos, which are circuits made of silver nanoparticles printed on the same film used for children's tattoos. These electronic tattoos have applications that range from health care to personal electronic devices to gaming.

(Carnegie Mellon University)

In Medical PCB Design, Innovation Never Stops

Feature Interview by Andy Shaughnessy
I-CONNECT007

Medical electronics is an exciting field to be working in right now, with new ideas coming online almost daily. We last interviewed medical PCB designer Kenneth MacCallum in 2015. Recently, I asked him to give us an update on trends he's seeing in medical electronics, and some of the challenges in adapting the latest technology to this segment of the industry.

Andy Shaughnessy: Give us a brief background on StarFish Medical, and your work there. We don't see many physicists who are also PCB designers.

Kenneth MacCallum: StarFish is a medical device design, development and contract manufacturing company. We help medtech innovators throughout North America overcome challenging technology obstacles to create breakthrough products that improve health and save lives. We're different from our competitors because we focus on enabling medical device start-up companies to dial in their value proposition.

I am an engineering physicist, which means I have a strong mathematics and physics background and apply it through engineering. My deepest skillset is electronic design, with a system level, first principles approach. I believe that to design the best PCBs for a problem, the overall solution will be a balancing act across all disciplines. A tricky set of requirements is rarely optimally addressed without give and take from everyone involved: industrial designers, human factors specialists, mechanical engineers, software developers, optical designers, regulatory specialists and project managers. This is particularly true when the primary function of a device is fundamentally reliant on some other discipline, like microfluidics or optics. In those cases the electronics is really a support role.

Shaughnessy: A lot has happened with medical tech since our last interview almost three years ago. Can you give us an update on some of the trends you're seeing in medical electronics?


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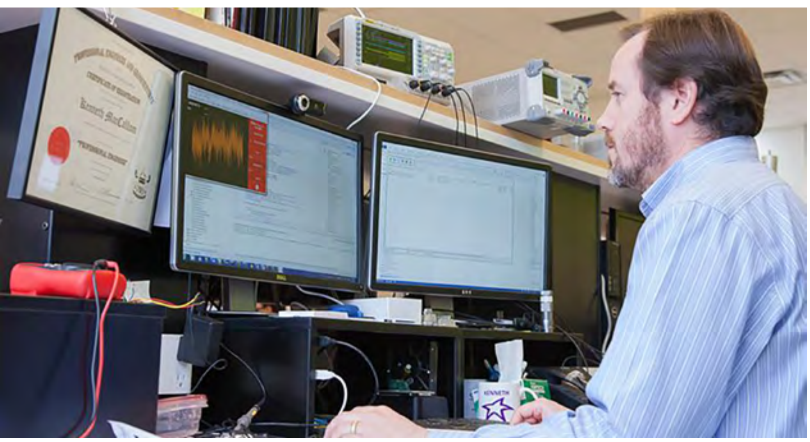
Are you working on any wearables, for instance?

Kenneth MacCallum

MacCallum: There is a growing desire to bring medical devices into the patient's home. This means that many devices no longer interact primarily with doctors, nurses and technologists but with the patient, and without direct supervision. These devices often consist of multiple elements: those that are wearable, portable and even implanted.

Three years ago, there was a growing buzz around connectivity, "big data" and "the cloud." In the medical device industry, these terms collectively lumped into the term "digital health" and this in turn has morphed into the concept of "connected health." Since then, it's become clearer how to successfully leverage and implement these ideas in a practical and economical fashion. We're also learning how to address the associated regulatory hurdles, including the mandated attention to ensuring that identifiable patient data remains protected and secure.

Notwithstanding the trends, the fundamental focus on device safety and efficacy has not changed. In fact, if anything this primary goal of medical device design has strengthened. No matter how cool and progressive technology gets, if we can't ensure that we can control the safety of the patient and operator or if we cannot demonstrate that the intended use is implemented in a reliably effective manner, then we have not succeeded.



Shaughnessy: What are the biggest technical challenges you and your team face today?

MacCallum: Now, more than ever, our clients are expecting the same richness in user interfaces and connectivity with their medical device design as they see in the consumer products that they interact with every day. This means not only harnessing the latest trends in technology and their implementation but also developing creative ways to adapt them to the nuances of the medical device market.

For instance, although the margins tend to be higher in our industry, the quantities are often orders of magnitude smaller. Also, because of the regulatory hurdles of getting market clearance for just one product, leveraging development effort across suites of related products is rarely achieved. The challenge is to adopt all of these varied features and modalities in a cost-effective and efficient manner.

Shaughnessy: Is IoT becoming fairly standard in the medical segment?

MacCallum: The growth in IoT is certainly generating plenty of interest in the medical device field. We see it creeping into our industry as medical devices become smaller and also as functionality that used to be limited to clinics and hospitals is made available for home use. Treatment and monitoring are increasingly done without direct physician supervision and in much less controlled environments. This means that technology must fill the gap to process and convey the data effectively, safely and securely to ensure the best clinical results.

It used to be that connectivity was a desired add-on. Now, many devices that we are working on could not achieve their intended use without it. Fortunately, we are able to leverage many of the connectivity solutions springing out of the IoT trend. Similarly, the sensor technology that is evolving rapidly for cell phones and IoT can be readily applied to medical devices to solve some of the problems with gathering clinically valid data in less controlled environments.

Shaughnessy: What advice would you have for any companies considering moving into the medical electronics field? I understand that the FDA regulations alone are pretty interesting to deal with.

MacCallum: The traditional medical device market is quite different from consumer product development, the development cycle is longer, it is more highly regulated, there is a strong requirement for a methodical and deliberate design process. Not only must the products we develop comply to the regulations, standards and guidelines, but the design and development processes that we follow to achieve this are also regulated. We are regularly audited to be sure that our processes continue to comply as the standards evolve, and that there is clear evidence that we are following those processes.

This can seem from the outside like a real downer when we just want to get on with our engineering. Fortunately, most of the requirements boil down to good engineering practices.

Shaughnessy: Is there anything that you'd like to add?

MacCallum: The opportunities to design some really cool circuits in the medtech space seems to be growing without bounds. Embracing the latest and greatest tech that the semiconductor industry has to offer is a continuing opportunity, so long as we keep in mind the fundamental premise of ensuring the safety and efficacy of our devices.

Shaughnessy: Thanks for your time, Kenneth. We appreciate the update.

MacCallum: Thank you, Andy. **DESIGN007**

Electronic Skin Points the Way North

Researchers at the Helmholtz-Zentrum Dresden-Rossendorf (HZDR) in Germany have developed an electronic skin (e-skin) with magnetosensitive capabilities, sensitive enough to detect and digitize body motion in the Earth's magnetic field. As this e-skin is extremely thin and malleable, it can easily be affixed to human skin to create a bionic analog of a compass. This might not only help people with orientation issues, but also facilitate interaction with objects in virtual and augmented reality.

What was science fiction 16 years ago has now become reality, thanks to Dr. Denys Makarov and his team of HZDR researchers. All it takes is a sliver of polymer foil, no more than a thousandth of a millimeter thick, attached to a finger–and the Earth's magnetic field.

"The foil is equipped with magnetic field sensors that can pick up geomagnetic fields," says the lead author Gilbert Santiago Cañón Bermúdez.

With a sensor attached to his index finger, the user started out from the north, first heading west, then south and back again, causing the voltage to rise and fall again accordingly.

In these experiments, pointing to the north corresponded to a movement of the panda to the left, pointing to the south to a movement to the right. When the hand was on the left (i.e. magnetic north), the panda in the virtual world started moving in that direction. When it swiped in the opposite direction, the animal turned on its heels. "We were able to transfer the real-world geomagnetic stimuli straight into the virtual realm," Makarov summarizes.

(Source: Helmholtz-Zentrum Dresden-Rossendorf)

Dock Brown on Succeeding at Failure Analysis

Feature Interview by Barry Matties and Happy Holden
I-CONNECT007

Dock Brown of DfR Solutions gave a keynote speech at SMTAI, "Requirements for Both Cleaning and Coating to Building Medical Hardware." Barry Matties and Happy Holden sat down with Dock to discuss the current trends he sees in failure analysis, the concept of "rules versus tools," and how predictive engineering software used early in the design cycle can help predict failures in components and microvias and drive cost down.

Barry Matties: Dock, can you just tell us a little bit about what DfR Solutions does?

Dock Brown: DfR Solutions is an international reliability consulting firm. There are basically three aspects to the technical portion of our business. We do 1,200–1,300 failure analyses a year. The value proposition that we offer to our clients is that we have a whole suite of on-staff Ph.D. material science folks. These people are experts in chemistry, physics, and metals. What we try to do first is to understand the customer's problem because most of the time, they don't just want a quick cross-section in a picture—they want us to get to the root cause of the root cause of the root cause.

We first try to thoroughly understand the problem or set of problems the customer is facing, and then when we acquire the samples, we treat those very gingerly. We make sure that we have damaged and exemplary sample because oftentimes, you want to do an A/B comparison between the two. Then, we do a very careful disassembly or cross-section; we do non-destructive kinds of things first. Usually, you can see the issue there, and even if you can't see the problem non-destructively, it will help you focus in on it. For example, if you have a 600-ball ball grid array (BGA) with an issue, we can't afford to cross-section every single one of those little guys; we have to focus on the ones that are most likely to be problematic. Once we get down to the failure in the BGA ball, where is that fracture occurring—is it in the metallization or the ball itself, or is it even a pad cratering kind of issue?

The second part of our business is that we sell a software package called Sherlock that does reliability physics analysis. We're applying mathematical modeling to all the various complex material structures that are involved in any kind of electronics applications. You have, in the case of a circuit board, polymers, metals, ceramics, etc. All of these materials

have very different properties, such as stress and strain properties, fracture mechanics, etc.

The Sherlock software can model all that. We combine the modeling with the failure analysis work to do what the people in the automotive industry, for example, are calling "shift left." This is instead of waiting until the last portion of the product development cycle where you're doing low-rate initial production, and then verification validation qualification testing—if you discover problems there, it's very expensive. What the shift left means is that they try to do pre-failure analysis and reliability physics modeling right at the schematic capture and board layout portion of the design development sequence.

What the shift left means is that they try to do pre-failure analysis and reliability physics modeling right at the schematic capture and board layout portion of the design development sequence.

Matties: Predictive engineering, basically.

Brown: Exactly. We can model all those stresses, strains, and ruptured things you're looking for while it's still in software. If you're going to have problems, you want to find those early. In the early part of my career, I worked at Rocket Research Corporation, which made rocket engines for satellites and things like that. The watchword there was if you had a problem, where and when do you want to find it? Do you want to find it when it shows up or when it blows up? In the rocket business, sometimes blowing up is literal. That's an analogy for the solution set that we're trying to offer people nowadays. You can do that shift left kind of thing and find the problem when it shows up, as opposed to when it blows up in testing.

Matties: That's a new shift in thinking though. Do you see more companies looking for this?

Brown: More and more people are looking at it because it's a heck of a lot less expensive. You find issues earlier, and time is money. That's particularly true in the case of automotive. The automotive industry is working on new standards, not only for the circuit board applications, but also within the integrated circuits themselves. As geometries are shrinking in the integrated circuits, as well as at the board level, the CMOS properties inside memory elements and processors are not as long-lived as they used to be.

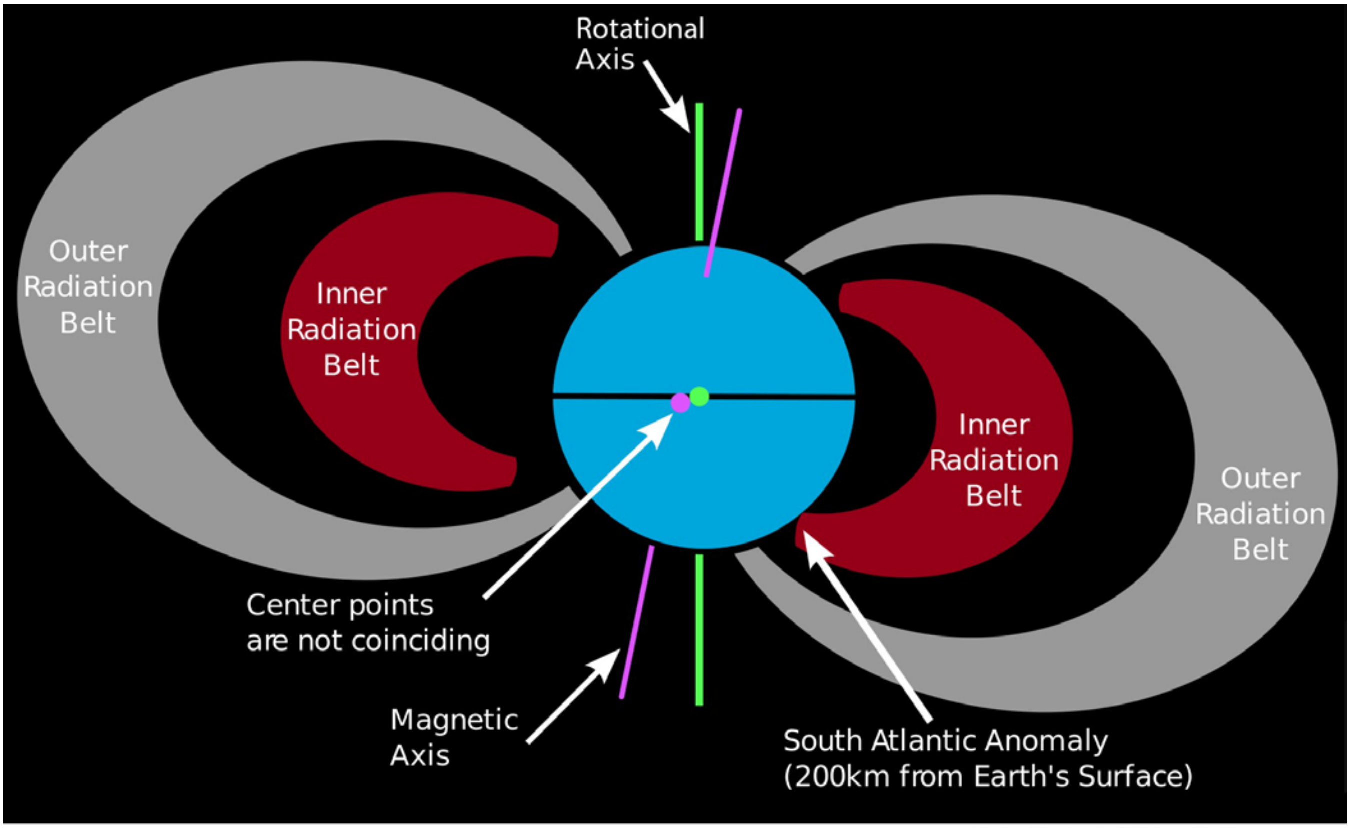
In the old days, people would say, "It's not a tube anymore, it's a transistor—it's all solid state; nothing moves, and nothing will break." What we're finding is those geometries are shrinking in integrated circuits, then at the atomic level, things really do move. We can now model that movement mathematically—for example, electromigration in the metallization of the integrated circuit. If semiconductor manufacturers are going to have a problem with electromigration, we can help them figure that out before they go with the production. In the case of end users in automotive, which is such a harsh environment, if you're going to have those kinds of issues, you want to be able to figure that out.

Matties: Obviously, it's driven by the cost of failure, right? The higher the cost, the more likely they are to look at it on the front end?

Brown: It's also the consequence of failure.

Matties: That's part of the cost, for sure. As technology changes, I would think that you're seeing new types of failures. What trends and failures are you seeing?

Brown: One of the big surprises for all of us was a presentation at the SMTA Pan Pacific Microelectronics Symposium about three years ago.



Marko Markovic, Wikimedia Commons

Some scientists at RESRI and IMS in Europe were looking at what was going on with the radiation effects in COTS integrated circuits. For a long time, that wasn't that big of a deal because most applications are terrestrial rather than up in the air. We have the atmosphere protecting us, and in this particular presentation, what the folks from Europe showed was an aircraft was transiting the South Atlantic Anomaly.

The South Atlantic Anomaly is an area on the earth's surface where the level of cosmic radiation is quite a bit higher, and it has to do with how the Van Allen belt twists. The Van Allen belt is this ionizing belt that shields and screens earth from cosmic radiation. There's a small twist to the belt, and the South Atlantic just off the coast of Brazil has a much higher total of ionizing radiation nodes than any place else on the surface of the planet. There was an airplane that was transiting through that area, and there was a disruption in the flight control system; thankfully, they were able to recover, and the only thing that happened was some overhead bins popped. This is another area that people are becoming increasingly concerned about. As those geometries in processors and memories shrink, they become more susceptible to those single events.

Happy Holden: I'm surprised with the number of Army, Navy, and military contractors that have shown up at our meetings, including SpaceX and a few others, that are having failures and aren't sure what's caused them. That's why we're having this workshop today. Has anybody contacted you on the failure problem we're having with microvias and stacked vias?

Brown: Our Sherlock software does an excellent job of modeling those properties of the microvias. What we're seeing both in reliability failure analyses and cross-sectioning after failure is if the construction of the microvia configuration is done correctly, those microvia feedthroughs can actually be more reliable than a plated via for plated through-holes.

Holden: That's what we expect, but we're not getting that.

Brown: What we see in the modeling and laboratory is that when people stack up microvias, they can actually be less reliable than plated through-holes. The kind of design configuration that seems to work better is one where if you have to go a long distance through a board, you go a little way, shoot over on the internal layer, go down a little bit, and shoot over through another spot. As I mentioned earlier, these material configurations in today's boards are extremely complex structures. They have all of those different properties of polymers and metals and things like that, so yes, you can model the behavior of those microvias and then see what kinds of failures are anticipated.

When we initially tried to validate this reliability physics package about 10 years ago, we had some struggles with that validation process. We wanted a high correlation between what the model was showing and what we could demonstrate either in the field or laboratory with temperature cycling or shock vibration. What we discovered was that the material properties of the polymers, for example, in the prepreg and laminates in the board, weren't precisely per the manufacturer's datasheets. There were changes in the modulus of elasticity, in the X, Y, Z, and coefficient of thermal expansion (CTE) that didn't match up exactly with the manufacturer's datasheets. When we were going through the validation phase, part of the software development process was to match up those real-world physical constants with the way that they really play out inside board structures, rather than what's on the datasheet for just a polymer layer.

Holden: Nobody has gone to DfR yet with this because we think we have a containment process, so if the coupons pass, they'll assemble the boards, but we haven't figured out how to find the root cause. As many as 40% of the boards are being returned. They're failing the containment process, which is expensive for the fabricator and for schedules and timelines. We have dozens of theories about why it is, but no real hard evidence.

Matties: Thanks for your time today, Dock. Is there anything that we haven't talked about that you feel we should share with the industry?

Brown: One of the things that I would like to see a broader spreading of the knowledge that engineering is as much as art as it is a science, which is one of the things I talk about in my design for excellence classes at both SMTAI and IPC APEX EXPO. Part of engineering being an art means that as engineers, we are called upon to develop good intuitions as well as good analytical programs. Analyses and computer simulations are expensive. You can't analyze everything, so the art part of that comes in knowing when to deploy more expensive modeling techniques, and when you can allow your intuition to take place.

Back to the example of automotive; for instance, there were design rules that people of various industries applied in the old days. The origin of those design rules for temperature cycling was a relatively smooth diurnal day-night cycle where things gradually heat up in the morning, get hot around 4:00 p.m., and cool off at night. The next morning, you go through that same thing in a gentle once-a-day diurnal cycle. What some of the people in automotive are now discovering is that infotainment products that are in the cabin of the automobile are seeing temperature cycling profiles that are dramatically different.

Let's say you live in Phoenix, Arizona. You grab the kids in the morning and take them to school. Then, you pick them up, take them out to the soccer game, park the car in the sun, and when the soccer game is over, you turn the air conditioning up full blast and drive them off to an ice cream place. You take them in for some ice cream and a hamburger while the car sits in the sun and gets all hot. You come back out, throw on the AC on full blast again, drive to the grocery store—you see where I'm going with this.

There's no longer a gentle one-per-day cycle; The cycles occur at an extremely rapid rate with multiple cycles—four, five, six, or seven—per day for the electronics inside the cabin of an automobile. It's not a smooth ramp rate; it's very jagged, which exercises the solder joints even more. What we've been able to show in our modeling work is that modest changes in the X and Y CTEs of the circuit board—for example, going from a 16 to a 13—can double the life of solder joints for certain BGA parts.

Holden: Would you call this intuition a skill?

Brown: It's to be aware that your intuition, for example, would realize that a modest change in X, Y, and CTE of a board wouldn't make all that much a difference in the life of a solder joint. In fact, it makes two times the difference. For an infotainment automobile manufacturer, that could mean the difference between meeting the requirements of the top automotive customer and failing.

Holden: I'm interested in the essential skills that you have to develop after college, or the things that they don't teach you in college but are still essential. If we step back into something more basic, how would you define the skill of intuition of the artistic part of engineering?

Brown: I'll leave you with this final thought, which is rules versus tools. In the old days, we had design rules. We had a separate set of design rules for medical, avionics, industrial, automotive, and consumer products. Those worked very well when the change of pace was more sedate; today, with shrinking geometries and shorter development lifetimes, we need to make the transition from rules to tools. There's a variety of tools out there—our Sherlock reliability physics modeling software is only one—but it's up to design engineers to know what rule and tool to apply under different circumstances.

Holden: I think I've found another skill—rules versus tools.

Matties: Thank you so much for spending time sharing your wisdom with us, Dock. We greatly appreciate that.

Brown: My pleasure. **DESIGN007**

New Designer: The Best Advice I Have Been Given

by Barry Matties, I-CONNECT007

At the recent AltiumLive event, we had a chance to meet a few of the young designers of our industry. While we spent time asking some of the seasoned designers what advice they would give to a young designer, I took a few minutes to ask Tyler Middleton, a young designer working at Lyft, what advice has he been given that has been the best or most helpful so far. Here's what Tyler had to say.

"I'm fairly new to the industry, but in the time I've been here, I've had a lot of people tell me to collaborate," said Middleton. "Collaborate, collaborate, collaborate–work with fabricators, mechanical engineers, etc. I'm still new, but I try to do that as well as I can. It's useful advice."

PCB Designers: What You Do Matters

Tim's Takeaways

Feature Column by Tim Haag, CONSULTANT

Her name is Nonny. She has this name because that is what my oldest boy named her when he first began to talk. All of his brothers followed suit, then the extended family, neighborhood, and kids at the school where she worked. Eventually, everyone on social media also called her Nonny. To tell you the truth, I'm not sure that most people even know her real name anymore.

I, on the other hand, call her Mom. She isn't actually my birth mother; she is my wife's mother and my mother-in-law. When my mother passed away many years ago, I was looking for someone to fill the position. Times being what they were, Nonny took the job and now I call her Mom. I'm a little surprised that she agreed to the whole "Mom" thing because like a lot of mother's dealing with the boys (I mean, men) who marry their daughters, she was a little wary of me at first.

It didn't help matters much when on a trip to Disneyland, I laughed really loudly as one of the ride operators on the Jungle Cruise said, "Tuesdays are mothers-in-law's day, half fare for halfway—no questions asked." The bad thing was later on that same trip I did start to drive off, stranding her while she was still outside of the car. I didn't realize she wasn't in the car and it was an honest mistake on my part, although I'm not sure if she believes me. When it comes to that particular memory, my wife laughs, I cringe, and Mom glares at me.

All kidding aside, Mom and I have a great relationship. But something new has happened, and it's pretty serious. A little over a month ago, Mom was diagnosed with lung cancer and within a couple of weeks, started full treatment for it. She has moved in with us temporarily so that we can take her to chemotherapy and radiation treatments as well as care for her. In a moment of incredible timing, this *Design007 Magazine* is highlighting PCB design in medical applications this month. If you are thinking that I might have a few things to say along those lines, you would be right!

Most PCB designers do not have the opportunity in their everyday lives to use the final results of their efforts outside of the workplace. This makes a lot of sense when you think about some of the things that we design. For example, missile guidance systems are not intended to be played with casually, or if you do, you probably shouldn't tell anyone about it. I've been lucky enough to have designed a few things that I have been able to use in my everyday life, like computers and data or video projectors. However, those are the exceptions because most of my designs have been for devices that are entirely out of the norm for everyday life. This kind of detached relationship with work has made me a little lackadaisical towards electronics until cancer came along and I suddenly realized how much we all rely on modern electronics.

Here are some of the things that I've recently become very grateful for:

- **Computers:** Yes, like you, I've used computers for many years, and they are pretty commonplace, but now I'm using my computer to research medical procedures and definitions. I'm also working online with clinics to schedule and track various things in spreadsheets and documents.
- **Entertainment:** We bought Mom a tablet so she can keep in touch with her friends on social media and play games. This allows her to relax in her comfortable chair instead of always having to move to where the computer is set up.
- **Smart home devices and IoT:** What started as a fun hobby has become more important as we now have devices set up as intercoms and voice-activated lighting to assist Mom when needed.
- **Home medical devices:** Has anyone shaken a mercury thermometer or pumped a manual blood pressure cuff lately? Neither have I since we've gained the modern electronic versions of these tools.
- **Professional medical devices:** Whether it is the mechanisms for preparing and injecting the chemotherapy medication, the diagnostic machines that tell the doctors what is happening with Mom, or the radiation delivery system that administers her treatments, the electronics in the medical machinery working to heal her is impressive.

As I write this, Mom is still undergoing radiation treatments. She is being cared for by Dr. Lanceford Chong and the amazing staff at Radiation Oncology Care at Meridian Park Hospital. It has been a pleasure to work with these people, and they were kind enough to give me permission to snap a picture of the machine that is at the heart of these radiation treatments for Mom (Figure 1). I must confess,

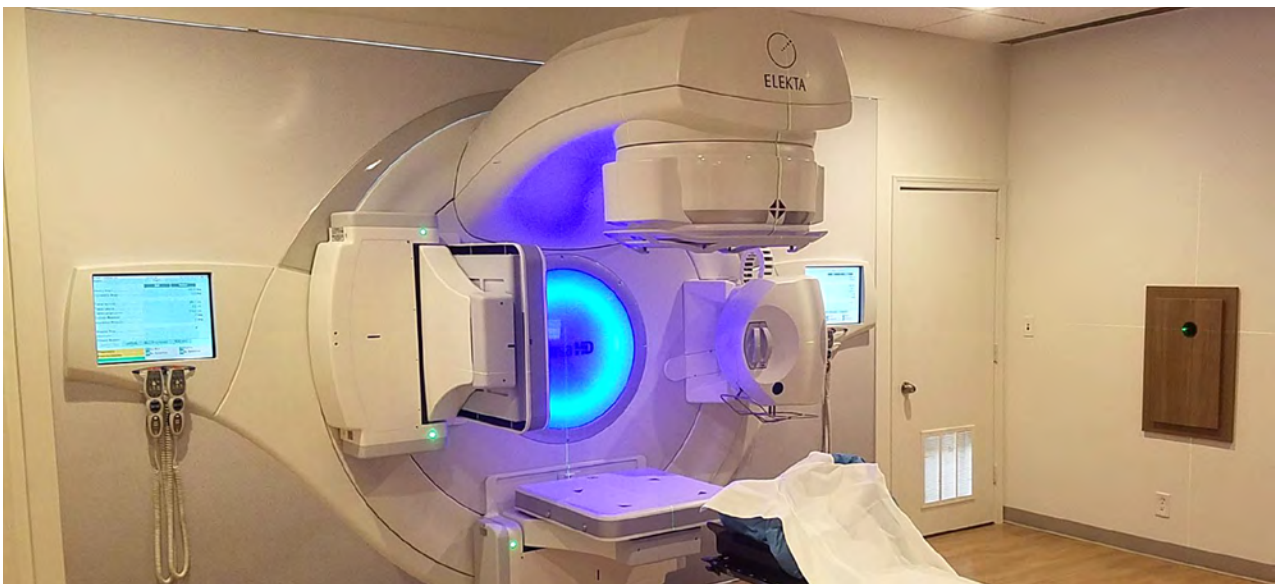


Figure 1: Radiation treatment equipment has come a long way over the years.

the idea of radiation treatment intimidated me at first with all kinds of mental images of science fiction scenarios that didn't end well. However, these are wonderful people in a professional facility using state-of-the-art technology to heal their patients, and my family and I are incredibly grateful to them.

Radiation therapy has been around for over a hundred years in one form or another, but it wasn't until the late 1970s when computers were first used to help with the controllability of the treatment. This opened up a new era in the history of radiation therapy [1], and it meant that there needed to be a lot more electronic design to accompany it. Just looking at that machine made me want to peek inside to see what kind of technology it held, but I don't think that the staff would have been too happy if I started poking around with a screwdriver and a pair of pliers.

As PCB designers, many of us have done work in the medical field. Many years ago, I worked on some of the first wearable devices for measuring your pulse rate, and the technology has grown far beyond that since then. Some of you are working on flex designs that put different sensors and treatment dispensers into wearable devices that merge medical and IoT technologies. Others of you are working on high-speed and HDI designs that are used in computer electronics for medical equipment. There's also the circuitry for high-power applications and everything else that goes into making a complicated machine, such as a radiotherapy treatment delivery system.

Fortunately, designers now have the tools to design the next level of technology needed for the medical field. PCB design systems today are well equipped to handle the needs of everything from small flex circuits to large multilayer HDI designs. There are a lot of people who did tons of work to create these electronic medical wonders. I am truly in awe about how much design has been done by many individuals over time that has filtered down to our little corner of the world, and I cannot tell you how happy I am to see the reality of PCB design in the real world helping Mom to beat cancer. It doesn't get any more real than that.

All of this has left me with a couple of thoughts. The first one is this: perhaps what you are designing isn't in the medical field, but chances are that it will help someone, somewhere, somehow. To put it simply, what you do matters. At times, it may seem that all of the colored circles and lines of a PCB design on your computer screen have less relevance in life than the latest zombie apocalypse video game, but don't listen to those voices of doubt in your head. Trust me when I say that what you do matters, so keep doing it—we all need you.

The second thought is that there is more to life than our work. During this difficult time, we have been supported by the help of our neighbors and the love of our family and friends. Our bosses have worked with us to help us manage our work schedules with doctor appointments, and our co-workers have supported us where they can. Many others have come together and even brought us food. You all are amazing people. Thank you. I think Editor Andy Shaughnessy summed it up well when he encouraged me, "Take care of what you have to do. The circuit boards will still be there."

Those are my thoughts, and as always, fight the good fight and keep designing. As for me, it's time to turn out the lights and get some sleep. Oh wait, that's not a light, that's just Mom softly glowing from the radiation in the other room. In case you were wondering, she will read this and probably throw something at me. I'm going to start running now. **DESIGN007**

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1. S. Gianfaldoni, R. Gianfaldoni, U. Wollina, J. Lotti, G. Tchernev, & T. Lotti. "An Overview of Radiotherapy: From Its History to Its Current Applications in Dermatology." U.S. National Library of Medicine National Institutes of Health, 2017.

Tim Haag is a PCB design consultant based in Portland, Oregon. To read past columns or contact Haag, click here.

Tamara Jovanovic

New Grad Designs PCBs for Smart Baby Beds

Feature Interview by Andy Shaughnessy
I-CONNECT007

The best ideas in the electronics industry improve the quality of our lives. At AltiumLive, I ran into Tamara Jovanovic, a new PCB designer and junior electrical engineer with Happiest Baby, a Los Angeles-based company that makes smart beds that can protect babies from crib death. After joking that I save the world from dangling participles while she's saving babies, I asked Tamara to tell us more about smart baby beds, and how she got into PCB design in the first place.

Andy Shaughnessy: Tamara, you are a brand-new designer and a freshly minted EE. How did you wind up being a circuit board designer?

Tamara Jovanovic: I went to college at Loyola Marymount University in Los Angeles, and I just graduated in May. I was looking for a job and was lucky enough to get an interview with Happiest Baby. I'd heard of them before, and I know about their CEO, Dr. Harvey Karp, who is amazing. He's a very famous pediatrician, and I guess they liked me during the interview so here I am.

Shaughnessy: Do you have an EE degree?

Jovanovic: Yes, I graduated in electrical engineering with a minor in applied math. I was a rower in college too, so I did rowing and engineering. It was an interesting four years, but it was worth it.

Shaughnessy: When you were in school, did you know that you wanted to be a circuit board designer? If not, what was your original plan?

Jovanovic: The plan was to study electrical engineering. I am actually from Serbia, so I only came here four years ago when I was 18. I didn't know anything about PCBs until my junior year of college. I wish my school offered more courses on it, but they don't. I started getting into it a little bit on my own. Once I got my job, it's something that they expected me to do, so I have to get better at it.

Shaughnessy: Does your company use Altium tools?

Jovanovic: Exactly, we use their tools to design and evaluate PCBs for our products.

Shaughnessy: Your company makes safe baby beds that keep infants from having SIDS and problems like that?

Jovanovic: Yes. At Happiest Baby, we make a bassinet called the Snoo; it's a smart baby bed, which moves on its own and produces white noise sounds that soothe the baby on its own. We like to say that we're the safest baby bed out there because the infant is swaddled and clipped in; only then, can the Snoo turn on and start moving. There is no accidental rolling or suffocation, God forbid. It's very safe and is basically an extra set of hands for the parents because they can leave the baby in it without having to be attached while taking a shower or making a meal.

Shaughnessy: You're helping protect babies and doing good things for the world. That's great.

Jovanovic: We're trying, slowly. It's beautiful, and we're not just helping babies—we're also helping the parents. Everyone who's had a newborn in the house before knows it's hard with the sleep schedule; babies don't sleep like we do. With the Snoo, we actually give the parents more rest as well. Some studies show that if an exhausted parent drives, it's almost similar to drunk driving, so if the parent can sleep at night while the baby's asleep in the Snoo, we are helping the parent as well.

Shaughnessy: So you've been designing for a couple of months now, is that right?

Jovanovic: I haven't gotten into it solidly, but I'm hoping that this event will deepen my knowledge and widen my horizons within the industry, which will set me up for the future.

Shaughnessy: You're starting at a good time. I don't know if you've seen our magazine or not, but we had an issue a couple of months ago about who's going to fill the shoes of the designers. Many designers in North America are retiring or preparing to retire within the next 10 years, so we need new designers like you. If you want to do this job for 40 years, you probably can.

Jovanovic: That's good to know. Someone in my lecture said the same thing today, and it's not so much that it reassures me, but engineering is my passion, and I've always liked science a lot; hopefully, this is something that I can do for a long time.

Shaughnessy: It's great to meet you. I'm always glad to see young people because we need a lot more in this industry.

Jovanovic: At first, it was hard having minimal experience during my internships. I had practically no experience with circuit board design in general—just engineering. I'm glad to be here and meet all these awesome people. I'm excited.

Shaughnessy: It's good to be in a company that will pay for your training too—a lot of companies don't do that. If you're in a company that doesn't send you to training, it's still up to you to keep going. You have to take care of yourself and your education.

Jovanovic: Definitely. I'm in a great company. I love where I am. I appreciate the fact that they sent me here. I want to show them that I can do this and that I'm worthy of the job; hopefully, they will see that one day.

Shaughnessy: I'm sure you'll do fine. Thanks for speaking with me tonight, Tamara.

Jovanovic: Thank you. DESIGN007

Internet of Body: The Next Big Thing for Medical

Feature Interview by Nolan Johnson
I-CONNECT007

During SMTA International, I sat down for an interview with Titu Botos, Ph.D., the VP of engineering at NeuronicWorks. We discuss the next big thing to come after the Internet of Things (IoT), which Titu believes is the Internet of Body (IoB). IoB could include implantables and ingestible medical devices to monitor your body better. Overall, it's a great time for medical electronics.

Nolan Johnson: I'm here with Titu Botos from NeuronicWorks in North York, Canada. Where is North York?

Titu Botos: It's about 14–20 kilometers away from downtown Toronto.

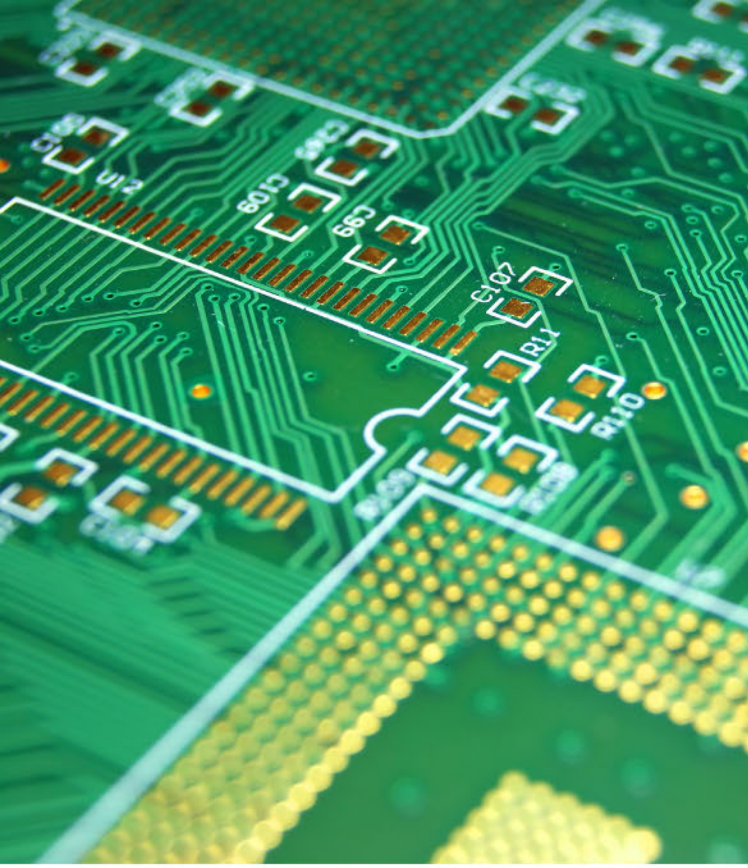
Johnson: Let's start with a quick overview of what NeuronicWorks does for its customers.

Botos: We're an engineering house and a design shop. We take an idea and bring it to life. When a customer comes to us, they leave functional products as well as blueprints for manufacturing; we call that the "cookbook." Although we strive to help them after that for the manufacturing itself, they are fit to go anywhere they want to. In other words, our business model is that when everything is said and done, they have the intellectual property (IP); they can do with the IP whatever and wherever they please. That's our business model.

Johnson: And they can go from an idea or a concept all the way through the engineering methodologies for all of the pieces to a finished product, or they can manufacture where they want.

Botos: Yes. We have in-house design for PCB electronics, firmware—which is low-level software—and high-level software from the cloud. We complement these three main skills with industrial, graphical, and mechanical design. On the other side, we have apps, the Internet, and the cloud. All of that comes under one roof, and we are able to serve the customer fully. We call those "full-house" projects.

Johnson: What are some of the industries that you serve with these design services?



Titu Botos

Botos: We started 10 years ago from an industrial control background surrounding any type of motors—valves, pressure, temperature, etc. We do not use a programmable logic controller (PLC), but we can design a PLC and do the electronics and the firmware for a controller to make it work. After starting this way, we expanded into a few automotive projects, and medical more recently, which means another set of troubles and challenges.

Besides these three main paths, we are very interested in wearables, which you might call our fourth industry. I believe it's the next big thing to come because on the industrial side right now—even automotive and medical—we ride the IoT wave where everything gets connected. Every node brings data into the cloud. We have a collection of information that we can peruse, digest, and make a decision based on.

This is the current trend, and I hope we can still ride that wave for a while. However, it will die down, like anything else, because everything has a beginning and an end. After IoT goes down, I hope IoB will come up and propel us forward further. IoB is a similar concept to IoT, but right now, we have a sensor attached to the body of the person, which will be the new wave. First, it was the PC, and then it was cellular, dot com, etc. Now it's IoT. What's the next trend? We think it will be IoB.

Johnson: Do you have customers coming to you with IoT projects at this point?

Botos: IoT is the thing now, and it's huge. We have project after project going into the cloud right now. There are two types of customers: startups that want to make the next little gadget that collects some data, and then other types of enterprises and businesses that have been established for years that do pumps or controls, but were never in or reported to the cloud before.

There is a shift in the business. Customers try to change their positioning so that they charge for the service as much as possible. For example, for reading temperature or pressure, they may even think to give a sensor, including the transducer, electronics, Bluetooth, or Wi-Fi. All of those options can be used for free and guaranteed to work for five years, but every time anyone accesses your pressure, you come to our cloud or web portal and are charged 0.00 something. With IoT, everything is connected to the cloud. It's a huge amount of data that can be used afterward to find trends and convey messages to see what happens.

Johnson: How do you see IoB and medical merging in the future?

Botos: They are very closely related because they all touch the body. IoB and medical sense what happened to the body—primary signals. They pull up signals and send what happens to the body, such as heart rate.

For me, IoB is beyond wearables like the Fitbit. All due respect for Fitbit—there is nothing wrong with them—but there are many other medical devices right now that get attached to your wrist or placed in your ear that can tell you things besides the heartbeat. Some wearables can even tell you about your stress level. Right now, my stress level might be off the chart, but it's going there because by analyzing the signals the body puts out, you are able to infer quite a few things.

I believe the two niche markets that will go first into IoB are kids and seniors—the two extremes. For example, I'd be very happy to see what my mom is doing right now. She's back home in Romania. Yes, I talk to her every second or third day, but it would be interesting to know, "Did she fall? What is her heart rate? How is her well-being?" If you can characterize that in a word, it would be the signals. I believe seniors might want to take it because, for example, I tried to convince her to have such a device to see what happens.

The second one is the kids. I like to know what my monkeys are doing and if they are fine. The problem with this thing is that it opens a new era of privacy. It's a new meaning because you can be hacked. Two weeks ago, there was a Bloomberg Businessweek magazine story with what happened to Apple and Amazon, and that's another story. Now we are overwhelmed because somebody can find these things out about you. If not for bad reasons—for lack of better words—then for life insurance. You have your whole life in a data center somewhere.

There is still time until this becomes a reality. I'm still concerned about my privacy. I'm not doing anything special or wrong, but I'm still concerned. If I look at my daughters, they don't care; they post everything everywhere—it doesn't matter. With this approach, if you give it to kids first, they will grow up and, as adults, will say, "Sure. I'd like to know what happened to my heartbeat in the last 24 hours." It's another approach.

Johnson: Not only do we have the possibility of invasiveness around data privacy, but IoB starts to touch on a number of different ways of connecting to the body.

Botos: IoB would become successful the moment you forget you have that attachment. Today, it's still bulky. You still have to put it on, pull it off at night, and eventually charge it. That is still a threshold that many people have to go above or surpass to accept the technology. The moment it touched your skin, like a sticker, you could forget about it. You could have it there for weeks, months, or even more, and you wouldn't have to do anything. You could shower and maybe even swim. That will be a true application for IoB.

Johnson: Do you see IoB moving into implantables?

Botos: Yes. It's already there.

Johnson: I could easily see a pacemaker doing something like that or an implantable blood sugar monitor.

Botos: Yes. The other class I was talking about besides patches is implantables. I saw it last year at the Wearable Technologies Conference in San Francisco where you could have a glass-based encapsulated pill if you want. It's a near-field communication (NFC) tag that you put under your skin, and from that moment, you can start paying with your hand. You can identify yourself to a tag or a door: "Yes, I am Titu. Here I am." That's a completely different class. It has a higher class in the medical industry because it has to survive inside your body and should have as little of an effect on your body as possible. The first implant I saw was encapsulated in medical-grade sterile glass.

The other class of IoB devices would be the ingestible ones. You swallow it as a pill, and it has two purposes. First, it's sensor-based as in it goes, stays in your body for about 24 hours or so, and it collects data as it travels through your digestive tract. You have a receiver on your body somewhere very close because the energy is low like a patch. It transmits that, and when it goes out, it's basically disposable.

The other scope for this digestible would be to deliver drugs to the right place. Yes, invasively entering the bloodstream is one way—the old way; for example, with something like insulin, we cannot have it as a pill. There have been hundreds of trials where they try to convert insulin into a pill so you can take a pill instead of taking a shot every time you need it.

It's much easier to swallow, but it's proven that the digestive tract is breaking the insulin into pieces, so that is not the drug anymore.

The point is to have a vehicle that will deliver that insulin intact, so it can do what it was meant to do. That would help, but recognize that it's a third class. We hope blind people will start to see one day. We have a project in our labs, but it's still far away from taking somebody from the street and having them regain their vision the next day—that day is still very, very far off.

We have a project in our labs, but it's still far away from taking somebody from the street and having them regain their vision the next day—that day is still very, very far off.

Johnson: What are some of your customers' biggest challenges regarding FDA approvals? Do you have any advice for design teams looking at starting to do a medical device around this technology?

Botos: Go with a team that has been doing that for a while because there are a few hoops you have to jump through that can be costly if you don't know how to approach them.

Johnson: Give me an example.

Botos: All the specifications, for instance. I'm hard-pressed to give all the details for a test now, but to satisfy something for the Federal Communications Commission (FCC) and industrial control is one thing. To do medical—something that touches the body or goes in the body of a patient—is a totally different ballgame. Choose the right horse, so to speak. You need time, money, and patience because it doesn't happen by applying today and getting an approval the next month. No—it's months and months of pushing, providing data, doing tests, and answering questions because this is the part where we come in again because we can shield the customer for most of it.

A medical device is not developed in three days either—you need months to do that. By the end of working with the customer, we know the product inside as well as the customer if not even better, if I dare say. We want to be able to answer questions when the officers come. We can let the customer know what we did so they don't have to bother with, "Give me all the details this component has. What are the materials?" We have all that prepared. In the end, the specification stays with the customers. We are there for support and to make life a bit easier while going through that process.

Johnson: When you're developing a medical device for a customer, how soon are you bringing the FDA into the process on the design?

Botos: That's a great question. After a few projects, we have a little experience, and we don't have to bring it in as soon as the system design. However, as soon as we start to choose components and technology, then you should have somebody on your side looking over your shoulder and guiding you through the process. It would be a pity to arrive six months or a year and a half later to discover that the device will work but it's a nightmare to get it certified.

Johnson: When you're starting to make the design and component selections, is that when you're also starting to talk to the FDA?

Botos: When we do the system design and choose the technology that you think you are going to employ in a project, that's the best time because that's the moment you choose your future.

Johnson: There's also been a lot of discussion about supply chain issues with some long lead times for components, especially passives. Is your team facing challenges coming up with the right kinds of parts?

Botos: Yes. Oddly enough, there is a Chinese saying that goes something like this: "May you live interesting times." This is what we are doing right now. It started in 2001–2002 when manufacturing jobs left North America and went offshore; it became a big challenge. Then, design jobs are going somewhere far; that's another level of challenges. Now, jobs are coming back for multiple reasons: getting lost in translation, and a shortage of components.

You have to prove to your customer that you understand them, are on the same page, and are speaking the same language, for lack of a better word. By that, I don't mean English, but you understand fully what they mean. When they say green, it's green, and when it's yellow, it's yellow. I feel that's very important.

Prove to them that you can control the source of the components you choose. You know exactly where they're coming from and the quality and you can provide those components. The big challenge that we have seen in the last year or so is with automotive electronics because cars are crazy right now. Five or 10 years ago, you had around 40 processors in a car. Today, I don't even know; there are so many. As I said, IoT is coming. Even now, portable toilets have sensors. Sensors and electronics are everywhere.

The huge demand on the components is a strain on manufacturers. The big picture is the manufacturers want to speak with Apple, Amazon, IBM, and other big guys. When startup customers come to talk to us, one of the advantages we bring to the table is that we know where to talk, how to get the components, and we give them a view and bill of materials (BOM). This shows we did our homework and the component is available and in the right point on its lifecycle.

To answer your question, it's very important to make sure that after a year and a half of development, you have a BOM that can be replicated again for the next 15 years. There are customers—especially medical and even industrial and automotive—who are fine with developing a new version eventually (a better product), but they're not okay with redesigning the product next year because a component is obsolete. That's an entirely different thing.

We face the challenge of making sure that you know that the component is coming; industrial is one level of quality, automotive is another, and environmental is even more stressful. Medical is one step above that. You have to make sure the component is correct, has the right materials inside, and can last for 15 years. If I design it well in that environment, it will last 10–15 years. That's a requirement.

Then, do we have that component? Can we make sure the component will be available for manufacturing? We are moving as a company into thousands of pieces with continuous growth, and our projects now are manufactured in hundreds of thousands of pieces. For that, the supply chain has to be very well established.

I appreciate our connections with Avnet, Arrow, and Fisher Electronics. Those are the guys who are helping us. They can vet the BOM we propose and say, "Yes, this is the thing you can use today and in five years," and provide all of the components.

Johnson: Fantastic. This has been helpful. Is there anything else that we should talk about before we wrap it up?

Botos: Everything is very interesting and becoming increasingly challenging. There are still projects where you have to drive an LED on and off or blink it or dim it, but most of it is going very small. As I said, IoB has to be very small to be successful—that's the bottom line. The pairing of IoB and IoT with artificial intelligence is another thing entirely. What is a human anymore? That's a good question to ask at one point. One problem is we have less time for each other, but we try to do more things. A doctor can reach 1,000 or 10,000 patients, but an engineer of a product can touch millions. This is a great job.

Johnson: Thank you for your time, Titu. I really appreciate it.

Botos: Thank you very much. It was my pleasure. **DESIGN007**

PCB007 Highlights

EPTE Newsletter: Taiwan Electronics are Heating Up (Figuratively) ▶

Dominique Numakura considers electronics manufacturing in Taiwan to be the barometer for the global consumer electronics industry. Market trends can be predicted by analyzing shipping data from Taiwanese circuit board manufacturers. Annual volume increases every year, despite slow monthly cycles.

Aspocomp Raises Outlook for Net Sales and Operating Result in 2018 ▶

Aspocomp Group Plc upgrades its outlook for full-year 2018 net sales and operating result. In 2018, net sales are expected to grow approximately 15% compared with 2017 and the operating result to be approximately EUR 2 million. In 2017, net sales amounted to EUR 23.9 million and the operating result to EUR 0.8 million.

Ventec at electronica 2018: No Compromises for High-Frequency Materials ▶

Ventec International Group will announce the launch of its extended ceramic-filled hydrocarbon thermoset material series designed for the world's most demanding high-frequency printed circuit board applications at this year's electronica show in Munich.

I-Connect007 Publishes Automation eBook by Happy Holden ▶

I-Connect007 is excited to announce the release of the latest title in our eBook library: *Automation and Advanced Procedures in PCB Fabrication.*

The Changing Shape of the HDI Market ▶

With more mobile device designers looking to utilize the benefits of FOWLP and other direct attach package types, a new generation of HDI PCBs is already in the market. Targeting less than 30 mm features and based on mSAP techniques, these substrate-like PCBs make use of the latest high-end manufacturing processes and materials, to enable the next evolution in advanced HDI boards.

It's Only Common Sense: What the Heck is an SEO? ▶

Have you ever wondered what it takes to get to the top of a Google page? Why do some companies always seem to have all the business they need even without any outside salespeople? It seems to be some kind of black magic. How do they do it? Read on.

IPC President Commends White House for Assessment of US Defense Industrial Base ▶

On behalf of the electronics industry, I commend the White House for the release today of a sweeping and detailed assessment of the nation's defense industrial base. The report reflects more than a year of painstaking data collection, sector by sector analysis, and industry engagement.

FPCB Market to Display Significant Growth by 2027 ▶

The demand for flexible printed circuit boards by manufacturers of smartphones, other mobile devices, LCD display, connectivity antennas, and rechargeable batteries, is currently on the rise. With exploding consumer electronics sector, soaring popularity of IoT, and growing applications in the automotive sector are identified to be the key factors that are likely to hold a positive impact on the sales of FPCBs in near future.

Chapter Roundup and CID+ Certification

The Digital Layout

by Steph Chavez, CIT, CID+, IPC DESIGNERS COUNCIL

This month's column will detail the proceedings from the most recent IPC Designers Council (DC) Executive Board meeting. You will find updates on local chapters—from the United States (spotlight on the Silicon Valley chapter) to Mexico, France, and Asia—educational opportunities, upcoming events, and one engineer's story to achieving CID+ certification.

Attendees

The IPC DC Executive Board meeting included local members and leaders and a variety of IPC course instructors representing chapters across the United States: Tony Cosentino, Randy Faucette, Mike Creeden (MIT), Scott McCurdy, Bob Griffith, Gary Ferrari (MIT) Rick Hartley, Bob McCreight, Susy Webb, Paul Fleming (CIT), Faisal Ahmed, and me.

Global Steering Committee

The global steering committee meetings were approved at the last IPC DC Executive Board meeting and formally began at the most recent meeting. The next meetings are scheduled for IPC APEX EXPO 2019, the third week in May, and PCB West. As mentioned in my last column, I was nominated and approved to chair a new communications committee comprised of representatives from each of the IPC DC chapters. The first order of business was to resurrect the council's newsletter with industry media companies to discuss chapter reports, events, and other related news.

During their fall meeting, the IPC Designers Council, Silicon Valley Chapter, toured Levi's Stadium.

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2 - 10 Layers Expedited Lead Time	24 Hours	48 Hours	24 Hours	-
12 - 24 Layers Expedited Lead Time	48 Hours	72 Hours	48 Hours	-
Filled Via in Pad Technology				
Standard Lead Time	15 Days	15 Days	15 Days	20 Days
Expedited Lead Time	2 - 3 Days	4 - 5 Days	2 - 3 Days	5 - 7 Days
HDI Technology				
2x Lam Cycles Standard Lead Time	15 Days	20 Days	20 Days	20 Days
2x Lam Cycles Expedited Lead Time	3 - 5 Days	5 Days	3 - 5 Days	10 Days
3x Lam Cycles Standard Lead Time	20 Days	20 Days	20 Days	-
3x Lam Cycles Expedited Lead Time	7 Days	10 Days	7 Days	-
4x Lam Cycles Standard Lead Time	25 Days	-	25 Days	-
4x Lam Cycles Expedited Lead Time	10 Days	-	10 Days	-

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Chapter Spotlight

by Bob McCreight
SILICON VALLEY CHAPTER PRESIDENT

The IPC Designers Council is an international network of designers. Its mission is to promote printed circuit board design as a profession and to encourage, facilitate, and promote the exchange of information and integration of new design concepts through communications, seminars, workshops, and professional certification through a network of local chapters.

This month's spotlight is the Silicon Valley Chapter. We held our fall quarterly meeting on October 25, 2018, at none other than Levi's Stadium in Santa Clara, California—yes, the site of Super Bowl 50 and the soon-to-be 2019 College Football Playoff National Championship game. This was made possible by our host, Sierra Circuits, and sponsor, Altium. We thank them both graciously. Out of 33 total RSVPs, 24 were able to attend the lunchtime meeting. Fun fact: of the members who RSVPed, six of them were CID certified and 10 were CID+ certified with Faisal Ahmed being the most recent (hear more from him later).

Amit Bahl


Amit Bahl

After addressing some chapter business, Amit Bahl, director of sales and marketing at Sierra Circuits, spoke about a newly patented process called CATLAM. Watch for a new term they are coining—trench circuit board (TCB). The secret sauce they are developing involves etching a trench in the PCB material and filling it with copper by an electroless process, for which there are numerous benefits.

Ben Jordan


Ben Jordan

Following that, we introduced Ben Jordan, director of community tools and content at Altium. He gave us a brief preview of Altium Designer 19. Not to give away too much right now, but library management has some really cool new features, some of which will leverage their Octopart extension.

For the main presentation, Ben gave an overview of multi-board design, which involves projects that have more than one PCB and are interconnected by either plug-in connectors, wire harnesses, or another method. Some of the examples Ben demonstrated were very cool, like his own guitar mixer box. One point that he stressed was to put plenty of thought into how you divide the boards up. For instance, the power supply can be on a simple two-sided board while the communications can be on a more complex multilayer board. Mixing them may have signal integrity consequences.

Following the conclusion of the meeting, the networking portion of the agenda was blended into a stadium tour. From our seventh-floor boardroom, we went up the elevator to the NRG Solar Terrace, or "Green Roof," where there is a thriving, sustainable garden that basks in the brilliant sunlight. From part of the terrace, you get a grand view of the field plus Silicon Valley and the southern San Francisco Bay Area, which you can also rent for events. Next, we visited the Verizon Press Level where all the media hangs out during game day action. We ended by visiting the field itself, including being able to look up at all the seating, lighting, and signage. It's a very nice stadium if I do say so myself. Too bad the home team is not doing so well this year (sad face).

Below is our tentative 2019 meeting schedule (exact dates may vary):

- January 24 sponsored by Mentor, a Siemens Company
- April 25 sponsored by Cadence Design Systems
- July 25 sponsored by Altium
- October 24 sponsored by Zuken

We are looking for great speakers so feel free to volunteer! Lastly, I'd like to extend many thanks to those who attended, Ben Jordan and Judy Warner from Altium, and Amit Bahl and his team at Sierra Circuits, including Lucy, Rachel, Bianca, and Joel.

Why CID+?

by Faisal Ahmed
CADENCE DESIGN SYSTEMS

A Silicon Valley DC Chapter member—Faisal Ahmed, lead application engineer at Cadence Design Systems—took the IPC CID+ course at PCB West 2018. He shares why he pursued IPC advanced designer certification, and his thoughts on successfully achieving CID+ status.


Faisal Ahmed

After 20 years of creating masterpieces of art with copper on glass resin, I decided to take on advanced designer certification (CID+). Many of my friends in the industry have asked, "Why so late and what did you achieve?"

The simple answer is that having my CID+ gives me the highest possible PCB design status in the industry. One recent survey found that two-thirds of PCB designers are 51–70 years of age; astoundingly, one-fourth are 41–51, which leaves me in the youngest 10% of designers. To my friends out there, I am not late, but don't worry if you fall in the top 90%. As George Eliot said, "It's never too late." It is to your advantage to get the certification when you really know the industry and are proficient with the PCB design flow. Unlike CID certification, which is designed for anyone at any level involved in developing, designing, fabricating, and producing PCBs—from sales to management, procurement, and quality—CID+ certification is designed for the advancement of the designer.

The process of reviewing PCB design from new product introduction (NPI) to the end product with the fear of being tested on the content helped me focus on the material and provided me with an enhanced learning experience. In product development, PCB designers are the liaison who converts electronic ideas into reality; therefore, it is critical for them to understand electronics and manufacturing.

Being a CID+ is the ultimate certification for a designer, and it certifies me to be an industry professional.

Chapter Updates

San Diego, California: Bob Griffith
- Status: Strong
- Regular attendees: 70–75
- Meetings per year: Five (four core meetings) during lunch
- Leaders: Six core executive chapter members
- Events: Host city to IPC APEX EXPO 2019

Orange County, California: Scott McCurdy
- Status: Strong
- Regular attendees: 45–70
- Meetings: Four during lunch
- Leaders: Four core executive chapter members
- Successes: Lunch meetings and diverse speakers

Silicon Valley, California: Bob McCreight
- Status: Active
- Regular attendees: 20–30
- Meetings per year: Four during lunch

Seattle, Washington (Cascade Chapter): Tim Mullin
- Status: Active

- Regular attendees: 8–14
- Meetings per year: Four during lunch
- Leaders: Five core executive chapter members
- Successes: New members being brought in through local CID/CID+ training; hopefully, this will continue with the formation of a new Altium user group following chapter meetings
- cascade-ipcdc.org

Phoenix, Arizona: Stephen Chavez and Paul Fleming
- Status: Dormant
- Leaders: Four core executive chapter members (seeking new leadership to take over)
- Meetings per year: None currently (but typically, four)

Research Triangle Park (RTP), North Carolina: Tony Cosentino and Randy Faucette
- Status: Strong
- Regular attendees: 30
- Meetings per year: Three to four during the evening
- Leaders: Nine core executive chapter members
- Events: Annual PCB Carolina event with 700–1,000 attendees

Monterrey, Mexico: Luis Saracho
- Status: Active
- Regular attendees: 8–12
- Meetings per year: Four during the evening with technical presentations
- sites.google.com/view/mtyipcdc/home

Design Council Chapter France (DCCF): Thomas Romont
- Status: Active
- Regular attendees: 34–60
- Successes: Professional presentations and workshops, design community surveys
- Events: February 2018 was the first DCCF conference in Paris (IPC Day Design)

Penang, Singapore, and Philippines Chapters: Cheah Soo Lan
- Status: Active
- Regular Attendance: 73 (Penang), 30 (Singapore), 14 (Philippines)
- Successes: CID and CID+ certifications
- Events: Plant visits (Singapore)

Education

New IPC Edge 2.0 Program
- Mandatory testing
- Required 80% to pass
- Must score 16 out of 20 or higher
- Must take the same test for each IPC certification

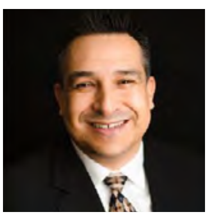
Upcoming Activities at a Glance

Two-day hands-on power integrity workshop: Steve Sandler
- December 3–4, 2018
- Santa Clara, California
- Registration: click here
- Contact Lucy Iantosca at Sierra Circuits for details

IPC APEX EXPO 2019
- January 26–31: Meetings and courses
- January 29–31: Conference and exhibition
- January 31–February 2: IPC Designer Certification CID/CID+
- San Diego, California
- ipcapexexpo.org

DesignCon 2019
- January 29–31
- Santa Clara, California
- designcon.com

Next month will cover the upcoming IPC APEX EXPO in late January and highlight the San Diego Chapter. DESIGN007



Steph Chavez is a member of the IPC Designers Council Executive Board and chairman of the communications subcommittee. To read past columns or contact Chavez, click here.

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10 Fundamental Rules of High-speed PCB Design, Part 3

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Figure 1: The 10 fundamental rules of high-speed PCB design.

Today's high-performance processors have fast rise times, low driver output impedance, and simultaneously switching of busses, which create high transient currents in the power and ground planes that degrade the performance and reliability of the product. Inadequate power delivery can exhibit intermittent signal integrity issues.

Continuing from my previous columns (Parts 1 and 2), I will elaborate on power distribution networks (PDNs) and define power planes and paths.

IV. Define the Power Delivery Planes and Paths:

Define the power/ground regions and plane layers. Partition (not split) the ground planes.

The power and ground planes in a high-speed, multilayer PCB perform six crucial functions:

1. Allow the routing of controlled impedance transmission lines in both microstrip and stripline configurations
2. Provide a reference voltage for the exchange of digital signals
3. Distribute stable power to all logic devices
4. Control crosstalk between switching signals
5. Provide planar capacitance to decouple high frequencies
6. Present a shield for electromagnetic radiation on internal layers

For these reasons, planes are essential in today's high-speed multilayer PCBs. Unfortunately, the number of power supplies required is increasing dramatically with IC complexity. Now, accounting for them all has become a real challenge. The high number of supplies generally leads to higher layer count substrates. In the past, we used to have more signal routing layers than planes; the opposite is now the case when the majority of stackup layers are reserved for power distribution. Although this increases the cost, it may be a godsend because it provides segregation of critical signals to avoid crosstalk and reduces radiation due to close coupling of signal traces to the reference planes.

In a recent complex design that I completed, I counted over 10 individual power supplies

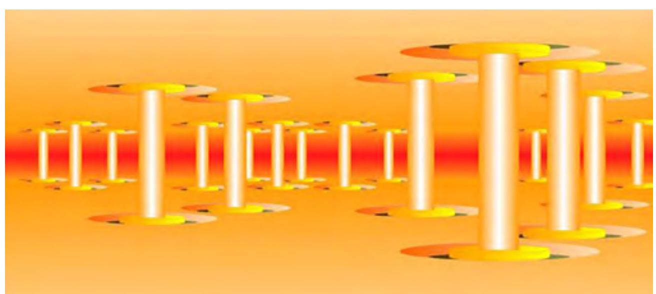


Figure 2: Enlarged 3D cross-sectional view of a plane cavity with a transparent core.

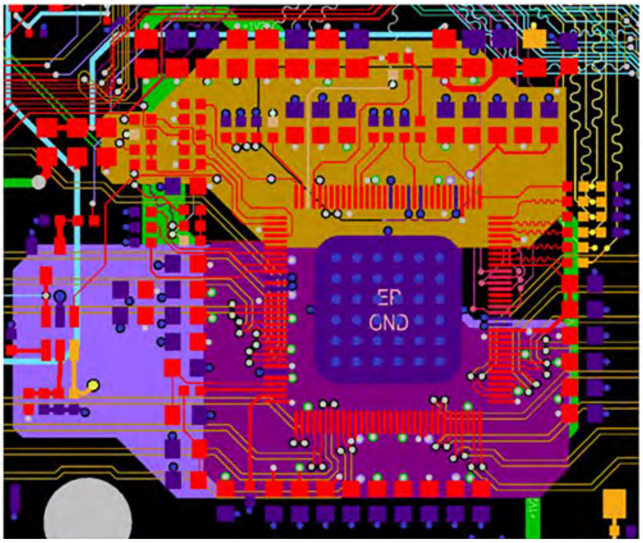


Figure 3: Supplies poured under an IC on multiple layers separated by ground planes.

ranging from the 5V input power to the board to 0.75V DDR3 VTT reference voltage. These supplies required six layers (including ground) of the 10-layer stackup, which left only four layers for signal routing.

The methodology I follow to define the planes is as follows. First, it is beneficial to define the power supply regions in conjunction with placement. Group all components by functionality and their common power supply. Second, work on the critical circuits first and ensure there is a contiguous ground plane on one side and the corresponding power plane on the other. This creates a minimum loop area and a low-inductance return current path. Third, segregate critical circuits with ground planes. For example, the top portion of a symmetrical stackup can be used for one circuit and the bottom for another.

Fourth, arrange the power regions so that they do not overlap on adjacent layers because coupling between different supplies can transfer plane noise. A ground plane in between power planes prevents this and also adds valuable planar capacitance. Next, keep the regions as square as possible because a long, rectangular shape plane can create rogue waves in the plane cavities. Lastly, ensure that no signal crosses a split in the ground plane into a different domain.

Power planes can be split into many different power areas (Figure 3). And since digital circuits are normally referenced to the same ground, there is no real need to split a ground plane. As mentioned in Part 2, route fences (keep-outs) can be used to control the routing and prevent signals from crossing over into different logic domains. Split ground planes create discontinuities of impedance, crosstalk, and EMI, and should not be used. Controlled routing is the key to a successful mixed-signal design. The ground planes should not be split; instead, they should be partitioned, and a pass-through gap should be left in the route keep-out so that control signals can enter and leave the sensitive areas.

V. Optimize the Power Distribution Networks (PDNs): Create a low AC impedance delivery path by optimizing the bypass and decoupling capacitors, and mount inductance and plane resonance from DC to the maximum required frequency (including harmonics).

The PDN must accommodate variances of switching current with as little change in power supply voltage as possible (a 5% voltage ripple is a typical requirement). The goal of PDN planning is to design a stable power source for all the required power supplies. Ideally, the effective impedance of the PDN should be kept as low as possible up to the maximum operating frequency.

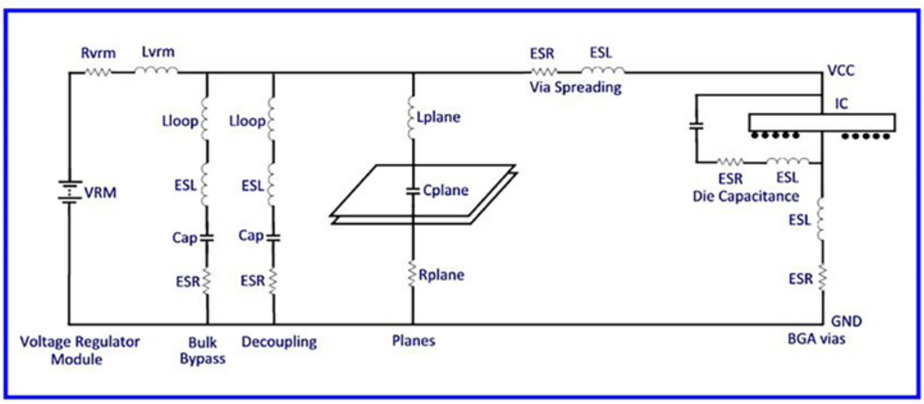


Figure 4: Typical PDN topology.

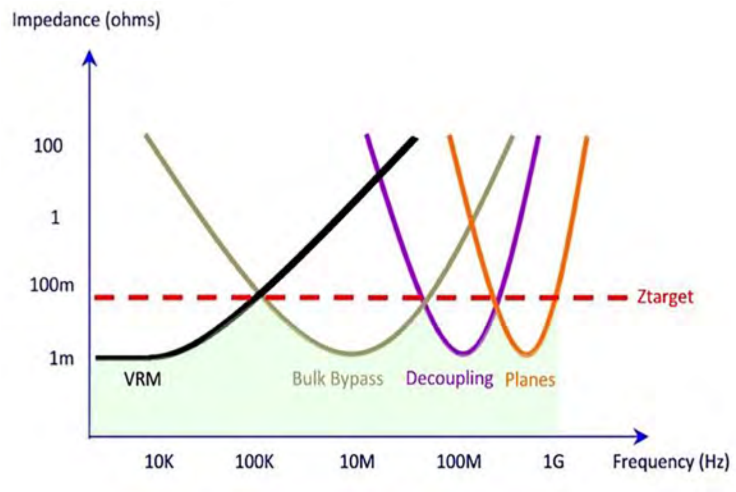


Figure 5: Target impedance, VRM, capacitor, and plane profiles of a PDN.

Figure 4 shows the topology of a typical PDN, which includes the voltage regulator module (VRM), bulk bypass and decoupling capacitors, plane, die capacitance, BGA via, and via spreading inductance. Each of these components has a specific resonant frequency where the impedance will be low. However, these components interact to create anti-resonance peaks that may occur at undesirable frequencies and wreak havoc on an otherwise stable supply.

The target impedance (Ztarget) of the PDN is the combination of the worst-case transient current and the voltage noise specification, which act together to set the maximum allowable PDN impedance with an assured performance. Target impedance is the most crucial metric when evaluating PDN performance. The further the PDN impedance is above the target impedance, the greater the risk of intermittent operation or even complete product failure.

Taking the VRM and planes into consideration, selected values of bypass and decoupling capacitors are added to the PDN to lower the impedance at a particular frequency (Figure 5). Capacitors reach their minimum impedance at their resonant frequency, which is determined by the capacitance, equivalent series resistance (ESR), and the equivalent series inductance (ESL) together with the mounting inductance. To meet the target impedance at a particular frequency, a capacitance value is chosen so that when mounted on the PCB, it will resonate at the desired frequency and have an impedance that is equal to its ESR. Then, a sufficient number of those capacitors are placed in parallel so that the combined parallel ESRs approach the desired target impedance.

As one can see from Figure 6, each value capacitor has a different resonant frequency depression. Thus, one would assume that by placing many different values of capacitors on the board, the entire frequency range would be covered or have minimal impedance from DC to maximum frequency. Unfortunately, it is not as simple as that.

Decoupling capacitors are only effective up to about 200 MHz; above that, only on-die capacitance or planar capacitance can reduce the PDN impedance significantly. In Figure 6, I used a thin core dielectric of 2.3 mils between the planes to lower the effective impedance at high frequency. This is relatively easy to accomplish with multiple plane layers in the stackup—another bonus! This strategy provides low impedance up to 1.58 GHz, in this case.

Providing a balance of capacitors selected at the right frequencies and combined with planar capacitance can lower the anti-resonance peaks to the target impedance up to the maximum operating frequency.

Key Points:

- The power and ground planes in a high-speed, multilayer PCB perform six crucial functions
- The high number of power supplies generally leads to higher layer count substrates
- These days, the majority of stackup layers of a complex design are reserved for power distribution
- Power planes can be split into many different power areas, but digital circuits are normally referenced to the same ground, so there is no real need to split a ground plane

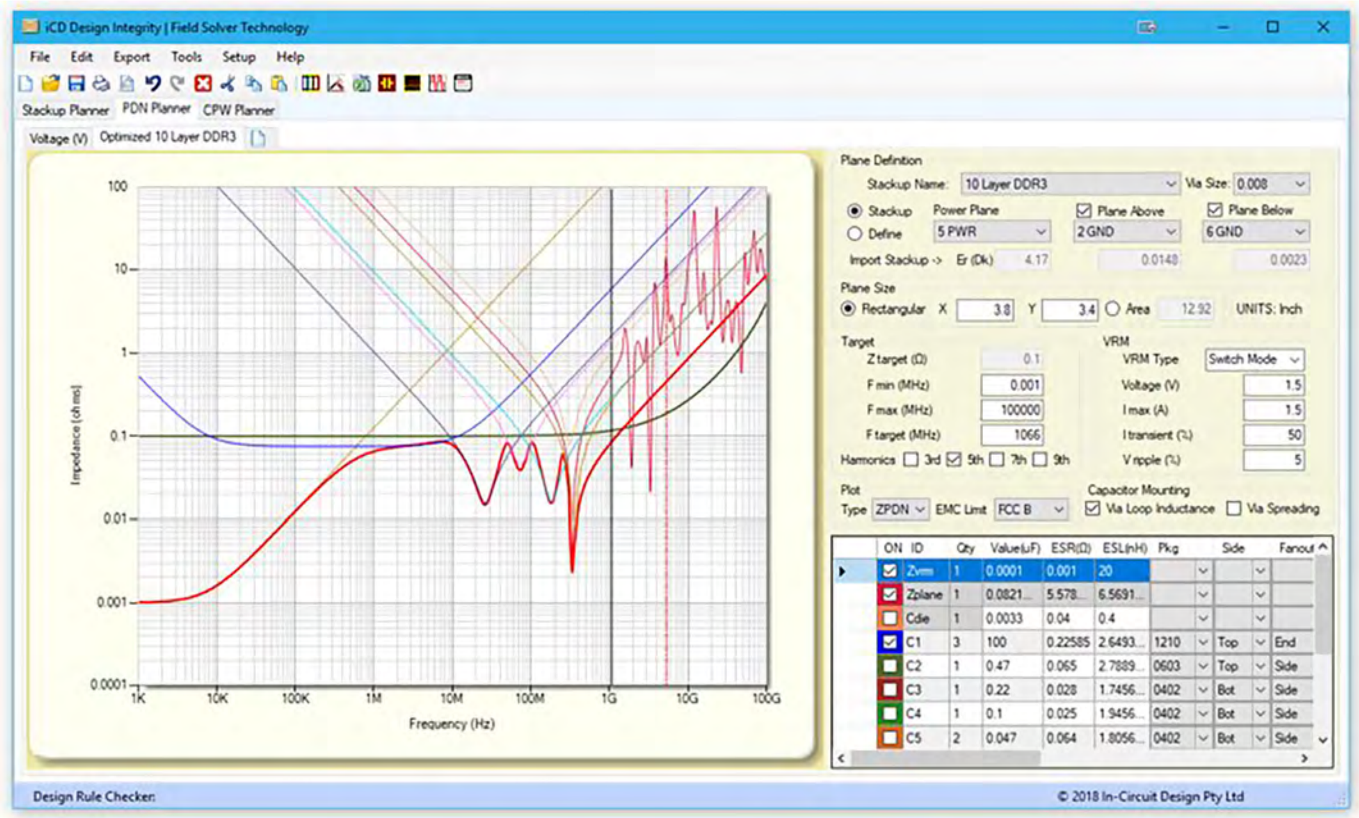
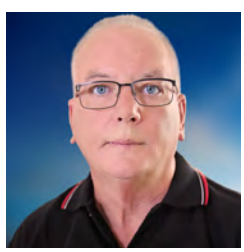


Figure 6: Optimized PDN for a 1066 MHz DDR3 (iCD PDN Planner).

- Split ground planes create discontinuities of impedance, crosstalk, and EMI, and should not be used
- The ground planes should not be split, but partitioned instead
- The goal of PDN planning is to design a stable power source for all the required power supplies
- Each component of the PDN has a specific resonant frequency where the impedance will be low
- PDN components interact to create anti-resonance peaks that may occur at undesirable frequencies
- The further the PDN impedance is above the target impedance, the greater the risk of intermittent operation or even complete product failure
- Decoupling capacitors are only effective up to about 200 MHz; above that, only on-die capacitance or planar capacitance can reduce the PDN impedance significantly

Further Reading

- Beyond Design: Power Distribution Network Planning by Barry Olney, *The PCB Magazine,* May 2012.
- Beyond Design: Plane Crazy, Part 1 by Barry Olney, *The PCB Design Magazine,* December 2015.
- Beyond Design: The Target Impedance Approach to PDN Design by Barry Olney, *Design007 Magazine,* February 2018.
- *High-Speed Digital Design: A Handbook of Black Magic, First Edition* by Howard Johnson and Martin Graham, Prentice Hall, 1993.



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded from www.icd.com.au. To read past columns or contact Olney, click here.

Embedding Components, Part 5:
Alternative Termination Methodologies and Surface Plating Variations

Designers Notebook
by **Vern Solberg**, CONSULTANT

Embedding discrete passive components in a multilayer PCB combines two process disciplines: PCB fabrication and SMT assembly. Locating a supplier with both capabilities may be a challenge; however, a growing number of PCB fabricators have installed SMT assembly capabilities, or they have partnered with a company already established to offer assembly services.

Because they are furnished with a very thin profile, resistor and capacitor components with different values can be mounted directly onto land patterns on a subsurface layer of the printed circuit structure. However, handling and placing of these small components requires systems with a high level of positional accuracy. Interconnection can be accomplished using either deposited solder paste and reflow processing or applying a conductive polymer material. Due to the extremely small land pattern geometries required for mounting the miniature passive components, companies commonly rely on precision dispensing these materials.

Component Attachment Site Preparation

Land patterns for embedded passive components—previously explained in Part 4 of this series—furnish geometries that maximize adhesion and ensure electrical interface between the terminals and lands of the components.

Key attributes for solder or conductive polymer process control include:

- Uniform surface planarity
- Minimal intermetallic propagation
- Inhibited surface oxidation

The surface finish on the passive component terminals and the land patterns provided on the substrate must enable a reliable electrical and mechanical interface.

Solder Processing

The alloy composition commonly furnished on discrete passive component terminals is tin (Ag) over nickel (Ni) base plating. AgNi-plated component terminals will be compatible with any one of the commercially available lead-free solder alloy compositions listed in Table 1.

Solder paste is essentially a fine metal alloy powder suspended in a thick flux medium. Flux

Solder Composition	Alloy Materials	Liquidus Temperature	Peak Reflow Temperature
Sn96.5/Ag3.5	Tin/Silver	221°C	240°C - 250°C
Sn99.3/Cu0.7	Tin/Copper	227°C	245°C - 255°C
Sn93.6/Ag4.7/Cu1.7	Tin/Silver/Copper	216°C	237°C - 247°C
Sn95/Ag4.0/Cu1.0	Tin/Silver/Copper	218°C	238°C - 248°C
Sn96.5/Ag3.0/Cu0.5	Tin/Silver/Copper	218°C	238°C - 248°C
Sn95.5/Ag4.0/Cu0.5	Tin/Silver/Copper	218°C	238°C - 248°C
Sn95.5/Ag3.8/Cu0.7	Tin/Silver/Copper	218°C	238°C - 248°C
Sn96.3/Ag3.2/Cu0.5	Tin/Silver/Copper	218°C	238°C - 248°C
Sn95.75/Ag3.5/Cu0.75	Tin/Silver/Copper	218°C	238°C - 248°C

Table 1: Lead-free solder alloy compositions. (Source: Indium Corporation)

promotes wetting and serves as a temporary adhesive to hold components until the soldering reflow process is complete. Solder paste is furnished in various jar and cartridge sizes for stencil print processing. To accommodate both manual and automated dispensing systems, the solder material is commonly furnished in a syringe-like cartridge container formulated to provide a viscosity that ensures good flow characteristics (Table 2).

Although Type 3 solder paste may be suitable for conventional SMT stencil print processes, Types 4 and 5 are better choices for mechanical dispensing applications.

Solder Joining Process

Reflow solder processing is the most common and efficient technique for completing the component termination process. A substantial infrastructure already exists for supplying systems for both high and low volume manufacturing.

Common methods for mass reflow soldering include:

- Hot air/gas convection
- Infrared
- Conduction

For example, tin-silver-copper (SAC) alloy compositions become liquidus and enable flux activation at a temperature range of 220–230°C. However, the temperature required to complete the joining of the component to the land will reach 245–260°C.

A concern of using SAC solder alloys attaching embedded components is that after laminations are completed, the now-buried components solder termination will react during multiple exposures to the same high temperatures experienced during board-level assembly processing. To avoid the potential for disturbing the buried termination sites, assembly process specialists may consider adopting an alternative alloy composition for attaching the surface mounted components. A number of low-temperature solder alloy compositions are available. For example, some require only a 185°C peak temperature (compared to 245°C for SAC alloys). To achieve the lower melting temperature, solder paste suppliers add alloys such as bismuth (Bi), indium (In), and even a small amount of gallium (Ga) to the tin-based material, which significantly reduces the liquidus temperature of the composition (Table 3).

Solder Powder	Mesh Size	Particle Size
Type 3	-325 / +500	45µm to 20µm
Type 4	1400 / +635	38µm to 20µm
Type 5	-500	25µm to 10µm

Table 2: Solder particle size comparison. (Source: Nordson Corporation)

Alloy Composition	Liquidus Temperature (°C)	Solidus Temperature (°C)
Sn 57.68Bi 0.4Ag	142	137
Sn 57.0Bi 1Ag	142	137
Sn 38.0Bi 1Ag	176	137
Sn 58.0Bi 1Ag 1In	137	133
Sn 58.0Bi 1Ag 3In	133	125

Table 3: Low-temperature solder alloys. (Source: Alpha Assembly Solutions Publication)

Material	Solder	Isotropic	Anisotropic
Fillers	Alloy powder	Alloy particles	Alloy particles
Alloy	Sn/Ag/Cu	Ag	Ni/Ag or Ni/Au
Proc. Temp.	235°C-245°C	50°C-100°C	150°C-180°C
Proc. Time	~ 300 sec.	100-300 sec.	10-20 sec.

Table 4: Comparing solder and conductive polymer process variations.

SnBi alloy families have a competitive advantage over SnIn or SnGa variations due to their lower cost and broader source of supply.

Conductive Polymer Termination

The polymer-based materials used for component termination are a "thermoset" composition furnished with a catalyst to accelerate curing and a large percentage of silver alloy particles for electrical conductivity. "Thermoset" refers to the characteristic of the material to remain solid once cured even if subjected further to high temperatures.

To enable even dispensing of the polymer-based material, a small amount of solvent is added to the polymer/tin mixture that is eventually dispersed when exposed to the elevated temperature required for activating the catalyst. The conductivity of these materials will vary with different crystallographic orientation. When conductivity flows in one direction (bidirectional), the material is defined as anisotropic. Alternatively, when the conductivity flows in all directions (unidirectional), the material is classified as isotropic (Figure 1).

Similar to the solder paste materials previously noted, manufacturers offer conductive polymer materials in a paste form for screen and stencil printing and a more fluidic form for dispensing. Dispensing of the conductive polymers is preferred when in-cavity component placement is required.

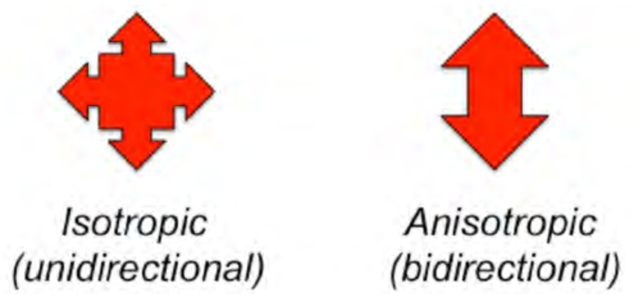


Figure 1: Conductive polymer characteristics.

Following component placement, the joining material will thermally cure to a solid state. The cure temperatures required may range from room temperature for two-part epoxy systems to 80–175°C for other single-component materials. In particular, thermoset materials will cure more quickly in an elevated temperature environment.

Process variations for SAC solder material and the conductive polymer joining families noted above are compared in Table 4.

Even though the materials referenced in Table 4 require elevated temperatures to complete the joining process, some anisotropic materials are available for room temperature joining using a single component ultraviolet (UV) curable polymer. To prepare for component termination with solder or tin-based conductive polymers, the copper land pattern surface must be clean and free of oxidation to ensure conductivity with the SnAg terminal plating commonly furnished on commercial passive components.

Microvia Termination

Microvia is term identifying a small plated via hole formed between layers of the circuit structure (either blind or buried) that is less than 150 µm in diameter. These copper-plated via holes may exist between one or more adjacent board layers or extend through all layers of the circuit board. Some companies have found that rather than relying on solder or a

Figure 2: A 01005 microvia termination. (Source: IPC-7092)

conductive polymer to terminated embedded components, a plated copper microvia can be a less complex method for providing the electrical interface.

However, to prepare for this termination alternative, the passive devices selected for direct microvia interface must be furnished with copper alloy-plated terminals. Although copper-plated terminals are not generally stocked in the commercial component distribution channels, they are an available option by ordering the components directly from the manufacturer or through the manufacturer's representative.

The basic component attachment process begins with the deposition or printing of a small amount of non-conductive adhesive material at the designated attachment sites followed by the precise placement of the devices and thermal curing to lock the components in position. A layer of resin-coated copper or glass-reinforced prepreg material is then laminated over the passive components, fully encasing them with the polymer material. The process employs both heat and pressure to complete the lamination. Next, laser ablation of the microvia holes over the terminals of the components is performed, followed by copper plating, imaging, and an etching process to complete the mechanical and electrical interface between the passive device terminals and upper layer circuit pattern. When microvia plate termination and etch processes are complete, the substrate is made ready for additional build-up circuit layering (Figure 2).

A primary concern is the post-lamination surface condition. The outer surfaces of the finished circuit board must remain flat to have proper control over solder printing processes for outer surface component attachment. When the thickness of component parts is greater than 0.2 mm, it can result in a slightly raised surface area at each component location. The raised areas will continue to impact the planar condition of each additional circuit layer resulting in irregular outer surface topography.

For components with a thickness greater than the prepreg material, it will be necessary to provide a cavity in the dielectric, which was also detailed in Part 4. The cavity feature is generally prepared within the dielectric layers before lamination. The opening can be mechanically punched, laser ablated, or milled while the material remains in the sheet form.

Embedding discrete component elements within the PCB structure is not a trivial process. Embedded components will increase the cost of the raw board, so a thorough technical evaluation must be made to justify implementation based on fabrication, product volume, and projected life cycle.

Next month, Part 6 of this series will consider alternative techniques for embedding active semiconductor elements, die preparation, and mounting and termination methodologies. **DESIGN007**

Vern Solberg is an independent technical consultant specializing in surface mount technology, microelectronics design, and manufacturing technology.
To read past columns or contact Solberg, click here.

Internal Trace Temperatures: More Complicated Than You Think

Brooks' Bits

by Douglas G. Brooks, Ph.D., with Dr. Johannes Adam

IPC-2152, published in 2009, was the most thorough study of trace current and temperature relationships ever undertaken [1]. It contains over 90 pages and charts that examine the relationships from numerous directions. Before IPC-2152, the industry used a set of charts that went back to a National Bureau of Standards (NBS) Report #4283 published in 1956 [2]. The charts were first published as a part of MIL-STD-1495 in 1973. They were later published in a subsequent series of standards that culminated in MIL-STD-275E in 1984. Further, the charts were published as part of IPC standard IPC-D-275, and IPC-2221A in 2003.

One of the most interesting findings in IPC-2152 was that internal traces are cooler than external ones for the same size and current. Independent experimentation was not done on internal traces in earlier charts. Internal traces were merely assumed to be hotter than external traces, and the external trace data was derated by 50% by that assumption.

Traces are heated by Joule, or I2R, heating. They are cooled by a combination of conduction through the dielectric, convection through the air, and radiation. It had previously been assumed that convection conducted heat away from the traces and cooled the traces more efficiently than conduction through the dielectric. Hence, the assumption that internal traces were hotter than their external trace counterparts. It turns out that dielectrics cool traces more efficiently than does convection plus radiation, and internal traces are relatively cooler [3].

One question is, "Is there a predictable relationship between the external temperature of a trace and the internal temperature of the same trace carrying the same current?" That is, is the internal trace 10% cooler, 20% cooler, or is there another predictor we can use to predict internal temperatures? The data in IPC-2152 makes it possible to explore this question. Internal and external temperature curves are provided for 1.0-, 2.0-, and 3.0-oz. traces and a variety of trace widths, so these relationships can be explored directly.

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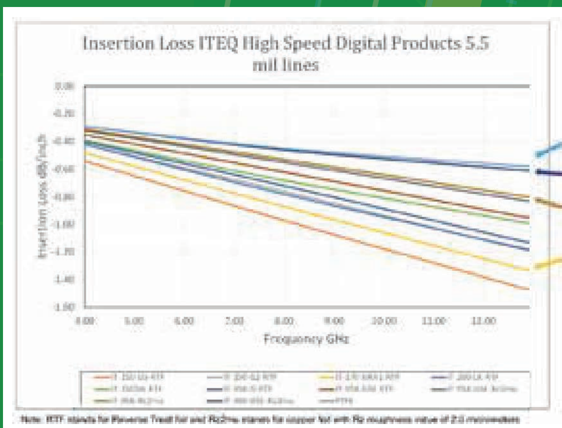

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- 100G / 400G Solution
- Lower Dk (<3.24 @ 10GHz)
- Ultra low Df (<0.0014 @ 10GHz)
- Very Stable Dk-Df across frequency
- HDPUG MRT-6 - LRC and HRC passed all thermal requirements
- HDPUG MRT-6 - LRC and HRC passed CAF requirements
- Proven thermal stability beyond 7 lamination cycles and suitable for HDI applications

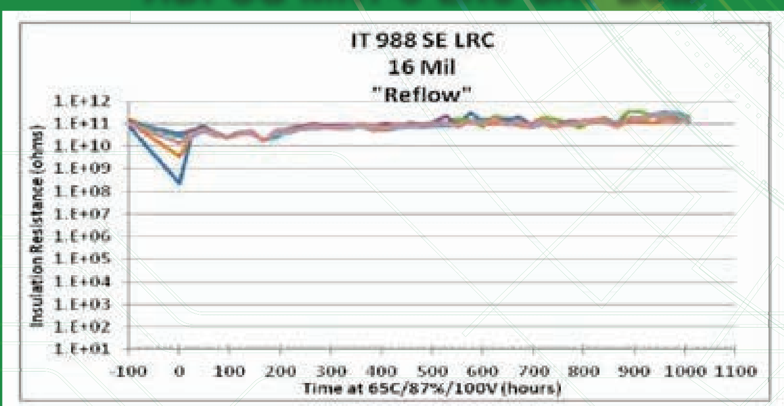
Sequential Lamination

7 Lamination cycle data

Lamination	DMA	DSC	TMA	T300 with CU	Solder Dip PCT: 1h @ 121°C	Td 2wt% / 5wt%
1	213	187 / 187	182	> 60	> 60	408 / 435
2	216	194 / 199	193	> 60	> 60	417 / 438
3	214	186 / 192	185	> 60	> 60	417 / 442
4	216	193 / 194	184	> 60	> 60	424 / 443
5	217	194 / 199	190	> 60	> 60	418 / 442
6	218	191 / 197	188	> 60	> 60	405 / 436
7	218	190 / 197	194	> 60	> 60	425 / 444

No thermal degradation observable after 7 lamination cycles

HDPUG MRT-6 LRC CAF Data



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The following procedure was followed. A sample of 44 observations (data points) was taken of both internal and external trace temperatures for otherwise identical trace and current situations. The change of temperature (DT) and the ratio of DT(internal)/DT(external) was recorded for each sample. The data was compared, and the relationship was found to be much more complicated than first assumed. A regression analysis was performed with the following result: R2 = 0.9981 (R2 is a measure of correlation or "goodness of fit" where 0.998 is exceptionally good).

Equation 1:

DT(internal)/DT(external) =

81.9 * TH^.053 * W^.0213 * ExDT^(-.0243)

- TH = trace thickness in mils
- W = trace width in mils
- ExDT = DT(external)

If we want to compare this equation with the actual ratio of the temperature change as derived from IPC-2152, we can calculate the ratio of the temperature changes for each observation using the equation for the analysis. Then, we can graphically compare this calculated result with that derived from IPC-2152. Figure 1 illustrates the result. It graphs the predicted versus the actual ratio of the change of temperature DT(external)/DT(internal) for each of the 44 elements of the sample. A 45° line is superimposed on the graph. If the predictions were perfect, they would all lay precisely on the 45° line.

Examining Equation 1, we can determine three relationships:

1. The ratio of internal change of temperature to external change of temperature decreases with increasing external trace temperatures, ceteris paribus (all other things equal). That is, internal traces get relatively cooler as external temperatures increase.
2. Thinner (internal) traces cool more efficiently than thicker traces, ceteris paribus.
3. Wider (internal) traces cool more efficiently than narrower traces, ceteris paribus.

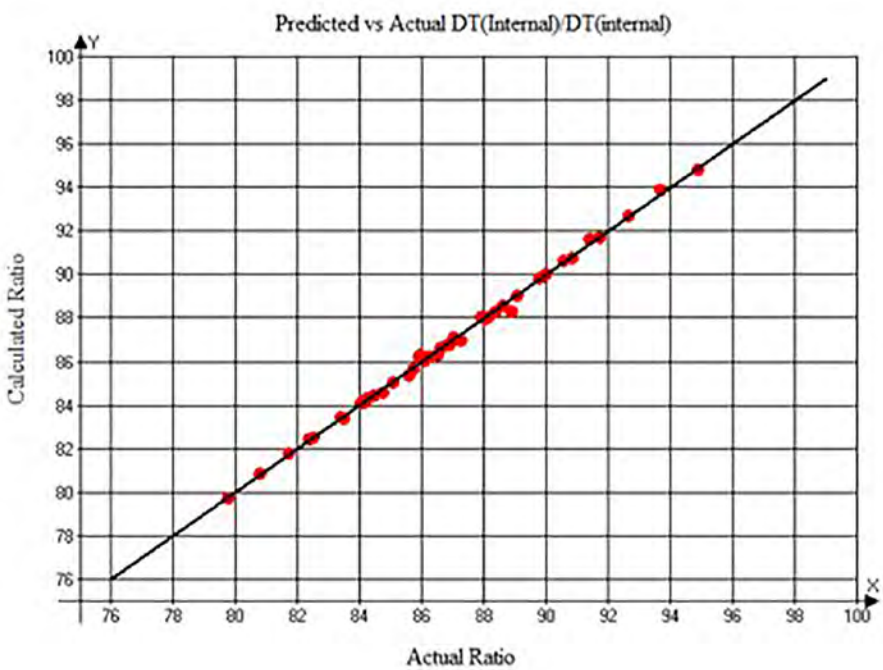

Figure 1: Predicted vs. actual ratio of the change of temperature DT(Internal)/DT(internal).

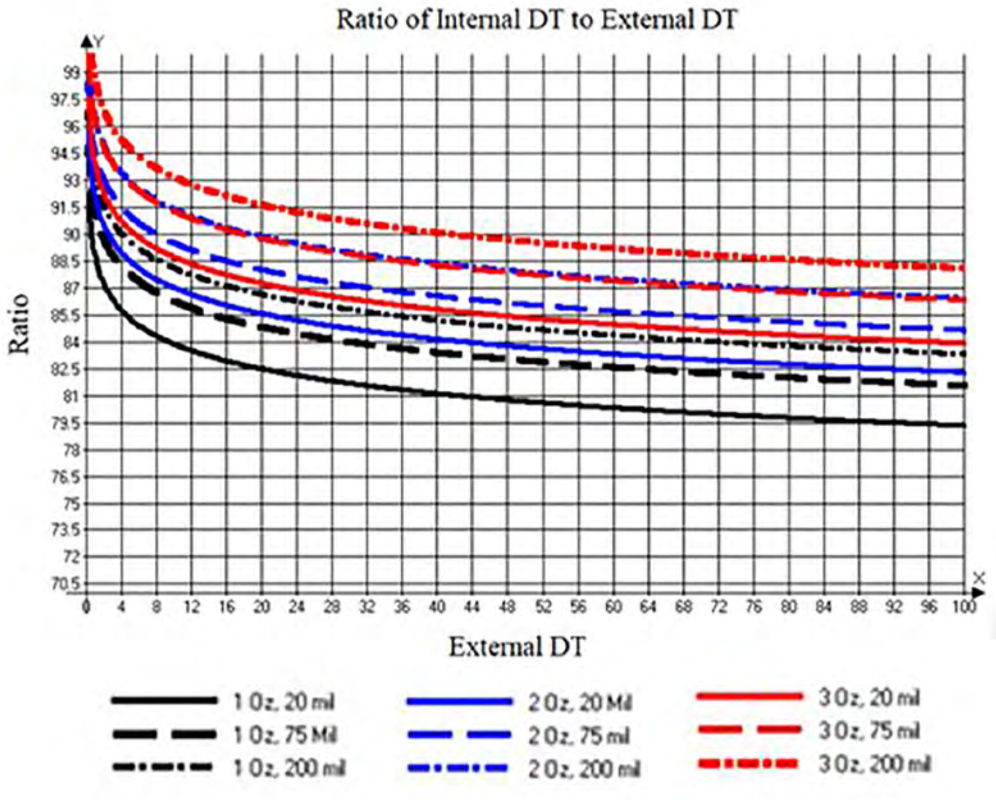

Figure 2: Ratio of internal change of temperature to external change of temperature for a variety of trace configurations.

These three relationships can be seen in Figure 2.

The results apply for internal traces in the middle of the board. Another question is, "What happens to the relationship for traces closer to an outside layer (i.e., not in the middle of the board)?" It seems intuitive that the difference between the internal and external temperature change is greatest at the middle of the board, and lessens somewhat as the internal trace gets closer to the external layers. We have modeled with the Thermal Risk Management (TRM) software simulation tool [4], which suggests that the cooling effect internal to the board kicks in at very shallow depths. TRM was originally conceived and designed to analyze temperatures across a circuit board, considering the complete trace layout with optional Joule heating as well as various components and their own contributions to heat generation.

Figure 3 illustrates this. At a relative depth of 0.5 (middle of the board), the ratio of the internal temperature change to the external temperature change is 100% (1.0) of the result previously predicted. However, let's say a trace is at a relative depth of 0.1 (6 mils into a 60-mil board). At that point, the change of temperature for the internal layer would be 43% of what was previously calculated.

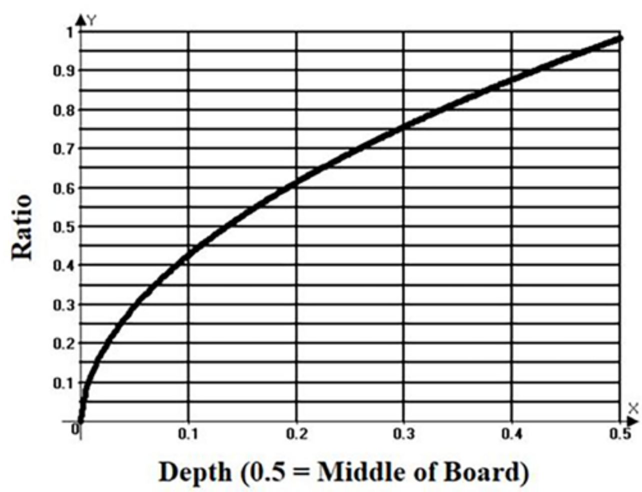

Figure 3: Ratio of full internal temperature change as a function of trace depth.

As an example, let's assume a 60-mil FR-4 board is 20 mils wide with 1.0-oz traces on the top layer and at the middle of the board. If the external trace is carrying 2.8 amps, we might find that the external change of temperature is 40°C. From Figure 2 or Equation 1, we can calculate that the internal change of temperature will be 40°C x 0.81 = 32.4°C, which is 7.6°C cooler than the external change of temperature. Now, if the trace is 12 mils below the surface instead of the middle of the board (i.e., the trace is at a depth of 12/60 = 0.2), then the difference between the internal temperature and external temperature changes would only be 0.62 times that calculated, or 0.62 x 7.6°C = 4.7°C. The internal change of temperature would be 35.3°C (a few degrees hotter than at the midpoint), but still cooler than the external trace.

There are a few caveats to this analysis. As we point out in our book [3], one of the most important determinants of trace temperature is the thermal conductivity coefficients of the dielectric. There are two such coefficients: one in the in-plane orientation (parallel to the traces), and one in the through-plane orientation (perpendicular to the traces). These coefficients relate to the cooling efficiency of the dielectric, and the trace temperature is heavily dependent on them.

However, the problem is most material suppliers do not specify a thermal conductivity coefficient for their product offerings, and if they do, they typically offer only one value without specifying which coefficient it is. You probably cannot know the coefficients for the materials you are using, and IPC-2152 does not report the applicable coefficients for their measurements. We can be comfortable that the prior analyses apply well to the IPC-2152 data (since that's where our analyses were derived from). It is less clear how well they will apply to your particular boards and designs. **DESIGN007**

References

1. IPC-2152, "Standard for Determining Current Carrying Capacity in Printed Board Design," August 2009.

2. National Bureau of Standards (NBS) Report #4283, D.S. Hoynes, "Characterization of Metal-insulator Laminates," May 1, 1956. Commissioned by the U.S. Navy's Bureau of Ships. For more information, see IPC-2152, Appendix A7, p. 85. A copy of the original NBS chart is included in Figure A89, p. 86.

3. Douglas Brooks and Johannes Adam, "PCB Trace and Via Temperatures: The Complete Analysis, 2nd Edition" CreateSpace Independent Publishing Platform, February 2017 (Chapter 4 provides a thorough discussion of trace heating and cooling).

4. Thermal Risk Management (TRM) simulation software is available at www.adam-research.com.

Douglas Brooks has a BSEE and an MSEE from Stanford and a Ph.D. from the University of Washington. For the last 27 years, he has owned a small engineering service firm, written numerous technical articles on PCB design and signal integrity issues, and published two books on these topics, as well as trace temperatures and currents. Brooks has given seminars several times a year all over the U.S., Moscow, China, Taiwan, Japan, Israel, Australia, and Canada. He primarily focuses on making complex technical issues easily understood by those without advanced degrees. To read past columns or contact Brooks, click here.

Johannes Adam received a doctorate in physics from Heidelberg University in 1989. He worked on numerical simulations of electronics cooling at software companies like Cisi Ingenierie S.A., and Flomerics Ltd. and Mentor. In 2009, Adam founded ADAM Research and now works as a technical consultant and software developer for electronics companies. He is the author of a simulation program called Thermal Risk Management (TRM) designed for electronics developers and PCB designers who want to solve electro-thermal problems at the board level. He is also a Certified Interconnect Designer (CID) and lives in Leimen, Germany.

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IPC's John Mitchell extends his congratulations and appreciation to the governments of the U.S., Mexico and Canada for their many months of tireless negotiations on a new trilateral trade agreement.

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David White has been involved with artificial intelligence research for almost 30 years. Now, David is the senior group director of R&D for Cadence Design Systems, and I knew we'd have to speak with him for this issue on AI. In a recent interview, we discussed his decades of work in AI, Cadence's research into AI and machine learning, and what he believes AI could mean for the EDA tools of the future.

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Measurement-to-simulation Correlation on Thin Laminate Test Boards

Quiet Power

by Istvan Novak, SAMTEC

A year ago, I introduced causal and frequency-dependent simulation program with integrated circuit emphasis (SPICE) grid models for simulating power-ground plane impedance [1]. The idea behind the solution was to calculate the actual R, L, G, and C parameters for each of the plane segments separately at every frequency point, run a single-point AC simulation, and then stitch the data together to get the frequency-dependent AC response. Here, using the measured and simulated data on test boards with four different thin laminates and a regular reference laminate, I will demonstrate how that simple model correlates to measured data and simulation results from other tools.

A number of different test boards were fabricated, tested, and simulated. The active area of all boards was 6x6" square, and all boards had the same 4-layer construction (Figure 1).

The device under test (DUT) laminate was centered in the middle and had five variants (Table 1).

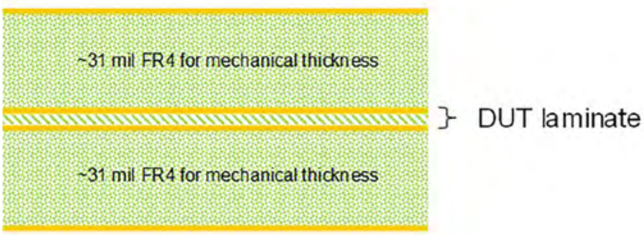

Figure 1: Stackup construction of test boards.

Reference laminate: FR406, 4-mil thickness, 1ou ED copper
HK04J 2536E, 1-mil thickness, 1ou ED coppers
HK04J 7423E, 0.5-mil thickness, 1ou ED copper
HK04J 0.35-mil ED, 0.35-mil thickness, 2ou ED copper
HK04J 0.35-mil RA, 0.35-mil thickness, 2ou RA copper

Table 1: Variants of DUT laminates.

The 4-mil regular FR406 laminate served as a baseline since it is common in low-cost PCBs as a power-ground sandwich. The other four options represent thin laminates in the range of 1 mil down to 0.35 mils in thickness. To check for the effect of copper weight and type, the 1-mil and 0.5-mil laminates had 1-ounce electrodeposited (ED) copper, while the thinnest option used two-ounce copper with ED and rolled-annealed (RA) variants.

To attach probes of measuring instruments and various bypass components to the board, there were 121 via pairs arranged as test points on a 0.5-inch grid. Notice the close-up of the cross-sectional view of the test points and the board top view sketches in Figures 2 and 3. Each circle in Figure 3 represents two vias, as

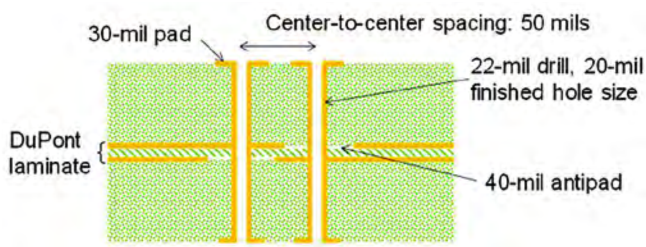

Figure 2: Cross-section of a test point via pairs.

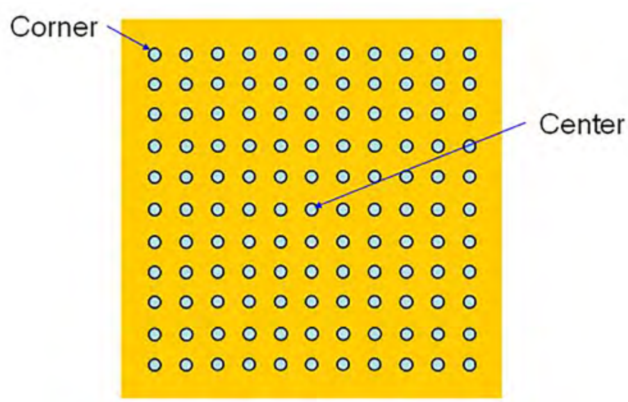

Figure 3: Top view of test boards showing the grid of connection points for probes and components.


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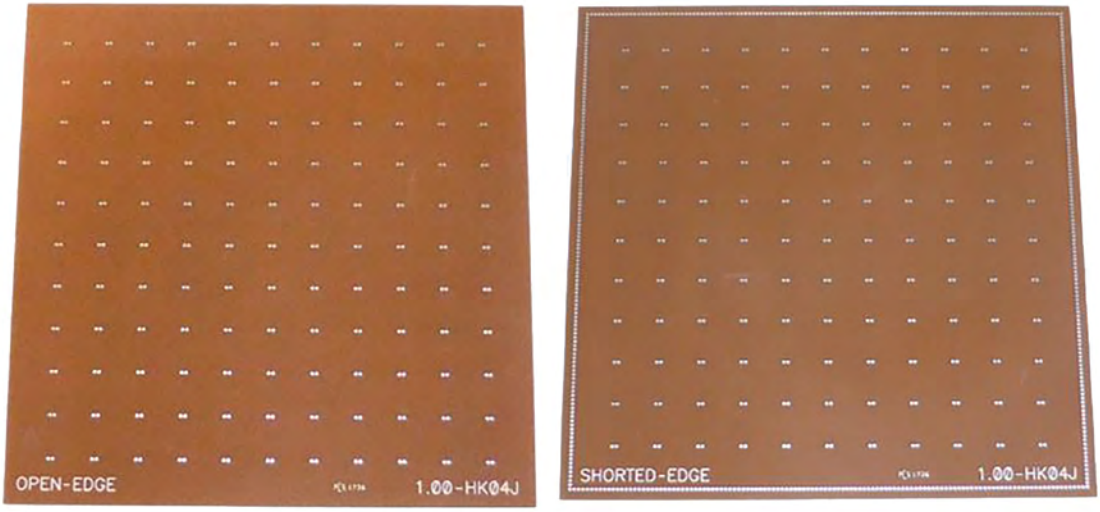

Figure 4: Test boards with 1-mil DUT laminate: (L) open-edge and (R) shorted-edge versions. Due to the tight spacing, the shorting vias along the board edge blend together and look like a trace.

shown in Figure 2. The via pairs are arranged on a 0.5-inch grid centered on the board. The corner and center labels mark the test points where I measured and simulated the planes.

Test boards with each laminate flavor had two additional subvariants: one with the board and plane edges left open (which is the typical case in our boards), and another with vias along the board edge, shorting the DUT laminate. The shorting vias have a center-to-center spacing of 50 mils. Figure 4 shows photos of the open-edge and shorted-edge 1-mil test boards.

These test boards have been measured and simulated in a large number of different configurations. Figure 3 includes the summary of data referring to two locations: corner and center.

For data shown here, I did not attach any component to the boards. Figure 5 shows the measurement setup for the open-edge boards. I used a Keysight E5061B vector network analyzer in two-port shunt-through connection. On the left, you can see the semirigid probes with a red heat-shrink tube, and the full setup on the right. For shorted-edge boards, the setup is the same except I also added a common-mode toroid [2] to reduce the cable-braid error (see Figure 17).

The first pass of simulations on the open-edge test boards started with nominal or estimated values. The boards were also cross-sectioned so that I could use the actual geometry

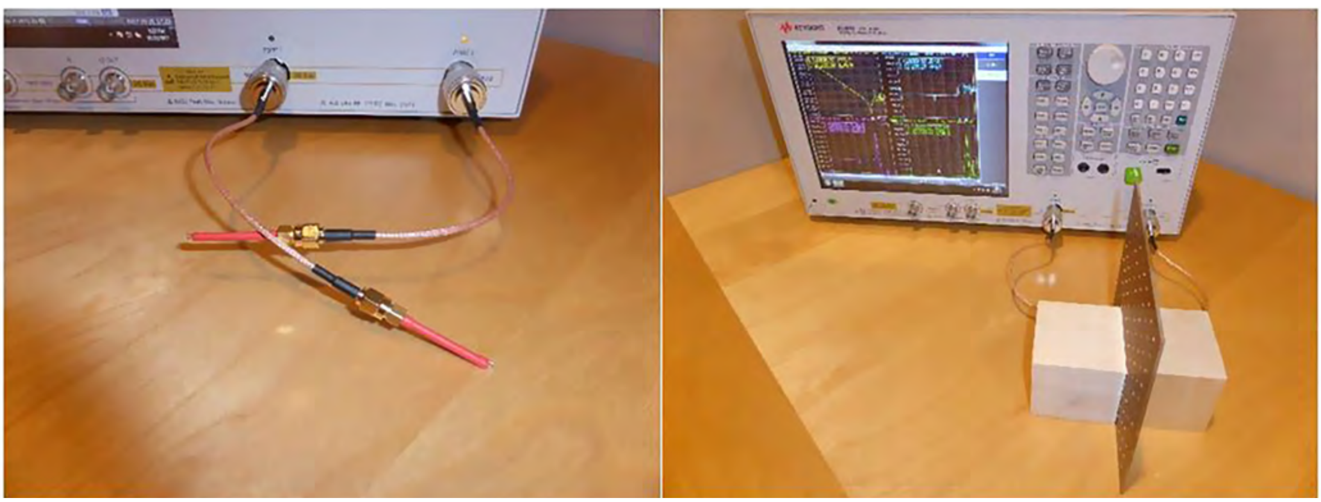

Figure 5: Test setup for the open-edge test boards.

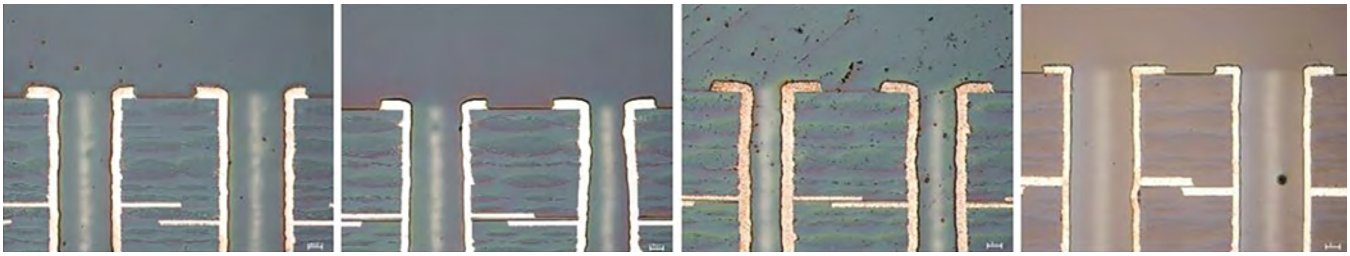

Figure 6: Cross-sections of the test board with four different laminate thickness: (L to R) 4, 1, 0.5, and 0.35 mils. Only the upper half of the stackup is shown. The DUT laminate is towards the bottom of the photos.

	4mil nom	4mil act.	1mil nom	1mil act.	0.5mil nom	0.5mil act.	0.35mil nom	0.35mil act.
Dielectric thickness [um]	101.6	100	25.4	25.6	12.7	13.6	8.89	9.22
Dielectric constant at Fo [-]	4.3	4.49211	3.3	3.254612829	3.3	3.687295468	3.3	4.096994964
Dielectric loss tangent at Fo [-]	0.02	0.01638	0.01	0.000500367	0.01	0.000500367	0.01	0.000500367
Fo [Hz]	1.00E+07	1.00E+07	1.00E+07	1.00E+07	1.00E+07	1.00E+07	1.00E+07	1.00E+07
Copper thickness [um]	35	29.1	35	33.6	35	32.6	70	69.3
Copper conductivity [S/m]	5.80E+07	46400000	5.80E+07	46400000	5.80E+07	46400000	5.80E+07	46400000
Copper type	ED	ED	ED	ED	ED	ED	ED	ED

Table 2: Nominal and actual simulation parameters.

in the second pass of simulations. Based on the measured dielectric thickness and measured capacitance, the dielectric constant and dielectric loss numbers were also updated. Figure 6 shows the representative cross-section photos, and Table 2 details the nominal and actual simulation parameters.

For the open-edge test boards, three different simulators were used: a simple analytical solution based on loss-less cavity models implemented in Excel macros [3], a causal SPICE grid model solved by Berkeley SPICE [1], and a hybrid solver (Cadence Sigrity PowerSI) [4].

You can see the correlation for the 4-mil laminate in open-edge test boards in Figures 7 and 8. The impedance magnitude correlation is quite good. Even the lossless analytical formulas (black trace labeled "Excel") capture correctly the capacitive downslope, overall inductive upslope, as well as the antiresonance peak frequencies. What it cannot capture properly are the loss-related items: magnitudes of the

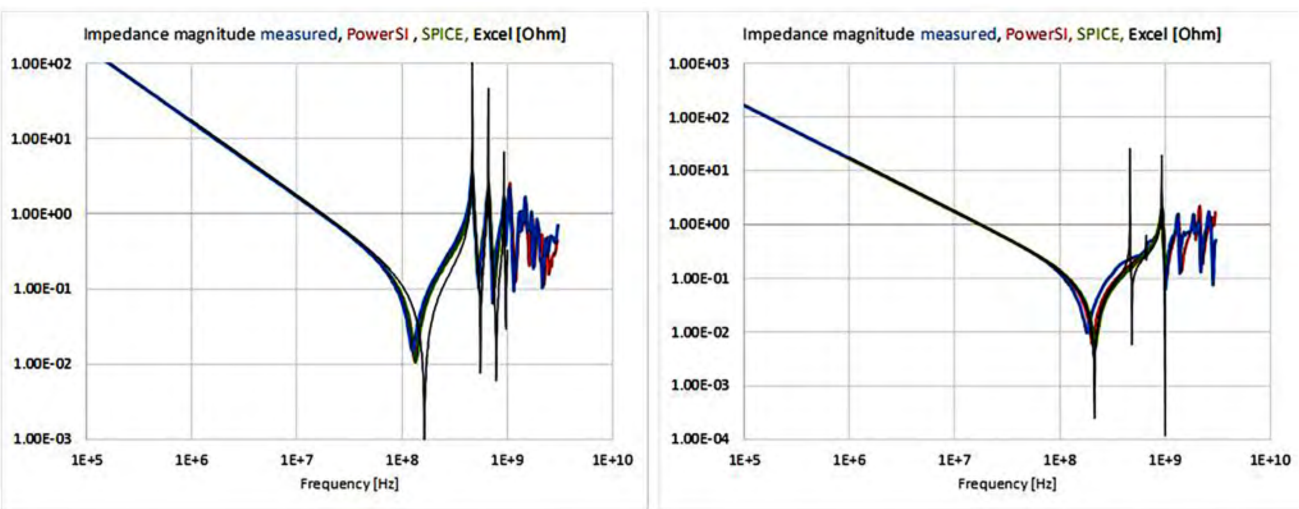

Figure 7: Impedance magnitude correlation of the 4-mil laminate data at the corner (L) and center (R).

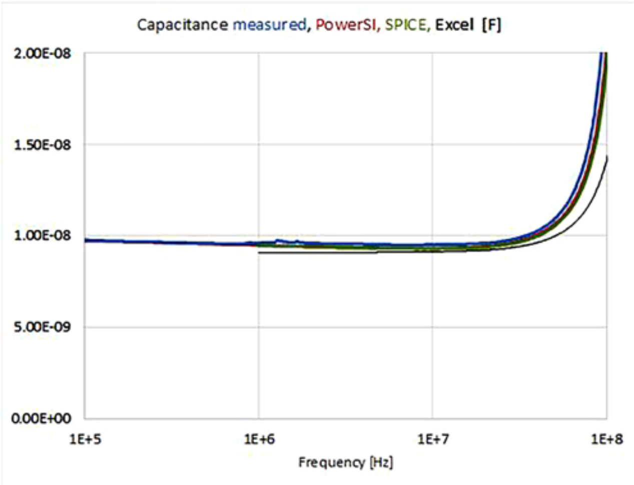

Figure 8: Capacitance extracted from the imaginary part of the impedance of the 4-mil open-edge board data.

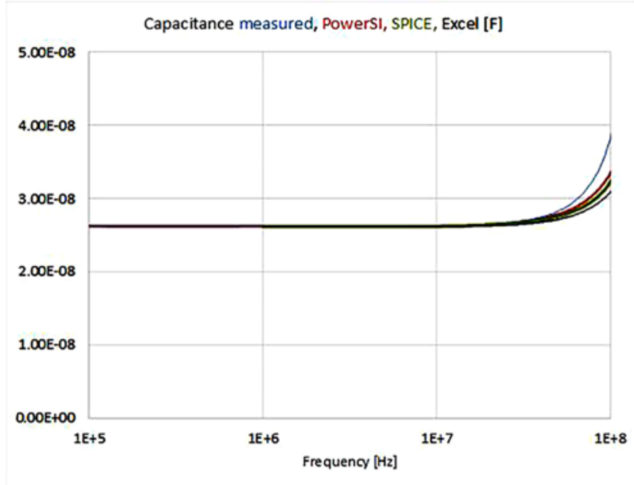

Figure 10: Capacitance extracted from the imaginary part of the impedance of the 1-mil open-edge board data.

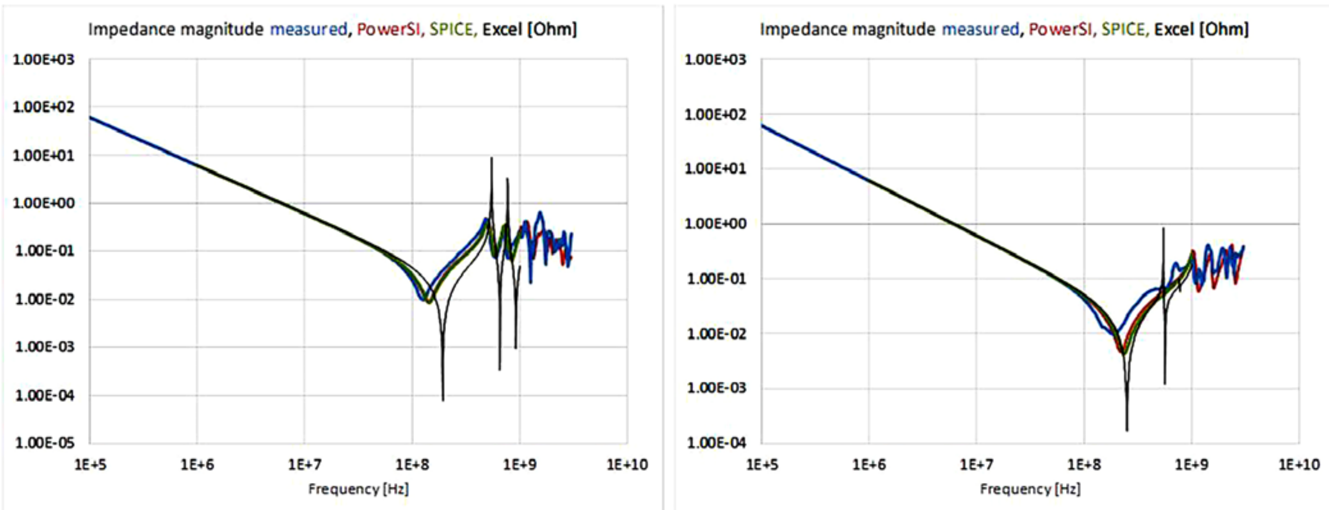

Figure 9: Impedance magnitude correlation of the 1-mil laminate data at the corner (L) and center (R).

modal resonance peaks and valleys, and the frequencies of the minima, which shift with losses.

Figure 8 shows the same effect with the extracted capacitance at the corner (the plots look the same at the center as well, and therefore, are not shown). Note the slight tilt of capacitance versus frequency curves, which is due to the dielectric loss. You can see this tilt in the measured data and simulated data alike, except the loss-less simulation (black trace), which ignores losses.

Figures 9 and 10 show the impedance magnitude and capacitance correlation for the 1-mil laminate.

The expected trend was observed: the reduced dielectric thickness comes with an overall lower impedance and higher capacitance. The conductive losses start to attenuate the modal resonance peaks. Also, the extracted capacitance curve is flat, indicating very low dielectric losses, and therefore even the lossless analytical Excel model correlates well.

This trend continues as I switch to the 0.5- and 0.35-mil laminates: overall impedance decreases, resonance peaks and valleys become less pronounced, and capacitance increases. The data for the 0.35-mil laminates are shown for the RA copper, though there was no measurable difference between the board

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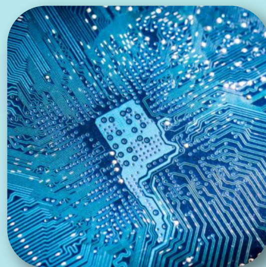

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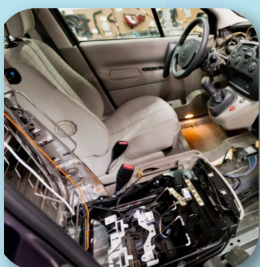

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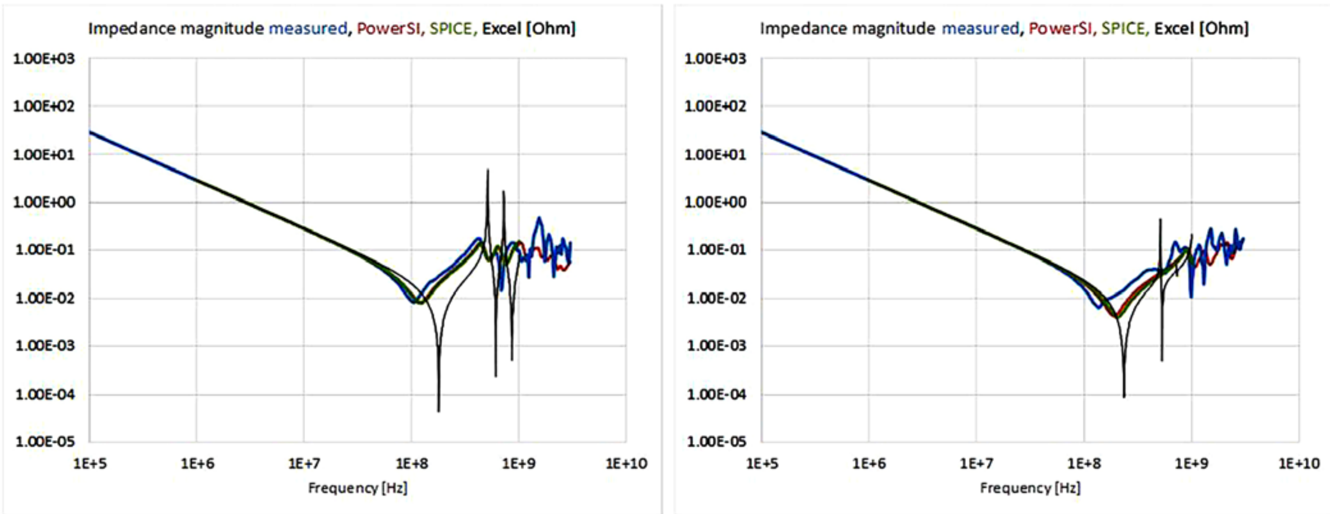

Figure 11: Impedance magnitude correlation of the 0.5-mil laminate data at the corner (L) and center (R).

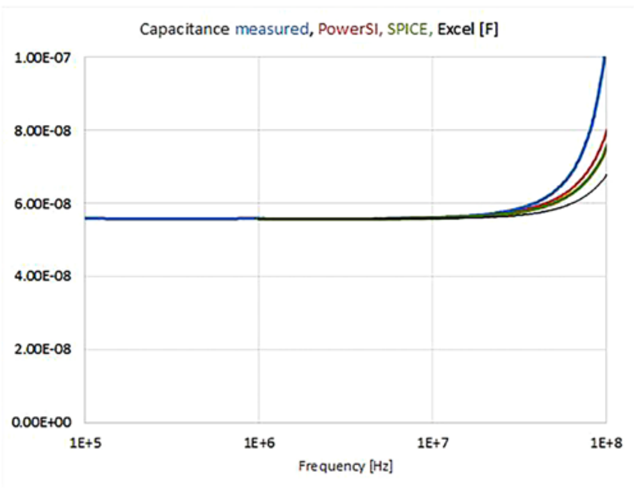

Figure 12: Capacitance extracted from the imaginary part of impedance of the 0.5-mil open-edge board data.

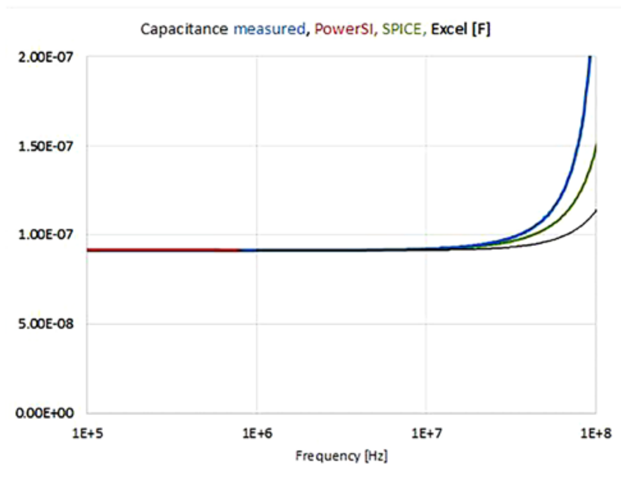

Figure 14: Capacitance extracted from the imaginary part of impedance of the 0.35-mil open-edge board data.

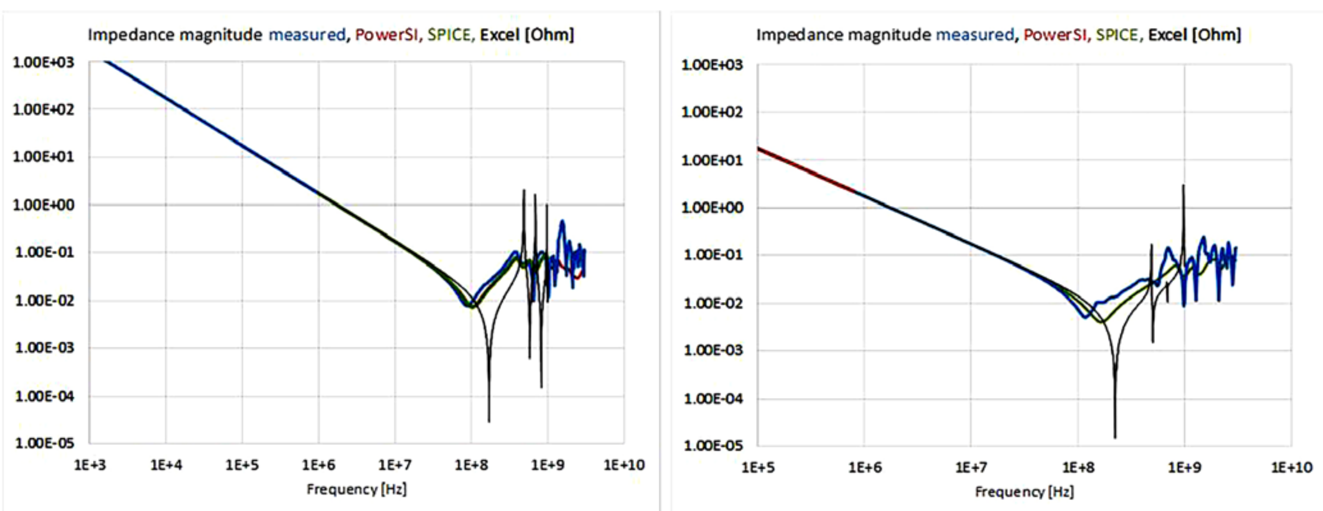

Figure 13: Impedance magnitude correlation of the 0.35-mil laminate data at the corner (L) and center (R).

impedances with ED or RA copper. Also, you don't see the effect of copper weight on these plots; it will show up in the data of shorted-edge boards.

Now that I showed a good correlation between measured and simulated data, the comparison of different laminates with the clean simulated data from PowerSI can be done. Figure 15 shows the impedance magnitude, and Figure 16 shows the capacitance comparison.

On the comparison plots, you can see that as the laminate gets thinner, the peak-valley ratio of modal resonances goes down, which makes it less likely that noise at the peaks would get too big and cause power or signal integrity issues and is a clear signal integrity benefit of thin laminates. You can also see that there may be different resonant frequencies depending on the location where you look at the board. In the center, the reflected waves coming back from the open edges cancel for the first two resonant peaks below 1 gigahertz, and therefore, do not see those peaks at the center.

Also note that the capacitance curves have very little dependence on location: at low frequencies the static plane capacitance is the same at every location. However, approaching

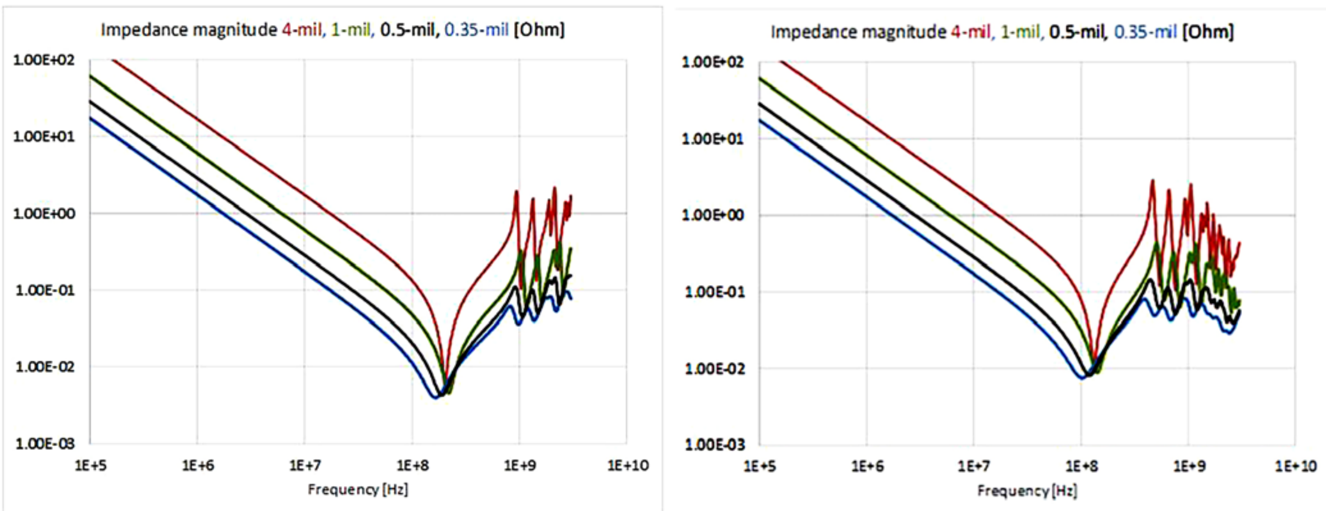

Figure 15: Comparison of PowerSI simulated impedance magnitude with different laminate thicknesses at the center (L) and corner (R) of boards.

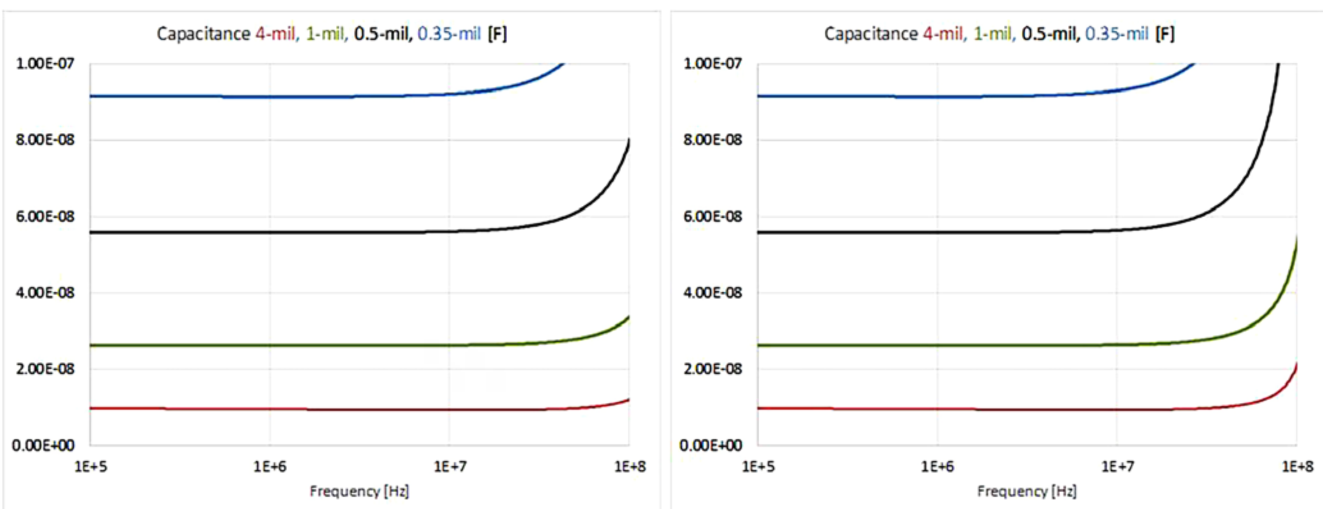

Figure 16: Comparison of PowerSI simulated capacitance with different laminate thicknesses at the center (L) and corner (R) of boards.

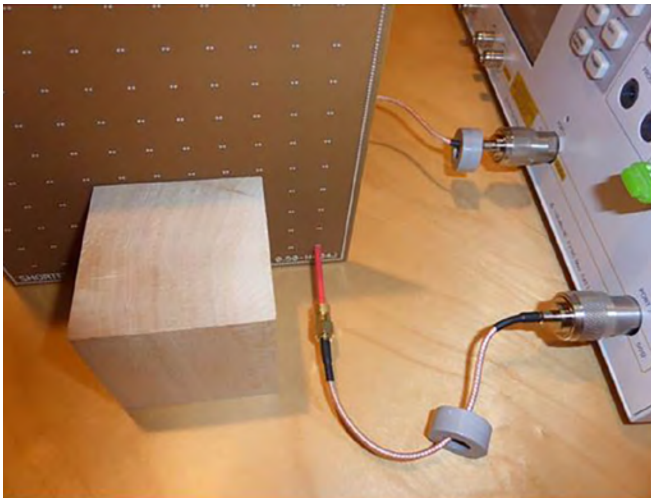

Figure 17: Setup for measuring shorted-edge boards. Note the grey high-permeability toroids on each of the cables.

100 MHz, all traces curve up, which is where you see slight differences because the series resonance frequency varies a little with laminate thickness. Remember that the uptick of extracted capacitance is not real—it is just a side-effect of the approaching series resonance, which happens at slightly different frequencies with different laminate thicknesses.

The main takeaway from Figure 16 is that the static capacitance of power-ground laminates is inversely proportional to the laminate thickness. With thinner laminates, you get more capacitance, which is the reason why thin laminates are sometimes called buried capacitance. However, while the plane capacitance itself may be sufficient for bypassing for nanopower circuits, in medium- and high-power circuits, the lower inductance and resonance peaks greatly help. To see clearly how the inductance of laminates depends on dielectric thickness, I look at the data on shorted-edge test boards next.

The measurement setup for the shorted-edge test boards is similar to the open-edge boards, but I must reduce the low-frequency error caused by the cable-braid resistance. This is not an issue when you measure open-edge boards because their impedance at low frequencies is much higher than the cable-braid resistance. With shorted-edge boards, you have to measure in milliohms or less impedance at low frequencies—which is practically the resistance of plane loops—and cable braid resistances in the same order of magnitude because it would create too much error. There are different ways of reducing this error. Here, I used common-mode toroids on the measurement cable. Figure 17 shows this setup.

For shorted-edge test boards, the simulations were done with PowerSI. Figures 18 and 19 demonstrate the correlation for the 4-mil laminate shorted-edge boards. Up to about 1 MHz, the impedance magnitude is flat, because I measured the resistance of shorted planes. Above 1 MHz, the impedance slopes upwards, indicating a combination of increasing skin resistance and inductive reactance. The impedance magnitude plots at the center have resonance peaks and valleys at high fre-

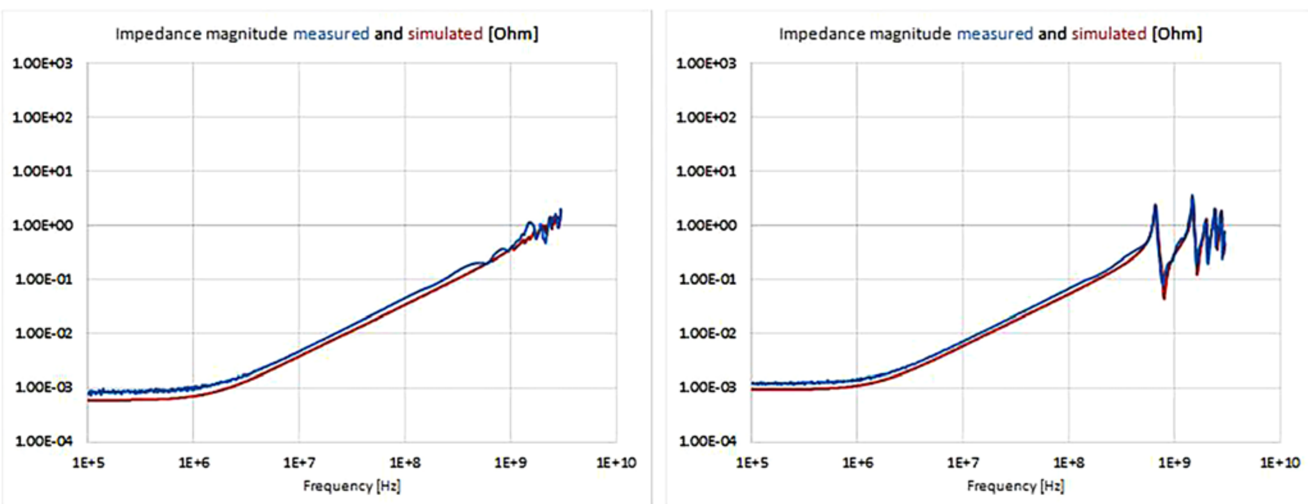

Figure 18: Impedance magnitude correlation of the 4-mil laminate data at the corner (L) and center (R).

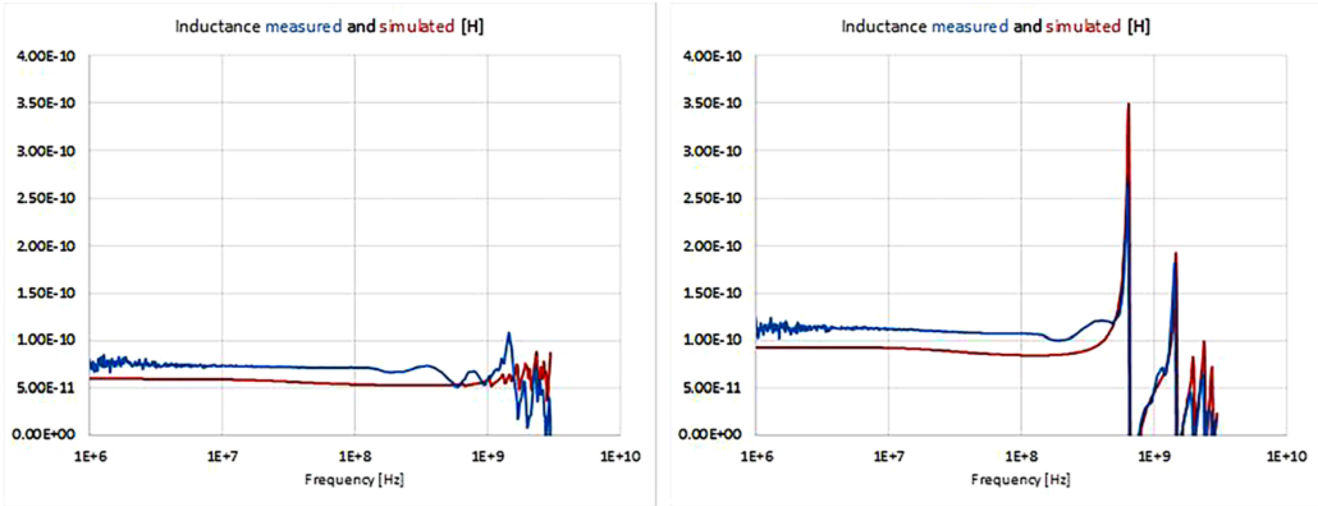

Figure 19: Inductance extracted from the imaginary part of impedance of the 4-mil shorted-edge board data at the corner (L) and center (R).

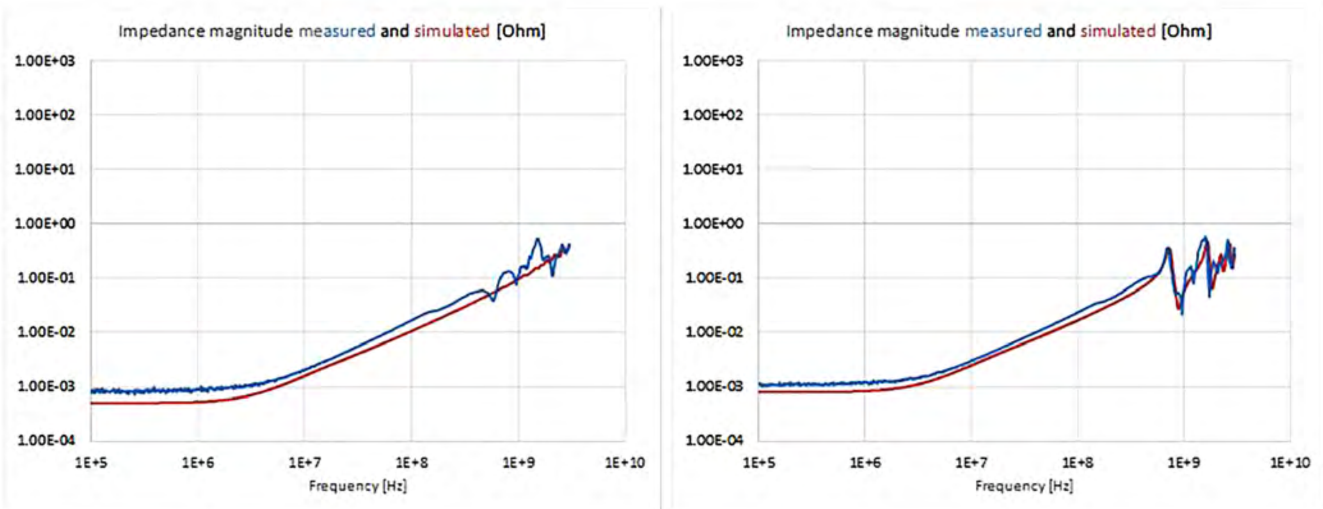

Figure 20: Impedance magnitude correlation of the 1-mil laminate data at the corner (L) and center (R).

quency. You don't see those resonance peaks at the corner because the wall of shorting vias is only a quarter of an inch away, forcing the impedance low.

Figure 10 displays the same trend. As opposed to the static capacitance—which is the same at the center and corner—the extracted inductance does depend on the location. As you move closer to the wall of shorting vias, the loop inductance gets lower. If you want inductance values representative to the laminate, you must take the inductance at the center. The inductance is around 100 pH, which correlates approximately with the spreading inductance estimate of planes, which is 33 pH for each mil of dielectric spacing. The inductance curves are relatively flat, but there is a small downslope starting around 10 MHz.

You can see the correlation for the 1-mil laminate in Figures 20 and 21. It follows the same basic signature; however, the primary difference is the lower inductance. Not only does the entire curve runs lower, but you can also see a more pronounced change of inductance with frequency. The inductance starts to drop at 10 MHz, which is commonly considered the skin corner frequency of 1-ounce copper.

Figures 22 and 23 show the 0.5-mil correlation. The data follows the same trend—lower

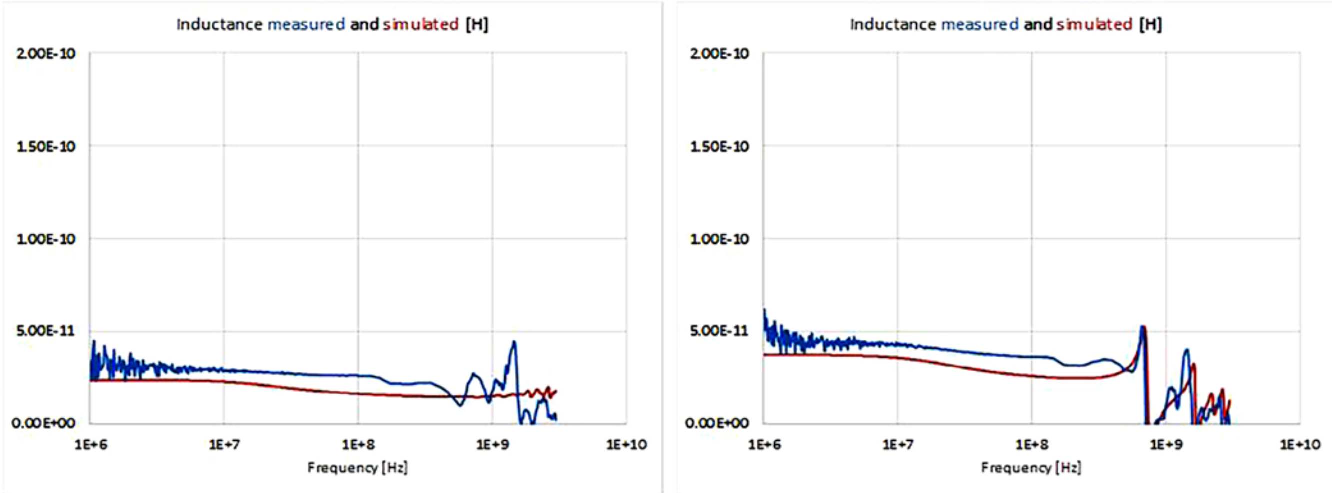

Figure 21: Inductance extracted from the imaginary part of impedance of the 1-mil shorted-edge board data at the corner (L) and center (R).

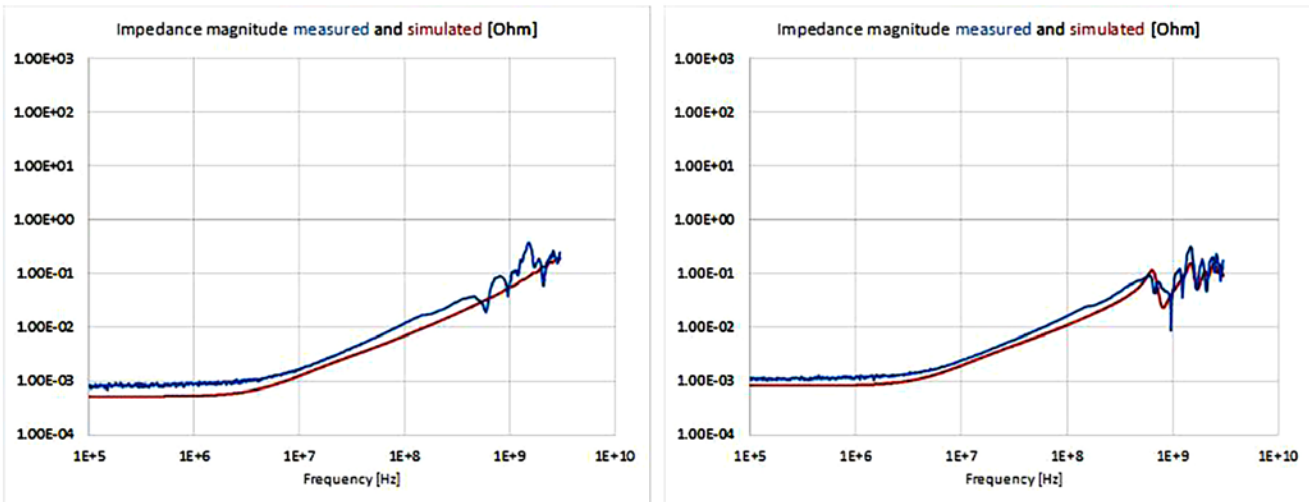

Figure 22: Impedance magnitude correlation of the 0.5-mil laminate data at the corner (L) and center (R).

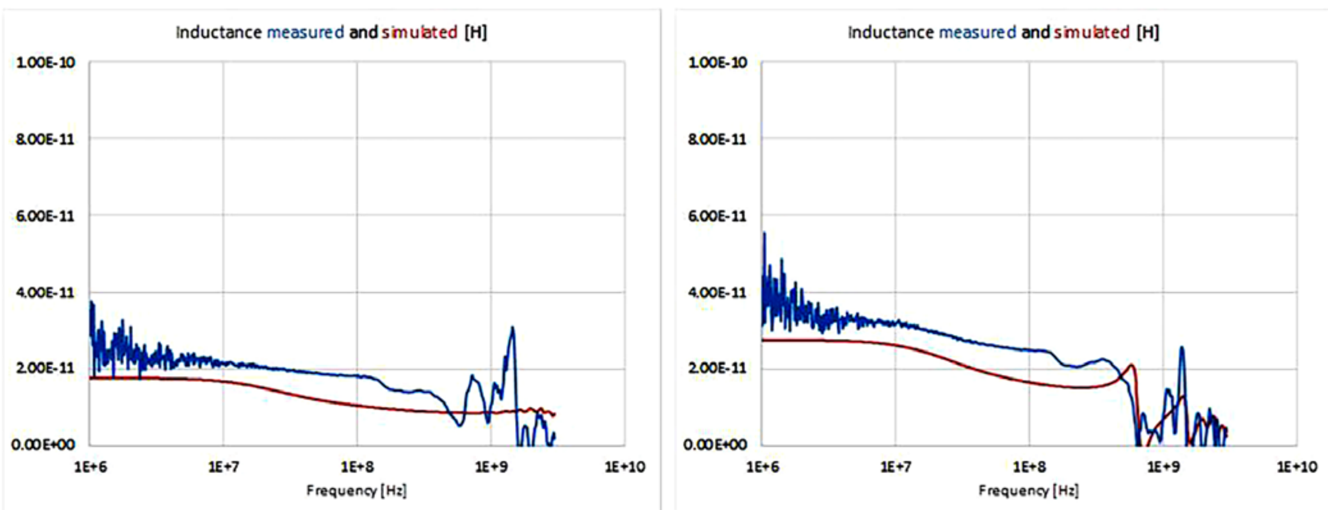

Figure 23: Inductance extracted from the imaginary part of impedance of the 0.5-mil shorted-edge board data at the corner (L) and center (R).

inductance—but notice that the inductance did not drop by a factor of two because the inductance of the unavoidable antipad opening around the test vias penetrates the plane that they do not connect to. Unless I use smaller vias and antipads, this eventually becomes a limiting factor for utilizing the full low-inductance benefits of thin laminates.

Figures 24 and 25 show the correlation for 0.35-mil laminate with two-ounce copper. Here, you will see that at low frequencies, the impedance magnitude curves start at lower values because of the lower resistance of the two-ounce copper planes. The thicker copper allows for a more vertical spreading of the current loop, which results in a higher inductance at low frequencies. The low inductance originating from the thin laminate kicks in at higher frequencies.

The next two figures show the overall comparison of the shorted laminates. You can see the impedance magnitude comparison in Figure 26 and the inductance comparison in Figure 27. Below 1 MHz, the impedance magnitude plots follow the DC resistance of the planes. The three boards with 1-ounce copper run around 1 mOhm, and the 0.35-mil test board using 2-ounce copper runs at 0.5 mOhm.

In the inductive upslope region, the order of curves follow the laminate thickness values—

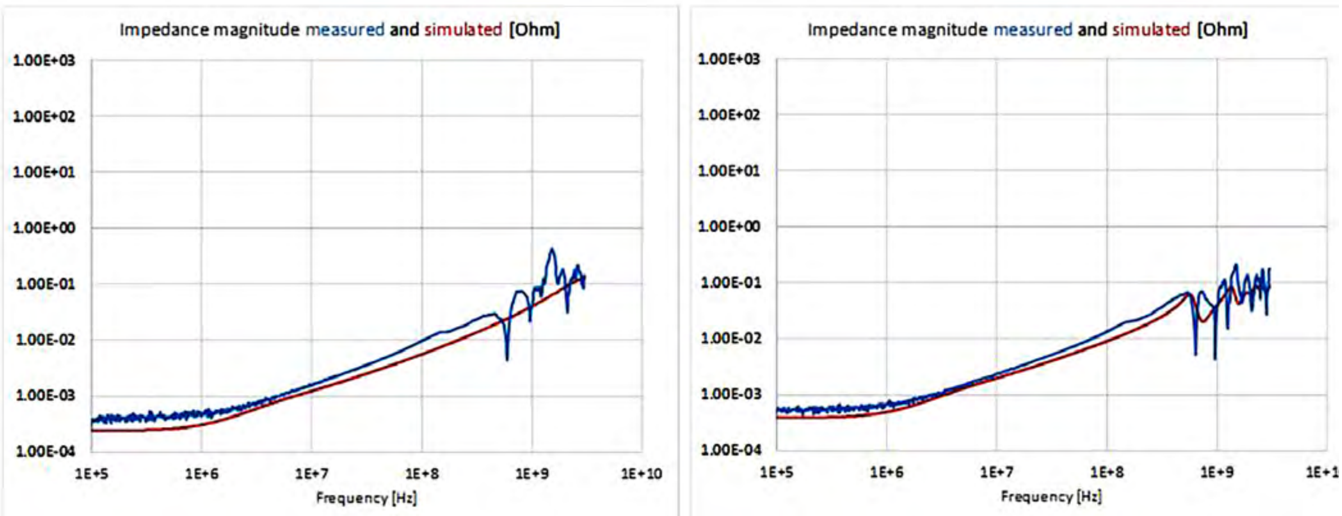

Figure 24: Impedance magnitude correlation of the 0.35-mil laminate data at the corner (L) and center (R).

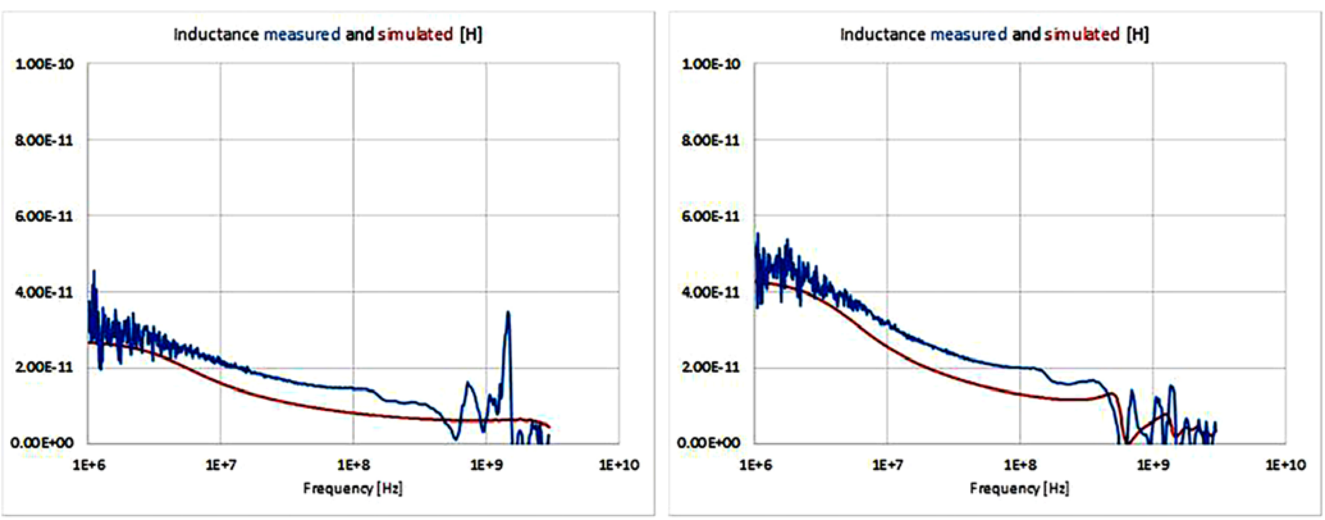

Figure 25: Inductance extracted from the imaginary part of impedance of the 0.35-mil shorted-edge board data at the corner (L) and center (R).

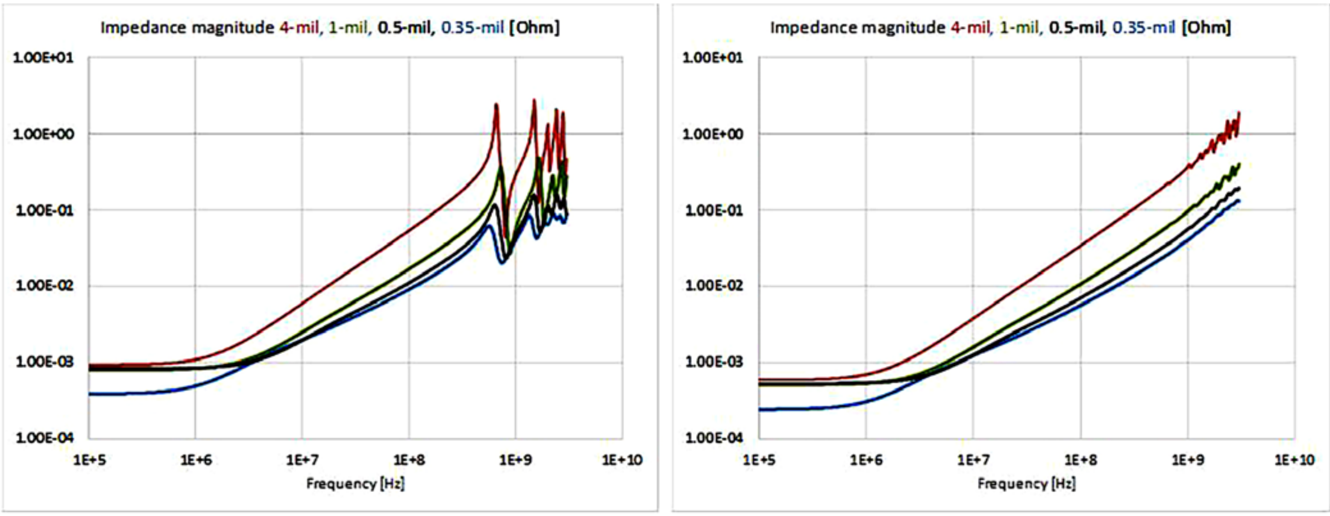

Figure 26: Comparison of PowerSI simulated impedance magnitude with different laminate thicknesses at the center (L) and corner (R) of boards.

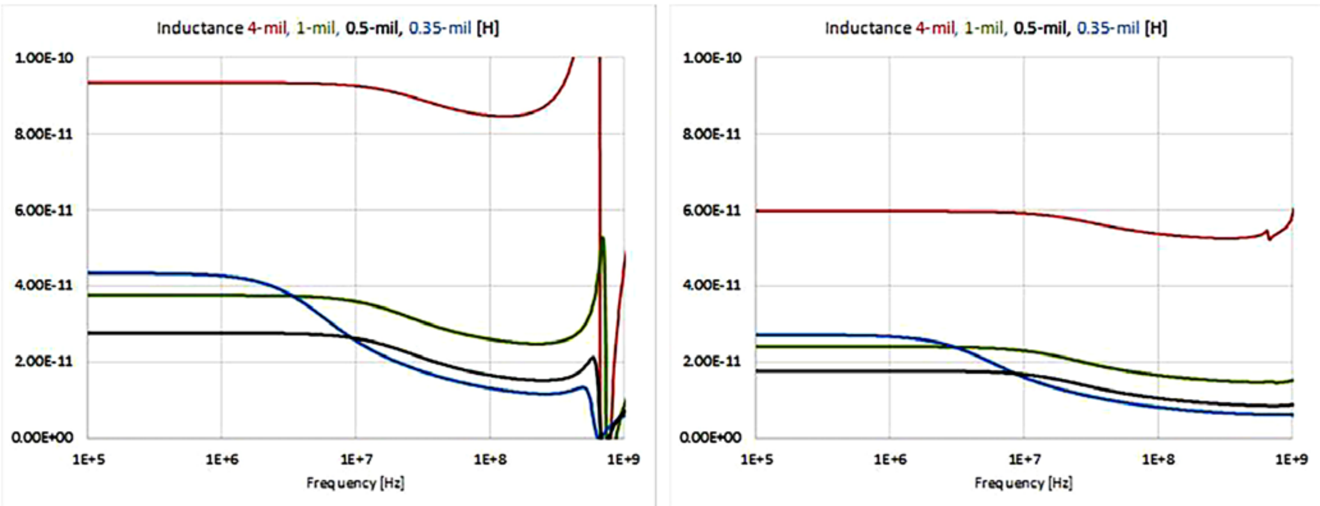

Figure 27: Comparison of PowerSI simulated inductance with different laminate thicknesses at the center (L) and corner (R) of boards.

thinner laminates produce lower impedance. The inductance comparison in Figure 27 demonstrates how the different laminates compare in their frequency ranges. In the entire frequency range, the 4-mil laminate produces the highest inductance. With thinner laminates—and also because the copper thickness now becomes comparable to the dielectric thickness—the order of inductance depends not only on the laminate thickness, but also on the copper weight and frequency. Below 1 MHz, the highest inductance comes from the thinnest dielectric, but just because this laminate had 2-ounce copper. Above 10 MHz, the order of curves follows the laminate thickness.

Conclusion

I showed the correlation of impedance and extracted capacitance and inductance values of 6x6" laminate test boards with open and shorted edges. The correlation was shown with three different simulation tools for the open-edge boards, including loss-less analytical formulas to capture the capacitive downslope of impedance magnitude curve, but without the small tilt due to dielectric losses. They also capture the peak frequencies of resonances properly, but due to ignoring losses, the peak/valley values and valley frequencies are off. The causal SPICE models and professional hybrid solvers capture all of those effects correctly.

However, the inductance of laminates depends on the combination of laminate and copper thicknesses and frequency. At high frequencies, the inductance is clearly proportional to dielectric thickness, which is the primary power distribution benefit. Below the skin cutoff frequency, the inductance gets bigger with heavier copper. Thin laminates also naturally suppress plane resonances. The correlation is somewhat worse for shorted-edge test cases because the causal SPICE models ignore and hybrid solvers only approximate for the impact of test-via antipads. To get that level of correlation, you must use 3D solvers [5].

Acknowledgement

The DUT laminates and fabrication are courtesy of DuPont, the network analyzer personal loaner is courtesy of Keysight, and the PowerSI simulations are courtesy of Cadence. Special thanks to Jin-Hyun Hwang, Tom Hilger for running the simulations, and Brad Brim for his valuable comments and guidance. **DESIGN007**

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How Can We Design Electronic Devices That Don't Overheat?

The heat produced by electronic devices does more than annoy users. Heat-induced voids and cracking can cause chips and circuits to fail.

Now a Stanford-led engineering team has developed a way to not only manage heat, but help route it away from delicate devices. Writing in *Nature Communications*, the researchers describe a thermal transistor—a nanoscale switch that can conduct heat away from electronic components and insulate them against its damaging effects.

"Developing a practical thermal transistor could be a game changer in how we design electronics," said Senior Author Kenneth Goodson, a professor of mechanical engineering.

Researchers have been trying to develop heat switches for years. Previous thermal transistors proved too big, too slow and not sensitive enough for practical use. The challenge has been finding a nanoscale technology that could toggle on and off repeatedly, have a large hot-to-cool switching contrast and no moving parts.

Aditya Sood, a postdoctoral scholar with Goodson and Pop and co-first author on the paper, likened the thermal transistor to the thermostat in a car. When the car is cold, the thermostat is off, preventing coolant from flowing, and the engine retains heat. As the engine warms, the thermostat opens and coolant begins to move to keep the engine at an optimal temperature.

Thinking about this process is crucial to designing safer batteries. In a more distant future, the researchers imagine that thermal transistors could be arranged in circuits to compute using heat logic.

(Source: Stanford University)

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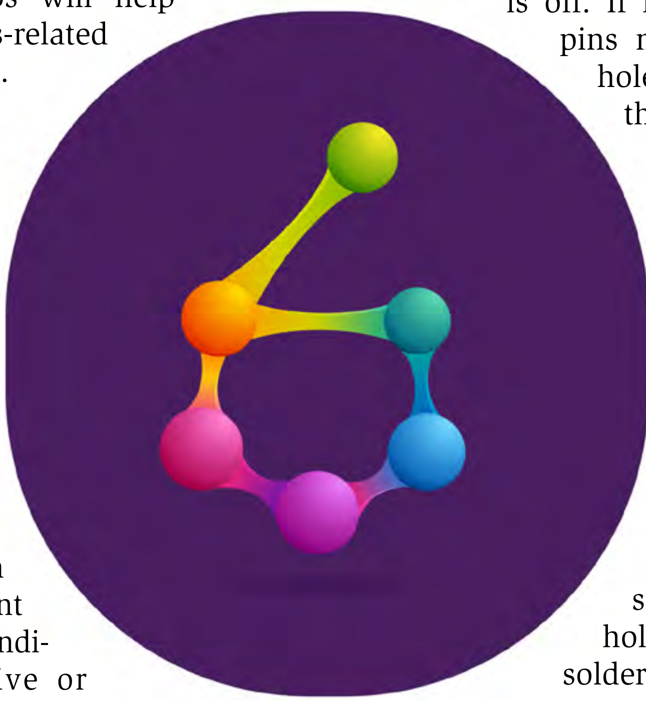
Six Tips to Ensure Parts Fit on Your Board

Connect the Dots

by Bob Tise and Dave Baker, SUNSTONE CIRCUITS

"Will my parts fit on the board?" That seems like an easy enough question to answer as you transition from the design stage to manufacturing, but issues with parts fitting are one of the most frequent causes of delays and cost overruns. We see it every day. Designs are submitted that can't or shouldn't be manufactured because the parts will not fit properly. This creates issues with performance and durability—effectively reducing the overall quality of the board.

The six following tips will help you avoid common parts-related manufacturability pitfalls.



1. Avoid Pinhole Pitfalls

It's essential to check component physical dimensions, consider dimension tolerances, and account for variations that could impact fit. Pins could be the wrong size or have the wrong spacing, and components could be much larger than their footprint or land pattern might indicate. Further, alternative or replacement components could be on the wrong end of the tolerance range. After all, it just takes a few mils before things don't fit and assembly starts going wrong. Finding a good alternative part can be a challenge, which is why datasheets can be your best friends. In addition to watching part sizes, pay close attention to the minimum, nominal, and maximum material conditions for the original part.

2. What to Do When the Land Pattern and Pin Size Differ

One of the most frustrating mismatches with alternative through-hole parts occurs when the land pattern matches, but the pin size is off. If hole sizes are too tight, pins may not fit through the holes, or if they do go into the holes, they may not solder well. Solder will need to flow through the gap between the pin and the hole barrel. If there is not enough space to allow enough solder mass to flow through the hole, the circuit board will absorb heat from the molten solder and cause the solder to solidify partway up the hole. This is called a cold solder joint and can result in a premature failure of your circuit.

To avoid this issue, make sure that when you design your land pattern, you know the pin size and tolerance range for your components. With that information, you can plan

the proper hole size. Component holes should be sized correctly to allow 12–16 mils in diameter larger than the component pin at maximum material condition (MMC). MMC is the condition where the hole is drilled at the low end of the tolerance range and the pin measures at the high end of the tolerance range. Pin locations should be placed at nominal locations or the basic dimensions shown on the datasheet.

3. Datasheets Can Disagree with CAD Software

Third-party CAD libraries can contain millions of different parts, so it's no surprise that a few bad apples lurk among them. When the datasheet and library part don't match up, your project is dead before you make the first connection. Always check any library part for accuracy before you use it the first time. The datasheet for a part usually tells the real story—a long story, but one worth reading. Some datasheets can run upwards of 200 pages, and it's just a few lines that provide you with the information you need to make crucial decisions about sizing. It's important to read and comprehend the datasheets, so problems in CAD don't lead to the wrong sizing and spacing on the PCB.

4. Pay Attention to Pinouts When Using Alternative Vendor Parts

Even if you've paid attention to pin and through-hole size and made sure your solder joints are good, a part can still not work as expected. Similar parts with the same footprint might look like they should act identically, but they won't always have the same pinout. Sure, each transistor has a gate, drain, and source, but different manufacturers can vary in what goes where. A Motorola part can differ from a Texas Instruments (TI) part, and if you're buying generics, all bets are off. The same basic component will come in multiple packages. Sometimes the variations are tossed into the back of a datasheet as an afterthought, but these can be critical. Similarly-named packages can even come in different widths.

5. Be Aware of Mechanical Fit

It's not just the footprint and through-holes that you need to pay attention to. The physical size of your component body can keep parts from fitting into designated spaces. Again, pay close attention to the MMC size and the tolerance range—both are critical. As parts get larger, or you start sourcing your parts from multiple vendors, your footprint size may need to expand considerably to accommodate all of the dimension and tolerance variables. When combining multiple part body dimensions, always take the largest dimension, or you could end up trying to violate the Pauli exclusion principle, which states that two identical fermions (particles with half-integer spin) cannot occupy the same quantum state simultaneously. In short, you are going to smash something.

6. Datasheets Are Helpful but Do Not Replace Experience

When it comes down to it, the datasheet is considered king, but that doesn't mean you shouldn't question it when necessary. Many problems with fit can be counterintuitive or difficult to diagnose, so understanding size requirements will prevent a lot of headaches. Every dimension needs to be looked at, from pin and through-hole size to capacitor height.

Frequently, these issues will crop up when replacement components are used. Watch those tolerance ranges carefully. When you evaluate replacements, make sure your replacement parts fall between the minimum and maximum measurements stated in your original part datasheet. You could get away with parts that are smaller in some regards, but this should be carefully evaluated. And don't forget to pay attention to pinouts and alternative packages. **DESIGN007**


Bob Tise


Dave Baker

Bob Tise and **Dave Baker** are engineers at Sunstone Circuits. To read past columns or contact Tise and Baker, click here.

Top Tips for Successful Potting

Sensible Design

by Alistair Little, ELECTROLUBE

My last column turned to some of the more technically challenging aspects of resins and their applications and was largely based on customer queries concerning thermal conductivity, dielectric constant, and choice of resin chemistries. With important resin considerations aside—which hopefully had you thinking a bit more deeply about these extraordinary materials—I thought it appropriate to return to the nitty gritty of resin encapsulation and offer my top tips for successful potting.

For effective potting, ideally, the layout of the circuit components should be such that the material can flow smoothly around them without too much turbulence. When possible, it is always good practice to space components in a regular pattern. Irregular spacing—particularly bunching of components in discrete areas of the PCB—causes the formation of eddies in the resin as it is poured, which can lead to voids and air entrapment, which compromise the thermal performance of the resin.

Where large volumes of resin are required, particularly where the encapsulated volume is deep, it is far better to cast the resin in layers to achieve the desired thickness, rather than attempting the cast in a single pour. This helps control the exotherm potential (remember—two-part resins in large volumes get quite hot when mixed) and reduce void formation.

Void formation (air bubbles) is a particular bugbear of resin application that must be avoided at all costs because it reduces the thermal performance of the cured resin encapsulation and may entrap areas of high moisture content at the surface of the PCB, which can lead to corrosion issues. The best method to prevent void formation is vacuum potting, but this may not always be possible due to the geometry of the device to be potted, production volumes, or cost. If vacuum potting is not an option, then the best approach is to handle your materials with great care to minimise air entrainment at every stage of the application process.

For example, careful decanting of the resin and hardener

into the dispensing equipment reservoirs and then leaving the material undisturbed for a couple of hours will allow the bulk of any air that has been trapped in the mix during the decanting process to be released naturally back into the environment. If the reservoir is equipped with a stirrer, then this should be set to a low speed not to incorporate air during the mixing process. Also, make sure that the lines of the dispensing equipment are fully bled of air before commencing production.

It is good practice to check the shot weights of both components of the resin periodically during the day to ensure that the dispensing equipment is operating reliably. If the weights begin to drift significantly, this could be a sign that the pumps are not working correctly, such as air coming into the system from a split pipe or leaking coupling, or the pipe was not properly bled before starting.

Polyurethane resins are susceptible to moisture, which will react more readily with the hardener to release bubbles of carbon dioxide, adversely affecting the cure. Meanwhile, silicone resins are sensitive to certain chemicals that can inhibit the cure of silicone encapsulants. When using polyurethane and silicone resins, it is essential to ensure that the pipes and reservoirs are both clean and dry before filling with these materials.

Desiccant towers or a supply of dry air or nitrogen should be used to keep the system as dry as possible. It is also important to ensure that material containers are kept closed at all times when not in use, and that desiccant towers fitted to automated equipment are regularly monitored. The desiccant medium, which is usually either a molecular sieve or silica gel, should also be renewed as necessary. Moreover, the relative humidity of the mixing, dispensing, and curing environments should be monitored and ideally kept below 70%; otherwise, the ingress of moisture can lead to blocked pipes, cured materials in the reservoir, and pumps seizing as a result of fouling by cured materials.

In the case of heavily filled resin systems, these will always show signs of sedimentation over time; thus, it is best to operate a policy where the oldest material is used first in production to maintain good stock rotation. Make sure that the material is properly dispersed before use or as it is being decanted into a reservoir. Try to keep only one day's worth of material in the reservoir at a time. Also, use a stirrer operating at its lowest speed setting to keep the material agitated, which will ensure that any fillers contained within the resin disperse correctly.

Heating the resin will help to lower its viscosity, allow the mixed system to flow more readily, and make it easier to process. A note of caution—heating will reduce the useable life and the gel times of the mixed resin system, and where polyurethanes are concerned, heating of the hardener is not recommended.

If your production volumes are low, you are more than likely to use resin packs, which provide accurate weights of both hardener and resin. When using these handy packs, always make sure that the two components are correctly mixed before use. In particular, pay careful attention to releasing any material that may linger in the corners of the pack; otherwise, you will have an incorrect mix ratio in the material being dispensed.

If lots of small volume units are to be potted by resin pack, it is often easier to use a smaller pack size and have better control over dispensing the material rather than a single large volume pack, which can be difficult to control when attempting to dispense the correct amount of resin.

Overall, pay attention to these basic do's and don'ts and you are likely to achieve the levels of reliability and long service life that will ensure happy relationships with your customers. **DESIGN007**

Alistair Little is global business/technical director at Electrolube. To read past columns from Electrolube, click here. To download your copy of Electrolube's micro eBook, *The Printed Circuit Assembler's Guide to... Conformal Coatings for Harsh Environments*, click here.

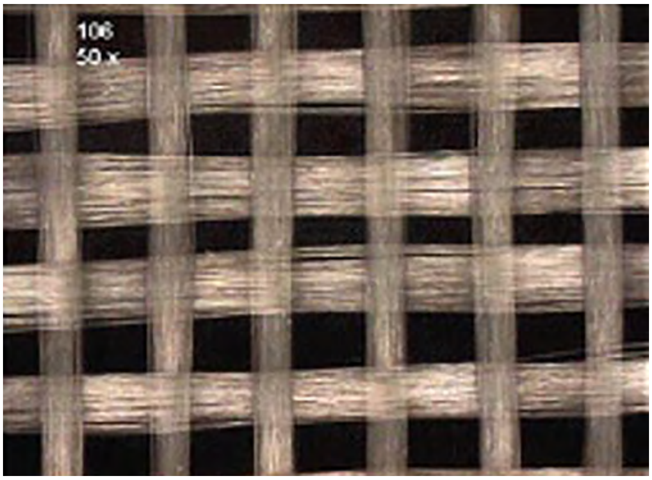


Figure 1a: Fiber weave with a 106 configuration.

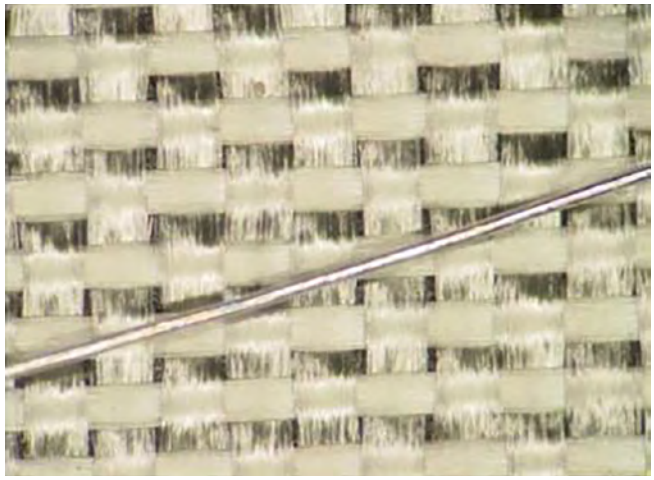


Figure 1b: Fiber weave with a 3313 configuration.

Effects of PCB Fiber Weave on High-Speed Signal Integrity

by Chang Fei Yee
KEYSIGHT TECHNOLOGIES

This article studies the effect of PCB fiber weave on signal integrity in terms of mode conversion and differential channel loss due to intra-pair skew. The study used Keysight ADS 2DEM simulation to observe s-parameter (i.e., insertion loss and differential to common-mode conversion) and eye diagram for signal transmission at 1 Gbps and 10 Gbps.

Introduction

A PCB dielectric substrate is composed of woven fiberglass that is strengthened by epoxy resin. The microscopic top view of PCB substrates of fiber weave 106 and 3313 are illustrated in Figures 1a and 1b. The thick lines in light brown color are fiberglass, while the square columns in black color are an epoxy resin. A higher-numbered configuration (e.g., 3313) denotes denser fiberglass weave.

Fiberglass material features dielectric properties that differ very much from the properties of the epoxy resin. For instance, NE-glass fiber has a dielectric constant (Dk) and loss tangent (Df) of 4.4 and 0.0006, respectively; meanwhile, E-glass fiber has a Dk and Df of 6.6 and 0.0012. Epoxy resin has a Dk of 3.2, which is very different than that of fiberglass. When a substrate with sparse fiber weaving is used, PCB traces could cross different regions of resin and fiberglass more frequently. As a result, the speed or propagation delay of the signal changes frequently along the trace from transmitting to receiving end. The relationship between them is governed by Equation 1.

$$v = \frac{c}{\sqrt{D_k}} \qquad \text{Equation 1}$$

v = signal's speed on PCB (in unit inches/ns)
c = speed of light (12 inches/ns)
D_k = dielectric constant

This phenomenon poses a critical challenge to multi-gigabit serial signal transmission. In the worst-case scenario, for example, the trace of a non-inverting signal could be routed on fiberglass without crossing the resin region

while the trace of the inverting signal could cross many resin regions. As a result, due to the consistent change in propagation delay experienced by the inverting signal, the phase difference between non-inverting and inverting signals in common mode could be much less than 180°C at the receiving end. The large extent of skew or misalignment between the rising and falling edges leads to the reduction of width and height of the eye diagram. Ultimately, a high bit error is experienced by the receiver.

Two case studies are performed to investigate the effect of fiber weave on high-speed signal integrity. In the first case study, the effect of various non-homogeneous substrates (i.e., when the substrate segment of the non-inverting signal does not have the same dielectric properties as the inverting signal) and segment length experienced by the signal are studied. The entire transmission channel is fixed at 5 inches in length. The non-homogeneous substrate segment increases from 10% to 50% of the total channel length. This case study is performed for channel models on PCB microstrip and stripline. All of the simulation models for Case Study 1 are listed in Table 1, where NE-glass fiber is applied.

In the second case study, the effect of different fiberglass materials on the signal transmission is investigated. The entire transmission channel length is set at 5 inches, while the non-homogeneous substrate segment length is set as 0.5 inches or 10% of the total channel length. This case study is performed for channel models on PCB microstrip and stripline respectively. All of the simulation models for Case Study 2 are listed in Table 2, where NE-glass and E-glass fiber are chosen as materi-

Simulation model	PCB layer	Length of homogeneous segment (inches)	Length of non-homogeneous segment (inches)	Total T-line (inches)
1A	Microstrip	5	0	5
1B	Microstrip	4.5	0.5	5
1C	Microstrip	4	1	5
1D	Microstrip	3.5	1.5	5
1E	Microstrip	3	2	5
1F	Microstrip	2.5	2.5	5
1G	Stripline	5	0	5
1H	Stripline	4.5	0.5	5
1I	Stripline	4	1	5
1J	Stripline	3.5	1.5	5
1K	Stripline	3	2	5
1L	Stripline	2.5	2.5	5

Table 1: Simulation models for Case Study 1.

Simulation model	PCB layer	Length of homogeneous segment (inches)	Length of non-homogeneous segment (inches)	Total T-line (inches)	Fiberglass material
2A	Microstrip	5	0	5	NE-glass
2B	Microstrip	4.5	0.5	5	NE-glass
2C	Microstrip	4.5	0.5	5	E-glass
2G	Stripline	5	0	5	NE-glass
2H	Stripline	4.5	0.5	5	NE-glass
2I	Stripline	4.5	0.5	5	E-glass

Table 2: Simulation models for Case Study 2.

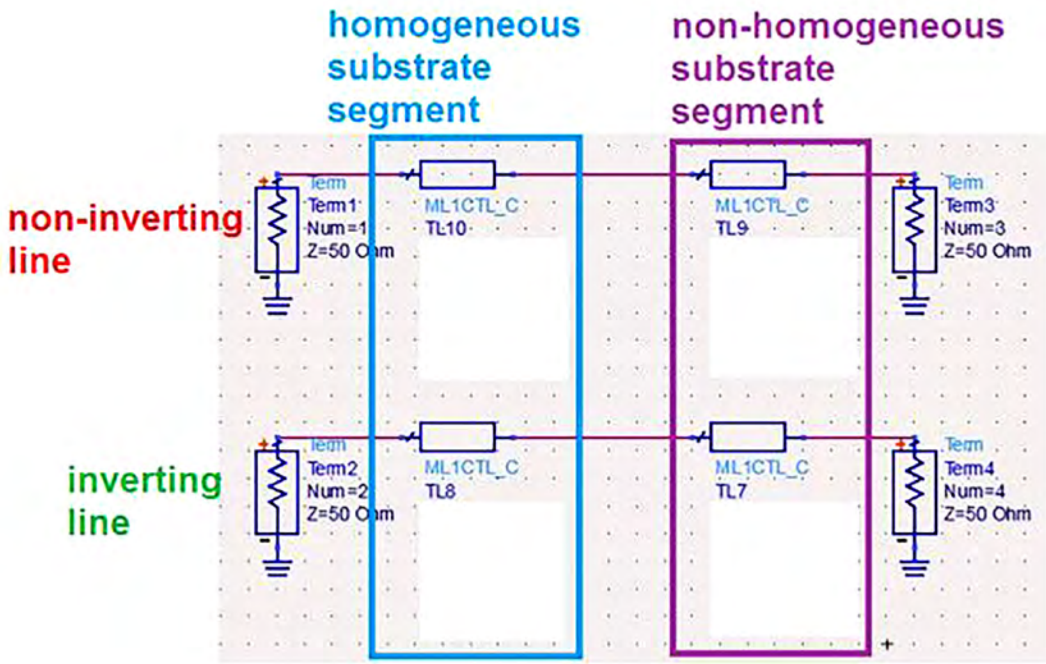


Figure 2: Simulation topology of an s-parameter.

als for comparison. The analysis is conducted using the 2DEM solver in Keysight ADS.

For both case studies, analysis of differential insertion loss, mode conversion, intra-pair skew, and eye diagram at the receiver are conducted. Results of the analysis are presented and discussed in the next section.

Analysis and Results

Case Study 1

A simulation of s-parameter with topology shown in Figure 2 is performed to study the impact of non-homogeneous substrate segment length on signal transmission.

The 4-port single-mode insertion loss was converted to differential mode (i.e., Sdd21) using the math function in ADS. The plots of Sdd21 for microstrip and stripline are shown in Figures 3a and 3b. These plots indicate that resonance frequency or channel bandwidth gets lower when the overall non-homogeneous segment becomes longer for both microstrip and stripline models.

The plots of mode conversion from differential to common (i.e., Scd21) for microstrip and stripline are shown in Figures 4a and 4b. A smaller absolute magnitude of Scd21 in dB indicates more easily differential is converted to common mode, which is encountered by

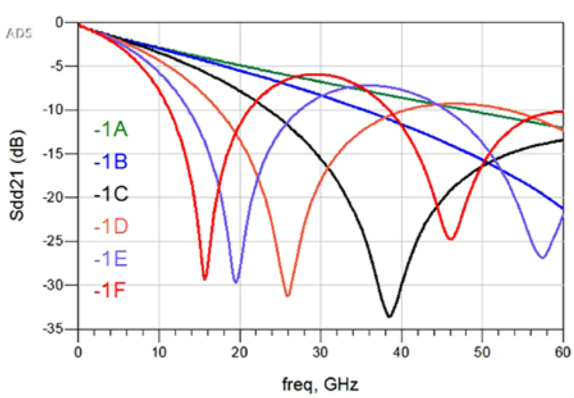


Figure 3a: Sdd21 for microstrip.

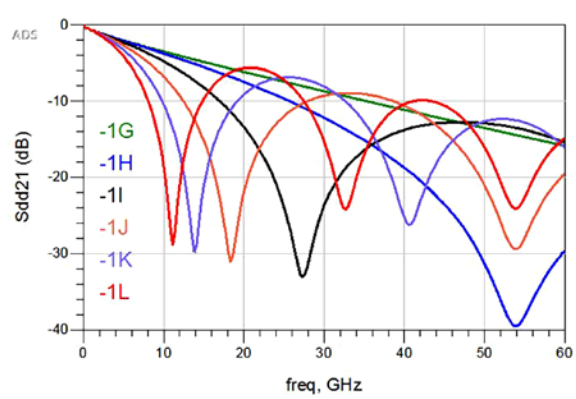


Figure 3b: Sdd21 for stripline.

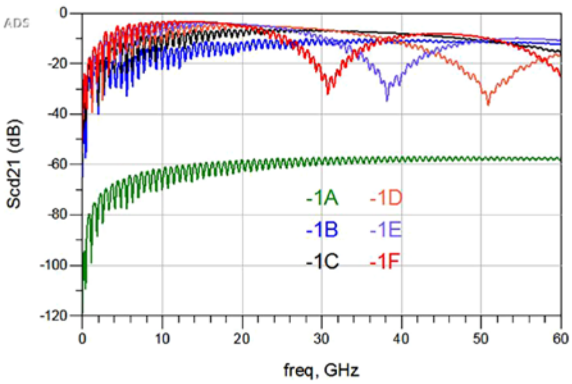


Figure 4a: Scd21 for microstrip.

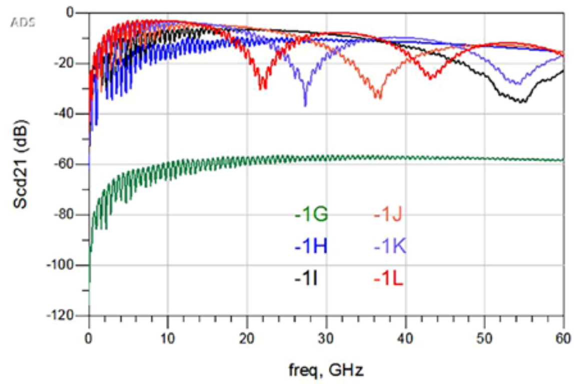


Figure 4b: Scd21 for stripline.

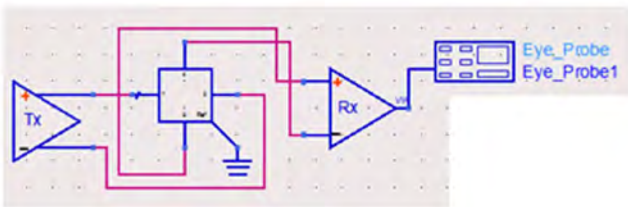


Figure 5: Simulation topology of the eye diagram.

transmission channel with longer non-homogeneous substrate segment on PCB. This weakens the immunity of the channel against common-mode noise or crosstalk.

Besides analysis in the frequency domain, the study is also performed in the time domain (i.e., eye diagram and intra-pair skew) with simulation topology depicted in Figures 5 and 6. In these two analyses, a differential signal with a 600 mVpp amplitude at 1 Gbps (35 ps rise-fall time) and 10 Gbps (5 ps rise-fall time) is injected into the transmission line models listed in Table 1. The results of intra-pair skew and eye-opening are summarized in Table 3.

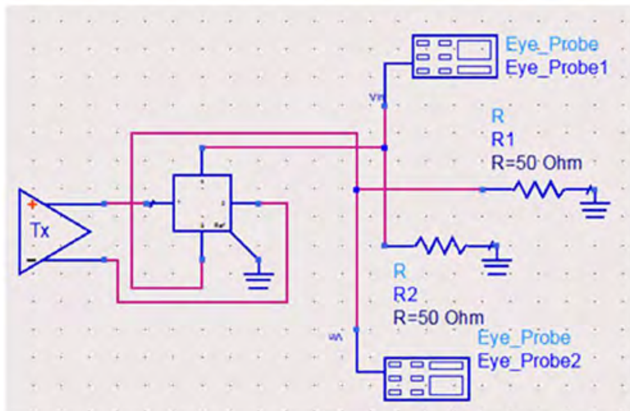


Figure 6: Simulation topology of an intra-pair skew.

Simulation model	PCB layer	Intra-pair skew (ps)	Eye height (mVpp) at 1 Gbps	Eye width (ps) at 1 Gbps	Eye height (mVpp) at 10 Gbps	Eye width (ps) at 10 Gbps
1A	Microstrip	0	477	985	452	98
1B	Microstrip	6.3	477	985	447	98
1C	Microstrip	12.5	477	985	444	97.5
1D	Microstrip	18.8	477	985	439	95
1E	Microstrip	25	477	985	420	94.5
1F	Microstrip	31.3	477	985	403	94
1G	Stripline	0	472	980	434	97
1H	Stripline	9.4	472	980	427	97
1I	Stripline	20	472	980	423	95
1J	Stripline	27.4	472	980	420	94.5
1K	Stripline	36.7	472	980	407	93
1L	Stripline	45.3	472	980	399	90.5

Table 3: Summary of skew and eye-opening.

In Table 3, at 1 Gbps signal transmission, the attenuation at the receiving end is due to dielectric loss. The intra-pair skew due to non-homogeneous length up to 50% of 5 inches does not have a significant impact on attenuation. However, at 10 Gbps, the signal attenuation at the receiving end is more than 5% contributed by the non-homogeneous length up to 40% of 5 inches. This poses a critical impact to the signal integrity at 10 Gbps and beyond. A larger intra-pair skew worsens the jitter and attenuation of the channel, which is indicated by the smaller eye width and height.

Case Study 2

Simulation of the s-parameter illustrated in Figure 2 was conducted to study the impact of fiberglass materials on signal integrity. The plots of Sdd21 for microstrip and stripline are shown in Figures 7a and 7b. These plots indicate that with the same non-homogeneous length on the substrate, the channel on NE-glass experiences lower attenuation compared to E-glass. This is due to the fact that the difference in dielectric constant values between NE-glass and resin is smaller compared to E-glass and resin. This weakens the non-homogeneous effect.

The plots of Scd21 for microstrip and stripline are shown in Figures 8a and 8b. A larger absolute magnitude of Scd21 indicates that tougher for differential be converted to common mode, which is encountered by transmission channel with NE-glass versus E-glass fiber. This strengthens the immunity of the channel against common-mode noise or crosstalk.

As in Case Study 1, this study was also performed in the frequency and time domains. In these two analyses, a differential signal with a 600 mVpp amplitude at 1G bps (35 ps rise-fall time) and 10 Gbps (5 ps rise-fall time) is injected into the transmission line models listed in Table 2. The results of intra-pair skew and eye-opening are summarized in Table 4.

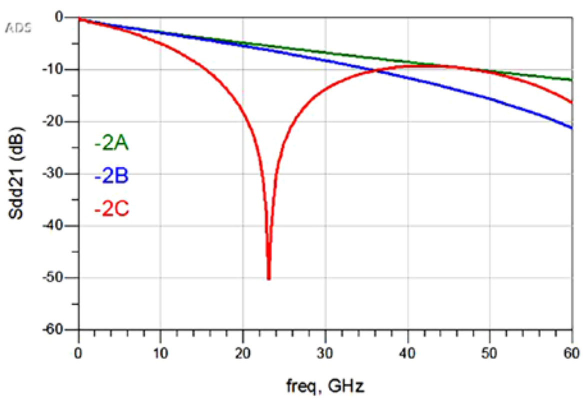


Figure 7a: Sdd21 for microstrip.

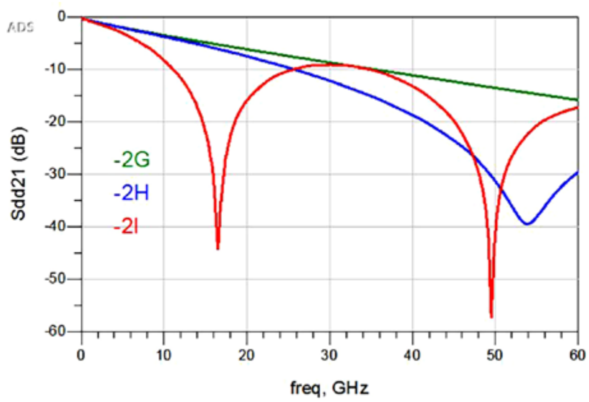


Figure 7b: Sdd21 for stripline.

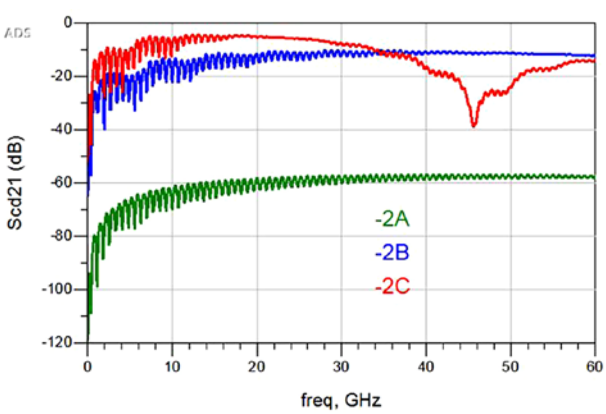


Figure 8a: Scd21 for microstrip.

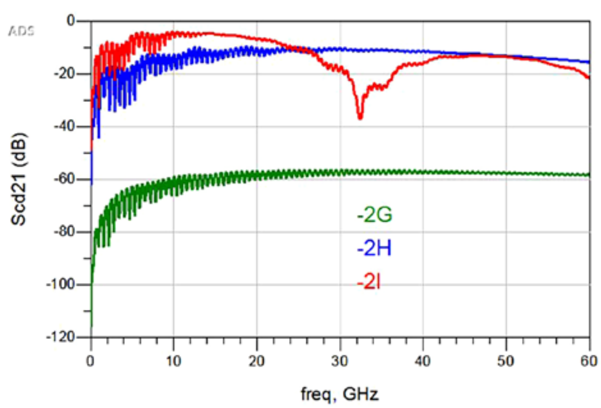


Figure 8b: Scd21 for stripline.

Simulation model	PCB layer	Intra-pair skew (ps)	Eye height (mVpp) at 1 Gbps	Eye width (ps) at 1 Gbps	Eye height (mVpp) at 10 Gbps	Eye width (ps) at 10 Gbps
2A	Microstrip	0	477	985	452	98
2B	Microstrip	6.3	477	985	447	98
2C	Microstrip	28.9	476	984	426	96
2G	Stripline	0	472	980	434	97
2H	Stripline	9.4	472	980	427	97
2I	Stripline	28.9	472	978	409	93

Table 4: Summary of skew and eye-opening.

In Table 4, at 1-Gbps signal transmission, the attenuation at the receiving end is due to dielectric loss. The intra-pair skew due to the non-homogeneous length up to 10% of 5 inches using either NE-glass or E-glass does not have a significant impact on attenuation. However, at 10 Gbps, the signal attenuation at the receiving end is more than 5% contributed by the non-homogeneous length up to 10% of 5 inches for E-glass versus NE-glass. This poses a critical impact on the signal integrity at 10 Gbps and beyond. A larger intra-pair skew worsens the jitter and attenuation of the channel, as indicated by the smaller eye width and height respectively.

Summary

In multi-gigabit transmission, NE-glass fiber with denser weave such as 3313 shall be applied in PCB substrate to minimize the attenuation and intra-pair skew, which strengthens the signal integrity. The attenuation due to fiber weave effect shall be kept below 5% to allow more headroom for channel loss contributed by other factors, such as dielectric loss, copper surface roughness, etc. **DESIGN007**

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5. E. Chua, J. Zhang, & K. See. "A study on fibre weave effect on intra-pair skew of differential lines using analytical approach." IEEE, 2017.

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Chang Fei Yee is a hardware engineer with Keysight Technologies. His responsibilities include embedded system hardware development, and signal and power integrity analysis.

New Insulating State Found in Stretched Graphene

By using the powerful K supercomputer to simulate with unprecedented accuracy what happens to graphene as it is stretched, RIKEN researchers have discovered a new state of the material.

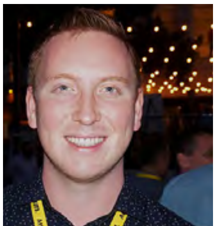
Graphene is being intensively investigated for applications ranging from electronics and energy storage to optics and even tissue engineering. But graphene still needs to be integrated with non-conducting or insulating elements to provide useful functionality. For many years, Seiji Yunoki from the RIKEN Center for Computational Science has been seeking to ascertain the conditions under which graphene switches from conducting to insulating.

Now, by using quantum simulation methods that model electron interactions explicitly, Yunoki and his colleagues have discovered that graphene instead transitions to a more exotic nonmagnetic topological state called a Kekulé-like dimerized nonmagnetic insulator, which could have interesting technological applications.

"This discovery only became possible using our quantum Monte Carlo simulations, for which RIKEN's K computer was essential due to the extremely heavy computations involved," notes Yunoki. (Source: RIKEN)

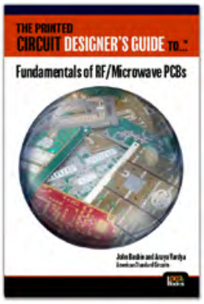
Editor Picks from PCBDesign007

1 Amway Sells Beauty Products—and Designs its Own PCBs ▶


Dugan Karnazes

The company is famous for selling nutritional supplements and soap, but apparently Amway has been busy diversifying over the years. Dugan M. Karnazes, an Amway associate electrical engineer and PCB designer discusses his role and how this company grew into an $8 billion global giant.

2 RF/Microwave eBook: Beneficial Tool for Engineers ▶



Released earlier this year, hundreds of engineers and other readers interested in PCB design have downloaded *The Printed Circuit Designer's Guide to… Fundamentals of RF/Microwave PCBs* micro eBook

3 Simon Fried: Additive Manufacturing Through Printed Electronics ▶

Simon Fried, president of Nano Dimension, discusses how the company has taken the additive manufacturing process to the next level through printed electronics.

4 Karl-Heinz Fritz on Cicor's DenciTec Technology ▶


Karl Heinz-Fritz

In a recent interview, Karl-Heinz Fritz, VP of technology at Cicor, discusses the business, DenciTec technology, the impact of tariffs on trade, and applications for 3D printing and additive manufacturing, including potential new opportunities for PCB designers.

5 Rick Hartley is Bullish on PCB Design, 3D Printing ▶


Rick Hartley

At the recent PCB West in Silicon Valley, Consulting Technical Editor Tim Haag met with long-time design industry veteran Rick Hartley to discuss the changing landscape of circuit board design, the layout designers of the future, and how designers can benefit from 3D printing of circuit boards.

6 Book Review: *The Printed Circuit Board Designer's Guide to... Producing the Perfect Data Package* ▶

Over the course of his career, Mark Thompson, CID+, engineering support at Prototron Circuits, has evaluated thousands of data packages and delivered numerous talks to designers and engineers about how to create the perfect package. In the spirit of "garbage in, garbage out," data packages must be perfect to create quality boards. Learn all this and more in *The Printed Circuit Designer's Guide to… Producing the Perfect Data Package!*

7 One-Question Survey, Part 2: What Advice Would You Offer a New Designer? ▶

During AltiumLive 2018, the I-Connect007 editorial team asked some of the attendees to answer one question: What advice would you offer to a brand-new PCB designer? Here are just a few of the replies we received. Read how John Watson from Legrand, Cherie Litson of EPTAC and Francis Allotey from Ward Leonard answered this question.

8 Catching up With Scott McCurdy and Freedom CAD ▶


Scott McCurdy

During PCB West, Scott McCurdy of Freedom CAD Services sat down with Technical Editor Tim Haag for an interview. We discussed Freedom CAD's latest news, some trends in PCB design software tools, and the continuing need to draw more young people into a career in PCB design.

9 Cadence: Bullish on AI ▶

David White has been involved with artificial intelligence research for almost 30 years. Now, David is the senior group director of R&D for Cadence Design Systems, and I knew we'd have to speak with him for this issue on AI. In a recent interview, we discussed his decades of work in AI, Cadence's research into AI and machine learning, and what he believes AI could mean for the EDA tools of the future.

10 Darwin E. George: Seeking PCB Design Job at Retirement Age ▶


Darwin George

Some of us dream of living a life of leisure at 70. But not Darwin E. George. This septuagenarian wants to find a job designing PCBs. We met up with Darwin at AltiumLive, where he was networking and trying to get his foot in the door with one of the companies that are hiring now. Darwin told us about his career in PCB design, his experience learning a new EDA tool, and why he would rather design high-speed PCBs instead of playing shuffleboard for the rest of his life.

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- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Produce service reports
- Cooperate with the technical team and share information across the organization
- Assist with the crating and uncrating of equipment

Requirements and Qualifications:

- Three to five years of experience with SMT equipment or an equivalent technical degree
- Proven strong mechanical and electrical trouble-shooting skills
- Proficient in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Organized, detail orientated, and capable of multitasking
- Have strong written and oral interpersonal skills with an ability to work under minimum supervision
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- EXPERT knowledge of Allegro 16.6/17.2
- Passionate about your PCB design career
- Skilled at HDI technology
- Extensive experience with high-speed digital, RF and flex and rigid-flex designs
- Experienced with signal integrity design constraints encompassing differential pairs, impedance control, high speed, EMI, and ESD
- Experience using SKILL script automation such as dalTools
- Excellent team player that can lead projects and mentor others
- Self-motivated, with ability to work from home with minimal supervision
- Strong communication, interpersonal, analytical, and problem solving skills
- Other design tool knowledge is considered a plus (Altium, PADS, Xpedition)

Primary Responsibilities

- Design project leader
- Lead highly complex layouts while ensuring quality, efficiency and manufacturability
- Handle multiple tasks and provide work leadership to other designers through the distribution, coordination, and management of the assigned work load
- Ability to create from engineering inputs: board mechanical profiles, board fabrication stack-ups, detailed board fabrication drawings and packages, assembly drawings, assembly notes, etc.

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Product Group Field Manager Waterbury, CT

The Product Group Field Manager is responsible for creating and driving the regional product line strategic plan in coordination with the global product line managers, strategic account manager and regional business managers. The successful candidate must balance commercial obligations to assist the sales teams in closing new business, perpetuating technical expertise throughout the field and develop best practices for the region.

Education: Bachelor's degree; 5 years of related experience; or equivalent combination of both.

Responsibilities

- Thorough understanding of the PCB business; specifics in wet processing areas.
- Facilitate developing commercial and technical strategy for customers.
- Create and deliver customer facing presentations.
- Training.
- Create and execute a product rationalization program aligning with global product managers.
- Develop roll-out packages for new product introductions, including operating guides.
- Excellent written and oral communication skills.
- Expert in chemistry and chemical interaction within PCB manufacturing.
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- Modify customer supplied data files and interface with customers and engineers
- Responsible for releasing manufacturing tooling to the production floor
- Prepare NC tooling for machine drilling, routing, imaging, soldermask, silkscreen
- Netlist test, optical inspection
- Work with Production on needed changes
- Suggestions on continual improvements for engineering and processing.
- Be able to read write and communicate in English
- Must understand prints specifications
- Must be US Citizen or permanent resident (ITAR)
- High School Graduate or equivalent

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Role: Vice President Gardien Taiwan

TAOYUAN COUNTY, TAIWAN

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Candidate Profile:

- Proficiency in Chinese and English (written and spoken)
- Excellent communication and organization skills
- Experience in change management
- PCB background appreciated, but not mandatory
- Management experience in internationally operating companies
- Savvy in standard office software (Word, Excel and Power Point)

If this sounds like you, please click here to send us an email with your attached CV.

About Gardien Group - Gardien is the world's largest international provider of independent testing and QA solutions to the PCB industry with a global footprint across 24 service centres in five countries and we cater to a whole range of customers, from small family owned PCB shops to large international fabricators. Gardien's quality solutions and process standards are trusted by leading high-tech manufacturers and important industries including aerospace, defense, and medical technology.

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- Assist in resolving customer complaints and queries
- Meet deadlines and financial goal minimums
- Make recommendations to the customer
- Maintain documentation of customer communication, contact and account updates

Job requirements:

- Located in Mexico
- Knowledge of pick-and-place and electronics assembly in general
- 3+ years of sales experience
- Customer service skills
- Positive attitude
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The successful candidate is expected to have solid experience within the PCB assembly industry and the ability to represent the Valor solutions with authority and credibility. A solid background in PCB Process Engineering or Quality management to leverage in day-to-day activities is preferred. The candidate should be a good "storyteller" who can develop relatable content in an interesting and compelling manner, and who is comfortable in presenting in public as well as engaging in on-line forums; should have solid experience with professional social platforms such as LinkedIn.

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HKPCA/IPC International Printed Circuit & South China Fair ▶
December 5–7, 2018
Shenzhen, China

IEEE Rising Stars Conference ▶
January 4–6, 2019
Las Vegas, Nevada, USA

48th NEPCON JAPAN ▶
January 16–18, 2019
Tokyo Big Sight, Japan

IPC APEX EXPO 2019 ▶
January 26–31, 2019
San Diego, California, USA

DesignCon ▶
January 29–31, 2019
Santa Clara, California, USA

MD&M West 2019 ▶
February 5–7, 2019
Milan, Italy

IPC High Reliability Forum ▶
May 14–16, 2019
Hanover (Baltimore), Maryland, USA

Additional Event Calendars

IPC

SMTA Surface Mount Technology Association

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