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NOVEMBER 2020

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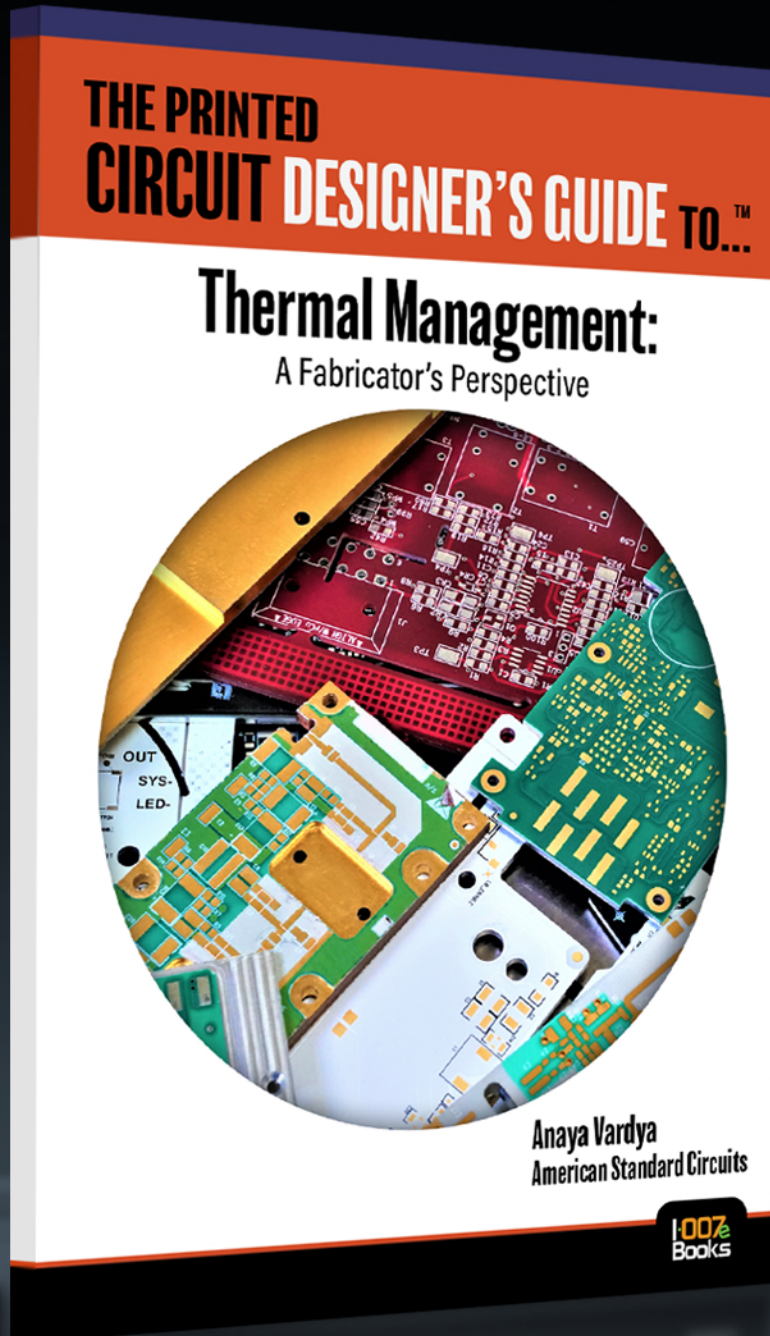
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The Via Issue

There has been quite a bit of activity in the world of vias, especially microvias. Military contractors have been experiencing microvia failures that occur during reflow but remain undetectable at room temperature. A failure that you can't detect is never a good thing, especially if you're building PCBs for missiles or fighter planes.

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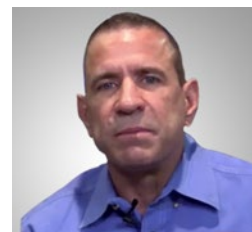
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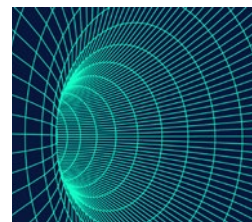
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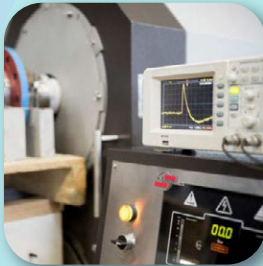


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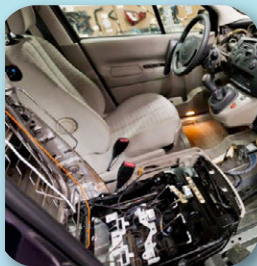
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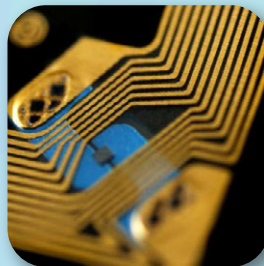
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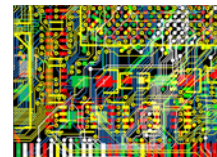


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Integrated Tools to Process PCB Designs into Physical PCBs



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Use manufacturing data to generate a 3D facsimile of the finished product.



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Ensure that manufacturing data is accurate for PCB construction.



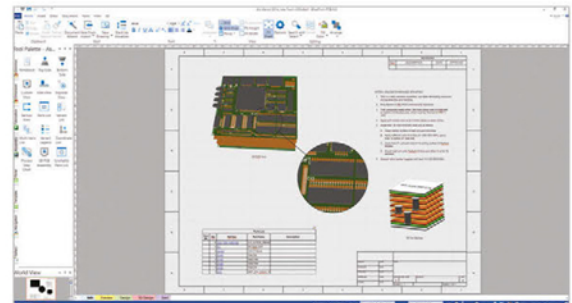
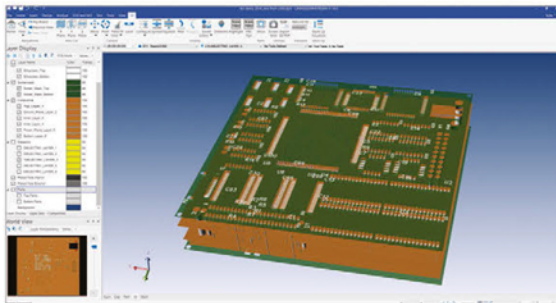
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This Month in Flex

Flexible and rigid-flex circuits offer a variety of advantages over their rigid brethren. But there are dozens of potential hurdles awaiting flex designers, especially those transitioning from the rigid world. Designing vias for a flexible circuit is a unique process with its own set of challenges.

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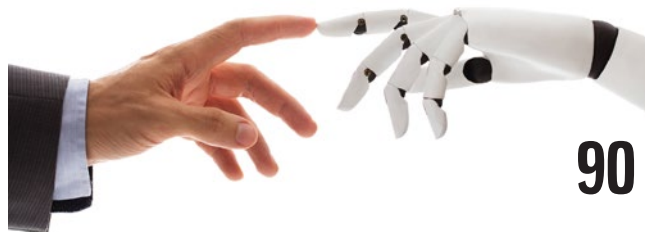
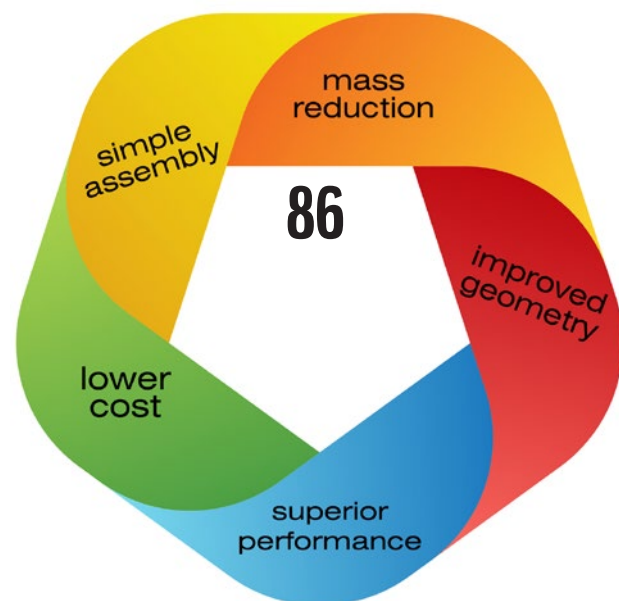
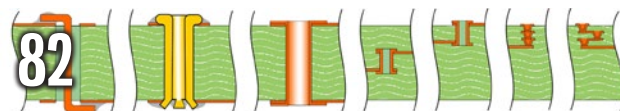
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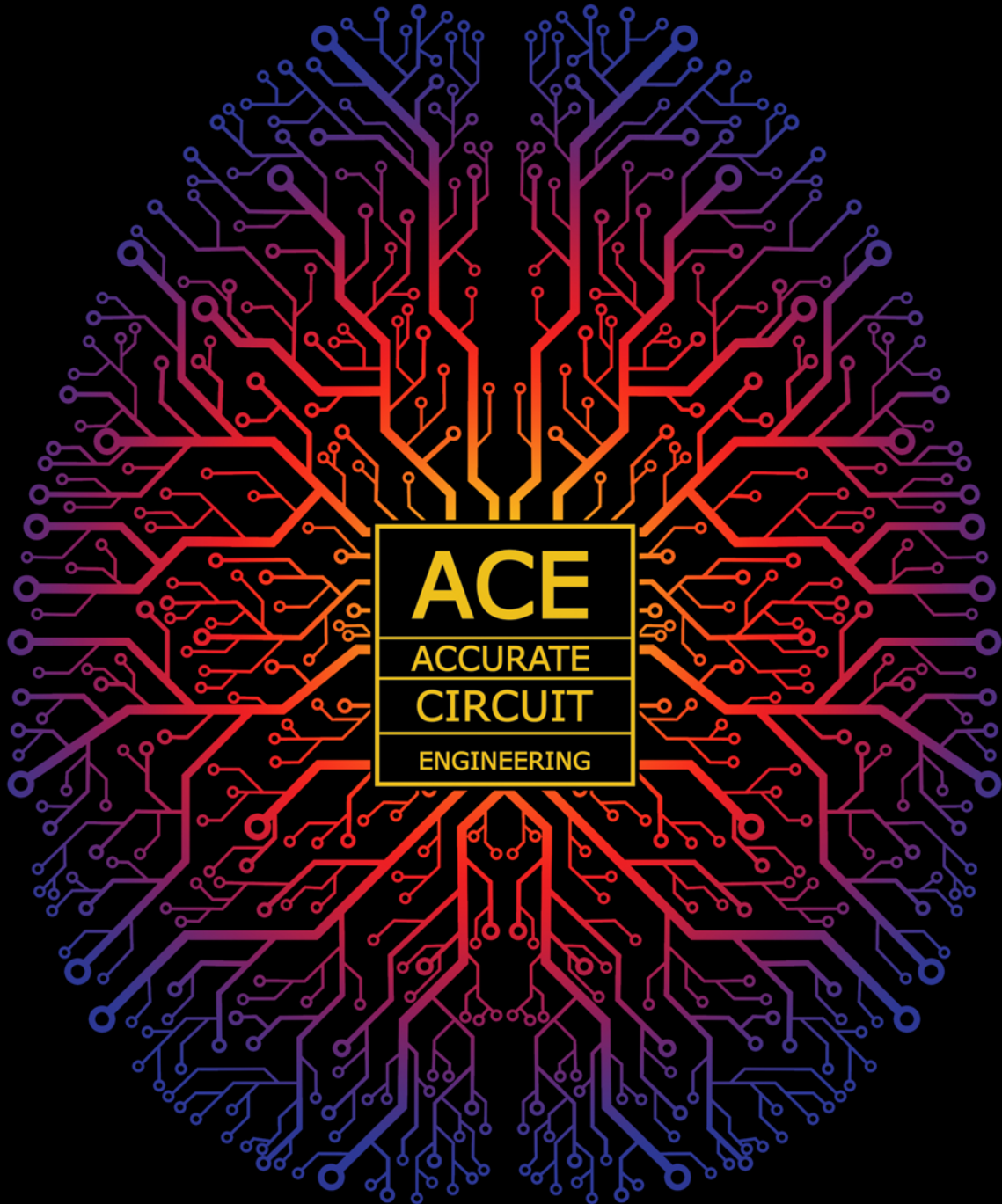
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Time to Make the Vias

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

When we started planning this issue on via design, I was reminded of the Dunkin' Donuts commercials from the 1980s. The commercials starred a sleepy character named Fred the Baker dragging himself out of bed before dawn, muttering his mantra, "Time to make the donuts." Dunkin' Donuts retired Fred's character in 1997 and gave away six million donuts in his honor.

With its annular ring, a finished via has always reminded me of a donut, and it's not much more complicated. A via is basically just a fancy hole, yet the industry continues to have issues with vias.

You've heard stories of the OEMs who send out a dozen test boards, chock full of vias, to a dozen fabrica-

tors to get a feel for how they manufacture their vias. And they get back a dozen boards with vias built in a dozen different ways.

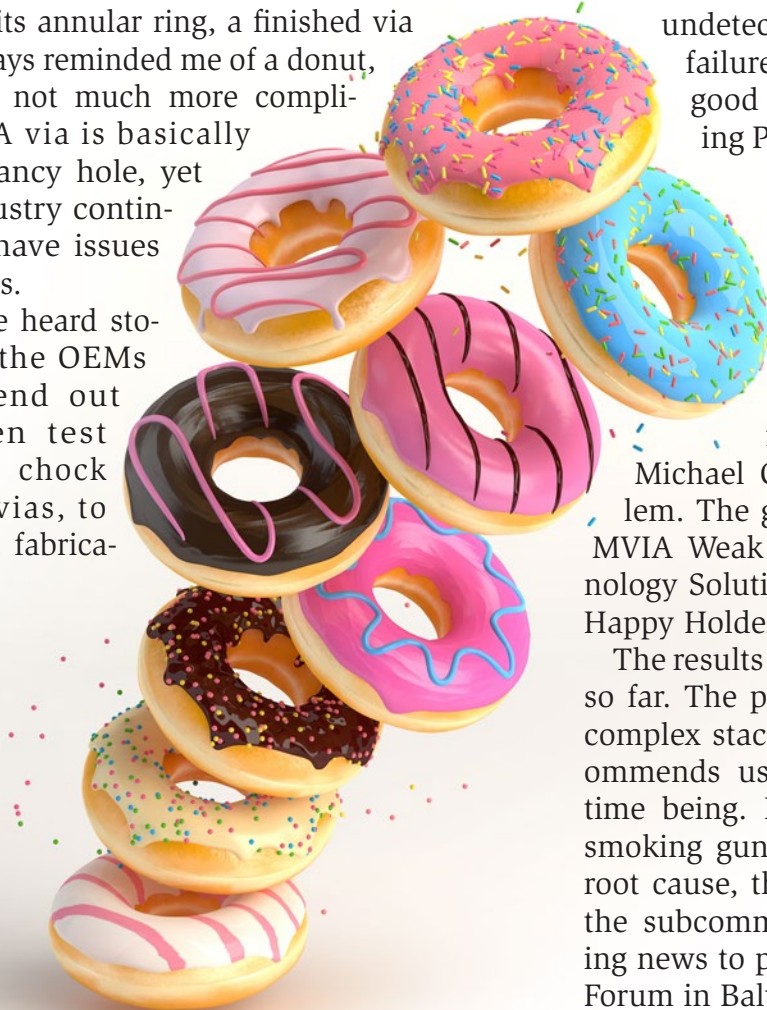
Vias are usually in the top five when we survey readers about their biggest challenges, and there has been quite a bit of activity in the world of vias, especially microvias. Military contractors have been experiencing microvia failures that occur during reflow but remain undetectable at room temperature. A failure that you can't detect is never a good thing, especially if you're building PCBs for missiles or fighter planes.

In response, IPC recently came out with new thermal test methods that require the coupon to undergo a solder paste reflow profile to reach 230°C or 260°C, where the latent failures can be observed. IPC also formed a group of experts, led by

Michael Carano, to investigate this problem. The group, now known as the V-TSL-MVIA Weak Interface Microvia Failure Technology Solutions Subcommittee, also includes Happy Holden as a founding member.

The results of their research have been mixed so far. The problem seems to be restricted to complex stacked microvias, so this group recommends using staggered microvias for the time being. But there doesn't seem to be a smoking gun. (If anyone has figured out the root cause, they're not sharing it.) Hopefully, the subcommittee will have some encouraging news to present at the IPC High-Reliability Forum in Baltimore, Maryland, next May.

For this issue, we lined up a group of expert contributors to discuss the best methods for



designing reliable vias and microvias. First, we start with an interview with PCEA Chairman Stephen V. Chavez, Happy Holden, and Dan Feinberg, who discuss everything from microvia failures to the challenges the designers face when laying out ever-shrinking traces and components. Next, James Hofer of Accurate Circuit Engineering explains the problems he encounters with customers' HDI designs, particularly with PTFE laminates, and some of the remedies he utilizes, such as landless vias.

We have a really informative "Stacked Microvia/Weak Interface Reliability Study" edited by Happy Holden, which provides a snapshot of the investigation into the military microvia failures and the work that remains to be completed from Marc Carter's IPC High-Reliability Forum presentation. Tim Haag discusses the many ways that vias can alleviate pain on one part of the board but can cause trouble elsewhere when designers don't follow best practices. Mark Thompson, CID+, offers a wide-ranging look at the design and fabrication of vias and microvias and shares examples that illustrate why attention to detail and communication are so vital to via design. And Joe Fjelstad shares a brief history of vias from the 1950s on.

We have an article by John McMillan of Mentor, a Siemens Business, that focuses on criteria for selecting your next PCB design software tool. And Chris Clark of Minco discusses how rigid-flex circuits are now driving innovation around the world. We also have columns from regular contributors Jade Bridges, Barry Olney, Matt Stevenson, Kelly Dack, Patrick Crawford, John Talbot, and Dominique Numakura.

We're coming up on the end of the year, and I, for one, can't wait for 2021. Next year is looking promising so far. IPC APEX EXPO and DesignCon are set for live, in-person events in March and April, respectively, and PCB East is making a comeback, set for May in Marlborough, Massachusetts, which will also be a live event.

If these events go as planned, we'll be there to provide complete coverage. Let's hold a good thought! **DESIGN007**



Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 20 years. He can be reached by clicking [here](#).

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Stephen Chavez and Happy Holden on Designing **Reliable** Vias

**Feature Interview by the I-Connect007
Editorial Team**

Andy Shaughnessy and Happy Holden speak with Stephen Chavez, a staff engineer with an aerospace company and chairman of the Printed Circuit Engineering Association (PCEA), about designing vias for greater reliability. They also address several areas where they can look to improve reliability, a variety of steps that designers should take to help ensure more robust vias, and some testing and educational resources that PCB designers and design engineers should be aware of.

Andy Shaughnessy: Welcome, gentlemen. Companies keep having problems with vias. Some OEMs will send out a dozen test boards with different-sized vias to a dozen different fabricators, and they'll come back built a dozen different ways. What can the designers do? What are your thoughts on via design for reliability?

Stephen Chavez: My initial thought on this is that at the earliest stages of the design cycle, communication with your suppliers is an extremely important part of your overall PCB

design success. Collaborating with your supplier to lock in your PCB stackup is also a vital step in the early stages of your design. This leads to solidifying your constraints before parts are placed and any traces are routed, which includes the types of via technology that will be implemented in the design. By collaborating with your suppliers and applying industry best practices for PCB design, the odds of achieving a robust, high-reliability DFM design is very good.

As today's printed circuit engineers strive to meet today's challenges, there are three competing perspectives for success when designing PCBs: design for layout solvability (DFS); design for performance (DFP), meaning SI/EMC, power delivery, and thermal; and design for manufacturability (DFM). In the end, the main goal is to get it right the first time. Make Revision 1 work by maximum placement and routing density, optimum electrical performance, and efficient, defect free manufacturing to achieve high yield and lower cost.

When I talk about meeting today's challenges when designing multilayer PCBs while keeping in mind the three competing perspectives for success, the via strategy and quality



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of the via structure is very important. No matter which via technology you utilize in your design—whether it is standard PTH, HDI, microvias, or a combination of the three—you want it designed so that the via is in the board fabricator’s sweet spot while meeting your design requirements and DFM for downstream optimization. If you’re not doing that, you’ll be having a lot of problems. I am still surprised to find there are many people who aren’t talking to their suppliers, and they’re just throwing the design over the fence.

Then, you have to understand the material you’re choosing. Are you choosing the right material for your application and the widget that you’re building? Are you designing in the core sweet spots for success, or are you pushing the rail on complexity? You had better be speaking and understanding the industry terminology and language when talking to your supplier to make sure that you’re on the same page so that there are no surprises at the end.

Happy Holden: If an OEM is naïve enough to send a board out to multiple vendors, they shouldn’t be surprised that they’ll come back different because every fabricator optimizes drilling, desmear, metallization, and plating to be as reliable as they can possibly make it. But because of the multiple vendors, machines, and processes, there are 10,000 different permutations and combinations that make up every multilayer. An OEM deserves whatever they lose if that’s the way they’re going to manage their supply chain. They should develop a qualification process that’s statistically significant, but they won’t, and the fabricators won’t tell them that they’re foolish.

And many OEMs don’t understand reliability, so they ask for 15 boards with a cross-section. That does not guarantee any kind of reliability at all because 15 boards are not statistically significant unless your entire year’s purchase



Stephen Chavez

is 15 boards. Also, a cross-section has been proven to be so unreliable to tell you about what’s really happening on the interconnect because you’re only looking at a plane cut through the hole. You’re not looking at all 360 degrees.

When companies hired me, I gave them a quality program that included reliability and used the IPC PCQR² methodology, which meant that the fabricator had to produce 250,000 holes in the qualification, or half a million holes if they chose the blind laser drill

to panel. But those boards were tested so, there was a 99.5% reliability confidence that there was less than a 0.5% error over the entire lifetime. And they redid that qualification every year. If there were coupons and things like that, then they tested on the same panel as the PCQR² so that there was traceability.

Most people don’t want to do that even though that’s money well spent. I worked a lot with Asian fabricators that supply Intel, and Intel’s qualification is 20,000 boards and modules, which Intel pays for, and they are split over an entire year. They want to know that the boards are made day and night, Monday through Friday or Saturday, summer and winter, because the measurements go up and down depending on seasons and a whole bunch of other factors.

But the people who really sink their money into reliability, like the packages for the Intel microprocessors, do it properly, and pay the fabricator to do that, so they have extremely high confidence and know exactly what they’re doing. But don’t order three boards or 15 boards and cross-section them, and think, “That’s a good fabricator.” They might be, but maybe not.

Do you think people really understand reliability and statistical significance?

Chavez: I’d like to think so, but there are still many that simply don’t understand or don’t

pay attention to the details. A lot of times, a company will qualify with one or two specific suppliers. Then, once a prototype moves into production, they want to start minimizing the expense, so they start looking to shop around to see where they can get it cheaper. And then that just blows everything out of the water at that point, because who knows what you're getting with regard to quality?

Holden: But if you want to read really good explanations about vias, go back to some of the publications by Intel and other aerospace companies around 2000, when they were starting to qualify microvia vendors and using the IPC benchmark PCQR², and you'll see there's a report on the lots. Every page is loaded with data because the qualification is that you have to be able to fabricate panels three separate times at least two weeks apart.

I always joke because we used to disqualify Chinese companies that thought they could fool us by building 25 panels, picking the best 15, and then shipping five of them two weeks apart. They didn't understand that the testing machines were so sophisticated that they expected to see three peaks when they'd analyze each work order. If you have one lot, you're only going to see one peak. They were disqualified for an inter year because they cheated, and they'd ask, "How did they do that?" I had to explain to them how it's tested and built and that there's a reason why they want you to build three separate lots: to find out what your lot-to-lot variance is.

Building one lot, you might think you can fool them, but not these testing machines. The PCQR² is just an outstanding benchmarking and qualification tool, and it doesn't cost that much because the test is all automated for it. But most people have never heard of the PCQR² except the aerospace and military guys.



Happy Holden

Shaughnessy: Has your company had any issues with vias?

Chavez: We are a large corporation. We have technical fellows, subject-matter experts (SMEs), and our appropriate departments in place to validate this type of information. But are the lower-level business units following that? Are they taking those lessons learned and applying them in their design? And what you would find is, in some cases and companies, they aren't—

even though they've already benchmarked and said, "These are our lessons learned." You'll find that at the low level, in the weeds, these one-off divisions of small groups of engineers are just pumping stuff out. That's where you start getting anomalies because they're not following the lessons learned or industry best practices.

Holden: You need a rigorous qualification process, which is not going to be that expensive but is going to help you in the long run. You also need a miniaturized coupon on that qualification so that you can put a coupon on every one of your SMT runners so that you have sample vias or a net on every single panel that you assemble; then, you can hold those for three or four months, or if something happens, you can go back and test them.

You might also require a report in every shipment that tests those coupons to the fundamental qualification, so you have the confidence that, "You passed our qualification, but we want to know that your process is still in control now, six months later." The one thing I've learned in 50 years of making PCBs is that no matter how good you are, the PCB process can go south on you before you know it just because you looked at it cross-eyed.

It's so convoluted and complex, and it has so many complicated steps. We're lucky that we can make multilayers at all, but we do. You have to be on top of this thing all the time,

which is why I preach process control and automated analytics.

Chavez: I agree. You must have that feedback loop constantly going because if you don't, you're potentially going to end up with issues.

Holden: Making PCBs is one of the toughest manufacturing processes in the world because of the variability. You look at materials in our chemical processes, and nobody in their right mind would take hydroscopic materials, dunk them in water, try to make precise control of them, dunk them in water again, dry them out, and then dunk them in water again. The silicon companies don't have any aqueous processes. It's silicon and hydrophobic on practically everything—but laminate sure isn't.

Making PCBs is one of the toughest manufacturing processes in the world because of the variability.

Chavez: I feel it's important for every EE and every designer who's designing boards to get their butt over to a fab shop and walk through it to see what a board goes through to get fabricated and to see all the required intricate details that need to be addressed to successfully produce a PCB.

Shaughnessy: We see a lot of designers who haven't been in a board shop in 25 years, or they've never been in one.

Chavez: Or even worse, a lot of companies don't allow their engineering teams to talk to the suppliers. Instead, it's the supply chain that's talking to them, which I have a hard time understanding, but there are companies out there that are so big and complex regarding their departmental structure that all the engi-

neering teams know is that they release their design into their PLM system, and then the supply chain takes it from there.

Holden: I never had so much fun as when I took a bunch of EDA software designers and coders on a tour of a PCB fab shop. These are the people who write all the design tools, and they'd never been through the process and seen how a PCB is actually made.

Chavez: It is extremely important to go take these tours. It's a great way to continue one's education. Within most successful corporations, they make sure to continually develop engineering teams. Collaborating with today's PCB suppliers, whether they come on-site to provide training or education sessions, or do tours of their facilities, continued professional development is crucial for success. Another great way to continue professional development is to get involved with industry associations. I highly recommend that everyone join the PCEA collective and get involved. It's an excellent industry source to tap into. The PCEA's core mission is to collaborate, inspire, and educate. I definitely encourage anyone that has anything to do with PCBs to get involved with their local PCEA chapter.

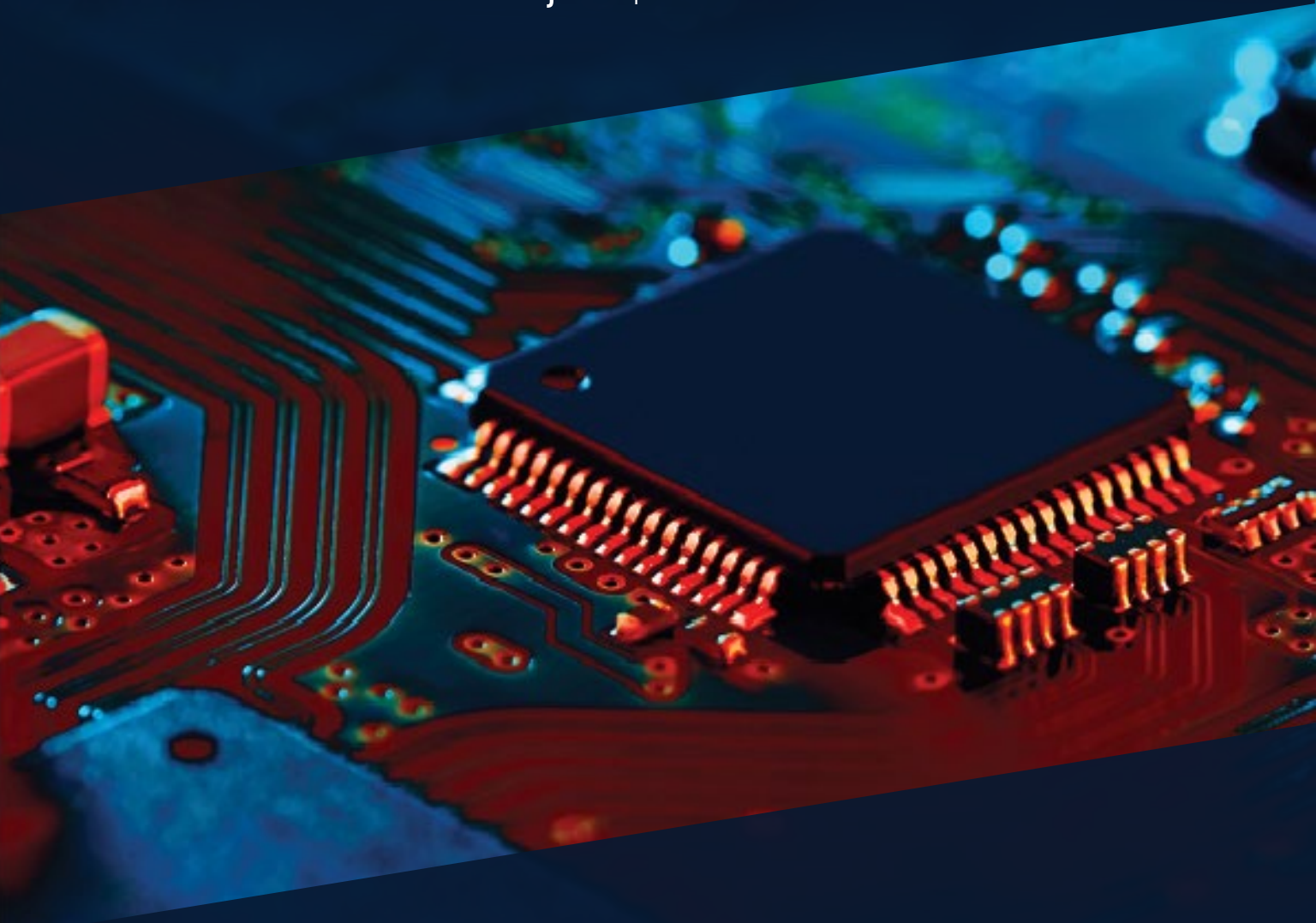
Shaughnessy: I was at the IPC Reliability Conference last year, and it was all about military PCBs having microvia failures. They didn't realize the failures were happening during reflow, and they were undetectable at room temperature or during assembly. Members of this IPC group have been investigating this. Right now, they advise against using stacked vias, especially complex stacked microvias. Has this been an issue for you and your company?

Chavez: We do both stacked and staggered microvias, but it depends on what product you're designing and where it's going to go on the aircraft. With stacked microvias, it's preferred not to stack them more than two on top to each other. The main reason for limiting the number of stacked vias is due to DFM and reliability concerns. And because we're working

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so closely with our suppliers, reliability teams, manufacturing teams, and producibility teams, we continue to collaborate to optimize our processes and designs. That way, our end-product is produced using industry best practices and lessons learned to meet all necessary requirements.

And latent failures, which is what you just described, are a problem that you don't initially see; it just happens all of a sudden. The worst case is to have a latent failure out in the field because it potentially has a significant negative impact as it can ruin your company's reputation, costs hundreds of millions of dollars, or causes permanent injury or death.

Shaughnessy: And they still haven't figured out exactly what's causing that.

Holden: Somebody might have, but they won't share it with us. We tried to get the data, and although the scientists and the process engineers agreed to it, the legal department and management shut down the sharing of the data. My best hope right now is that we're going to get the results from the European Space Agency, where they've done staggered and stacked vias. They use four different methods of testing, which gives us a whole lot of data about which methods of testing the final board are reliable, and which ones aren't, and how they manage to slip through.

IPC paid for the European Space Agency to make a set of these panels for us in the U.S. using a laminate that we're accustomed to using because the European Space Agency is not using laminates that our military aerospace companies in North America are using. But once we get those panels and get them tested, we'll start to have some data. We didn't do a design of experiments, so we're not going to get at the root cause, but we are going to get at what's reliable and what's not, how much can you stack, etc.

I'm depending on Marc Carter—founder of Aeromarc and former director of technology transfer for IPC—and his experiments. Marc has process variables that he's changed. Hopefully, he can provide insight into what the root cause of military via failure might be this year because he's actually going to build boards

using direct metallization as well as electroless copper. A lot of experts tell me that the solution is simple, "Go to direct metallization," but the military doesn't allow that. Marc's data, which the Army is paying for, may say, "You can make it work with electroless copper," or, "sometimes it doesn't work, but it always works with direct metallization." That's kind of an answer.

Shaughnessy: What would you say are some of the things that designers can do to help achieve more reliable vias?

Chavez: The biggest thing that I always say is to communicate with your suppliers. You must have that collaboration and communication. The second thing is that it has to be designed to industry best practices. It's okay to push the envelope, but if you're pushing the envelope, you had better have justification as to why you're doing it, as well as collaboration with your suppliers to back up what you're doing. With aerospace, the volumes are significantly less than what you would see on the commercial side, with volumes of 1,000 or even 100,000 units. In aerospace, you could have 250 units, and that's a lifetime run.

Holden: I always tell people, "If you have to do something different, for heaven's sake, start with a test vehicle."

Chavez: A lot of the times, especially within these large corporations, you have a budget for that. With other projects, you often don't have that luxury. With your first prototype or article, you have one shot at it. If you're going to do that, you need to have all the stakeholders at the table. That way, you're doing it right from the beginning, and you have everyone's input to give you your best shot at success.

Shaughnessy: Do you use landless vias?

Chavez: No. I do know that's out there, but we do not, to my knowledge.

Holden: Landless is not Class 3. Because of the way they define it, Class 3 has lower reliability

than Class 1 because Class 3 military allows a minimal annular ring. Data shows that a minimal annular ring basically guarantees you barrel cracking and corner cracking. In many cases, everything built to military Class 3 can be less reliable than Class 2 and Class 1.

Gary Ferrari wanted to test it because I showed him the data that proves that all of this Class 3 stuff isn't really good data. Our Japanese partner introduced landless vias to us, and we said, "That won't work. It doesn't have any lands," and they said, "Test it." We built an elaborate test vehicle with different sizes of annular rings all the way down the landless, and the landless vias were 10 times more reliable than the vias with the land. The smaller the annular ring, the less reliable the via. We put a bunch of Ph.D. metallurgists on this to explain this to us, and then they showed us the Coffin-Manson models and the data. We said, "We understand now."

Chavez: I heard about this many years ago at one of the IPC APEX EXPO Design Forums. But to my knowledge, landless vias just haven't taken off in the aerospace industry. Within aerospace, it's extremely important to be well within the safety zone of design and manufacturing margins, so we're not pushing the envelope, as you would see in the commercial industry. Aerospace is usually several years behind in the industry, and it's purposefully that way because we always want to be in a safety sweet spot for reliability.

Holden: Aerospace companies are still using tin-lead because that solder is highly ductile.

Chavez: Yes, we're still using the industry-standard tin-lead, but some designs are produced lead-free. It all depends on the customers' requirements. With lead-free, tin whiskers are a serious issue that comes into play and must be addressed. Parts, such as some BGAs, only come in lead-free. And today's BGAs are getting smaller and smaller ball pitch that requires HDI and micro technology vias.

Often, we don't have a choice regarding which via technology to implement. Because

of these fine pitch components, we have to use microvias. These parts are getting smaller, smaller, and smaller, and we don't have a choice. The minute an EE selects a part with these 0.65-mm pitch BGAs or smaller, they've already boxed us in a corner to HDI and microvias. We have no choice.

Holden: I'm judging a board right now that's 782 I/O at 0.4-millimeter pitch. The board that this thing is mounted on is an eight-layer ELIC, in which there are no through-holes. Every single layer is "microvia-ed" to the next layer. Now, they don't talk about what material it's made out of, but I sure hope the fabricator and the material are well tested because I took a look at that BGA and said, "My gosh."

Chavez: In that case, it is what it is, and you have to adapt to it. As engineers, we have to do what we can that's in our repertoire not just for design but also for manufacturing. This is where you had better be talking to your suppliers. They need to be all in with the engineering aspect as well.

**As engineers, we have to do
what we can that's in our
repertoire not just for design
but also for manufacturing.**

Shaughnessy: Does it matter to a designer whether the vias are going to be laser drilled or mechanically drilled?

Chavez: You should know what you're getting into. You should know those details up front when you're dialing in your stackup and adjusting your stackup with your supplier. You should collaborate with them to achieve your results because you want to minimize your expense and maximize your yields. That way, you're getting the best bang for your buck at

the highest quality possible, and the intent is always to design it right the first time.

Holden: And hopefully use the simplest, most robust technology that's within your price focus. Don't go after bleeding-edge, state-of-the-art technology just because it's exciting. Instead, keep it simple, and reduce the complexity.

Chavez: That is aerospace in a nutshell: You want to do the best you can with the simplest technology that's there because that's the sweet spot of the industry and for safety. You also want to design it to be built anywhere, any place, any time.

Holden: We've been drilling holes in laminate for 60 years, so we know an awful lot about drilling a good hole. You stick with the basics if you can get it done. But unfortunately, the semiconductor people, with their packaging and fine pitch, make it impossible. And there's the physics of their rise time: A three-nanometer transistor turns on and off awfully fast in there.

We've been drilling holes in laminate for 60 years, so we know an awful lot about drilling a good hole.

Because of that, their interconnected links have to be shortened, which means they have to use more grounding pins, and they have to use a smaller package. Physics drives them to that. Like death and taxes, miniaturization is inevitable. But we can also now drill 0.1-millimeter holes mechanically, so nobody says we have to use a laser if you can mechanically drill 0.1-millimeter holes. And with VeCS, we don't have to drill holes at all. We just route a trough and get the same density as HDI without any microvias.

Chavez: Usually, when we're talking with our supplier, we ask, "If there's a way we can get by with a standard through-hole, then let's go that route." We'd rather do that instead of using HDI if we can because it keeps us within the sweet spot, and then we can go from there. But if we don't have a choice because of the part that was selected, it is what it is. You just do your due diligence to try to mitigate and achieve success as best you can.

Shaughnessy: It sounds like a lot of times, it comes down to communication. Everyone agrees there should be communication between the designer and the fabricator, but not many are doing it.

Chavez: Absolutely, and if you have the funding, you would be running a test. But if you don't, and you have one shot at it, you'd better reach out to the suppliers and work with them as you produce your board.

Holden: And if you want to know about the reliability of bare PCBs, the new chapter in the seventh edition of *The Printed Circuit Handbook* by Dr. Reza Ghaffarian from Jet Propulsion Laboratory is one of the best I've ever read in print about bare board reliability. It's outstanding.

Chavez: Yes, and [I-Connect007's eBooks](#) are a very good starting point, plus they're free. I hope all the designers and engineers are taking full advantage of your eBooks. They're gold. There are some other books out there, and there are some great webinars in today's "new normal." It's up to you to take the time to attend or sign up and watch the presentation.

Shaughnessy: Thank you, Steph. I look forward to meeting up again in person.

Holden: Maybe next year.

Chavez: Thank you both. It was my pleasure. This has been a great conversation. **DESIGN007**

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Top Tips for a Successful Thermal Management Process

Sensible Design

by Jade Bridges, ELECTROLUBE

This month, I'd like to concentrate on some of the complications you are likely to encounter when selecting and applying a thermal interface material. I'll also look a little more closely at thermal resistance, viscosity, and vibration, as well as their effects on performance.

Choosing a thermal management product is not just about ticking all of the correct boxes on a specification sheet; it's a complex process that requires consideration of how to apply the product in accordance with production schedules and testing of the product in the final application. Selecting the right type of thermal management method for a particular electronic assembly and its predicted operating conditions is far from easy.

Once selected, it is vitally important to ensure that the thermal management product continues to perform satisfactorily throughout the expected lifetime of the product. To establish this, the performance of the device or the thermal resistance between the device and the

heat sink needs to be measured again after accelerated aging or with environmental tests that simulate the real-world application conditions. This is the only way you can be sure that the thermal management product chosen is really suitable for the job.

Without further ado, let's explore how you can fully optimise your thermal management process using our trusted five-point question and answer format.

1. How do I ensure that my choice of thermal management material is the most appropriate one? What factors should I take into consideration?

Choosing a thermal management product must always take into account the application under production conditions because the thickness and uniformity of a thermal interface material can have a dramatic effect on the effectiveness of thermal transfer. A product tested under lab application conditions, there-



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fore, may not behave in the same way as a material that is applied in production. For this reason, the most appropriate choice on paper might not be the best overall choice when taking in these additional factors.

2. What is thermal resistance?

Thermal resistance doesn't just rely on the bulk thermal conductivity alone; it considers the product's performance in the actual use conditions by also factoring in the bond line thickness and the contact resistance at the two interface surfaces. The most common way to evaluate the performance of a thermal management product is to check the thermal resistance between the component and heat sink with and without the thermal management product applied. Another common method is to measure the device or component operating temperature with and without the thermal management product applied.

3. Why does the viscosity of a thermal management material affect processing parameters and eventual performance of the product in use?

The initial viscosity of a thermal management material can impact the application method. For instance, with screen printing, the mesh size controls the thickness of paste applied. If the paste is too viscous, it may not spread very well over the screen; therefore, the desired thickness may not be applied. Similarly, with dispensing applications, if the product is too low in viscosity, it might spread too well and flow into unwanted areas.

When in use, the way a material responds to shear will indicate how the product may behave under changing temperature conditions, such as with the pump-out effect. If the thermal management material is shear thinning, it will reduce in viscosity with increasing shear. The effect of shear can occur between two surfaces, which expand and contract with changes in temperature, illustrated by their CTE. If you have large CTE values for the surfaces or big differences in CTE between the two surfaces, the effect of shear may impart

a viscosity change in the product and hence affect its stability in end-use.

4. How significant a problem is vibration when considering the choice of thermal management material?

Vibration can be a significant problem in certain applications. Like the pump-out effect, vibration is a physical change that happens in the surrounding environment. With such movement, a change in the position of the thermal management product may occur. This can lead to reduced efficiency of thermal transfer.

In gap-filling applications, the effects of vibration can be much greater, especially if the product is a non-curing paste or putty. Gap filling applications generally have significantly more product applied in one area; therefore, the movement from vibration can cause large shifts in the placement of the gap filling product if it is not contained by the structure of the PCB casing. If vibration tests are required for the PCB, these tests should definitely be repeated with the chosen thermal management product present to ensure no significant changes are seen during the expected lifetime of the device.

5. What are your top five tips for success?

One factor I cannot stress enough is to adopt the "test before you buy" approach. If a thermal management product is not tested before use, the end performance of your product might be very different from what you expected.

The following points are essential for a successful thermal management process:

1. Consider all influential external conditions (temperature, vibration, etc.).
2. Decide on the ideal production process for the volumes being produced.
3. Look at the board design. For TIM applications, review if the interface gap can be minimised and ensure it is not excessively wide.
4. Consider the materials present on the PCB/unit. Are there any sensitive materials present or high CTE values?

5. Test, test, test! Select the most suitable products based on the required heat transfer and take points 1–4 into account. Always test in end-use application conditions.

Conclusion

To enhance your reputation in the market, it is fundamental to ensure that the desired efficiency of heat transfer is achieved over the lifetime of your product. Deciding on the right choice of material and/or application technique can be challenging; however, many companies have years of experience resolving customer thermal management issues.

As always, I strongly recommend you get some expert advice before you settle on any particular material or method, rather than

attempt to resolve your thermal management queries in-house. I hope this month's column will help you with your thermal management choices.

Look out for my next column, where I will elaborate more on thermal management issues. And please get in touch in the meantime if you have any suggestions for specific areas of discussion. **DESIGN007**



Jade Bridges is global technical support manager at Electrolube. To read past columns from Electrolube, [click here](#). Download your free copy of Electrolube's book, *The Printed Circuit Assembler's Guide to... Conformal*

Coatings for Harsh Environments, and watch the micro webinar series "Coatings Uncoated!"

Figure It Out: Effective Collaboration Tools for Post-COVID-19 Engineering

by **Dugan Karnazes**

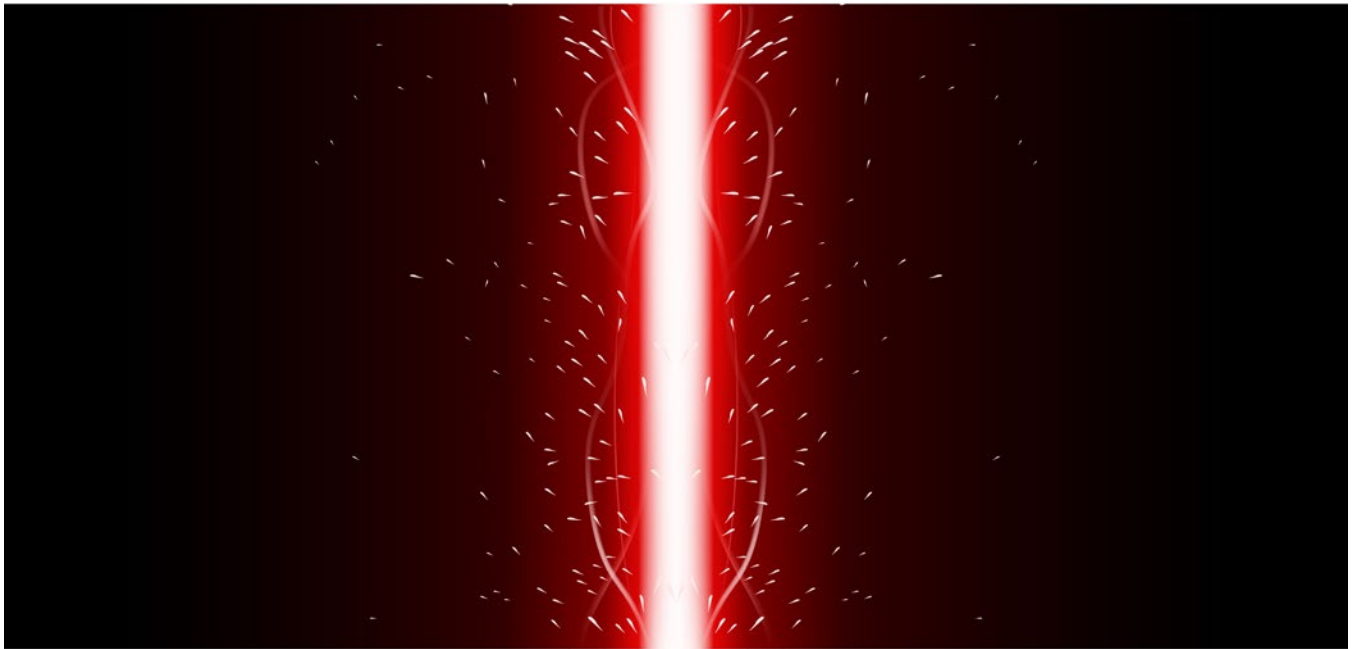
VELOCITY RESEARCH FOUNDER AND CEO

As far as engineers in the electronics industry go, I'm still on the young side with 10 years of experience compared to the veterans of the industry. I've been around long enough, however, to understand firsthand the struggles that organizations (large and small) go

through when they're designing their own electronics. I'll bet my last 555 timer that a lot of you have run into these scenarios: the Wizard, the Wishful, and the Wise. These scenarios are exaggerated for the points I'm going to make, but they're designed to resonate with the experienced.

To read Dugan's full debut column, [click here](#).





HDI Design, Landless Vias, VeCS, and More

Feature Interview by the I-Connect007 Editorial Team

Andy Shaughnessy, Happy Holden, and Dan Feinberg recently met with James Hofer, general manager of Accurate Circuit Engineering, to discuss via design techniques and via reliability from the fabricator's viewpoint. As Hofer explained, even with open lines of communication between the designer and the board shop, there are plenty of variables to contend with regarding proper via design, especially when working with PTFE materials.

Andy Shaughnessy: James, start by telling us some of the problems that you see with failures in vias and microvias.

James Hofer: I face a couple of challenges. Designers tend to want to do HDI designs with laser-drilled vias with aspect ratios of 1.5:1 or 1.8:1, or they want to do laser-drilled vias through multiple layers without removing pads. I don't yet have a reliable copper-fill process that gives me as flat a surface fill as I want. As you know, most of our product is

PTFE. Stacking laser vias on PTFE and copper-filled vias presents a couple of challenges. I see more and more customers want a PTFE dielectric, and they want to put a 4- or a 6-mil via in it. That presents issues both in the drilling of the via and with the plating of the via. I see a lot of that, so I find myself trying to redo designs after the fact with most customers.

Shaughnessy: They're trying to use HDI when they don't necessarily need it.

Hofer: And when they don't necessarily understand some of the give and take that goes with it. They don't want to abide by some basic principles and rules that we manufacturers have to live by.

Happy Holden: Why would they get into HDI but not do any basic investigation on how to optimize drills or design with it?

Hofer: I agree. That's exactly what we face.

Holden: Or they read about it or heard about it, and they're going to use it, even though they don't know anything about it.



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Hofer: That sums it up right there. The majority read something about it. Perhaps they read the first couple of paragraphs of one of Happy's articles and think, "Great, I can do this," and then off they go. It is far more appropriate to discuss with the manufacturer before you implement the technology.

Holden: *The HDI Handbook* is free. It goes into reliability and plating and metalization, materials, aspect ratio, and cycle integrity.

Dan Feinberg: Why wouldn't they read it and use some of those recommendations? That's a good investment.

Holden: Or just type HDI into Google or Yahoo.

Shaughnessy: Don't designers communicate with you beforehand? I know they say they're going to talk to their fabricator, but do they really?

Hofer: No. We face that problem pretty much on a daily basis.

Feinberg: What do you consider to be the most reliable process for electroplating copper vias? Is it still a thin coating of electroless copper followed by an electrolytic? Is it a thick coating of electroless, as one company was trying to push a couple of decades ago?

Hofer: Generally, the most-used process is a thin-to-medium deposition of electroless, and then into barrel plating the vias and copper plating them. Copper-filled through-vias are making an emergence, especially in mixed materials or PTFE or hybrid materials, the most tried and true method is still to plate the via, fill it with a non-conductive fill, and plate over the top. In HDI design, where we stack



James Hofer is the general manager of Accurate Circuit Engineering.

the vias, we're looking to offset that stack so that they're not dead center on top of each other.

Holden: We have a lot more material choices today than we did way back then, but fewer laminate makers are making the materials.

Hofer: I agree. They have really consolidated.

Shaughnessy: Tell us about landless vias. Last year, you were doing a lot of

landless vias. How did you get into that, and what are the benefits?

Hofer: The main benefit is savings on real estate, and we got into that with exactly the same kind of situation we face now, where somebody wanted to stack microvias but didn't really know what they were doing. We found a way not to have to stack them, and that's with landless vias. It's a take on copper-filled vias. You make the land into the void of the drilled hole. Again, it's involving button plating and still the same copper electroless and electroplate, and then button plate to fill the hole with copper. At that point, you have a landless via.

If I were asked about the biggest changes in the last 20 years, it's the fact that everything has to be smaller, more reliable, and cost less. Those are the big industry changes, and the industry has adapted. One of those things was stacking microvias and going to landless vias. That's how rigid-flex started to come in, so we could connect things without having to do a ribbon bonding, and that's where we're at today.

Holden: The other big change from long ago was that technology used to be driven by the military, and today, the most advanced technology is the consumer segment.

Hofer: That is absolutely correct.

Holden: In fact, the military is kind of trailing everybody else.

Shaughnessy: You do a lot of the stuff in PTFE, and that offers its own challenges with it being hard to register, and it's kind of squishy. How does that affect the way you create vias?

Hofer: As we get into PTFE, dimensional stability becomes an issue, and not necessarily Z-axis dimensional stability, though there is a bit of that, but very much so in X/Y stability. And when we're doing landless vias or microvias, that makes it even more challenging because with the technology today, every methodology for plating and/or filling those vias requires a mechanical planarization methodology, and that just doesn't work well with PTFE. We have to walk a fine line between being able to planarize the surface, making it flat, without disrupting the X/Y stability of the PTFE. I look forward to a technology that will allow us to fill those vias without the need for planarization. There have been a couple of tries at that technology, but they've not quite gotten it.

Holden: Strangely enough, that was the first microvia board we built in 1982: an eight-layer PTFE multilayer with a metal core, cavities, and selectively plated pure gold with microvias to do wire bonding, attaching the chips in the cavities down to the metal core. If I circulated that board today, nobody would quote on it. They would say it's impossible to build. But that's vintage 1982.

Hofer: Yes. I find that to be a little more manufacturable with the metal core because it helps hold the stability down in the processing of the subsequent microvias. But we do a lot of cavity boards with wire bonding outside of the cavity because with many RF components, the shorter the leads to the pads, the better. Having the heat absorption of the core that the chip can sit right on is extremely beneficial.

Holden: There was always a nickel barrier.

Hofer: We, too, prefer a nickel barrier, but we find a lot of our RF folks are not liking the nickel because of the added loss, so we're doing a lot more EPIG and EPAG now, where they can still wire bond without the use of the nickel underplate.

Feinberg: One of the things that I've always tried to push with our people as a supplier back in the day was communication with the designers. The designers never communicated much with the suppliers. You really don't have much communication with the designers?

Hofer: Once we have an established customer, our dialogue with the layout and the electrical engineer and even the mechanical engineer increases dramatically. It's the referrals and the new folks. With their first order, we get their files and say, "Wow, I wish you would have talked to us a few weeks ago." But with our current relationships, the majority of my day is spent on the phone with either the layout person, the EEs, or the MEs, or trying to get the project managers on the line. I like that because that's a huge benefit to both the customer and us. Let's face it, even though board shops all basically do the same thing, there are different nuances between shops.

**Let's face it, even though
board shops all basically do the
same thing, there are different
nuances between shops.**

Getting to talk with a customer before the data is over the fence helps them understand what your processes are. I always make it a point to help them understand what other folks' processes are as well so that they design not only so that I can build but also so that other folks can build, because I realize that I'm not going to be everything to everybody all the time.

I also do seminars for customers, where we talk about how PCBs are manufactured because, believe it or not, a lot of layout people and EEs have no clue how we build circuit boards—none whatsoever. My seminars are not nearly as good as Happy's, but I do one on how to properly stack microvias, and I've included a lot of what I've learned from you in that presentation as well.

Shaughnessy: Do designers ever ask to take a tour of your shop?

Hofer: Not unless they become a customer or we're talking about a project. With COVID-19, not a lot of people want to visit these places.

Shaughnessy: Related to vias, there have been failures with military boards. They found out later that they were opening during the reflow process, but then they would close back up, and it would pass. After the fact, they found out it was shorting during reflow, and then it would heal itself at room temperature. IPC has a task group looking for the cause, and Happy is a member. They're saying to stagger the vias until they can figure out what's going on.

Holden: The more you stack, the bigger the stress on the landing pad. The electroless copper is cracking during the reflow but resealing so that you can't detect it any other way. You have to go up to 240–260 C to get the stress to cause the open. Once the mechanical contact heals, it can take months or years for everything to relax so that you start getting an intermittent open. Unfortunately, these are military missiles and things like that. Some of them are warheads, and the military doesn't like intermittent opens on warheads when you're underneath the polar icecap. They get really angry when they start seeing red indicators showing that something has opened up.

Some people probably have already solved the problem, but they don't want to share it with the industry, so we're still back to looking for money and test vehicles where we can get data that can be shared with everybody. Hopefully, we'll have it next year. We have the

data from the European Space Agency where they've gone two buildup layers, and their second phase is three buildup layers. They've built test vehicles for our group that are stacked and staggered that are four high. We have two, three, and four high.

We're using electroless copper and direct metallization, and a couple of other variables, but a standard material that's used a lot in military aerospace. The European Space Agency is using materials not commonly used in North America. Although we can report their results, the boards are fabricated in Europe with materials that we typically don't use, so we don't know how to interpret their data so much into our situation.

Shaughnessy: Do you see any new technology that looks promising as far as doing vias, anything that piqued your interest?

Hofer: No. I recently returned from a trip to Asia and watched them using the direct metallization that we had tried here years ago, and kind of phased out. I found it interesting that the European Space Agency will be using direct metallization in their testing.

Holden: We have two PCB shops with electroless copper and direct metallization with the same process at each shop. As they build the test vehicles, they'll build them both ways.

Hofer: That will be very interesting. But currently, there's no new technology to tackle this ongoing challenge. You're going to have an uphill battle tearing us away from a standard electroless and electrolytic copper plate methodology.

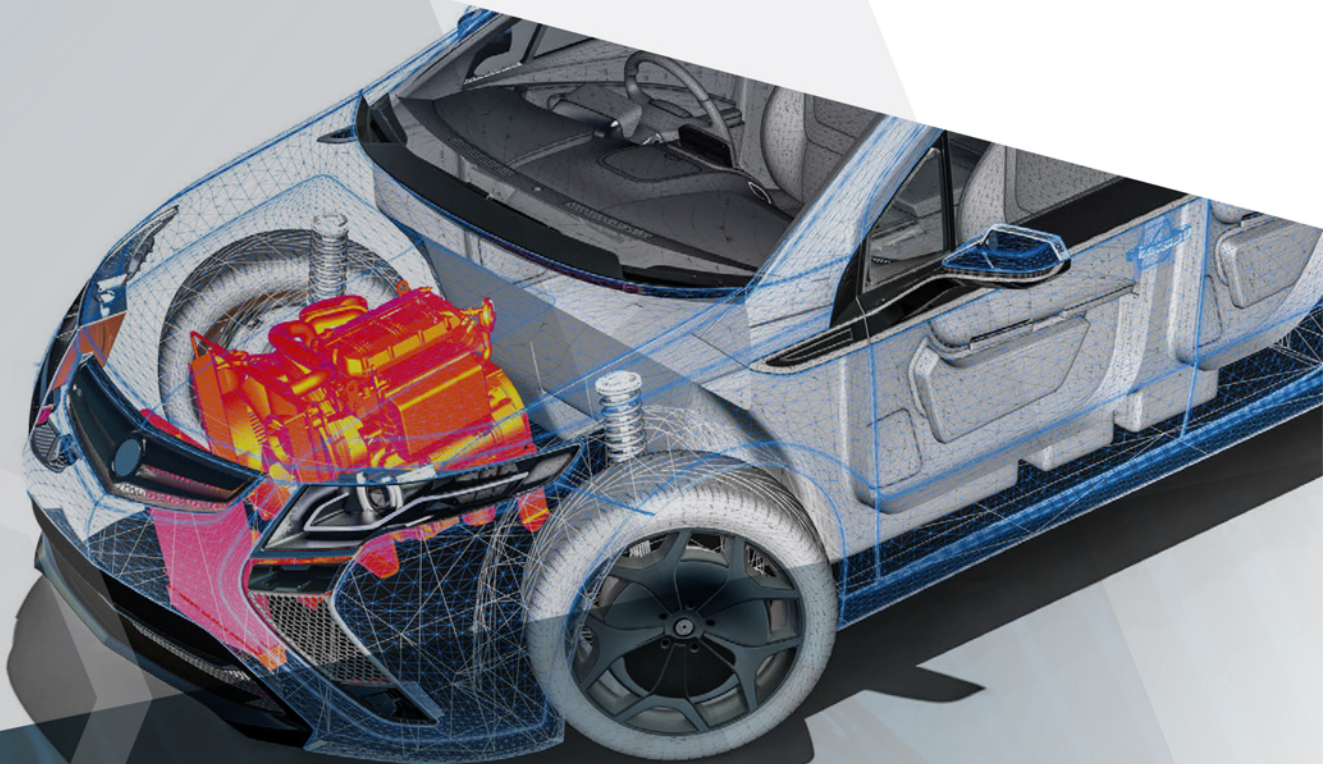
Shaughnessy: Tell us about Accuwrap.

Hofer: Accuwrap is a way to meet the IPC Class 3 wrap plating specification without adding a significant amount of copper plating to the surface. It is a proprietary process that allows you to meet both IPC-6013 and IPC-6018 wrap requirements without adding too much copper to the surface of the PCB. IPC-6018 is 0.002" on all classes, and IPC-6013 is half a mil for



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Class 3 products. If you have two terminations of line vias and then a through-hole filled via and then through-holes, you already have a mil and a half of wrap required on the surface of that layer.

And if you're trying to etch fine lines and spaces, including through-hole plating, then you just end up with way too much copper. Especially in the RF world, you want to model with the expected amount of copper on the surface, and nobody really needs three or four mils of copper on there for RF technology. There's a lot of thermal technology people who want three-ounce or four or five mils of copper on a surface, but that's a different group.

If you're trying to etch fine lines and spaces, including through-hole plating, then you just end up with way too much copper.

Believe it or not, the demand for it is not as high as we would have thought. I think it's because we've taught our customers to call out the right specification. If you're building an RF board, go with IPC-6018—not IPC-6013, which is for analog and digital boards. It's not really intended for RF products. Once we get past that minimum requirement of a half mil of copper wrapped on every termination of a subassembly or filled via set, then things move better. And I could debate the reliability of having half mil of wrap around a plated through-hole and whether that's any stronger than two-tenths.

That's one of those ongoing debates that's similar to etchback. There are those who say positive etchback gives you a better interface for internal layers and others who say negative etchback gives you a better interface.

Shaughnessy: Are you still doing some funky boards for autonomous vehicles?

Hofer: We have several customers in the autonomous vehicle realm. It's funny because we have three of the bigger players. They'll say, "We want to do this and that," and it's so difficult not to say, "We have some ideas," because, obviously, you can't share those.

Shaughnessy: For autonomous vehicles, you want reliability. What kind of via processes are you using typically for boards for autonomous vehicles?

Hofer: We are starting to stack quite a bit for one of the players. Another player has a whole different technology, but for one of them, we're starting to stack and stack. We've just been tasked with taking a 12-layer and making it all stacked microvias, which would take us over five per side, and I'm recommending against it. But to fit in the real estate and to get the chips on it that they want, we have to discuss it. It will be interesting.

Shaughnessy: You must do a lot of your own research on this.

Hofer: We do test some ideas and processes. I don't want to say too much, so we do lots. We work together to run some sample boards and have them tested. I started having a lot of people ask about our surface roughness, and until recently, we never sent out for surface roughness testing. Why would we? Now, I'm constantly looking at what processes cause a certain amount of roughness and what the end result is because that's becoming more and more a topic of concern.

Holden: The vertical conductive structure (VeCS) process gives you a microvia density without laser drilling. It's great for your PTFE boards because you can get microvia density, but you don't have to use a laser drill, and you only need one lamination instead of sequential laminations to connect to different layers.

You rout in slots in the board, and with the slot, after metallization, you can connect to any layer, anywhere along the slot, up or down. You can make a slot all the way through the board,

or you can just make a slot halfway through, depending on where you want to interconnect the layers vertically inside the slot.

Because it's a slot, it has very good fluid distribution for plating. That's why it's the greatest thing in the last 20 years because it allows a conventional printed circuit shop to do equal or greater density than HDI without buying a laser drill or dealing with the aspects of blind via plating in metallization.

Hofer: That's interesting because we're doing something very similar for one of the autonomous vehicle companies, without even knowing that this was out there. It has some challenges, not the least of which is registration to the original slots, on into copper pullaway when you're drilling to remove the vertical plating as well. There are challenges that are faced that make it difficult.

Holden: But it's not rocket science. The OEM takes out the license, not the fabricator, so the technology is free to the fabricator.

Hofer: Shoot, I hope so. We're doing something like this without even knowing that somebody

had made this a process. It's basically drilling and plating a slot, and then drilling away the copper in between it—somewhat not unlike doing castellations.

Holden: My first impression was how is this different from castellations? And the fact is that it's mostly around the BGAs so that you can get to all the connections on a BGA. Castellations is the outside edge.

Shaughnessy: Was there anything else you'd like to mention?

Hofer: Read [I-Connect007's eBooks](#). They're free and offer good advice. I'd hate to sound like Channel 4, but "the more you know..." And we're gearing up for our NIST-800 certification. We're doing 15 webinars a day. It's ridiculous.

Shaughnessy: James, thanks for speaking with us. This has been great.

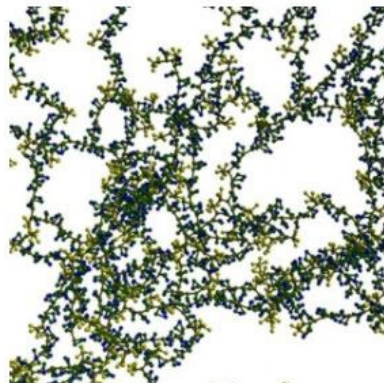
Hofer: Thank you, Andy. Maybe we can meet at DesignCon 2021. **DESIGN007**

Siemens Adds Multiscale Chemistry Modeling With Culgi Acquisition

Siemens has signed an agreement to acquire Culgi, a computational chemistry software company with a focus on multiscale simulations in the process industries. Culgi will join Siemens Digital Industries Software, where its solutions will expand simulation capabilities of the Xcelerator portfolio with quantum and molecular chemistry models that seamlessly couple with the continuum approach in Simcenter STAR-CCM+ software. This unique engineering workflow can deliver significant cost savings and accelerate innovation in the materials and process industries, increasing the potential for product and process transformations.

"Innovations in soft materials engineering begin at the quantum and molecular levels," said Jan Leuridan,

Senior Vice President, Simulation and Test Solutions, Siemens Digital Industries Software. "With Culgi technology as part of the Simcenter portfolio, process engineers will gain access to a comprehensive digital twin that combines micro-scale, meso-scale and macro-scale modeling."



The acquisition of Culgi builds on Siemens' November 2019 acquisition of MultiMechanics, which added efficient prediction of solid material properties and behavior to the Simcenter portfolio. Through the addition of Culgi's soft materials simulation, Simcenter can now offer a unique integrated CAE solution that enables performance-driven optimization of advanced materials.

[Source: PR Newswire]

PCB Vias, 'You Have a Go'

Tim's Takeaways

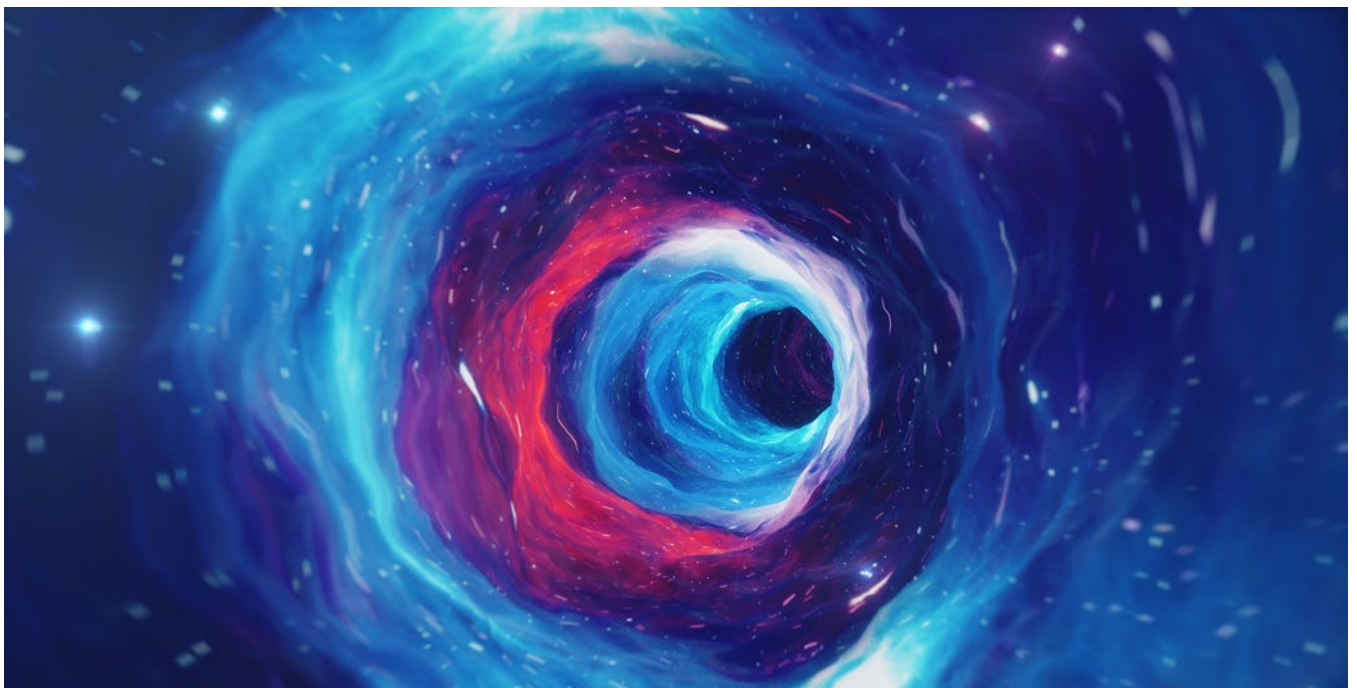
Feature Column by Tim Haag, FIRST PAGE SAGE

Do you remember the old TV show “Stargate SG-1?” Debuting in 1997, it was a continuation of the 1994 movie “Stargate” and ran for 10 seasons, spawning two additional shows in the Stargate franchise. “Stargate SG-1” was known for its unique blend of sci-fi action and adventure, as well as a generous amount of humor.

The show also showcased a variety of well-done special effects, including creature design, makeup, and amazing starships and battles in space. The signature effect, of course, was the stargate itself, which was described as a wormhole through space. With the exhortation of “SG-1, you have a go” from their commanding officer, the stargate would instantaneously transport an intrepid band of heroes to new and exciting locations each week.

In addition to the general fun factor of the show, there was something else about it that appealed to me on a deeper level as a PCB design professional. It took me a long time before I figured it out, but when I finally did, I was stunned to realize that the stargate is nothing more than a giant via in space!

Okay, that may sound pretty lame, but if you think about the nature of a via, you can see where I’m coming from. Just as the stargate fictitiously conducted people directly from one place to another without the need for intergalactic space travel, a via will conduct a signal directly from one layer of the board to another. Of course, when you start adding time travel, energy weapons, and little gray aliens that aren’t wearing any trousers, the analogy falls apart pretty quickly. But at least we’re on the



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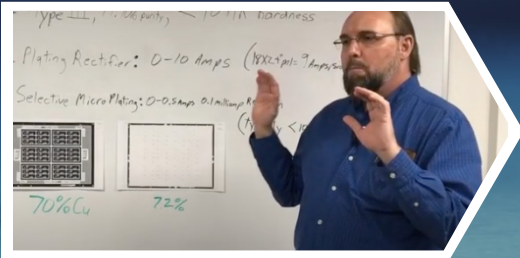
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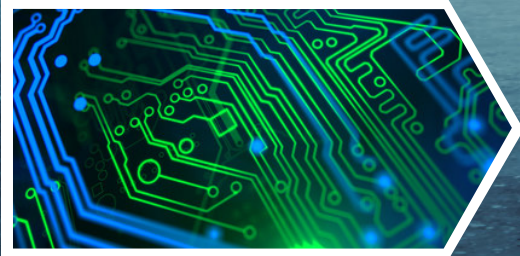
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topic of vias now, which is where we wanted to be all along.

There was a time early in my career as a PCB designer, where we didn't give much thought to the vias that we used. The signal speed of the designs we were working with was very slow compared to today's standards, and except for fabrication costs, it didn't really seem to matter how many holes got punched on the board. But as you know, that level of design technology is a long way behind us now. Vias are now much more than just a hole in the board to connect a signal from one layer to another; they are an integral part of the overall signal integrity of the design.

Vias are now much more than just a hole in the board to connect a signal from one layer to another; they are an integral part of the overall signal integrity of the design.

Take high-speed transmission lines, for example. For the best signal integrity, the traces of a transmission line should be contained on a layer that is sandwiched between two ground plane layers in a stripline configuration. This gives the best impedance control and shielding for the signal, plus the signal return path on the adjacent reference plane will be coupled directly to the signal.

The problem, of course, is that you can rarely contain a trace on just one internal layer. Even if the routing can be done on that one layer, you still need to transition to a surface layer to connect to the components through a via. Back in the day, we would have simply dropped a through-hole via and been done with it, but the high-speed routing requirements of today's designs need a via solution with a little more finesse.

A through-hole via can act as an antenna and radiate energy, so we've come up with some ways to guard against that. Back-drilling the via is one of those ways while using blind vias is another. For high-density interconnect routing on boards with large pin-count ICs, microvias are often the best option. All of this is done to keep the signal path as short as possible through the via, with the added benefit of opening up some more routing channels where the through-hole via used to be. But using vias on a high-speed transmission line opens up yet another can of worms that, interestingly enough, requires the use of even more vias to resolve.

A signal needs a return path, and this is usually accomplished through a ground plane. For a high-speed transmission line, however, the return path becomes even more important and must be clearly defined in order to avoid problems that can disrupt the function of the circuit. The reference planes in a design are looked at very carefully now to make sure that there aren't any plane splits, slots, and other congested areas that can clog up the signal return paths. Without a clear return path for the signal, the circuit may develop unwanted noise resulting in crosstalk, interference, and even false triggering of the signal.

Therefore, to maintain the best signal integrity, the transmission line needs to be directly adjacent to the ground plane that it is using for its signal return path, and the plane must supply a clear path. When the signal transitions to another layer through a via, however, the return path will be severed unless there are ground stitching vias nearby for the return path to hitch a ride on. These ground vias provide the means for the signal return to continue its path back to the source in what is known as layer paired routing.

There's still more to how we choose which vias to use and where they should be placed, as well as the need for transmission line signal integrity. For instance, power circuits will need a larger via to handle the current that they are carrying. Without an adequate size, things can get a little toasty for the smaller vias, which is why power pins are usually routed with wider lines and larger diameter vias.

In some cases, vias are also used to transfer heat. Since a circuit board with all its different internal layers and metal planes makes for an excellent heatsink, adding vias under hot components will dissipate that heat throughout the board. This can bring a lot of heat relief to those parts instead of allowing the heat to build up in those areas of the board where the parts are located.

Circuit board test is another important use of a via. To test the connectivity of a fabricated board—as well as the assembly integrity of a fully manufactured board—a variety of tests are conducted on the PCB. These include using test fixtures with probes for every net on the circuit board that contact all the points designated as testpoints simultaneously.

Another method is known as a flying probe test, which is a machine that probes each testpoint individually. The important part of these different testing methods, however, is that vias usually serve as the testpoints which the probes come in contact with.

To facilitate this testing, a PCB designer will use some specialized features in their CAD tools to flag specific vias as testpoints. With a via marked as a testpoint, the location of that via and the net it is attached to then can be extracted from the CAD database in order to create a testpoint file. This data is then used for building test fixtures and programming the test machines. In some cases, the size and shape of the testpoint vias will even be changed on the layout to visually identify them as a testpoint on the fabricated circuit board.

Additionally, these testpoint vias are usually subjected to additional design rules and constraints than a regular via is. For obvious reasons, they can't be placed under components, and they need to have specified clearances from each other to ensure that the probes on the bed-of-nails test fixture can easily access them.

Considering all that they are used for and what is required of them, vias are actually subjected to a lot more action and adventure than I would have expected. I wouldn't put them on the same level of excitement as SG-1, but vias do have a lot of intricacies to them that commands respect. There is a lot to consider when working with them to ensure that your PCB design performs up to specification and is manufacturable the way you intended it to be.

Thankfully, there are people in the design community who are a whole lot smarter than I am about the best way to work with vias. You have the opportunity to learn from them in this edition of *Design007 Magazine*. I'm looking forward to reading myself what I-Connect007 and its experts have to say about vias when I receive my own copy. Until next time then, keep on designing, and vias, you have a go! **DESIGN007**



Tim Haag writes technical, thought-leadership content for First Page Sage on his longtime career as a PCB designer and EDA technologist. To read past columns or contact Haag, [click here](#).



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Stacked Microvia / Weak Interface **Reliability** Study

Feature Edited by Happy Holden
I-CONNECT007

At the IPC High-Reliability Forum, Marc Carter gave a presentation on a study that covered stacked microvia/weak interface reliability. I have assembled the highlights of Marc's presentation, including the transcript, which has been slightly edited for clarity.

Marc Carter is the president and owner of Aeromarc LLC, as well as an [I-Connect007 columnist](#). He has worked in the electronics interconnection industry since 1984 in a variety of roles in fabrication and assembly materials, processes, environmental compliance, and supply chain management activities around the world. Marc has had the honor and privilege of working with and learning from many of the true giants of this industry in multiple functions over many years. His experience includes a major mil-aero OEM, field and development work at material suppliers to the printed circuit industry, and an educational stint as the sole proprietor of a manufacturer's agency representing multiple high-tech mil-aero material suppliers.

Background

I am going to outline a project that a number of us in the industry have undertaken, recognizing the lack of publicly shared information that has been commented on several times. Intended as a tool in guiding our future designs and procurement, this stacked microvia and weak interface reliability study is a three-year, three-phase iterative industry and academia collaborative research project.

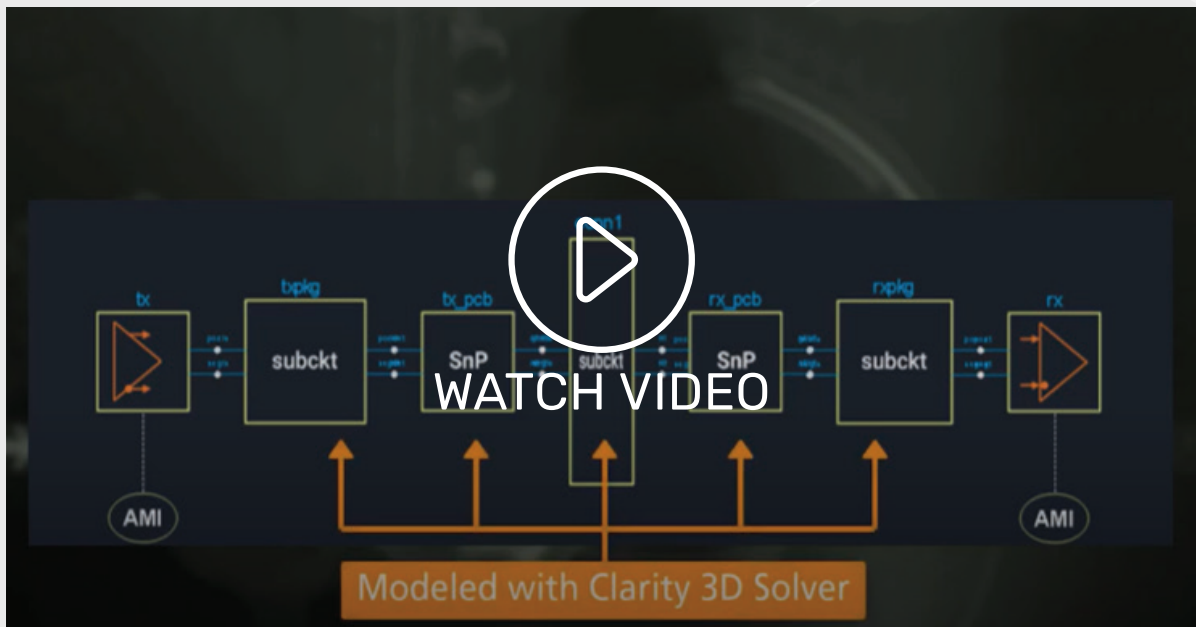
The methodology we undertook does not try to look at everything. We did not try to "boil the ocean," and we wanted to approach it in manageable stages, each providing some immediately useful knowledge, revising subsequent stages based on what is learned. Here are some of the team participants that we are working with at this point:

- Fabrication: Calumet Electronics and Electrotek Corporation
- Simulation: ANSYS (Sherlock)
- Statistics: Michigan Technological University (MTU), electrical and computer engineering
- Test: Foresite Inc. and Robisan Laboratory
- Project facilitation: Aeromarc LLC

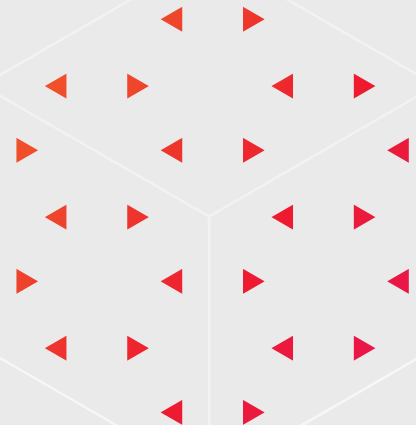


System Analysis

Empowering system-level analysis
of 112G SerDes and DDR designs



Application example for 112G SerDes



The industry has been using microvias for decades, and most of us shared a basic misconception about microvias and high-reliability applications. The microvia was believed to be the most robust type of interconnect. In many ways, it still is. This is a low-probability problem, but its latency and inability to be detected by traditional testing methods is unfortunate. Seeking certain density designs, we incorporated two, three, four, or more stacked microvias, possibly without sufficient forethought as to what that might do to uncover new failure mechanisms. Because of our preconceptions, we miss diagnosed problems quite often and early on. In some cases, companies drifted along for some years, thinking they uniquely had the problem—until they started comparing notes ^[1].

We are in a containment position. We have received guidance from the IPC, and we have internal companies with their own guidance. You've seen the Motorola red, yellow, green structure ^[2]. That involves a kind of containment by limiting the complexity and being very careful to qualify sources because not everybody is equally good at this. Using intensive screening and perhaps over-conservatively defined lot rejection, this problem is corralled but limits advancement.

Many OEMs felt confident about what they were getting and fielding. With limited capability, especially as you get to the more complex structures, that limited capacity in the industry in North America. Some of those failures and rejections have reportedly led to late deliveries, etc. In today's world, the biggest impact is scheduling.

We have made a lot of progress in screening technology. Screening helps prevent escapes to the field. We are much further along in containment than we are in understanding the interaction with the multiple contributing mechanisms ^[3]. There are some papers listed. This project is intended to add to the publicly



Marc Carter

available knowledge of those mechanisms.

Project History

It was a little before mid-2019 that we started having conversations. From some of the candidate organizations—mostly centered around bemoaning the absence of definitive conferences of industry accessible data—we know that there is very good testing that has been done by some of the larger OEMs and large printed circuit

networks. However, due to the nature of the commercial world we live in, a lot of that is proprietary IP and has been difficult sharing. That is perhaps starting to open a little bit. But when we started this project, it was a real problem, and the VTSL data sorting microvia group had hoped to do a lot of mining of existing data and was thwarted by that inability to get it past the IP police of various organizations.

We began the process of saying, “What are we going to do about this?” We began discussions among a select group of manufacturers, test organizations, simulation labs, and universities. The market segments were served, and similar processes were especially important.

One of the things that took the longest, if you are going to have two or more fabricators building a test vehicle, is getting an exact consensus on the details of layup and construction, which became an exceptionally long, hard, arduous process. In September of last year, the fabrication companies began the consensus material selection; we were in a fairly quick and early agreement. We wanted a material and stackup that was widely used and available, but perhaps not the most used, as the ultimate material. And that was also covered by those who would supply the material to support this test in return for access to the information.

In October of last year and running through at least January, the two fabricators collaborated in an exceptionally open manner. Those of us in the industry are used to helping each other out, but this was remarkable and resulted

in a consensus on a detailed layout and layout for the test article. We struggled with that because, as those of you that are familiar with the industry realize or have recognized in the past, if you put the exact same stackup layout design in front of two different fabricators, there are differences in their press operation, relief pattern, panel layout, and DFM projection software. That will get you two different results. We finally had to give ground on one dielectric layer in each to get to an identical predicted structure. In February, the test labs that we are working with on this began consensus discussions will continue detailed sample handling and testing.

And in late April of this year, the project proposal was submitted to the U.S. Army's Cornerstone Group at Rock Island. I must stress that at this point, when this was submitted, many thousands of dollars and hours of time were invested because we were concerned about this problem. We have gone about as far as we can go off the cuff. We need to get some funding, and since this is aimed primarily at military applications and use, that's why we're going to Cornerstone with this.

Objectives

Project objectives were to provide publicly accessible information on some contributors to the weak interface failure mechanism. If you try to do an ideal design that covered every possible element on a fish-bone diagram, we would all be much older, grayer, and many millions of dollars poorer than we are today. We have taken the approach of getting this in bite-sized chunks. From a manageability standpoint, getting viable data was quickly deemed preferable to getting the ultimate answer to all problems and questions in 10 years. We have taken the mini-phase approach.

We are going to help determine current limits on reliable design production methods and materials for use in high-density interconnect microvia electronics and critical high-reliability applications. We are not building cellphones or addressing that. This is a narrow market segment.

We are very eager to help enable improved correlation between predictive modeling, sim-

ulation reliability, and actual results. This is one of the reasons that our friends from ANSYS are so willing to help with this; they very much want to improve their ability to handle all different structural types of high-density stacked/staggered microvia reviews and be much more confident that those are going to provide reasonably good predictability.

**We are very eager to help
enable improved correlation
between predictive modeling,
simulation reliability, and
actual results.**

Each phase of this project is designed to inform and direct subsequent phases in terms of specific structures, materials, manufacturing testing techniques, etc., and to successively improve the predictive modeling. The first results will be compared with the predictive modeling, the predictive modeling will be readjusted, and then the second phase will make the same iterative loop.

The test article is seen in Figure 1, including covers stacked and staggered from one to four. It is a little more aggressive than the iMac ESA Structure. It is probably less aggressive than Lockheed's structure. We purposely chose to limit it to a single material in this first phase. It will provide a readout, though, on a few commonly commonly employed structural choices during the design phase. It gives staggered microvias in varying offset staggered, and there are a couple of microvia sizes there.

Methodology and Variables

- "Shop A" vs. "Shop B"
- Structure (stack height, stacked vs. staggered, stacked over buried, degree of offset, etc.)
- 17 different D structure coupons were required (when metallization included)

Layer	Min	Max	Thickness (Inch)	Stackup Picture TopLayer L1 / L12	Family	Description	Type DK / DF
SM1					TAIYO HFX		0.00 / 0.0000
L1	0.00042				Copper Foil	.375	POWER_GROUND-COPPER FOIL
	0.00273				370HR	2113-59%	4.02 / 0.0210
L2	0.00162				Copper Core	.375 + 0.0007	SIGNAL - COPPER
	0.00273				370HR	2113-59%	4.02 / 0.0210
L3	0.00162				Copper Core	.375 + 0.0007	SIGNAL - COPPER
	0.00330				370HR	106-76%	3.74 / 0.0210
L4	0.00162				Copper Core	.375 + 0.0007	SIGNAL - COPPER
	0.00412				370HR	106-76%	3.74 / 0.0210
L5	0.00060				Copper Core	.5	SIGNAL
	0.00500				370HR	0.0080 (1-7628)	4.28 / 0.0210
L6	0.00060				Copper Core	.5	SIGNAL
	0.00504				370HR	1080-65%	3.90 / 0.0210
L7	0.00060				370HR	1080-65%	
L8	0.00060				Copper Core	.5	SIGNAL
	0.00412				370HR	106-76%	3.74 / 0.0210
L9	0.00162				Copper Core	.375 + 0.0007	SIGNAL - COPPER
	0.00330				370HR	106-76%	
L10	0.00162				Copper Core	.375 + 0.0007	SIGNAL - COPPER
	0.00273				370HR	2113-59%	4.02 / 0.0210
L11	0.00162				Copper Core	.375 + 0.0007	SIGNAL - COPPER
	0.00273				370HR	2113-59%	4.02 / 0.0210
L12	0.00042				Copper Core	.375	POWER_GROUND-COPPER FOIL
SM2					TAIYO HFX		0.00 / 0.0000

Figure 1: Test vehicle article showing stackup, materials, constructions, and thicknesses.

- Reflow simulation temperature (eutectic, 230 °C, vs. lead-free, 260 °C; 10 reps)
- “Test Lab A” vs. “Test Lab B”
- Microvia formation method (mechanically drilled vs. laser-ablated, such as UV/CO₂/UV)
- Metallization (direct metallization vs. electroless copper)
- Note: Laminate material is not a variable in Phase 1

Some of the variables will be examined. Those of you who have been around the industry for a long time and have tried to do comparative studies of a particular problem or issue recognize that with the best of intentions and the most stringent controls on processes, process consistency and trying to match processes between two operations, is quite often the biggest and most statistically significant variable about who built the boards.

The two participating fabricators were selected in part because of the common processes they had and our ability to coordinate their efforts with back and forth shuttles. We have gracious technical support from chemical suppliers that supply the same direct metalli-

zation and electroless processes at both. We are making every effort we can to reduce the effect of uncontrolled variables but will try to capture that information and those side effects of shop-to-shop differences.

The structures we selected resulted in 17 different IPC-D structured coupons. Comparing direct metallization to electroless, that doubles. I will touch on reflow simulation temperatures later. There has been some discussion, and our test labs were very helpful in working through this. We are concentrating exclusively on the weak interface; we are not worrying about the various through-holes that are in the structure by necessity. Even more traditional microvia failures (cracks or voids in microvia sidewall, for example) are outside the scope of this study.

We intend to force the failure of the weak interface of the microvias by concentrating on the reflow simulation with the fabricator shops or test labs. Each test lab will get 102 samples of D-coupons from each of the two fabricator shops.

One of the variables will be microvia formation. And that is one of the differences between these two shops. Their microvia formation method: one is mechanically drilled, and

the other uses a UV/CO₂/UV laser formation technique. For metallization, both have the same electroless copper bath and the same direct metallization process offered by the same manufacturer.

Half of the coupons or panels at each shop will be done with direct metallization, and half will be done with electroless copper. And I must note that comparing different laminate material was not considered in phase one. We'd love to have the luxury of looking at different materials, but that's going to have to wait for phase two.

We expected to see some failures. I am counting on failures. The primary measurements for our statistics are going to be the survival number of cycles and the statistical likelihood of failure.

We're pretty confident we'll be able to do some good statistics on the relative significance of each individual variable. There has been a lot of work with each contributor to this problem. I'm going to be counting heavily on our friends at MTU, working on statistical analysis to see how much statistical reliability we can get from what really is—even though it is several hundreds of D coupons—still a small statistical sample. We need to see if we can determine the statistical significance of interactions.

One of the goals here is the final report out at a public venue, and the results will be the guide. Phase two and phase three structures are material and methodology.

Status

Build structures and data packages are ready to release to production, and materials have been donated by the material supplier. In return for access to the data, the raw material and technical support offered by both the material and the chemical suppliers have been very gratifying. The simulation will commence simultaneously with the start of the build. At this point, we have taken this project as far as we can out of pocket. We're waiting for funding.

Simulation for the sake of simulation is sort of a sterile exercise. Once we can commence the build of the test articles, then the simula-

tion will begin. And we have talked about this before, but the equivalent of thousands of dollars has already been invested in this thing.

What is the cost to completion? Phase one would be rated at about \$140,000 to just build test vehicles. Can you read that we estimate very conservatively? Time to completion is defined as this point of a phase one report out at a public venue is nine months after the funding is secured.

You may have noticed there has been some disruption of government finances in the past five months. There is some uncertainty. We have discussions ongoing about getting government entities to partner on funding through the Cornerstone Group. And for those of you who have tried to deal with government funding in the past, I can only recommend working through the Cornerstone Group as opposed to other funding venues that you tried to work with in the Defense Department. It is a far cleaner and more straightforward process, and the Cornerstone Group has been immensely helpful.

The future is obvious at this point for this group. We must secure the funding to complete phase one. We need to start getting some real data. Then, we can share that with others. One thing that was not immediately obvious in this from the start is that there was an area reserved on each of the panels that contains those test articles that each of the shops will retain for their own testing. They can perform their own internal and proprietary testing. That is fine. Everybody got something out of this discussion when we started this project. **DESIGN007**

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3. Yan Ning, "Reliability of Copper-Filled Stacked Microvias in High-Density Interconnect Circuit Boards," Doctoral Dissertation, UMD-CALCE, 2017.

This article first appeared in the October 2020 issue of PCB007 Magazine.



PCB007 Highlights



An Update on Walt Custer's EIPC Business Outlook Webinar ▶

"We're not out of trouble yet, but it's a whole lot better than a couple of months ago." Walt Custer's business outlook update, with emphasis on the European electronics industry, attracted a capacity audience to EIPC's webinar on October 2. Pete Starkey details how it wasn't all bad news.

Just Ask John Mitchell: The Exclusive Compilation ▶

We asked for you to send in your questions for IPC President and CEO John Mitchell, and you took us up on it! We know you all enjoyed reading these questions and answers, so we've compiled all of them into one article for easy reference. We hope you enjoy having another bite at the apple. And if you'd like to hear more from John Mitchell, view his column series "One World, One Industry."

Trouble in Your Tank: A Process Engineer's Guide to Interconnect Defects ▶

For those associated with PCB fabrication, one of the biggest nightmares is often the infamous interconnect defect (ICD). Essentially, an ICD is a separation of the plating from the interconnect foil. In this column, Mike Carano focuses on Type 1 ICD and D-sep.

The Big Picture: Globalization—Imagine a United States That Isn't United ▶

What if the U.S. was fragmented with 50 state fiefdoms, each with their own rules and barriers blocking the free flow of goods and services across state lines? We cannot even imagine such a scenario, yet that is exactly what's happening—fortunately not across state lines, but across global borders. Mehul Davé

advocates for starting the hard work to get globalization back on track.

Punching Out! Bringing PCB and PCBA Industries Back to the U.S. ▶

Although U.S. PCB companies have been waving the flag for years, the COVID-19 crisis has shined a spotlight on the U.S. dependency on overseas suppliers for many electronics products. Tom Kastner lists five ways production will come back to the U.S.

American Standard Circuits Now Offers Copper Filled Blind Vias ▶

West Chicago circuit board fabricator American Standard Circuits now offers copper filled via technology.

Insulectro Opens Shop With All-New Printed Electronics E-Commerce Site ▶


Insulectro, the largest distributor of materials for use in the manufacturing of PCBs and printed electronics, rolled out its new online shopping center (insulectro-pe.com) for conductive inks and pastes plus advanced substrates and films.

EIPC Technical Snapshot: Automotive Technology ▶

Although current circumstances have forced the postponement of its live conferences, seminars, and workshops, EIPC continues to provide a platform for the exchange and dissemination of the latest knowledge and technical information to the European interconnection and packaging industry. Pete Starkey details how its current series of technical snapshots, delivered in a webinar format, address technology challenges facing the automotive, telecom, and high-speed sectors of the industry.

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Routing Strategies for High-Speed PCB Design

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

As the typical PCB design becomes more complex, so do the techniques and strategies required—not only to complete the design but also to create a functioning product that performs to specification. Autorouters have improved dramatically over the past 20 years, allowing the PCB designer to produce seemingly hand-crafted results in an incredibly short time. However, the autorouter is guided by design constraints, and there are only so many rules that can be practically defined. Every situation is different, requiring unique tradeoffs. The limiting factor with any autorouter is describing just what it is that human decision-makers actually do.

PCB designers need to understand the underlying high-speed issues of the design based on simulation (Figure 1) and then translate these into corresponding design constraints. Constraints can always be altered on the fly if a particular constraint is too tight, providing the designer can justify the easing of the specification and that the product is still manufacturable.

Firstly, a pre-layout simulation defines the extent of placement. Controlling the placement of devices limits maximum trace length, reduces flight-time-delay and skew, and assists in compliance with timing specifications. To obtain a high route-completion rate, component

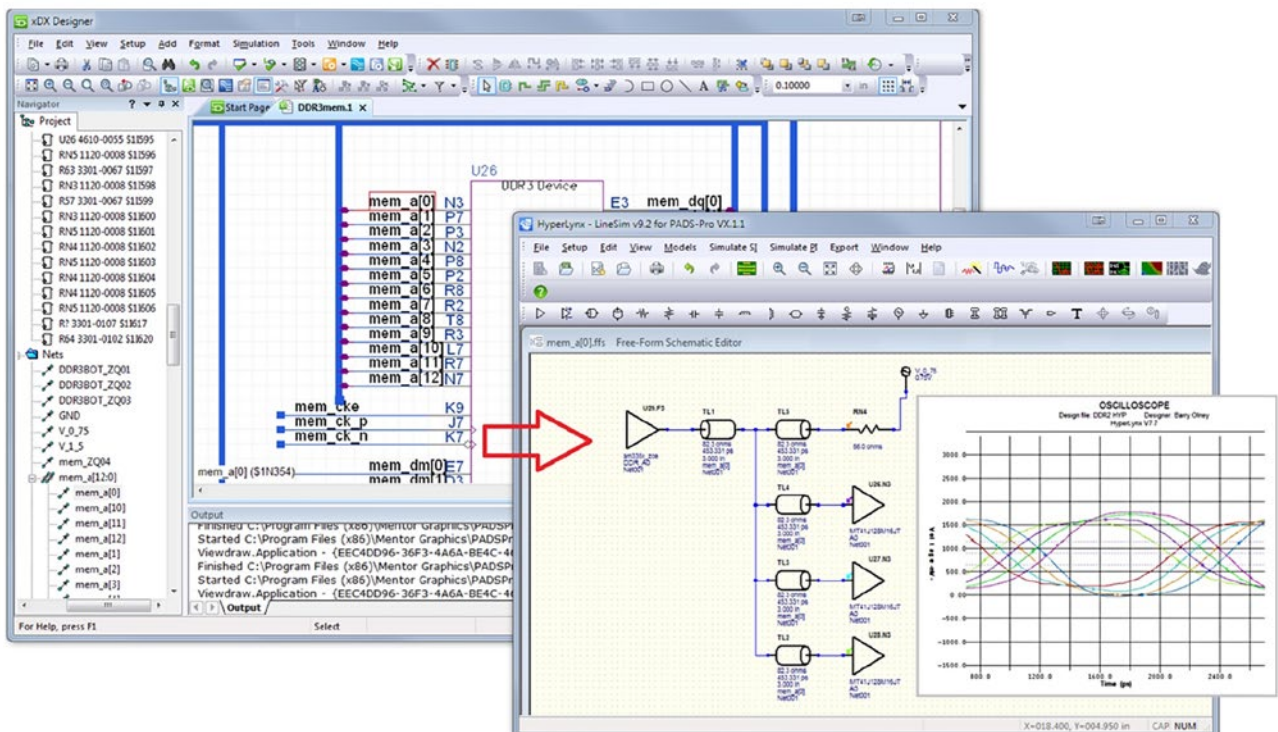


Figure 1: Develop high-speed design constraints based on pre-layout simulation.

Create Comprehensive PCB Documentation to Drive Fabrication, Assembly and Inspection



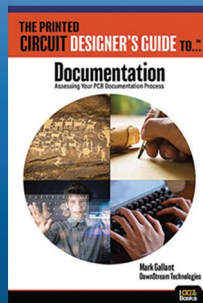
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placement is extremely important. If the board is difficult to route, it may just be the result of poor placement, slots/gates positioned all over the board, or perhaps the sequence of pins on components are flipped. We need to assist the router as much as possible by opening route channels and providing space for vias.

Secondly, there are six important issues to consider before you commence with the process of formally routing the board:

1. The stackup should be planned to ensure that controlled impedance signals have been calculated correctly and that the return current for each signal layer has a clear return path. The resulting stackup configuration should then be transferred to the design rules to define the correct trace width and clearance for each layer and to specify the differential pairs.
2. The power distribution network (PDN) should be planned and bypass and decoupling capacitors placed in the appropriate positions. The iCD PDN Planner is an ideal sandbox for this analysis. It is a good idea to color the power nets with individual colors so that they can easily be recognized without having to name the net.
3. Design rules and constraints can be passed from the schematic, which automatically sets the design rules in the PCB database, though there is always some adjustment to be done on the PCB side.

4. Via sizes for different net classes need to be defined. This is important for route completion.
5. For rules to properly support the design process, they need to be defined in the correct priority so that the most important rules prevail over rules of lesser importance.
6. Set up the routing options. It amazes me that most EDA tools do not come with the router set to the most useful functions straight out of the box. Before routing, one must tweak the route options to get the tool to do what you want. Details vary by the tool, of course, but the nuisance is near-universal.

Thirdly, most popular EDA tools have the ability to cross-probe between the schematic and the router. This is a fantastic feature that enables a PCB designer to build up an extremely dense, complex route in a couple of hours by controlling the router from the schematic rather than just pushing the autoroute button and hoping for the best.

Cross-probing can also be used as a powerful search tool, locating parts and nets on the schematic or PCB. And cross-probing is not limited to schematic and PCB. Mechanical tools allow the cross-probing between PCB and 3D MCAD database, enhancing mechanical visualization of the product.

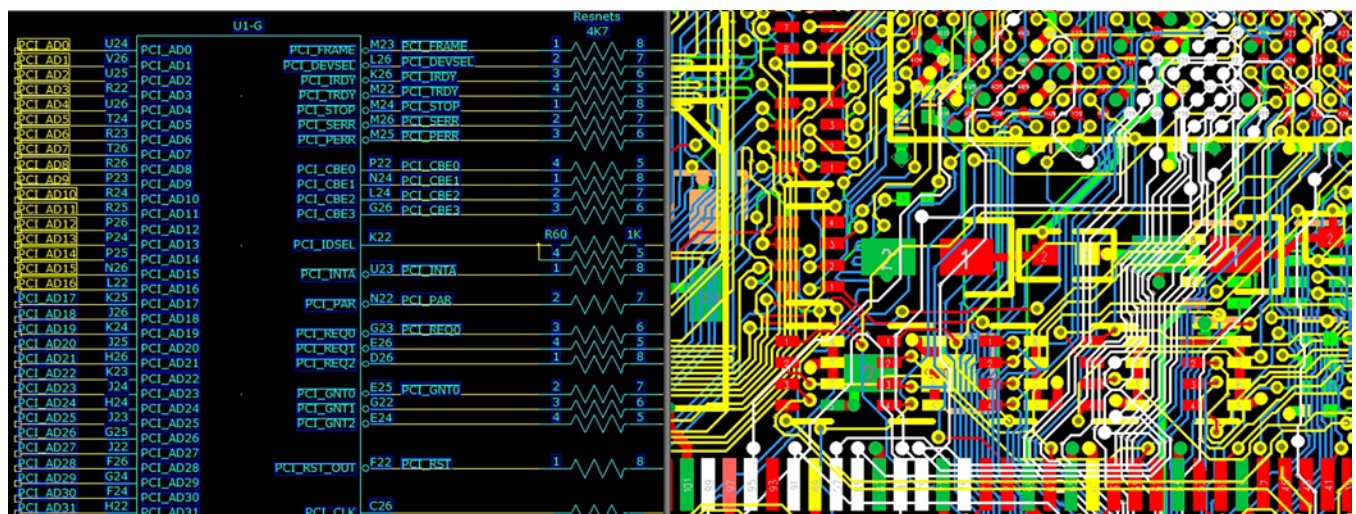


Figure 2: Cross-probing from schematic to router of part of the PCIe bus.

Finally, one should avoid routing high-speed signals on the outer microstrip layers of a multilayer PCB. This can decrease radiation by up to 10 dB. Plus, inner stripline traces are less susceptible to outside noise as they are sandwiched between two planes.

The four constraints to keep in mind are as follows:

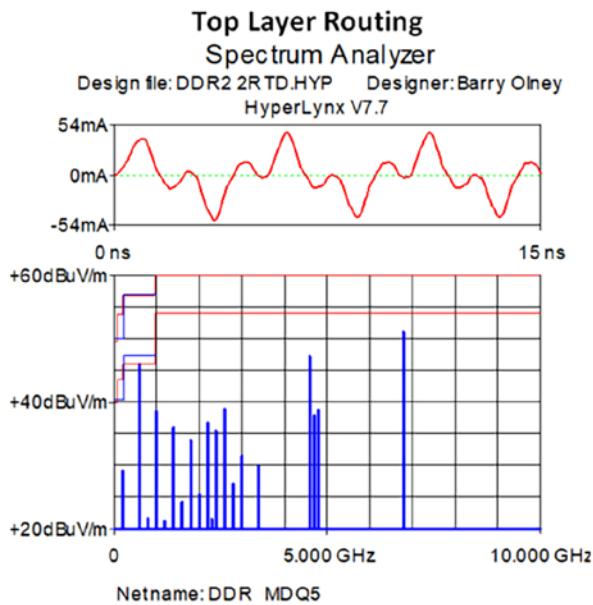
1. Keep the mark to space ratio of the waveform equal as this eliminates all the even harmonics leaving only the odd harmonics.
2. Route high-speed signals out from the center of the board where possible as any radiation will be in the opposite direction and will tend to cancel out.
3. Route high-speed signals between the planes. Fan-out close to the driver (200 mils), dropping to an inner plane, and route back up to the load again with a short fan-out.
4. Use the same reference plane for the return signals, as this reduces the loop area and hence radiation.

Let’s make a comparison of the radiated noise between the top layer and inner layer routing, as in Figure 3.

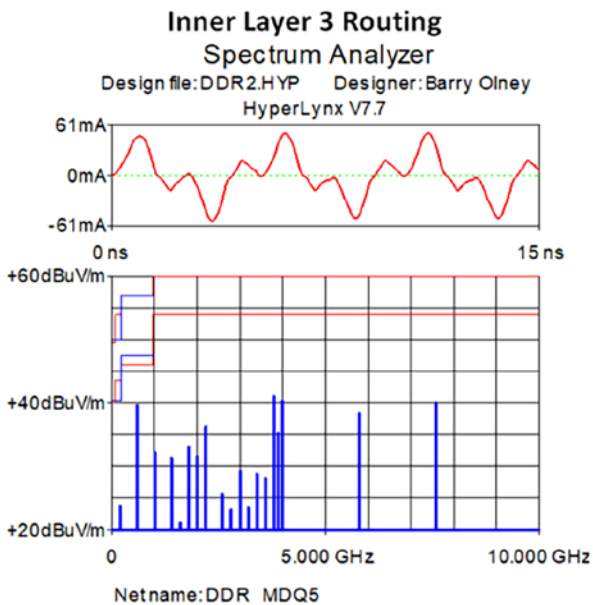
As you can see (with all other factors being equal), in this case, the trace routed on inner layer 3 exhibits 4–10 dB less noise than the trace routed on the top layer. The high-frequency components radiate more readily because their shorter wavelengths are comparable to trace lengths, which act as antennas.

You do not need to do any manual routing yourself to get an acceptable route of the non-critical nets. Of course, matched delay, differential pairs, and other critical signals should be routed with the precision they demand. This is the process:

1. Start by placing all the components by functionality, selecting the desired component on the schematic, and placing it in the best location/rotation to aid the routing.
2. Similarly, when routing, select a chip on the schematic (the nets are highlighted on the PCB) and then fan-out with the router.



Top layer Harmonics:
46 dB @ 595 MHZ
45.65 dB 4.595 GHz
49.73 dB @ 6.76 GHz



Inner layer 3 Harmonics:	Difference:
39.69 dB @ 619 MHz	6 dB
41 dB @ 3.8 GHz	4 dB
40 dB @ 7.57 GHz	10 dB

Figure 3: Comparison of radiation from microstrip and stripline routing.

3. Select the critical nets on the schematic, fan-out, and then route with the auto-router.
4. Push and shove the traces to the desired location, move on to the next group of nets, and repeat. Each group of routed traces should be verified after completion. Lock if necessary.

When you drive the router from the schematic, it's possible to see what needs to be done without entering too many conditional design rules, and you can later manipulate the traces as if they were hand-routed.

Once the routing is complete, apart from running design rule checks (DRCs), run a sanity check on the board. You can either do this in the simulation environment or the PCB database. Simply highlight each net one by one. This is tedious but gets results. You can quickly see if any nets are longer than the Manhattan length or spiral around the board before termination.

Key Points

- The autorouter is guided by design constraints, and there are only so many rules that can be practically defined. Every situation is different, requiring unique tradeoffs.
- The underlying high-speed issues of the design need to be translated into corresponding design constraints.
- A pre-layout simulation defines the extent of placement.
- If the board is difficult to route, it may just be the result of poor placement.

- The stackup configuration and PDN needed to be addressed before commencing routing.
- Cross-probing enables the PCB designer to build up an extremely dense, complex route in a couple of hours by controlling the router from the schematic.
- Cross-probing can also be used as a powerful search tool, locating parts and nets on the schematic or PCB.
- One should avoid routing high-speed signals on the outer microstrip layers of a multilayer PCB. This can decrease radiation by up to 10 dB. **DESIGN007**

Further Reading

- B. Olney, "Beyond Design: High-Speed PCB Design Constraints," *Design007 Magazine*, May 2019.
- B. Olney, "Beyond Design: Embedded Signal Routing," *The PCB Magazine*, September 2011.
- B. Olney, "Beyond Design: Interactive Placement and Routing Strategies," *The PCB Design Magazine*, December 2012.
- B. Olney, "Beyond Design: Routing Techniques for Complex Designs," *The PCB Design Magazine*, January 2013.
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Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at icd.com.au. To read past columns or contact Olney, [click here](#).

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High Reliability PCBs.

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7 Things to Consider When Buying a PCB Design Tool

Article by John McMillan
MENTOR, A SIEMENS BUSINESS

“Once a new technology rolls over you, if you’re not part of the steamroller, you’re part of the road.”
—Stewart Brand

Price is only one factor to consider when making a PCB tool purchase decision. Indeed, in EDA, it is a tool’s differentiating qualities and capabilities, more than initial cost differences, that, in the long run, actually save you more in time and money.

For example, if your PCB design tool has a unique capability or functionality that can eliminate even a single PCB prototype build or respin, any price difference can quickly become insignificant. Likewise, if a design tool has capabilities that enable you to accelerate the design cycle by as little as 10% and gets your product to market faster than a competitive tool, it can quickly make a price difference irrelevant.

Clearly, PCB design tools come with different capabilities and can be targeted for different

electronic product spaces. Most importantly, perhaps, choosing the wrong tool for your designs can cost you dearly in terms of time, profits, and even the health of your business. It is essential that you fully understand the cost-performance measurements for each aspect of the products you are considering.

But how do you know what to look for? This article describes seven important things you should consider when purchasing or replacing a PCB design tool or flow. By following these guidelines, you will help your company choose the right tools for your design environment and product markets.

1. Adopt Tools That Make Your Products Best-in-Class

The PCB design tools you select should have the features and functionality to make sure your products are best-in-class. That is, the tool flow must allow your products to be designed optimally, reliably, cost-effectively, and in a single pass. The leading motivators for improving PCB design, according to a November 2019 Aberdeen study, are shown in Figure 1.



Because failure is not an option.

In your daily life you are dependent on a lot of products. The car you drive, the airplane you fly in or the ECG equipment measuring your heart. You expect them to work – because they have to.

All electronic products have a PCB inside. At first sight they may all look the same. But it could be a world of difference between a normal and a High Reliability PCB.

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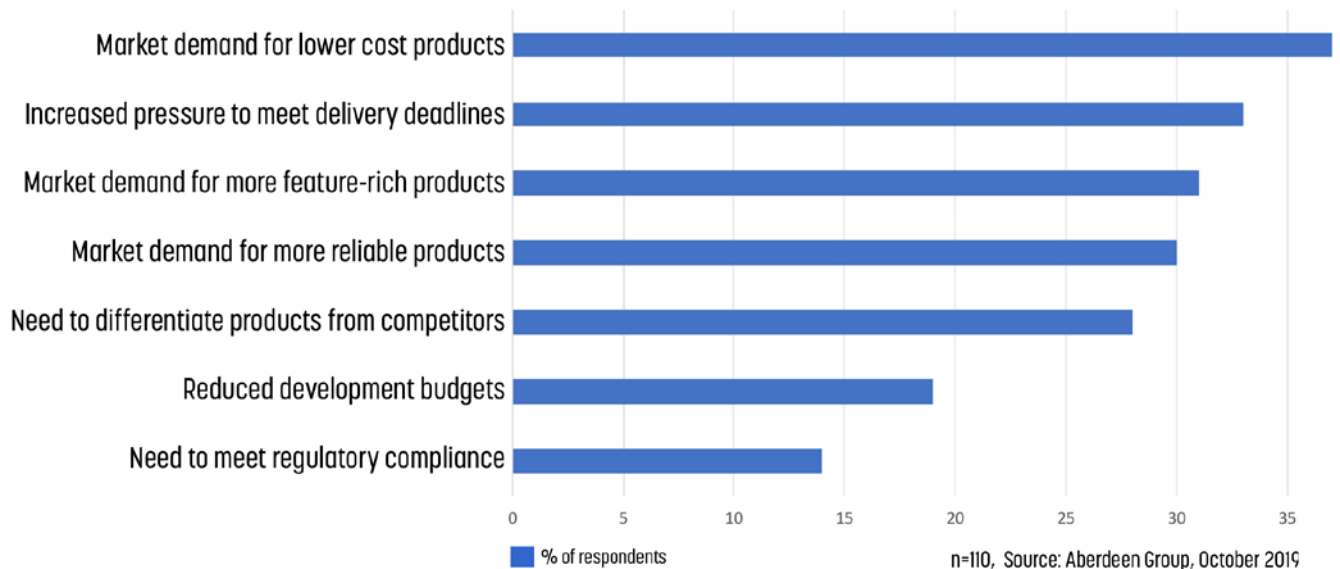


Figure 1: Pressures to improve PCB design.

To meet these pressures, companies need PCB design tool features and capabilities that help reduce product cost, accelerate time-to-market, and ensure product reliability in their electronic product's space. For example, in the cellphone market, you know that product dimensions, physical interfaces, buttons, and screen locations, etc., are all influenced by the competition and the consumer. Therefore, in this space, a PCB tool with features, including MCAD collaboration, rigid-flex, and RF-centric design capabilities—along with the ability to simulate and address possible signal integrity, power delivery, and thermal issues—is essential.

2. Size PCB Design Tools to Fit Your Products

As the spectrum of PCB design complexity is very broad—from very simple, inexpensive, single- and double-sided PCBs to highly complex, high-density, multilayer, and mixed-technology systems—so is the range of PCB design products. Thus, PCB design tools are developed with various levels of functionality and cost targets to support different product markets.

Determining the PCB design tool flow that fits your specific product space is critical for

ensuring that you have all the functionality your designs require. Likewise, selecting a PCB design tool that is too complex for your designs can unnecessarily complicate and delay product creation.

There is a vast array of design tools—from freeware tools created predominantly for makers and hobbyists to enterprise tools, also referred to as enterprise application software (EAS), used by the world's leading technology companies. Maker and hobbyist tools are typically easy to use and intuitive. They are best suited for one-off or short-run production designs. Enterprise software must provide the sophistication to drive innovation and invention in all areas of electronic design. Step two in a PCB tool purchasing decision is to determine your product complexity and business needs.

3. Select PCB Design Tools That Match Your Business

Keep in mind the technologies your product requires, as well as your business' capabilities, expertise, and challenges when selecting a PCB design tool. PCB design tool companies in each PCB tool segment compete by implementing design features and functionality that differentiate their tool from those of competitors,

which provides levels of integration that suits their design environment and product market.

From simple PCB design tools created for makers to tools aimed at desktop, small, and mid-sized businesses, to fully integrated enterprise solutions, the features and capabilities for each tool vary from market to market and from tool vendor to tool vendor.

Developed predominantly for the student, hobby, hacker, and maker communities, maker PCB tools are available as freeware or very low-cost tools. They are best suited for making PCBs that are single layer or generally simplistic designs with only a few layers and are typically limited in functionality but intuitive and easy to use.

Small electronics design companies want a few more PCB design tool features and capabilities than maker tools provide. These tools typically support more layers, pad and shape definitions, better manual routing, some level of properties and net management, pre-made libraries, and online technical support. They typically lack features like schematic-layout integration, constraint management, and rules-driven place-and-route, yet they are suitable for creating small products.

Mid-sized businesses usually need the horsepower to design complex PCBs without the infrastructure demands and challenges associated with an enterprise tool. These are typically self-contained, integrated, full PCB design flow tools that support hardware engi-

neers and small workgroups. With support for FPGA design, enhanced RF, rigid-flex, and high-speed design, MCAD collaboration, part and model libraries, and more, these tools generally have or make available access to the advanced features and capabilities required to design today's modern electronic products.

Enterprise tools not only provide access to all PCB design capabilities but also support the level of integration required to address all the complexities of working with big design teams, even those spread throughout the world. The enterprise design flow helps large companies more efficiently leverage design team resources and manage intellectual property on a global basis by supporting things like IP management, supply chain integration, and design team coordination across multiple divisions and sites.

4. Compare the Differences Between PCB Design Tool Features

Ensuring that your electronic product can be designed in any PCB design tool flow may very well require taking the time to evaluate and benchmark competitive tools. The aim of benchmarking is not to determine mastery of the tool but rather to identify the product's strengths and weaknesses and use that information to ensure you are making the correct product selection.

There are unique and specific ways that different PCB tools approach design. Same-named



Figure 2: Differentiation between two mid-sized PCB design tools.

operations, like routing, that seem intuitively straightforward can be vastly different from design tool to design tool. Capabilities like rigid-flex, radio frequency, MCAD collaboration, simulation, and validation are other areas in which PCB design tool features and capabilities are not created equally, are unavailable, or may require third-party tools to accomplish.

Understanding the PCB’s technologies and execution is extremely critical when selecting a design tool. Tech companies that do not fully consider all of their product’s design requirements and later discover the design tool they have selected falls short will see detrimental impacts on their product’s cost, performance, and time-to-market—even on their business.

5. Pick a Design Tool That Can Shift-Left Your Methodology

The goal of the shift-left approach is to move as much verification as possible to as early in the design cycle as permissible while also automating analysis to provide the highest possible degree of coverage. Identifying and correcting issues at the source eliminates time-consuming debug efforts and costly respins. It

is a more efficient process that provides more predictable results, eliminates design respins, and yields higher quality products in less time.

When we rely on physical prototypes or sophisticated simulation tools to verify designs late in the design cycle, simple errors that should have been caught earlier can require weeks of effort to identify and fix. Though many companies accept this as an inevitable result of increased product complexity, it doesn’t have to be that way. Product creation and PCB design flows as a whole have evolved over the past decade. We’ve gone from the traditional “linear approach”—where a single, simple mistake can derail a project and cost thousands or even millions of dollars—to a design flow based on a modern shift-left methodology that is more intelligent, accelerates design cycles, and ensures product reliability and performance.

Within this shift-left PCB design methodology, verification tools are integrated throughout the design process, enabling designers to find and fix errors where they happen instead of waiting until later in the flow. This is accomplished with automated verification tools that



Figure 3: Shift-left design flow example.

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are part of the design process instead of forcing designers to run separate tools. Analysis is run automatically, and users are immediately presented with issues to investigate and fix if needed. This means basic errors are caught and fixed before they have a chance to propagate and cause other problems, making the whole design process more effective and predictable.

The shift-left solution integrates a broad range of analysis and verification tools during the schematic and layout phases of the project. These tools are aimed at non-specialist PCB design engineers and layout designers, enabling them to work within their familiar authoring environments to identify problems early in the design cycle.

6. Create a Tool Flow That Supports Early Collaboration Between Design Disciplines

There are numerous design challenges in electromechanical systems that can cause issues that affect both the electrical and mechanical domains. A PCB design flow that supports electromechanical collaboration ensures that both domains are synchronized to enable consistent, iterative communication between design disciplines. This is essential to productivity, product success, eliminating electromechanical respins, and reducing product costs.

A design flow that allows design engineers or teams of engineers to simultaneously work together to create an electrical design from schematic through to PCB is exponentially faster than if each step is done by one person at a time. Similarly, a mechanical engineer or team can collaboratively utilize electronic data transfer information to simplify the start of a PCB design and make traditionally time-consuming engineering changes in just a matter of minutes.

In modern electromechanical designs, tight synchronization between the electrical and mechanical flows is required to ensure that both design domains are correctly aligned for fabrication, which ultimately decreases the design effort and accelerates product time-to-market. Today, many companies still utilize

the traditional Intermediate Data Format (IDF) to transfer information between electrical and mechanical systems, versus a more advanced MCAD collaboration.

7. Make Sure Your PCB Design Solution Is Scalable

From the earliest stages of an electronic product's definition and functional specification, careful consideration of all of the product's hardware design requirements and complexities must be fully understood early on. Thoughtful consideration for a product's evolution helps in determining a PCB tool design flow or environment that not only accomplishes your design needs for today but tomorrow as well.

Regardless of the size of your tech company, the number of designers/engineers working on a project, or the complexity of a design, you need a PCB design tool flow that provides the appropriate capabilities as they become necessary. This kind of scalability is needed not only to move designs from conception to manufacturing but also to transition and support designs when a maker requires a desktop tool, when a start-up company grows from a small to a mid-sized business, or when a small or mid-sized company becomes the next Fortune 100 company and requires a fully integrated enterprise design environment.

Conclusion

Clearly, price is only one factor to consider when making a PCB tool purchase decision. Hopefully, these seven tips will help you choose the right tools for your design environments and product markets. **DESIGN007**



John McMillan is a technical marketing engineering manager at Mentor, a Siemens Business. He has over 30 years of experience in the EDA industry. Visit I-007eBooks.com to download

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The Fundamentals of Via Design

The Bare (Board) Truth

Feature Column by Mark Thompson, CID+, MONSOON SOLUTIONS

This month's column will address what vias are and what they are used for, as well as how they are used in PCB design. I'll also cover some criteria on pad size vs. via size for fabrication.

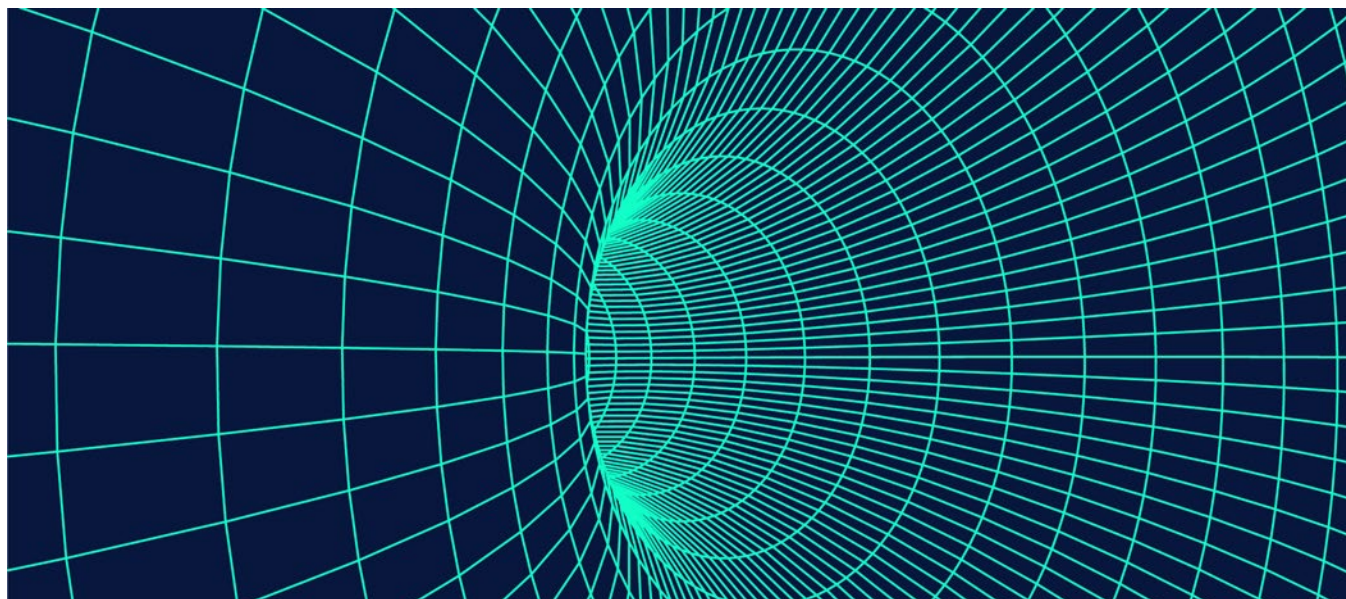
Introduction to Vias

But first, how did vias come about? That's easy. The first PCBs were all through-hole components, meaning a plated hole from one side to the other, from top to bottom. When board densities became more of an issue based on available real estate, components went from a 4-pin to an 8-pin or a 12-pin connector, etc., using all through-holes to a surface-mount-type connector in an effort to use less board space. Thus, the first use of mechanical through-hole vias.

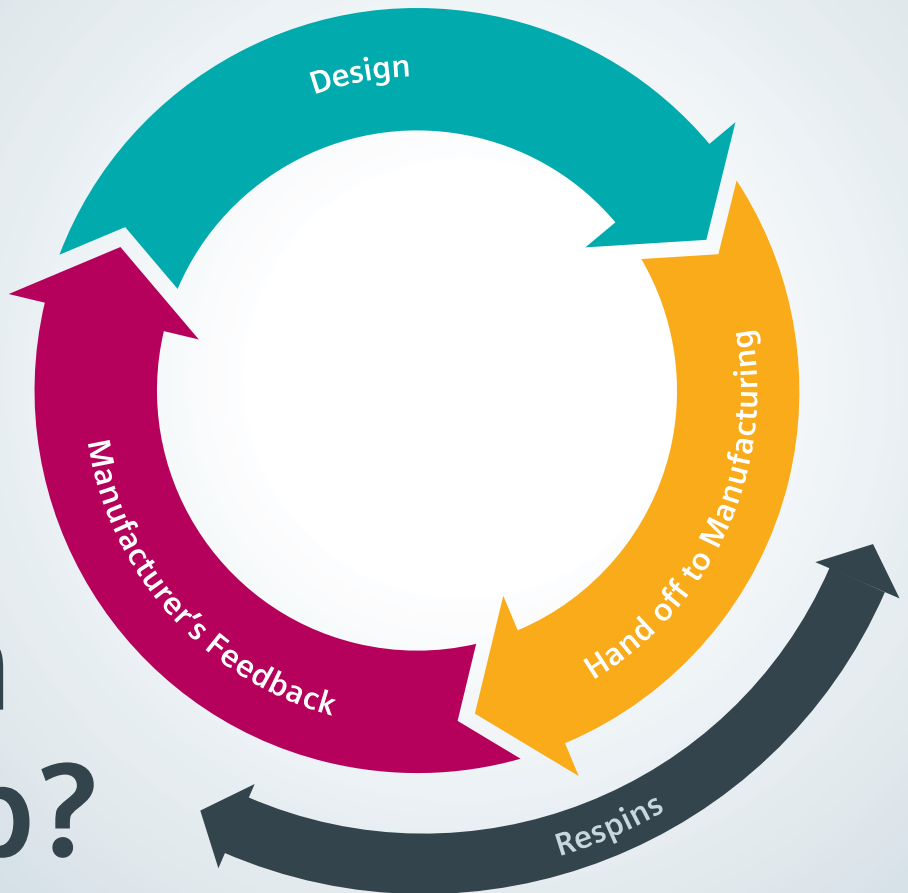
The process for this is quite simple. Based on the tolerance expressed on the drill draw-

ing, the vias (and component through-holes) are drilled larger (typically, 0.004–0.005") than the necessary finished hole size. If the part is a simple two-layer board, the process is as follows. The dielectric material is pulled then taken to the drilling department. Before this operation, the CAM department will specify the proper drill size to use, and a drill programmer will set up the start and stop codes using those drill sizes for the N/C drill machine.

Once drilled, the part would go through a series of cleaners and conditioners and then into a catalyst before the electroless copper stage, where the electroless copper deposition is done. The electroless stage is not an electro-winning process like electroplate and only lays down about 0.4 mils of electroless copper in the barrel of the hole and on the panel surface. This acts as a "tooth" or a bit of metal for the electroplated copper to adhere to.



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The parts are then taken to an imaging department where a photoresist is applied to the panels, and the panels are imaged. Then, the image is developed and taken to the electroplating department where the now-exposed traces and pads are plated—hence the reason holes are compensated larger before the plating process. After plating, they end up at the size and within the tolerance described on the fabrication drawing.

A multilayer is slightly different. The core material is pulled and coated in the dry-film department, and the parts are also imaged. If a standard multilayer with no blind or buried vias exists (I will get into them later in this column), the process in the plating department is a develop, etch, and strip process. The image is a negative image, so where the light sees the panel, it hardens the resist, thus protecting the traces and plane layers.

IPC Standards

Why did I talk about how a fabricator processes a given hole? Let’s talk about IPC standards. However, I will not talk about Class 1 since most products are Class 2, 3, or even 3A.

In a Class 2 IPC-6012 part, both external and internal holes can have as much as 90-degree breakout and still be acceptable (Figure 1). But for Class 3 and Class 3A, the external *must* have a minimum of a 0.002” annular ring *after* drill and plate, and the internal layers must have at least 0.001” annular ring.

That means if the part needs to meet a higher class based on its function and application, you need to design the board knowing

the fabricator will over-drill the plated holes approximately 0.004–0.005” over the hole’s size stated on the drill/fab drawing. A 0.008” hole with a 0.012” pad would not be acceptable, as the part will be over-drilled by 0.004–0.005”; in the case of Class 3 and Class 3A, the part must also have an additional 0.002” annular ring. Add to this that a fabricator has both a true position tolerance and a machine tolerance (normally ± 0.003 ”), so truthfully, given Class 3 IPC-6012, the pad size should take into consideration all of these variables. Is that even feasible?

Let’s say the Class 3 IPC-6012 via size is 0.008” expressed as ± 0.003 ” tolerance. If that were true, you would need to drill the hole at approximately 0.0138”, and the machine tolerance plus the true hole position tolerance of ± 0.003 ” would mean a 0.016–0.018” addition to the nominal hole size (again expressed as ± 0.003 ”). Thus, the pad size would need to be 0.026”. That is not feasible in board design where real estate/board area issues exist.

This brings me to the reason I bring up the fabrication process for holes in the first place. If the holes are simply vias, for many years now, I have told our customers (in my previous life as a board fabrication guy) to call them out as ± 0.003 ” the entire hole size. This way, a 0.008” via could be drilled at 0.008”, and no compensation or over-drill would be required. This now means a Class 3 IPC-6012 part could be as little as 0.016–0.018” for a pad size and even less if negotiated with the fabricator if they have good control of their machine and true position tolerance.

Plated Through-Hole Characteristics		
Class 1	Class 2	Class 3
180° annular ring breakout from the land is acceptable, provided the minimum lateral spacing is maintained.	90° annular ring breakout from the land is acceptable, provided the minimum lateral spacing is maintained.	The minimum annular ring should not be less than 0.05 mm.
The land/conductor junction should not be reduced by more than 30% of the minimum conductor width.	The land/conductor junction should not be reduced by more than 20% of the minimum conductor width.	The minimum external annular ring may have a 20% reduction of the minimum annular ring.
	The conductor junction should not be less than 0.05 mm or the minimum line width—whichever is smaller.	

Figure 1: IPC annular ring acceptance criteria.

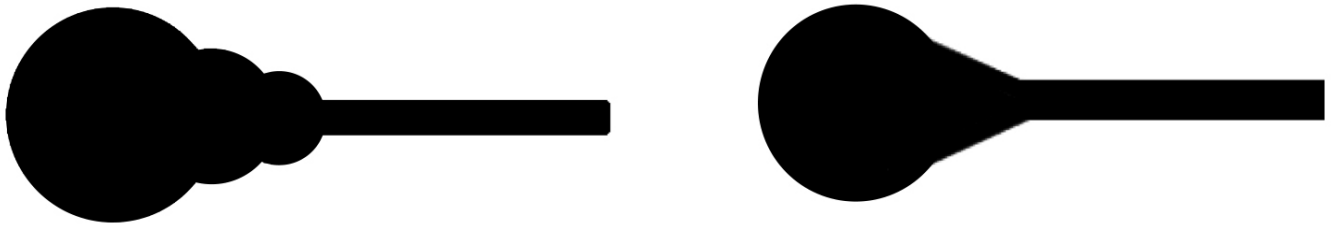


Figure 2: Snowman teardrop (for obvious reasons) on the left; fillet-style teardrop on the right.

One thing I was told many years ago was, if we added up all the tolerances, we would never be able to build a PCB. Luckily, many of the tolerances cancel out each other.

Teardrops

What about the use of teardrops? Teardrops are simply a fillet at the junction where the trace connects to the pad. This is done so that the hole will not break out of the throat where the trace meets the pad causing a disconnect. If you have enough room on your board design, one way to mitigate the induced drill wander that occurs in a fab environment is to use teardrops. Some examples of various teardrop styles are shown in Figure 2.

Via Types

Here, I'll detail a variety of via types, including (1) through-hole vias, (2) blind vias, (3) buried vias, and (4) stacked and staggered vias (Figure 3).

1. Through-Hole Vias

These are simply vias that go from the top to the bottom layer and are through-hole plated. They are used to pass a signal from one side of the board to the other or to make interconnects in the case of a multilayer.

2. Blind Vias

These are vias that either start from the top or the bottom side and terminate on a given internal layer. They are typically used for where board space is a premium. Examples include blinds 1-2, blinds 1-5, and blinds 3-6 (6 being the bottom layer). Note that you will need a separate NC drill file for each blind via scenario.

This can typically be done 2-3 times, but normally no more than 2-3 times from a given

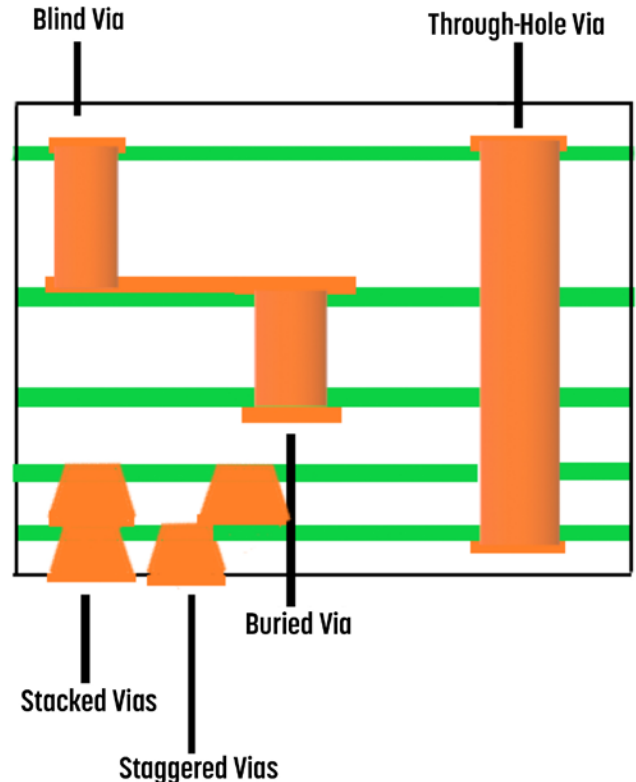


Figure 3: Types of vias.

side. The limitation is the number of plating cycles the outer layer sees. A 10-layer example would look like top to layer 2, top to layer 3, top to layer 4, bottom layer to layer 9, bottom layer to layer 8, and bottom layer to layer 7. To make more layer connections for 14-, 16-, or 18-layer boards, buried vias can be used in conjunction with the blind vias.

Types of Blind Vias

Sequential Blind Vias

The termination inner layer is processed on the core, leaving the associated outer layer as a copper sheet only to be imaged after lamination.

Controlled-Depth or Back-Drilled Vias

All the inners are processed as a normal multilayer and then laminated as normal. The connection to the inner blind layer is done with controlled-depth mechanical drilling. The drilling can drill partially into the core between layers but must not connect to the layer past the blind termination layer.

Laser Blind Microvias

Use of a laser, either Nd:YAG (neodymium-doped yttrium-aluminum-garnet) or Nd:YLF (yttrium-lithium-fluorine), can only go through very thin substrates. An infrared laser can inherently penetrate deeper but is not able to remove copper with the longer wavelength they emit.

Laser Microvias

These are typically used for high-density interconnection (HDI) designs. Due to the physical shape of a laser microvia, the depth of a given microvia is typically two or less consecutive layers deep due to the copper plating constraints of having to remove the ablated ash produced by the laser. They can be stacked or staggered, and both are additive processes. Microvias are used for higher functionality in less space, such as cellphones or tablets.

3. Buried Vias

A via is either mechanically or laser drilled between inner layers and does not extend to the surface layers (such as blind vias). They are drilled and filled (either laser or mechanically drilled). They are usually filled during the lamination process by the prepreg.

Uses of Various Vias

Via-in-Pad and VIPPO

With the extensive use of fine-pitch devices and smaller PCBs came the advent of via-in-pad structures. Via-in-pad is literally a via inside of a pad. It is first drilled, plated, or flash plated, filled with either epoxy or copper epoxy, and planarized so the surface is made flat for the assembly process. The advantage of this technology is tighter, more closely packed compo-

nent placement, enhanced thermal management, and elimination of parasitic inductance and capacitance as these reduce the signal path lengths.

Via-in-pad plated over (VIPPO) is basically the same as via-in-pad with the exception that it is associated with an SMT pad, not a normal pad, such as one for a blind via. Additionally, VIPPO is also used where they will also back-drill (controlled depth drill) out the excess metal from the hole beneath the termination to an internal layer.

Thermal Vias

These dissipate heat from one side of the board to the opposite side of the board and are typically placed directly below (or as close as possible) heating elements or components that generate a lot of heat. PCBs are more conductive across the board than they are through the dielectric.

If traces are only present on the outer layers, then most of the heat is carried sideways (horizontally), and the internal core planes may be cooler. This adds thermal stitching vias connecting surface features to the internal planes and creates more conductivity that dissipates heat to the core, reducing the overall temperatures more effectively.

Stitching Vias

Via stitching uses ground coupling. The most common use for stitching vias in a plane is to ensure short return paths for signals or to help maintain a constant ground. As soon as any current starts to flow, it will cause a voltage across the copper through which it is flowing, serving to both spread the current out but also cause the ground to bounce around. Via stitching can be an effective and low-effort way to more tightly couple ground across the PCB.

Shielding Vias or Via Fences

After reading a lot of literature on shielding vias, I will paraphrase the information I found. Via fences, also known as “picket fences,” are structures to improve isolation between components that would otherwise be coupled by

electromagnetic fields. They contain a row or two, or even three rows, of vias spaced close enough together to form an electromagnetic wave barrier.

Via fences can be used to shield microstrip and stripline transmission lines or functional circuits from each other. However, via fences too close to the line being guarded can degrade the isolation of the line/circuit. They can also be used around the periphery of a board to prevent electromagnetic interference with other equipment.

4. Stacked and Staggered Vias

Stacked and staggered microvias are done with a laser (Nd:YAG or Nd:YLF) exactly as described earlier. Stacked vias are literally stacked upon each other by an additive process, and staggered vias are staggered so that they do not reside directly over each other.

The advantage of stacking vias is extremely dense board designs, such as via-in-pad structures within tight-pitch BGA footprints. For this, the vias are drilled with a laser and then plated, filled, and planarized to create the

interconnect. The next layer is done by laminating another layer on top of the previous via. This can typically be done 3–4 times (or more, depending upon the fabricator). Then, the surface layer is planarized (made flat) so that the PCB is flat at assembly, and no “part rocking” will occur.

Conclusion

In this column, I repeatedly oversimplified both the function and process for vias. Ultimately, consult your chosen fabricator for more detail on capabilities and process limitations. Thanks for reading! **DESIGN007**



Mark Thompson, CID+, is a senior PCB technologist at Monsoon Solutions Inc. To read past columns or contact Thompson, [click here](#). Thompson is also the author of *The Printed Circuit Designer's*

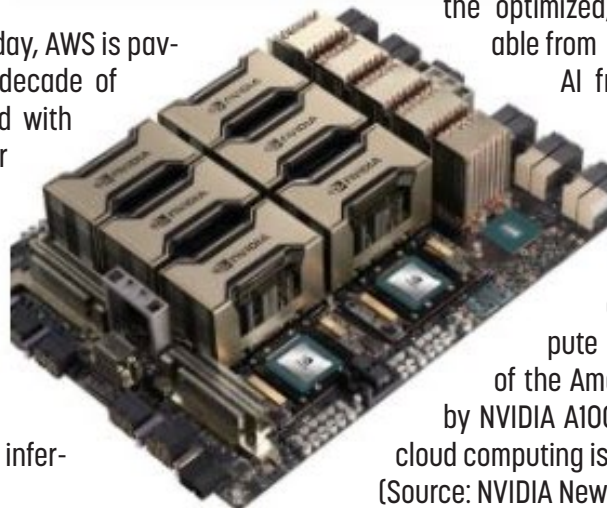
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NVIDIA A100 Marks Dawn of Next Decade in Accelerated Cloud Computing

Amazon Web Services' first GPU instance debuted 10 years ago with the NVIDIA M2050. Since then, AWS has added to its stable of cloud GPU instances, which has included the K80 (p2), K520 (g3), M60 (g4), V100 (p3/p3dn) and T4 (g4).

With its new P4d available today, AWS is paving the way for another bold decade of accelerated computing powered with the latest NVIDIA A100 Tensor Core GPU.

The P4d delivers AWS's highest performance, most cost-effective GPU-based platform for machine learning training and high-performance computing applications. They also provide exceptional inference performance.



In addition, the P4d instance is supported in many AWS services, including Amazon Elastic Container Services, Amazon Elastic Kubernetes Service, AWS ParallelCluster and Amazon SageMaker. P4d can also leverage all the optimized, containerized software available from NGC, including HPC applications, AI frameworks, pre-trained models, Helm charts and inference software like TensorRT and Triton Inference Server.

The first decade of GPU cloud computing has brought over 100 exaflops of AI compute to the market. With the arrival of the Amazon EC2 P4d instance powered by NVIDIA A100 GPUs, the next decade of GPU cloud computing is off to a great start. (Source: NVIDIA Newsroom)



MilAero007 Highlights



The Government Circuit: U.S. and European Lawmakers Eyeing Changes That Would Affect Our Industry ►

The seasons may be changing, but IPC's commitment to advocating for the electronics manufacturing industry remains constant as we look to position our industry for success in the coming year. Chris Mitchell shares some highlights of the top issues IPC is focused on this month.

Programs for Veterans: A Blackfox Update ►

At IPC APEX EXPO 2020, I spoke with Al Dill, president and CEO of Blackfox, about the Evolution Foundation, a nonprofit program to assist veterans with training and assistance into civilian tech jobs. Here, we get an update from Dill, Jahr Turchan, director of veteran services and advanced manufacturing programs, and Sharon Montana-Beard, VP and director of sales and operations, on Blackfox's programs for veterans.

STI Achieves AS9100D Certification ►

STI Electronics Inc.—a full-service organization, providing training services, training materials, analytical/failure analysis, prototyping, and contract PCB assembly—announced received AS9100D recertification for manufacturing/engineering services and initial certification for its Training Resources Division.

From The Hill: Pillars of Mil-Aero Technology and Revenue ►

The military-aerospace (mil-aero) electronics business is always in constant flux as new methodologies, like AI and space, create the know-how for new PWB designs. Mike Hill captures some of the most unusual old and new design ideas to support the notion that mil-aero revenue will continue to increase.

Understanding MIL-PRF-31032, Part 4 ►

Continuing with Part 4 of the discussion on understanding the military PCB performance standard MIL-PRF-31032, Anaya Vardya explains how the next step in the process is to create four new procedures to address the unique requirements of the military.

Defense Speak Interpreted: Rad-Hard Electronics ►

Have you ever seen electronics described as “rad-hard,” or radiation-hardened, and wondered what that meant and how that was done? Did you like me just assume that “rad-hard” and “expensive” were synonymous? Did you think that this was a Defense Department term since they deal with nuclear weapons? Denny Fritz explores this and more.

Mr. Laminate Tells All: Is Your Laminate and Prepreg Supplier Cheating? Only One Way to Find Out ►

According to Doug Sober, a huge void now exists in the base materials specifications for PCBs and PCB assemblies with the inactivation of MIL-S-13949 for base materials and the loss of the military's oversight function. IPC-4101 replaced the specification for MIL-S-13949, but there was no mechanism established for an oversight function.

Sabrewing Aircraft Receives \$600 Million Order for VTOL Aircraft ►

Sabrewing Aircraft Company has announced an exclusive representation agreement with Arabian Development & Marketing Co. (ADMC) headquartered in Riyadh, Saudi Arabia. The five-year renewable agreement includes exclusivity for Saudi Arabia, the GCC, and the Pan-African region.

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The New Recipe for Customer Service Success

Connect the Dots

by Matt Stevenson, SUNSTONE CIRCUITS

Hi, it's Matt from Sunstone. How are you holding up during the pandemic these days?

We are 100% committed to keeping our employees safe and doing well as a company, but each of us, like you, is dealing with life struggles and changes differently. We continue to concentrate on the current best practices for keeping our employees safe during this time: remote work for those employees that can, social distancing, regular cleaning and disinfecting, limiting our onsite visits to only necessary visits, and many more.

It brings me great joy to report that, so far, we have been very effective in maintaining employment and health for all our employees. With this in mind, I asked Al Secchi, global

customer support and sales manager, what he has learned professionally from the pandemic and how we can use this experience to provide even better customer service.

Matt Stevenson: Al, thank you for joining the conversation. What have you and the team learned from the coronavirus pandemic about how to serve our customers?

Al Secchi: Thank you, Matt. It is great to be able to talk about this and represent the many great thoughts of my team members.

This has been an epic year of unprecedented challenges. We rang in the New Year with a pandemic that showed just how fragile our global

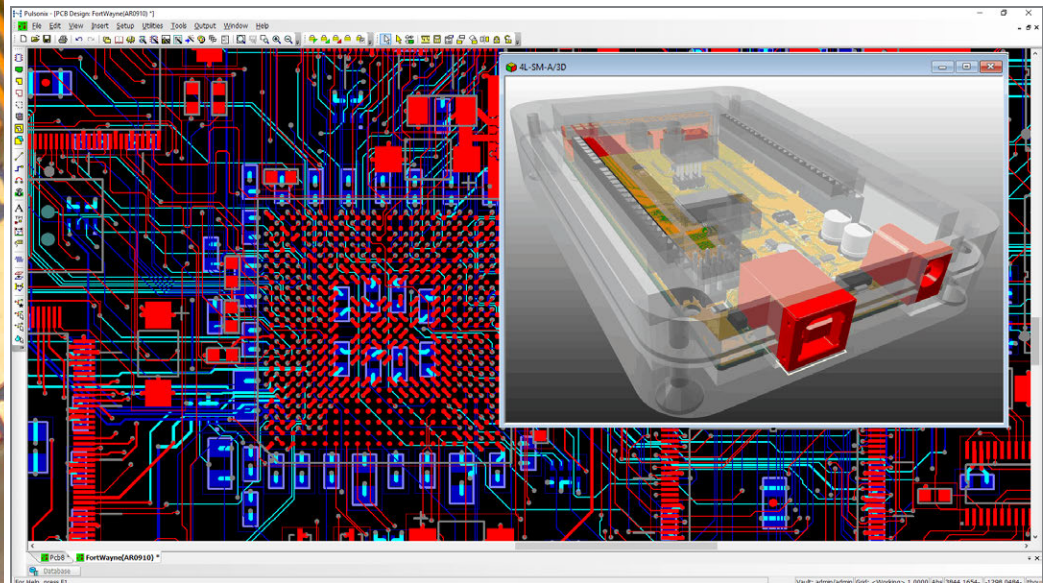


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Al Secchi

supply chains really are. As time went on, a new normal was created that redefined our industry, country, and the world. Businesses closed, jobs were lost, and essential workers were put into a new environment—one whose war cry centered on being “safe and healthy.” Those who were required to go into the office had to wear masks and have their temperatures taken at the start of and throughout their day; they also washed and disinfected continuously and maintained a safe six-foot distance from each other. Other employees—those who could—worked remotely.

With all these changes and unknowns created from the coronavirus, the critical part of creating a customer-centric work environment has been put at risk. Some businesses need to reduce work hours or cut staff; otherwise, they simply cannot deliver the product or service that they promise to their customers. This finds company buyers and consumers alike searching to find new reliable sources.

Without a reliable source, their businesses struggle to maintain production, and a domino effect further down the supply chain is in jeopardy of happening—no materials, no parts, no product, no sales, no revenue, and ultimately no jobs. Customer service people had their work cut out for them to be able to ensure ongoing business and provide reassurance and peace of mind to their existing customer base and new customer prospects.

What does customer service look like now? What does it need to look like to not only meet the needs of customers but also exceed them to the point of being memorable and creating loyal customer advocates? How do we create this exceptional level of service in today’s world in 2020?

Simply put, it takes a team, but not just any team. It needs to be a team of committed customer service professionals that understand both the challenges of the company they work for, as well as the needs and expectations of the customers they also work for. To support a customer and provide the highest level of service, you must first know what you can commit to and how best that commitment fits into the customer’s supply chain—both in product and delivery. After all, isn’t that what we all want when we are looking for a product or service—a company whose employees understand your needs and are willing to do whatever is possible to meet those needs?

With all that has happened in 2020, the one thing that can be a shining light is how a business focuses on its customers and helps them to be successful. Sure, everything may be a little different for you, but the customer’s need is still there, and it is the most important thing. Your customers are looking for a reliable partner that shows an understanding of their needs—one that gains their confidence and builds a level of trust that they can feel good about.

Along with this, you must use technology to provide them with an easy way of contacting you through multiple communication channels that they can choose from: phone, chat, email, or text. Every customer wants to be able to reach you easily and confidently and in a way that they are most comfortable with. They also want you to be proactive in contacting them with both the good news and the not so good news. The important thing is that you proactively reach out and be that honest, helpful partner they are looking for. Don’t make them have to contact you; you need to reach out to them in an honest, helpful, and timely way.

I tell my customer service team to consider themselves master chefs with customer ser-

vice as a menu option, and the main dish that everyone wants to be tasty and satisfying. The following would be a recipe to consider.

Start with a high-quality product or service that you believe in and can stand behind. Add an understanding of your customer—who they are, what they do, and what they need. Show that you understand them and their need and that you care! Then, if—and only if—you can meet that need, you share with them how you can help them to be successful. Only make realistic commitments that you can stand behind. Then, be timely in all your communications as you mix in a good portion of proactiveness and work as a good partner would. Now, combine, and add an unexpected positive—more than and faster than expected.

Your ingredients should include:

- 1 part of high-quality product/service
- 3 parts of understanding the customer's needs—show them you understand and that you care
- 2 parts of sharing how you can help the customer be successful
- 3 parts promises you can confidently commit to
- 2 parts timely and as proactive as possible communications
- 5 parts exceeding your customer's expectations

Mix these time tested critical ingredients with an easy multi-channel way of communicating with your customers that includes self-service FAQs where they can easily and quickly find answers to their questions—including the use of chat-bots that can provide answers based on keywords your customers enter. This will create an award-winning customer service dish.

Lastly, always remember that you can only be as successful as you can make your customers. Good luck in 2020, and be the best customer service master chef that you can be!

Stevenson: Thank you, Al. It is great that your team strives to keep customers' peace of mind and improve the experience. I agree that it takes a team, so a big shout-out to you and your team for their hard work. I love how each member thinks of themselves as a master chef, allowing them to cater and personalize the experience for each customer in each situation as it changes.

Secchi: Thanks, Matt. **DESIGN007**

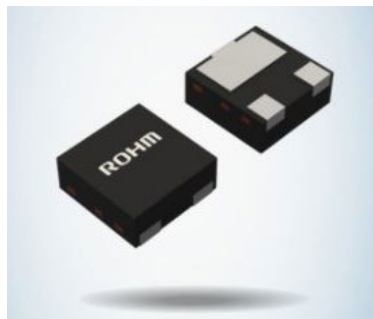


Matt Stevenson is the VP of sales and marketing at Sunstone Circuits. To read past columns or contact Stevenson, [click here](#).

Rohm Reducing Size of Automotive Designs With Ultra-Compact MOSFETs

Rohm has released the ultra-compact AEC-Q101 qualified MOSFETs, RV8C010UN, RV8L002SN and BSS84X, best-in-class 1mm² size that deliver automotive-grade reliability. The products are suitable for high-density applications such as ADAS and automotive ECUs.

The continuing electrification of vehicles in recent years has significantly increased the number of electronic and semiconductor components used per vehicle. For automotive parts, automated optical inspection (AOI) is performed after mounting to ensure reliability, but with bottom electrode



components the solder joint cannot be verified since the terminals are not visible, making it difficult to conduct visual inspection that meets automotive standards. Rohm has solved these issues with its original Wetable Flank technology that ensures an unprecedented side electrode height of 125µm in the 1.0mm x 1.0mm size and leading to increased adoption by a number of vehicle manufacturers.

In addition to MOSFETs, Rohm is committed to continuing to expand its product lineup of bipolar transistors and diodes. (Source: Globe Newswire)

PCEA and Industry Leaders Who Happen to Be Women

The Digital Layout

by Kelly Dack, CIT, CID+, PCEA

Introduction

In this month's column, I introduce a few of our inspiring PCEA leaders who happen to be women. Next, PCEA Chairman Stephen Chavez offers his take on the importance of diversity in a collective organization. As always, I'll include our list of professional development opportunities and events. Lastly, I'll tease some upcoming coverage we'll be doing on one of the PCEA's educational networking events.

PCEA Updates

One of the most inspiring events I've had the opportunity to cover over the past decade was an early morning Women in Electronics at IPC APEX EXPO. This event brings together women in the electronics industry to join their colleagues across the supply chain to network, share ideas, and discuss career experiences. It

is a unique trade show opportunity for women in the industry to learn from and inspire one another.

Recently, I've appreciated that within our PCEA meetings, we experience that same zeal with our executive staff every time we convene. It is not difficult to realize the impact of leadership by women in electronics in the PCEA. Many of our leaders—who happen to be women—reach out, team up, and work together to tackle many of the tough tasks which must be accomplished as the PCEA moves forward.

Tara Dunn, Susy Webb, and Eriko Yamato are well known in the electronics industry for service and leadership in their areas of expertise. They are subject-matter experts, and their experience spans high-tech electronic materials, flexible PCB manufacturing, emerging





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additive process technologies, and solid PCB design instruction. These women are a few of the many who dynamically serve their companies and customers each day and still find enough time and energy to contribute their leadership to the PCEA.

Here, I share their backgrounds, as well as their hopes for the PCEA.

Tara Dunn

Tara Dunn is a seasoned professional and an [I-Connect007 columnist](#) with more than 20 years in the electronics industry exclusively focused on the PCB sector. Her experience spans roles from manufacturing to sales and marketing.



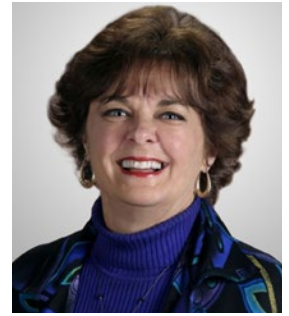
Tara is now president of Omni PCB, a manufacturers' rep firm, which is uniquely focused on the PCB market, offering sales and engineering support with technology ranging from standard technology to high-end HDI products. Specialties include flex, rigid-flex, RF microwave designs, and microelectronics. Her website (pcbadvisor.com) shares technical information related to all segments of the PCB industry.

Tara is also a founder of Geek-A-Palooza. This annual event provides all aspects of the local electronic industry with a unique networking experience focused on expanding resources and knowledge, building relationships, and bringing the industry together in a social atmosphere.

"My vision for the future of PCEA is to be all-inclusive, offering strong technical content, networking, and relationship building for designers, fabricators, and assemblers. My desire is for experienced PCB engineers to offer support to those new to the field, and for those who new to bring energy and new ideas in return. With a strong network, what this industry can accomplish is limitless, and PCEA provides tools and community to inspire."

Susy Webb

Susy Webb is a senior PCB designer with 40 years of experience. Her career includes experience in coastal and oceanographic oil exploration and monitoring equipment, point-to-point microwave network systems, and CPCI and ATX computer motherboards. Webb is a regular speaker at PCB West, IPC events, and international design conferences. She also consults for individual companies and groups. Her presentations discuss the practical implementation of complex engineering concepts into board layout and methods to improve the overall design and flow of PCBs.



Susy is CID-certified, a chapter contributor for The Printed Circuits Handbook, and one of the judges for the annual Mentor Technical Leadership Awards. She is also an active member of the PCEA Executive Board and education committees and is a member and past president of the Houston Chapter of the Designer's Council.

While working a full-time PCB engineering job, Susy constantly seeks to learn more about the physics, electronics, and DFM concepts that lead to better board design. She shares those concepts as a speaker/teacher at conferences and companies, and strives to show others the reasoning behind why things are best done a certain way. Susy also maintains an active involvement in the industry in the form of professional associations.

"The PCEA is an organization where engineering professionals can come together and discuss ideas and share experiences. There is an overwhelming amount of engineering information online. As a part of the education group, we seek to continually update the information on our web page about resources, articles, and books we have enjoyed to be sure that others know about them, and which we find most accurate and beneficial. In the coming year, we also hope to share some of our

own articles and be available to give presentations to local or web-based groups. We would also like to work up some training programs to help people who do not yet have a PCB background to design effective boards, and correct the first time boards.”

Eriko Yamato

Eriko is originally from Kobe, Japan, and spent five years in San Francisco during her childhood. After getting her B.S. in political science at Keio University in Tokyo, she worked at a TV station for five years, producing infotainment programs, sports news, and documentaries. In 2000, she returned to California to pursue her passion for documentary film production at Stanford University, where she received her M.A. in communication and discovered her other passion: marketing.

Eriko has 15+ years of experience in technical marketing of EMC, SI, PI, and RF/wireless products and is currently marketing and QTA manager at Oak-Mitsui Technologies headquartered in Frankfort, Kentucky. She has been active with the IEEE EMC Society since 2012 as an officer and currently serves as the treasurer for the IEEE EMC Society Atlanta Chapter. Eriko is also the marketing representative for the IEEE EMC Young Professionals Group. In her spare time, she enjoys traveling, cooking, wine tasting, CrossFit, and hiking.

“I was truly honored when Steph Chavez and Mike Creeden asked me to help out PCEA as the events committee chair. I have been involved with the IEEE EMC Society for several years, and I enjoy giving back to the electronics industry. The PCEA is such a great organization where you can connect with other industry professionals, share information, and educate and support each other. This year has not been the easiest for all of us, to say the least, and I hope to organize an in-person event in 2021 where we can all reconnect and re-energize. Through events, I would like to showcase



how resourceful PCEA is and encourage professionals to be part of this collaborative organization.”

Message From the Chairman by Stephen Chavez, MIT, CID+

Activity overload? Not for many, like those within the PCEA leadership team, who tend to shift it into a higher gear and thrive in this last quarter of the year, as they do year after year. There is no doubt that



PCEA activities continue with great success. As I review how the PCEA started, including where we are today and how we are coming along, it's awesome to see that we are evolving beyond expectations.

At the core of this success is the engine that keeps PCEA moving forward—the core leadership team comprised of talented, passionate, experienced, and selfless individuals. One of the many things I love about this team is it's a diverse group of special individuals and includes some awesome women who are vital parts of the PCEA leadership engine.

The PCEA strongly believes in and supports diversity. We see it, realize the strength in and importance of it, and encourage it. And when I refer to diversity within PCEA, I mean the women who are part of this PCEA engine. In no particular order, Susy Webb, Cherie Litson, Judy Warner, Tara Dunn, Terri Kleekamp, and Eriko Yamato are a force to be reckoned with. I am honored to work alongside each and every one of them. They are more than industry colleagues; they are close friends.

What these women do in their day jobs is great on its own, but what they do for and bring to our industry is where they truly shine. We are blessed to have such professional women of their caliber in our industry and the PCEA. Each of them leads the pack, and they are great examples of professional women for the younger generation to follow.

As always, refer to our column and the PCEA website to stay up to date with upcoming

ing industry events. There are many free webinars offered out there, so take advantage of them. And if you have not yet joined the PCEA collective, I highly encourage you to visit our website at pce-a.org and become a member.

I continue to wish everyone and their families to be healthy and to be safe.

Next Month

By the time you are reading this, the San Diego and Arizona chapters of the PCEA will have co-hosted their first chapter meeting, which took place on October 28 and featured Insulectro speakers Mike Creeden and Chris Hunrath, who spoke on the following scintillating PCB materials topics:

- Design innovation
- Hybrid stackup models
- Material properties and considerations
- Effects of loss tangent
- Mixing laminates
- Embedded capacitance
- Advanced HDI structures

I'll be sure to check in with our chapter presidents and attendees for their thoughts on this event.

Upcoming Events

- March 6–11, 2021: **IPC APEX EXPO** (San Diego, California)
- April 13–15, 2021: **DesignCon** (San Jose, California)

- May 11–13, 2021: **IPC High-Reliability Forum 2021** (Baltimore, Maryland)
- November 10, 2021: **PCB Carolina** (Raleigh, North Carolina)

Spread the word. If you have a significant electronics industry event that you would like to announce, please send me the details at kelly.dack.pcea@gmail.com, and we will consider adding it to the list.

Conclusion

There are so many interesting printed circuit engineering folks out there who we can learn from, and we will focus on the most interesting people in the PCEA from time to time. As a collective, we want to expand our diverse membership and foster healthy connections among people in printed circuit engineering. We believe that this will be a fulcrum that will help our members become inspired to connect and collaborate, and it will open doors to educate and positively contribute to the wider electronics industry.

See you next month or sooner! **DESIGN007**



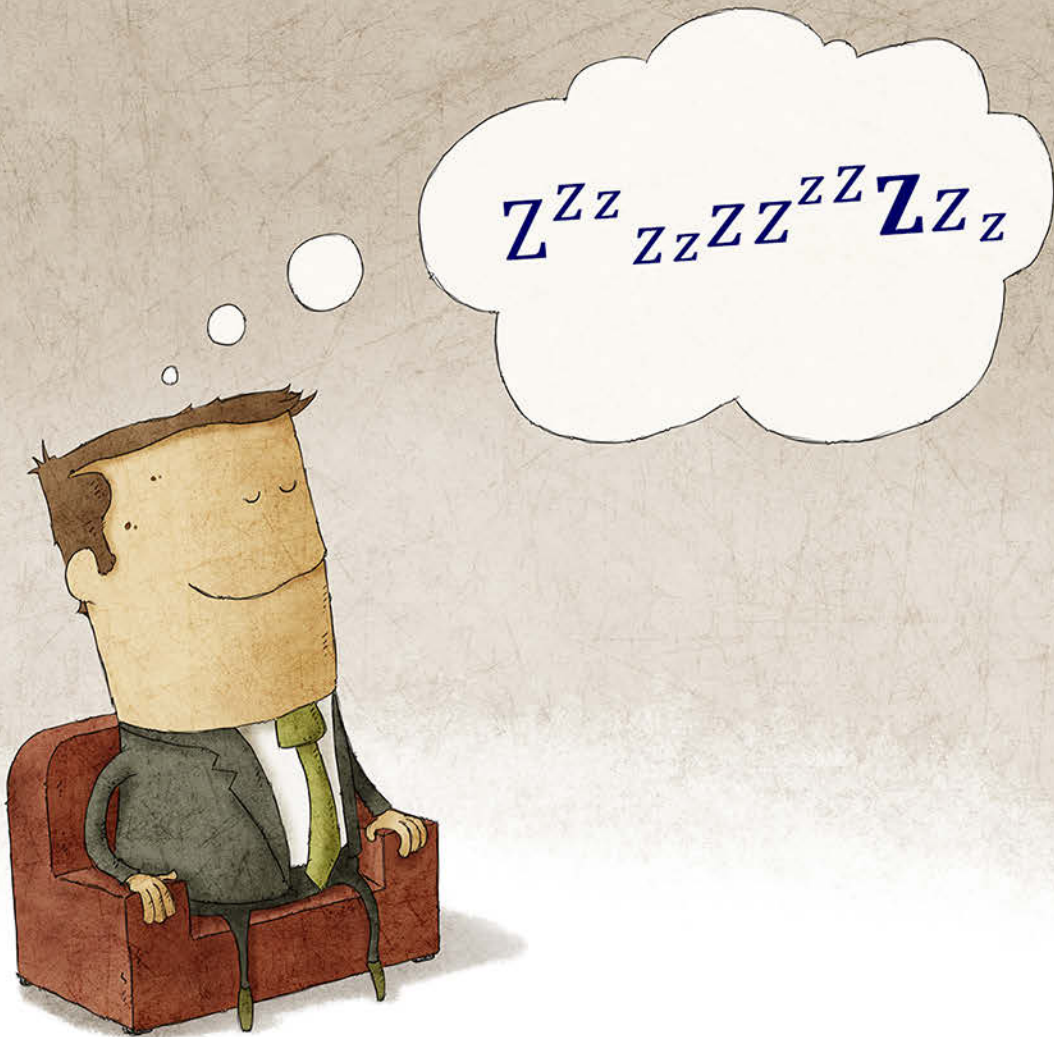
Kelly Dack, CIT, CID+, is the communication officer for the Printed Circuit Engineering Association (PCEA). To read past columns or contact Dack, [click here](#).

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Failures of Imagination: A Column of Caution

Design Circuit

by Patrick Crawford, IPC—ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES

Regarding board design, IPC has been busy. IPC-2581 (Generic Requirements for Printed Board Assembly Products Manufacturing Description Data and Transfer Methodology)—often referred to as DPMX—is currently being updated to the C revision. At the time of this writing, it is undergoing the final typesetting necessary for publication. IPC-2231 (DFX Guidelines) is also receiving an upgrade with an A revision that is currently entering into the final draft for industry review.

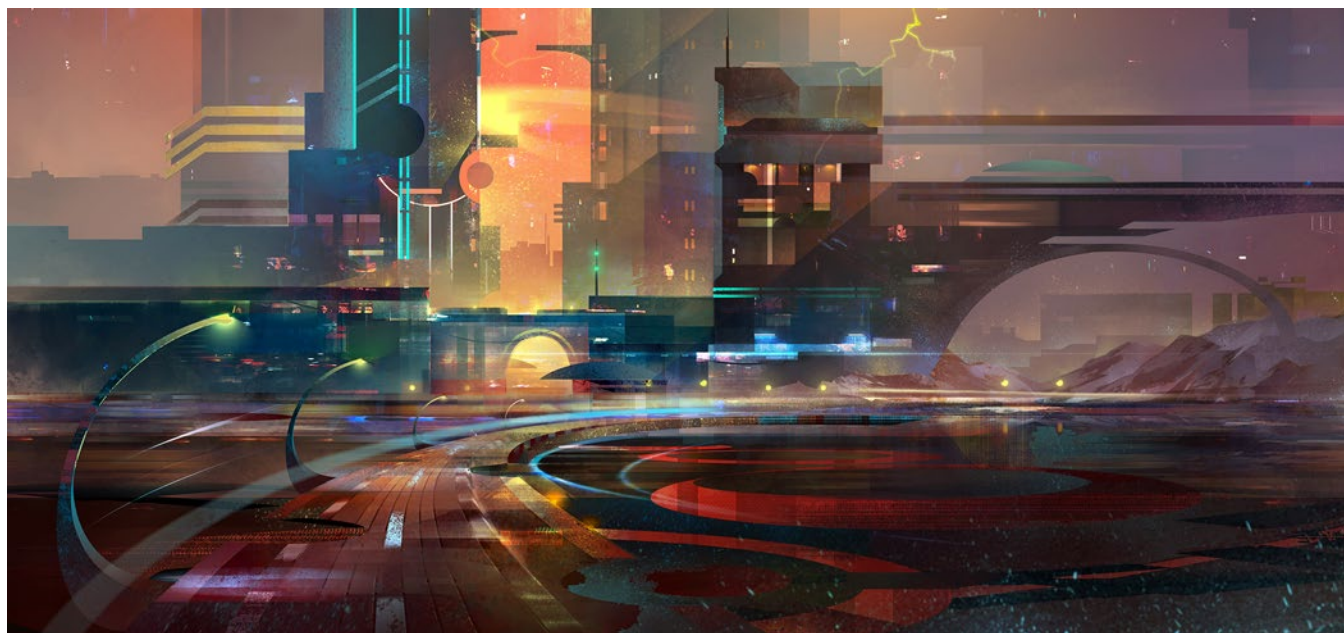
And finally, we have listened to your constructive criticism regarding IPC Design and how it can better serve the printed board design community. We are revamping it to be more lightweight and user friendly. We will be unveiling the new IPC Design model before the end of November.

These developments are exciting, and they will each get their own column in the coming

months. However, for this month, I wanted to step back from IPC and the advancement of its printed board design offerings and instead focus on the advancement of electronics and technology in general. Hopefully, I can offer some nuggets of insight, inspiration, or at least a fleeting thought of, “Oh, that’s kind of cool.”

In 1962, the late Sir Arthur C. Clarke penned and published *Hazards of Prophecy*—an essay that is now considered to be one of the foundational texts of 20th-century futurism. As its name suggests, *Hazards of Prophecy* describes how past “prophets” of science and industry failed to predict their immediate future as it related to advances in technology. Clarke delineates these failures into two kinds: a failure of nerve and a failure of imagination.

As Clarke defines it, a failure of nerve “occurs when even given all the relevant facts, the would-be prophet cannot see that they point



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to an inescapable conclusion.” These individuals see the writing on the wall, so to speak, and still do not change their views or challenge their own assumptions.

Clarke recalls the writings of the prominent 20th-century American astronomer, Simon Newcomb, who declared that heavier-than-air flight was utterly impossible. To arrive at his conclusion, Newcomb performed mathematics using the model of a flat board suspended in air and powered by a steam engine. Newcomb’s paper was published in October 1903 and received high praise from the scientific community.

As Clarke defines it, a failure of nerve “occurs when even given all the relevant facts, the would-be prophet cannot see that they point to an inescapable conclusion.”

In December 1903, the Wright Brothers achieved the first reported heavier-than-air flight of their prototype aircraft at Kitty Hawk. Unlike Newcomb’s thought experiment, the prototype aircraft utilized complex airfoil geometry and an internal combustion engine. While Newcomb’s mathematics were sound, his inability to be open-minded and embrace contemporary technologies inhibited him from making correct predictions of the impending state of the art.

Failures of nerve happen within the bounds of known science and engineering. Failures of imagination, on the other hand, occur outside of those bounds. Clarke defines these failures as arising “when all the available facts are appreciated and marshaled correctly—but when the really vital facts are still undiscovered, and the possibility of their existence is not admitted.” These failures occur because you don’t know what you don’t know.

Clarke gives another excellent example. Referring to stars, the 18th-century philosopher Auguste Comte wrote that “we can see how we may determine their forms, their distances, their bulk, their motions, but we can never know anything of their chemical mineralogical structure; and much less, that of organized beings living on their surfaces.”

Of course, reading that quote in 2020, we can simply Google “spectra of main-sequence stars” or even “NASA exoplanet archive” to learn all that is known about the chemical structure of stars; and if not the organized beings themselves, then at least their potential habitats. This is really an existential issue, and Comte’s failure is one that we may well be struggling through as an industry right now—and we wouldn’t even know it.

As a moonshot example, in current materials physics, the highest operational transition temperature observed for an intact superconductor has been approximately 250°K for pressurized lanthanum decahydride (LaH₁₀). While this transition temperature is within reach of systems operating in permanent installations that have access to even somewhat-robust cooling and pressurization systems, it is a far cry from what would be needed to work effectively as an everyday conductor replacement in consumer electronics. (Yes, I realize that there are plenty of areas where we want latency, but please, for the sake of the example!) If you ask any materials engineer or solid-state physicist whether we will have true room-temperature superconducting materials within their lifetime, if at all, they will scramble to hand you a *BCS Theory for Dummies* before laughing themselves unconscious.

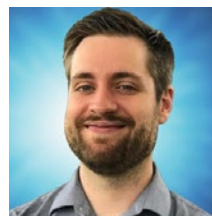
But then again, what if tomorrow, a university lab churns out the right topology of graphene that allows for room-temperature superconductivity? What if this is easily reproducible in commercial and academic labs the world over? The overtime at the patent office will be great for its employees, and those scientists and physicists who laughed themselves unconscious will quickly sober up before reveling in the new discovery and designing experiments of their own.

At this point, you might be wondering why you should care. A science-fiction author from the mid-1900s wrote about failure. That's great, but what does that mean for you?

Clarke's work cautions against prophesizing; however, I believe that the failures he described are rampant and occur around the world in every industry, every day. As a modern board design engineer—and within the limits of your job description and responsibilities—you have a high stake in the design process. Therefore, you can communicate with your superiors and your colleagues about the challenges you face and, most importantly, the solutions that you propose to overcome them.

When faced with these challenges, do not be like Simon Newcomb and engage in a failure of nerve. Seek out and explore the exist-

ing and most up-to-date knowledge available to you, your department, your company, or the industry in general. Advocate for and implement creative solutions for those challenges. If you wake and find that a technique or methodology you have been using for your entire career has been supplanted by something new, then do not let your failure of imagination get the best of you and become a failure of nerve. Learn, get caught up, and continue to advocate for the excellence of your designs. **DESIGN007**



Patrick Crawford is the manager of design programs and related industry programs at IPC. To read past columns or contact him, [click here](#) or email PatrickCrawford@ipc.org.

Volvo Cars Now Designing, Developing Electric Motors In-House

Volvo Cars is making significant investments that allow for the in-house design and development of electric motors for the next generation of Volvo models, as the company continues to move towards becoming a fully electric car maker.

The company opened a brand-new electric motor lab in Shanghai, China, the latest addition to its global network of facilities for the development and testing of electric car components. The lab comes in addition to ongoing e-motor development in Gothenburg, Sweden and state-of-the-art battery labs in China and Sweden.

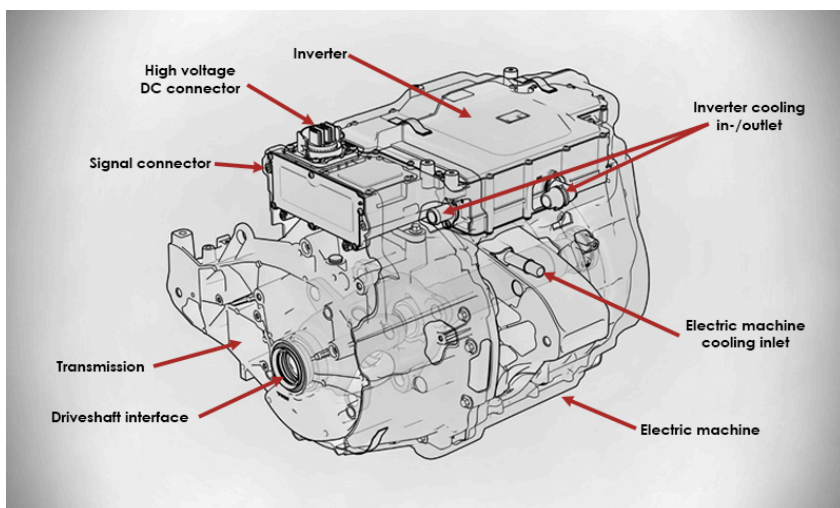
Bringing the development of electric motors in-house will allow Volvo Cars engineers to further optimise electric motors and the entire electric driveline in new Volvos. This approach will allow engineers to make further gains in terms of energy efficiency and overall performance.

"Through in-house design and development, we can fine-tune our e-motors to ever better levels," said Henrik Green, chief technology officer at Volvo Cars. "By constantly improving their overall performance levels in terms of energy efficiency and comfort, we create an electric driving experience that is unique to Volvo."

E-motors enable hallmark features that electric cars are known for, such as instant acceleration and so-called One Pedal Driving, whereby drivers use the gas pedal both for acceleration and deceleration, depending on whether they push in or lift their foot off the pedal.

The newly opened electric motor lab in Shanghai became operational last month. It will mainly focus on electric motor development for use in fully electric and hybrid cars based on Volvo Cars' forthcoming SPA 2 modular vehicle architecture.

(Source: Volvo Cars)



A Brief History of Electrical Vias in PCBs

Flexible Thinking

by Joe Fjelstad, VERDANT ELECTRONICS

Printed circuits have been in use in the manufacturing of electronic products for roughly 80 years. Early circuits were simple and often only required a single layer of circuits. The circuit patterns were typically screen printed or stenciled using conductive inks—hence the name “printed circuit” was quite apropos. And for those who have been paying attention to technological trends, the printing of connective inks to make circuit patterns has seen a surge of recent interest in use to make a variation of flexible circuits that market makers have labeled flex hybrid electronics (FHE).

Thin copper foils were soon after applied to insulating laminates, and printing was again used to print the circuit pattern, only this time as an etch resist to protect the desired circuit pattern when subjected to an etchant. Holes were commonly drilled into the copper foil and

substrate, where a connection to electronic component leads was desired, and solder was used to interconnect them. As electronics increased in complexity, a second layer of copper was laminated to the back side of the insulating material. And where an interconnection between the top and bottom circuits was required, wires—often referred to as Z wires (Figure 1) —were pushed through those holes and the ends soldered to opposite sides. This was arguably the first form of PCB via.

Enterprising and attentive engineers saw the potential of making such side-to-side interconnection by using the equivalent of metal shoe eyelets, and a second-generation alternative was introduced. Not long after, other engineers, seeing the limitations of one by one via formation, realized the potential benefit of using plating to make interconnection through

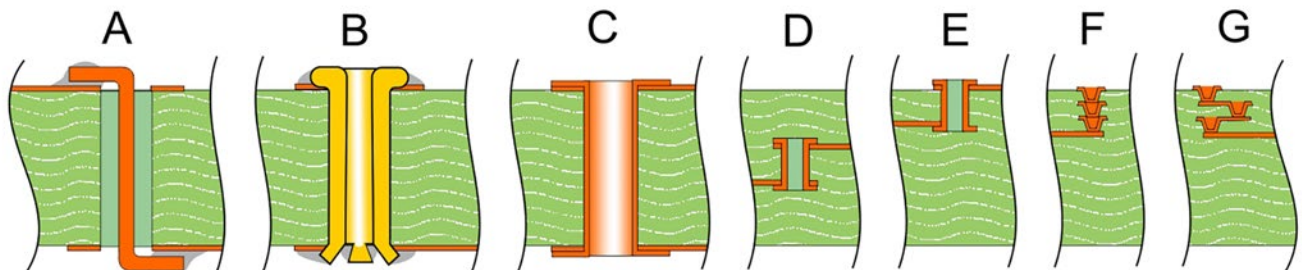


Figure 1: Via types, including (A) Z-wire, (B) rivet, (C) plated via, (D) buried via, (E) blind via, (F) stacked via, and (G) staggered via.



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all the holes in the laminate at one time. That was in the 1950s, and it is still the basic technology used today for through-holes and vias.

Increases in performance demand improved and standardized components in the late 1960s and 1970s, such as the dual in-line package (DIP), along with increased circuit complexity, led to the development of multilayer PCBs. And vias were used not only to make the connection from side to side to connect the DIPs and other discrete components but also to interconnect circuit runs routed through the inner layers of the multilayer board along with making the connection to internal power and ground planes.

Connection to the thin ring of copper exposed on the wall of the drilled hole was again made by electroless and electrolytic copper plating. It served not only to make connections to component leads but to increasingly important vias. Because vias did not need to hold a component lead, they could be made smaller. This helped to reduce the board space required as well while improving performance. However, it was becoming increasingly evident that leaded components not only required greater space as I/O counts increased, but the larger size limited the effective performance of the electronic device.

This ushered in the era of surface-mount technology in the 1980s, where component leads were first placed on the edges of the component body and mounted on the surface of the PCB. The newer components were temporarily attached by means of a solder paste stenciled to the land pattern and subsequently soldered to the matching land pattern using a high-temperature reflow oven to affix them permanently. SMT components and technology allowed for a significant reduction in the size of electronics while allowing an increase in the lead count due to the finer pitch of the component's leads. SMT largely made possible the era of portable electronics, which holds true to this day. It also drove advances in via design and manufacture but also caused concern about the reliability of the solder joints and plated interconnections due to the heat of the soldering process.

To deal with the increase in circuit interconnections required, manufacturers began to increasingly use vias, which interconnected to one or more internal layers, as well as internal or buried vias, which were created in the circuit layers before the lamination process to make a multilayer board. At the same time, there was a possibility to make both blind and “semi-buried/semi-blind” vias, which extended from the surface to a subsurface layer but not all the way through. Mechanical drilling was still the most common way to make the via hole at this time, but lasers were poised to take over the task as they were and are much better suited to making very small holes, and they dominate the process to this day.

The early 1990s saw the arrival of area array components in both larger BGA and much smaller CSP formats. They were developed to accommodate the increasing demand for I/O while holding the line on the size of the PCB for cost and performance reasons. This development precipitated a big increase in via technology and the introduction of new ways of creating them, including buried bump interconnection technology (BBIT) developed by Toshiba and any layer interstitial via hole (ALIVH) developed by Panasonic (Figure 2).

These technologies require a license and thus have not enjoyed the breadth of use of more traditional and generic plated via technologies. Both of these novel techniques involved the use of the conductive paste to make the via connection from layer to layer. The BBIT (also called B2IT) process was unique in that it involved sequential stenciling of conductive paste in the form of a pattern of cones, which pierced the bond ply used to join circuit layers during lamination.

With an ever-increasing I/O count and reduced contact pitch, micro vias (nominally less than 75 μm in diameter) have been increasingly called upon to mitigate the wiring congestion in today's most advanced designs. Over time, the microvias are often being stacked sequentially in a buildup process. This approach has been called to question from a reliability perspective; an alternative where

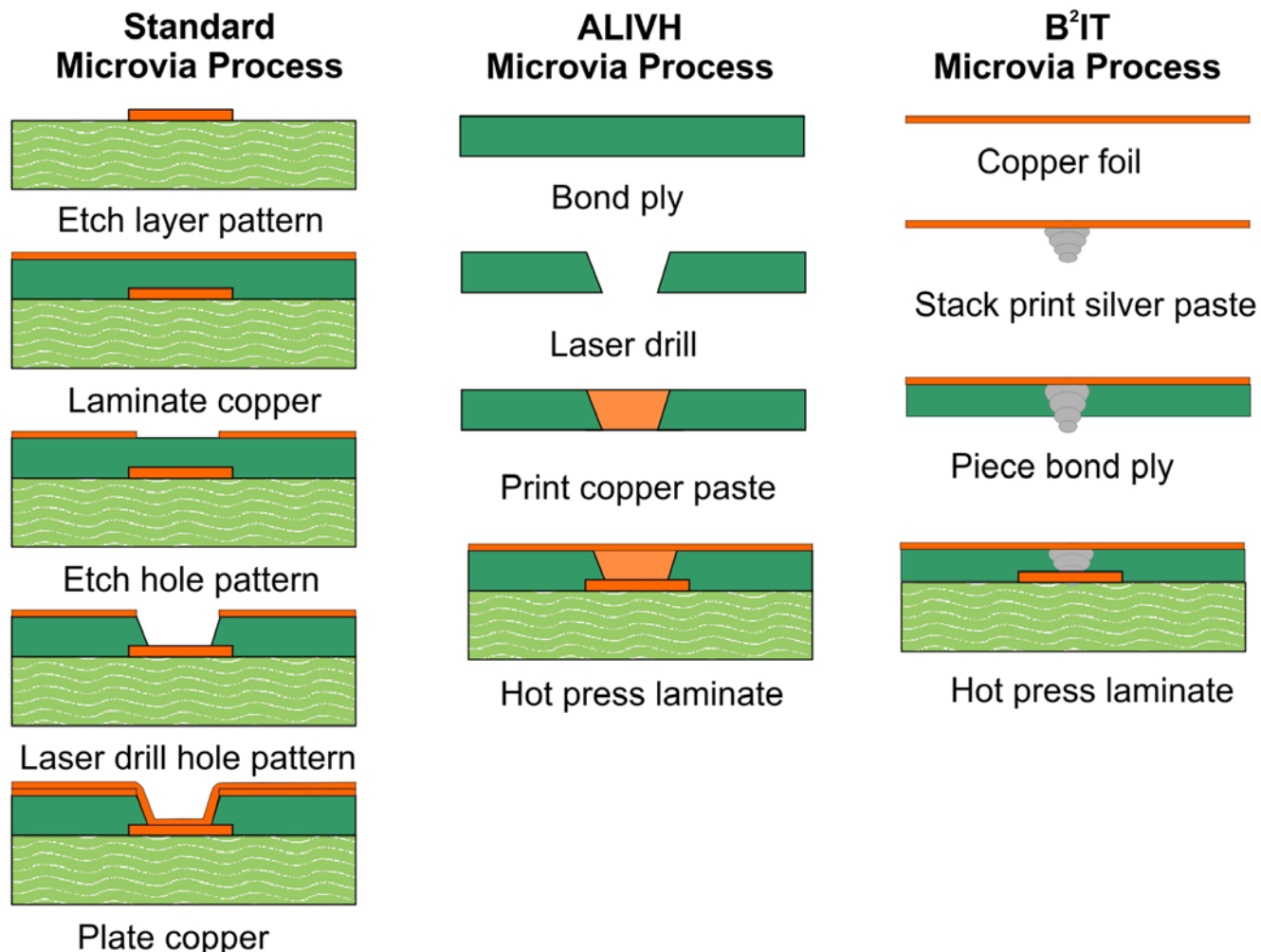


Figure 2: An abbreviated comparison of frequently used proprietary microvia processes with that of traditional microvia processing.

vias are staggered is being viewed by some as a more reliable way of constructing such designs (Figure 1G). Regardless of the design approach, all have been enabled by continuous advances in hole formation and copper plating chemistries/technologies—the former by steady improvement in lasers of every sort used for drilling microvias.

To complete the discussion, it might be worth mentioning interesting variations on the practice. One was (and is) the via-in-trace concept, which was demonstrated in the early 1980s. There was (and is) also the possibility to make vias using a photoimaging process, which could potentially greatly reduce manufacturing complexity and increase productivity. These things are mentioned because technical approaches that were once thought long dead

have a way of reentering the picture when conditions are right.

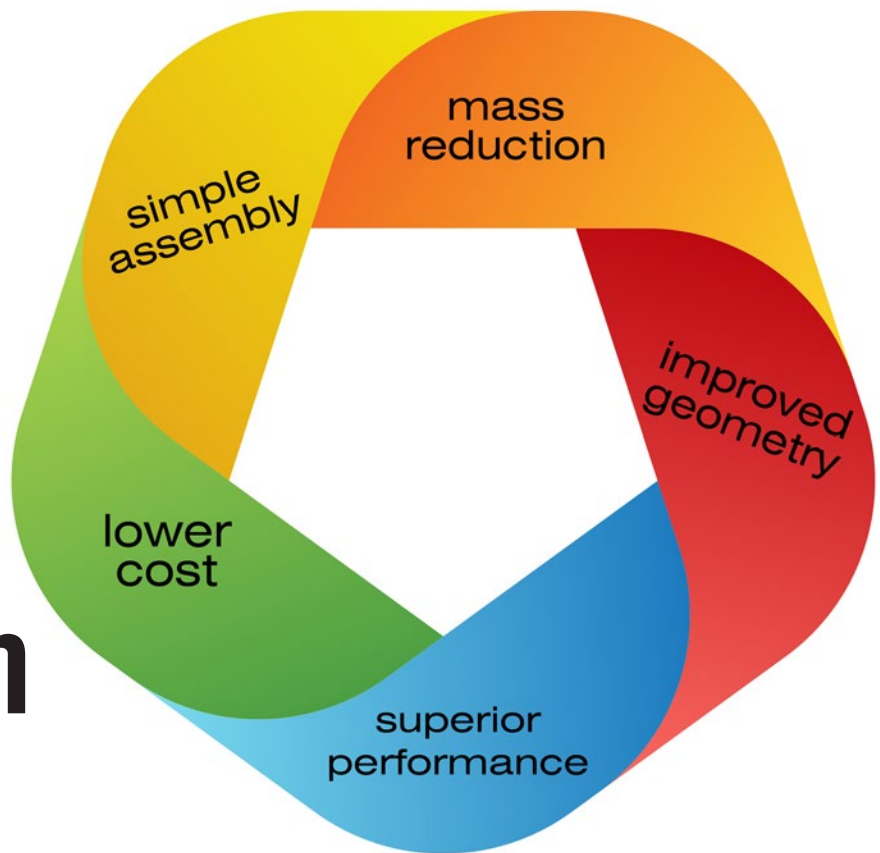
This brief review has hopefully provided those unfamiliar with the history some appreciation of how we got to where we are in circuit via technology and why, as well as where we might go next. **FLEX007**



Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185 patents issued or pending. To read past columns or contact Fjelstad, [click here](#). Download your free copy of Fjelstad's book *Flexible Circuit Technology, 4th Edition*, and watch his in-depth workshop series "[Flexible Circuit Technology](#)."

Five Ways Rigid-Flex Is Driving Global Innovation

Flex007 Feature by Chris Clark
MINCO



Every now and then, advances in technology come along that dramatically improve the way entire industries are able to address key challenges.

In healthcare, IoT-enabled devices continue to make waves. IoT components—like innovative sensors that can track heart rhythm, body temperature, and many other physiological signals—are delivering accurate, real-time measurements at the bedside to help doctors and nurses monitor key health data with greater ease than ever before. With similar advances in data accessibility, hospital executives can respond quickly to changes within their systems while also navigating fluctuating and external pressures like staffing shortages and labor costs.

In aerospace, new emerging part manufacturing processes are empowering manufacturers to imagine and design lightweight, customized parts. These innovative practices are driving down aircraft weights and reducing the burden of the traditional cost of ownership factors such as fuel and machine downtime.

While IoT and manufacturing advances rightfully receive their due for these performance and cost-saving innovations, each requires key technology components at their foundation. For example, the printed circuit board (PCB) manufacturing industry—no doubt a contributor in many IoT-enabled systems—has seen the rapid adoption of rigid-flex technology in recent years. Alongside trends in IoT and manufacturing, engineers across industries are integrating rigid-flex into their designs to save space, increase durability, and reduce production costs—a sought after trinity of benefits. In fact, according to one recent market report ^[1], industry forecasters anticipate a compound annual growth rate (CAGR) of 9.8% over the next five years in the rigid-flex PCB category—rising to an estimated \$7.53 billion by 2025.

When we look a little deeper, it's easy to see why this is the case. As industries drive for more sophistication and improved total cost of ownership, rigid-flex is uniquely positioned to give engineering teams and manufacturers the best possible chance of building components

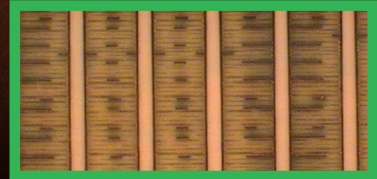
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BY TAIYO

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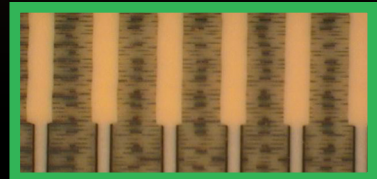
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THP-100 DX1 VF (HV)

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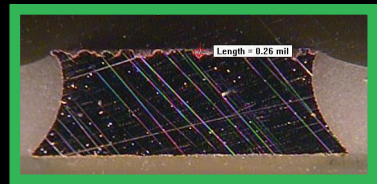
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that meet these lofty objectives. Here's a list of five key benefits rigid-flex offers when compared to traditional PCB offerings.

Five Building Blocks for Design Innovation With Rigid-Flex

1. Simple Assembly

This advantage is clear just by looking at a rigid-flex rig compared to the bulky wire harness designs of old. Traditionally, an engineer might have used a combination of hard board and wire harnesses to integrate the desired circuit capabilities into a system or device. With rigid-flex, engineers can replace these two components with one—reducing the need for complicated connections between hard board and wire harnesses. From an assembly perspective, rigid-flex circuits eliminate color coding and bundles of wrapped wire. Additionally, fewer parts and reduced assembly specifications mean fewer opportunities for assembly error, which can improve production efficiency and reduce manufacturing costs—especially with volume production.

2. Significant Mass Reduction

As manufacturers seek more compact components that reduce weight and enhance design flexibility, they are moving away from large, bulky hard board and wire harness packages. Rigid-flex designs have become a simple fix for this problem. In many cases, the flex portion of a rigid-flex circuit can save up to 75% of the space and weight of conventional wire harnesses—and replace multiple hard boards, cables, and connectors. In many industries, such as aerospace or other engine-powered applications, these weight reductions can deliver measurable improvements in performance and reliability.

3. Improved Packaging Geometry

Rigid-flex circuits strike the perfect balance between hard board and flex componentry. Flex areas allow engineers to create a fully customized package, capable of fitting in spaces where no other circuit designs can. They also retain a

flex circuit's ability to deliver repeatable routing and precise control over dense circuitry. Meanwhile, rigid areas provide hard-mount points on both sides of the circuit to connect to additional components in secure ways that maximize performance and package size.

4. Superior Mechanical and Electrical Performance

From a mechanical perspective, reduced circuit weight delivers added benefits in the form of greater shock and vibration resistance. Due to the low mass and superior ductility of rigid-flex, repeated impact and shock events—especially at high speeds—do not carry significant potential for component damage. By contrast, conventionally wired components deliver greater vibrational mass, which can increase stress on both the wires themselves and their related connections during impacts.

As for electrical performance, dielectric polyimide layers in the flex regions protect circuits beyond solder mask coverings found in other PCB configurations. Rigid-flex's highly predictable electrical characteristics improve signal integrity and meet high standards for impedance.

5. Lower Total Cost of Ownership

The cost benefits of using a rigid-flex solution can be found as early as assembly. Partnering with an experienced rigid-flex provider during the design process can help unlock assembly efficiencies that reduce production time and limit the potential for routine assembly errors. Over the life of the device, robust materials and their vibration resistant characteristics can help keep systems running at optimal performance for longer. These savings, in addition to potential fuel cost savings and performance advantages created by a low weight design, can combine to make investing in rigid-flex technology a no-brainer.

Selecting a Rigid-Flex Partner

Integrating powerful rigid-flex capabilities into your next design starts now. When you collaborate with an experienced flex circuit

provider early in the design process, often-times, they can help your engineering team bring new ideas to the table—pushing beyond existing performance standards to find a better way. The greatest performance improvements, space reductions, cost savings, and new capabilities are a direct result of integration ideas introduced and tested early on. To help identify the right rigid-flex specifications for your application needs, flex circuit experts lean on decades of proven experience helping engineering teams uncover more efficient designs across a wide variety of industries, including healthcare, aerospace, defense/military, and more.

In the coming years, TCO-driven strategies will continue to gain steam—joining perfor-

mance and efficiency objectives atop the list of key considerations procurement teams will identify in their decision-making process. Moving forward, designing innovative systems that can deliver on all three of these goals will be a central part of a winning strategy. **FLEX007**



Reference

1. Research and Markets, "Rigid-Flex PCB Market: Forecast (2020-2025)," March 2020.

Chris Clark is a product marketing manager at Minco.

Notion Systems, PV Nano Cell Partner in Digital Printed Electronics

Notion Systems GmbH, a leading manufacturer of industrial inkjet systems for functional materials and PV Nano Cell Ltd., an innovative provider of inkjet-based conductive digital printing solutions and producer of conductive digital inks, announced that a non-exclusive agreement was signed between the companies.

The two companies are world-leaders in their respected domains and plan to jointly go-to-market strategy to offer complete solutions including inks, printers and the printing process to be implemented in digital additive manufacturing of printed electronics. This approach is aimed at

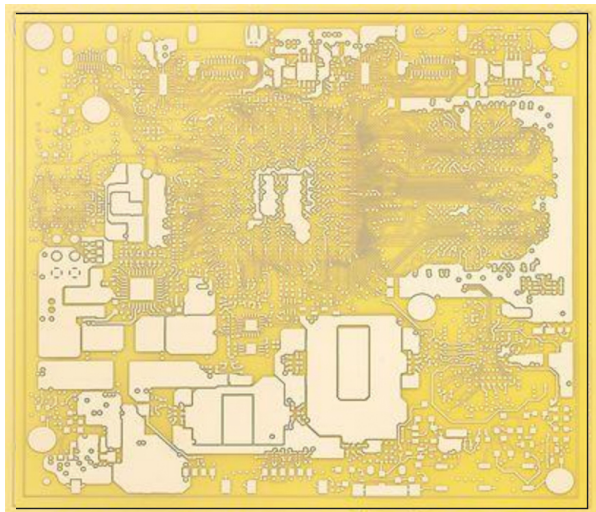
simplifying and accelerating the adoption of digital printed electronics by mass-producers.

One of the primary challenges of any printing solution is the development of its printing process that integrates the chemistry of the ink, printer parameters and the customers' design requirements. In order to overcome this challenge, the companies will work together and exchange information to optimize both the overall performance of printing and its time-to-market. The companies have been working together for years and are partners in the most prestigious European Funded projects such as the eurostars inkjetPCB that focuses on inkjet-based fabrication of multilayer printed circuit boards with embedded printed passive elements.

Another new funded project the two companies are working on with other partners is Project Tinker that focuses on providing a new cost and resource-efficient pathway for RADAR and LIDAR sensor package fabrication with high throughput up to 250 units/min.

"The new partnership will bundle forces and provide a one stop solution for customers," said Notion Systems CEO Dr. Michael Doran. "The inkjet electronics platform is already fine-tuned to work very well with PV Nano Cell's materials and provides the highest yields and outputs."

(Source: Globe Newswire)



Future Flex Circuits as Robot Skin Sensors

Consider This

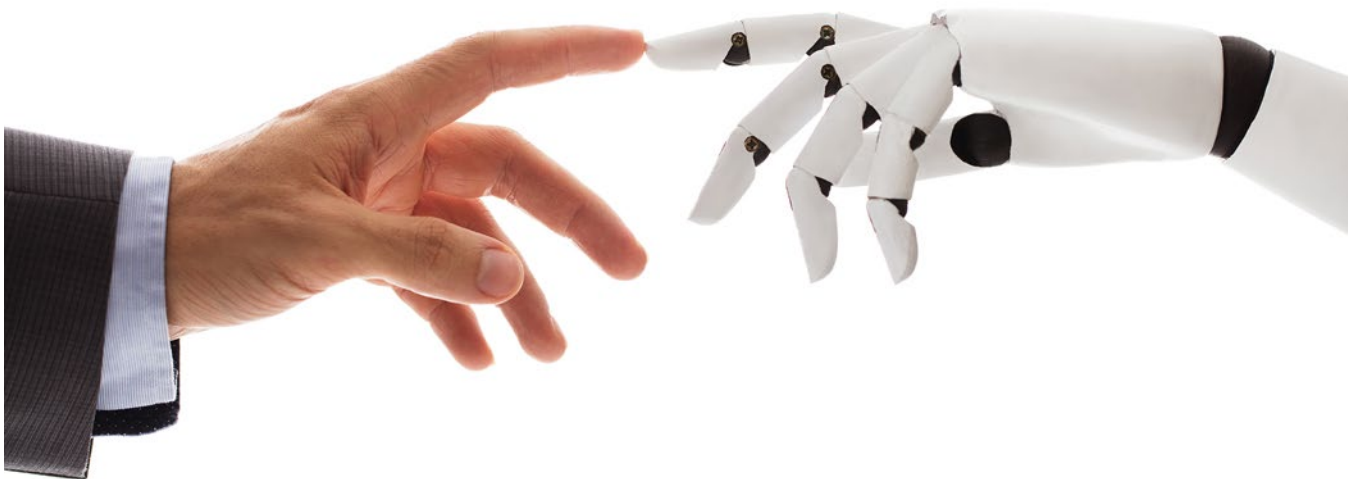
by John Talbot, TRAMONTO CIRCUITS

In today's ever-increasing robotic world, future robots will need more human features to properly integrate comfortably into our society, especially if they are to have direct skin to skin contact with humans. With the added power of artificial intelligence (AI), robots will be able to increasingly perform more human-like functions. One example of improved sensory applications is the fingertips on a robotic hand. Through touch, the hand requires it to sense temperature, pressure, pain, and even air flow for proper human-like operation. Inventive applications of flex circuits and simple sensors integrated with robotic skin like silicon can emulate a human's highly sensory fingertips.

To sense touch, we can use a resistive layer and connections to a microprocessor, which would be similar to a touchpad on your laptop. The resistor touchpad would allow the

computer to know the position of the touch, as well as pressure sensing. The resistive layer could be printed on a flex layer with a skin-like latex, protective outer surface. Pressure would change the resistance, telling the AI smart robot to squeeze lighter or heavier. Alternatively, they can use capacitance, like the touch-key screen on your computer, to sense the position of touch on their fingers, as well as pressure.

To sense temperature, we can silk screen or implant resistive or chip temperature sensors on the flex layers connected to a microprocessor to measure finger temperature due to resistive or pulse output changes. A layer of thermally conductive skin material could transport the heat inward quickly. The microprocessor would compare the resistive reading to a look-up scaling chart and quickly generate an accurate temperature reading.





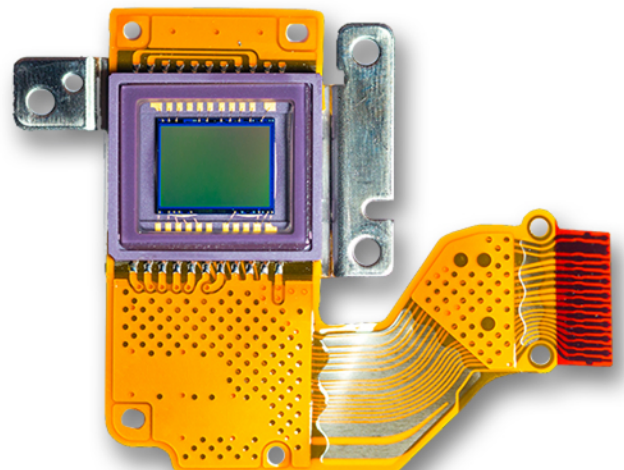
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When the fingers of our robot touch something hot, our robot can assess if they are holding something too hot for the silicon skin. At that point, the robot can decide to suffer finger damage if needed to save a human life or protect property, unlike humans, who instinctively jump back quickly and drop the hot object. For example, if the robot is working in the lab, picks up a hot beaker of sulfuric acid, and senses that it is so hot it will damage its silicon skin layer, rather than drop the acid and possibly hurt humans or do damage to property, the robot can simply place the hot object back and walk over to the repair shop for new finger sensory pads.

To sense pressure, the flex circuit can have carbonized rubber pads attached to gold pads between the flex layers, or small integrated chip pressure sensors. As the finger pads press on an object, the resistance of the carbonized rubber will decrease, or the chip will send a signal regarding the pressure applied. As the softer carbonized rubber pressure sensors compress flat with increasingly more pressure, a series of harder, durometer rubber pads will continue to react to stronger pressures such as the difference between your robot picking up an egg or your bowling ball.

The AI computer would look at the object it needs to pick up, judge the size and weight, and adjust finger pressure accordingly. Known as tactile feedback, the robot can control pressure on their fingers, knowing which object they are to pick up, the fragile egg versus a hard, heavy bowling ball. The flex circuits can have capacitor sensors, which would offer an advantage over humans in that it could sense how close the fingertips are to an object by measuring capacitance change.

For pain or damage sensors, a series of fine 0.5-mil copper tracks on the outer layer flex circuit or embedded in the skin coating would open if the finger pad is severely damaged. The tracks would be covered with a thin, soft silicon or latex rubber to act as skin. The pain or damage tracks could be shaped similar to your fingerprints. The height of the copper or some other metal pain tracks would cause the silicon to follow the pain-sensing tracks and protrude

with a similar shape, allowing for robot identification. Should your robot run amuck and rob an electronics parts store for a snack, it will leave its fingerprints all over the store.

To make the robot feel more human to us, and if they are required to touch you, the robot's skin should be around 95°F. A series of screen-printed carbon resistors placed on one of the outer flex layers, with a little current and temperature feedback sensors, would heat the silicon skin slightly to the touch. The temperature sensors would allow the microprocessors to keep the skin heat constant and yet still measure fingertip contact temperature. Similarly, they could use Peltier cooling diodes or even cooling/heating coils embedded within the robot's hands to keep the skin cool in hot climates and to disperse any heat generated by the electric motors.

The heat resistors can also measure air flow, just like your hands do, with a heated resistor and a non-heated resistor. Any air flow will cause a rise in current required to keep the temperature constant, and you can measure air flow as hair and skin do. There is not much room inside a human's finger for too many tubes, wires, or sensors. The small space is needed for all the electric muscles and the joints. This is where flex circuits shine, as they can easily be made very small, thin, and very flexible as well as loaded with electronic sensors.

I predict the next generation of flex circuits may even be molded right into the robot's silicon skin, increasing space available inside the fingers for little motors and skeleton structures. If you order the new SE 3000 version personal satisfaction robot, you will want as many tactile sensors as possible, as well as heated skin (just kidding about the SE 3000 robot). However, this column shows it is possible to use flex circuits for many other purposes. **FLEX007**



John Talbot is president of Tramonto Circuits. To read past columns or contact Talbot, [click here](#).

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Flex007 Highlights



Flexible Thinking: Thermal Management—Electronic Technology's Rodney Dangerfield ▶

Thermal engineering has, unfortunately, often been treated with less respect than it deserved. Dealing with the heat generated by electronics was often not given full consideration until after the design was completed and prototyped, and the problem manifests as a failure. Joe Fjelstad emphasizes why keeping devices cool is a vital objective.

Flexible Circuit Technology Workshop #6: Designs, Principles, and Practices ▶

In less than 30 minutes, learn from flex expert Joe Fjelstad about considerations when designing flexible circuits. Segments include topics such as flexible circuit designs, principles, and practices; design guidelines for bending, folding, and dynamic movement of flexible circuits; flexible circuit singulation methods; assembly aids, and more.

Flex on the Brain: The Future of Neural Interfaces ▶

The SMTA Additive Electronics TechXchange took place virtually on October 14, with presentations from a wide variety of technologists involved in additive processes. One of the highlights was a presentation titled “Flexible Electronics for Neural Interfaces” by Dr. Jonathan Viventi, assistant professor of biomedical engineering at Duke University.

Thinfilm Announces First Multi-Cell Solid-State Battery ▶

Thin Film Electronics ASA—a developer of ultrathin, flexible, and safe energy storage solutions for wearable devices and connected sensors—announced significant progress in

device manufacturing and packaging innovation in support of its premium microbattery products based on solid-state lithium battery (“SSLB”) technology.

EPTE Newsletter: Hitachi Chemical Now Showa Denko ▶

Hitachi Chemical, a consolidated subsidiary of Showa Denko, recently changed its name to Showa Denko (they will now be part of this company). Dominique Numakura details how company officials released a statement commenting on the new name and adding that this collaboration will generate new business trends.

Trackwise Implements Further Upgrading of FPC Manufacturing Operations ▶

Trackwise, a recognised innovator of flexible printed circuit (FPC) technology, continues to strengthen its production capability and capacity by investing in new equipment. The company has installed a highly advanced roll-to-roll direct imaging system and has also invested in a roll-to-roll flexible circuit laser drilling system.

PV Nano Cell, Profactor Publish Results of Printed Embedded Passive Components ▶

PV Nano Cell Ltd., an innovative provider of inkjet-based conductive digital printing solutions and producer of conductive digital inks, and PROFACTOR GmbH (Steyr, Austria), an applied production research company in the field of industrial assistive systems and additive micro/nanomanufacturing, published the first results of printed embedded passive components including silver and carbon-based resistors and capacitors.

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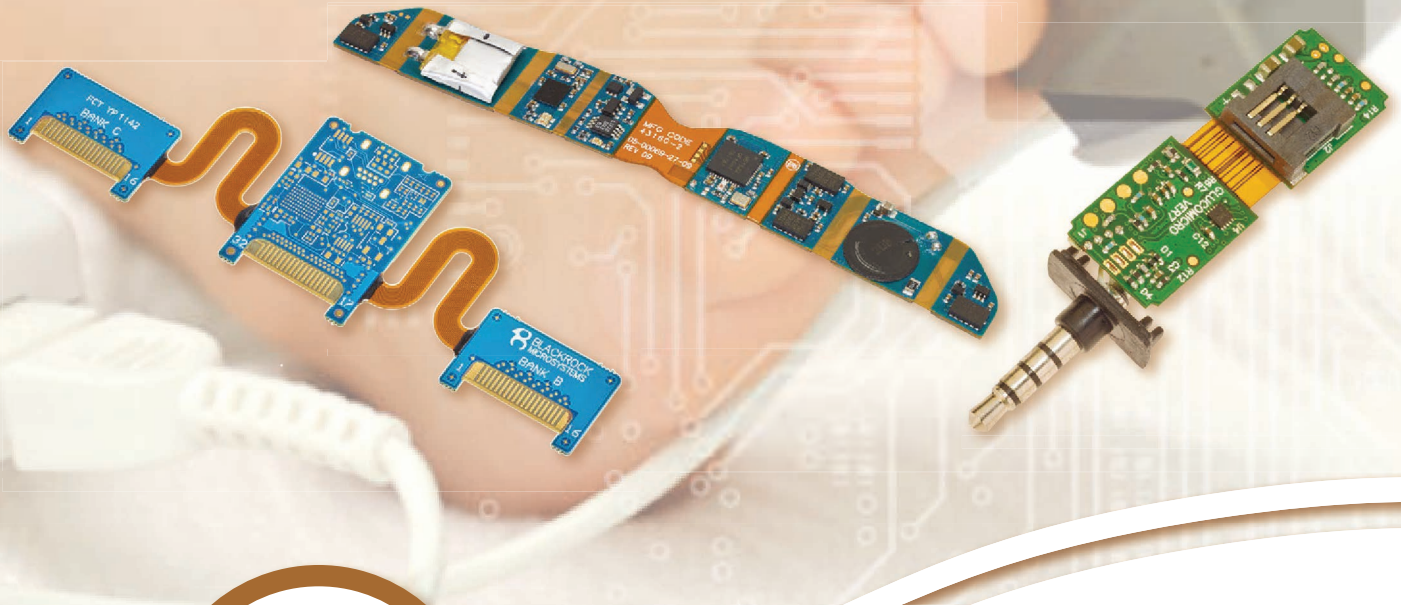
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Next-Generation Flex Circuits: Printable Is Compatible With Flexible

EPTE Newsletter

by Dominique K. Numakura, DKN Research LLC

Copper foil is the primary conductor material used in traditional flexible circuits. These thin metallic foils laminated on heat-resistant plastic films are called copper-clad laminates. Photosensitive chemicals are coated on the copper foil, and circuit patterns are printed. Next, a process called photolithography or subtractive is used, and the result is the production of electronic circuits (once unnecessary material is removed).

The photolithography process is now popular in the printed circuit industry, and circuit manufacturers have an etching line process in their basic manufacturing. The chemical etching is not environmentally friendly. Its by-products are considered chemical waste and require supplemental recycling; this adds cost to printed circuit products.

Thick-film circuits are another option to generate flexible circuits. They are created using a printing process that is very simple. Conductive ink (such as silver and graphite conductive powders) is printed on plastic films from a traditional screen-printing process, dried, and baked in a thermal oven. Copper-clad laminates are not required, so material expenses are minimized. Almost any material can be used (papers, textiles, or rubber sheets) with the flexibility from printing.

Wearable and medical devices require abnormal performances such as stretchability, transparency, moisture permeability, and more. These new products and applications require the use of flexible circuits and are dependent on non-traditional electronic materials. Conductive inks are very compatible with these



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non-traditional materials, and thick-film printing is very suitable. The screen-printing process can increase up to 1000 mm x 1500 mm, and an even larger circuit sizes are possible as long as the screen is available.

Another advantage of thick-film technology is the availability of functional materials. Various devices—such as flexible sensors, flexible ELs, photovoltaic cells, and switches—are built with a simple process using appropriate inks. The thick-film process does not generate any chemical waste; thus, the manufacturing is very cost-effective.

Thick-film circuits have conductivity and silver atom migration issues. Advancements have improved over the last few years, but the conductivity from a silver ink circuit is at least

two orders smaller as compared to copper foil circuits. Applications may be limited.

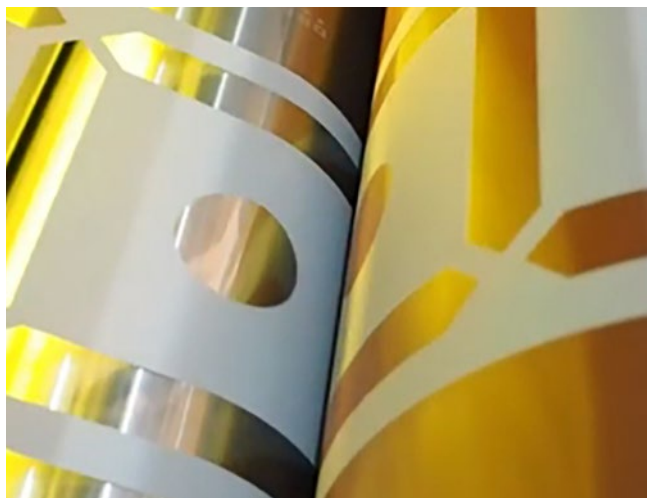
With thick-film flexible circuits, advantages outweigh the disadvantages. Applications continue to expand, and a printable process is an excellent option for flexible electronics. Technological collaborations will create more opportunities for flexible circuits. **FLEX007**



Dominique K. Numakura is the managing director of DKN Research LLC. Contact haverhill@dknresearch.com for further information and news. To read past columns, [click here](#).

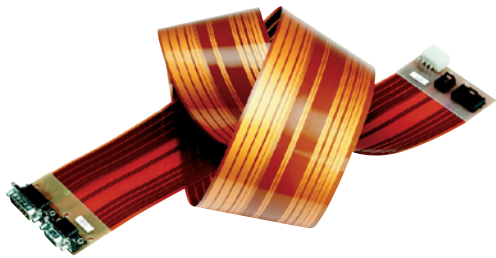
Ynvisible Delivers Roll-to-Roll Printed Scoreboard Displays to Pickletech

Ynvisible Interactive Inc. has announced the first commercial delivery of wholly customized roll-to-roll printed segment displays to Pickletech, LLC, a technology company providing portable scoreboards for use in Pickleball tournaments and events. A proprietary mobile application remotely operates the highly visible display in both indoor and outdoor applications. The successful delivery to Pickletech is the largest roll-to-roll display production order by size to date from Ynvisible's production facilities in Linköping, Sweden.



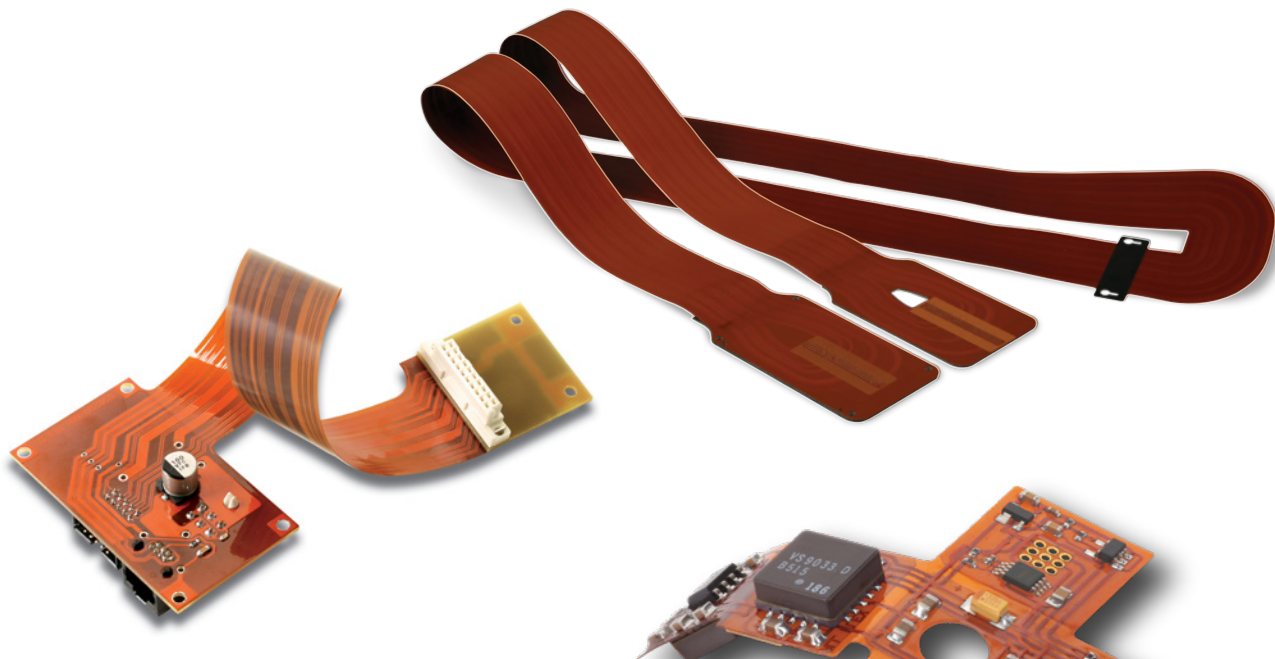
"We are excited about this delivery to Pickletech as the displays are used in real-life situations where large audiences will see the displays in use. This is an accomplishment of our prototyping services and the successful transition to large area roll-to-roll production of electrochromic displays. We can make displays completely customizable to a client's needs and deliver in increasing volumes. We are thrilled with yet another client success," said Tommy Hoglund, Ynvisible's Vice President of Sales and Marketing.

"Ynvisible's technology has allowed us to have custom displays specific to our needs that are 7x larger than our previous design and cost savings of 60% over the previous, smaller displays. That unit cost savings includes full design, prototyping, and a modest initial production run. The operation of the displays is also much more visually appealing compared to ePaper. The transition from one number to the next is smooth without the flashing/blinking associated with ePaper technology. Lastly, the driver interface for the displays was much simpler than the ePaper displays. This allowed us to further reduce costs by simplifying the design of the other electronics needed to operate the scoreboard," said Jarick Rager, owner of Pickletech. (Source: Ynvisible Interactive)

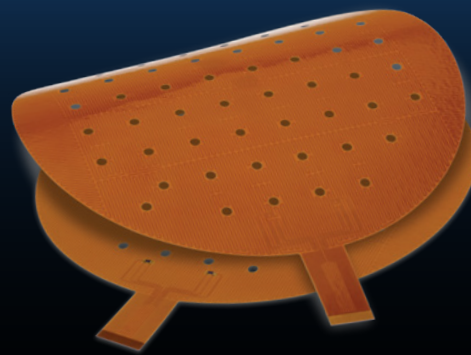


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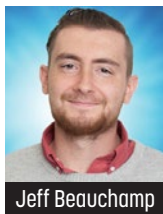
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1 Fresh PCB Concepts: 4 Characteristics to Consider When Selecting PCB Base Materials ►

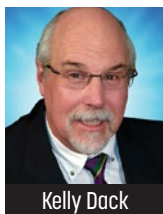
Selecting the correct material is critical if you want your circuit board to survive the assembly process or come out of the assembly process in good condition. Jeffrey Beauchamp explains the four main characteristics from the IPC-4101 material specification that are critical in finding the performance of your base material.



Jeff Beauchamp

2 The Digital Layout: Education Unlocks the Golden Door to Freedom ►

Kelly Dack speaks with the PCEA Educational Committee regarding the team's take on the PCEA's role in education. What do they have in store? PCEA Chairman Steph Chavez also weighs in on the strength of our education committee and why it is crucial to the PCEA's mission.



Kelly Dack

3 Standard of Excellence: 4 Areas That Will Improve by Next Year ►

As we continue to work our way through this pandemic, it makes us wonder about—and even yearn for—what things will be like one year from now. Anaya Vardya shares four things that we have been forced to do today that we will still be doing in October of 2021.



Anaya Vardya

4 Connect the Dots: Unraveling the Mysterious BGA Routing Mess ►

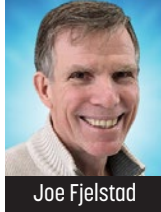
A ball-grid-array (BGA) device can be a daunting component to route, especially in fine-pitch arrays featuring solder ball counts in the hundreds and pitch values as tight as 0.5 millimeters. Bob Tise and Matt Stevenson describe how you can take the mystery out of BGA routing and create a PCB design that can handle all those pesky narrow spaces.



Stevenson & Tise

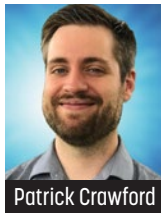
5 Flexible Circuit Technology Workshop #5 Tackles Structures, Applications, Materials, and Manufacturing Processes: Think and Plan in Three Dimensions! ►

In just 15 minutes, flex expert Joe Fjelstad will teach you about implementing this useful technology into your manufacturing operation. Joe suggests you start with defining your end-product requirements and understanding cost and product life cycle expectations, as well as end-user needs. He further addresses the many considerations with adopting this useful technology.



6 Design Circuit: IPC-2231 Captures Board Design Best Practices ►

There are new document revisions being prepared for industry review throughout the IPC standards development ecosystem. Patrick Crawford focuses on one such document: the IPC-2231 DFX Guidelines, which is currently being revised into IPC-2231A and will help create excellent boards.



7 I-Connect007 Editor's Choice: Five Must-Reads for the Week ►

It's showtime! This past week, we saw quite a bit of news about virtual trade shows. It's great to see show managers pivot from live, in-person events to virtual shows with only a few months to make it all happen. How would you like to be a show manager today?

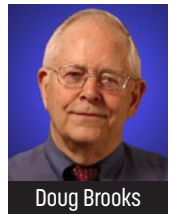
8 Elementary, Mr. Watson: Location, Location, Location ►

When it comes to PCB design, one of the most overlooked principles is component placement. Similar to a home, the component location has a considerable impact on the quality and is the real value of a PCB design. John Watson examines five rules to follow when it comes to component placement.



9 Stop Relating Trace Temperature to Current Density ►

Many design engineers and even many software suppliers make the significant mistake of equating changes in trace or via temperature with current density. This is incorrect at best and dangerous at worst. There is little if any correlation between temperature and current density. Current and trace dimensions (among other things) are the relevant variables, but current density is not. Doug Brooks shares four illustrations to help understand this.



10 Real Time with... AltiumLive 2020: Eli Hughes' Full-Stack Hardware Engineer Keynote ►

Nolan Johnson details TZero Co-founder Eli Hughes' keynote presentation titled "Crossing the Chasm: The Road to Becoming a Full-Stack Hardware Engineer," demonstrating how it takes cross-disciplinary thinking to truly innovate.



PCBDesign007.com for the latest circuit design news and information.

Flex007.com focuses on the rapidly growing flexible and rigid-flex circuit market.

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The technical service rep will be responsible for day-to-day engineering support for fabricators using our chemical products. The successful candidate will help our customer base take full advantage of the benefits that are available through the proper application of our chemistries.

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Career Opportunities



SMT Operator Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for a **surface-mount technology (SMT) operator** to join their growing team in Hatboro, PA!

The **SMT operator** will be part of a collaborative team and operate the latest Manncorp equipment in our brand-new demonstration center.

Duties and Responsibilities:

- Set up and operate automated SMT assembly equipment
- Prepare component kits for manufacturing
- Perform visual inspection of SMT assembly
- Participate in directing the expansion and further development of our SMT capabilities
- Some mechanical assembly of lighting fixtures
- Assist Manncorp sales with customer demos

Requirements and Qualifications:

- Prior experience with SMT equipment or equivalent technical degree preferred; will consider recent graduates or those new to the industry
- Windows computer knowledge required
- Strong mechanical and electrical troubleshooting skills
- Experience programming machinery or demonstrated willingness to learn
- Positive self-starter attitude with a good work ethic
- Ability to work with minimal supervision
- Ability to lift up to 50 lbs. repetitively

We Offer:

- Competitive pay
- Medical and dental insurance
- Retirement fund matching
- Continued training as the industry develops

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SMT Field Technician Huntingdon Valley, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:

- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:

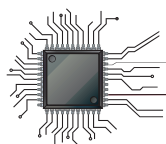
- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
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- Ability to arrange and schedule service trips

We Offer:

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- Retirement fund matching
- Continuing training as the industry develops

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MivaTek Global: We Are Growing!

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For more information, click below.

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Sales Account Manager

Sales Account Management at Lenthor Engineering is a direct sales position responsible for creating and growing a base of customers that purchase flexible and rigid flexible printed circuits. The account manager is in charge of finding customers, qualifying the customer to Lenthor Engineering and promoting Lenthor Engineering's capabilities to the customer. Leads are sometimes referred to the account manager from marketing resources including trade shows, advertising, industry referrals and website hits. Experience with military printed circuit boards (PCBs) is a definite plus.

Responsibilities

- Marketing research to identify target customers
- Identifying the person(s) responsible for purchasing flexible circuits
- Exploring the customer's needs that fit our capabilities in terms of:
 - Market and product
 - Circuit types used
 - Competitive influences
 - Philosophies and finance
 - Quoting and closing orders
 - Providing ongoing service to the customer
 - Develop long-term customer strategies to increase business

Qualifications

- 5-10 years of proven work experience
- Excellent technical skills

Salary negotiable and dependent on experience. Full range of benefits.

Lenthor Engineering, Inc. is a leader in flex and rigid-flex PWB design, fabrication and assembly with over 30 years of experience meeting and exceeding our customers' expectations.

Contact Oscar Akbar at: hr@lenthor.com

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Senior Process Engineer

Job Description

Responsible for developing and optimizing Lenthor's manufacturing processes from start up to implementation, reducing cost, improving sustainability and continuous improvement.

Position Duties

- Senior process engineer's role is to monitor process performance through tracking and enhance through continuous improvement initiatives. Process engineer implements continuous improvement programs to drive up yields.
- Participate in the evaluation of processes, new equipment, facility improvements and procedures.
- Improve process capability, yields, costs and production volume while maintaining safety and improving quality standards.
- Work with customers in developing cost-effective production processes.
- Engage suppliers in quality improvements and process control issues as required.
- Generate process control plan for manufacturing processes, and identify opportunities for capability or process improvement.
- Participate in FMEA activities as required.
- Create detailed plans for IQ, OQ, PQ and maintain validated status as required.
- Participate in existing change control mechanisms such as ECOs and PCRs.
- Perform defect reduction analysis and activities.

Qualifications

- BS degree in engineering
- 5-10 years of proven work experience
- Excellent technical skills

Salary negotiable and dependent on experience. Full range of benefits.

Lenthor Engineering, Inc. is the leader in Flex and Rigid-Flex PWB design, fabrication and assembly with over 30 years of experience meeting and exceeding our customers' expectations.

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- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

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APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

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Sales Representatives (Specific Territories)

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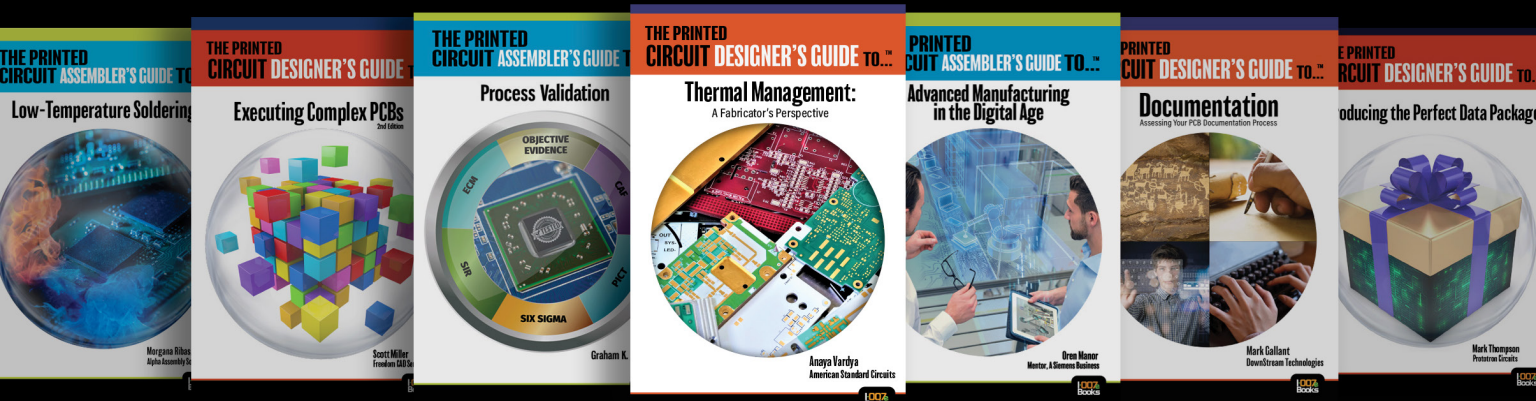
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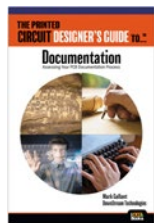
Implementing “Digital Twin” Best Practices From Design Through Manufacturing with Expert Jay Gorajia, a 12-part micro webinar series.



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Thermal Management: A Fabricator's Perspective, by Anaya Vardya, American Standard Circuits
Beat the heat in your designs through thermal management design processes. This book serves as a desk reference on the most current techniques and methods from a PCB fabricator's perspective.



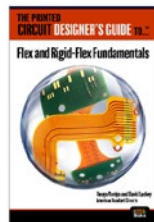
Documentation, by Mark Gallant, Downstream Technologies
When the PCB layout is finished, the designer is still not quite done. The designer's intent must still be communicated to the fabricator through accurate PCB documentation.



Thermal Management with Insulated Metal Substrates, by Didier Mauve and Ian Mayoh, Ventec International Group
Considering thermal issues in the earliest stages of the design process is critical. This book highlights the need to dissipate heat from electronic devices.



Fundamentals of RF/Microwave PCBs, by John Bushie and Anaya Vardya, American Standard Circuits
Today's designers are challenged more than ever with the task of finding the optimal balance between cost and performance when designing radio frequency/microwave PCBs. This micro eBook provides information needed to understand the unique challenges of RF PCBs.



Flex and Rigid-Flex Fundamentals, by Anaya Vardya and David Lackey, American Standard Circuits
Flexible circuits are rapidly becoming a preferred interconnection technology for electronic products. By their intrinsic nature, FPCBs require a good deal more understanding and planning than their rigid PCB counterparts to be assured of first-pass success.

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