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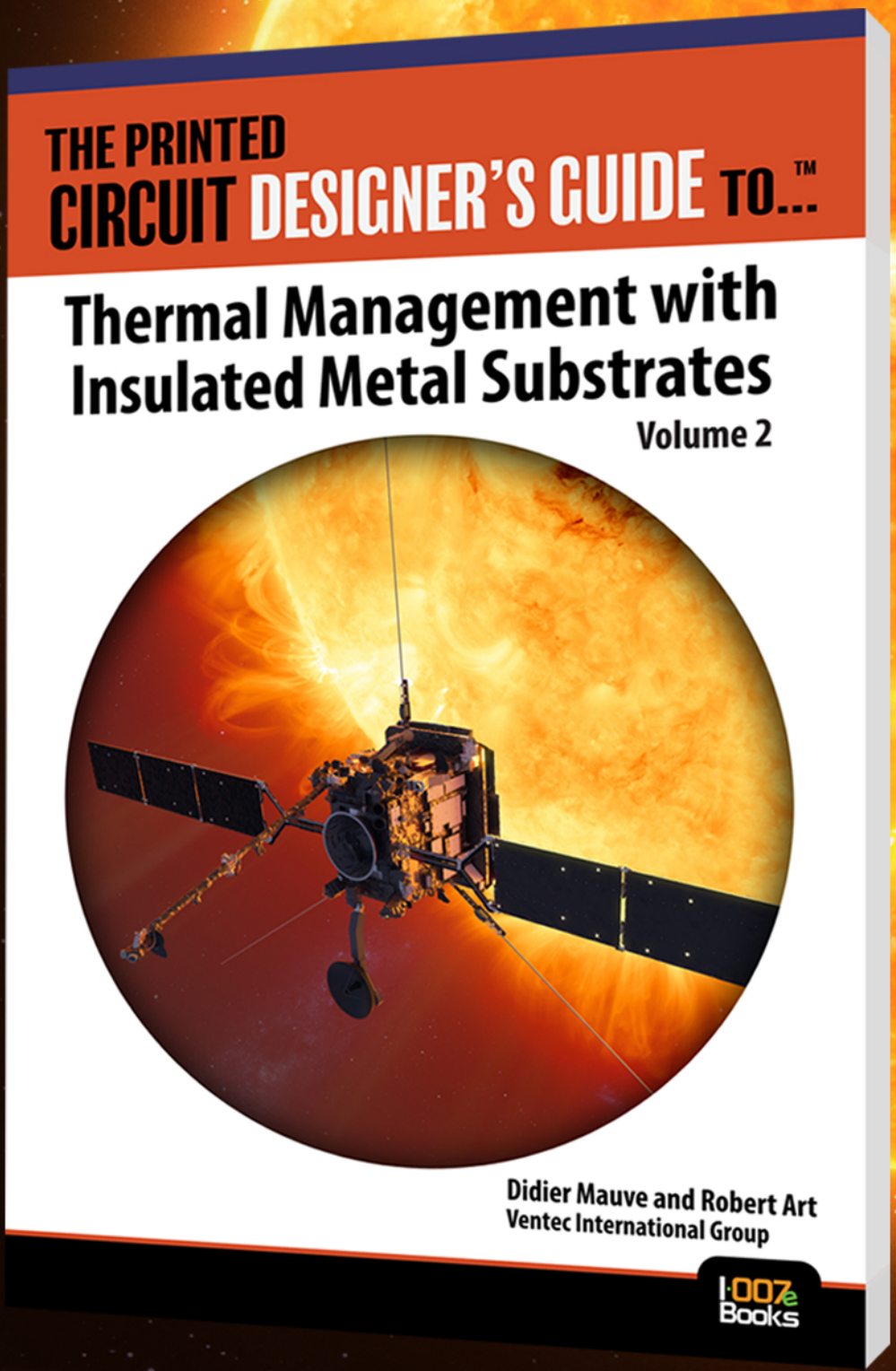

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To UHDI and Beyond!

It is tough to get much smaller than ultra HDI. This is a whole new level of miniaturization for most PCB designers and fabricators. UHDI folks speak in terms of microns, not mils. And everything changes when you start working with 15-micron lines and spaces. For this issue, we asked some of the top UHDI experts to share their knowledge about designing and fabricating these tiny features. Join us as we journey to UHDI and beyond!

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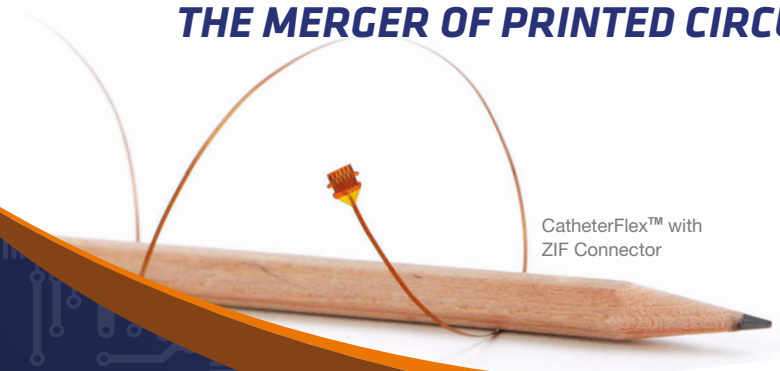

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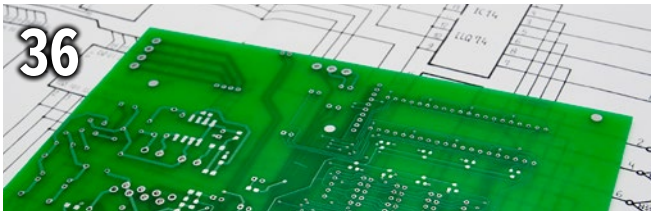

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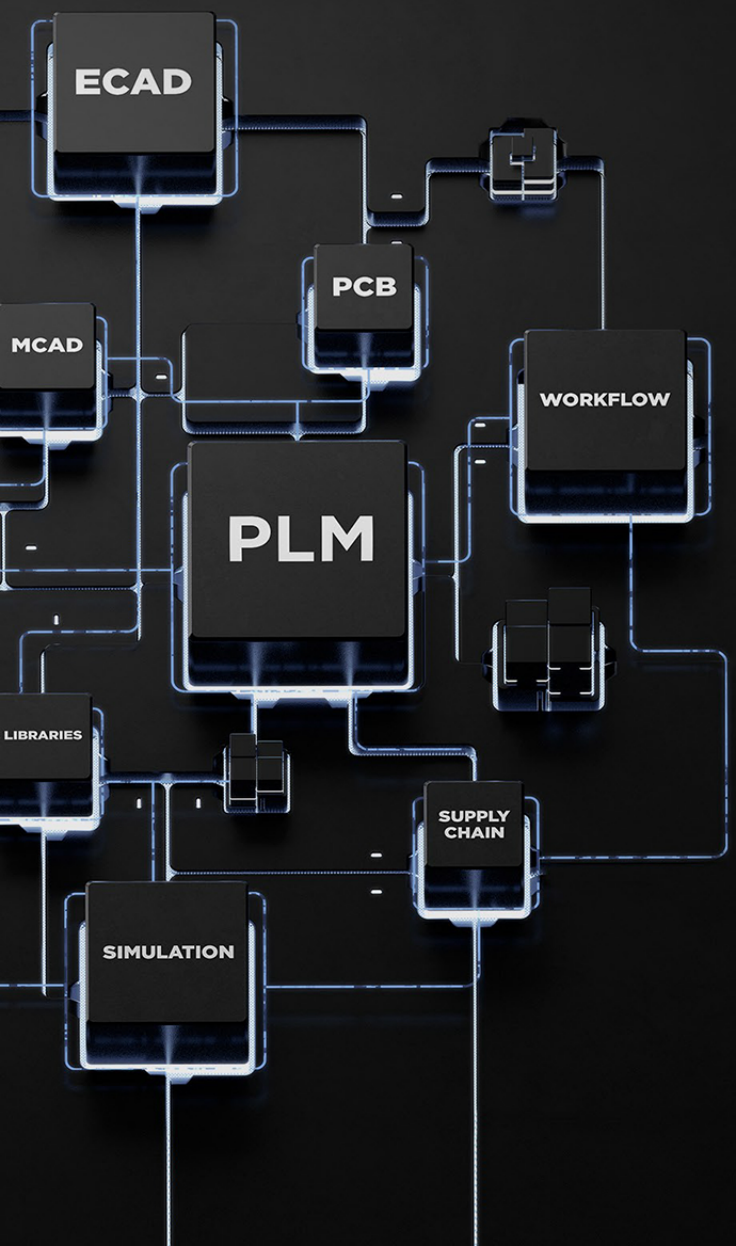

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Let's Get Small

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

Comedian Steve Martin could have been talking about this issue of *Design007 Magazine* when he released his album "Let's Get Small" in 1977—or maybe not. Well, as Steve would say, excuuuuse me! (You may have to explain that reference to any young people in your company.)

But it is tough to get much smaller than ultra HDI. This is a whole new level of miniaturization for most PCB designers and fabricators. UHDI folks speak in terms of microns, not mils. Everything changes when you start working with 15-micron lines and spaces.

The IPC D-33AP Task Group is working hard at updating standards for UHDI because standards can barely keep up with UHDI processing. Cleanliness becomes all-important at that level, as a speck of dust can wreak havoc on UHDI circuitry. We're talking about near-cleanroom quality.

When we started planning this issue, we quickly discovered that there aren't that many UHDI experts in North America; the overwhelming majority of UHDI technologists and facilities are in Asia. As a designer half-jokingly told me recently, "Most of the world's experts in UHDI speak Mandarin." (I only know about 10 words in Mandarin, and half of those are slang, so that could be a problem.)

The DoD has begun to recognize that the United States is behind the rest of the world in critical electronics manufacturing, and UHDI is a perfect example. But it's no easy feat for a fabricator to jump into UHDI; a direct imaging machine alone runs close to $1 million.

Even as the use of UHDI continues to grow with processes such as A-SAP and mSAP, there's a dearth of information available in English. Very few instructors in our industry teach UHDI design or fabrication curriculum, and there are not many UHDI resources online or elsewhere. We realized this was a great chance for *Design007 Magazine* to help fill that void by focusing on UHDI processes.

So, we asked some of the top UHDI experts to share their knowledge about designing and fabricating these tiny features. In this issue, we cover the challenges and opportunities in UHDI design, and the level of commitment required to become one of these top-level designers. Our goal is that you understand the critical points in the UHDI fabrication process to advance your capabilities of UHDI design.

In our conversation with Royal Circuits' UHDI expert Herb Snogren, he explains exactly what constitutes ultra HDI, where the current cutting edge lies, and the hurdles facing anyone who wants to design or manufacture boards at the 20-micron level or below. Instructor Cherie Litson breaks down the semi-additive manufacturing process and shares some of her tips and tricks for designing A-SAP and mSAP circuits. Columnist Tara Dunn explains how to speed up the "learning curve" for UHDI circuits, and she answers common questions from new UHDI technologists.

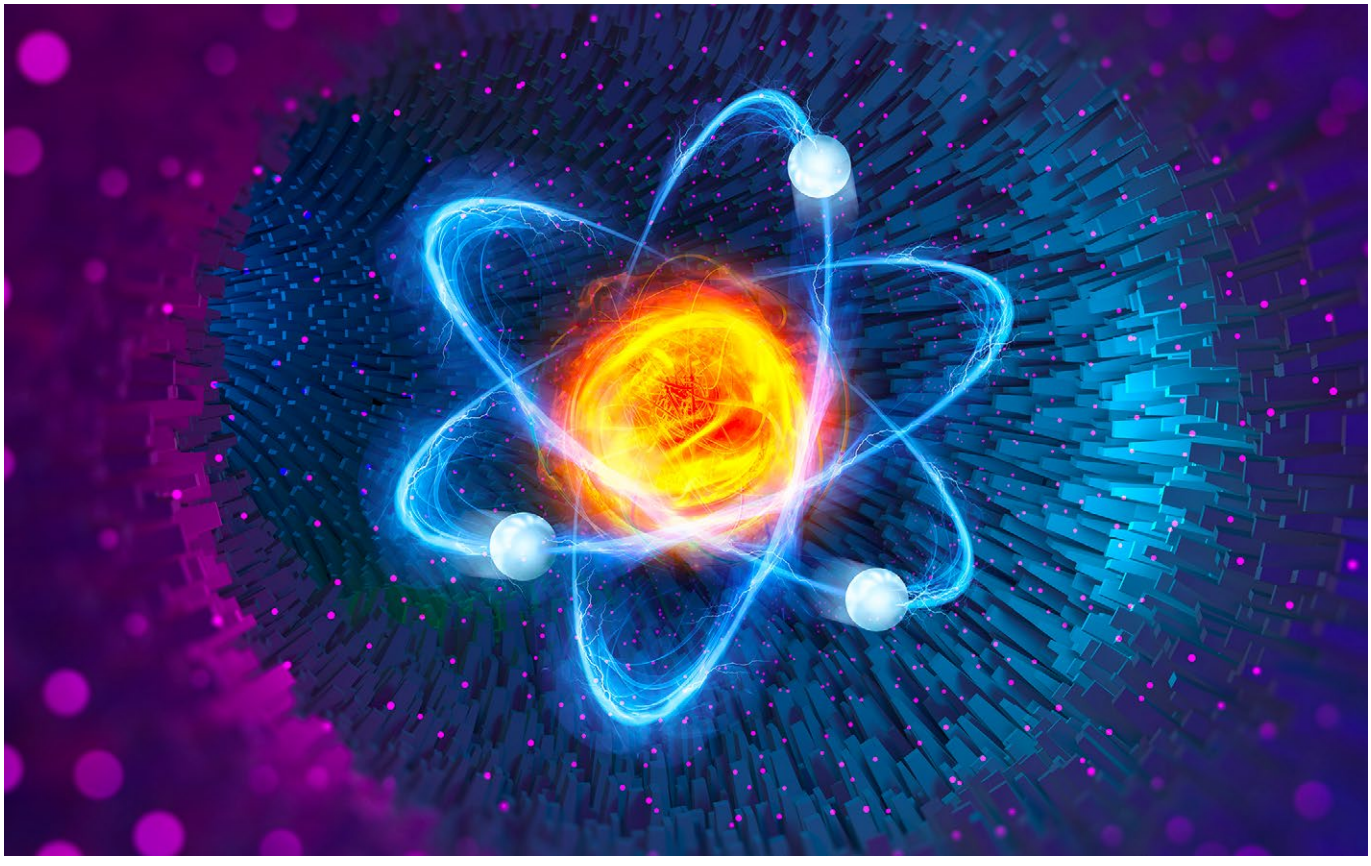
Columnist Vern Solberg discusses how to conduct an interconnect capacity analysis to determine whether a design should utilize HDI or UHDI features. Jan Pedersen of NCAB, co-chair of the IPC D-33-AP Subcommittee, details their efforts to form UHDI standards. Kelly Dack then describes how he suddenly found himself working on designs with 15-micron lines and offers some advice for working on these tiny features.

We bring you columns from Barry Olney, Matt Stevenson, John Coonrod, Istvan Novak, Saskia Hogan, Matt Walsh, and Joe Fjelstad. In our flex space, we have an article by Stan Farnsworth and the concluding installment of our printed electronics roundtable with Kevin Miller, Mike Wagner, John Voultos, and Tom Bianchi.

There's a real need for information about UHDI. As you move forward into the world of microns, I hope you will consider this month's *Design007 Magazine* as a reference. One final note, if you haven't already, be sure to follow us on LinkedIn and Twitter. There you'll find updates and links to many of our most popular features. Let's have a conversation online, and get small! **DESIGN007**

Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 23 years. To read past columns, click here.

Ultra HDI Primer



Feature Interview by the I-Connect007 Editorial Team

We recently spoke with Herb Snogren, an industry veteran and consultant with Summit Interconnect tasked with leading the company's ultra HDI efforts. Herb is co-chair of the IPC ultra HDI subcommittee, IPC D-33-AP. In this interview, Herb discusses the current state of UHDI, how designers and fabricators can get started working in this new frontier, and why the U.S. must invest in UHDI technology now to counteract Asia's near dominance of the UHDI segment, which has left some of our critical industries vulnerable to supply chain disruptions.

Andy Shaughnessy: Herb, almost everyone I talk to about this topic asks me, "What is the definition of ultra HDI?" What's the manufacturable limit?

Herb Snogren: We've developed an IPC subcommittee, IPC D-33-AP. Jan Pedersen of NCAB Group is my co-chair, and we've defined ultra HDI as printed circuit boards that have line widths and spaces below 50 microns, and microvias at 75 microns and below in diameter. We came up with that delineation because of IPC-2226, which lists product attributes with producibility levels A, B, and C. Level C is the lowest producibility level and that stops at 50-micron lines and spaces.

Shaughnessy: Tell us about the committee's efforts.

Snogren: What's important to understand is that circuit boards are following the path of packaging substrates. We now have the term

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Elevate Your PCBs

Herb Snogren

SLP (substrate-like PCB) because printed circuit boards, at least in Asia for small form-factor products, are being produced with manufacturing techniques similar to IC substrates. IC substrates now have line widths and spaces down to 6 and 8 microns, and that's where we're going. When you look at some of the Apple and Samsung products, they're in the 20- to 25-micron line and space range in high volumes.

Shaughnessy: For years, we've been hearing that the convergence of IC and PCB processes was on the horizon. It seems like we're finally there now.

Snogren: We are. Historically, IC substrates were made with semi-additive or modified semi-additive processing, and now printed circuit boards are being made with semi-additive and modified semi-additive processing. It is really happening.

Shaughnessy: Is Asia the center of ultra HDI?

Snogren: Yes. It really started with Apple working with their suppliers in Asia to get their line widths and spaces down. They did it in a big way, but because of that, other companies are taking advantage of the capability that's been established. There are companies in other parts of the world that can do that. There may be one or two in Israel and Europe, but more than 95% of the volume is being done in Asia, with most of it in China.

Shaughnessy: What segments are driving the development of ultra HDI?

Snogren: It's anything that has a small form factor. It started with the cellphone, just trying to pack more capability into a small space. You see it in medical devices that need to be small, such as in-ear devices or hearing aids. We need to do implantable devices that must be small and innocuous. With heterogeneous integration and cramming more transistors into a square inch through heterogeneous packaging, there are more I/Os on the device. The I/O density increases, so your pitch decreases, and that's driving this as well.

Shaughnessy: Are design engineers from the PCB side studying IC laminate design processes, and vice versa?

Snogren: Product designers need to understand there is a manufacturing process capable of producing these finer features, and they can employ those in their products to reduce the size of the product or reduce layer count. The problem is you can't get it in the United States, so if they design it, they don't have a place to buy it here. You must go to Asia. Right now, companies are trying to develop it. Averatek has some licensees who can do this. Winonics (Additive Circuits Technologies) has a similar technology it is developing. But I don't know if anyone is doing anything in a meaningful way or volume. Certainly not in any kind of volume at this point.

Shaughnessy: UHDI seems to be uncharted territory. What's the biggest hurdle for fabricators

who want to get involved? What will they need to learn and upgrade?

Snogren: On the equipment side, you must invest in direct imaging equipment that has 20-, 25-micron feature size capabilities or less. You find resists that are compatible with your imaging system. Then there's AOI equipment. You need specialized plating equipment for doing simultaneous pattern plate and micro-via filling, and equipment for handling thin foil and ultra-thin foil, 1- to 3-micron foils, and differential etching equipment. If they want to go fully into semi-additive processing, they should look into something like Averatek or eSurface to get electroless copper to stick to a wide variety of laminates.

Shaughnessy: Because this is all build-up at this point, right? You can't do subtractive at this level.

Snogren: It's difficult. Asian fabricators were doing subtractive down to 30- to 40-micron lines and spaces. Once they hit that point, most of them started using modified semi-additive processes. One big aspect is cleanliness. I don't know that any of us in the U.S. understand the cleanliness aspect of it, and how clean our processes must be. Once you start running in volume, those small particulates that don't bother you when you're at 3-mil line and space suddenly become a big percentage of a 20-micron line and space. We may have to deal with much different environmental issues in our factories with clean air, water, and processing tanks, ultra-filtration, special handling. It's going to be different.

Nolan Johnson: It seems that we're down to the dimensions that triggered cleanroom environments in the IC world 20 or 30 years ago, and that was very successful. We will be looking at that for our fabrication facilities in those dimensions as well, which will raise the cost of a UHDI facility.

Snogren: Yes, it will be difficult to justify having this cleanroom environment and ultra-filtered processes and air just to build standard 4-layer or 6-layer 4-mil line and space products. That's why some Asian factories doing these types of products are specialized. All they do is build these HDI and ultra HDI products.

Shaughnessy: It seems like a big opportunity here for our fabricators.

Snogren: It's a chicken or the egg scenario. You must develop the capability and hope people will buy it. But if you don't develop the capability, they won't even design those features because they can't get it. It's a tough investment decision to make for companies in North America. But I believe if you have the capability and demonstrate it, people will begin to design products that take advantage of that capability.

It's a chicken or the egg scenario. You must develop the capability and hope people will buy it.

Shaughnessy: Will UHDI change the PCB designer's job?

Snogren: The HDI design standards in IPC-2226 don't really address some of the requirements for feature sizes, alignments, and spaces below 50 microns very well. That's something that our D-33-AP committee is trying to address. How do the design standards need to change or how do we need to adapt them for ultra HDI features?

Here are some things that we've already identified: The plating thickness requirements, annular rings, and dielectric thicknesses are different. We may not even use foil if we go to semi-additive, and many of the design standards

don't address that. Of course, 6012 needs to be modified as well to allow for thinner copper conductors because they're not doing 1 mil or 1.2 mils of plating on line widths that are 20 microns and below. They're typically in the 12- to 18-micron thickness range, which doesn't meet 6012. Solder mask thicknesses may need to decrease when you have devices with 0.2-millimeter BGA pitches; you can't have thick solder mask or you get a standoff.

Shaughnessy: What about EDA tools? Can they go down to the 20-micron level?

Snogren: Yes. That's not a problem as far as EDA tools go, because a 25-micron line is just another D-code in the system. Some of the design rule criteria would be different, certainly, such as the annular rings. Some of the requirements that you would have on the drawing with conductor thickness or plating thicknesses would be different.

Shaughnessy: It seems like, as far as signal integrity, there would be a lot of advantages, but still quite a few hurdles as well.

Snogren: Yes. UHDI can be beneficial in one way: You can certainly get a higher precision line width and spacing when you're doing semi-additive processes because your etch loss is virtually nothing. You can be very precise, but you're dealing with very small features and any minor imperfection will cause an issue that you wouldn't see on a 3-mil line and space job.

Shaughnessy: It seems like at this level you would want to simulate and run analysis every time?

Snogren: Yes, and you need to do that in conjunction with the fabricator because there are so many different techniques now for manufacturing a given feature. You can do it with subtractive, semi-additive, or modified semi-additive. They will all give you a slightly different result in maybe conductor thickness or tolerance. You must work in conjunction with the fabricator, understand their process, what the result will be, and design around their process. It's no longer just designing it, throwing it over the fence, then seeing who will snag it and try to build it. There must be more cooperation between the designer and the fabricator.

Shaughnessy: I mean, you're not going to start off an ultra HDI project without already having your fabricator selected. You've said that some vias are the thickness of a human hair?

Snogren: That's right. They're getting down below 3 mils in diameter. You're looking at 25- to 50-micron diameter microvias.

Shaughnessy: That's really intriguing. What does the typical UHDI process look like?

Snogren: It will be a buildup technology, where you start with a core and sequentially build layers on both sides as you go, using microvias as an interconnect between the layers. In some ways that's easy because registration is so simple. Each layer automatically registers to the layer below it, and you really don't have the kind of mismatch in registration that we have with regular multilayer boards and blind

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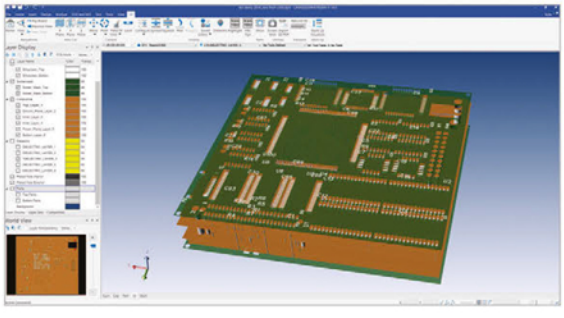

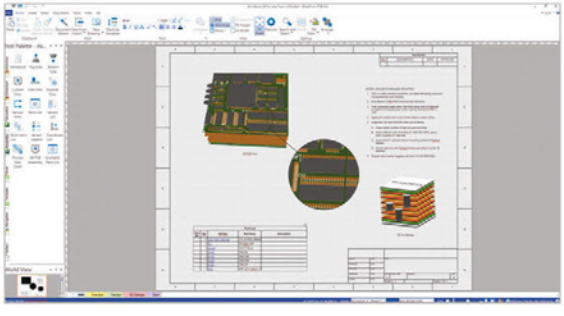

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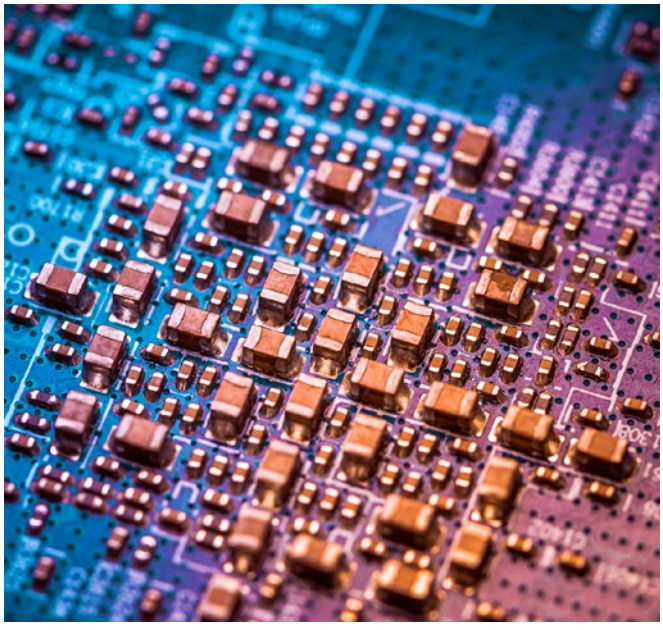


and buried vias. It's a sequential process. If you have five lam cycles sequentially, and you screw up the last one, you just burned up two to four weeks of work and you have to start over.

Shaughnessy: Now, much of this wouldn't have been possible even 10 to 15 years ago because these enabling technologies didn't exist, right?

Snogren: Direct imaging is a big one. That has helped with registration and feature size capabilities. When we were using film in the past, we had registration issues because the film moved, and we had to register it manually. It expanded and contracted with temperature and humidity. We had to pin it and the pinning wasn't always perfect.

Now we can have much smaller annular rings, much smaller feature sizes. With film, typically we had a really hard time getting down to 2-mil lines and spaces consistently when we were using a phototool. Not that it can't be done because they use phototools for ICs, but they're tiny and they use stepper cameras. They're not doing panels on a single sheet of film. Direct imaging is probably the biggest example. Anybody can buy a direct imaging system that can go down to 12 microns and maybe even less if you want to spend the money. If you get the right resist, you can resolve 20-micron lines and spaces fairly easily. That was unheard of 10 years ago. You couldn't even think about it.

Shaughnessy: Where are the bottlenecks in this whole process? Where do we need to innovate?

Snogren: It's just adopting the thin foils. Designers need to understand what the manufacturing process is like so they can design around it, whether it be using thin foils or semi-additive process with electroless copper. It's about understanding what the copper thicknesses will be, what the feature size capabilities are. For the fabricator, it's about getting the systems in place: the direct imaging system, AOI, electrical test, differential etch, the proper via fill and laser drill capabilities. HDI manufacturers already have these, so it's just a matter of adapting them to a slightly different process flow and adding a few other processes.

Shaughnessy: I keep hearing about the Asian companies doing UHDI well and for fairly cheap. What do we need to learn from them?

Snogren: They've already adopted modified semi-additive processing and semi-additive processing. With the modified semi-additive processing, which gets you down to 20- or 25-micron lines and spaces relatively comfortably, we must copy what they're doing. Remember, when they do this in Asia, it's in a factory that was designed to do nothing but that. They're not building a wide variety of products; they're only doing ultra HDI.

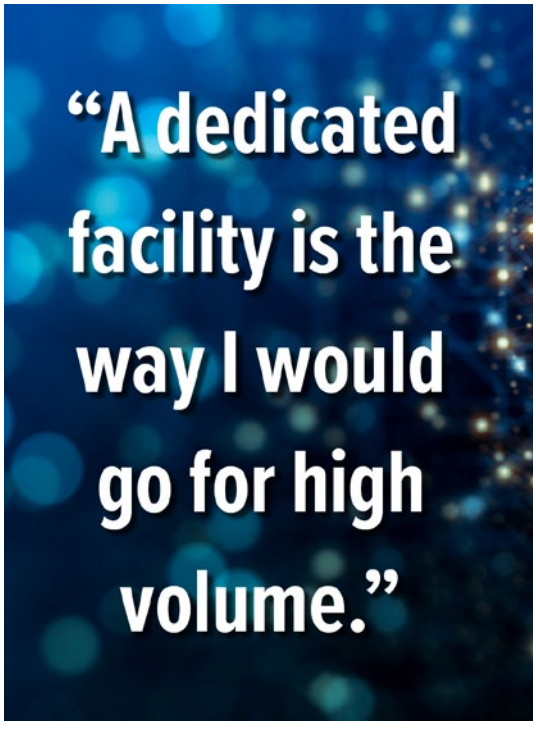
Shaughnessy: Those are all greenfield facilities.

Snogren: It's what they do all day, so it's a fairly standardized well-controlled process where they build things that are within a narrow design feature range.

Shaughnessy: What percentage of ultra HDI now is mSAP or A-SAP?

Snogren: When you look at printed circuit boards on the high-end cellphones, watches, and things like that, almost all of that is mSAP. The semi-additive process really is being used more on the packaging substrates, and they're using either electroless copper or vacuum-deposited copper on those products. I don't know that many circuit board manufacturers are trying to use semi-additive processing in volume anyway. But with Averatek, the licensed companies are starting to use that. It's certainly a viable way to approach it.

Shaughnessy: You mentioned that our process, our technologies, should learn to be more like the semiconductor industry, that we should learn from them. What are some things that we should take away from the way semiconductor manufacturers have been doing it?



Snogren: When they design a factory, it's around a capability. They deal with a process node and technology node, and if you're a semiconductor designer, you design into that node, you design into that factory. They don't just accept any design. They give you the design criteria in a file and you must follow that criterion. If you don't, they don't build it.

Shaughnessy: We had a magazine focused on design rules several months ago. With ultra HDI, will we need to have some uniform design rules and constraints?

Snogren: We need some general ones, and my IPC committee is working to develop those guidelines. We are developing a general guideline so designers know when they need to diverge from IPC-222x and IPC 60xx standards. We're trying to make it process agnostic as much as possible. We want it to be more general, suggesting that the designers talk to and work with their suppliers more closely on the design because they may use multiple techniques to fabricate the job. We haven't even talked about fully additive with inkjet printing conductors.

Johnson: When we start talking about UHDI, do you see that as the tipping point where cleanroom technology needs to happen? Is UHDI where we move to just greenfield facilities?

Snogren: For volume, yes. If you want to do volume and repetition, and do things with good yields, there's no doubt in my mind that's the case. For small companies in the U.S. that want to offer that as a capability, I don't really know where we start to run into the hurdles. I've been running some testing on 25-micron lines and spaces here and I haven't gotten to the point where it's become an issue, but we haven't really done a lot of volume. A dedicated facility is the way I would go for high volume. For an existing HDI factory, I believe one can produce small quantities of UHDI product with a decent cleanroom for the imaging processes and good filtration in electroless copper and electrolytic copper plating.

Johnson: Now it starts to feel like integrated circuits where, as you were saying, you build the factory around a particular technology. It feels like we're on the cusp here of having the cutting-edge printed circuit board fabrication philosophy start to look like IC.

Snogren: Yes. And when Apple decided it needed UHDI, the company didn't just throw designs over the fence and get somebody to build it. They went to companies like AT&S and Multek, and said, "Here's where we need to go. Here's our roadmap. Start developing capabilities to get there." They started doing that in factories that were already pretty specific to a certain capability anyway. I have friends who worked at a Multek HDI factory in Zhuhai. They said Apple and Samsung were migrating from 50-micron line and space to 40 and 35, then saying, "We've hit the wall in this factory. We're having to build a factory somewhere else that's going to do mSAP."

Johnson: Well, that's a fundamental shift for thinking in North America, for sure, and Europe as well.

Snogren: You can't be all things to all people. That's the thing. Multek is a good example. On their campus in Zhuhai, they have an HDI factory, a flex factory, a daughter board factory, and a back panel factory, and they're very segregated for a very specific type of printed circuit board.

> You can't be all things to all people. That's the thing.

Shaughnessy: Are there any good resources to learn more about ultra HDI, maybe in the form of websites, books, or instructors?

Snogren: Yes, there are a few resources, but not many. I learned about semi-additive processing when I first started.

Shaughnessy: How did you get into ultra HDI? Your father, Richard, wrote for me years ago.

Snogren: My father owned a circuit board factory, Reliable Circuits in Clearwater, Florida, when I was in high school. I worked there during college. After college, I worked at a couple of circuit board shops in Denver. Then my dad and I decided to start a shop in Colorado back in the mid-'80s, and we ran that for 16 years. I went to Coretec for a while, and then got hired as a consultant by Viasystems. I was in China for four years at the Guangzhou factory and the Zhongshan factory. I got to see another side of things. It's just ridiculously high volume.

I've been working with smaller companies recently, like Royal Circuits, which was acquired by Summit. I helped Royal Circuits develop its HDI capability several years ago. But the migration into ultra HDI really came through my work with the DoD and the PCB executive agent. I'm on the IPC-1791 committee, and we were talking about whether we should include IC substrates into IPC-1791. We found out there really aren't any industry design or quality standards for substrates. I started researching it a little bit and educated myself about IC packaging. I realized that not much happens in the U.S., certainly none of the fabrication of the substrates. This led to the creation of the IPC-D -33-AP committee to develop design and product performance standards for UHDI PCBs.

Shaughnessy: What does your roadmap look like for UHDI?

Snogren: We developed a roadmap at Royal Circuits last year. It's interesting because I came in originally about eight years ago when Royal was doing mostly 2, 4, and 6 layers. I worked with them to develop the capabilities to build HDI. I left for a while, then I approached Milan, Royal's owner, last year. I said, "Look, you're proficient now at HDI. You can do an eight- and 10-layer buildup board with five lam cycles and stacked microvias. You're good at it, but you are limited to 3-mil line and space. Let's put a roadmap together, get you down to

25-micron line and space because, if we can develop that capability, I believe we can get designers to design around that. We're not going to have a lot of competition." We put together a roadmap that we're in the process of implementing. We're not there yet, and we've got a couple pieces of equipment we need to buy, but we're moving in that direction and it's feasible.

Shaughnessy: This is the roadmap that you show your customers or is this internal?

Snogren: It's internal now. We have established the direct imaging equipment capability and the dry film capability. We have the inspection and test equipment capability. We need to upgrade our microvia filling system and purchase a differential etcher. Once we have the via filling system and the etcher, we'll be able to produce products with 25-micron lines and spaces. Whether our yields are going to be great, I don't know. But typically, these are tiny little boards so even if the defect density is a bit high, we will still have good board yields within a panel.

Johnson: Right. What do we tell designers?

Snogren: First, work with a vendor or several vendors to determine whether they can lay out a manufacturing roadmap. The roadmap for many OEMs could say, "We're seeing finer-pitch BGAs. We're going to have to use 0.3-mm or 0.25-mm BGAs and we're going to need 25- and 30-micron lines and spaces. We need you all to get there because we have a whole line of products coming in the next few years that require this." Then you pick a process and say, "We're going to use ultra-thin foil. I can already buy 1.5-micron foil, so we'll start developing this capability slowly and put together the roadmap." The designer can work with the fabricator to establish the design criteria and test vehicles and put that together. The fabricator will need to buy some equipment to support that.

From a designer standpoint, if they don't want to go straight to Asia and get what they want, they need to work with a fabricator and design around the fabricator's capability or develop that capability along with the fabricator. But it's the chicken or the egg. As a fabricator, do you invest in that capability? It's going to cost you money if you don't have potential orders coming in.

Six to eight years ago when you bought an LDI machine, you were limited at maybe 2-mil lines and spaces. Then they went down to 1-mil line and space, but they were expensive. Now, if you're buying a new direct imaging system, there's no reason not to get it with 25- or 12-micron line and space capability.

You can buy an LDI machine today for not a lot more money that's capable of getting you into ultra HDI, and it's still going to support doing your 3- to 4-mil line and space jobs. That's what happened at Royal Circuits. We bought a machine, not even for that capability, and I found out, "Hey, I can do 25-micron lines and spaces on this thing." We didn't even plan for that one.

Shaughnessy: Herb, thank you for your time today. This has been very informative.

Snogren: Happy to help. Thank you. DESIGN007

A Designer's Point of View

Feature Article by Cherie Litson
LITSON1 CONSULTING

HDI—high-density interconnect—designs require some different thinking on the part of the designer. One of the first things to consider is whether you need HDI, and how much. The HDI option comes into play as soon as you purchase any components with 0.5 mm pin pitch. The number of these components and other specifications of your design will determine the amount of HDI you will need. Here's a quick list of HDI options:

- Smaller vias
- Smaller traces
- Thinner dielectrics
- Tighter solder mask clearances
- Controlled paste mask construction

Each option brings choices that will affect fabrication and assembly, so a little research is needed before making these choices. I'm only going to explore the first two, as these often determine which fabrication process you want to use.

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Smaller Vias

A variety of options are available here:

Blind vias with through vias

This is the optimal choice. It adds a little expense while giving you the ability to place components on both sides of the board without having to be confined by opposing pad with different nets.

Blind and buried vias with through vias

This option gives you the most routing control; however, it also adds the most cost.

Through vias only

While this can cut fabrication costs, it limits breakout, routing, via size, and component placement. Smaller vias are dependent upon the aspect ratio of the board. Keep the board thin and most fabricators can produce smaller vias, down to 6 mils (0.15 mm) if your board measures 50 mils of thickness or less, without additional costs.

Both the A-SAP and mSAP processes can be used to plate holes. Again, the aspect ratio will make a difference. How much plating do you need? Are you plugging the vias with conductive or non-conductive material?

Smaller Traces

How small you go depends on the fabrication process you select and how small the component pin pitch is.

It's important to understand the differences between A-SAP and mSAP before you commit to a process. Standard subtractive etch processes start with very thin copper foils, etch a pattern, and then add copper for the finished traces and copper features. Table 1 is a chart for starting copper thicknesses from the IPC-6012.

When using basic core material, mSAP usually starts at the quarter-ounce copper thick-

Weight[1]	Absolute Cu Min. (IPC-4562 less 10% reduction) (µm) [µin]	Plus minimum plating for Class 1 and 2 (20 µm) [787 µin][2]	Plus minimum plating for Class 3 (25 µm) [984 µin][2]	Maximum Variable Processing Allowance Reduction[3] (µm) [µin]	Minimum Surface Conductor Thickness after Processing (µm) [µin]	
					Class 1 & 2	Class 3
1/8 oz.	4.60 [181]	24.60 [967]	29.60 [1,165]	1.50 [59]	23.1 [909]	28.1 [1,106]
1/4 oz.	7.70 [303]	27.70 [1,091]	32.70 [1,287]	1.50 [59]	26.2 [1,031]	31.2 [1,228]
3/8 oz.	10.80 [425]	30.80 [1,213]	35.80 [1,409]	1.50 [59]	29.3 [1,154]	34.3 [1,350]
1/2 oz.	15.40 [606]	35.40 [1,394]	40.40 [1,591]	2.00 [79]	33.4 [1,315]	38.4 [1,512]
1 oz.	30.90 [1,217]	50.90 [2,004]	55.90 [2,201]	3.00 [118]	47.9 [1,886]	52.9 [2,083]
2 oz.	61.70 [2,429]	81.70 [3,217]	86.70 [3,413]	3.00 [118]	78.7 [3,098]	83.7 [3,295]
3 oz.	92.60 [3,646]	112.60 [4,433]	117.60 [4,630]	4.00 [157]	108.6 [4,276]	113.6 [4,472]
4 oz.	123.50 [4,862]	143.50 [5,650]	148.50 [5,846]	4.00 [157]	139.5 [5,492]	144.5 [5,689]

Note 1. Starting foil weight of design requirement per procurement documentation.
Note 2. Process allowance reduction does not allow for rework processes for weights below ½ oz. For ½ oz. and above, the process allowance reduction allows for one rework process.
Note 3. Reference: Min. Cu Plating Thickness
Class 1 = 20 µm [787 µin] Class 2 = 20 µm [787 µin] Class 3 = 25 µm [984 µin]

Table 1: External conductor thickness after plating, according to IPC-6012.

ness, and A-SAP starts with bare dielectric and adds 0.2 mm of thin electroless copper. Table 1 shows typical additive copper thicknesses after processing. These build up in a trapezoid formation depending upon the photoresist thicknesses. The A-SAP process does not build traces in a trapezoidal fashion.

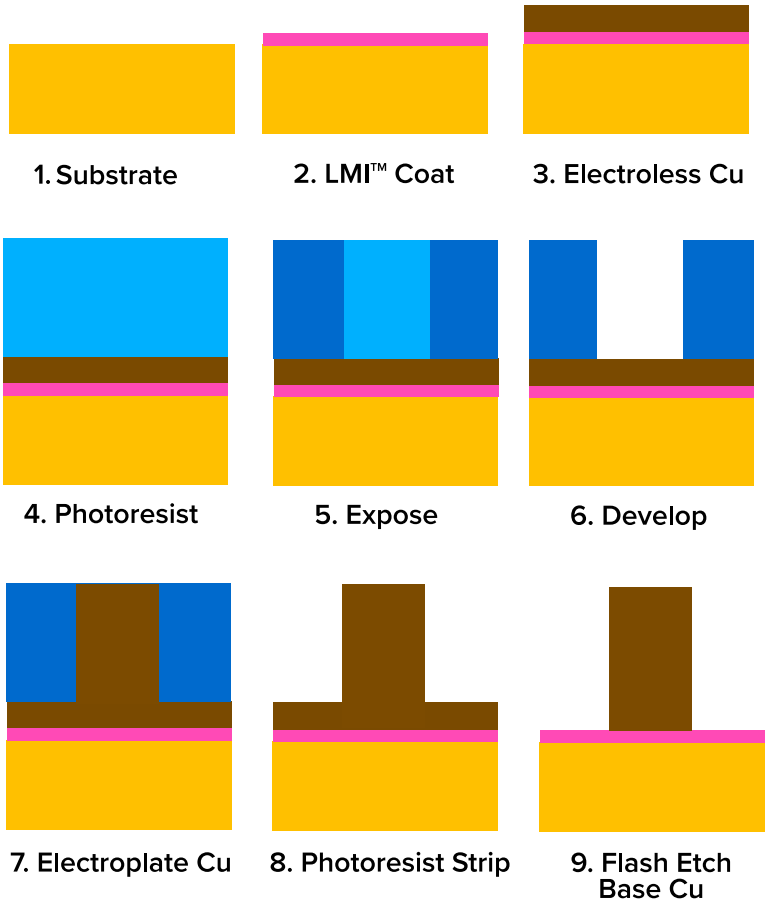

Figure 1: Liquid metal ink (LMI) can change your entire process flow. (Courtesy of Averatek Corporation)

The thicker the base copper, the more of a trapezoid shape you'll have to start with. Both can start with typical foil. When they do, mSAP usually starts with a thicker copper foil and A-SAP starts with a much thinner copper base. Averatek's Steve Iketani and Mike Vinson wrote an informative article on this topic in the July 2019 issue of *PCB007 Magazine*[1].

Optionally, both A-SAP and mSAP can use an additive process vs. a subtractive process at fabrication using LMI (liquid metal ink) for the starting copper thickness. When using LMI to apply the starting copper, as seen in Figure 1, the density at the interface with the laminate increases dramatically.

The process flow now becomes very different. So does the shape of my traces, the copper thickness and width. Figure 2 shows an example of what this looks like.

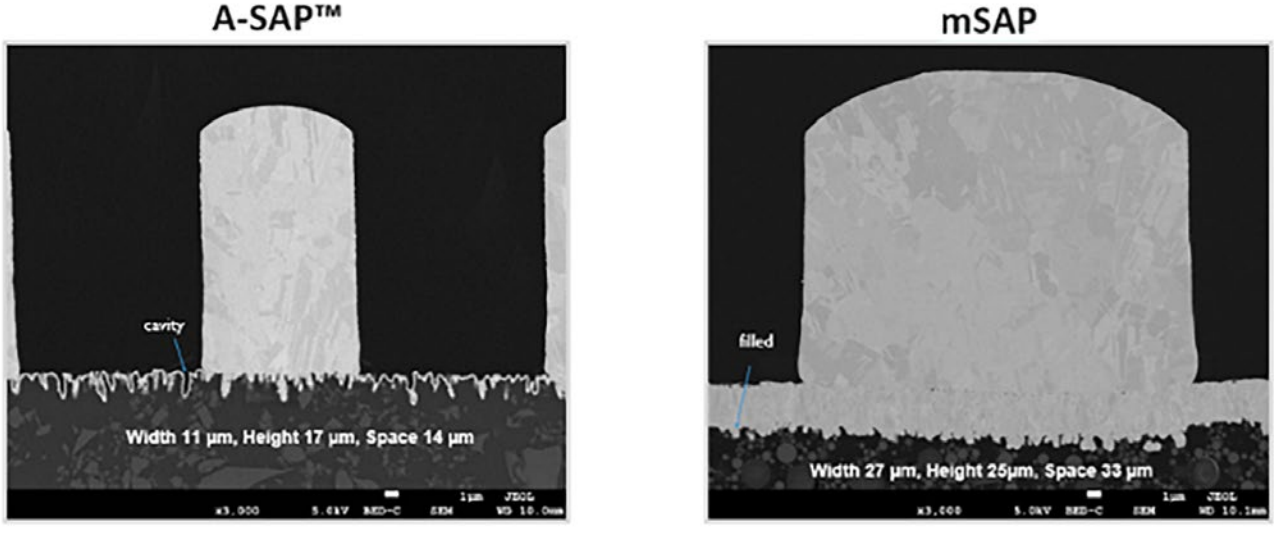

Figure 2: Examples of A-SAP and mSAP trace constructions. (Courtesy of Averatek Corporation)

Now, as a designer, I need to have some numbers. Plus, I have a lot of questions, as should you. On the following Q&A, you will find some questions that I ask at the beginning of each A-SAP or mSAP design.

Q: Do I need to do anything different with my output files to the fabricator to support this?

A: No. Fabricators use additive and subtractive processes all the time. You just need to know if they have the chemistry and experience working with mSAP and A-SAP processes.

Q: Do I need to have a special layer for SAP processes?

A: No. These processes can be constructed on outside and inside layers. Keeping them "balanced" (per good design practices) will certainly help keep costs down.

Q: Can I mix thicker traces with these thinner traces on the same layer?

A: Yes, but spacing is important here. It's a good idea to group these as much as possible to support the processes. Design rules are also very important.

Q: How will this affect my impedance values?

A: Fine traces affect impedance, but not as much as you might think. Eric Bogatin, Chaithra Suresh, Melinda Piket-May of the University of Colorado Boulder, and Haris Basit and Paul Dennig of Averatek have published a white paper[2] on the effects of using fine-line traces in HDI boards. Th ey explain it much better than I can, and I trust their analysis.

Q: Do I need to teardrop all pad entries?

A: Basically, I just have to route my designs as I normally would and consider the geometry stresses of using smaller traces as they go into solderable areas. Either teardrop or increase the trace size as it goes into a pad.

Read all you can about A-SAP and mSAP, and don't look back. Companies like Averatek have experts on hand, including Haris Basit, who will be speaking at the IPC Advanced Packaging Symposium in Washington, D.C., Oct. 11–12. Knowledge is power. **DESIGN007**

References

1. "SAP Utilizing Very Uniform Ultrathin Copper," by Steve Iketani and Mike Vinson, *PCB007 Magazine*, August 2019.
2. "Utilizing Fine Line PCBs with High Density BGAs," by Eric Bogatin, et al, *Signal Integrity Journal,* January 2022.

Cherie Litson, MIT/CID, CID+, is the founder of Litson1 Consulting and a master instructor at EPTAC.

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Routing Strategies to Minimize Radiation

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Electromagnetic (EM) energy propagates through the dielectric materials of a multilayer PCB guided by the signal traces between the planes, for inner stripline layers (Figure 1), but it acts slightly differently on the outer microstrip layers. Microstrip layers generally have a solid ground reference plane on one side but allow radiation from the boundless surface into the air. A well-thought-out routing strategy can avoid up to 10 dB of radiation from the substrate. Embedding signals between the planes reduces these emissions, and susceptibility to radiation, as well as providing electrostatic discharge protection. So, not only can one prevent noise from being radiated but also reduce the possibility of being affected by an external source.

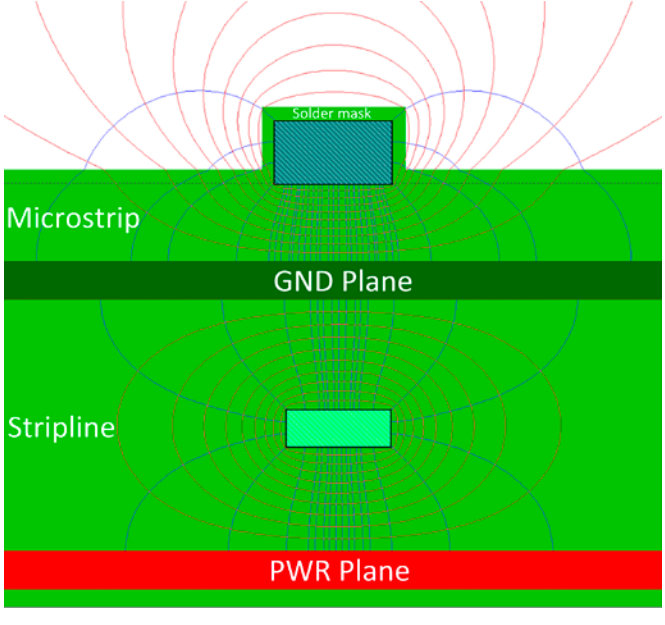

Figure 1: Microstrip EM fields (top) and stripline EM fields (bottom).

Studies conducted by Hewlett-Packard have found that there are up to 20 dB greater emissions from edge-located traces compared to traces located in the centre of the board on outer layers. Yet the same test performed on buried traces indicated no change as the traces were placed nearer the PCB edges. This implies that it is best to keep well away from the edge of the board when routing on the outer microstrip layers. The impedance changes as the reference plane decreases in the area beneath the trace.

On a multilayer PCB, critical signals should be routed on a stripline layer adjacent to a solid reference plane to reduce radiation. The spacing between the signal trace and the return plane should be as small as possible to increase coupling and reduce the loop area.

The three constraints to keep in mind:

- Keep the mark-to-space ratio of the waveform equal as this eliminates all the even harmonics.
- Route high-speed signals between the planes, fanout out close to the driver (200 mils) dropping to an inner layer, and route back up to the load again with a short fanout.
- Use the same reference plane (GND if possible) for the return signal, as this reduces the loop area and hence radiation.

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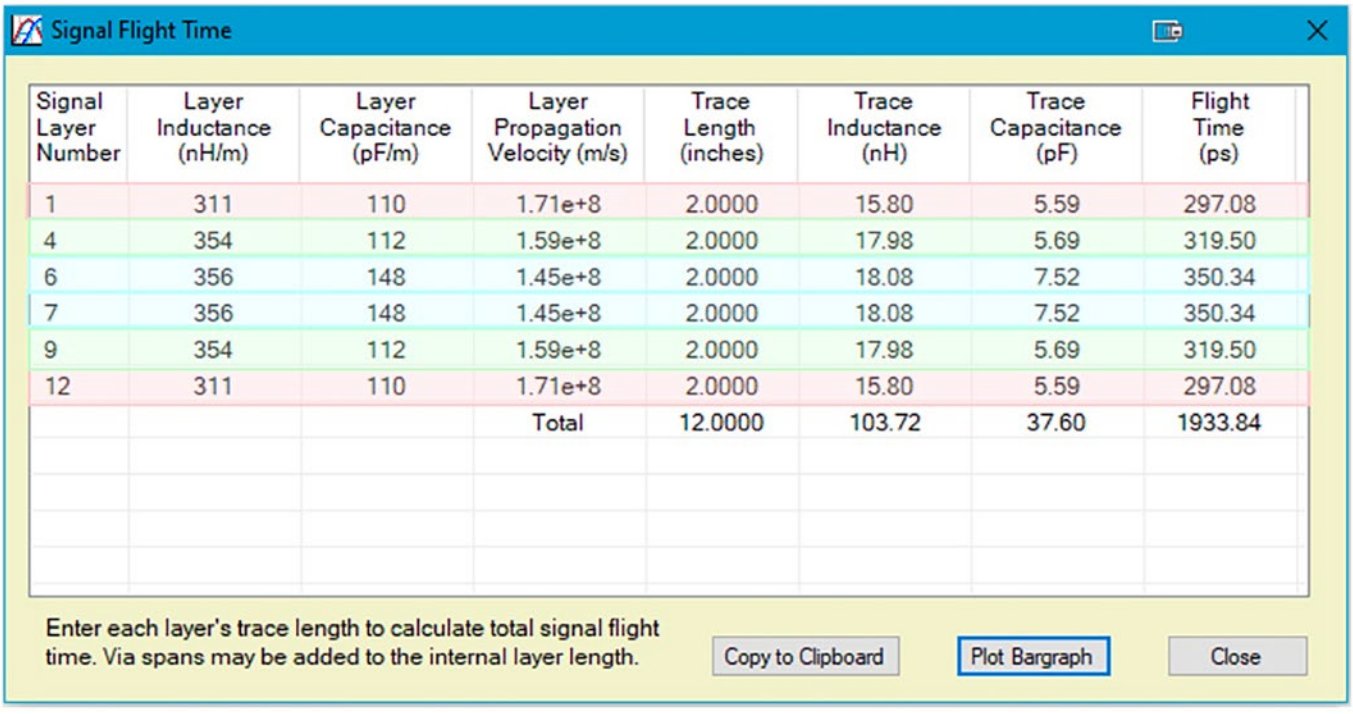

Figure 2: Relative signal propagation of microstrip and stripline (simulated in iCD Design Integrity).

The electric fields surrounding the microstrip exist partially within the dielectric material(s) and partially within the surrounding air. Since air has a dielectric constant (Dk) of one, it will speed up the signal propagation compared to the stripline. Even if the trace widths are adjusted on each layer, so as the impedance is identical, the propagation speed of microstrip is always faster than stripline—typically by 13-17%. The speed of propagation of digital signals is independent of trace geometry and impedance.

If you are aware of this issue, then the flight time (as shown in Figure 2) can be matched to compensate for the varying trace delays, so that at the nominal temperature, all signals running on either microstrip or stripline will arrive at the receiver simultaneously. Alternatively, many routers these days have matched delay routing which enables one to take the flight time variation between microstrip and stripline configurations into account. Note that matched delay is quite different from matched length routing which does not consider flight time.

For the DDR3/4 fly-by configuration, for instance, it is best to route all the critical traces on two symmetrical paired layers. In this case, the paired layers are 1 and 12, 4 and 9, plus 6 and 7. Layers 4 and 9 are best, as they are embedded and close to the plane pairs and active devices of a 12-layer PCB. There are 200-mil fanouts from the microstrip layer to these (not shown). These two layers have identical delays of 319.50 ps and are symmetrical in the stackup embedded between planes. Figure 3 shows the routing directions of the data lanes (0-3) combined with the associated differential strobes and the address, control and command (ACC) signals combined with the differential clock. One does not need to worry about layer-induced flight time skew because layers 4 and 9 are identical.

Figure 4 graphs the relative radiation between outer and inner layers. In this case, the trace routed on the inner layer 4 exhibits between 4 to 10 dB less noise than the trace routed on the top layer. Note that there are radiating harmonics above 40 dB on the top layer routing. Also, high frequency components radiate more

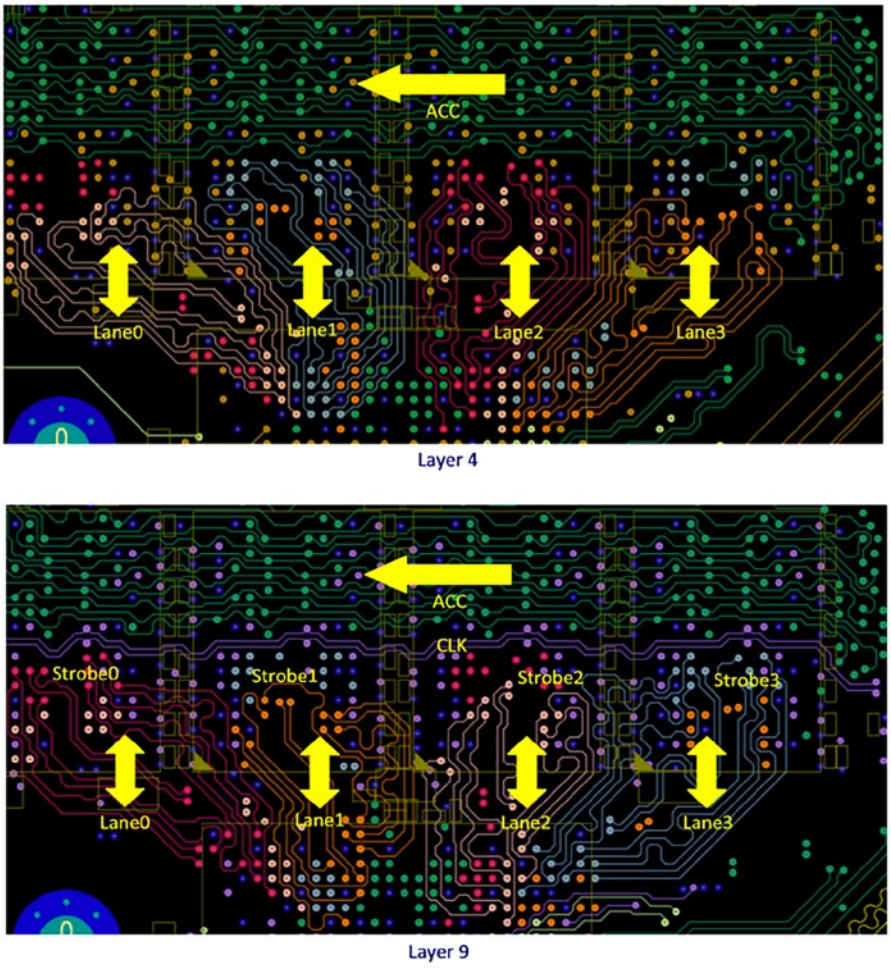

Figure 3: Routing strategy for DDR3 fly-by configuration.

readily because their shorter wavelengths are comparable to trace lengths, which act as antennas. Consequently, although the amplitude of the harmonic frequency components decreases, as the frequency increases, the radiated frequency varies depending on the trace characteristics.

So, apart from the short 200-mil microstrip fanouts, the emissions of this design are well below that of the FCC/CISPR Class B limit (lower red line). Whereas, the radiation would have been 49.73 dB at 6.76 GHz and 52.10 at 7.8 GHz if it was routed on the outer layers, possibly failing testing. If you plan your routing strategy and stackup design prior to commencing the layout, then design for electromagnetic compliance takes very little extra effort.

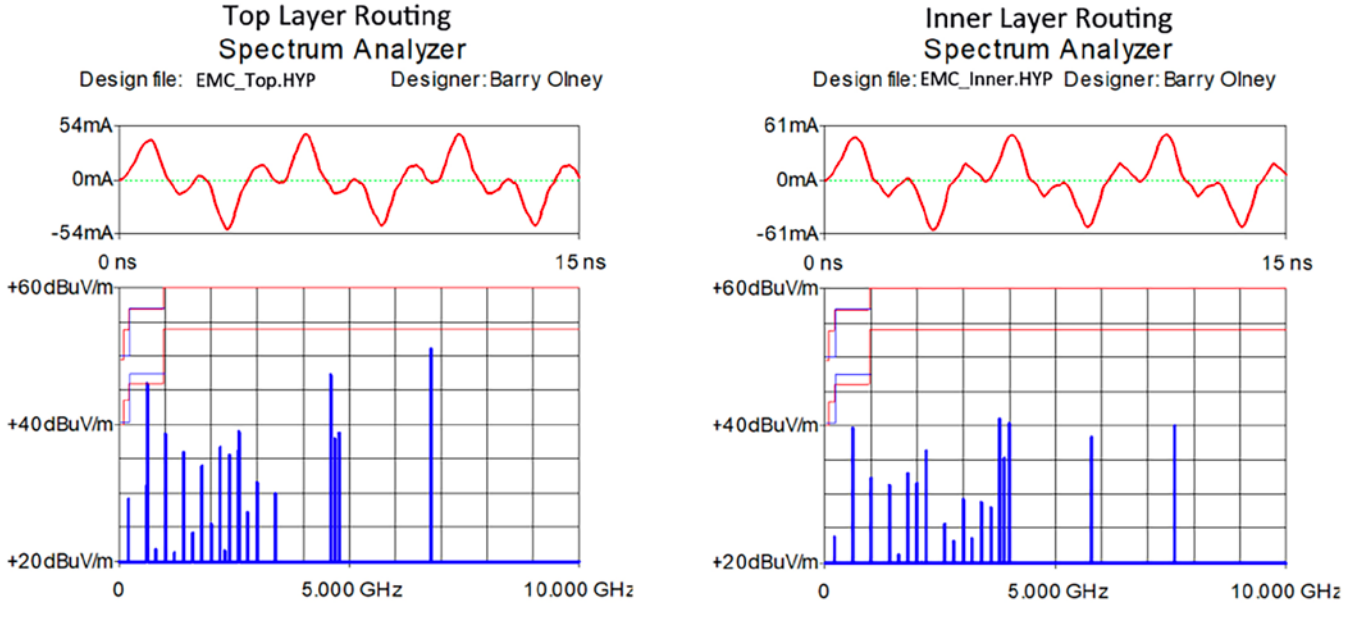

Figure 4: Comparison of radiation from signals routed on the top microstrip layer vs. inner stripline layer.

Key Points

- Embedding signals between the planes reduces these emissions and susceptibility to radiation as well as providing electrostatic discharge protection.
- It is best to keep well away from the edge of the board when routing on the outer microstrip layers.
- On a multilayer PCB, critical signals should be routed on a stripline layer adjacent to a solid reference plane to reduce radiation.
- The propagation speed of microstrip is always faster than stripline—typically by 13-17%.
- Many routers these days have matched delay routing which enables one to take the flight time variation into account.
- The trace routed on the inner layer 4 exhibits between 4 to 10 dB less noise than the trace routed on the top layer.

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Resources

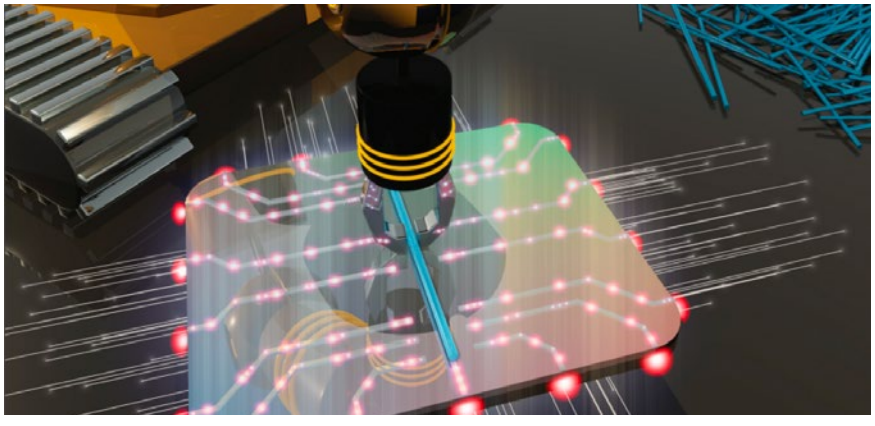
1. Beyond Design by Barry Olney: The Fundamental Rules of High-Speed PCB Design Part 4; Embedded Signal Routing; Signal Flight Time Variance in Multilayer PCBs.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns, click here.

Discovery of New Nanonwire Assembly Process Could Enable More Powerful Computer Chips

In a newly-published study, a team of researchers in Oxford University's Department of Materials led by Harish Bhaskaran, Professor of Applied Nanomaterials, describe a breakthrough approach to pick up single nanowires from the growth substrate and place them on virtually any platform with submicron accuracy.

This technique is readily scalable to larger areas, and brings the promise of nanowires to devices made on any substrate and using any process. This is what makes this technique so powerful.



The innovative method uses novel tools, including ultra-thin filaments of polyethylene terephthalate (PET) with tapered nanoscale tips that are used to pick up individual nanowires. At this fine scale, adhesive van der Waals forces (tiny forces of attraction that occur between atoms and molecules) cause the nanowires to "jump" into contact with the tips. The nanowires are then transferred to a transparent dome-shaped elastic stamp mounted on a glass slide. This stamp is then turned upside down and aligned with the device chip, with the nanowire then printed gently onto the surface.

Deposited nanowires showed strong adhesive qualities, remaining in place even when the device was immersed in liquid. The research team were also able to place nanowires on fragile substrates, such as ultra-thin 50 nanometre membranes, demonstrating the delicacy and versatility of the stamping technique.

(Source: University of Oxford)

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The Learning Curve for Ultra HDI

Feature Q&A With Tara Dunn

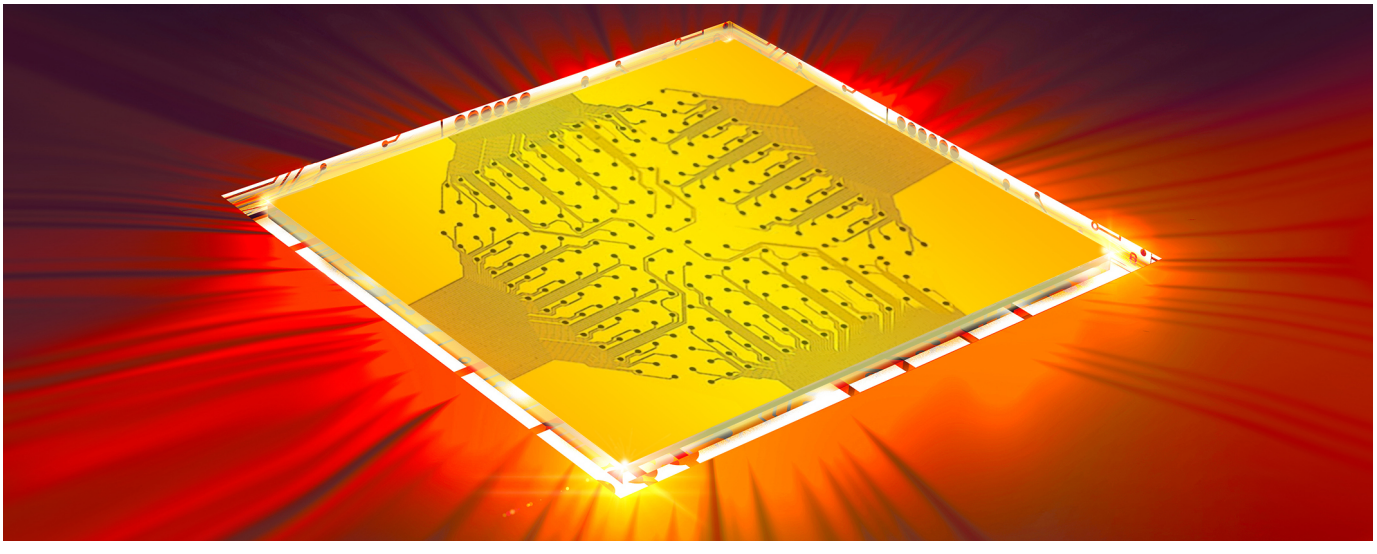
For this issue on ultra HDI, we reached out to Tara Dunn at Averatek with some specific questions about how she defines UDHI, more about the company's patented semi-additive process, and what really sets ultra HDI apart from everything else. Do designers want to learn a new technology? What about fabricators? We hope this interview answers some of those questions that you may be having about these capabilities and what it could mean for your designs.

Q: How do you define ultra HDI? What is the cutoff in mils or microns?

A: That is an excellent question. At this point I think it means different things to different people depending on where their current "HDI" capabilities are. IPC has created an ultra-HDI working group and I believe the definition they are working with is that to be considered ultra-HDI, a design needs to include one or more of these parameters: Line width below 50 µm, spacing below 50 µm, dielectric thickness below 50 µm, and microvia diameter below 75 µm.

Q: Averatek has developed the A-SAP™ semi-additive process, which can produce traces down into the UHDI space. Can you clear up the differences between mSAP and A-SAP, and what this means to designers and design engineers?

A: In general, SAP, or a semi-additive process, is a process that starts with a very thin layer of copper and then builds the trace patterns from there. One common differentiating factor in these two approaches to SAP is the starting copper thickness. Typically, copper thickness that is 1.5 microns or above would be considered mSAP, or a modified semi-additive process. Because the copper is a little thicker than other SAP processes, it requires more etching, which can have impacts on trace width and space and also the sidewalls of the trace. This



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process can typically provide features as small as 30 microns in highly specialized facilities that are running extremely high-volume manufacturing. This technology is commonly seen in our smartphones.

Averatek's A-SAP begins with a much thinner electroless copper, typically 0.2 micron and this copper thickness, or thinness if you will, enables the fabricator to produce much finer feature sizes. The technology is capable of traces and spaces as small as 1 micron if the fabricator has advanced imaging equipment. Typically, PCB fabricators have equipment that can image traces to 12.5 µm today. There are also signal integrity benefits to this process. Because the base copper is so thin, there is minimal impact on the trace sidewalls, and greater control to line width resulting in impedance control tolerance improvements.

One other difference between the mSAP and A-SAP technologies is in the ratio of trace height to trace width. mSAP processes allow a 1:1 ratio of height to width and A-SAP traces can be produced with aspect ratio of 2:1 or greater. For example, a 25-micron wide trace could be 40 microns tall. This has gotten a lot of attention from a signal integrity perspective.

Q: How is designing in the ultra-HDI arena different from designing a typical PCB, or even an HDI board?

A: I sometimes worry that designers will think they must learn a whole new way to design if they want to work with ultra HDI designs. I believe it is not that different than when a designer first learns to design with flex materials. Most things are the same as designing with rigid and once you learn the specific items that are different and why, designing with a new technology becomes much easier.

That said, this does give the industry the opportunity to reimagine how PCB design is done. In general, the constraints have been at 75-micron line and space for so long that, collectively, we have learned to work around that with blind and buried vias, stacked and staggered microvias, an increasing number of lamination cycles to create enough space to route out tight pitch BGAs, etc. The SAP processes and finer line widths can free up valuable real estate and help to simplify the design and reset the technology curve.

There are a couple of different ways to approach a design with ultra HDI and I think the approach varies according to a designer's particular priorities. For some, the priority is overall miniaturization, which may be in size, or overall thickness. For others, a top priority is via reliability and the focus is on reducing lamination cycles or even using space to increase hole size and move from an HDI construction to a through-via construction.

Circling back to the flex comparison, I want to be sure to mention that SAP processes can be built with a variety of materials including flexible materials and that not all layers in a PCB design need to be done with SAP. It is a layer-by-layer selection, and it is common that power and ground layers, or any layer with only 75 micron or greater feature sizes will be built with subtractive etch process.

Q: What are some of the benefits of UHDI?

A: I think the primary benefits are:

- **Dramatic size and weight reduction over current subtractive etch processing.** PCBs can be made much smaller and thinner.
- **Improved reliability:** This could be from reduced layer count, reduced lamination cycles, reduced dependence on microvias, etc.
- **Improved signal integrity:** As I mentioned, higher aspect ratio of height to width, which opens up several things to PCB designers, and tighter control on feature sizes improves impedance control.
- **Reduced costs:** This one may seem coun-

terintuitive, but it is rare that costs are compared as apples to apples. I often see designs reduce layer count, reduce laminations, and shrink overall size. All these things simplify the design, improve yield, and reduce costs.

- **Biocompatibility:** I don't think I mentioned earlier, but the A-SAP process begins by completely removing the copper foil and a thin layer of electroless copper is added to the dielectric. But this process is not limited to only copper. I have seen several applications where gold and platinum are used as the conductive metal. This, done with polyimide or LCP, provides a much more biocompatible solution for medical applications.

Q: What are some of the hurdles facing designers—and fabricators—who work on UHDI boards?

A: In my mind, the biggest hurdle is the learning curve that both designers and fabricators need to go through. Fabricators are learning a new process, and while that process of creating the traces is not difficult, it does need to mesh with other processes. For example, what is the new process for via-in-pad-plated over or what thickness of copper can be plated in the hole? There may be different approaches based on customer design. Fabricators are well-versed in using various techniques to meet customer needs and this is no different, but it does require thought and experience.

From a design perspective, as we mentioned earlier, there are a lot of questions. How do you design with controlled impedance at these fine lines? There are white papers, by the way, to help with that. What materials are compatible with this process? Where does it make sense to use subtractive etch vs. SAP layers? Is there reliability data? These are a few of the common initial questions.

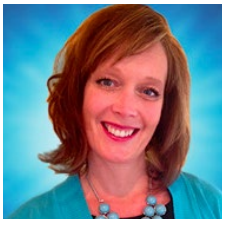
Q: Are there any resources—books, websites, instructors, etc.—for UHDI design techniques? I imagine people are coming to Averatek with questions.

A: Yes, we do field a number of questions, which is one of the best parts of my role at Averatek, and along with the work we are doing, we are also working with a number of PCB designers who are interested in really understanding how to apply these fine features. These designers are starting education programs, writing papers, presenting at conferences, and are available to assist as others go through this learning curve.

A good place to start is the Info Center on Averatek's website, where we have compiled a number of white papers and articles addressing the subject. I also believe most of the PCB-focused trade shows are now offering tracks about SAP and I have seen several webinars available as well, both from fabricators and from equipment suppliers such as Orbotech.

Q: What advice would you give designers who are considering moving into UHDI?

A: It is the same advice I give to anyone new to designing with HDI, new to designing with flex or rigid-flex, and now new to designing with ultra HDI: Work closely with your fabricator. Learn to understand their capabilities and let them help guide you through the design. They have the experience of building many designs with these technologies and are always happy to help PCB designers design a manufacturable part. **DESIGN007**



Tara Dunn is the vice president of marketing and business development for Averatek and an I-Connect007 columnist. To read past columns, click here.

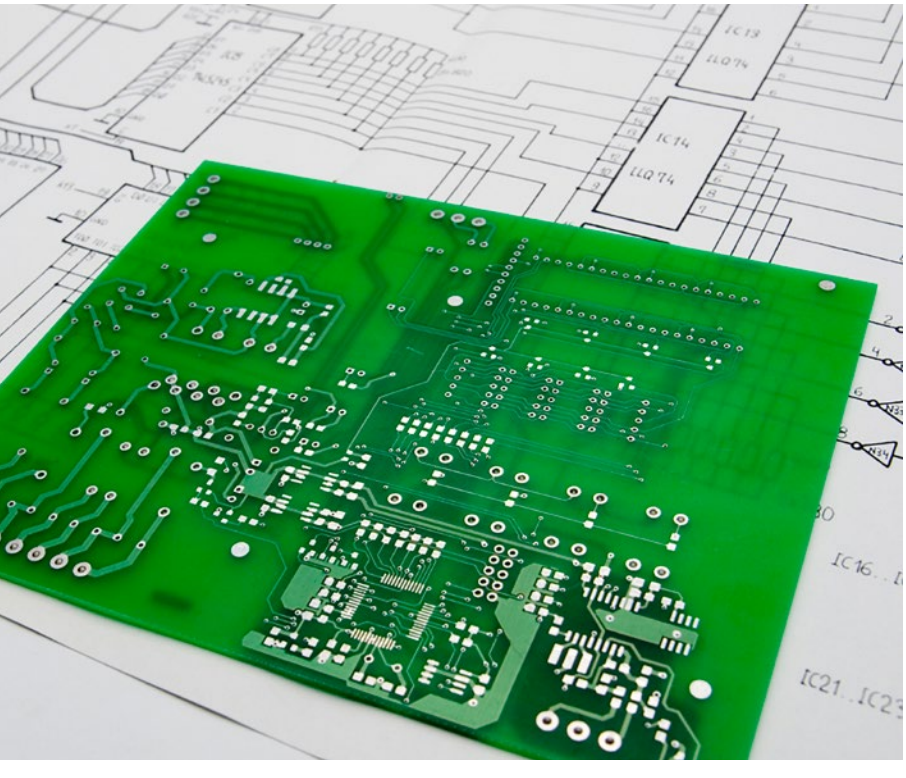
The ABCs of Clean Schematics

Connect the Dots

by **Matt Stevenson,** SUNSTONE CIRCUITS

The production team is always excited when the first shipment of boards for a new electronic device comes back from the PCB manufacturer. Anticipation builds as the engineer connects the first set of components, puts everything together, and gets ready for that first test.

But when something goes wrong—a tiny pop, a sizzle, a puff of smoke, or nothing happens at all—the mood can turn from excitement to frustration. The engineer performs a postmortem and discovers a pinhole melted into the integrated circuit (IC), and then the culprit (a missing decoupling capacitor) led to a completely predictable voltage spike.



Where did the process go wrong? The engineer is certain that they put the capacitor in the right place. However, on closer examination, perhaps it is not close enough to the IC pad. Is it the fault of the PCB designer? Chances are that the designer will claim that they put the capacitor right where the schematic said it should be.

In a case like this, the fix is easy. The designer and the engineer get on the same page and produce a new design in 15 minutes. Unfortunately, the current batch of boards is now only useful as a set of coasters—delaying the project and potentially creating budget overruns.

This is a common issue for electronics manufacturers, and it is completely avoidable.

Good Schematics Are Good Communication

When engineers start to put together projects, the schematics are vital to good communication with the PCB designer. Theirs is a team effort. The schematic is where the engineer thinks through the project. However, by the time they hand it off to the designer, it needs to be a clean, comprehensible document that isn't vague and doesn't confuse. Most importantly, the engineer needs to communicate everything the PCB designer needs to design the right board for the project.

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Best Practices Are There for a Reason

We all know that best practices exist, but real-world circumstances often lead to cutting corners. Saving time by ignoring best practices—like performing one last design check before submitting to the manufacturer—is just going to cost more time and money later. Even though it seems exhausting and repetitive, best practices involve starting at high-altitude block diagrams and then breaking each block into schematic sheets, checking flow and accuracy carefully, and then finally designing the board.

After that, a best practice has the engineer and designer picking over the design carefully, ensuring that it matches the specs—before it goes to the PCB manufacturer.

Designers Will Do What You Tell Them to Do

Engineers need to remember that designers don't read minds; they read schematics. The engineer may understand implicitly the locations for all their bypass capacitors, but they can't rely on the designer's interpretation to properly place the elements. Instead, locate devices in roughly the manner of the final design to help the designer avoid bad interconnects, placement assumptions, or other errors.

It never hurts to provide the designer with explanatory notes about the elements. You will never hear a designer say that the engineer provided too much guidance for their work.

For example, utilize good naming conventions for connections or net names. Automated labels from design software are rarely helpful or intuitive. Create labels a human can understand.

Leverage Your Tools, But Don't Use Them as a Crutch

Sometimes, engineers will give implicit connections using port symbols for the entire schematic. Unfortunately, this practice leaves no trail for the designer to follow. While the engineer may have saved a couple of minutes, the designer spends more time sorting out the nest of connections.

Let the software be on your side. It tracks and confirms those connections for a reason. This may feel like an obstacle for the engineer, but for the overall project, these tools are a lifeline.

The design rule check (DRC) is another example where the tool exists, but results may get ignored in the interest of saving some time. Too often, issues are ignored because they seem unimportant. However, over time these errors build up and create a confusing mess that may obscure errors that are truly important. One of your team's best practices should be generating a DRC report that reads no warnings and no violations.

More Recommendations for Clean Schematics

In addition to the broader best practices of fostering good communication and not relying too much on technology, the following are key methods that help ensure a clean schematic and a manufacturable, functional PCB design.

- Design the schematic in the design program and label all connects with comprehensible net names—no auto-generated names
- Lay out the schematic in a manner that clarifies locations

- Label the schematic so that the next person can understand it
- Create an environment where designers are comfortable asking for clarification if they are uncertain how to proceed
- Use the DRC and address the warnings and violations it reports

Well-designed schematics will save time, money, and frustration both for your current project and future endeavors. If your schematic is nice to look at and easy to understand, your team can utilize blocks for other similar projects down the road. Teams that commit to good schematic practices win the long game.

Commit to Best Practices and Good Process

We all want to create great final products. Designers want to make great boards. Engineers want to make great schematics. To get there, we also need to think about making the work of the next person easier. When you commit to best practices, clear communication, and clean schematics, everyone benefits. **DESIGN007**

Matt Stevenson is the VP of sales and marketing at Sunstone Circuits. To read past columns or contact Stevenson, click here.

A World First: Self-calibrated Photonic IC:

New Interchange for Optical Data Superhighways

Research led by Monash and RMIT Universities in Melbourne has found a way to create an advanced photonic integrated circuit that builds bridges between data superhighways, revolutionising the connectivity of current optical chips and replacing bulky 3D-optics with a wafer-thin slice of silicon.

This development, published in the prestigious journal Nature Photonics, has the ability to warp-speed the global advancement of artificial intelligence and offers significant real-world applications such as:

- Safer driverless cars capable of instantly interpreting their surroundings
- Enabling AI to more rapidly diagnose medical conditions
- Making natural language processing even faster for apps such as Google Homes, Alexa and Siri.
- Smaller switches for reconfiguring optical networks that carry our internet to get data where it's needed faster

Whether it's turning on a TV or keeping a satellite on course, photonics (the science of light) is transforming the way we live. The photonic chips can transform the processing capability of bulky bench sized utilities onto fingernail sized chips.

The project's lead investigator says this breakthrough complements the previous discovery of Monash University's Dr. Bill Corcoran who, in partnership with RMIT in 2020, developed a new optical microcomb chip that can squeeze three times the traffic of the entire NBN through a single optical fibre, regarded as the world's fastest internet speed from a single fingernail-sized chip.

The optical microcomb chip built multiple lanes of the superhighway, now the self-calibrating chip has created the on and off ramps and bridges that connect them all and allow greater movement of data.

(Source: Monash University)

MilAero007 Highlights

Will Marsh: CHIPS Act Update ▸

Nolan Johnson reconnects with PCBAA President Will Marsh, who brings him up to speed on the initial stages of implementation and administration, and provides more insight on the Supporting American Printed Circuit Boards Act of 2022.

A Deeper Look at the CHIPS Act Investment ▸

In this interview with Chris Peters at U.S. Partnership for Assured Electronics (USPAE), Nolan Johnson seeks for better understanding regarding the implications of funding the CHIPS Act. Frankly, where and how will the $52 billion be spent? Who will decide how the funds are allocated?

North American PCB Industry Sales Up 15.1% in August ▸

IPC announced the August 2022 findings from its North American Printed Circuit Board (PCB) Statistical Program. The book-to-bill ratio stands at 0.98.

IPC APEX EXPO 2023 Offers New Courses, New Instructors, and IPC E-Textiles ▸

Registration is now open for IPC APEX EXPO 2023, to be held at the San Diego Convention Center in San Diego, Calif., Jan. 21–26, 2023.

Boeing Invests $5M in Advanced Manufacturing Innovation Center ▸

Boeing announced it is investing $5 million to help expand the Advanced Manufacturing Innovation Center in St. Louis. The investment will help fund a state-of-the-art advanced manufacturing facility and grow the region's talent pipeline and technical and manufacturing abilities.

Electronics Industry Calls for U.S. Presidential Determination on Key Components Under Defense Production Act ▸

The electronics industry is calling on U.S. President Joe Biden to address urgent industrial base vulnerabilities and deliver on the promise of the CHIPS Act by prioritizing domestic development of printed circuit boards and integrated circuit substrates under Title III of the Defense Production Act.

Designing Through Supply Chain Pain ▸

Engineers are accustomed to the demanding challenges of designing for miniaturization, cost reduction, cross platform compatibility, and harsh environments. What has proven to be the most painful experience of my career (and for many of my colleagues) is the sheer lack of components from which to build our designs.

CAES Wins Contracts for Development of Next-Generation, Octa-Core, User-Selectable CPU for Space ▸

CAES, a leader in advanced mission-critical electronics for aerospace and defence, announced that it has won multiple contracts with the European Space Agency (ESA) for the development of the GR765 System-on-Chip (SOC), the first user selectable CPU for space.

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Ultra High Density Circuit Board Design

Designers Notebook

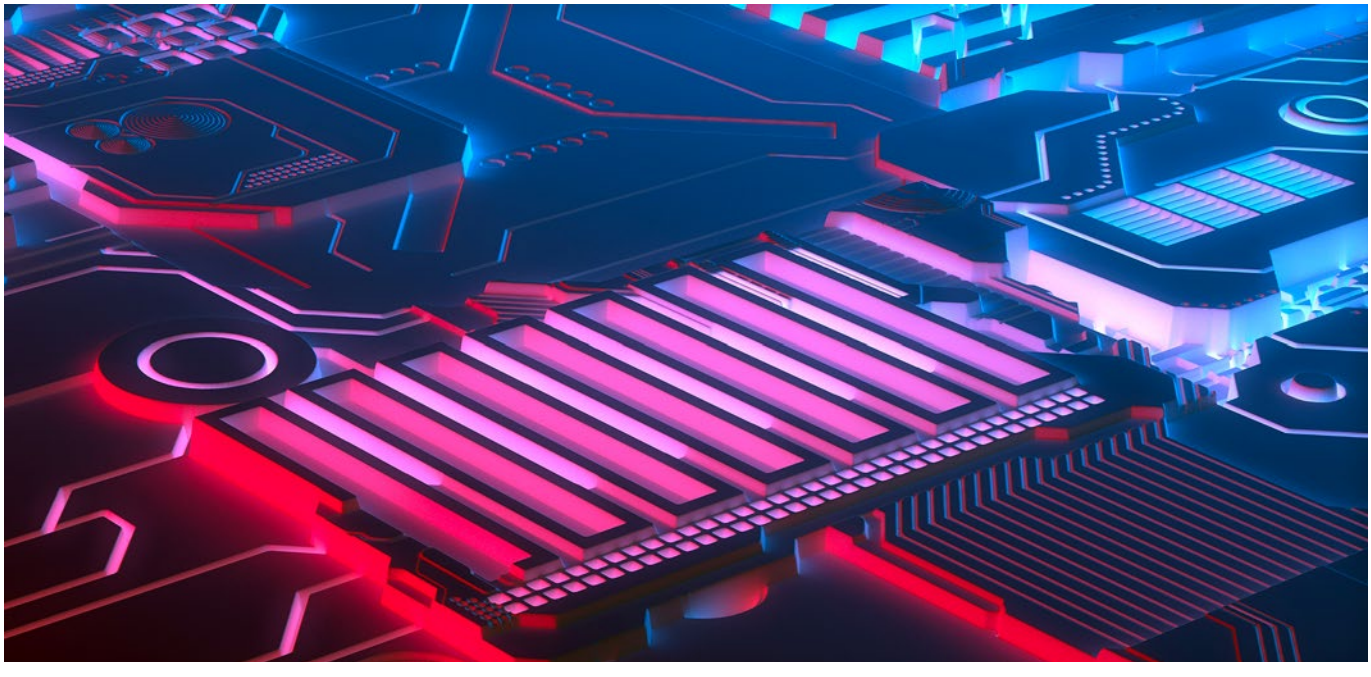
Feature Column by Vern Solberg, CONSULTANT

To facilitate new generations of high I/O semiconductor packaging, circuit board technology is undergoing significant refinement in both fabrication process methods and base materials selected. Many of the new high-function semiconductor package families require significantly more terminals than their predecessors. Interconnecting these very fine-pitch, high I/O semiconductors can dramatically affect the procedures used in both circuit board design and assembly processing.

When defining the complexity level for the HDI circuit, the designer will first establish a criterion for fabricating the circuit board. This will include the board outline, thickness limitation, and any special features required for the end product. A clear objective will be established to identify the maximum number of circuit layers that are to be dedicated to signal routing and the number of layers reserved for power and ground distribution. Establishing the required number of signal layers will be determined by the overall component density and interconnect complexity.

Interconnect Capacity Analysis

This analysis is based on the board's usable area. To determine the basic component area, the designer will first compile the mechanical outline specifications and electrical data for both active and passive components. Minimum clearances for assembly processing and in-process inspection must be considered as well as the spacing reserved for surface circuit



PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

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interconnect. From this data, the designer can assign the associated land pattern geometries and the pad-stack pre-established in the CAD systems library. For those components without existing pad-stack data, the manufacturer's mechanical and electrical data must be collected to enable the creation of new parts in the systems library.

While a significant number of semiconductor packages will have a moderate level of complexity (I/O and terminal pitch), others may have an excessively high I/O density. When assessing the PCB design complexity, first consider the component area to board area ratio. For example, the "standard" level of complexity will represent what the individual fabricators recommend for the highest yield and most favorable unit quality. When component density and area reserved for interconnect exceed the space defined by the circuit board outline and established maximum layer count, designers will need to migrate to a higher level of fabrication technology. The interconnect complexity may necessitate more circuit layers or an increase in interconnect density. Two fabrication methods can be applied when the surface area for component interface is restricted: adding additional layers to the core or base structure (increasing overall board thickness) or adopting sequential build-up (SBU) PCB fabrication.

The interconnect complexity may necessitate more circuit layers or an increase in interconnect density.

Advances in Circuit Fabrication Capability

Printed circuit board fabrication process capabilities have continued to expand on a global scale. Fabrication process capability from one supplier to another, however, is not likely to be equal. This is because of the continuous advancement in related chemistries, processing systems, materials, and overall process control. Ensuring the success of the end-product functionality requires an understanding of the selected fabricator's primary capability attributes and how greater design complexity will affect the PCB producibility and cost. To ensure a successful outcome for the HDI circuit board, it is important that the designer recognize the manufacturing process complexities and associated cost impact when implementing more advanced fabrication procedures.

While a majority of the components will require a relatively moderate circuit interconnect density, the high I/O array-configured components will pose the most challenging aspect of the circuit routing process. Narrow conductors routed in parallel will generally have a conductor separation that is equal to the conductors' width. The spacing separating the circuit conductors must also consider the established minimum electrical clearance required for fabrication process variables, solder-mask adhesion, land pattern features, via land patterns, and other fixed elements on the board.

One answer for solving conductor routing roadblocks is to adopt blind via-in-land techniques to transfer a majority of the interconnect responsibility to the circuit boards' sub-surface layers. Adapting blind and buried microvias and furnishing pre-defined routing channels will best facilitate efficient routing of these often very fine-pitch and array terminal configured semiconductor packages. When establishing copper conductor width and spacing of the circuit, the IPC-2226, for example, defines three HDI complexity levels for both external and internal locations. A relatively few companies can produce Cu conductors as narrow as 25 µm (~0.001") but they likely rely on using dielectric materials that have a very

Table 1: Comparing HDI fabrication process variations

Fabrication Process	Copper Thickness Int.	Ext.	Conductor Width Int.	Ext.	Conductor Spacing Int.	Ext.
Subtractive: Image and Etch	9µm (0.25 oz.)	18µm (0.50 oz.)	45µm (.0018")	50µm (.002")	45µm (.0018")	50µm (.002")
Semi-Additive: Cu build-up	4.5µm. (0.12 oz.)	9µm (0.25 oz.)	18µm. (.0007")	37µm (.0015")	18µm. (.0007")	37µm (.0015")
Fully Additive: Cu deposition	0.1µm – 10µm (.00004" – .0004")		12µm (.0005")	25µm (.001")	12µm (.0005")	25µm (.001")

thin Cu foil or use base materials prepared for a semi-additive Cu plating process. When conductor lines and spaces must be reduced further, the fabricator will utilize base materials prepared for a semi-additive or primed for a fully additive copper plating process. Examples shown in Table 1 compare general process capability for subtractive, semi-additive, and fully additive copper deposition and micro-via hole-forming variations.

Electrical interconnect on internal layers for the board enables significantly greater circuit routing density. The circuit path between key components can be more direct as well, providing greater circuit speed and lower resistance. To ensure the greatest interconnect efficiency, the designer should alternate the overall direction of the circuit path from one layer to another, using plated via holes to accommodate direction change as needed. With the circuit width and space requirement already established in the CAD system, the auto router function can quickly complete the initial interconnect process. Exhibited in Table 2 are three levels of HDI PCB conductor routing complexities.

High-Density Circuit Fabrication Solutions

For many applications, the cost of high-density printed circuit boards has remained a detractor. Although PCB complexity has increased, the prices for HDI have declined and analysts expect this trend to continue to decline further each year. This is due in part to increased competitive conditions, but we can also attribute the trend to diligence in refining fabrication process control methods and con-

Table 2: HDI conductor routing complexity levels

Aspect Ratio	Level A	Level B	Level C
Internal conductor width	127µm (~.005")	75µm (~.003")	50µm (~.002")
Internal conductor spacing	127µm (~.005")	100µm (~.004")	50µm (~.002")
External conductor width	127µm (~.005")	75µm (~.003")	25µm (~.001")
External conductor spacing	127µm (~.005")	100µm (~.004")	25µm (~.001")

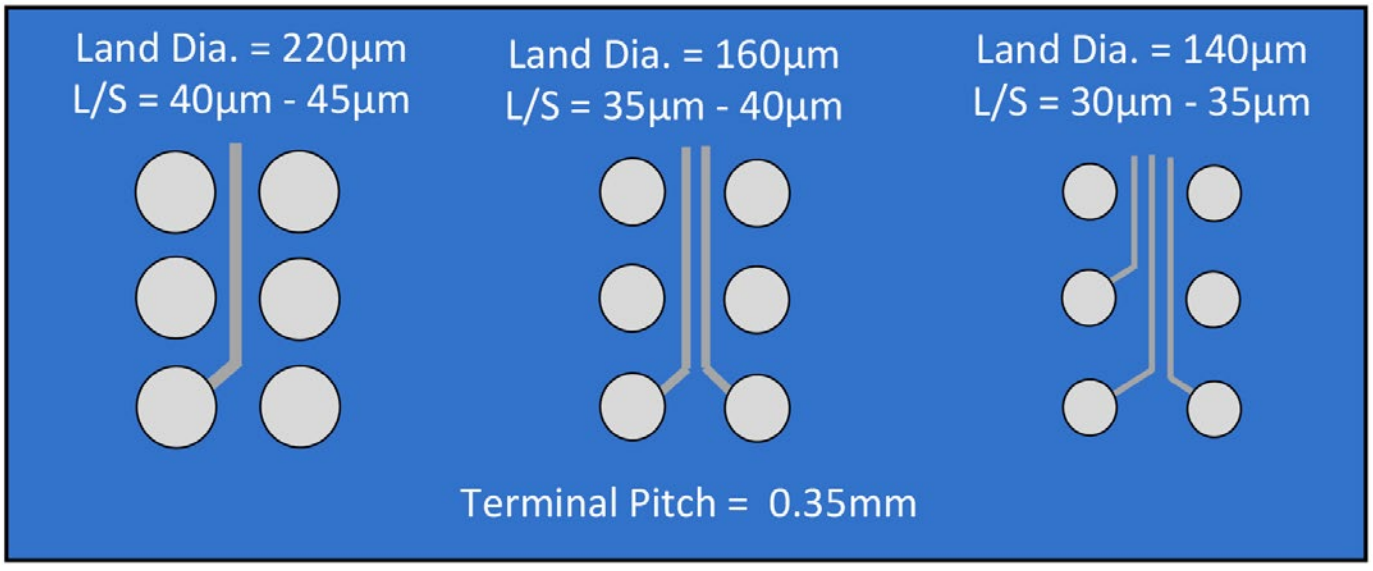

Figure 1: Planning escape routing for very fine-pitch array components.

trolling material utilization. The examples in Figure 1 compare circuit escape routing capability for very-fine-pitch BGA.

Process refinement for the ultra high-density circuit includes more efficient imaging capability and greater utilization of alternative hole-forming techniques, advances in etching and plating chemistry, and refinement in base materials and lamination methods. A key contributor to enabling higher density circuits is in the advances made in imaging. Laser direct imaging (LDI) and diode imaging systems have become mainstream technology for a wide segment of the PCB fabrication industry. Where circuit pattern imaging relied on first photoplotting the circuit pattern onto film-based masters and using contact printing to transfer the image to the etch resist coating on the copper-clad panel surface, fabricators have streamlined their processes with transferring the image directly from the CAD file onto the panel's resist coating. Direct imaging eliminates the effect of contact film stability and improves layer-to-layer registration capability.

Before committing to adopting any level of UHDI technology, however, the designer should take the time to consult with the designated PCB supplier(s) selected to validate their capability to furnish the required complexity level at the expected production quantity. Many users have already established a business relationship with key pre-qualified suppliers that have demonstrated their level of expertise and proficiency. These suppliers can be the designer's best source for evaluating the design before manufacturing, often suggesting refinements that will affect both cost and reliability of the finished product.

Note: The feature size dimensions furnished in the above tables may be beyond the process capability of many printed circuit board fabricators. To minimize production delays, review the selected fabricators' design rules before initiating the HDI or UHDI project. **DESIGN007**

Vern Solberg is an independent technical consultant, specializing in SMT and microelectronics design and manufacturing technology. To read past columns, click here.

PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

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Forming Standards for Ultra HDI

Feature Q&A with Jan Pedersen
NCAB GROUP

To get the latest news about ultra high-density interconnections (UHDI), we checked in with Jan Pedersen, NCAB Group's director of technology. Jan is co-chair of IPC D-33-AP Subcommittee, and a great source of overall DFM expertise as well. We asked him to give us a snapshot of UHDI in the industry, where we're headed, and what this means to PCB designers.

Q: How do you define ultra HDI? What is the cutoff in mils or microns?

A: UHDI is defined in the IPC UHDI task group as a PCB design with lines and spaces below 50 microns, dielectric thickness below 50 microns, and microvias below 75 microns. These are attributes beyond the existing IPC-2226 Producibility level C.

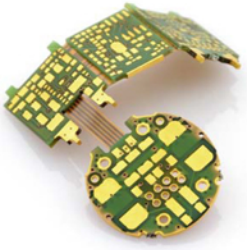
Q: Tell us about your work on IPC's UHDI committee. What are you working on right now? Are the standards keeping up with UHDI technology?

A: The UHDI task group has now developed a basic description and parameters. We are ready to hand over our work to the next group at IPC to start building the standards structure, starting with design, followed by performance and acceptance standards.

The standards will keep up with UHDI technology, but this will need our full attention for the standard to reflect current production capabilities globally.

Q: Much of the ultra HDI we see involves semi-additive technology. Can you clear up the dif-

Focused on Flex



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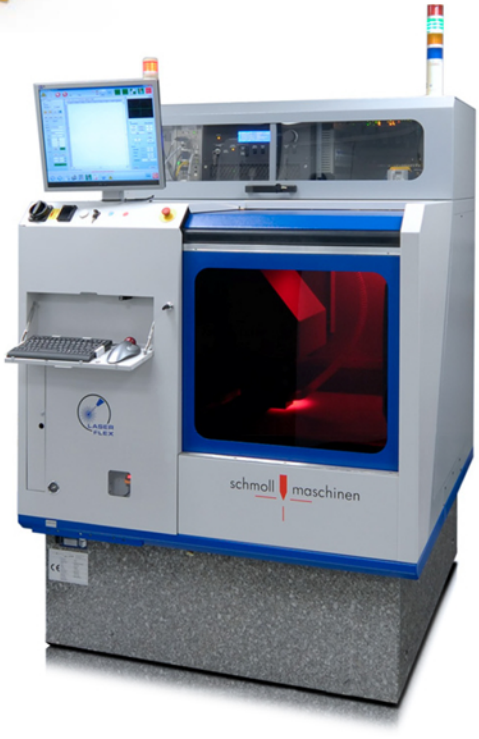

Typical applications:

- Polymer cover foil
- Covered polymer laminates
- Thin, rigid-flex materials
- Inner layers and prepregs
- Separation or decap from tracks
- Structuring cavities
- Micro-via and through-hole drilling

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ferences between mSAP and A-SAP, and what it means to designers and design engineers?

A: SAP stands for semi-additive processes, and there are a few versions out there such as mSAP and A-SAP. We call them semi-additive because they all start with a thin layer of copper before creating the circuitry. This can be either from a copper-clad material, similar to what we use in traditional PCB manufacturing but with thinner copper, or a non-clad material where the PCB factory plates the seed layer. The difference between mSAP and A-SAP is the thickness of the seed layer where mSAP starts with a copper layer, typically 3–4 microns, while A-SAP starts from an unclad material activating the surface, adding a very thin chemical copper layer of less than 1 micron. Then both processes use photolithographic methods to plate up copper traces to around 20-micron thickness before flash etching the seed layer. Basically, the thickness of the seed layer, as we see with A-SAP, is the main factor for the process to create thinner traces.

Jan Pedersen

Q: How is designing in the ultra HDI arena different from designing a typical PCB? What are some of the hurdles?

A: Designing ultra HDI is a challenge today because of a lack of standards, both for PCB production and material availability. The big hurdle today is fabrication availability. There are processes and some materials available, but very few PCB factories can offer anything below 40-micron trace and space. Some factories claim to offer UHDI, but that is very often only down to 35- to 40-micron traces, while the components you want to use requires traces and spaces below 30 microns.

Q: Are there any resources—books, websites, instructors, etc.—for UHDI design techniques?

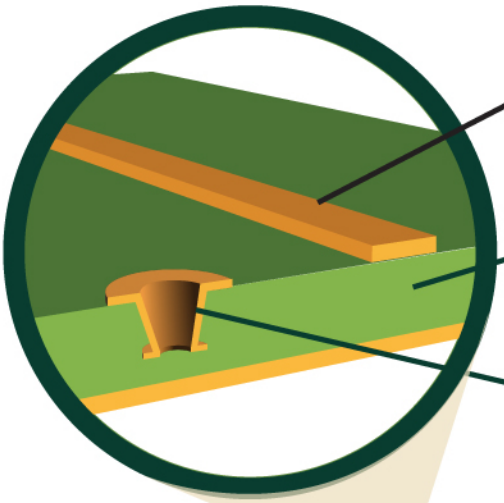
A: For designers who want to learn more about UHDI, there are a limited number of resources. I would start with Tara Dunn's Altium blogs and her I-Connect007 columns, which often cover semi-additive and UHDI. Anyone considering moving into ultra HDI should follow the NCAB blogs, available on our website and on LinkedIn. Read everything that you can.

Q: What advice would you give designers who are considering moving into UHDI?

A: The best advice I can offer is to find a supplier and be sure that you design within their capabilities. NCAB has a plan to be providing high-mix, low-volume UHDI starting as early as 2023. Today all factories that offer less than 35-micron traces have extremely long lead times. Not to sound commercial, but NCAB Group has a clear plan to change that. We are not there yet but will be very soon.

I am leading the NCAB Technical Council, and one of the focus teams is working actively with ultra HDI. As soon as we have a factory that can offer shorter lead times on UHDI, we will develop design guidelines and webinars, and provide workable parameters for designers. We need safe parameters to secure manufacturing yields and product quality from the start. It is paramount for NCAB Group to be transparent about what we can offer and how ready we are with new technologies. **DESIGN007**

Anatomy of Ultra HDI



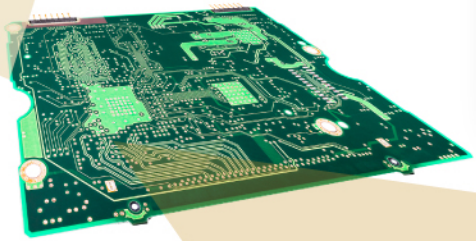
Lines and spaces thickness: **<50 microns**

Dielectric thickness: **<50 microns**

Microvia diameter: **<75 microns**

...and getting even smaller

- Lines and spaces 20–40 µm can be achieved using modified Semi-additive Process (mSAP)
- Semi-additive Process (SAP) makes lines and spaces <20 µm possible
- Fully-additive Process (FAP) creates lines and spaces <10 µm

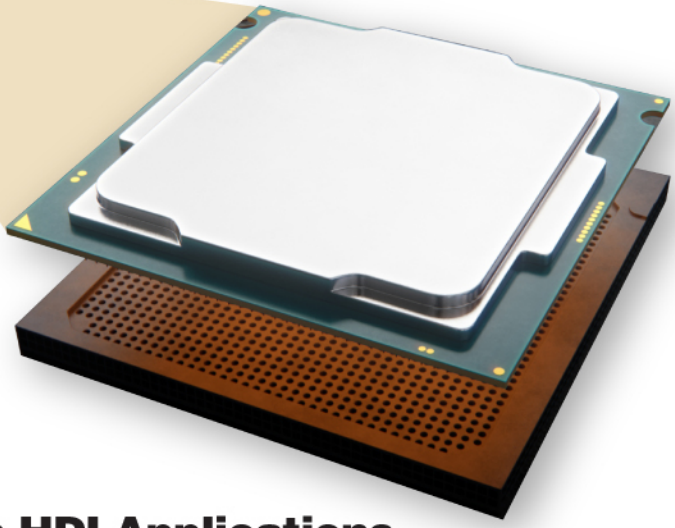


Chiplet Integration

2.5D and 3D IC packaging has gained momentum as an ideal chiplet integration platform due to their merits on achieving extremely high packaging density and high energy efficiency.

New thin, organic materials (ABF) replaces silicon as the substrate.

Source: ASE Technology Holding, Co., Ltd.



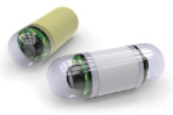
Examples of Ultra HDI Applications

Wearable devices

Implantable medical devices

5G devices

Hearing aids



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Thermal Management Isn't Getting Easier

Lightning Speed Laminates

by John Coonrod, ROGERS CORPORATION

I haven't written anything on thermal management for some time, and from my perspective, it continues to get more complicated as applications become more complex. Even applications at millimeter-wave frequencies, which typically use lower power, also have thermal management issues. It is a large topic, and this article will focus on practical issues related to PCB design and construction.

To start, heat can be generated for a circuit application in a variety of ways. Sometimes the heat is generated from an active device, sometimes from the resident power within the PCB, sometimes from the operating environment, and sometimes it is a mix of these issues. It is easier to deal with thermal management if you take one issue at a time.

Heating due to an active device usually occurs on the outside layer of a PCB and typically the heat needs to transfer through the PCB to a heat sink below. For this example, the main thermal issue is related to thermal conductivity of the PCB laminate(s) and the PCB design. For the PCB design, placing many grounding plated through-hole (PTH) vias near the heat source is commonly used. The via has copper plating. Copper is extremely high in thermal conductivity (~400 W/m·K) and the via can act like an efficient thermal path to the ground plane on the bottom of the circuit which would be in contact with the heat sink. In some cases, which often depends on the active device generating the heat, the grounding vias cannot be made and then the thermal conductivity of the laminate(s) becomes more critical.

Laminate thermal conductivity is typically in the range which would be regarded as a thermal insulator and not the desired thermal

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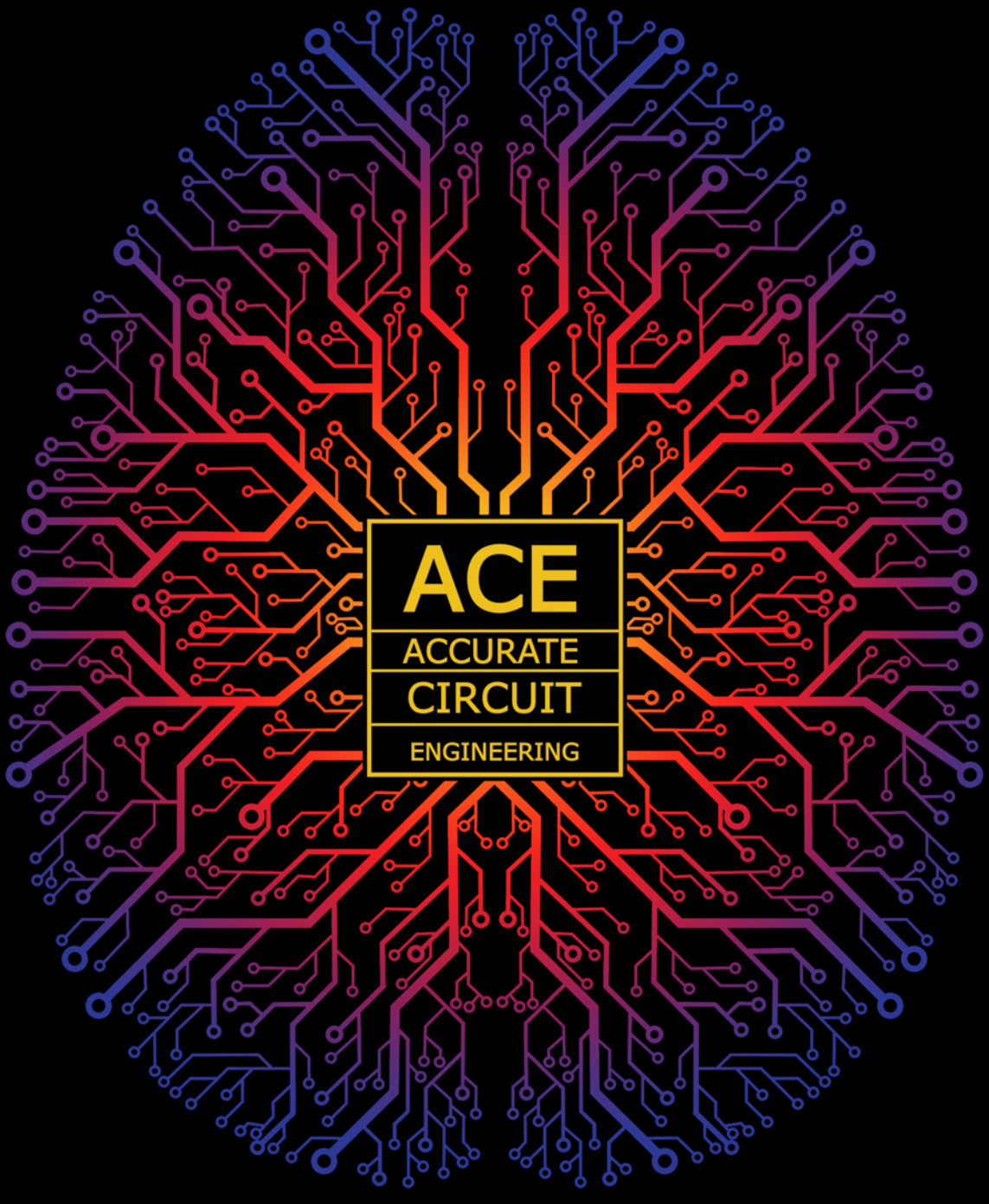

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conductor. Most PCB laminates have a thermal conductivity of 0.2 to 0.4 W/m·K. There are some laminates which have higher thermal conductivity, and a laminate with one of the highest thermal conductivities comes from Rogers. This laminate has a thermal conductivity of 1.24 W/m·K and that is when testing the substrate only. In some evaluations for thermal conductivity, the laminate supplier will include the copper cladding and that will cause the reported thermal conductivity to be higher. Rogers does not test copper with the substrate and the thermal conductivity associated with this particular laminate is the value of the substrate only. Lastly on this subject, having a combination of PTH grounding vias that are used in conjunction with a laminate having high thermal conductivity is advantageous for thermal management.

A thermal management issue related to the circuit heating due to applied power is a different thermal management issue than previously discussed. In this case, the heat flow path through the circuit as previously mentioned still applies, however, there are other issues which need to be considered. In the case of the circuit being heated due to RF applied power, then the insertion loss becomes more important to consider. Basically, an increased insertion loss will cause an increase in heat generated. One tradeoff to consider is between thermal conductivity and insertion loss. If a circuit material has low thermal conductivity, it may still be acceptable if the material has very low loss. If the insertion loss is very low, there will be less heat generated and the thermal conductivity becomes less important. On the opposite end of that concern would be to use a material that has high thermal conductivity but is not as good for insertion loss. The poor insertion loss will generate more heat, but using a material with high thermal conductivity will have the heat move through the circuit efficiently. Ideally, it would be best to have a material that is very low for generating insertion loss and high for thermal conductivity.

Another complication with RF heating of the circuit is that different thicknesses of the circuit dielectric material will cause differences in insertion loss. A circuit using a thicker low loss substrate will generate less heat due to lower insertion loss, however the heat flow path through the material is now longer due to the substrate being thicker. The heat flow formula is thickness-dependent, and a thicker circuit will have a longer heat flow path and will not be more efficient at moving the heat through the circuit to the heat sink.

Additionally, the dielectric constant of the material can have an impact on thermal management. A circuit using a material with a low dielectric constant will cause the conductors to be wider. Having wider conductors will generate less insertion loss and less heat. Also, a wide conductor will have more surface area on the signal plane. Increased surface area on the signal plane will cause a wider heat flow path and the heat flow will be more efficient from the signal plane to the planes below.

The Rogers circuit material mentioned earlier is a high-frequency circuit material that is formulated to have good qualities for thermal management. When the laminate is evaluated at 10 GHz, it has a Dk of about 3.5, and dissipation factor of 0.0017. It has a thermal conductivity of 1.24 W/m·K, which is considered very good, and it is available in a variety of thicknesses. Additionally, the laminate is available with different copper types, and the reverse-treated copper foil that is available has a relatively smooth copper surface. The smoother copper can also support lower insertion loss, which will help to decrease the heat generated and make thermal issues better. **DESIGN007**

John Coonrod is technical marketing manager at Rogers Corporation. To read past columns, click here.

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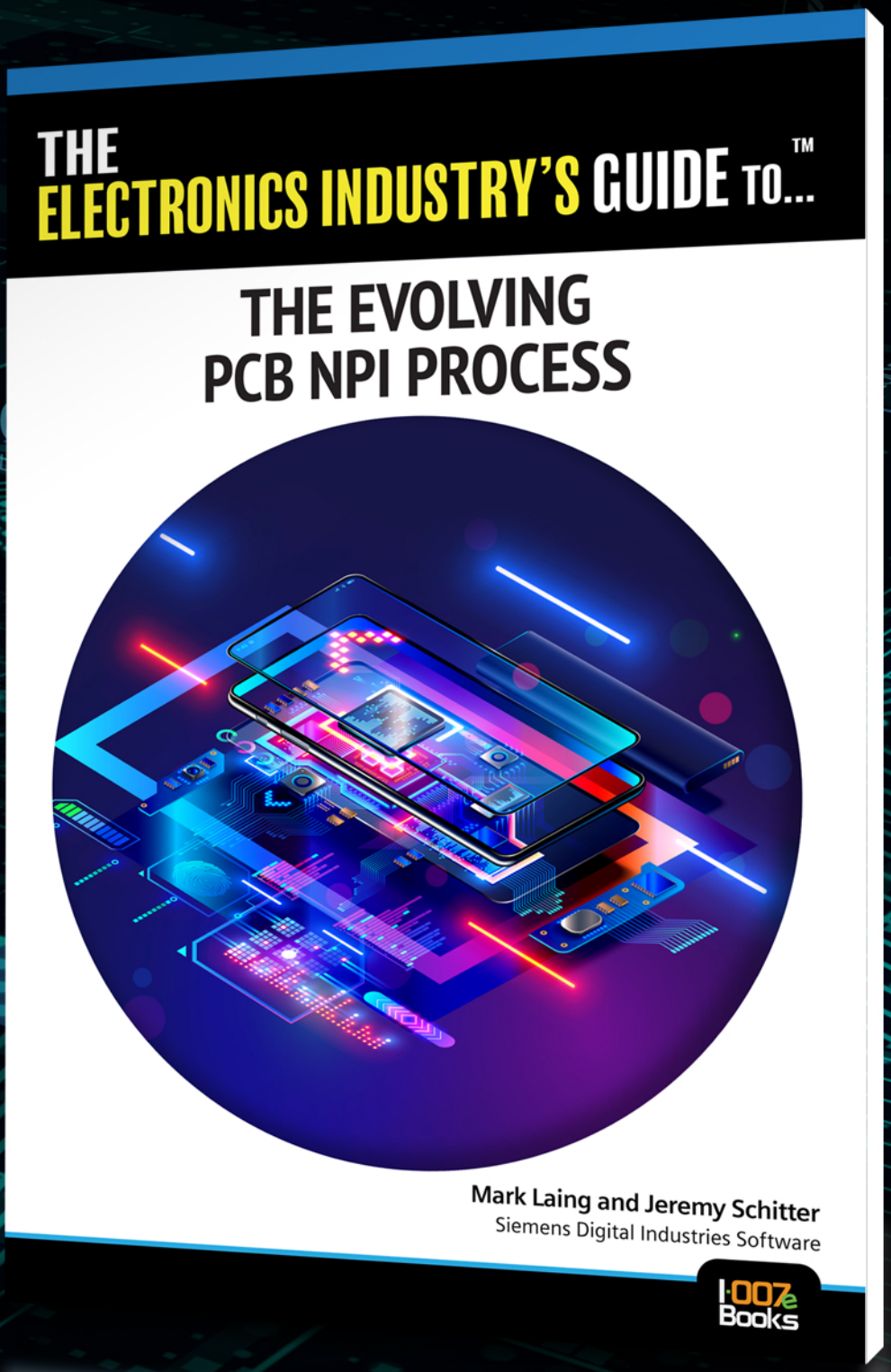

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Noise Mitigation in Power Planes

Quiet Power

by Istvan Novak, SAMTEC

Inductive kick has been a well-known phenomenon in the electronics industry from very early on. First associated with motors, AC mains transformers and mechanical relays, people noticed large voltage spikes when the current-carrying circuit was opened. Later, as more sophisticated electronic circuits emerged, the same thing was noticed any time current was changing through an inductor, or for that matter, through any inductance, whether it was an intentionally placed discrete inductor piece or just the parasitic inductance associated with a current path. This phenomenon is captured by the third Maxwell equation, which describes Faraday's Law[1]. In its simple form we know this rule from signal integrity as it describes the Dv ground bounce as a function of the dI/dt rate of change of current through an inductance of L:

$$\Delta v = L\frac{dI}{dt}$$

In today's electronics, the components are held and connected by printed circuit boards, which have been around for several decades. The front and back side of a small printed circuit board I designed, etched and populated in the late 1960s, are shown in Figure 1.

It was the audio amplifier for a battery-powered portable radio using all germanium transistors. The printed circuit board dielectric was unreinforced, fairly brittle, and to connect all components it was enough to use copper traces only on the back side of the board. The power and ground nets were carried by the wider etches near the two edges of the board. Being an analog audio amplifier using low-frequency transistors with a transit frequency in the order of a megahertz, the circuit did not create high-frequency or high-speed noise, and to carry power around simple traces with no special high-frequency bypassing was sufficient. Though the L inductance of the widely-spaced power and ground traces must have been very high,

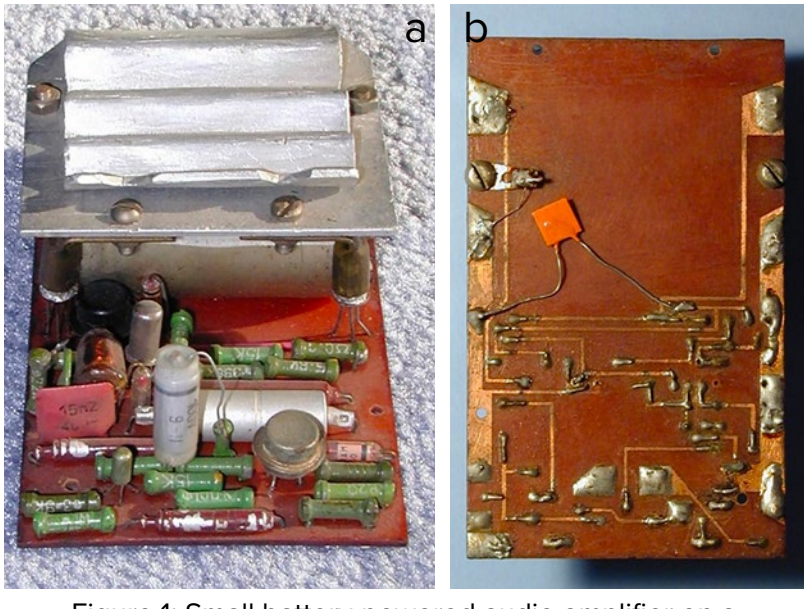
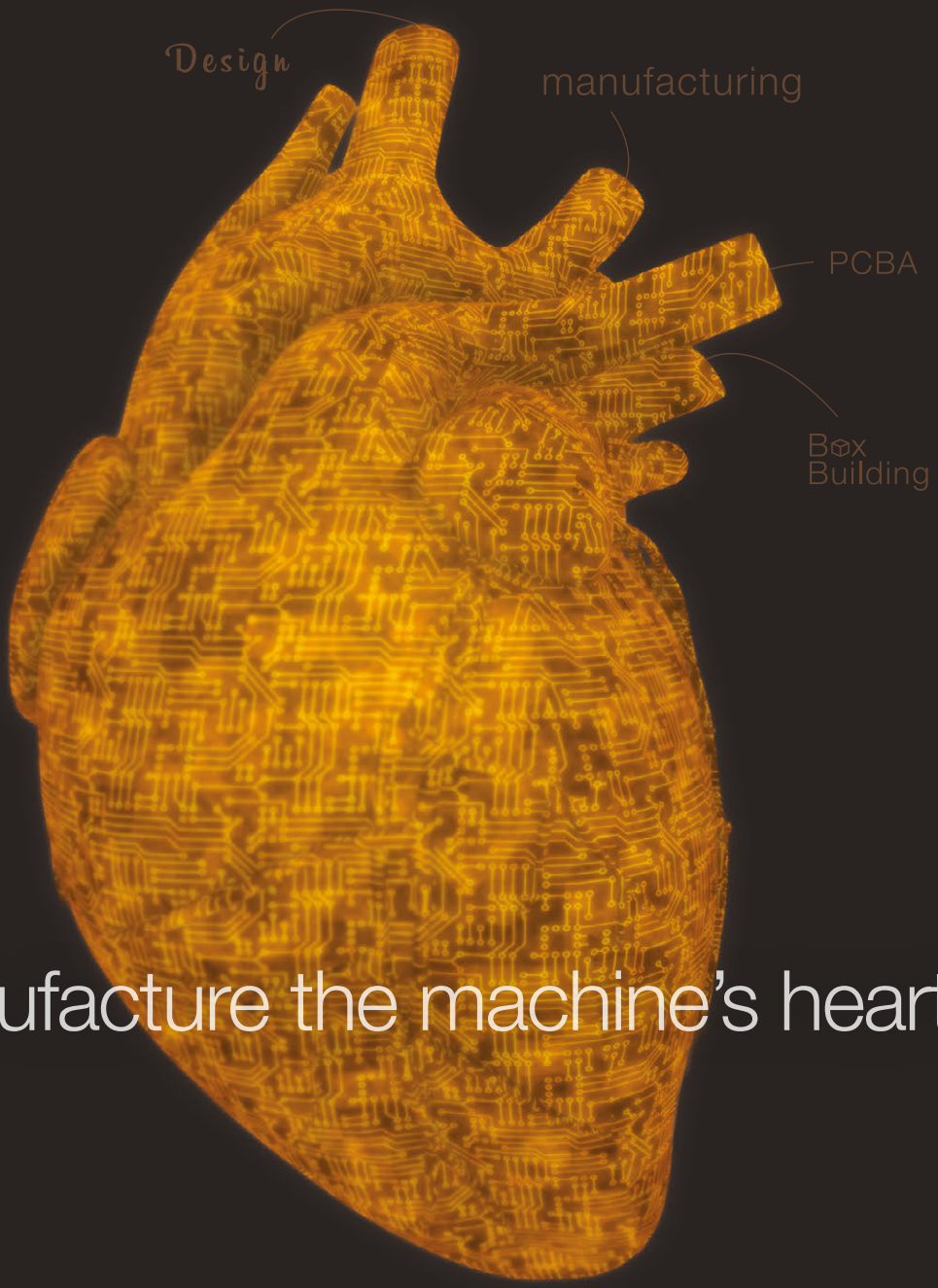


Figure 1: Small battery-powered audio amplifier on a single-sided printed circuit board from the late 1960s.



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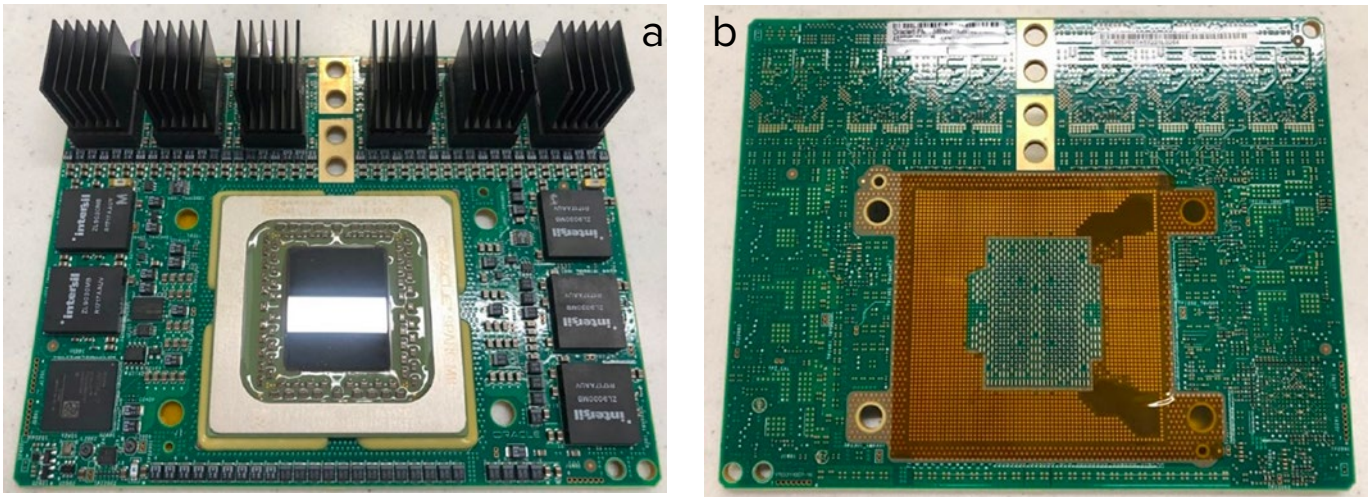

Figure 2: CPU module from the late 2010s.

possibly in the tens of nHs, the noise across it was low because the dI/dt rate of current change was even smaller.

Fast-forward about 50 years; Figure 2 shows the front and back of a CPU module from the late 2010s[2]. I designed the power distribution network for this board that consumed hundreds of watts, had 20+ layers, and used several hundred bypass capacitors. The board had multiple solid ground layers and multiple power planes for the high-current supply rails. The power and ground planes in close proximity produced very low inductance in the tens of picohenries range, which was necessary to counter the high dI/dt of the chip.

Large power planes provide not only lower inductance, but they are also necessary to keep the DC voltage drop low. However, power planes come with some downsides as they produce resonances that can interfere with both the power delivery, or most likely, with our high-speed signaling. We know that signal traces will resonate if we don't terminate them properly. Even with proper terminations at the ends, additional reactances along the signaling channel can create quarter-wave or half-wave resonances[3]. Traces are one-dimensional transmission lines, exhibiting a series of modal resonances associated with their length. Traces are one-dimensional, because we must keep the trace width and dielectric separation much smaller than the shortest wavelength of interest. In contrast, planes are two-dimensional resonators and rectangular plane pairs exhibit modal resonances both along their length and width[4,5]. As an illustration, Figure 3 shows a simulated impedance surface created by the standing-wave pattern on a 2:1 aspect ratio rectangular plane pair.

Depending on the resonance frequencies and the functionality of our circuit on the board, the standing waves and resonances can create

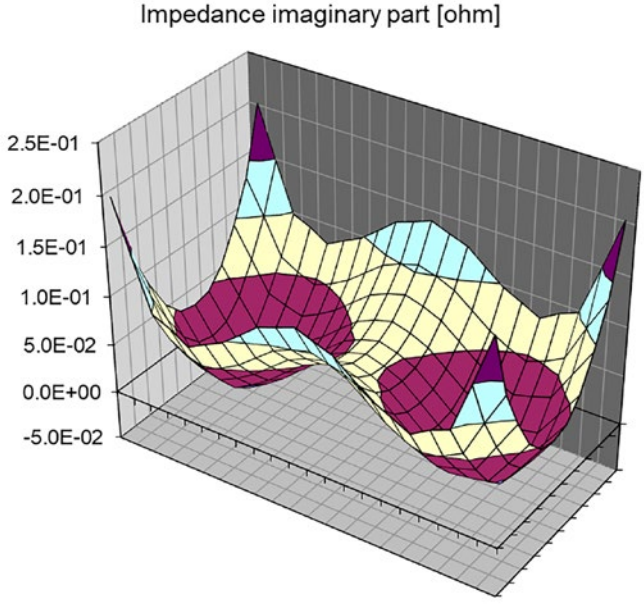

Figure 3: Impedance magnitude showing two-dimensional standing-wave pattern on a rectangular pair of power/ground planes.

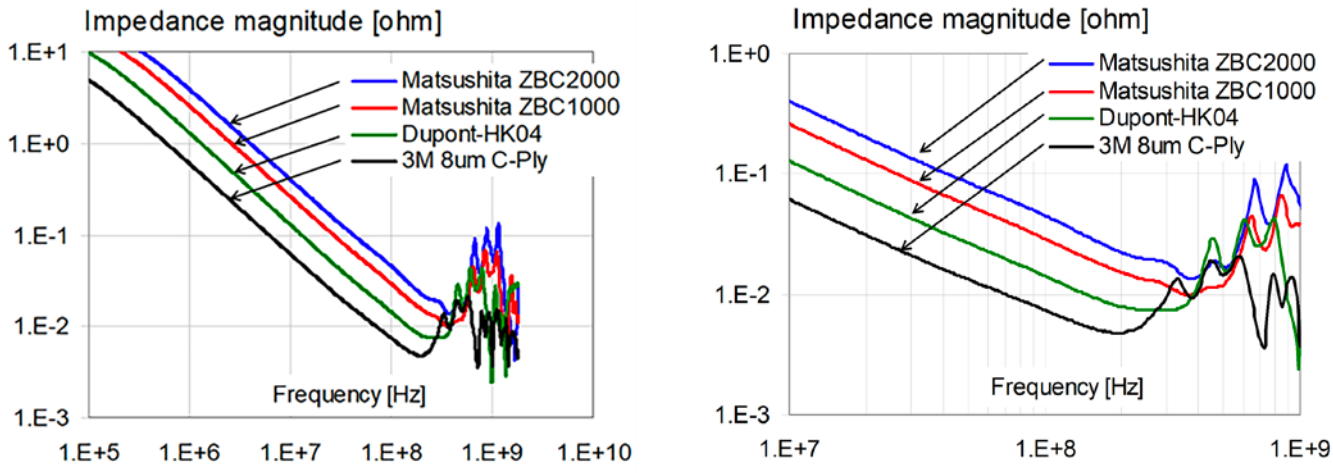

Figure 4: Transfer impedance plots of measured transfer impedances with different laminate thickness values[6].

issues in any of our major disciplines: signal integrity, power integrity, or electromagnetic compatibility. At locations and frequencies where the impedance is high, a signal via going through the power-ground plane cavity will introduce a dip in the trace's transfer function (S_{21}), which could be a signal-integrity problem. At the same locations and frequencies, power noise will be higher and if at those frequencies there is sufficient excitation energy from our circuit, the conducted noise can create power integrity issues and the circuit potentially could also radiate enough to create electromagnetic compatibility issues.

If we determine that the resonances could impose a risk to the operation of our circuit, we have a few options to deal with it. One possibility is to push the resonance frequencies high enough that our high-speed signals or power noise from our circuit will not excite them. Since we often use power planes to feed multiple electronic devices on our boards, this possible solution depends on how many devices we need to feed and what are our constraints for their placement. If this mitigation does not work, we must find a way to suppress the modal resonances. One "easy" solution is if the density of our bypass capacitors becomes so high that eventually the cumulative impedance of bypass capacitors become dominant at the resonance frequencies.

While this is a practical possibility and may often happen in very dense and physically small applications, large boards may require too many components to make this a viable option. Another alternative is to use power-ground plane pairs on thin enough laminates that naturally will suppress modal resonances. As it was explained and documented[6], the natural attenuation of a power-plane pair increases with decreasing dielectric thickness. With medium and large size boards, a dielectric thickness of 25 mm (1 mil) or less greatly suppresses the resonances. As an illustration, Figure 4 shows measured transfer impedance plots on the same board design manufactured with different dielectric thickness values.

However, laminates thinner than 75 mm (3 mils) come with a price premium, and we also need to consider the usual stackup requirements calling for symmetry. This means we cannot just use one thin laminate layer, we need to use them in pairs in the stackup, even if the circuit would otherwise require only one. Also, in case only a smaller portion of a larger board would require the suppression of plane resonances, we will end up with the same thin laminate horizontally everywhere on the board, also where you don't really need it. In those applications we can consider another potential solution: terminating the planes[7], just as we reduce trace resonances by connect-

ing the proper termination resistance to both ends. Since planes do not have well-defined "ends," as traces do, we need to connect termination components along their periphery. Power-plane pairs, except for a few special shapes, do not have a specific characteristic impedance and therefore we need to rely on approximations, such as this approximation of a rectangular plane pair with X and Y horizontal dimensions:

$$Z_p = \frac{266\left(\frac{h}{x}\right)}{\sqrt{\varepsilon_r}\left(1+\frac{y}{x}\right)} = \frac{532}{\sqrt{\varepsilon_r}}\frac{h}{P}$$

Where

Z_p is the approximate characteristic impedance of the plane pair in ohms

e_r is the relative dielectric constant of the laminate

h and P are the laminate thickness and periphery in arbitrary, but identical units

With typical plane sizes and laminate thickness values we use today, the impedance comes out in the tens to hundreds of milliohms range. We need to match this impedance with a number of termination elements, placed around the plane periphery. The number of elements depends on our frequency of interest. We need to make sure that up to the highest frequency of interest, often chosen as the tenth harmonic in the modal resonance series, the phase difference between adjacent termination components is much less than 90 degrees. As a result, we typically end up with a centimeter or so spacing. We then take the P periphery of plane shape and divide by the spacing between adjacent elements and it gives us the N number of terminations. Each termination resistor has to have an $N*Z_p$ value; many times it comes out as a few ohms. We also add a small series capacitor in series to each termination resistor to avoid shorting the power-ground plane pair with the termination resistance.

Terminating power planes was an attractive and viable solution a couple of decades ago when computer systems still had a lot of single-ended signaling and fewer supply rails with larger planes. In these days it still could be a viable alternative if system constraints prevent us from placing bypass capacitors to their optimum location. An example of plane termination on a recent computer board in volume production was described in a paper presented at DesignCon in 2021[8]. In this case, the very high density of memory sockets ruled out the placement of bypass capacitors next to the power pins of memory sockets. The simulated and measured impedance of that supply rail is reproduced in Figure 5. Note the logarithmic

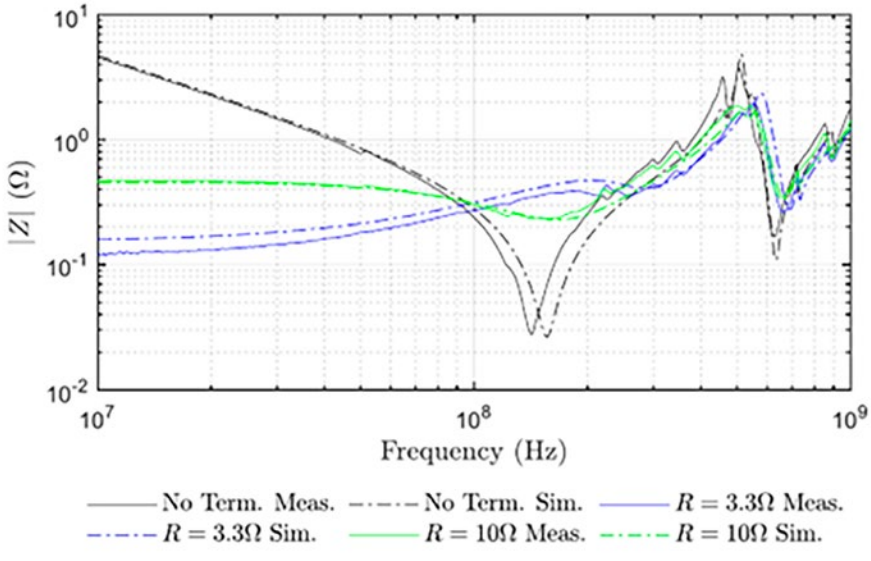

Figure 5: Simulated and measured power rail impedance on a production board with and without resistive edge termination[8].

vertical scale; using the proper termination components, the peak impedance was reduced by at least a factor of two.

Conclusion

Power planes provide a convenient means to connect multiple loads to a single power rail, but they introduce a series of modal resonances. The resonances can be suppressed by many bypass capacitors, or by using sufficiently thin dielectrics or by placing termination components along the plane periphery. **DESIGN007**

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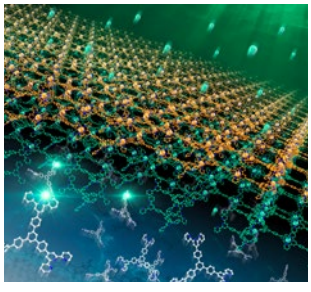
At the Water's Edge: Self-assembling 2D Materials at a Liquid-Liquid Interface

In a recent study, a team of scientists from Tokyo University of Science (TUS) and The University of Tokyo in Japan reported a remarkably simple way to synthesize heterolayer coordination nanosheets. Composed of the organic ligand, terpyridine, coordinating iron and cobalt, these nanosheets assemble themselves at the interface between two immiscible liquids in a peculiar way.

To synthesize the heterolayer coordination nanosheets, the team first created the liquid-liquid interface to enable their assembly. They dissolved tris(terpyridine) ligand in dichloromethane (CH_2Cl_2), an organic liquid that does not mix with water. They then poured a solution of water and ferrous tetrafluoroborate, an iron-containing chemical, on top of the CH_2Cl_2. After 24 hours, the first layer of the coordination nanosheet, bis(terpyridine)iron (or "Fe-tpy"), formed at the interface between both liquids.



Following this, they removed the iron-containing water and replaced it with cobalt-containing water. In the next few days, a bis(terpyridine) cobalt (or "Co-tpy") layer formed right below the iron-containing one at the liquid-liquid interface.

The team made detailed observations of the heterolayer using various advanced techniques, such as scanning electron microscopy, X-ray photoelectron spectroscopy, atomic force microscopy, and scanning transmission electron microscopy. They found that the Co-tpy layer formed neatly below the Fe-tpy layer at the liquid-liquid interface. Moreover, they could control the thickness of the second layer depending on how long they left the synthesis process run its course.

(Source: Tokyo University of Science)

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Nano Dimension Ltd., a leading supplier of additively manufactured electronics (AME) and multi-dimensional metal and ceramic additive manufacturing (AM) 3D printers, announced financial results for the second quarter ended June 30, 2022.

Happy's Tech Talk #11: An Update on Inkjet Technologies ▸

Since the first inkjet printer appeared from Hewlett-Packard in 1980, engineers have been trying to use it in printed circuit manufacturing. The first successful application was by HP PCB engineers in 1983 that created an inkjet printer mechanism to serialize each PCB with a unique S/N for traceability.

Møn Print Joins ICAPE Group ▸

From the 29th of August, Møn Print A/S joins ICAPE Group's worldwide organization to become ICAPE Denmark.

Alun Morgan: Price Increases Are Here to Stay ▸

Barry Matties and Nolan Johnson recently spoke with Alun Morgan, technology ambassador at Ventec International Group and president of EIPC, about global supply chain challenges, as well as efforts by government and industry to mitigate some of these issues.

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ITEQ Reports Lower July Sales ▸

ITEQ Corp., a Taiwan-based manufacturer of high-performance copper clad laminate (CCL) materials used for the fabrication of printed circuit boards (PCBs), has posted sales of NT$2.2 billion ($72.35 million at $1=NT$30.45) for July, down by 13% from the previous month and by 25.4% year-on-year (YoY).

Rogers Corporation to Highlight Materials for Millimeter Wave Designs at PCB West 2022 ▸

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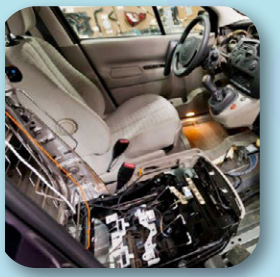

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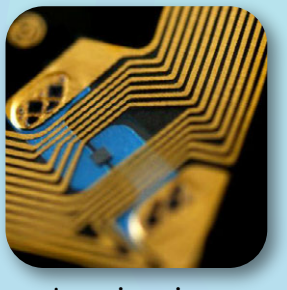

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Scaling PCB Design to the Power of 10

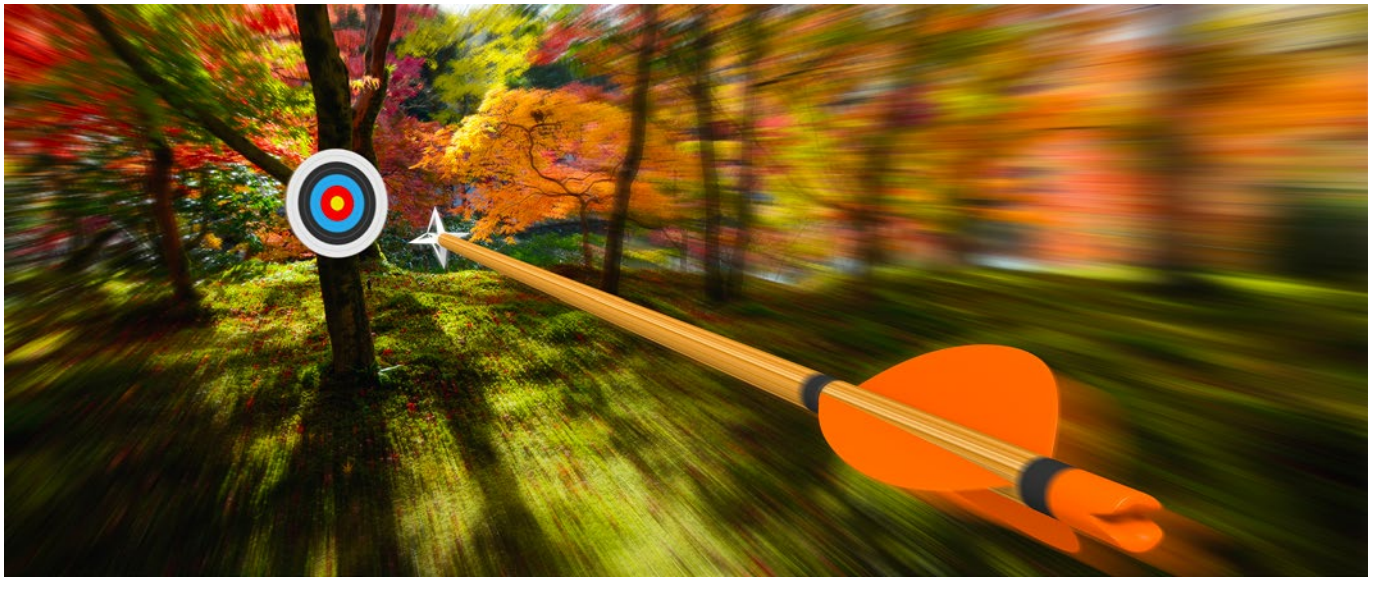
Target Condition

Feature Column by Kelly Dack, CIT, CID+

I often reflect on the formative years of my PCB design career when a senior design engineer gave me some sound advice: "Kelly, never design anything that can't be built." I think of his words every time I begin laying out a board and while I'm reviewing and performing DFM audits on customer PCB designs which are being transitioned to volume production.

The process of design shapes an idea into a readily producible, physical prototype which can be evaluated for functionality and performance. With regard to "build-ability," these days, once a prototype materializes, we are challenged differently than when I began designing boards back in the 1980s.

Since then, our manufacturing industry capabilities have scaled seemingly by powers of 10—in macro and micro directions—in their ability to process materials. Capability to process heavy copper onto power circuit substrates in thicknesses greater than 20 ounces is available using advanced print, etch, and electroplating processes. In the micro direction of scale, laser processing has enabled us to shrink many PCB features. Take via processing, for instance. We've gone from large, clunky, plated through-holes to elegantly formed HDI (high-density interconnect) microvias. Laser direct imaging (LDI) technology has allowed processing of smaller scale design topology to match the requirements of ever-shrinking electrical parts. More than ever, but not without time and significant investment, PCB manufacturing stakeholders have been able to respond to the requirements put forward by PCB design and engineering stakeholders to shrink process capability if a tangible application and corresponding justification exists.



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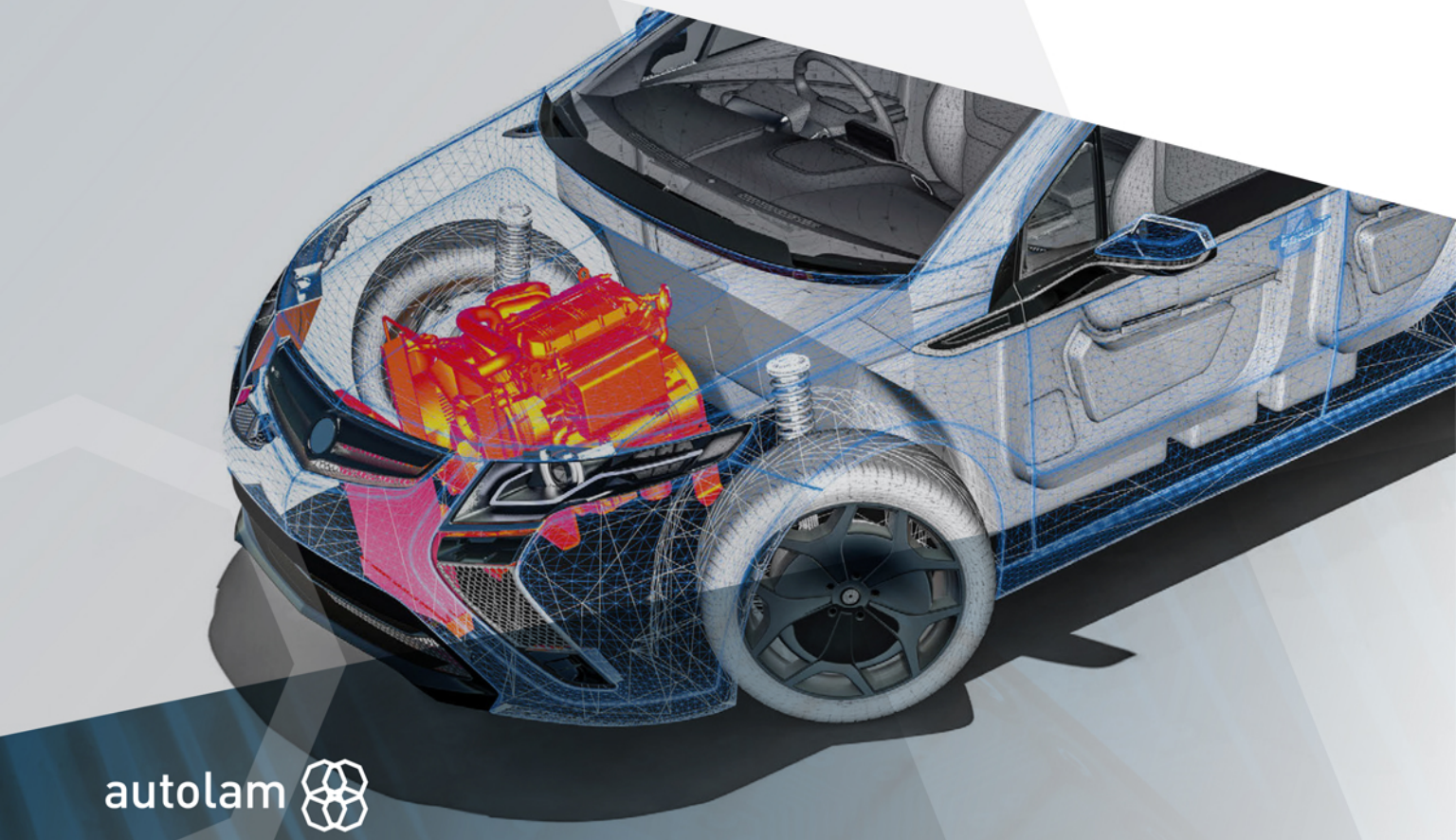

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Telescope Images Got Me Thinking

As many of us gaze upon the images taken recently by the James Webb Space Telescope (JWST), there is a great deal of discussion regarding the attributes of scale, definition, and clarity. Some excited scientists point out that these new images let us see much deeper into space than ever before. Others are forming new hypotheses about what the curious images reveal regarding the origins of matter forming each of the galaxies. Most scientists, however, remain apathetic and detached from the images because they don't reveal much about their areas of subject matter expertise.

To give our readers an idea of the scale these images are missing, I suggest viewing a 1977 short film called "Powers of Ten,"[1] produced by Charles and Ray Eames. It does an outstanding job of zooming out, then zooming back into the universe by adding an additional zero to each view, scaling to the power of 10, and helping us to understand the relative size of things. I reference this film often around campfire discussions on metaphysics, the meaning of life, and our place in the universe as PCB designers.

The film starts from an elevation of one meter over a park in Chicago. The first scene depicts a couple enjoying a picnic on a blanket. This view represents the common scale of our "neighborhood" (10 to the 0) at which average folks live and work. In the next scene, we zoom away from the blanket by a power of 10 every 10 seconds. The camera shot begins to zoom out so we can see a 10-meter wide (10 to the 1) square of grass on which the couple's blanket rests. At 100 meters out (10 to the 2), the couple disappears. The journey continues out to a dark and "lonely scene" at 10 to the 24 meters out—the equivalent span of 100 million light years—until quickly plunging back to the Chicago park to travel in the opposite direction of scale.

As I viewed the JWST images, which were shared in the news and on social media, I must say that I thought they were interesting—to a point. Yes, these images are clearer than those captured years ago by the Hubble Space Telescope (1990), showing light emitted from matter existing millions of light years away. But the image data lacks present, real-time information on the original matter. The data that's been collected in the images is obsolete by millions of years. I can see how the JWST images are newsworthy and marketable. Publishing the images proving that nebulas and exoplanets existed (past tense) is rocking the scientific world. But for me, new information about distant, million-year-old things are of little value unless I can tangibly understand them and think of a useful application for them. Heck, tiny 01005 chip component packages have been around for only a few short years, and I still have not found a use for them in a PCB design layout due to limited processing capability.

Figure 1: Image of distant galaxies from the James Webb Telescope.

A PCB Concept That Lacks Manufacturing Capability

I know there are PCB designer scientists in the electronics industry working on design standards and ways to present ultra-HDI to our industry stakeholders in a tangible format. I salute them

and their efforts to bring these images and potential standards into the view of our PCB design and manufacturing neighborhoods.

But until then, with all the advertising pageantry and displays of low-digit micron trace patterns, I'm afraid some designers will think they can try this out on "normal" design topologies. In fact, I'm currently working on a board in which the designer utilized 15-micron lines to route out of an ultra-fine pitch BGA package. This Hail Mary approach was due to the ongoing effects of our present supply chain crisis. The original design had a much larger processor appropriately matching the PCB topology scale of the layout surroundings. But like a thief in the night, the parts became unavailable and the only procurable parts with similar functionality were packaged within a 143 pin 0.4 mm pitch BGA.

To avoid substantial redesign using conventional HDI via-in-land technology affecting the stackup, the designer chose to route out the inner row connections through the outer row contacts with 15-micron lines. The designer "went all UHDI" without any special processing notes or material specification. Our volume bare board suppliers have "no bid." I have called three advertised suppliers of "X-SAP" processing, stating that I have money to spend, but I have not received a single call back.

Can UHDI and X-SAP technology help get an EMS stakeholder out of a bind by delivering on this customer design application with delivery requirements of 2,700+ boards per month? Is this layer 1 customer artwork containing 15-micron tracks a viable solution? Can we just add a note which says *"Add UHDI processed copper here using supplied artwork?"* Should we continue punching down this UHDI path or re-design the entire area of the design to conventional HDI via technology? Which solution will give our customer less sticker shock?

Diving Into UHDI on a PCB

As I depict in Figures 2 through 5, it is easy for a PCB designer to draw a 15-micron (0.59 mil) trace with a CAD tool. But now what? Is X-SAP viable, available, and cost effective for use on any PCB? These questions must be answered before layout or PCB designers risk hitting "send" and shooting their design data beyond the comfort of our manufacturing stakeholder neighborhood.

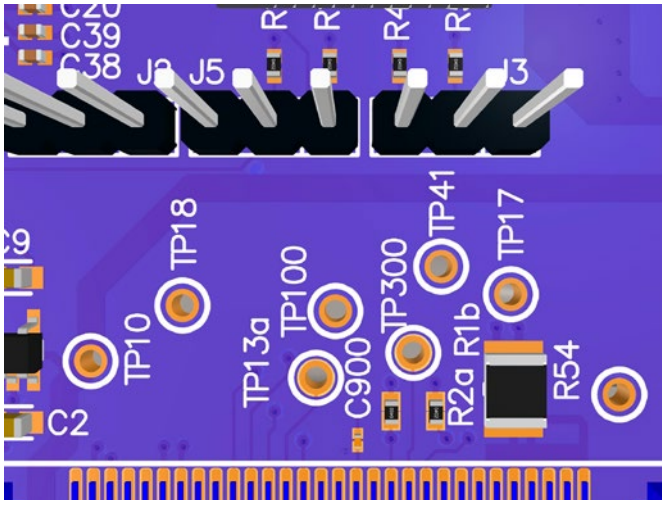

Figure 2: A common PCB design layout neighborhood. Not without its own challenges of manufacturability but at this scale appears to be exceptionally rich with applicable, perceptible attributes. For our PCB project stakeholders, this is like starting with that view of the blanket on the grass in the park in "Powers of Ten."

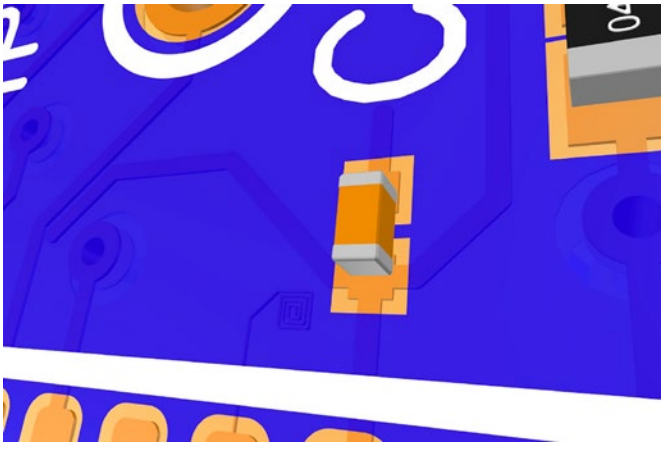

Figure 3: Zooming in to the metallized contact end of a common 0201 chip, we can see the transition point between the land and the trace. We can see how the solder mask clearance around the land will allow the solder to flow out and away from the contact allowing disproportionate amounts of solder on each end of the chip, possibly leading to an assembly defect.

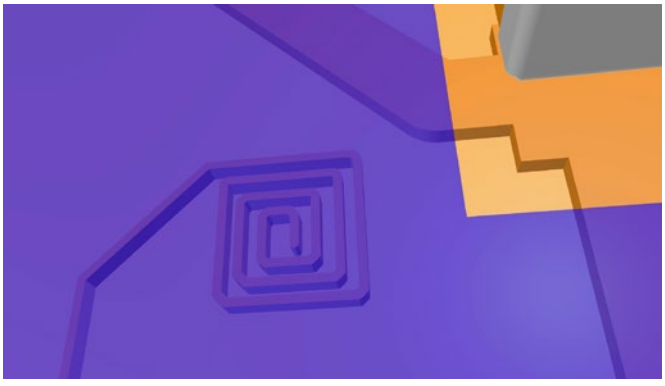

Figure 4: Zooming past the transition between land and trace we see a small UHDI trace emerge. What it will be used for (application and cost) is yet to be determined, but it is good to know that the manufacturing capability is there to support the requirement when an application arises.

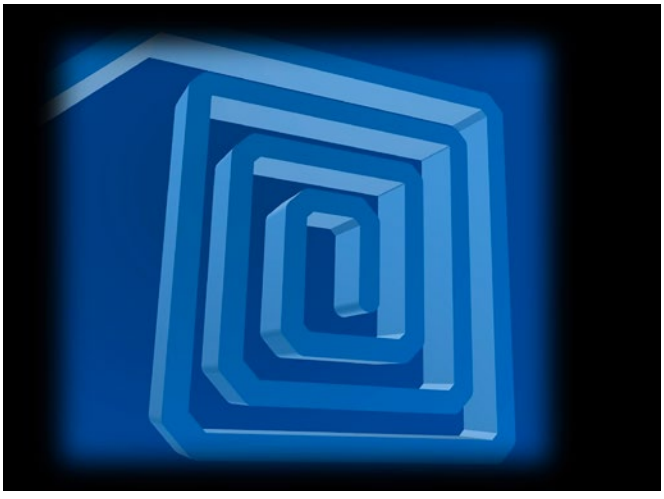

Figure 5: I whipped this layout up on my own CAD tool. Proof that common CAD design capability exists to create a 15-micron trace. But for many PCB designers, applications for this capability are surrounded by darkness. Designers and engineers will need help to see how to implement and scale UHDI to volume production to realize value.

I hope PCB designers will find ways from our contributors to tangibly understand and apply UHDI technology. Will UHDI remain as limited for use as are the tiny 01005 chip packages due to manufacturing capability? Will there be confusion on how to implement UHDI into a PCB which already suffers assembly challenges while processing micro-scaled 0201 chip packages? Designers don't have to voyage too far into smaller scales of technology before pushing a PCB destined for low-cost, volume production into outer darkness. It is notable that the narrator of "Powers of Ten" makes the point that most of space—galaxies and quarks—are like dust suspended in darkness. (Hey, this sounds like my recent request for an UHDI quote.) The narrator comments, "The richness of our own neighborhood is the exception."

Is our propensity to focus on the distant macro matter of space or the micro matter of PCBs just a distractive diacatholicon, diverting our attention from the problems and challenges of our present scale? "Our house is on fire," warn our supply chain managers, quality engineers, and DFM auditors. We've got substantial problems to solve within our own neighborhoods in the PCB industry right here on Earth.

I do think the messaging of the "Power of Ten" film somehow transcends into scales of PCB design. We must first and foremost consider the neighborhoods of our PCB industry stakeholders.

As PCB designers creatively zoom out or in, we must avoid venturing into manufacturing darkness. Be thankful for the scientists who go there and bring back applicable data. Let's help where we can and as project stakeholders, wisely stay in touch, understand, and apply appropriate scales of technology in our industry neighborhoods or we risk losing vision and sense of purpose.

"We are stardust, we are golden, we are billion-year-old carbon, and we've got to get ourselves back to the garden." —Joni Mitchell. **DESIGN007**

References

1. "Powers of Ten," a 1977 film adapted from *Cosmic View,* authored by Kees Boeke. The film is available for viewing on YouTube.

Kelly Dack, CIT, CID+, provides DFx centered PCB design and manufacturing liaison expertise for a dynamic EMS provider in the Pacific Northwest while also serving as an IPC design certification instructor (CID) for EPTAC. To read past columns, click here.

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Avoiding Conformal Coating Pitfalls

Sensible Design

by Saskia Hogan, ELECTROLUBE

Electronic circuits are abundant in modern life and will continue to surge in growth as former manual processes increasingly become automated. The rapid advances we see in technology are driving electronic circuitry to perform faster in harsher environments, in the smallest form, and with the lightest weight. Circuitry failure is not only inconvenient and expensive but as electronic infrastructures become more interconnected, individual failures will put an entire system at risk, which could ultimately put lives in danger for critical applications. It is so important to factor in careful consideration for conformal coatings. In this month's column, I will cover some important areas to help you steer clear of coating disasters.

Get It Right at the Design Stage

The earlier the coating is factored into the design process, the more likely there will be a successful coating outcome. It saves time and expense in rectifying any problems that may occur later. Important considerations include specifying:

- "Must-coat" areas of the PCB
- "Must-not-coat" areas
- Transition areas, sometimes referred to as "can-coat" or "don't care" areas

Check how close together the components are and whether there is a sufficient gap between the components. If the gap is insufficient, it can lead to the coating bridging the gap rather than correctly conforming to the

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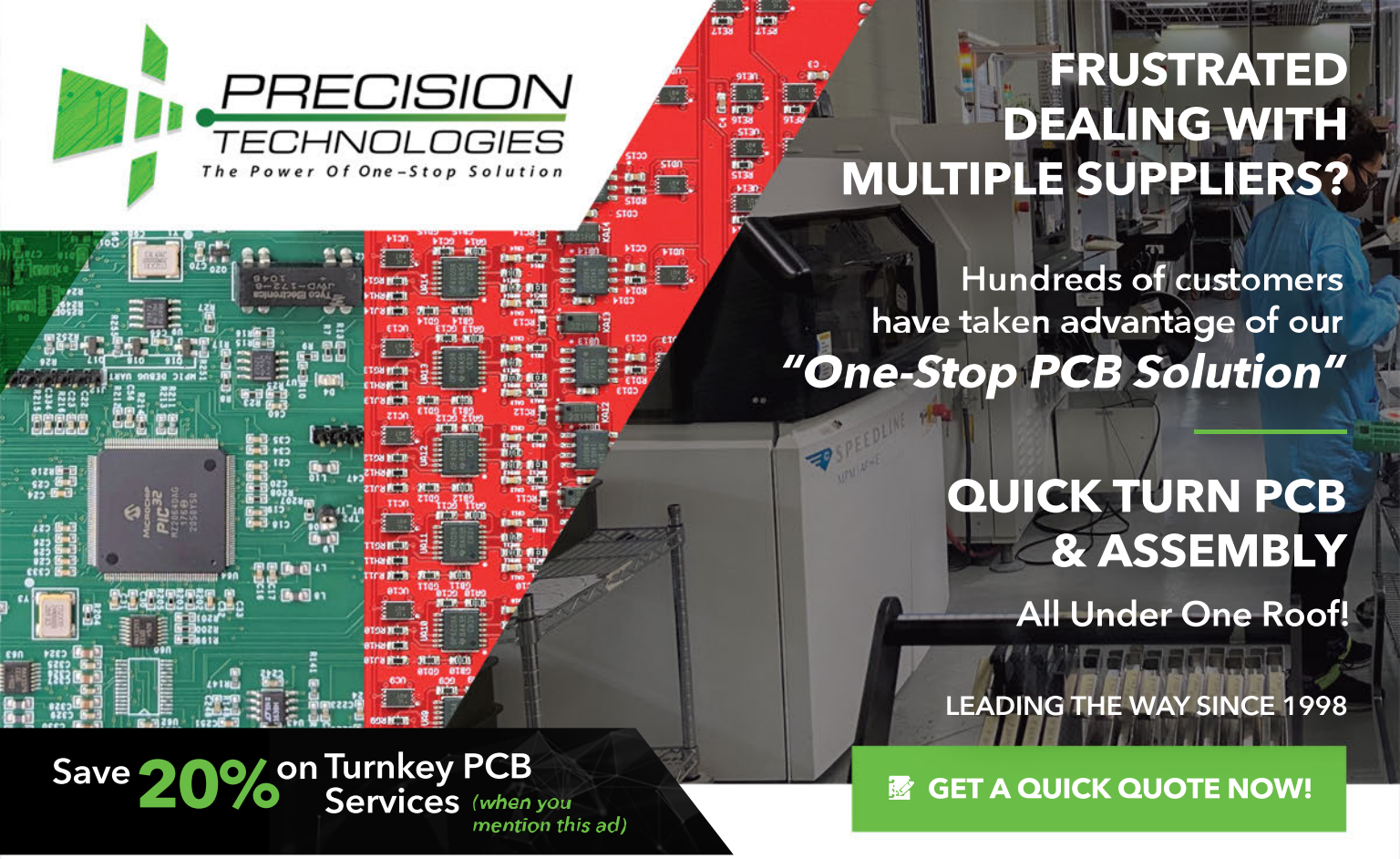

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board, which can also cause the coating to become too thick and crack or it can leave pockets under the coating where solvent can gather and cause corrosion. Tall components can bring their own challenges by creating shadowed or hard to reach areas. It is therefore sensible to avoid placing tall components in direct proximity to "must-not-coat" areas of the PCB. Larger spacing between such areas can help to achieve a cleaner coating picture. If a larger gap is not maintained, coating may splatter onto "must-not-coat" areas.

Tall components can bring their own challenges by creating shadowed or hard to reach areas.

Preparation the Key to Success

To truly minimize the risk of defects and failure, cleaning prior to coating needs to be a top priority, otherwise potential residues on the substrate will have a critical impact on coating performance. Without cleaning, residues may interfere with curing, leading to poor adhesion of the coating to the substrate and trapping conductive/ionic materials under the coating. Without a pre-coat cleaning regimen, corrosive residues bridging the PCB's conducting tracks can cause failures over time. It is of key importance that the PCB is fully dry following the cleaning process to ensure that any residual solvents and moisture are removed prior to the coating and curing procedures. Humidity below the coating can lead to corrosion. Residual solvent on the board can cause bubbles or cracking during the curing process.

Apply the Coating Well

Applying a coating correctly is probably the biggest factor for coating success. You may have purchased the best coating known to the industry, but if it isn't applied well, it simply will not deliver sufficient protection. Attainment of the "right" coating application is just as important as selecting the right material.

Top Tips

1. Check the coating thickness that's required. Do not apply the coating in a thicker layer than is recommended. If the coating is applied too thickly, solvent entrapment can occur, causing a weakness for external influences to attack the board.
2. Check the level of coverage. Gaps in the coating coverage can leave areas of components exposed to humidity or corrosive gasses, providing an entry point to metal surfaces of components.
3. Consider the adhesion of the coating to the board and its components. Contamination or processing residues on the board can lead to an insufficient wetting of the coating. Even where the coating is showing a good level of adhesion, the contaminant may not show the same good adhesion to the substrate, potentially leading to delamination.

Remember: The typically successful application method would ensure that each board receives a suitable coating coverage on all required metal surfaces, at a sufficient thickness to provide protection against the environment. These requirements will change with different board designs and environments and will need to be tested and verified ahead of production.

Coating Selection

There are many coating options to choose from, such as an acrylic, a polyurethane, a silicone, a UV cure, or a two-part system. The design of the board may or may not affect the choice of coating material, but it will definitely

influence the methods that are suitable for application of the coating. Certain materials, such as moisture-curing or UV-curable materials, are difficult to use in a dip process due to the material curing prematurely, so it could be said that the choice of coating is indirectly related to the board design. Factors such as operating temperature range, temperature excursions (such as thermal shock and thermal cycling), corrosion, condensation, and resistance to chemicals, solvents, and water are all key in determining the successful outcome f or a coating. Working with an experienced provider can help you navigate which coating is best for your application and advice on methods.

Consider the Two Primary Failure Mechanisms

Aside from insufficient planning at the design stage, a poorly applied coating, or ignoring pre-coat cleaning, two of the most common reasons for coating failure include corrosion and loss of insulation, which leads to short circuits. Corrosion is a complex process that takes place on an exposed metal surface, usually in the presence of water and ionic contaminants. Cleaning prior to conformal coating will go a long way toward removing these two pre-requisite conditions for corrosion as coatings help prevent the formation of electrolytic solutions by acting as moisture barriers. However, small voids in the coating that expose a PCB's metal surfaces can accelerate corrosion under the right environment. The challenge for a conformal coating is to achieve good coverage and adhesion to the complex, three-dimensional topography of a PCB. Poorly performing coatings also risk loss of insulation at the PCB surfaces when water condenses in combination with ionic impurities to form conductive pathways between PCB tracks. Without doubt, condensation can severely test the insulation resistance of a coating.

Avoiding coating pitfalls is a fine balance of material selection, understanding the engineering requirements for coverage, and thickness, as well as choosing a suitable application method. Understanding the intricacies of conformal coatings will pay off in determining a successful coating outcome. There's a great deal more to discuss and over the following months I hope to provide more useful tips and advice that will help you accomplish reliable circuit protection. **DESIGN007**

Saskia Hogan is global product manager, conformal coatings, at Electrolube. To read past columns from Electrolube, click here. Download your free copy of Electrolube's book, *The Printed Circuit Assembler's Guide to... Conformal Coatings for Harsh Environments*, and watch the micro webinar series "Coatings Uncoated!"

Unblocking Innovation With a Component Digital Thread

Digital Transformation

by Matt Walsh, SIEMENS EDA

In our series of digital transformation columns, we've hit on several highly relevant topics that electronic systems design companies face today, including a look at supply chain resilience as a challenge and an opportunity and then optimizing multi-domain co-design. This month takes up another important new development: establishing component digital threads. The positive impacts on systems design companies and the electronics ecosystem will be revolutionary.

Note: In this article, "component" and "part" are used interchangeably.

I can remember the days, as a young electrical engineer at a leading mil/aero company, when the source of passive and IC device data for my circuit functional designs was based on the contents of a floor-to-ceiling bookcase filled with data books of production parts from the leading semiconductor suppliers. The vertical search engine of the day was the simple stepstool I used to comfortably read the spines of the data books on the upper shelves. You trusted the data was accurate, especially the DC and AC switching characteristics and physical package specifications.

Still, thankfully, access to electronics part data went digital and has been improving for many years now, so you can go to any number of component distributor or popular industry aggregation websites to accomplish your component research. The represented component supplier data is plentiful, and filtering options make the data easy to search, but given the volume of data, it is too often stale, incomplete, and hard to fully verify. Moreover, when a part is chosen, engineers and teams tasked with product creation must sift through and interpret copious amounts of information presented in static PDF files that differ subtly in format, style, and naming conventions from one supplier to the next. With PDFs in hand and still needing to translate an idea


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into a product, engineers must expend additional time and effort to create or search-to-acquire all the models (simulation, IBIS, ECAD, mechanical, etc.) needed to get their job done.

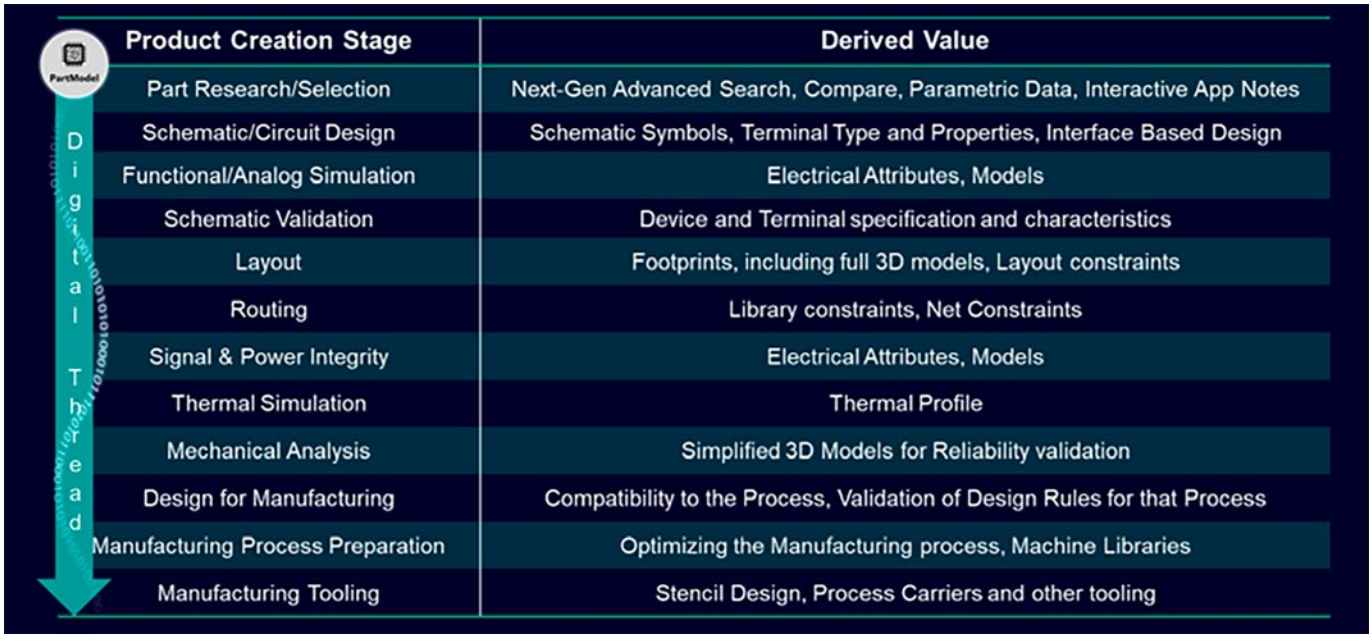
I don't know what all the latest stats say but, honestly, the engineer's journey is riddled with speed bumps and potholes that lead to wasted, unproductive time. The world may have gone digital with tools for component research, ideation, design, and analysis, and hand-off to manufacturing may have improved greatly, but as Figure 1 depicts, chasms persist in the electronics value chain. Nevertheless, today, somehow, some way, electronics design innovation still happens. Yet there is so much potential to be realized if there was greater digitalization along the systems value chain. The time to achieve that has arrived.

In 2018, JEDEC ratified the JEP30 standard. The website states: "This standard establishes the requirements for exchanging part data between part manufacturers and their customers for electrical and electronic products. This standard applies to all forms of electronic parts." JEDEC, one of the most widely respected (open) standards bodies for the microelectronics industry, with several hundred member companies (mostly part manufacturers), fired the "shot heard round the world."[1]

My intent here is not to do a deep dive into JEDEC[2] but it's important to underscore the milestone that set the stage for the current revolutionary phase of digital transformation within the electronics industry. Why? Because the JEP30 Part Model standard effectively defines the digital twin for an electronic part. That's a big deal. In short, the part model combines information (related to electrical, physical, thermal, assembly process classification, and more) about a part into an industry-standard-based digital container defined with an XML schema. The part model schema also comprehends standard interfaces and has the flexibility to access specialized models (for example an IBIS model) that can be added to the part model for an applicable device. The standard also extends electrically to support the notion of reference designs associated with the part model of a specific component. So, number one, the JEP30 Part Model is an industry standard, but here's the game changer: The JEDEC JEP30 Part Model will now be consumable directly by every tool in the product creation lifecycle.

I mentioned the engineer's journey above and the potholes that lead to wasted time on less productive tasks. These challenges are made even more daunting when overlayed onto the complexity faced by engineers and development organizations given the ever-increasing requirements of each successive generation of electronics product, not to mention the complexity of the underlying components being used. For example, even tra-

Figure 1: Today's electronics value chain.



Product Creation Stage	Derived Value
Part Research/Selection	Next-Gen Advanced Search, Compare, Parametric Data, Interactive App Notes
Schematic/Circuit Design	Schematic Symbols, Terminal Type and Properties, Interface Based Design
Functional/Analog Simulation	Electrical Attributes, Models
Schematic Validation	Device and Terminal specification and characteristics
Layout	Footprints, including full 3D models, Layout constraints
Routing	Library constraints, Net Constraints
Signal & Power Integrity	Electrical Attributes, Models
Thermal Simulation	Thermal Profile
Mechanical Analysis	Simplified 3D Models for Reliability validation
Design for Manufacturing	Compatibility to the Process, Validation of Design Rules for that Process
Manufacturing Process Preparation	Optimizing the Manufacturing process, Machine Libraries
Manufacturing Tooling	Stencil Design, Process Carriers and other tooling

Figure 2: Component digital thread derived value.

ditional "analog" components are becoming more "digital"—adding programmability, state machines, and other advanced features that are beyond the capabilities of existing analog design tools. Conquering this complexity quickly is essential to maintain the innovator's edge. Armed with part model digital twins, innovation is more readily facilitated and extended.

A digital thread is a communications framework that allows a connected data flow and an integrated view of product data throughout its lifecycle—spanning ideation, realization, and utilization. The digital twin is an essential element of the digital thread, connecting the virtual and physical worlds across the value chain of product, production, and performance. As outlined in Figure 2, at every stage of product creation the part model digital twin will deliver derived value directly to the tools used at each step. In action, part models will enable and empower engineers with greater strategic decision capacity at every point in the design process. Their use will streamline the design process by shortening dependencies, because critical information and model content can be derived from the part model. Most importantly, part models powering the design process will improve first-pass success rates because their use will greatly reduce the risks to successful product delivery caused by time delays and human error that accumulate throughout the product creation process. No more searching for model content. No more fixing data integrity errors from a third-party model. No more misinterpreting the numbers in DC and AC switching characteristic tables because it was difficult to decode the naming conventions used by a given component manufacturer.

As the electronics industry continues to embrace the transformation of component data into industry-standard-based digital twins, it will unblock and unleash the innovation process as the connection between OEM and the component ecosystem they rely on goes from handshakes based on PDF files to high-bandwidth, intelligent links composed of digital part model threads.

Component suppliers will play a critical role in this digital transformation because the data sourced in the part model XML files of tomorrow are presently sourced using static PDF files. Many component suppliers are already shifting to part model representations of their parts. Others will follow as more tools are

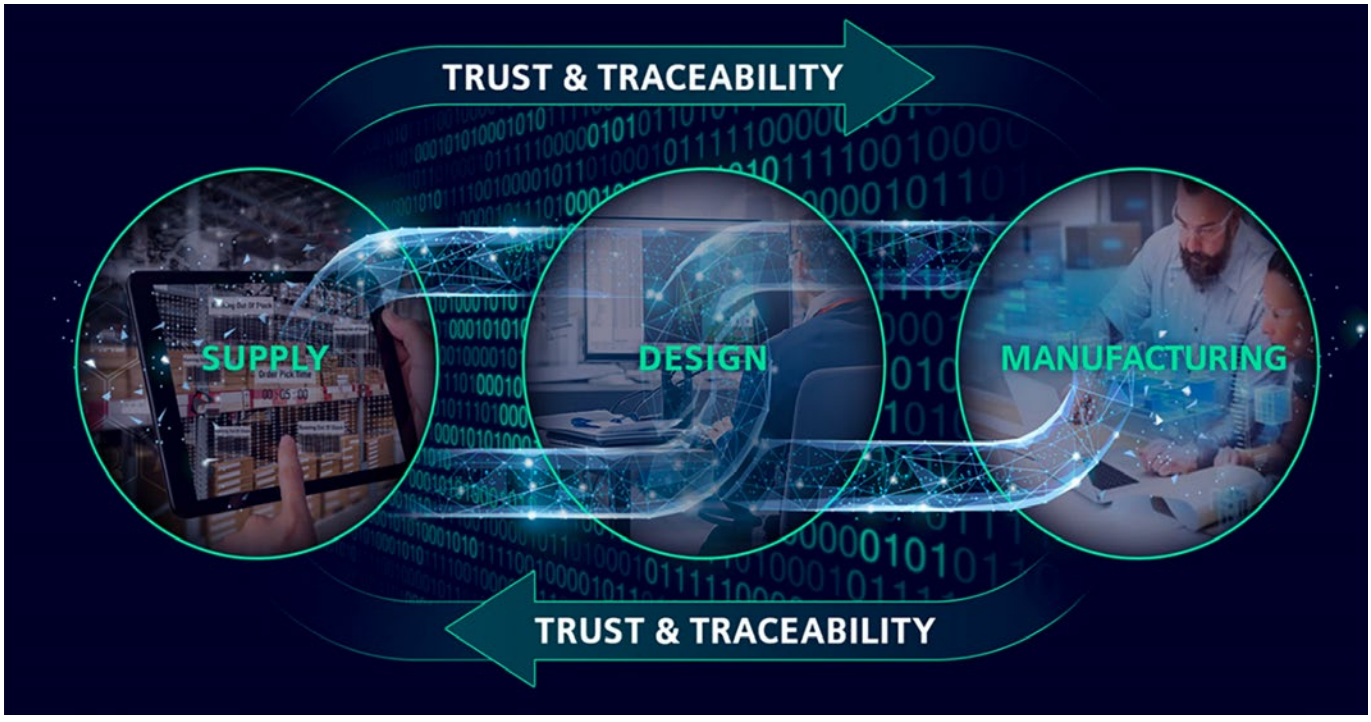


Figure 3: The part model era.

made available to facilitate the transition and validation to the industry standard.

PDFs as a means of exchanging datasheet information aren't going away, but in the part model era, they will be augmented by datasheets in digital form and interactive application notes that will offer more robust component supplier to end-customer user experiences and connections. As the shift to digital twins of component data accelerates, building in trust is a natural progression. Part models are complete digital representations of parts. You can therefore envision a day when the part model, or different sections of the part model, will assimilate digital signatures to establish the basis for an immutable ledger that will initiate trust throughout the design chain.

The part model era will enable digital transformation that will touch all players in the electronics value chain. This is a big "T" transformation because it will revolutionize the electronics industry; it will accelerate the design process, leading to greater profitability; and it will pave the way for new levels of innovation—so you can unleash the full potential of your engineering team today. **DESIGN007**

References

1. "Concord Hymn," Ralph Waldo Emerson, 1837.
2. Learn more about their work and the JEP30 Part Model standard at jedec.org.

Matthew Walsh is a product marketing manager in the Electronic Board Systems division of Siemens Digital Industries Software. To read past columns, click here.

More Information

- **Siemens' 12-part, on-demand webinar series *"Implementing Digital Twin Best Practices From Design Through Manufacturing."***
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Flex007 Highlights

Print, Recycle, Repeat: Scientists Demonstrate a Biodegradable Printed Circuit ▸

According to the United Nations, less than a quarter of all U.S. electronic waste gets recycled. In 2021 alone, global e-waste surged at 57.4 million tons, and only 17.4% of that was recycled.

Flexible Thinking: The Rapidly Expanding Realm of Stretchable Circuits ▸

Flexible circuit technology has been rising ever higher on the radar of those charged with designing next generation electronic products for every imaginable application, from the mundane to the highly exotic. The technology is being embraced by a growing fanbase as they become increasingly aware of flex circuit technology's numerous benefits.

FCT: Powerful Growth in the Flex Segment ▸

After the initial impact of the global pandemic led to a somewhat flat 2020, Carey Burkett, vice president of Flexible Circuit Technologies, explains how the company's growth took off in 2021, positioning it well for industry trends that continue to show great promise in medical, automotive, consumer, and more.

Printed Circuits and All Flex Join Forces as 'All Flex Solutions' ▸

We are pleased to announce the merger of Printed Circuits and All Flex to become one company, named All Flex Solutions, Inc. The merger closed on Aug. 31, 2022, following two years of thoughtful collaboration and integration.

Part 2: The Printed Electronics Roundtable ▸

We recently held a roundtable with a team of printed electronic circuit experts from companies that run the gamut: John Lee and Kevin Miller of Insulectro, Mike Wagner of Butler Technologies, Tom Bianchi of Eastprint, and John Voultos of Sheldahl Flexible Technologies. In this second part of the roundtable, the participants discuss what designers and fabricators need to know to jump into printed electronics, and some of the drivers behind this growing technology.

Compeq August Revenue Up 24% YoY ▸

Compeq Manufacturing Co. Ltd, a Taiwan-based manufacturer of HDI, rigid-flex PCBs, and flex PCBs, has posted unaudited net sales of NT$7.19 billion ($232.6 million at $1:NT$30.90) for August 2022, up by 23.68% year-on-year and by 4.35% month-on-month.

Nan Ya PCB August Revenue Up 22% ▸

Nan Ya Printed Circuit Board Corp. (Nan Ya PCB) has posted unaudited sales of NT$5.76 billion ($183.4 million at $1=NT$31.39) in August 2022, up by 4% from the previous month and by 21.8% year-on-year.

Fralock Earns IPC-1791 Qualified Manufacturers Listing (QML) as Trusted Electronics Designer ▸

IPC's Validation Services program has awarded an IPC-1791, Trusted Electronics Designer Requirements Qualified Manufacturer Listing (QML) to Fralock, located in Valencia, California.

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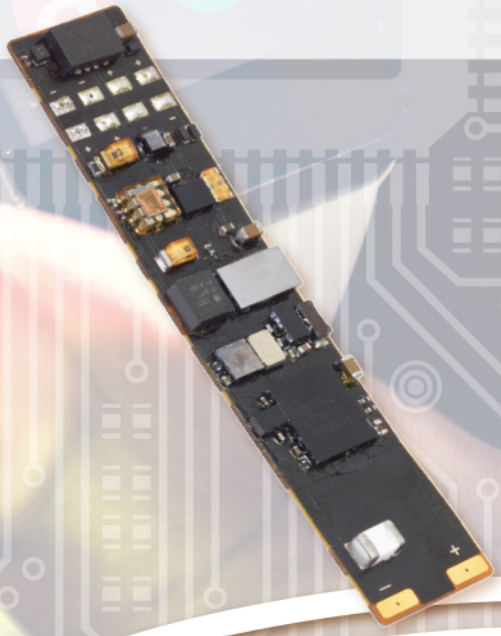

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Market and Tech Convergence: Electrically Conductive Inks

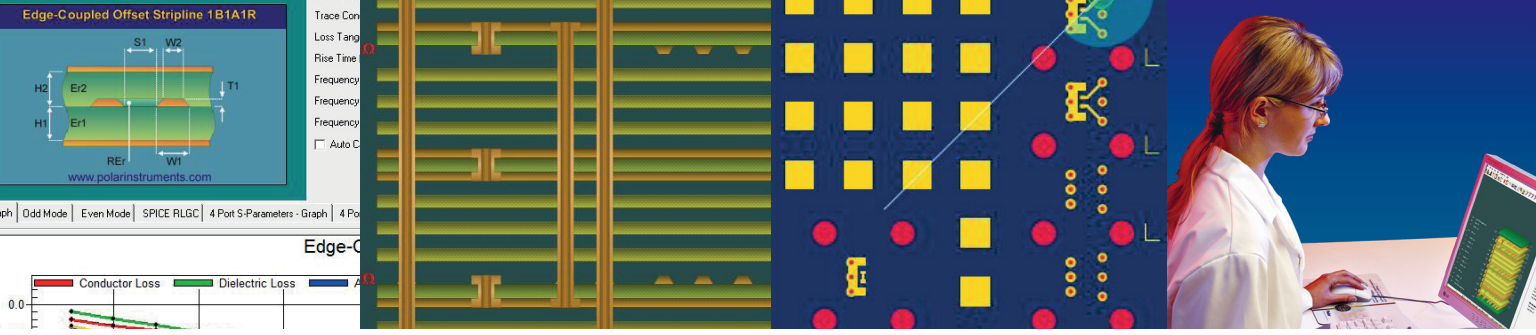
Article by Stan Farnsworth
NOVACENTRIX

It's no secret that electronics products are being asked to do more, pushing the boundaries of technological capabilities. Next-gen consumer products like flexible wearables and foldable mobile devices are proving themselves to be more than a fad, with start-ups and major companies alike booming on the market for the past few years.

In July, Samsung announced 2021 foldable phone sales were up 300% from 2020, at more than 10 million phones. Samsung's Galaxy Z Flip3 Bespoke Edition foldable smartphone even won the "Best of Innovation" award at CES 2022, along with Abbott's FreeStyle Libre 3 wearable diabetes monitoring system. These products represent the current state of a convergence of evolving consumer interests with long-developing advancements in enabling technologies, such as materials and processes.

Electrically-conductive inks are one of the long-developing technologies already being utilized in the design and manufacturing of products ranging from smartphones to automotive, medical devices (like MRI imaging vests), and prototype space suits. High-performance electrically conductive inks can be sorted into a few major categories: solids-based inks incorporating materials such as metal or carbon in some form, particle-free metal complex inks, and conductive polymer inks.

Full disclosure: I'm a founding member of NovaCentrix, and our team has developed a range of nanoparticle-metal-based conducting inks going back to the early 2000s. That said, I also see great advancements and opportunities for the other types of inks as well. It's important to note that inks are generally formulated



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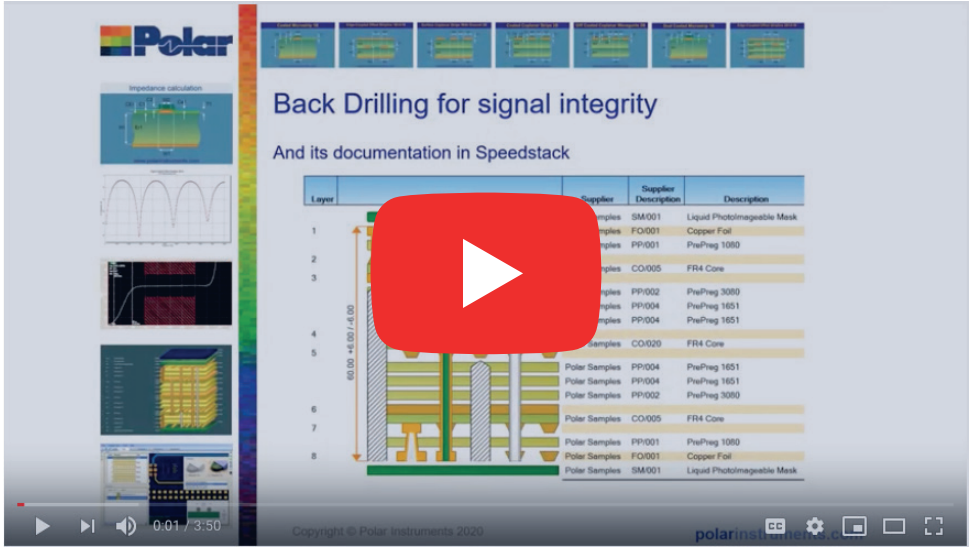

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to be applied with a specific printing technology, and a non-exhaustive list includes screen printing, inkjet, aerosol jet, flexographic, and gravure. Inks are formulated for attributes such as optimal conductive performance, substrate adhesion, shelf stability, and for use in a specific print method.

State-of-the-Art Conductive Inks

While conductive screen-printed pastes—such as for solar cells, or onto polyimide such as for computer keyboards—are not new, 25 years ago the use of conductive inks outside those applications was rare. The DARPA MICE (Mesoscopic Integrated Conformal Electronics) program of the late 1990s and early 2000s dramatically re-evaluated the possibilities of electrically-conductive inks. Since then, the ability to widely and cost-effectively produce new materials such as nanomaterials, and the proliferation of advanced chemistries and polymer science, has led to profound progress demonstrated by modern inks.

Today, the best electrical conductivities are almost on par with that of bulk silver, within a factor of two or three in some cases. Ink formulation chemistries are very advanced and now allow excellent adhesion to a wide range of substrates, with specific formulations available for specific substrates. It is fair to say that the conductive inks community has matured substantially in the past 20 years, with new technologies coming to market, and creative and clever people joining this space each year.

Why Use Conductive Inks?

Simply, use of conductive inks can allow designers to think outside of the rigidity box, allowing much broader creative realization. Conductive inks are a form of additive manufacturing and can be applied only where needed, so they offer a very efficient use of materials. Conductive inks can be printed onto a variety of substrate materials, including substrates that are flexible, perhaps have already been processed with layers of added materials, or both. They can be applied with minimal or no impact on any adjacent or previously applied materials, unlike other additive processes for applying conductive materials like electroplating, or subtractive processes like traditional plate and etch.

A number of current electronics products and applications have been enabled by the use of conductive inks, either by design or by economic feasibility. I know many exciting and novel products in the pipeline rely on the use of conductive inks.

So, What's the Catch?

From a performance perspective, conductive inks just don't match the electrical conductivity of etched copper for use in electronics. If the dominant design requirement is maximum electrical conductivity in a very small area or volume, then traditional etched or plated copper is still likely the right answer. As soon as other design requirements come into play however, such as a requirement for the utilization of flexible or low-temperature substrates, then conductive inks become more viable. The difference in performance of conductive inks means that inks are not simply a plug-and-play swap for etched or plated alternatives. Circuits must be designed from the start based on the electrical properties of the inks.

Using the inks is not just about the inks themselves. Successful utilization depends on printing equipment capable of dispensing the right type and formulation. Often the inks also require post-processing to effectively dry and sinter them. Again, as full disclosure, NovaCentrix developed the PulseForge tools as a unique class of thermal processing equipment specifically for sintering conductive inks on temperature-sensitive substrates. An evolution of the PulseForge tools is now being used for soldering on temperature-sensitive substrates. Also, successful utilization of conductive inks requires well-trained staff who have the expertise to design and manufacture products utilizing conductive inks, including selecting and

operating the equipment, and troubleshooting at every step of the process.

Looking Ahead

The continued convergence of evolving markets and further refinement in the direct and associated technologies of conductive inks builds an opportunity that some will find compelling. Who will it be? Will current electronics designers and manufacturers expand their core competencies to include conductive inks and associated technologies? Will the growing ecosystem of flexible electronics organizations and individuals, such as members of the OE-A (the largest international association dedicated to the space), expand their scope and capabilities into historically traditional EMS/SMT provider arenas?

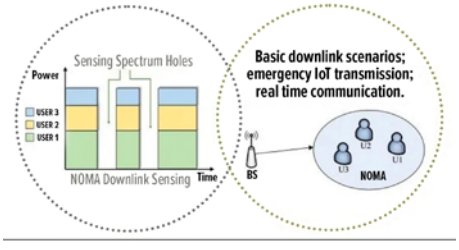
So far, the adoption leaders are the product companies themselves. Our largest adopters are OEMs that have designed conductive inks into their products, and we are working directly with them and their Tier 1 suppliers. In most cases though, imposed confidentiality by the OEMs prevents the ink providers from announcing many details regarding specific customers and application cases. So, for now at least, who is using them? That's the secret. **DESIGN007**

Stan Farnsworth is chief marketing officer with PulseForge and a founder of NovaCentrix.

Researchers Develop Novel Spectrum Sensing Technique for 6G-oriented Intelligent IoT Communications

With the explosive growth of the spectrum demand of the Internet of Things (IoT), Non-orthogonal Multiple Access (NOMA) and spectrum sensing are considered as key candidate technologies to improve spectrum utilization in next generation wireless communications technology. However, given the complexity of future IoT scenarios, it brings new challenges on how to ensure the performance of spectrum utilization and system throughput in large-scale IoT scenarios when using both technologies at the same time.

Motivated by such a challenge, a joint research team from the Shanghai Advanced Research Institute (SARI) of the Chinese Academy of Sciences, VTT Technical Research Centre of Finland and University of Windsor of Canada, creatively proposed a novel spectrum sensing technique for 6G-oriented intelligent IoT communications, seeking a feasible way to provide underlying support for perceptual interference and intelligent identification between large-scale coexistence and aliasing IoT users in future 6G scenarios.



Schematic diagram of download link hybrid IoT sensing scene and an illustration for frequency band occupancy status. (Image: SARI)

Focused on inter-system orthogonal/non-orthogonal aliasing coexistence scenarios, the researchers designed a multi-layer spectrum sensing technology based on feature detection in NOMA scenarios with multi-users. The corresponding rational workflows and transceiver structures according to different scenarios were presented, and the threshold expressions were deduced accordingly.

Oriented towards the upcoming 6G complicated scenarios, the researchers designed one downlink mode and two uplink modes to describe relationships among users' priorities, power, and transmission forms.

Based on the characteristics of each mode, they further customized the detection probability optimization algorithm according to the characteristics of each scene, so that the proposed technology can effectively improve the detection probability of orthogonal/non-orthogonal hybrid IoT systems and improve the overall system throughput.

(Source: Chinese Academy of Sciences)

The Chameleon of Interconnection Technologies

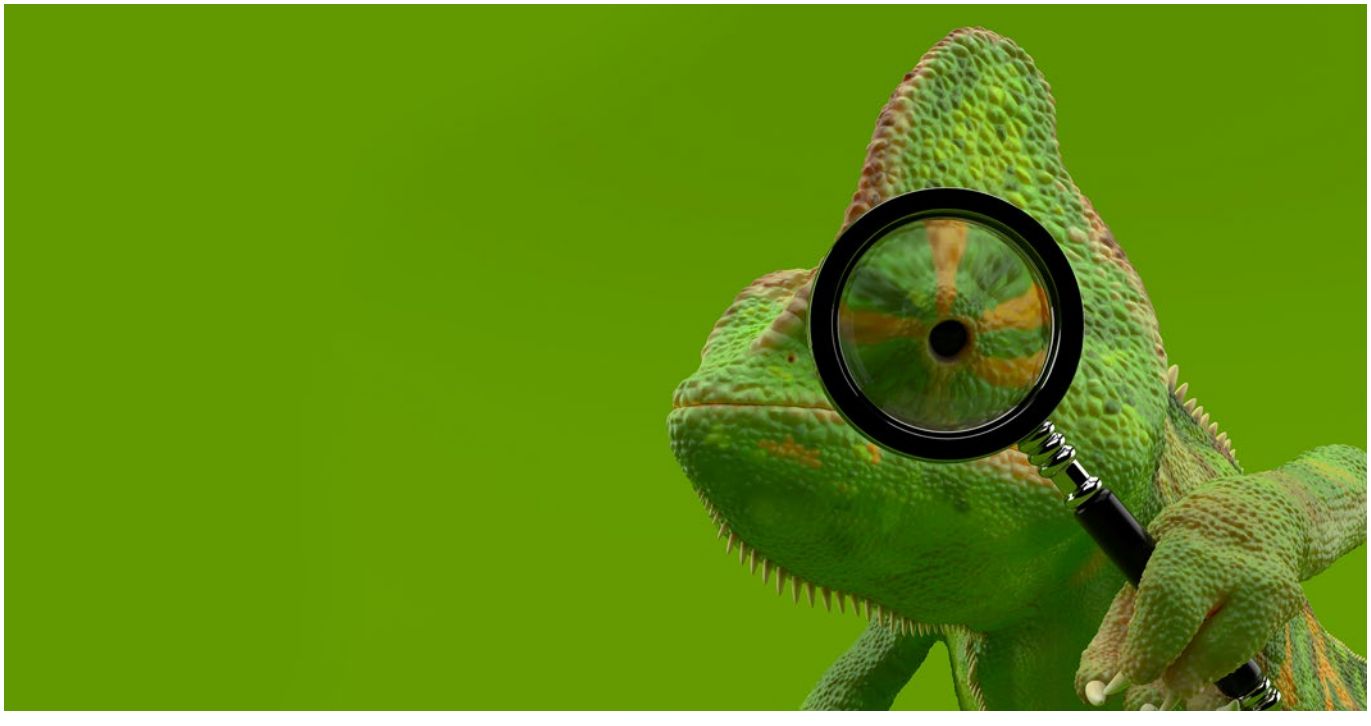
Flexible Thinking

by Joe Fjelstad, VERDANT ELECTRONICS

Flexible circuits are arguably the first instantiation of electronic interconnections. A flexible interconnection structure was first disclosed in patent literature by Albert Hansen—unearthed by gifted researcher, innovator, and self-described technology generalist Dr. Ken Gilleo[1]. The roots of flexible circuits, as determined by the patent Gilleo uncovered, date back to a 1903 British patent issued to Albert Hansen of Germany, entitled "Improvements in, or Connected with, Electric Cables and the Joining of Same." The invention was designed to serve the new world of telephony and improve interconnection design.

Hansen was an amazingly prescient inventor who not only appears to have anticipated the flexible interconnections the industry relies so heavily on, but in a later disclosure, something that looks very much like a multilayer circuit of sorts. In the beginning, the flexibility of the circuit enabled the user to utilize all three dimensions of space to accomplish their design for interconnection needs. Today this continues to be an objective of all interconnections with 3D having become a watchword in electronic design at every level—from semiconductor chips and chip-lets to forklift installed systems—all of which take advantage of flexible circuit technology.

Since Hansen's invention, a hallmark measure of flexible circuits is how they have become a ubiquitous chameleon-like technology for



electronics, capable of adapting and facilitating the myriad changes required to build the dizzying array of electronic devices that have come to enhance and improve our lives—even as they increasingly invade life in general. Like a chameleon, these circuits largely stay out of sight and remain invisible to the user. We are not just surrounded and laden with electronics, we increasingly wear them as flexible circuits. We have even changed the way we refer to them, not as simply flex circuits but as flexible electronics and flex hybrid electronics.

Like a chameleon, these circuits largely stay out of sight and remain invisible to the user.

While traditional flexible circuit technologies will likely continue to serve the needs of designers in established roles such as electrical and electronic cables, they are also enabling and pervading a fascinating range of new personal products. Note: The flex circuit technology getting ever greater use and attention these days was historically called polymer thick film technology (PTF). Polymer thick film is currently being rebranded as flexible electronics (FE) and flex hybrid electronics (FHE)[2]. Regardless, the printing of electronic conductors has been in the tool chest of circuit designers for nearly three quarters of a century. Once largely relegated to the production of PTF membrane switches, which serve nearly every imaginable type of electromechanical machine interface, the printing of conductors has been paired with a wide range of substrates because the printing and joining technologies used in manufacture do not require the high temperatures associated with soldering.

As well, for some time there have been semiconductor chips increasingly thinned to the point where they can be bent without fracturing, attached to the flexible base film, and interconnected directly to the circuits. This solution has been thoroughly embraced at NextFlex and it opens doors to products that can conform to the contours of the product being served, arguably in the same way that the chameleon adapts its appearance to mimic its surroundings. In that regard, most flexible circuits are "invisible," hidden from the view of the user. We see this with electronic textiles, and I expect this trend to increase as more designers conceive of clever products to tempt consumers, whether for vanity, utility, or a combination. It may well be the addition of textile-based circuits that will allow clever designers to create adaptive, wearable camouflage for the military that helps keep future war fighters out of enemy sights. Now that would most definitely be a worthy demonstration of a flex circuit's chameleon nature.

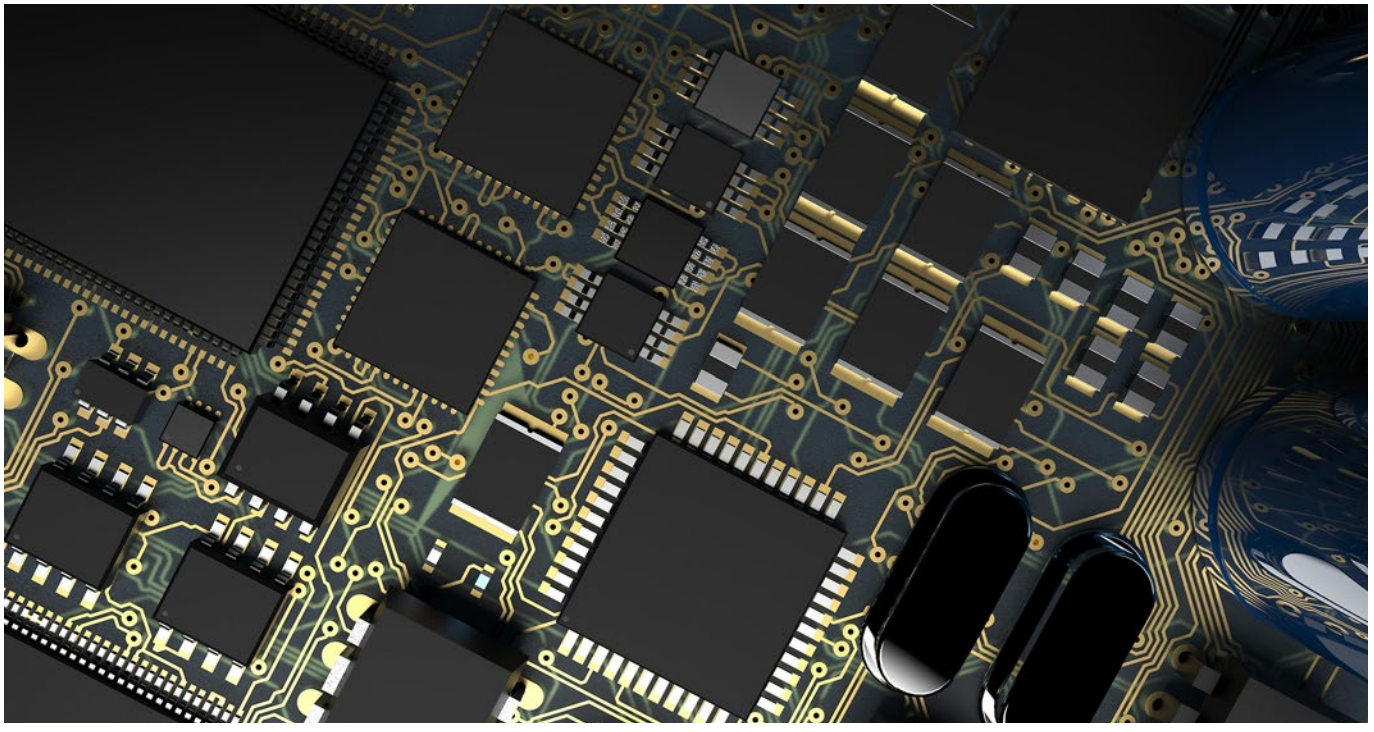
In summary, flexible circuits, regardless of the terminology used to describe them, are enabling an untold number of new products, performing their illusory magic flawlessly and unobtrusively. We can expect to see them (or not) in products long into the future. **DESIGN007**

References

1. "The First 105 Years of Flexible Circuitry," by Ken Gilleo.

2. To learn more, I recommend reading "The Chip Shortage Leads to Innovation," by Dr. Malcolm Thompson, NextFlex, September 2022, *Design007 Magazine*.

Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185 patents issued or pending. To read past columns or contact Fjelstad, click here. Download your free copy of Fjelstad's book *Flexible Circuit Technology, 4th Edition,* and watch his in-depth workshop series "Flexible Circuit Technology."



The Printed Electronics Roundtable, Part 3

Interview by Andy Shaughnessy
I-CONNECT007

We recently conducted a roundtable with a team of printed electronic circuit experts from companies that run the gamut: John Lee and Kevin Miller of Insulectro, Mike Wagner of Butler Technologies, Tom Bianchi of Eastprint, and John Voultos of Sheldahl Flexible Technologies.

In the first part of this roundtable, the team dispelled a variety of myths surrounding PEC. In the second part of the roundtable, the participants discussed what designers and fabricators need to know to jump into printed electronics, and some of the drivers behind this growing technology.

In this third and final installment of the roundtable, these experts discuss some of the differences and similarities between PEC and traditional PCB processes, the future of printed electronic circuits, and why the best way to learn about this technology is through networking with veterans of this segment who are eager to share their expertise with the next generation.

Mike Wagner: Andy, another myth I hear is that printed electronics has not arrived yet. But depending on what you look at, there have been PEC heaters and electroluminescent lamps in cars for years. Diabetes test trips have been around a long time. Those are printed electronics. Diagnostic strips have been around for years. It's there, but either people don't realize or they're just starting to classify it as such. I see it starting to bloom across industries and technologies.

Kevin Miller: We're working with DuPont on some inks that will potentially cross over to PCB since we know both technologies and we know their process. There are some resistor inks that will take out a lot of steps in making a printed circuit board. There are polyimide coverlay prod-

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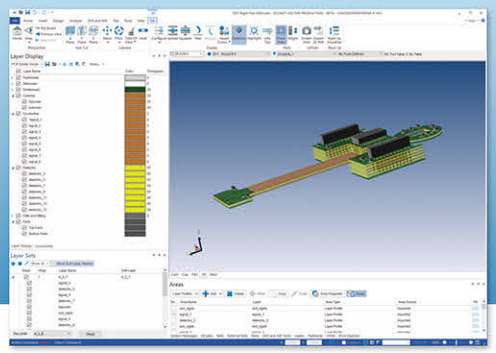

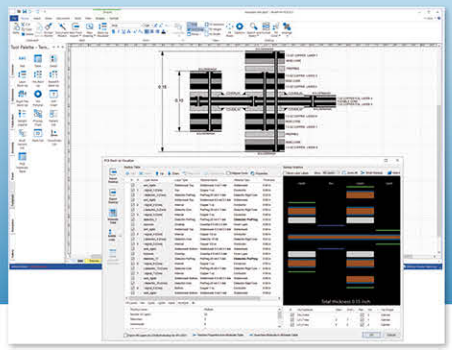

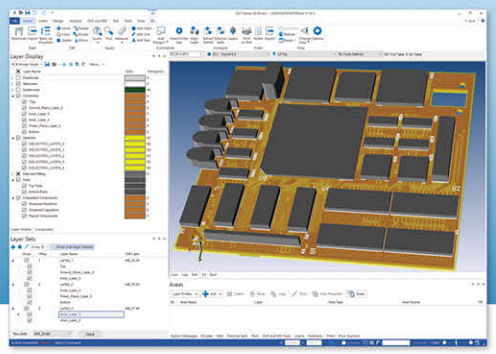

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Mike Wagner

Kevin Miller

John Voultos

ucts that we're working on. We're not there yet, but there are applications that are looking for it.

John Lee: Andy, where do you think printed electronics will go in 20 years?

Andy Shaughnessy: That's what this is all about, really. We're trying to wrap our own heads around this. Like I said, we get inquiries from the readers and it's just one of these things where I don't have a handy expert on PEC to recommend. We do see a lot of action in flexible screens.

Wagner: Flexible screens are everywhere. Sensitive touch and sensing everywhere, garments that can do just about anything as far as sensing remote healthcare. It's going that way now. It's just going to get better.

Lee: Mike, do you think that's replacing PCBs or is it growing in parallel?

Wagner: It's growing in parallel because even if you do a flexible display, you still may need a PCB in some other part of the equipment, but it could be a copper flex circuit or it could be a printed circuit. It depends on how they develop all the other printed components: resistors, capacitors, memory, storage, batteries, etc.

Tom Bianchi: There's one example on YouTube that illustrates the future of printed electronic applications. It's a color-changing BMW that has the E-ink technology integrated onto it.

Miller: They had that car at LOPEC. It was really neat how it just went from white to dark.

Bianchi: The benefit of working for our parent company Flex, which is an EMS company, is seeing and hearing what the industry is shifting toward. Clearly, electronics is ending up in places that we traditionally haven't seen or experienced. So, if you think about the future of cars, it's autonomous, electrified, smaller, and it will have more electronics.

Well, where will you put all the electronics? How will you bend and curve them? A printed circuit board, by nature, doesn't bend and curve. Printed electronics, etched copper, is clearly the future of this industry that we're playing in. Just look at the nature of appliances over the years, how they've evolved and changed. It's just a start. I really do believe that we're just touching the beginning.

It's about the industry coming together to

develop the solutions. That's why the printed circuit board industry has been so successful—they all worked together, and they developed standards. This elevates that industry every day. We've done a good job with printed electronics, but I think we could do better.

John Lee

Wagner: You're dealing with a whole generation of folks who are used to touch and different form factors than we were. I grew up with the "boxiness" of cars. This generation is not expecting that. They want to see something different, more interfacing with the operator.

Bianchi: How did Elon Musk describe the Tesla? A computer on wheels. I got my first chance to drive in one. Personally, I didn't like it because it was not what I want in a car. I'm used to driving something that feels like and acts more like a car. Well, I would bet the first time somebody who was used to a landline phone and then switched over to a smartphone probably said that it didn't act like a phone, but then adapted and started seeing this as the norm.

It's just a matter of time as things evolve, and this is the technology to solve that problem. Flexible technology is coming and it's just taken a little while. It's not that it hasn't happened. I think all of us would say that we have successful business from it, but there's more to come.

Miller: Yes. We participate heavily in the printed circuit board flexible market, and we see our flex circuitry sales experience about 10% growth every year. It usually outpaces what the rest of the industry is doing, as more products that used to be on a rigid application are now on a flexible one. You may have a high temperature with the flexible polyimide, but you could also do some of that with polyester printed electronics.

Shaughnessy: This has been great. Let's go around the table and share any advice you might have for PCB engineers or anyone else who wants to get into PEC.

Wagner: We talked earlier about how people get into printed electronics. You must network with everybody who partakes in this, because the technology really has a collaborative feel at this point. The technology is moving rapidly and there's a lot of expertise, but you can't necessarily have it all in-house. You must reach out and make use of your suppliers, your whole ecosystem of suppliers and partners. I recommend that you don't close yourself off, but really get involved with the industry and your partners—and even friendly competitors like Tom. We can talk if we need to.

Bianchi: Yes, I agree. I enjoyed spending pre-pandemic time with all these guys, John and Mike, even though we're "competitors." The biggest thing that I've seen from the printed circuit board folks and some of your readers is that getting a design and a cost for a printed electronic project is vastly different than getting one for a printed circuit board. There isn't a per-square-inch price that can be created to do a printed electronic, like you do with two layers, four layers, eight layers or whatever the case might be. Printed electronics is a little more of an engineered solution at this point.

Shaughnessy: Is it like the Wild West now?

Bianchi: There are just different material sets, requirements, and equipment sizes. There's a lot that goes into it.

Shaughnessy: John, what do you think?

Voultos: I'm going to build off what Mike and Tom said. I do believe it's strongly about working together and leveraging your suppliers. They're developing some new technologies that are usually ahead of the curve and you should leverage them as best you can. But at the same time, there's opportunity. I know Butler and Sheldahl work together and leverage the capabilities for each other.

Tom Bianchi

It's not really the Wild West. That, to me, means being at the very beginning. This industry has existed for years in the shadows. That's probably a good way to say it. I really do believe this is the technology. People are looking at their product and trying to evolve it. We use the term "from ordinary to extraordinary."

We're taking something rather flat and ordinary, and then making something extraordinary by bending, curving, and putting it in places where electronics haven't existed before. That's a key element. It's in the shadows, but as you're seeing more of these products come out, you will see more of these electronics become very much like from the circuit board industry stance. That's my two cents. I enjoy working with these three gentlemen, but I miss speaking to Tom the most, even though he's technically a competitor.

Bianchi: We need to get another in-person conference.

Voultos: I know we do. I need to at least come visit you.

Shaughnessy: Kevin, any final words?

Miller: I haven't been in this segment as long as John, Mike, and Tom, but I have seen it evolve over the past seven years that I've been involved. There are a lot of new technologies coming out, whether it's IME or wearables, some of these resistor-type inks. There's definitely a lot of development work happening from the suppliers to bring on new technologies. We truly believe there will be a crossover between the two industries and there will be companies that will be doing both.

The sad part is that we had a yearly trade show called IDTechEx, which was canceled because of COVID, so there's not a yearly get-together like we have in the printed circuit board business, which is IPC APEX EXPO. Maybe the guys in printed electronics or the manager of IDTechEx could develop a conference that's part of APEX EXPO, because there are a lot of similarities. A lot of it has to do with circuitry and assembly as well.

Shaughnessy: Good, thank you for doing this.

Voultos: Thank you, Andy. Good to talk with you guys again. Let's meet up in person soon.

Bianchi: Definitely. This has been great. **DESIGN007**

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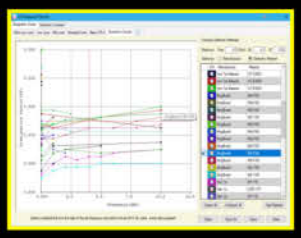

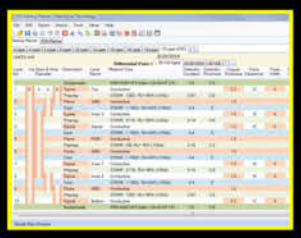

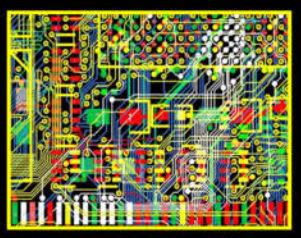

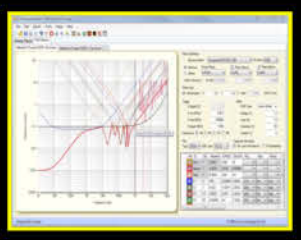

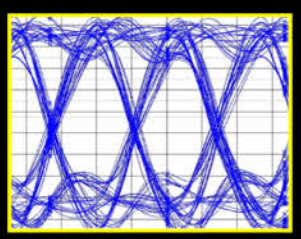

A Comprehensive Report Includes:

Material Selection for Cost/Performance to Required Frequency and Bandwidth, Design Constraint Review

Stackup Impedance Analysis, Single-ended, Differential Pairs and CPW Blind and Buried Via Definition, Reference Plane Assignment Validation

Critical Placement and Routing, Plane Pour Definitions, Return Current Paths, Plane Cross-overs and Broadside Coupling Review

PDN Analysis - Minimizes AC Impedance, Decap Selection, Mounting Inductance Analysis, Plane Resonance Dampening

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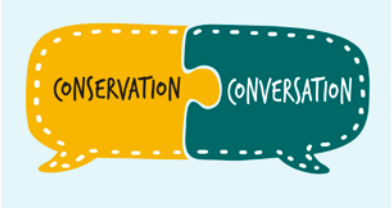
TOP TEN

EDITOR'S PICKS

Altium's EDDI Report Tracks Components' Availability—Today and Historically

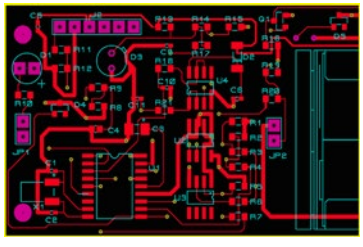
There's one lesson that all designers have learned over the past few years: Components might be here today and gone tomorrow, so tracking your parts is more important than ever. Any resources that help you keep tabs on your required parts are invaluable in these days of 40-week lead times.

Material Conservation: The PCB Designer's Role



During these times of supply chain uncertainty, many product developers are considering new ways to conserve materials—from laminates to components, layer reduction, and everything in between. Barry Matties and Happy Holden recently spoke with Alun Morgan, president of EIPC and technology ambassador for Ventec, about material conservation strategies for today's PCB designers and design engineers.

Elementary, Mr. Watson: Anatomy of Your Component—Footprint, Part 2



Have you ever gone to a buffet hungry and looking forward to digging in? You get to the end of the buffet, but there's no room on your plate for the good stuff. At this point, you probably feel much like that with the first part of looking at our footprint, but rest assured, although your plate is already full, the good stuff is still waiting for us.

The Shaughnessy Report: Working Through the Design Pain

In a recent issue of *SMT007 Magazine,* we discussed "supply pain management." This reminded us of the question that doctors often ask: "What's your pain level on a scale of 1–10?" PCB designers really deserve a lot of credit. For years, they've been working through supply chain pain, like Rip Wheeler after he got shot on "Yellowstone." It hurts, but we're short on cowboys, so get back to work.

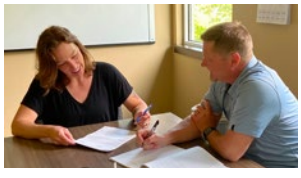
Ventec Thermal Management Book Excerpt: Chapter 1

Regarding basic principles of thermal dissipation there are three ways of dissipating energy: Conduction, convection, and radiation. The integrated metal substrate (IMS) printed circuit boards rely predominantly on heat conduction all the way through the different layers of the substrates from a hot point (the base of the component) to a cold point (the furthest surface of the metal base) and, usually, thereafter, through a dissipator.

Sensible Design: Comparing Traditional and Bio-based Resins

In this month's column, two of Electrolube's leading resin specialists have collaborated to give you the clearest focus of how introducing bio-based resins systems will impact your production process and the benefits they bring in terms of performance.

Connect the Dots: Examining the Benefits of Laser Direct Imaging



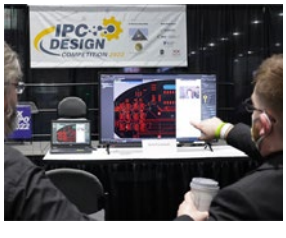
One of the most amazing advances in PCB manufacturing technology has been the advent and usage of laser direct imaging (LDI) technology. Though the LDI revolution began more than 20 years ago, there's still room for more PCB manufacturers to invest in this powerful tool.

A New Sourcing Paradigm

We've seen many changes over the past few years, and nowhere are they more evident than in the world of sourcing components. Sourcing has become one of the biggest challenges facing PCB designers and design engineers today.

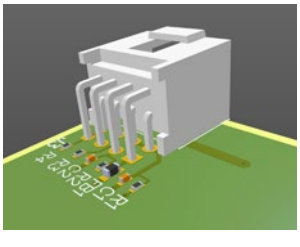
PCB Designers to Vie for Design Champion Title at IPC APEX EXPO 2023

For the second consecutive year, IPC is hosting an IPC Design Competition, inviting printed circuit board designers to compete to become the IPC Design Champion of 2023.



Target Condition: Practical Packaging Density in PCB Design

Just as I tend to exhibit discomfort in oversized conference halls and meeting rooms, I self-diagnose as agoraphobic when it comes to entering PCB layouts full of wasted space. Mechanical constraints which utilize the printed circuit board substrate material as a mechanical or structural "filler" within an electronic product, under-utilizing the material for its intended purpose to support conductive circuitry, grate on me like nails on a chalkboard.



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- Provide electrical/control support to customer service
- May require occasional travel and overtime

Qualifications:

- Bachelor's degree in electrical engineering or an EMET degree
- Machine control design experience a plus
- Good communication skills working in a team environment
- Strong ability to work independently with minimal supervision
- PLC and HMI experience a plus (ex. Studio 5000 Logix Designer, Factory Talk)
- Experience with AutoCAD, Microsoft Word, and Excel

Chemcut benefits include: Medical, dental and vision Insurance, life and disability insurance, paid vacation and holidays, sick leave accrual, and 401K with company match.

To apply, please submit a cover letter and resume to hr@chemcut.net.

apply now

EMA Design Automation®

Technical Marketing Engineer

EMA Design Automation, a leader in product development solutions, is in search of a detail-oriented individual who can apply their knowledge of electrical design and CAD software to assist marketing in the creation of videos, training materials, blog posts, and more. This Technical Marketing Engineer role is ideal for analytical problem-solvers who enjoy educating and teaching others.

Requirements:

- Bachelor's degree in electrical engineering or related field with a basic understanding of engineering theories and terminology required
- Basic knowledge of schematic design, PCB design, and simulation with experience in OrCAD or Allegro preferred
- Candidates must possess excellent writing skills with an understanding of sentence structure and grammar
- Basic knowledge of video editing and experience using Camtasia or Adobe Premiere Pro is preferred but not required
- Must be able to collaborate well with others and have excellent written and verbal communication skills for this remote position

EMA Design Automation is a small, family-owned company that fosters a flexible, collaborative environment and promotes professional growth.

Send Resumes to: resumes@ema-eda.com

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Career Opportunities

TAIYO AMERICA

Field Service Technician

Taiyo Circuit Automation designs and manufactures the world's finest dual sided soldermask coating and vertical drying equipment. Since 1981, we have served the printed circuit board industry with highly reliable innovative machinery, engineered to exceed.

PRIMARY FUNCTION:

The Field Service Technician is responsible for troubleshooting and providing technical services on Taiyo Circuit Automation's mechanical and electro-mechanical products and systems.

ESSENTIAL DUTIES:

1. Identify mechanical issues and implement process control solutions for process improvement and new projects
2. Consult with maintenance, operations, engineering, and management concerning process control and instrumentation
3. Specify, install, configure, calibrate, and maintain instrumentation, control system and electrical protection equipment

QUALIFICATIONS/SKILLS:

1. 3 years of experience with equipment, preferably in PCB or related electronics industry
2. 3 years of experience in similar process industries with hands-on experience in operations, maintenance and project implementation—OMRON, Koyo, Allen Bradley experience preferred
3. Experience in installation and calibration of process control elements and electrical measurement devices
4. The ability to read and understand electrical, pneumatic diagrams and control systems

REQUIRED EDUCATION/EXPERIENCE:

1. High school graduate
2. Associate degree in Industrial Engineering Technology, Mechanical or Electrical Engineering, preferred.
3. PLC experience

Email: BobW@Taiyo-america.com (Subject: "Application for Field Service Technician for TCA")

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Altium®

DevOps Engineer

Altium is a publicly traded global company responsible for the most widely used PCB design software in the industry. Altium 365® is our cloud-based design and collaboration platform; it gives more power to every contributor in the electronics product chain, from the PCB designers to manufacturing. Our R&D teams are the driving force behind Altium 365 and all our technological accomplishments.

- The primary role of the DevOps Engineer is to help continue our transition to a cloud-based SaaS model as part of the production engineering team
- The team's top priorities are product reliability, security, feature delivery, and automation
- DevOps is responsible for the CI/CD process, streamlining automation for provisioning and deployment, scalable infrastructure, uninterrupted service, other DevOps activities

Required Skills and Experience:

- Analysis, troubleshooting
- 4+ years' DevOps/SRE/ Linux/Windows
- AWS (EC2, RDS, S3, Storage, Route53, and network appliances
- Architecting and securing cloud networking

Altium offers a culture built and managed by engineers. We don't micromanage; we define the goals and give engineers the freedom and support to explore new ideas for delivering results. In doing so, we all have a hand in shaping the future of technology.

https://careers.altium.com/

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Career Opportunities

Supplier Quality Manager

Headquarters, New Hartford, NY

JOB SUMMARY:
The Supplier Quality Manager is responsible for maintaining and improving the quality of Indium Corporation's supplier base as well as compliance with identified quality standards and risk mitigation. This position will work cross-functionally with Supply Chain, Operations, and our suppliers. The role will ensure that the quality levels of all Indium Corporation suppliers and products meet customer requirements while supporting the company's growth, vision, and values.

REQUIREMENTS:
- Bachelor's degree in business, supply chain or a science-based discipline
- Minimum 3 years in a supply chain role supporting or leading supplier quality
- Obtain and/or maintain International Automotive Task Force (IATF) auditor certification within first 3 months of employment
- Able to work independently or lead a team, as needed, to meet goals
- Excellent oral and written communication skills
- Knowledge of quality standards
- Proficiency in MS Office

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Technical Service & Applications Engineer

Full-Time — Midwest (WI, IL, MI)

Koh Young Technology, founded in 2002 in Seoul, South Korea, is the world leader in 3D measurement-based inspection technology for electronics manufacturing. Located in Duluth, GA, Koh Young America has been serving its partners since 2010 and is expanding the team with an Applications Engineer to provide helpdesk support by delivering guidance on operation, maintenance, and programming remotely or on-site.

Responsibilities
- Provide support, preventive and corrective maintenance, process audits, and related services
- Train users on proper operation, maintenance, programming, and best practices
- Recommend and oversee operational, process, or other performance improvements
- Effectively troubleshoot and resolve machine, system, and process issues

Skills and Qualifications
- Bachelor's in a technical discipline, relevant Associate's, or equivalent vocational or military training
- Knowledge of electronics manufacturing, robotics, PCB assembly, and/or AI; 2-4 years of experience
- SPI/AOI programming, operation, and maintenance experience preferred
- 75% domestic and international travel (valid U.S. or Canadian passport, required)
- Able to work effectively and independently with minimal supervision
- Able to readily understand and interpret detailed documents, drawings, and specifications

Benefits
- Health/Dental/Vision/Life Insurance with no employee premium (including dependent coverage)
- 401K retirement plan
- Generous PTO and paid holidays

apply now

Career Opportunities

Electrical Engineer/PCB/CAD Design, BOM/Component & Quality Support

Flexible Circuit Technologies (FCT) is a premier global provider of flex, rigid flex, flex heaters, EMS assembly and product box builds.

Responsibilities:

- Learn the properties, applications, advantages/disadvantages of flex circuits
- Learn the intricacies of flex circuit layout best practices
- Learn IPC guidelines: flex circuits/assemblies
- Create flexible printed circuit board designs/files to meet customer requirements
- Review customer prints and Gerber files to ensure they meet manufacturing and IPC requirements
- Review mechanical designs, circuit requirements, assembly requirements, BOM/component needs/ and help to identify alternates, if needed
- Prepare and document changes to customer prints/ files.
- Work with application engineers, customers, and manufacturing engineers to finalize and optimize designs for manufacturing
- Work with quality manager to learn quality systems, requirements, and support manager with assistance

Qualifications:

- Electrical Engineering Degree with 2+ years of CAD/PCB design experience
- IPC CID or CID+ certification or desire to obtain
- Knowledge of flexible PCB materials, properties, or willingness to learn
- Experience with CAD software: Altium, or other
- Knowledge of IPC standards for PCB industry, or willingness to learn
- Microsoft Office products

FCT offers competitive salary, bonus program, benefits package, and an outstanding long-term opportunity. Location: Minneapolis, Minn., area.

apply now

Regional Manager
Midwest Region

General Summary: Manages sales of the company's products and services, Electronics and Industrial, within the States of KS, MO, NE, and AR. Reports directly to Americas Manager. Collaborates with the Americas Manager to ensure consistent, profitable growth in sales revenues through positive planning, deployment and management of sales reps. Identifies objectives, strategies and action plans to improve short- and long-term sales and earnings for all product lines.

DETAILS OF FUNCTION:

- Develops and maintains strategic partner relationships
- Manages and develops sales reps:
  - Reviews progress of sales performance
  - Provides quarterly results assessments of sales reps' performance
  - Works with sales reps to identify and contact decision-makers
  - Setting growth targets for sales reps
  - Educates sales reps by conducting programs/ seminars in the needed areas of knowledge
- Collects customer feedback and market research (products and competitors)
- Coordinates with other company departments to provide superior customer service

QUALIFICATIONS:

- 5-7+ years of related experience in the manufacturing sector or equivalent combination of formal education and experience
- Excellent oral and written communication skills
- Business-to-business sales experience a plus
- Good working knowledge of Microsoft Office Suite and common smart phone apps
- Valid driver's license
- 75-80% regional travel required

To apply, please submit a COVER LETTER and RESUME to: Fernando Rueda, Americas Manager

fernando_rueda@kyzen.com

apply now

Career Opportunities

pluritec®

MACHINES FOR PRINTED CIRCUIT BOARDS

Field Service Engineer

Location: West Coast, Midwest

Pluritec North America, ltd., an innovative leader in drilling, routing, and automated inspection in the printed circuit board industry, is seeking a full-time field service engineer.

This individual will support service for North America in printed circuit board drill/routing and X-ray inspection equipment.

Duties included: Installation, training, maintenance, and repair. Must be able to troubleshoot electrical and mechanical issues in the field as well as calibrate products, perform modifications and retrofits. Diagnose effectively with customer via telephone support. Assist in optimization of machine operations.

A technical degree is preferred, along with strong verbal and written communication skills. Read and interpret schematics, collect data, write technical reports.

Valid driver's license is required, as well as a passport, and major credit card for travel.

Must be able to travel extensively.

apply now

Manncorp™

SMT Field Technician
Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:

- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:

- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
- Ability to arrange and schedule service trips

We Offer:

- Health and dental insurance
- Retirement fund matching
- Continuing training as the industry develops

apply now

Career Opportunities

ventec INTERNATIONAL GROUP 騰輝電子

European Product Manager
Taiyo Inks, Germany

We are looking for a European product manager to serve as the primary point of contact for product technical sales activities specifically for Taiyo Inks in Europe.

Duties include:

- Business development & sales growth in Europe
- Subject matter expert for Taiyo ink solutions
- Frequent travel to targeted strategic customers/OEMs in Europe
- Technical support to customers to solve application issues
- Liaising with operational and supply chain teams to support customer service

Skills and abilities required:

- Extensive sales, product management, product application experience
- European citizenship (or authorization to work in Europe/Germany)
- Fluency in English language (spoken & written)
- Good written & verbal communications skills
- Printed circuit board industry experience an advantage
- Ability to work well both independently and as part of a team
- Good user knowledge of common Microsoft Office programs
- Full driving license essential

What's on offer:

- Salary & sales commission--competitive and commensurate with experience
- Pension and health insurance following satisfactory probation
- Company car or car allowance

This is a fantastic opportunity to become part of a successful brand and leading team with excellent benefits. Please forward your resume to **jobs@ventec-europe.com.**

apply now

MivaTek Global

Field Service Technician

MivaTek Global is focused on providing a quality customer service experience to our current and future customers in the printed circuit board and microelectronic industries. We are looking for bright and talented people who share that mindset and are energized by hard work who are looking to be part of our continued growth.

Do you enjoy diagnosing machines and processes to determine how to solve our customers' challenges? Your 5 years working with direct imaging machinery, capital equipment, or PCBs will be leveraged as you support our customers in the field and from your home office. Each day is different, you may be:

- Installing a direct imaging machine
- Diagnosing customer issues from both your home office and customer site
- Upgrading a used machine
- Performing preventive maintenance
- Providing virtual and on-site training
- Updating documentation

Do you have 3 years' experience working with direct imaging or capital equipment? Enjoy travel? Want to make a difference to our customers? Send your resume to N.Hogan@MivaTek.Global for consideration.

More About Us

MivaTek Global is a distributor of Miva Technologies' imaging systems. We currently have 55 installations in the Americas and have machine installations in China, Singapore, Korea, and India.

apply now

Career Opportunities

INSULECTRO

Are You Our Next Superstar?!

Insulectro, the largest national distributor of printed circuit board materials, is looking to add superstars to our dynamic technical and sales teams. We are always looking for good talent to enhance our service level to our customers and drive our purpose to enable our customers build better boards faster. Our nationwide network provides many opportunities for a rewarding career within our company.

We are looking for talent with solid background in the PCB or PE industry and proven sales experience with a drive and attitude that match our company culture. This is a great opportunity to join an industry leader in the PCB and PE world and work with a terrific team driven to be vital in the design and manufacture of future circuits.

apply now

Prototron Circuits

Sales Representatives

Prototron Circuits, a market-leading, quick-turn PCB manufacturer located in Tucson, AZ, is looking for sales representatives for the New England and Northern California territories. With 35+ years of experience, our PCB manufacturing capabilities reach far beyond that of your typical fabricator.

Reasons you should work with Prototron:

- Solid reputation for on-time delivery (98+% on-time)
- Capacity for growth
- Excellent quality
- Production quality quick-turn services in as little as 24 hours
- 5-day standard lead time
- RF/microwave and special materials
- AS9100D
- MIL-PRF- 31032
- ITAR
- Global sourcing option (Taiwan)
- Engineering consultation, impedance modeling
- Completely customer focused team

Interested? Please contact Russ Adams at (206) 351-0281 or russa@prototron.com.

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Career Opportunities

The Test Connection, Inc.

Rewarding Careers

Take advantage of the opportunities we are offering for careers with a growing test engineering firm. We currently have several openings at every stage of our operation.

The Test Connection, Inc. is a test engineering firm. We are family owned and operated with solid growth goals and strategies. We have an established workforce with seasoned professionals who are committed to meeting the demands of high-quality, low-cost and fast delivery.

TTCI is an Equal Opportunity Employer. We offer careers that include skills-based compensation. We are always looking for talented, experienced test engineers, test technicians, quote technicians, electronics interns, and front office staff to further our customer-oriented mission.

Associate Electronics Technician/ Engineer (ATE-MD)

TTCI is adding electronics technician/engineer to our team for production test support.

- Candidates would operate the test systems and inspect circuit card assemblies (CCA) and will work under the direction of engineering staff, following established procedures to accomplish assigned tasks.
- Test, troubleshoot, repair, and modify developmental and production electronics.
- Working knowledge of theories of electronics, electrical circuitry, engineering mathematics, electronic and electrical testing desired.
- Advancement opportunities available.
- Must be a US citizen or resident.

apply now

Test Engineer (TE-MD)

In this role, you will specialize in the development of in-circuit test (ICT) sets for Keysight 3070 (formerly HP) and/or Teradyne (formerly GenRad) TestStation/228X test systems.

- Candidates must have at least three years of experience with in-circuit test equipment. A candidate would develop and debug our test systems and install in-circuit test sets remotely online or at customer's manufacturing locations nationwide.
- Candidates would also help support production testing and implement Engineering Change Orders and program enhancements, library model generation, perform testing and failure analysis of assembled boards, and other related tasks.
- Some travel required and these positions are available in the Hunt Valley, Md., office.

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Sr. Test Engineer (STE-MD)

- Candidate would specialize in the development of in-circuit test (ICT) sets for Keysight 3070 (formerly Agilent & HP), Teradyne/ GenRad, and Flying Probe test systems.
- Strong candidates will have more than five years of experience with in-circuit test equipment. Some experience with flying probe test equipment is preferred. A candidate would develop, and debug on our test systems and install in-circuit test sets remotely online or at customer's manufacturing locations nationwide.
- Proficient working knowledge of Flash/ISP programming, MAC Address and Boundary Scan required. The candidate would also help support production testing implementing Engineering Change Orders and program enhancements, library model generation, perform testing and failure analysis of assembled boards, and other related tasks. An understanding of stand-alone boundary scan and flying probe desired.
- Some travel required. Positions are available in the Hunt Valley, Md., office.

Contact us today to learn about the rewarding careers we are offering. Please email resumes with a short message describing your relevant experience and any questions to careers@ttci.com. Please, no phone calls.

We proudly serve customers nationwide and around the world.

TTCI is an ITAR registered and JCP DD2345 certified company that is NIST 800-171 compliant.

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Career Opportunities

ARLON ELECTRONIC MATERIALS

Arlon EMD, located in Rancho Cucamonga, California, is currently interviewing candidates for open positions in:

- **Engineering**
- **Quality**
- **Various Manufacturing**

All interested candidates should contact Arlon's HR department at 909-987-9533 or email resumes to careers.ranch@arlonemd.com.

Arlon is a major manufacturer of specialty high-performance laminate and prepreg materials for use in a wide variety of printed circuit board applications. Arlon specializes in thermoset resin technology, including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, High Density Interconnect (HDI) and microvia PCBs (i.e. in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001: 2015 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customers' requirements.

For additional information please visit our website at www.arlonemd.com

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eptac

TRAIN. WORK SMARTER. SUCCEED.

Become a Certified IPC Master Instructor

Opportunities are available in Canada, New England, California, and Chicago. If you love teaching people, choosing the classes and times you want to work, and basically being your own boss, this may be the career for you. EPTAC Corporation is the leading provider of electronics training and IPC certification and we are looking for instructors that have a passion for working with people to develop their skills and knowledge. If you have a background in electronics manufacturing and enthusiasm for education, drop us a line or send us your resume. We would love to chat with you. Ability to travel required. IPC-7711/7721 or IPC-A-620 CIT certification a big plus.

Qualifications and skills

- A love of teaching and enthusiasm to help others learn
- Background in electronics manufacturing
- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

Benefits

- Ability to operate from home. No required in-office schedule
- Flexible schedule. Control your own schedule
- IRA retirement matching contributions after one year of service
- Training and certifications provided and maintained by EPTAC

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Career Opportunities

BLACKFOX
Premier Training & Certification

IPC Instructor

Longmont, CO; Phoenix, AZ; U.S.-based remote

Independent contractor, possible full-time employment

Job Description

This position is responsible for delivering effective electronics manufacturing training, including IPC Certification, to students from the electronics manufacturing industry. IPC instructors primarily train and certify operators, inspectors, engineers, and other trainers to one of six IPC Certification Programs: IPC-A-600, IPC-A-610, IPC/WHMA-A-620, IPC J-STD-001, IPC 7711/7721, and IPC-6012.

IPC instructors will conduct training at one of our public training centers or will travel directly to the customer's facility. A candidate's close proximity to Longmont, CO, or Phoenix, AZ, is a plus. Several IPC Certification Courses can be taught remotely and require no travel.

Qualifications

Candidates must have a minimum of five years of electronics manufacturing experience. This experience can include printed circuit board fabrication, circuit board assembly, and/or wire and cable harness assembly. Soldering experience of through-hole and/or surface-mount components is highly preferred.

Candidate must have IPC training experience, either currently or in the past. A current and valid certified IPC trainer certificate holder is highly preferred.

Applicants must have the ability to work with little to no supervision and make appropriate and professional decisions.

Send resumes to Sharon Montana-Beard at sharonm@blackfox.com.

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American Standard Circuits
Creative Innovations In Flex, Digital & Microwave Circuits

CAD/CAM Engineer

Summary of Functions

The CAD/CAM engineer is responsible for reviewing customer supplied data and drawings, performing design rule checks and creating manufacturing data, programs, and tools required for the manufacture of PCB.

Essential Duties and Responsibilities

- Import customer data into various CAM systems.
- Perform design rule checks and edit data to comply with manufacturing guidelines.
- Create array configurations, route, and test programs, panalization and output data for production use.
- Work with process engineers to evaluate and provide strategy for advanced processing as needed.
- Itemize and correspond to design issues with customers.
- Other duties as assigned.

Organizational Relationship

Reports to the engineering manager. Coordinates activities with all departments, especially manufacturing.

Qualifications

- A college degree or 5 years' experience is required. Good communication skills and the ability to work well with people is essential.
- Printed circuit board manufacturing knowledge.
- Experience using CAM tooling software, Orbotech GenFlex®.

Physical Demands

Ability to communicate verbally with management and coworkers is crucial. Regular use of the telephone and e-mail for communication is essential. Sitting for extended periods is common. Hearing and vision within normal ranges is helpful for normal conversations, to receive ordinary information and to prepare documents.

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Career Opportunities

U.S. CIRCUIT

Plating Supervisor

Escondido, California-based PCB fabricator U.S. Circuit is now hiring for the position of plating supervisor. Candidate must have a minimum of five years' experience working in a wet process environment. Must have good communication skills, bilingual is a plus. Must have working knowledge of a plating lab and hands-on experience running an electrolytic plating line. Responsibilities include, but are not limited to, scheduling work, enforcing safety rules, scheduling/maintaining equipment and maintenance of records.

Competitive benefits package.
Pay will be commensurate
with experience.

Mail to:
mfariba@uscircuit.com

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APCT
Passion | Commitment | Trust

APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to
hearing from you soon.

apply now

The Electronics Industry's Guide to... The Evolving PCB NPI Process

by Mark Laing and Jeremy Schitter, Siemens Digital Industries Software

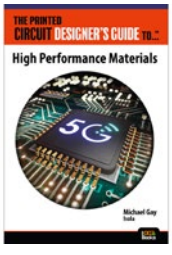
The authors of this book take a look at how market changes in the past 15 years, coupled with the current slowdown of production and delivery of materials and components, has affected the process for new product introduction (NPI) in the global marketplace. As a result, companies may need to adapt and take a new direction to navigate and thrive in an uncertain and rapidly evolving future. Learn how to streamline the NPI process and better manage the supply chain. ***Get it Now!***

I-007eBooks The Printed Circuit Designer's Guide to...

Thermal Management with Insulated Metal Substrates, Vol. 2

by Didier Mauve and Robert Art, Ventec International Group

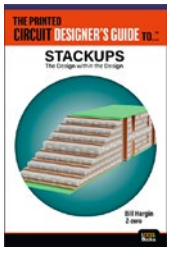
This book covers the latest developments in the field of thermal management, particularly in insulated metal substrates, using state-of-the-art products as examples and focusing on specific solutions and enhanced properties of IMS. **Add this essential book to your library.**



High Performance Materials

by Michael Gay, Isola

This book provides the reader with a clearer picture of what to know when selecting which material is most desirable for their upcoming products and a solid base for making material selection decisions. **Get your copy now!**

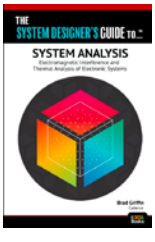


Stackups: The Design within the Design

by Bill Hargin, Z-zero

Finally, a book about stackups! From material selection and understanding laminate data-sheets, to impedance planning, glass weave skew and rigid-flex materials, topic expert Bill Hargin has written a unique book on PCB stackups. **Get yours now!**

The Systems Designer's Guide to... System Analysis



by Brad Griffin, Cadence

In this book, the author, Brad Griffin of Cadence, focuses on EM and thermal analysis in the context of data center electronics systems. Be sure to also **download the companion guide** for end-to-end solutions to today's design challenges.

Our library is open 24/7/365. Visit us at: I-007eBooks.com

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