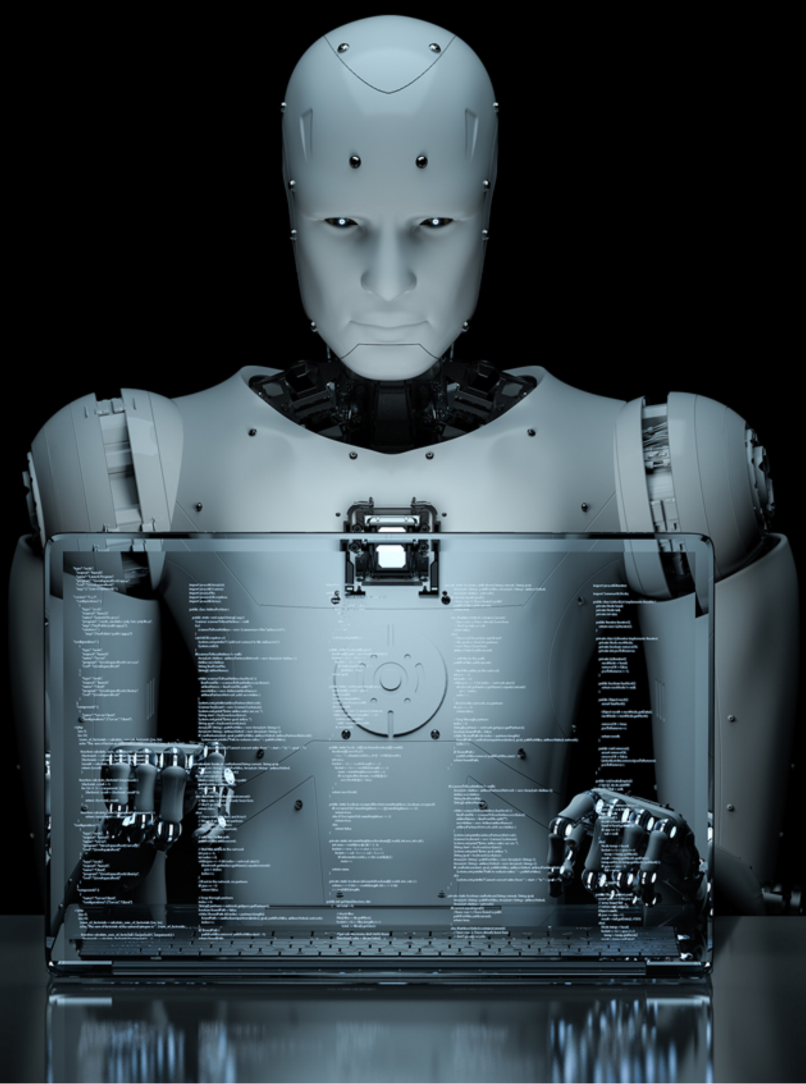
I-Connect007

SEPTEMBER 2018

DESIGN007 MAGAZINE

AI

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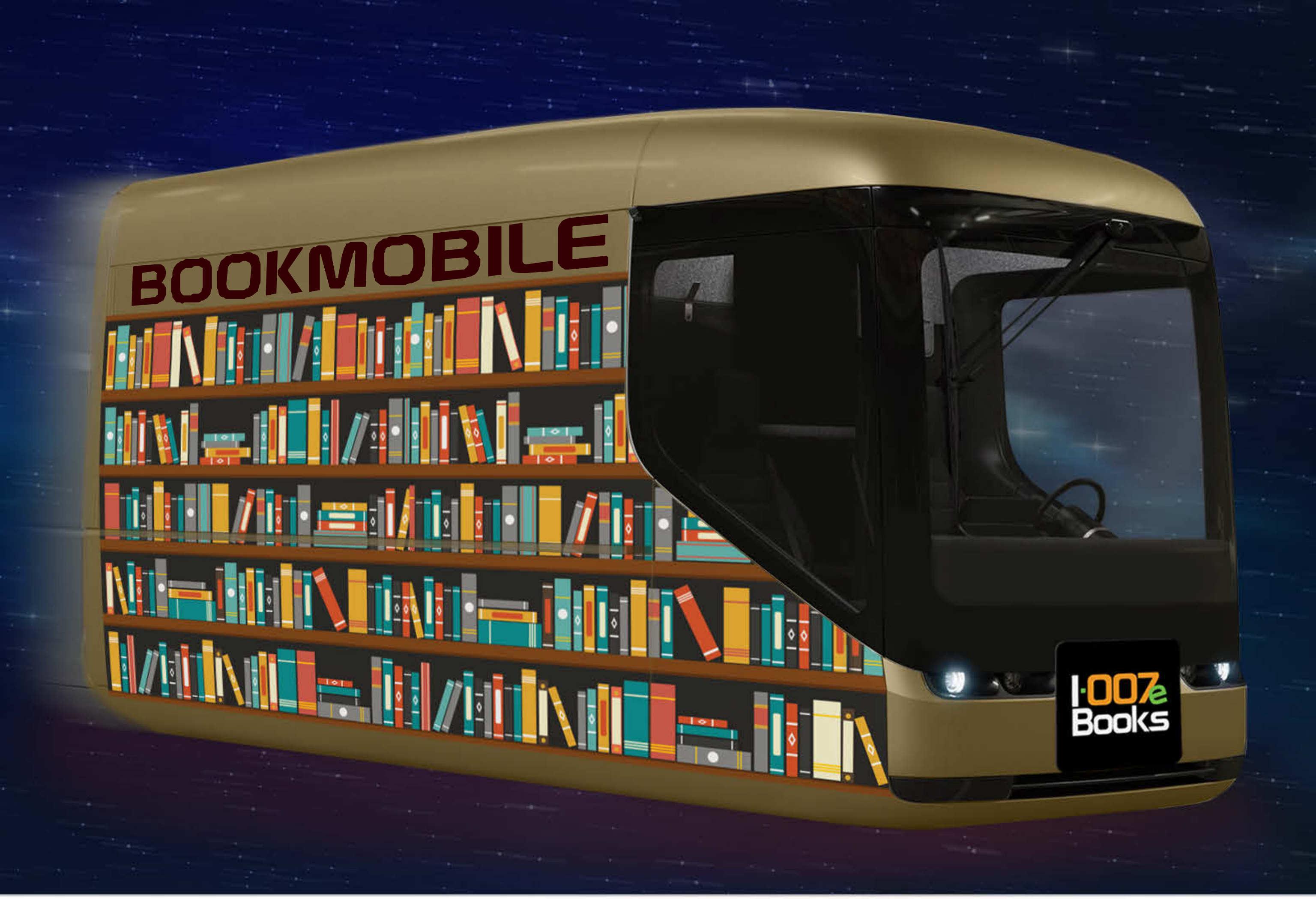
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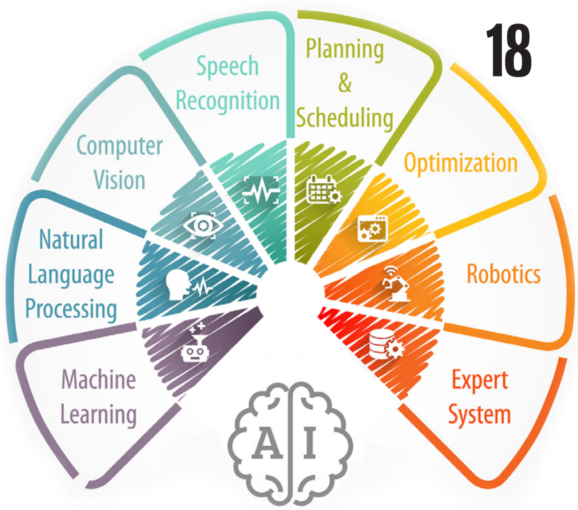
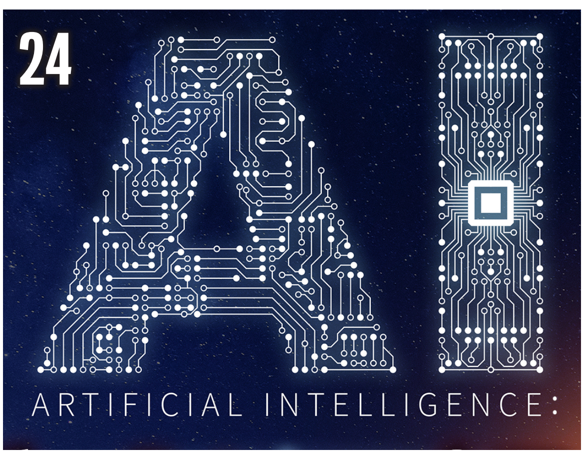
Artificial Intelligence

Artificial intelligence has been grabbing headlines over the past few years. It's one of the hotter segments to watch, especially with drones, robots, autonomous vehicles and virtual reality applications becoming more popular every day. What does AI mean for PCB designers and their EDA tools? This month, we asked our expert contributors to discuss AI and what it might mean to PCB design and the rest of the electronics industry.





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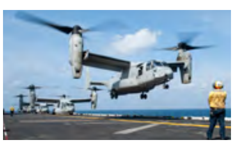

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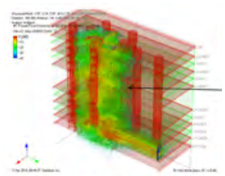


COLUMNS:

AI at the Crossroads

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

(Source: WikiCommons)

I don't know about you, but every time I hear the term artificial intelligence, it still reminds me of HAL 9000, the computer that took over the Discovery One spaceship in 2001: A Space Odyssey.

I always secretly rooted for HAL. I perfected my impression of HAL's voice when I was young. I'd walk around the house telling my little sisters, "I'm sorry, Dave. I'm afraid I can't do that."

AI has been grabbing the headlines for the past few years. It's one of the hotter segments to watch, especially with drones, robots, autonomous vehicles and virtual reality applications becoming more popular every day. AI isn't just popular, it's fun.

And AI can be a lucrative area for investors. Companies that were unknowns not long ago such as NVIDIA, Twilio, Alphabet and Baidu are riding the AI train all the way to the bank. Baidu is the top AI company in China, and the firm stands to benefit from that country's drive to be the global leader in AI by 2030.

AI and its cousin, machine learning, are slowly making their way into EDA tools, most often to increase the speed of an existing process, or to reduce simulation times. All of the big EDA companies are involved in AI research, and we can expect to see more AI-driven functionality in the future. But some AI experts believe that the current crop of EDA tools can never take full advantage of AI, because most of these tools are based on code written many years ago, and true AI-driven EDA tools would have to be developed from the ground up. I doubt any EDA company is looking forward to the prospect of creating a whole new platform of PCB or IC design tools from scratch.

AI's development has continued despite a fear among Luddites that intelligent computers could eventually enslave or kill us all. Movies like 2001 and "The Ultimate Computer" episode of the original Star Trek helped scare people into worrying about what could happen if AI ever ran amok. That could never happen, right?

Some people think it's already happening. Your Alexa could be considered one of the benevolent bots, but bots have also hacked

into the IRS and manipulated world finance markets. We've also seen the effect that bots can have on social media platforms like Facebook and Twitter, automating posts, manipulating the ranking algorithms, and (potentially) affecting a presidential election. It's all relative: If the bots are helping your organization, they're helpful tools, not a reason to distrust everything you see on social media.

The Neural Information Processing Systems Foundation (NIPS) understands the benefits and dangers of AI, offering workshops with titles like Machine Deception and Security in Machine Learning, as well as AI for Social Good. There are pros and cons to every new technology, and we've barely begun to see the potential for AI.

This month, we asked our expert contributors to discuss AI and what it might mean to PCB design and the rest of the electronics industry. Technical Editor Dan Feinberg has been reporting on AI for years, and he offers a look at where AI is now in terms of consumer products, and some of the hurdles that AI faces in the upcoming years. David White of Cadence Design Systems has been involved with AI since his college days, and he shares his thoughts on Cadence's work with AI and what it could mean to EDA tools. And Mentor's Paul Musto explains how the company plans to harness the power of AI, and why old-school PCB designers shouldn't feel threatened by AI-driven EDA tools.

We have Part 2 of Tom Hausherr's collection of standard PCB components, and an article by Chang Fee Yee of Keysight Technologies on reducing crosstalk in multi-board interconnect. And Simberian's Yuriy Shlepnev brings us an article on localizing interconnect structures at speeds above 10 Gbps. We also have columns from our regular contributors Barry Olney of iCD, consultant Vern Solberg, and consultant Tim Haag.

It's a great time to be in this industry. Show season is upon us, and I hope to see you at SMTA International in October. In the meantime, if you're not already a subscriber, click here. While you're at it, subscribe to our newsletters, too.

See you next month. **DESIGN007**

Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 18 years. He can be reached by clicking here.

Enabling 'Internet of Photonic Things' With Miniature Sensors

A team of researchers at Washington University in St. Louis is the first to successfully record environmental data using a wireless photonic sensor resonator with a whispering-gallery-mode (WGM) architecture.

In the grand world of the Internet of Things (IoT), there are vast numbers of spatially distributed wireless sensors predominately based on electronics. These devices often are hampered by electromagnetic interference, such as disturbed audio or visual signals caused by a low-flying airplane and a kitchen grinder causing unwanted noise on a radio.

But optical sensors are "immune to electromagnetic interference and can provide a significant advantage in harsh environments," said Lan Yang, the Edwin H. & Florence G. Skinner Professor of Electrical & Systems Engineering.

Yang's sensor belongs to a category called whispering gallery mode resonators, so named because they work like the famous whispering gallery in St. Paul's Cathedral in London.

Yang and her colleagues had to address stability issues, which were handled by the customized operation systems app they developed, and miniaturization of bulky laboratory measurement systems.

"We developed a smartphone app to control the sensing system over WiFi," Yang said. "By connecting the sensor system to the internet, we can realize real-time remote control of the system."

(Source: Washington University in St. Louis)

Artificial Intelligence: More Questions than Answers

Feature by Dan Feinberg
I-CONNECT007

I've been covering artificial intelligence (AI) and related technologies for years, particularly at events such as the annual Consumer Electronics Show (CES). As I write this, we are in the run-up to CES 2019 and the Artificial Intelligence Conference in San Francisco, so the AI landscape is likely to change—at an ever-accelerating rate. Let's look at some of the challenges facing AI now, and then after CES 2019 we can take another look.

As the title suggests, in this quickly changing segment of the electronics industry, there may be more questions than answers. Fittingly, I think it's best for us to start with one great question about artificial intelligence, and we'll go on from there.

Q. What is artificial intelligence (AI), and are machines capable of being intelligent?

A. The *English Oxford Living Dictionary* defines AI this way: "The theory and development of computer systems able to perform tasks that normally require human intelligence, such as visual perception, speech recognition, decision-making, and translation between languages."

Or how about simply, AI is something that hasn't been done yet without human intervention. Some technologies that were considered AI just a few years ago such as conversational speed language translation and optical character recognition are no longer considered AI.

It is obvious that we have entered the era of common use of AI. Autonomous transportation is now a case of when, not if, thanks

Figure 1: An AI server farm.

Figure 2: Games such as "Call of Duty" have helped make AI a mainstream technology.

to groundbreaking companies like NVIDIA. Virtual personal assistants such as Cortana, Alexa, Hey Google and Siri are now part of our everyday lives. Today's military training simulators and popular first-person shooting games such as "Far Cry" and "Call of Duty" make significant use of AI by utilizing artificial enemies that can analyze the user's environments and actions, as well as find objects and calculate actions that might be beneficial to the user's survival and victory.

Drones and robots have made plenty of headlines lately. Contract manufacturers in Asia boast of their plans to replace workers with robots capable of doing extremely technical assembly work. Drone hardware has also improved quite a bit in the past few years alone, and the cost of a drone has dropped dramatically. Once just expensive playthings, today's drones often feature an HD camera and sell for a few hundred dollars. As their AI improves, we will see more and more drones and robots.

As AI and machine learning continues to improve, there will be more communications and more human-sounding conversations between us and our digital assistants like Cortana, Alexa and Google Home. At CES, I expect to see a horde of new assistants that have learned to speak naturally. I also expect to see significant progress from as-yet unknown companies. After all, none of us are really that happy with the digital assistants that are available today, and most of us are concerned that we are inadvertently providing way too much information to the likes of Google or Facebook.

Because of AI, we now have fraud detection that happens faster than the blink of an eye, and purchase prediction such as Amazon's predicted anticipatory shipping project. This handy feature plans to send you items before you think you need them. The point is that AI is part of our lives and it is not as new as the

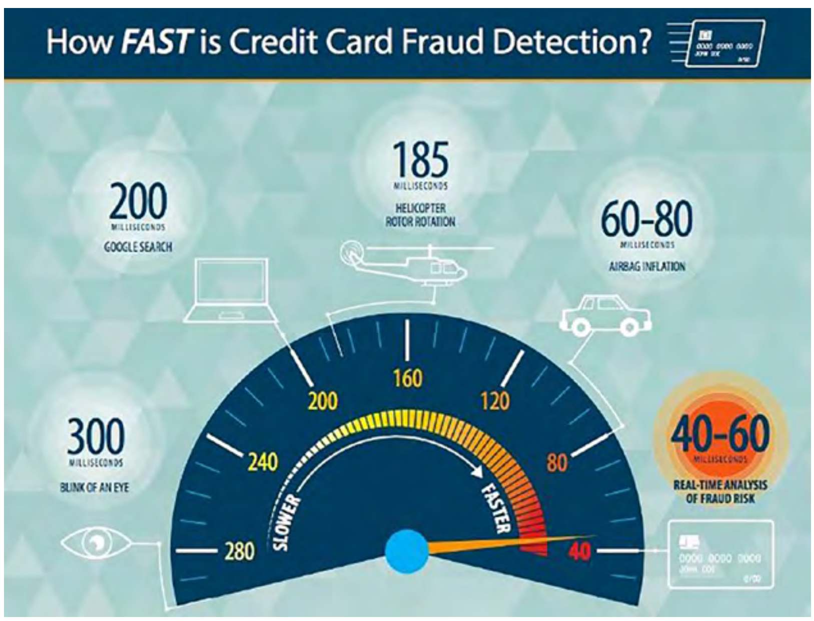


Figure 3: Fraud detection has come a long way, thanks in part to AI.

average person might believe.

Overall, we can expect very significant advances in AI over the next few years. I would guess that there will not be a segment of modern civilization that will not see advances beyond what was envisioned at the turn of the century. AI will change things for sure, but will all these changes be for the good? We will have to wait and see.

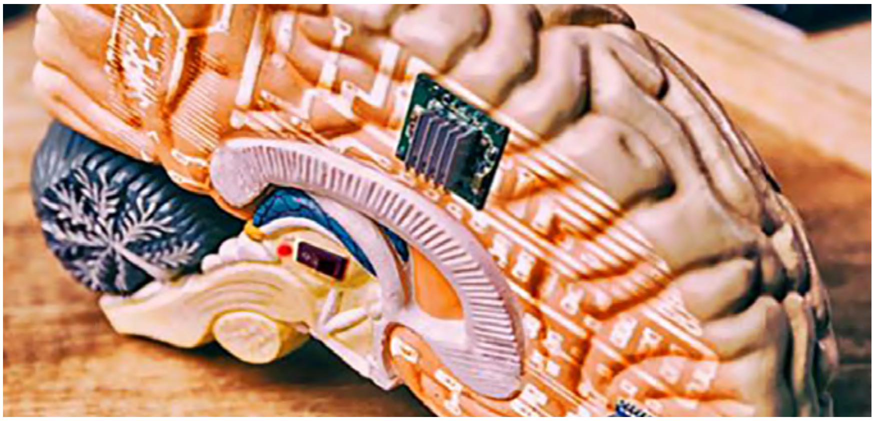


Figure 5: In the future, will the human brain be integrated with AI functionality? [1]

Price Waterhouse Cooper has been following the top trends in AI in 2018 [1], as shown in Figure 4.

Of all the trends shown in Figure 4, the most influential ones in the short term (and there are others) are what really get my attention as I study this topic: deep learning theory, probabilistic programming, and automated machine learning. If you want more examples and far more detail, see Reference 1.

In the meantime, I believe a prediction from my hero Nikola Tesla, in 1926, can help us to imagine what might be possible with AI. Remember, in 1926 global communication was possibly only by radio code, telegraph and basic one-way (at a time) radio with operator-assisted telephone. Primitive TV had recently been demonstrated. But Tesla knew this was the beginning of better things to come:

When wireless is perfectly applied, the whole earth will be converted into a huge brain, which in fact it is, all things being particles of a real and rhythmic whole. We shall be able to communicate with one another instantly, irrespective of distance. Not only this, but through television and telephony we shall see and hear one another as perfectly as though we were face to face, despite intervening distances of thousands of miles; and the instruments through which we shall be able to do this will be amazingly simple compared with our present telephone. A man will be able to carry one in his vest pocket.
—Nikola Tesla

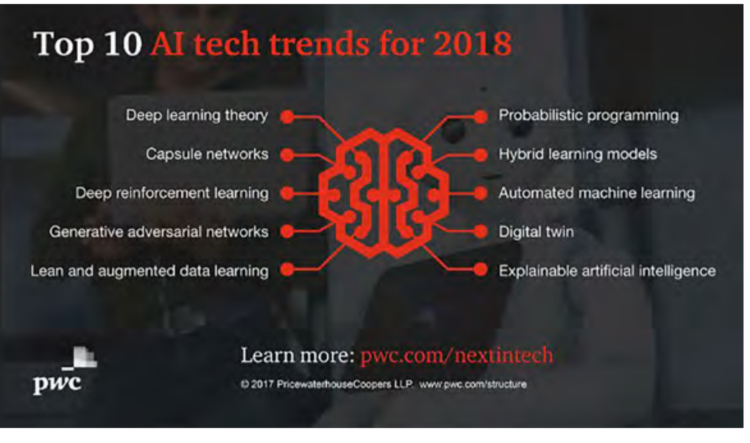


Figure 4: The top trends in artificial intelligence in 2018.

The topic of artificial intelligence itself is immensely broad and the possibilities are vast. I expect CES 2019 will truly begin to show the integration of AI into the other disruptive technologies and the effect that will have on the devices our industry will be required to produce in the decade ahead. We'll touch base again after CES. **DESIGN007**

References

1. Price Waterhouse Cooper's Top 10 Artificial Intelligence Technology Trends for 2018.

Dan Feinberg is the owner and president of FeinLine Associates Inc. and the technology editor for I-Connect007. To read his past columns or to contact Feinberg, click here.

Cadence: Bullish on AI

Feature Interview by Andy Shaughnessy
I-CONNECT007

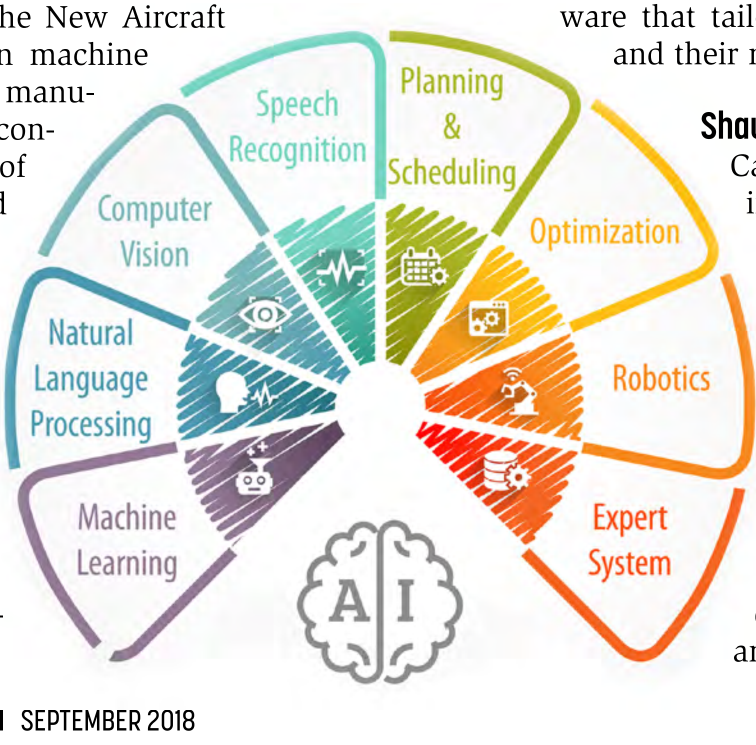
David White has been involved with artificial intelligence research for almost 30 years. Now, David is the senior group director of R&D for Cadence Design Systems, and I knew we'd have to speak with him for this month's issue on AI. In a recent interview, we discussed his decades of work in AI, Cadence's research into AI and machine learning, and what he believes AI could mean for the EDA tools of the future.

Andy Shaughnessy: Tell us a little about your background, your work with AI, and your thoughts on AI overall.

David White: I started working in AI in 1989 as a college student after discovering a copy of Parallel Distributed Processing, by David Rumelhart. I was so enthralled that I completed my undergraduate thesis on using neural network-based controls for a robotic arm. That work led me to McDonnell Douglas, now Boeing, where I worked in the New Aircraft Products Division on machine learning research for manufacturing and flight controls. As a result of this work, NSF asked me to chair the first NSF Workshop on Aerospace Applications of Neural Networks, which included machine learning researchers from across the country as well as a presidential science advisor and government officials.

I joined the MIT AI Laboratory where I continued my research and edited and co-authored a book on intelligent decision and control systems in 1992 with leaders in the machine learning world such as Michael Jordon, Paul Werbos and Andy Barto. I completed my graduate work at MIT where my research applied machine learning and chemometrics to semiconductor processing. I later co-founded and served as CTO of Praesagus, a company that was acquired by Cadence in 2006, and I have been working on electronic design automation with Virtuoso technology since 2009.

In terms of my thoughts on AI, I am really excited about the prospects of building intelligent decision systems that can learn from users and their environment. We believe we are bringing a unique perspective to how we build these systems. We are combining innovations in machine and deep learning with large scale optimization and distributed processing in unique ways. Much of what we are working on has applications beyond EDA and extends to how we can build design and analysis software that tailors itself to the user and their mission.



Shaughnessy: How did Cadence first get involved with AI?

White: I joined Cadence in 2006 when our company was acquired, so my frame of reference begins then. Cadence's research in machine learning (ML) for physical design and electrical analysis started in the

2009-2010 timeframe, with two persons and myself. Our motivation came from observing the scale and complexity that grew with the increase in data such as larger designs, larger simulations, etc.

To address these problems, we began to look at data-driven solutions such as analytics and machine learning. When we began the work, there was not the same buzz around machine or deep learning, and we just found it to be a useful tool to create fast models of complex non-linear problems that required long compute times using more traditional methods. Two machine learning-based solutions were released in 2013 in the Virtuoso Electrically Aware Design (EAD) environment and Virtuoso Analog Design Environment (ADE).

Shaughnessy: Tell us about Cadence's current research into AI. Are you continuously working to implement more AI in EDA tools?

White: As you can understand, I can't go into details on research and development that has not been released in our products.

First, we are fortunate to have a brilliant team of engineers who continually push the edge. Our machine learning team includes members of our Virtuoso technology team, which focuses on placement, routing, and analog design and electrically aware design as well as our OrbitIO package and board solution—so they have hands-on experience with the applications we are trying to automate.

We are constantly evaluating data-driven solutions such as machine and deep learning, as well as analytics, optimization and distributed processing. You always hear about machine and deep learning, but those other solutions are often required as well. Optimization is often overlooked in discussions about building intelligent, adaptive systems. From a decision systems perspective, you want to use optimization in conjunction with ML/DL to drive the system or decision sequence to some desired state (e.g., a placement and routing alternative that meets design intent). One solution is no more important than the other.

The biggest challenge in productizing AI is addressing the verification, deployment and support issues that every new technology faces. Most of the available open source software focuses on the creation of ML or DL models and not as much on how to verify, calibrate or adapt those models in environments that change. However, those factors are critical in CAD/EDA tools where design intent may not be fully observable or the environment changes

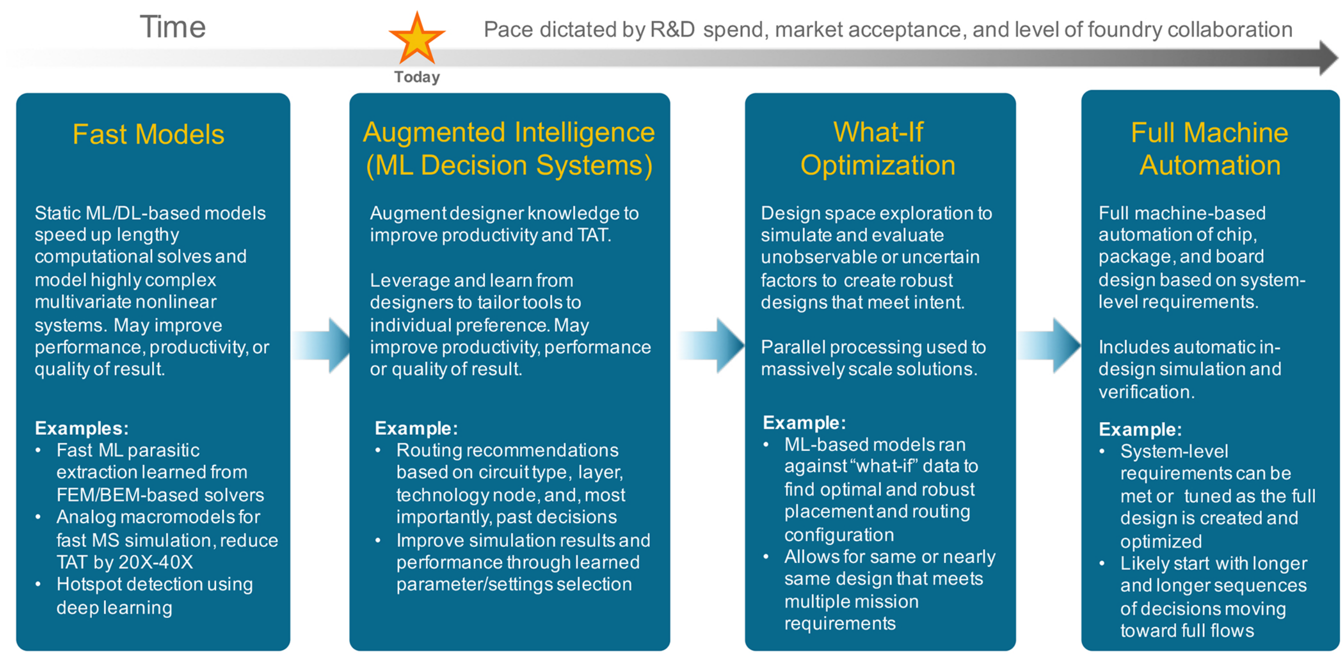


Figure 1: A graphic showing the development of machine learning and EDA over the years.

with the introduction of new silicon technologies.

Shaughnessy: Outside of EDA, what are some examples of AI that really impress you?

White: It is hard to answer that question—there are quite a few. I am impressed with the work Google has done under Jeff Dean. His understanding of the algorithms, and more importantly the implementation details, seems to put him on a different plane than many others. His presentations are mini-courses on problems you should be thinking about if you are not doing so already.

David White

Overall, I am fascinated with how far speech processing has progressed with AI/ML technology fueling it. We played around with neural network-based speech processing for a summer when I was at MIT, and I learned what a hard problem it is ...(and I have not attempted to solve it ever since). Google, Amazon and others have overcome some challenging problems with AI technology, extending it from improved recognition to include translation as well.

I am a fan of Netflix and over the years have seen large improvements in their recommendation engine. There are some interesting talks that describe the AI and analytics-related innovations that go into their ability to personalize and tailor their recommendations, as well as how they tailor the quality of the user experience across many countries and cultures. That is a really dynamic and adaptive environment in which to work and as a user, I see improvements regularly.

Shaughnessy: Some PCB designers are worried that AI will put them out of a job. I've told them not to worry, but do they have a point?

White: Our view is that the introduction of machine and deep learning into electronic design and CAD systems in general will be an evolution not a revolution. In other words, I foresee several stages of innovation as the technology and methodology align. In the first stage, ML/DL is used inside existing products to improve productivity, performance or quality of results, and we can see that occurring now.

In the second stage, machine and deep learning will be used to augment the knowledge of the designer and allow them to work at high levels of abstraction. They can move away from pushing shapes and move toward thinking about system design enablement. It is difficult to capture the intent of the designers, so the challenge is building ML/DL technology that can discover user intent and tailor recommendations accordingly. Think of a design assistant that makes recommendations to speed productivity through the manual steps of a design.

In the third stage, we use large-scale optimization to drive multiple design decisions to one or more desired states (e.g., in EDA it could be design intent, QoR, or PPA) within a set of constraints (e.g., reliability and design rules). In the fourth stage, we will be able to automate sequences of decisions and eventually achieve longer sequences leading to full flows.

Automation will continue to impact electronic design as it has impacted other industries, but I don't see it happening overnight. If we can automate lower level tasks in the next few years, those same designers can spend more time at the systems level focusing on higher-level goals and how to manage mission profiles where single solutions are used or tailored for multiple missions or uses. The lead architects of our OrbitIO solution are working on next-generation solutions to address these goals and have already achieved promising results.

Shaughnessy: Thanks for your time, David. We appreciate it.

White: Thank you, Andy. **DESIGN007**

Feature Interview by Andy Shaughnessy
I-CONNECT007

Artificial intelligence (AI) has been making inroads into a variety of industries in the past decade or so, from automobiles to medical devices. Naturally, EDA tool companies are taking a look at AI. Does AI offer a way forward for PCB design tool developers?

I recently interviewed Paul Musto, director of marketing for the Board Systems Division of Mentor, A Siemens Business. We discussed Mentor's plans for integrating AI into EDA tools, and why we may be at the very beginning of understanding the pros and cons of this new technology.

Andy Shaughnessy: Paul, what do you think about AI and where it is right now?

Paul Musto: Artificial intelligence, where computers are trained to perform tasks that normally require human intelligence, will have a place in almost every facet of our lives. We are really at the beginning of understanding the implications and opportunities of AI. As the technology matures, it's not hard to imagine that AI will have a critical role in product development.

Shaughnessy: How likely it is that we'll see more AI in EDA tools? With chunks of AI in EDA tools already, like for reuse and things like that, is there a place for more AI in EDA tools?

Musto: It's very likely, and we are at the beginning of this journey. If you look at the mechanical engineering world, you see examples, like generative design. With AI software and the cloud-based computing power, generative design enables engineers to create thousands of design options by simply defining their design problem, such as basic parameters like height, weight, strength, and material options. As AI becomes more integrated, you will see better, more productive application of generative design principals. There is reason

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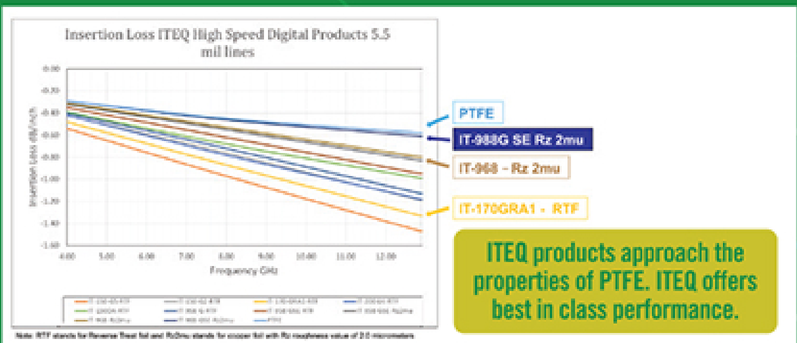

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- IST - Passed 1000 cycles, 6x 260°C precondition
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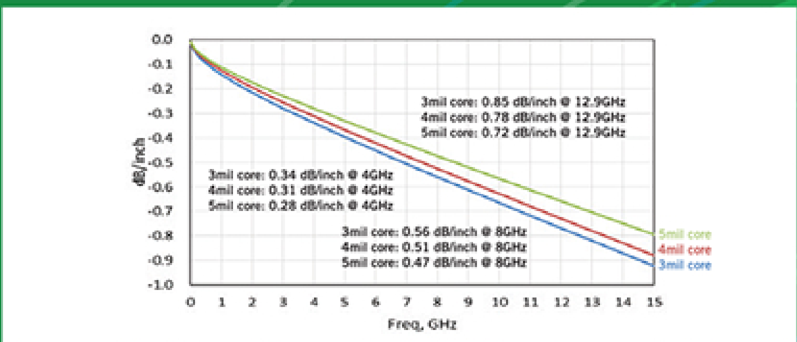
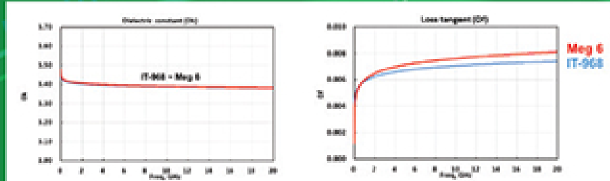
IT-968 Loss Performance



IT-968 SPP Comparison



GHz	10		12.9		16		20	
Parameter	Df	Dk	Df	Dk	Df	Dk	Df	Dk
IT-968	0.0071	3.39	0.0072	3.39	0.0073	3.38	0.0074	3.38
M6	0.0076	3.39	0.0078	3.39	0.0079	3.38	0.0081	3.38
%	7.95	0.04	8.52	0.04	8.98	0.03	9.45	0.02

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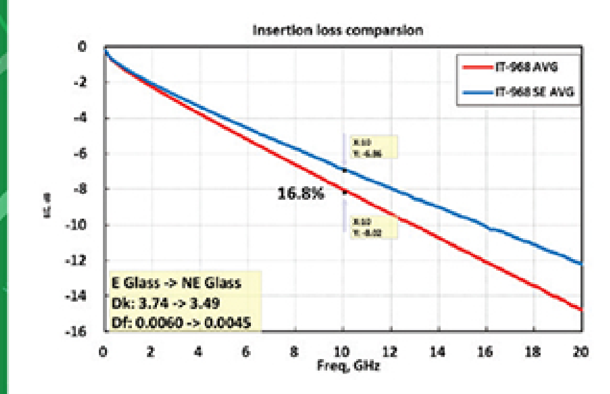
Property	Test Method	IT-968	IT-968 SE
Tg (°C)	DSC	185	185
T-288 (w/ 1 Oz Cu, min)	TMA	120+	120+
Td-5%(°C)	TGA 5% loss	390+	390+
CTE (%), 50-260°C	TMA	2.2	2.2
Peel strength (lb/inch)	1 oz	6	6
Water Absorption	D-24/23	< 0.1	< 0.1
Dk , 1 GHz 2-10 GHz	IPC TM-650 2.5.5.9 IPC TM-650 2.5.5.13	3.8 3.8-3.7	3.4 3.4-3.3
Df , 1 GHz 2-10 GHz	IPC TM-650 2.5.5.9 IPC TM-650 2.5.5.13	0.0032 0.0038-0.0050	0.0028 0.0031-0.0040

E-Glass vs Low Dk Glass



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to expect that to happen in the EDA world and in PCB design. Mentor, as part of Siemens, is well positioned to take advantage of Siemens' delivery of a digital thread, which includes product design, manufacturing process, and product performance. We will be able to capture and rationalize data from a myriad of sources like requirements, actual manufacturing data, or field performance, and use that intelligent data to drive better design practices. The basis of our future AI won't be built on design automation alone, but on predictive principals based on actual manufacturing and field performance.

Paul Musto

Shaughnessy: Can you describe what Mentor is doing in AI?

Musto: Being part of Siemens gives us real advantages to deliver cutting-edge solutions to our customers. A key area of investment is in simulation technologies and in design exploration and design recommendations.

Shaughnessy: What consumer applications have you seen that use AI?

Musto: Obviously, I am a gadget freak. I have home automation assistants in my house. All of us are familiar with Amazon and digital services like Netflix or Spotify that give users recommendations based on past consumption behavior and search history. Can you imagine these applications in EDA? Like implementation wizards based on predictive analytics, simulation models, manufacturing resources and availability, or field performance.

Shaughnessy: Should designers be worried that they'll be out of a job if AI has a greater role in EDA? Some designers tell me, "We're the AI!"

Musto: Obviously, the topic of AI brings anxiety to any workforce. My recommendation is that we focus on the upside versus downside. We have been here before with automation, like Mentor's automated Sketch Router technology, or our concurrent platforms for design collaboration. All of these met some resistance in that productivity advances could eliminate skilled workforces. This simply did not happen. What has happened is that design teams are much more productive than ever, and design starts seem to be increasing all the time. These automated technologies actually allowed design teams to invest more time in design innovation.

With designs becoming more complex and with increased electronics content in everything, it's hard to imagine that AI will completely replace entire workforces. What it will mean is that our expertise will be focused on areas where we are underinvesting now, such as better simulation techniques or innovation initiatives in product design or packaging. With the electronics industry growing at an amazing pace, it's hard to imagine the work ending any time soon. If anything, we need more engineers to apply these emerging technologies, and Siemens is committed to industrial digitization and innovation.

Shaughnessy: Sounds like we're in a really interesting time, for designers and for EDA companies. Thanks for your time, Paul.

Musto: Thank you, Andy. Always good to talk with you. DESIGN007

PCB007 Highlights

Industry Veteran Nolan Johnson Joins I-Connect007 Editorial Team ▶

I-Connect007 welcomes the recent addition of industry veteran Nolan Johnson to its editorial team. In his new position, Johnson will take over as managing editor of *SMT007 Magazine* and *PCB007 Magazine*. Nolan brings 30 years of career experience focused almost entirely on electronics design and manufacturing.

An Owner's Positive Take on IMPACT 2018: American Standard Circuits' Founder & Chairman Gordhan Patel ▶

During a full day at IMPACT 2018, I had a chance to speak with American Standard Circuits' founder and chairman Gordhan Patel. We had much to talk about after listening to several speakers from the departments of Defense and Education, and the International Trade Administration.

Welcome to the Silicon Valley Neighborhood: Nano Dimension Arrives in California ▶

I-Connect007 Technical Editor Dan Feinberg accepted an invitation recently to tour Nano Dimension's new USA headquarters in Santa Clara's Silicon Valley, which included a sit-down with President and Co-Founder Simon Fried.

The PCB Norsemen: Lean Challenges—Standard vs. Non-Standard Products ▶

Writes Didrick Bech: People tend to treat standard and non-standard products in the same way; however, they represent two parallel product segments and consequently different challenges for your Lean manufacturing process, especially in relation to production and logistical operations. When you fail to differentiate the processing of standard and non-standard products, not only is the Lean manufacturing process disrupted, but you also introduce a variety of production, financial and logistical challenges.

Graphic PLC Team Completes Business Improvement Apprenticeship ▶

The 12-month program is a formally recognized NVQ apprenticeship qualification combining classroom-based learning and simulations alongside practical improvement projects, providing an opportunity to apply the skills they have gained.

DSBJ Completes Acquisition of Multek ▶

Multek announced the completion of its previously announced acquisition by Suzhou Dongshan Precision Manufacturing Co. Ltd., a diversified manufacturer headquartered in Suzhou, China.

It's Only Common Sense: A Peek at Future Technological Advancements ▶

It's that time again—time for a peek into the future. The following ideas come from an excellent book by Mark Penn called Microtrends Squared: The New Small Forces Driving Today's Big Disruptions.

One World, One Industry: Automotive Electronics–Past/Present/Future ▶

As electronics play an increasingly important role in automotive manufacturing, tremendous change and great progress have been made worldwide. We are at the crossroads of incredible technological advancements, and it's been exhilarating to watch. I am eager to see what happens next.

10 Fundamental Rules of High-Speed PCB Design, Part 1

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Over the years, I have focused on high-speed design, signal and power integrity, and EMC design techniques in a plethora of published technical articles—all of which have key points to consider and present a tremendous amount of information to absorb. In my next few columns, I will elaborate on ten of the most important considerations to embrace to achieve successful high-speed PCB designs that perform reliably to expectations.

Figure 1 lists the 10 fundamental rules of high-speed PCB design that I deem the most important to follow, although they may change after months of deliberation, like what happened with the laws of thermodynamics. The first established thermodynamic principle, which eventually became the second law, was formulated by Sadi Carnot in 1824. By the late 1800s, three laws of thermodynamics were clearly defined. However, in the 1930s—long after these three laws were already widely accepted—Sir Ralph Fowler and E.A. Guggenheim felt that another law, which they saw as the foundation of earlier laws, should be incorporated. Hence, it was numbered the zeroth law. Thus, there is always room for one more at the top!

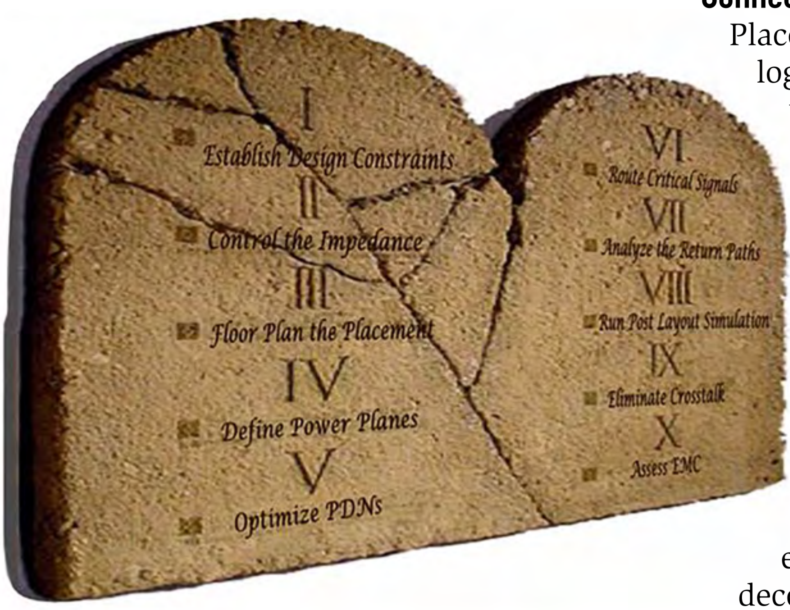

Figure 1: The 10 fundamental rules of high-speed PCB design.

The 10 fundamental rules of high-speed PCB design are:

I. Establish Design Constraints

Always create a strategy for high-speed design requirements and set constraints based on pre-layout analyses or recommendations and guidelines prior to commencing the design.

II. Control the Impedance

Match the transmission line impedance to the driver and load. Create the stackup and define terminations to match the impedance.

III. Floor Plan the Placement Based on Connectivity

Place components by functionality and analog and digital groups to minimize interaction between different logic families and improve routability and timing.

IV. Define the Power Delivery Planes and Paths

Define the power/ground regions and plane layers. Partition (not split) the ground planes.

V. Optimize the Power Distribution Networks (PDNs)

Create a low AC impedance delivery path by optimizing the bypass and decoupling capacitors and mounting inductance and plane resonance from DC to the

maximum required frequency (including harmonics).

VI. Route the Board Based on Critical Signals

Adhere to the defined routing strategy. Clock signals should always have the longest delay of the group. Differential pairs should maintain constant impedance along the entire length.

VII. Analyze the Return Current Paths

All signal traces should be tightly coupled to a contiguous reference plane and have a clearly defined minimum loop inductance return current path.

VIII. Run the Post-Layout Simulation

Simulate critical signals and match signal propagation and timing. Check for signal ringing and eye jitter.

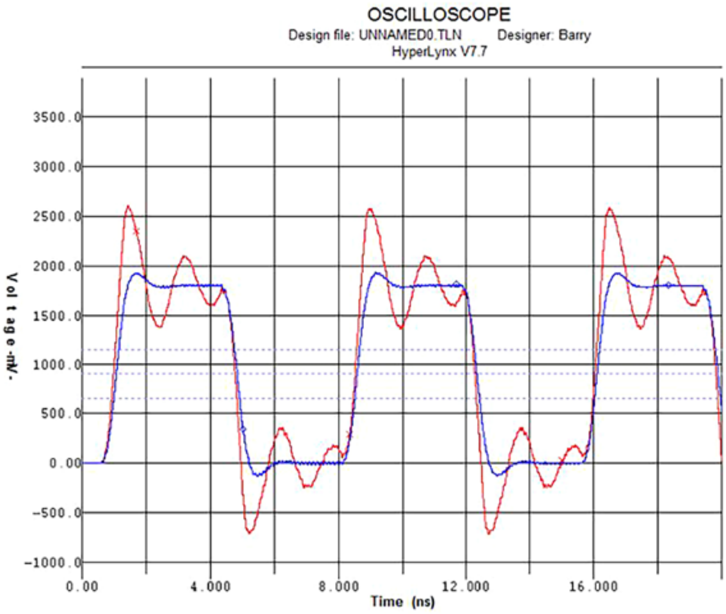

Figure 2: Pre-layout simulation with correction of clock ringing. (Source: HyperLynx)

IX. Eliminate Crosstalk

Scan the board for possible crosstalk. Crosstalk can be coupled trace-to-trace on the same layer or broadside coupled by traces on adjacent layers.

X. Assess Electromagnetic Compliancy (EMC)

Control EM radiation at the source. Ensure that differential mode signals do not convert to common mode and eliminate any possible antennae.

Without further ado, I will begin with an elaboration of the first rule: Establish design constraints.

Complex, high-speed multilayer boards should be designed using a proven design methodology incorporating a pre-layout simulation before placing a single chip on the board. This includes reviewing component datasheets and design recommendations prior to the schematic capture. Simulation tools can be used to analyze various issues, such as reflections due to impedance discontinuities, crosstalk, signal attenuation, and PDN noise—all of which can impact interconnect performance.

Simulation of a PCB design after placement and routing is recommended, but simulation early in the design phase is even better. Both are essential. Pre-layout analyses allow critical interface topologies, termination schemes, and I/O buffer selections to be defined and analyzed for synchronous, source-synchronous, and clock interfaces before placement and routing. Figure 2 depicts a simulated clock signal with (blue) and without (red) a series termination. Simulation opens one's eyes to what the circuitry is doing. It also leads to an enhanced perception of what might be a potential issue once the system is built.

There are multiple facets to pre-layout analyses, including:

- Stackup planning for controlled impedance, signal integrity, and crosstalk
- Dielectric material selection for high-frequency operation, manufacturing yield, and cost control
- I/O buffer and drive strength selection
- Topology optimization for signal integrity, timing, and EMC
- Series and parallel termination strategy
- Derived layout routing constraints, including trace width, spacing, and delay/length matching

- PDN analysis and decoupling capacitor optimization
- Signal integrity analysis to meet the design specifications with respect to noise margins, timing, skew, crosstalk, and signal distortion

Pre-layout simulations also allow a designer to identify and eliminate signal integrity, crosstalk, and EMC issues early in the design process. This is the most cost-effective way to design a board with fewer iterations. However, if you do not have access to simulation tools, then follow best practices from Design007 Magazine, IC manufacturers guidelines, etc.

While designs continue to increase in complexity and time-to-market remains critical, it is imperative to have a constraint system that is integral to your design flow. The constraints—based on a pre-layout simulation—manufacturing restrictions, and IC manufacturer's recommendations and guidelines should flow from pre-schematic to PCB layout, routing, fabrication, and assembly.

Before starting placement and routing, detailed interconnect routing constraints should be established (Figure 3). Of course, these are based on the pre-layout simulation and impedance requirements. Firstly, determine the single-ended and differential impedance required for each technology used. Synchronous bus delay or length matching should be set up in the constraints editor along with differential pair rules and clearance between signal groups to prevent crosstalk while giving priority to critical signals.

Appropriate grouping and defining of net and constraint classes in the early stages of the design process significantly simplifies constraint definition and management. Grouped constraints can increase layout efficiency, reduce design time, and ultimately lower PCB design costs.

The prime objective behind setting constraints up front is to ensure that the design is going to perform to expectations. It is essential that the system can alert the designer to any errors as they occur. Interactive design rule

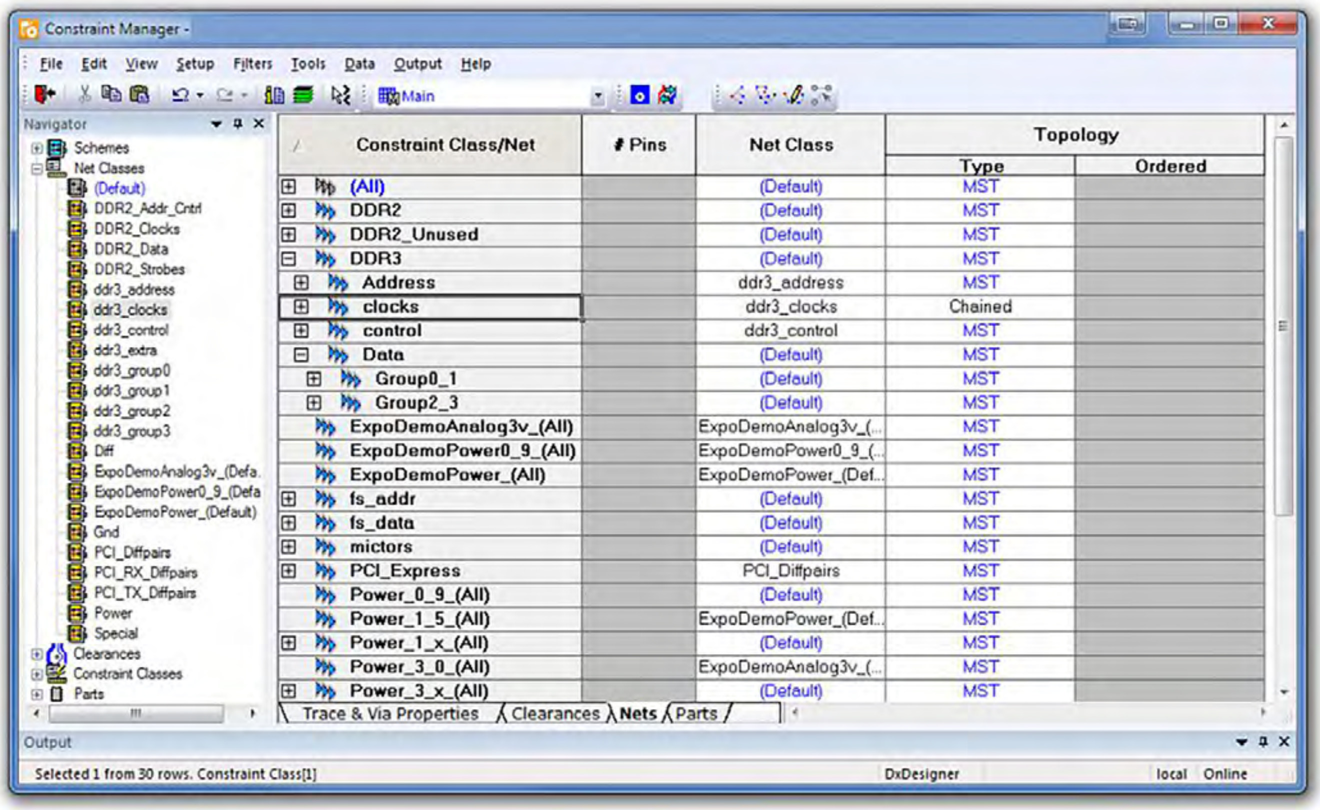

Figure 3: Typical high-speed design constraints. (Source: PADS Professional Constraint Manager)

checks (DRCs), which are adhered to throughout the design cycle, provide for an error-free, correct-by-construction design when carefully planned early in the design phase.

A robust constraint management system should be unified and integrated into the schematic and layout editors with cross-probing, including:

- Integrated topology-driven constraint definition
- Controlled impedance rules, including spacing and clearance to other nets
- Length or time-based constraints
- Electrical constraints with custom equation capability
- Physical trace and spacing rules (class-to-class rules, etc.)
- Region and technology rules
- Same net DRCs for advanced technologies (HDI)
- PCB fabrication, assembly, and testability rules (if required)

Although all designs are different, one should reuse existing rules where possible as a template to eliminate the need for re-entry of any common constraints. These include DDRx, PCIe, USB, SATA, Ethernet, differential pair rules, manufacturing requirements, etc. This also minimizes the possibility of input errors.

When constraints are defined at the beginning of the design process, designers can be confident that once the design phase is completed, the product will move through the production phases with fewer errors. A constraint management system that can check work in real time as the design process is executed provides reduced risk and peace of mind that the constraints will prevent the PCB designer from violating the rules set up front. Although we cannot plan for the unexpected, having a reliable constraint management system in place will ensure that the majority of issues are covered and will alert you if any unforeseen issues arise.

Stay tuned for next month's column that will continue to elaborate on the 10 fundamental rules of high-speed PCB design.

Key Points

- Simulation of a PCB design early in the design process is essential
- Pre-layout simulation leads to an enhanced perception of what might be a potential issue once the system is built
- It is imperative to have a constraint system that is integral to your design flow
- Detailed interconnect routing constraints should be established before starting placement and routing
- The prime objective behind setting constraints up front is to ensure that the design is going to perform to expectations
- Reuse existing rules when possible to eliminate the need for re-entry of any common constraints
- A constraint management system that can check work in real time as the design process is executed provides reduced risk and peace of mind

Further Reading

- Beyond Design: Pre-Layout Simulation by Barry Olney, The PCB Magazine, July 2012.
- Beyond Design: Split Planes in Multilayer PCBs by Barry Olney, The PCB Design Magazine, March 2015.
- Beyond Design: Plane Crazy, Part 1 by Barry Olney, The PCB Design Magazine, December 2015.
- Beyond Design: Interactive Placement and Routing Strategies by Barry Olney, The PCB Design Magazine, December 2012.
- Beyond Design: Controlling Emissions and Improving EMC by Barry Olney, The PCB Design Magazine, August 2011.
- 5 Ways to Assess PCB Constraint Management Systems for High-Speed Designs, EMA Design Automation Blog.
- Why impose PCB design constraints? by Steve Hughes of Mentor, a Siemens Business.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded from www.icd.com.au. To read past columns or contact Olney, click here.

VERIFY
OPTIMIZE
ANALYZE
PREPARE
PANELIZE
COMMUNICATE
DOCUMENT

Embedding Components, Part 3:

Implementing Discrete Passive Devices

Designers Notebook

by Vern Solberg, CONSULTANT

Note: Part 1 of this column appeared in the June 2017 issue of *The PCB Magazine* and Part 2 appeared in the June 2017 issue of *The PCB Design Magazine.*

For many, the driving force to integrate passive components within the layers of the PCB structure was the need for providing the consumer with smaller and lighter products. Once the commercial sector began developing and refining embedded component processes and overcoming quality and reliability issues, the automotive, telecom, aeronautic, and aerospace industries recognized the advantages of embedded passives technology for the following benefits:

- Improved density and functionality
- Reduced PCB area and weight
- Increased assembly process efficiency
- Improved functional performance and reliability

Most of the passive components used in electronics are discrete surface mount components configured to mount onto land patterns furnished on the surface of a PC board. Designers have several choices for providing passive functions in a system design, such as discrete surface-mounted passives, array passives or passive networks, integrated (Rs and Cs) passive devices, and embedded discrete passive components. A growing number of PCB sup-

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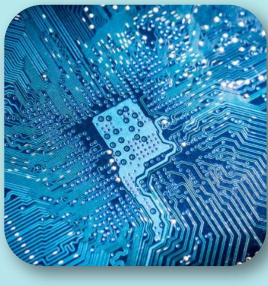
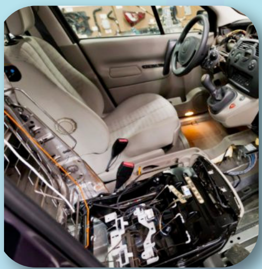


High-Speed Data



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pliers with experience in build-up of circuits can embed both passive and active components. Although a majority of companies furnishing high-volume embedded component circuit boards are in Europe and Asia, there are number of proficient North American suppliers as well.

Providing formed resistors and capacitors within the circuit structure remains the most economical process with the least level of risk; however, value range and tolerance control is somewhat limited.

Providing formed resistors and capacitors within the circuit structure remains the most economical process with the least level of risk; however, value range and tolerance control is somewhat limited. Placing discrete component elements furnishes a greater value range and superior tolerances.

Embedded Component Process Planning

The process for embedding discrete passive component elements within the multilayer PCB structure is a sequential process requiring specialized SMT process skills and assembly systems typically outside the realm of the average circuit board supply chain—a process capability more common to OEMs and board-level assembly service providers. To prepare for efficient high-volume production, the PCB fabricator will need to establish in-house component placements and attachment capabilities and reliable component sources or develop partners for the procurement of components that are suitable for embedding. The PCB supplier must also determine which systems and methodologies will be required for applying termination materials (conductive polymer or solder) that can ensure precise component placements, curing polymers or reflowing solders, and specialized systems required for electrical testing during the progressive stages of the fabrication process.

When choosing discrete resistor, capacitor, and inductor components for embedding, both device outline and thickness must be considered. While some passive components are very thin and require no special preparation, others may have profile dimensions requiring encroachment into contiguous circuit layers.

Discrete Resistors

Several companies are now able to furnish thin, small outline resistors and capacitors that prove to be ideal for embedded component applications. The outline of currently available components can be as small as 0.4 mm x 0.2 mm (01005) and 0.6 mm x 0.3 mm (0201). Discrete thick-film resistors are offered in a 0.015-mm profile. Specifically developed for embedding, these devices are described as a flat thick-film resistor furnishing a value range of 1.0 Ω to ~10 MΩ with a power rating of 0.063 watts and working voltage maxing out at 50 volts.

Although these devices have a relatively low power rating, the operating temperature range, resistor value, and tolerance (1% and 5%) specified for the smaller devices are the same as the larger resistor variations and available with copper terminals. While tin-based alloy terminals are acceptable for solder or conductive polymer termination, copper terminals will be necessary when using plated microvia interface technology. For applications requiring resistor value tolerances less than 1%, an alternative nickel-chromium thin-film family is available, but the package dimensions are significantly greater than the thick-film resistor previously described.

Discrete Capacitors

Low-profile ceramic capacitors have been developed for height-restricted applications where device thickness is a key design constraint—perfect for embedded or other applications with thickness limitations. Ideal for decoupling and filtering applications, the com-

ponents are available with the same small outline dimensions as the resistor family, but device thickness will vary somewhat due to the dielectric type and required volume.

For example, the body thickness for the 01005 capacitor is specified as 0.20 mm while the 0201 outline component thickness can increase to 0.30 mm. Additionally, the dielectric type and working voltage will impose limits on the capacitor value range for these smaller device outline families. The 01005 and 0201 type capacitors with a C0G dielectric are available in a value range of 5–100 pF. The X7R dielectric capacitors can furnish a value range of 68–470 pF for the 01005 capacitor and 68–10,000 pF for the 0201 variation. The standard terminal plating is tin-alloy over a nickel base metalization for solder and conductive polymer attachment. Because the base layer is a nickel-alloy, termination of the component to the circuit conductor pattern with copper-plated microvias may be possible.

Discrete Inductors

A limited value range of miniature inductors is available from several leading suppliers. The multilayer ceramic inductor family is available in both 0402 and 0603 (1.0 mm x 0.50 mm and 1.60 mm x 0.80 mm) outlines with a thickness equal to the device width (0.50 mm for the 0402 device and 0.80 mm for the 0603 variation). The terminal plating is a nickel-alloy with a tin-alloy based coating for solder or conductive polymer interface.

The available inductance value ranges between 6.8 nH for the low and 220 nH for the high with a tolerance value of +/-5%. An alternative thin-film small outline and low-profile inductor family is available too. For this variation, the inductor element is printed onto the surface of a ceramic base material, passivated and fired to protect the printed pattern, and furnished with a tin-alloy terminal for joining to the circuit structure. Small outline thin-film inductor elements will range in size from 0402 to 0603. The actual dimensions for the 0402 device are 1.0 mm x 0.50 mm x 0.35 mm, and 1.6 mm x 0.8 mm x 0.50 mm for the 0603 device.

The value range for these two thin-film inductor components is between 1.0 nH and 82 nH with a tolerance of +/-2%. Manufacturers claim that the miniature inductors furnish up to twice the rated current and half the DC resistance of comparable ferrite inductors. Designers should be aware that inductors size and value range varies somewhat between suppliers.

Next Column

Part 4 of this embedded component technology series will focus on land pattern development criteria, ways to accommodate higher profile passive components, and alternative termination methodologies.

Upcoming Appearance

Vern Solberg will be conducting a half-day professional development course on “Design and Assembly Process Principles for High-Density Flexible and Rigid Flex Circuits” at SMTA International 2018 in Rosemont, Illinois, on Sunday, October 14 from 8:30 a.m.–12:00 p.m.

This tutorial has been developed primarily for design professionals with a focus on applying best design practices for fabricating flexible and rigid-flex circuits. Participants will have an opportunity to study and discuss alternative fabrication methodologies as well as practical guidelines for implementing automated assembly processing. Information presented will also include the selection criteria for base materials, alternative fabrication methodologies, SMT component selection, land pattern development, and features required to accommodate SMT-on-flex assembly.

For further information on this conference and to sign up for this tutorial (PDC 01), click here. **DESIGN007**

Vern Solberg is an independent technical consultant specializing in surface mount technology, microelectronics design, and manufacturing technology. To read past columns or contact Solberg, click here.

Contract Positions: Go the Extra Mile

Tim's Takeaways

by Tim Haag, CONSULTANT

A few years back while vacationing in the Tri-Cities area of Eastern Washington, my wife and I took a tour of the Hanford Site near Richland. The Hanford Site contains nine nuclear reactors used to produce fissionable materials in atomic weapons. These reactors were all shut down by the fall of 1989 and are now being cleaned up and entombed to protect the environment. However, the very first one built—B Reactor—has been designated a national landmark and refurbished for tours [1].

The tour was a fascinating experience and I would highly recommend it if you are ever in the area. The fact that the whole project was put together during World War II, in such a short amount of time, is amazing. Hundreds of thousands of people were involved in different sites across the country and most did not know what was being produced—only that it was critical for the war effort.

A whole city was created at the Hanford Site, with housing, shopping, hospitals, schools, and entertainment facilities for those who worked there [2]. Of course, the creation and use of atomic weapons is a very serious matter and I am not trying to comment on either side of the issue. Instead, I want to look at how and what these people did to accomplish something that had never been done before. For example, simply providing dessert for the workers required machines to create over 7,000 pies for just for one meal served in the cafeterias that totaled eight football fields in size.

The reason I bring this up is to highlight an engineering achievement. The original design for the reactor came from scientists at the Metallurgical Laboratory (Met Lab) in Chicago, and they specified that the reactor needed to be built with 1,500 fuel tubes [3]. However, the engineers from DuPont who built the reactor

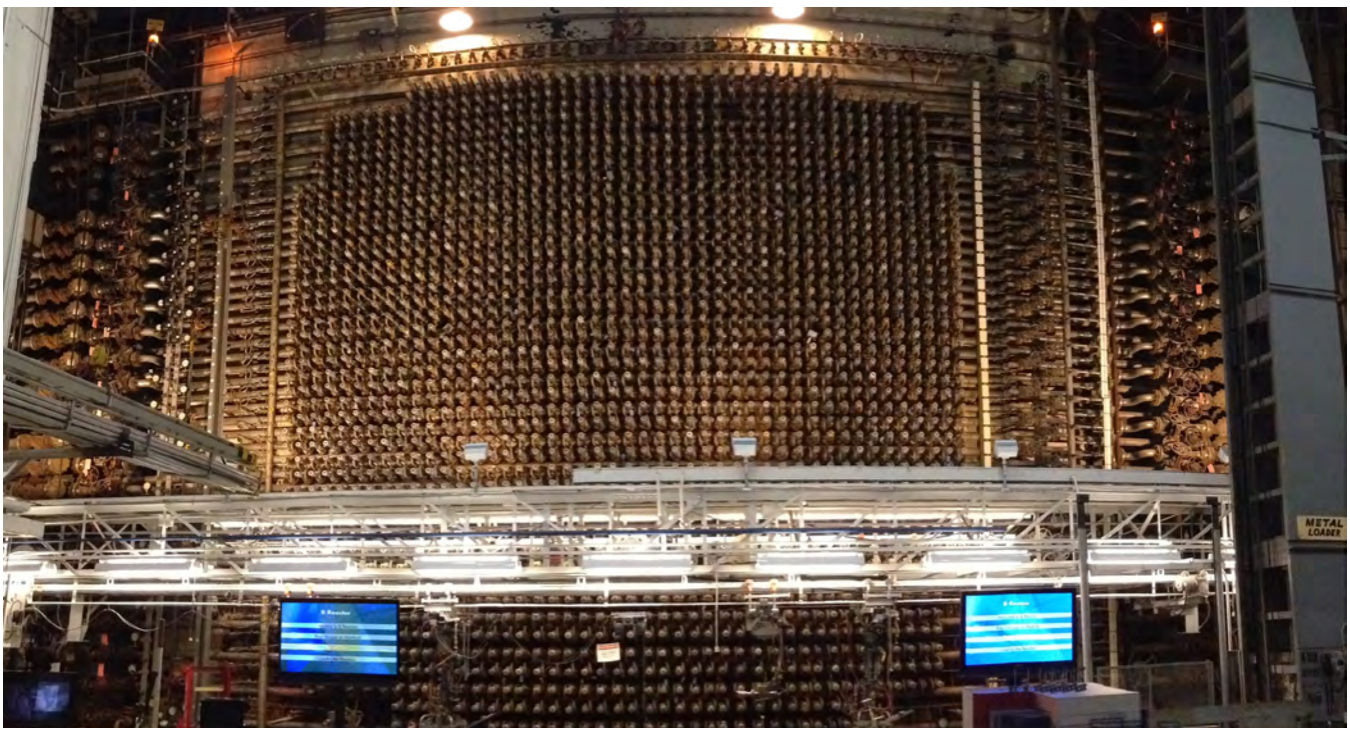


Figure 1: Fuel tube loading face at B Reactor. Go ahead—count them.

Figure 2: Control room.

argued for additional fuel tubes even though many scientists seriously objected. The engineers based their request on years of experience building industrial plants. In the end, they won the argument and were able to build the reactor the way they wanted. Although it was a significant increase in cost, the engineers completed the reactor with a total of 2,004 fuel tubes.

Early in the morning on September 27, 1944, the first nuclear reaction started in reactor B (Figure 1). Engineers decided to only use the original 1,500 fuel tubes in the first test and the reactor performed above expectations. However, after less than a day of operation, the reactor experienced a problem that caused it to lose power and shut itself down. This problem initially baffled the reactor operators, but they eventually discovered the issue was caused by xenon that had been produced as a byproduct of the fission process. The operators determined that the solution was to increase the power of the reactor. After some recalculations, the full array of 2,004 fuel tubes was loaded and the reactor was back to full power with the xenon problem eliminated by December 26.

If not for the persistence of the engineers wanting to build in a safety margin in the original reactor design, the reactor would have required a complete rebuild to operate. This would have affected the reactor's ability to produce fissionable material for the war effort by a considerable amount of time while it was upgraded.

My dad used to say, "A job worth doing is worth doing right." I cannot tell you how many times I heard this axiom growing up—too many to keep count—and I eventually started to hate hearing him say it. But in the end, he was right, and the story about the DuPont engineers over-building the Hanford reactor is a great example of it. They saved the day by going the extra mile.

I'm sure there are many other stories of engineering feats that saved the day due to the persistence of those who made sure that the job was done right the first time. So how does this apply to us now?

Contract Positions

With the way the PCB design industry is changing, many folks are undergoing career changes. Some are changing jobs or fields, and others are looking for contract work rather than full-time employment. For newbies just entering the industry or experienced designers who have always worked for a corporation, the transition to contractor can be a real culture shock. The allure of working from home and setting your own hours can quickly be replaced by the realities of chasing jobs and wondering where your next payday will come from.

However, there are some wonderful aspects of working as a contractor that can make it very worthwhile. You have more freedom to make your own choices about what you will be doing and where, and you are not as tied to a single company or specific way of doing things. Working as a contractor can be great, but the key to success is being prepared for the differences.

Tips

Here are some ideas to help anyone starting a contract position:

• **Show up ahead of schedule:** I've heard from more than one manager who has a negative impression of contractors because they don't seem to follow through on commitments they have made. I've experienced this myself with contractors outside of the PCB design industry, such as painters or builders who arrive days or even weeks late with excuses that would make for excellent plot twists in a novel. Don't be that person. When you commit to being somewhere or doing something, make sure you are ready to go ahead of schedule.

• **Close your mouth and open your ears:** I'm always amazed when I work with someone new in a job and they try to come across as an expert in something they aren't. I realize that the temptation is to try to make a good impression, but doing so when you clearly don't know what you are talking about only makes you look worse. Meanwhile…

• **Don't be afraid to show your expertise when required:** It is likely that you were hired as a contractor because of your expertise in a certain area. When your boss or co-workers look to you for help, this is when you need to shine. However, be cautious of shining so brightly that you blind everyone. You want to be a flashlight that can expertly help others through the darkness as opposed to a floodlight that leaves everyone squinting from too much light.

• **Don't overcharge:** When you bill for the time you've worked, make sure you work more than what you bill. I'm not talking about giving away the farm—just make sure your customers feel like they are getting more than their money's worth. The last thing you want is to become known as the person who cuts out early and isn't worth what they're being paid. It is much better to add a few minutes to your schedule each day so that your customers feel that paying you is a good deal for them.

• **Do the job right:** Thanks for the advice, Dad. I have known people who don't always give their best while at work. This can happen with full-time employment as there are often ways to work the system in order to get away with it. If you've ever read the Dilbert comic strip, you know there are real-life "Wallys" in the work world that always seem to be on a coffee break. This lazy attitude won't work for you as a contractor. If your customer doesn't feel that they are getting the work out of you that they are expecting, they will simply cut you loose. Again, don't be that person. Do your job the best you can.

• **Go above and beyond what is expected of you:** You have the opportunity to show your customers they made a great choice when they hired you. Don't be afraid to go that extra mile and give them more than they expect. Of course, you do have to balance this out with the reality of being paid for your work. You don't want to give away hours of extra work for free, but when you have the chance to take a little time to overachieve, go for it. Be the person that your customers want to continue to work with for a long time.

Conclusion

Most of us do not build nuclear reactors. However, we can learn from the example set by the DuPont engineers at Hanford and make a commitment to be better employees—contractors and part-time or full-time personnel. Not only will this elevate your status in your employer's eyes, but who knows—maybe one day you will get an opportunity to save the day with your extra efforts. It's worth a shot, so go the extra mile.

P.S. I really appreciate you all reading my columns. I hope that my musings have been helpful or at least entertaining. PCB design has been my passion for a long time, and I enjoy sharing my thoughts with the design community. If you have any feedback, shoot me an email. Until next time, keep on designing. DESIGN007

References

1. Preserving the Hanford B-Reactor: A Monument to the Dawn of the Nuclear Age by Robert F. Potter, American Physical Society.
2. B Reactor, Hanford Government.
3. Section 8: B Reactor, National Park Service.

Tim Haag is a PCB design consultant based in Portland, Oregon. To read past columns or contact Haag, click here.

MilAero007 Highlights

IPC Lauds Government Act to Advance Workforce Education ▶

IPC—Association Connecting Electronics Industries is applauding the U.S. Congress for sending legislation to President Trump that will strengthen workforce education and training efforts.

Eltek Receives Non-Compliance Notice from Nasdaq ▶

Eltek Ltd. received a notice from Nasdaq advising that in light of the resignation of Lian Goldstein, an independent director, the company is currently not in compliance with Nasdaq's audit committee requirements as set forth in the Nasdaq Listing Rules.

DARPA's $2 Billion Campaign to Develop Next Wave of AI Technologies ▶

DARPA is currently pursing more than 20 programs that are exploring ways to advance the state-of-the-art in AI, pushing beyond second-wave machine learning techniques towards contextual reasoning capabilities.

George Janosko Joins Ventec International Group Technical Sales Team for Midwest USA ▶

Ventec International Group Co., Ltd., a world leader in the production of polyimide and high-reliability epoxy laminates and prepregs, announced the appointment of George Janosko, responsible for technical sales for the U.S. Midwest.

Calumet Electronics on IMPACT 2018 ▶

This year at IMPACT Washington, D.C., I-Connect007's Patty Goldman sat down with Steve Vairo and Mike Kadlec of Calumet Electronics, to get their overview on the event.

Rockwell Collins and Lockheed Martin to Present a Dual Keynote Presentation at SMTA International 2018 ▶

The SMTA is pleased to announce Ron Heberlein, Rockwell Collins, and Tony "Brick" Wilson, Lockheed Martin, will keynote SMTA International the morning of Tuesday, October 16 with their presentation "The World's Most Advanced Fighter Jet Helmet—from Development and Production to the Fight."

IMPACT on DIVSYS and NWSC Crane ▶

I-Connect007's Patty Goldman has known DIVSYS' Stan Bentley for many years, having met when the company was called Diversified Systems and they made circuit boards and finished products at their facility in Indianapolis. They saw each other at IMPACT recently, and of course had to have a chat.

Army's New 3-D Printed Shape-Shifting Soft Robots Crawl, Jump, Grab ▶

New 3-D printed robotic structures can squeeze in tight spaces like a crack in the wall of a cave, jump over trip wire or crawl under a vehicle—all complex Army-relevant functions impossible for humans to perform safely.

Utility Drones Market to Reach $538.6 Million by 2023 ▶

The global utility drones market is expected to grow from an estimated $110.2 million in 2018 to $538.6 million by 2023, at a CAGR of 37.34% from 2018 to 2023.

Standard PCB Component Families, Part 2

Article by Tom Hausherr
PCB LIBRARIES

Today, there are a wealth of PCB components and packages available to the PCB designer and design engineer. Any senior designers who were laying out boards in the 1970s can remember when this was certainly not the case.

The August issue of *Design007 Magazine* featured Part 1 of this compendium of standard PCB component families. This month, we present Part 2 of this collection.

To read Part 1 of this series, click here.

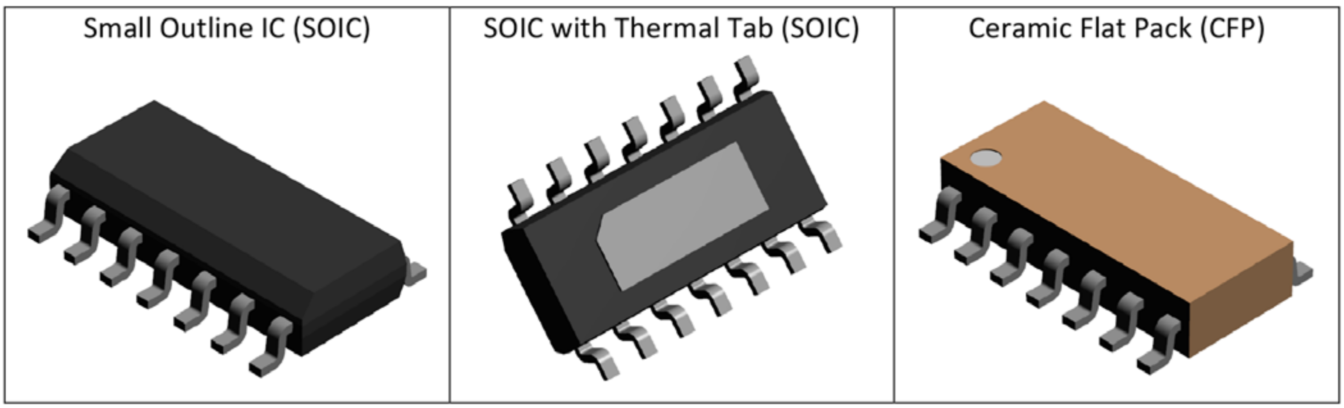


Figure 1: Small Outline IC (SOIC) Note: Pin pitch is imperial units 0.050″ (1.27 mm).

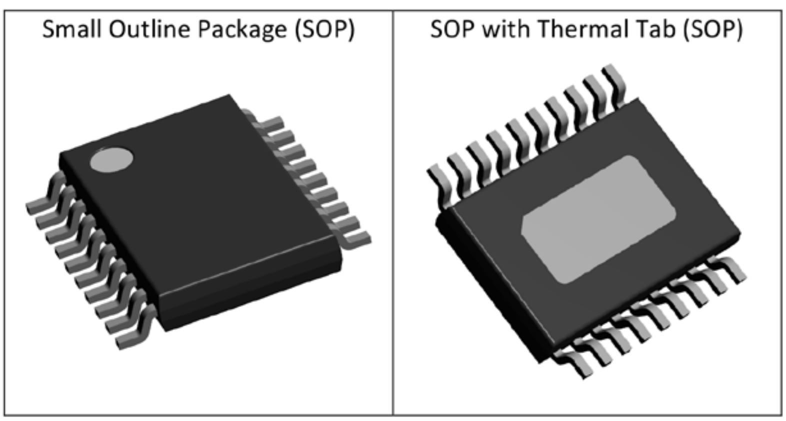


Figure 2: Small Outline Package (SOP) Note: Pin Pitch is metric units 1.00, 0.80, 0.65, 0.50 & 0.40.

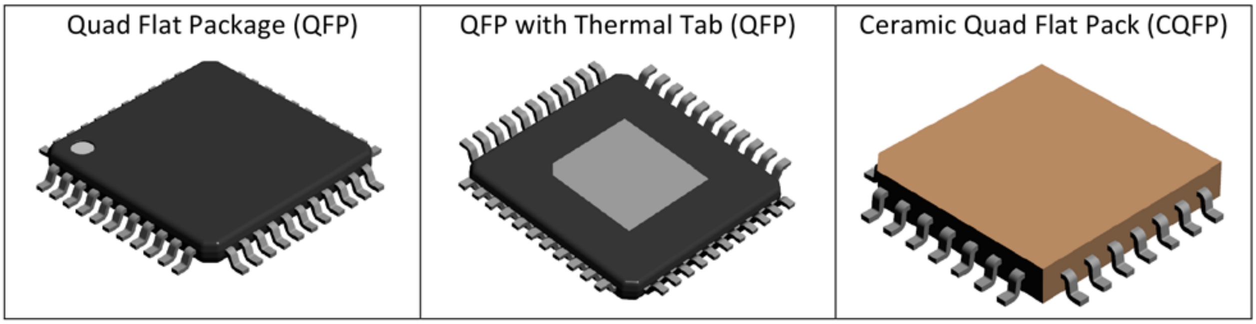


Figure 3: Quad Flat Package (QFP & CQFP).

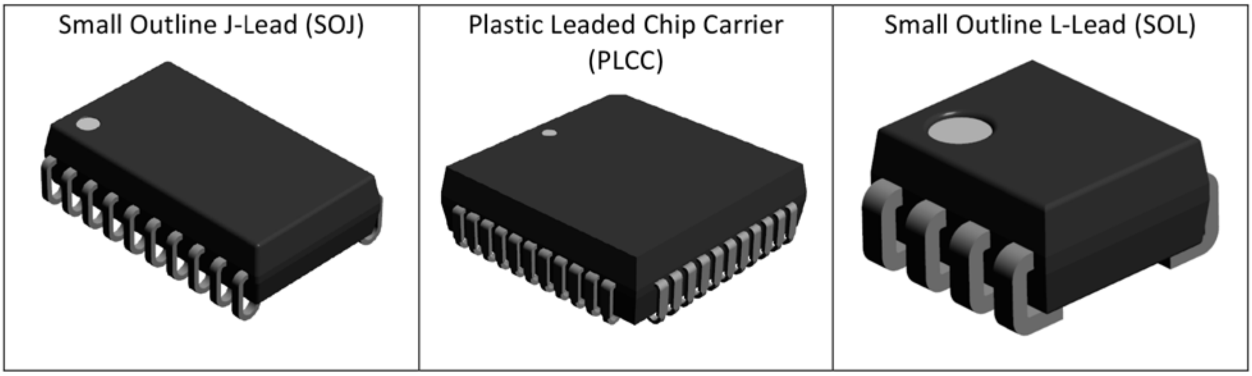


Figure 4: J-Lead & L-Lead Packages (SOJ, PLCC & SOL).

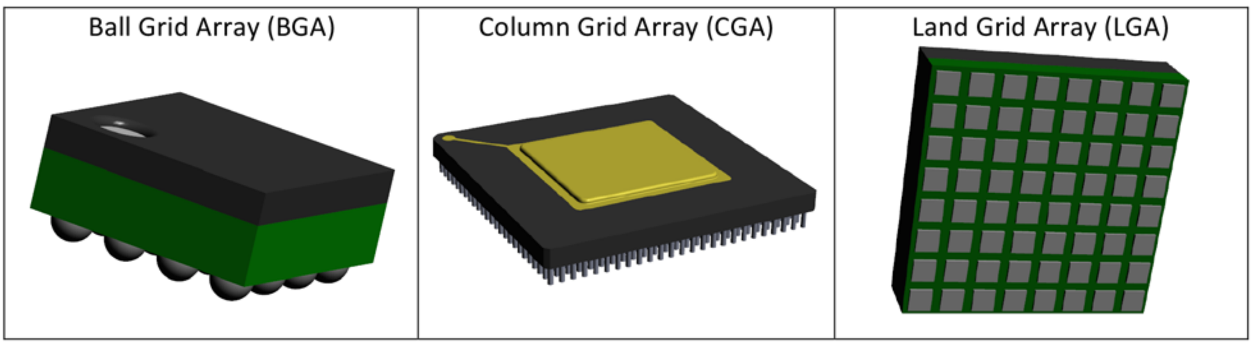


Figure 5: Grid Array Packages (BGA, CGA & LGA).

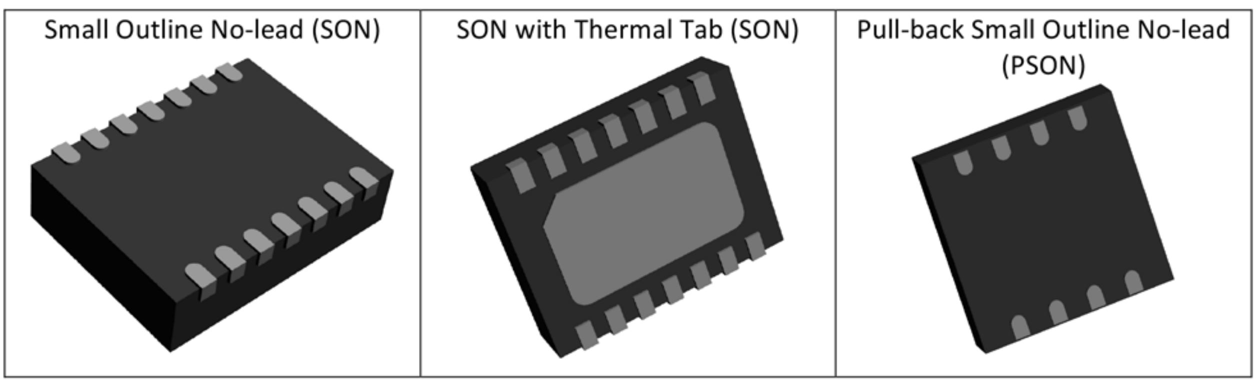


Figure 6: Small Outline No-lead (SON & PSON).

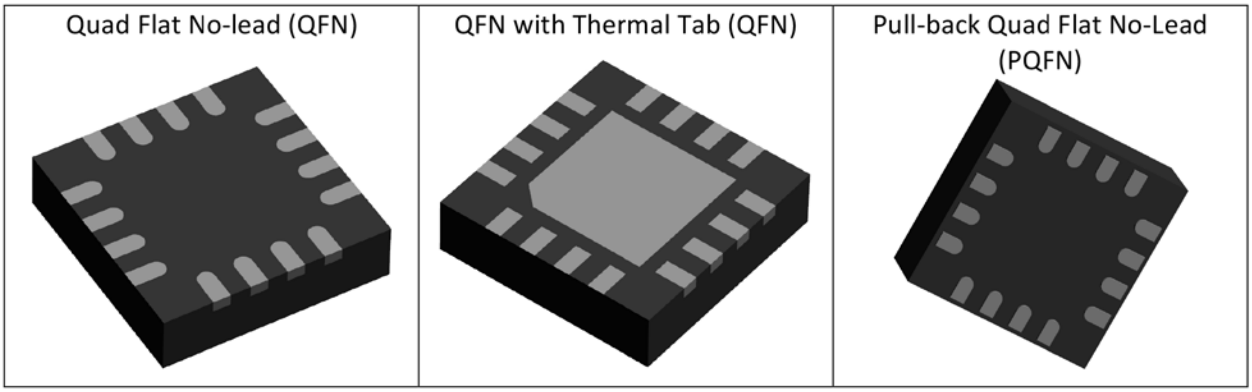


Figure 7: Quad Flat No-lead (QFN & PQFN).

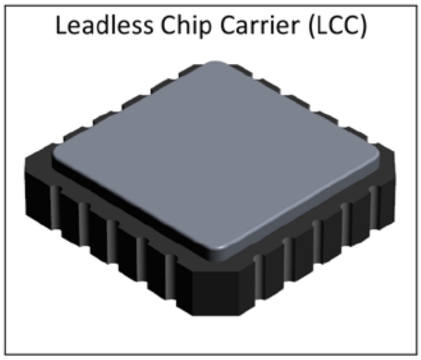


Figure 8: Leadless Chip Carrier (LCC).

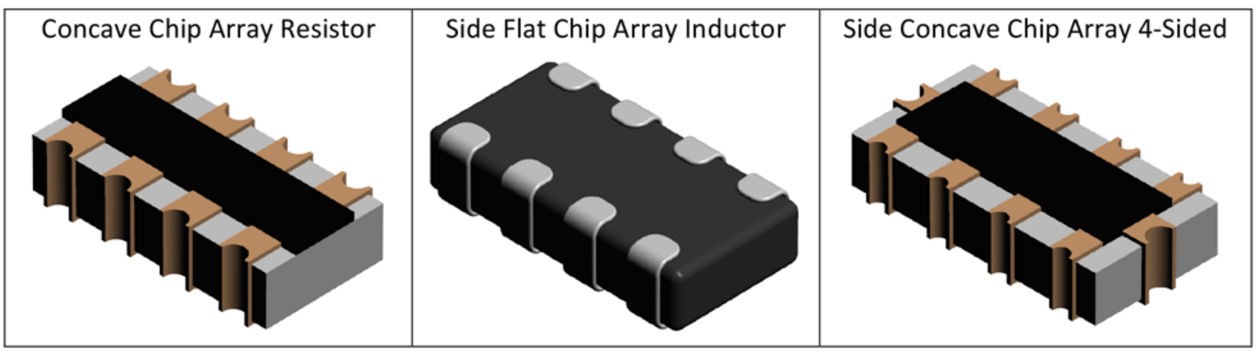


Figure 9: Resistor, Inductor & Capacitor Side Concave Chip Array (RESCAV).

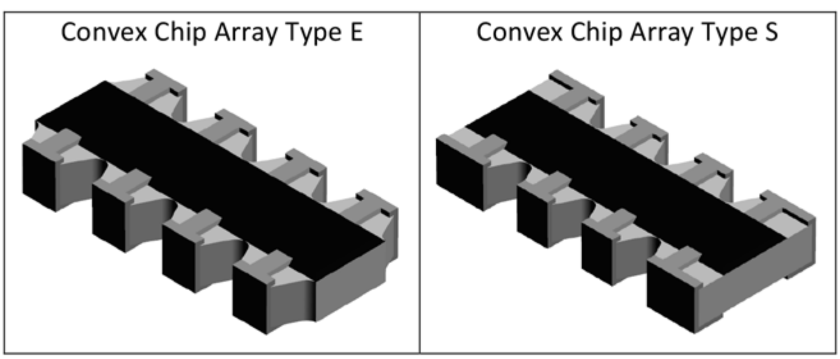


Figure 10: Resistor, Convex Chip Array Type E & S (RESCAXE & S).

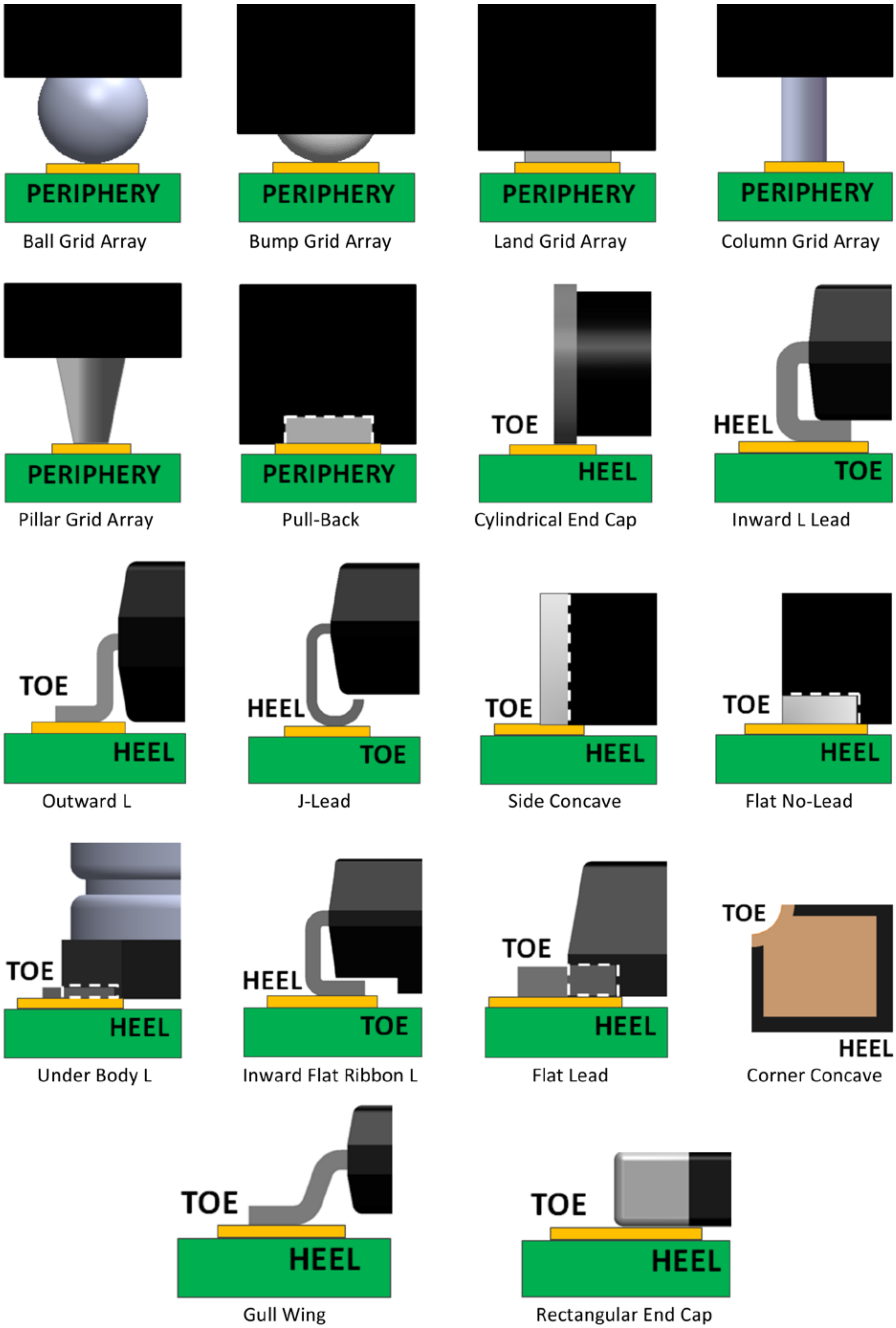


Figure 11: Surface Mount Component Terminal Lead-Forms.

Standard Through-hole Component Families

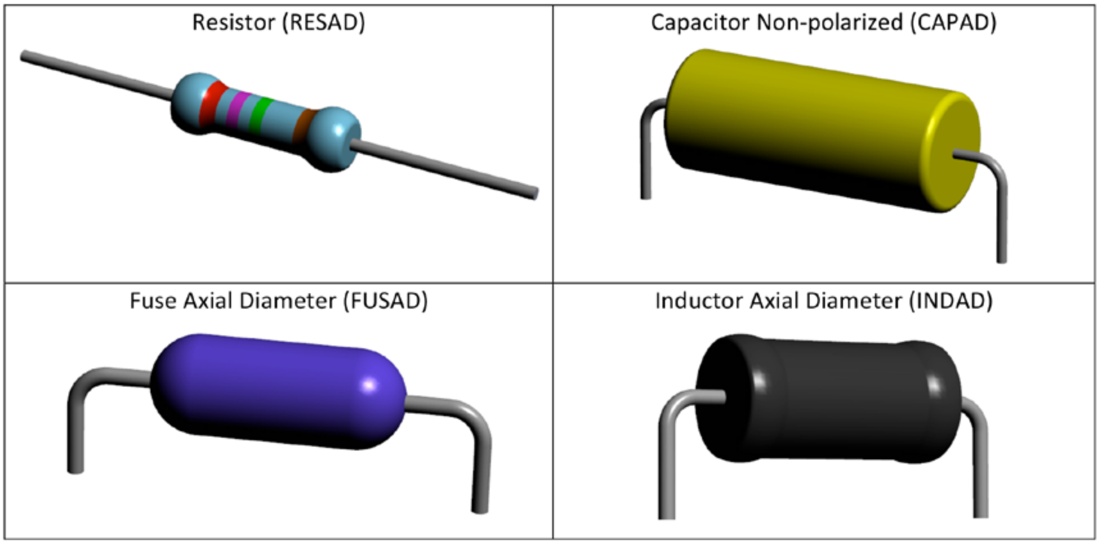


Figure 12: Non-polarized Axial Diameter Leaded Component.

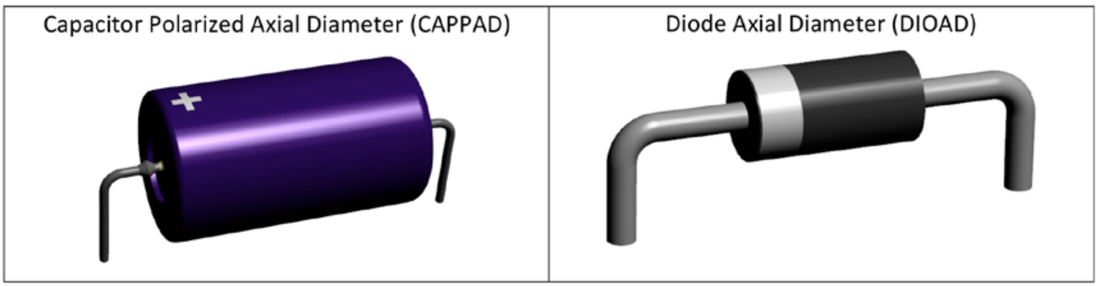


Figure 13: Polarized Axial Diameter Leaded Component.

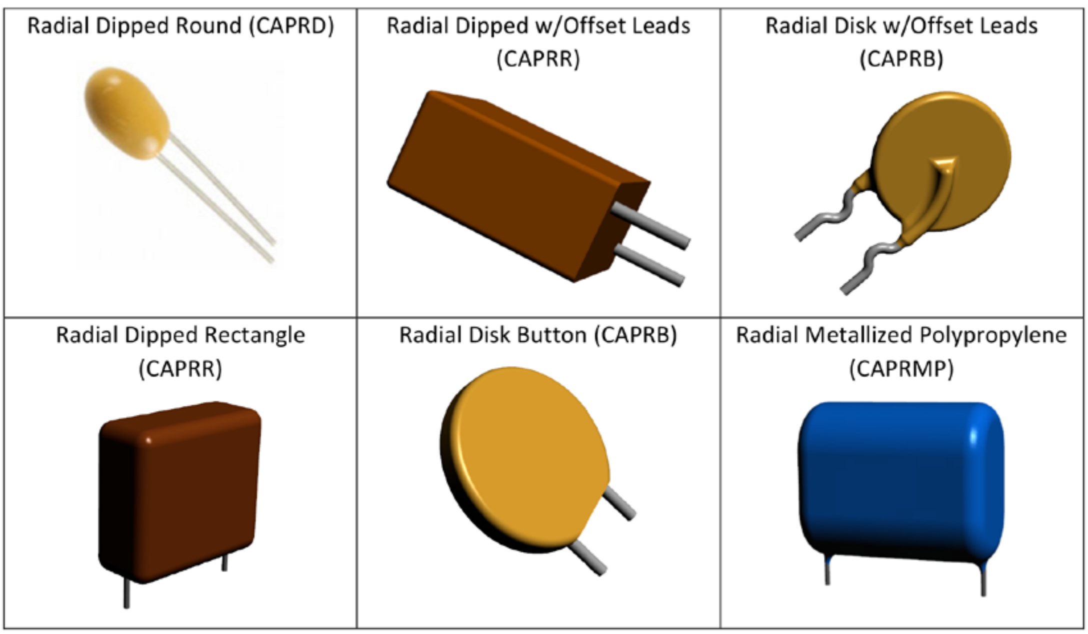


Figure 14: Non-polarized Radial Rectangular Leaded Component.

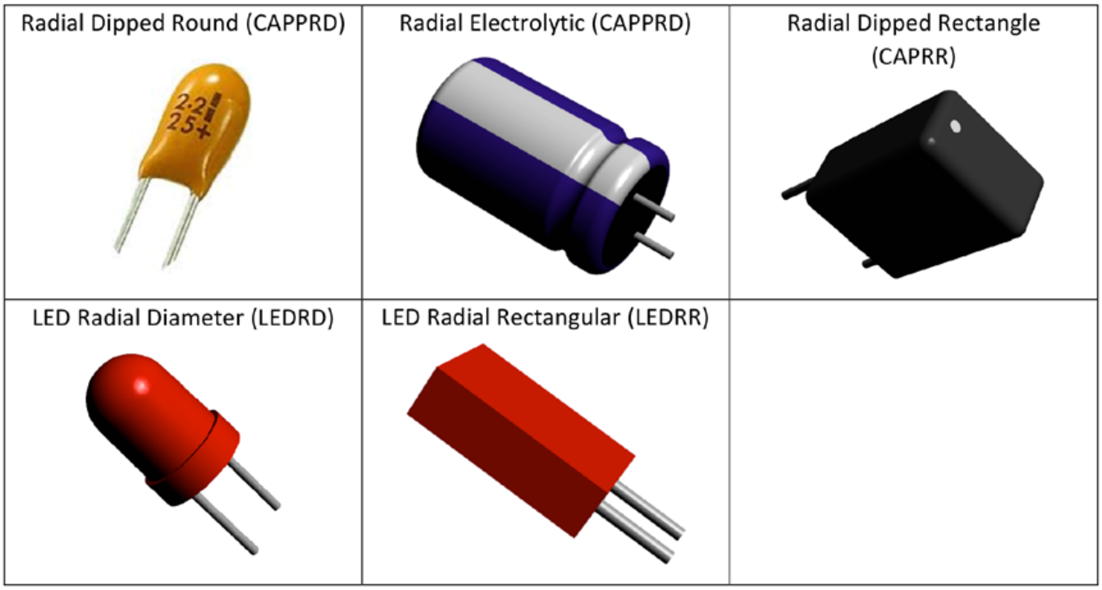


Figure 15: Polarized Radial Rectangular Leaded Component.

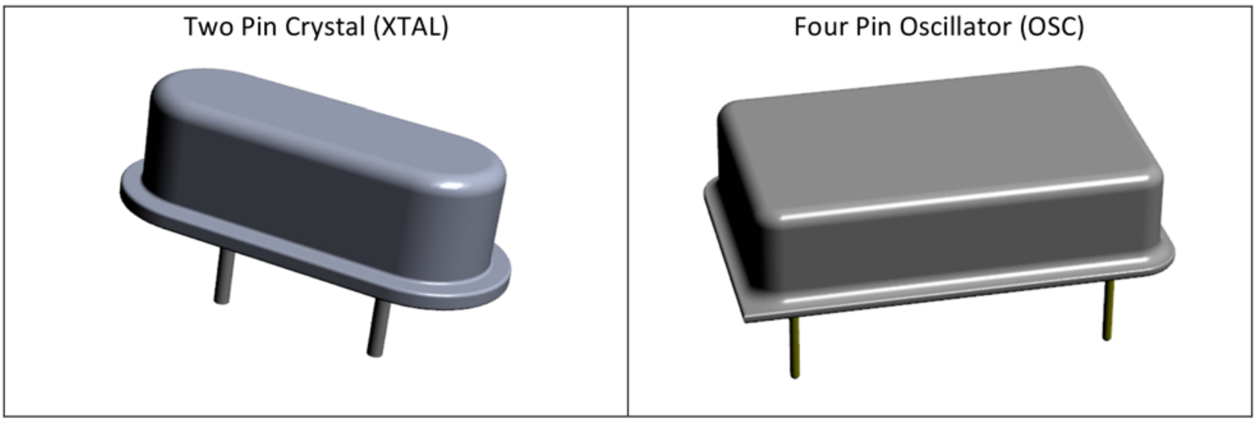


Figure 16: Two Pin Crystal (XTAL) and Four Pin Oscillator (OSC).

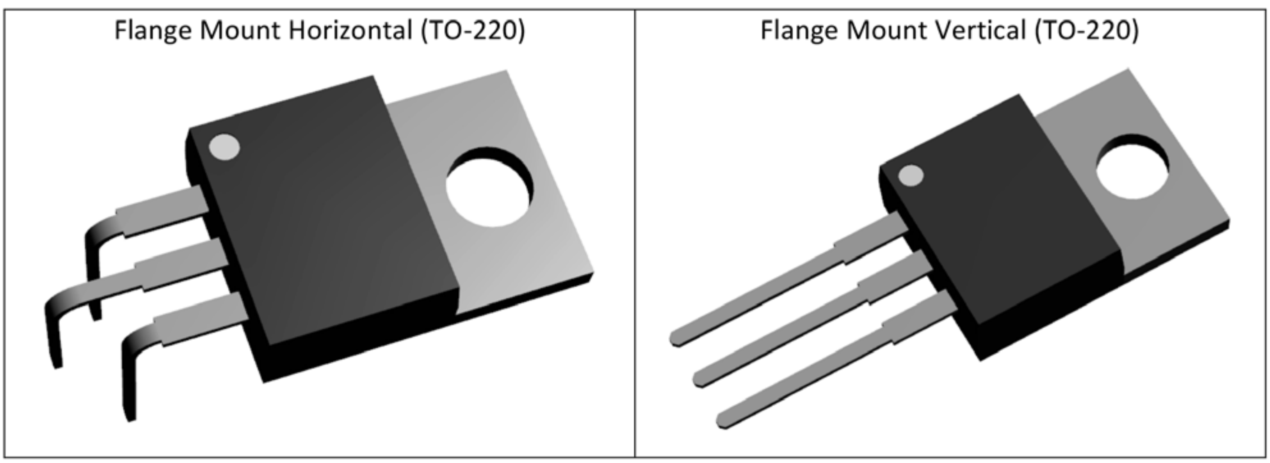


Figure 17: Flange Mount Horizontal (TO-220).

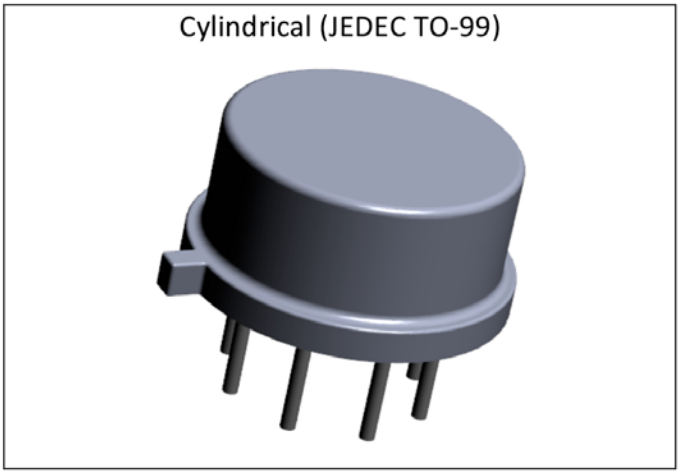


Figure 18: Cylindrical (JEDEC TO).

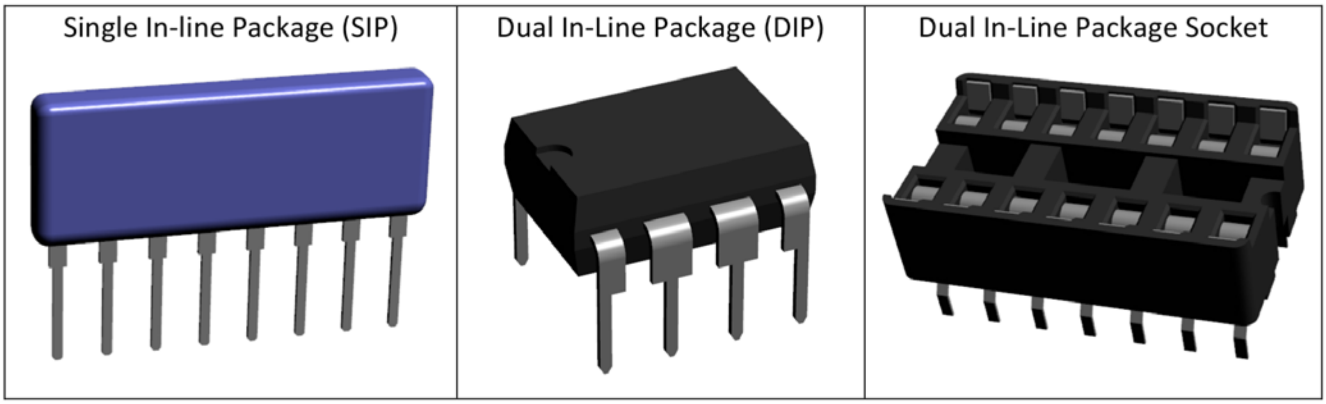


Figure 19: Single In-line Package (SIP) & Dual In-Line Package (DIP).

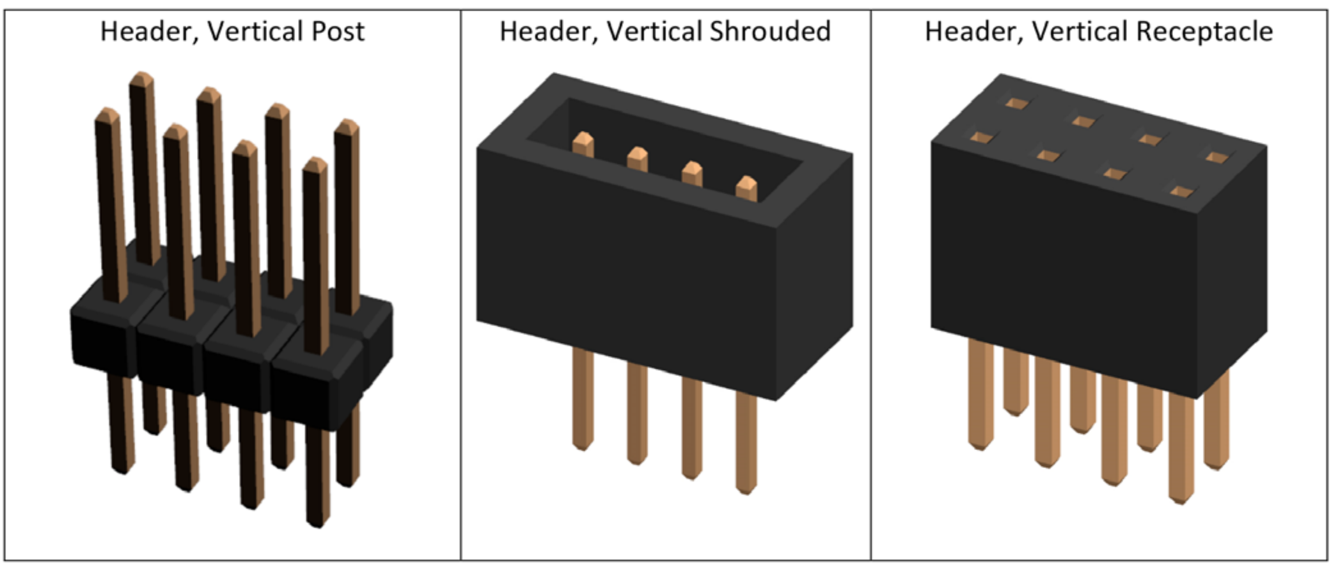


Figure 20: Header, Vertical (HDR).

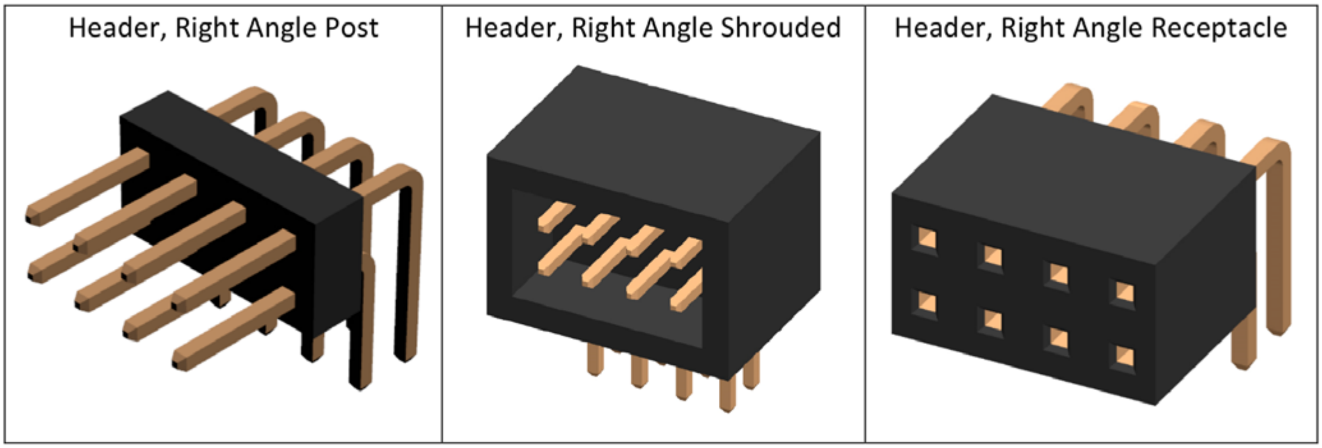


Figure 21: Header, Right Angle (HDRRA).

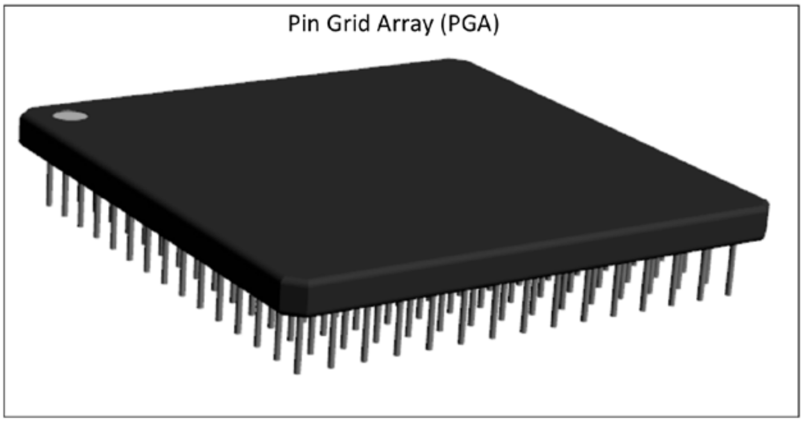


Figure 22: Pin Grid Array (PGA).

All 3D package models in this article were auto-generated by the free Library Expert Pro using package dimensions provided by the component manufacturer datasheet. **DESIGN007**

Tom Hausherr CID+, CIT, is president of PCB Libraries.

Bismuth Shows Novel Conducting Properties

A team of international scientists including Maia G. Vergniory, Ikerbasque researcher at DIPC and UPV/EHU associate, have discovered a new class of materials: higher-order topological insulators.

According to theoretical studies, the conducting edges are extraordinarily robust for higher-order topological insulators: the current of topological electrons cannot be stopped by impurities and if the crystal breaks, the new edges automatically also conduct current. However, the most extraordinary property of these new materials is that they can in theory conduct electricity without any dissipation as superconductors do at low temperatures. This would be a specific property of higher-order class topological insulators.

Now, thanks to a wider scientific collaboration where scientists from Paris-Sud University and CNRS were also involved, it has been confirmed that bismuth, an element consistently described as bulk topologically trivial, follows a generalized bulk-boundary correspondence of higher-order, that is, hinges host topologically protected conducting modes instead of the surface of the crystal.

Finally, this work establishes bismuth as a higher-order topological insulator and opens the way to identify new ones.

(Source: University of the Basque Country)

Achieving Minimal Crosstalk in Multi-Board Interconnect

Article by Chang Fei Yee
KEYSIGHT TECHNOLOGIES

This article discusses the impact of signal routing and return path or reference on crosstalk in multi-board interconnect. The investigation is performed with 3DEM simulation using Keysight EMPro. Subsequently, crosstalk in frequency and time domain are observed, along with surface current density on the return path.

Introduction

In an electronic system, the signal transmission exists in a closed-loop form. The forward current propagates from transmitter to receiver through the signal trace. On the other hand, for a single PCB, the return current travels backward from receiver to transmitter through the ground plane closest to the signal trace. Meanwhile, for multi-board interconnect (e.g., connectivity through flex or ribbon cable), the return current travels back to the transmitter through the ground or return wire, preferably as close as possible to the signal wire. The path of forward current and return current forms a loop inductance.

It is important to provide sufficient ground or return wire in multi-board interconnect. Otherwise, the "return current" might detour and propagate on a longer path that leads to the sharing of common return wire or path by different signals that poses high risk of interference or coupling among the signals due to higher mutual inductance. This interference results in signal crosstalk. This phenomenon is proven in the following section with 3DEM simulation [1].

Analyzing Crosstalk with 3DEM Modeling

To investigate the impact of signal routing and the return path on multi-board signal integrity, three test models of 3DEM were constructed using Keysight EMPro. In test case 1 (Figure 1), two microstrip signal traces (shown in brown) with 50 ohm characteristic impedance in single-ended mode on board "A" are connected to board "B" using flex cable. The signal traces on each board are 100 mils long, 1.2 mils thick and 5 mils wide. The solid ground plane exist

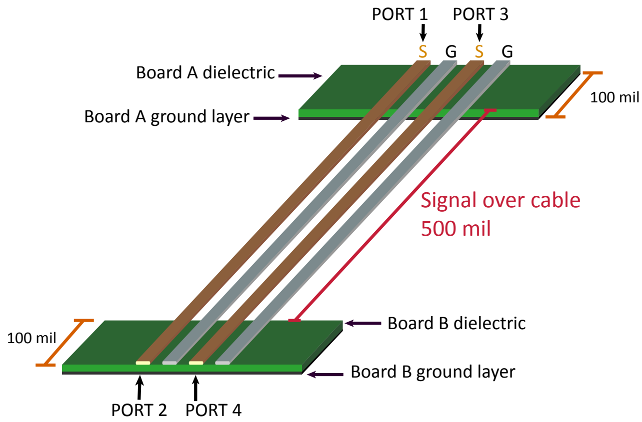


Figure 1: The 3DEM structure in test case 1.

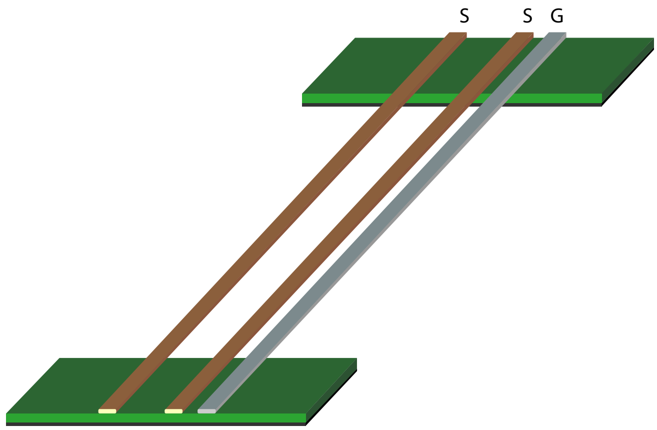


Figure 3: The 3DEM structure in test case 3.

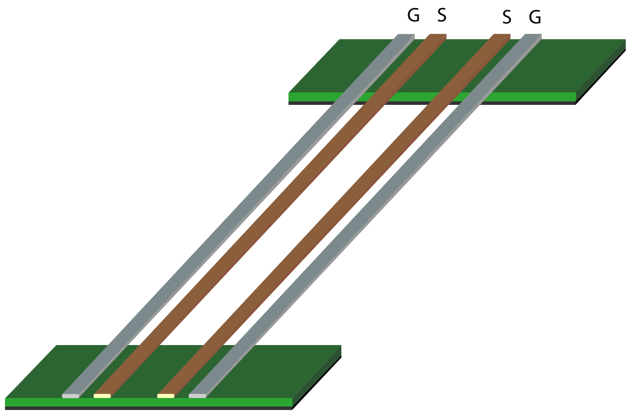


Figure 2: The 3DEM structure in test case 2.

3 mils beneath the signals on each board. FR-4 is used as the PCB dielectric substrate. The two signal traces on each board are 15 mils apart (i.e., triple of the signal trace width for minimum crosstalk). The ground trace (5 mils in width, shown in grey) is placed 5 mils away to the right of each signal trace to electrically connect the ground or reference plane of each board. On the other hand, the signal and ground traces over the flex cable are 500 mils long.

From a crosstalk perspective, port 1 and port 2 represent the transmitting and receiving end, respectively, of the aggressor line. Meanwhile, port 3 and port 4 represent the transmitting and receiving end, respectively, of the victim line.

In test case 2 (Figure 2), the 3DEM structure is similar to test case 1, except the ground trace between the two signal traces are placed 5 mils away to the left of the port 1 signal. This is to simulate the negative impact of ground trace removal on the forward signal crosstalk vs. test case 1.

But in test case 3 (Figure 3), the 3DEM structure is left with only a single ground wire connecting electrically the reference planes of board "A" and "B." The rest of this example is the same as test case 2. This is to simulate the effect of insufficient ground or return wire on crosstalk vs. test case 2.

The S-parameters of the 3DEM models in these test cases are plotted in Figure 4 (i.e., spans from 1MHz to 8GHz). S41 parameter represents far-end crosstalk (FEXT). A more severe signal crosstalk is indicated by smaller absolute value in dB. With reference to Figure 4, across the wide band range, the most severe FEXT is experienced in test case 3, followed by case 2 and the least severe in case 1.

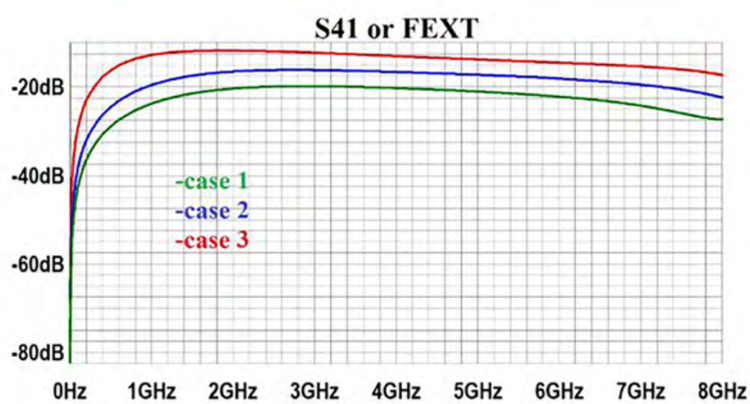


Figure 4: Simulated plots of S41 (FEXT).

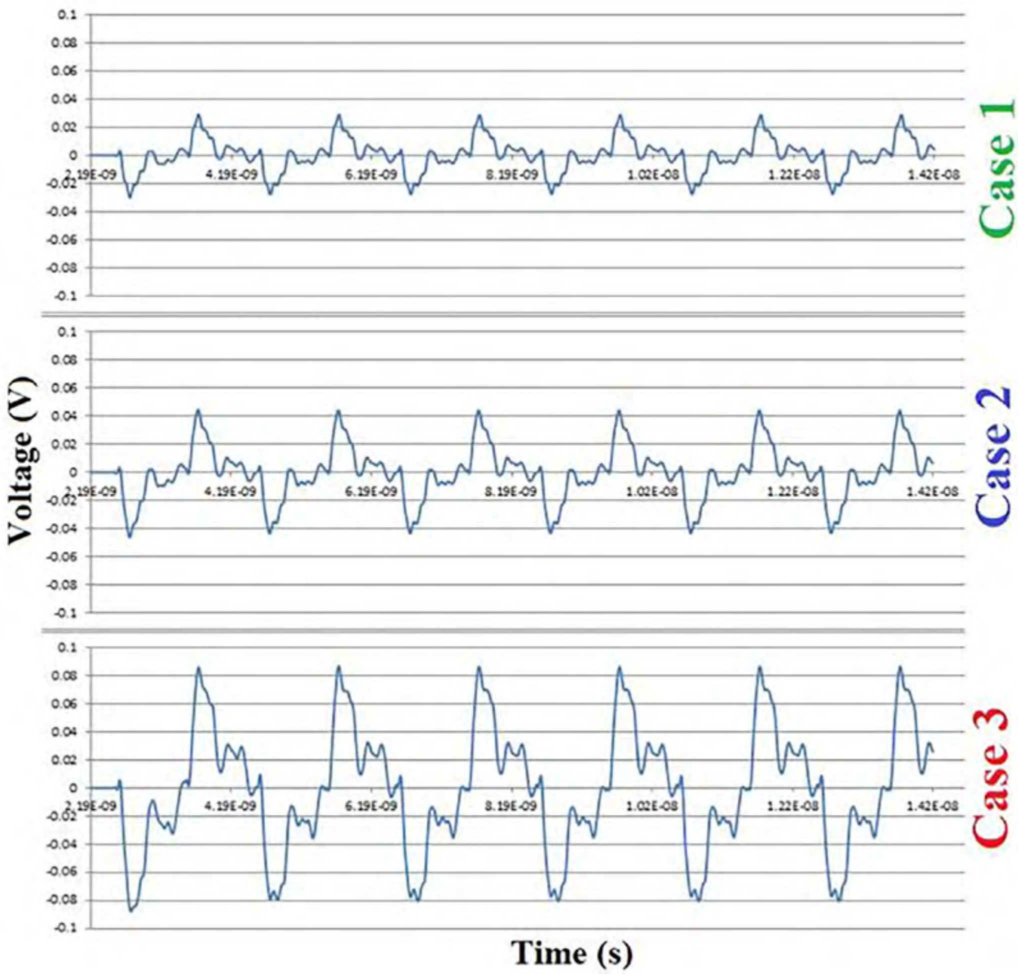


Figure 5: Noise induced at victim's far end-point due to crosstalk for three test cases.

Subsequently, transient simulation was performed for the abovementioned three test cases to observe the phenomenon of FEXT in time domain. In this transient simulation, a square wave signal with 500MHz Nyquist frequency, 1.2Vpp amplitude and 3V/ns slew rate is injected into port 1 of each test case's 3DEM model, with port 3 being pulled low (i.e., serves as near end point of victim line), followed by probing at port 4 (i.e., serves as far end point of victim line). Referring to Figure 5, the noise induced at the far end-point of the victim line in time domain for test case 1, 2 and 3 is 60mVpp, 90mVpp and 170mVpp, respectively.

The least severe crosstalk is encountered in test case 1 because each signal has its own return path, and the ground trace between the two signal traces minimizes the crosstalk between them. This structure provides a perfect and sufficient return path for the signal. In test case 2, each signal has its own return wire or path too. However, ground trace removal between the two signal traces worsens the forward signal crosstalk vs. test case 1. On the other hand, for test case 3, there is only a single ground wire connecting the reference planes of two boards. This sole ground wire becomes the return path bottleneck of the two signal traces and results in more critical crosstalk for the return current vs. test case 2, contributed by the sharing of a common return path by different signals that intensifies the interference or coupling among the signals due to higher mutual inductance.

Lastly, the surface return current density on ground wire for these three test cases is depicted in Figure 6. When a square wave at 500 MHz Nyquist frequency is injected at both

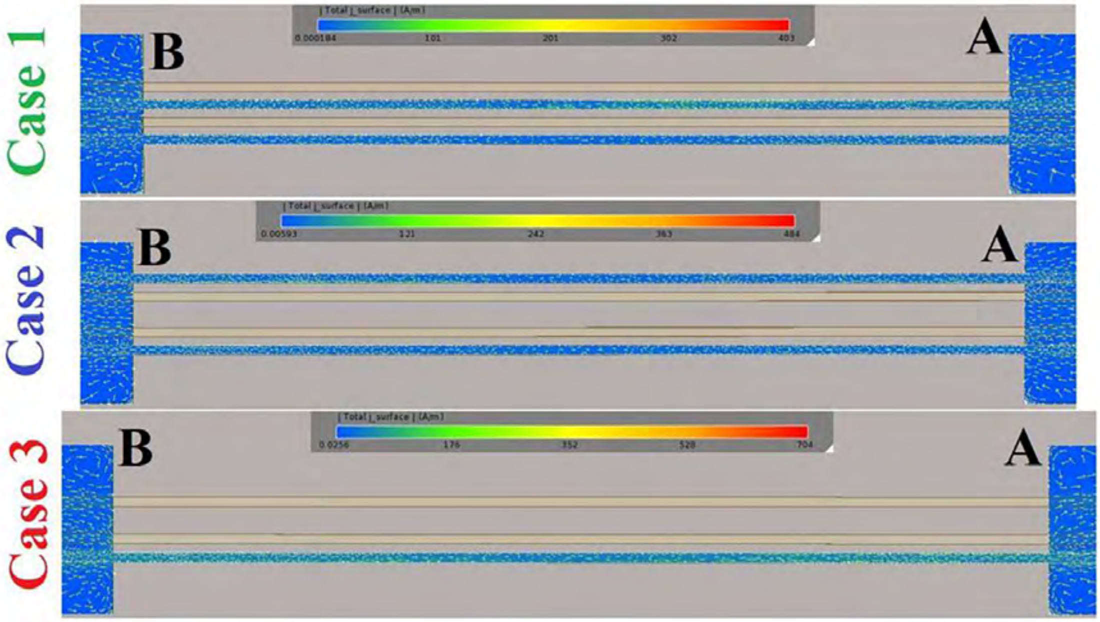


Figure 6: Surface current density on ground wire for the three test cases.

Port 1 and 3 in the same phase respectively, the forward current flows along the signal wires from board "A" to "B," whereas the return current flows along the ground wires from board "B" back to "A." The surface return current density for test case 1, 2 and 3 is 40A/m, 50A/m and 90A/m respectively. Current density for case 3 almost doubles vs. the other two cases, because its sole ground wire becomes the return path bottleneck to be shared commonly by two signal traces.

Summary

It is crucial to provide a continuous and sufficient ground or return path for signals during multi-board connection to minimize signal crosstalk. This is achievable by assigning signal routing in the pattern of signal-ground-signal-ground. **DESIGN007**

References

1. Keysight EMPro guide.

Chang Fei Yee is a hardware engineer with Keysight Technologies. His responsibilities include embedded system hardware development, and signal and power integrity analysis.

Diamond Dust Enables Low-Cost, High-Efficiency Magnetic Field Detection

UC Berkeley engineers have created a device that reduces the energy needed to power magnetic field detectors.

"The best magnetic sensors out there today are bulky, only operate at extreme temperatures and can cost tens of thousands of dollars," said Dominic Labanowski, a postdoctoral researcher in the Department of Electrical Engineering and Computer Science. "Our sensors could replace those more difficult-to-use sensors in a lot of applications from navigation to medical imaging to natural resource exploration."

Medical applications of magnetic sensors include magnetoencephalography or magnetocardiography. The sensors could also be placed in planes or drones to aid in spotting rare earth metals underground, or in cell phones.

(Source: UC Berkeley)

Life Beyond 10 Gbps: Localize or Fail!

Article by Yuriy Shlepnev
SIMBERIAN INC.

What does it take to design predictable PCB or packaging interconnects operating at tens of Gbps? Properly identified dielectric and conductor roughness models, known manufacturer geometry adjustments, and properly validated simulation tools are necessary conditions. One of the sufficient conditions is the localization property; to be predictable, all elements of an interconnect link must be localized up to a target frequency. This article introduces and illustrates the localization concept, with the power-flow density computed using the unique Trefftz finite element solver available in Simbeor THz software.

Ideally, all interconnects should look like uniform transmission lines (or wave-guiding structures) with the specified characteristic impedance. In reality, an interconnect link is typically composed with transmission lines of different types (microstrip, strip, coplanar, coaxial, etc.) and transitions between them such as vias, connectors, breakouts and so on. Transmission lines may be coupled to each other that cause crosstalk. The transitions may reflect and radiate energy due to discontinuities in signal and reference conductors. The crosstalk, reflections and radiation cause unwanted and sometime unpredictable signal degradation. If analysis of traces or via hole transitions is possible in isolation from the rest of the board up to a target frequency, the structure is called localized [1]. Structures with behavior that is dependent on other structures and board geometry are called not localized, and they should not be used in multi-gigabit interconnects in general.

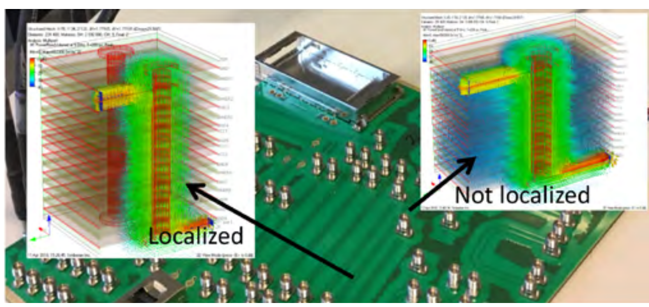
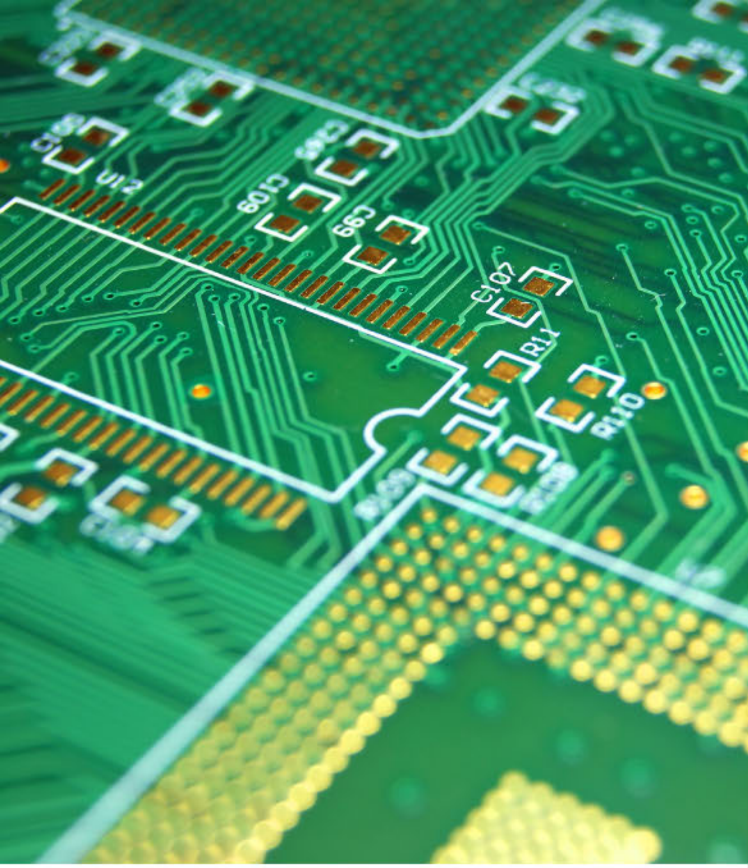


Figure 1: Localized vs. not localized.



Examples of non-localized structures are coupled traces, striplines with non-connected reference planes, traces crossing gaps in reference planes, vias with far, no or insufficient stitching vias (vias connecting reference planes of the connected traces). Analysis of non-localized structures is usually possible only at the post-layout stage with substantial model simplifications that degrade accuracy at higher frequencies. To design predictable interconnects, only localized structures must be used—this is one of the most important elements for design success. The localization is always bandwidth limited for striplines (two reference conductors) and for vias (two or more reference conductors). How do we estimate the localization property of a transition? One way is to run an electromagnetic analysis of the structure with different boundary conditions or simply change simulation area size without changing phase reference planes and evaluate the differences in the computed S-parameters. If the difference is small, the structure may be considered localized and suitable for final design [2]. Alternatively, compute and plot the power-flow density and literally see the localization of the signal in space as illustrated in Figure 2.

First, let's get familiar with the power-flow density concept using a simple example and analogy with the circuit theory for a stripline structure in Figure 2.

Voltage in the circuit theory corresponds to the modal electric field intensity E, current corresponds to the modal magnetic field intensity H. Cross-product of the electric field and magnetic field intensities is the vector of power-flow density (or Poynting vector), measured in Watt/m^2. It is energy through unit area in space transferred in one second. When we look at the power-flow density vectors, we basically see where the energy of the signal is in space around a trace or via hole. Total power through a cross-section of the stripline corresponds to the power flow in corresponding transmission line model, equal to product of the voltage and current. To understand the localization concept, it is very important to know that the signal energy is actually distributed in space around each element of interconnect structure. For instance, the power-flow density of the dominant quasi-TEM mode in stripline is shown in Figure 3 at four frequencies.

The strip is 1.2 mil thick, 7 mil wide trace, in homogeneous dielectric with Dk = 3.76, LT = 0.006 @ 1 GHz, planes 0.77 mil thick and 17.2 mil apart, 1 V excitation and 50-ohm terminators.

The power-flow density is depicted by vectors with the direction along the t-line (into the picture) outside of the conductors. The value of the vectors is expressed with color scale in dB from zero (red color) to -60 dB (blue color).

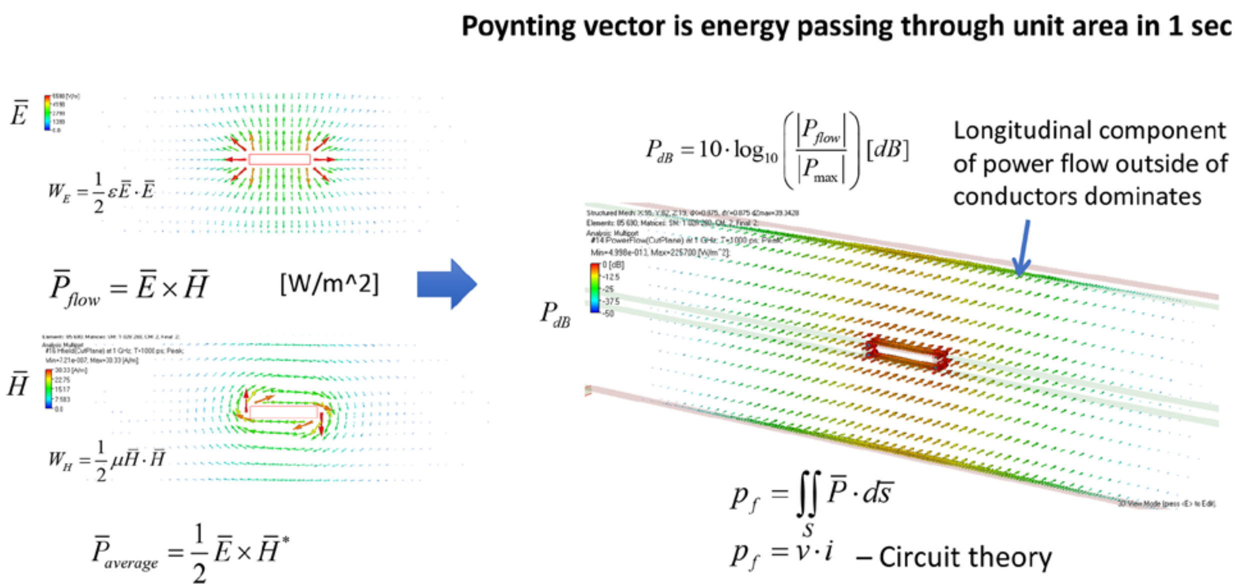


Figure 2: Simple example of the power-flow density concept.

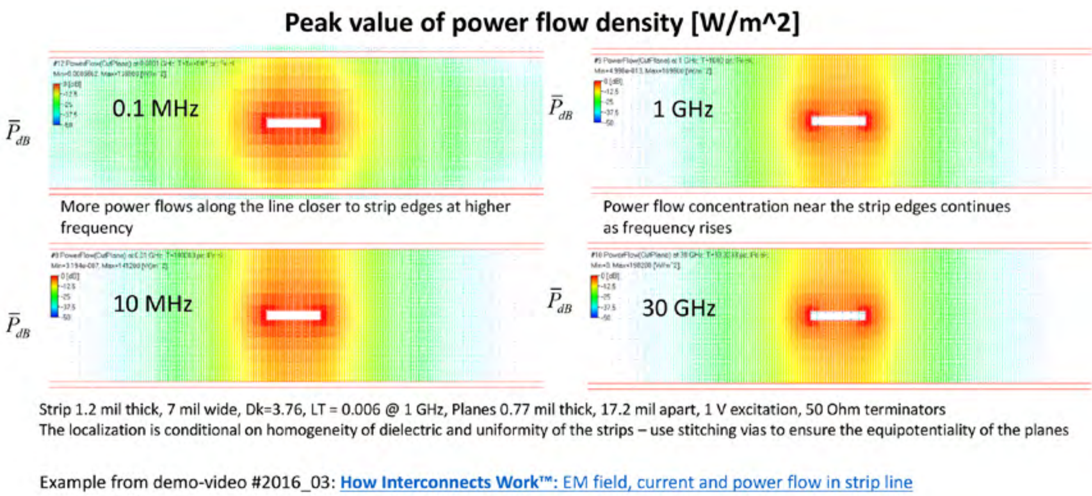


Figure 3: The power-flow density of the dominant quasi-TEM mode in stripline at four frequencies.

The power-flow drop by 0.5 corresponds to -3 dB, by 0.1 to -10 dB, by 0.01 to -20 dB and so on. We can observe that the maximal power density is uniform around the strip at lower frequencies and concentrates around the strip edges at higher frequencies. As we can also see, the power of the signal drops around the strip rather quickly to -50 dB (by 0.00001 times). We can say that the structure is well localized if there is nothing in the area with the significant power flow (no coupling to the other strips for instance).

However, the localization is conditional on homogeneity of dielectric and uniformity of the strips. If such conditions are not satisfied (and they are usually not satisfied for PCB interconnects—dielectrics are not homogeneous and there are large variations in manufacturing), the energy of the quasi-TEM mode can be transformed into the dominant TEM wave of the parallel plate waveguide formed by the top and bottom plane. To avoid it, the stitching vias connecting the planes should be used along the traces at higher frequencies. The distance between the stitching vias should be less than half of wavelength in dielectric at the highest frequency of interest—and that may be a lot of additional vias. The stripline localization can be easily violated if the equipotentiality of the reference planes is not ensured with the stitching vias. The result is the signal energy leak along the trace (observed on TDR as flat or decreasing impedance). Due to the reciprocity it works both ways—the energy of the power distribution network can be coupled to the trace, if it is not localized with the stitching vias.

Now let's take a look at the power-flow density in via holes. One of the links on EvR-1 board was designed by Marko Marin with two single-ended vias specifically to test the localization importance. One of the vias has two stitching vias at about 30 mils from the signal via, and another has no stitching vias in the vicinity, as shown in Figure 4.

This is an example from an award-winning DesignCon 2018 paper the author co-wrote with M. Marin, *40 GHz PCB Interconnect Validation: Expectations vs. Reality* [3]. We used the "sink or swim" formula for predictable interconnect

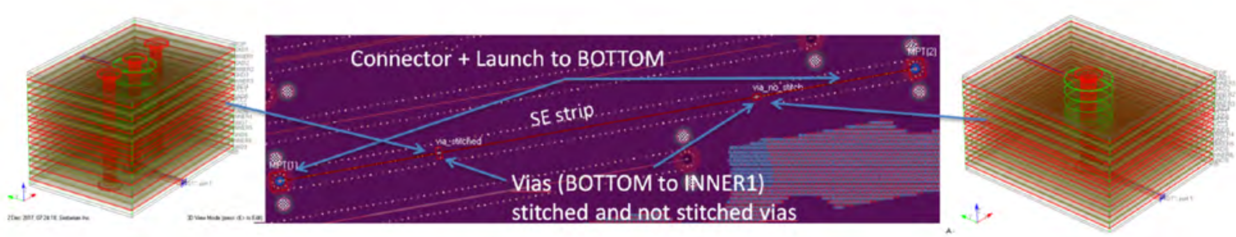


Figure 4: Two vias, one with two stitching vias and one without.

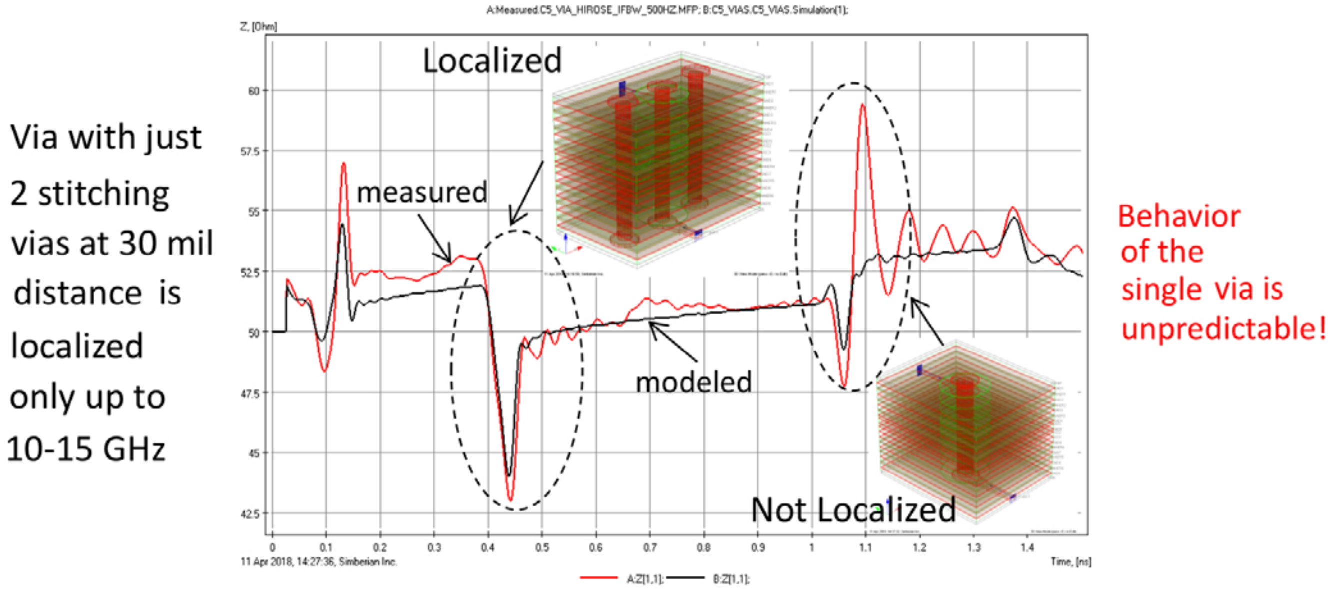


Figure 5: A TDR plot shows discrepancies in measurements.

design that is based on tree components: interconnect geometry adjustments + identified material models + validated software -> predictable interconnects. With all three components in place, we were able to reliably predict behavior of most of the interconnect structures on EvR-1 board without additional tuning or calibration for 28-30 Gbps NRZ signal. However, the analysis to measurement correlation was acceptable only up to about 5 GHz for the structure with the non-localized via. It makes it predictable for signals with only about 3-5 Gbps data rate. The TDR plot shown in Figure 5 reveals the large discrepancies in the measurements and the model at the location of the single via without the stitching vias. We can see some oscillations at the via location, which means that the via is coupled to a resonating cavity formed by parallel planes and multiple distant vias around the traces.

To see how the coupling occurs, let's use the power-flow density visualization. The 1 V signal source is connected to the microstrip port at the bottom of the board. Both microstrip and stripline ports are terminated with 50 ohm. As we can see, the power from the microstrip at the bottom does not go all the way to the stripline in the layer INNER1; some energy is radiated into the inter-plane areas as shown in Figure 6 for 5 GHz (peak values of the power-flow density).

This model uses absorbing boundary conditions on the outside boundaries of the simulation domain; it absorbs the energy of the parallel plane waves going from the via. For instance, Figure 7 is a close-up of what is going on between reference planes GND7 and GND8—the power flows along the via in the anti-pad area and flows mostly outward between the parallel planes and is absorbed at the outer boundary.

In reality, the energy injected into the inter-plane area does not completely disappear—it may be reflected from the fences formed by vias and returned back to the signal via in form of the oscillations observed on TDR above (coupled to cavities formed by distant stitching vias). Behavior of such vias can be predicted only in the post-layout analysis with either huge computational cost (large simulation area) or with simplified models of the whole board with substantial model accuracy degradation. The easier alternative is to localize it.

The second via in this link was designed to test the effectiveness of placing two stitching

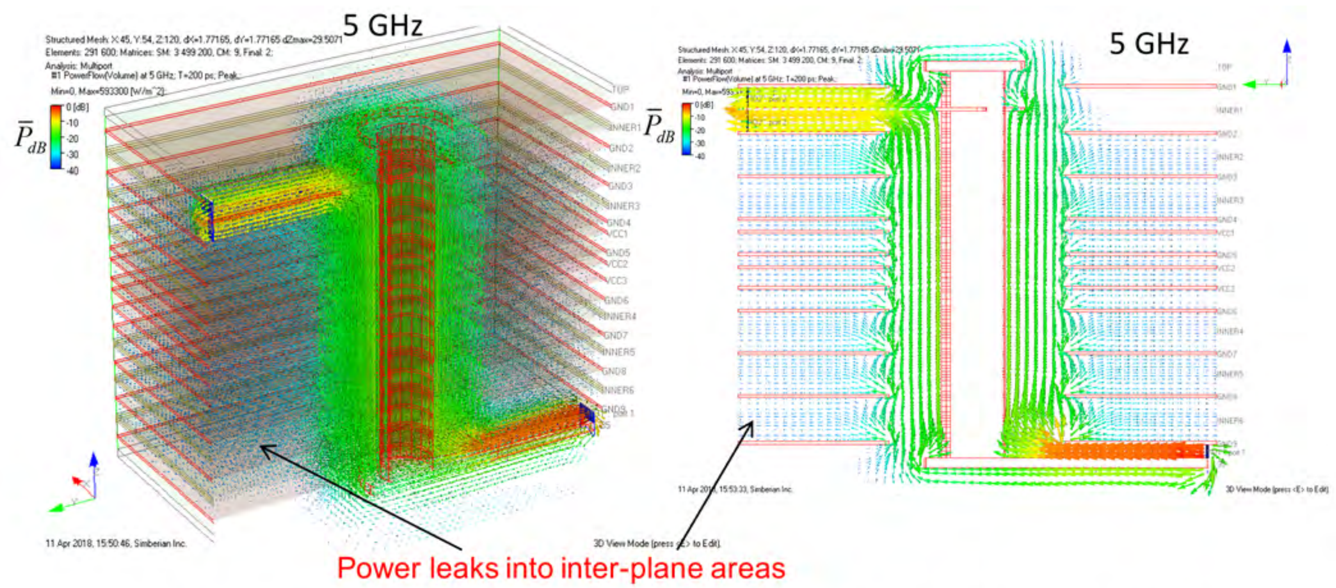


Figure 6: Power from the microstrip does not go all the way to the stripline in layer INNER1.

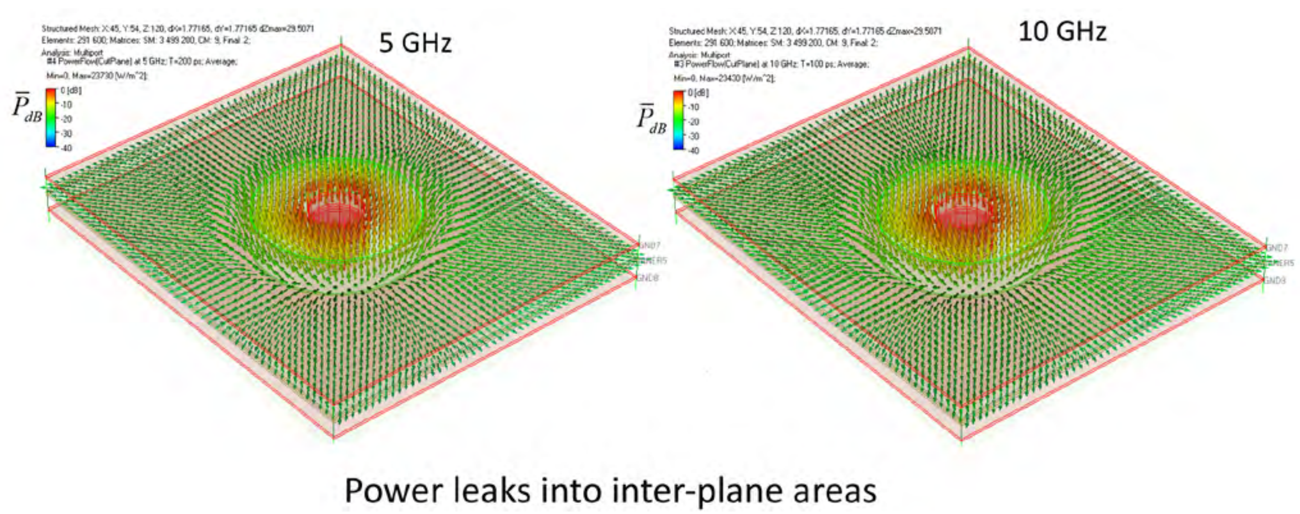


Figure 7: A close-up of interaction between reference planes GND7 and GND8.

vias about 30 mil from the signal via. The TDR correlation for this via is acceptable, so let's look at Figure 8 and Figure 9 to see how the power propagates along that structure at different frequencies.

What a difference two properly designed stitching vias make! The localization bandwidth of the single via is extended to 15-20 GHz. The localization degrades progressively starting from about 20 GHz in this case—it means that this via becomes coupled to the parallel plane structures with all the unpredictability consequences as we observed for the single via. What if we want to extend the frequency range to 50-60 GHz? That is very difficult task for the single-ended through vias in general. Just take a closer look at an example of the single via launch localized up to about 60 GHz with 17 stitching vias as shown in Figure 10.

This via transition was designed by Scott McMorrow for one of our material model identification projects reported in Design/Optimization with 50 GHz Material Characterization (D. Dunham, J. Lee, S. McMorrow, Y. Shlepnev, DesignCon2011) [4].

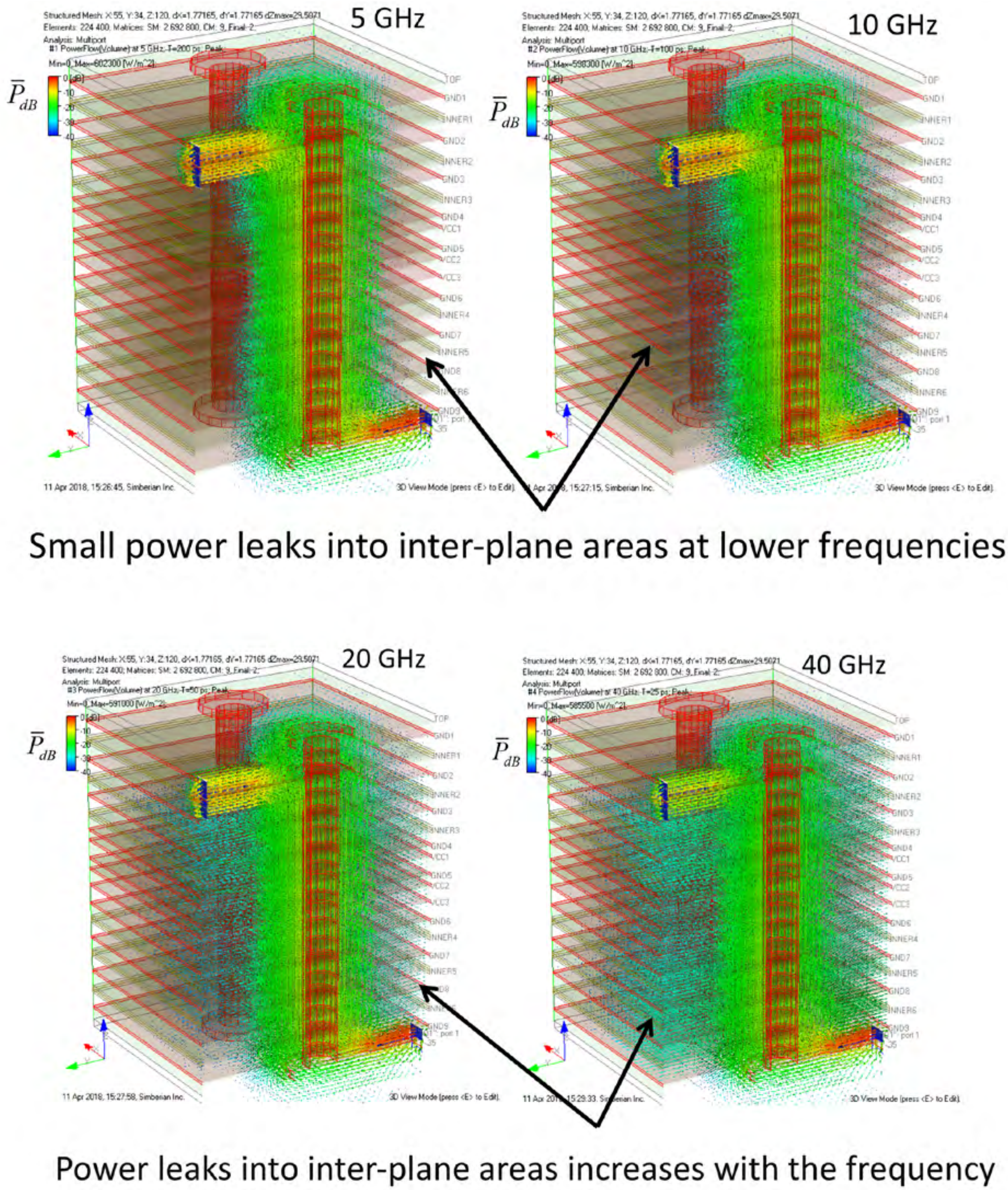


Figure 8: How power propagates at different frequencies.

The bottom line is that the possibility to simulate a link in isolation from the rest of the board or localization is probably the most important condition to design predictable interconnects. Only structures with behavior predictable up to a target frequency should be used to design links for tens of Gbps data rates. The closeness of the stitching vias should be measured relative to the wavelength—the stitching vias can be considered close, as long as the distance does not exceed a quarter of the wavelength at the target frequency.

The number of stitching vias also matter. Without localization, the interconnects cannot be accurately simulated in most of the practical cases. If interconnect behavior cannot be predicted, the outcome is uncertain. It may work, or it may fail! **DESIGN007**

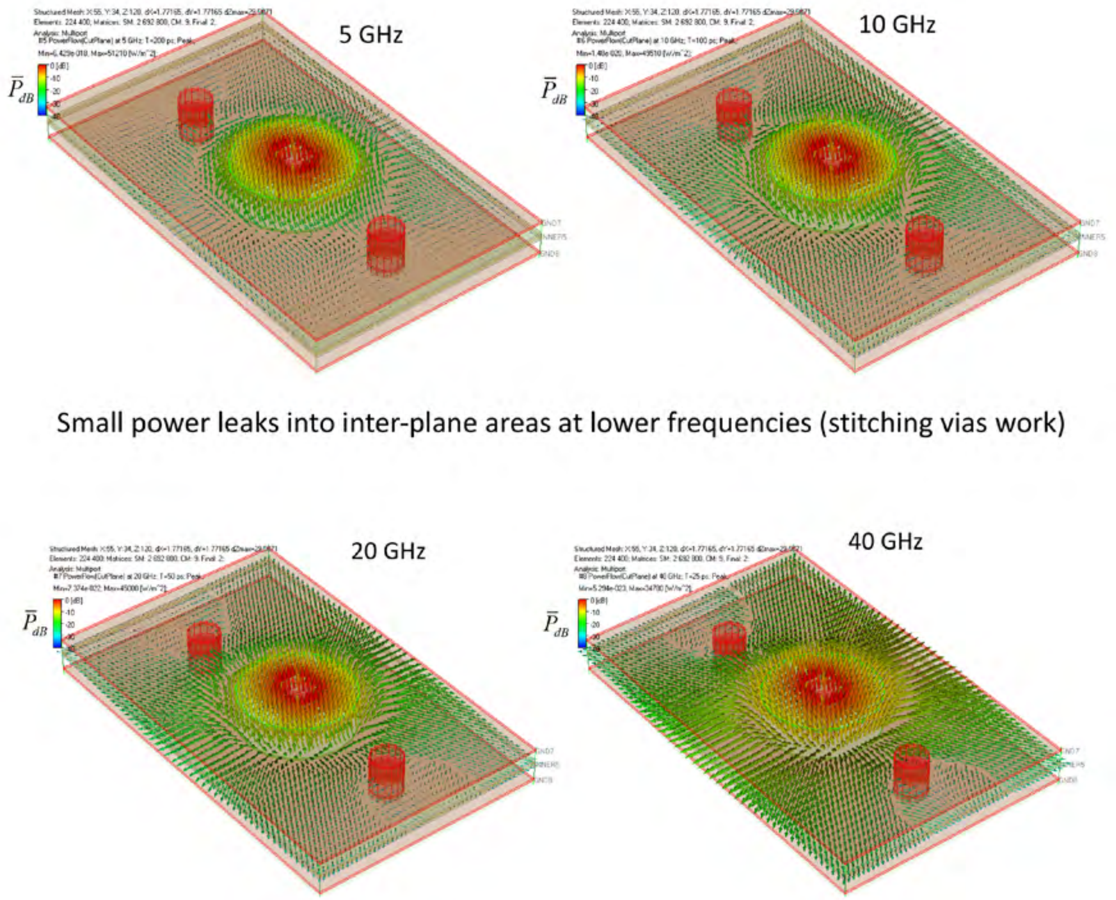


Figure 9: Comparison of stitching vias, both effective and not so effective.

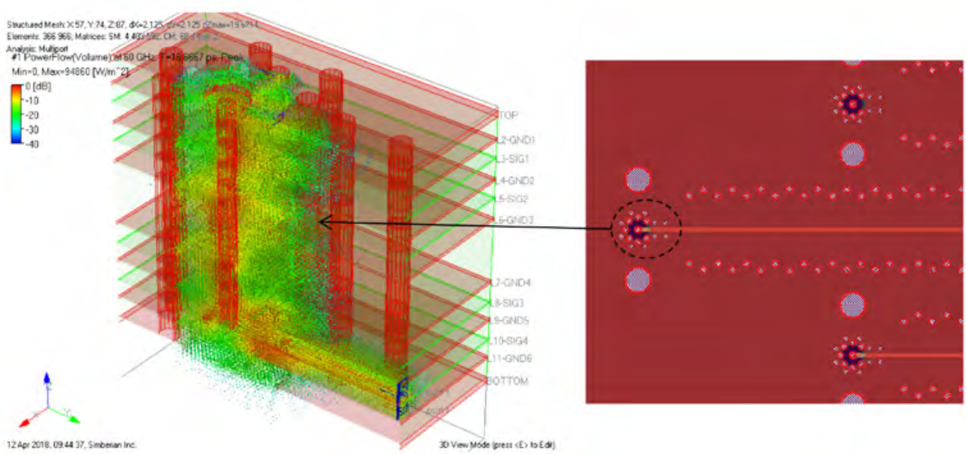


Figure 10: A single via launch localized up to about 60 GHz with 17 stitching vias.

References

1. App notes #2009_05 and #2013_05 at Simberian.com.
2. App note #2013_05 at Simberian.com.
3. Paper available at Simberian.com.
4. Demo video #2018_01 at Simberian.com.

Yuriy Shlepnev is president of Simberian Inc.

Recent Highlights from Design007

1 Mentor Preparing for Next-Gen PCB Designers ▶

In this interview, Paul Musto, director of marketing for Mentor's Board Systems Division, explains the company's initiatives aimed at drawing more students into PCB design. We also discussed the recent movement of electrical engineers into PCB layout, the need for students seeking to become PCB designers, and some of the ways that young people are already beginning to revolutionize this industry.

2 Polar Instruments Releases Updates on Speedstack Tool ▶

Polar Instruments released detailed information documenting recent changes and improvements to their Speedstack tool for rigid PCB layer stackup design and documentation. Polar Instruments claims that Speedstack PCB stackup design tool slashes stack creation time to a fraction of that taken by traditional methods, reducing the chances of miscommunication with PCB manufacturers and the supply chain.

3 Pulsonix Version 10.0 Features 3D PCB Design ▶

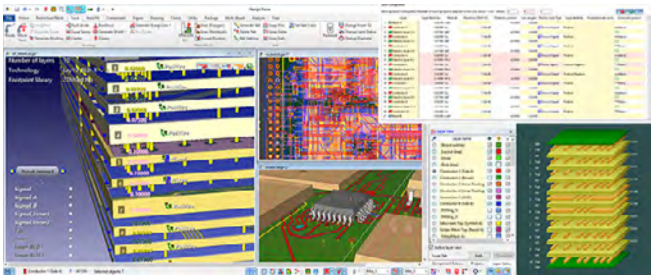
The latest release of Pulsonix expands its product portfolio with intelligent interactive editing within the 3D design environment. By enabling the co-design of the PCB within the 2D PCB and 3D environments, Pulsonix shortens the time to market with a more productive workflow and reduces costly errors.

4 Chuck Bauer Discusses the Future of Packaging ▶

When we decided to cover the future of PCB packaging, we knew we would have to interview Charles Bauer, Ph.D., owner of TechLead Corporation. Chuck recently spoke with Happy Holden, Andy Shaughnessy and Barry Matties about current trends in packaging, the need for product designers and manufacturers to communicate, and why no matter how cool the technology is, cost is still king.

5 Zuken and Polar Instruments Collaborate to Achieve Design Consistency ▶

CR-8000 Design Force users can now exchange pre-layout stackup designs seamlessly with Polar's Speedstack for IC Packaging and PCB design. The stackup can be validated in Zuken's DFM Center before release to manufacturing.



6 The Impact of PCB Dielectric Thickness on Signal Crosstalk ▶


Chang Fei Yee

This article studies the impact of dielectric thickness on crosstalk for transmission lines in single-ended and differential mode on outer (microstrip) and inner (stripline) PCB layers. Crosstalk analysis is performed in 2D simulation and S-parameters are subsequently observed.

7 BGA Fanout Routing Overview ▶

PCB developers are deluged with new challenges caused by increasing density and smaller components. Ball grid arrays (BGAs) create particular challenges during layout, with hundreds of connections in just a few square centimeters. Fortunately, designers now have options for addressing these issues.

8 Occam Prize Competition for Electronic Design Now Accepting Entries ▶

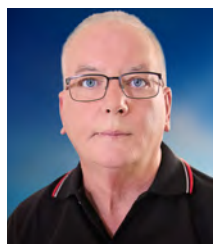
The first annual Occam Prize International Design Competition has begun accepting registrations from circuit designers from around the world. Cash prizes totaling $5,000 will be awarded to top designers in the inaugural year of the planned annual competition.

9 In With the New at Cadence ▶


Bryan LaPointe

For our issue on the disappearing designer, I recently interviewed Cadence's Dan Fernsebner, a veteran EDA guy, and Bryan LaPointe, who represents the younger generation. They discussed the next generation of PCB designers, some of the best ways to draw smart young people into this industry, and why the PCB designers of the future may need to have a college degree just to get an interview.

10 Beyond Design: It's a Material World ▶



Years ago, when clock frequencies were low and signal rise times were slow, selecting a dielectric material for your PCB was not difficult; we all just used FR-4. And we didn't really care about the properties of the materials. However, with today's multi-gigabit designs and their extremely fast rise times and tight margins, precise material selection is crucial to the performance of the product.

Career Opportunities

Pssst!
Are You Looking for Someone?

Place your notice in our Help Wanted section.

For just $500, your 200 word, full-column—or, for $250, your 100 word, half-column—ad will appear in the Help Wanted section of all three of our monthly magazines, reaching circuit board designers, fabricators, assemblers, OEMs and suppliers.

Potential candidates can click on your ad and submit a résumé directly to the email address you've provided. If you wish to continue beyond the first month, the price is the same per month. No contract required. We even include your logo in the ad, which is great branding!

To get your ad into the next issue, contact:
Barb Hockaday at barb@iconnect007.com or +1.916.608.0660 (-7 GMT)

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Career Opportunities

PCB DFM Engineer

Apple products are as alluring on the inside as they are on the outside. Inside our products are some of the world's most challenging consumer PCB assembly and flex designs. Imagine yourself as a select member of the team that brings these assemblies from concept to high-volume manufacturing.

Key Qualifications

- At least 5 years of experience with printed circuits, including hands-on process engineering experience
- Creativity and curiosity about materials science and electronics packaging at all levels
- Deep knowledge of industry specifications, especially IPC and JEDEC specifications
- Understanding of the relationship between manufacturing processes and printed circuit defect conditions, especially latent defects
- Ability to travel overseas for up to 25 percent of your time

Primary Responsibilities

- Maintenance of PCB design guidelines for all Apple products as well as the technology road map and acceptability specifications
- Establishment and maintenance of the supplier site/material/technology qualification matrix
- Direct responsibility for all PCB-related quality issues and excursions
- Providing mentorship to product designers on available PCB technologies and materials

Education

BS or higher in Materials Science or Mechanical, Chemical, or Electrical Engineering

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Senior Manager, Flex/PCBA DFM

On this team, you'll be responsible for new product development, sustaining products and failure analysis while leading and mentoring design, process, and quality engineers and managers. You'll collaborate cross-functionally with Product Design, Electrical Engineering, strategic suppliers, and contract manufacturers to ensure the manufacturability of Apple products and maintain Apple's high standards for quality.

Key Qualifications

- At least 10 years of experience, with 5+ years of experience as a senior manager or director
- Experience managing other managers is preferable
- Experience in design and manufacturing, preferably in the electronics fabrication and assembly industry
- Deep technical knowledge complemented by a good sense of how engineering decisions impact business concerns
- Excellent communication skills, from extemporaneous discussion to synthesis of detailed technical reports and distillation to executive-level presentation

Primary Responsibilities

- Development of several design engineers and first-level managers
- Primary escalation point to resolve blocking issues related to design release, design spec compliance, or production process problems
- Engagement with vendor senior management to set expectations and to communicate feedback
- Highlighting all project risks to executive management and identifying, evaluating, and recommending the best path to resolution

Education

BS or higher in Materials Science or Mechanical, Chemical, Electrical, or Industrial Engineering

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Career Opportunities

American Standard Circuits
Creative Innovations In Flex, Digital & Microwave Circuits

CAM Operator

American Standard Circuits is seeking a CAM Operator for its Phoenix, Ariz., office. Qualified applicants will need experience in using Valor/Genesis (GenFlex) CAD/CAM software with printed circuit board process knowledge to edit electronic data in support of customer and production needs.

Job Requirements:

- At least 5 years' experience in PCB manufacturing
- Process DRC / DFMs and distinguish valid design and manufacturing concerns.
- Modify customer supplied data files and interface with customers and engineers
- Responsible for releasing manufacturing tooling to the production floor
- Prepare NC tooling for machine drilling, routing, imaging, soldermask, silkscreen
- Netlist test, optical inspection
- Work with Production on needed changes
- Suggestions on continual improvements for engineering and processing.
- Be able to read write and communicate in English
- Must understand prints specifications
- Must be US Citizen or permanent resident (ITAR)
- High School Graduate or equivalent

Join our Team!

Founded in 1988, American Standard Circuits is a leading manufacturer of advanced circuit board solutions worldwide. Our ongoing commitment to leading-edge higher-level interconnect technology, cost-effective manufacturing and unparalleled customer service has put us at the forefront of advanced technology circuit board fabrication.

We manufacture quality rigid, metal-backed and flex printed circuit boards on various types of substrates for many applications.

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ELECTROLUBE
THE SOLUTIONS PEOPLE

Sales Development Manager

Electrolube has a new opportunity for a sales development manager covering the Midwest United States. This is an exciting role involving all aspects of sales development and account management for the Electrolube brand.

The successful candidate will have relevant experience within the electro-chemicals industry and a strong commercial background. This position will report directly to the U.S. general manager.

Applicants should apply in writing and submit a CV by clicking the button below.

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Career Opportunities

Ucamco
Former Barco ETS

International Field Service Engineer located in ITALY

The successful candidate will:

- Install and service our plotters and direct imaging machines at customer sites Europe-wide
- Carry out maintenance in the field
- Frequent travel: 4 to 5 days a week, 3 to 4 weeks a month
- Assist product manager

We are looking for a team player who is:

- Strongly customer-oriented and experienced in on-site support
- Accustomed to travel, and willing to travel frequently
- Motivated, independent and enterprising
- Technically-minded with training/background in electromechanics/electronics
- Experienced with software (setup, configuration, and usage of Windows-based CAM front-end software and Linux-based RIP software)
- Fluent in Italian and English (German and/or French is a plus)
- An analytical thinker
- Capable of problem solving

The right candidate will be a valued member of a friendly, team-oriented, growing international company that is a leader in its field, dedicated to excellence in all it does. Dynamic and fun, the company offers a great working atmosphere, and this new position is forward-looking and open, with plenty of opportunities for enterprising individuals whose results could be rewarded with prospects for progression in technical development.

Apply to Anja Ingels after clicking below.

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MacDermid Enthone
ELECTRONICS SOLUTIONS

Product Group Field Manager Waterbury, CT

Do you have what it takes? MacDermid Enthone Electronics Solutions is a leading supplier of specialty chemicals, providing application-specific solutions and unsurpassed technical support.

The position of the Product Group Field Manager will be responsible for creating and driving a strategic plan for the regional product line, including the following:

- Possess a thorough understanding of the overall PCB business, and specifics in wet processing areas
- Play an integral part in developing a commercial and technical customer strategy
- Create and deliver customer facing presentations
- Provide technical training for field staff
- Create and execute a product rationalization program
- Develop new product roll-out packages

Hiring Profile

- Bachelor's degree or 5 years' job-related experience
- Strong understanding of chemistry and chemical interaction within PCB manufacturing
- Excellent written and oral communication skills
- Strong track record of navigating technically through complex organizations
- Willingness to travel

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Career Opportunities

Role: Vice President Gardien Taiwan
TAOYUAN COUNTY, TAIWAN

Gardien Taiwan is a service provider of circuit board (PCB) quality solutions, including electrical testing, AOI optical inspection, engineering (CAM), fixture making, repair and rework. Gardien Taiwan operates service centers in Taoyuan and employs about 100 employees and is currently seeking a vice president to manage and oversee the entity.

Candidate Profile:
- Proficiency in Chinese and English (written and spoken)
- Excellent communication and organization skills
- Experience in change management
- PCB background appreciated, but not mandatory
- Management experience in internationally operating companies
- Savvy in standard office software (Word, Excel and Power Point)

If this sounds like you, please click here to send us an email with your attached CV.

About Gardien Group - Gardien is the world's largest international provider of independent testing and QA solutions to the PCB industry with a global footprint across 24 service centres in five countries and we cater to a whole range of customers, from small family owned PCB shops to large international fabricators. Gardien's quality solutions and process standards are trusted by leading high-tech manufacturers and important industries including aerospace, defense, and medical technology.

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Zentech Manufacturing: Hiring Multiple Positions

Are you looking to excel in your career and grow professionally in a thriving business? Zentech, established in Baltimore, Maryland, in 1998, has proven to be one of the premier electronics contract manufacturers in the U.S.

Zentech is rapidly growing and seeking to add Manufacturing Engineers, Program Managers, and Sr. Test Technicians. Offering an excellent benefit package including health/dental insurance and an employer-matched 401k program, Zentech holds the ultimate set of certifications relating to the manufacture of mission-critical printed circuit card assemblies, including: ISO:9001, AS9100, DD2345, and ISO 13485.

Zentech is an IPC Trusted Source QML and ITAR registered. U.S. citizens only need apply.

Please email resume below.

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Career Opportunities

Manncorp™

Sales Associate - Mexico

Manncorp, a leader in the electronics assembly industry for over 50 years, is looking for an additional sales associate to cover all of Mexico and to be part of a collaborative, tight-knit team. We offer on-the-job training and years of industry experience in order to set up our sales associate for success. This individual will be a key part of the sales cycle and be heavily involved with the customers and the sales manager.

Job responsibilities:
- Acquire new customers by reaching out to leads
- Ascertain customer's purchase needs
- Assist in resolving customer complaints and queries
- Meet deadlines and financial goal minimums
- Make recommendations to the customer
- Maintain documentation of customer communication, contact and account updates

Job requirements:
- Located in Mexico
- Knowledge of pick-and-place and electronics assembly in general
- 3+ years of sales experience
- Customer service skills
- Positive attitude
- Self-starter with ability to work with little supervision
- Phone, email, and chat communication skills
- Persuasion, negotiation, and closing skills

We offer:
- Competitive salary
- Generous commission structure

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Use your knowledge of PCB assembly and process engineering to promote Mentor's Valor digital manufacturing solutions via industry articles, industry events, blogs, and relevant social networking sites. The Valor division is seeking a seasoned professional who has operated within the PCB manufacturing industry to be a leading voice in advocating our solutions through a variety of marketing platforms including digital, media, trade show, conferences, and forums.

The successful candidate is expected to have solid experience within the PCB assembly industry and the ability to represent the Valor solutions with authority and credibility. A solid background in PCB Process Engineering or Quality management to leverage in day-to-day activities is preferred. The candidate should be a good "storyteller" who can develop relatable content in an interesting and compelling manner, and who is comfortable in presenting in public as well as engaging in on-line forums; should have solid experience with professional social platforms such as LinkedIn.

Success will be measured quantitatively in terms of number of interactions, increase in digital engagements, measurement of sentiment, article placements, presentations delivered. Qualitatively, success will be measured by feedback from colleagues and relevant industry players.

This is an excellent opportunity for an industry professional who has a passion for marketing and public presentation.

Location flexible: Israel, UK or US

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Career Opportunities

BLACKFOX
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This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

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Mentor®
A Siemens Business

Technology Communications Writer/Content Manager
Board Systems Division

Mentor Graphics, a Siemens business, is a global technology leader in EDA software, enabling global companies to develop new and highly innovative electronic products in the increasingly complex world of chip, board, and system design.

Job Duties:

The Mentor printed circuit board (PCB) technical writer/content manager will:

- Write and produce high-quality content for various properties (blogs, product collateral, technical white papers, case studies, industry publications, etc.)
- Gather research and data, interview subject matter experts, and transform complex information into clear, concise marketing communications
- Manage projects across multiple PCB product teams (high-speed design/analysis, advanced packaging, board design) within a deadline-driven environment

Job Qualifications:

The ideal candidate should possess:

- Strong writing and editing skills with experience in PCB design technologies
- Desktop publishing skills (InDesign) using project templates and knowledge of online publications and social media
- A technical background (B.S. in electrical engineering or computer science preferred; this role works closely with the PCB division's technical marketing engineers and managers
- Solid project planning and management skills; appreciation for adhering to deadlines; creativity for turning technical information into compelling content; teamwork and strong interpersonal communications skills; ability to be a self-starter

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Events Calendar

2018 Silicon Valley Hardware Symposium: Robotics and Automation, Are You Ready?
September 20, 2018
Mountain View, California, USA

electronica India & productronica India
September 26–28, 2018
Bengaluru, India

electronicAsia 2018
October 13–16, 2018
Hong Kong

SMTA International
October 16–17, 2018
Rosemont, Illinois, USA

TPCA Show 2018
October 24–26, 2018
Taipei, Taiwan

electronica 2018
November 13–16, 2018
Munich, Germany

IDTtechEx Show
November 14–15, 2018
Santa Clara, California, USA

IPC IMPACT Europe 2018
November 28–29, 2018
Brussels, Belgium

HKPCA/IPC International Printed Circuit & South China Fair
December 5–7, 2018
Shenzhen, China

48th NEPCON JAPAN
January 16–18, 2019
Tokyo Big Sight, Japan

IPC APEX EXPO Conference and Exhibition
January 26–31, 2019
San Diego, California, USA

DesignCon 2019
January 29–31, 2019
Santa Clara, California, USA

Additional Event Calendars

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COVER: **SHELLY STEIN**

COVER IMAGE: **ADOBE STOCK © phonlamaiphoto**

DESIGN007 MAGAZINE

DESIGN007 MAGAZINE®
is published by BR Publishing, Inc.,
942 Windemere Dr. NW, Salem, OR 97304

September 2018, Volume 7, Number 9
DESIGN007 MAGAZINE is published monthly,
by BR Publishing, Inc.

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