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Crosstalk Measurement, Extraction and Validation in 10Gbps Serial Systems

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Abstract

Connectors are a significant source of crosstalk noise in a system, which could increase jitter in the resulting eye pattern. Since crosstalk jitter is uncorrelated from the link data pattern, it is hard to remove through equalization techniques. This paper provides a process to extract accurate coupled models from connectors. It also describes how modeling was used to predict crosstalk noise in a 10Gbps channel and shows how a small percentage of connector crosstalk can have a significant impact on the over all signal distortion, if the connector pin assignment is done randomly.

Author(s) Biography

Pravin Patel pravinp@us.ibm.com Pravin Patel is a Senior Engineer and Technical Leader working for IBM xSeries Server Development. He is involved in defining product architecture, creating product strategies, and time and frequency domain SI analysis/simulation of Intel base server products. His current activities include the design and analysis of Serdes interfaces for BladeCenter product. He performs modeling, simulation and measurements of the high speed serial link Channels. The other areas of his responsibilities include design and development of models for line cards, backplanes, traces, via and performing simulations for system level voltage and timing budgets and jitter characterization. He is an active member of T11.2 and IEEE802.3 channel model standard committee from IBM. He received a B.S. degree in electrical engineering from the New Jersey Institute of Technology in 1989. Pravin has received 12 U.S. Patents, 3 IBM Invention Plateau Achievement Awards, 7th IBM Authors Recognition Awards, one IBM Outstanding Technical Achievement Awards, and One IBM Corporate Award. IBM. He has authored or co-authored 25 technical papers in IEEE EPEP, IEEE ECTC and DesignCon conferences.

Rubina is an R&D Engineer/Scientist with IBM's x Series Signal Integrity group. She graduated from NC State University with a MS in Electrical Engineering in 2003 with a focus on the fields of Signal Integrity and High Speed Digital design. Her areas of expertise include analysis, modeling, simulation and design of High Speed Interconnects (cables, connectors) and PCBs as well as High Speed measurement techniques in the Time Domain (TDR) and Frequency Domain (VNA). Her current activities also include High Speed Interconnect standards validation at physical layer level including PCI express, Infiniband, Cx4, Ethernet, SAS, SATA.

Moises Cases has thirty-eight years of progressive experience in very-large scale integration chip and package designs, in system level electrical and package designs, and in complex project and people management. Presently, he is a Distinguished Engineer at IBM System and Technology Group and the team leader for system electrical design and integration of modular and blade servers. Responsible for signal and power distribution integrity, and system level timing for complex multiple board system designs. He obtained Master of Science in Computer Engineering from Syracuse University, NY in 1979, Master of Science in Electronic Engineering from New York University, NY in 1973, and a Bachelor of Science in Electrical Engineering from City College of New York, NY in 1969. He is a senior member of IEEE and a member of Tau Beta Pi and Eta

Kappa Nu honor societies. Mr. Cases has received the Hispanic in Technology Corporate Award from the Society of Hispanic Professional Engineers in 2006, the Corporate Business/ Community Representative of the Year Award from Austin Independent School District in 2007, and the Albert V. Baez Award from HENAAC in 2007. Mr. Cases has received 43 U.S. Patents and has published 88 refereed technical papers on numerous proceedings, journals and transactions.

Gourgen Oganessyan is Strategic Marketing Manager, Quellan Inc. Gourgen works on developing applications and technology strategies for Quellan's lane extender and crosstalk cancellation products. Previously he was Senior Electrical Engineer with Molex, Inc where his work on signal integrity aspects and design of high-speed connector solutions included modeling and high-speed characterization of interconnects, as well as design of reference backplane architectures and participation in OIF and IEEE 802.3 industry forums. He has a Master's degree in theoretical physics from Yerevan State University, Armenia, and a Master's degree in applied optics from University of North Carolina – Charlotte.

David Dunham was named electrical engineering manager for Molex Incorporated in 2000, responsible for managing signal integrity engineers for next generation connector development. Products he helped developed include I/O solutions; board-to-board, backplane and edge-card connectors; and plated plastic technology. Dunham began his career at Molex in 1997 as senior electrical engineer, which he focused on developing signal integrity capabilities within Molex's Data Communications division, including analytical/empirical modeling and measurement methodologies. Previous to Molex, Dunham worked 12 years for Augat/LRC, where he developed cable TV coaxial connectors. Throughout his career, he also held various positions in Avionics as well as the field of Test and Measurement. Dunham received several connector patents related to plated plastic technology and high speed backplane interconnects. Additionally, he has written several white papers for industry shows including DesignCon and the International Microwave Symposium. Dunham received a Bachelor of Science degree in electrical engineering from the University of New Mexico in 1970.

Introduction

Design choices in a Blade Center backplane system are based on simulation models. Accurate simulation models are critical to making good design trade-offs, especially in 10Gbps serial systems. Models for several components provided by external suppliers may have limited accuracy. As serial link speeds have increased, minimizing crosstalk has become a major Signal Integrity challenge. In a 10Gbps system connector crosstalk can be a significant jitter contributor if the connector pin assignment is done randomly. However, the effect on the overall system can be reduced by following certain design guidelines.

This paper provides a process to extract accurate connector crosstalk models. The Molex SEARAY™ [2] connector was evaluated to determine its suitability in the high speed backplane system. As shown in Figure 1 below, the BladeCenter interconnects are card to card high speed channels, which enable system compatibility between shared devices. The backplane in a blade system can be defined as a flexible interface to attach shared devices such as processor blades, switches, management modules, etc.

Two different techniques were used to measure the near end and far end crosstalk contribution of the connector. The correlation of crosstalk measurement techniques was done using a VNA in the frequency domain and a TDR in the time domain. This procedure validated the connector crosstalk measurements which allows for evaluating the impact of crosstalk with a high degree of confidence. In addition to characterizing the crosstalk contribution of the connector by itself, a channel simulation using the StatEye tool was performed using the validated coupled models that were created by exporting measured frequency domain data into the touchstone format.

System channel Overview

The System Backplane Channel, as sketched in Figure 1 provides electrical interconnections between all of the chassis components including the Processor Blades, Switch Modules, Management Modules (MM) and Media device. The backplane accepts up to 14 blade slots, 4 switch slots, 1 media bay, 2 management modules and 4 power modules all of which support hot-swap capability. In order to provide high availability and maximize up-time for the customer, many of the interconnects go through multiple connectors and 15 in. to 30 in. channel lengths. [1] The Molex SEARAY™ connector is the "con.1" in the figure below and is a possible source of crosstalk noise.
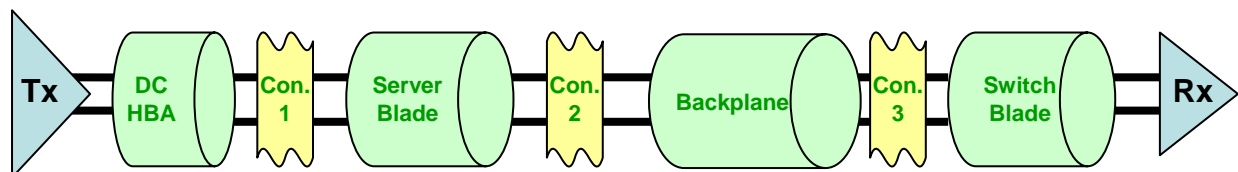

Figure 1: System Channel Representation

Frequency and Time Domain Crosstalk measurements – Overview

Crosstalk can be measured either in the time domain using a Time Domain Reflectometer (TDR) or the frequency domain using a Vector Network Analyzer (VNA). It is theoretically possible to convert data from one domain into another using Fourier transforms. Tools like Agilent PLTS™ (Physical Layer Test System) and Tektronix Iconnect ® allow conversion of measurement data between two Domains. Most channel simulation tools, including StatEye, require models extracted into the Touchstone format containing S parameter information for the System in Test including the Insertion Loss and Crosstalk. It is possible to extract such models from either the VNA or the TDR using the above mentioned tools, with minimal some effort. This paper describes two methods for measuring crosstalk, their correlation through domain transformations, as well as model extraction.

Crosstalk Measurement Setup

The Molex SEARAY™ is a high density, high performance board to board mezzanine connector. It is designed for high speed differential pair performance up to 10Gbps and is intended for low profile applications. The signal integrity evaluation used a test fixture provided by Molex, which contained a 7mm Molex SEARAY connector terminated onto a test card. All traces on the test cards were uncoupled 3.5" low-loss stripline.
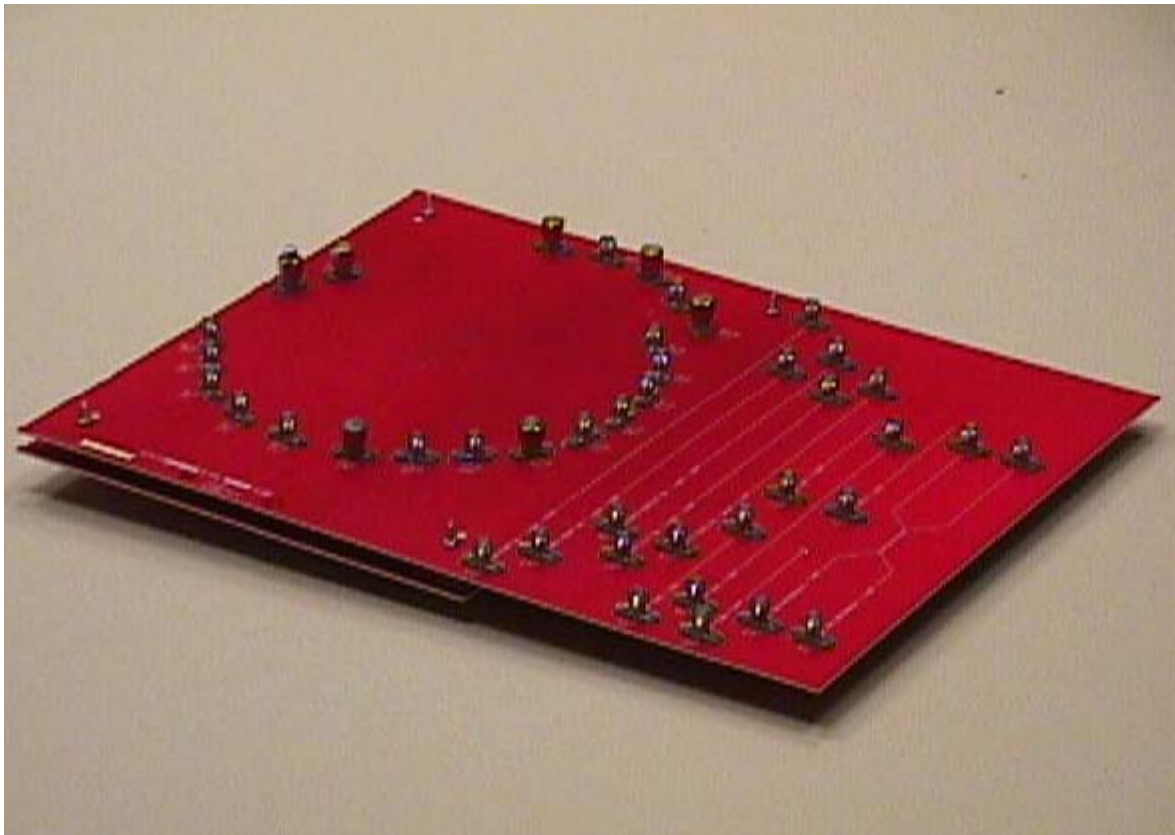

Figure 2: System Channel Representation

All measurements were done on a vertical staggered pair configuration in the connector. The vertical staggered pair configuration was adopted as the configuration of choice in the final connector layout. This configuration makes it easy to run board wiring to obtain skew matched pairs.
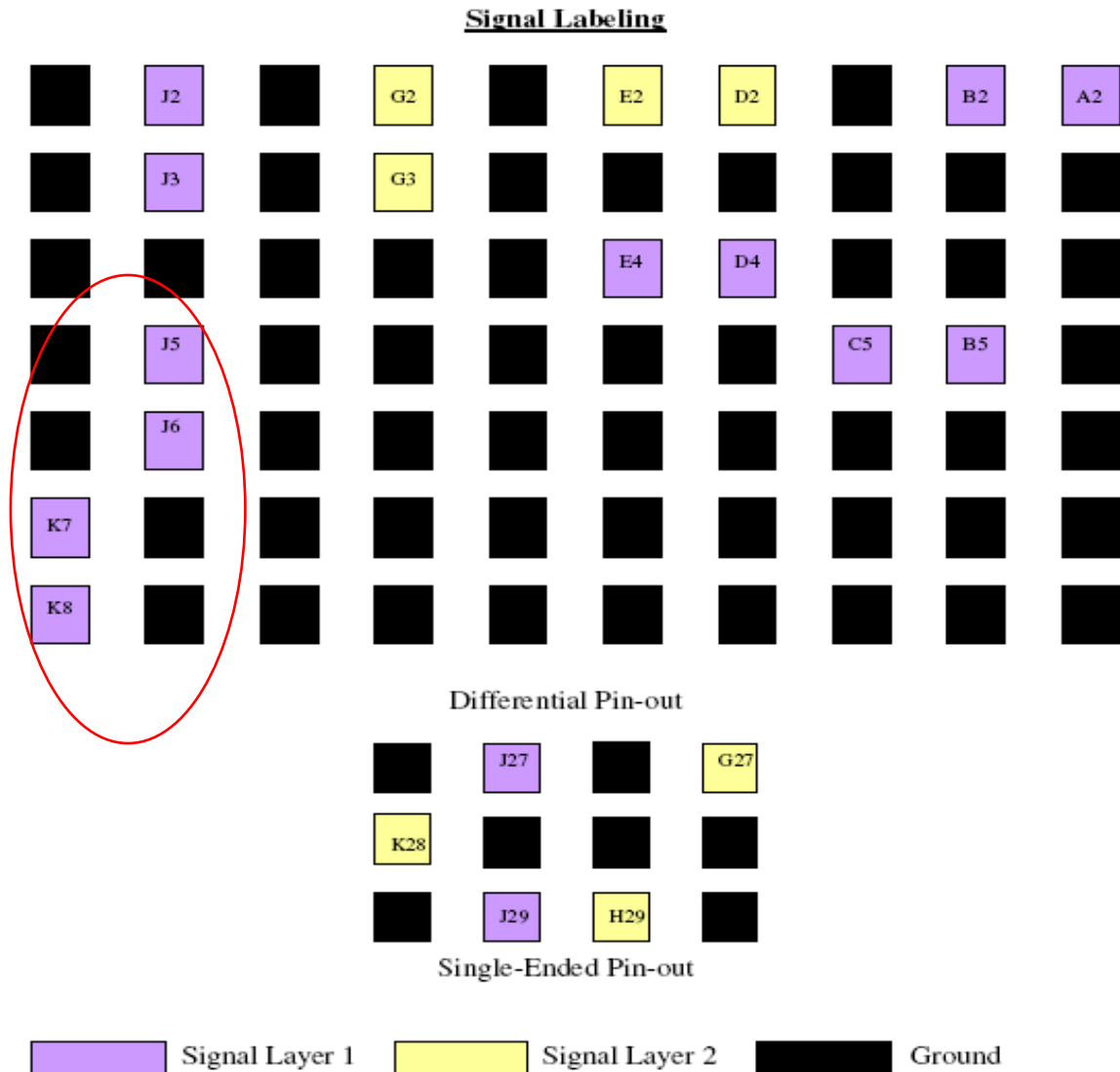

Figure 3: System Channel Representation

Figure 4 shows the TDR and VNA setup used to measure the Near End Cross Talk (NEXT) and the Far End Cross Talk (FEXT) that was coupled from the closest neighboring differential pair within the connector. All other ports, including all other adjacent pairs were terminated into 50 Ohms to suppress reflections from the near or far end. The two methods for measuring crosstalk are explored and compared below.
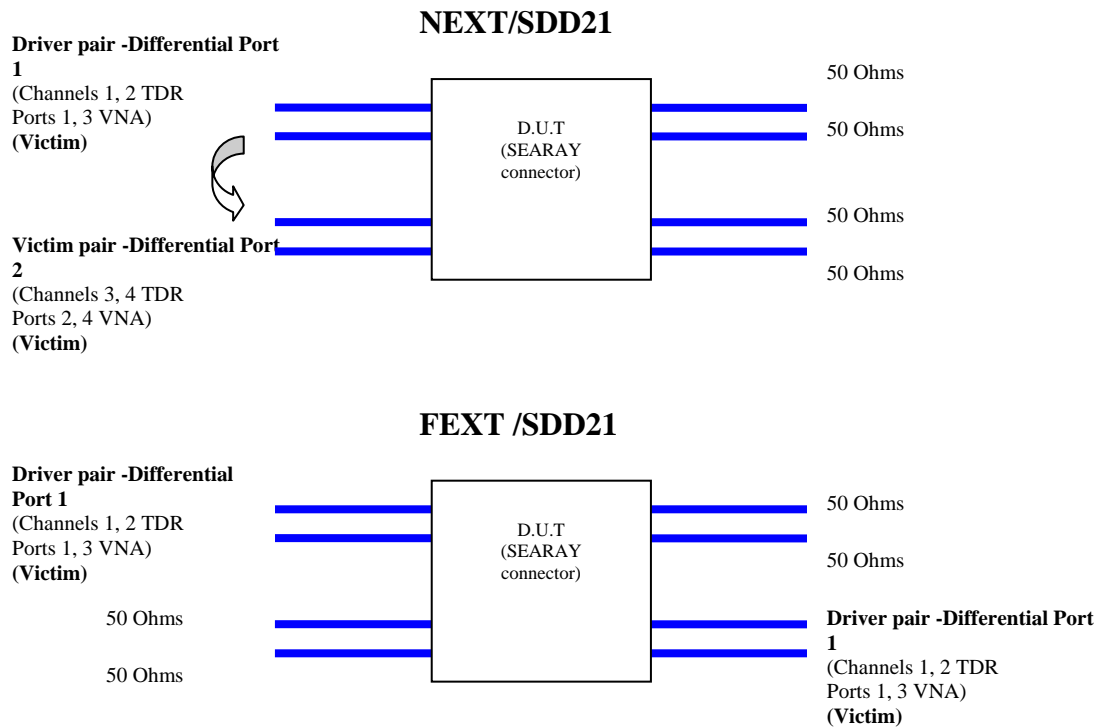
NEXT/SDD21

Driver pair -Differential Port 1
(Channels 1, 2 TDR Ports 1, 3 VNA)
(Victim)

50 Ohms

50 Ohms

D.U.T
(SEARAY
connector)

50 Ohms

Victim pair -Differential Port 2
(Channels 3, 4 TDR Ports 2, 4 VNA)
(Victim)

50 Ohms

FEXT /SDD21

Driver pair -Differential Port 1
(Channels 1, 2 TDR Ports 1, 3 VNA)
(Victim)

50 Ohms

50 Ohms

D.U.T
(SEARAY
connector)

50 Ohms

50 Ohms

Driver pair -Differential Port 1
(Channels 1, 2 TDR Ports 1, 3 VNA)
(Victim)

Figure 4: Crosstalk Measurement Configuration

Time Domain Crosstalk measurements

In the first measurement method explored, the crosstalk contribution of the nearest pair in the vertical staggered configuration was measured in the time domain. A Tektronix CSA8200 TDR (Time Domain Reflectometer) [3] with 80E04 heads was used for the measurements. The input excitation signal had a rise time of 35ps (20-80%) unfiltered and an amplitude of about 480mV. The 35ps rise time allows characterization of the connector for 10Gbs applications. The differential crosstalk was measured in millivolts from baseline to peak.

Figures 5, 6 are TDR plots of the measured NEXT and FEXT in the connector. The shape and location of the crosstalk pulse as seen in the time domain, gives information about the origin of the crosstalk within DUT. Also seen in the figures is the impedance profile of the connector showing the via capacitive dips and other impedance mismatches resulting from how the connector was soldered to the board.   The NEXT and FEXT originate from the connector and via region as shown in the impedance profile. As expected, the width of the NEXT pulse is twice the time delay of the connector. The amplitude of the FEXT pulse is almost similar to that of the NEXT pulse because of the relatively short connector length. The FEXT appears as a pulse, which is a derivative of the signal edge i.e. the width of the pulse is the rise time of the signal edge through the DUT.
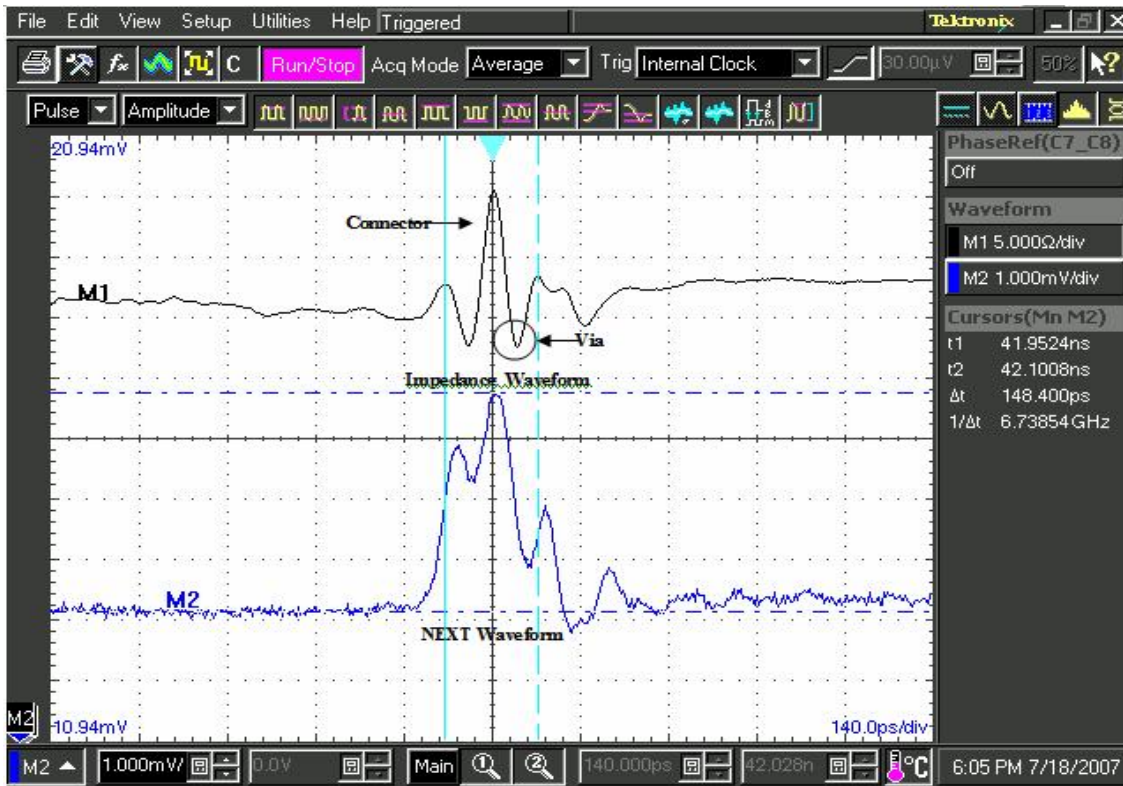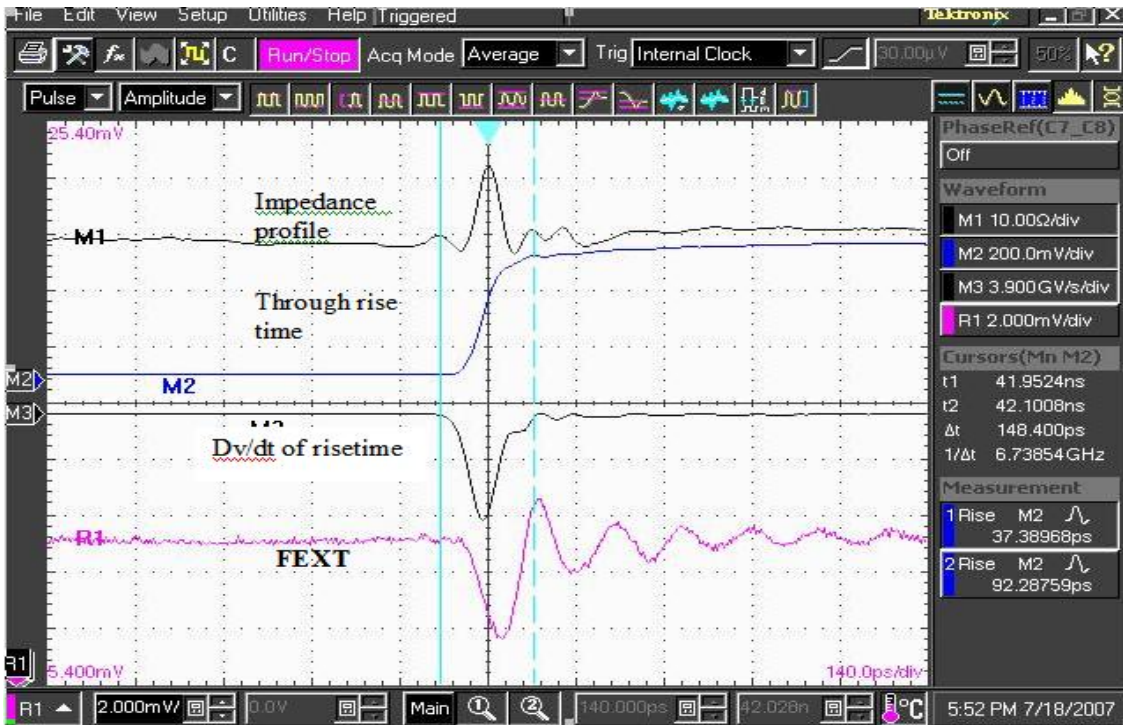
Figure 5: NEXT waveform from TDR

Figure 6:FEXT waveform from TDR

NEXT (mV, %)	(3.5, 0.74)
FEXT (mV, %)	(2.8, 0.6)

Table 1

Table 1 shows measured crosstalk in millivolts along with the crosstalk calculated as a percentage of the launched input voltage (480mv).

Frequency Domain Crosstalk Measurements

In the second measurement method explored, differential S parameter crosstalk measurements (both near end and far end) were taken using an Agilent 8720ES Vector Network Analyzer with an ATN Microwave 4112A four port test set. Agilent's PLTS (Physical Layer Test System) [4] measurement and analysis software was used to collect the measurement data. The bandwidth used for these measurements was from 10MHz to 20 GHz.

Viewing the crosstalk in the frequency domain allows us to measure crosstalk energy on individual frequencies of interest e.g. the data rate and significant harmonics. See figures 6 and 7.
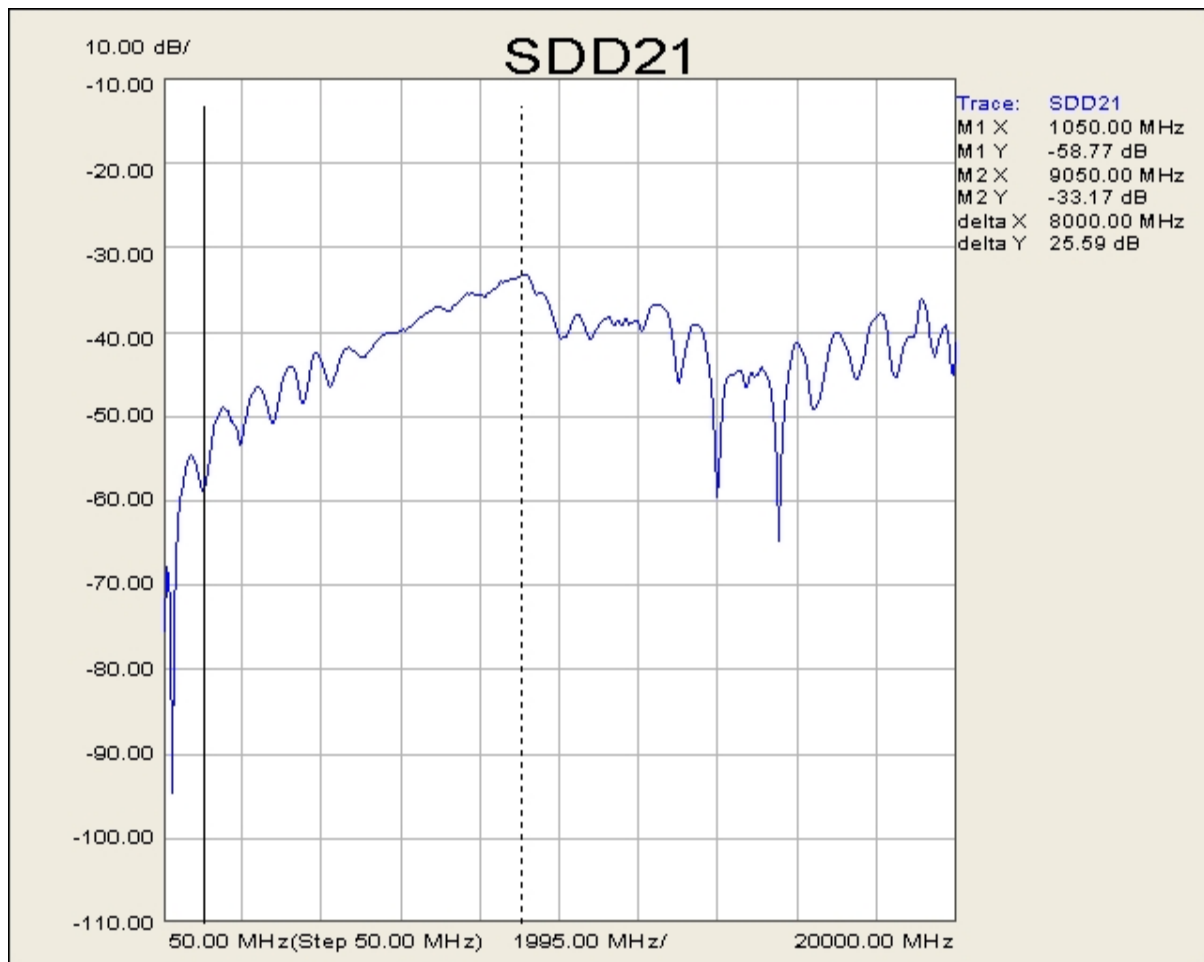

Figure 6: NEXT plot from VNA

Figure 7: FEXT plot from VNA

Frequency (GHz)	4.25 GHz	5GHz	10GHz
NEXT (dB, %)	-39.98, 1.0	-42.94, 0.7	-40.27, 0.97
FEXT (dB, %)	-32.7, 2.32	-42.84, 0.7	-50.22, 0.3

Table 2

Table 2 shows measured crosstalk in dB along with the crosstalk calculated as a percentage. Crosstalk in dB can be converted into percentage units by using the formula Antilog (crosstalk in dB/20).

Even though both time domain crosstalk and frequency domain crosstalk can be expressed in percentage units, the two approaches are different and should not be directly compared. This is because time domain crosstalk is measured at a particular launch rise time unlike the frequency domain crosstalk which is swept across a frequency range. Also, crosstalk measured in the time domain has the effect of the test cables built in, while crosstalk measured in the frequency domain has the effect of the test cables calibrated out from the measurement.

The two methods discussed above can be used to characterize and compare the crosstalk performance of various pin pair configurations. Crosstalk performance is one of the factors in choosing the final pin-out configuration of the connector to be used in the system. The vertical staggered pair configuration was adopted as the configuration of choice in the final connector layout in the Blade Channel. This configuration makes it easy to run board wiring to obtain skew matched pairs.

Correlation of Frequency and Time Domain Measurements

Frequency domain data can be converted into time domain data and vice versa using the tools -Agilent PLTS and Tektronix IConnect [3] and by following certain guidelines. This allows for demonstrating correlation of measured data between the two domains with reasonable accuracy. This also proves that measurements can be ideally limited to one domain/ instrument if certain procedures are followed to interpret the measured data correctly.

Time Domain Crosstalk measurement using the VNA
The measured S parameter data was transformed into Time domain (or T parameters) using the Agilent PLTS tool, which uses this technique. A 'nominal time domain window' option was used in extracting the T parameters in PLTS to ensure that the time domain response is computed with an excitation signal with a rise time similar to that of the TDR measurements (35ps). The T parameters (TDD21) obtained using the reverse Fourier transform in the tool were then overlaid on the TDR measurements after running the data through a series of steps.

- First, a normalization factor was used to compensate for different input voltage amplitudes. The PLTS uses an input amplitude of 400mV while the TDR uses a 500mV launch.

- A second adjustment was to gate out the time delay introduced by the test cables in the TDR measurement.
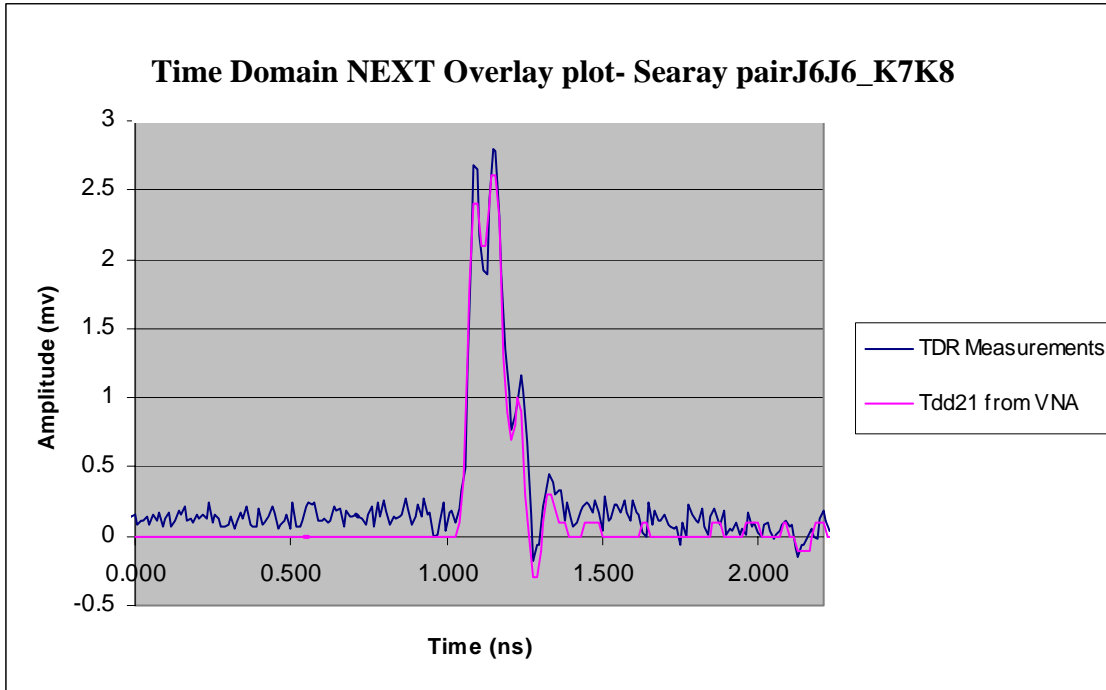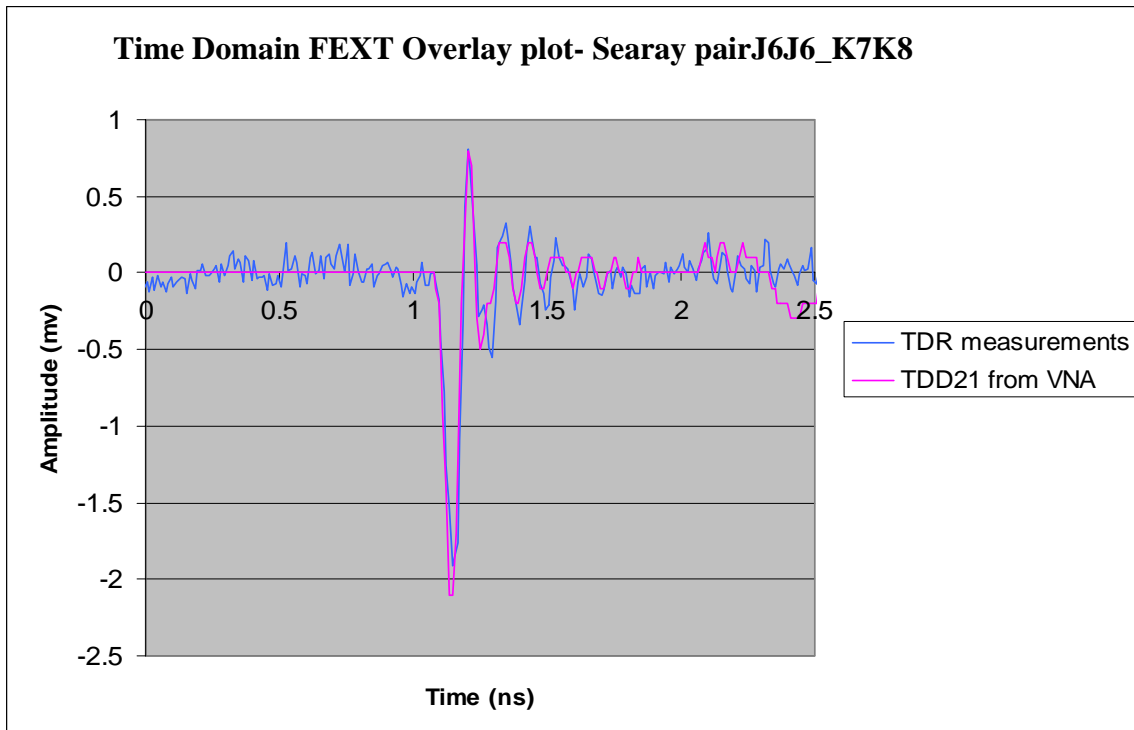
Figure 8: Time Domain correlation - NEXT

Figure 9: Time Domain correlation – FEXT

The plots show an excellent correlation between the two overlaid waveforms.
As seen in figures 8 and 9, the transition times of the two waveforms match perfectly.
The amplitudes differ by 0.1mv for NEXT and 0.2 mV for FEXT. The TDR waveforms

have a baseline noise resulting from the lower dynamic range of the TDR heads used in our setup. As seen from the plots, simply subtracting the baseline noise from the waveform will result in an excellent correlation between the two approaches. Using TDR heads with a better dynamic range suitable for measuring crosstalk in the 35-50dB range will improve the measurements further.

Frequency Domain Crosstalk measurement using the TDR
To transform the time domain into frequency domain S parameters, the IConnect tool was used to capture the TDD21 waveform (TDR) The Tektronix CSA 8000 was set up with a Record Length of 4000 and tbase = 3ns/division. Both the TDR and TDT head were deskewed, the open reflection was measured at the end of the SMA test cables and stored via the IConnect software. A terminated TDR measurement was taken with the test cables connected to the DUT. Channel noise was subtracted from this waveform. Near End Crosstalk was then calculated in IConnect with the open reflection measurement used as the reference and the terminated reflection measurement with the channel noise subtracted, as the DUT.

The plots (Figures 10 and 11) show a reasonable correlation. Again, using TDR heads with a better dynamic range will improve the correlation further.
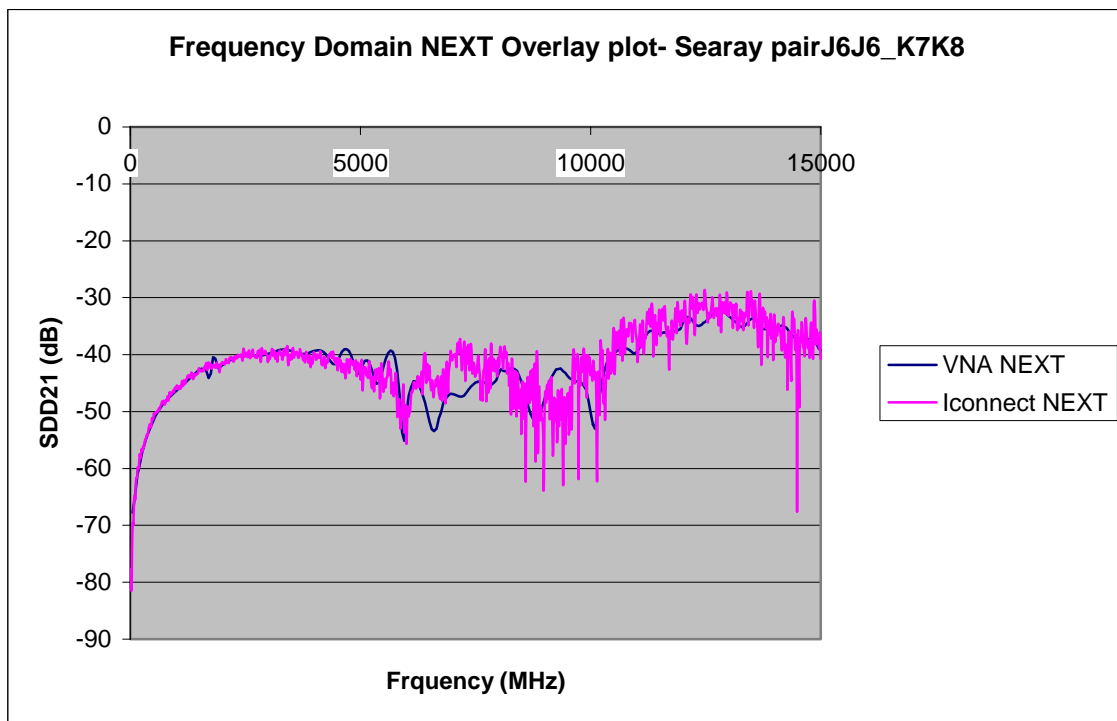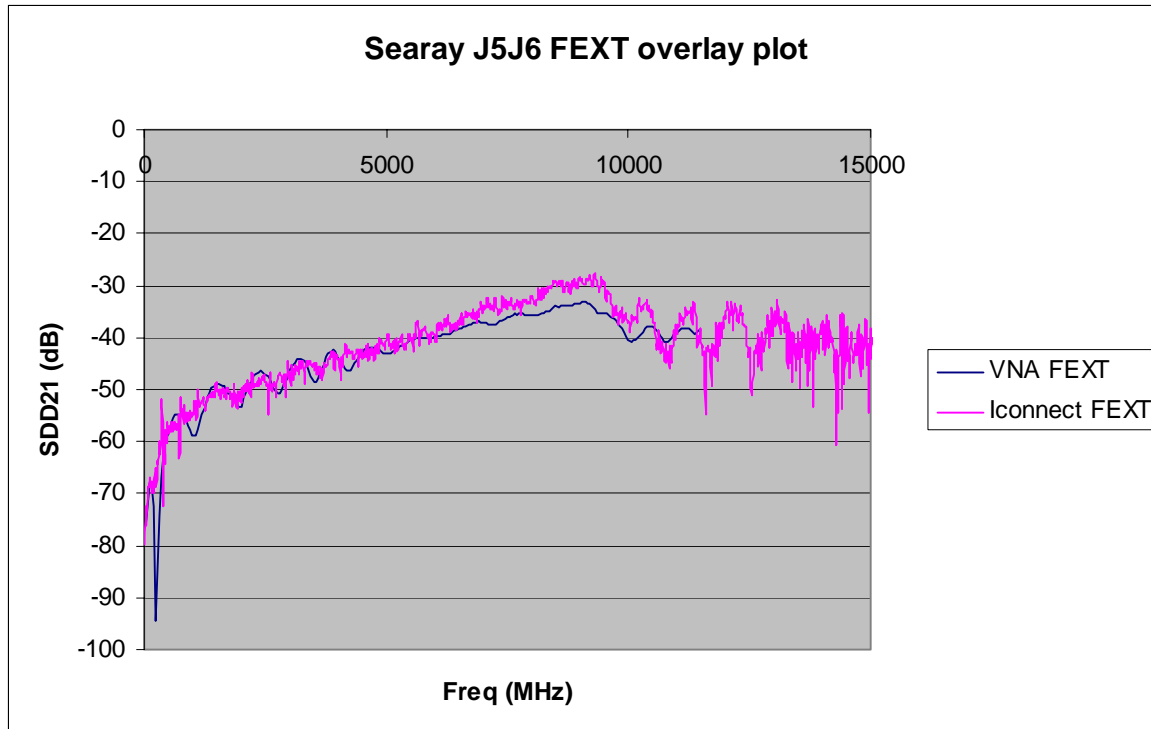

Figure 10: Frequency Domain correlation - NEXT

Figure 11: Frequency Domain correlation - FEXT

Model Extraction for Channel simulations

Once the measurements in the frequency domain are obtained, both PLTS and IConnect allow exporting data into the Touchstone format. Most simulators require an S4P file for differential DUTs. Not counting the calibration measurements, frequency domain data obtained from a single measurement of the DUT on the VNA can be exported to file with the mixed mode S4p format. Creating a mixed mode S4p file using IConnect requires multiple measurements, but requires no formal calibration. Insertion Loss is also required for modeling the channel. It can be similarly measured but is beyond the scope of this document.

Simulated Effect on Overall Channel

The effect of crosstalk on the overall channel may be demonstrated by using measured S-parameter data in a channel simulation tool. In this paper, we use StatEye v4.2.3 software which is basis for establishing channel compliance in Optical Internetworking Forum's Common Electrical Interface (CEI) Implementation Agreements.[7] StatEye uses a statistical algorithm to extrapolate Bit-Error Rate eye contours to very low BER values (something that would take huge computer resources and long simulation times if non-statistical simulations were used, such as direct HSPICE channel simulation).

For this paper, S-parameters extracted from a system backplane channel concatenated with mezzanine SEARAY™ connector were used. The effect of crosstalk on the margin of the channel is shown by comparing the results of a single quiet channel against those simulated in the presence of SEARAY™ crosstalk aggressors. Pure near end aggressors

for SEARAY™ were used, while far end aggressors were attenuated by the backplane channel.

The margin deterioration is dependent on how intelligently the designer assigns his Transmit and Receive pairs in the connector pin-out. Figure 12 shows the various pin-outs with crosstalk.

Figures 13, 14, 15 and 16 show the eye pattern output of the simulation after passing through a 3 tap equalizer. Several cases are shown, in the order of increasing crosstalk effect: 1) A single quiet channel, no crosstalk, 2) A single quiet victim surrounded by two far-end aggressors, as per TX/RX grouping recommended by Molex for the use of its SEARAY™ connector; 3) A single quiet victim surrounded by one near-end and one far-end aggressor, as per interleaved TX and RX, not recommended by Molex but inevitable for some applications; 4) A single quiet victim surrounded by two near-end aggressors, as per worst case TX/RX grouping, not recommended.
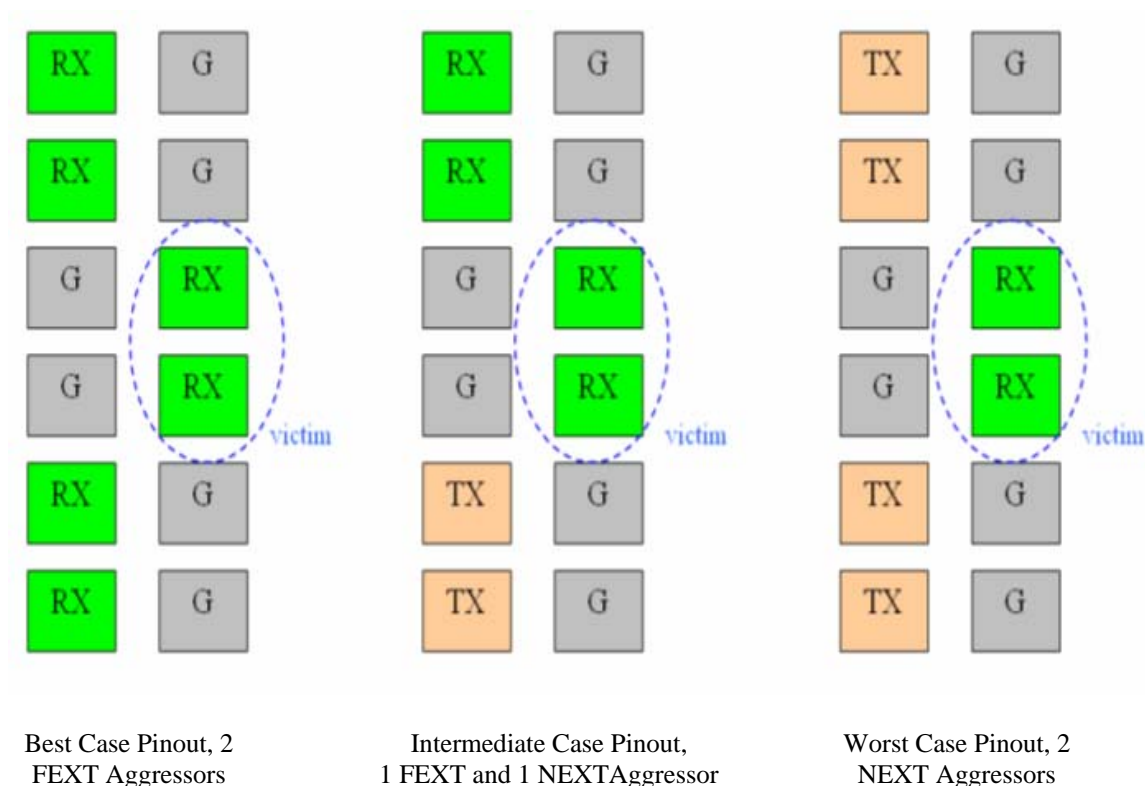
| Best Case Pinout, 2 FEXT Aggressors | Intermediate Case Pinout, 1 FEXT and 1 NEXTAggressor | Worst Case Pinout, 2 NEXT Aggressors |

Figure 12: Various pin-outs with crosstalk

The vertical eye opening numbers from figures 13, 14, 14 and 16 show that if proper pin assignment is not done then there could be a significant problem. For example, 1% of NEXT at TX voltage levels would result in 10% of Rx voltage levels. At 10 Gbps, the results of the channel are marginal to begin with, and the worst case TX/RX grouping clearly pushes it over the edge.
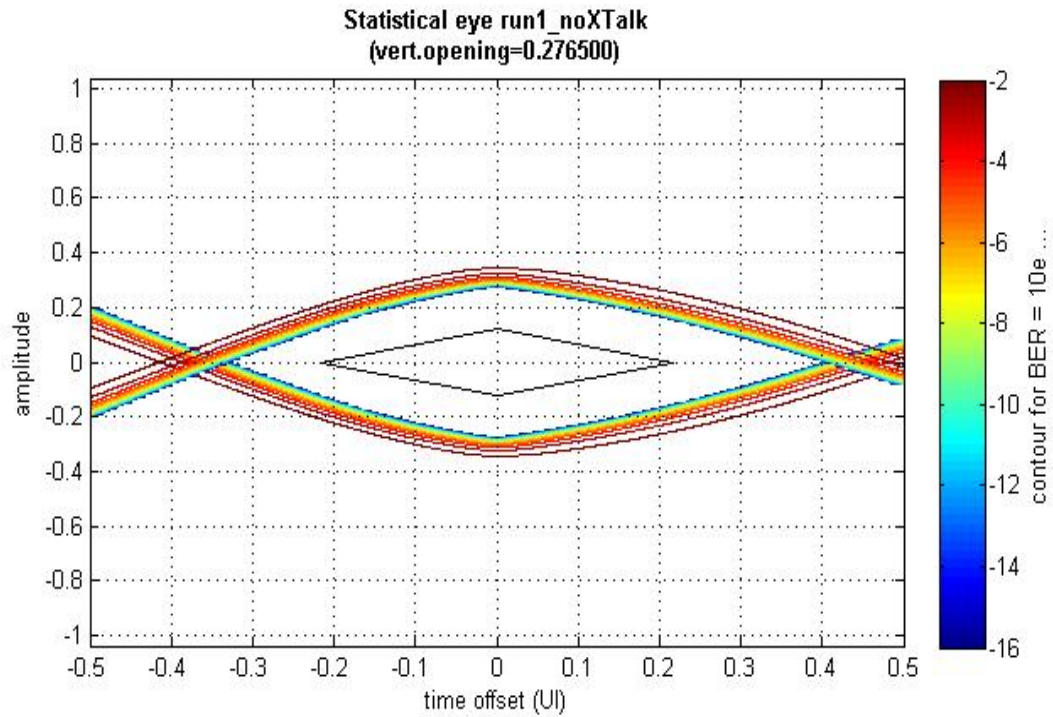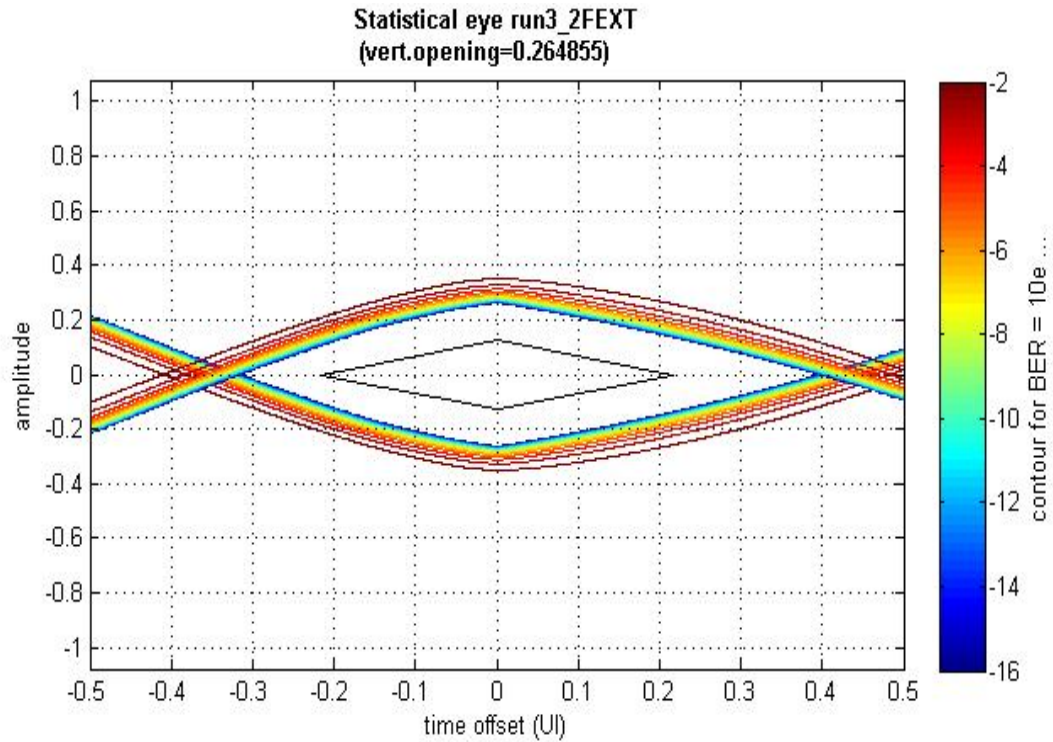
Figure 13: A single quiet channel, no crosstalk

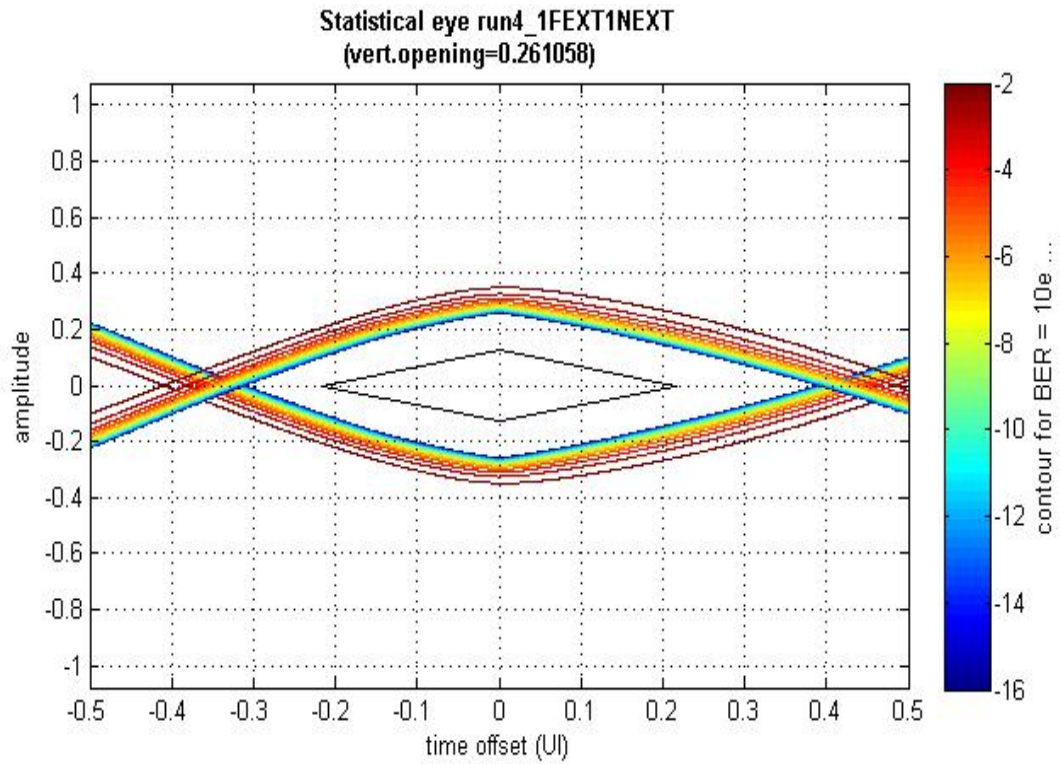**Figure 14: A single quiet victim surrounded by two far-end aggressors**

Figure 15: A single quiet victim surrounded by one near-end and one far-end aggressor
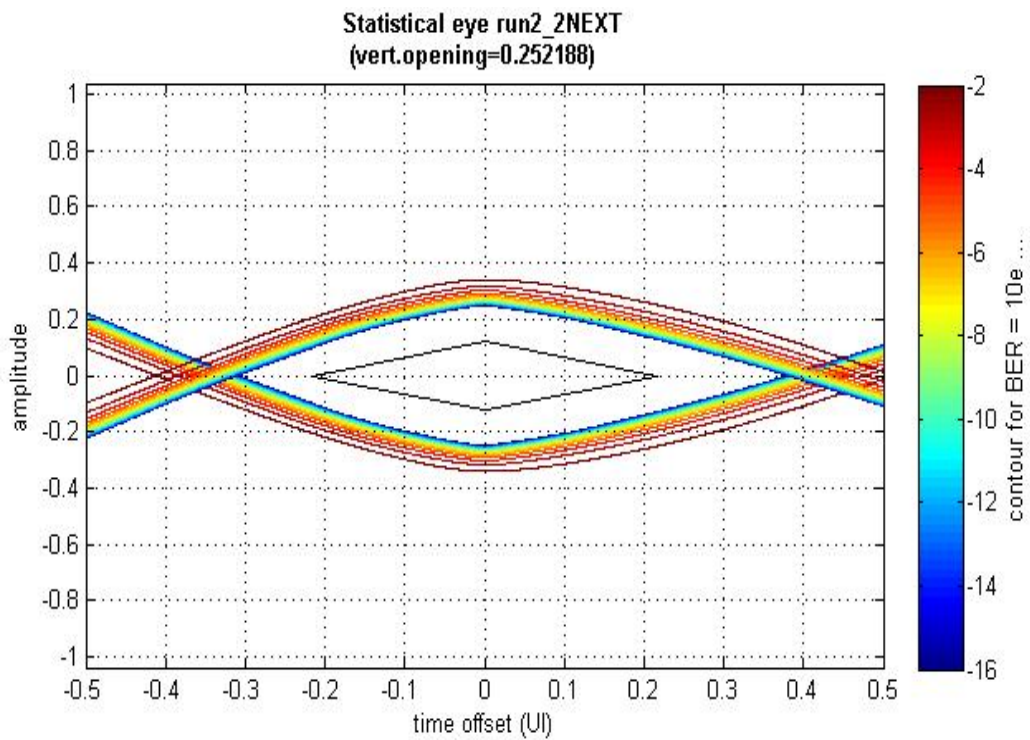

Figure 16: A single quiet victim surrounded by two near-end aggressors

Conclusion

A system based on the Molex SEARAY™ connector and IBM BladeCenter backplane was examined. A new and broadly applicable methodology was demonstrated to measure connector crosstalk using both frequency domain and time domain instruments. After applying adjustments, the time domain and frequency domain results correlated very well. This validated the connector model data and demonstrated that system level simulations could be done with a high degree of confidence to determine the impact of connector crosstalk. It is clear from the simulation results that careful assignment of connector pins is critical because, victim lines surrounded by two near end aggressors could significantly reduce channel margin at 10Gbps. This configuration is not recommended by Molex, but it illustrates the effect.

References

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