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Fast Physics-Based Via and Trace Models for Signal and Power Integrity Co-Analysis

Xiaoxiong Gu[1], Renato Rimolo-Donadio[2], Zhenwei Yu[3], Francesco de Paulis[4], Young H. Kwark[1], Matteo Cocchini[5], Mark B. Ritter[1], Bruce Archambeault[5], Albert Ruehli[3], Jun Fan[3], Christian Schuster[2]

[1] IBM T.J. Watson Research Center, NY
[2] Technische Universität Hamburg-Harburg, Germany
[3] Missouri Institute of Science and Technology, MO
[4] University of L'Aquila, Italy
[5] IBM Systems and Technology Group

Abstract

Physics-based models for vias and traces including new component models are applied to simulate multilayer interconnects on printed circuit boards. A variety of interconnect structures, including via arrays and differential links between package via fields, are studied with model-to-hardware correlation. These models also enable efficient signal integrity and power integrity co-analysis with focus on modeling simultaneous switching noise coupled into high-speed signal nets as well as understanding the effects of decoupling capacitor placement. Simulation time has been reduced at least three orders of magnitude with respect to comparable full-wave simulations.

Author's Biographies

Xiaoxiong Gu received the B.S. degree from Tsinghua University, Beijing, China, in 2000, the M.S. degree from the University of Missouri, Rolla, in 2002, and the Ph.D. degree from the University of Washington, Seattle, in 2006, all in electrical engineering. He is currently a Research Staff Member with the IBM T. J. Watson Research Center. His research interests include characterization of high-speed interconnect and microelectronic packaging, signal integrity and computational electromagnetics. Dr. Gu received the best paper award at ECTC in 2007 and DesignCon Paper Award in 2008.

Renato Rimolo-Donadio received the B.S. and Lic. degrees in electrical engineering from the Technical University of Costa Rica (ITCR), Costa Rica, in 1999 and 2004, respectively, and the M.S. degree in microelectronics and microsystems from the Technical University of Hamburg-Harburg (TUHH), Germany, in 2006, where he is currently working toward the Ph.D. degree in electrical engineering. Since November 2006, he has been a Scientific Research Assistant at the Institute of Electromagnetic Theory, Technical University of Hamburg-Harburg. His main research interests include system level modeling and optimization of interconnects, and analysis of signal and power integrity problems at PCB and package level.

Francesco de Paulis received his Laurea degree and his Specialistic degree (summa cum laude) in Electronic Engineering from University of L'Aquila, L'Aquila, Italy, in 2003 and 2006, respectively. He was involved in the research activities of the UAq EMC Laboratory from August 2004 to August 2006. From June 2004 to June 2005 he had an internship at Selex Communications s.p.a. within the layout/SI/PI design group. In August 2006 he joined the EMC Laboratory at the Missouri University of Science and Technology (formerly University of Missouri-Rolla), where he pursued a Master of Science Degree in Electrical Engineering in May 2008. He is currently enrolled in PhD program at the University of L'Aquila, L'Aquila, Italy. His main research interests are in developing fast and efficient analysis tool for SI/PI design of high speed signal on PCB, RF interference in mixed-signal system, EMI problem investigation on PCBs.

Zhenwei Yu received his B.S. degree in Mathematics and Physics, and M.S. degree in Electrical Engineering from Tsinghua University, Beijing, China, in 2005 and 2007 respectively. Currently he is a Ph.D. candidate with the EMC Laboratory at Missouri University of Science and Technology (formerly University of Missouri-Rolla). His research interests include modeling of IC emissions, RF interference, PCB noise mitigation, and tool development for Signal Integrity and Electromagnetic Compatibility designs in high-speed PCBs. He was a Co-op at IBM, Research Triangle Park, NC, from January to July 2009 and worked in the EMC modeling tool development.

Young H. Kwark received his BSEE from the Massachusetts Institute of Technology and his MSEE/PhD from Stanford University. His work experience as a Research Staff Member at the IBM T. J. Watson Research Center, Yorktown Heights, NY, includes circuit design for optical links and wireless applications.

He is currently involved in package characterization for high performance computing platforms. Dr. Kwark received DesignCon Paper Awards in 2005, 2006 and 2008.

Matteo Cocchini received his Laurea (5-year degree) in Electronic Engineering in June 2006 from University of L'Aquila, L'Aquila, Italy, where he got involved in the research activities of the UAq EMC Laboratory in 2005 and 2006. In August 2006, he joined the MST EMC Lab at the Missouri University of Science and Technology, where his research activity included via transition modeling and power distribution network simulations. He got a Master of Science in Electrical Engineering from the same University in May 2008. He currently works as Signal and Power Integrity Engineer for the IBM I/O packaging and development team in Poughkeepsie, New York.

Mark B. Ritter received a B.S. degree in physics from Montana State University in 1981 and M.S., M.Phil. and Ph.D. degrees in Applied Physics from Yale University in 1987. His work at IBM has focused on high-speed I/O circuit and package design, with work including Fibre Channel, 10 Gb/s Ethernet, and 40 Gb/s analog front end circuits as well as interconnect structures for high-speed data transmission. Dr. Ritter presently manages a group focusing on high-speed I/O subsystems. Dr. Ritter was the recipient of the 1982 American Physical Society Apker Award and DesignCon Paper Award in 2008.

Bruce Archambeault is a Senior Technical Staff Member at IBM in Research Triangle Park, NC. He received his B.S.E.E degree from the University of New Hampshire in 1977 and his M.S.E.E degree from Northeastern University in 1981. He received his Ph. D. from the University of New Hampshire in 1997. Dr. Archambeault has authored or co-authored a number of papers in computational electromagnetics, mostly applied to real-world EMC applications. He is currently a member of the Board of Directors for the IEEE EMC Society and a past Board of Directors member for the Applied Computational Electromagnetics Society (ACES). He has served as a past IEEE/EMCS Distinguished Lecturer and Associate Editor for the IEEE Transactions on Electromagnetic Compatibility.

Albert E. Ruehli received his Ph.D. degree in Electrical Engineering in 1972 from the University of Vermont, and an honorary Doctorate in 2007 from the Lulea University in Sweden. He has been a member of various projects with IBM including interconnect tools and modeling and manager of both a VLSI design and CAD group. From 1972 to 2009, he was with IBM's T.J. Watson Research Center. Currently, he is an Adjunct Professor at the Missouri University of S&T and an Emeritus at IBM. He is the editor of two books and author or coauthor of over 180 technical papers. He received five IBM Awards, the Guillemin-Cauer Prize in 1982, and the Golden Jubilee Medal from the IEEE CAS Society in 1999. He received a Certificate of Achievement from the IEEE EMC society in 2001, the 2005 Richard R Stoddart Award, and in 2007 he received the Honor ary Life Member Award from the IEEE EMC Society and is a Life Fellow of the IEEE and a member of SIAM.

Jun Fan received his B.S. and M.S. degrees in Electrical Engineering from Tsinghua University, Beijing, China, in 1994 and 1997, respectively. He received his Ph.D. degree in Electrical Engineering from the University of Missouri-Rolla in 2000. From 2000 to 2007, he worked for NCR Corporation, San Diego, CA, as a Consultant Engineer. In July 2007, he joined the Missouri University of Science and Technology (formerly University of Missouri-Rolla), and is currently an Assistant Professor with the UMR/MS&T EMC Laboratory. His research interests include signal integrity and EMI designs in high-speed digital systems, dc power-bus modeling, intra-system EMI and RF interference, PCB noise reduction, differential signaling, and cable/connector designs. Dr. Fan serves as the Chair of the TC-9 Computational Electromagnetics Committee, the Secretary of the Technical Advisory Committee, and a Distinguished Lecturer of the IEEE EMC Society.

Christian Schuster received the Diploma degree in physics from the University of Konstanz, Germany, in 1996, and the Ph. D. degree in electrical engineering from the Swiss Federal Institute of Technology (ETH), Zurich, Switzerland, in 2000. From 2001 to 2006 he was a Research Staff Member at the IBM T. J. Watson Research Center, Yorktown Heights, NY. Since October 2006, Dr. Schuster is a full professor of electrical engineering at the Technische Universität Hamburg-Harburg (TUHH), Germany. Dr. Schuster received DesignCon Paper Awards in 2005 and 2006. He is a senior member of the IEEE.

1. Introduction

A multilayer PCB can be divided electrically into two functional parts: a signal link path and a power delivery network (PDN). The signal path consists of traces and vias whereas the PDN is defined by a stack-up of power and ground planes, large numbers of vias connecting the planes in different layers, and many decoupling capacitors. To meet the requirement of increasing input/output (I/O) bandwidth and density, a large number of signal nets are densely routed often interwoven with the PDN which makes them susceptible to power and ground switching noise. Efficient and accurate modeling and simulation of interconnects is essential to perform signal integrity (SI) and power integrity (PI) co-analysis for high-speed link design on a multilayered PCB.

Our research interests have focused on constructing physical link component models without resorting to full-wave EM field simulations. In previous work, the authors have presented scattering-based semi-analytical via models [1], physics-based via models [2─6] using parallel-plane impedance Z_{pp} and via-to-plane capacitance [7], [8], and trace models based on the modal decomposition technique [9], [10]. Our link analysis methodology provides a complete and systematic end-to-end solution for trace and via design of the entire link path [5], [6]. It can be used during the pre-layout phase to quickly perform design discovery and to narrow the design space through manual or automated optimization.

In this paper, the authors further extend the approach including models for components such as decoupling capacitors. Next, we focus on applying the new models and the methodology to analyze several design problems considering both signal integrity and power integrity performance. We analyze via array field coupling and multilayered differential links between two package via fields and compare predictions to measured data. We also investigate simultaneous switching noise coupling through the PDN to high speed signal nets as well as studying the impact of decoupling capacitor placement on noise reduction.

2. "Via and Trace" models + "Component" models

Figure 1 illustrates a cross-section view of a typical multi-layered PCB with a stripline trace referenced to both power and ground planes and which is connected to signal vias on both ends. Ground and power vias located some distance away from the signal via are also included. Components such as decoupling capacitors and termination resistors are often connected to power or signal vias on the PCB surface. The overall link analysis addresses

-- Vias including geometric effects and coupling;
-- Stripline transitions to/from vias;
-- Coupled striplines referenced to both power and ground planes;
-- Termination and decoupling components;

In [5], we described the key models developed and implemented in this link analysis methodology: the multi-layered via structures are modeled using the physics-based model for rectangular or infinite shaped plane pairs to account for the coupling among vias. The effects of via geometric parameters are represented by an analytical form of via barrel-to-plane capacitance. Transmission lines routed between power and ground planes are represented by appropriate admittance matrices. These component models are then concatenated in terms of S-parameters based on the link topology.

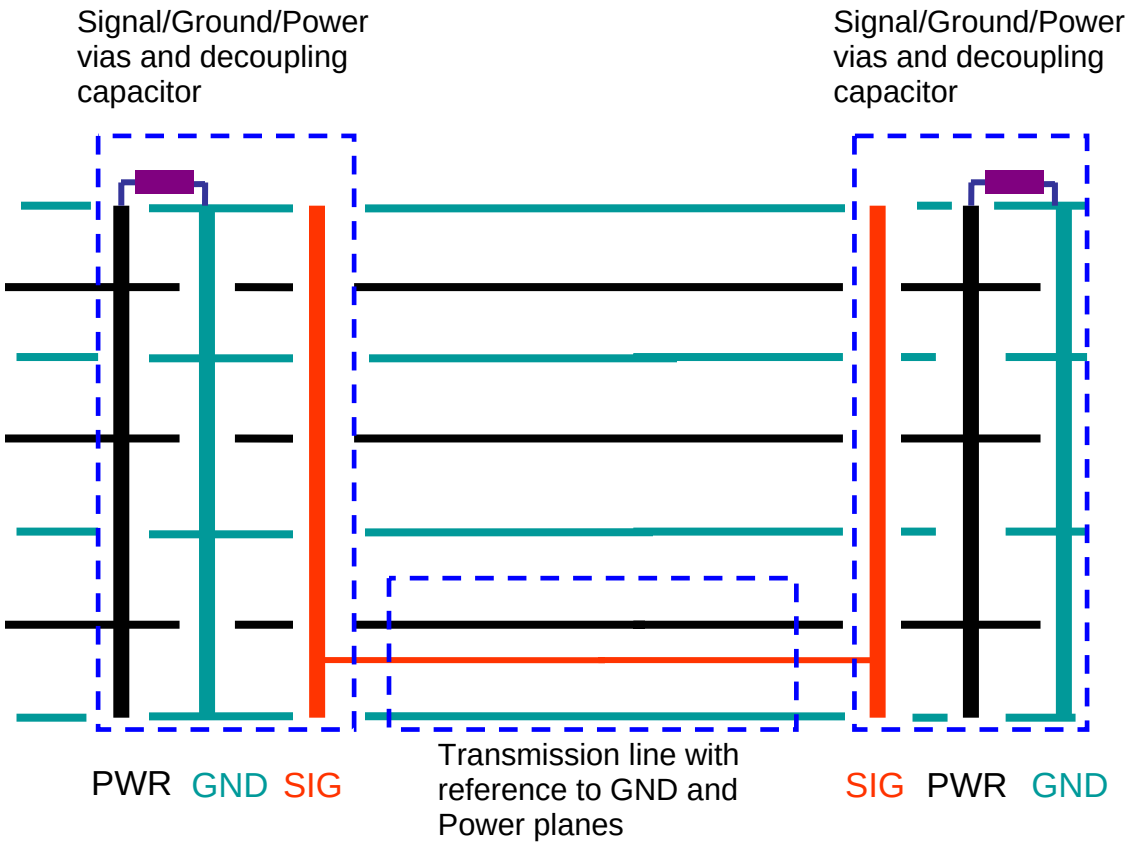


Figure 1. Example of an end-to-end link on PCB including stripline and vias.

Recently, we have implemented modeling components which are directly connected to vias. The components can be represented by a RLC series circuit, a RLC parallel circuit, or network scattering parameters. Figure 2 (left) illustrates series/parallel RLC circuits for the component models. Here, one terminal of the RLC model would be connected to the via and the other terminal would be connected to the reference plane. For example, in case of modeling a decoupling capacitor as shown in Figure 1, one terminal of the RLC circuit is connected to a PWR via and the other terminal is connected to the top ground plane. Figure 2 (right) illustrates a general N-port scattering parameter block which can be connected to m vias (m<=N). Here, one via connects to one individual S-parameter port. In addition to the via ports, the S-parameters can also contain an I/O port (i.e. port defined in the final solution) or an OPEN port. This feature is useful in modeling when we need to take into account any connectors, cable fixtures, or probes that connect to the

vias. Figure 3 illustrates a 4-port S-parameter block in which port 1 and port 2 are connected to two signal vias of a differential pair, while port 3 and port 4 are either OPEN ports or I/O ports. For example, the 4-port S-parameters here may represent a dual SMA launch or a dual microwave probe of which the S-parameter frequency response can be obtained from separate characterization either by measurement or by simulation.

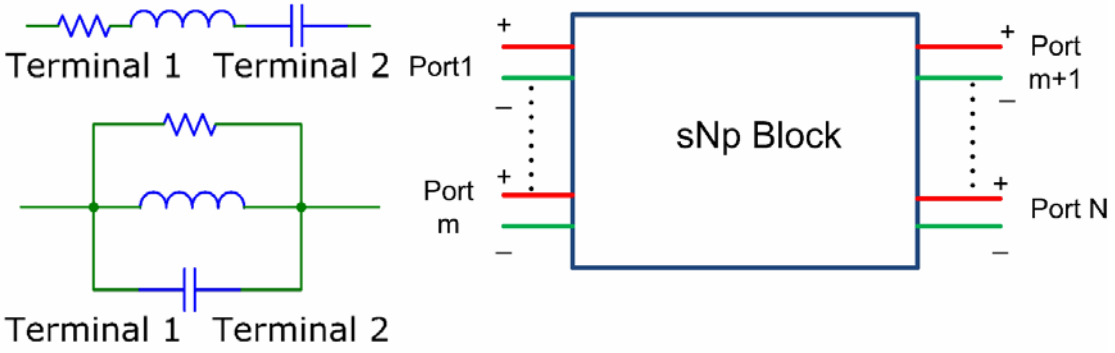


Figure 2. Series/parallel RLC circuits and S-parameter network for component models.

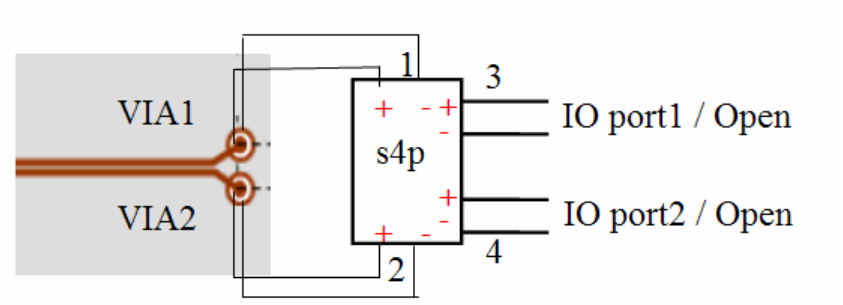


Figure 3. Example of a 4-port scattering parameter block for component models.

Having added the new component models, we revise the flow chart in [5] for assembling all the models together in a link analysis environment (Figure 4). Simulation set-up parameters and geometries of a PCB link first need to be specified in a text based I/O file for analysis. These include

- Frequency sweep parameters;
- Computational method for Zpp with different boundary conditions;
- Board dimensions;
- Board layer stack-up including dielectric properties;
- Pad stack for signal vias, power vias and ground vias;
- Via map including via location, type of pad stack, and connection with signal nets
- Trace definition which defines transmission line models in touchstone format for selected nets;
- Component models in terms of RLC circuits or S-parameter data and their connection to the vias;
- Input/Output manager which configures ports for S-parameter analysis and post-processing.

Efficient generation of the via geometries and simulation parameters was managed through a MATLAB graphical user interface (GUI), which implemented all the above functions and created a text I/O file. The GUI can also load and modify any existing I/O file. After reading the I/O file, the engine performs link analysis computations. All the component models, including via capacitance, Z_{pp}, striplines and component models are incorporated in the engine. Models are self-assembled and the final results are given in terms of S-parameters and stored in standard Touchstone format. The S-parameter file can also be loaded and plotted using the GUI.

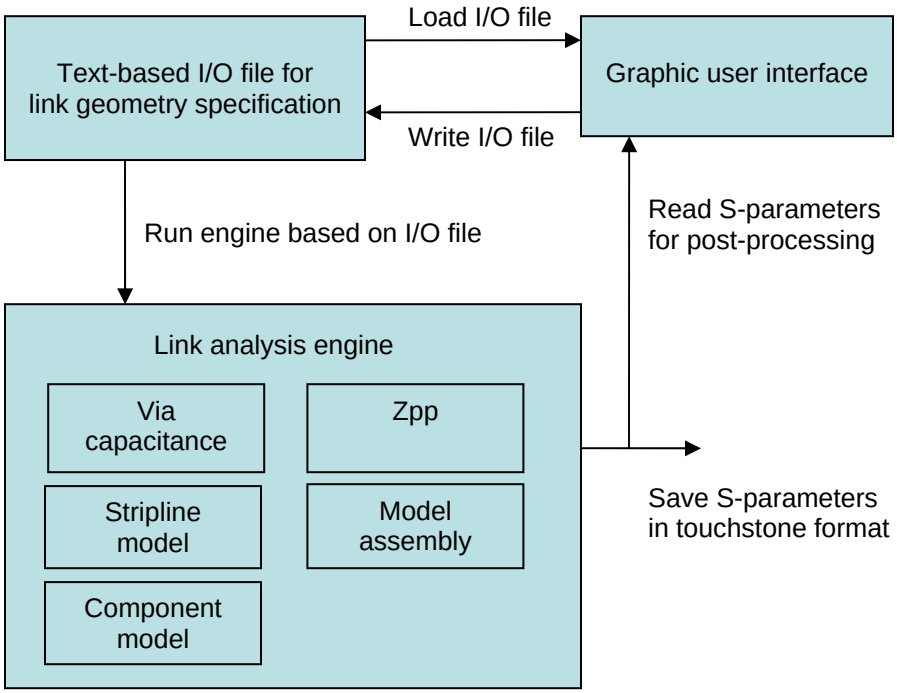


Figure 4. Flow chart of implementing link analysis.

3. SI and PI Study of Design Examples

Via Array Field Analysis

Via arrays such as those found in ball/land grid array (BGA/LGA) fields often introduce significant signal cross-talk and degradation of the signals. To apply our models to study the electromagnetic field coupling in the via array, we have built via array structures without any trace connection in an 18-layer test board. Figure 5(left) shows the measured layer stack of the board. All vias in the array go through from the top plane to the bottom plane. Figure 5(right) illustrates the pattern of an 8-by-8 via array with an 80-mil pitch. There are 29 signal vias and 35 ground vias in this array. The radius of the via drill is 5 mils with an antipad radius of 15 mils. Only the top and bottom planes have circuilar pads with a radius of 10 mils. All ground planes have the same size as the original board panel (21.8-inch by 16.8-inch) except for the top and bottom planes which have a much smaller square shape with a size of 600-mil by 600-mil. The dielectric material of the

board is Nelco4000-13. Three vias labeled in Figure 5(right) were measured using a vector network analyzer with GS probes (225um pitch) from the surface of the top plane as shown in Figure 6. Except for those contacted with the probes, both ends of all the signal vias were left open in the measurement set-up. The additional capacitance due to the fringing field from the surface via pads was not taken into account in the model.

Figure 7 gives a comparison of simulated and measured near-end crosstalk expressed in terms of scattering parameters. Excellent correlation between the simulation and the measurement in these cases were obtained up to 20GHz. We can see that because of the ground via and larger distance between via 1 and via 2, the cross-talk S23 is significantly higher than S12 and S13. Also, the crosstalk S13 is higher than S12 at some high frequencies due to the field scattering by adjacent vias despite of the larger distance between the two signal vias.

For the numerical simulation of the 80-mil pitch via array structure, our simulation using the physics-based via model took only about 37 seconds of CPU time for 200 frequency points up to 20 GHz on a single Intel processor (3GHz), whereas a 3D full-wave (HFSS®) simulation took more than 12 hours even with sweep interpolation enabled.

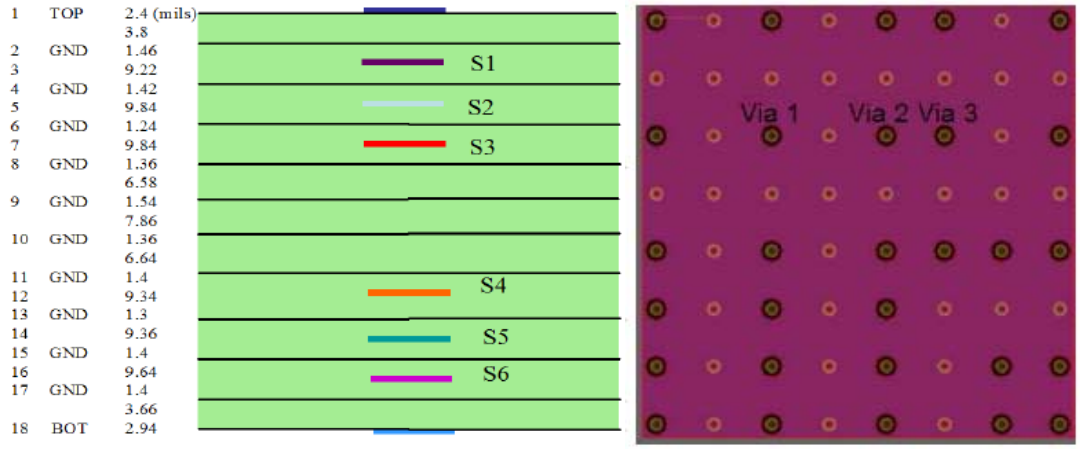


Figure 5. Measured layer stack of the test board (left), top-view of the via array with 80-mil pitch (right).

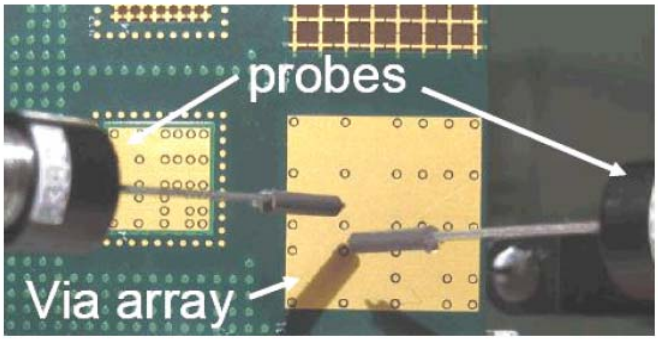


Figure 6. Probing measurement setup on the board surface.

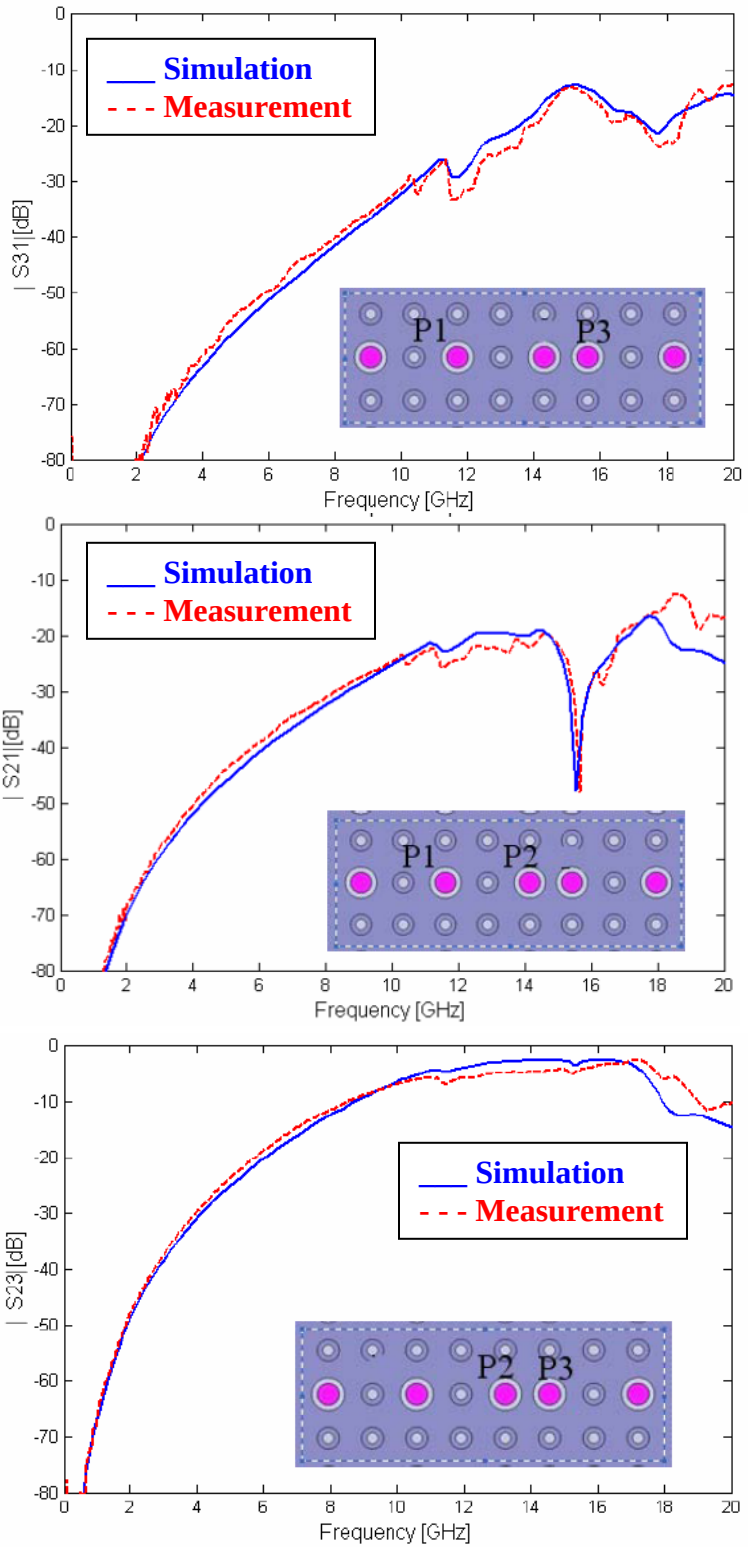


Figure 7. Near-end crosstalk among via 1, via 2 and via 3 in an array with 80-mil pitch.

Differential links between BGA via fields on a multilayered PCB

We also applied the updated models and the link analysis method to revisit a real on-board link described in [5]. Figure 8 shows a measurement set-up for an end-to-end differential link between two BGA via fields on a 24-layer low loss PCB. The analysis we show here is a major extension to the previous analysis in that we study channels on two different signal levels (i.e., 7 channels on S3 layer and S5 layer, respectively, as opposed to 2 channels on one S3 layer in [5]). For those adjacent signal vias whose stripline connections are not considered, we also terminated these vias using 50Ohm resistors to avoid via resonance artifacts in the modeling results. Figure 9 illustrates the layout of via fields and striplines on S3 layer and S5 layer. Board dimensions, layer stack, pad stack definition, as well as dielectric properties can be found in [5]. There are in total 119 vias (76 signal vias; 43 ground vias) and 14 differential pairs in the extended model.

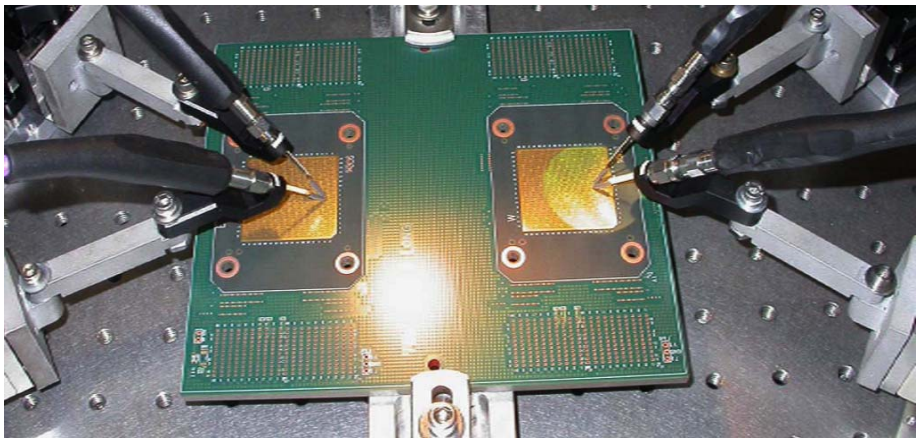


Figure 8. End-to-end differential link measurement on PCB.

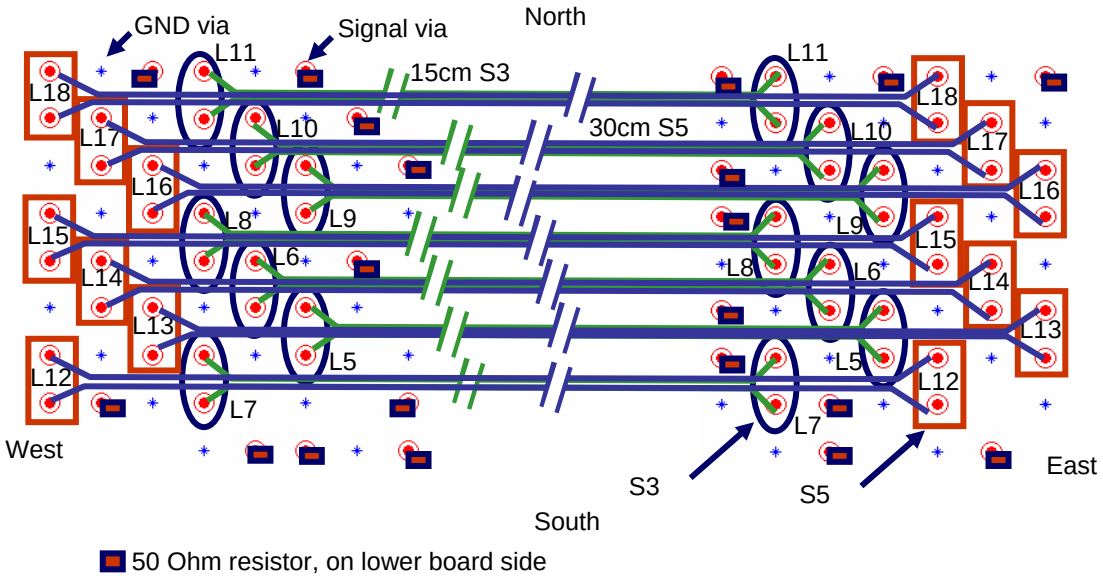


Figure 9. Top view of configuration of via array and stripline layout.

The model-to-hardware correlation results in terms of single-ended S-parameters (link 9 on layer S3) are plotted in Figure 10 up to 40 GHz. The cross-talk in the via array field, as well as the via stub effect on the insertion loss curve, are well captured in the simulation. The correlation between simulation and measurement are satisfactory considering the complexity of the real board structures and model simplifications. The model parameters were calculated based on physical geometries and they were not fitted in the simulation.

With these simulation results, it is possible to compute the time-domain response for data rates up to 15 Gb/s with good accuracy. Figure 11 shows that the shape, vertical and horizontal opening of the eye diagram agree well (within 10%) up to that speed. Figure 12 shows that the insertion loss differences between links at the same layer are small. The same trends are observed between measurement and simulated results. Figure 13 illustrates the far-end crosstalk and transmission for link 17 on layer S5. Models also capture the salient features of the response for the longer link at S5.

The total run time (excluding generating transmission line models) was about 2 minutes 47 seconds using Z_{pp} calculation with PML boundary condition for 200 frequency points on a single processor (3.0GHz) with 4GB memory. This model was too large to run in a full-wave simulator.

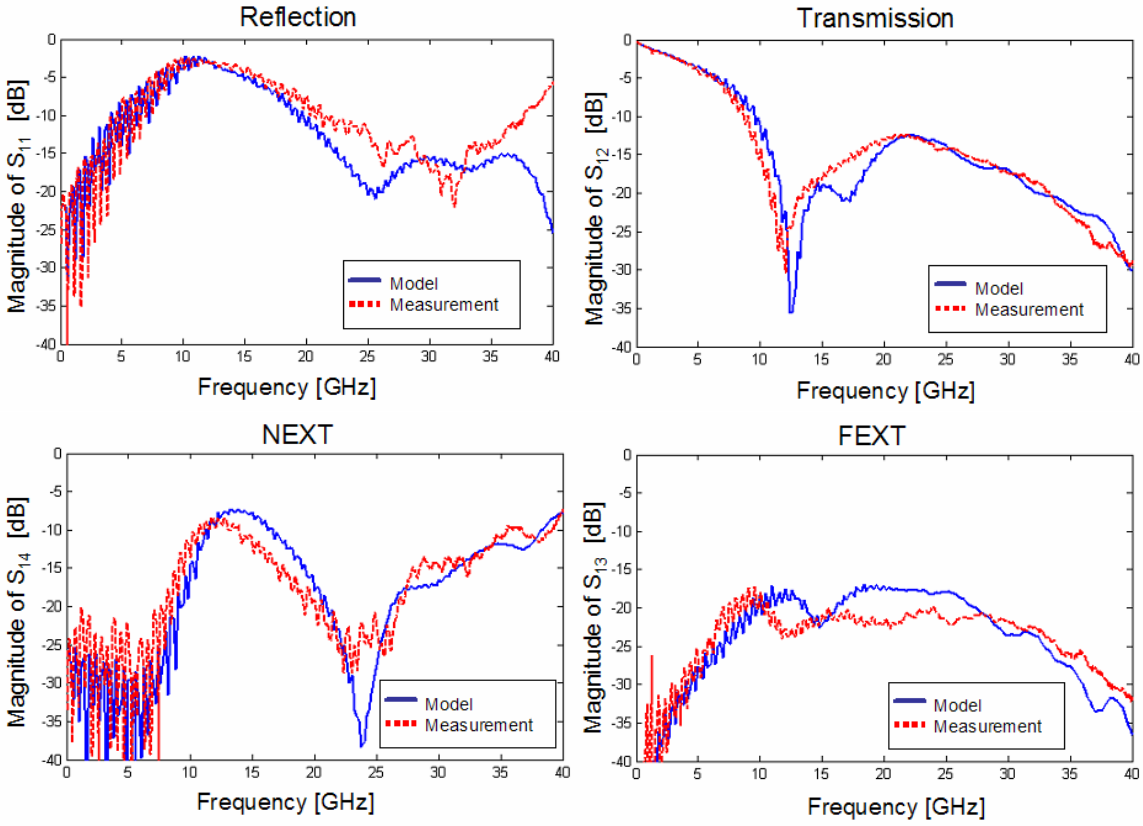


Figure 10. Comparison of single-ended S-parameter results for link 9 (red: measurement; blue: simulation).

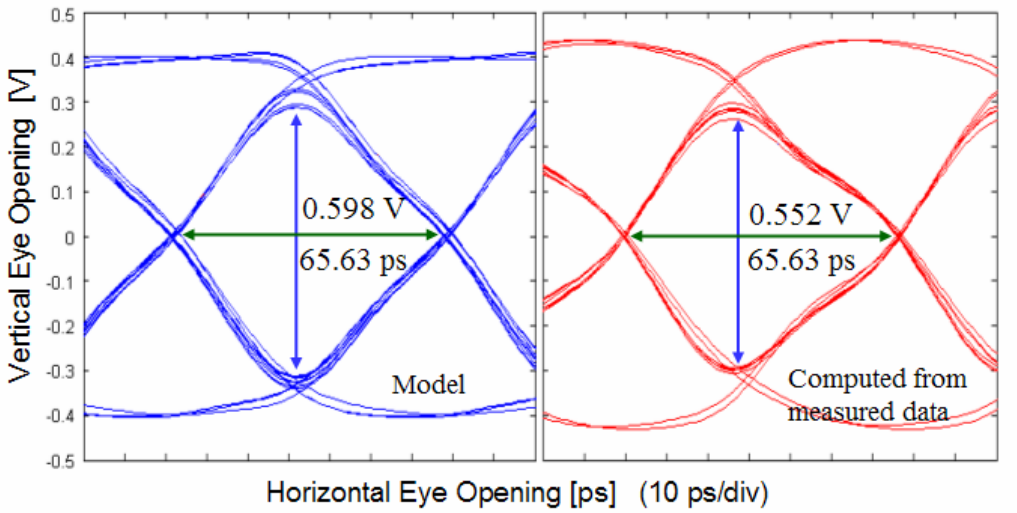


Figure 11. Eye diagrams for the differential link 5 on layer S3 at 15Gbps, assuming10ps rise/fall time ($tr_{20\text{-}80}$).

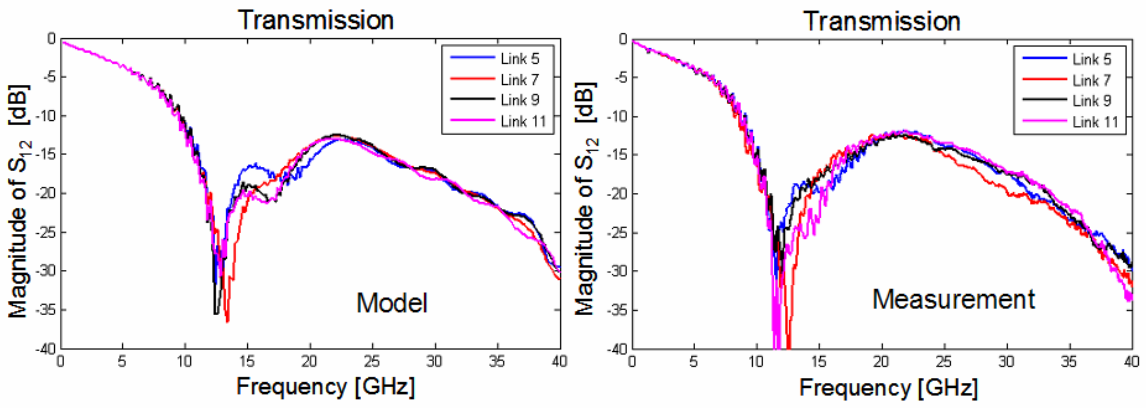


Figure 12. Insertion loss comparison for different striplines on layer S3 (left: simulation; right: measurement).

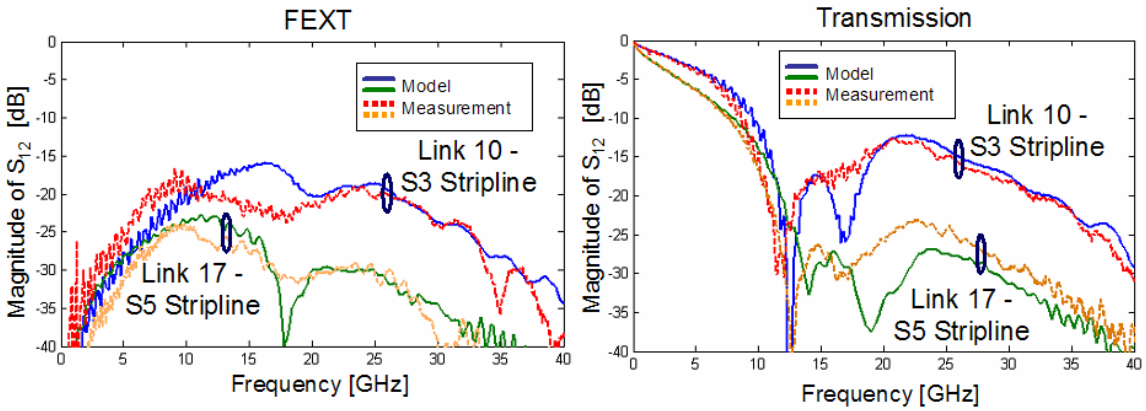
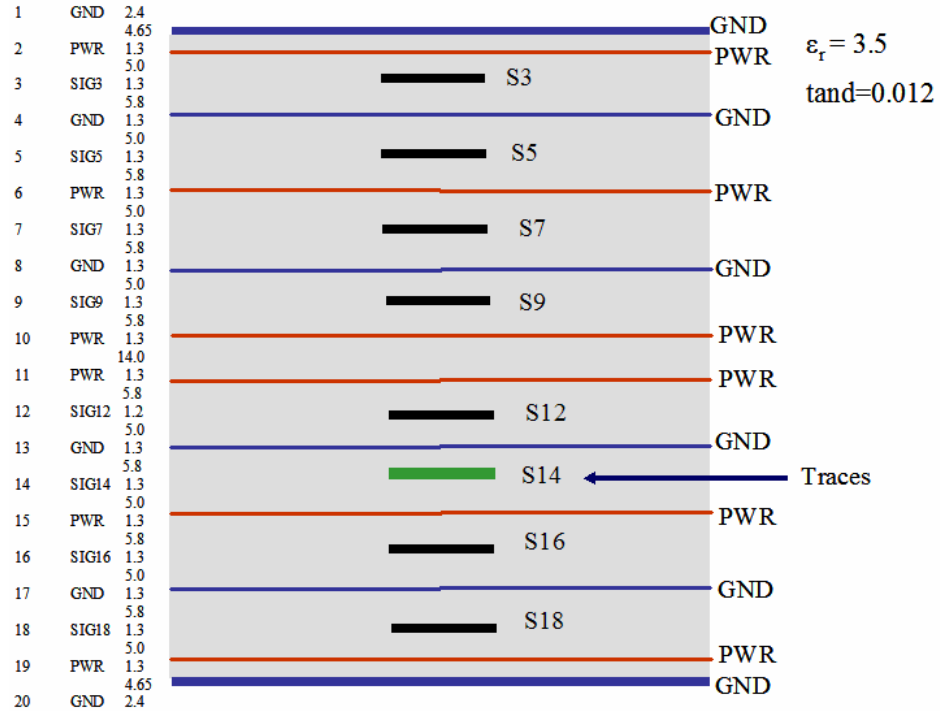


Figure 13. FEXT and transmission comparison for links on layer S3 and layer S5.

PDN noise coupling and decoupling capacitor placement

The last example is targeted at analyzing how simultaneous switching noise couples into the high-speed signaling nets through the PDN and whether placing decoupling capacitors would reduce the noise impact on signals. It is well-known that the PDN in the form of parallel plane pairs serves as current return path for signals. However, these plane pairs also behave as waveguides and support propagation of switching noise excited by vertical currents along vias. The propagation of the noise is affected by the shape and the size of plane pairs as well as the vertical vias which may be connected to decoupling capacitors [11], [12]. In this example, we look at transfer impedance in particular between signal via ports and noise sources to evaluate the strength of noise coupling. A smaller transfer impedance means less switching noise coupling and thus better signal integrity performance.

Figure 14 depicts a test coupon including sketches of the via and trace layout and layer stack-up. Unlike the link example above where all the reference planes are ground, this test coupon has interleaved power planes and ground planes connected by power vias (in red) and ground vias (in blue) respectively. The via arrays on both ends of the differential links have a 1-mm pitch. All the signal/power/ground vias have 10mil drill diameter and 30mil antipad diameter. There are 4 pairs of 2-inch long differential links on layer S14. We modeled the structure using our physics-based link models and also verified the model with 3D full-wave simulation (HFSS®). Correlation results in terms of single-ended S-parameters are shown in Figure 15 indicating good accuracy up to 20GHz. The total run time (excluding generating transmission line models) was about 5 minutes using a Z_{pp} calculation with PMC boundary conditions (single summation with 100 iterations) for 200 frequency points on a single processor (3.0GHz) with 4GB memory.



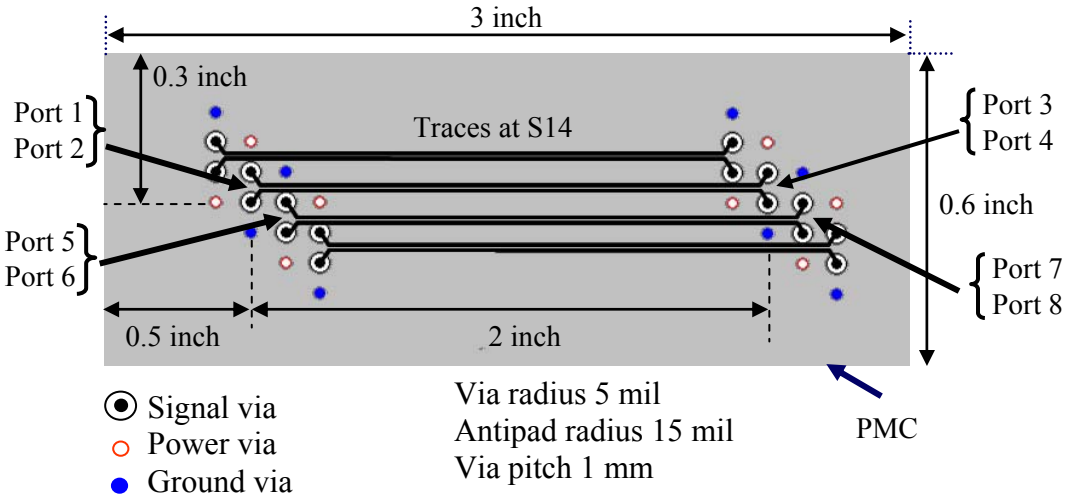


Figure 14. Description of via/trace layout and layer stack with mixed reference planes.

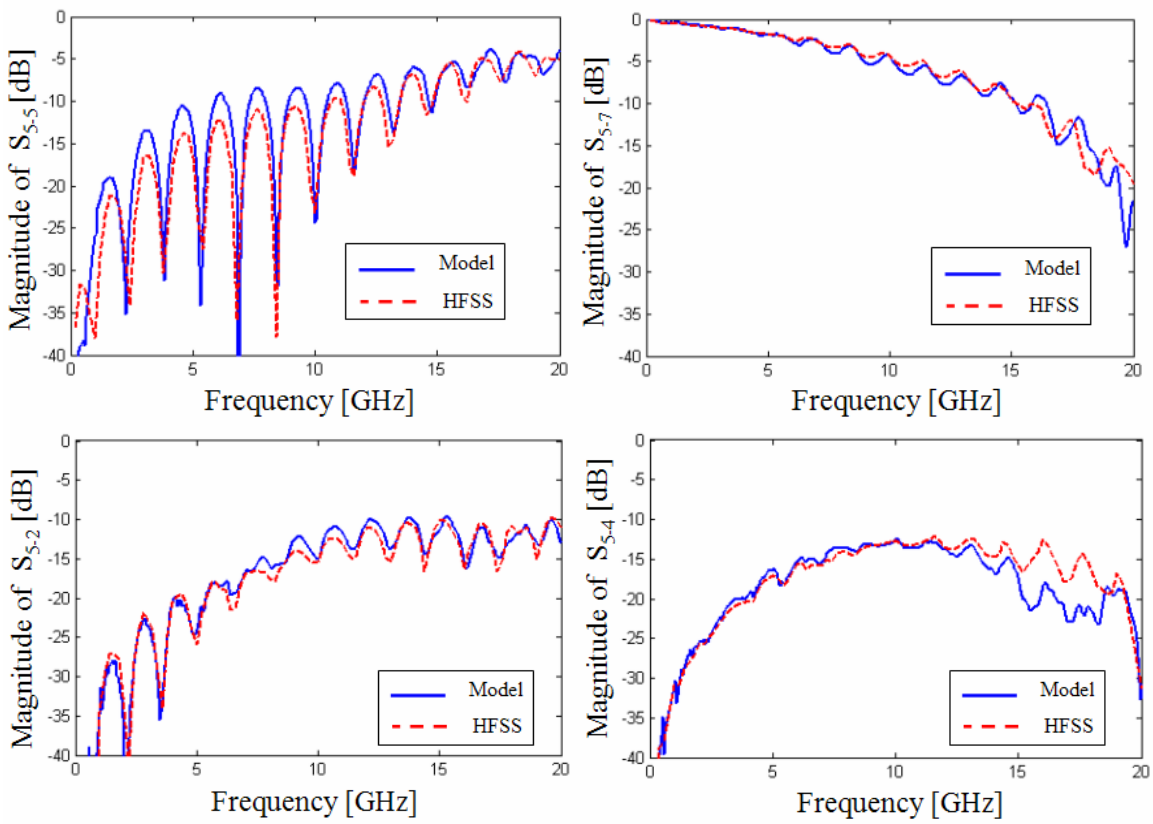
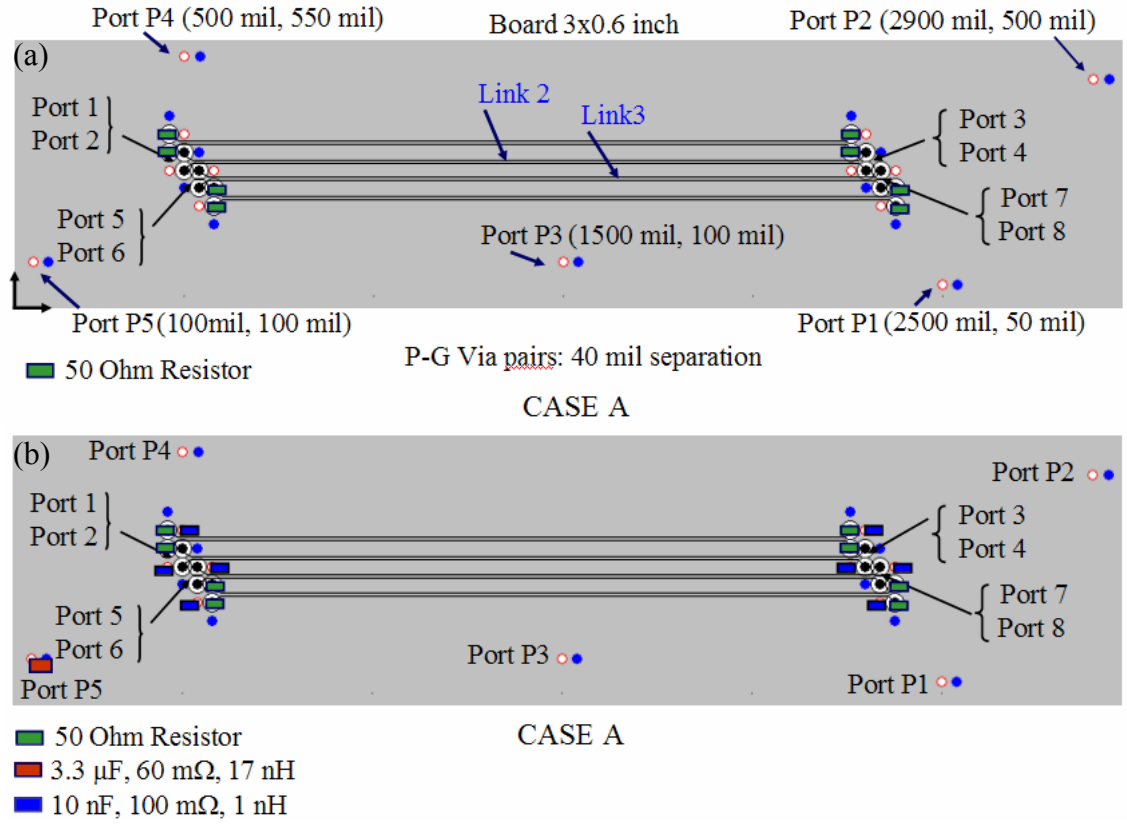


Figure 15. Comparison of single-ended S-parameter results.

To study the PDN noise coupling, we simulated two cases with four test coupons illustrated in Figure 16. Here, two of the four differential links are terminated by 50 Ohm resistors on top of the PCB surface. There are also 5 power/ground via pairs (indicated as P1-P5) located around the high-speed links for either decoupling capacitor placement or noise injection.

We first compared the transfer impedance between switching noise source P1 and signal via port 1 or port 8 as shown in Figure 17. The dotted blue curve represents the case (case A) without any decoupling capacitor (Figure 16-a). The dashed green curve represents the case (case A) where eight small decoupling capacitors (10nF, 100mΩ, 1nH) and one large global decoupling capacitor (3.3uF, 60mΩ, 17nH) are put in connection with the power vias on the PCB surface (Figure 16-b). These RLC values were obtained from curve fitting to measured S-parameters of MLC capacitors. It is shown that the decoupling capacitors are only effective in low frequencies (below 2GHz, e.g.). In high frequencies, the effects of decoupling capacitors are not observable due to parasitic inductance. The noise coupling through the PDN is mostly dominated by the plane pair resonance mode where we can actually see the impedance curves of two cases overlapping each other.

Next, we added 72 extra ground/power via pairs in two rows (with 40-mil pitch) on two test coupons (case B) without any decoupling capacitors (Figure 16-c) and with decoupling capacitors (Figure 16-d). The transfer impedance responses are plotted in Figure 17. Without decoupling capacitors, the low frequency response of the transfer impedance does not change as expected. However, adding two rows of power/ground via pairs forms two conducting walls next to the signal via ports and changes the plane pair resonances, shifting them to higher frequencies. On the other hand, adding many decoupling capacitors to these via pairs further reduces the equivalent series inductance and increases equivalent capacitance (and resistance). Below 2GHz, we can see that having 85 decoupling capacitors lowers the impedance much more than having 9 decoupling capacitors.



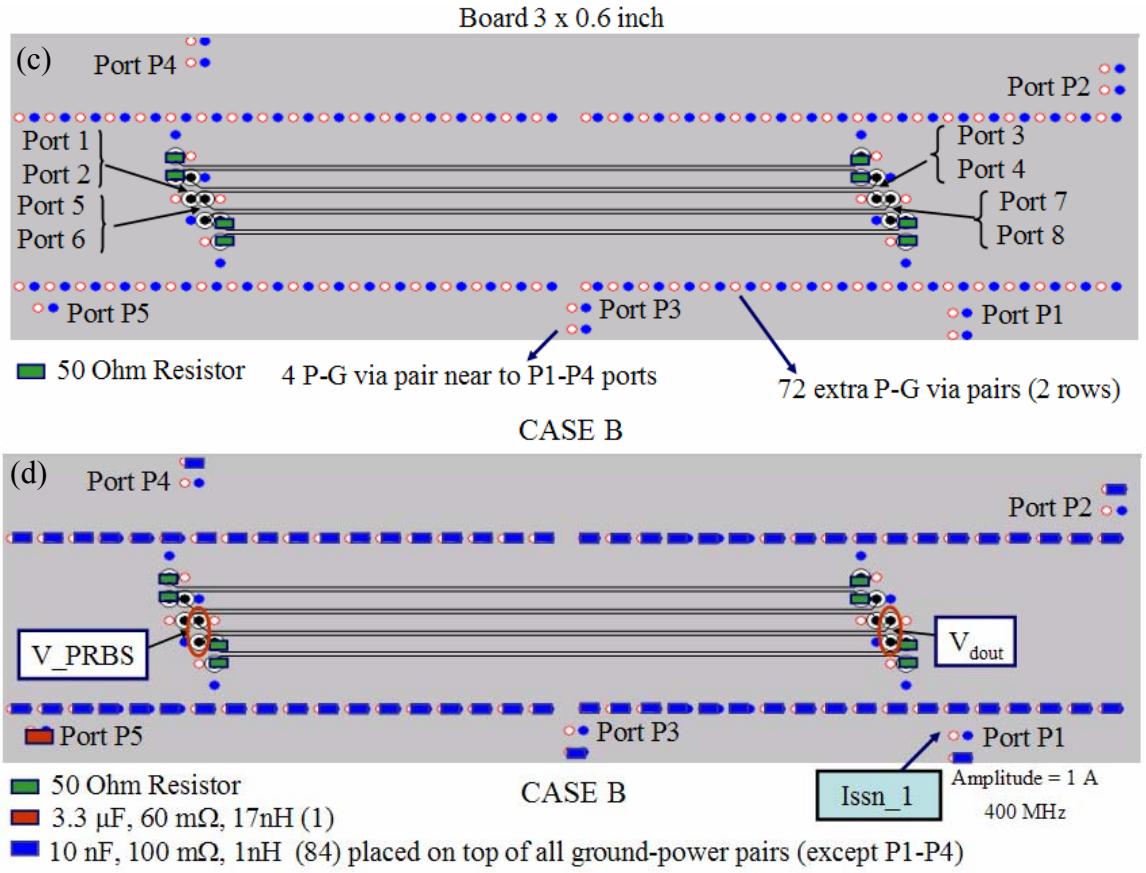


Figure 16. Top view of configuration of via array and stripline layout: (a) Case A without decaps; (b) Case A with 9 decaps; (c) Case B with extra ground-power via pairs, no decaps; (d) Case B with extra ground-power via pairs and 85 decaps.

The simulation (excluding generating transmission line models) took about 6 minutes and 5 hours for case A and case B, respectively, using Z_{pp} calculation with PMC boundary condition (single summation with 100 iterations) for 200 frequency points on a single processor (3.0GHz) with 4GB memory. The difference in simulation time is mostly due to the Z_{pp} calculation which slows down for a large number of via ports and for finite rectangular-shaped plane pairs.

Figure 18 illustrates the simulated eye diagrams using ADS® for differential signals received at port 7 and port 8 at 0.8Gbps. PRBS8 125ps rise time data (±0.5V differential amplitude) were input to ports 5 and 6. Switching noise was modeled with symmetric triangular pulses (50% duty cycle) with a frequency of 400MHz and peak amplitude of 1A [13], [14]. The noise is injected at P1. Because the links have relatively low loss (short length, small via stub, low data rate), the eyes are all wide open in the simulation even after considering the noise coupling effect. Adding extra power/ground via pairs has little impact on the time domain response, although adding decoupling capacitors increases the vertical eye opening slightly. In case of a very lossy channel, the attentuated signals at the receiver end would become more susceptible to the coupled noise. In that

case, our models would predict that the decoupling capacitors will cause a more significant reduction of low frequency noise.

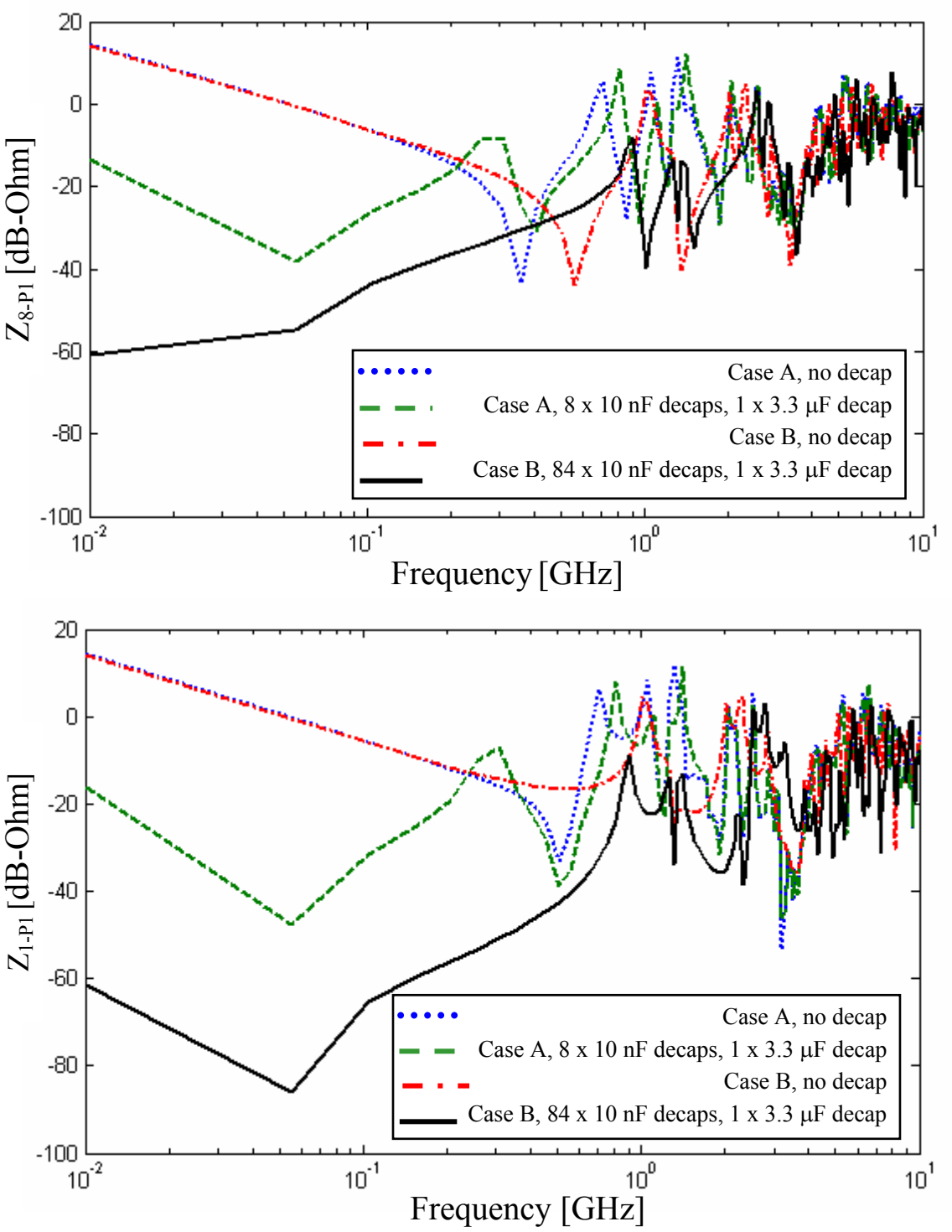


Figure 17. Transfer impedance plots from noise source to signal via ports.

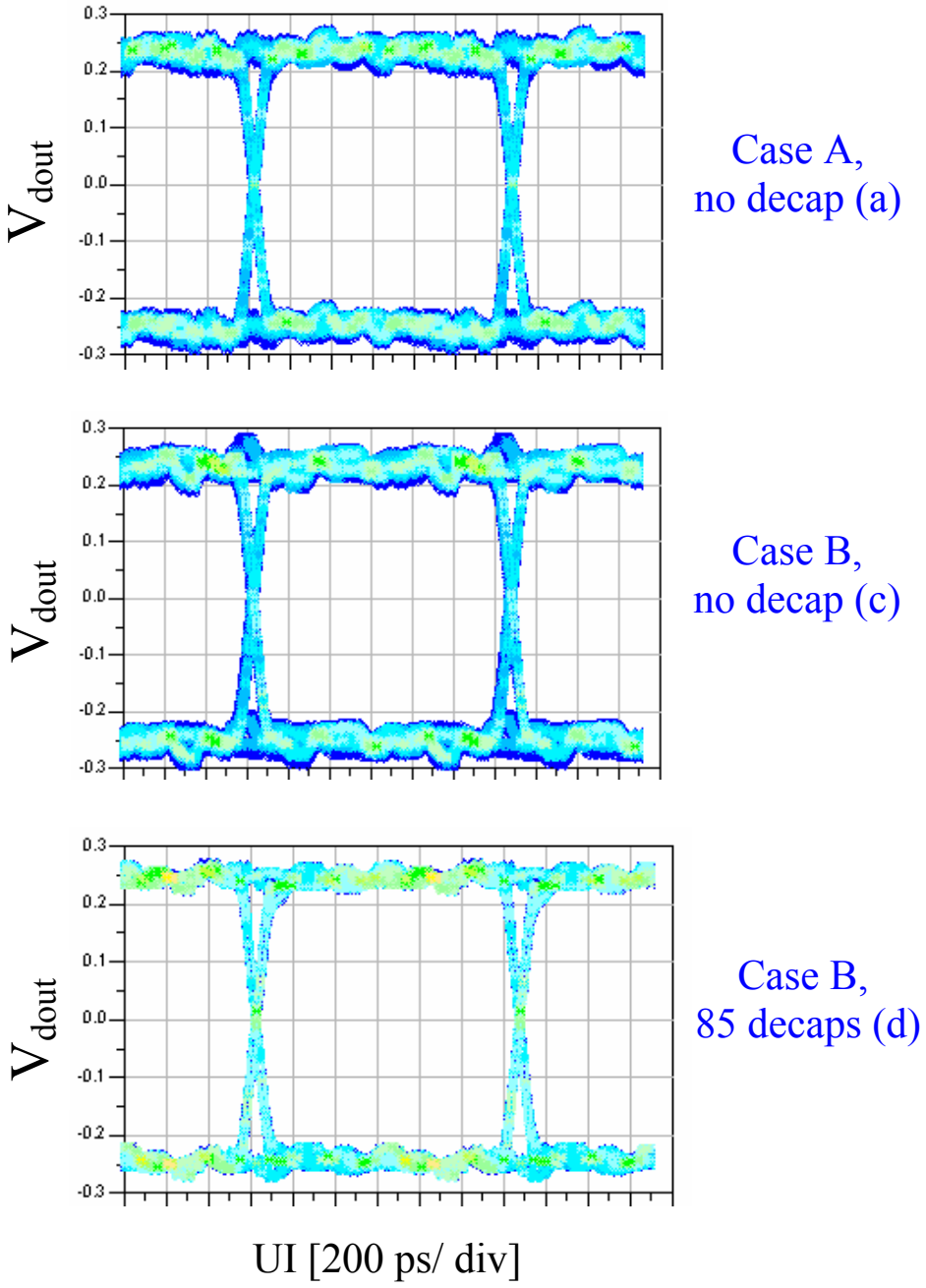


Figure 18. Simulated eye diagrams for the differential link at 0.8Gbps using PRBS_8 pattern with 125ps rise time in ADS®.

5. Conclusions

In this paper, we have extended our physics-based via and trace modeling methodology to now incorporate discrete components, such as decoupling capacitors, based on the joint research efforts between IBM and several universities. We have applied these models to study signal and power integrity performance of real designs including via arrays, high-speed links modeling between BGA fields, PDN noise coupling and decoupling capacitor placement. The models demonstrated good correlation with full-wave simulations and measurements.

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