# DesignCon 2007

# Differential PCB Structures using Measured TRL Calibration and Simulated Structure De-Embedding

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## Abstract

A combined Through-Reflect-Line (TRL) calibration and de-embedding procedure based on measured and computed data for extracting S-parameters of differential structures in multilayer printed circuit boards is presented. The proposed technique starts with measured data using a single mode TRL calibration to remove the coaxial to planar PCB structure and then simulates the planar single-ended to differential structure transition for de-embedding their effect from the measured data. The result is very accurate mixed mode Scattering Parameters (S-Parameters) of the device under test (DUT). This technique is demonstrated on a 4-Port and 12-Port system looking at inter-layer via transitions and shows the benefit of eliminating large multi-port calibration structures.

## Authors Biography

**Heidi Barnes** is a high frequency device interface board designer for Agilent's 93000 semiconductor test system focusing on both digital and analog controlled impedance transition design for full path integrity. Prior to this she was with the Agilent's Microwave Technology Center working with thinfilm, thickfilm, PCB laminate chip and wire, and machined metal packaging technologies for DC to 20 GHz analog and digital applications. She joined Agilent Technologies in 1997 and holds a Bachelor of Science degree in electrical engineering from the California Institute of Technology.

**Antonio Ciccomancini Scogna** is an application engineer at CST of America. He received the PhD degree in electrical engineering from the University of L'Aquila, Italy in 2005, with a dissertation focusing on full-wave simulations and de-embedding techniques for the characterization of PCB discontinuities. In 2004 he received the CST University Publication Award for the use of the FIT technique in signal integrity applications and in August 2005 he joined CST. He is a member of IEEE.

**Mike Resso,** the Signal Integrity Applications Expert in the Component Test Division of Agilent Technologies, has over twenty years of experience in the test and measurement industry. His background includes the design and development of electro-optic test instrumentation for aerospace and commercial applications. His most recent activity has focused on the complete multiport characterization of high speed digital interconnects utilizing Time Domain Reflectometry (TDR) and Vector Network Analysis (VNA). Mike has twice received the Agilent Spark of Insight award for his contributions to the company. He has authored or coauthored over 25 professional publications and received one US patent. Mike received a Bachelor of Science degree in Electrical and Computer Engineering from University of California.

**Ming Tsai** is a staff hardware development engineer for Xilinx in the Product Technology Division. His responsibilities include signal integrity analysis for the high-speed signal transitions, high-speed loadboard design and characterization. He joined Xilinx in October 2004 and earned his Ph.D. degree from the electrical engineering department of University of California, Los Angeles in 1996.

# I. Introduction

In modern digital systems based on high speed interconnection technologies, the correct characterization of discontinuities is mandatory for meaningful signal integrity (SI) analysis [9], [10]. The layout of printed circuit boards (PCBs) involves a large number of discontinuities such as connectors, unusual terminations, bends, presence of packages, via holes, and line crossings (Figure 1). Their presence can cause signal distortion and functional problems for the mounted digital device. The evaluation of the electrical performance of the discontinuities allows high speed digital designers to extract equivalent circuit models that can be included as part of more complex circuits representing the board. Such evaluation, conveniently performed in terms of S-parameters, can be done by means of numerical simulations or by measurements.

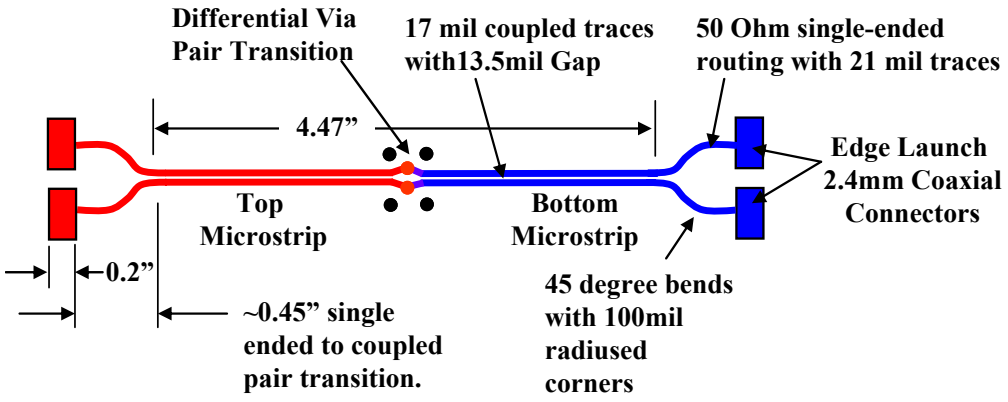


**Figure 1: PCB layout showing the characterization problem.**

Numerical simulations must capture the correct distribution of the EM field in order to take into account all the significant effects due to the discontinuity [1]. In multi-gigabit telecommunications systems this means a high level of detail in the description of the geometry that often requires a significant amount of CPU resources and simulation time. Obtaining measured data provides an excellent calibration point to verify a complex model and insure that it accurately represents a structure before significant time is spent on optimization for a specific application.

On the other hand, from a measurement point of view, it is generally not possible to gain access to the structure without impacting performance data. An example of this phenomenon is the experimental characterization of a via hole (Figure 1) in which the presence of feeding parts (traces, adapters or pads) connecting the instrument’s ports to the DUT via must always be present. To overcome the above mentioned difficulties it has become standard practice to characterize the effects of the test access ports by feeding lines or adapters and then to separate them from the measurement relative to the complete structure. The remaining data are those associated with the electric behaviour of the DUT

or discontinuity of interest. This procedure is known as de-embedding. In recent years, a number of de-embedding methods have been reported in the literature and their references give useful hints for combining simulations and measurements [2].

A customized single-mode TRL (Thru-Reflect-Line) calibration is one method of providing error correction to remove the launch connector effects when compared to the network analyzer coaxial calibration that just calibrates to the end of the connecting coaxial cable (Figure 2). However, a simple single mode 2-port TRL calibration does not take out the effects of transitioning from single ended microstrip to differential microstrip routing for a differential structure. Fabricating a 4-Port differential mixed mode TRL structure is feasible [3], but one quickly sees the increase in board area and measurements that it will require. A 4-Port differential mixed mode TRL also requires additional mathematics to handle the odd and even modes of propagation found in coupled differential lines when implementing the TRL algorithm. Expanding to a 12-Port differential TRL structure has thus far proven to be challenging due to the complexity required.

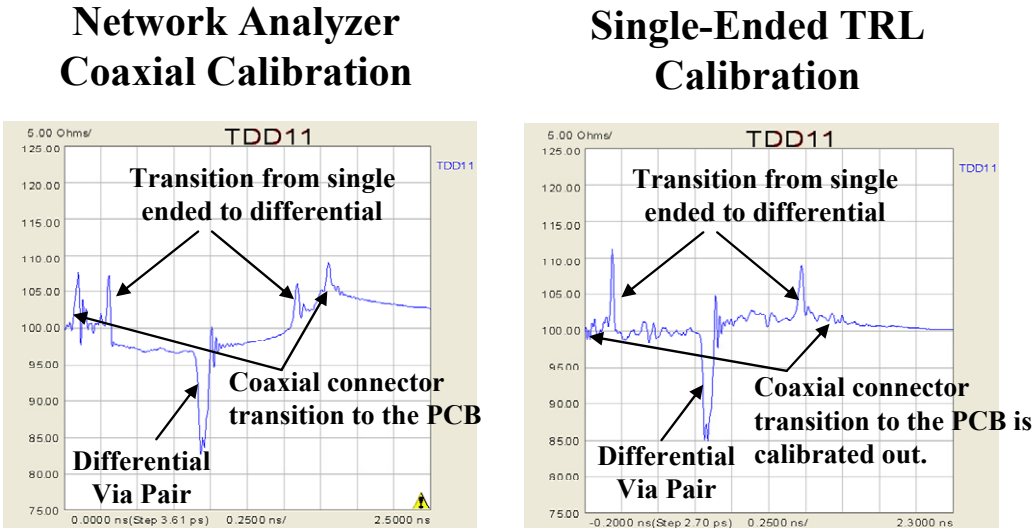


**Figure 2: TDR results comparing a Network Analyzer coaxial calibration versus a Single-Mode TRL calibration for the coupled differential via pair structure in Figure 1. The TRL calibration removes the connector discontinuity, but not the effect of transitioning from single-ended to differential transmission line routing.**

The present paper will show how relying on a single mode TRL calibration to remove connector effects and then how the de-embedding of simulated single ended to differential coupled pair transitions is an effective calibration technique for N-Port systems. The technique will be demonstrated by obtaining the S-parameters of passive differential inter-layer PCB via transitions when used in 4-Port or 12-Port routing topologies. Section II describes the justification for this technique, Section III describes the single-ended TRL, Section IV describes the simulated de-embedding structure, Section V looks at a DUT via structure for analysis, Section VI looks at verification of this calibration technique with the mixed-mode 4-Port TRL, and finally Section V concludes with the S-Parameters for a 12-Port via structure measurement.

# II. Combined TRL Calibration and Simulated Structure De-Embedding for Multimode N-Port Systems

Obtaining accurate S-Parameter data for a 2-port, 4-port, or N-Port system using a Network Analyzer requires cabling and connectors to launch the signal into the structure under test. The three dimensional (3D) properties of launching from a coaxial cable onto a planar PCB are defined by numerous mechanical and material tolerances on the mating connectors and PCB fabrication that can make accurate 3D-Electromagnetic (EM) modeling a difficult task. The utilization of a TRL calibration structure fabricated with the same process as the structure to be measured accurately represents this transition feature and allows the TRL calibration to calibrate out this transition discontinuity from the measurement. Taking a look at the simple single-ended microstrip structure of Figure 3 one can excite the structure with a 10Gbps PRBS31 signal but the results will include the whole structure including the coaxial connector transition to PCB.

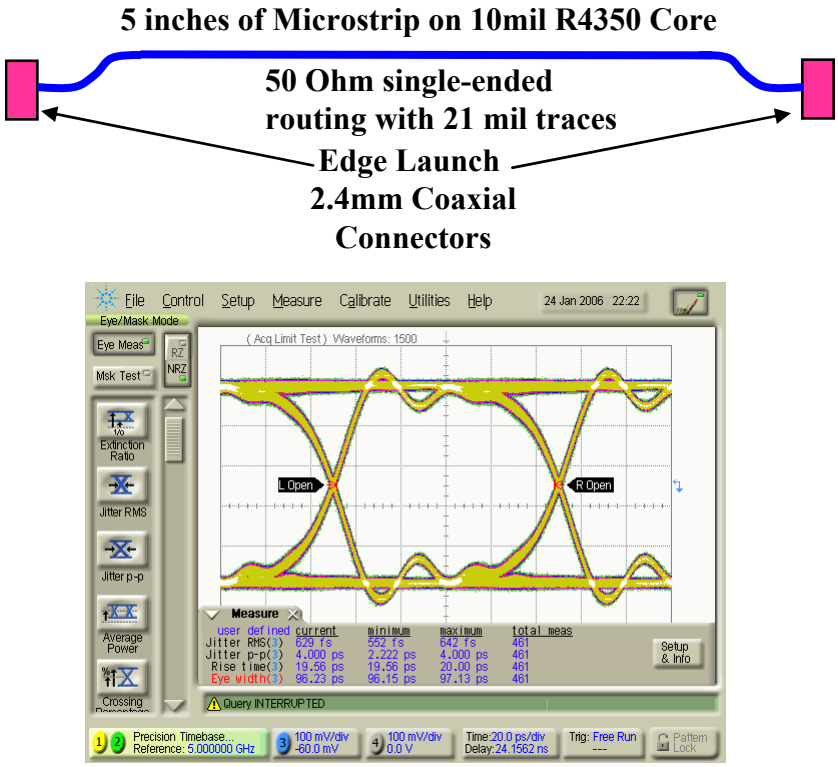


**Figure 3 - Single Ended microstrip transmission line and measured data using a 10Gbps PRBS 31**

Applying a single-ended TRL calibration to remove the coaxial connector transition provides the S-Parameters of just the transmission line which can then be used to generate a resulting eye diagram that does not include the connectors as seen in Figure 4. Comparing the eye diagram for these two types of calibrations clearly shows that the edge connectors increase the amount of jitter and ripple.

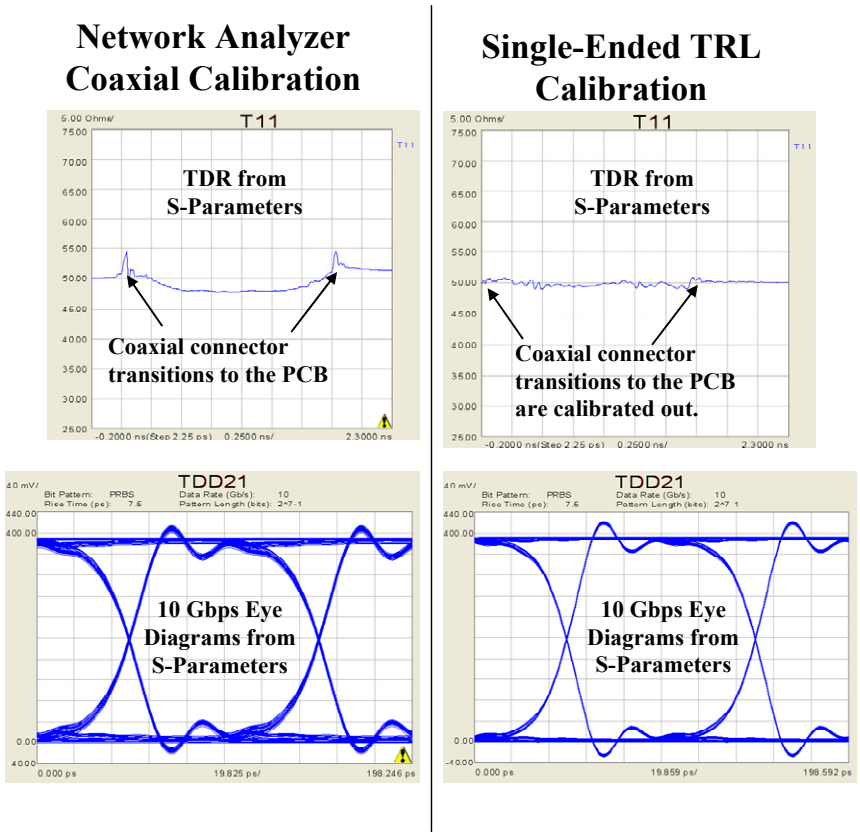


**Figure 4: Network Analyzer coaxial calibration vs single-ended TRL results for the microstrip trace in Figure 3.**

The TRL calibration is a well utilized technique for single-ended structures but as the number of ports increase for N-Port systems the physical space required for the connectors and routing can quickly become cost prohibitive for layout and materials as well as the increased test time to make all of the connections for an N-Port mixed mode calibration. Faced with this challenge one looks for a different approach and realizes that the transition from single ended planar transmission lines to differential or n-port coupled planar transmission lines is a relatively simple structure to model with existing 2D or 3D EM simulators. In this way accurate S-parameters of the planar transitioning structure can be obtained and used within de-embedding techniques to remove their effect from the measurement, so that one is left with the S-parameters of the desired N-Port structure under test.

Applying this technique to a 12-port system quickly shows the benefit. Figure 5 illustrates an example of a structure that routes 3 stripline differential pairs through a PCB via structure to another layer. The goal is to obtain a full set of 12-port S-Parameters so that this component can be used as a part of a model library for PCB design and analysis that will include the affects of crosstalk with neighboring differential pairs. A secondary item of interest is to obtain high frequency performance of the structure so that a time domain response of the structure can be used for verification of 3D-EM simulations and additional tuning of capacitive and inductive elements.

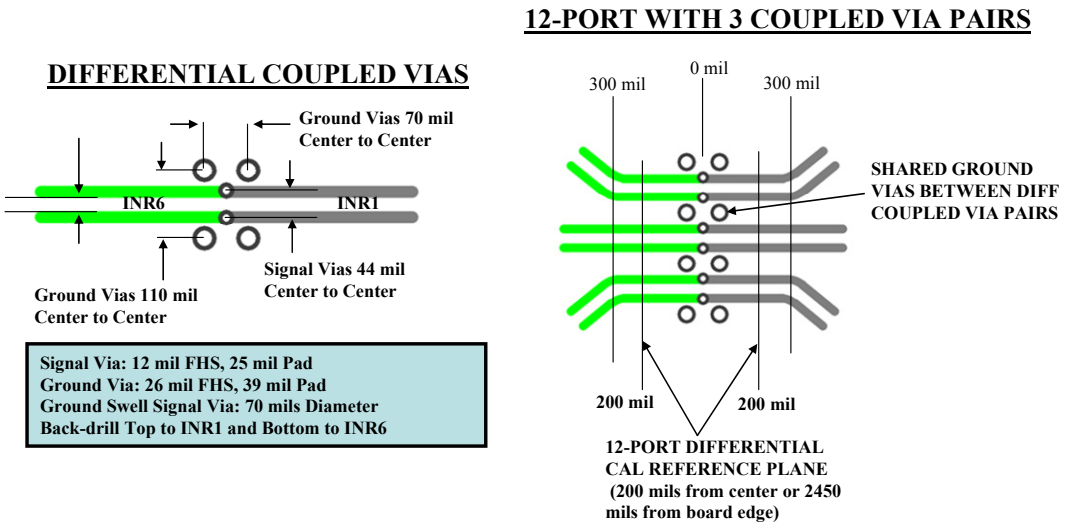


**Figure 5: 12-Port Differential Via Pairs for the DUT structure.**

To achieve the high frequency data on this structure a 2.4 mm coaxial connector is selected for use with a 12-port 50GHz Agilent Physical Layer Test System so that reliable and accurate coaxial calibration standards can be used. This test system consists of a 2-port 50GHz E8364B Vector Network Analyzer and a 10-port U3025AE10 10-port 50 GHz test set. This aforementioned 2.4 mm connector is significantly larger then the via structure under test and thus requires a large area of routing to get from the connectors down to the small structure under test. This feeding line structure is represented in Figure 6 and it clearly shows the large area required by the connectors as compared to the structure under test.

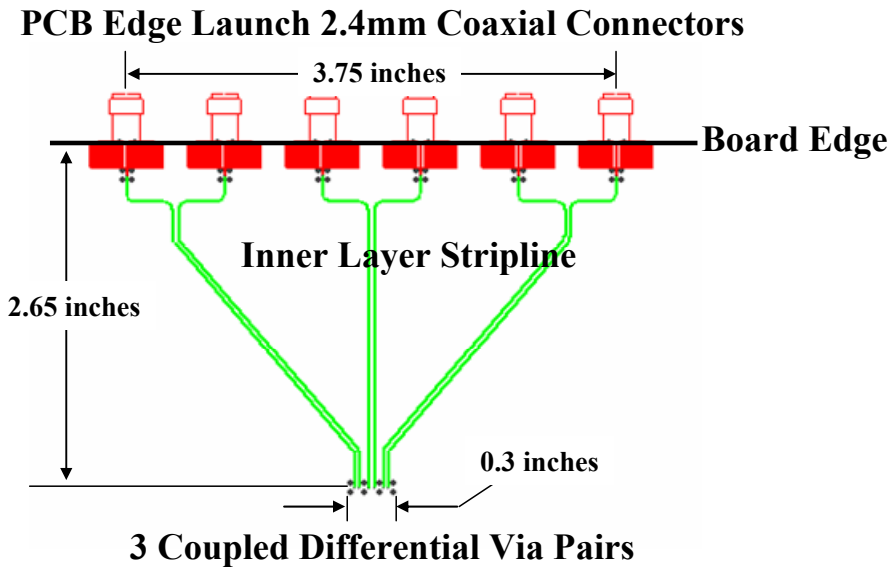


**Figure 6: 12-Port feed line routing to get from coaxial connectors to the via structure under test.**

The justification for utilizing a single-ended 2-Port TRL with 12-Port simulated structure de-embedding quickly becomes clear looking at this structure and comparing the resources that would be required for a 12-Port calibration. The edge connectors alone for a 12-Port TRL would take close to 4 feet of board edge space and if one was to use a 2-port network analyzer for the 12-Port TRL it would take 672 coaxial connections just for the calibration. The 2-Port TRL with simulated structure de-embedding may not be as accurate as a 12-Port mixed-mode TRL, but with only 12 connections required for calibration of a 12-port system it is a very practical approach.

| Calibration Technique | 2-Port TRL Cal 4-Lines | 4-Port TRL Cal 4-Lines | 12-Port TRL Cal 4-Lines | 12-Port with 2-Port TRL and Simulated Structure De-embed |
|---|---|---|---|---|
| Number of Connector Footprints | 11 | 22 | 66 | 11 |
| 2-Port Network Analyzer # of Connections | 12 | 44 | 672 | 12 |
| 4-Port Network Analyzer # of Connections | 12 | 24 | 312 | 12* |
| 12-Port Network Analyzer # of Connections | 12 | 24 | 72 | 12* |

***Assumes all ports are equal after VNA cal and applies characterized standards for TRL de-embedding on all ports using one set of 2-port TRL Calibration measurements.**

**Table 1: Simple comparison of coaxial connector connections to be made for 2, 4, and 12 port TRL calibration with 4 line lengths vs that of the combination TRL and simulated structure de-embed calibration. Assumes network analyzer coaxial calibration has been performed.**

## III. TRL Calibration Structures and Measurement Technique

The Through-Reflect-Line (TRL) calibration technique has a long history of use with wafer probing for device characterization where it is necessary to calibrate out the effect of the probes using a TRL calibration [5], [6]. The technique provides accurate full two port calibration of a Vector Network Analyzer by employing an 8-term error model for a complete analytical derivation of the error terms. The TRL utilizes three types of standards starting with the zero length through line where all the S-Parameters are known, an open or short for a high reflect condition, and a non-zero through line with the length chosen so that the frequency of interest has from 20 to 160 degrees of phase rotation over the length of the line. This means that for a wide band calibration one will need multiple non-zero length through lines for complete coverage of the required

frequencies. The through lines should also be used in a frequency ratio of 1:8 to allow for enough phase margin in the solution (frequency overlap between bands)

When designing a TRL structure for a printed circuit board one must consider things like repeatable connector performance and attach methods to get from the network analyzer coaxial connector to a planar structure, optimized discontinuities to reduce mismatches and reduce calibration errors, selection of routing feed lines that match the DUT of interest, and long enough structures to reduce radiation cross-talk errors. Significant effort has also been put into analyzing microstrip and stripline routing structures, and it has been found that the etching consistency, shielding, and dielectric uniformity of the stripline routing structure has some significant benefits over that of microstrip for the TRL standards. The other reality is that with the existing applications (that use high density BGA's), it becomes impossible to route everything on the top and bottom microstrip layers, therefore stripline structure quickly becomes the preferred feedline routing to a DUT.

The 12-Port via structure of Figure 5 has been designed to transition from one inner layer to another and thus requires a via transition to get to this inner layer from the coaxial connector. Since the via is also sensitive to numerous board fabrication tolerances including layer to layer alignment, drill placement, and etching it has been placed next to the edge launch connector so that the TRL calibration can calibrate out these effects. Figure 7 shows the topology for the single-ended launch structure using a very repeatable 2.4 mm edge launch connector to PCB with an optimized via transition to a 19 mil inner layer stripline.

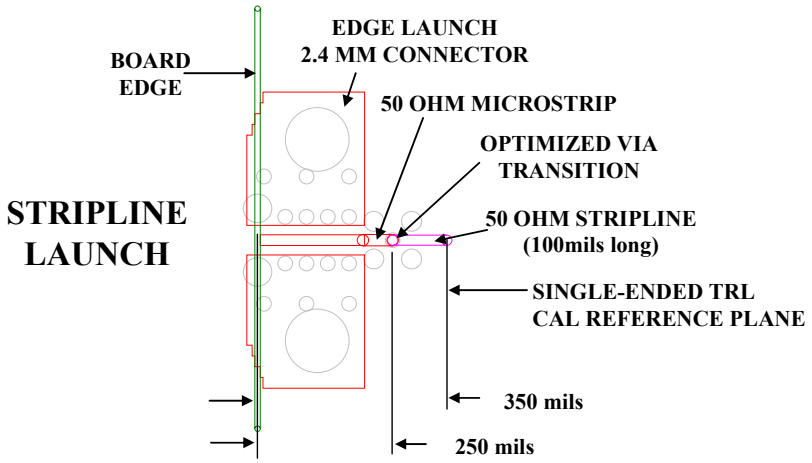


**Figure 7: Single Ended Launch to Inner Layer Stripline**

Putting this altogether, it results in the following line lengths and structures for the single-ended TRL calibration. The Through structure just uses two back to back structures of the launch in Figure 7 for a zero length line. The Reflect structure uses an open since this is easier to implement than trying to get low inductance vias correctly located at the extended port TRL calibration reference plane. The non-zero line lengths require 4 different lengths to cover the broadband 100MHz to 40 GHz range needed for detailed

time domain analysis of the DUT using measured S-parameters. Additionally, a frequency ratio of 1:7 was selected for the line's start frequency to its stop frequency so that the phase rotation will stay within the required 20 to 160 degrees for the start to stop frequencies of the line. Line lengths are calculated based on the Agilent 8510 Network Analyzer Product Note 8510-8A [7].

| TRL Structure | Start Frequency | Stop Frequency | Line Length |
|---|---|---|---|
| **Line 1** | 85 MHz | 595 MHz | 4,600 mils |
| **Line 2** | 0.35 GHz | 2.45 GHz | 1,300 mils |
| **Line 3** | 1.55 GHz | 10.85 GHz | 250 mils |
| **Line 4** | 10 GHz | 70 GHz | 40 mils |

**Table 2: Single Ended TRL Line calibration structures with a frequency range and eletrical length based on the propagation velocity in R4350 with a dielectric constant of 3.48.**

## IV. Simulated 4 -port and 12 -port De-Embedding Structure

The use of 3D-EM simulation tools to obtain the S-Parameters for the feed line routing from the single-ended launch (depicted in Figure 7) to the DUT structure of interest can be a reasonably quick task due to the import capability of most modeling tools. Either Autocad dxf style CAD drawing data or PCB Gerber files can be used to import the exact trace shape that is being used to route from the single-ended launch to a mixed mode stripline structure. The import feature can minimize the modeling time and avoid errors which can occur when manually drawing complex geometries. The most common error source in full-wave modeling is the incorrect description of the geometry and this happens if the geometrical dimensions are wrong or some crucial details have been simplified.

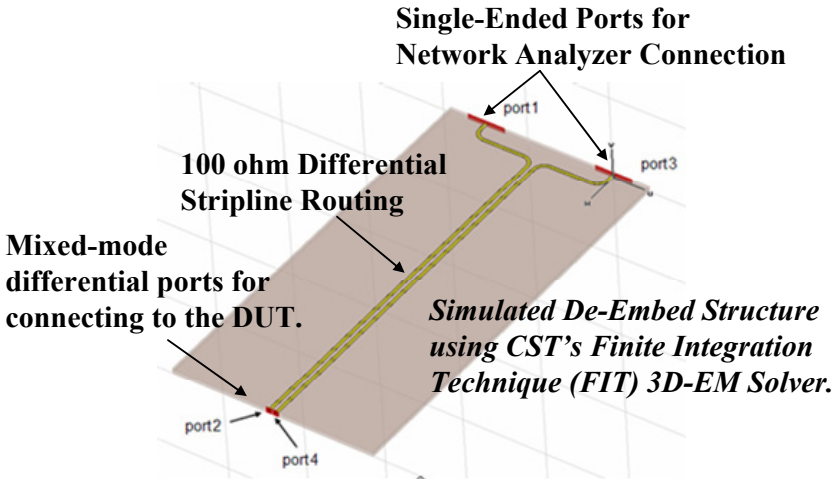


**Figure 8: Example 3D-EM model of a feed line structure for connecting from the single-ended TRL reference plane to the DUT.**

The S-parameters from the modeled structure can then be de-embedded from the measured data to provide full S-Parameters for the DUT structure [1], [2]. A simple stripline de-embed structure is illustrated in Figure 8.

De-embedding is a mathematical process that removes the effects of unwanted portions of the structure that are embedded in the measured data by subtracting out their contribution. The de-embed mathematics relies on the ability of S-Parameters to be converted into a T matrix which has the following relationship

$$T_{TOT} = T_A T_{DUT} T_B \quad (1)$$

From the previous, by inverting the matrices $T_A$ and $T_B$ it is straightforward to obtain

$$T_{DUT} = T_A^{-1} T_{TOT} T_B^{-1} \quad (2)$$

The $T_{DUT}$ matrix can then be converted back to S-Parameters for cascading together with other structures in order to predict the performance of a full path with multiple routing structures.

The loss of the simulated transmission line structure will depend on the board fabrication process used and the final structural dimensions. Accurately capturing trace edge features, plating thickness, line widths, dielectric thickness, and conductor surface roughness to name a few is not always a practical task. A simplified method of using the longest TRL calibration through line measurements to establish the impedance and loss of the coupled stripline routing will provide the necessary reference point to tune the loss of the simulation and improve the accuracy of the final de-embed structure.

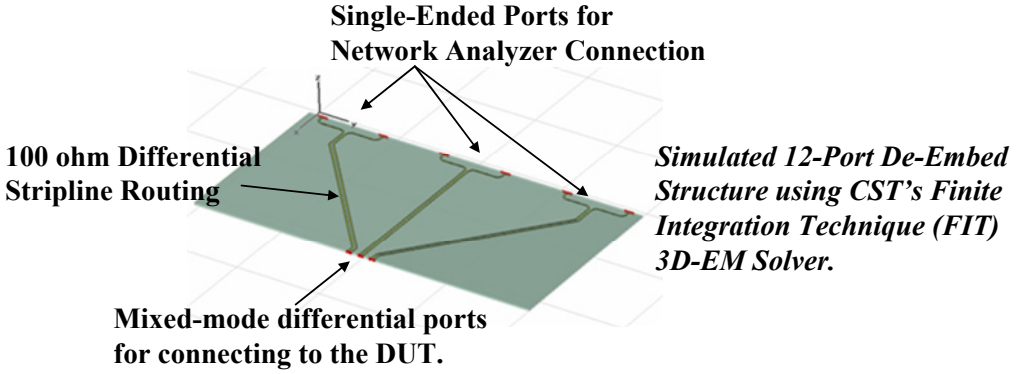


**Figure 9: 12-Port De-Embed structure showing the flexibility in routing to the DUT from the larger coaxial connectors.**

Figure 9 shows how the feed lines can be routed from the large coaxial connectors to the differential ports on a DUT structure. One of the main benefits of the simulated 12-Port de-embed is that it provides significant flexibility in the routing of the feedlines. A full 12-Port TRL would require that the feedlines for all DUT structures being measured use

the same routing path to feed into them, however, this is not always practical due to layout space constraints or changes in physical size of the DUT structure. The simulated 12-Port de-embed feed line routing can easily be adjusted to match the specific DUT structure and allow one single-ended TRL standard calibration to be used for a variety of DUT structures and board layouts.

## V. Device Structure under Test: Coupled and Un-Coupled Via Pairs

Numerous papers have been done on the modeling of via transitions for PCB layouts to fulfill the growing need for high frequency performance [1], [8]. Most papers deal with single-ended via transitions, a few with differential coupled via transitions, and very few if any deal with obtaining calibrated mixed-mode S-parameters for the via structure. A poorly designed via can quickly become a well designed low pass filter that if one is not careful can block the higher frequencies and significantly reduce rise times of a digital signal. Via performance optimization can be tuned using TDR techniques [8] to understand what portions of the structure are capacitive or inductive. Tuning of features can easily be done with a 3D-EM solver, but one must have at least one accurate measured data point on a representative structure so that a 3D-EM model can be verified before extensive time is put into optimization using the simulator.

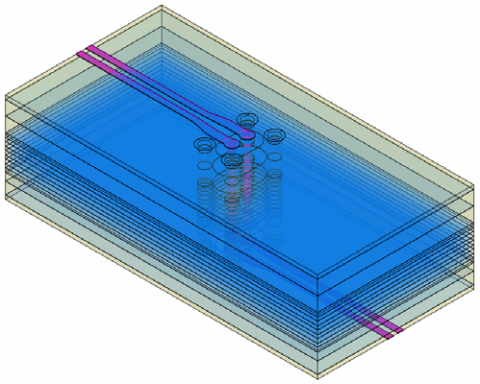

**Figure 10: 3D-EM structure modeling can benefit from validation with measured data prior to extensive time spent on optimizations.**

In the case of differential signals, it becomes slightly more complex in that now one has to work with the single ended and differential impedances. It has been shown that the S-Parameters can easily be converted to a reciprocal mixed mode S-Parameter matrix that shows the differential behavior of a pair of transmission lines [11]. Comparing the results (Figure 11) of the single-ended common mode performance with that of the differential quickly shows that any tuning or optimization must be done with the differential performance since the benefit of coupling can improve the performance of the differential mode.

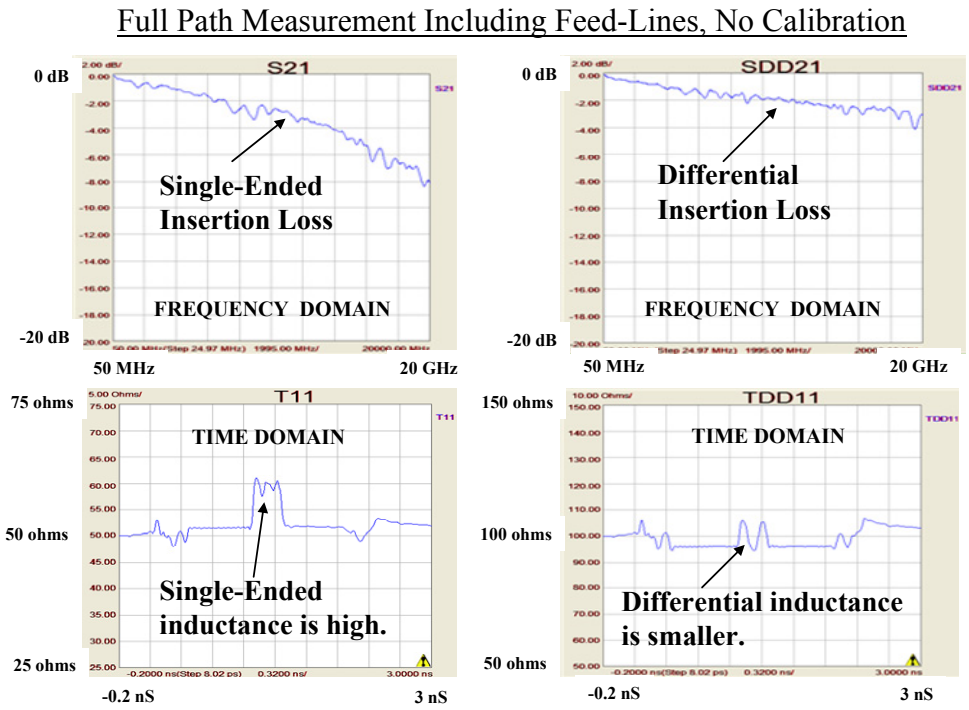


**Figure 11: Single-ended vs mixed mode S-Parameters for the full-path structure of Figure 1.**

The via structure of Figure 5 with the neighboring differential via pairs for NEXT/FEXT crosstalk measurements becomes significantly more complex to model with a 3D-EM solver and must rely more on measured data. One approach is to optimize the differential via pairs as separate structures before bringing them together in a NEXT/FEXT coupling proximity. The full-path DUT structure for 3 different via pair topologies has been fabricated on a R4350 test board and measured data exists for these 3 DUT structures. The first of the 3 via pair topologies is what it has been shown in Figure 10 and used in the simulated full path of Figure 11.

## VI. Verification Using 4-Port Multimode TRL Calibration

With the ever increasing frequencies for digital communications the need for accurate calibration of mixed-mode differential structures arises. It has been shown that the single ended TRL can be modified to accommodate the coupling of a mixed mode structure and provide a calibrated measurement of the DUT [3]. The design of a 4-Port mixed mode TRL structure is similar to the technique described for the single-ended TRL in Section III with the added requirement that the phase rotation remain between 20 and 160 degrees for all modes. The validity of this 4-Port mixed-mode TRL has been demonstrated [4] and is an excellent way of checking the performance of the simpler single mode TRL with simulated structure de-embedding that is being presented in this paper.

The fabricated mixed-mode TRL structures will have the topology shown in Figure 12. This structure uses the same launch as the single ended TRL structure so that one can use either calibration method when looking at a full path measurement.

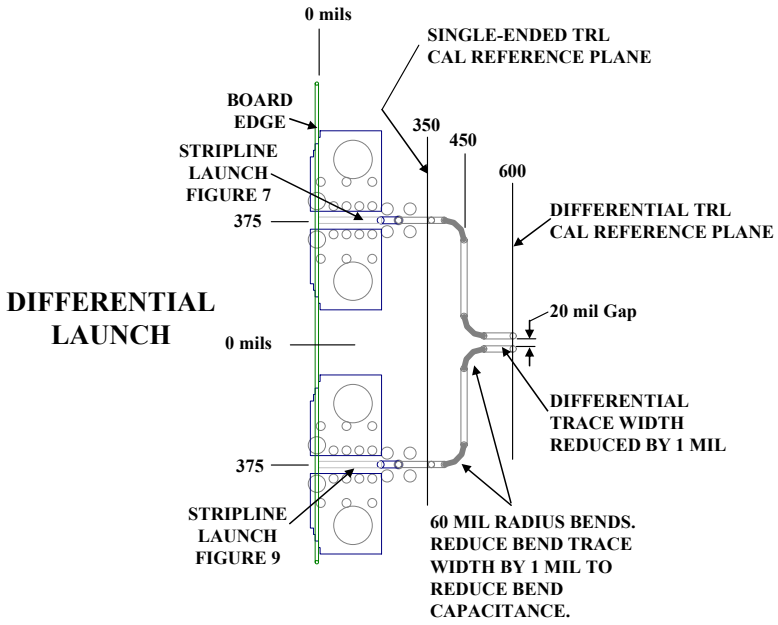


**Figure 12: Differential Launch to Coupled Inner Layer Stripline – 4 Port**

The line lengths for the mixed-mode TRL Lines are shown in Table 3.

| TRL Structure | Start Frequency | Stop Frequency | Line Length |
|---|---|---|---|
| **Line 1** | 95 MHz | 665 MHz | 4,100 mils |
| **Line 2** | 0.5 GHz | 3.5 GHz | 800 mils |
| **Line 3** | 2 GHz | 14 GHz | 200 mils |
| **Line 4** | 10 GHz | 70 GHz | 40 mils |

**Table 3: Mixed-mode TRL Line calibration structures with frequency range and electrical length based on the propagation velocity in R4350 with a dielectric constant of 3.48.**

To insure that the methodology works mathematically, one can start with simulated TRL structures, connector S-Parameter data, and modeled DUT via performance to create a full path structure (Figure 13). Running the mixed mode TRL algorithm should result in getting back the via data that one started with and the same is true for de-embedding the connector and feed lines with the simulated structure de-embedding to get back to the via structure S-Parameters.

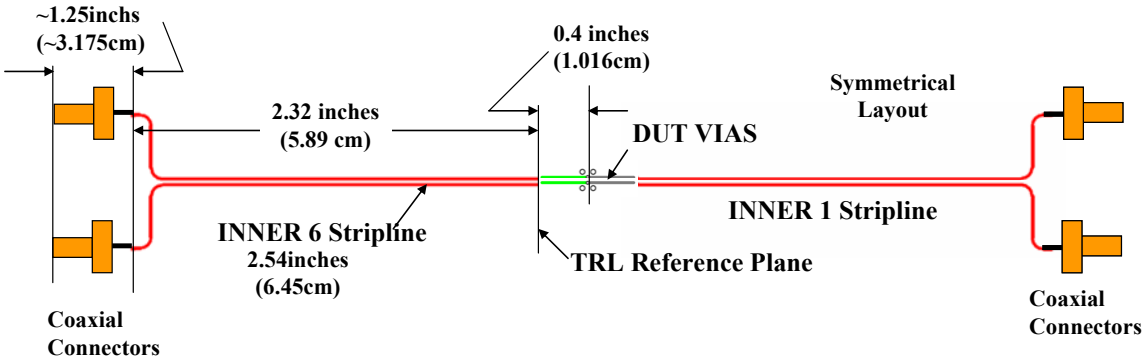


**Figure 13: Simulated full-path structure and data for verification of the de-embedding and mixed-mode TRL algorithms.**

Running this simulated comparison (Figure 14) shows that the technique is valid; however care must be used in verifying the correct characteristic impedances when implementing the algorithms. This comparison quickly shows that the TRL through line would benefit from being increased in length so that the TRL reference plane is further from the transition from single ended to differential pair routing. When the transition fields are not allowed to settle, then it results in the through line path not having the same characteristic impedance as the longer lines. The final application of comparing measured mixed-mode TRL structures with that of the simulated structure de-embedding will be done once the fabricated structures become available.

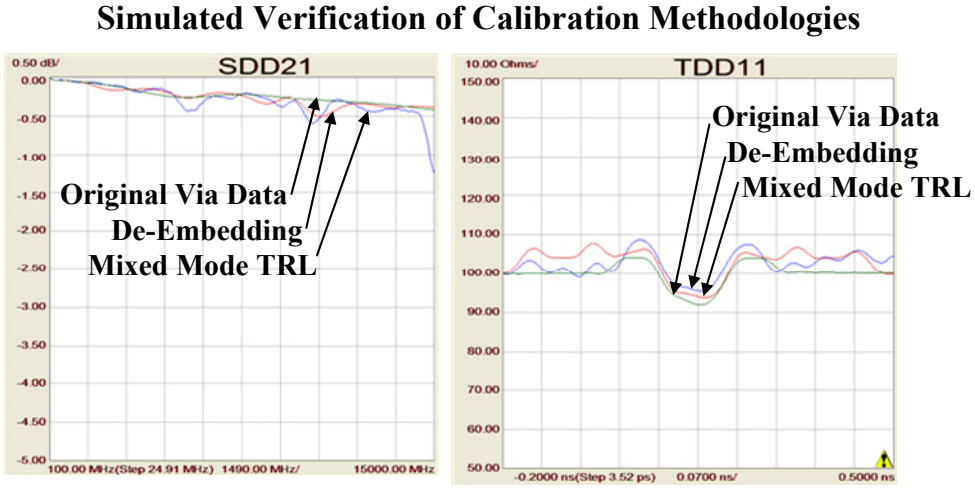


**Figure 14: Simulated differential SDD21 to 15GHz and time domain TDD11 verification of the mixed-mode TRL and single-ended TRL with simulated feed-line de-embedding. Variations in the mixed-mode TRL show that the TRL structure through line is not long enough for the single ended to differential fields to settle resulting in a characteristic impedance that is different from that of a longer line.**

# VII. Demonstration of the Combined TRL Calibration and Simulated Structure De-Embedding Technique for Multi-mode N-Port Systems.

The final set of calibration boards are still in progress for the structure of Figure 6 for looking at NEXT/FEXT crosstalk issues, but as mentioned in section V it is still very interesting to look at three separated via pairs to obtain their individual S-parameters.

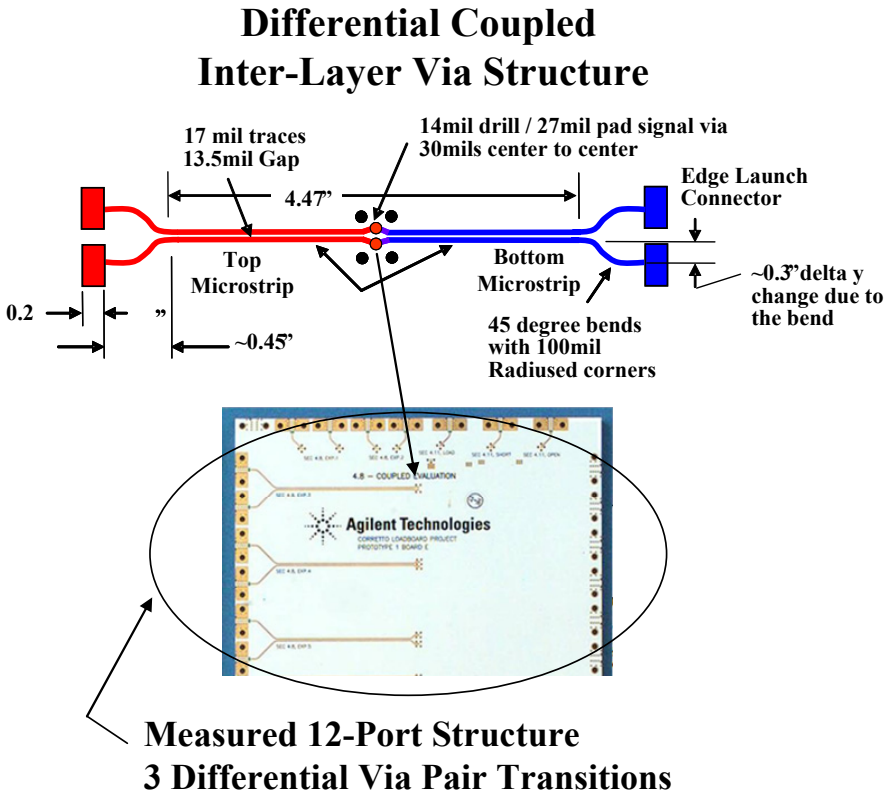


**Figure 15 : Differential Via Experiments and TRL Calibration**

Although TRL data is not yet available for the single-ended connector topology of this board, one can get close to implementing this same technique by probing a measurement of the connector for use with mathematically de-embedding its contribution from the full path measurement. This is not as accurate as the single ended TRL, but it is a very flexible method when one does not have access to TRL structures for the topology of interest. The S-Parameters for the connector can be seen in Figure 15 and the feed line topology for de-embedding is illustrated in Figure 17.

The simulation of the feed-line structure in Figure 17 proved to be a bit more troublesome than expected due to the use of the microstrip routing. The microstrip routing for a large scale DUT loadboard application utilizes 50 micro inches of Au over 200 micro inches of Nickel plating on top of 2 mils of plated up copper on the outside of the board. The etching variations and the mushroom shaped edge affects of this style of microstrip resulted in a far more complex modeling problem. The final calibration

structures that are in the process of being fabricated will use stripline feed-line routing to provide a much simpler structure for modeling and de-embedding. The topside plating issues will be calibrated out in the single-ended TRL calibration to remove the connector transition and the via transition to inner stripline so that modeling of these variations can be avoided.

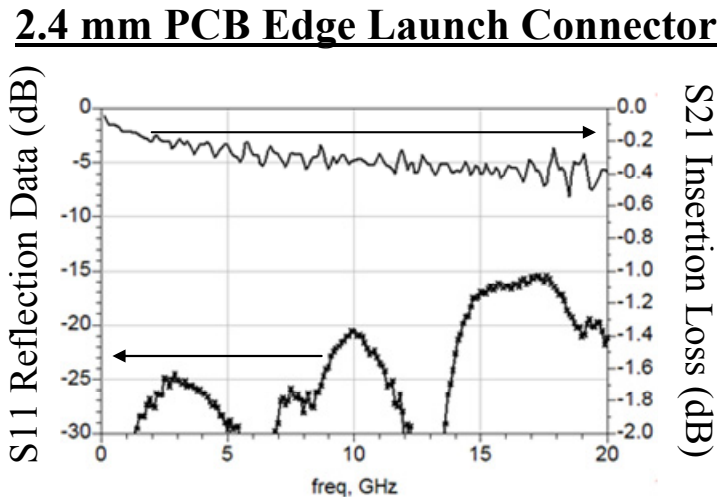


**Figure 16: S-Parameter data for the Southwest 2.4mm PCB edge launch connector using *GigaTest Labs* probe measurements.**

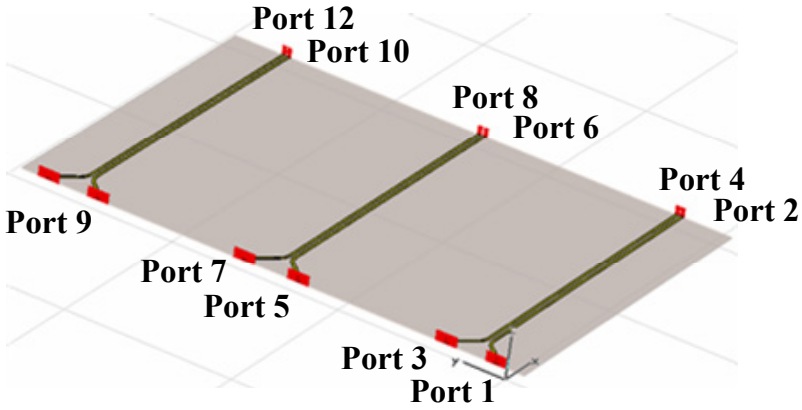


**Figure 17: Simulated 12-Port de-embed microstrip structure.**

Applying this technique to the existing microstrip structures of Figure 15 demonstrated the importance of choosing stripline routing paths to implement this single ended TRL calibration with simulated feed line de-embedding. The use of microstrip feed-lines would require additional work to correctly account for plating and etching affects in the simulated structures. The final application of obtaining 12-Port S-Paramaters for coupled via pairs will be done once the fabricated stripline structures become available.

## VIII. Summary and Conclusions

The methodology outlined in this paper demonstrates one of the few practical approaches to calibration of mixed-mode differential pairs for 12-Port systems. The high number of connectors and connections required for a full 12-Port TRL make this a tedious task that quickly benefits from a reduction in the number of connectors and connections at the expense of some loss of precision. The selection of a single-mode TRL structure for de-embedding the coaxial to planer connector launch and any via transitions to inner layers is an efficient way of accounting for PCB fabrication tolerances that are often difficult to determine for an accurate 3D-EM simulation. The use of a simulated N-Port planar feed-line structure to transition from the single-ended routing to coupled mixed-mode routing is a simple task for a 3D-EM simulator and provides the necessary mixed-mode S-Parameters for de-embedding this structure from the single-ended TRL calibrated full path measurement. The single-ended TRL structures also provide the necessary through line loss information for additional tuning of the simulated N-Port de-embed structure for a particular as fabricated PCB.

The increased complexity of multiple transmission lines with the desire to look at NEXT/FEXT crosstalk affects requires accurate S-Parameters for use as components in a model library for fullpath simulations. This paper has presented a practical solution for obtaining these S-Parameters using a combination of single-mode TRL with simulated N-Port feed-line de-embedding to achieve an N-Port calibration for measuring an N-Port structure.

## Acknowledgements

The authors would like to thank the cooperation between Agilent, Verigy, CST, and Xilinx to make it possible to bring multiple simulation products together to verify the validity of this technique. Key contributors include Jose Moreira of Verigy for the inspiration and funding to make this paper possible, Bob Schaefer of Agilent for the Physical Layer Test System (PLTS), Sanjeev Gupta of Agilent Eesof EDA Division for his technical guidance and assistance with ADS simulations, Yoshio Akashi of Agilent for his Multi-Mode TRL calculations, Orlando Bell of Gigatest Labs for connector probe measurements and 12-Port measurements, Will Burns at Altanova for PCB layout, and Morgan Culver of Agilent for high quality time domain measurements.

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