Next Progression in Microvia Reliability Validation–Reflow Simulation of PCB Design Attributes and Material Structural Properties During the PCB Design Process

Gerry Partida
Summit Interconnect

Abstract

As has long been known, each time there is a step up to the next level of PCB technology, the industry is faced with new or the broadening of existing challenges. Today, this is particularly true of microvias. Once relegated to a small segment of PCB designs, microvias, and their reliability, are a growing factor within today's designs.

This paper will provide an overview of the history of microvias, the challenges associated with the failures of them and the ways in which they can be proactively predicted and addressed during the early stages of the design process.

A Bit of History

In order to understand how best to address the failures of microvias, it's useful to go back into history. And, in particular, to start with the test method process.

Historically, PCB fabrication and delivery of finished products preceded test methods to validate the finished PCB. In the 1970s, PCBs were fabricated and shipped without electrical test (ET) validation. At the beginning of the 1980s, electrical testing became standard and a requirement for all but the simplest products. For the next decade, PCBs were built by using "Golden" board programming. The Golden board method used a finished PCB from a finished lot of boards, and it was placedon a test fixture by an operator who would then initiate a self-learned shorts and opens program from the board. If the secondPCB matched the first, a Golden board was established. One of the short comings of the Golden board testing was that it was susceptible to missing the errors in the fabrication data that had been supplied. This method would also allow for CAM errors to go undetected up to assembly. A solution finally came about when CAM and net list compare was made available in the late 1980s. In this process, software was used to validate the received data before fabrication started and then the same software was used to generate an ET program to validate the finished PCB. This method saved product cycle time, prevented the loss of material, and saved manufacturing time at both the PCB fabrication and assembly levels.

Today the industry is facing a similar challenge with microvia reliability especially after reflow of the PCB at assembly, during rework or operating in the field. As with the short comings of electrical testing in the past, the industry designed PCBs with microvias without evaluating the thermal properties of the material or the geometries in the design. Fabricators produced the finished goods and evaluated the finished PCB to established performance standards such as IPC-6012. When difficult to detect failures occurred post assembly, a test method IPC-TM-650 2.6.27 was established and a caution was added to the IPC-6012 rev E in section 3.6, Structural Integrity. The testing of a D coupon via IPC-TM-650 2.6.27 did validate that the finishedPCBs were safe for assembly, but it did not stop a fabricator from building a bad design. Until now, there was not a method to simulate a PCB design that validated that the material selection, dielectric thickness, microvia size, and configuration (single, stacked or staggered microvias) could survive 6X reflows. As with the evolution of electrical test and the use of the software to validate the design and the final test, we now have software that will validate the structural integrity of a microvia in a design during PCB stackup before a design has been approved and placed into the fabrication process. This new software provides the industry a way to validate the design, fabricate a microvia design with confidence, and validate that the PCB has meet the structural requirements by testing to IPC-TM-650 2.6.27. This paper will demonstrate real cases where validation software has identified structural issues with a microvia design and how this software can provide modification of the PCB design geometries that will result in a working stackup.

Microvia Failure Location: In the Target Pad and Plated Microvia Interface

There have been many studies regarding microvia failures. In this document, the focus is not on the location of the failure but instead elaborating on the mechanics that initiate microvia failures. The goal is to show how our industry can now plan and prevent microvia failures in a finished PCB by planning and validating a stackup at the layup stage and then simulating how that PCB can survive 6X reflow cycles when the fabrication process has been completed.

Presented and published for the 2022 IPC Apex Expo Technical Conference – San Diego, CA

To date, many different studies have identified that microvias are weakest at the electroless copper interface. Electroless is deposited over the microvia and lies between the target pad and the electroplated microvia. In most cases, the failed microvia is found in the electroless at the bottom of the single microvia and almost always at the bottom of stacked microvias.

Improvements in electroless copper have been made and they have improved microvia reliability. The new advanced electroless chemistry can demonstrate that epitaxy and bottom-up recrystallization can occur between the target pad and the electroplated microvia. Studies have shown that direct metallization, which does not use electroless, also achieves epitaxy and bottom-up recrystallization. In both cases, reflow testing demonstrates improved microvia reliability, but these structures can still fail and not meet 6X reflows with resistance changes less than 5%.

The question arises as to why are microvias weak. They are not but simply put, microvias are butt joints and, as such, are inherently weak. Buried or epoxy filled vias require wrap plating for these types of interconnections per IPC-6012 table 3-4 and 3-6. It is not possible to have wrap plating at the microvia target pad, and the best that can be done is to improve the interface with epitaxy and bottom-up recrystallization. However, it should be noted that even with these improvements and with direct metallization that has no electroless, we can still create microvia failures during reflow and D coupon testing.

What Causes the Microvia to Fail?

During reflow there is temperature cycle material expansion of the laminate that creates stress on the microvia butt joint. When the stress created by the expansion exceeds the strain limit of the target pad and electroplated microvia interface, plastic deformation occurs, and non-conformance exists.

Many studies have tested microvias before reflow and after reflow and have concluded that microvias are fine. However, microvias typically fail during reflow and the resistance change can only be detected during the peak reflow temperature cycle. A microvia failure at peak temperature will cause an open, and plastic deformation in the microvia will create permanent damage at the target land microvia interface. What makes this type of failure so frustrating is that the open does not exist at ambient room temperature so chasing down the type and cause of the failure is a lengthy process that can impact both engineering cycle time and overall product development costs.

Actions taken to reduce the microvia failures have included increasing the microvia diameter and reducing the aspect ratio. These actions and the new rules resulting from them have reduced failures. The benefits of these rules are described below.

- Increasing the microvia diameter increased the interface area.
  - A small increase of a microvia from .1mm to .127mm increases the surface area by 56%.
  - A wider surface area increased the survivability of a microvia if the same material expansion was exerted on the larger target pad interface.
  - Reducing the aspect ratio typically reduced the overall dielectric thickness.
    - This thickness reduction decreased the material expansion potential which improved the microvia survivability.
  - Stacked microvias required a lower aspect ratio than a single microvia for consistent 6X reflow passes.

While these new rules have worked for most builds, failures have still occurred. Most of the failures occurred with dielectrics that exceeded .15mm/.006" or if high resin content prepreg was used. When failures did occur, the typical solution was to try and increase the microvia diameter, reduce the dielectric and rebuild the parts with the hope that the rebuild would pass.

The Traditional Stack Up and Material Selection Processes and How They Affect Microvia Reliability

During the traditional stackup and material selection processes, the importance of microvia reliability is often not considered. This is due, in part, to not clearly understanding the stackup and material selection process in general and, specifically, how microvia reliability factors into these processes and why it needs to be addressed so early on.

Material selection for a stackup may be specifically defined by the PCB designer. In this case, each ply of prepreg and each core construction is defined and a stackup is provided to a PCB fabricator. When a stackup is not provided by the PCB designer, the fabricator is allowed to make the material selection. In many cases, the fabrication drawing can simply state thatlead free FR-4 material is to be used by specifying IPC-4101 /126. The simplest instructions are that there are no dielectric callouts on the fabrication print and a PCB fabricator can select any core thickness or prepreg glass style that will accommodate the required overall thickness and, if required, impedance requirements. These basic generic instructions open the door to infinite stack up variations. A PCB designer or the Electrical Engineer could make all of the stackup decisions by specifyingthe resin system brand; the core and prepreg openings and the core constructions and prepreg types. But these practices are

not standardized within the industry and are dependent upon the company's design practices as well as the experience level of the designer or engineer.

PCB Planners will select dielectric woven glass styles that are compatible with laser drilling. Another consideration for planners is to select resin rich prepreg to fill internal plated layers that are found in HDI designs. Electrical Engineers will select low loss and spread glass weave to improve the electrical performance of high-speed designs. Stackups will favor a high resin content and spread glass combination to meet fabrication and electrical performance needs.

Figure 1 depicts the image of a resin-rich spread glass material. In this image, the white portion is resin, and the woven glass is gray.

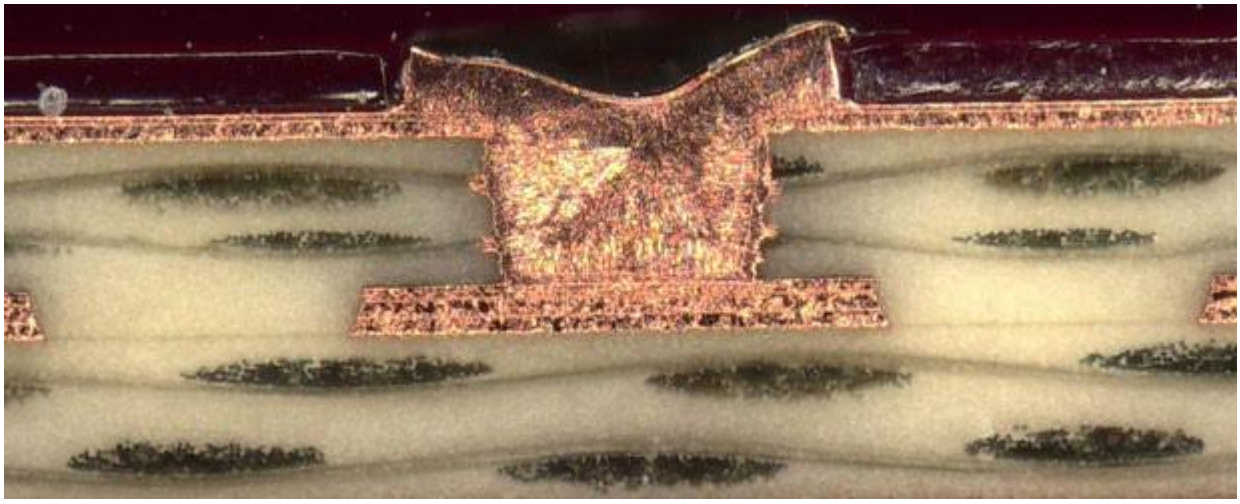


Figure 1. Image of A Resin-Rich, Spread Glass Material

Material datasheets will provide information regarding a specific product type. Here is the list of typical material properties that are provided. The coefficient of thermal expansion (CTE) alpha-1 and -2 are in boldface type.

- Glass Transition Temp (This is the resin transition)
- Thermal Decomposition Temp
- Time to Delamination
- CTE alpha-1 X & Y axis
- **CTE alpha-1 Z axis**
- **CTE alpha-2 Z axis**
- Thermal Conductivity
- Volume Resistivity
- Surface Resistivity
- Dielectric Constant (Dk)
- Dissipation Factor (Df)
- Water Absorption
- Flexural Modulus
- Peel
- Flammability

Datasheets may or may not state the test sample thickness for the datasheet values. In many cases, the test vehicle uses a thick, double-sided construction that has low resin content. Most HDI designs and the spread glass laminates have much higher resin content than the test vehicles that are defined in most datasheets. The actual alpha-2 expansion in an HDI design can be 50% to 100% greater than the generic datasheet values. Without the actual expansion for each resin system's weave and resin percentage, it is not possible to determine if a PCB can withstand the reflow temperatures.

Table 1 provides examples of available prepregs with resin content and as received sorted by thickness.

Table 1. Prepregs with Resin Content Sorted by Thickness.

Prepreg Glass Weave	Inches	mm	Percent Resin
1035	0.002	0.051	69.0%
1067	0.0022	0.056	70.0%
106	0.0023	0.058	76.0%
1067	0.0024	0.061	71.5%
1035	0.0026	0.066	75.0%
1067	0.0026	0.066	74.0%
1067	0.0029	0.074	76.5%
1078	0.0029	0.074	65.0%
1078	0.0031	0.079	67.5%
1078	0.0035	0.089	70.5%
1080	0.0038	0.097	72.0%
1078	0.0037	0.094	72.0%
1078	0.0042	0.107	75.0%
1080	0.0043	0.109	75.0%
1080	0.0046	0.117	78.0%
1078	0.0046	0.117	78.0%
3313	0.0046	0.117	63.5%
3313	0.0051	0.130	66.5%
2116	0.0058	0.147	62.0%
2116	0.0064	0.163	65.0%

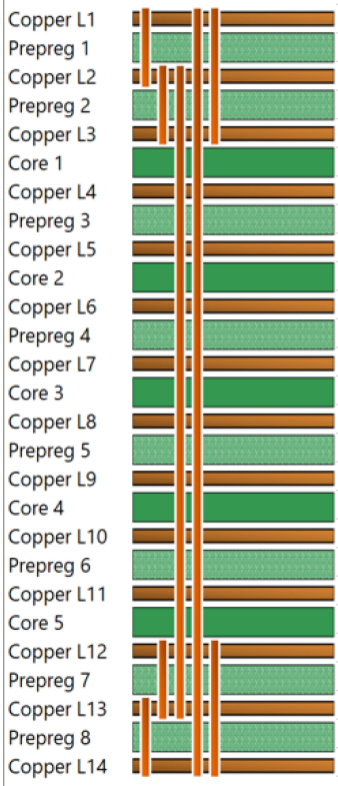
Traditional material selection for a stackup would use a table similar to Table 1. A PCB planner would pick and choose materials that would achieve correct overall thickness and satisfy individual dielectric call outs to satisfy specified impedance requirements. Then, glass weaves that are compatible with laser drilling are selected. Material selection also focuses on avoiding glass stops and lamination voids. To avoid these defects, a planner would select a prepreg with higher resin content. Almost universally, high resin content has long been regarded as an aid in preventing lamination voids and glass stops and improving the overall electrical performance of a high-speed digital or RF design.

However, the above practice of selecting high-resin content materials lacks an evaluation of materials reliability. For example, resin expansion below Tg (alpha-1) is relatively close to the copper expansion. At alpha-2, the expansion is 4-8X. As a result, itis necessary to perform modeling to confirm that a stackup can reliably survive the assembly process. In addition, since the properties of each core and prepreg are not readily available for analysis, a designer or a fabricator cannot predict, at either the design stage or before fabrication begins, if a new design will pass reflow resistance testing or assembly.

The Ability to Achieve Stackup Validation and Predictive Pre-Production Engineering

Predictive simulation of a stackup is now possible. The modeling is based on each core and prepreg construction in the intended stackup. The modeling is based, not on a datasheet value, but on each core construction and bond ply/prepreg and the composition of each dielectric opening. The modeling also must take into consideration the percentage of retained copper on each layer along with the total thickness of each copper layer. Analysis of the microvia considers the diameter of the microvia, the layers the microvia spans, the density of the microvia and whether the microvia is stacked or staggered. This simulation represents a unique approach and capability heretofore not available in the industry. Figures 11 and 13 provided later in this document show that actual testing verified the results of the simulations.

The new process still follows the standard process of creating a stackup. The overall thickness, layer counts, and layer types are ordered; drill sizes and spans are defined, and impedance requirements are defined and verified. Figure 2 is an example of a defined stackup using low Tg material. This stackup will help to demonstrate a poor material set that cannot meet 6X reflow requirement.



Name	Thick (mils)	Ret. Cu Frac	Glass Style or Rz (µm)	Vendor Name	Layer Style or Resin Style	Resin Content	No. Plies	Dk	DF
Solder Mask	0.3								
Plating	1.4								
Copper L1	0.45	0.2	2		SIG				
Prepreg 1	4.707		E-106	X	FR4 150Tg	0.75	2	3.52	0.016
Copper L2	1.2	0.8	4		PLANE				
Prepreg 2	4.227		E-106	X	FR4 150Tg	0.75	2	3.52	0.016
Copper L3	0.6	0.2	2		SIG				
Core 1	8		E-2116	X	FR4 150Tg	0.45	2	4.11	0.012
Copper L4	1.2	0.8	4		PLANE				
Prepreg 3	4.227		E-106	X	FR4 150Tg	0.75	2	3.52	0.016
Copper L5	0.6	0.2	2		SIG				
Core 2	8		E-2116	X	FR4 150Tg	0.45	2	4.11	0.012
Copper L6	1.2	0.8	4		PLANE				
Prepreg 4	4.113		E-106	X	FR4 150Tg	0.75	2	3.52	0.016
Copper L7	0.6	0	2		SIG				
Core 3	8		E-2116	X	FR4 150Tg	0.45	2	4.11	0.012
Copper L8	0.6	0	2		SIG				
Prepreg 5	4.113		E-106	X	FR4 150Tg	0.75	2	3.52	0.016
Copper L9	1.2	0.8	4		PLANE				
Core 4	8		E-2116	X	FR4 150Tg	0.45	2	4.11	0.012
Copper L10	0.6	0.2	2		SIG				
Prepreg 6	4.227		E-106	X	FR4 150Tg	0.75	2	3.52	0.016
Copper L11	1.2	0.8	4		PLANE				
Core 5	8		E-2116	X	FR4 150Tg	0.45	2	4.11	0.012
Copper L12	0.6	0.2	2		SIG				
Prepreg 7	4.227		E-106	X	FR4 150Tg	0.75	2	3.52	0.016
Copper L13	1.2	0.8	4		PLANE				
Prepreg 8	4.707		E-106	X	FR4 150Tg	0.75	2	3.52	0.016
Copper L14	0.45	0.2	2		SIG				
Plating	1.4								
Solder Mask	0.3								

Figure 2. Defined Stackup Using low Tg Material.

While this stackup meets all of the defined requirements, reliability simulation of the selected material properties will demonstrate that the microvias are incapable of surviving six reflow cycles.

Figure 3 depicts the evaluation of the microvias on copper layers 1 and 2 with a .006" microvia diameter. The results show that these microvias will only survive 4.2 reflow cycles.

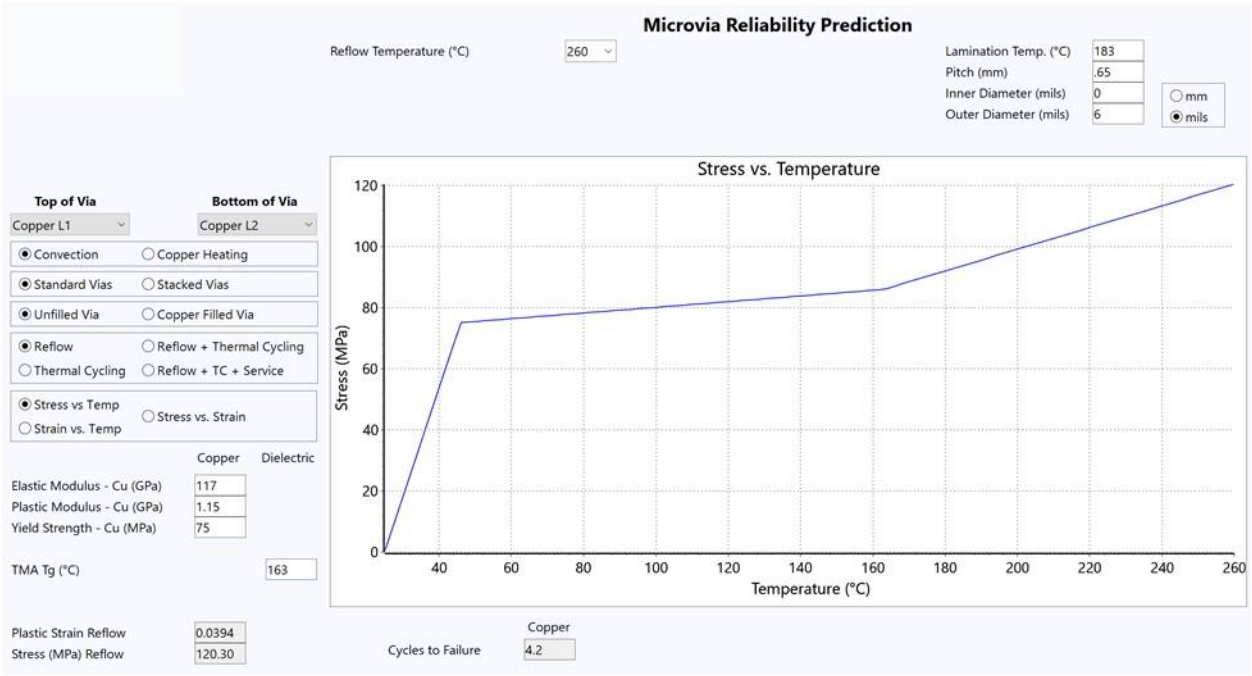


Figure 3. Evaluation of Microvias on Copper Layers 1 and 2 with a .006″ Diameter.

In Figure 4, the evaluation of two stacked microvias on copper layers 1 and 3 shows a much weaker condition. This simulation predicts a failure after 2.1 reflow cycles. When there are two vias that are stacked and go down to layer 3 where there is more dielectric and that dielectric is reflowed, it expands such that the attachment is compromised.

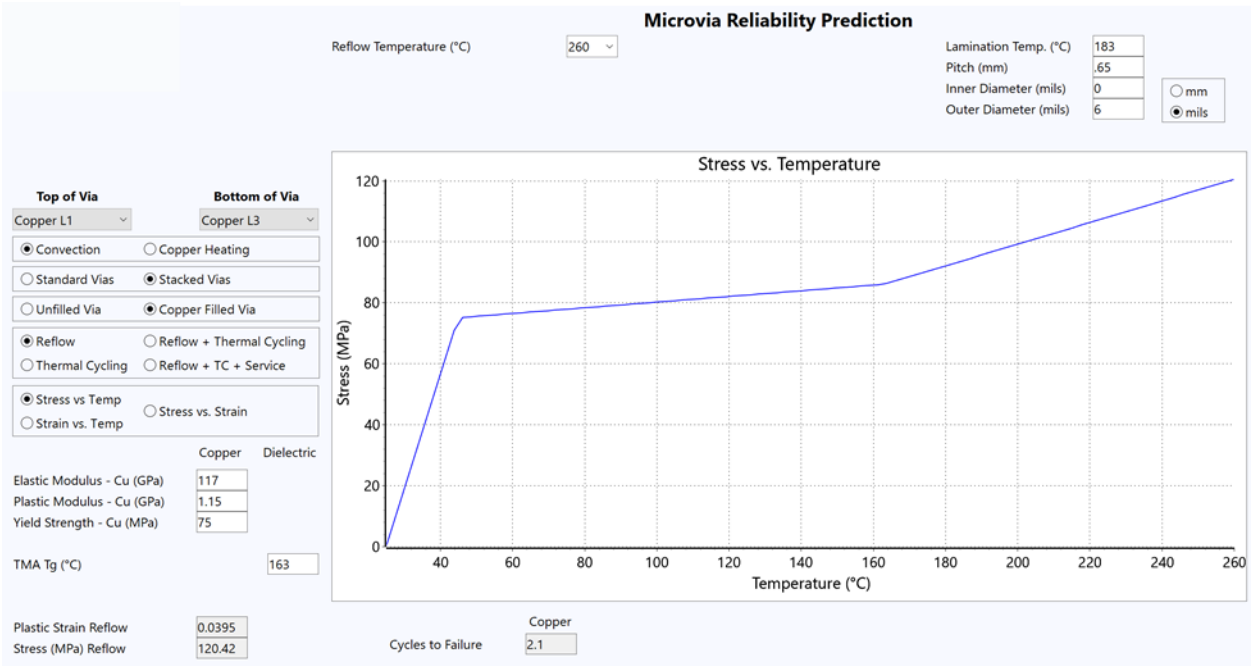
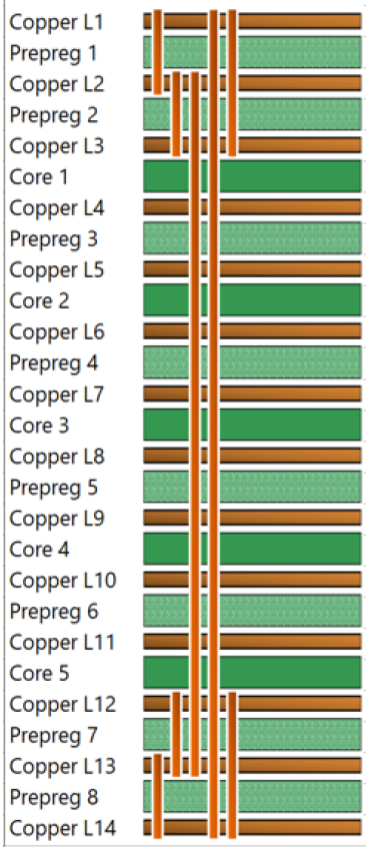


Figure 4. Evaluation of Stacked Microvias on Copper Layers 1 and 3.

With predictive engineering and reliability simulation, it is now possible to screen out an unreliable stackup and change to a material type that allows design geometries to pass the required reflow test requirements. It is also possible, through simulation, to determine that the microvia design must be modified by increasing the microvia diameter, staggering the microvias or changing the prepreg selection.

Figure 5 depicts the stackup in Figure 3 with the laminate changed to a material selection that has half of the CTE Z expansion of Figure 2.



Name	Thick (mils)	Ret. Cu Frac	Glass Style or Rz (µm)	Layer Style or Resin Style	Resin Content	No. Plies	Dk	DF
Solder Mask	0.3							
Plating	1.4							
Copper L1	0.45	0.2	2	SIG				
Prepreg 1	2.707		E-1078	High TG	0.65	1	4.39	0.009
Copper L2	1.2	0.8	4	PLANE				
Prepreg 2	2.227		E-1078	High TG	0.65	1	4.39	0.009
Copper L3	0.6	0.2	2	SIG				
Core 1	8		E-3313	High TG	0.565	2	4.58	0.008
Copper L4	1.2	0.8	4	PLANE				
Prepreg 3	3.827		E-106	High TG	0.75	2	4.18	0.01
Copper L5	0.6	0.2	2	SIG				
Core 2	8		E-3313	High TG	0.565	2	4.58	0.008
Copper L6	1.2	0.8	4	PLANE				
Prepreg 4	3.713		E-106	High TG	0.75	2	4.18	0.01
Copper L7	0.6	0	2	SIG				
Core 3	8		E-3313	High TG	0.565	2	4.58	0.008
Copper L8	0.6	0	2	SIG				
Prepreg 5	3.713		E-106	High TG	0.75	2	4.18	0.01
Copper L9	1.2	0.8	4	PLANE				
Core 4	8		E-3313	High TG	0.565	2	4.58	0.008
Copper L10	0.6	0.2	2	SIG				
Prepreg 6	3.827		E-106	High TG	0.75	2	4.18	0.01
Copper L11	1.2	0.8	4	PLANE				
Core 5	8		E-3313	High TG	0.565	2	4.58	0.008
Copper L12	0.6	0.2	2	SIG				
Prepreg 7	2.227		E-1078	High TG	0.65	1	4.39	0.009
Copper L13	1.2	0.8	4	PLANE				
Prepreg 8	2.707		E-1078	High TG	0.65	1	4.39	0.009
Copper L14	0.45	0.2	2	SIG				
Plating	1.4							
Solder Mask	0.3							

Figure 5. Stackup in Figure 3 With Material Change.

Figure 6 is the evaluation of the microvias on copper layers 1 and 2 with a .006" microvia diameter using the changed material in Figure 5. The results show that the microvias on copper layers 1 and 2 will survive more than 10+ reflow cycles.

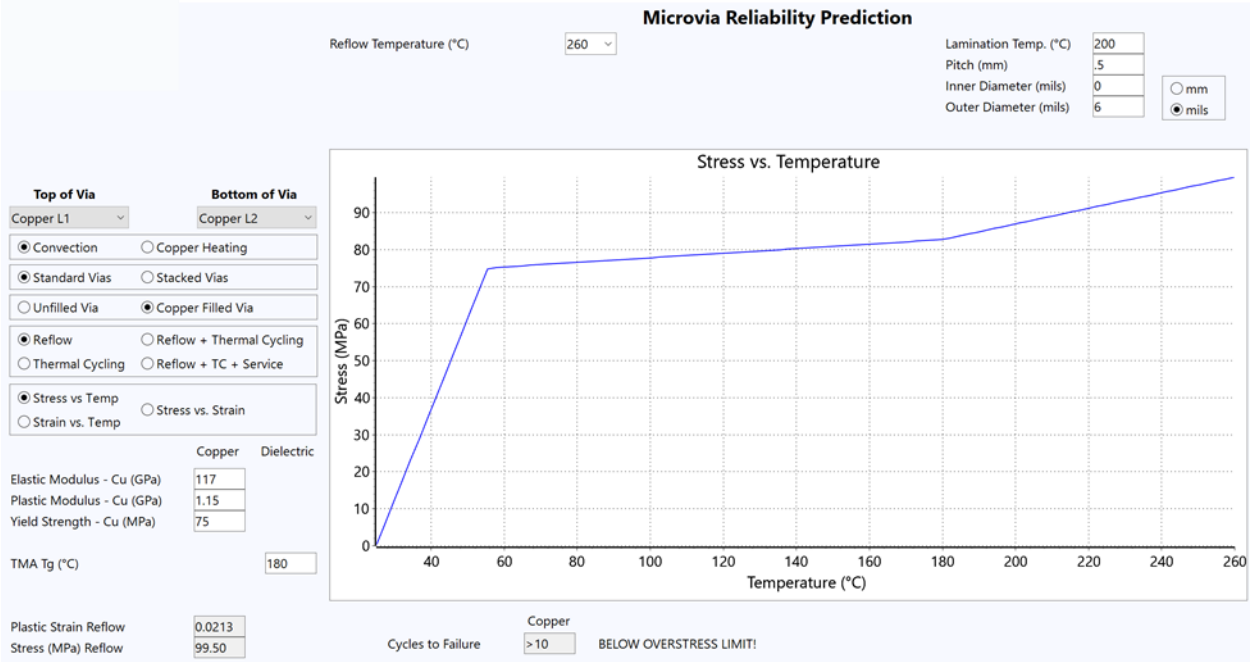


Figure 6. Evaluation of Microvias on Copper Layers 1 and 2 with .006" Diameter, Changed Material.

Figure 7 shows that the evaluation of 2 stacked microvias on copper layers 1 and 3 will withstand 6.2 reflow cycles.

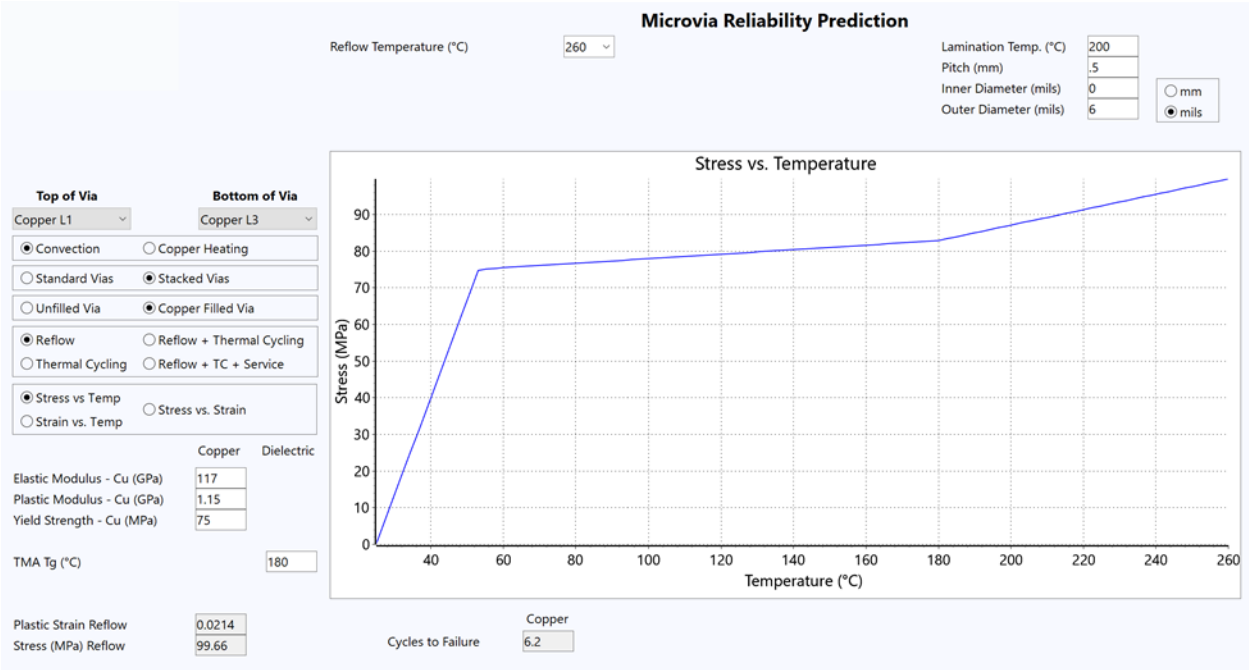


Figure 7. Evaluation of Stacked Microvias on Copper Layers 1 through 3 at 260°C.

To improve the design reliability, a simulation can be performed on a staggered microvia in copper layers 2 and 3 as is depicted in Figure 8. This shows that a staggered microvia on layers 2 and 3 can survive 10+ reflow cycles.

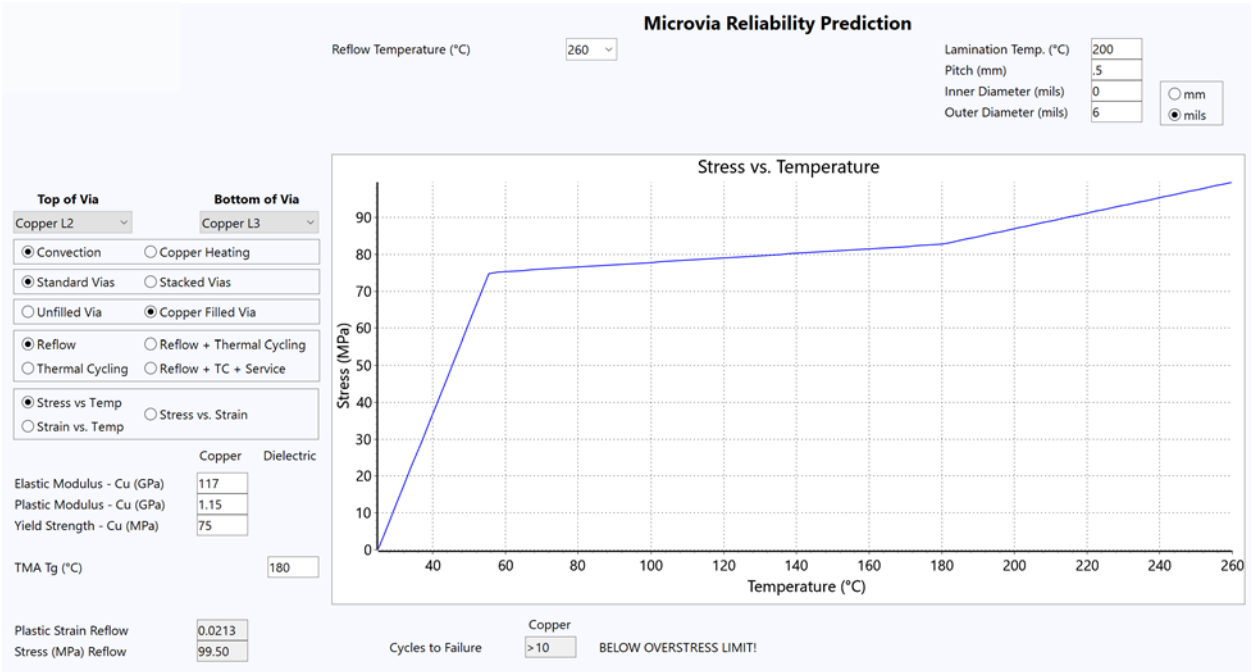


Figure 8. Evaluation of Staggered Microvias on Copper Layers 2 and 3 Demonstrates That a Staggered Design is Safer Than Two Stacked Microvias.

In addition to the foregoing simulations, the predictive modeling can also model temperature reflow to determine if the same two stacked microvias on copper layers 1 through 3 can safely achieve more than six reflow cycles. Figure 9 shows the modeling simulated with the reflow temperature being reduced from 260°C to 245°C.

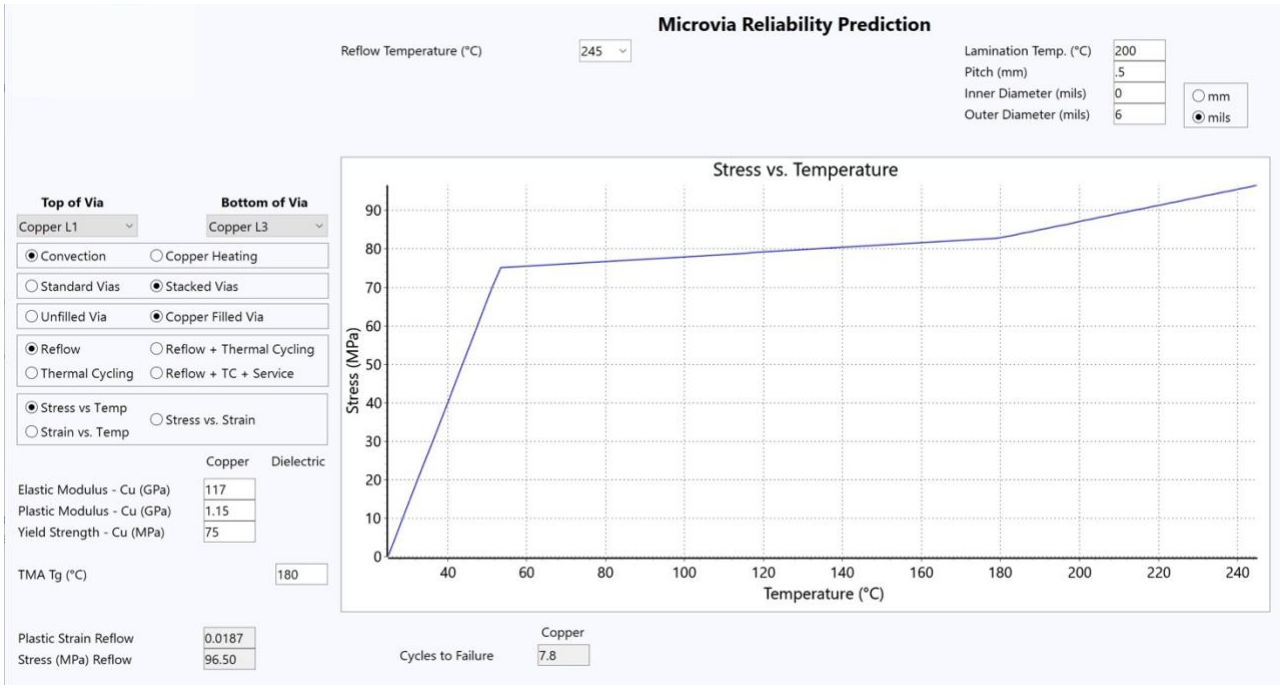


Figure 9. Modeling of a Lower Temperature Reflow on Stacked Vias in Copper Layers 1 and 3 Demonstrates That Lowering the Reflow Temperature Will Increase the Reliability of the Finished PCB.

As noted earlier in this article, the results of the microvia simulations were compared against the actual results from the actual results of D coupon testing (per IPC-TM-650 2.26.27). The following figures provide the results of that analysis.

Figure 10 shows the prediction of reflow, obtained during simulation, to failures at 2.8 cycles.

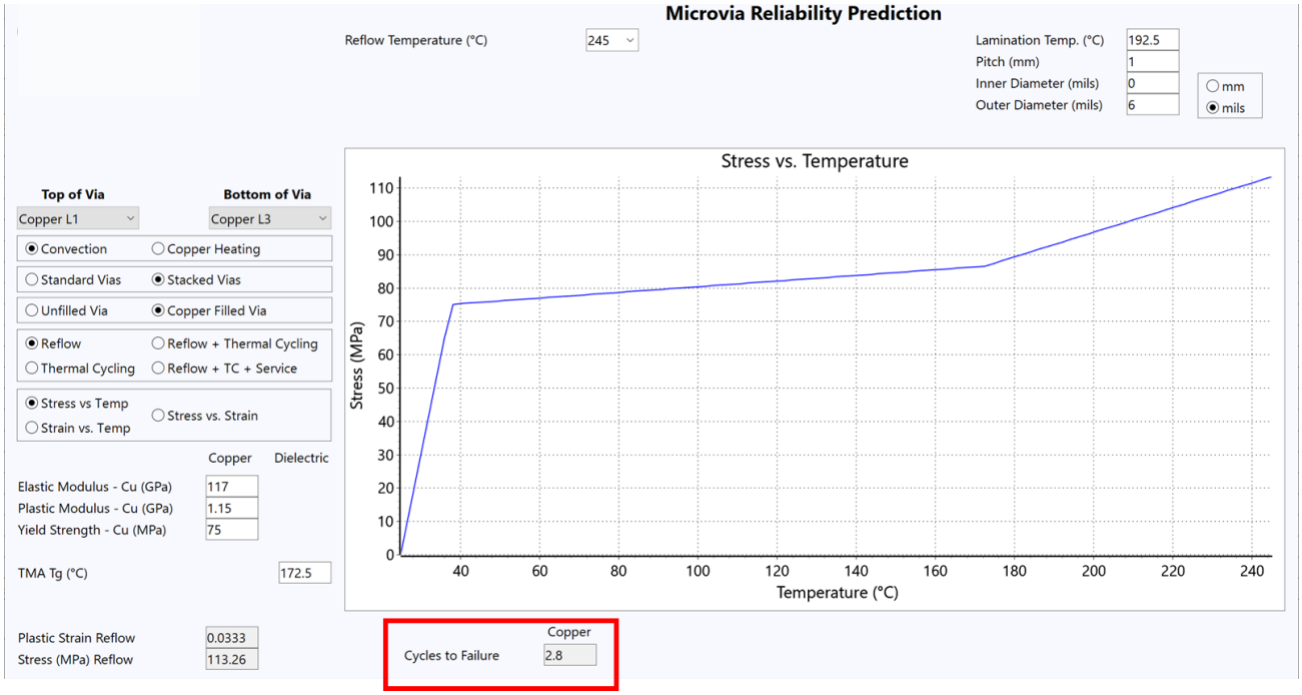


Figure 10. Simulation of Two Stacked 0.152mm [0.006"] Microvias at 245°C.

Figure 11 shows the recorded D-Coupon results that were tested to IPC-TM-650 2.6.27 at 245°C at 6 cycles.

Coupon Number	Nominal Resistance at Room Temperature (ohms)		Reference Resistance at 245C (ohms)		Cycles to 5% Change		Change after 6 Cycles (%)	
	Net 1	Net 2	Net 1	Net 2	Net 1	Net 2	Net 1	Net 2
1	0.793	0.768	1.422	1.379	4	4	Open	Open
2	0.788	0.778	1.478	1.449	2	2	Open	Open
3	0.795	0.722	1.474	1.348	3	4	Open	Open
4	0.727	0.763	1.364	1.420	4	>6	Open	1.3
5	0.810	0.782	1.503	1.452	5	4	16.9	Open
6	0.825	0.794	1.530	1.469	3	3	Open	Open
7	0.775	0.742	1.427	1.372	3	2	Open	Open
8	0.711	0.710	1.337	1.317	3	4	Open	Open
9	0.779	0.752	1.431	1.385	3	3	Open	Open
10	0.789	0.780	1.469	1.448	2	2	Open	Open
11	0.807	0.777	1.491	1.441	3	2	Open	Open
12	0.774	0.762	1.423	1.396	6	6	6.3	22.7
13	0.801	0.770	1.540	1.500	2	2	Open	Open
14	0.795	0.791	1.476	1.469	5	4	20.6	Open
15	0.770	0.736	1.474	1.431	2	2	Open	Open
16	0.766	0.747	1.456	1.411	2	3	Open	Open
17	0.763	0.724	1.641	1.604	2	2	Open	Open
18	0.704	0.685	1.319	1.271	3	6	Open	8.4
19	0.773	0.739	1.439	1.384	4	3	65.7	Open
20	0.730	0.717	1.425	1.394	2	2	Open	Open
21	0.773	0.753	1.608	1.698	2	2	Open	Open
22	0.726	0.763	1.414	1.438	2	2	Open	Open
23	0.801	0.758	1.516	1.454	2	2	Open	Open
24	0.793	0.770	1.475	1.422	2	2	Open	Open

Figure 11. IPC-TM-650 2.6.27 Test Results for 48 nets.
Average Failure 2.95. Simulation Prediction: 2.8 cycles tofailure.

The next simulation was done based on using a material that has a low CTE Z value of 58 ppm/C. Here, the microvia was 0.076mm [0.003"] with an aspect ratio of 1:1.

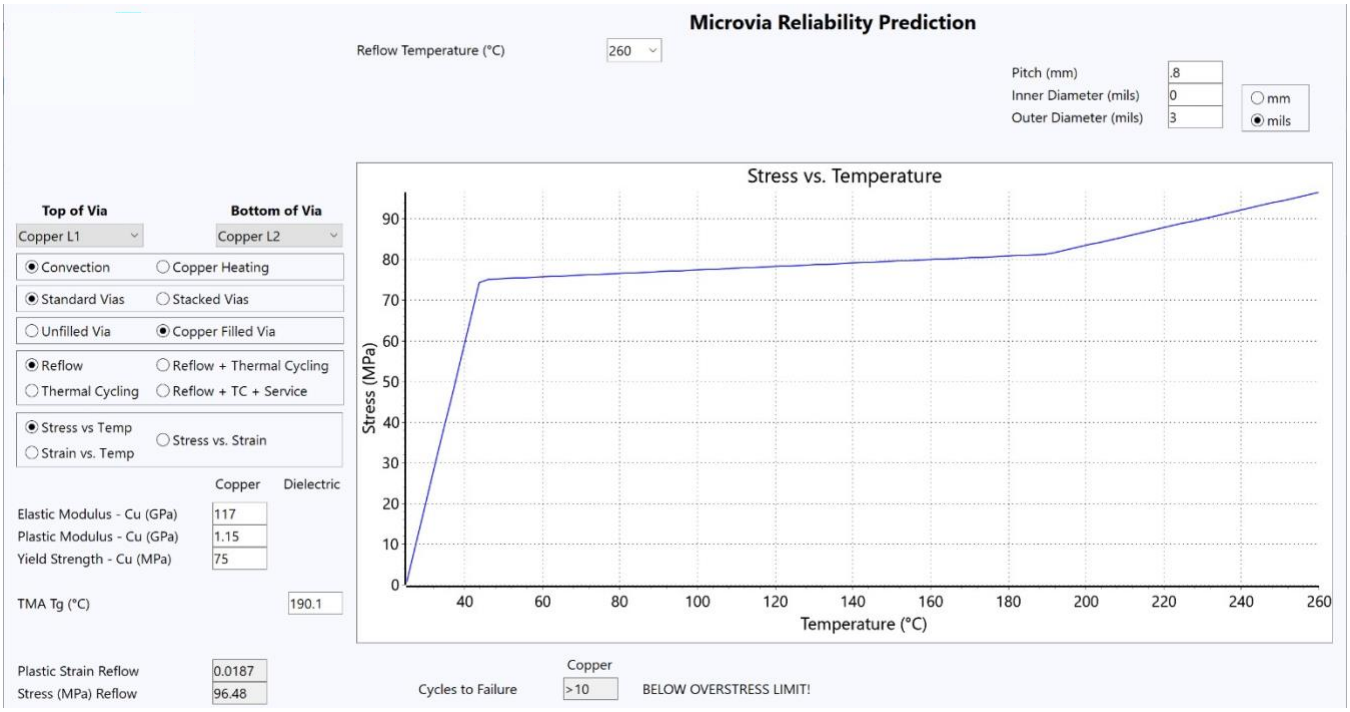


Figure 12. Single 0.076mm [0.003"] Microvia Simulation, Prediction of +10 Reflow Cycles at 260°C.

Figure 13 shows the actual D-Coupon results for the change in resistance during reflow for 24 nets and 24 cycles at 260°C. (As tested to IPC-TM-650 2.6.27).

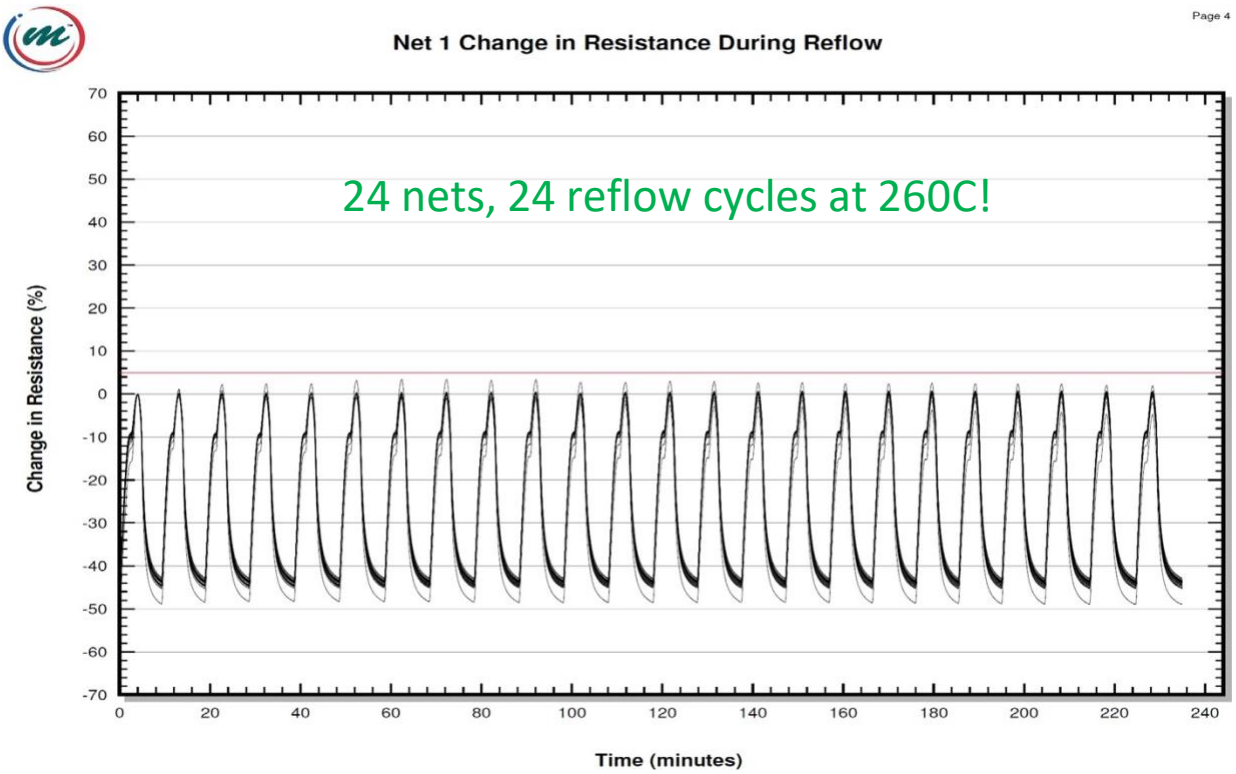


Figure 13. 24 Reflow Cycles at 260°C. Change of Resistance No Greater Than 5%.

The foregoing information demonstrates that the predictive simulation results are borne out with actual testing. This creates the new paradigm of computational PCB prototyping that provides greater insight during stackup to bridge the design-to-manufacturing process with greater granularity and accuracy.

Summary:
Today's high frequency, high data rate designs have pushed the envelope in terms of what is achievable with traditional PCB design practices and PCB laminates. Increasingly, these designs require the use of microvias and there is very little leeway for mistakes with these structures. Miscalculations or poor choices made during the design process can lead to microvias that willnot be able to withstand the standard-specified, mandated reflow process. New software previously unavailable to the industry now makes it possible to select, during the design process, among the microvia options available to ensure a design will workas developed and as specified across all of the product life cycle from design to manufacture, operation and long-term reliability.