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CAD/CAM

This month, experts from Altium, CadSoft, Mentor Graphics, and Prototron Circuits bring you in-depth articles that detail the ins and outs of CAD/CAM for fabricators.

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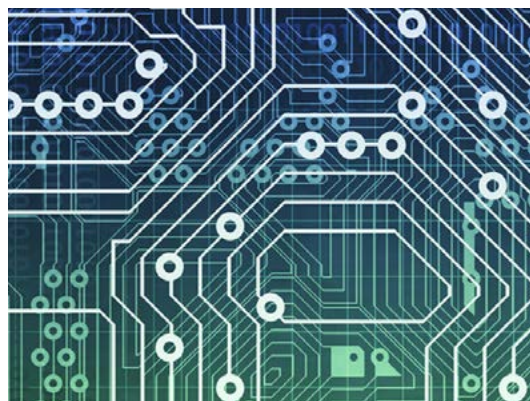
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20 Understanding the Typical CAM Process

by Mark Thompson



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CAD/CAM

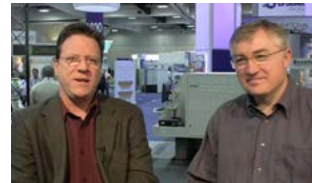
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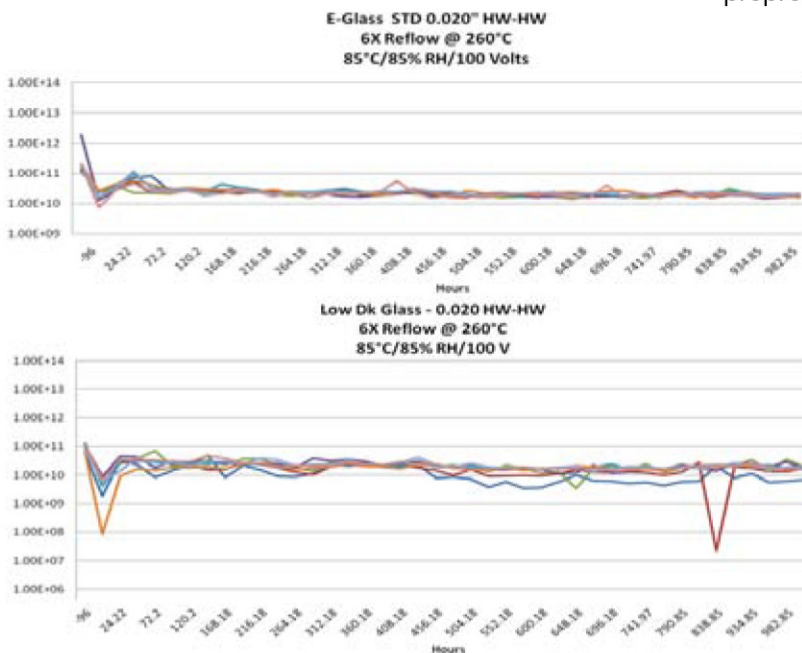
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IPC Forms a PAC

by Ray Rasmussen

I-CONNECT007

IPC just announced they're forming a political action committee. Here's their reasoning for creating a PAC:

Political action committees (PACs) have become an important tool for any group that wants to be heard when laws and regulations are written. Given the growing number of government regulations that influence the electronics supply chain, having clout in Washington, D.C. is something that can no longer be ignored. As a result, IPC's Board of Directors has decided to join the many trade associations and large companies that have established PACs.

I have reservations about IPC's new direction in D.C. There's some history.

In the early '90s, I was a huge supporter of prodding the industry to be more active in local and national government. Rules and regulations were constantly being developed without any input from our industries. The onslaught of environmental regulations coming from the EPA, the state regulators, and local municipalities left the industry frustrated and seemingly powerless. Something had to be done and the logical approach was for our national association, IPC,

to take the lead. They had the industry clout to present the issues to the regulators or those in the Congress who would listen. They could tell the story and make the case for or against specific requirements. When approached, IPC's position was that they were a standards organization, and that lobbying and politics wasn't their game. That stance changed as pressure mounted and newer, more open-minded board members began to see the importance of telling our story and having a seat at the table when new requirements on our industries were being proposed. Most in Congress, we found out, had no idea who we were or what we did. They didn't know the role we played in everything electronic. They only knew of the big guys. And in their minds, anything to do with the electronics industry was "big business."

As we began to get more involved in the political and regulatory processes, we learned that we had a distinct advantage over our much larger, political action committee-holding, big electronics brethren. They all had their PACs and lobbyists, but we had something special that they didn't: a geographically diverse membership made up of small, independent busi-



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nesses. The members of Congress loved that and almost always welcomed our letters or our phone calls as well as our visits during Capitol Hill Days. In fact, there were a few larger organizations with common interests around certain rules or up-coming legislation, which lent their support but let IPC take the lead precisely because of the makeup of our industries.

Back then, IPC hired the lobbying firm Wayne Sayer and Associates to represent the industry in Washington. Sayer's team would present our position regarding regulations and review new legislation affecting the industry. They also organized the Capitol Hill Day events, which included lobbying training, preparation for visits with our representatives as well as the specific issue we'd be presenting during the visits to the Hill. Each member had meetings with their representatives in the House and Senate. It was quite enlightening to most of us who'd never done anything like this before. I would encourage everyone in the industry to support the next Capitol Hill Day event. It's quite an experience.

Within a few years, IPC realized they needed their own people on the ground in D.C., which began a new era as we became directly involved in the policy-making. We had a seat at just about every table. Most in Congress knew who we were, what we were about and, more importantly, who we represented. By then, our industry's companies had even invited quite a few of their representatives to tour their factories. Now, when we had an issue with a regulation or piece of legislation, we had the ear of Congress. One of our member companies, South Dakota-based Electronics Systems Inc. and its CEO, Leo Reynolds, forged a strong relationship with then-Senate Majority Leader Tom Daschle of South Dakota, which brought our issues to the forefront. We gained a lot of ground back then.

Since the mid-'90s, the industry has done a lot to stay active in governmental processes. It's hard to quantify the dollars associated with our inaction in the '80s and '90s, but we did miss the boat with NAFTA and lead-free legislation. Not having a seat at the table for those two issues alone has certainly cost the industry dearly. Of course, RoHS wasn't a U.S. initiative, but IPC definitely should have been at the

table. We might have been able to steer the ship a bit. I wonder what would have happened if IPC, along with the other electronics associations, had leveraged their clout in Congress and had just said "no." I know what happened with NAFTA. We didn't have the systems in place to be able to address our concerns to the government back then. They asked, but received no input from us. Regarding lead-free, we were just asleep at the switch.

On the positive side, IPC's efforts in support of equipment depreciation along with minor tweaks in regulations and legislation have saved the industry quite a bit over the years. As an active industry player, IPC has certainly upped our stature and has been able to influence at least some of the things coming our way. Before the mid-'90s we had no voice. And maybe that's what IPC's founding fathers originally wanted—to stay under the radar, focusing on standards. Back then we were dumping most of our waste down the drain or, in the case of a few really bad actors, into creeks behind our factories.

For me, a PAC has a negative connotation. It's buying votes instead of leveraging the grassroots power we have as an industry. It cheapens us. Now, instead of being an industry of small businesses (which we mostly are), we push that aside in the minds of our representatives and regulators and join the likes of IBM, Dell, Cisco and Google (Motorola), the AEA and SIA. It seems to me a better course of action would be to encourage our member companies to donate to their representatives based on IPC recommendations, but keep the IPC out of PACs so that it can remain "pure," without "blemish."

Couldn't we take that PAC money and use it to strengthen our team in D.C. instead? What would bring the greatest return?

Let me know what you think. **PCB**



Ray Rasmussen is the publisher and chief editor for I-Connect007 Publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuiTree Magazine*. To read past columns, or to contact Rasmussen, [click here](#).

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CLOSING THE GAP BETWEEN DESIGN AND FAB

by Ben Jordan
ALTIUM

Recently, I've been doing a bit of investigation to find out what really needs to happen to get a good turnaround on designs—from idea to a working board, that is. There is a more pressing need than ever for ECAD vendors to do some close work with PCB fabricators, but it seems that ECAD vendors have a complete disconnect. I think that CAD tool vendors in general have done a fantastic job of making design easier and faster, but there is still a huge gap between what a PCB designer intends, thinks, and lays out in CAD and what a PCB fabricator needs in order to build and assemble the boards with reasonable yields. It's one (good) thing to support universal data transfer formats, but that's not an automatic fix-all, either. What I'm really talking about is DFM.

Over the years, IPC has made efforts to fix this disconnect. This is why the current CID and CID+ programs have an emphasis on DFX. For those unfamiliar, DFX means “design for

x”, where x = manufacturing, assembly, and test—together we call it Design for eXcellence. The thought process here is that if PCB designers are trained to know the materials, processes, steps and limitations of a PCB fab, then they will inherently know how to design the PCB to be “manufacturable.” Part of this also is the classification of PCBs based on complexity and producibility levels.

Of course, the designer then has a new job as a kind of mediator between engineering management, product marketing, and the fab: having to laboriously explain why the product they are working on cannot be designed the way marketing wants it, or why moving a button one inch to the left will cause the product assembly costs to significantly rise. It's a big ask for designers to have to bear in mind all the fabrication and assembly processes, and then have to turn around and put these practical limitations up against the wants of other stakeholders. If I were hiring designers, I would limit my search to CID-certified people for this reason alone. Yet, in a sense, this is like having a

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BY TAIYO



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It counts a lot to actually go to a PCB fab and take a tour, and fortunately most fabs with oil in their lamps are willing to oblige if you give them enough notice. I have done this myself, recently spending a fair amount of time with a few fabs near me in California. And taking tours of real PCB fabs and interrogating them has confirmed my suspicions.

I can illustrate the sorts of problems that can occur between design and manufacturing with a tangible real-world example. On a visit to Sierra Circuits in Sunnyvale (also known as ProtoExpress.com) I got to walk through the entire process of preparing and laminating a rigid-flex panel “book.” It was an eye-opening experience—not only for getting to see how a rigid-flex board is made, but just as much to be made aware of the fabrication process and its limitations. This was a particularly interesting example, because the PCB in question was very

small and had to have thin flexible sections—about 3mm in width—between the rigid sections, each about the size of a U.S. quarter. The final board prototype is shown in Figure 1.

The big deal with this board was that with such narrow flex-circuit sections, it was not possible to use “bikini” coverlay for the flex. This meant that polyimide coverlay film had to extend through the entire lamination of the board, which in turn meant that acrylic adhesive layers had to be used to adhere the polyimide coverlay layers to the rigid cores. This may not seem like a problem, except that the PCB is four layers in the rigid areas, and with such densely populated components on top and bottom layers, the vias were on the risky side of smallness. Why? Because the adhesive layers are known to expand in the Z-axis during solder reflow.

In other words, the fab already knew that this board was going to have lowered yields in assembly caused by cracking vias, in turn caused

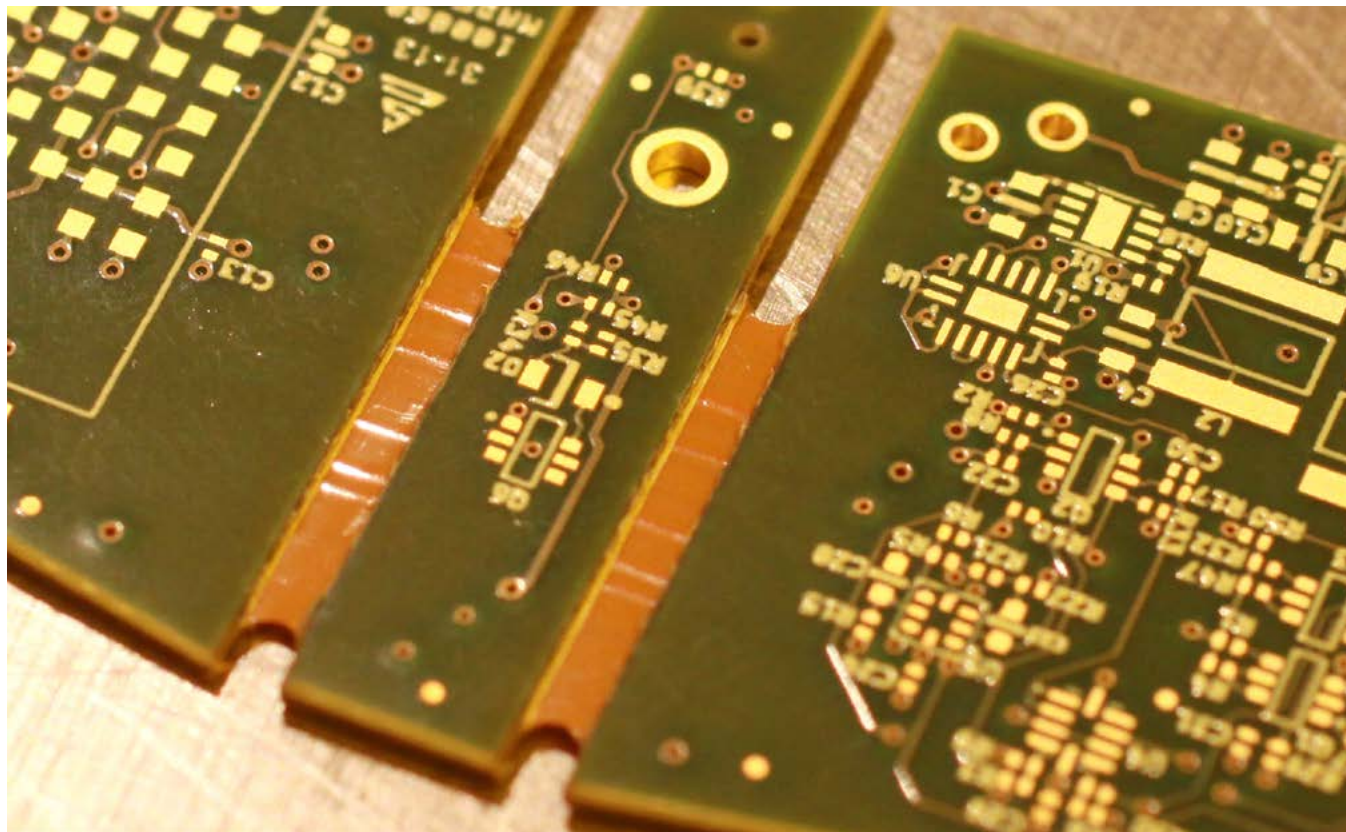


Figure 1: Difficult-to-make rigid-flex board.

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Figure 2: White acrylic adhesive layers are added to the lamination book.

.....

by adhesive expansion, caused by the need to have coverlay film within rigid sections of the board, caused by the size constraints of the design and its mechanical form factor. They actually advised the designer about the problems, and the risk, but in this case the designer was out of time and really could not easily redesign for better assembly yield and maintain the necessary product form factor. This falls into the age-old trade-off between form (a largely marketing driven design aspect) and manufacturing cost (i.e., scrap). In this case, the prototypes were needed quickly, so the designer requested production in spite of the associated risk.

Sierra is an example of what I call an educator fab—these are the guys who will tell you what is wrong with your design so that you can try to get it right next time. But there is still a level of frustration for them, as it seems like the designers rarely perform comprehensive DFM checks on their designs. I'm told that it is still most common that designs are at first rejected for DFM issues when the fab runs their own

DFM checks using their own CAM/DFM tools.

Another type of fab, such as Hughes, in San Marcos, California, is just as likely to request the original source documents from the PCB designer in the native CAD format. I refer to these guys as a fix-it fab. You could say part of their service is to make the changes necessary to your design to improve the manufacturing yield and lower costs—optimizing your design to their processes and equipment. Most high-volume fabs would want to work with the designer in similar ways to ensure low waste, but if you're working with fabs on distant shores this may not be desirable. As an example, I asked Hughes how they need masks to be generated in the CAD software; their response was a firm, "Don't; let us do that for you in CAM."

From all the PCB fabs I've talked with, there is an overwhelmingly common message: Even though PCB designers have access to DFM checks and tools, there's no easy industry standard way for the PCB designer to fully run DFM checks before hand-off. This common

complaint from the fabs is that designers still largely don't hand over manufacturing-ready designs.

In response, it would be easy to ask, "What about constraint-driven design?" It's a good question. I think that a designer having a good understanding of the constraints and then being able to run design rule checks against the fabrication constraints is an essential part of the solution. The problem with this, however, is that you often have one design, but multiple fabricators who may use different equipment. Of course, the answer to that problem appears to be well-accepted transfer data formats such as IPC-2581 or ODB++. IPC-2581 has promise for streamlining the data handoff, but it still doesn't address the basic problem that, from the outset, designs often begin with too little awareness of how the boards will actually be made once the design is finished.

When discussing these issues with Sierra, Hughes and others, I received a surprisingly overwhelming response that "ECAD tools don't have proper DFM checks in them." Frankly, the first time I heard that I was taken aback. Really? Yet when I probed deeper, I discovered that the DFM checks referred to are available in the ECAD tool's design rule check engine. The real problem is actually that the designer either does not apply them, or applies them without properly defining the constraints according to their fab's capabilities.

For example, let's consider silkscreen ink being allowed to print over bare copper. As a test, I sent a design that had a small bit of silkscreen designator text over an untented via (a via with no soldermask over the copper lands) to three different fabs: an educator fab, a fix-it fab, and a broker for offshore fabs. The educator fab immediately informed me that I had silkscreen over a mask opening and it had to be fixed in my design. The fix-it fab asked for the files in the native (Altium Designer or Protel) format, and the broker simply sent the Gerbers to a fab, which eventually emailed me informing me that some silkscreen items would be removed because of overlap with mask openings. In all three cases, at a minimum, the production date would be delayed. So what are the options for a solution?

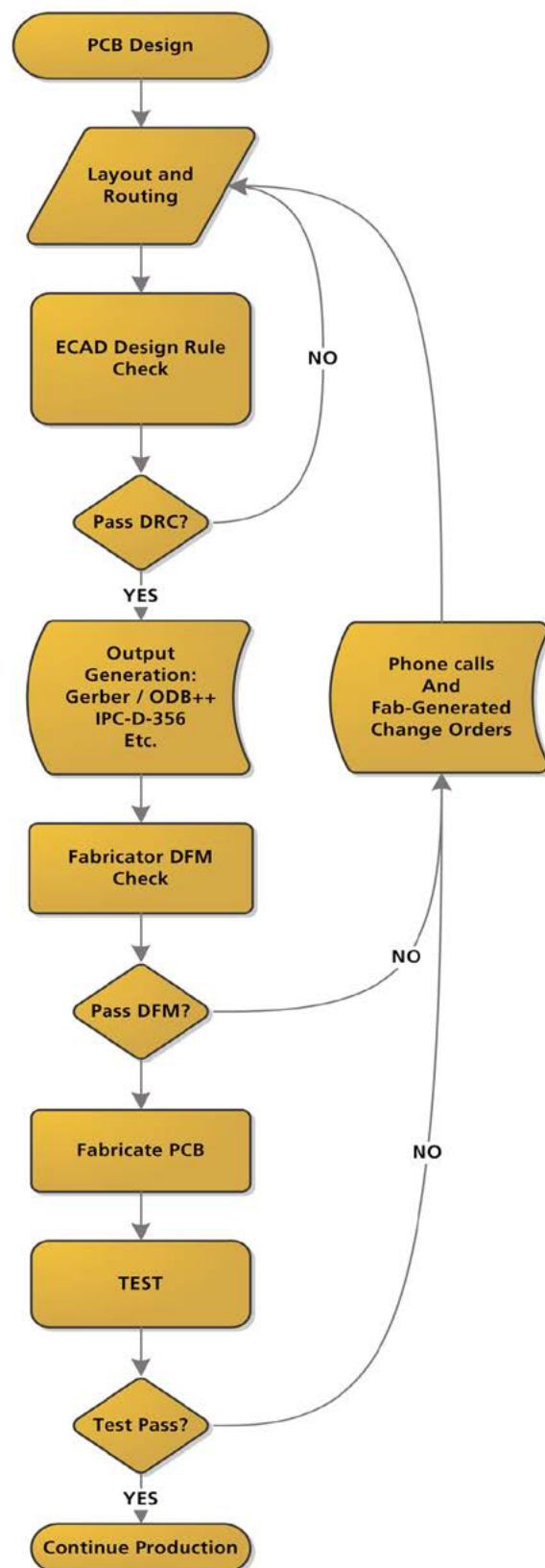


Figure 3: The usual PCB design-to-fab flow looks connected, but there's plenty of room for error.

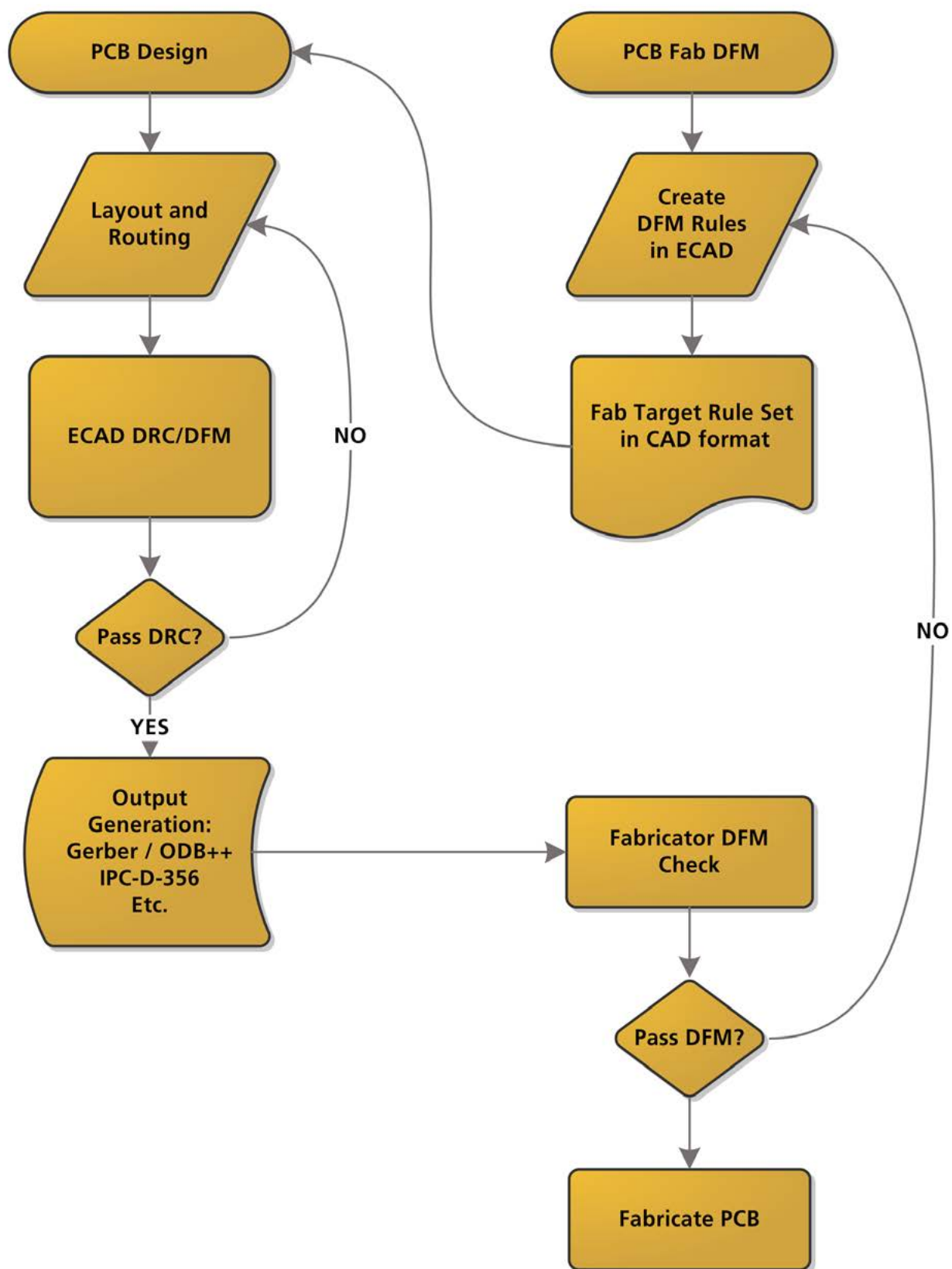


Figure 4: A better way: Involve the fabricator early with DFM.

One option is to develop some standard, basic DFM checks which all designers can handle for simple to moderate (Level 1 and 2 producibility) designs. In this case, an industry body could publish a list of DFM checks and their tolerances which could easily be ported into any ECAD design rule check engine, so designers could efficiently apply them and have confidence that most fabs would successfully produce the boards. This sounds good, but it's actually quite a difficult thing to achieve—the number of constraints that would have to be thought of ahead of time is staggering.

Another option is for the fabricators to be more involved in ECAD tool development. While some have actually used free PCB design tools as a loss leader, it is a very difficult thing to make tools which can handle cutting edge or even some mainstream designs efficiently. I would go as far as to say it could financially detract too much from the core business of the fabricator. Personally, I would prefer the fabs to put money into expanding their production lines with newer equipment to tackle the next generation of products. But I do think for DFM, we might actually be onto something here...

A better solution space for this problem then, the best in my opinion, is for fabricators to have technical staff actually involved in design planning and in setting up the rules and constraints as early as possible in the design process. The difficulty on the face of this solution is that you may have to know up front who your fab is. Most companies tend to use the same fabs over the long haul so it's not such a big deal. This can be further eased by the fabs. The fabs have a great opportunity to improve business here and I can see at least a few ways of making this easy for designers to really get it right the first time:

At the simplest level, the fabs need to get into each ECAD toolset, and produce a pre-packaged set of DFM rules (or constraints) for each production line or process complexity level they support. Then, those DFM rule sets can be published or made as a download from the web for the customers who are working with that fab. In turn, the designer can then run a DFM check which gives a high confidence when everything passes, that the fab they are

using will be able to get good yields with their design.

Going a step further, PCB fabs could offer whole template projects for various toolsets as free downloads for their registered customers, which in a “shrink wrap” include the various DFM checks for their production lines.

Take this one step further again: ECAD tool vendors like Altium could make the API for the software available to the fab, who can build their own quoting and DFM check systems into the ECAD tool, so the designer who intends to use that fab can make sure their design is good with the click of a button and even receive a quote from the fab for prototyping.

There's a lot that can be done here. The third solution requires the fabricator to have the necessary software infrastructure in place and secure links between ECAD and online DFM servers. However it adds two distinct advantages. The first is that the PCB fabricator can run full DFM without exposure of their processes, and the other is that the designer can run DFM checks against a real fab's processes without other humans interacting with their design source documents.

For these problems to be solved in a way that best suits the designer, integration is really needed. Closing the gap between design and fabrication needs reliable and universal data transfer, yes, but above all, it needs good collaboration between all parties involved. Having good file formats is important, but it is not the complete solution. While work has been done with ODB++ and IPC-2581, the uptake is slow—ODB++ has less than 20% use according to the fabs, and IPC-2581 is in its infancy. But if we attack the problem with a one-two punch of good data format combined with early, integrated and direct involvement from fabricators themselves, then lots of wasted time and materials can be avoided. **PCB**



Ben Jordan is a senior manager at Altium. To contact him, [click here](#).

Understanding the Typical CAM Process

by **Mark Thompson CID+**
PROTOTRON CIRCUITS

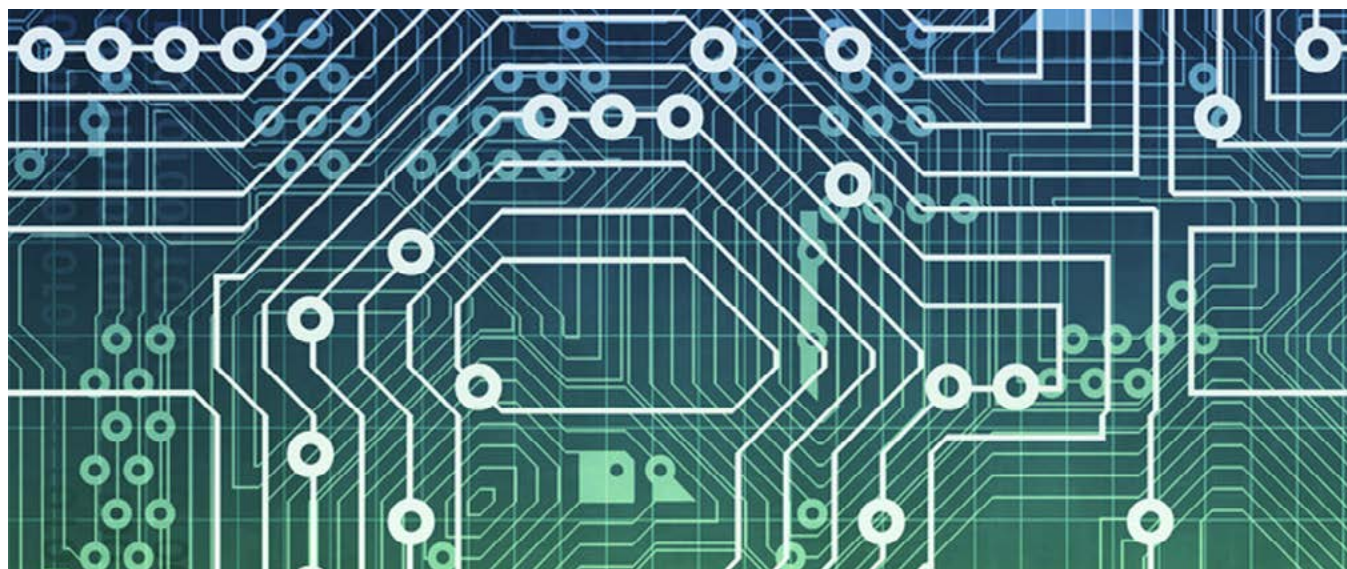
CAM vs. Capability

Many new customers have some misconceptions about what a typical fab shop can and cannot do. There are levels of manufacturing that need to be well understood by the buyer. The PCB buyer needs to know where a board will be a good fit based on the parts' complexity. How does this happen? How does the PCB buyer or a contract manufacturer know who is (or is not) a good fit based on a myriad of different designs, from simple 2–4 layer RF parts to high-layer count HDI, blind and buried via parts? If the part is of medium complexity, it can be built by virtually any mid to higher level PCB fabricator. Many times it boils down to things like quote response time. More diligent buyers may use a tool such as The PCB List where they can compare technology levels side-by-side and make good decisions about where a part should go. Not all PCB buyers need a shop that can do 2 mil lines and spaces or laser stacked vias. Sometimes the product dictates a shop of this type must be used; other times, when a given design does not "push" the fabricator's limits, more fabricators obviously have an opportunity to show what they can do.

What is CAM?

Not all board fabricators have the ability to have both CAD and CAM. You may say to yourself, "But a CAM tool should be able to do some, if not all, CAD functions," and that is true; but if you are really getting to the design level, you need to have a design team. Many PCB fabricators do not have design capabilities but do have the ability to understand the customers' needs and recognize design attributes.

Let me give you some examples of this from simple CAM assumptions to more complex ones. Let's say a design has copper poured right to the edge of the part, but is NOT a Z-axis or edge-plated part. A good CAM department may do a very minimal clip of the metal around the periphery like .003–.004". This is imperceptible to the end user as it appears metal is right to the edge and if the metal would have been left alone there may be burring at final rout (functional, but not cosmetically the best). Again, this is where a good CAM person comes into play: When would they NOT do something like a minimal clip for rout? RF launches on an obvious RF part; here, we know the intention is to literally have metal right to the edge and that





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any burring at final rout is acceptable with the customer. This is where their understanding of electrical function comes in as well, plus years of practical experience.

And when I say CAM department, I mean both people and tools, as the tools are only as good as the people behind it. I have said many times that a good CAM operator is worth his weight in gold.

Likewise there are many levels of designers and layout folks, some with years of knowledge and good common-sense layout practices. These are the guys and gals that ask the important questions at the right time, which is to say at the design/layout stage and not after the PCB gets to the board fabricator.

What does a fabricator do with data needed to produce parts?

To start, let's go through what a board fabricator needs from an output CAD package briefly and talk about what edits are done at the manufacturing stage and why you need to know about them.

Regarding output packages, what does a fabricator need to be able to fab your part?

1. Image data of all the layers involved including mask files, silkscreens and pastes exported as either Gerber 274D, 274X, or ODB++.

At least one of these files should have a part outline on it, unless you are providing a drawing with a dimensioned hole or feature.

2. NC drill file or files (for blind or buried). Typically, Excellon 1 or Excellon 2 format.

3. An IPC-356 type netlist so the fabricator can run the design against the exported Gerber.

4. A drill drawing with hole sizes, dimensions and drill symbols chart.

If the part is impedance controlled, the drawing should describe what lines are being

controlled, where they reside and what threshold and tolerance they need to perform at.

Now the fabricator has the job. Will my data undergo any modifications for manufacturing? Yes, so let's go through them.

Sometimes CAM is a compromise between pad size, drilled hole size, copper weight and available space. Don't rope yourself into anything if you don't have to. If the hole is a legitimate via and you really don't care about its finished hole size make it $+.003''$ minus the entire hole size.

1. Drill compensation for plated holes, slots or edge features

Depending upon surface finish, fabricators will drill anywhere between $.004''$ and $.005''$ over your specified finished hole size (FHS) to plate back down to your nominal size. Since this is something done by all manufacturers your output data should have already taken this into account. Fabricators like to see a minimum of $.002''$ per side annular ring pad to hole after this drill compensation on signal layers and at least $.005-.006''$ per side pad to copper pour after the drill compensation.

Sometimes CAM is a compromise between pad size, drilled hole size, copper weight and available space. Don't rope yourself into anything if you don't have to. If the hole is a legitimate via and you really don't care about its finished hole size make it $+.003''$ minus the entire hole size. This tolerance tells the fabricator it is okay to drill smaller to deal with things like annular ring minimums and can mean the difference between a quote from a fabricator and a "no bid."

2. Etch compensations for image data

Depending upon the starting copper, all image data is compensated at the CAM stage to account for the known loss at the fabricators etcher. Typical rule of thumb is a half-mil of additional line or metal feature width for every half ounce of starting copper.

Exception to this rule is quarter oz copper foil where no etch compensation needs to be

added. Quarter oz foils are typically only used for outer or surface layers.

Again, your design should be able to accommodate these compensations. Example: If your design is .003"/.003" and you are asking for 2 oz. copper you will get a phone call from your fabricator.

3. Panelization

If you are ordering parts as an array either as a tab rout, score or combination of both you will want to provide a sub panel drawing with any particulars your assembler may need like additional tooling, fiducials, specific areas where not to place a tab due to part overhang issues at assembly, etc.

If you have no preferences and your chosen assembler does not need anything special typically the board fabricator can come up with a good sub panel that works well for both manufacturing and assembly. For instance: Even if no tooling or fiducials are specified for the given array, many times fabricators will add them to the array anyway. They are generally of no harm at that point and can be quite helpful if tooling and fiducials were not foreseen.

4. A 1-up compare and net-list compare

The fabricator will perform a 1-up compare at the CAM stage even if no IPC netlist is provided. This is to ensure the addition of the drill and etch compensations does not create manufacturing capability violations. A 1-up compare is only that; it is not a netlist compare. If an IPC-356 file is provided, the fabricator will also run the provided IPC netlist against your provided exported Gerber data. Remember this is a design vs. exported Gerber file comparison. If you do not provide an IPC netlist for a class 36012 job, your fabricator will ask for one. I have been asked many times over the years to simply generate a net-list based on their exported Gerber data. If a netlist is generated by the fabricator based on the Gerber data, at what point would we ever find a mismatch? So what is my point? If you would like us to verify your design iteration against your exported Gerber data please provide an IPC net-list.

A brief note about IPC net-lists and their generation: Avoid creating test points for things

that will be connected only after the devices are loaded, such as surface mounts or edge-plated castellations. This will avoid a phone call from your fabricator with false or erroneous "broken" or open nets. Likewise, many times in a design an AGND to DGND short is designed in and is intentional. Make note of these intentional net-list anomalies.

Throughout this article I have used the term "artwork" but today you have fabricators that can send the image data from CAM directly to a direct image device, eliminating the use of films and thus another transgression of the artwork image. Every copy you make loses a little in the translation. If you can image the cores and outer layers directly, this loss is minimized.

Common Fabrication CAM Issues

1. RF parts

RF type applications typically require a specific design tool suite that does not always deal with things like RF impedance controlled traces in a conventional manner. For example:

RF traces are often drawn as a composite of many smaller line sizes to be able to deal with the unique shapes and reflections needed for RF work. This is a nightmare for a CAM operator. The size being controlled may be specified as .025", but when the CAM operator queries the apertures used for .025", they do not exist. Again, this is because they have been drawn as a conglomerate or composite of many smaller trace widths.

2. Same size trace width for single-ended impedance structures, differential pairs and copper pour

This does not allow the CAM operator to easily select one or the other for any unique re-sizing that may be necessary for meeting or getting closer to the customers' desired impedances.

For years, I have advocated using a tenth or a hundredth of a mil to differentiate between single-ended traces, diff pairs and copper pour that are using the same draw size. Fabricators cannot resolve this small difference but it allows the CAM operator to select and deal with

those structures without affecting the others. I am happy to see this is becoming the norm.

3. Etch and drill compensations not taken into account at the design and layout stage

This can mean the difference between a quote and a “no bid” from a fabricator.

Do not make the pads only .005” over the finished hole size or you will get a phone call from your fabricator, as this does not allow for drill compensation plus a minimum of .002” per side annular ring pad/hole. The same goes for slots or other edge-plated features.

Additionally, make sure the design allows for etch compensations based on the copper weight you are specifying. Again the rule of thumb is half mil for every half-ounce of starting copper. Specific information about etch and drill compensations can be gleaned from the fabricator as different shops require different process minimums. Add to that, if your design needs to meet IPC these things should have already been factored into the design.

Drawings and data that don't match:

Sometimes this happens due to rounding errors from metric to inch or vice versa, but sometimes it happens because the part has been revised and the note is no longer applicable. Remember to review the drawings to make sure all information contained is valid and/or still required.

These are but a few examples of things a CAM department will run into. I hope this has helped you understand a small part of the CAM process as it relates to board fabrication. Feel free to send me your feedback! **PCB**



Mark Thompson is in engineering support at Prototron Circuits. His column, The Bare (Board) Truth, appears bimonthly in *The PCB Design Magazine*.

To read past columns, or to contact Thompson, [click here](#), or phone 425-823-7000, ext. 239.

VIDEO INTERVIEW

Happy Birthday to the ODB++ Solutions Alliance

by Real Time with...Designers Forum 2013



The ODB++ Solutions Alliance celebrated its first anniversary with a banquet at IPC APEX EXPO. Julian Coates, director of the ODB++ Solutions Alliance, discusses the newest version of ODB++. He also talks about the testimonials presented by ODB++ users at the party, some of whom say that they no longer even think about ODB++ anymore--it's become a part of their workday.



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The Internet of Things Drives New PCB Design Approach

by **Mark Toth**
CADSOFT COMPUTER

The most common question asked of electronic product developers today is how to do more with less. How do you incorporate newer, faster technologies in smaller packages to take advantage of new products and architectures that provide more functionality and power efficiency, all on time and under budget? Is it possible to retool processes without negatively impacting designer productivity? Can advanced techniques and current best practices be made available at the designer's fingertips during development, without leaving the design environment?

Increased consumerization of electronics and a convergence of various elements of functionality, due in part to the Internet of Things (IoT), are putting intense economic pressure not only on time-to-market, but on cost of development as well. Add to that increased competition in the electronics industry and continued globalization, and we're seeing increased investments in tools, training, new best practices and increasing openness to collaboration.

To illustrate the continued globalization, according to information released by the [EDA Consortium](#) in an October press release, PCB and multi-chip module revenue is at \$148.3 million, a YoY increase of 5.2% compared to the same quarter in 2012. The four-quarter

moving average for PCB and MCM, however, increased 10%. This is compared to overall industry revenue which increased only 3.8% YoY for the same quarter reported, but dropped almost 1% in sequential quarters. The four-quarters moving average, which compares the most recent four quarters to the prior four quarters, increased by only 5.3%.

Not surprising, a geographic trend for the design tool industry shows revenue for all design tools in the Asia-Pacific region increased



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to \$431.9 million in the most recent quarter reported, an increase of 18% compared to the same quarter of the prior year. The four-quarter moving average increased 14.4%.

The financial opportunity for electronic product development is exponential, but there are major pitfalls as well. A simple rule of thumb in management consulting practices states that, on average, companies lose a third of after-tax profit when they ship products six months late. One could easily argue the penalties are significantly greater in the consumer electronics market, which has now far exceeded the \$200B mark.

Design cycle time plays a big part in determining a product launch schedule, and the PCB layout part of this process is often called upon to make up for early design phase schedule slips. In today's competitive climate, finding ways to reduce design cycle times is a priority for all engineers. Of chief concern for many companies is that as PCB design becomes more and more complex, engineers need to have cost-effective tools that reduce time-to-market. Another potential challenge is the fact that companies have design teams dispersed all over the world.

Given all those factors, it's easy to see how completing a product launch within the specified time frame can be daunting. To address all of these challenges, companies need tools that can leverage their existing resources (both human and computer), allow interoperability, have a gentle learning curve and can offer extensions that link other time-intensive parts of the design cycle or supply chain.

In a recent industry survey conducted by CadSoft Computer, designers from 42 different countries weighed in on future requirements, as well as emerging trends in electronic product development.

Some of the results were surprising:

- Sixty-four percent of respondents think development boards are reducing the need for custom PCB design
- Almost half (46%) are developing with open source hardware platforms
- Eighty-three percent agree peer-to-peer communities are important, while 25% believe they are essential

Other results were not unexpected:

- The majority of designers put functionality before cost when buying design tools, with 60% of respondents rating functionality as an "extremely important" factor
- A design tool should offer a gentle learning curve
- Design tools should:
 - Allow multiple designers to lay out a single project without sacrificing productivity
 - Have a plug-and-play model for tasks that are intensive to increase productivity
 - Allow designers to collaborate with each other in real-time from anywhere in the world

While it is true that more and more design projects are being started with off-the-shelf development kits and boards instead of designing a PCB from scratch, engineers will often need to design an interface board (such as a shield, cape, expansion, daughter card, etc.). This is a market where many PCB tool companies, including CadSoft, have significantly benefited.

As more and more open source hardware platforms are finding their way into commercial development projects, some large global silicon suppliers are now offering such low-cost open source kits to the maker and hobbyist in hopes of increasing demand for their technologies. TI's Launchpad series is just one example.

What about peer-to-peer, social media, designing in the cloud and other forms of collaboration? Are these trends fuelling designer productivity?

Although somewhere between novel idea and trend, a few considerations need to be addressed before the cloud is deemed mainstream for electronics design. These considerations include risk and compliance (such as data security and retrieval), flexibility (access and control) and timing (different services will benefit from moving to the cloud sooner). From a business standpoint, it is more likely to occur in PCB design first, as there are so many more PCB designers to make it a more sustainable

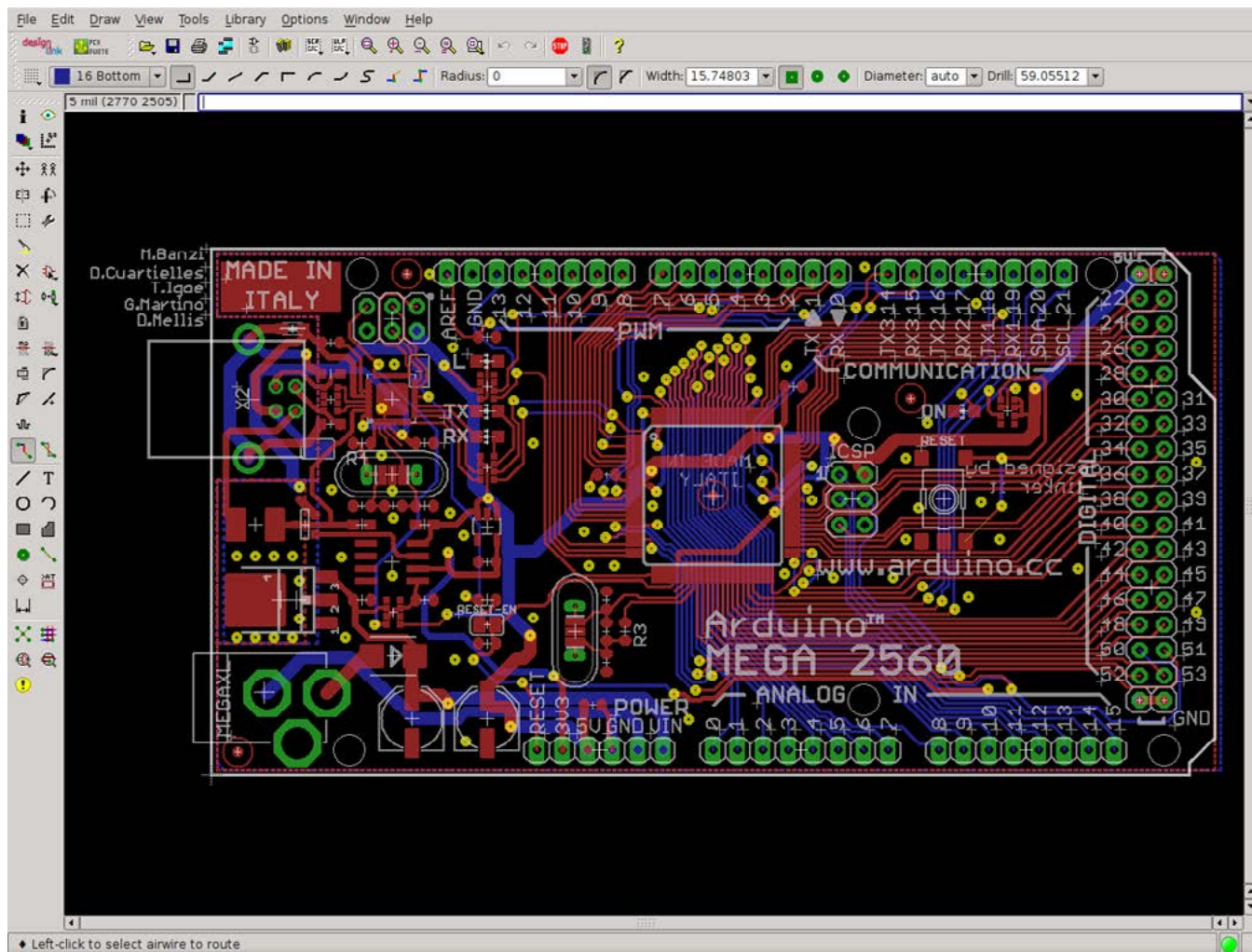


Figure 1: The Arduino Mega 2560 [reference design](#) in CadSoft EAGLE.

model. Determining factors for a design application to harness the power of the cloud are tied to obvious benefits such as increased speed and capacity, lower cost, security and so on. If your design application is not performance-intensive, or the cloud does not lower your development costs or improve productivity, it might not make sense just yet.

Other online resources and communities, however, have existed for years helping engineers get answers, find common design elements and identify new technologies faster. Element14.com, the first and largest online engineering community with more than 200,000 members, enables developers to connect with like-minded peers to gain design inspiration

or obtain expert answers and opinions. One of its most active forums is hosted by the CadSoft EAGLE user community. In addition to answers and advice, element14 contains a free database of CAD libraries, which are searchable by component supplier, thus enhancing designer productivity and cost to develop.

Another trend that continues to evolve in the PCB design industry is tighter forms of integration between electrical and physical design. To efficiently bring a new product into production, electrical CAD (ECAD) and mechanical CAD (MCAD) data must be merged. A virtual 3D representation of the PCB geometry within MCAD tools allows mechanical engineers to quickly design product housings

as well as other mechanical features that fully utilize the available 3D real estate. MCAD features such as cross-section views and interference checks help ensure that there will not be any future fit issues when prototypes are built.

Keith Richman, president of Simplified Solutions, said:

Generating a virtual 3D representation of PCB geometry within MCAD tools has historically been a time consuming task. Intermediate Data Format (IDF) has been around for 20+ years, but in the earlier days of IDF, the labor involved to create 3D PCB representations was time consuming and costly. In

2014, many tools are available to help expedite the 3D PCB process. Manufacturers and online services now provide 3D STEP models that can help populate a 3D PCB. In addition, some solutions contain integrated 3D component libraries that allow the 3D geometry task to be completed in just hours. 3D printer technology can then be utilized to generate a geometric 3D representation of PCB geometry prior to the more expensive manufacture of PCB prototypes.

Speaking of component libraries, the amount of information needed on thousands of different components threatens to overwhelm even the most organized professional.

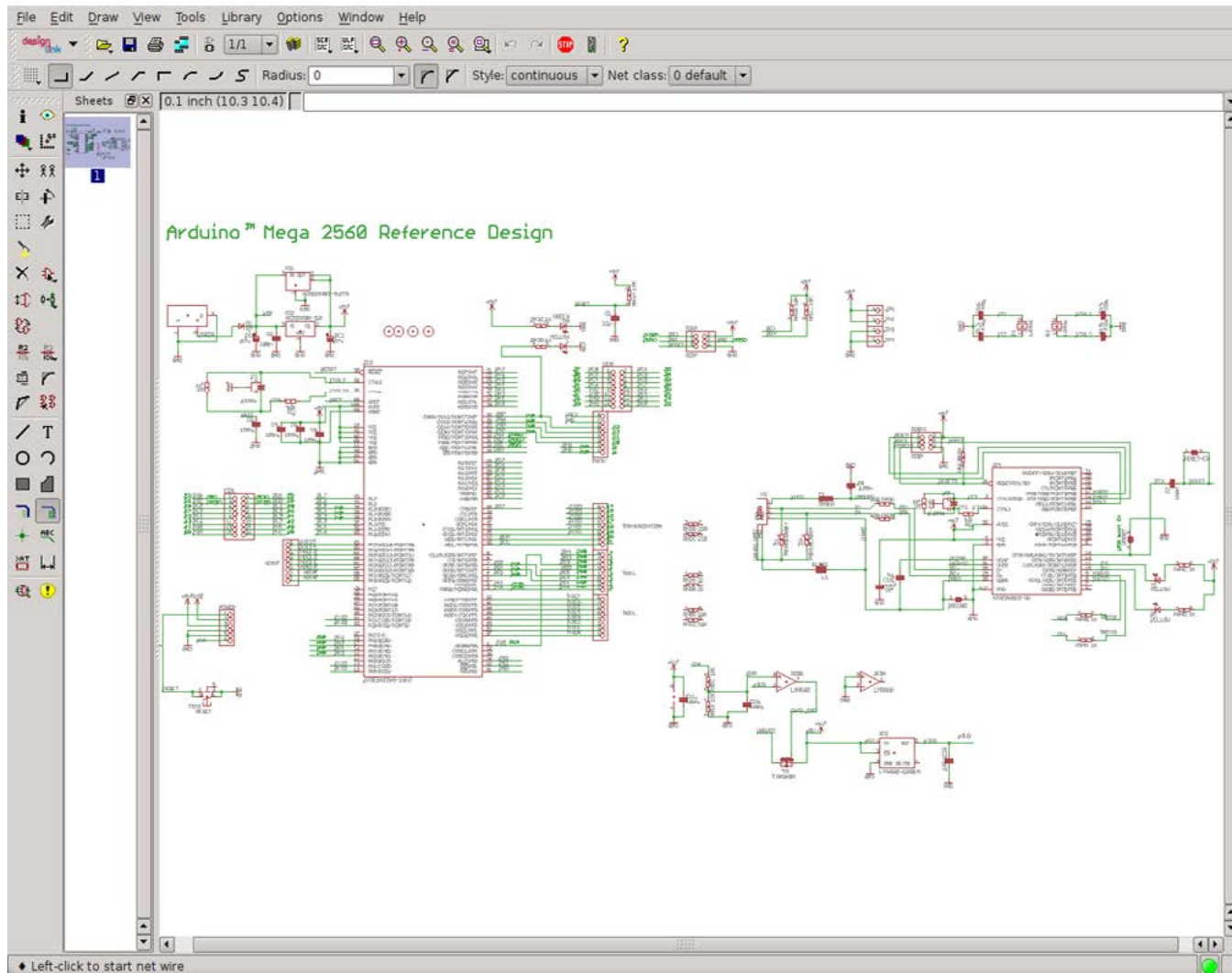
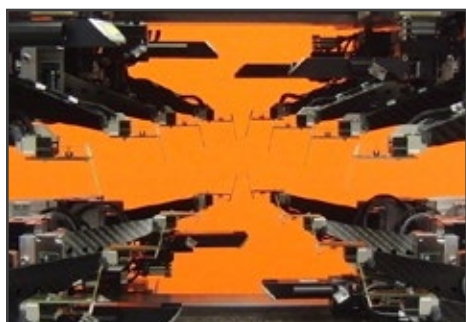


Figure 2: Schematic of the Arduino Mega 2560 reference design.

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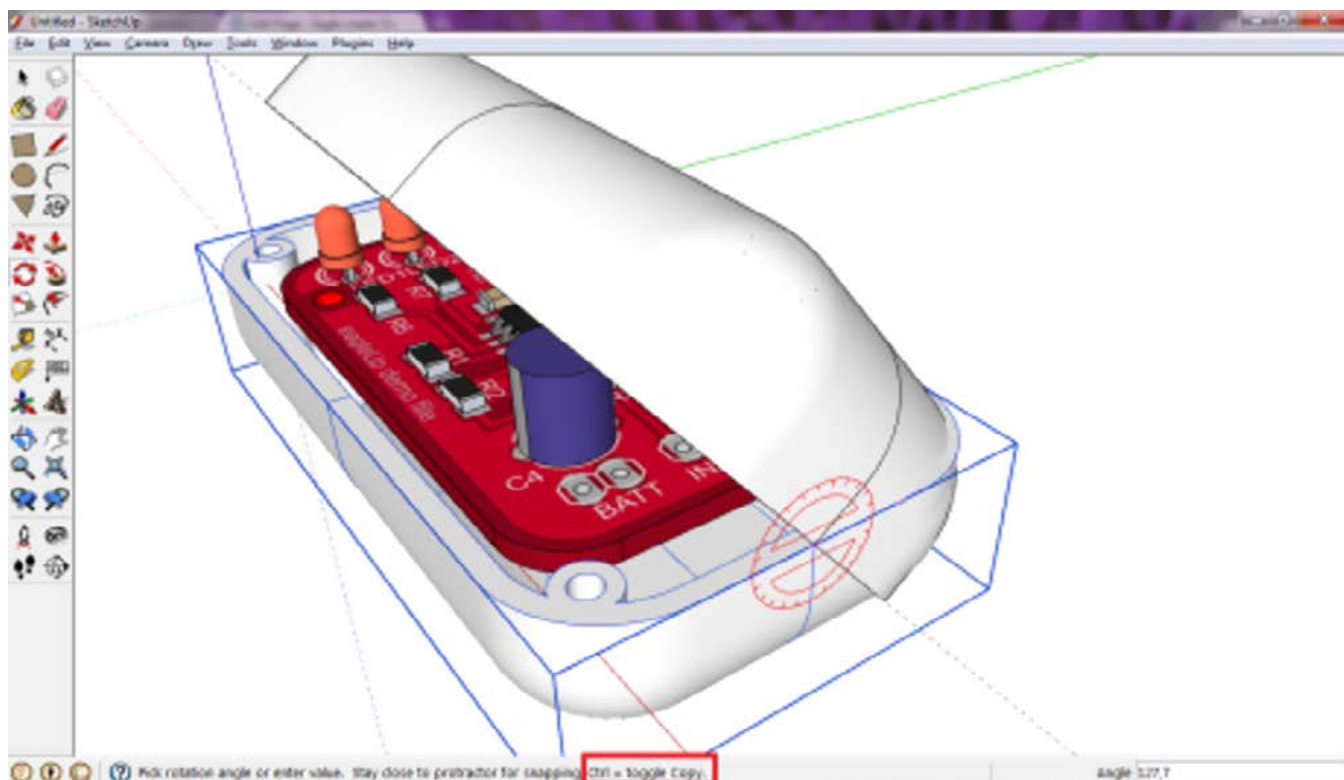


Figure 3: 3D visualisation enables users to simulate larger systems, here shown as a PCB board design in an enclosure. This saves time and cost even before prototype is built. (Source: EagleUp)

A challenge for board designers with this sort of technology is dealing with and creating the complex shapes needed to implement the components. Engineers regularly mention spending too much precious product development time creating footprints or in other parts of library management. This is a very important issue. You can't be designing a custom part for each component you want to add to your circuit.

While some third-party tools come with many libraries already, tens of thousands more are available online or in design portals from manufacturers and user shared libraries such as the element14 community. Building a custom library from scratch can take over 20 minutes per part for a small quantity, so being able to rely upon a rich pool of information validated by an active community is a significant benefit. Within complex devices, if the design is open users can specify the parts through an integrated search on a parts database with an online distributor or electronics supplier. This allows electronic design engineers to immediately search and find

parts online with parametric search to choose the right components, and they have access to a huge amount of technical information regarding the components themselves. This includes technical datasheets, links to guidance on solutions for specific applications, pricing and availability. This "virtual integration" of the design chain not only enhances design quality and designer productivity, but it reduces risks associated with misidentifying a critical component or selecting a part that is obsolete or out of stock.

Jeremy Blum, open hardware designer and hardware engineer at Google, points out:

As designs continue to get more and more complex, following best practices becomes more and more important. For novice designers, it's easy to encounter a myriad of potential design problems that may or may not be caught by traditional DFM checks. Some of the things to look for when preparing a PCB for production are problems that are only fully understood by designers who have been

doing PCB CAD for many years. Luckily, as open source designs become more common place, and as more and more professional designers join communities like element14, it becomes easier and easier for new designers to get help and tips from industry veterans. A truly community-driven design platform makes the barriers to entry lower than ever before.

Once engineers have honed in on the bill of materials that fits the project budget and are ready to fabricate the PCB, very often one has to send it off and wait. Users should be able to access instant quotations for their small volume PCB fabrication and take advantage of quick-turn prototyping service from reliable, high-quality service partners through a one-click integrated "PCB quote" link.

Prototyping is as much about mechanical fit and manufacturability as it is about functionality, quality and performance. Designers are packing more and more components onto smaller and smaller boards into smaller enclosures, placing unprecedented demands on design, analysis and simulation tools.

Ed McMahon, CEO of Epec Engineered Technologies:

Many are resorting to exotic and/or aluminium-clad PCB materials that are blind/buried via technology to fit all of the required functionality onto their circuit boards. Choose a design solution that not only easily places those features into your design, but also allows you to clearly and accurately communicate to your PCB fabricator what you are trying to accomplish. Many design products allow

you to use the features and test them in your design, but do not give the fabricator the specific data they need to manufacture the product.

While there are a plethora of commercial products available (most of them expensive to very expensive), there are relatively few that are low cost and lend themselves to the notion of "virtual design chain integration." For whichever path you choose, it is important to weigh factors such as openness and capacity for integration, ease of use, flexibility and community affiliation. It is this ease-of-use that is increasingly becoming important to balance how complex design can be accelerated while keeping the upfront design costs low.

Despite the increasing levels of semiconductor integration and readily available systems-on-chips for many applications, not to mention the increasing availability of highly-featured development boards which can be used out-of-the-box, electronics product development in many cases still relies heavily on custom PCB design. Even for one-off developments, the humble PCB still performs an important role; it's a physical platform for your design and it's also the most flexible ingredient to pull any electronics system together. **PCB**



Mark Toth is the business development manager at CadSoft Computer.

MRAM Technology Boosts Information Storage

A team from the Department of Electrical & Computer Engineering at the National University of Singapore (NUS) Faculty of Engineering has developed a new magnetoresistive random access memory (MRAM) technology that will boost information storage in electronic systems and enhance memory, which will ensure that fresh data stays in-

tact, even in the case of a power failure. The team has already filed a U.S. provisional patent.

Led by Dr. Yang Hyunsoo, the team developed a new device structure useful for the next generation MRAM chip that can potentially enhance the user experience in consumer electronics, including personal computers and mobile devices. The new technology can also be applied in transportation, military and avionics systems, industrial motor control and robotics, industrial power and energy management as well as health care electronics.



Smart Data Transfer Formats Automate CAD/CAM

by **Julian Coates**

MENTOR GRAPHICS VALOR DIVISION

With ever-increasing functionality, density, and complexity, fabricators and assembly houses must look for new ways to meet demands for high quality and on-time delivery. Once the schematic is complete and the PCB has been laid out, the complex process of transferring all the product design into manufacturing begins. The data handed off constitutes a complete definition of the designer's intentions for the product to be manufactured. From this data-model of the product the complete set of manufacturing process data, tooling and machine-files is derived. Thus, having an integrated CAD/CAM

strategy is imperative for today's sophisticated PCBs.

For decades, this design-to-manufacturing handoff has required a wide range of different files, each containing a part of the final picture, similar to a jigsaw puzzle. These files can include Gerber data with the physical layout of the individual PCB layers; Excellon drill data; netlists; and other documentation files as needed.

Once the PCB fabricator receives this set of files, they must put the puzzle back together—then perform a time-consuming verification process to determine if they have received all the necessary files to produce the PCB, and to ensure that the data is error free. Because the process has a lot of manual input, human errors often creep into the process. Fabricators es-

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timate that about one-quarter of all Gerber file sets received have errors of one form or another.

Smart Data Transfer for CAD/CAM Disciplines

The better way to transfer data between design and manufacturing disciplines is to have an intelligent manufacturing-oriented data format from the outset. Intelligent data conveys not just the physical attributes, but complete data for fabrication without the need to re-integrate the data and carry out extensive error checking.

The ODB++ format was first introduced in 1995, and since then it has been globally implemented by PCB design and manufacturing organizations both large and small. This format output is available on virtually all major CAD/CAM tools, and it delivers an integrated manufacturing oriented product-model, requiring minimal work to prepare at the fabricator before moving on to defining the manufacturing process. Although not a formal standard, it has been accepted to the point of being a de facto standard, adopted by many top-tier electronics manufacturers for many years already. The ODB++ format was created and maintained by Valor Computerized Products (now Mentor Graphics), and Mentor formed the ODB++ Solutions Alliance (www.odb-sa.com). Here, more than 5,000 members share a forum for implementers and supporters of the ODB++ format and discuss their interest and success with others.

The ODB++ format is an open, ASCII file structure containing all product data for fabrication, assembly and test in a single file, including DFM analysis (Figure 1). Because of design and data quality checks, the ODB++ file does not need the rigorous examination by the fabricator. Minimizing the amount of manual

manipulation and packaging all required data together ensures high quality and the quickest turnaround.

Viasystems' PCB fabrication division in Forest Grove, Oregon, has been an active supporter of the intelligent ODB++ data format for transferring their designs into fabrication process-preparation. Stephan Hackl, CAM lead at Viasystems, sums it up succinctly: "Our number one issue is the amount of time required to successfully import, analyze and prepare design packages for production tooling. With full utilization of intelligent ODB++ files, we can greatly reduce the amount of manual time consuming human interaction, and reduce opportunity for quality errors."

Our number one issue is the amount of time required to successfully import, analyze and prepare design packages for production tooling. With full utilization of intelligent ODB++ files, we can greatly reduce the amount of manual time consuming human interaction, and reduce opportunity for quality errors.

What ODB++ brings to the design and manufacturing table is that it produces a manufacturable design, requiring very little work to prepare at the fabricator, using intelligent data. This combination of a manufacturable design and the intelligent data means products are fabricated in the minimum cycle time and significantly improves the quality risk in the new product introduction (NPI) phase of the product lifecycle.

Gerber Obsolescence Drives the Need for a New Data Format

The Gerber format has been used since 1980 and, while containing much of the graphical image information required for initiating PCB fabrication, it has some significant limitations. For example, drilling information is not contained in the file and is communicated with a separate file in another format, usually Excellon. Significantly, there is no information about how the PCB layers stack up, and there is no information about nets; all that comes in separate files or documents that have to be reintegrated by the fabricator. In recent years, the use of buried and blind vias, and complex

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sequential lamination techniques, combined with much greater diversity of surface finish requirements, have all expanded the problem of CAD/CAM data exchange—taking it even further away from the scope of traditional formats such as Gerber, Excellon and netlists.

Gerber files require a great deal of manual intervention before fabrication-ready process-tooling can be produced. The fabricator must manually examine each file and determine how the layers in the stackup fit. In addition, Gerber files can contain syntax errors or precision errors

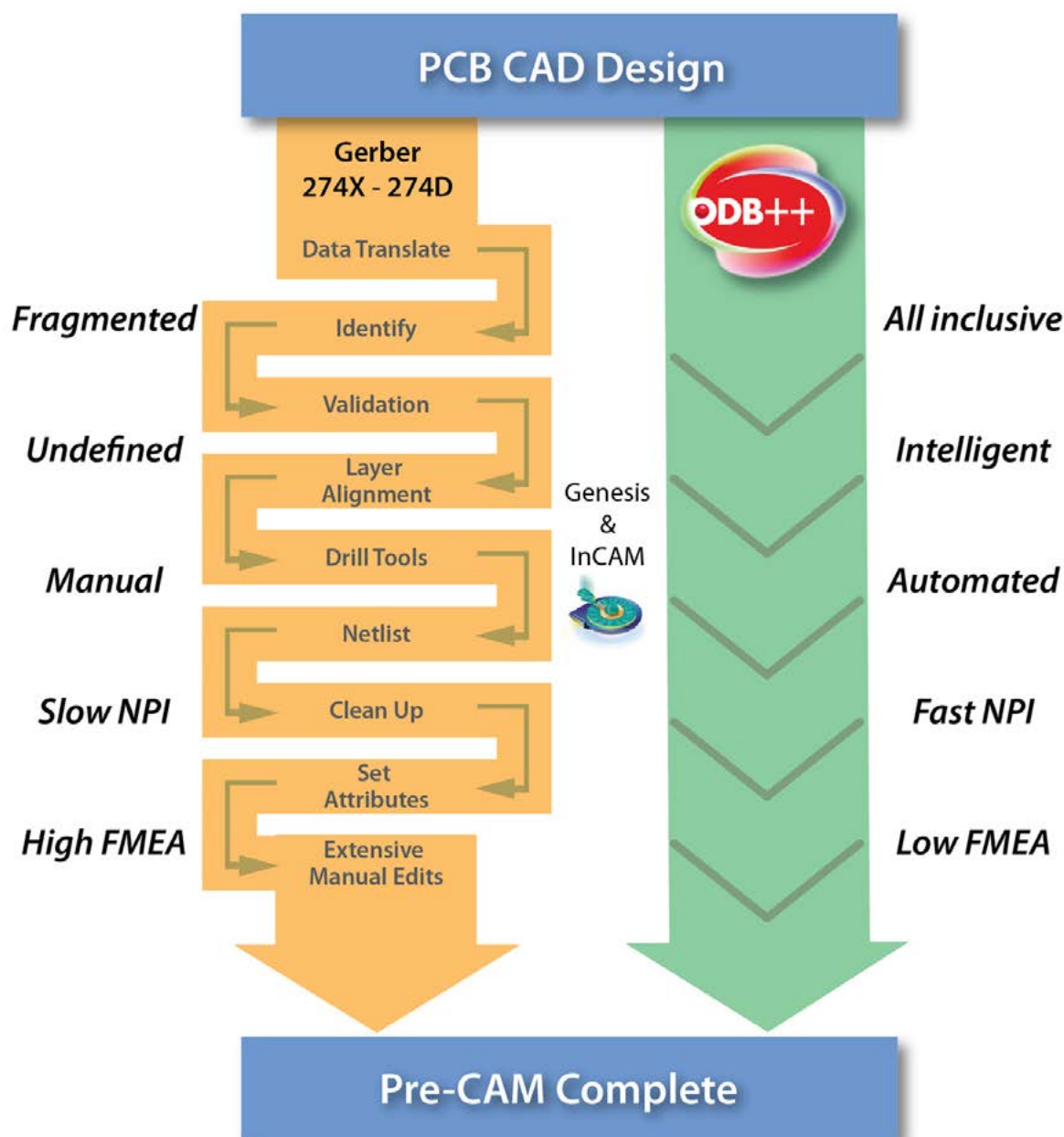


Figure 1: The traditional data set supplied to fabricators contains many manual steps, each of which can be error prone and induce unnecessary risk into the PCB manufacturing process. Using the intelligence of ODB++, virtually all steps are processed electronically, producing a low risk, high quality data set that makes fabrication virtually error free, and significantly reduces new product introduction time.



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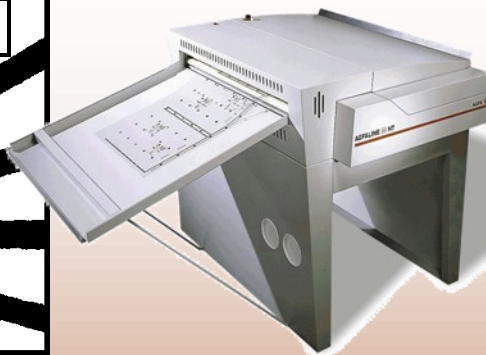
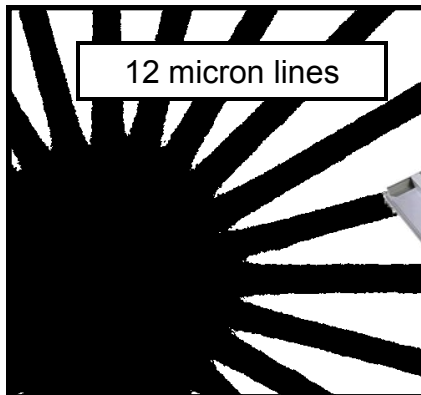
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from rounding. The time and effort required to extract a complete PCB product model from the Gerber, drill, netlist and document-information is significant.

Success is achieved through a combination of a completely-defined format, tools that work with it, and an organization behind it that supports customer deployment and ensures the format's vitality. The ODB++ format supplies the fabricator with a complete set of data. The files contain not only stackup information, but drilling, masking, net data and a wide range of intelligent attributes that make separate drawings unnecessary. The complete manufacturing-level definition of the product is contained in one self-contained file structure. Figure 1 graphically demonstrates the advantage of supplying ODB++ data to the fabricator instead of the outdated Gerber-type data. The low failure mode and effects analysis (FMEA) means that the quality of the fabricated board is also improved when using the full capability of ODB++.

It's important to note that a complete ODB++ file set is necessary to take full advantage of the automation capabilities of the format. This is best realized by defining a complete data transfer process. This process should include DFM analysis to check the fit of the product to the intended manufacturing process, and full communication of all appropriate attributes in the file set. Submitting just a partial file set to the PCB fabricator will not allow him to take advantage of the significant intelligence that ODB++ is capable of providing. Once the full set of files has been specified, those files should then be compressed as

a single .tgz file for the fabricator. Fabrication software automatically recognizes the .tgz file and understands the file structure and how to use those files.

Advantages for the Fabricator

There are good reasons why vendors such as Viasystems, a provider of complex multi-layer PCBs and electro-mechanical solutions to OEMs, based in St. Louis, Missouri, are fond of intelligent ODB++ data. It saves the company front end time, money, and allows a faster response to the customer. ODB++ helps ensure on-time delivery of a high quality end product. Gerber data, on the other hand, requires a multistep workflow just to get a set of data from which the PCB fabrication-process preparation can proceed.

At any place in the workflow, they may discover errors or omitted data, which can mean multiple communications with the customer to correct errors or get additional data. On average, about 25% of the data packages they receive have issues related to:

- Missing layers, fabrication drawings, drill files, etc...
- Netlist format violations
- Netlist exception violations

Kent Balius, Viasystems' VP of global front end engineering, has collected extensive data to support his preference for ODB++ over any other format: "Standard Gerber input takes us one to two hours just to import, analyze and prepare data for production CAM tooling. While ODB++

ODB++ Benefits for the PCB Fabricator
1. Import and export diagnostics are significantly reduced compared to Gerber
2. Errors can be identified and communicated to the customer much earlier in the process
3. Eliminates format errors and net exceptions that are common with Gerber
4. Fabricator can be allowed to see actual net name used by customer, easing the process
5. Less data is required for handling positive planes

Table 1.

has been around for several years, the designers and the fabricators have not taken advantage of integrating the potential intelligence, such as incorporating the many attributes available which can drive automation and reductions of operator manual interaction. The ODB++ with these intelligent attributes included can help reduce up to 25% (1–2 hours) of our pre-CAM environment, depending on the complexity of the design. It is a single file with intelligent attributes, and an all inclusive data package.”

Table 1 is a list of significant ODB++ benefits over Gerber across the entire fabrication process.

Advantages for the PCB Customer

The advantages of ODB++ data are not limited to the fabrication company. The customer or designer can realize significant benefits as well. These benefits can save significant cost and design time, and even result in getting the product to market more quickly. More importantly, the new product introduction (NPI) quality risk to the PCB customer is substantially reduced. The higher-quality data supplied to the fabricator accounts for that risk reduction, and it propagates into board assembly as well.

Table 2 lists the more significant advantages of using ODB++ from the perspective of the PCB designer.

In addition to the usual set of information

that is conveyed in ODB++, many attributes can be communicated as well, and automatically. Attributes such as impedance, plugged vias, surface finish, and others can be included in the ODB++ data, automatically read and understood by the fabricator. Users can also assign user-defined attributes of characteristics to easily communicate this information both internally and to suppliers that have been chosen to receive the definition of the attribute.

IP Protection

While a great deal of product design information is contained in the ODB++ file sent to the fabricator, there is no risk of disclosing the design IP of the product. ODB++ can carry net names, inner layer information, and component data up to the level that the user feels appropriate for transmission into manufacturing, according to how the CAD or DFM tool is configured to create and manage the data. The intention of ODB++ is to give all necessary information to manufacturing, in an intelligent and integrated data-structure, no more and no less, enabling the most efficient manufacturing.

Lean NPI for Optimum Efficiency

The accepted best-practice for the NPI flow is, as with other aspects of manufacturing, to be Lean. Lean NPI means elimination of waste in the NPI process by ensuring a right-first-time

ODB++ Benefits for the PCB Designer

1. Reduced overall risk of errors in fabrication and assembly
2. Intelligent data means more on-time deliveries of fabricated and assembled PCBs
3. Less time spent correcting errors and resending data sets because of missing files
4. Reduction in the chance of wrong data passing into manufacturing and creating rejects, lost time and money
5. Less chance of incorrect file definitions (stackups and polarity errors)
6. Elimination of the fairly common Gerber problem of drill pattern misalignment
7. Quicker feedback from fabrication and assembly engineers and quicker resolution of errors

Table 2.

philosophy. The first step in Lean NPI implementation is to shift the DFM validation process from the manufacturer upstream into the design process, while still using the manufacturer's DFM rules, thus ensuring minimal engineering changes after hand-off to manufacturing. A well-known rule-of-thumb indicates that the cost of an engineering change goes down by 10x for every step of "left-shift" taken in the product lifecycle back towards the early stages. Thus, finding and fixing DFM problems during design, not afterwards in manufacturing, offers a substantial opportunity for cost and time-saving. New generations of PCB design and NPI software offer close integration of DFM analysis into the layout process, thus enabling the PCB designer to ensure that his product matches the constraints of the intended manufacturing process while he is laying out the board, not af-

terwards—when the most elegant solutions to DFM problems are no longer available due to all most aspects of a product-design now being fixed and committed to. The second dimension of the Lean NPI best-practice is the hand-off of a complete and well-integrated model of the product to be manufactured, such that all wasted and error-prone work to rebuild the product-model prior to process-preparation is avoided.

The Lean NPI flow

Running a Lean NPI process comprising DFM tools integrated into the design, coupled with the industry-proven intelligent ODB++ data, can cut engineering change orders (ECOs) in half and errors by even more—and ensure that what is manufactured is precisely what the designer intended.

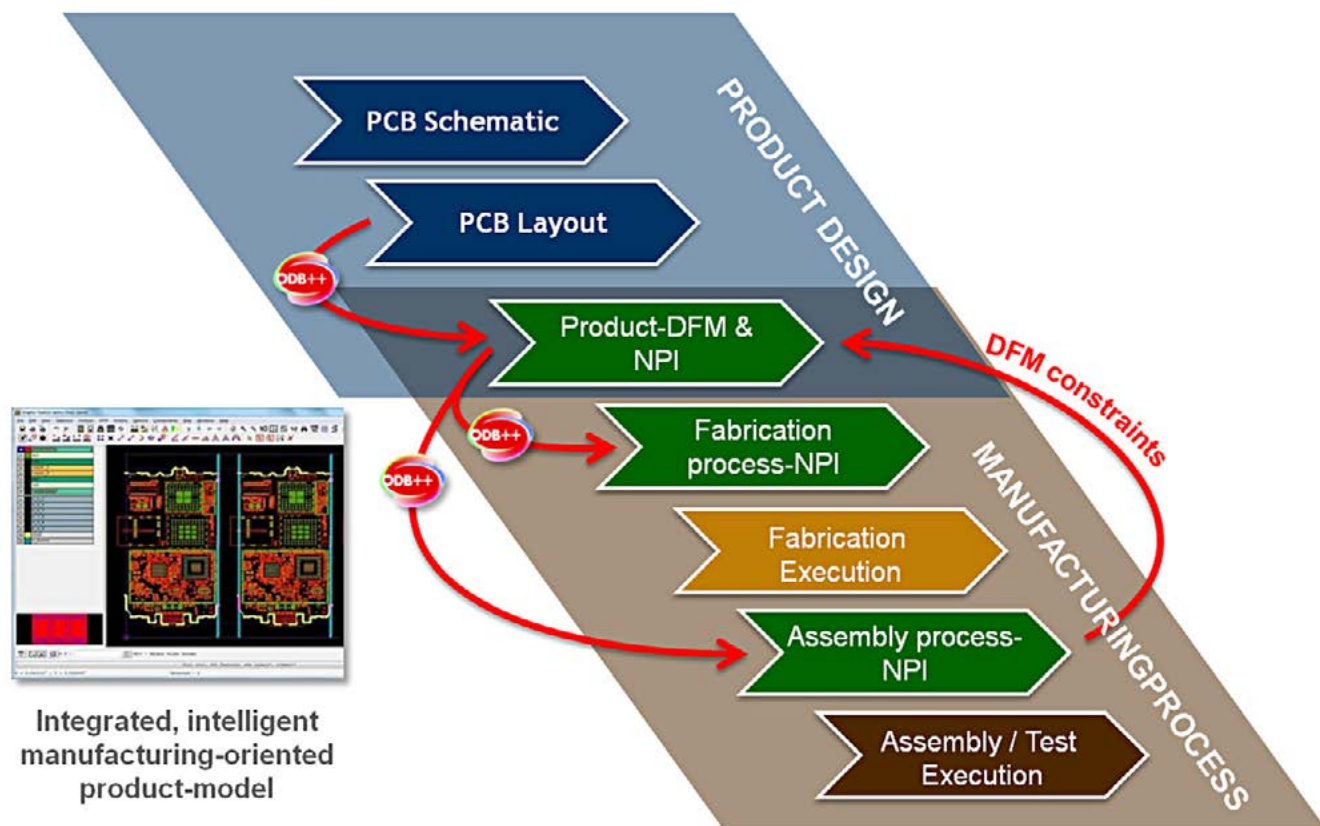


Figure 2: The Lean NPI Flow eliminates waste in the NPI process by ensuring a right-the-first-time philosophy. CAD, NPI, DFM or CAM processes must each be able to generate or input ODB++ data that is complete and of maximum intelligence, with NPI functionality that can make automatic use of the integrated data content for minimal human error and maximum process-repeatability.

To experience the maximum benefits of the Lean NPI process, the designers, NPI engineers, fabricators and assembly manufacturers must all play their part so to avoid discontinuities in the value-chain. CAD, NPI, DFM or CAM processes must each be able to generate or input ODB++ data that is complete and of maximum intelligence, with NPI functionality that can make automatic use of the integrated data content for minimal human error and maximum process-repeatability.

The significant advantages and automation abilities associated with the ODB++ format make it the clear choice for manufacturing data transfer in the future. Fewer errors mean less expense, fewer re-spins, and quicker turnaround on PCB fabrication, assembly and test. The integrated DFM data helps ensure that board assembly will proceed without any glitches to send the process back to design.

Balius wishes that more of his customers would provide intelligent ODB++ files, which

would benefit both Viasystems and their customer. "First, I don't think some customers know how simple it is to generate an intelligent ODB++ files with integrated attributes in their design software. Second, I have heard from some customers that they are concerned about sending their IP to the fabricator. In truth, after our data reintegration work with traditional formats, we end up with virtually the same exact information as ODB++ and we are not getting the core design-IP from the customer." **PCB**



Julian Coates is the director of business development for Mentor Graphics Valor division. Since joining Mentor Graphics Valor division in 1994, Coates has fulfilled a number of roles including managing director of Valor's European subsidiary, followed by product management, marketing and business development.

VIDEO INTERVIEW

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Martyn Gaudion reviews a successful productronica with lots of interest from PCB fabricators in Europe and the UK. Polar launched Atlas, a testing system for accurate signal loss measurement in multi GHz PCB fabrication.



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PCB007 Market News Highlights



CEA: Rise of Connected Health & Wellness Devices

The Consumer Electronics Association has released a comprehensive new report, "The Connected Health and Wellness Market," quantifying the dramatic growth in sales of connected health and wellness devices. The report defines the market, lays out key market growth drivers and challenges, and highlights important technology trends and regulatory issues.

PC Monitor Market: Positive Growth in Q3

Total worldwide PC monitor shipments were more than 35 million units in the third quarter of 2013, an increase of 4.5% compared to the previous quarter and 1.2 million units more than forecast, according to the International Data Corporation (IDC) Worldwide Quarterly PC Monitor Tracker.

CES 2014: A Preview from Dan Feinberg

"I'm heading to Las Vegas again for CES; this is my 16th year attending this exciting show and I have seen it change quite a bit over the years. This year change seems to be accelerating. Gone are the huge Microsoft booths and gone are many of the top-tier sub assembly suppliers," says Columnist Dan Feinberg.

Smartphone AP Market Up 31% in Q3 2013

According to the report, Qualcomm, Apple, MediaTek, Samsung and Spreadtrum grabbed the top-five revenue share spots in the smartphone apps processor market in Q3 2013. Qualcomm continued its lead in the smartphone applications processor market with 53% revenue share, followed by Apple with 18%.

Memory Sector Drives Semiconductor Sales in 2013

Following a 2.5% decline in 2012, the global semiconductor market has regained its footing in 2013 with revenue set to expand by nearly 5% because of the strong performance of the memory sector.

Global semiconductor sales in 2013 will amount to \$317.9 billion, up 4.9%.

Consumer Sentiment on Overall Economy Flat in December

Consumer confidence toward the overall economy and technology spending in December both remain steady with last month's elevated sentiment levels, according to the latest figures released by the Consumer Electronics Association.

December Manufacturing ISM Report: PMI at 57%

Bradley J. Holcomb, CPSM, CPSD, and chair of the Institute for Supply Management Manufacturing Business Survey Committee, comments, "The PMI registered 57%, the second highest reading for the year, just 0.3 percentage point below November's reading of 57.3%."

Consumer Electronics Market to Reach \$1.6 Trillion by 2018

Consumer Electronics market to witness a value of US \$1.6 trillion by 2018. Geographical analysis shows the highest Compounded Annual Growth Rate (CAGR) of 17.6% is foreseen from Asia-Pacific region during the analysis period 2011–2018.

SSV Sales to Reach 55 Million Units Annually by 2022

Stop-start vehicles (SSVs), which eliminate idling by shutting off the engine when the vehicle is stationary and restarting it automatically when it is time to move, offer a portion of the fuel economy benefits of hybrid vehicles at a fraction of the cost premium.

Strategic Analysis of European EMS Industry 2012-2017

This is the eleventh edition of the European Electronic Manufacturing Services Industry report and updates both the tenth edition published in September 2011 and the first edition of the European Electronic Manufacturing Services Industry—Strategic Market Analysis published in September 2012.



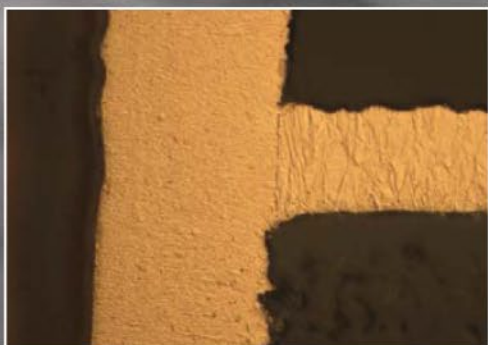
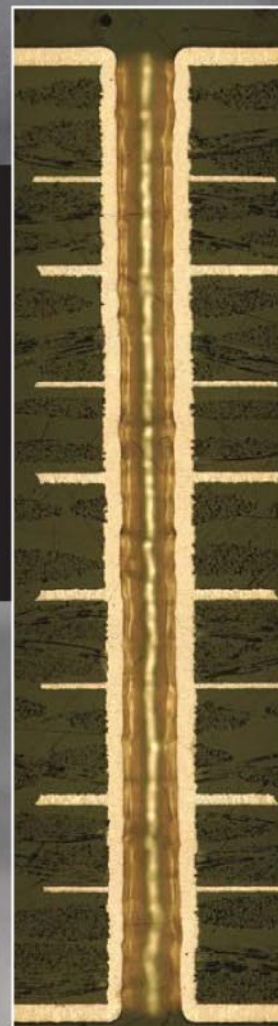
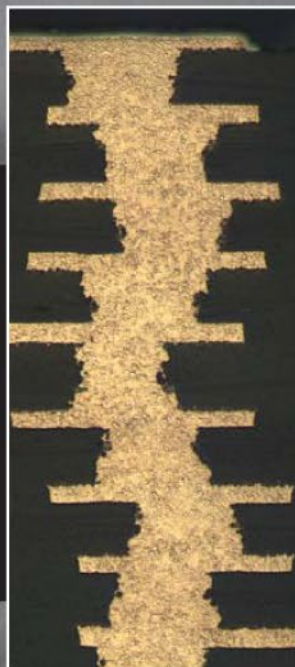
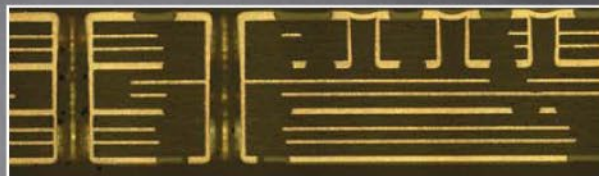
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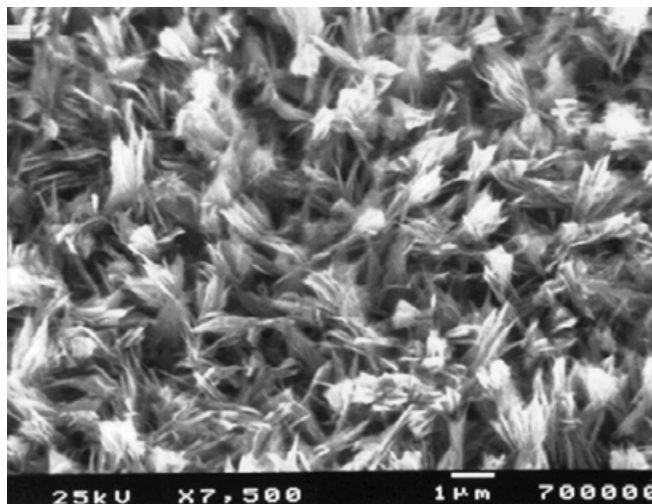


Figure 1: Conventional oxide chemistry formulation.

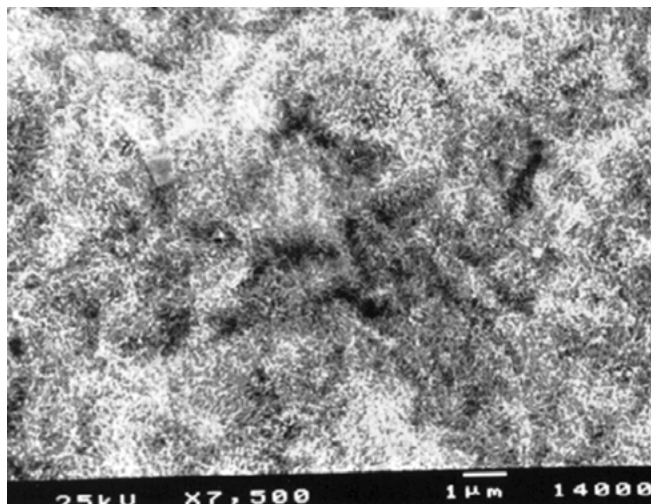


Figure 2: Reformulated oxide chemistry, more applicable to polyimide.

the bond significantly. A properly passivated copper surface will resist water formation, thus eliminating delamination from occurring (with respect to moisture). Note this warning: A properly passivated copper surface is very important. In a future column, I will discuss this subject in more detail, including what constitutes a poorly passivated copper surface.

While it is true that most of the early market penetration for conventional oxide coating rested in FR-4 materials, the need for higher reliability for the military/aerospace segment necessitated a slightly different approach. Specifically, the military/aerospace market used polyimide resin materials due to the need for higher reliability. In effect, the temperature profile employed for polyimide multilayer lamination is much more severe than that of FR-4. It was determined that when fabricators used conventional black oxide, the bond strengths deteriorated significantly on polyimide resins compared to FR-4. It was assumed that the large fragile oxide crystals of the standard oxide coating easily fractured during multilayer lamination. With the higher temperatures and pressures inherent in polyimide fabrication, the oxide crystals easily fractured significantly reducing the bond strength. Higher lamination pressures and temperatures also share some the blame for the failures to the polyimide itself. It is well known that polyimide cured materials are more brittle

than FR-4 resins and thus exhibit a much lower bond strength in general. However, the solution to this issue was to develop an oxide coating that was thinner and denser (Figure 2). As a result of a modification of the chemistry, the oxide coating was much denser, thinner and the copper oxide crystals were much shorter. All of these attributes combined to provide a superior heat resistant bond not only for FR-4 but for polyimide as well.

The reformulated oxide chemistry was designed to limit the oxide crystal growth and thus the overall thickness of the coating. Thin and more uniform coatings provided a more stable innerlayer bond between the copper and the resin. So in this case, thinner is better. When the oxide chemistry is properly formulated, the coating is self-limiting. Essentially the structure and thickness of the oxide coating is dependent on several factors:

- Operating temperature of the oxide solution
- Concentration of the chemicals' reactants of the oxide solution
- Dwell time in the solution

From my standpoint, the goal is to grow the oxide structure quickly and uniformly. I want to avoid low temperatures and excessive dwell times that can leave too thick of an oxide coat-

ing. Essentially this is a matter of reaction kinetics. The key chemical materials for the oxide process are sodium chlorite and sodium hydroxide. In addition, a buffer in the form of trisodium phosphate is also added to the working solution. These chemicals in the proper concentrations along with operating temperature ultimately control the thickness and uniformity of the oxide coating (and ultimately the peel strength). If a finer grained, short oxide needle structure is desired (Figure 2), then keep the sodium hydroxide content at 0.6 N or less (not more) and the sodium chlorite concentration greater than 80 grams per liter.

One of the control methods used is to employ a standard copper foil coupon of known surface area. It is used much like a rate coupon on the electroless copper plating line. Essentially one is measuring weight gain. The recommended procedure is as follows:

Procedure

- A. Process the copper coupon down the normal oxide production line.
- B. Dry the coupon completely, bake at 110°C (230°F) for 10 min, then cool at room temperature for 10 minutes.
- C. Weigh the copper coupon and record the weight (X) to the nearest 0.001 g.
- D. Immerse the coupon in 20% sulfuric acid solution at room temperature and strip all oxide off of the coupon. Do so for three minutes.
- E. Rinse and dry the coupon completely, bake at 110°C (230°F) for 10 min, then cool at room temperature for 10 minutes.
- F. Reweigh the copper coupon and record the weight (Y) to the nearest 0.001 g.

Calculations

- A. Weight gain (Z) = X – Y
- B. Coupon area (A) = length x width x 2 (cm²)
- C. Weight gain per coupon area (mg/cm²) = $\frac{Z \times 1000}{A}$
- D. Weight gain per coupon area (mg/in²) = $\frac{Z \times 6452}{A}$

Oxide Characterization	Weight Gain	Comments
Heavy black oxide	0.60 mg/cm ²	Generally lower peel strengths, but ok for FR-4
Mid-range oxide	0.45–0.60 mg/cm ²	Needed for higher performance FR-4 resins
Light brown oxide	0.25–0.45 mg/cm ²	Ideal for polyimide coating; thin and actually looks light brown to bronze in color

Table 1.

The recorded weight gains will serve as a good process control metric and should be measured once per shift. Keep in mind that the more brittle resins such as polyimide perform better in terms of peel strength with thinner oxide coatings as opposed to very thick coatings. A guideline for measured weight gains is shown in Table 1. Keep in mind the thinner, lighter coatings are favored for polyimide, while the heavier coatings can be used with FR-4 resins.

If the sodium chlorite concentration drops or the sodium hydroxide concentration increases, there can be a significant increase in the oxide weight gain. What many people don't realize is that over time, the combination of high temperatures, sodium hydroxide and oxygen will form sodium carbonate. The concern here is that sodium carbonate contributes to the total alkalinity of the oxide solution. If not accounted for, the carbonate will give a false reading of the sodium hydroxide content. Sodium hydroxide influences the oxide crystal growth and overall structure.

In the next Trouble in Your Tank, I will cover more in-depth information related to oxide chemistry and process control and present the latest thoughts on pink ring and what it really means. **PCB**



Michael Carano is with OMG Electronic Chemicals, a developer and provider of processes and materials for the electronics industry supply chain. To read past columns, or to contact the author, [click here](#).

PCB007 Supplier/New Product News Highlights



Multiple PCB Manufacturers Choose atg Flying Probe Tech

atg Luther & Maelzer GmbH, confirms multiple new orders for high-speed bare board testing technology. Three leading PCB manufacturers and one leading outsourcing company have recently released orders for atg's A7 test equipment systems.

PCB Solutions Nets Another Perfect Score on Supplier Review

"Our internal processes provide consistency for our customers and the quarter after quarter of perfect scores with companies like MAC prove our system is working," said Greg Engstrom, president of PCB Solutions.

Isola Expands Production of I-Speed Material Into Asia

The company announced it has successfully transitioned the manufacturing of its low-loss, I-Speed material to Asia. Ray Sharpe, president and CEO, commented, "In addition to reducing the cost of I-Speed in Asia, this transition will reduce lead times and enables our customers to be more responsive to the market."

Sunshine Employs Frontline's InPlan Engineering System

Orbotech Pacific Ltd., the Asia Pacific subsidiary of Orbotech Ltd. has announced that Shenzhen Sunshine Circuits Technology Co., Ltd., a leading PCB producer in Shenzhen, China, has fully applied the InPlan engineering system developed by Frontline PCB Solutions.

Park Electrochemical Reports Sales Drop in Q3

Park Electrochemical Corporation reported net sales of \$39,678,000 for the third quarter ended December 1, 2013 compared to net sales of \$41,265,000 for the third quarter ended November 25, 2012. Park's net sales for the nine months ended December 1, 2013 were \$127,613,000 compared to net sales of \$133,741,000 for the nine months ended November 25, 2012.

Burkle Gets Capital Increase with New Investor

The plant manufacturer Robert Burkle GmbH announces the arrival of the private equity company Nimbus, based in Zeist, the Netherlands. The investor with an interest in long-term investments has acquired a stake with a significant capital increase.

Atotech Details New Photoresist Adhesion Process

CupraEtch DT25, Atotech's new photoresist adhesion process, is a very suitable pre-treatment for dry film and liquid photoresist. It features tracer elements for an optimized process control and is ideal for high-volume manufacturing.

MorTech Offers Wide Range of PCB Mfg Products to U.S.

Mortech President Lino Sousa states, "We strive to provide our customers with unparalleled products, service and support. Superior quality is of the utmost importance so we've partnered with some of the top suppliers in the industry in order to afford just that."

LPKF Offers New UV Laser Depaneling Systems

The MicroLine 2000 Series benefits from a low-stress UV laser source, which provides two main advantages: The elimination of mechanical stress and the ability to process a wide variety of circuit materials, including flexible, rigid, and rigid-flex substrates.

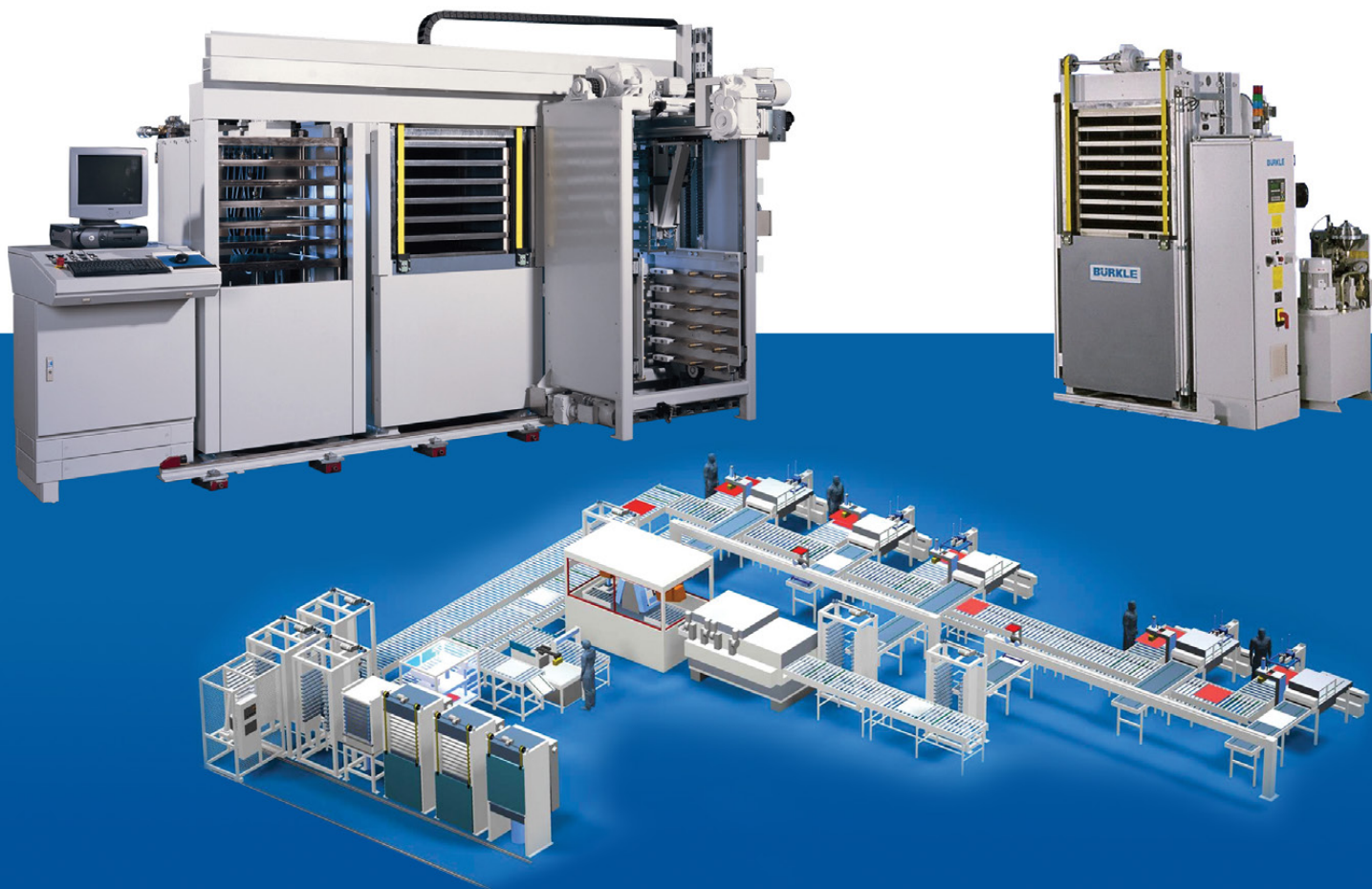
Court Rejects Patent Infringement Claim Against Atotech

The second instance of the Taiwan Intellectual Property Court confirmed that Atotech's Stan-natech® process and equipment were not affected by a competitor's patent. The judgment confirmed the first instance's rejection of a patent claim against Atotech after a competitor took legal action for the alleged infringement of one of its patents.

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Phototools, Part C

by Karl Dietz

KARL DIETZ CONSULTING LLC

The objective of this column is to familiarize the reader with silver halide phototools.

Halides are salts that contain an ion from the group of elements called halogens, Group 7 of the periodic table. The word halogen is derived from the Greek words for "salt" and "to generate." The halides found in silver halide phototools are typically chloride or bromide and sensitive to UV radiation. When exposed to UV radiation, nuclei of metallic silver are formed and can be grown into larger silver crystals by treating them with a reducing chemical.

Silver halide films are much more versatile than diazo films and can be used in a broader range of applications than the diazo materials. High-speed films are typically 100,000 times faster than diazo films, allowing them to be used in low light and high-speed recording applications such as photo plotters, cameras, and step-and-repeat machines.

Figure 1 shows silver halide crystals. The silver halide crystals used in silver halide films are composed of a combination of silver bromide, silver chloride, and silver iodide. They are typically cubic or triangular in shape with edges approximately 200–300 nm long. A crystal of this size will contain about 10 million atoms. To each crystal are added a few atoms of a sensitizing material, such as gold or sulfur, to form a sensitivity center.

During exposure, the crystal absorbs a photon of light, and the energy is used to form an atom of metallic silver at the sensitivity center. The absorption of more photons increases the number of silver atoms formed. When the number of metallic silver atoms exceeds a threshold of between four and 10, the crystal is said to have a latent image. It is this latent image that allows the entire crystal to be turned to metallic silver during development. The amount of exposure the film receives must be adjusted to give optimum results. If the original is negative appearing or the film is exposed on a plotter,

too much exposure will yield lines and features (dark areas) that are too wide. Too little exposure will produce features that are too narrow and have low optical density. Select an exposure which accurately reproduces the line width of your original as measured with a microscope.

Figure 2 shows the structure of a typical silver halide film. The various layers include an overcoat to provide protection against scratches and abrasions. Most films also contain a small amount of matte in this layer to permit faster and more uniform drawdown in a vacuum

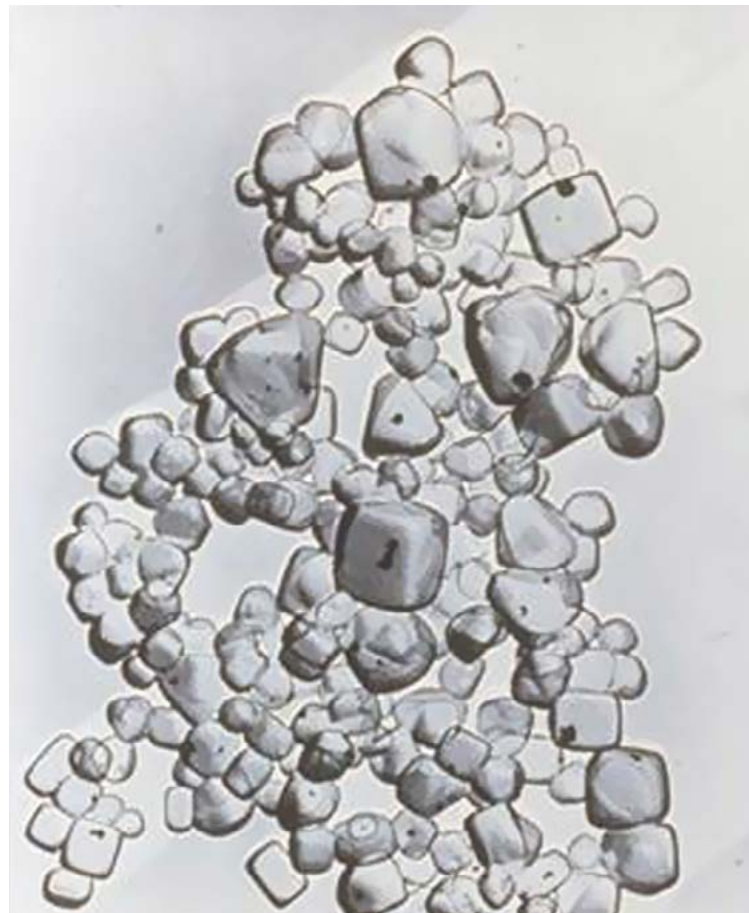
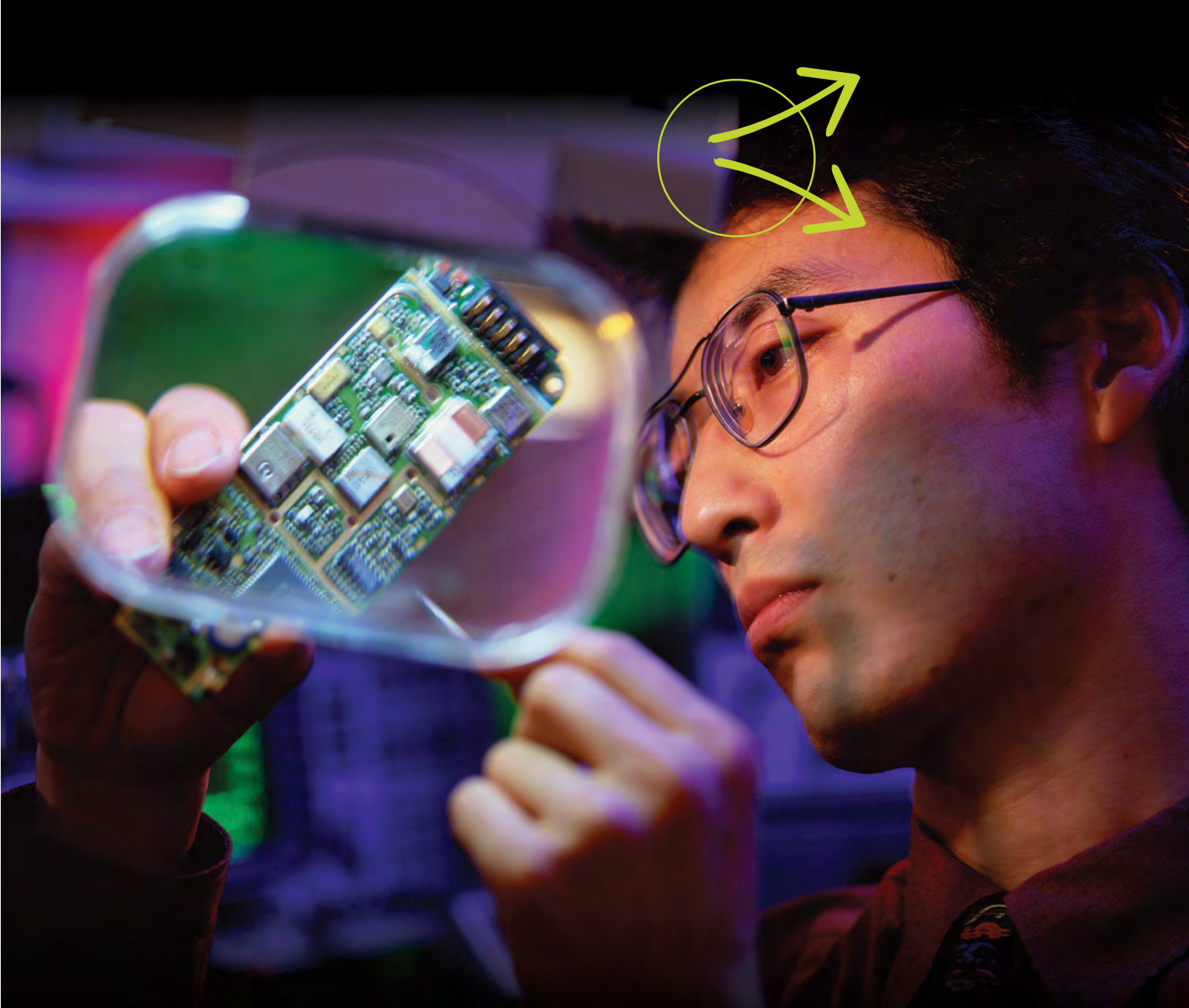


Figure 1: Silver halide crystals.



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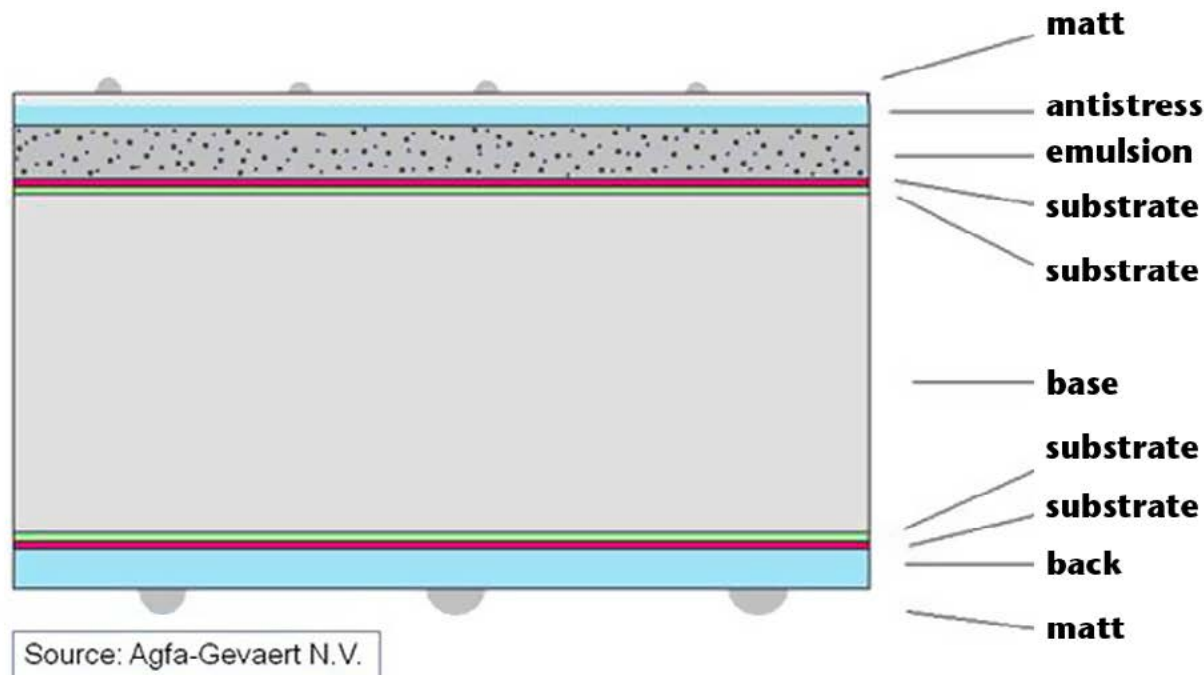


Figure 2: Example of a silver halide film structure.

frame. The emulsion layer contains the light-sensitive silver halide crystals. This layer is where the visible image is formed during exposure and processing. It consists of a uniform dispersion of silver halide crystals in gelatin. The sub-coat is a series of very thin coatings which allow the gelatin to adhere to the base. The base is usually a 7-mil thick polyester film, though glass has been chosen for use in some applications. It is the base which gives the film its strength, durability, flexibility, clarity, and dimensional stability characteristics. Another sub-coat is required to provide adhesion to the backing gelatin. The backing is a layer of gelatin containing a colored anti-halation dye and anti-static agents. Its purpose is to improve image quality, help control curl, and minimize dirt pick-up. The drawing you see here is not to scale. Typically, the base is 7 mils (175 μm). The coated layers, including the backing, add only 0.2–0.3 mils (5–7 μm) to the total thickness.

Figure 3 shows just one crystal that has formed some metallic silver.

The first processing step is called development (Figure 4). Here, the exposed silver halide crystals are converted to metallic silver. The la-

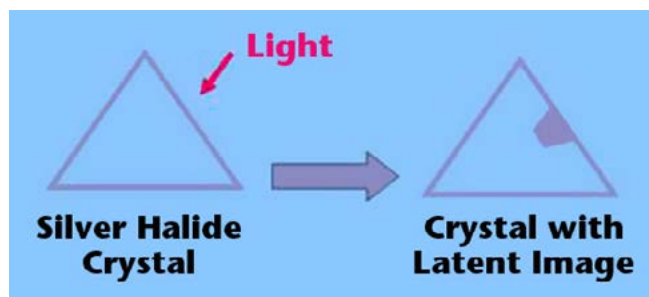


Figure 3: Formation of latent image.

tent image acts as a catalyst for this reduction reaction, thus providing a means to distinguish between exposed and unexposed crystals. Once the reduction of the crystal starts, the entire crystal is converted, yielding an amplification factor that can be as much as 10 million! The amount of development a film receives in a specific application must be adjusted to give optimum results. Too much development will produce lines that are too fat and fuzzy. It may also produce high background fog levels in some systems. Too little development will give you skinny lines with low optical density. Usually,

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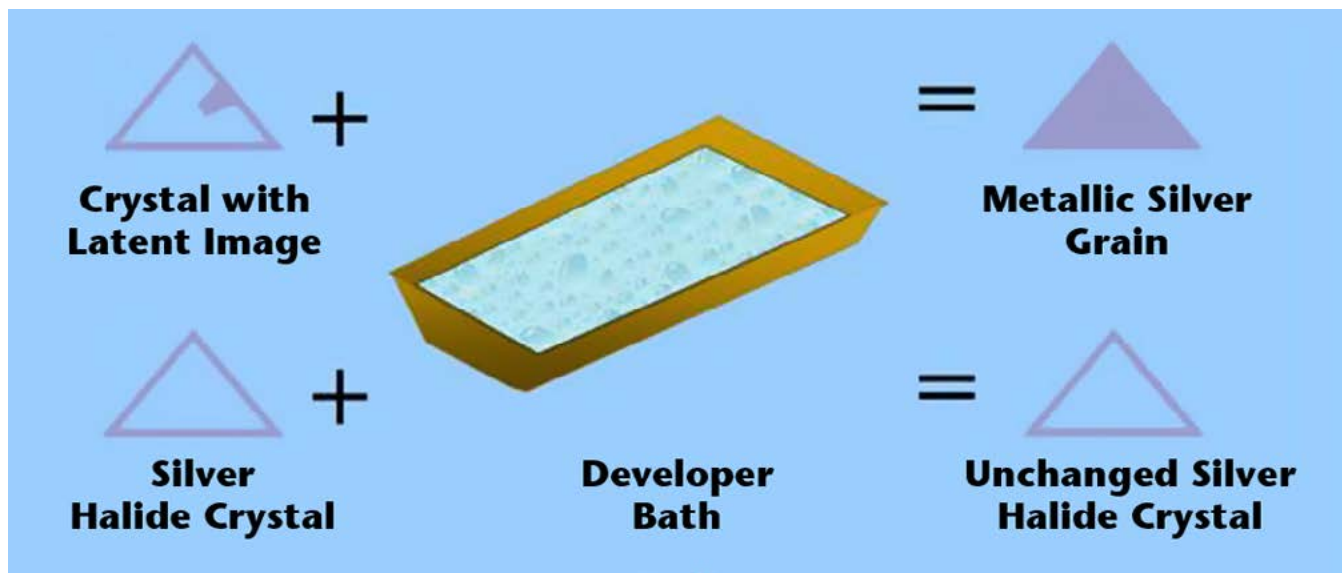


Figure 4: Development of silver halide film.



Figure 5: Cross-section after development.

the easiest and most appropriate control of development is adjusting the processor throughput speed. The optimum development conditions for films and chemicals in most applications are provided in the technical data sheets provided by the supplier.

Looking again at the film cross-section (Figure 5), one can see that the silver halide crystals that were struck by light have been converted to metallic silver. Unexposed crystals remain unaffected by the development step. Although we have an image at this point, it is not yet permanent.

To make the image permanent, the film must go through a fixing step (Figure 6) to remove the

remaining silver halide crystals. During fixing, ammonium thiosulfate is used to convert these crystals to several soluble silver salts which are removed from the emulsion. The metallic silver image is unaffected by this step. Within reason, it is not possible to give a film too much fixing. Under-fixing will produce films which in time will turn gray in clear areas. In extreme cases of poor fixing, the film will exit the processor exhibiting patches that appear milky white where they should be clear.

After fixing, the metallic silver image remains where there was exposure. The gelatin binder is still in place throughout the entire structure; it is not removed at any time in this process.

A clarification of terms may be in order. The word "development" means different things in dry film resist processing and in phototool processing. In phototool processing, development amplifies a chemical change that started during exposure. In dry film resist processing such initial chemical change and its amplification all happen during exposure. In dry film resist processing development means the removal of unexposed resist (i.e., for negative working resist), a step that can be compared to "fixing" in phototool processing where unexposed silver halide is removed.

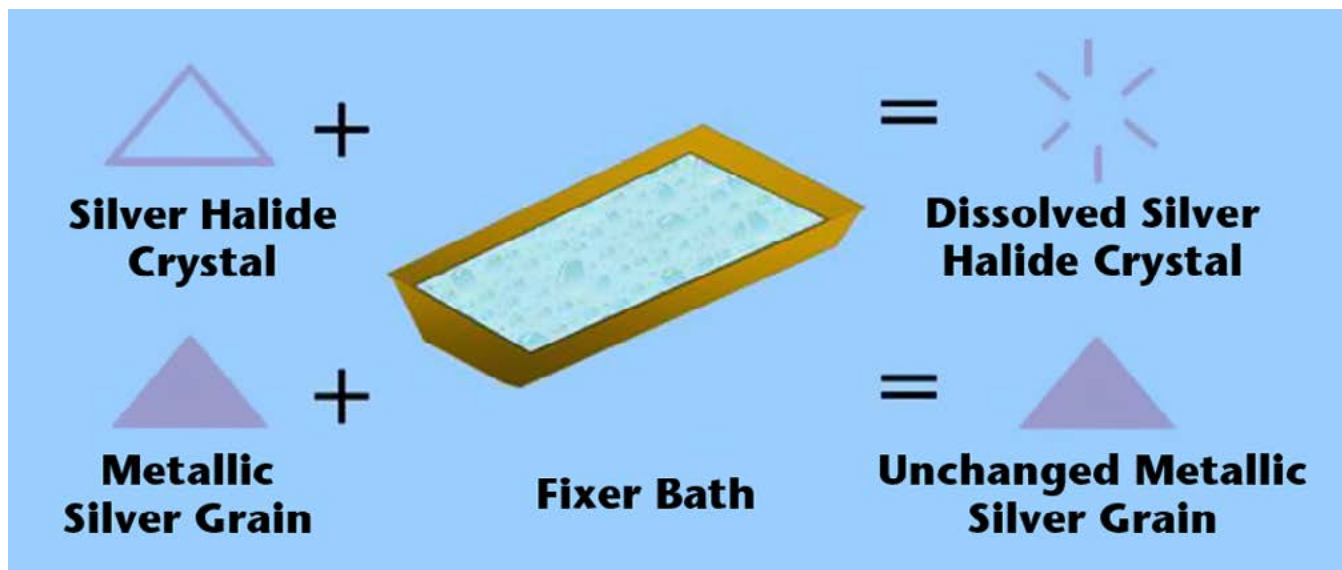


Figure 6: Illustration of the fixing step.

After development and fixing, the film must be thoroughly washed to remove all processing residues. If they are allowed to remain, the image will fade and the background will turn brown after extended storage.

Film drying would appear to be an uncomplicated process, but it is really quite complex. During drying, the water is evaporated away. As this occurs, the gelatin layers, which swelled when they were first immersed in the developer, will compress to perhaps one-tenth their size when wet. The polyester base will also give up much of the small amount of water it absorbed during the processing steps, resulting in some changes in overall dimensions.

Acknowledgment

Information provided by my friend and former colleague Robert Seyfert is gratefully acknowledged. **PCB**



Karl Dietz is president of Karl Dietz Consulting, LLC, offering consulting services and tutorials in the field of circuit board & substrate fabrication technology. To view past columns or to reach Dietz, [click here](#).

Dietz may also be reached by phone at (001) 919-870-6230.

3D Printing: The New Frontier?

ESA and the European Commission have embarked on a project to perfect the printing of space-quality metal components. The AMAZE project, Additive Manufacturing Aiming Toward Zero Waste & Efficient Production of High-Tech Metal Products, involves 28 industrial partners across Europe.

AMAZE aims to put the first 3D metal printer on the International Space Station allowing astronauts to

produce tools and new structures on demand.

The project envisages printing entire satellites and using the technology for missions to the moon and Mars. With no need of launching heavy payloads, manufacturing in space could save huge amounts of time and money.

To get to that future, ESA is looking at five metal additive manufacturing processes. New materials are also a possibility. Strong, lightweight components can be built by combining elements such as tungsten, niobium, or platinum with no waste.

Mil/Aero007 News Highlights



DfR Solutions Alliance Intensifies Government/Military Focus

"We are excited about the relationship with Circuit Solutions. Historically, DfR Solutions has successfully supported many government and military electronics reliability programs through SeaPort-e, NASA Safety and Mission Assurance Services, OSD Corrosion Prevention and other programs," said Craig Hillman, CEO of DfR Solutions.

3D Printing Coming to Military Applications

As researchers at Picatinny Arsenal explore the potential of three-dimensional printing, they envision the possibility of embedding a radio antenna on the side of a soldier's helmet or printing sensors directly onto a weapon or even an article of clothing.

Total Market for Electric UAVs to Top \$1B by 2023

The total market value for electric unmanned aerial vehicles will reach over one billion dollars by 2023 according to findings in the new IDTechEx report, "Electric Unmanned Aerial Vehicles (UAV) 2013-2023."

Global Electronic Warfare Market to Reach \$12.15B in 2014

The global electronic warfare market is estimated to be \$12.15 billion in 2014 and is expected to register a CAGR of 4.50% to reach \$15.59 billion by 2020.

Report Outlines Declines in Defense Spending

The decline of defense spending will likely force new revenue streams for the aerospace and defense industry that may include innovations in intelligence, precision strike technologies, and cyber security. "It is anticipated that global revenues for the defense sector will track to similar levels as in the past two years, particularly in the U.S. and Europe," said Tom Captain, DTTL Global Aerospace and Defense Sector leader.

Global Dimensional Metrology Market in Aerospace Industry

New analysis from Frost & Sullivan, Assessment of the Global Dimensional Metrology Market in the Aerospace Industry, finds that the market earned revenue of \$482.9 million in 2012 and estimates this to reach \$592.1 million in 2017. The research covers CMM, measurement gages, vision measuring machines, as well as optical digitizers and scanners.

Thermal Imaging Market to See CAGR of 10.9% 2013-2018

The thermal imaging market is estimated to grow from \$3.49 billion in 2013 to \$5.84 billion in 2018. This represents a compound annual growth rate (CAGR) of 10.9% from 2013 to 2018.

Port Security Market to Hit \$36.99 Billion by 2018

The global port security market is being driven by the increasing need for sustaining business continuity, threats on ports, and government initiatives. Security of the ports is extremely important to attract both domestic and international investors.

APAC Maritime Issues Impact U.S. Military Needs

The recent U.S. strategic pivot toward the Pacific has placed that region at the forefront of change in the military. Where in the recent past activities in the area of responsibility for the U.S. Central Command defined military needs, now the requirements for the U.S. Pacific Command are emerging as the leading edge of the defense technology sword.

U.S. ISR Video Analytics Budget to Decline

According to new research from Frost & Sullivan's U.S. ISR Video Analytics, the defense budget for this market will reduce to \$837.5 million in 2018 from \$1,207.2 million in 2012, as the combat operations in Afghanistan cease.

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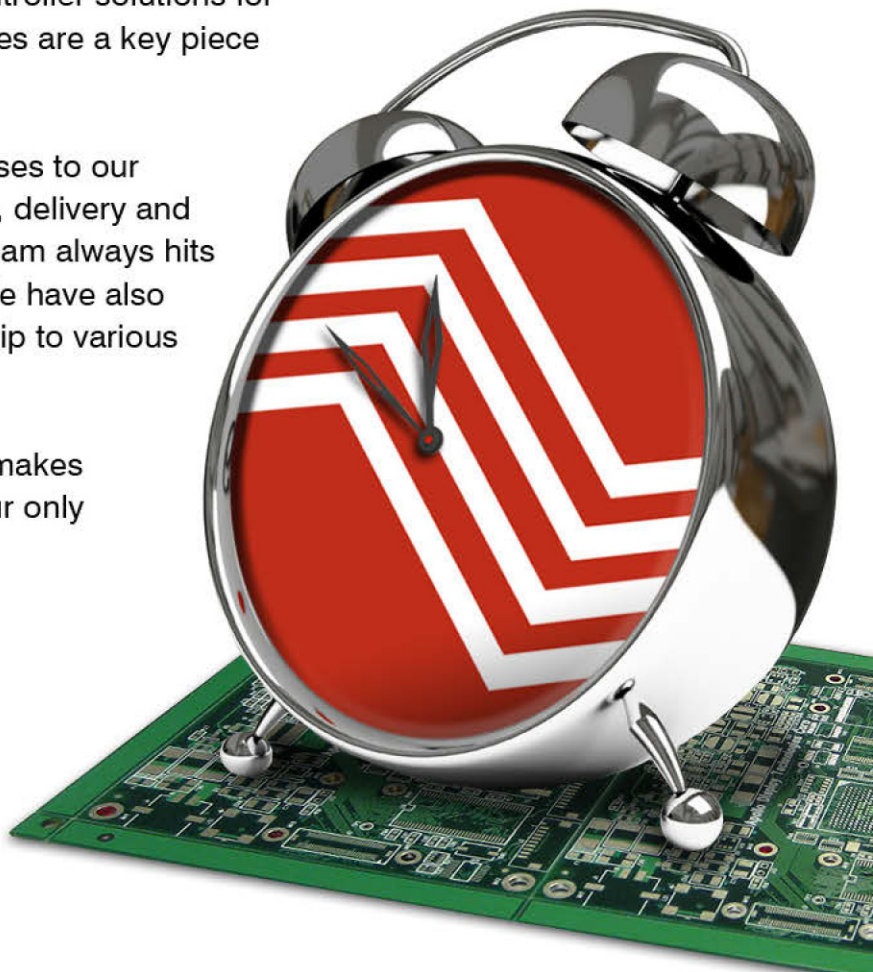
We have appreciated the timely responses to our requests for quotes for various quantity, delivery and board finish scenarios. The Prototron team always hits the delivery date with quality boards! We have also appreciated your willingness to drop ship to various Technology Kitchen partners.


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Are Boringly Predictable Operations Possible?

by Gray McQuarrie
GRAYROCK & ASSOCIATES

Self-help gurus like Tony Robbins claim that the more uncertainty and unpredictability we can tolerate in our lives, the greater our quality of life. But we don't want uncertainty and unpredictability in our operations. [Click here](#) to see why not.

Without question, we have excelled at developing new technologies, new materials, and new processes, and we continue to do so. This is exciting, creative stuff where we thrive and appreciate the statement, "variety is the spice of life." But, what we have grown to accept in our operations are the unpleasant surprises and problems that too many of us describe as "burning platforms." Is there anything we can do with our operations to make them significantly more predictable? Or is our only strategy throwing darts at the wall?

A big part of making our operations more predictable is by being able to model and simu-

late our PCB plants. The ability to simulate our operations, like an airline pilot can in an aircraft simulator, would allow us to sharpen our skills, broaden our intuition, and develop and test new strategies, with the goal of achieving boringly predictable operations. As nice as this sounds, there are three reasons why modeling is often instantly rejected before a discussion can even start: 1) we don't understand it; 2) we believe our operations are far too complex to be modeled; 3) nobody seems to have built a useful one in our industry (or has shared one publicly).

In order to serve the industry well and prove our factories could be modeled to a high level of detail, this modeling system had to be developed from within the four walls of our industry. So I decided to do it myself. And with the help of Robin Clark of the QMT group (my modeling mentor and Yoda) it has been done: fait ac-





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compli! Having said that, I know that for you to trust a model I built (or anyone else built, for that matter), you would have to be able to understand it, watch it, and change it to any scenario you could dream up. And it had to be as easy as running a “what if” analysis with a spreadsheet. To help build your trust further that our factories can be modeled, here is a link to a YouTube video of the [PCB Customized Factory Model](#).

One of the more complex operations to model in our factories is lamination, and here’s why. Each job has a certain lot size. Because of the variety of materials and board designs, an increasing number of press cycles have to

be spawned. This, along with the fact that our presses have different numbers of openings and the panels we build have different thicknesses, means there are varying numbers of panels that can be in a book and thus there are varying numbers of panels that can be in a press load. Specifically, jobs have to be split up into panels, combined using very precise rules into books, and then these books combined very precisely into a press load where they all must have the same press recipe or cycle. This recombination of materials and rules establishes the varying distribution of product across all of the presses that is impossible to see and comprehend dynamically, using a spread sheet. After the lami-

Record #	ArrivalTime	PanelID	JobID	NumOfLams	ProductType	PressCycle	Send	BookID	PressLoadID
1	0.33	21	3	1	C	▼ C	▼	6	2
2	0.33	22	3	1	C	▼ C	▼	6	2
3	0.33	23	3	1	C	▼ C	▼	6	2
4	0.33	24	3	1	C	▼ C	▼	6	2
5	0.33	25	3	1	C	▼ C	▼	7	2
6	0.33	26	3	1	C	▼ C	▼	7	2
7	0.33	27	3	1	C	▼ C	▼	7	2
8	0.33	28	3	1	C	▼ C	▼	7	2
9	0.33	29	3	1	C	▼ C	▼	0	0
10	0.33	30	3	1	C	▼ C	▼	0	0
11	0.33	31	5	1	D	▼ C	▼	8	2
12	0.33	32	5	1	D	▼ C	▼	8	2
13	0.33	33	5	1	D	▼ C	▼	8	2
14	0.33	34	5	1	D	▼ C	▼	8	2
15	0.33	35	5	1	D	▼ C	▼	8	2
16	0.33	36	5	1	D	▼ C	▼	8	2
17	0.33	37	5	1	D	▼ C	▼	9	2
18	0.33	38	5	1	D	▼ C	▼	9	2
19	0.33	39	6	1	D	▼ C	▼	9	2
20	0.33	40	6	1	D	▼ C	▼	9	2
21	0.33	41	6	1	D	▼ C	▼	9	2
22	0.33	42	6	1	D	▼ C	▼	9	2
23	0.33	43	6	1	D	▼ C	▼	0	0
24	0.33	44	6	1	D	▼ C	▼	0	0
25	0.33	45	6	1	D	▼ C	▼	0	0
26	0.33	46	6	1	D	▼ C	▼	0	0
27	0.33	47	7	1	D	▼ C	▼	0	0
28	0.33	48	7	1	D	▼ C	▼	0	0
29	0.33	49	7	1	D	▼ C	▼	0	0
30	0.33	50	7	1	D	▼ C	▼	0	0
31	0.33	51	7	1	D	▼ C	▼	0	0
32	0.33	52	7	1	D	▼ C	▼	0	0
33	0.33	53	7	1	D	▼ C	▼	0	0
34	0.33	54	7	1	D	▼ C	▼	0	0

Table 1: The composition of product sitting at layout at a specific moment in time.

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nation pressing has been completed, the books have to be deconstructed into panels, where they sometimes have to wait for other panels to catch up in order for them to be combined back again into their specified job lots. It is this reality, present in almost every department and operation in our shop, which overloads our EPS software's ability to predict and forecast; even though our EPS software vendor might claim

modeling is occurring behind the scenes, it often proves not to be useful and understandable. Hence, in order to figure out and plan our work, we are left to our own devices and our own singular survival instinct to try to create certainty in our lives, if only for a few hours after a stressful manufacturing planning meeting.

In the PCB Customized Factory Model, I exploited the use of a relational database struc-

Record #	Press	NumOfOpenings	InLamQueue	SentTo	InPress	FinishTime
1	A	5	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	1.33
2	B	4	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	0.00
3	C	4	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	0.00
4	D	3	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	0.00

Table 2: The status of all of the lamination presses at a specific moment in time.

Record #	TimeIn	TimeOut	NumOf Lams	ProductType	Press	PressCycle	NumPanels	PressLoadID
1	0.33	1.33	1	C	A	C	20	1
2	0.50	1.50	1	C	B	C	8	2
3			1	D	B	C	12	2
4	0.67	1.67	1	C	C	C	12	3
5			1	D	C	C	6	3
6	2.17	3.17	1	D	D	C	6	4
7			2	C	D	C	8	4
8	2.50	3.50	2	C	A	C	20	5
9	2.67	3.67	2	D	B	C	12	6
10			2	C	B	C	8	6
11	8.00	9.00	2	D	C	C	12	7
12			2	C	C	C	4	7

Table 3: The lamination log record for an entire run of 64 panels.

Record #	TimeIn	TimeOut	NumOf Lams	ProductType	Press	PressCycle	NumPanels	PressLoadID
1	0.33	1.33	1	C	A	C	20	1
2	0.50	2.50	1	D	B	D	24	2
3	0.67	1.67	1	C	C	C	16	3
4	2.18	2.85	2	C	D	B	12	4
5	3.37	4.37	1	C	A	C	4	5
6			2	D	A	C	24	5
7	3.53	4.20	2	C	C	B	16	6
8	9.20	9.87	2	C	B	B	12	7

Table 4: The lamination log record for an entire run of 64 panels using different press recipes than in Table 3.

ture with dynamic tables (tables that grow and shrink based on conditions as a model run proceeds). This allows for an accounting of a high level of detail, an ability to make changes easily and quickly, and transparency to see and validate what is going on as it is happening. For example, as jobs come into layup, they get broken down into individual panels and become part of a bin of material or what I call the layup queue.

Table 1 shows the panels selected for the second press load in the layup queue. This table shows there are a total of 34 panels in the layup queue consisting of a certain number of product C and product D panels. According to the "NumOfLams" column, all product in the layup queue at this point in time are at their first pressing. The last column on the right shows the press load ID column. The next column to the left shows the Book ID number.

Now earlier in the run, the first press load went to press 1. Table 2 shows the lamination press load status with the first press load in Press A, which is a five opening press (as seen in the "NumofOpenings" column). Since product C, for its first lamination pressing, has 4 panels per book, there should be 5 books or 20 panels for this first press load. Table 3 shows the lamination log for doing 24 panels of product D and 40 panels of product C where each product requires two pressings. At 0.33 hours the first press load entered and at 1.33 hours the first press load left. Table 3 also confirms that 20 panels were used in the first press load.

Table 3 shows the results coming out of lamination after the entire run of 64 panels had been completed. Tables 1 and 2 show the state of the lamination queue and the state of the presses where the simulation was stopped at a specific time. These tables are a specific snapshot in time, thus why they are called "dynamic database tables." In Table 1, the check marks in the "Send" column show books 6 through 9 making up press load 2. This press load consists of two, four-panel books of product C and two, six-panel books for product D. When the panels that are checked are sent to a lamination press, these records are instantly deleted from this table. The accounting of what occurred

is recorded and confirmed in the lamination log in Table 3. The information in Table 2 also changes dynamically and can be watched just like a movie or game film that a coach might study, going backwards and forwards, slow and fast, stopping and starting. One more thing to observe in Table 1 and Table 3 are mixed lot and mixed jobs in the press loads just as would occur in your own shop.

What happens if you make an oddball combination of press cycles? Table 4 shows the lamination log results where product C used press cycle C for the first lamination and press cycle B for the second lamination and product D used press cycle D for the first lamination and press cycle C for the second lamination. So books for the second press lamination of product D can be combined with books for the first press lamination of product C to make press loads. This is an ugly situation to try to map on paper considering each press cycle has a different time, so different presses will become free in a seemingly unpredictable sequence. All of this unpredictability, that has nothing to do with random variation or noise, can be predicted within the model and alternative scenarios can be studied as many times as you wish.

What impact will more products and press cycles, more or fewer press openings, more or fewer presses, different process and routing sequences, and all sorts of other possibilities, have on your entire plant? That will be the subject of a future article on modeling and simulation. For now, you may begin to believe that it is possible to model your plant to a high level of detail so that your operations can become more predictable. And who knows; you might find a pleasant, unpredicted surprise that adds plenty to the quality of your life and the quality of your business. **PCB**



Gray McQuarrie is president of Grayrock & Associates, a team of experts dedicated to building collaborative team environments that make companies maximally effective. To read past columns, or to contact McQuarrie, [click here](#).

Conversations with...

Gardien's Todd Kolmodin

by **Dan Beaulieu**

DB MANAGEMENT INC.

A couple of weeks ago I had the chance to catch up with Todd Kolmodin, vice president of quality for Gardien Services USA. I was particularly interested in talking to Todd because his new monthly column will be starting next month in *The PCB Magazine*. I consider Todd one of our industry's leading experts when it comes to electrical test and other reliability issues, so he's always a wonderful resource when it comes to those subjects. And he's a pretty interesting guy to talk to.

Dan: *Todd, thanks for speaking with me. For those readers who don't know you, can you tell us something about your background?*

Todd: Hi, Dan. As always, nice to chat with you. In a nutshell, I'm currently the vice president quality North America for Gardien Services. I began in the PCB industry in March 1986 in a test facility in Oregon. I learned all that is ET back then from CAM, drill, fixture assembly to test machine operation. As the years passed

I moved into the quality aspect of Test and Quality Assurance. Specifications and customer requirements can be very confusing at times. Specification review, training, documentation and customer service are many of my daily functions. I've seen this industry grow and change like the seasons. It's really amazing how technology has grown. From the PTH standard holes in the '80s to hybrid microBGA technology of the 2000s, it's really exciting.

Dan: *Can you tell us a little bit about what Gardien offers?*

Todd: Dan, Gardien has really taken a 20,000-foot approach to the PCB industry. Today, a company needs to look at the overall facets of the industry and tailor a specific genre to the requirements of the given customer. That is where Gardien excels, working with the cus-





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tomers, taking the background research initiative and providing the utmost quality assurance to their needs.

Dan: Can you elaborate on your work with the boards shops, and how you provide them with customer test services?

Todd: Gardien provides quality assurance using one or more of our independent test facilities throughout North America and Asia. Our customers and partners can send their product to us to be tested and returned. We also provide onsite service, where we actually perform the test services within their facility using our equipment or theirs. We effectively integrate into their manufacturing process.

Dan: Tell me about your new column, "Testing Todd," which debuts in the March issue of The PCB Magazine.

Todd: Dan, I can tell you that our industry is starving for information. Specifications change all the time and manufacturers can panic when trying to maintain compliance to the specifications they need to build. Gardien supplies that. Whether it is IPC, ITAR or DLA, the Gardien Group strives to stay in front of the curve and provide our customers an absolute resolution. I strive to make sure we are compliant and I sit on committees regarding these specifications and requirements.

Dan: What are some of the specific topics you will be covering in your columns?

Todd: I want to be able to cover all things related to electrical test. Feedback from our readers will provide ideas for future articles and I will continue to provide information around technologies and methods regarding ET.

Dan: And who do you anticipate the reader to be?

Todd: I would expect any quality manager or OEM to be reading. We take the time to review these requirements, debate them and also take our rebuttals to the IPC workshops.

Dan: How about test department managers and even people working in test? I would think this would be something they would be interested in as well?

Todd: Absolutely. Understanding customer requirements, challenges with electrical test reading and understanding terminologies on the fab drawings are all subjects these people need to know.

Dan: Todd, how do you see things in our industry right now, both in North America and globally?

Todd: I think North America is in a rebound now after falling off a bit in the last few years. I'm seeing new growth in military and communications. I think some of it is a concern to keep it in the U.S., and this is a good thing for our economy.

Dan: I look at your business as a service of the future. Do you agree with that?

Todd: Yes. As I see it, the requirements and specifications for new products are difficult to understand. I see companies like Gardien supplying this expertise to our OEMs and offloading the worry. We are experts and we spend a lot of time working with IPC, DLA and the DoD to make sure, regardless, that the OEM prints are within specifications to their build requirements.

Dan: *Where do you see Gardien in five years?*

Todd: Really Dan, in five years or 10 years I see Gardien as the absolute answer to quality assurance for the PCB industry. I know all the OEMs are throwing equipment to test the product, but Gardien goes way beyond that. Can we supply equipment solutions, yes. However, with this industry you have to go way beyond that: supply the test, and back it up with experts that know what the OEM world wants, challenge OEM requirements that don't meet specification and ultimately close the loop from the OEM to the manufacturer.

Dan: *Todd, when did we actually start electrically testing boards and why? Did people just take their chances before we tested boards?*

Todd: I cannot speak to the genesis of electrical test, as I joined the industry in 1986, even though I'm really not that old! I know there was manual testing done before that. In that era we were dealing with standard PTH technology and using digitizing tables to plot drill programs to do self-learning of the materials we drilled. Back then it was all self-learn and comparison testing. We would roadmap a piece of film and using a digitizing table to map out the drill program necessary. Then we would drill the plate and just place pins in a 1" fixture and let the test machine learn the electronics. This was a long time ago. I pioneered some of the netlist testing back in the 80s with some colleges from Tektronix.

Dan: *What method was first used? Was it point-to-point or did we use bed of nails test or what?*

Todd: As I stated, it was all self-learning back in the day. As a test house, we never had the Gerber data or any means to create the strong programs used today. As testing evolved it became necessary for test houses to gain strength in this arena and bring stronger quality assurance solutions to the market. The problem back in that era was that the technology did not exist.

Dan: *I know that early on, test heads were very expensive, and then Mania came up with the system where you could drill your own head templates and use four-inch pins to make up test heads. If I remember right, the pins were reusable.*

Todd: That's right. The early days of test fixtures were either 1" or a catalogue of other topographies. Mania brought their Cube that did use the longer spring-loaded probes. In this era the solutions were just being developed for testing of the PCBs. There were a lot of manufacturers of test equipment that were getting into the arena. However, netlist testing still had not been born. These technologies in this time were still using self-learn logics.

Dan: *Please take me through the next stages of equipment development.*

Todd: For me it came down to the fact we need to evolve. In the late '80s, the company I worked with was working with Tektronix, and a brilliant software engineer by the name of Alan Kent took it upon himself to work with us and design programs that would load in to the now-ancient Trace 948 Grid Test Machine. We worked a lot of hours troubleshooting the process but in the end we had a working netlist program that would have the intelligence of the board loaded in the machine prior to the board being tested. Although I know the industry was also perfecting and developing this technology





I think that where I was at the time was crucial in the development of what we call netlist testing today.

Dan: *When did the test service bureaus come into being?*

Todd: That's an interesting question. The fact of the matter is that we have always been here, at least as far as I have been in the industry. Really, in that timeframe, the service bureaus were the solution for the manufacturers. The manufacturers really didn't have the capital or the expertise to handle testing of their product. So back in that era the service bureaus really had the advantage.

Dan: *What was the first one?*

Todd: You might have me there. That's a hard one for me. In the '80s there were quite a few bureaus competing. I really don't know who the first was. We had a lot of new equipment hitting the market back in that era. Trace, Everett Charles, TTI, Mania/Testerion. They were all players in that time frame.

Dan: *What do we have today? Tell us a little bit about what is available in testing today.*

technology being produced there. For the U.S. and North America we still have a bit of a bell curve to get over to be able to test these new designs. We need to be sure we are diligent and moving forward with our Asia colleagues to break this barrier.

Dan: *Thanks, Todd. It's been a pleasure talking to you.*

Todd: Thank you, Dan. Let me know what you think of my column next month!

Do you have any questions about electrical test? Is there anything that you always wanted to know but were afraid to ask? E-mail Kolmodin at todd.kolmodin@gardien.com. **PCB**



Dan Beaulieu is a PCB industry veteran, and sales and marketing expert and writer who has contributed to numerous industry publications, on topics ranging from sales and marketing, to board shop performance. Beaulieu has more than 30 years of experience in the PCB industry. To read past columns, or to contact Beaulieu, [click here](#).

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There are few in our industry that have his experience and expertise in just about every aspect of the business. Dan knows what works, and perhaps more importantly, what doesn't.

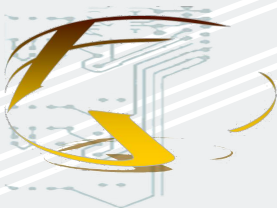
When additional expertise is needed, or when senior management just needs an independent opinion, companies large and small alike get the guidance of Fein-Line Associates, especially in the areas of New Product Market Entry and M&A Due Diligence.

In our business, there's a lot on the line, not just sometimes, but every time. The line between success and the alternative can be razor thin. That's why winning companies choose Fein-Line time after time.



Dan (Baer) Feinberg
Fein-Line Associates

**Sales Training General Marketing Assistance · New Product Market Entry
Merger and Acquisition Due Diligence · Printed Circuit Technology assessment
Market Research (It may work but will it sell) · Expert Witness assignments
Technology Transfer**



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TOP TEN

PCB007
News

PCB007 News Highlights This Month

① **IPC: PCB Sales Improving Despite Weaker Orders**

"While sales continued to strengthen in the North American PCB industry compared to last year, orders declined," said Sharon Starr, IPC's director of market research. "This disparity between sales and order growth pushed the book-to-bill ratio to its lowest point since March 2009," she added, "indicating a slow and possibly bumpy recovery going into 2014."

② **Spirit Circuits Acquires Lyncolec**

After six months of negotiation, innovative PCB manufacturer Spirit Circuits is pleased to announce the acquisition of Poole, UK-based PCB manufacturer Lyncolec. The company is well-known for supplying rigid, flex, and hybrid multilayer PCBs.

③ **IPC Redefines Microvias, Again**

In 2013, IPC changed its definition of a microvia. Before then, a microvia was defined as any printed board with holes that have a diameter of equal to or less than 0.15 mm [0.006 in]. Over time, that size became common, while more challenging geometries emerged to alter the definition of microvia structures.

④ **IPC's 2013: A Year in Review**

Within the printed board fabrication arena, IPC released updates to two of its most popular flexible circuit standards: IPC-6013C, Qualification and Performance Specification for Flexible Printed Boards, and IPC-4203A, Cover Bonding Material for Flexible Printed Circuitry.

5 PCB Solutions Doubled PCB Engineering Projects in 2013

PCB Solutions is pleased to announce yet another year of excellent growth in one of its core services: Engineering design and PCB layout. The company developed engineering services most of the 2013 year and made great strides in growing its engineering division.

6 Innovative Circuits Doubles Capacity with Drill Acquisitions

"These new drills allow us to use all of our drills more efficiently," says Russell Nolan, manager of drill and route operations. "This acquisition speeds up our operations tremendously and increases our ability to meet our customers' quick-turn demands."

7 Murrietta Circuits Achieves ISO-13485 Certification

Albert Murrietta, COO and co-owner, announces that his company has achieved full ISO-13485 registration for the medical marketplace. Murrietta is now one of the few companies in the nation that can offer a true full turnkey solution, from design through final assembly, with complete medical ISO registration.

8 MFLEX Doubles Sales to New Customers

Reza Meshgin, CEO, commented, "Net sales to our newer customers more than doubled sequentially, and are expected to represent approximately 23% of total net sales. Looking ahead to the fiscal second quarter, we expect a significant sequential decline in net sales that we anticipate could approach 40%."

9 AT&S Named ZTE's Best Quality Performance Supplier

On December 12, 2013 ZTE held an awards ceremony for Excellent Suppliers. In addition to winning the "Excellent Delivery" Award in 2012, AT&S was awarded the "ZTE Annual Best Quality Performance Award 2013" as core supplier.

10 Impact of Inexpensive Flex PCBs on Cell Phone Production

Using flex circuits as the interconnect choice in the assembly of cell phones will bring huge benefits. These boards have low mass and cause cell phones to be much lighter. They are capable of housing small conductors with high wiring density, taking up less space. Being lighter and smaller will result in an end-product that is more versatile.

For the latest PCB news and information, visit: PCB007.com



EVENTS

For the IPC Calendar of Events, [click here](#).

For the SMTA Calendar of Events, [click here](#).

For the iNEMI Calendar of Events, [click here](#).

For a complete listing, check out [PCB007's full events calendar](#).

[SPIE Electronic Imaging](#)

February 2–6, 2014

San Francisco, California, USA

[MD&M West Conference](#)

February 10–13, 2014

Anaheim, California, USA

[Pan Pacific Microelectronics Symposium](#)

February 11–13, 2014

The Big Island, Hawaii, USA

[Dallas Expo & Tech Forum](#)

March 4, 2014

Plano, Texas, USA

[NORDIC HDI 2014](#)

March 5–6, 2014

Copenhagen, Denmark

[Houston Expo & Tech Forum](#)

March 6, 2014

Stafford, Texas, USA

[SMTA Webtorial: Tin Whiskers—All You Should Know](#)

March 11, 2014

[IPC APEX EXPO—Conference & Exhibition](#)

March 25–27, 2014

Las Vegas, Nevada, USA

[Electronics New England](#)

March 26–27, 2014

Boston, Massachusetts, USA



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PCB007 Presents

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Coming Soon to *The PCB Magazine:*

Don't miss these upcoming issues!

• **March:** Materials
(plus: special IPC APEX EXPO pre-show section)

• **April:** HDI

• **May:** Plating and Etching

Interested in being a contributor to *The PCB Magazine*?
Drop us a [note here!](#)

See you next month!