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July 2013

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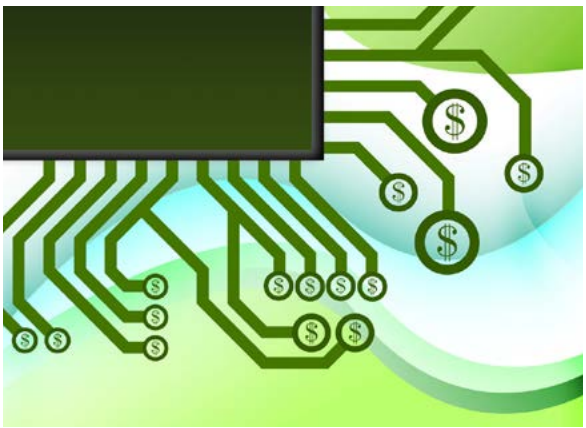

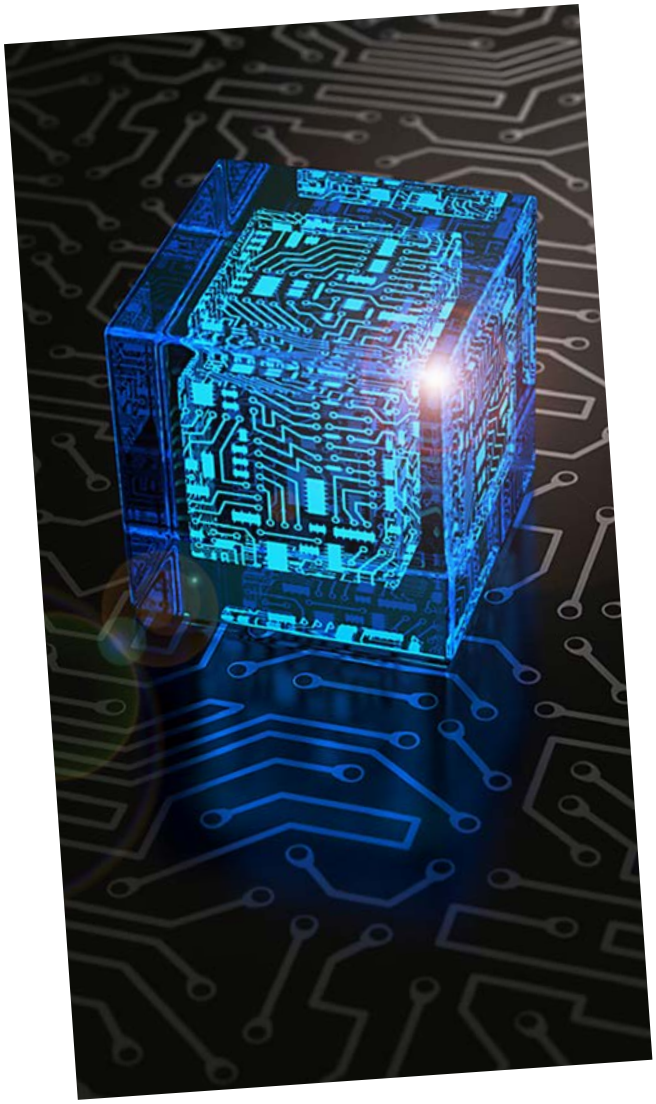

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NEW INTERCONNECTS

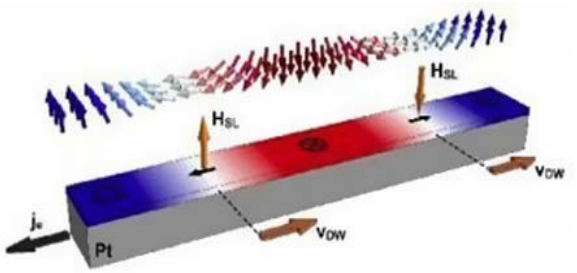
CONTENTS

COLUMNS

EXTRAS

VIDEO INTERVIEWS

SHORT



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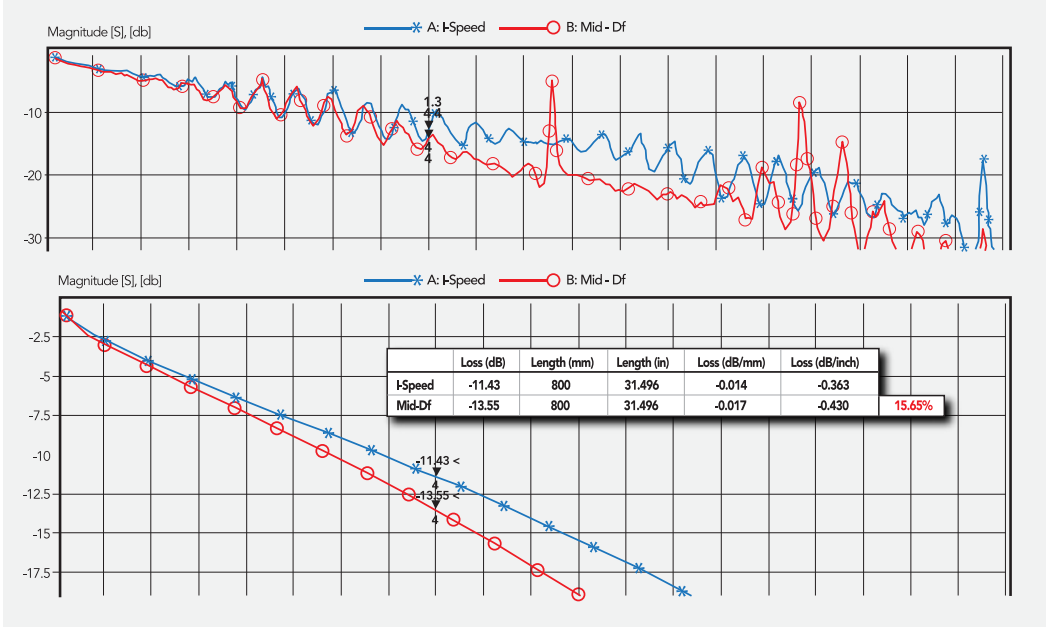

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THE WAY I SEE IT

Here We Go!

by Ray Rasmussen
I-CONNECT007

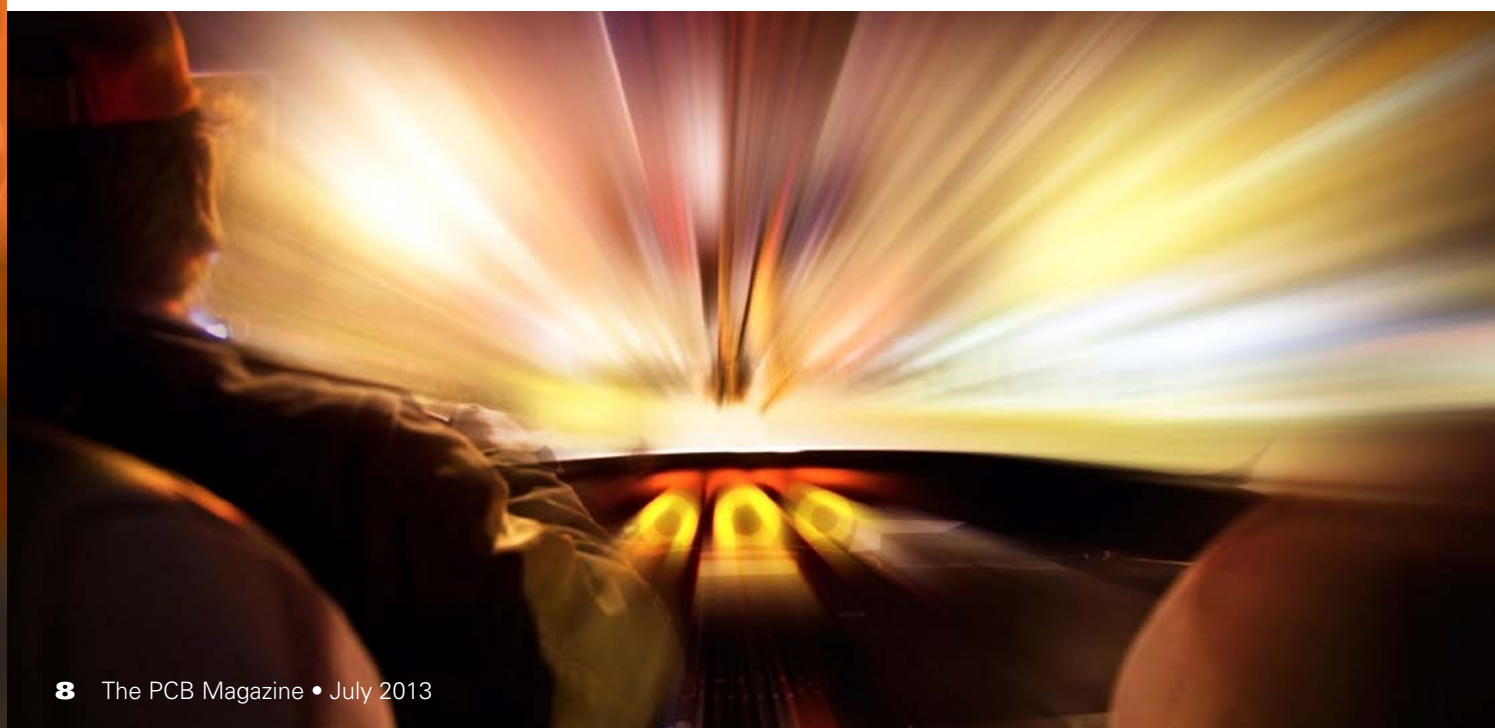
I recently talked with a friend of mine who works at Intel. He manages big OEMs that buy ICs in huge quantities for their PCs and other consumer products. We had a short conversation about the market in general, and he said that his customers were starting to put a lot of pressure on him to provide them with the information they need for their next acquisitions.

These OEMs are becoming really impatient; they seem to be under a lot of pressure themselves. My friend said something along the lines of, "I don't know what people are talking about when they mention a slow economy. We're not seeing it." In his world, which slices through consumer electronics, they're all busy. Demand is up.

It sounds to me like the normal build-up to the Christmas season is driving the demand. Maybe the big PC makers feel that if enough folks have figured out how to use Windows 8, more consumers and businesses will take the plunge and upgrade their PCs. We know Apple will likely introduce a new phone this fall (it's already being built, I suppose), which will generate a lot of activity.

IPC sent over a press release in mid-June titled: *Slow Growth Ahead for Economy and Electronics Industry, According to IPC*. I retitled it, IPC: Economic Growth Ahead. Now, I'm not trying to discount the experts at IPC, but I do believe the market out there could be better than we might think. IPC did talk about the second half being potentially better. Here's a paragraph from that news item.

Economic activity in the U.S. manufacturing sector expanded in March for the fourth consecutive month, and the overall economy grew for the 46th consecutive month. IPC's North American Electronics Industry Performance Index reflects an outlook for slow growth in the months ahead. Another leading indicator for electronics supply chain sales growth in North America is the PCB book-to-bill ratio, which reached a 34-month high in April at 1.10, indicating that sales across the supply chain may resume positive growth momentum in the latter half of 2013.



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-Arthur C. Clarke

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THE BETTER WAY

IPC seems to be taking a very cautious approach, not wanting to appear too optimistic. It just doesn't feel dreary and dismal out there to me, but rather bright and cheery. At least, that's how I see it.

I sent another item to a friend who works in the construction industry: Homebuilder Confidence in U.S. Rises to a Seven-Year High. That's always a good sign and bodes well for the overall economy.

Now, check out this PBS interview with Charles Morris, the man who predicted the crash of 2008. The article, Comeback: Why the U.S. Sits at the Brink of a New Boom, talks about an unprecedented recovery and boom, the likes of which the U.S. hasn't seen in decades. In the article, Morris makes this prediction: "It's the best-kept secret in the economics media: The United States is on the brink of a period of solid, long-term growth rivaling that of the 1950s and 1960s. It is not a finance-driven, self-destructive boom, like the 2000's housing bubble. No, the new economy will be durably grounded in energy and heavy manufacturing, even though it will take several years to come to full fruition."

"Morris makes this prediction: "It's the best-kept secret in the economics media: The United States is on the brink of a period of solid, long-term growth rivaling that of the 1950s and 1960s."

Things feel good right now and if Morris is right, we're in for a good ride. Not that I'm an expert, but in a 2009 column, I did say that the fundamentals would become strong and allow for a longer, stronger recovery. It just made sense to me that if you fixed the fundamentals, the rest would take care of itself. Keep in mind that the U.S. is still the largest, strongest economy in the world. When it rights itself, things will really start to move. I'm sure of it.

Irrational Exuberance

Not all is rosy out there, however. The global economy faces a variety of challenges from China.

Having experienced several boom and bust cycles over the years—in the U.S., in Japan in the '90s and with the recent European defaults—I've learned that when things get out of balance, the markets tend to seek equilibrium. The more out of balance things are, the more correction is needed. Another article from Fitch Ratings claims that China is on the verge of some dramatic "rebalancing." Published in the Telegraph, the article, Fitch says China credit bubble unprecedented in modern world history, is a bit scary. Charlene Chu, Fitch Ratings' senior director in Beijing, said, "There is no way they can grow out of their asset problems as they did in the past. We think this will be very different from the banking crisis in the late 1990s. With credit at 200pc of GDP, the numerator is growing twice as fast as the denominator. You can't grow out of that." Chu does believe the Chinese government, with its deep reserves, can handle a potential banking crisis. They've already been trying to manage a soft landing. If you're vested in China, read this article.

For the sake of our economies and businesses, let's hope that the Chinese are able to stay on top of this. The last thing we need is to derail this fragile recovery and take the wind out of the coming boom.

Call me an optimist, but it really is our turn for a bit of good economic news. I think we can all use a break from the struggles of the last decade and a chance to enjoy the good years ahead.

That's the way I see it. **PCB**

Ray Rasmussen is the publisher and chief editor for I-Connect007 publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuiTree Magazine*. Contact Rasmussen here.

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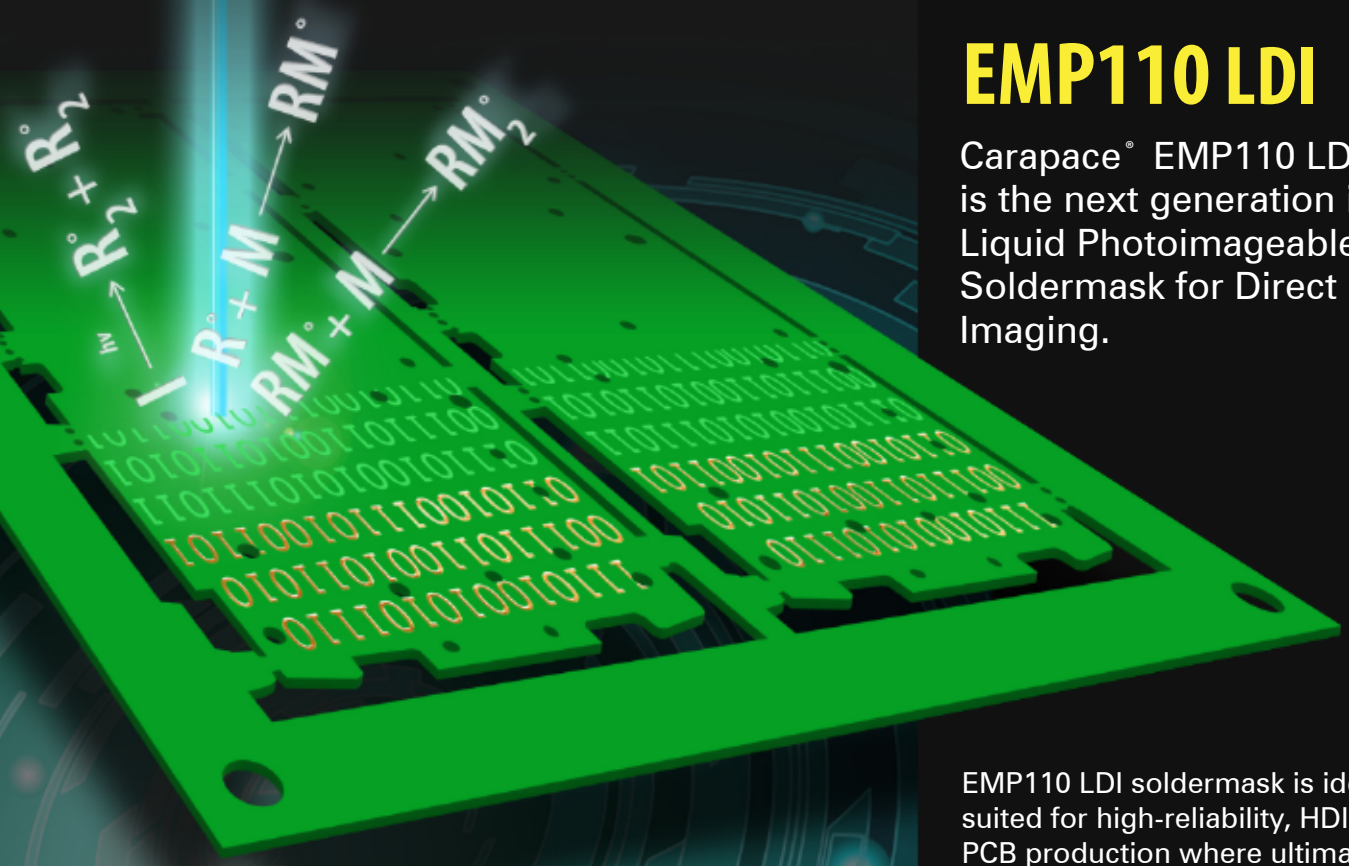

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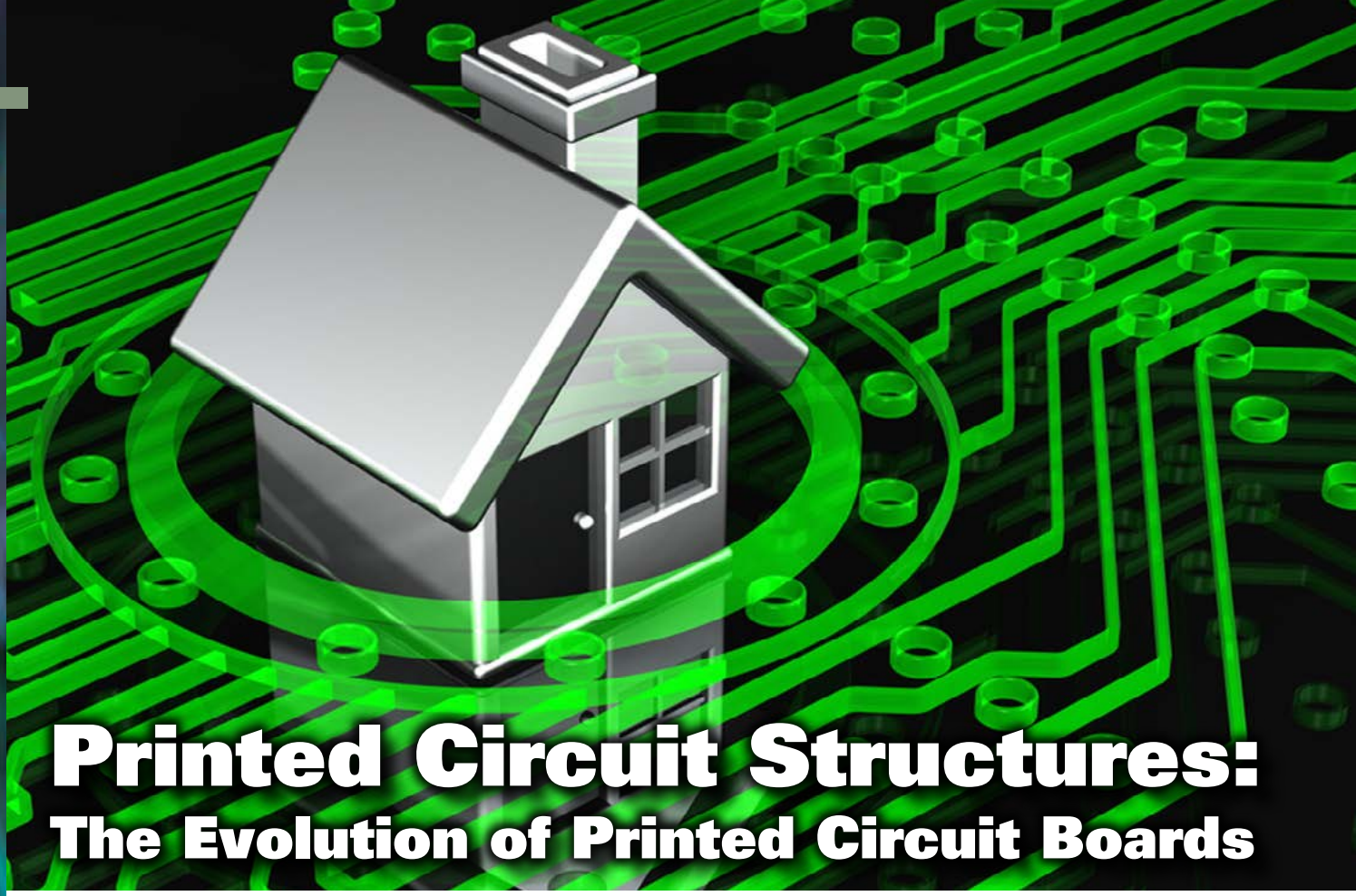

Printed Circuit Structures:
The Evolution of Printed Circuit Boards

by Kenneth H. Church, Harvey Tsang, Ricardo Rodriguez, Paul Defembaugh, Raymond Rumpf
nScrypt Inc., Orlando, Florida
and the University of Texas at El Paso

Abstract

The printed circuit board is the backbone of electronics and a large number of consumer devices. The challenge to put more function in a smaller space requires more components utilizing smaller bond pads, smaller lines and tighter pitch. The electronic packaging industry has aggressively pursued novel ways to shrink and stack multilayer boards inside smaller volumes. The industry is approaching serious obstacles in the continued size reduction requirements with the need for wires, epoxy, vias, solder and sometimes bolts and screws to mount the boards. The next logical step is to move beyond 2D stacking, which is 2.5D, to make 3D packages and to utilize the third dimension directly. Eliminate the traditional 2D FR-4 board and the wires, epoxies, vias and solder and make the next-generation packages utilizing 3D: the printed circuit structure (PCS).

The PCS concept will allow passives, actives and even antennas to move out of the XY plane and into the XZ and YZ planes. This new dimension will appear to be very complex and next-generation circuit optimization will be required, but the end result will net a significant improvement in volume utilization. In addition, if new materials are developed and utilized properly, the PCS will be the box or the package, thus eliminating all the bolts and screws necessary to mount a PCB in a traditional box or package, saving space and reducing weight.

In this paper, nScrypt and the University of Texas at El Paso will present 3D printing of printed circuit structures. A demonstration of true 3D electronic structures will be demonstrated and shown as well as novel approaches that utilize CAD to 3D printing, including the electronics portion.

Introduction

Printed circuit boards are a critical component in almost every electronic device. Electronics come in a variety of shapes and sizes, determined by function, environment and physical shape of the device. The electronics

portion of the device is limited to a standard 2.5D approach. This implies building a multilayer board with dimensions in X and Y and then mounting that board to a structure of specific shape and volume. But data transfer speeds are seeing their limitations in this conventional PCB approach. New materials are being used to overcome these limits, but the actual structure will need to see improvements too[1,2]. Wires, epoxy, vias, solder and connectors all contribute parasitic harmonic effects to standard PCBs due to impedance mismatching and/or sharp turns that create electromagnetic (EM) reflections[3,4]. Using 3D printing, there will no longer be a need for wires, epoxy, vias, solder or bolts and screws. The 3D printing process can move from building a circuit which is flexible enough to be rolled into a cylinder, to building a cylinder with a curved circuit within it. These structures will be solid or even porous depending on the applications of the PCS. 3D printing has been around since the 1980s and started as a novel demonstration, but is now becoming more ubiquitous. With the introduction of tabletop fused deposition manufacturing (FDM), machines and even home users have the opportunity begin exploring possible 3D prints. These printers allow users to convert their CAD into physical structures for prototyping or even small part replacements[5].

3D Printing

3D printing or additive manufacturing (AM) is an efficient and green form of manufacturing that fabricates products by building successive layers of material, thus creating little to no waste. Traditional subtractive techniques start with bulk materials and machine away unwanted excess. The first concept of AM known as selective laser sintering (SLS) places a thin layer of the powdered material onto a work surface and a laser beam patterns metal thin shapes by sintering the powder particles together. The work surface is lowered and a second layer of powder is spread on top of the existing metal shape. Through multiple lowering, powder spreading and sintering cycles, a 3D structure can be built with features and voids that subtractive processes cannot achieve; resolution of lines are around 0.005" and layer thickness of 0.004".

Stereolithography apparatus (SLA) is another 3D printing approach that is a similar SLS but instead of sintering powder, it hardens photosensitive resin (liquid). There are some builds that require support structure materials if there are large gaps in the 3D structure during the build. Support structure materials are temporary and typically dissolved with water. SLA, like SLS, is an expensive process given the time it takes to build a part (minutes to hours) and the photosensitive resin is very expensive. The features created are solid and the surface finishes can be smooth; feature sizes can be as small as 0.001" for commercial grade tools, but research tools have achieved 0.0001" features. Figure 1 shows commercial tools for 3D printing and direct printing.

Fused deposition manufacturing (FDM) is another 3D printing approach using a heated nozzle to extrude plastic directly onto a surface. This will print a pattern and then repeat the print, thus layering for 3D builds. Like SLA, FDM will sometimes require a support structure material during builds. The nozzle and head is moved mechanically on a motion platform and coordinated with the flow of melted plastic flow rate to the XY motion. A disadvantage of FDM is in the printing process which induces porous structures during the build. This is due to the shape of the extrusion and the fact the material is not self leveling as this would be counter to the 3D build concept. This process typically requires an 80-90% overlap of the lines to be placed into the building parameters creating

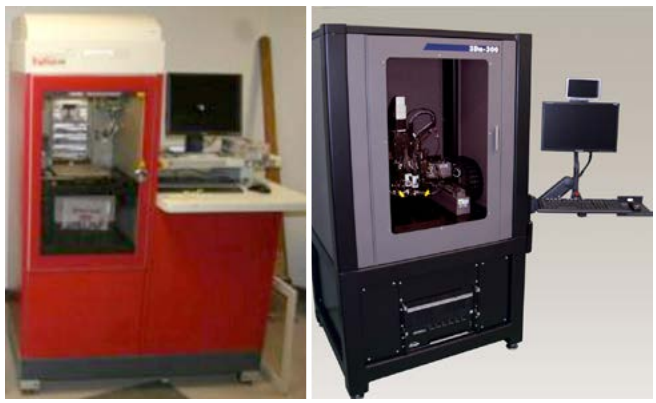

Figure 1: Commercially available SLA machine (l) and commercially available direct print machine (r).

a stable build but also small air pockets. The problem can be improved with high resolution prints and control of the overlapping parameters. This type of build imposes surface finishes that are rough and additional post-processing is sometimes needed to smooth the surfaces. This approach for 3D printing has larger features (0.005" at high resolution), but the parts produced are more rigid which allow for functional parts.

Printed Electronics

Printed electronics is a printing process that can pattern an electrical circuit onto various substrates, including cheap substrates such as vinyl. These processes were designed to be fast, low-cost and achieve small features. The screen printing process is well known for its use in solar cell manufacturing, low temperature co-fired ceramic (LTCC) and multi-chip modules, where a screen with a set pattern is laid on top of a substrate and a thick film ink is pressed through the screen. Screen printing can achieve throughputs of 50 m^2/h with a resolution of 100µm. This is standard for manufacturing in industry and has the ability to produce thick layers from a wide range of high viscosity materials.

> ***Just like the inkjet method, aerosol printing requires custom inks that can be aerosolized, but aerosol has the widest range of working distances and line widths.***

In addition to using screens, there are direct digital manufacturing (DDM) approaches such as inkjetting. Similar to household printers, inkjets use a low viscosity ink with solvent materials which are deposited via droplets onto a substrate, line by line. These inkjettable materials can exhibit a number of electrical attributes, including conductivity. For many applications, low temperature processing is required and many of these materials contain additives to enhance adhesion to the surface after low-temperature post-processing. Inkjetting can have a throughput of around 100 m^2/h with a thickness of around 0.0005".

Electroless plating is another common printing process used extensively in the production of PCBs. This process deposits a metallic film with the aid of a chemical reducing agent in solution. This allows plating of non-conducting substrates and is typically used to coat vias after drilling with copper. While electroless plating is typically slower than electrolytic plating, the resolution is better and finer, and thinner lines can be achieved. This is becoming more attractive as circuits are becoming smaller and require higher frequency performance, which require higher resolution.

Other forms of printed electronics include the direct print methods (DP), which some have coined direct write. These include nozzle, quill and aerosol[6]. (The nozzle method is covered in the 3D Printed Circuit Structures section later.)

The quill method deposits material much like a quill pen on paper. The quill tip is dipped into a container of material which adheres to the tip and then the tip is moved onto a substrate where the material is transferred from the tip and onto the substrate with 3-axis movement. This method is able to produce 14 nm line widths with 5 nm spatial resolution, but only able to build small length scales and requires flat surfaces and custom inks. Inkjet printing has been covered before and the advantages include high-speed printing due to parallelization of print heads, but these approaches typically require flat surfaces and custom inks that have low viscosities.

Just like the inkjet method, aerosol printing requires custom inks that can be aerosolized, but aerosol has the widest range of working distances and line widths. Aerosol requires the material to be atomized into a mist which is surrounded by a coaxial sheath of air flowing out of an orifice directed at the substrate; dimensions as small as 5µm have been done using this approach.

Since these are all forms of 3D printing, it is natural to combine some or all of these methods to create a complete electronic product with small feature sizes and fine conductive line

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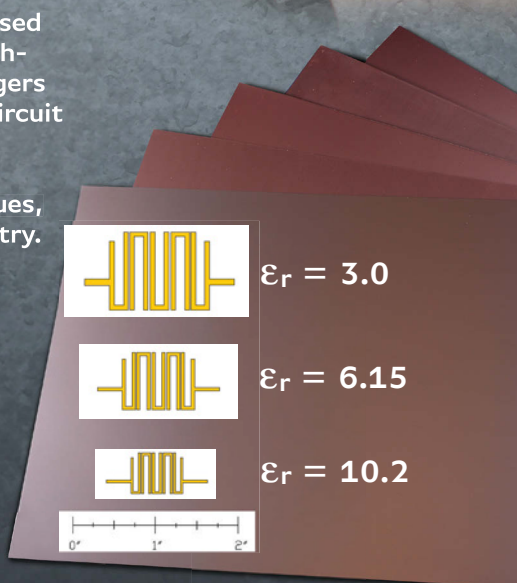

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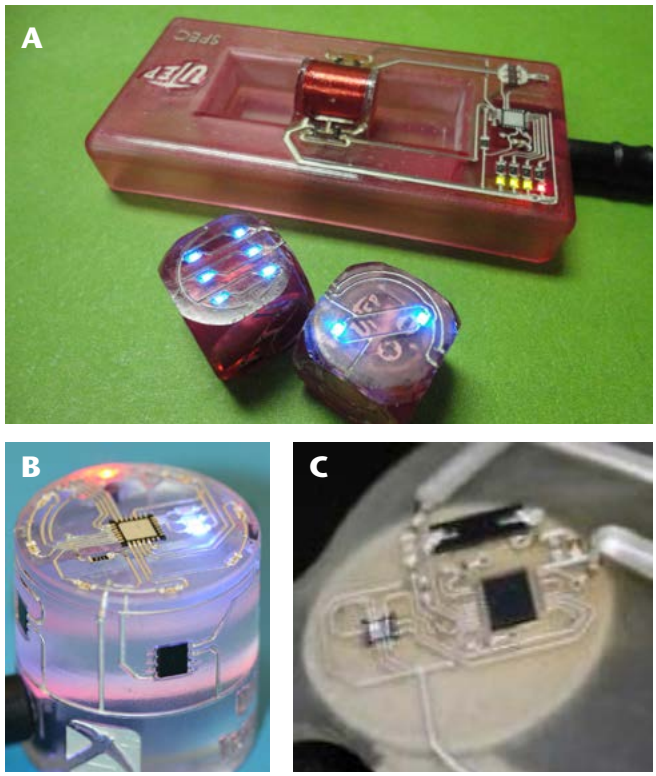
Printed Circuit Structures

The printed circuit structure (PCS) is a new area for 3D printing. While early demonstrations were done in the early 2000s, recent studies and demonstrations are being presented as a viable alternative to traditional circuit board manufacturing. Unlike conventional PCBs that build 2D layers consecutively on top of each other (otherwise known as 2.5D), a truly 3D PCS would utilize side walls, curves and reduce unused volumes that exist in current electronic devices. A graphic artist's rendition of a true PCS is shown in Figure 2.

The idea of utilizing the structure as the circuit carrier implies there will be no need for PCBs. This reaches beyond simple conformally printing circuits and changes the structure to an electrically functional structure; the electronics are the structure. In 2D, components can only be placed on a level plane while in 3D components and traces can be built up, around and within structures. Components can be smoothly integrated into a structure and even hidden within a solid structure which makes reverse engineering much more challenging. It will also enhance the ruggedness of the device as the device will become a monolithic piece with no glue, snaps, solder, wiring or bolts. This monolithic piece could also be water proof as the electrically workings could be buried within the structure leaving no entry point for liquid. The shapes of the structures will not restrict the printability of electronic components and traces, therefore enhanced performing devices may be possible to include higher gain antennas. Additionally, this will be most the most volumetrically optimized approach to electronic packaging, thus enabling many more functions per cubic volume. A few examples of PCS are shown in Figure 3.

But as these structures get smaller, the electromagnetic (EM) interference between traces and components become a larger problem. But with the introduction of anisotropic materials and spatially variant lattices, it would be possible to manipulate fields around and directed towards other components to achieve complex structures that perform in ways that 2D structures cannot[7,8]. Current research demonstrates that 3D structures can manipulate

Figure 2: A graphic rendition of future PCS.



Figures 3a-c: 3D printed dice and charger (a), 3D printed magnetometer (b) and 3D printed accelerometer (c).

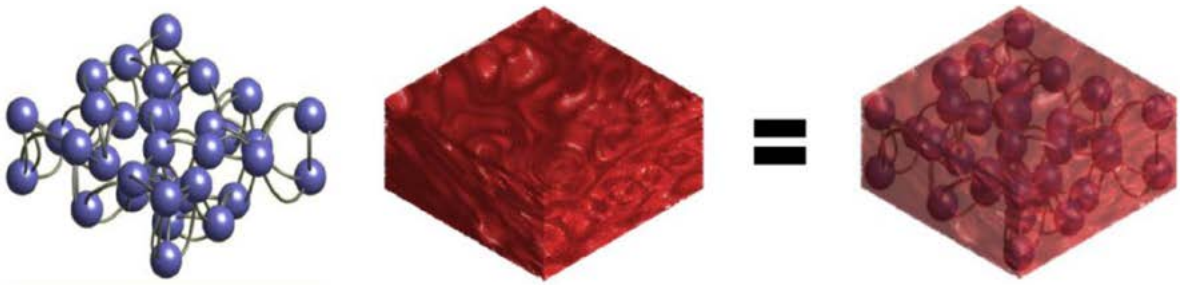


Figure 4: Metal components with dielectric field management equals complex functional structures.

fields using meta material designs in ways that standard 2.5D structures cannot. Figure 4 is an artist rendition of designing material properties in 3D, thus providing control over EM fields. This will be an enabling technology as more and more functions are packed into smaller volumes.

Unfortunately, PCS building methods are still premature and are labor-intensive since automation has not yet been achieved. Currently, 3D printing and DP are used in succession to achieve such results, but a tool which can combine these two methods with the same resolution as DP would require a new definition. A direct printing additive manufacturing system (DPAM) is being developed to obtain the build and curing of such structures within one automated tool.

Automation Within a Single Tool

The primary strength of the nScrypt 3Dn-600HPx DPAM system lies in its many integrated tools. Rather than performing only one function and requiring operators or conveyors to move parts from system to system, time is saved by being able to perform all functions in just one machine on one gantry. Future, larger 3D electronic printing systems may use conveyors connecting several dedicated machines; however, for low-volume experimental fabrication, the compact nature of a single, integrated system is easily seen. An additional advantage is that because the part never moves from start to finish, less alignment fiducially is required, thus easing the realization of high accuracy printing.

Here is a list of hardware that the DPAM tool is equipped with:

- Precise 3D Cartesian gantry allowing all tools to reach any point in a 600 mm x 600 mm area
- Four independent precision valve dispensing pumps
- 650 nm laser displacement sensor
- 12.4W/cm2 (3 mm beam diameter) 385 nm UV LED lamp
- 30-watt CW or pulsed (150 ns) 1080 nm laser
- Rotating vacuum pick-and-place nozzle and 7-bay tool changer
- 18" square milled-flat porous ceramic vacuum chuck
- Motorized dual camera Ethernet-based machine vision multi-tool automatic calibration system embedded below the printing deck
- Ethernet-based machine vision camera with automatic computer vision and recognition software
- Motorized process-view camera

Here are a few possible applications for these tools, arranged in a hypothetical order of operations. Each of the concepts has been successfully demonstrated.

1. Place either plastic sheet on vacuum chuck or remove vacuum chuck and place an arbitrary part in printing area as the printing substrate

2. Scan the object contours using the laser displacement sensor for conformal printing on the substrate. A 3D scan file is produced and used to accurately print on the arbitrarily-contoured part

3. The machine camera using image recognition software automatically identifies mark-

ers fiducially and adjusts and rotates the design files to match the actual substrate or to orient and accurately place components using the pick-and-place system

4. Using one of the four dispensing pumps, layer-by-layer print UV-curable dielectric/structural material such as the photopolymer used in SLA equipment

5. Between layers of photopolymer, use the 385 nm UV lamp to cure the dispensed material

6. Pick-and-place surface mount components into photopolymer structure

7. Another pump dispenses thick film, micro-silver flake conductive traces to form electrical interconnects. A second laser displacement sensor scan may be used in order to print non-flat interconnects

8. Thermally cure the thick-film ink using the high power 1080 nm laser

9. Continue process of printing structure, conductor, curing, and placing components until a finished 3D structural electronic part is formed

Process Integration, Synchronization, and Control Hardware

Each of the integrated tool technologies is centrally-controlled by the precise motion control platform. The motion control platform is connected via IEEE 1394 serial bus to the PC. The motion control platform uses multi-axis synchronous motion in order to print along arbitrary 3D paths as is needed in the case of following the contours measured by the laser displacement sensor. From the same control system are many digital, analog, and serial inputs and outputs connected to each of the subsystems such as the UV light, pick-and-place, etc. In this manner, complete integration of machine operations is easily achieved because the hardware operations of each device are directly controlled from the central motion control platform. Each device does, however, have some type of interface electronics so that the complexities of each device's control are masked from the central motion control platform. In the case of the laser, for instance, an RS-232 serial port and a set of digital IO lines are used to set the optical power and operation mode of the laser. Each of these signals is adapted by electronics within the laser control box to control the actual laser diode. In the case of the pick-and-place system, digital output modules convert 5V signals from the motion control platform to control pneumatic solenoids for pick-and-place vacuum, up/down actuation, and tool changer operation. Each of the tools is controlled in a similar manner.

> ***Using this method with the excellent hardware motion control system allows accuracies of better than 1 micron to be realized.***

From a software perspective, designs start as 2D layer drawings in the DXF file format such as slice files generated from 3D model files in STL format. Each of these layers is called a job and are arranged as an ordered list of separate tasks called a job tree, which the machine executes when the run button is clicked. Each job has particular attributes such as which tool is to be used (pump, UV light, laser, etc.) as well as more advanced settings such as 3D laser displacement sensor scan data in order to print conformal to the actual measured surface. Within each job, a text-based script file is provided which contains the motion commands as well as custom commands such as "light on/off" or "pick/place" which control each specialized tool. In order to achieve smooth, accurate, and perfectly synchronized operations, each of the jobs is precompiled into a single program code file which is first downloaded to the precise motion control hardware from the computer running a real-time kernel (RTX) via IEE 1394 serial bus before execution begins. Using this method with the excellent hardware motion control system allows accuracies of better than 1 micron to be realized.

Operation

From a user's perspective, the entire system is controlled from a Windows PC running proprietary software. Designers start with a 3D

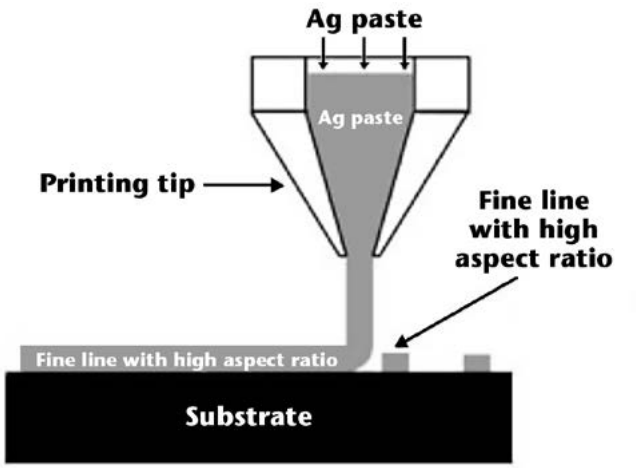


Figure 5: Cross section of printing tip.

modeling software; then, each surface mount component is modeled in 3D and each conductive trace is drawn. The structure of the part is also modeled around the components and traces. The structural or dielectric components (analogous to the FR-4 PCB substrate) are sliced and a set of 2D layer files are produced. Conductive areas are also converted to 2D files. The positions of each component to be pick-and-placed are measured and saved to a pick-and-place file. The resulting set of design files are then imported into the proprietary software as individual jobs and the specifics of each job are assigned, such as whether the given job will be a conductive trace or a layer of structural material. Added to this are jobs which perform 3D laser displacement scans of the part that will be used to modify the exact printing height of each print job or execute automated recognition fiducially. Once all the design files have been imported into configured jobs, the set of jobs, called a project, constitutes a fully automated 3D printing program code which can be run over and over at the touch of a button.

3D Printed Circuit Structures using a 3D Layering Process

Building three dimensional objects through a DPAM nozzle process is done through the deposition of layers in a process known as layering. Similar to stacking pages of papers to form a pile, a nozzle (or pen tip) dispenses material at a certain thickness (in the Z direction) onto an initial substrate, then, repeating the process, creates a 3D object. Each layer is deposited on top of the previous layer in a continuous, serpentine fill pattern. Figure 6 below is an artist's rendition of the direct print layering process.

The pitch between the dispensed lines is a critical factor in how successful a build is. It determines not only the volume of the objects, but the surface finish of the print surface of the subsequent layer. Maintaining a constant layer thickness ensures that each layer is consistent and thus the reliability of the build. Little variation in layer thickness cuts down the overall build time by omitting an intermediate step for measuring the exact layer thickness. The thickness of each layer is primarily controlled by the space (or dispense gap) between the pen tip and the surface it is dispensing on. Several dispense parameters (see the 3D Build Optimization section) can be tuned to allow for different thicknesses; however, these are governed by the physical characteristics of the material itself (i.e., viscosity, particle size, thixotropic or Newtonian, etc.). Consideration of the large spacing between lines can lead to material not adhering in the following layer, thus causing the build to fail. Lines that are overlapping produce an irregular, non-flat surface. This can lead to an uneven amount of material deposition in the

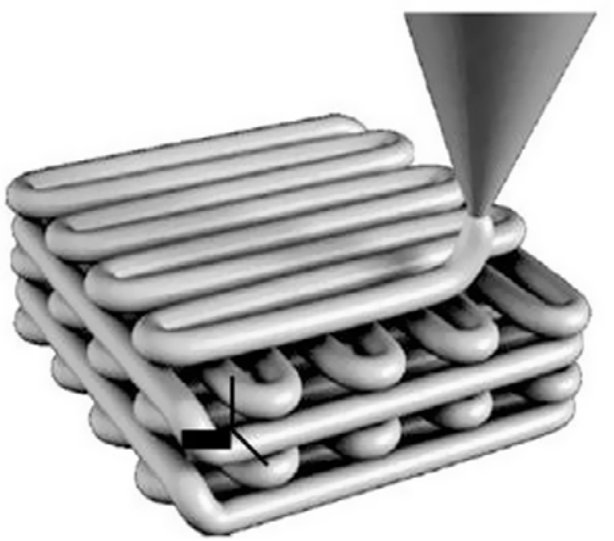
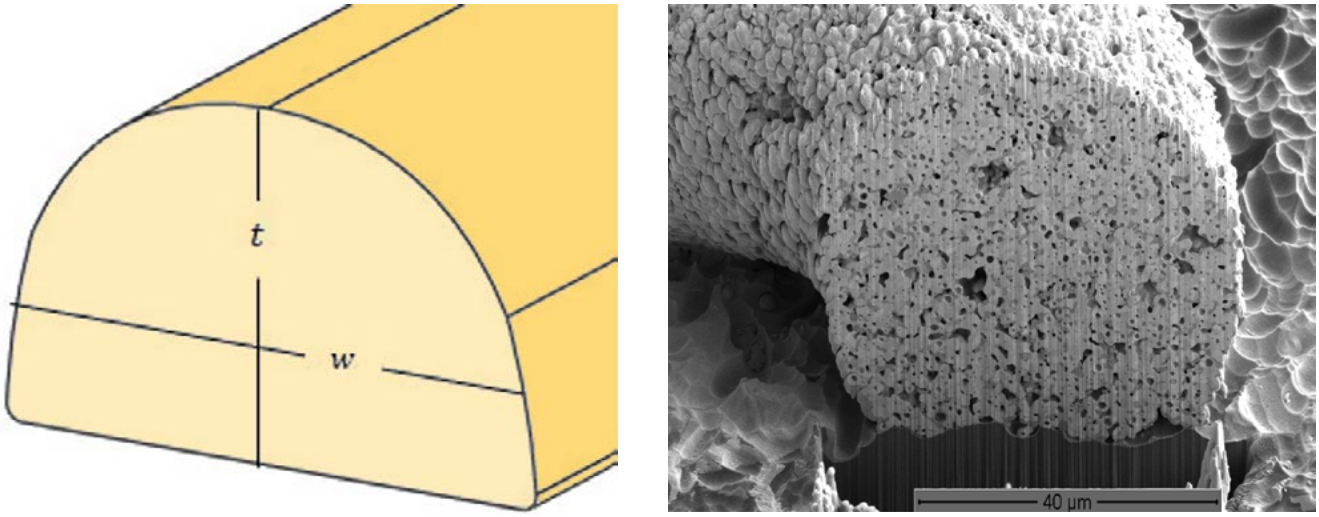


Figure 6: Example of building a three dimensional object through a direct print layering process[6].



Figures 7a and b: Graphic of a cross-section of a printed line showing dimensions (a) and a directly printed line of silver on silicon cross sectioned (b).

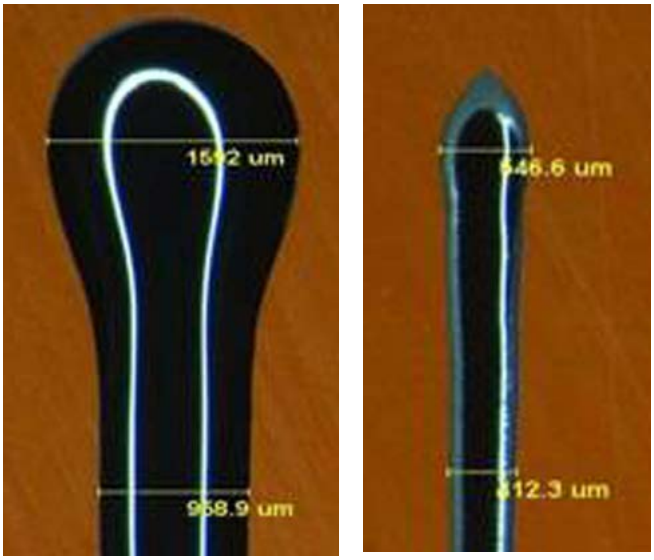
superstrate. The consistency of lines deposited lines can be studied by measuring their width (***w***) and thickness (***t***) as shown in Figure 11.

Optimizing the Printing Process

A process that can employ the dispensing of multiple materials is essential to characterize and study how these materials will behave during the process. The current DPAM nozzle technology has several different parameters that can be adjusted for optimal dispense control. A side-by-side comparison of controlled and uncontrolled resistive paste is shown in Figure 8.

The large, circular blob seen in the Figure 8a that was made at the beginning of the print is caused by improper settings of the different print parameters. In this particular case the dispensing pump was set to dwell on the start for too long (on the scale of milliseconds). In this case, the gantry system was idle during the valve opening sequence; hence, material would flow out of the pen tip, accumulating around the sides. Another issue is the steady state or continuous print condition which can cause the line to be much wider than intended. By drastically decreasing the dwell time and increasing the print speed, the line from Figure 8a was able to be narrowed and made into a much more uniform shape, as shown in Figure 8b.

Determining the dimension of the nozzle tip, also known as the pen tip, is the first step when designing a process to build an object. As previously mentioned, a material's dispensed dimensions can be affected by the size of the pen tip, the material composition of the pen tip and the material being dispensed. The surface energy of the substrate must overcome that of the pen tip's orifice in order for the material to release from the pen tip and adhere to the substrate. Additionally, there is a pressure from the pump that will add an additional force down-



Figures 8a and b: Uncontrolled material dispense (a) and controlled material dispense (b).

ward and away from the pen tip. Combined, these two forces will provide continuous flow that will force the material to release from the pen tip and onto the substrate. Maximum accuracy is achieved when the pen tip is kept close to the substrate (less than 1 mm) so that material will lie down onto the surface. The outer diameter of the pen tip (OD) will dictate the width of the printed line given the surface tension drawn to the pen tip. If the print parameters are set accordingly, then only the bottom surface of the pen tip should come into contact with the pen tip before being applied onto the substrate and subsequent superstrates.

The inner diameter of a pen tip restricts a material's ability to flow. Depending on the distribution and particle size within the material carrier, the material can be made to flow reliably during a printing process. Typically the bulk of the material's particle size is one-tenth the size of the pen tip's inner diameter for consistent flow, d[3,4,9,10]. For "large gap" applications, the inner diameter (ID) of the pen tip will determine the width of the line. This is because the bottom surface of the pen tip is no longer in contact with material being dispensed. However, the flow rate of the material through the pen tip must be high enough so that it forces material away from the pen tip and breaks the surface tension that can be created from the outer edges thus forming good adhesion to the surface of the substrate. The flow rate can be controlled by the valve displacement, essentially restricting material from flowing out of the pen tip. A larger displacement increases the volume of material flowing while a smaller displacement restricts and decreases the volume of material flowing. The rate of valve displacement can also contribute to the control of the material dispensing process. Higher speeds of valve movement cause the initial shear force on the interface of material and valve to be high. This transient mechanism can cause an accelerated flow rate out of the pen tip which yields less control on the initial dispense of material. However, this parameter is critical for low viscosity and thixotropic materials. Figure 14 shows four lines dispensed while only increasing the valve displacement by 100 µm from right to left.

Restricting how much material can flow through the opening between the seal of the valve and inner chamber of the dispensing pump can help control how much volume is displaced within the printing system. However, the rate at which the material is actually displaced is dependent on the amount of back pressure that is applied to the material. Figure 11 shows pressure being decreased from 45psi to 15psi (left to right) while all other parameters are kept constant.

It is evident that increasing pressure will cause more material to flow out of the pen tip. The print speed, or the speed at which the dispensing pump moves while dispensing, was kept constant thus material flow rate is much

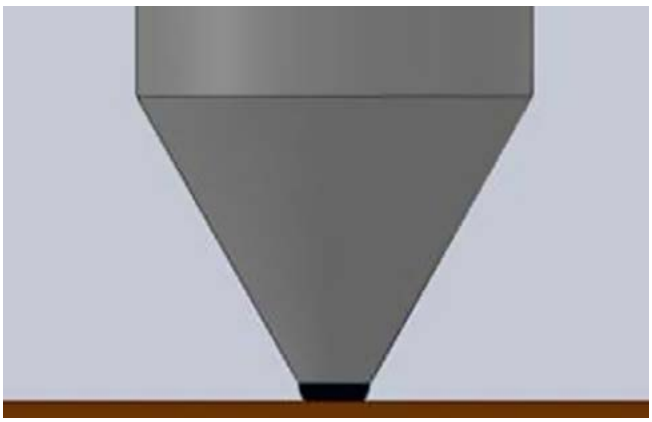


Figure 9: Dispensing pen tip with optimized print parameters.

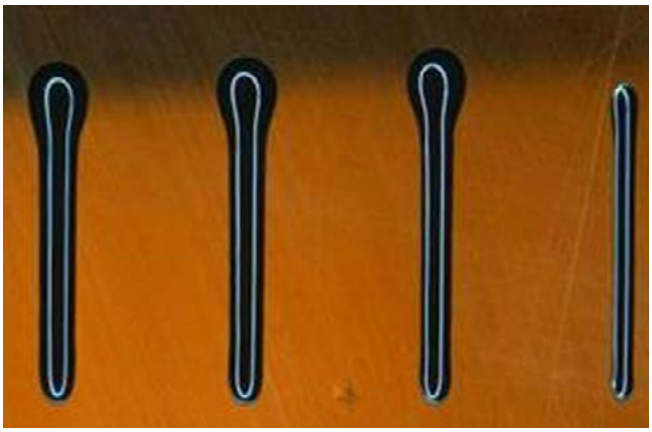


Figure 10: Material study of only varying valve opening. Rightmost line is smallest opening.

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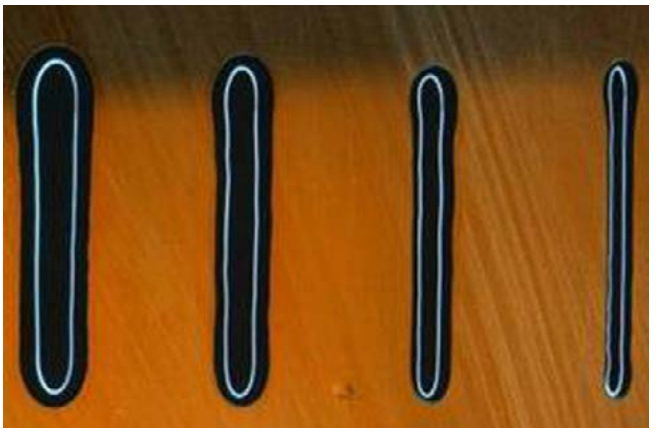


Figure 11: Material study by only decreasing pressure.

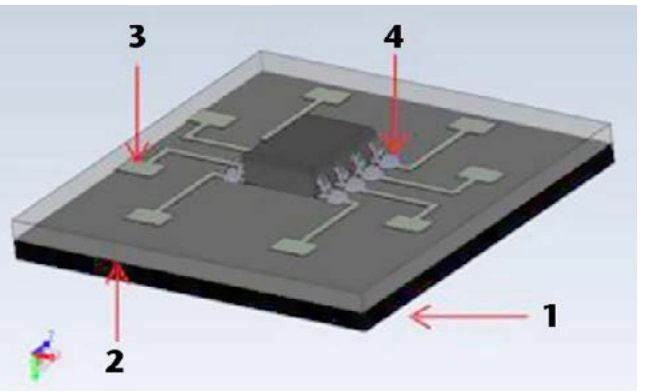


Figure 12: IC test circuit. CNT composite (1); SLA material (2); silver conductive paste (3); silver adhesive (4).

greater than what was minimally necessary for the material to adhere to a given substrate. Closely matching the print speed to the material's flow rate optimizes the line dimension, thus controlling the material dispensed. This becomes paramount when trying to build 3D objects with DPAM because it prevents excess or unwanted material from interfering with adjacent lines. Lines that overlap in a patterned layer while building a 3D object will lead to a greater surface roughness and cause subsequent layers to also be uneven.

Printed Circuit Structure Demonstration

The DPAM tool is equipped with a pick-and-place system consisting of an actuating head, components rack, multi-vacuum head changer, and fiducial camera. The TL555 integrated circuit timer's (IC) pins are 1.27 mm long and 0.5 mm wide and the traces are designed to be just as wide (pen tip with an OD of 400 µm) to better facilitate the placement of component. The substrate is a carbon composite of nanotubes (CNT) with a superstrate layer of SLA material. Silver conductive traces are DPAM printed on top before components are placed on top. The IC is adhered to the printed traces with a silver adhesive.

The entire part is built in one process with no need for fiducial points to be taken. However, the component rack's individual slots were designed to be slightly larger than the component in order for components to be manually inserted into the slot. This creates a situation where the component is not guaranteed to be sitting straight in the rack. It was corrected by the image recognition camera fiducially. From the center of the slot where the component sits, the camera goes over to the two points specified and shows the location of where they are meant to be. The user is then prompted with an image of a where the system recognizes the fiducial points. If incorrect, the user can indicate where the correct fiducial point is located. Figure 13 shows a picture of the proprietary fiducial image recognition interface and how

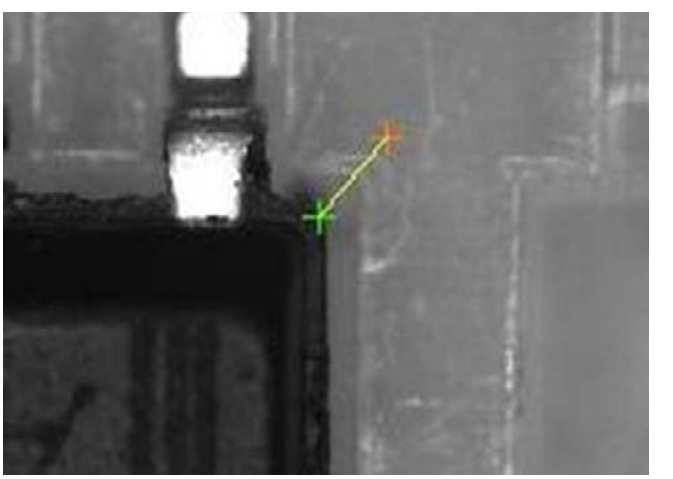
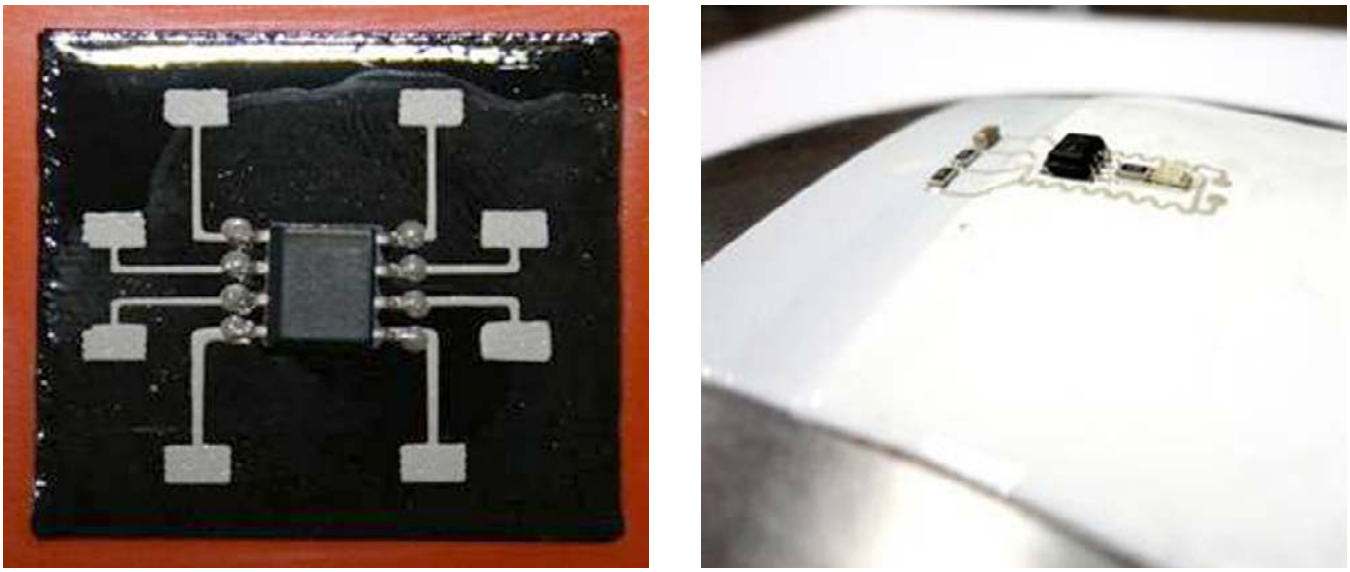


Figure 13: The orange marker indicates the coordinates of registered fiducial point; the green marker indicates the user correction.



Figures 14a and 14b: Completed test circuits built with DPAM process. Flat surface (a) and curved surface (b).

it allows for human intervention to correct for the component's position.

This system can correct for translation and rotation. These transformations ensure the vacuum head will grab the IC perfectly in the center. The angle computed is used to rotate the actuating vacuum head to the misplacement, enabling the component to be accurately placed.

The actuating vacuum arm has a threshold pressure sensor that sends an electronic signal to the tool when it has detected that the vacuum has been plugged. This allows the system to know whether it has created a sufficient amount of suction to lift the component. The suction head is brought down to a height in the Z direction until the suction threshold sensor is set off. The component is then lifted and the suction head, which was homed before it made its descent, is rotated by the angle calculated from the fiducial correction process.

The distance between the center of the traces and the IC's location on the component rack is computed for the IC to be placed. The laser displacement sensor is used to find the distance from the suction head to the surface where the component is to be place. The IC is 1.75 mm tall from where the leads touch the surface to the top of the packaging. This distance was subtracted to the reading from the laser displacement sensor to calculate the distance to travel to place the component. After the component has been successfully placed, the suction head is actuated and a dispensing pump pre-loaded with silver adhesive is brought over to the IC's pins. Material is dispensed for 500ms to ensure enough material is deposited for contact to be made between the conductive traces and the pins of the IC.

Conclusion

DPAM is able to combine 3D printing's structures with printed electronics' functionality at the resolution of DP. But it is still early, requiring labor intensive procedures that take time to produce the desired products and the desired automation that current 3D printers have achieved. While 3D printing has been around for more than three decades, DPAM has been around for less than one. The future of PCB will be heterogeneous printing thus enabling a new generation of electronic packaging. Future work for this will be in material research to functionally load materials for specific mechanical and electrical properties that promote 3D building. Additionally, new processes will be important to achieve proper features during printing; surface roughness or excess voids will need to be controlled. The DPAM process has not been fully studied nor optimized and this will be important.

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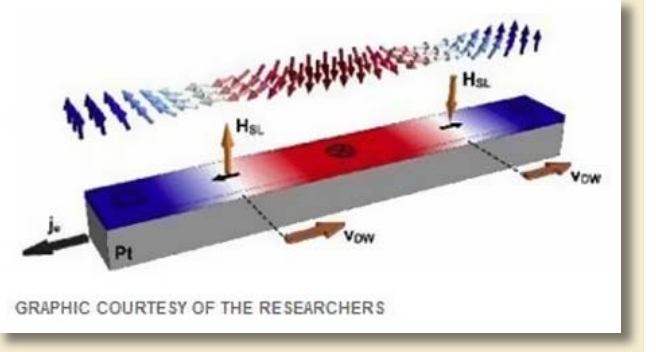
New Magnetic Phenomenon Leads to Better Data Storage

A magnetic phenomenon newly discovered by MIT researchers could lead to much faster, denser and more energy-efficient chips for memory and computation.

The findings, reported in the journal Nature Materials, could reduce the energy needed to store and retrieve one bit of data by a factor of 10,000, says the paper's senior author, Geoffrey Beach, an assistant professor of materials science and engineering at MIT. The paper's co-authors are graduate students Satoru Emori and Uwe Bauer, post-doc Sung-Min Ahn, and Eduardo Martinez of the University of Salamanca, Spain.

Beach says that hints of the new phenomenon have been reported for several years, but these had remained unexplained until now. "The new results could overcome a lot of what had seemed like fundamental limitations," in the control and use of magnetic materials. "It's a whole new approach to the design of magnetic materials."



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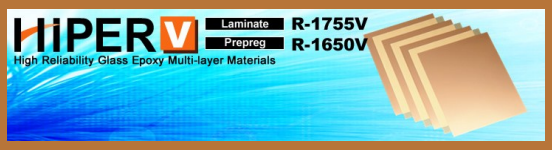

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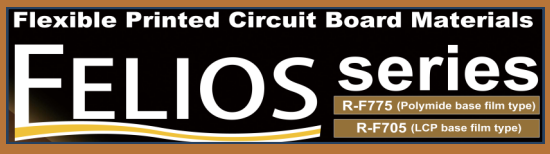

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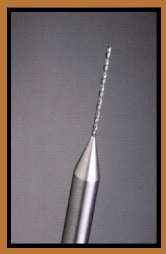




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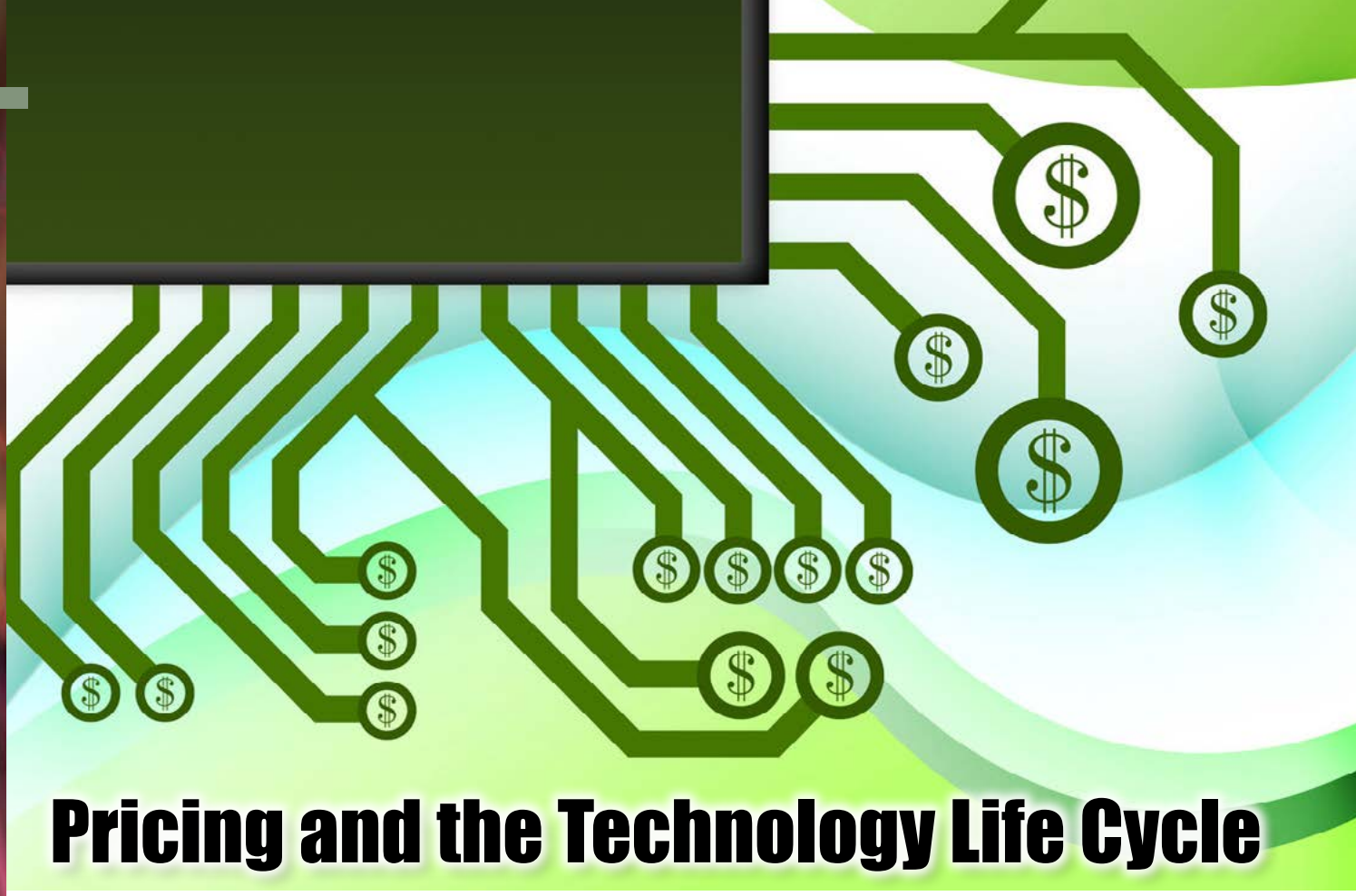

Pricing and the Technology Life Cycle

by Bill Burr and Nick Pearne
BPA CONSULTING

SUMMARY: Even without the distortions caused by greatly differing cost structures around the world, the economic impact of yield and efficiency improvements during the life of manufactured products and systems predicted by learning curve theory is an inevitable part of the technology life cycle.

How much is a product going to sell for next year if you've never made one before? Even without the distortions caused by greatly differing cost structures around the world, the economic impact of yield and efficiency improvements during the life of manufactured products and systems predicted by learning curve theory is an inevitable part of the technology life cycle. It can therefore be useful when developing a business/marketing strategy around an innovative product or technology to understand where pricing (and margins) may end up, particularly if the innovation has the potential to catalyze new applications and markets, implying that some sort of pricing history is nonexistent.

One of the problems with new technologies is the conflict that develops between proprietorship and standardization. If a technology is proprietary, single sourcing becomes an issue due to the need for supply-chain redundancy. If a technology is easily passed into the public domain, then commoditization becomes an issue with the inevitable erosion of margins and progress up the so-called "S" curve shown (Figure 1).

The Makings of a Winner: the 10X Factor

To have an impact, a completely new technology should offer an order of magnitude improvement over existing techniques—whether in cost, improved yields, manufacturing characteristics, or reliability. Something new has to be 10 times better to overturn the established order, as can be seen with, for example, the reductions in assembly time and improvements in assembly reliability and quality which occurred with the introduction of printed circuits as an alternative to hand wiring or wire-wrap (Figure 2).

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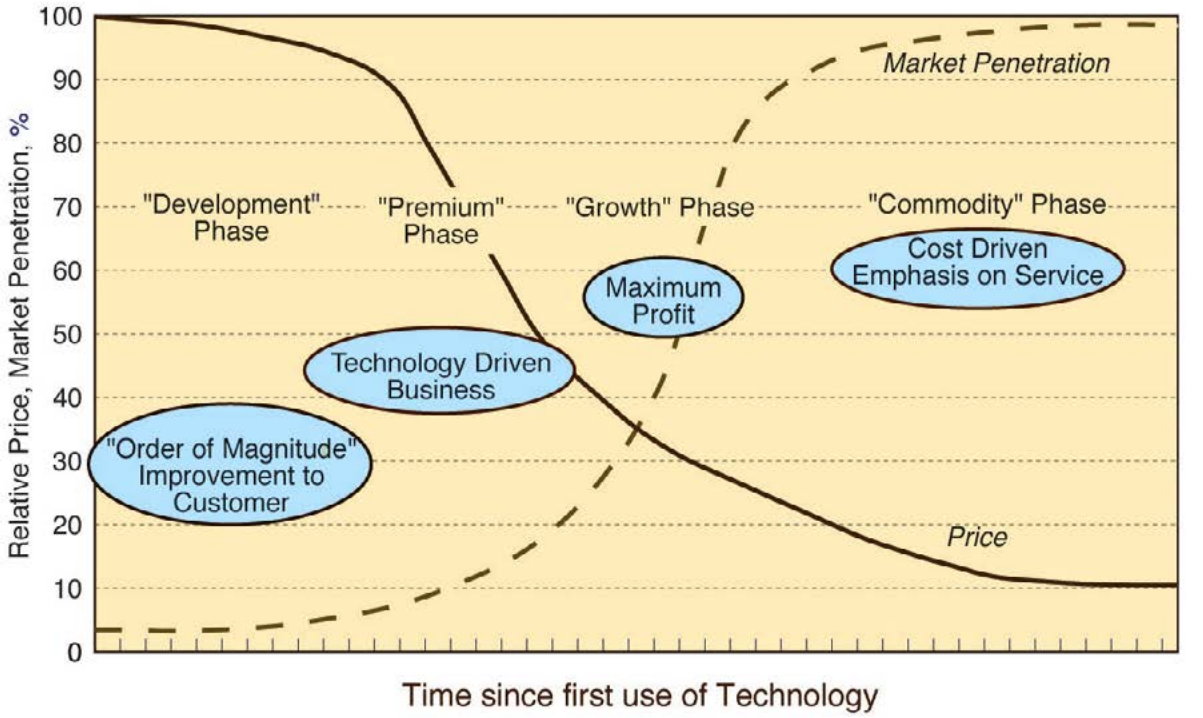

Figure 1: The technology S curve.

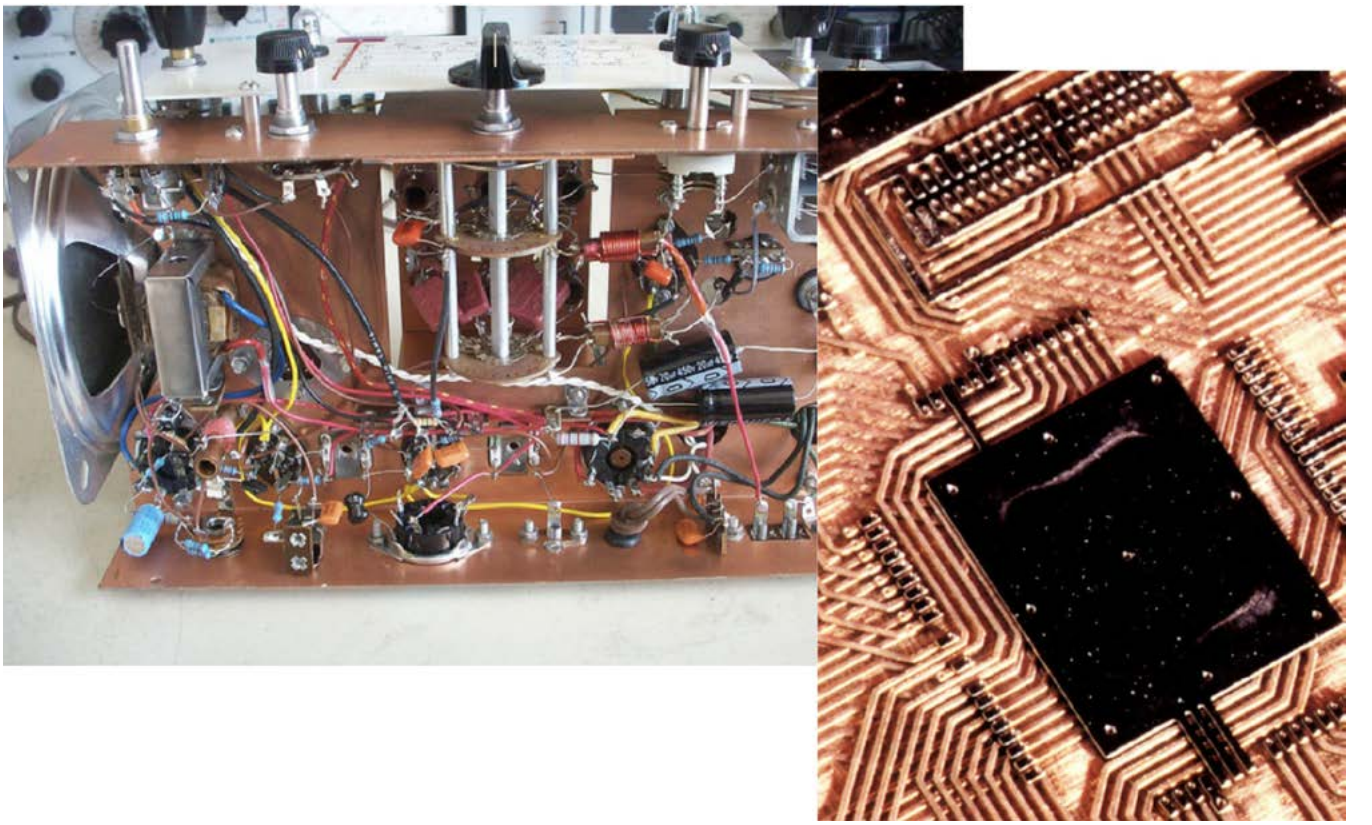

Figure 2: Printed circuits—a 10X improvement.

This level of improvement generally represents a significant margin opportunity. However, as a technology progresses up the S curve and demand grows, with very few exceptions, the early adopters and developers are generally unable to keep up: A developmental business model does not scale easily and experimentation is not compatible with on-time delivery performance. The technology is licensed or otherwise transferred to the public domain, and, as in the case with printed circuits, the transfer of the technology content inherent in materials, chemistry, and processes to specialised companies means the role of the printed circuit manufacturer becomes that of a transformer—of the customer's designs into printed circuit boards, and of a translator—of the customer's interconnection needs into specifications guiding the development of materials and processes to meet those needs. The result of this process is an inevitable erosion of margins.

Recombinational Opportunities: Regaining the High Ground

Despite the commodity aspects of the business, the position of the printed circuit manufacturer offers several advantages when the evolution of semiconductor technology or package types offer "recombinational" opportunities—interconnection and/or power management challenges can be met by recombining standard building blocks within the board. Such a situation is occurring now in the field of digital power. BPA's just-released report "Metal in the Board—Opportunities for Substrates Providing Enhanced Thermal and Power Management," details the dynamic markets and new applications becoming possible by the shift to surface mounted power devices and the rapid improvements in LED efficacies according to Haitz' Law. These opportunities are being met by a range of solutions, many of which are coming from the printed circuit manufacturers themselves as existing building blocks are recombined to provide low resistance thermal and electrical pathways in the board, such as those shown in Figure 3.

These recombinational solutions represent either specialized materials, advanced process know-how, or some degree of proprietorship. Depending on the width of the "moat" (the barrier to entry made up of know-how, engineering, and proprietorship) and the value recaptured by the technology (external functions it replaces, such as heatsinks, busbars, cabling, connectors, daughterboards, etc.), there is a window where development overheads can be recovered thanks to improved margins. But sooner or later, the transformation process and associated margins will fall under the iron fist of learning curve theory, even for what appear to be highly complex technologies.

Knowledge is Power

Most manufacturing people don't care for learning curve theory because it looks like a systematic approach to leaving money on the table. The learning curve pricing practices adopted in the '50s and '60s by major players in the budding U.S. semiconductor industry were more responsible than any other single factor for the financial erosion of the world semiconductor and consumer electronics industries. Billions of dollars in potential profits were sacrificed by pricing from learning curve forecasts to obtain market share, instilling along the way an expectation of dramatic reductions in cost per function. This "buy your way in" approach is consistent with the essentially infinite market demand for digital information processing. However one of the findings of BPA's MiB research is that certain applications, most notably

Figure 3: Innovation at work: MiB "DWPCB" type. (source: Häusermann GmbH)

solid state lighting, don't necessarily represent endless opportunity.

Yet, there are many applications in which the learning curve approach has real use because, like it or not, in a competitive market environment and for a wide range of processes, there is always at least a tendency for costs to follow its laws. An understanding of this process can provide a competitive edge in bringing new technologies to market.

The learning curve applies in some degree to any process or class of processes in which costs are susceptible to reduction by manufacturing experience, for example:

- Better tooling methods are developed and used
- Productivity is increased as equipment, processes, and, where needed, materials are evolved
- Design flaws are detected and corrected
- Engineering changes decrease over time
- Yields improve, reducing rework/recut and associated scheduling/setup issues

The degree of fit tends to be excellent for long-running processes with low material content and high added value such as making widgets, turbine blades or spark plugs. It is probably the worst for processes with extreme and uncontrolled variability. Printed circuit and particularly multilayer processes are certainly somewhere in the spectrum: The steady erosion of prices that has occurred over time suggests that both experience and market growth are, in fact, having an effect on cost and therefore on pricing. If such a trend is now in effect, there is no reason to expect that it will not continue into the future, therefore learning curve and market growth relationships might be used for MiB and other new technologies to look ahead at least in a qualitative way.

Learning Curve Analysis

The Cost vs. Quantity Relationship

As mentioned earlier, the learning curve depends on the fact that experience gained from increased production of any commodity causes a decline in manufacturing costs, and therefore inevitably in prices in a competitive market environment. More exactly, the theory states that every time the quantity of units (or lots) produced is doubled, the corresponding unit (or lot) costs decline by an experience factor F, also known as the learning or improvement ratio. This is determined by the relationship between resources (typically process cost) required to produce double the reference quantity, Q_o:

$$F = C_2/C_1 \qquad (1)$$

where C_1 is the initial average unit cost and C_2 is the average unit cost for double the reference quantity. From (1) it is evident that the higher the value of F, the less change in cost is to be expected due either to process maturity or highly customized content as might be expected from build-to-order machine tools. It is also important to note that the term "experience factor" does not refer to the actual experience a given vendor may have in the manufacturing of the product. The term relates to the degree of maturity of the process (i.e., the headroom that still exists for cost reduction through automation, enhanced material sets, tooling modifications, and so forth).

For an initial quantity Q_o and a final quantity Q, the number of "doublings" or fractions thereof for the total quantity produced is given by $\log(Q/Q_o)/\log(2)$. Therefore the unit cost behavior as a function of quantity can be written as:

$$C = C_1*(F/100)^{(\log(Q/Q_o)/\log(2)} \qquad (2a)$$

where C is the unit cost after quantity Q units or lots, C_1 is the first unit cost, and F is the experience factor in percent: a value of 75 for F would be typical of very steep (fast) learning curves, in which process consolidation proceeds rapidly with corresponding reductions in changeover time, improvements in yields, etc.

Equation (2a) is awkward to handle since the principal variable, Q, appears in the exponent. It can be rearranged (and simplified) by noting that in general a^log(b) is equivalent to b^log(a) since either expression can be writ-

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ten as e^[log(a)*log(b)]. An alternate and better form for (2a) is therefore

$$C = C_1*q^k \qquad (2b)$$

where $q = Q/Q_o$ and $k = \log(F/100)/\log(2)$.

The total cost, T, to produce a quantity Q units or lots can be obtained by integrating eq. (2b) over the limits q = 0 to q = Q:

$$T = C_1*\int q^k\, dq = C_1*Q^{(k+1)}/(k+1) \qquad (3)$$

The average cost, A, per unit or lot quantity is the total cost divided by the quantity:

$$A = T/Q \qquad (4)$$

For processes where the experience factor is accurately known, the average cost is often used to quote a lot or piece price to be effective over the entire production.

Suppose, for example, that a first lot of 10 pieces is produced at a cost of $20.00 by a process with a known experience factor of 80%. What would be the predicted piece cost for 1000 units?

For F = 80%, k is found to be log(.80)/log(2) = -.3219, and for this case the experience quantity Q = 1000/10 = 100. Therefore,

$$C = 20.00*100^{(-.3219)} = 4.5412$$

so that at the end of the run the production cost has declined to $4.54 per lot. The total cost, from eq. (3) becomes:

$$T = 20*100^{(.6781)}/.6781 = 669.7274.$$

The average production cost per unit quantity (1 lot) is therefore T/Q = $6.70 and the piece cost is about $0.67.

This approach can be used to create log-log plots for various experience factors, giving unit costs as a function of quantities and initial costs. For example, a process with 80% experience factor and an initial cost of 1.00 per unit can expect unit costs to decline to about 0.11 by the time 1024 (2^10) units have been produced. This not atypical of the semiconductor industry, where F may be 75% or even less. At the other end of the scale a complex, low volume product may be 90 or even 95%.

New Technologies: The Experience Factor

To use this analysis for new technologies, it is necessary to determine the experience factor. This can done using a broader experience base than the simple doubling shown in equation (1) by flipping equation (2a) around, provided the data are available. Specifically:

$$F = 10^{(\log(2)*\log(C/C_1)/\log(Q))} \qquad (5)$$

If the production cost of an MiB type IMS LED multichip substrate was 2.00 when 10,000 pieces had been produced (C_1) and the cost (C) is now 0.65 when 4,000,000 have been produced (Q=400), what is the experience factor F?

$$F = 10^{(\log(2)*\log(0.65/2.00)/\log(400))}$$

$$\text{or} \quad F = 0.878$$

What will be the cost for the 20,000,000th piece when Q will be effectively 2000 (20,000,000/10,000)?

$$k = \log(.878)/\log(2) = -.18771$$

$$C = 2.00*2000^{(-.18771)} = .4801$$

This example assumes a limited degree of process innovation is necessary in the introduction of a new layout for the same function/substrate. As is often the case in printed circuit manufacturing, where the emphasis is less on products and more on capabilities built on standardized processes, the experience factor may be even higher than 88%. It is important to remember that the experience factor "F" does not imply any particular degree of expertise or mastery of the technology. It is simply an index of the expected stability of processing costs over the lifetime of the design. Innovative technologies such as the DWPCB (discrete wire) and HCPCB (embedded bus) types, where "recombinational" techniques are used that vary greatly from design to design can expect to have factors in the mid to low '80s, depending on complexity (Figure 4). This suggests that first movers will de-

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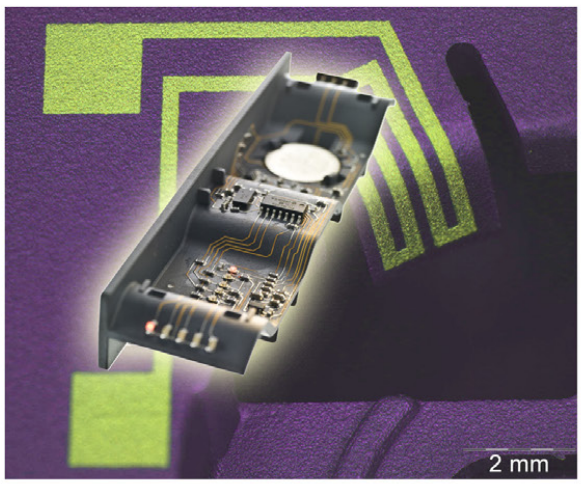

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MID is the abbreviation for "Molded Interconnect Device." The goal of MID technology is to unite electrical and mechanical functions in a single construction unit. The circuit tracks are integrated into the housing, enabling the reduction of weight and space, and are more eco-friendly than conventional PCBs.

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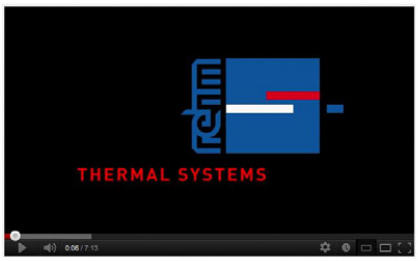

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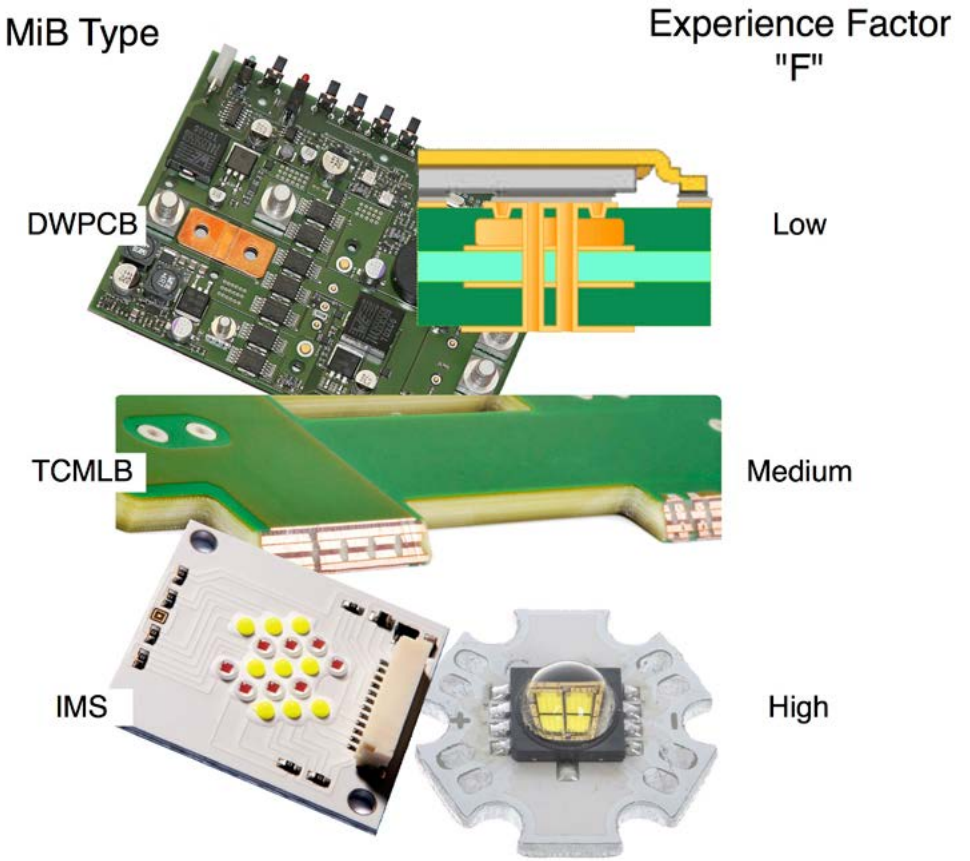


Figure 4: Relative experience factors for MiB types. (source: Häusermann GmbH, Schweizer Electronic AG, Lumitech, BPA/commercial)

rive maximum benefits from innovation, as subsequent price movements will be steep unless offset by functional integration or other "must have" characteristics of the new technology.

Integration with Market Growth

The basic insight that can be derived through the learning curve technique is an attempt to relate expected developments in competitive pricing directly to growth in the market, since growth in the market implies increased volumes and therefore declining unit prices. This can be done by integrating what is known about the learning curve relationships into the market forecast.

Generally speaking the volume in the electronics market follows an exponential growth law. Although there is lots of noise in the fine structure of the data, as for example the effects of the dotcom implosion, the recent recession, etc., some useful trend forecasting can be done on smooth averages. An exponential growth relation is

$$S = S_0 * 10^{\wedge}(T*\log(1+R/100)) \quad (6)$$

where S = sales volume at any time, S_0 = sales at time T = 0 (beginning of the period), and R = annualized percentage rate of growth.

BPA's forecast for the MLBTV (thermal via type) through the end of this decade gives an annualized percentage growth rate, R, of about 11%. and, if T = 0 at 2013, S_0 is \$0.60 billion. By 2020 (T=7) we have S = .60*10^(7*log(1.11)) = \$1.24 billion.

Forecast MiB type growth trajectories are shown in Figure 5. As we look out into the future with these projections it would be useful to know what might happen to pricing for the various types as a function of time.

In a competitive market based on standardized processes with limited proprietorship prices are probably related to costs in some rational manner so that we can also think of C and C_1 in equations (1) and (2) above as PRICE. This relationship can be fine-tuned considering those components within the build (such as laminates, copper, resists, etc.) which are externally sourced and therefore responsive to different cost dynamics. With this in mind we can say that for any sales volume S the corresponding quantity q must be S/C. From equation (2b) we can get

$$C = C_1 * (S/C)^{\wedge}k \text{ or}$$
$$C = (C_1 * S^{\wedge}k)^{\wedge}(1/(1+k)) \quad (7)$$

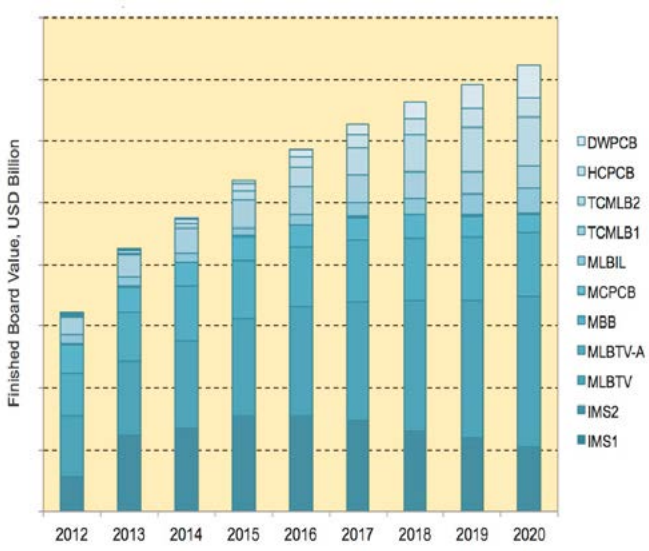


Figure 5: Forecast growth trajectories for MiB Types. (source: "Metal in the Board"; BPA Consulting)

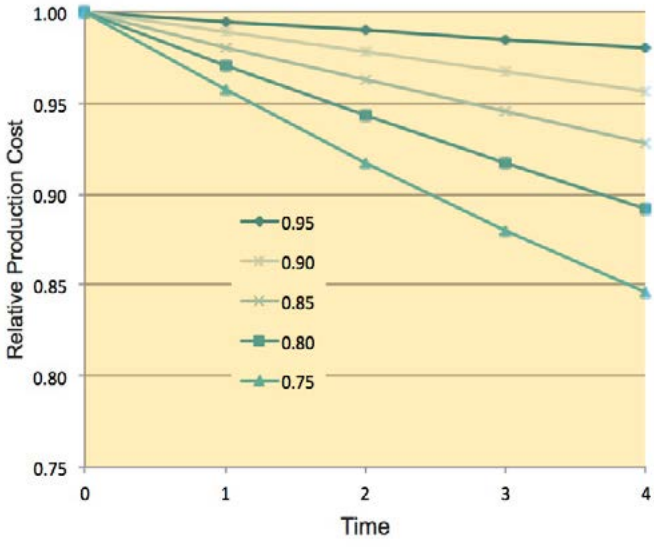


Figure 6: Relative production cost as a function of time in a growing market.

Then we can substitute the market movement from (6) and get C as typical price (cost) behaviour as a function of time in a growing market:

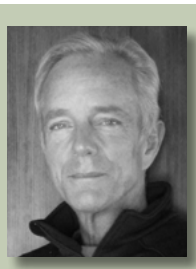
$$C = (C_1*(S_0*10\text{^}(T*\log(1+R/100)))\text{^}k)\text{^}(1/(1+k)) \quad (8)$$

This relationship is not as bad as it looks, and is easy to explore on a spreadsheet. Some results for the overall MiB market CAGR of 11% per annum are shown in Figure 6.

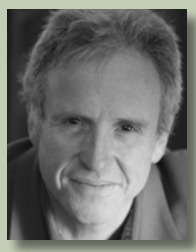
Conclusion

The measurable impact of the learning curve will be different depending on which sector of the MiB universe we're in: The trajectory of an MiB type with a high materials content such as IMS will be quite different from that of those types with higher process complexity and added value. As a consequence, the experience factor is likely to vary widely—from the high 90s for standardized IMS substrates and thermal via/MLBTV multilayers using consolidated, well characterized processes, to mid–low 80s for complex recombinational solutions such as DWPCB, HCPCB, and inlay board types. With typical 2–5-year lifetimes in a competitive marketplace, prices can be expected to drop from 7% to almost 50% of the value-added component of the board.

There is no escape from continuing and inexorable downward price pressure from entrenched expectations and trends. A clear understanding of how these work will confer a competitive advantage to the strategist concerned with bringing innovative technologies to the marketplace. **PCB**

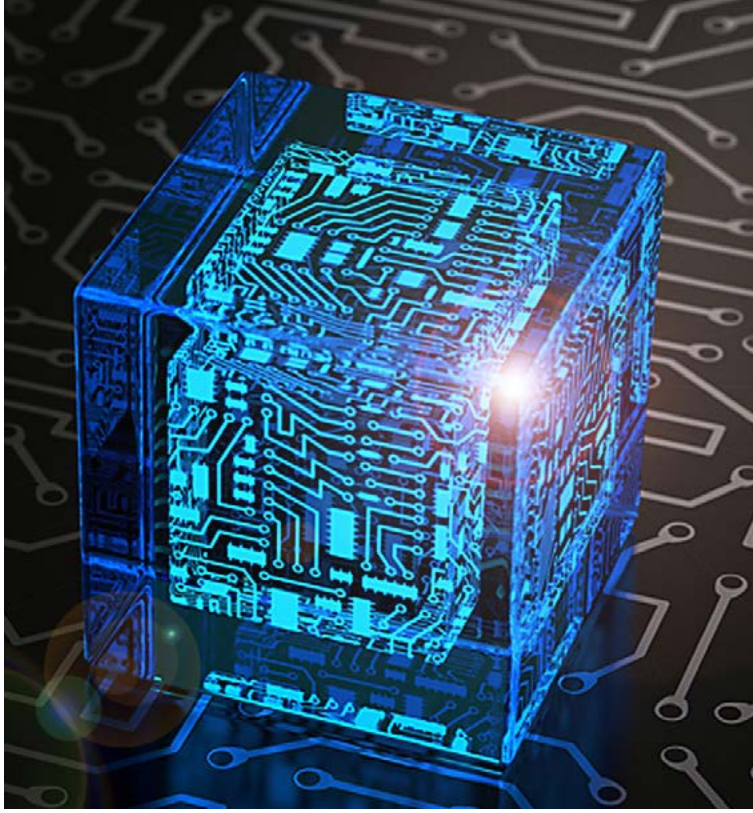


Owner and principal of LPC Ltd, William (Bill) Burr collaborates with BPA as senior consultant, and is a past president of the EIPC and vice chairman of EFIP. He may be contacted at w.burr@bpaconsulting.com.



Nick Pearne is co-founder of BPA and the director of several companies primarily involved in technology marketing and business development. Pearne may be contacted at npearne@bpaconsulting.com.

Building HDI Structures Using Thin Films and Low Temperature Sintering Paste



by Catherine Shearer and James Haley,
ORMET CIRCUITS INC.
Chris Hunrath, INTEGRAL TECHNOLOGY

This paper was originally published in the proceedings of the 2013 IPC APEX EXPO.

Abstract

Circuit complexity and density requirements continue to push PCB fabrication capability limits. Component pitch and routing requirements are continually becoming more aggressive and difficult to achieve in good yield with current fabrication strategies. The trend is to bring the PCB closer to the density requirements required for semiconductor packaging. The ability to place interconnecting vias in any location on any layer is crucial to PCB fabricators in meeting this high density interconnect (HDI) trend.

The two fundamental elements in any type of PCB, conductors and dielectrics, both have to be considered when building "any layer" HDI. These PCBs have specific challenges for processing while maintaining thermal and electrical performance. Careful consideration of the interplay of the fundamental elements is critical to fulfilling all of these requirements.

New methods and materials designed specifically with these challenges in mind are becoming available for building HDI.

Using materials specifically designed for HDI PCBs can significantly reduce the challenges faced when producing these boards. However, along with easing the challenges of fabrication, these materials must also demonstrate the right combination of properties to meet electrical and thermal requirements while also being reliable. Validation of these new technologies is currently underway.

Background

Back in the day, just taking advantage of double-sided-clad increased density. Being able to route traces in the same location on each side of the PCB, interconnected with plated through holes, added significant density compared to a single-sided PCB (Figure 1). Logically, as chips became more powerful with more I/Os, adding layers became the natural progression.

However, HDI is not just about layer count. Adding layers has a diminishing return as the through holes and vias grab valuable real estate.

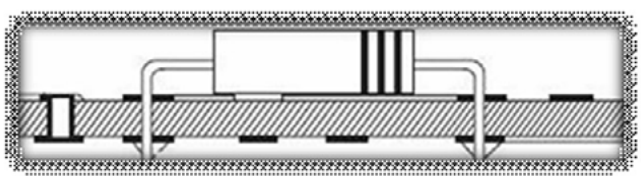


Figure 1.

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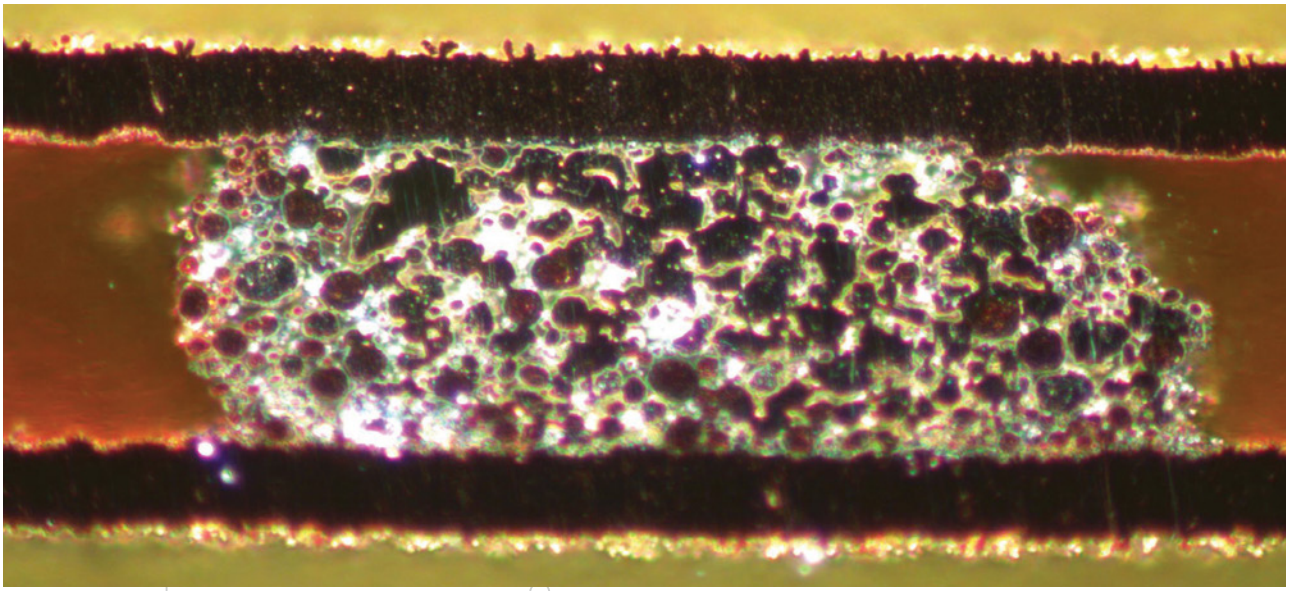

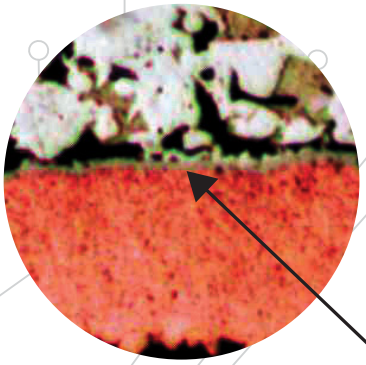

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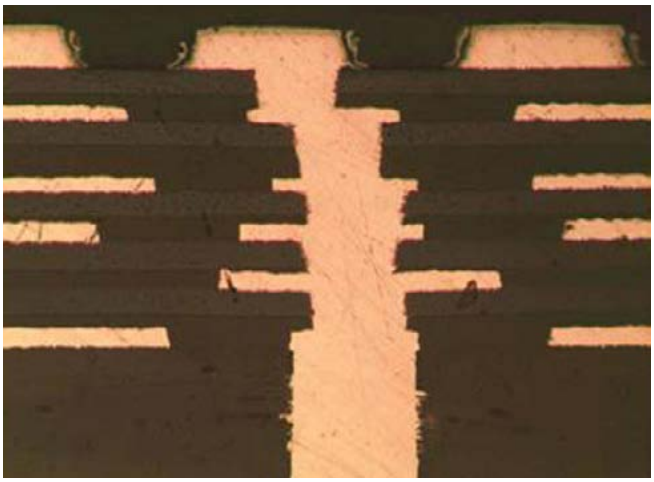

Figure 2: Sequential build-up.

Buried vias and "subs" provide an intermediate solution to higher density requirements, but these techniques greatly increase the process complexity and time in the PCB fabrication facility.

As the high density trend marched onward, build-up or sequential lamination became popular as laser drilling and better plating technology enabled blind microvias. Sequential build-up has the big density advantage of placing vias anywhere on any layer, but each layer has the process steps of an individual PCB. Lamination and plating capacity must be greatly increased to accommodate this solution (Figure 2).

There is a growing gap between cost-effective PCB manufacturing and HDI PCB requirements. New technologies—materials and methods—are needed for the industry to meet current and future demands.

Introduction

What if vias could be formed without plating? More importantly, what if the vias could be formed before lamination? If vias could be made this way, trips through plating and lamination can be greatly reduced. Making this possible would require the insertion of a conductor into vias in the dielectric layers between the individual circuit layers. This may be done several ways.

Some methods do this to C-stage (cured) dielectrics and some to B-stage (uncured) dielectrics. Ideally, the conductive material would be in liquid or paste form so it may be inserted into the vias after drilling, but before lamination. In applying the ink or paste, measures must be taken to ensure that the surface of the dielectric is not contaminated with conductive residue that can lead to electrical leakage, migration, etc.

Creating the interconnecting vias before lamination can greatly simplify the PCB manufacturing while still enabling via placement anywhere on any layer. In addition, formation of conductive vias prior to lamination may be combined with traditional processes for circuit formation and lamination, thus allowing the most efficient and cost-effective use of the PCB shop.

First Element: The Conductor

Sintered vs. Non-Sintered

Sintering refers to a process where a mixture of particles are fused together, usually thermally. Sintering mixtures can be used for structures and dielectrics, as well as conductors.

Conductive sintering products have been used in electronics for some time with ceramic thick film technology (cermet). Cermets require high temperatures (>800°C) for sintering and often ceramic substrates as the dielectric base material.

Non-sintering conductive pastes based on polymers, rather than ceramics, have been used with PCB materials as well as in printed electronics. These polymer thick film (PTF) materials are typically uncured liquid polymers, usually epoxy or acrylic based and filled with conductive particles. As the polymer cures and shrinks, the particles come in to contact with each other and the substrates making the connection (Figure 3).

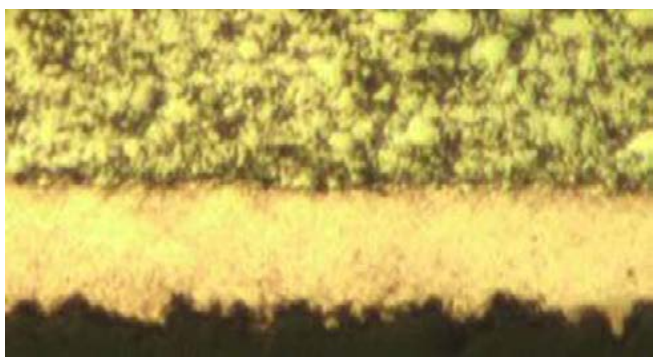

Figure 3.

PTFs have the benefit of low cure temperatures and are compatible with all kinds of polymer substrates. Two challenges with PTFs are changes in conductivity due thermal expansion and oxide on the surface of the individual particles. Silver is a popular choice for the latter because its oxide is reasonably conductive.

Sintered Interconnect Matrix Components	Melting Point (°C)	Percentage of Matrix
Cu	1085	>85%
Cu6Sn5	415	
Cu3Sn	640	
Bi	271	< 15%

Table 1.

The resistance behavior of PTFs is altered by temperature changes in reliability testing as well as in-service conditions. The need to pass traditional reliability testing therefore makes it challenging to implement PTFs in Z-axis interconnects.

Transient Liquid Phase Sintering

TLPS (transient liquid phase sintering) takes advantage of the fact that a liquid metal (e.g., tin) will interdiffuse with a non-molten metal (e.g., copper) to form a solid metallurgical joint at relatively low temperatures. This type of interdiffusion—in this case between copper and tin—results in a metallurgical bond between the two metals that is stronger than a mere layer-to-layer interface.

Interdiffusion between metals has long been used in electronic assembly to create strong, environmentally robust electrical interconnects. Solder joints of all kinds rely on a copper/tin diffusion and intermetallic formation to provide a strong, lasting bond.

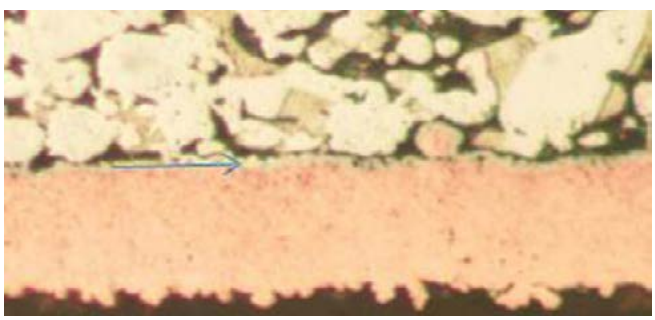

Figure 4: TLPS interconnects that provide a continuous metallurgically bonded electrical pathway.

A conductive paste may be formulated with TLPS characteristics so that sintering of the metals in the paste is possible at normal PCB laminating temperatures (as low as 180°C). The use of tin in such a TLPS paste has the added benefit of forming metallurgical bonds not just through the bulk of the paste interconnect, but also with the copper foil circuitry—just like solder would (Figure 4). However, unlike solder, the TLPS paste will not wet beyond the vias footprint and will not remelt during subsequent processing. Thus, the TLPS-paste-filled-via metallurgically ties the circuit layers in the Z-axis during standard lamination conditions. Like plated vias, TLPS paste interconnects provide a continuous metallurgically bonded electrical pathway.

Within the bulk of a TLPS paste via, copper and alloy particles "micro-weld" together to form a network of copper particles joined by copper-tin intermetallics and alloys. The remelt temperatures of the various phases are well above reflow temperatures and for all intents and purposes, non-reversible in the PCB (Table 1).

TLPS pastes can provide the via conductor stability necessary to enable a change in the PCB manufacturing sequence. Because the bonds are metallurgical and not just relying on particle contact, they have the ability to meet traditional electrical and thermal reliability requirements.

This opens many possibilities in PCB design and fabrication.

Second Element: The Dielectric

TLPS pastes have been used successfully with both C-stage and B-stage dielectrics. Using B-stage dielectrics have the benefit of creating

the Z-axis connections while bonding layers together. Of course a B-stage dielectric becomes a C-stage dielectric once laminated and cured. Consideration must be given to the flow characteristics of this layer for two important reasons. First, any resin that might flow and travel between the innerlayer copper foil surface and the TLPS paste before the intermetallic is formed will prevent the best possible interconnect. Second, flow of the resin may push the TLPS particles before they are locked in place. Successfully controlling these two characteristics comes from understanding and managing the process, but the right choice of materials can lead to high repeatability and high yields.

B-Stage Materials for TLPS Paste Z-Axis Interconnects

While flow of the B-stage resin may cause sintering issues, it is essential for layer-to-layer bonding. Loss of adhesion as well as lamination voids will cause issues in the PCB structure, and any successful HDI system must be free of these two defects.

Ideally, a B-stage material well suited for a TLPS interconnect would flow in the Z-axis only. This would allow bonding and in-fill between the copper circuits without pushing the paste around laterally before sintering. Such a material would be impossible to make; however, it is possible to manage the x-y flow and make very reliable connections.

Standard flow prepregs rely on the glass fabric for Z-axis thickness control and for resin retention to prevent voiding. They are the industry standard building block, even in HDI build-up methods.

Using standard prepregs with TLPS requires a greater understanding of their flow characteristics because of the potential for the prepreg resin to alter the shape or position of the TLPS-paste-filled-via as it flows. Things like heat rise and shelf life become even more critical.

HDI builds often require thinner, low glass/resin rich prepregs. This has the advantage of better laser drilling and better fill in fewer plies; however, the higher resin content has a disadvantage in the TLPS paste interconnect process. The higher proportion of resin exacerbates the flow problem. Not managed, the flowing resin can push the paste, even to the point of sweeping it away. Figure 5 shows a laser drilled, paste filled via before lamination. Note the gaps in the glass fabric.

Figure 5: A laser drilled, paste filled via before lamination. Note the gaps in the glass fabric.

These areas are resin-rich and can move the paste in the via and potentially interfere with sintering quality and the formation of a continuous metallurgical network during lamination. In order to reduce the need to pre-engineer the process for suitable flow characteristics, no-flow prepregs may be substituted for standard prepregs in the TLPS paste via process. No-flow prepregs, more accurately called "very low flow" prepregs, do not rely on the glass as much for flow control. This offers better predictability in lamination and will help preserve the shape and position of the TLPS-paste-filled-via before sintering.

No-flow prepregs come in many different varieties from epoxy to polyimide, lead-free compatible and so on. These materials need to be studied individually for compatibility with both the fabrication process and the PCB requirements, but may offer many opportunities for straightforward implementation with TLPS interconnects.

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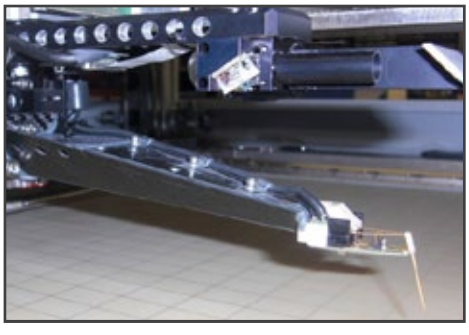

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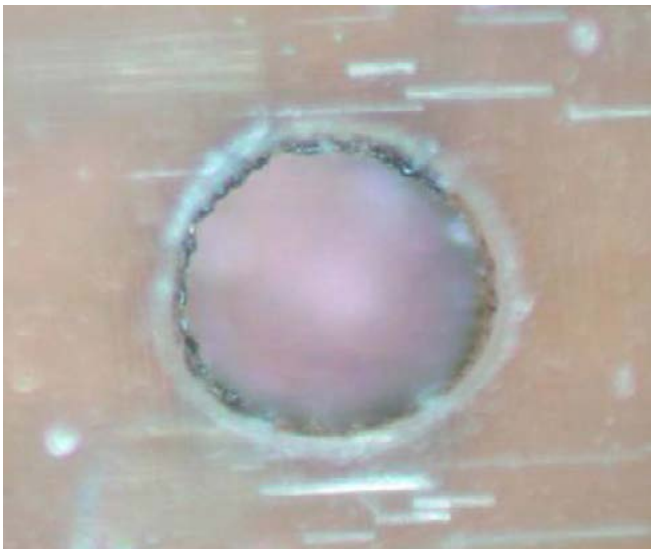


Figure 6.

Laser drilling B-stage materials is not normally done, but is required to take advantage of the pre-lamination via formation sequence. With glass fabric materials, the ends of the fibers tend to melt, forming "slag" droplets at the ends of the bundles (Figure 6).

Films tend to laser drill better, even in B-stage form. This is due to a uniform composition—all polymer instead of polymer plus glass. The type of laser used needs to be matched to the film as optically transparent films do not respond well to UV laser energy.

Many bonding films are available to the industry for flexible PCBs. These films are designed to be flow-reduced because it is common to machine the film prior to lamination. This kind of flow characteristic is very good for TLPS paste. Unfortunately, flex films contain one or more plasticizers which not only impart flexibility, but are integral to the flow control. Many plasticizers soften readily with heat and undergo large amounts of thermal expansion. Neither of these is desirable in HDI stack up structures.

Considering the requirements for HDI PCBs implementing TLPS interconnect, it is possible to develop a film without the plasticizers needed for flex. HDI PCBs are free from the dynamic bending requirement. This opens up some interesting formulation possibilities.

The new film concept is to replace the "rubberized" matrix with a polymer matrix that will behave more like the glass weave, but without the negatives. A proprietary high-temperature polymer is crosslinked to better mimic woven glass without the differential lasing characteristics, poor dielectric performance and resin wetting issues common to glass. This matrix is combined with a primary high-temperature B-stage resin with high bondability, long shelf life and will not advance during via formation and TLPS paste installation steps. This system can provide ease of use with interconnecting TLPS pastes, offering process latitude and thermal reliability.

By designing the dielectric film with both the paste interconnect process and the HDI PCB form-factors in mind, implementation of TLPS Z-axis interconnect becomes straightforward. The entire materials set has been designed to work together, with minimal impact to standard PCB manufacturing processes, and to support thin high-density PCBs with high electrical performance characteristics. With this film design, proper flow control of the resin can be tailored to the TLPS paste to maintain the unsintered paste in a well-defined via shape and not allow resin interference with the formation of a metallurgical bond to the copper pads (Figure 7). The interconnect is therefore dense, continuously metallurgically interconnected from pad to pad, and consistent from via to via.

The film system is not dependent on glass fabric, thermal aging, etc., for flow control, so the resin effect on the TLPS via is predictable and consistent over a long shelf life. Also, the film

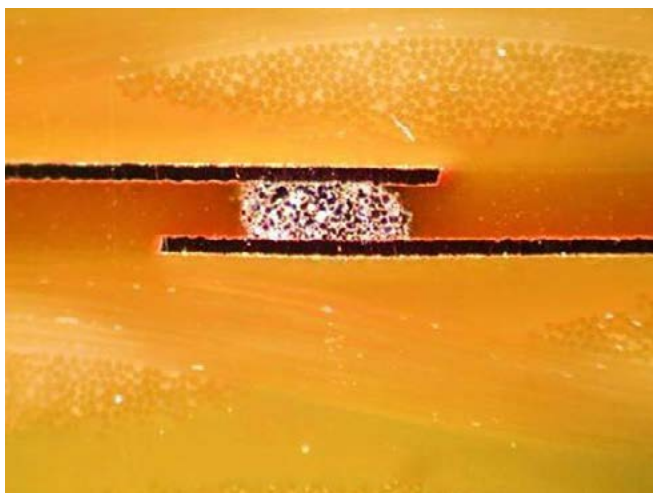


Figure 7.

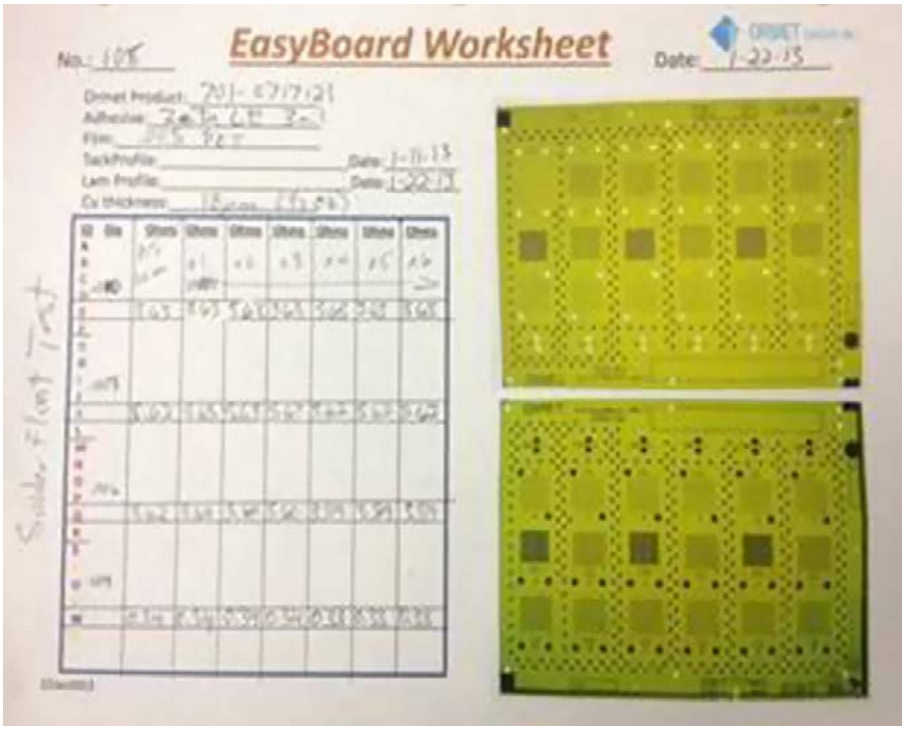


Figure 8: The effects of thermal shock on the TLPS Z-axis interconnects.

as copper plated and filled microvias.

This new film design was put into a test vehicle to examine the effects of thermal shock on the TLPS Z-axis interconnects (Figure 8).

Figure 8 shows some resistance measurements on a "daisy chain" test vehicle with six, 10-second solder floats at 288°C (Figure 10).

Also tested were 4, 6, 8 and 10 mils vias. 100% of the interconnects had very little or no change in resistance. The 4 mil via daisy chain was put back in the 288°C solder for a full minute and rechecked for resistance; again, there was no change. Figure 9 shows a continuous alloy formation with the copper foil at the bottom of the via.

is a stand-alone dielectric without the electrical performance and thickness constraints imposed by glass, but with thermal properties similar to a lead-free compatible glass reinforced system. The TLPS interconnects can therefore be short, in addition to the capability of placement anywhere in the PCB, and the overall structure can be very thin.

The intended result of this system approach is an HDI process that is less demanding on the PCB shop while providing the same reliability

Conclusion

Combing a TLPS paste with a film that is engineered without the constraints of flex can produce thermally reliable Z-axis interconnects. The TLPS paste offers a plating-like metallurgical bond to the copper innerlayers while the film allows proper sintering and controlled Z-axis expansion. Together, these materials give the PCB manufacturer ease of implementation of high-reliability sintered-paste interconnects and more construction options for HDI structures. **PCB**

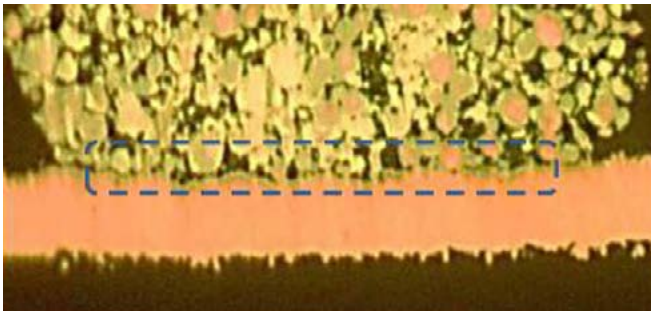


Figure 9: A continuous alloy formation with the copper foil at the bottom of the via.

Catherine Shearer is a senior scientist at Ormet Circuits in San Diego, California.

James Haley is vice president of sales and marketing at Ormet Circuits in San Diego, California.

Chris Hunrath is vice president of technology at Integral Technology, based in Lake Forest, California.

Operational Excellence Through Continuous Improvement

by Steve Williams

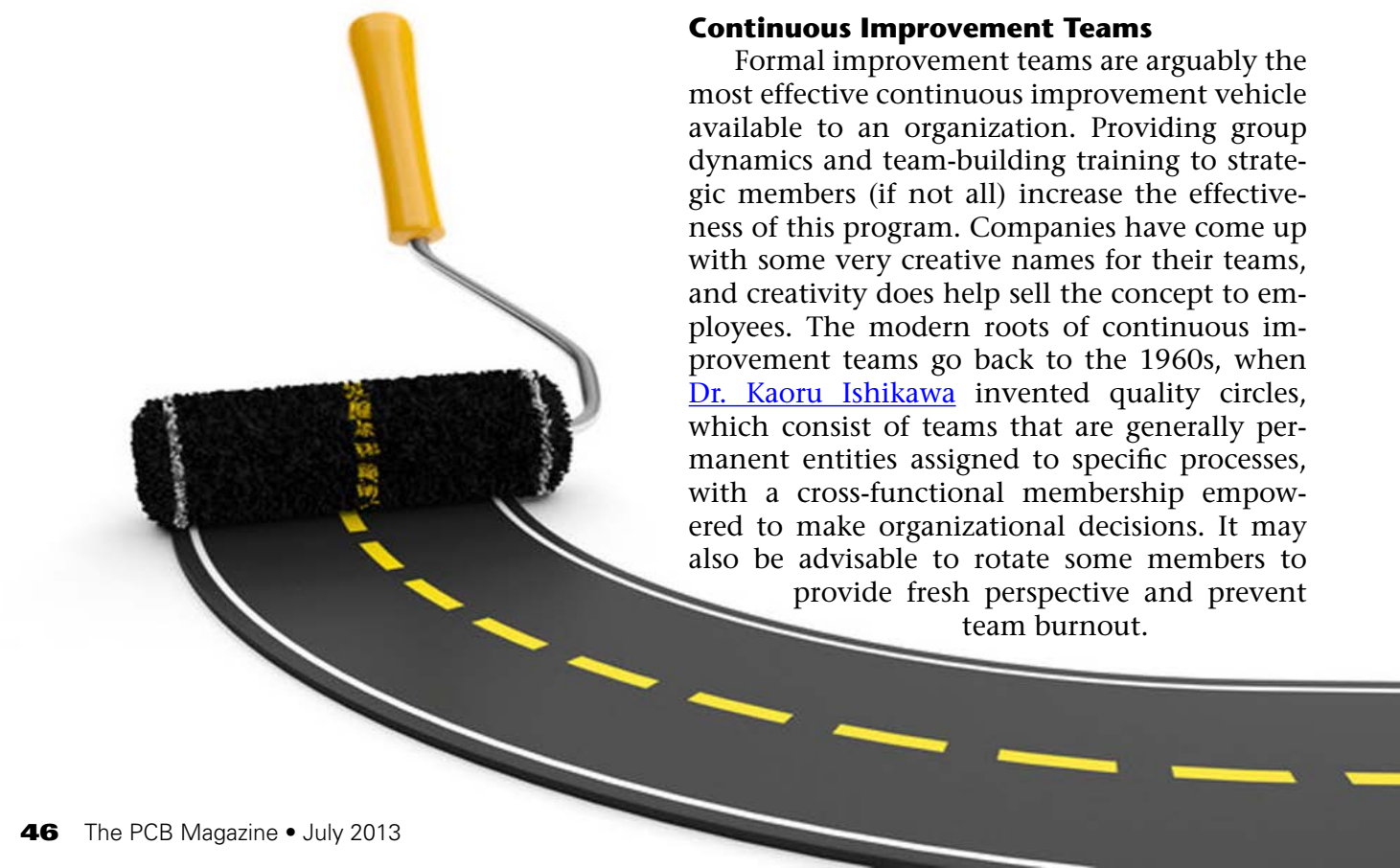
Continuous improvement is a journey, and as with most things worthwhile, needs to be an integral part of an organization's everyday life. It can only come from people, motivated and committed, learning what they can learn, solving problems that they can solve, and implementing solutions that they develop.

Definition

The venerable quality guru W. Edwards Deming defined continuous improvement simply as "improvement initiatives that increase successes and reduce failures." Sounds simple, right? In concept it is simple; it is the execution that requires perseverance. The need for continuous improvement is present in every industry, but mandatory in technology industries such as PCB manufacturing. Continuous improvement cannot be defined as putting together an ad-hoc group to put out a fire. Crisis management is not continuous improvement; crisis prevention is.

Philosophy

The underlying philosophy, which ensures the success and growth of an organization, is that every facet of the operation must continuously improve. This means that instead of having one specific objective that once met signals the end of progressive effort, employees at every level of responsibility must always strive to perform better next month, than last month. Such a never-ending plan defines excellence as continuous improvement. This philosophy must permeate the entire organization, not just manufacturing. Tremendous benefits can be achieved in the areas of customer service, sales and marketing, quality, and engineering, but are often overlooked in a continuous improvement program.



Continuous Improvement Teams

Formal improvement teams are arguably the most effective continuous improvement vehicle available to an organization. Providing group dynamics and team-building training to strategic members (if not all) increase the effectiveness of this program. Companies have come up with some very creative names for their teams, and creativity does help sell the concept to employees. The modern roots of continuous improvement teams go back to the 1960s, when Dr. Kaoru Ishikawa invented quality circles, which consist of teams that are generally permanent entities assigned to specific processes, with a cross-functional membership empowered to make organizational decisions. It may also be advisable to rotate some members to provide fresh perspective and prevent team burnout.

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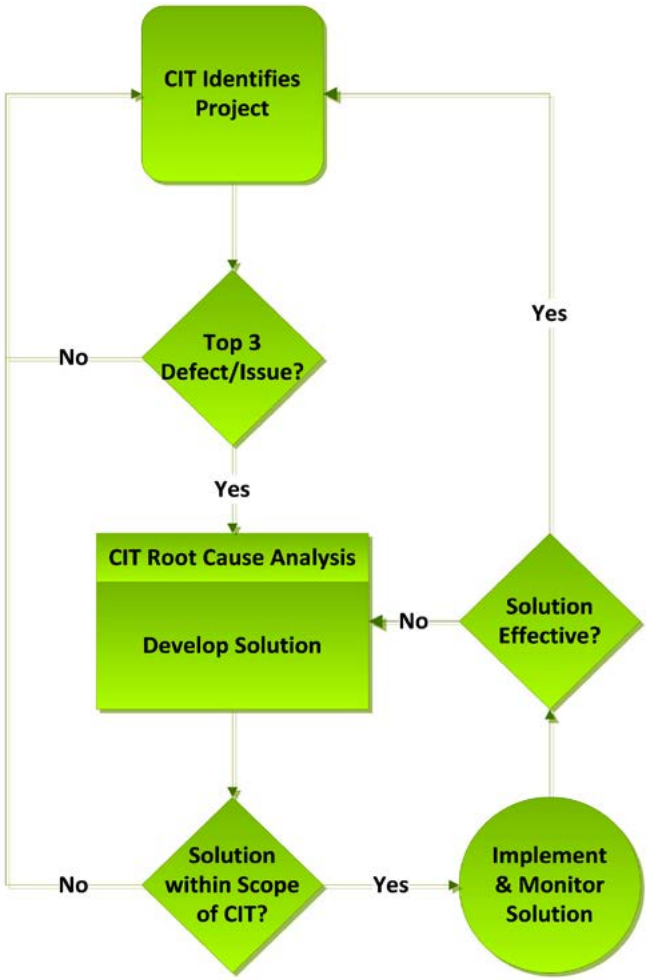

Figure 1: A typical continuous improvement team cyclic process flow.

Implementation

There should be no lack of available continuous improvement projects in the average PCB manufacturer. Developing a strategy for identifying the potential projects should be the first step in the process. Using defect data and Pareto analysis you can easily see where the largest dollar return can be gained in each functional manufacturing unit. Customer complaints, quoting accuracy, and customer (external and internal) surveys are good sources for identifying continuous improvement projects within support functions. Focusing on improving the top three issues within any one functional unit will achieve much higher return than trying to reduce the bottom 80% of the issues (the old reliable 80/20 rule).

Developing solutions that result in improvement can be expedited by utilizing tools such as failure mode effects analysis (FMEA), process control plans, SPC reports & process capability (CPK) data, and Gauge R & R Studies. Advanced problem-solving techniques such as group brainstorming, Ishikawa (fishbone) cause & effect diagrams, and design of experiments (DOE) are very effective in facilitating root cause analysis. Figure 1 shows a typical continuous improvement team cyclic process flow.

Customer Excellence

The term customer service is quickly being replaced in today's business environment with customer excellence. Arguably, all organizational activities revolve around satisfying the customer, and a continuous improvement program is a powerful vehicle to assure this result. If you break it down, all profits come from the customer, not from products and services. An argument could be made that a satisfied customer is just one that is not yet dissatisfied! Customer service is no guarantee of customer retention, but customer excellence is a differentiator. This must be a strategic initiative integrated into planning along with profitability, ROI, and market share. This is where a comprehensive continuous improvement program comes in. A continuous improvement program can minimize (if not eliminate) the performance detractors of waste, rework and lost time, while developing employees capable of capitalizing on today's opportunities and effectively meeting tomorrow's challenges.

I think it appropriate to end this column with a quote from Jim Hudon of Hudon Associates:

"If you think your operation is the best that it can be, you have opened the door to a competitor to outdo you." **PCB**

Steven Williams is the commodity manager for a large global EMS provider, and author of the book Survival Is Not Mandatory: 10 Things Every CEO Should Know About Lean.

To read past columns, or to contact Williams, click here.

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PCB007 Market News Highlights

Promising Future for U.S. Semiconductor Manufacturing Market

Six years ago, the outlook for U.S. semiconductor manufacturing was dim and dimmer. At the time, Intel was building their Dalian fab, AMD was ramping up their Dresden facilities, TI was transitioning to a fab-lite model, and the U.S.-based fabless giants were growing their business through foundries based in Asia.

Printed Electronics to Become Integral Part of Our Lives

CETEMMSA's study reveals that in 2020, printed electronics will become part of our lives with products like electronic skin, electronic human tissues and organs, or architectural urban elements which react to external stimuli. By 2030, we will have digital food and will regularly use aerospace commercial transport thanks to the use of printed electronics in different sectors. The printed electronics industry will reach EUR 60 billion turnover in 2020.

3D Printing Poised to Grow Across All Markets by 2025

3D printing has come of age, surpassing $1B in revenues during 2012 and with growth expected to continue across all target markets to 2025. Across the board, printer manufacturers are reporting a surge in sales, and some cannot meet demand as awareness of the technologies and what they offer grows.

Data Science to Impact Medicine More than Drugs

"In the next 10 years, data science will have more to do with improving medicine than anything you will ever learn in medical school or anything currently being researched in the laboratory," said Frost & Sullivan partner Reenita Das at the 12th International BIOtech Exhibition and Conference.

Global Mobile Memory Revenue Down 5.2% in Q1

According to DRAMeXchange, a division of global research firm TrendForce, total 4Q12 revenue for the mobile DRAM industry grew 21.4% from the third quarter and reached US $2.74 billion, boosted by climbing shipments of low to mid-end smartphones as well as seasonality. In the first quarter of 2013, however, revenue fell to US $2.6 billion, a quarterly decrease of 5.2%.

Indicators Suggest Weakening Business Activity

Manufacturing firms responding to the monthly Business Outlook Survey suggest that regional manufacturing activity weakened this month. All of the survey's broadest current indicators were negative this month, indicating weaker conditions compared with April.

Global Automotive Electronics Market to Reach $314.4B by 2020

The global market for automotive electronics, estimated at US $191.3 billion in 2013 and forecast to be US $204.6 billion in 2014, is further projected to reach US $314.4 billion by 2020, thereby maintaining a CAGR of 7.3% between 2012 and 2020.

Global Semiconductors Sales Hit $23.62B in April

The Semiconductor Industry Association has announced that worldwide sales of semiconductors reached $23.62 billion for the month of April 2013, a 0.6% increase from the previous month when sales were $23.48 billion, but down slightly from the April 2012 total of 24.06 billion.

Digital X-ray Market to Hit $4.82 Billion in 2018

The digital X-ray market is driven by technological advances in automation, growing numbers of elderly people, and need for improved and faster imaging methods. The growing incidence of chronic disease like tuberculosis, pneumonia, and other gastrointestinal disorders are propelling the market in both developed and developing countries.

DRAM Industry to Witness Steady Growth in 2014

According to TrendForce, a global market research firm, PC DRAM prices have shown noticeable signs of rebounding in 2013, following two years of financial losses and declining output value. The prices of mainstream products like 4GB modules rose by nearly 60%, which helped to ease the declining ASP of both server and mobile DRAM.

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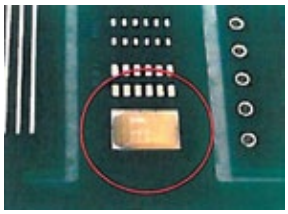
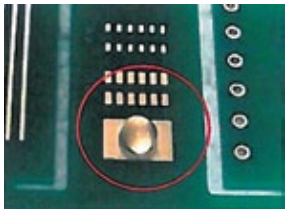


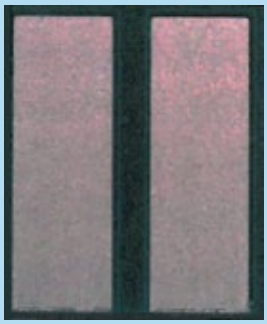
Without Post Dip



With Post Dip

Microscope Images

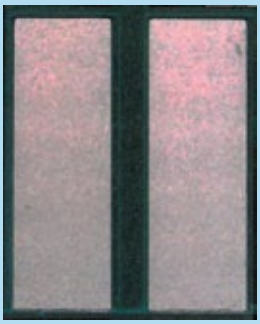
Fresh Deposit



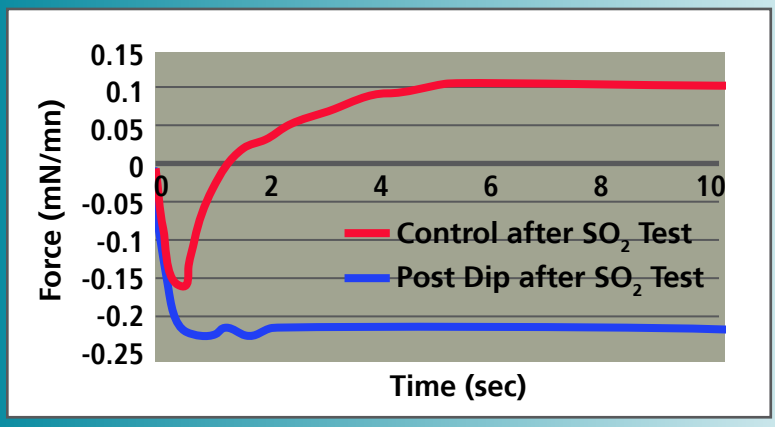
Control Deposit after SO_2

Some discoloration but no severe corrosion

Post Dip Treated after SO_2



No discoloration



Wetting Balance Curves of Deposit after SO_2 Test

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PTH Voids: Getting to the Root Cause, Part 2

by Michael Carano
OMG ELECTRONIC CHEMICALS

Introduction

While there are many causes for PTH voids, one should also consider poor drilling practices, multilayer lamination issues and the fact that higher performance resin materials are more difficult to desmear, all of which can lead to voids.

In Part 1 of this series, I approached the subject of PTH voids at the root cause as attributable to the difficulty of desmearing the more chemically resistant, high-performance laminate materials. In addition to the greater chemical resistance, these materials also present challenges with respect to drill debris that can lodge in the hole wall, and multilayer lamination challenges.

Debris

Debris remaining in the hole may become loosened later in the fabrication process, leading to a void within the via (Figure 1). Debris is typically caused by poor evacuation of drill chip particles. The vacuum on the drill machine is designed to remove debris from the through holes. Obviously, if the vacuum is insufficient, it is not uncommon for debris to remain. Proper selection of drilling feeds and speeds, drill retraction rates and sufficient vacuum will ensure reasonably clean vias.

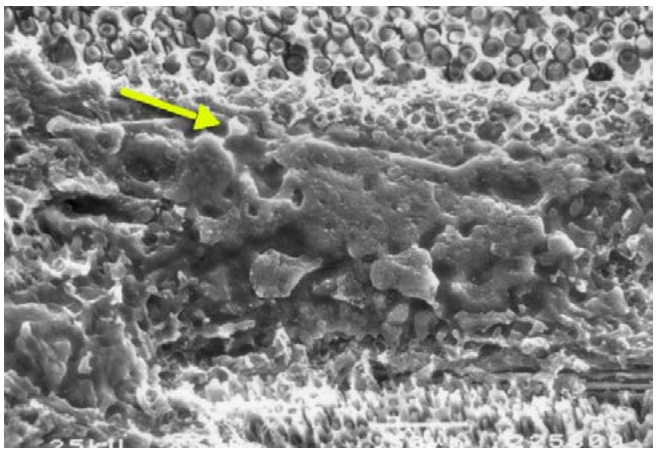

Figure 1: The arrow is pointing to debris remaining on the hole wall. Presence of debris may lead to voids.

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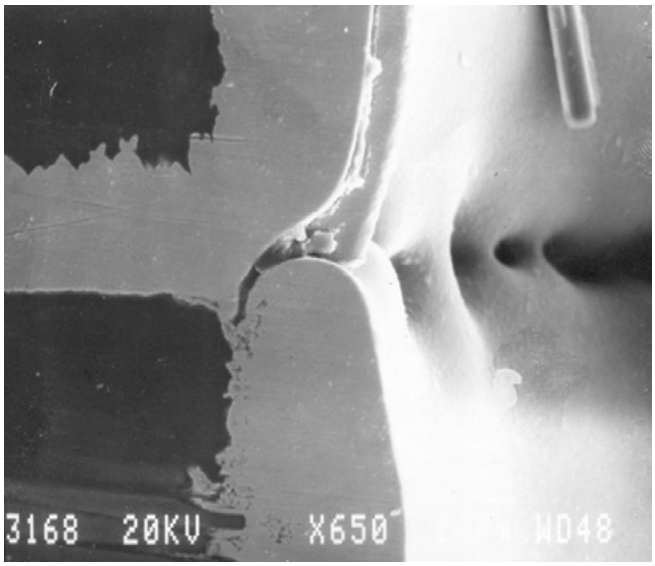

Figure 2: Example of wedge void after plating. (Photo courtesy of Dr. Karl Dietz, Dupont)

Multilayer Lamination

Poor resin flow and B-stage wedging create recesses and blind areas in the plated through hole. When this type of defect is created, it is very difficult to catalyze the recessed areas and ensure electroless copper deposition.

Obviously, there are a number of possibilities leading to this type of defect. First, one should note that although it is not exclusive, the wedge originates at the B-stage side. The mechanism of the "wedge void" formation discussed below will illustrate the significance of the defect and the genesis of a plating void.

One often overlooked cause of wedge voids is the drilling operation. During the drilling operation, vibration of the drill bit can create microfractures in the copper/dielectric interface. Of course, dull drill bits, excessive chip loads, extremely high heat generation during drilling and poor quality entry and back-up material will increase the likelihood of a wedge void. Figure 3 shows an extreme example of a wedge void caused mainly by poor drilling practice. See evidence of gouging in the hole wall and turn-out glass bundles. This type of drilling will generate significant heat, leading to the opening of the interface between the B-stage and the copper.

After drilling, the printed wiring board is subjected to a desmear process. During this process, a number of chemicals act on the PWB resin material. Solvent conditioners can get absorbed into the microgaps between the copper and the dielectric. Subsequent treatment with permanganate solution will oxidize (i.e., remove this already swelled resin, creating a wedge). Certainly, the overaggressive conditions in an alkaline permanganate desmear process (such as high caustic content and high temperature) will exaggerate the wedge opening. Once the electroless copper process is underway, various chemical steps further work to widen the gap.

For example, the microetch solution will attack the copper and widen the gap. Pre-dip and activator solutions typically are fairly concentrated hydrochloric acid-based solutions, which will further remove the copper treatment on the innerlayer. If electroless copper fails to completely seal the wedge, the chemical attack will continue when the article is immersed in acid cleaner, microetch solution, acid dip and acid copper. When the wedge is relatively small, acid copper will completely fill the gap resulting in typical "pink ring" appearance. If the gap is large enough, it may bridge only partially or

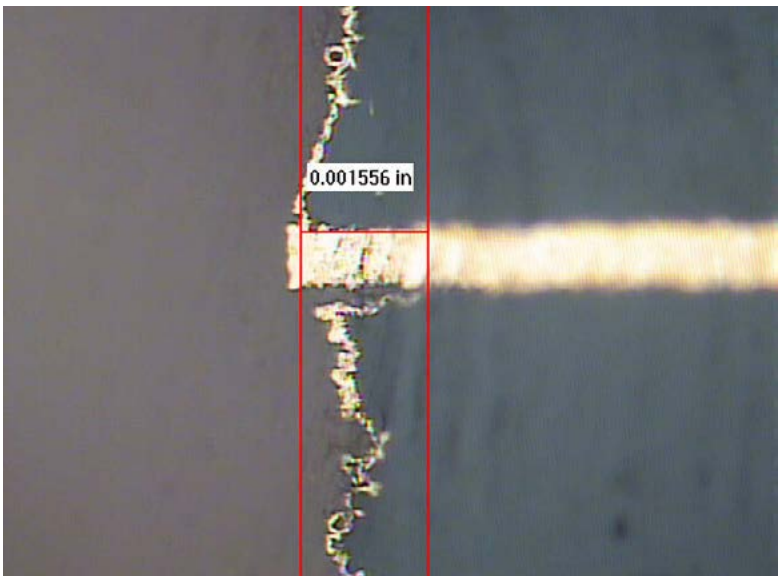

Figure 3: Wedge opening, which can lead to plating folds or voiding.

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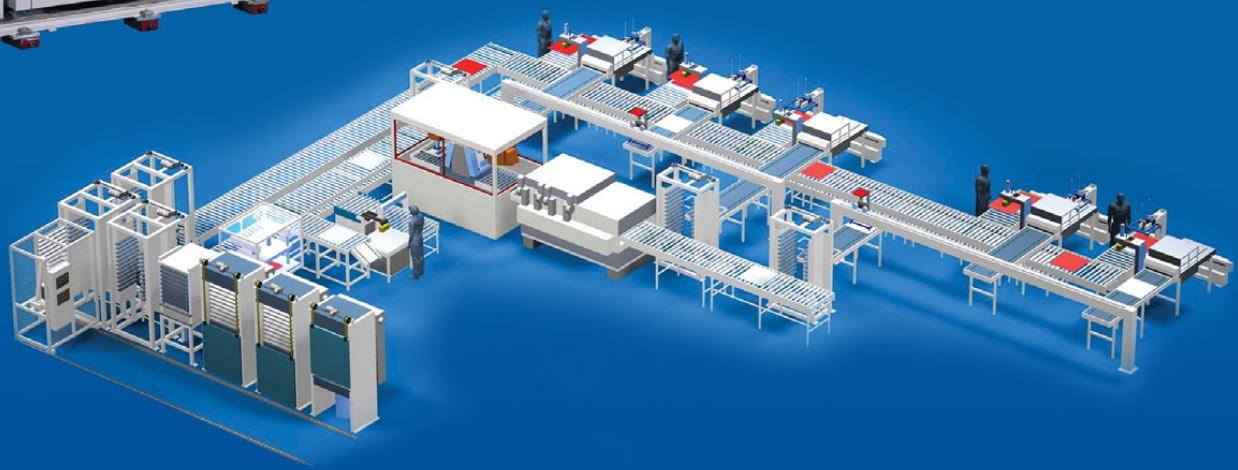

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may not bridge at all, leading to a wedge void defect. In the most severe cases, the plated copper "folds over," maintaining a voided area in the wedge.

The above notwithstanding, a need still exists for an improved method of enhancing the copper to dielectric bond in MLBs, while at the same time providing enhanced chemical resistance. Poor multilayer bonding practice leads to less than optimum resin flow and encapsulation. In turn, these effects lead to a weakened bond. Essentially, any weakening of that bond potentially leads to the formation of a wedge. While lamination best practices are a must, at the very least should include:

- Monitoring the rate of heat rise in the multilayer stack
- Moisture removal prebakes of innerlayer treated copper prior to lamination
- Dual stage (kiss cycle) and vacuum lamination to ensure most even resin flow

As a final word on multilayer PWB fabrication, the manufacturer must implement (if it's not in place at the time) a reduced oxide or an alternative oxide innerlayer treatment process. Both a reduced oxide process and an alternative oxide enhance the bond strength between the prepreg resin and the copper. In addition, the treated foil, if exposed by the wedge, is better able to stave off dissolution from the many acidic process steps the PWB will be subjected to. **PCB**

Michael Carano is with OMG Electronic Chemicals, a developer and provider of processes and materials for the electronics industry supply chain. To view past columns or contact the columnist, click here.

VIDEO INTERVIEW

The Future of PE: Assuming the Shape of 3D

by Real Time with...IPC APEX EXPO 2013

Ken Church enthusiastically speaks about the future of electronics, specifically 3D printed electronics. Using the example of a UAV with active printed 3D electronics built right into the shape of the wing, or a table the shape of a computer, Church even predicts a melding of the PCB industry to printed electronics.

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Mil/Aero007 News Highlights

Invotec Achieves Nadcap Merit Status at Tamworth Facility

Invotec Group announces that its Tamworth Facility has been awarded Nadcap Merit status for electronics, covering rigid, flex-rigid, and HDI products. Nadcap recognises the facility for its superior performance and commitment to continual improvement in aerospace quality.

New Sales Team to Market Lazer-Tech's Defense PCBs

Jamie Armitage, president and owner of Lazer-Tech, said, "Selling in the high-tech and defense areas requires having sales professionals like Jim Hyde and his team to represent our company. I am extremely confident that Jim and his team will take us to the next level as we continue to focus on the quick-turn market as well as the military and defense sectors."

ZESTRON Renews ITAR Registration

ZESTRON, the globally leading provider of high-precision cleaning products, services, and training solutions, is pleased to announce its renewal of the International Traffic in Arms Regulations (ITAR) registration with the U.S. Department of State, Directorate of Defense Trade Controls.

Tin Whiskers Focus of Papers Sought by IPC, CALCE

IPC and CALCE (University of Maryland) have issued a call for papers for the 7th International Symposium on tin whiskers. Sponsored by Lockheed Martin, the symposium will take place November 12–13, 2013. Expert presentations are sought on the full range of tin whiskers theory and practice in every market sector.

Multilayer Technology Achieves 2013 Best of Irving Award

For the fifth consecutive year, the company was selected for the 2013 Best of Irving Award in the printed circuit boards category by the U.S. Commerce Association. The award program recognizes outstanding local businesses throughout the country.

Cofan Secures UL Listing for Aismalibar/Cobritherm

Cofan has received its UL listing for Aismalibar/Cobritherm thermally conductive IMS/prepreg. The company is now certified to use the UL stamp on Aismalibar's Cobritherm Alcup-G, Alcup, and HTC materials.

Microtek Names Shepherd VP of Operations

Microtek Laboratories, an independent test laboratory, has announced the promotion of Russ Shepherd to the position of vice president of operations. Shepherd has worked for the company for more than 25 years and has been an integral part of its growth and success since first being hired in 1987.

Ground Robot Market to Reach $12.0 Billion by 2019

Military ground robot market growth comes from the device marketing experts inventing a new role as technology poised to be effective at the forefront of fighting terrorism. Markets at $4.5 billion in 2013 are expected to reach $12.0 billion by 2019.

Global Military Radar Systems Market to Hit $8.6B in 2013

In 2013, the global military radar systems market is evaluated at nearly US $8.6 billion. Developed countries lead the overall market in terms of radar technological developments.

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The Impact of Soldermask Processing on ENIG/ENEPIG Deposit Quality

by George Milad
UYEMURA

Soldermask (SM) is a permanent insulating coating designed to protect the printed circuit board. The mask creates a barrier to contamination, corrosion and handling defects, and it also prevents solder bridging during assembly. The most common type in use today is a liquid photoimageable soldermask (LPISM). The successful application of SM involves multiple processing steps; following vendor recommendations and proper process control could preclude many problems downstream.

The ENIG/ENEPIG deposition also involves multiple processing steps that require the same attention to detail. For best results and the highest solder joint reliability, the product coming to the ENIG/ENEPIG line must have uncontaminated clean copper on which to plate, with perfectly defined and cured SM.

LPISM processing involves the following process steps:

- Surface pre-treatment
- Application of LIPSM to PCB.
- Evaporation of solvent (tack dry)
- UV photo exposure (imaging)
- Development of exposed board
- Thermal final cure

Process control of the different steps involved in SM applications is paramount to the success of the ENIG/ENEPIG deposit. Out-of-control processing could lead to skip plating, and/or nickel corrosion; the former results in failure to deliver the desired nickel thickness and the later leads to problems with soldering and solder joint reliability.

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The following is a discussion of each process step and its impact on the quality of the ENIG/ENEPIG deposit.

Surface Treatment

Surface treatment removes surface contaminants like grease and oxidization and roughens the PCB surface for physical adhesion (anchoring effect) between solder mask coating and copper. Excessive roughening of the copper surface will produce great adhesion, but it will also produce a rough electroless nickel (EN) deposit, which is prone to corrosion during the immersion gold deposition step. Insufficient roughening in the pre-treatment surface preparation could lead to poor adhesion and may cause chemical seepage/entrapment under the mask during the ENIG of ENEPIG processing.

Coating/Application

There are three common methods of application or coating the soldermask, namely screen printing, curtain coating and spraying. The methods vary in their efficiency to fill a through-hole where one is needed.

Partial filled vias or through-holes is a coating defect that causes skip plating of the electroless nickel (EN) deposition. Small partial filled vias are not replenished with the depositing metal at the same rate as more accessible surfaces. This gives rise to a galvanic reaction between two dissimilar solutions. The pads connected to the partially plugged vias carry a charge that does not allow the activator (immersion Pd) reaction to proceed. The pad remains none activated and the EN deposition will not initiate, giving rise to skip plating.

Tack Dry

Tack drying removes solvent from the coating. Vendor recommendation of temperature and time must be followed closely. Inadequate tack drying will result in the mask sticking to the artwork film and weak UV polymerization, giving rise to poor image resolution, which, in turn, could lead to a positive foot defect. Excessive tack drying could lead to the loss of the ability to develop non-cross-linked monomers.

Exposure/Imaging

Positive and negative foot are defects associated with the side wall of the soldermask. Both defects could play havoc with the ENIG or ENEPIG deposition if they are associated with soldermask defined pads. Insufficient exposure gives rise to negative foot. The foot creates a crevice at the mask and pad interface that creates a galvanic cell, giving rise to corrosion of the copper at the interface. This defect is more prevalent with dark or black soldermask.

> ***Overexposure or lack of intimate contact between the film and the mask creates a positive foot. This foot behaves like a contaminant at the edges of the SM defined pad, producing a compromised EN deposit, that is susceptible to corrosion at the edges of the pad, and causes solderjoint reliability issues.***

Overexposure or lack of intimate contact between the film and the mask creates a positive foot. This foot behaves like a contaminant at the edges of the SM defined pad, producing a compromised EN deposit, that is susceptible to corrosion at the edges of the pad, and causes solderjoint reliability issues.

Shortage in UV energy and vacuum level may cause poor imaging and resolution, resulting in weak polymerization. Incomplete polymerization will allow the leaching of sulfur-bearing materials (natural components of the mask) into the hot electroless nickel bath during the extended dwell time for thickness build up of the nickel deposit. Higher sulfur contamination in the EN deposit will reduce the percent of phosphorous as well as the corrosion resistance of the deposit. Corroded nickel will lead to a compromised solder joint.

Development

In the developer, the non-polymerized monomers are emulsified into the develop-

ing solution. Good rinsing after developing is a must to ensure that none of these emulsified entities remain on the copper surface. Residues on the copper surface will become adherent in the drying step and would be further baked in the thermal curing step, making it difficult to remove in the ENIG/ENEPIG pre-treatment process.

The presence of SM residues leads to non-uniform/incomplete Pd activation on the copper surface, and this in turn leads to patchy EN initiation of deposition, resulting in rough and uneven nickel morphology. Rough morphology with crevices is the primary site for the beginning of corrosion during the immersion gold deposition.

Thermal Curing

Thermal curing is the last, critical step in SM processing, as it completes the cross-linking or polymerization of the mask. A well cured mask becomes hard and chemical resistant and not susceptible to leaching in the EN bath. Leaching in the EN bath produces a compromised nickel deposit and significantly shortens the useful life of the bath.

Understanding the complexity and the interdependency of the two processes, soldermask coating and ENIG/ENEPIG surface finishing, can help manufacturers stay clear of problems that adversely affect the final finish and lead to soldering defects that could compromise the reliability of the solder joint. **PCB**

George Milad is the national accounts manager for technology at Uyemura International Corporation. Milad is current chair of the IPC Plating Committee and a permanent member of the Technical Activities Executive Committee of IPC. Contact Milad at gmilad@uyemura.com.

What is the DAM Problem with Scheduling?

by Gray McQuarrie
Grayrock & Associates

"Never tell people how to do things. Tell them what to do, and they will surprise you with their ingenuity."
~General George S. Patton

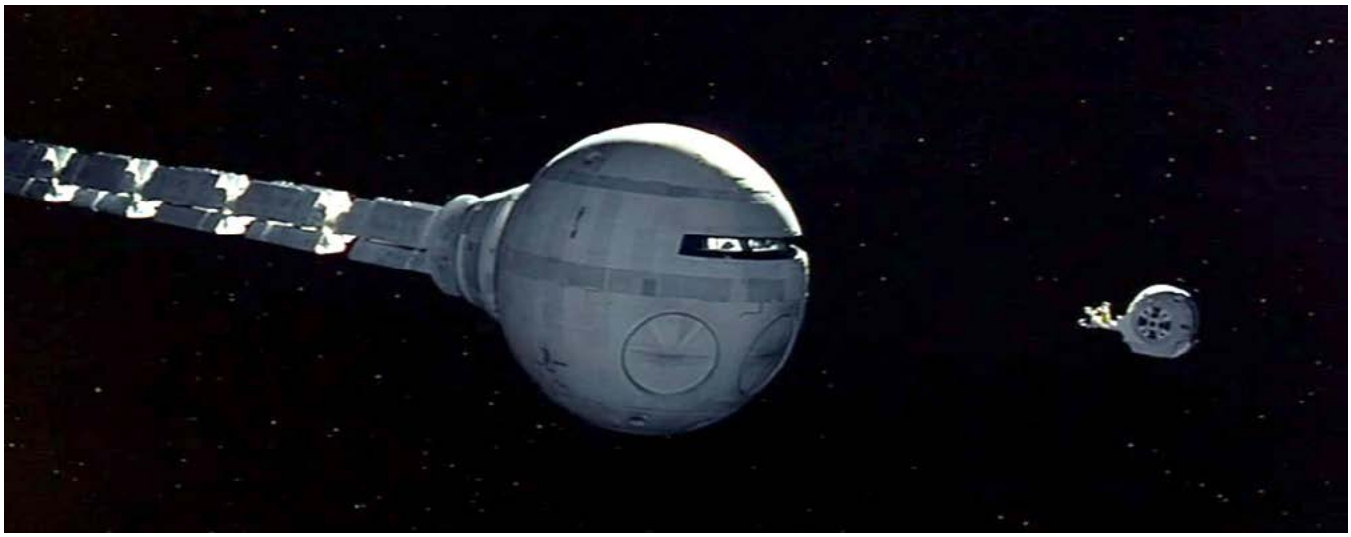
My good friend, retired U.S. Army Colonel Carl Schott, was once the commander in charge of the units that would have deployed tactical nuclear weapons if Russian tanks had ventured into West Germany. He once told me, "The very best plan never survives the first bullet." Part of his background was flying helicopters in Vietnam where, in one type of mission, he flew at night to draw North Vietnamese fire so that the gunships above him could identify the enemy and kill them.

Just like you, Carl had to deal with immediate reality. Rarely did anything go according to plan. Just as with the fog of war, in the fog of production, trying to figure out what is happening with the customer orders can be, at best, frustrating. We often find our master schedule is hardly that! It can cause any one of us to say, "What is the DAM problem with scheduling?"

Before I answer this question, I want to go off on one of my tangents. Recently, I was having morning coffee with Carl at Starbucks. He told me the German commanders told him that in World War II, they were extremely frustrated with the American infantry. For example, it was almost impossible to force the Americans into a defensive position and keep them there. The Americans were always improvising and deviating from the plan. The Germans couldn't predict how the Americans would respond in a given battle. If the Germans tried to deviate from their master plan, which often came from Hitler, they could get shot. The battle for Stalingrad exemplified the German war machine's rigidity to the plan and its inability to improvise.

What does this have to do with our master schedule and how we dispatch jobs in the shop? Production enterprise-level intelligent software systems, which tell us how material is to move on the factory floor, can create a rigidity that has the potential to sink us. I like to refer to these systems as HAL, the master computer system that controlled everything on the mothership in, "2001: A Space Odyssey." We are not to question HAL; we are simply to follow his orders: HAL, open the pod bay doors.

Let me illustrate why scheduling is so hard. In fact, in technical terms, scheduling is an NP-hard problem.



2001: A Space Odyssey, Metro-Goldwyn-Mayer 1968

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First, there is a factorial relationship that appears simple. For a plant with a single machine and three jobs you would have 3! (3 factorial = 3 x 2 x 1 = 6) possible jobs sequenced such as 1, 2, 3 or 3, 1, 2, and so forth. How would you determine which sequence or schedule is best? It's rather easy in this case. For example, if job 1 were due first, job 3 next, and job 2 last, then with an earliest due date rule we have 1, 3, 2. If jobs 1 and 2 were volume orders and no setup was required going from job 1 to job 2 (or vice versa) and they were due much earlier than job 3, well, it's looking like job 3 should be last. In addition, if job 3 had a very long complicated setup going from either job 1 or job 2 and it was a small volume order, then the optimum schedule has to be 1, 2, 3 or 2, 1, 3. Simple logic. No need for HAL.

Record #	M1 Time (min)	M2 Time (min)	Order	End Time (min)
1	1.00	20.00	1	21.00
2	2.00	19.00	2	40.00
3	3.00	18.00	3	58.00
4	4.00	17.00	4	75.00
5	5.00	16.00	5	91.00
6	6.00	15.00	6	106.00
7	7.00	14.00	7	120.00
8	8.00	13.00	8	133.00
9	9.00	12.00	9	145.00
10	10.00	11.00	10	156.00
11	11.00	10.00	11	166.00
12	12.00	9.00	12	175.00
13	13.00	8.00	13	183.00
14	14.00	7.00	14	190.00
15	15.00	6.00	15	196.00
16	16.00	5.00	16	201.00
17	17.00	4.00	17	205.00
18	18.00	3.00	18	208.00
19	19.00	2.00	19	210.00
20	20.00	1.00	20	211.00

Table 1: Best case for start order for the model in Figure 1. The order column is the order the jobs are to be run. The "EndTime" is the time each job was completed. Note: Every job requires a total of 21 hours of production time. Record 20 shows the last job was completed after 211 hours.

But what happens to this problem with modest increases in size? Factory Physics, by Hopp and Spearman, provides a discussion on this subject in their chapter "Production Scheduling." For example, they illustrate the 10 x 10 problem popular in operations research: finding the optimum schedule for 10 jobs with 10 machines. Just for fun, write down as many different production schedules as you think are possible. For example, is a billion too many or too few? Through just one machine you would have 10! (10 x 9 x 8 x 7 … x 1) or more than 3.6 billion scheduling possibilities. To get the number of possibilities for all 10 machines it is 10! x 10! x 10! x … 10 times. This is approximately 4×10^{65} possible production schedules, which far exceeds the number of atoms on Earth! This takes many hours of computer time to solve. Since many U.S. plants are large, quick-turn shops dealing with hundreds of jobs running

Record #	M1 Time (min)	M2 Time (min)	Order	End Time (min)
1	1.00	20.00	17	231.00
2	2.00	19.00	19	266.00
3	3.00	18.00	9	136.00
4	4.00	17.00	10	153.00
5	5.00	16.00	18	247.00
6	6.00	15.00	2	39.00
7	7.00	14.00	13	189.00
8	8.00	13.00	3	52.00
9	9.00	12.00	12	175.00
10	10.00	11.00	16	211.00
11	11.00	10.00	11	163.00
12	12.00	9.00	20	275.00
13	13.00	8.00	7	103.00
14	14.00	7.00	15	200.00
15	15.00	6.00	6	88.00
16	16.00	5.00	5	72.00
17	17.00	4.00	14	193.00
18	18.00	3.00	1	21.00
19	19.00	2.00	4	54.00
20	20.00	1.00	8	116.00

Table 2: Random case. Note the jumbled run order. Record 12 shows the last job was completed after 275 hours.

through easily 10 or more machines, finding the optimum schedule could take HAL 70 or more years to figure out even if he could process 1 billion scheduling scenarios a second! In other words, "I am sorry Dave. I can't do that."

What can we mere humans do? Table 1 shows 20 jobs and their process times for two machines, M1 and M2. Notice that the total time to make any one job is always 21 hours. How many scheduling possibilities are there? Well 20! x 20!, or about 6 x 10^{36}. How can we figure out the best solution within the next minute or so? I put together a simple discrete event model to help us (Figure 1). Notice that either machine 1 or machine 2 could be a bottleneck, depending on what job is being run. You don't want machine 2 to be idle for long, so you might run the short job first on machine 1 so machine 2 gets going instead of sitting idle.

Does it matter in what order the jobs are released? Well, if we run the jobs in random order (Table 2), it took 275 hours. If we run the jobs starting with the fastest jobs in machine 1 first, and work our way down the list, then we have minimized the total process time, which is 211 hours (Table 1). If we reverse this order we get 320 hours (Table 3). So the answer is yes; the order in which the jobs are released does matter! Minimizing the makespan (total time it takes to complete all jobs) on two machines is called Johnson's rule. Unfortunately, as we add machines, it blows up into an NP-hard problem again.

Record #	M1 Time (min)	M2 Time (min)	Order	End Time (min)
1	1.00	20.00	20	320.00
2	2.00	19.00	19	300.00
3	3.00	18.00	18	281.00
4	4.00	17.00	17	263.00
5	5.00	16.00	16	245.00
6	6.00	15.00	15	230.00
7	7.00	14.00	14	215.00
8	8.00	13.00	13	201.00
9	9.00	12.00	12	188.00
10	10.00	11.00	11	176.00
11	11.00	10.00	10	165.00
12	12.00	9.00	9	153.00
13	13.00	8.00	8	140.00
14	14.00	7.00	7	126.00
15	15.00	6.00	6	111.00
16	16.00	5.00	5	95.00
17	17.00	4.00	4	78.00
18	18.00	3.00	3	60.00
19	19.00	2.00	2	41.00
20	20.00	1.00	1	21.00

Table 3: Worst case. Record 1 shows the last job was completed after 320 hours.

An obvious take-away is this: When you are confronted with a bottleneck, get the fast jobs out upstream to feed it first. When the bottleneck is running, start producing the jobs that take longer in the upstream operations. Of course, always pay attention to promised due dates. By doing this, you have reduced the number of machines to consider in your plant. And you have reduced the number of possible schedules to look at. In this way you have reduced the hard problem into a much simpler one. After all, we should be able to manually open the pod bay door.

Some years ago I walked into a PCB facility that was making very complex HDI product, but wasn't making any money. By focusing on constraining the WIP (CONWIP), identifying and focusing on the production bottlenecks to help develop a scheduling paradigm, working side by side with the operators to devise their own rules for dispatching jobs, and implementing a production pull system using Kanbans, profitability soared, WIP was reduced by two-thirds, and the standard production lead time decreased from 15 to four days with one-day quick-turns.

Let me run through some highlights.

I found three primary constraints: 1) lamination, 2) laser drill, and 3) electrical test. For a variety of reasons, the upstream constraint, lamination, was chosen as the primary constraint that would dictate the heart beat: the takt time for the factory. It was also used to determine the production batch size, the number of jobs to be started at once, and the frequency for production starts. Within each production release a set allocation for quickturns was also established. What this made clear to everyone in the plant was there was a finite capacity.

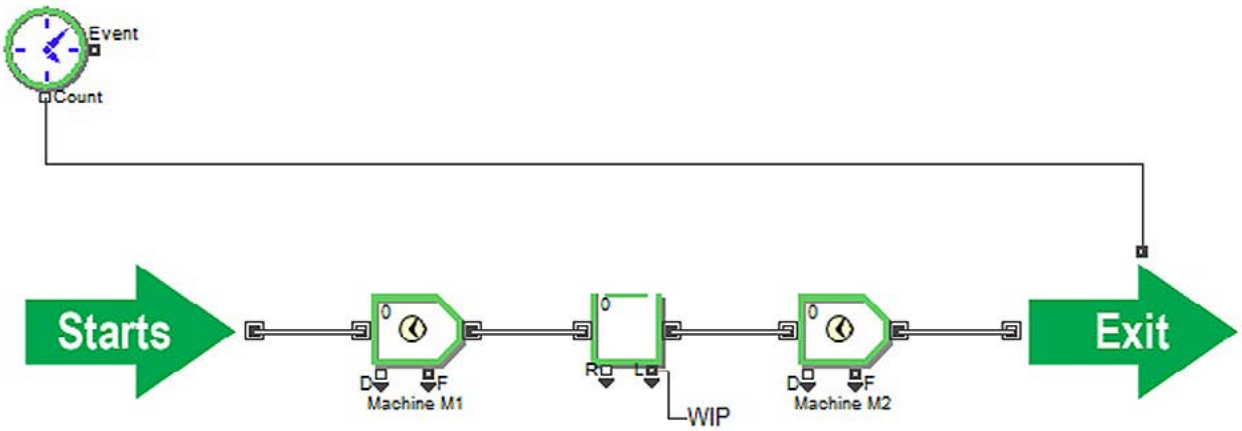

Figure 1: The Simple Discrete Event model. Tables 1, 2, and 3 show different sequences of jobs that come out of the "Starts" arrow, which have different processing times for M1 and M2. Note if the process time for M2 is long then it will be a bottleneck. Similarly if an M1 job is long, M2 will be waiting for work. How do we derive the best order or scheduling sequence? What will the WIP do between M1 and M2?

Overall profitability would be determined by how this capacity was managed. For example, if the quick-turn allocation wasn't full, everyone in the plant would know and begin to ask questions. This simple transparent scheduling system got everyone involved. Everyone understood what had to happen on a daily basis.

In order to manage the WIP level, the operators and supervisors created a Kanban system during their Kaizen. They created shelves to differentiate between sub-assemblies and repetitive processing. They created colored tags to go with the traveler to signify visually which jobs were due first. In order to figure out how to dispatch work from the Kanbans, they figured out ways the three bottlenecks would not starve. For the press area this meant organizing all material required for layup to be ready. The team was rather ingenious in how they organized this and made it work. Since most panels from the lamination department fed the laser drill department, the operators and leads, on their own, discovered that running the jobs with short lamination cycles at the beginning of the shift and abiding by the due dates was best.

I visit many factories that use computer dispatch, and I always find the operators have great ideas for improving the plant's flow, many of which are consistent with operations research theories even though they never had a class. Yet, despite their intelligent ideas, their voices weren't heard. Everyone must follow the computer dispatch list. Often when I look at the dispatch, I see jobs that have sat on the floor for 50 to 100 days or more! How can such a thing happen? It happens when you pay your employees not to think.

Months after the Kanbans were setup, I walked over to the press area where the WIP between lamination and laser drill was too high and violated the Kanban rule. I said to the lead, "Good grief, what are you doing?" The lead waved his hands as if he was a magician pretending to make it all disappear. Then he turned to me and said, "Don't worry about it."

He understood what was going on, and I did not. Let me explain. Figure 2 shows how the WIP changes for Table 2—the random case. Figure 3 shows how the WIP changes for the best case. Note that the maximum WIP for the best case, which got all of the jobs done the quickest, had 2x more WIP than the random case! Moreover, if the WIP between M1 and M2 is constrained to two units (Figure 4 shows the WIP result), then the time to make all of the jobs is much longer: 278 hours versus 211 hours. Not only that, the average cycle time was longer too: 153.5 hours versus 144.5 hours. This is an example where more WIP, not less WIP, makes the products move quicker! Why? Because we

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- Security and psychological issues in medical devices
- Miniaturized electronic packaging for wearable health monitors
- Wireless communication/solid state batteries in miniature implantable medical devices
- Designing more reliable medical products
- "Fantastic Voyage" meets medical device design

KEYNOTES

Sam Bierstock, M.D.

Day One Keynote

MEMS Technology and the Healthcare Industry: The Convergence of Timelines and the Perfect Storm

Sam Bierstock, M.D., BSEE Physician, Electrical Engineer, Medical Informaticist, Founder of Champions in Healthcare

Dr. Bierstock is a nationally recognized authority on healthcare and healthcare information technology. He is the Recipient of the George Washington Honor Medal, Freedoms Foundation for his work on behalf of our nation's veterans. ◆

Karthik Vasanth, Ph.D.

Day Two Keynote

Creating Solutions for Health Through Technology Innovation

Karthik Vasanth, Ph.D. General Manager, Medical and High Reliability Business Unit Texas Instruments

Karthik Vasanth received his Ph.D degree in Electrical Engineering from Princeton University in 1995. He joined the Silicon Technology Development group at Texas Instruments in 1995. In 2010 he became the General Manager of the Medical and High Reliability Business Unit at TI. ◆

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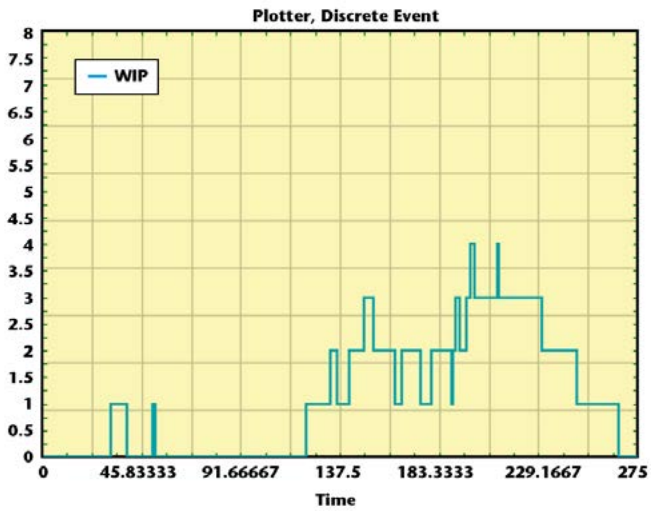

Figure 2: The WIP for the random case, which shows how WIP changed over the course of the jobs being run in random order (Table 2).

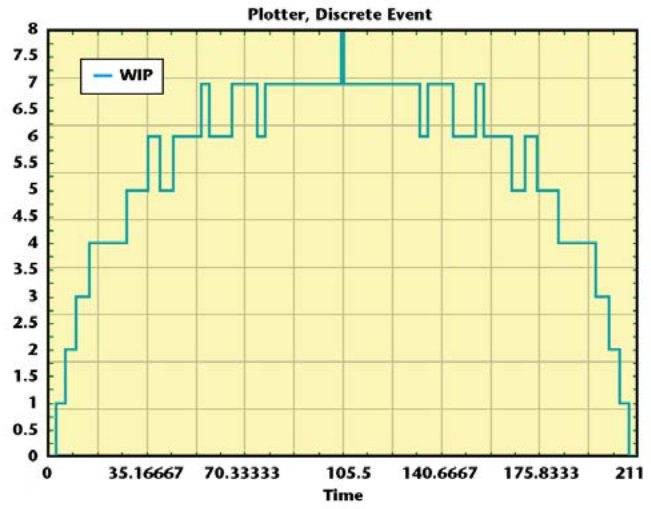

Figure 3: The WIP for the best case.

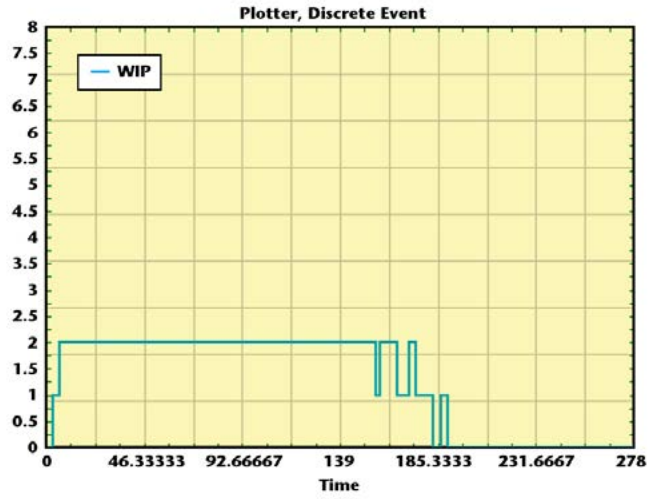

Figure 4: The constrained WIP case.

are dealing with jobs that have varying process times between two machines. Constraining the WIP causes blocking of machine 1, and as jobs cycle through in their sequence, eventually machine 2 will be starved. The leads and operators saw this, so they let the WIP and inventory float unconstrained; in this way they saw that both areas would always be producing.

How do you get everyone on the same page so this is understood? You won't do it with a spreadsheet. The only way you can see this type of dynamic behavior, without spending hours working on the plant floor, is building a simple model like the one in Figure 1. In this way, HAL serves us instead of the other way around. In this way HAL makes us all much smarter.

Figure 3 shows the relatively large amount of WIP that had the jobs going through the fastest with the shortest average cycle time when they were sequenced with the best case scenario (Table 1). This violates what we have come to understand about a low amount of WIP improving cycle time.

Figure 4 shows the WIP constrained to a maximum of two items, which if the jobs had the same process times, should be enough to keep both machines going. But this isn't the case. This produced a much worse result, though in Lean thinking and single piece flow thinking, this should have provided the best case and fastest cycle time, particularly in a scenario where only one item can be processed at a time. **PCB**

Gray McQuarrie is president of Grayrock & Associates, a team of experts dedicated to building collaborative team environments that make companies maximally effective. To read past columns, or to contact McQuarrie, click here.

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TOP TEN

PCB007 News Highlights This Month

① AT&S to Close PCB Plant in Austria

In light of the continued decline in the market for the technology used in single-sided PCBs and a lack of options for utilising available capacity, AT&S Austria Technologie & Systemtechnik Aktiengesellschaft has made the decision to close its production facility in Klagenfurt at the end of 2013.

② New Etching Tech Could Revolutionize PCB Fabrication

The growing functional range of smartphones, digital cameras, and tablets requires a high level of integration density in the semiconductor field and the miniaturization of electronic modules. Until now, the use of faster microchips was virtually impossible due to increased heat generation.

③ FastPrint Completes Acquisition of eXception's PCB Business

Mark O'Connor, CEO of eXception Group Ltd. commented, "This successful conclusion comes after a period of due diligence where all areas of the eXception business continued to work diligently and successfully toward its end-of-year goals…"

④ Sumitomo Begins Mass Production of New Type FPCs

Sumitomo Electric has developed a new flexible printed circuit with circuit layers connected by conductive paste based on the company's original metal nanoparticle technology. In April of this year, the company began full-scale operation of its mass-production line at Minakuchi Works.

5 IPC: PCB Book-to-Bill Ratio Highest Since July 2010

"North American PCB sales in April continued to lag behind 2012 levels, although sales in the flexible circuit segment are strengthening," said Sharon Starr, IPC director of market research. "Rigid PCB orders for the month exceeded last year's orders and continued to push the book-to-bill ratio up to a strong 1.10."

6 Spirit Circuits Invests in Viking Test's Optima System

Innovative PCB-manufacturer, Spirit Circuits, has recently invested in a high-technology CCD camera AOI system from equipment provider Viking Test. The system, Optima AOI, which was installed this May, uses high-resolution CCD camera systems and a unique software algorithm.

7 IPC: Economic Growth Ahead

Global economic growth is picking up, but the continuing economic crisis in the 17-nation Euro area is delaying a meaningful recovery. Leading macroeconomic indicators and electronics supply chain indicators point to slow growth in the second quarter of 2013.

8 Viasystems Newest Member of EICC

Viasystems Group, Inc. has been accepted as a member of the Electronics Industry Citizenship Coalition (EICC), a coalition of the world's leading electronics companies working together to improve efficiency and social, ethical, and environmental responsibility in the global supply chain.

9 Global PCB Industry Could Reach $93.9 Billion in 2017

According to a new report from Research and Markets, the global PCB industry is forecast to a CAGR of 8.1% during 2012-2017. By regional growth rates, Asia Pacific (APAC) is likely to be the leader of the industry over the next five years.

10 AT&S Sales Up 5%; Venturing into IC Substrate Market

The company finished the financial year 2012/2013 with sales of approximately EUR 542 million, 5% higher than the previous financial year. AT&S also plans to focus on building up its requisite expertise for the production of IC substrates and to prepare for the entry into the market.

EVENTS

- IPC Complete Calendar of Events
- SMTA Calendar of Events
- iNEMI Calendar
- PCB007 Online Events

Micromachine/ MEMS
July 3–5, 2013
Tokyo, Japan

Thermotec 2013
July 3–5, 2013
Tokyo, Japan

NANOTEXNOLOGY 2013
July 6–13, 2013
Thessaloniki, Greece

6th International Symposium on Flexible Organic Electronics (ISFOE13)
July 8–11, 2013
Thessaloniki, Greece

Printed Electronics Asia 2013
July 9–10, 2013
Tokyo, Japan

Semicon West
July 9–11, 2013
San Francisco, California, USA

ITAR and EAR: How Will Export Control Reform Impact Your Business?
July 9, 16 and 23, 2013
Online Webinar

Ohio Valley Expo & Tech Forum
July 11, 2013
Cleveland, Ohio, USA

Surface Mount Rework of BGA, PoP, CSP & QFN Components
July 11, 2013
Dublin, Ireland

Techno-Frontier 2013
July 17–19, 2013
Tokyo, Japan

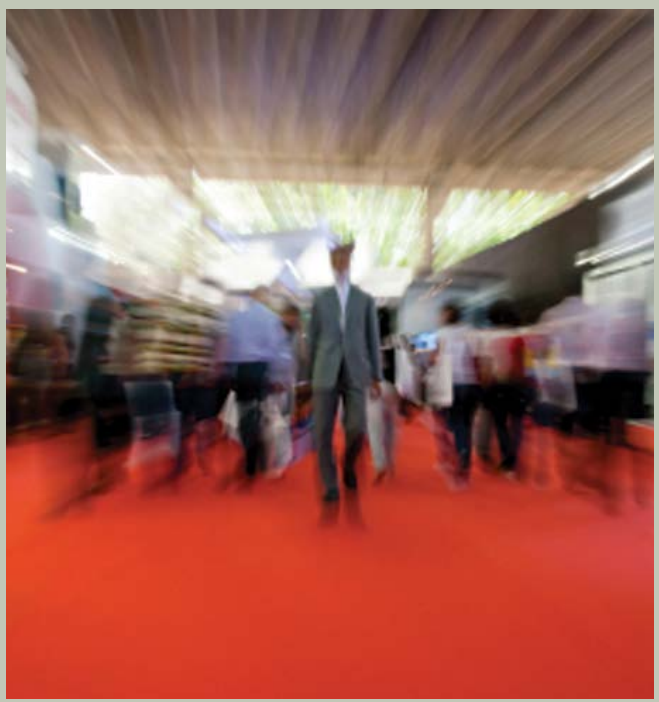
ISMSE 2013
July 27–29, 2013
Singapore

Microscopy & Microanalysis 2013
August 4–8, 2013
Indianapolis, Indiana, USA

Philadelphia Expo & Tech Forum
August 15, 2013
Cherry Hill, New Jersey, USA

NEPCON South China
August 27–29, 2013
Shenzhen, China

IPCA EXPO 2013
August 29–31, 2013
Gujarat, India



PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

PUBLISHER: **RAY RASMUSSEN**
(916) 337-4402; ray@iconnect007.com

SALES: **ANGELA ALEXANDER**
(408) 915-2198; angela@iconnect007.com

EDITORIAL:
GROUP EDITORIAL DIRECTOR: **RAY RASMUSSEN**
(916) 337-4402; ray@iconnect007.com

MANAGING EDITOR: **LISA LUCKE**
(209) 304-4011; lisa@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

MAGAZINE PRODUCTION CREW:
PRODUCTION MANAGER: **MIKE RADOGNA**
mike@iconnect007.com
MAGAZINE LAYOUT: **RON MEOGROSSI**
AD DESIGN: **MIKE RADOGNA, SHELLY STEIN**
INNOVATIVE TECHNOLOGY: **BRYSON MATTIES**
COVER: **SHELLY STEIN, BRYSON MATTIES**

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Next Month in *The PCB Magazine:*

Standards and Regulations

The PCB manufacturing industry is subject to standards and specifications intended to define reproducible levels of product quality and reliability, and harmonize fabrication processes and safety requirements. Which authorities are responsible for generating, maintaining and enforcing these standards? How should standards and specifications be referenced meaningfully when purchasing PCBs? The August issue of *The PCB Magazine* navigates the maze of standards and regulations.