I-Connect007 Presents

the pcb magazine

July 2016

Taking a Closer Look at Test & Inspection

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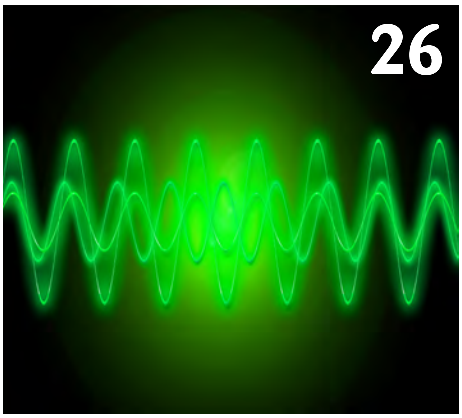

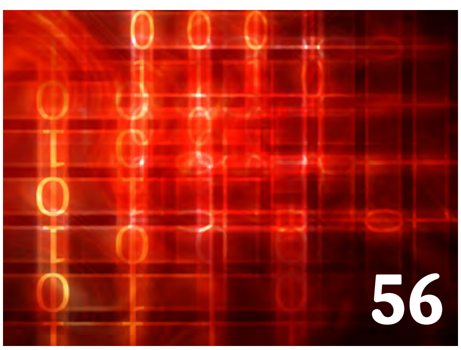

Inspection & Test

There's more to test and inspection than the latest and greatest AOI and electrical test equipment. This month, feature contributors from Orbotech, Gardien Services, Uyemura, and more, examine various testing methods that go into ensuring great product.

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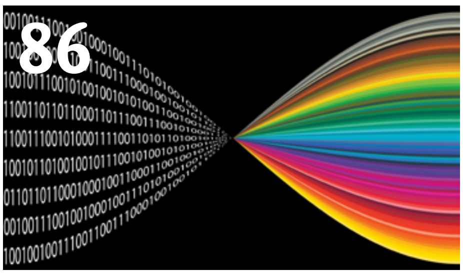

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Delving into Test and Inspection

by Patty Goldman
I-CONNECT007

I've always been a wet processing person, if not always in a PCB shop, at least at heart. My undergraduate degree is in chemistry and I cut my teeth working on electroless copper processes (just a metaphor, mind you!). Testing, testing and more testing in R&D can be sooo boring and repetitive. I've done my fair share of cross-sections and titrations and the myriad other tests required, as well as a fair amount of time peering into a microscope.

When I got into a real PCB shop and worked on all the wet processes, the quick test-on-the-line approach appealed to me. I continually wondered at the inspectors who could sit hour after hour and inspect finished product, and the lab personnel who could happily test the same bath over and over day after day.

So it was with trepidation that I approached our topic this month. What was there to talk about but the latest, greatest AOI and electrical test equipment? Ah, but there is so much more to this topic. What about all the other testing that goes on to ensure great product? And so we're off and running with one heck of a line-up for you and it isn't all about fancy test/inspect equipment.

That being said, we do start out with a great little article by Orbotech's Micha Perlman, in which he discusses the latest abilities of AOI equipment. It has come a long way since AOI

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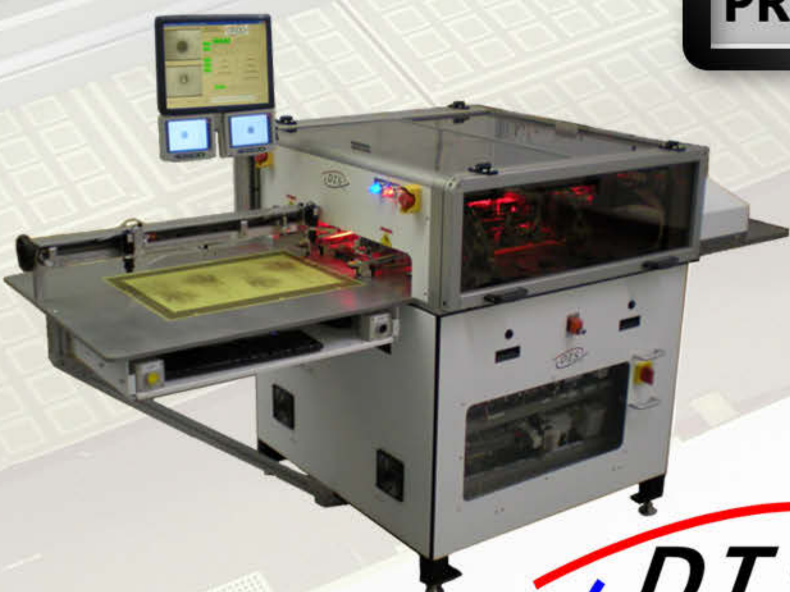

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was first introduced in the '80s. Identifying defects is just one part of the capabilities.

To balance that, we next introduce our newest columnist, Keith Sellers with NTS-Baltimore (formerly Trace Labs). In this first column Keith delves into fractographic analysis; in his example he visually analyzes substrate cracking and voiding using both microscope and SEM. There are many facets to inspection!

We are pleased to include the next article, which won the Best Paper award at IPC APEX EXPO this year, on the IPC Round Robin of high-frequency test methods. The principal author is Glenn Oliver of DuPont; co-authors include Chudy Nwachukwu of Isola, John Andresakis of Park Electrochemical, John Coonrod of Rogers Corp., David Wynants of Taconic and Don DeGroot of Connected Community Networks. There is much useful information in this thorough treatise. Due to its length, we have chosen to publish the first half in this magazine with a link to the second half that includes the Results and Conclusions.

"Test and inspection methods are only as good as the systems and equipment you are using."

Getting back to electrical testing, Todd Kolmodin of Gardien Services USA provides a useful overview of the various electrical tests and methods used to validate design and manufacture of PCBs.

Test and inspection methods are only as good as the systems and equipment you are using. Patrick Valentine of Uyemura USA gives us a clear step-by-step explanation of the Type 1 Gauge study to help you determine the accuracy and precision of your measurements. He uses a real-life example of plating thickness to illustrate his point.

Next we have another paper that was originally presented at IPC APEX EXPO this spring. Author François Lechleiter of Cimulec Group presents an innovative thermal conductivity measurement method for use on the composite materials used in the PCB industry.

And now let's hear what's happening in Brazil (other than the Summer Olympics). Our Brazilian correspondent, Renato Peres of Circuibras examines how best to improve impedence testing by making coupons match the board.

Our regular columnist Mike Carano of RBP Chemical Technology chose reliability as his subject this month—more specifically, the reliability of the plated through-hole of a PCB. He describes the various types of thermally-induced failures and includes photos along with trouble-shooting information.

Karl Dietz has supplied a great overview of digital imaging systems on the market today, including those recently introduced. He lists each manufacturer along with their equipment and what each can do. This is a great little reference piece for anyone considering DI equipment in the near or far future.

Last but not least, for a totally non-technical change, we have Barry L. Cohen (BLC) of Launch Communications with an entertaining little missive on the importance of literature to one's sales and marketing program.

So there you have it. Test and inspection has turned into a huge subject and gosh, we barely scratched the surface. Are there other T&I subjects that you would like to hear about? Let me know! We'll find someone to answer your questions, I'm sure. In the meantime, we really do want to hear from YOU, dear reader, for our August issue. We want to hear your thoughts and opinions. Send me a note or try clicking here for a few leading phrases to get you started. **PCB**

Patricia Goldman is a 30+ year veteran of the PCB industry, with experience in a variety of areas, including R&D of imaging technologies, wet process engineering, and sales and marketing of PWB chemistry. Active with IPC since 1981, Goldman has chaired numerous committees and served as TAEC chairman, and is also the co-author of numerous technical papers. To contact Goldman, click here.

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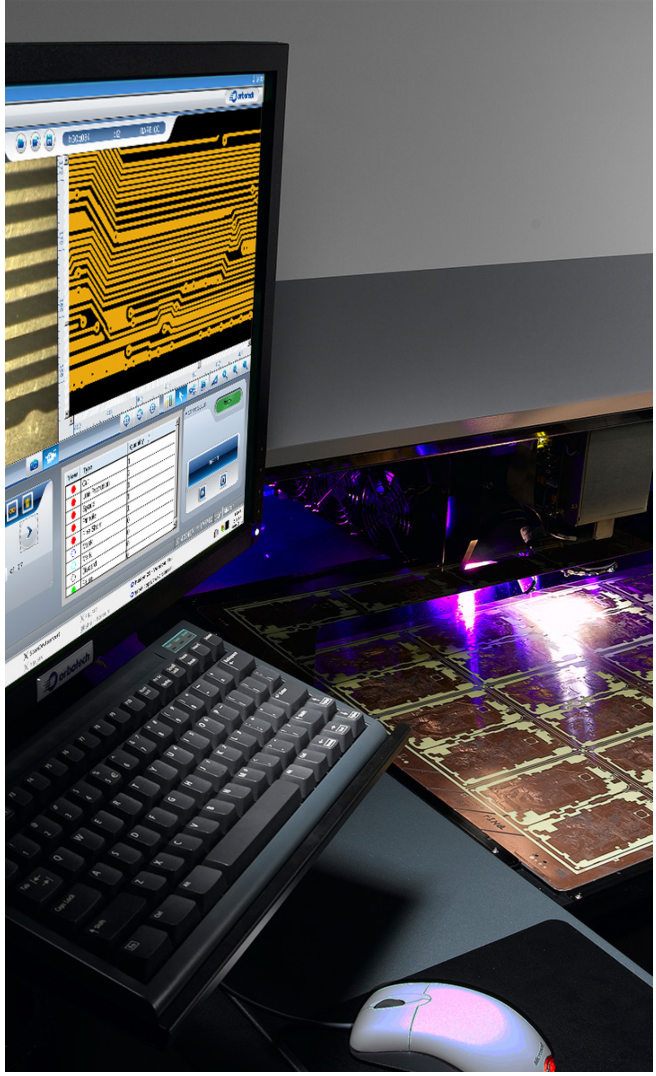
Faster, More Accurate AOI is More Important than Ever

by Micha Perlman
ORBOTECH



Among PCB manufacturers, there is a common perception that AOI has not changed much since it was introduced decades ago. Over the last few years, however, new advanced technologies have made AOI solutions smarter, faster and much more accurate. AOI system data have even been integrated with newly developed automatic 3D shaping tools to enable restructuring of defects in PCB patterns that are detected by the AOI solution.

Many of these new AOI technologies offer benefits to a broad range of PCB manufacturers, from high-volume mass production shops to those focused on special market segments with unique materials and PCB structures or those who need high flexibility and quick turnaround operation.

While not all AOI solutions are alike, it can be assumed that all PCB manufacturers and designers share a concurrent core of production goals such as shortening overall inspection time, increasing real defect detection while reducing false positives, and reducing both setup time and cost per inspection. If some or all of these goals are on your to-do list, you will definitely be interested in some of the new innovations in AOI.

Much More Accurate Defect Detection

AOI accuracy has always been important. Today, as designs become more complex and expensive, production defects have a greater impact on profit. In designs for automotive, aerospace, military and medical devices, for example, where reliability and safety are critical, 100% detection accuracy is essential.

Numerous factors increase the complexity of PCB defect detection. They can include higher-density designs with lines and spaces below 30 µm and a wide array of board types such as HDI, high layer count, flex and rigid-flex. In addition, there is a wide array of substrate materials including expensive high-frequency dielectric resins like Rogers and Teflon™. Not all AOI solutions can handle all of these factors.

Most AOI solutions are able to rapidly scan for errors using a single, monochromatic pattern image that is captured using a composited average illumination of the different materials and colors on the inspected panel. For low-cost products where, for example, scrap is a lower priority or where a higher defect count can be sustained, this method might suffice.

However, when these factors are in play, multiple imaging technology can be of great value. AOI solutions with multiple imaging technology simultaneously reveal details that are unseen by conventional single-image mono-

chrome AOI systems. Illuminating the panel with different wavelengths at different angles makes it possible to accurately classify materials such as clean copper, oxidized copper and contamination as well as abnormal shapes such as dish-downs or shallow shorts.

Two different defects might look the same under one illumination source. But the true difference is revealed using multiple illumination sources, which simultaneously detect the subtle differences between actual defects and false alarms (Figure 1). This results in the highest possible detection results without compromising on throughput.

Support of the Most Challenging PCB Materials and Types

For years, AOI solutions have been able to accurately inspect a range of designs and substrates. When it comes to flex and thin HDI layers, traditional AOI systems start to run into problems when trying to detect errors on the transparent and translucent layers. When imaging multiple layers, the lower layers tend to show through the layers that are being inspected, creating false defect reports.

Multiple imaging technology eliminates the multilayer confusion by illuminating the inspected layer with different light wavelengths. The multiple captured images provide the required visual information for accurate inspection with no false alarms from underlying layers. An example of this is shown in Figure 2.

Advanced Image Analysis Solutions and 'Oversensitivity' Reduction

The accuracy of the AOI system inspection relies on the accuracy of the imaging, but it also needs accurate CAM data to compare with the image to ensure that the anomalies in the image are, in fact, anomalies. Moreover, advanced integration of CAM data with all its inherent information with advanced AOI algorithm adds another critical dimension to detection accuracy.

Today, the most advanced AOI solutions significantly reduce oversensitivity—false positive errors—by using intelligent panel understanding algorithms. The AOI image analysis tools have the information about the detected error point including its location, specific role in the pattern and the defined dimension and

Figure 1: a) Microscopic image showing possible copper defect; b) using light source 1—still uncertain; c) light source 2—dust/pseudo-defect detected.

Figure 2: a) Microscope image; b) light source 1—lower layers show through; c) light source 2—only inspected layer is seen for accurate inspection.

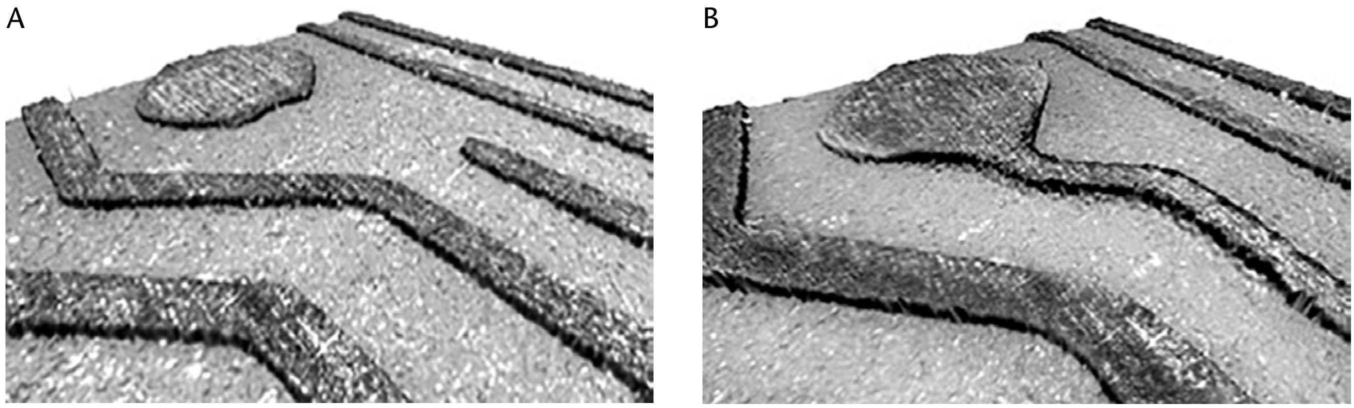


Figure 3: a) 3D image before shaping; b) 3D image after shaping.

tolerances. Taking this into consideration, an algorithm sorts the defects by whether they are in a critical area and eliminates oversensitivity alarms in less critical areas.

For example, an AOI solution with intelligent panel understanding will ignore small defects in non-active areas of the design such as copper residues, ground or shielding which will not affect the functionality of the board. At the same time, it will seek the finest defects on critical lines, spaces and pads.

Although you cannot expect to find multiple imaging technology and advanced panel understanding in every vendor's solutions, when you see their superior accuracy you will realize why it is becoming an AOI priority for PCB manufacturers.

Automation-Assisted AOI Setup

All PCB manufacturers want to reduce setup time in each phase of the production process. This is particularly true for producers of specialty boards and prototypes with short runs that could require tens of new setups on a daily basis. AOI setup is often a tedious, iterative process which now can be replaced with a faster, more accurate automated setup process.

In AOI systems with automation-assisted setup, a non-expert operator can create an optimal setup by visually categorizing true and false defects on the first panel of a job. Then the system automatically categorizes the defects into groups and sorts them according to severity, from the most critical to the least. It builds the optimal setup profile and automatically configures all relevant parameters accordingly. The result is an intuitive, optimal and much shorter setup process that is automatically implemented for the remainder of the run, increasing AOI throughput for the entire production cycle.

Of course, automated setup can only be performed if the system can integrate with the manufacturer's CAM system and when the AOI solution provides the level of inspection accuracy delivered by solutions with multiple imaging and intelligent panel understanding technologies.

Automated Optical Shaping Capabilities

Another reason that advanced AOI capabilities are more important today is that now the high-quality inspection data from the AOI process can be used to integrate with automated optical shaping (AOS) solutions. The most recent advances in 3D shaping mean that, in addition to shaping copper shorts where excess copper needs to be ablated, the latest AOS solutions can also shape opens where more copper needs to be added. Examples are shown in Figures 3 and 4.

When both shorts and opens are shaped in a one stop process, PCB scrap is virtually eliminated, even in the most advanced products such as any-layer HDI, complex MLB on multiple lines areas, corners and pads. These new AOS solutions can overcome traditional limitations of manual shaping, enabling shaping on boards that could not be saved otherwise.

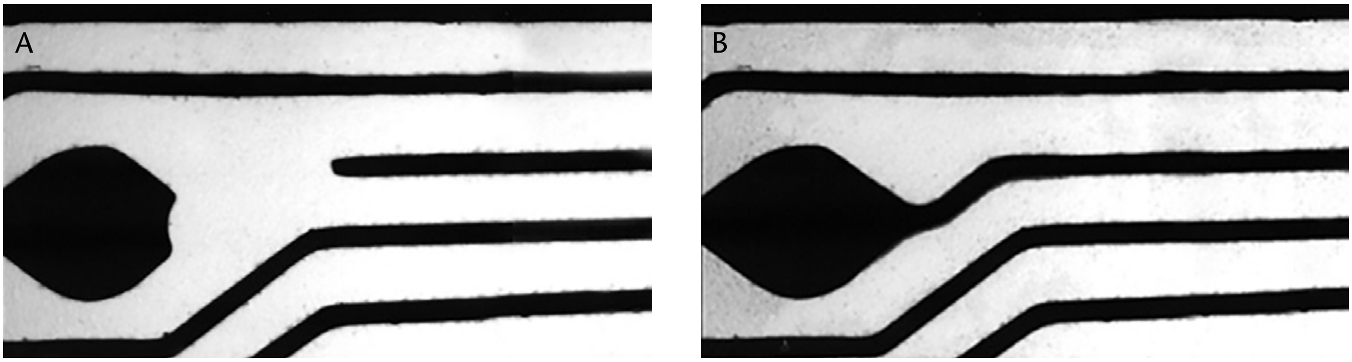


Figure 4: UV image before shaping; b) UV image after shaping.

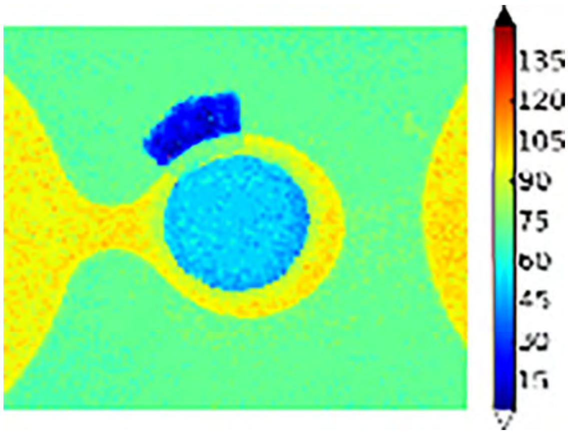


Figure 5: 3D measurement.

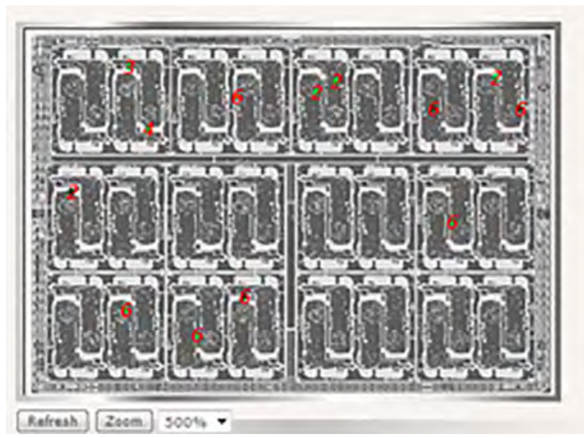


Figure 6: Defect mapping.

New Measurement and Reporting Capabilities

In many PCB manufacturing domains, and especially in those that serve aerospace, military, automotive and medical device market segments, safety and quality control measurements add tremendous time and labor obligations throughout production. Automatic measurement and reporting tools have been developed using the most advanced AOI inspection and measurement capabilities. These capabilities make it easier to meet the quality and reliability reporting obligations compared with less sophisticated manual solutions.

Solving PCB Production Problems with Advanced AOI

AOI is only a part of an automated PCB production process. But we've seen how the capabilities of the more advanced AOI solutions have increased the value and importance of AOI in the overall process. Using multiple imaging technologies, advanced optics, algorithms and data processing capabilities to detect, and categorize defects, advanced AOI solves many of the complex issues facing the industry.

With support for flex, rigid-flex, multilayer and HDI PCBs that use a wide range of materials, streamlining of the AOI process and enabling other advanced processes such as high-accuracy automated shaping for both shorts and opens, the new advances in AOI solutions increase production accuracy, reduce scrap and improve throughput. **PCB**

Micha Perlman is senior marketing manager, PCB Division with Orbotech.

Seeing is Believing
in Fractographic Analysis

by Keith M. Sellers
NTS-BALTIMORE

Editors note: This is Keith's first in a series of columns having to do with inspection and test—from the test lab perspective.

One of the more common types of failure analysis is the investigation of something that has broken. For this column, we will be discussing a broken material, or, more commonly, a fractured or cracked material.

Fractographic analysis is sometimes perceived as a difficult analysis, given its roots in material science, but one might be surprised to learn that failure modes for this type of study are well-established and well reported and can easily be found in textbooks, reference materials, and even with a Google search! Given that, this column is not being written to teach a lesson in fractographic failure modes, but more so to provide some insight in performing the analysis yourself, or at least give you some direction to get things started.

Unlike many types of forensic analyses, a fractographic investigation most times doesn't really need any high dollar, sophisticated instrumentation or equipment. This is true because the most pertinent information in a fracture based investigation is simply the visual examination of the fracture surface itself. Now, that can be problematic in some instances, because the fractured surface can become damaged before it is discovered. If a crack happens and is still connected on one end, it's possible that the opposing surfaces of the fracture can make contact with each other—through movement of the specimen while still in use or even through simple vibration—potentially damaging the surface characteristics that are needed to determine the failure mode at hand. This is not overly common, but can happen, and as such it's worth mentioning here. For this reason, one recommendation that can be made is…don't put the pieces back together! In line with what has been mentioned just a few sentences ago, putting the fractured pieces back together can accidently damage what you're really trying to inspect.

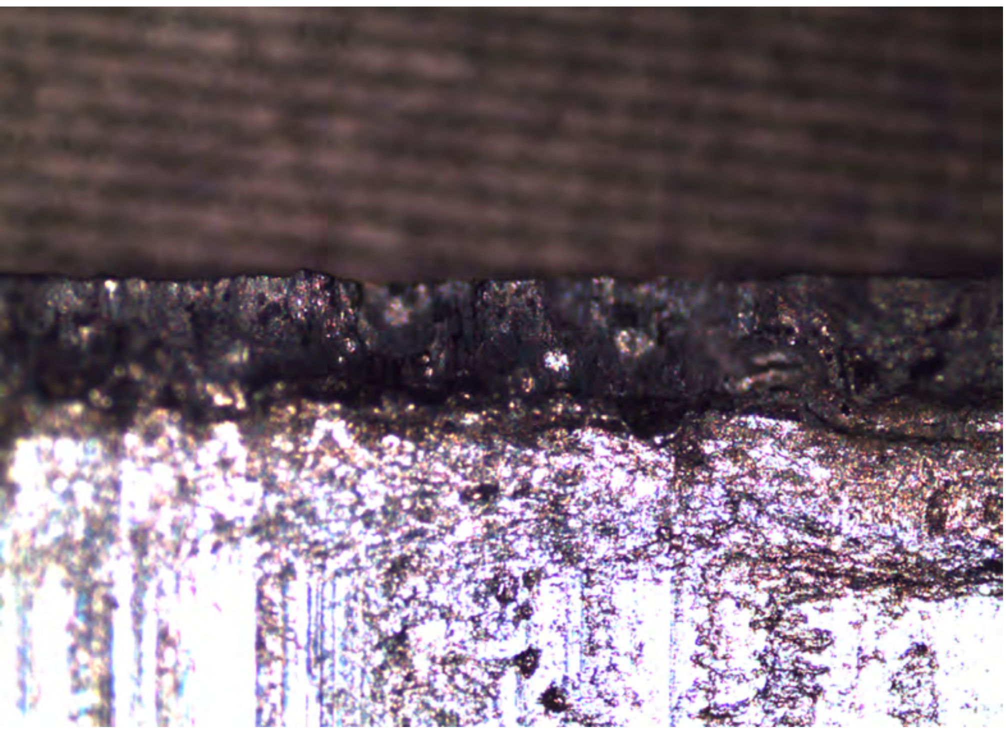


Figure 1: Representative overview of fracture surface using steromicroscopy.

Back to the topic of the visual examination…this tru-

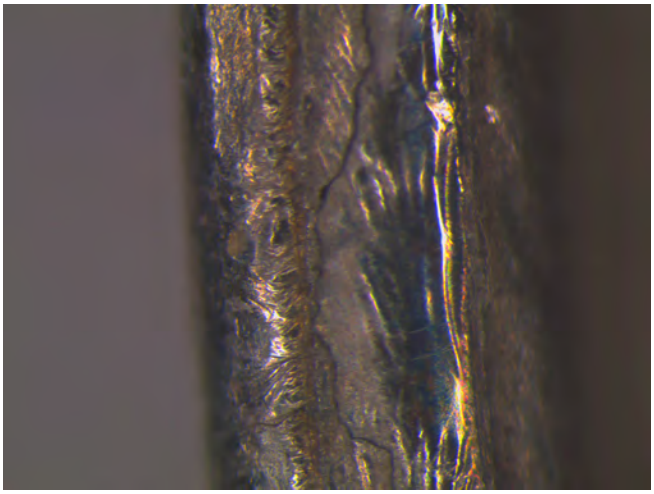


Figure 2: Representative close-up of fracture surface using steromicroscopy.

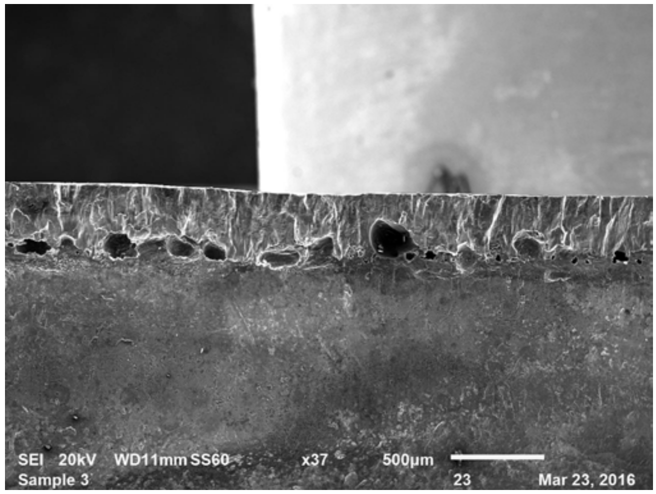


Figure 3: Representative SEM overview of fracture surface with voiding.

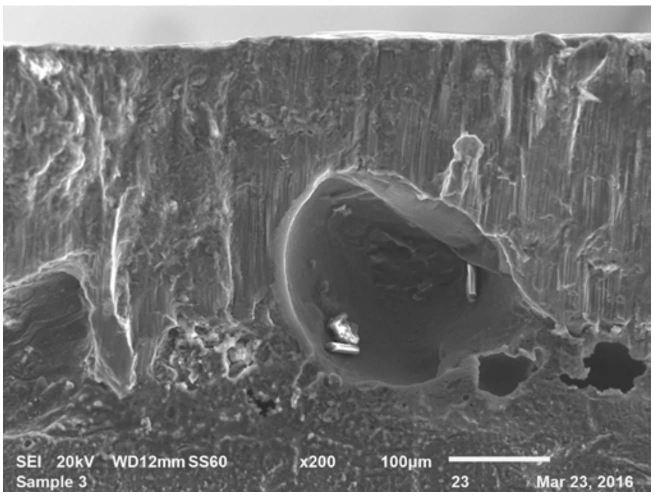


Figure 4: SEM close-up of fracture surface with voiding.

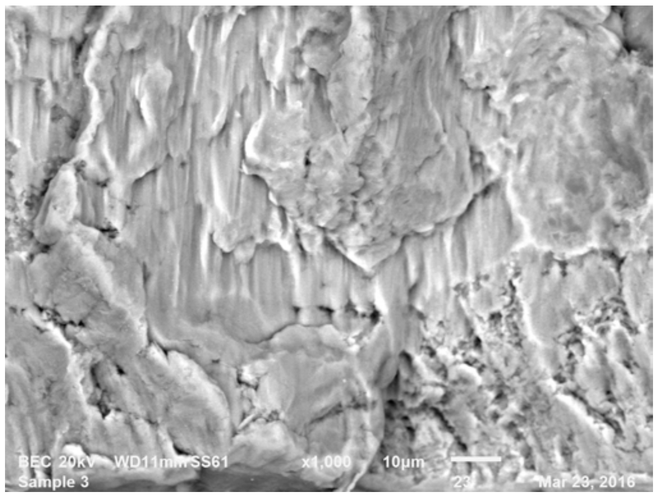


Figure 5: High magnification close-up of representative fracture surface.

ly is the most important part of a fractographic analysis. All of the important questions about type, initiation point, direction, etc., can all be answered just by looking. The tools which are needed for this type of investigation are common for most laboratories. Simply put, a microscope and a good light source. Stereomicroscopes are the norm for this type of visual examination as their two-eyepiece design allows for easier inspection of the non-smooth fracture surfaces. Inexpensive, relatively speaking, the stereomicroscope can commonly obtain images of fracture planes, voiding, etc., and provide a good bit of information in a very short timeframe.

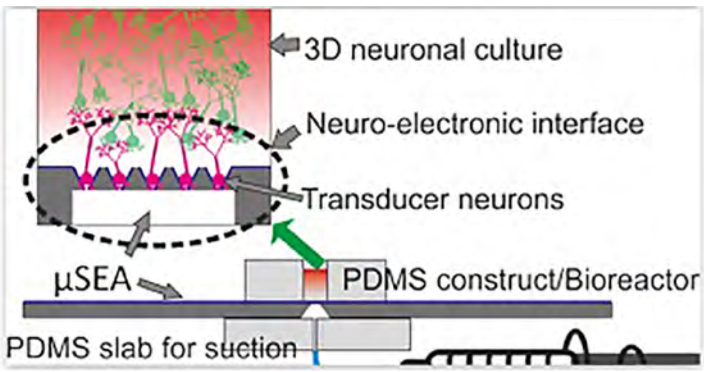
Taking your inspection to the next level, a scanning electron microscope (SEM) is another great tool for the visual inspection of fracture surfaces. Besides the fact that SEMs take a different kind of picture, using it as a visual examination tool, this type of microscope eliminates the potentially biasing visual characteristics of color, sheen, gloss, etc., that may get in the way when viewing your specimens with a traditional stereomicroscope. Visual examination via SEM is a lesson in shades of gray; however,

these gray-tones paint a different kind of picture for your investigation, easily showcasing clam shells, striations, coalesced voiding, grain boundaries, and other fracture surface trademarks.

Ultimately, as with just about any testing, having the correct instrumentation is key for obtaining the information needed to solve your problem or answer your question. For this topic, fractography, a solid visual inspection/examination is almost all you need to determine the root cause of the fracture and the stereomicroscope and SEM are key players. Obviously, further testing could be needed after this visual examination depending on what questions are being asked. For example, material properties—such as tensile strength, hardness, impact strength, alloy/material composition, etc.—may need to be investigated to determine if the correct material was called out or even, in some circumstances, if the correct material was used in construction. Nonetheless, a somewhat simplistic visual examination, along with a little background study on failure modes, will go a long way in the world of fractography. **PCB**

Keith M. Sellers is operations manager with NTS in Baltimore, Maryland.

Brain-on-a-Chip in 3D



To study brain cell's operation and test the effect of medication on individual cells, the conventional Petri dish with flat electrodes is not sufficient. For truly realistic studies, cells have to flourish within three-dimensional surroundings. Bart Schurink, researcher at University of Twente's MESA+ Institute for Nanotechnology, has developed a sieve with 900 openings, each of which has the shape of an inverted pyramid. On top of this array of pyramids, a micro-reactor takes care of cell growth. Schurink defends his PhD thesis June 23.

A brain-on-a-chip demands more than a series of electrodes in 2D, on which brain cells can be cultured. To mimic the brain in a realistic way, you need facilities for fluid flow, and the cells need some freedom for themselves even when they are kept at predefined spaces. Schurink therefore developed a micro sieve structure with hundreds of openings on a 2 by 2 mm surface. Each of these holes has the shape of an inverted pyramid. Each pyramid is equipped with an electrode, for measuring electrical signals or sending stimuli. At the same time, liquids can flow through tiny holes, needed to capture the cells and for sending nutrients or medication to a single cell.

Neuronal Network

After neurons have been placed inside all the pyramids, they will start to form a network. This is not just a 2D network between the holes: by placing a micro reactor on top of the sieve, a neuron network can develop in the vertical direction as well. Schurink's new µSEA (micro sieve electrode array) has been tested with living cells, from the brains of laboratory rats. Both the positioning of the cells and neuronal network growth have been tested. The result is a fully new research platform for performing research on the brain, diseases and effects of medication.

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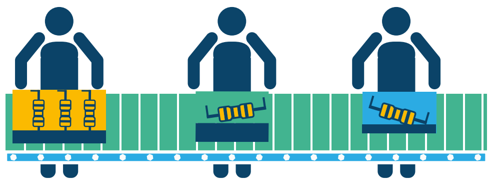
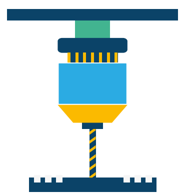


How Well Do Your Processes Meet IPC Standards



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Supply Lines Highlights

New Management and Strategies at eSurface

At the recent Geek-A-Palooza, I spoke with Alex Richardson and Rick McCann of eSurface Technologies, to learn about the condition of the company, their new semi-additive approach, and a couple of big announcements.

Rogers' John Coonrod on Insertion Loss

John Coonrod of Rogers Corporation gave a keynote presentation at the recent Geek-A-Palooza trade show, concentrating on printed circuit board fabrication's influences on insertion loss. I sat down with John to learn more about his presentation and what OEMs and designers need to be aware of to avoid insertion loss.

Orbotech Launches Nuvogo Fine at JPCA 2016

The Nuvogo Fine is specifically designed for new production methods and technologies, in particular for advanced high density interconnect (HDI), including modified semi-additive process (mSAP) and flexible printed circuits (FPC) at exceptionally high throughput on all types of resists.

Taiyo Announces Director & COO Appointed to Position of President and Director of Taiyo America Inc.

Taiyo America Inc.'s Director & COO Tadahiko Hanada has been promoted to the position of President and Director, effective June 6, 2016.

Ventec International Group Earns ISO 9001:2015 Certification for Its German Facility

Ventec International Group, a world leader in the production of polyimide & high reliability epoxy laminates and prepregs, is proud to announce that its Central European facility located in Kirchheimbolanden, Germany, has received certification under the ISO 9001:2015 quality management standard.

Laser Pointers: Automate to Innovate in Flex Processing

The growing market demand for mobile devices, wearables and Internet of Things (IoT) devices continues to create new challenges for suppliers and manufacturers in the electronics value chain. Along with this market demand comes a challenging set of market requirements for the underlying circuits and components that drive such devices.

Gold Plating Services Installs Technic ENEPIG Process

Technic is pleased to announce the installation of the TechniPad Electroless Palladium process AT7015 at Gold Plating Services (GPS) in Santa Clara, California. GPS is a contract plating service specializing in precious metal plating for the printed circuit board industry.

Gardien Group Named Worldwide Distributor for Kaima and Image Products

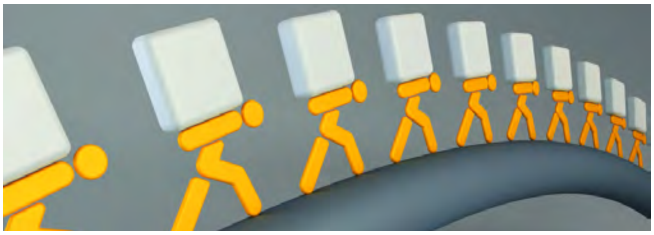
The Gardien Group recently announced that it has become a worldwide distributor of Kaima and Image products and services. Gardien will be the exclusive distributor for Europe, the Americas, Japan, Malaysia, Singapore, Vietnam and Indonesia, and a non-exclusive distributor for China and Taiwan.

Ucamco Updates Gerber Nested Step & Repeat Proposal

Ucamco is extending the Gerber format to make it more efficient in handling fabrication and assembly panels. To allow the Gerber user community to review and comment on the new feature before it is cast in concrete, a draft specification is made available for download from the Ucamco website.

Zuken Introduces Perfect Springback Routing in CADSTAR 17

Zuken has rolled out routing enhancements in the latest version of its CADSTAR desktop PCB design software. Other productivity enhancements include improved routing patterns for differential pairs, and etch factor support.



Round Robin of High-Frequency Test Methods by IPC-D24C Task Group (Part 1)

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DUPONT*

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Abstract

Currently there is no industry standard test method for measuring dielectric properties of circuit board materials at frequencies greater than about 10 GHz. Various materials vendors and test labs take different approaches to determine these properties. It is common for these different approaches to yield varying values of key properties like permittivity and loss tangent. The D-24C Task Group of IPC has developed this round robin program to assess these various methods from the "bottom up" to determine if standardized methods can be agreed upon to provide the industry with more accurate and valid characteristics of dielectrics used in high-frequency and high-speed applications.

Problem Statement

Accurate values of relative permittivity (ε_r) and loss tangent (tan δ) are important characteristics for designers and fabricators in predicting electrical performance of circuits at high frequencies[1]. The most common method for evaluating these parameters at frequencies up to 10 GHz is described in IPC-TM-650-2.5.5.5[2]. This method is equivalent to ASTM-D-3380[3]. This method excites a stripline resonator at both ends with the dielectric under test comprising most of the volume. The stripline is created by establishing intimate contact using a constant clamp force. This method is highly repeatable and is optimized for QA testing at a specific frequency. This method is not well suited for characterizing at frequencies higher than 10 GHz.

Both analog and digital applications now commonly excite dielectric materials at frequencies well above 10 GHz. Measurements at higher frequencies are especially challenging for many reasons. For instance, the wavelength of radiation at 30 GHz is <10 mm in air and <5 mm in FR4. This makes it more challenging to isolate the interactions of the waves with the material under test from any parasitics introduced by the test fixture. Another significant challenge at these high frequencies is that current is concentrated at the "skin" of metal surfaces. As frequencies increase, the microstructure of metal surfaces contributes more significantly to overall loss or degradation, and makes it nearly impossible to isolate the impact of the dielectric losses separate from the metal.

Introduction

In an effort to potentially determine standardized test methods at these frequencies, seven members of IPC D-24C Task Group developed a round-robin to measure ε_r and tan δ for various PCB materials using different methods of their choosing and compare results.

First, this paper details the problem followed by a description of the various evaluation methods being considered; each method is described with sufficient information to allow for third party replication. Next, the results from each labs independent dielectric property characterizations are presented and subsequently compared. Finally, this paper will discuss each methods pros and cons and any conclusions or next steps.

Each test lab participant measured ten circuit board material samples up to the highest frequency for which they could provide valid data. Each participating test lab measured material from the same lot. The circuit board materials for testing were constrained to the following general properties:

- 0.5 oz Copper Clad (18 µm thick)
- Dielectric Thickness: 100-150 µm
- Relative Permittivity (ε_r): 2.0 – 4.0
- Loss Tangent (tan δ) <= 0.005

Ten materials of various constructions from multiple manufacturers were provided for characterization. Table 1 presents these materials and their general properties while assigning each material an arbitrary designator.

The ε_r of each was measured using eight different methods and where it is demonstrated in this paper:

Microstrip Transmission Line Methods:
1. Extraction from impedance (ε_r only)
2. Group delay extraction from phase (ε_r only)
3. Differential phase length (ε_r only)

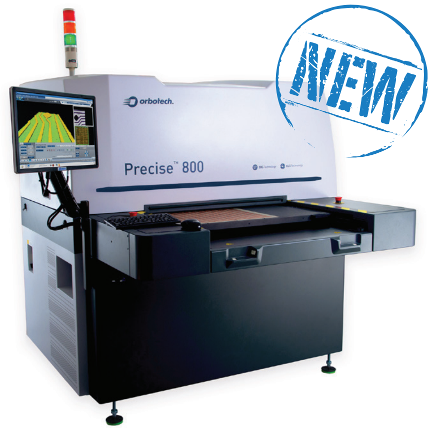
Free Space Transmission Method:
4. Free space quasi-optical (ε_r only)

Sample Name	Material Description	Expected Normal ε_r @ 10 GHz	Expected tan δ @ 10 GHz	Nominal Thickness, mil (µm)
Sample A	Flex Polyimide	3.3	0.0040	6 (150)
Sample B	Flex Fluoropolymer / Polyimide Composite	2.5	0.0020	4 (100)
Sample C	Liquid Crystal Polymer (LCP)	3.00	0.0016	4 (100)
Sample D	Ceramic Filled Polymer on Fiberglass Substrate	3.50	0.0028	5 (125)
Sample E	Glass Microfiber Reinforced PTFE	2.20	0.0009	5 (125)
Sample F	Ceramic Filled PTFE	3.6	0.0015	5 (125)
Sample G	Micro Dispersed Ceramic in PTFE Composite on Woven Fiberglass Substrate	2.94	0.0012	5 (125)
Sample H	Ceramic filled PTFE on Woven Fiberglass Substrate	3.50	0.0020	5 (125)
Sample I	PTFE on Woven Fiberglass Substrate	2.20	0.0009	5 (125)
Sample J	Ceramic Filled PTFE on Fiberglass Substrate	3.00	0.0011	5 (125)

Table 1: Circuit Board Materials Tested.

AP
YOUR YIELD

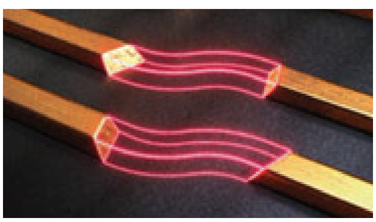
opens, shorts and other copper defects

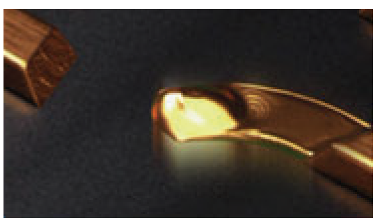


Precise™ 800 AOS

- 1-Stop solution for open and short defects
- Precise 3D shaping of opens and other missing copper defects
- Accurate shaping of shorts and other excess copper defects
- High quality shaping to mirror original CAM design data

3DS Technology™ **CLS** Technology™


3D Analysis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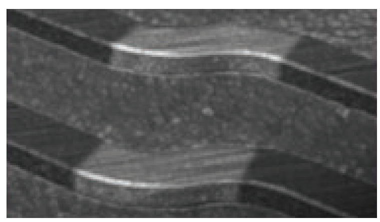

3D Visualization

Perturbed Resonant Cavities with Electric Field Oriented In-Plane of Dielectric:

5. Rectangular cavity and open resonator (ε_r and tan δ)

6. Split post dielectric resonator - SPDR (ε_r and tan δ)

Aperture-Coupled Stripline with Electric Field Oriented Normal to Plane of Dielectric:

7. Bereskin resonator (ε_r and tan δ)

Descriptions of Measurement Methods

Extraction of ε_r from Impedance Measurements of Microstrips

The objective of this method is to calculate normal ε_r values from time-domain measurements [4]. This method does not directly yield tan δ and is a fixed value without frequency dependence. The principle of this technique is to back-calculate ε_r from impedance values measured on a time-domain reflectometer (TDR). The advantage of this method is that it can utilize any microstrip transmission line or even impedance coupons on a circuit board. The disadvantages are that the values are limited by the pulse-width of the TDR and the back-calculation of ε_r requires a lot of assumptions.

For this study, samples were prepared by etching multiple micro strip transmission lines. These micro strip transmission lines were broken up into three line widths and two lengths. This produced six microstrip transmission lines of varying widths and lengths for each circuit board material sample. The microstrip lengths were 130 mm and 230 mm while the widths ranged from 210 µm up to 400 µm depending on the material. The three line widths were chosen for each sample based on the theoretical ε_r and corresponding 50 Ohm line width. The desire was for the narrow line to have impedance greater than 50 Ohms and the wide line to have impedance less than 50 Ohms with the other line falling squarely in the middle. An example of two equal line width microstrips of two different lengths can be seen in Figure 1.

Once the microstrips were prepared, the physical dimensions of each were needed. Figure 2 shows the measurements required for the impedance extraction method. Dielectric thick-

Figure 1: Two example microstrip transmission lines for impedance extraction.

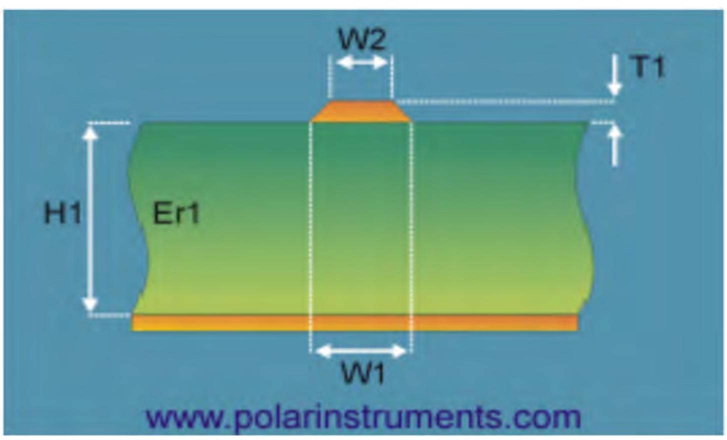


Figure 2: Microstrip transmission line cross section[5].

ness (H1) and microstrip line widths (W1) were measured using a pneumatic gauge and an optical comparator respectively. Additionally, after the impedance measurements were made, each line was cut and a cross section was taken to verify the dielectric thickness (H1), microstrip line thickness (T1), and microstrip line width on top (W2) and bottom (W1) of the microstrip. This provided the actual values needed to accurately calculate ε_r for the circuit board materials.

Utilizing a TDR, impedances were measured for all six samples from both directions for each material. This yielded 12 impedance measurements for three line widths and two lengths. Figure 3 illustrates an example (Sample A) of the TDR impedance output versus propagation time. This figure demonstrates one of the nuances to using this impedance extraction method. The TDR provides impedance measurements versus time. Subsequently, the impedance of test cables and connectors must be considered when choosing at which point in time to measure impedance. As time directly relates to distance, a time should be chosen where the impedance being measured is somewhere within the transmission line and away from the connectors. Additionally, this point in time must be identical for all lines measured.

The 12 impedances for each circuit board material were measured and plotted versus measured line width. A linear regression function was developed to allow for calculation of a microstrip line with 50 Ohm characteristic impedance. This set of tests yielded impedance, dielectric thickness, microstrip line thickness, and microstrip line widths for each test sample. The measured characteristics were then used in a commercial field solver in order to back-calculate the ε_r. There are many calculators and field solvers available and most are suitable for this calculation.

Group Delay Extraction of ε_r from Phase of Microstrips

Microstrip transmission lines are a type of quasi transverse electromagnetic (TEM) structure[6]. Since the electromagnetic field propagates in media with different relative permittivity below and above the signal, the structure is inherently dispersive. The rate at which a pulse of energy traverses a transmission line is called group velocity (ν_g). For dispersive transmission

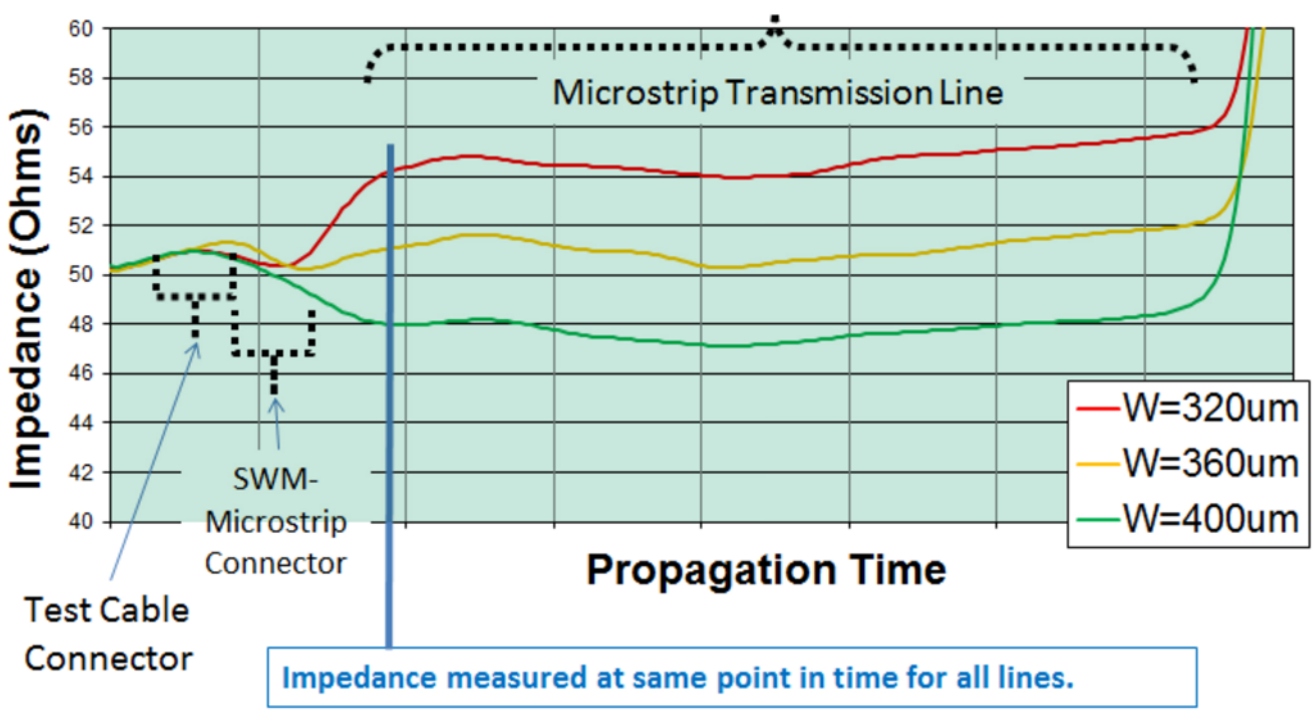


Figure 3: Time domain reflectometry (TDR), impedance versus time.

lines, v_g will depend on frequency. In the frequency domain, the change in phase with frequency is defined as group delay (τ_g) and can be measured and expressed as a time delay. Given the fields within the microstrip are propagating within a dielectric, the group velocity and group delay are necessary functions of the dielectric properties of the PCB on which the microstrip is constructed. Therefore, the relationship between group velocity/delay and the PCB dielectric properties allows for calculation of ε_r once the group delay of a particular microstrip transmission line is known.

The same microstrip lines utilized in the impedance extraction method of this paper were utilized here. The only difference is that data was measured in the frequency domain instead of the time domain. The group delay method utilizes the described dispersive properties of microstrip transmission lines and the swept frequency source of a vector network analyzer (VNA) to calculate frequency dependent normal ε_r. Fortunately, group delay is easily measured with a VNA using the simple relationship in the following equation [7]:

$$Group\ Delay\ (\tau_g) = \frac{\Delta\varphi}{\Delta\omega} = \frac{\varphi_2 - \varphi_1}{\omega_2 - \omega_1}$$

where

$$\varphi = phase\ angle\ (radians)$$

$$\omega = 2 * \pi * frequency = angular\ frequency\ \left({}^{Radians}/_{Second}\right),$$

$$\Delta\varphi = Difference\ in\ Phase\ Angle\ (Radians),$$

and

$$\Delta\omega = 2\pi f = Difference\ in\ Angular\ Frequency\ \left({}^{Radians}/_{Second}\right)$$

The phase data collected on a VNA must be unwrapped before this calculation can be fully accomplished. If the phase is not unwrapped and the difference in frequency corresponds to a 360-degree phase wrap, the calculated value will not provide a correct group delay. The wrapped and unwrapped phase can be seen in Figure 4. The group delay can be calculated locally if the phase is not unwrapped.

Once the group delay is obtained the effective dielectric constant (K_{eff}) can be calculated using the following equation:

$$\text{Effective Dielectric Constant } (K_{eff}) = \left(\frac{c * \tau_g}{L}\right)^2$$

where

$$L = microstrip\ transmission\ line\ length\ (meters),$$

$$c = 3x10^8 \left(\frac{meters}{second}\right),$$

and

$$\tau_g = group\ delay\ (seconds).$$

With the effective dielectric constant (K_{eff}) of the microstrip transmission line now known, the frequency dependent ε_r can be calculated. The effective dielectric constant of a microstrip transmission line is not the same as the PCB

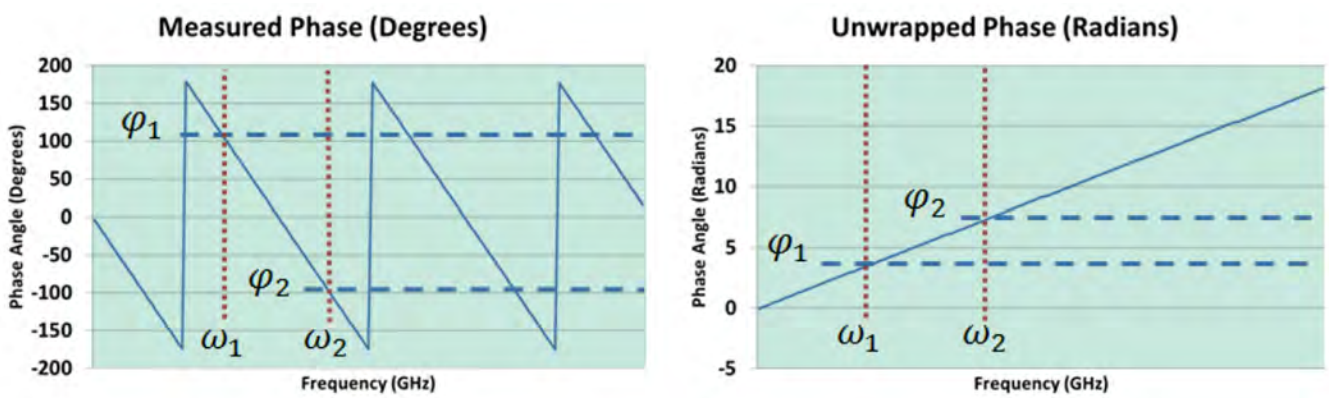


Figure 4: Wrapped vs. unwrapped phase for group delay calculation.

material's ε_r. Unlike other transmission line structures, half of the microstrip is exposed to free space with ε_r equal to that of air while the other half is in the circuit board material. The following equation is used to calculate ε_r using the effective dielectric constant when

$$\frac{h}{w} < 1,$$

the closed form analytical expression follows;

$$Relative\ Permittivity\ (\varepsilon_r) = \frac{1 + (2 * K_{eff} - 1) * \sqrt{1 + 12\frac{h}{w}}}{\sqrt{1 + 12\frac{h}{w}}}$$

where

$$h = Dielectric\ Thickness\ (\mu m),$$

and

$$w = Microstrip\ Conductor\ Line\ Width\ (\mu m).$$

The result is a calculated normal ε_r for the circuit board material at all frequencies of interest[8]. Unfortunately, this method for measuring normal permittivity does not directly yield a value for tan δ.

Microstrip Differential Phase Length ε_r

The microstrip differential phase length method is straight forward and (as the name implies) is the measurement of electrical phase differences for two microstrip transmission lines[9]. This method provides normal ε_r but does not directly provide normal tan δ. The measurement method requires only a VNA and a series of 50 Ohm microstrips of variable length.

Two lengths of microstrip were used for the measurements in this paper, one of six inches and the other of two inches; both were etched in close proximity to each other on the same panel to minimize geometric variations. Figure 5 illustrates the microstrip design and lengths used for this test.

In general, one of the microstrip lines should be measured using the VNA at a specific frequency. The phase angle of the energy traveling through the microstrip should be recorded. The other microstrip of a different physical length should then be measured and the phase angle of the energy should also be recorded. Calculation of the effective dielectric constant is simple using the following equations:

$$Phase\ Angle\ (\varphi) = \omega\left(\frac{\sqrt{K_{eff}}}{c}\right)L,$$

$$Phase\ Angle\ Difference\ (\Delta\varphi) = \omega\left(\frac{\sqrt{K_{eff}}}{c}\right)\Delta L,$$

$$Effective\ Dielectric\ Constant\ (K_{eff}) = \left(\frac{c\Delta\varphi}{\omega\Delta L}\right)^2,$$

where

$$L = Microstrip\ Length\ (m),$$

and

$$\Delta L = Difference\ in\ Microstrip\ Lengths\ (m).$$

Once the effective dielectric constant is calculated, ε_r is found by substituting the effective dielectric constant back into the equations under the group delay method, or by using a commercial transmission line calculator.

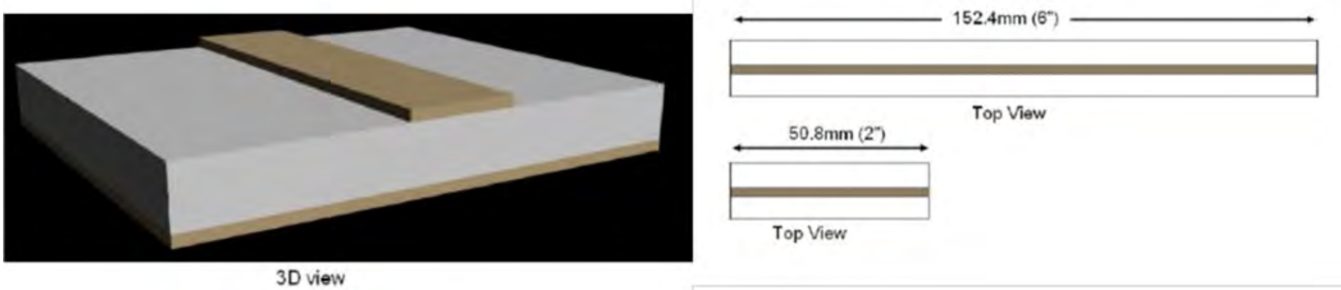


Figure 5: Microstrip design for differential phase length measurement.

This process is iterative and should be repeated for all frequencies of interest to build a ε_r versus frequency curve. In this effort this process was performed up to 110 GHz. Wideband circuit measurements at millimeter wave frequencies are very difficult to obtain accurately without building multiple designs and fine tuning for the frequencies of interest. Due to the lack of fine tuning in this study, some circuits demonstrated good wideband performance while others did not.

Free Space Quasi Optical Extraction of ε_r

The free space quasi optical method is perhaps the most intuitive way to measure the dielectric properties of materials, as the method consists of projecting a transverse electromagnetic (TEM) wave through the material under test and recording the transmitted and reflected energy. The method is defined as quasi optical because the size of the optical components is small with regard to the wavelength and the design requires use of geometric optics[10]. Despite this more obvious configuration, it is one of the most nontrivial due to the complicated mirror assemblies, frequency dependent beam size, and the non-ideal lossy mediums that are the unclad PCB materials under test. A typical configuration is presented in Figure 6.

The free-space quasi optical system utilizes a two-port VNA connected to two corrugated feed horn antennas specifically configured for a particular frequency band (K-Band or W-Band for example). The horn antennas point toward mirrors which shape the radiated beam pattern into a Gaussian beam reflected toward the unclad dielectric material under test. The antennas and mirrors are symmetric about the circuit board material under test. These methods evaluates the change in magnitude and phase of the transmission (S21) parameters, and can yield in plane ε_r and tan δ at frequencies within the band of interest. Note that any copper clad circuit board materials under test must have all copper removed before testing as this method only measures dielectric properties.

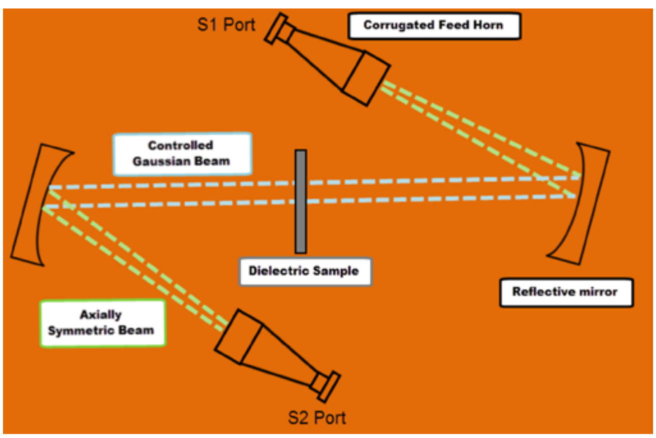


Figure 6: Quasi optical measurement system.

Calibrating the VNA for these measurements required the following steps:

1) Isolation: blocking the beam propagation path with a metal plate to account for diffraction effects at sample edges and multiple residual reflections from the antennas.

2) Reference: measuring the through transmission (S21) parameters without the material under test placed in the sample fixture to account for the permittivity contributions of air.

3) Time domain gating: mathematical elimination of multipath signals in time domain using the sum of the distance between the horn antennas and the dielectric sample (in this case +/- 2ns).

Circuit board materials in this test were measured from 40 GHz to 60 GHz using the presented setup. The measurements and calculations were accomplished with commercially available software and the resulting data is presented in the results section. ε_r was determined with relative ease but the determination of loss tangent was more difficult due to the thickness of the samples tested (~5 mil).

Perturbation of Resonant Cavities to Measure ε_r and tan δ

The cavity resonator method is widely used as a way of characterizing dielectric properties of circuit board materials at lower frequencies. The nature of resonant methods makes them particularly useful for measuring both permittivity and tan δ with relative ease. Collecting data and calculating ε_r is straight forward and requires only a suitable resonant cavity and a VNA. This method measures the in plane ε_r and

tan δ of a material under test by comparing the loaded (perturbed) and unloaded (unperturbed) resonant modes of a resonant cavity. The resonant frequency and quality factor will change with the loading of a resonant system with a dielectric material[8]. In order for the resonant cavity method to function, all circuit board samples must have all the copper cladding removed.

With the resonant cavity, measuring the ε_r and tan δ of a material is a quick and repeatable process. First, the resonant cavity must be connected to the VNA and the resonant frequencies and quality factors within the frequency band of interest must be mapped. Once this is accomplished the circuit material under test must be placed in the resonator and the resonant frequencies and quality factors must be mapped again.

Two different cavity resonant methods were implemented. The first was a rectangular waveguide cavity resonator, shown in Figure 7, which was used to characterize the dielectric properties of the circuit board materials up to 10 GHz.

Specifically, the waveguide resonator is setup with only enough space to fit the circuit board material sample between the two halves of the resonant cavity. This is done to allow for the material under test to be inserted and removed without disturbing the cavity dimensions. The cavity is designed to have six resonant modes at frequencies of approximately 2.2 GHz, 3.4 GHz, 5.0 GHz, 6.8 GHz, 8.6 GHz and 10.4 GHz. Data collection and processing is done through automated commercial software that interfaces directly with the VNA. It's important to note that the process was done twice for each sample, one with the sample in a vertical orientation and the other with the sample rotated 90 degrees in a horizontal orientation. This was done to determine if there are any differences in the in-plane permittivity and tan δ based on material orientation. The rectangular cavity has the advantage of being very simple and quick, but the precision of tan δ is limited to about 0.0005–0.001 since the resonator Q ranges between 2000–7000.

The second resonator was an open cavity, shown in Figure 8, which implements two concave spherical reflectors to create a concentric resonant cavity. This cavity was used to characterize the circuit board materials up to 40 GHz. The resonant mode frequencies are determined by the distance between the reflectors. Choosing the optimum cavity spacing requires some experimentation to minimize interfering modes across the range of

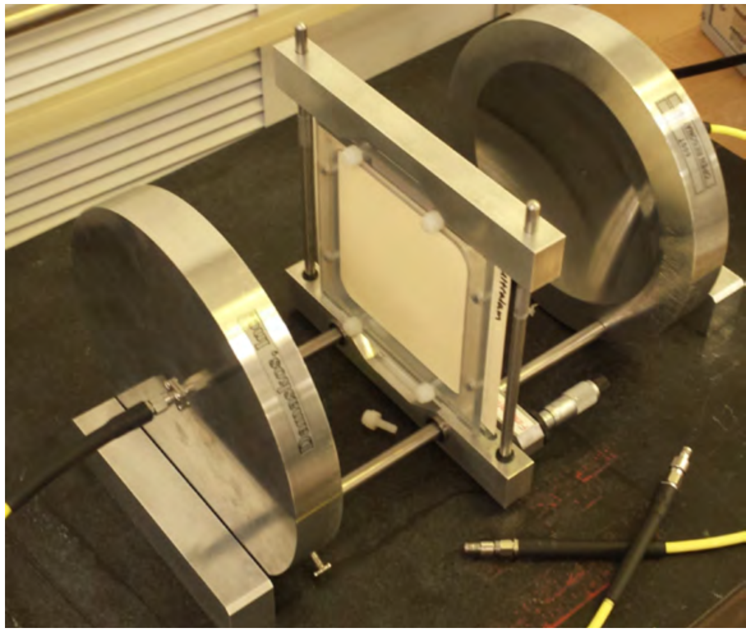


Figure 8: Open resonator.

Figure 7: Rectangular cavity resonator.

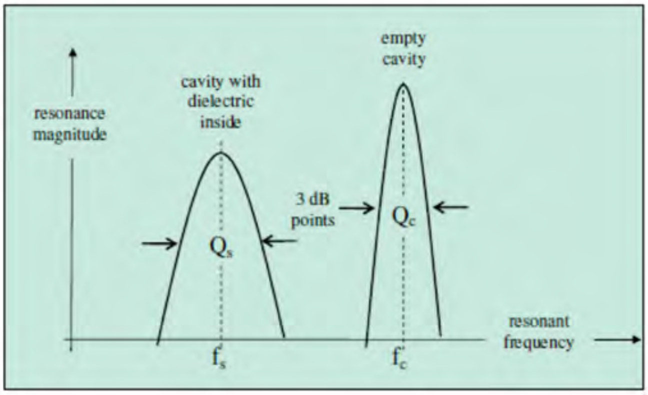


Figure 9: Illustration of resonant cavity method.

thickness and permittivity in the materials being measured. A configuration was chosen such that five resonances could be consistently and repeatedly measured. 26 GHz, 40 GHz, 49 GHz, 56 GHz, and 60 GHz were chosen. Data collection and processing is done through commercial software that interfaces directly with the VNA. In both cavities, the sample is placed in the middle and evaluated in both the vertical and horizontal orientation. The open resonator is capable of precision for tan δ measurement of about 0.0001 since the Q of the resonator is 50,000–100,000. The disadvantage of this technique is that it is quite tedious to perform and repeatability is limited by mechanical and ambient environmental stability that needs to be maintained for the fixture.

Figure 9 illustrates the overall resonant method concept. The higher quality factor (Qc) waveform is of the resonant cavity absent a circuit board material sample and the lower quality factor (Qs) waveform is of the same resonant cavity with a material under test present. The resonant frequency (fc) of the empty cavity is clearly shifted to a lower frequency (fs) and the quality factor (Qs) is clearly lower with a sample present. The resonant frequencies and bandwidths of the unloaded cavity and the loaded cavity should be measured and quality factor calculated for the frequencies of interest[12].

Once mapped, the equations below can be used to calculate ε_r and tan δ. These equations compare the differences in the resonant frequency and quality factor from the unloaded cavity to the cavity with a circuit board material present.

$$Relative\ Permittivity\ (\varepsilon_r) = \frac{\varepsilon}{\varepsilon_0} = \varepsilon_r' - j\varepsilon_r''$$

$$Loss\ Tangent\ (\tan\delta) = \left(\frac{\varepsilon_r''}{\varepsilon_r'}\right) = \frac{1}{Q}$$

where

$$Real\ Relative\ Permittivity\ (\varepsilon_r') = \frac{V_c(f_c - f_s)}{2V_s f_s} V_c + 1,$$

$$Imaginary\ Relative\ Permittivity\ (\varepsilon_r'') = \frac{V_c}{4V_s}\left(\frac{1}{Q_s} - \frac{1}{Q_c}\right),$$

$$Quality\ Factor\ of\ Unloaded\ Cavity\ (Q_c) = \frac{f_c}{\Delta f}$$

$$Quality\ Factor\ of\ Cavity\ with\ Sample\ (Q_s) = \frac{f_s}{\Delta f},$$

$$V_c = Volume\ of\ Cavity,$$

$$V_s = Volume\ of\ Sample,$$

$$f_c = resonant\ frequency\ of\ unloaded\ the\ cavity\ (Hz),$$

$$f_s = resonant\ frequency\ of\ the\ cavity\ with\ sampe\ (Hz),$$

and

$$\Delta f = f_{upper\ half\ power\ cutoff\ (3\ dB)} - f_{lower\ half\ power\ cutoff\ (3\ dB)}.$$

Split Post Dielectric Resonator (SPDR) to Measure ε_r and tan δ

The split post dielectric resonator, as seen in Figure 10, utilizes two circular dielectric resonators to measure ε_r and tan δ or a circuit board material. The method functions similarly to the previously described resonant cavities in that the unloaded quality factor (Qc) and resonant frequency (fc) of the resonator without a material sample is compared to the loaded cavities change in resonance quality factor (Qs) and shifted frequency (fs) with a material sample present. However, this method is different in that the Rayleigh-Ritz method is used to compute the resonant frequencies, the unloaded quality factors and all other parameters of the SPDR[13]. In this study, all calculations and measurements were accomplished with commercially available software and hardware.

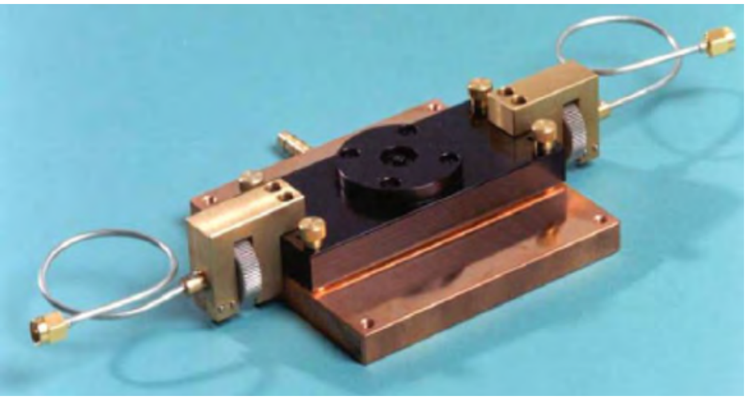


Figure 10: Split post dielectric resonator.

Figure 11 displays the cross section of the SPDR system. The two dielectric resonators are seen on top and bottom with the feed loops at the left and right. The cavity is setup such that the dielectric does not fill the entire cavity requiring that the air gap height (h_G) is greater than the sample height (h). The cavities unloaded resonant frequencies and quality factors are measured with an air gap of height $h_{G,}$ and the shifted resonant frequencies and quality factors are measured with the sample inserted within the fixture without adjusting this overall height.

As with other resonant methods, the dielectric characteristics can only be measured at certain fixed frequencies and the sample material must have all copper removed before testing. Additionally, the values of ε_r and tan δ are in plane with the material and not orthogonal. SPDR measurements were taken on all 10 samples at resonant frequencies of 10 GHz and 20 GHz.

Bereskin Clamped Embedded Stripline Resonator to Measure ε_r and tan δ

The Bereskin clamped imbedded stripline resonator test method operates from approximately 1 GHz up to 22 GHz. This resonant method, with a setup shown in Figure 12, operates through the use of aperture launched and received energy that excites the resonant modes in a copper strip clamped between two sheets of dielectric material under test. This method is similar to IPC-TM-650-2.5.5.5.1, Stripline Test for Complex Relative Permittivity of Circuit Board Materials to 14 GHz[14], but is more thoroughly explained in Dr. Bereskin's two patents[15,16]. This method has several pros, insomuch as it measures normal permittivity and tan δ directly. However, a downside is that air entrapped between the two dielectric layers creates measurement error due to localized variations in dielectric properties. The copper is removed from the dielectric prior to testing and the same copper strip is used in all the tests. The copper strip is stand-alone instead of being defined by etching in alternate stripline resonant methods. The specific test bed utilizes a signal generator and power meters, but a VNA can also be used if desired.

The output power from the resonator is received at the power meter connected opposite the signal source. Sweeping the signal source through all frequencies in the band and comparing variation in amplitude over frequency yields the resonant frequencies (fs) and quality factors (Qs) of the system. Unlike the other resonators the clamped embedded stripline

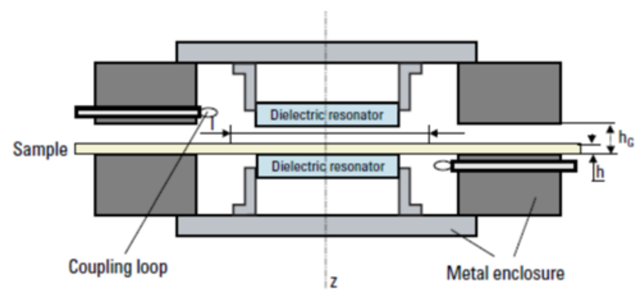


Figure 11: Split post dielectric resonator cross section.

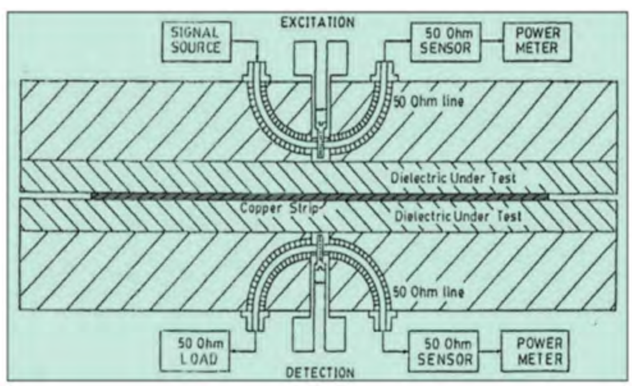
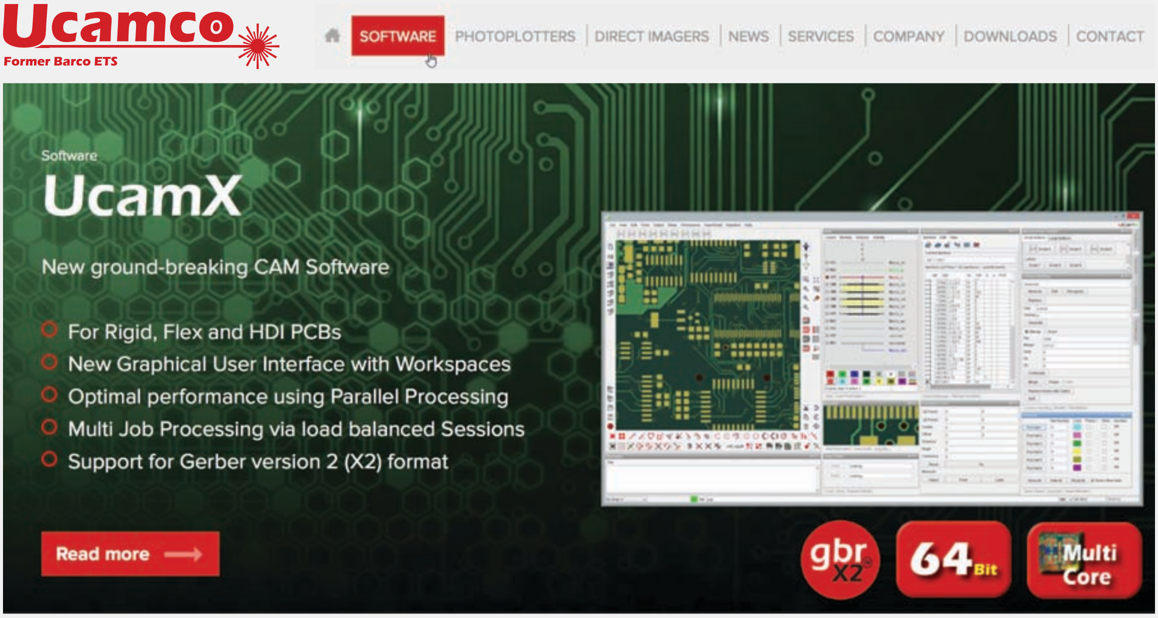
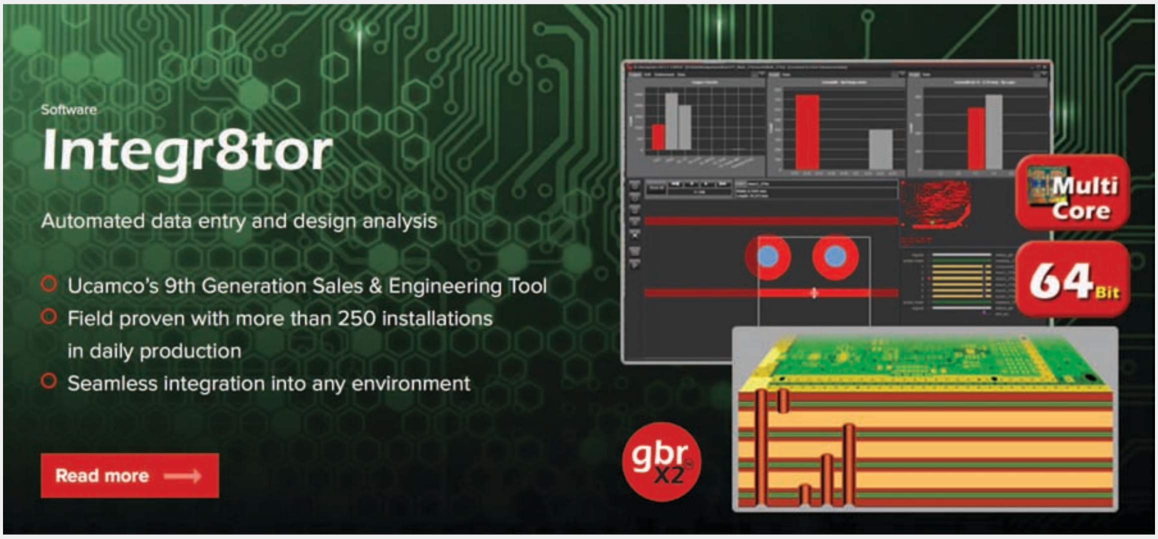
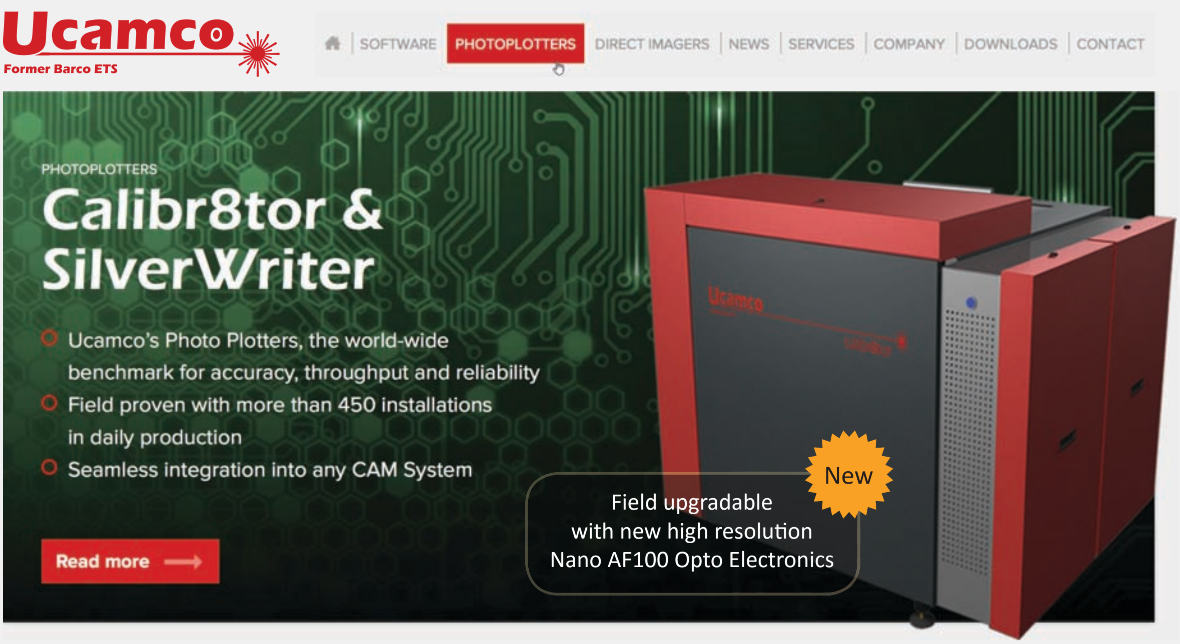


Figure 12: Clamped embedded stripline resonator.







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resonator does not work as a simple function of resonant frequency shifts from an unloaded to a loaded cavity. The resonator is a copper stripline and only functions with the material under test placed in the fixture therefore has no free space baseline for relative comparison. The basic calculations for ε_r and tan δ are shown in the following equations:

$$Relative\ Permittivity\ (\varepsilon_r) = \left(\frac{c}{2.54 f_s (L + \Delta L)}\right)^2$$

where

$$c = 3x10^8 \left(\frac{meters}{second}\right)$$

$$f_s = resonant\ frequencies L = physical\ length\ of\ resonator\ copper\ strip\ (meters)$$

$$\Delta L = effective\ increase\ in\ resonator\ length\ from\ fringing\ field\ (meters);$$

and

$$Loss\ Tangent\ (\tan\delta) = \frac{1}{Q_s} - \frac{1}{Q_c},$$

where

$$Q_s = Quality\ Factor\ of\ the\ Cavity\ with\ Sample$$

and

$$Q_c = Quality\ Factor\ of\ the\ Unloaded\ Cavity.$$

The quality factor of the cavity with sample (Q_s) is easily calculated using the above equations and the measured resonator values. However, the quality factor of the unloaded cavity (Q_c) is not so readily determined. The analytical approach is detailed in IPC-TM-650-2.5.5.5.1 as is the method for calculating the effective increase in resonator length from fringing field.

This study considered nine, and in some instances 10, resonant frequencies in the 1 GHz to 22 GHz band. The measured values of ε_r and tan δ were obtained for each sample and were averaged for comparison. The dielectric under test is presumed to be a single block on either side of the copper strip. Generally 60 mils [1.524 mm] is preferred as in IPC-TM-650 2.5.5.5. In this case, 5 mil [0.127 mm] material was supplied and stacked so the resulting ε_r values are skewed lower due to entrapped air from inconsistent thicknesses and embedded copper surface roughness pockets associated with cladding removal. **PCB**

Editors note: Due to the length of this article, we have chosen to publish the Results, Conclusion, Acknowledgements and References at this location.

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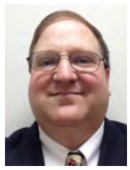

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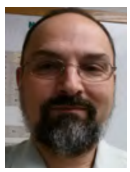

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The Quiet Mainstreaming of HDI Manufacturing

by Chris Ryder, ESI | Feb. 2016, I-Connect007

Although design engineers have driven the evolution of the current class of mobile devices, primarily through addressing market demand for new form factor innovation, the push to meet the associated manufacturing challenges has been responsible for a revolution in PCB manufacturing.

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Test & Measurement: *The Case for Validation*

by Todd Kolmodin
GARDIEN SERVICES USA

Test and measurement (T&M) are terms that can strike fear into the most robust of minds. Many engineers create designs and products of the future with specific results predicted for performance. Guaranteeing those predicted results requires specific tests and measurements. Although breadboards with ICs, jumpers and handheld meters still exist, the products of today require much more validation than any of the preceding examples can provide. Validating characteristics such as inductance, capacitance, buried passives, high voltage, dielectric breakdown, and Z-axis isolation (IR) are examples of electrical validation required. Along with that come validations of board thickness, plating quality across many aspect ratios, line width and space, hole diameters, surface finish, screening and even packaging. Whew! That is a lot to take into consideration in the market of today.

So how do the experts guarantee that your product will meet or exceed the expectations you have put forth? Through test and measurement of course. (Well along with a bit of fairy dust, mad skills and voodoo magic!) In all seriousness, test and measurement tools and equipment gets the job done efficiently, accurately and as expeditiously as possible.

Mechanical

This term can be used to define processes that mechanically change the state of the PCB. These are processes such as drilling, routing, lamination, milling, and beveling. Test and measurement play a large part in these processes as well. This is sometimes overlooked when thinking of T&M. Much of the inspection in these processes remains manual but there are automated alternatives available. Automated visual inspection (AVI) technology has advanced quite a bit in recent years. This is not to be confused with historic AOI, which is used for scanning cores or innerlayers. AVI in the current world can scan the finished board and validate a wide variety of variables. Missing silk screen or legend, metal inclusions, exposed copper, dishdowns, contamination, and soldermask violations are just a few.

Wet Process/Plating

Another variety of tests and measurements is required during these processes. Chemistry validation, material inspections and hole plating validation are all common here. Although required, the standard cross section of the plated hole is not the only validation for copper in the barrels. The electrical 4-wire Kelvin test is becoming a more common requirement in todays' builds. This test will detect finite changes in the resistive value of the copper in the barrel.

Figure 1: AVI tester.

Changes in the milliohm range can flag a potential defective barrel early in the process and remove the defective image/panel from further process, thus stopping a potential latent defect or field failure. The standard cross-section is a random sampling of a hole set and just cannot predict the possibility of a plugged hole or debris-entrapped anomaly that will cause a random defect even though the majority sampling of the panel reports acceptable criteria. 4-wire Kelvin is mainly provided by the flying probe test equipment available today.

Electrical Validation

Here is where many validations of the product take place. Here, terms such as TDR, IR, hipot, continuity and passive validation are common. Let's look at these one by one.

Time domain reflectometry or TDR is a measurement technique used to determine the characteristics of a line by observing reflected waveforms. The analysis is comprised of injecting a step or impulse of energy into the sample and observing the reflected waveform. Many shops incorporate a coupon in the panel for this purpose. Terms like stripline and buried stripline are common. These are usually but not always a resistive load. With a resistive load, when the signal or step is applied the resulting waveform is expressed in resistance. Common requirements of characteristic impedance are values in the 50-ohm range as measured on the reflectometer.

Insulation resistancetesting or IR testing is a test of dielectric integrity. Somewhat similar to the standard hipot or dielectric breakdown test, the IR test has a specific requirement of the insulation. This is very common when measuring insulation between shields and cores. This applies a voltage to the shield and measures the resistance from the adjacent core. This requirement is usually in the megaohm range. This value can be captured and reported as an acceptance criteria.

Dielectric breakdown or hipot is another test of the dielectric material separating cores. Similar to the IR test, the hipot test applies a ramped test voltage of a period of time and holds (dwells) at that voltage for a specific time. Any unacceptable current leakage during that time results in an immediate shutdown of the test and a fault is reported. Unlike the IR test, this is a "go/no-go" test. The only thing known is that an unacceptable current path exists between the nodes tested. The specific resistance is not reported. This test is mainly used to identify manufacturing defects rather than validate a specific insulation requirement.

4-wire Kelvin or low-resistance testing is a test designed to identify minute changes in resistance specifically to plated holes or vias. As with common continuity tests that have thresholds from 5–20 ohms, the 4-wire Kelvin measures for fluctuations in the milliohm range. Usually with this test the vias with the highest aspect ratio are selected. Aspect ratio (AR) is defined as hole size/board thickness. For example, 0.0098/0.062 = 0.158 or 15.8:1 AR. The sample is tested and a master value set is created. Subsequent boards are then tested and compared to the master. Any fluctuations outside of the acceptable control limits are reported as faults. Anomalies such as thin copper or tapered plating are captured with this test. Defects such as these will not be captured during a standard continuity test with thresholds between 5–20 ohms.

Buried passive testing validates buried or electrical components built into the board structure. Most common are the buried resistors. Today's market mainly uses a resistive material buried in the PCB where areas are etched away leaving a predetermined resistive characteristic or component on the given net. These values are predictable and can be measured and catalogued. The most common method today is by use of the flying probe. When the values are known, this can be programmed into the netlist

Figure 2: HiPot/IR tester.

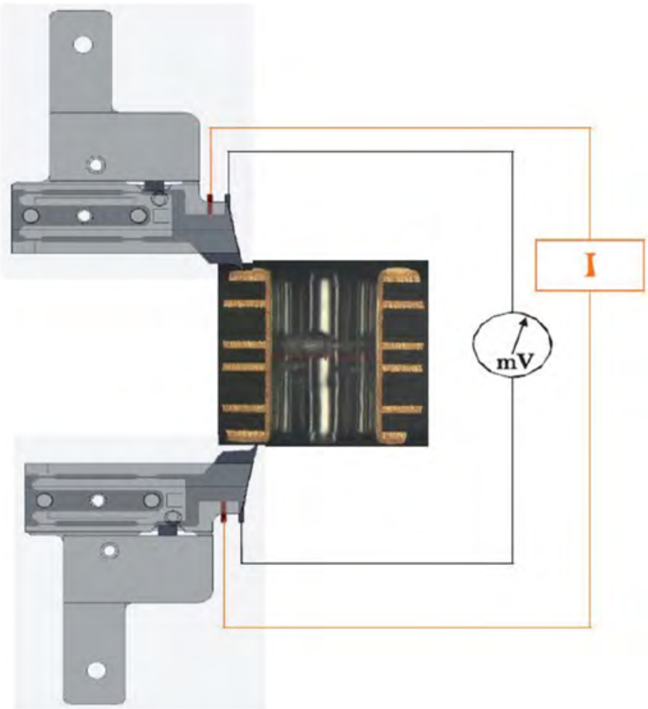


Figure 3: 4-wire Kelvin testing.

Figure 4: Flying probe tester.

Figure 5: Fixture tester.

and the test can validate these components, allowing for allowable manufacturing tolerances. The flying probe can perform this test exclusively or validate the resistors while also performing the standard continuity and isolation test.

Continuity test is a test for integrity of connection within any given node or net. A voltage is applied to one end of the net and a resistive reading is taken at the endpoints of the net. A threshold variable is monitored and any value outside that variable is reported as a fault. This threshold is expressed in ohms. Standard requirements for this variable are 5–20 ohms depending on the performance class. This test can be performed by fixture testers or flying probes.

Discontinuity or shorts testing is designed to find short circuits between individual nodes or nets. Here is where there is a difference between the fixture testers and flying probes as to how this test is performed. In the fixture testers it is a full parametric test where a voltage is applied to all nets simultaneously and each individual net is monitored for leakage to any other net. A leak encountered outside of the resistive threshold is reported as a fault. This threshold value commonly is between two and 100 megaohm. Now, with the flying probes the test is performed a bit differently. This is where you hear the term “adjacency.” The term adjacency means that only nets “adjacent” to the primary net being tested are monitored for discontinuity or shorts. This adjacency window is defined by the CAM system. This window is commonly 0.050 inches or 50 mils.

Flying Probe Direct vs Indirect Test

As mentioned earlier, with flying probes they test a bit differently than the fixture testers. The adjacency test for shorts has been covered above. Now, there are two modes to the flying probe that should be discussed, as there can be some confusion. The flying probe tester operates in two distinctive modes—direct and indirect. With direct testing the flying probe provides a full resistive test on every board. This includes continuity and discontinuity (within the adjacency window). Test time can be very easily calculated, as every board will take the same amount of time to test. All nets are screened against the continuity and discontinuity thresholds.

With indirect testing, also known as indirect testing by signature comparison, the method changes. With this method the first board goes through what is called a capacitive or discharge gather. These values are stored as a temporary master. The board then receives a direct test to validate the board against the design requirements. When the board completes and passes, the capacitive values are committed as the discharge or capacitive master. Now here is the big difference between indirect and direct: The second board receives the same capacitive or discharge gather, but once that test is complete, those values are compared to the master. ONLY those readings that are outside the capacitive master threshold are retested in direct or resistive mode. If the values of the second tested board are all within tolerance to the capacitive master the board will pass with no resistive retesting whatsoever. In this test method is how the flying probes develop their speed of test.

There is quite a gambit of tools in the T&M world to provide validation to your PCB. I know I have only touched on some highlights of all the test and measurement requirements in the field. There are other tests and tools necessary. My goal was to highlight some major specifics in the T&M theatre so the next time when you are wondering what some tests are all about and how they work you will have some background information to help. **PCB**

Todd Kolmodin is the vice president of quality for Gardien Services USA, and an expert in electrical test and reliability issues. To read past columns, or to contact Kolmodin, click here.

Turn Your Smartphone into Any Kind of Sensor

It started when NASA answered a call for a tool to detect dangerous gases and chemicals with a smartphone. The result became a smartphone-linked device that can do just about anything someone can build a sensor for.

When the Department of Homeland Security (DHS) put out its request in 2007, NASA Ames Research Center scientist Jing Li already had a sensor that reacted to various gases and compounds—she'd been working on it for space applications, like evaluating atmospheres on other planets.

Li needed a way for the device to "sniff" the air for samples and a system that would allow it to interface with a smartphone. Li's team settled on a small fan to gather the air samples, and approached George Yu of Genel Systems Inc., who was able to deliver the cell phone interface system.

Building on the system he developed with NASA, Yu created his NODE platform—a cylinder not much bigger than a thumb that can transmit data from sensors to a smartphone or other smart device or store it to be uploaded to any computer. Unlike the sensor developed for DHS, NODE operates independently of the cell phone and transmits the data it gathers using Bluetooth wireless technology.

"Using a common platform for multiple sensor modules, you save a lot of money," Yu says.

The product line went on the market in 2012, and by summer of 2014 it was already in its second generation, NODE+, which Yu says is faster, uses less power, is more durable.

Electronics Industry News
Market Highlights

Engineers Take First Step toward Flexible, Wearable, Tricorder-like Device

Engineers at University of California San Diego have developed the first flexible wearable device capable of monitoring both biochemical and electric signals in the human body. The Chem-Phys patch records EKG heart signals and tracks levels of lactate, a biochemical that is a marker of physical effort, in real time.

Fast, Stretchy Circuits Could Yield New Wave of Wearable Electronics

Fabricated in interlocking segments like a 3D puzzle, the new integrated circuits could be used in wearable electronics that adhere to the skin like temporary tattoos. Because the circuits increase wireless speed, these systems could allow health care staff to monitor patients remotely, without the use of cables and cords.

Flight of the RoboBee

One of the more unexpected robotics applications in recent years comes from the National Science Foundation (NSF)-supported "RoboBees" project, which aims to create autonomous robotic insects capable of sustained, independent flight.

The Inverter Industry in China: Local Players are Gradually Becoming Unavoidable

Chinese players have become leaders in diverse inverter market segments, forcing foreign players to collaborate with each other. The rail traction leader was created by the merger of CSR and CNR to form CRRC, which controls more than 40% of the market.

Discovery Could Energize Development of Longer-Lasting Batteries

A UT Dallas researcher has made a discovery that could open the door to cellphone and car batteries that last five times longer than current ones.

Over 8 Billion Connected Devices Globally

The current IHS Technology Connected Device Market Monitor report examines key trends and data for global devices, over the top (OTT) and pay TV multiscreen markets.

International Partners Provide Science Satellites for America's SLS Maiden Flight

NASA's new Space Launch System (SLS) will launch America into a new era of exploration to destinations beyond Earth's orbit. On its first flight, NASA will demonstrate the rocket's heavy-lift capability and send a crewless Orion spacecraft into deep space.

Graphene-based Transparent Electrodes for Highly-Efficient Flexible OLEDs

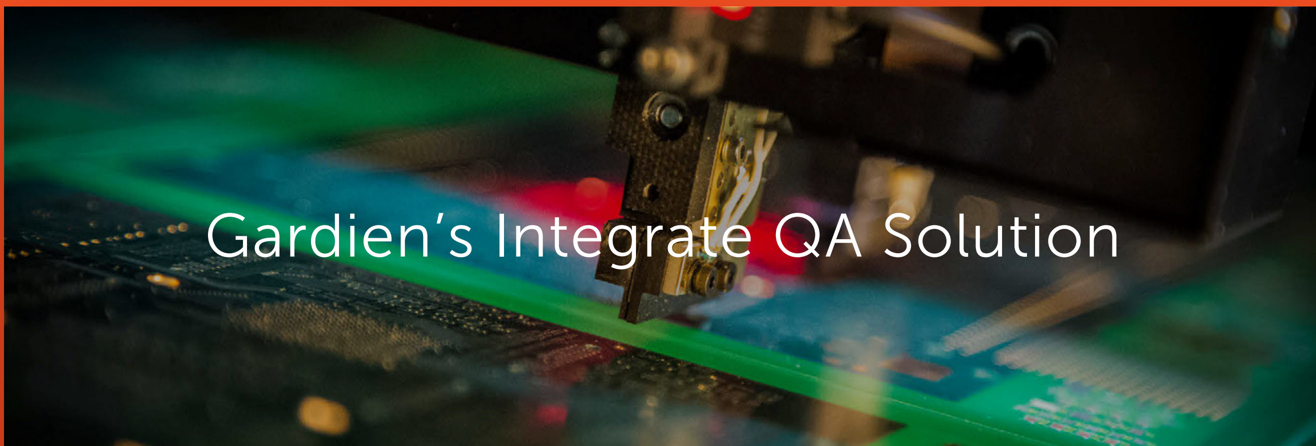
The arrival of a thin and lightweight computer that even rolls up like a piece of paper will not be in the far distant future. Flexible organic light-emitting diodes (OLEDs), built upon a plastic substrate, have received greater attention lately for their use in next-generation displays that can be bent or rolled while still operating.

Better Combustion for Power Generation

In the United States, the use of natural gas for electricity generation continues to grow. The driving forces behind this development? A boom in domestic natural gas production, historically low prices, and increased scrutiny over fossil fuels' carbon emissions.

Tiny Lasers Enable Next-Gen Microprocessors to Run Faster, be Less Power-Hungry

A group of scientists from Hong Kong University of Science and Technology, University of California, Santa Barbara, Sandia National Laboratories, and Harvard University were able to fabricate tiny lasers directly on silicon—a huge breakthrough for the semiconductor industry and well beyond.



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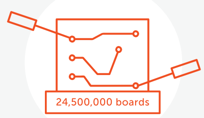

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Using the Type 1 Gauge Study to Assess Measurement Capability

by Patrick Valentine
UYEMURA USA

Measurement capability is a critical aspect of ensuring product quality, therefore a measurement system must be assessed before being used on products. Understanding how to assess measurement capability becomes critical. The Type 1 Gauge study is typically the first step in a measurement system analysis program. Type 1 Gauge parameters are explained, and a worked example using electroless nickel immersion gold (ENIG) is provided.

What Does the Type 1 Gauge Study Do?

There are two major types of measurement system variation:

1. Accuracy is variation between the measurement and a true or reference value
2. Precision is variation between repeated measurements

A Type 1 Gauge study involves repeated measurements of one sample by one gauge and by one operator. With this information, the Type 1 Gauge study provides an assessment of the following:

1. Accuracy, assuming a reference value is available
2. Precision of repeated measurements

Without an accepted reference value, the Type 1 Gauge study only measures precision, and accuracy becomes unavailable. Bias is a quantitative term used to describe accuracy. Bias is the difference between the average of measurements made on the reference value and its true value.

A Type 1 Gauge study considers only the inherent variation of the gauge itself. A Type 1 Gauge study isolates the effects of accuracy and precision, and evaluates the capability of the gauge to make accurate measurements with acceptable variability. A Type 1 Gauge study does not assess operator-to-operator or gauge-to-gauge variation. A more complex gauge repeatability and reproducibility (R&R) study is indicated for a more comprehensive measurement system analysis.

Gauge resolution is the gauge's smallest increments of measure. For the Type 1 Gauge

study, the resolution of the gauge should be less than or equal to 5% of the tolerance.

Reference Value

The reference value is the known and correct measurement associated with a standard or part. It serves as a master value for comparison during the Type 1 Gauge study. Reference values can be determined in several ways depending on industry standards and company and customer expectations. The preferred reference values are either:

- Standards traceable to NIST or equivalent
- Values agreed upon by the affected parties (AABUS)

If no appropriate standard is available, a production part should be calibrated and marked as a standard. Preferred methods of establishing a reference value from a production part include:

- Average of repeated measurements from a more accurate measuring gauge
- Focused ion beam (FIB) analysis and measurements after the gauge study is completed

In either case, the standard or production part used as the reference value must meet the following criteria:

- Permit an unambiguous result of measurement
- Be stable over a long period of time
- Have the same characteristics as the parts to be subsequently measured with the gauge
- Conform to qualitatively higher standards:
  - Calibration uncertainty (U_{cal}) must be significantly less than 10% of the difference between upper and lower specification limits, so that $C_{gk} \geq 1.33$ can be attained[1,2].
    - U_{cal} is the margin of error that exists about the results of the reference value. In colloquial terms, this would be expressed as "give or take." For example, an EN standard might be 150 micro-inches thick "give or take 3 micro-inches."
    - Two numbers are needed to quantify U_{cal}[3]:
      - Interval—the "give or take" margin
      - Confidence—how sure we are that the 'true value' is within the margin
      - In the EN example above: 150 micro-inches, ± 3 micro-inches at a level of confidence of 95%
  - Reference value intervals need to be known, preferably at 95% confidence

The reference value should be as close as possible to the center of the specification limit for the characteristic you are measuring. Ideally, the reference value should be within 10% of the center value of the specification limit. At a minimum, the reference value needs to be within the specification limit.

Tolerance Value

Always consult current standards for current specifications. The specifications cited here are example values only. IPC-4552A Performance Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards lists the following values for plated thicknesses:

Nickel:
Maximum: 236.2 micro-inches
Minimum: 118.1 micro-inches

Gold:
Maximum: 3.94 micro-inches @ +4σ
Minimum: 1.57 micro-inches @ -4σ

Tolerance values are calculated as follows:

Nickel: (236.2 - 118.1) = 118.1 micro-inches
Gold: (3.94 - 1.57) = 2.37 micro-inches

Opening up the specification limits would artificially inflate C_g & C_{gk} without ever improving the gauge itself. Generally, it's a bad idea to let the process or the measurement instrument dictate the tolerance[4]. Nevertheless, increasing the tolerance range and keeping the study variation (K) of the gauge fixed, does imply that measurement uncertainty takes a smaller chunk of the tolerance range, which is in fact indicative of better performance of the gauge[5].

Method

At one or more defined measurement points the reference standard is measured at least 25 times under repeatable conditions (one operator, normal production measurement conditions).

Statistical software is generally used to analyze the data. Capability indices are calculated:

- The capability of the gauge is given by:

$$C_g = \frac{(K/100\% * \text{Tolerance})}{SV}$$

Where:
K = percent of the tolerance for calculating C_g, default = 20%
Tolerance = USL - LSL
SV = study variation given by the standard deviation (n – 1 formula) of the n measurements multiplied by 6

- The capability of the gauge, considering both the gauge accuracy and precision is given by:

$$C_{gk} = \frac{(K/200\% * \text{Tolerance}) - |X - X_m|}{SV/2}$$

Where:
K = percent of the tolerance for calculating C_g, default = 20%
Tolerance = USL - LSL
X = mean of n measurements
X_m = reference measurement
SV = study variation given by the standard deviation (n – 1 formula) of the n measurements multiplied by 6

The default value of K = 20% has been used for several decades. Any positive value can be used if it meets the requirement 0< K< 100. Using values between 10% and 20% is common. The K = 20% is considered the "golden rule", and asserts that the measurement uncertainty (U_{mea}) should ideally amount to at the most one tenth of the tolerance[6]. Measurement uncertainty (U_{mea}) is the margin of error that that exists about the results of the reference value.

At the time this rule was formulated, it was considered that if it was adhered to the measurement uncertainty could be ignored. This is still widespread today. If measurement uncertainty is of specific concern with tighter specification tolerances, then values closer to K = 10% are recommended.

The assumed "width" of the measurement system distribution is 6. Hence the default value for study variation is 6σ, which contains approximately 99.73% of the values. The Automotive Industry Action Group (AIAG) recommends the use of 6σ in gauge R&R studies[1]. Some companies use 5.15σ which contains approximately 99% of the values[7]. Using 5.15σ is conditional AABUS.

Minimum acceptable capability indices[8]:

Cg	> 1.00
Cgk	> 1.00

Preferred acceptable capability indices[2]:

Cg	≥ 1.33
Cgk	≥ 1.33

Example

NIST traceable standards of electroless nickel immersion gold are used. Calibration uncertainty, gauge resolution, measurements, analysis, and capability indices are computed.

Calibration Uncertainty:

Standard:	180.00 micro-inches
Uncertainty:	3.15 micro-inches
Confidence:	95%
Nickel tolerance:	118.10 micro-inches
Significantly less than 10%:	(3.15/118.10) = 2.7%

Standard:	2.60 micro-inches
Uncertainty:	0.05 micro-inches
Confidence:	95%
Gold tolerance:	2.37 micro-inches
Significantly less than 10%:	(0.05/2.37) = 2.1%

Gauge Resolution Analysis:

Resolution:	0.01 micro-inches
Nickel tolerance:	118.10 micro-inches
Less than or equal to 5%:	(0.01/118.10) = 0.008%

Resolution:	0.01 micro-inches
Gold tolerance:	2.37 micro-inches
Less than or equal to 5%:	(0.01/2.37) = 0.42%

Electroless Nickel				
181.91	180.74	178.06	183.39	178.32
182.60	183.53	183.12	180.11	184.81
178.63	181.76	178.93	181.41	184.42
176.04	183.40	179.22	182.22	176.96
176.00	175.84	182.23	181.47	178.26

Immersion Gold				
2.69	2.54	2.67	2.64	2.68
2.57	2.66	2.49	2.56	2.73
2.58	2.65	2.70	2.67	2.56
2.65	2.70	2.56	2.68	2.58
2.65	2.56	2.54	2.62	2.63

	EN	IG
Measurements Average:	180.54	2.62
Standard Deviation:	2.742	0.063

Table 1: Results of the 25 ENIG standards measurements.

At one or more defined measurement points the reference standards are measured 25 times under repeatable conditions (one operator, normal production measurement conditions). Results are shown in Table 1.

Capability Indices:
Capability of the gauge:

Nickel $$C_g = \frac{(20\% / 100\% * 118.10)}{(2.742 * 6)} = 1.44$$

Gold $$C_g = \frac{(20\% / 100\% * 2.37)}{(0.063 * 6)} = 1.25$$

Capability of the gauge, considering both the gauge accuracy and precision:

Nickel:
$$C_{gk} = \frac{(20\% / 200\% * 118.10) - |180.54 - 180.00|}{((2.742 * 6) / 2)} = 1.37$$

Gold:
$$C_{gk} = \frac{(20\% / 200\% * 2.37) - |2.62 - 2.60|}{((0.063 * 6) / 2)} = 1.15$$

Results

Gauge meets minimal acceptable capability indices of 1.00. Improvements should be made to achieve preferred capability indices of 1.33.

Conclusion

Assessing measurement capability is the first step in process control. The Type 1 Gauge study is an excellent technique for doing this. The ease of use and interpretation of results has been presented in this paper. Once measurement capability is demonstrated, the process engineer and quality manager can systematically attack and reduce product variation. Variation reduction is evidence of improved process control, and improved product reliability. **PCB**

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A Thermal Conductivity Measurement Method, Adapted to Composite Materials Used in the PCB Industry

by François Lechleiter, CIMULEC GROUP
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Abstract

Most of today's printed circuit board base materials are anisotropic and it is not possible to use a simple method to measure thermal conductivity along the different axes, especially when a good accuracy is expected. Few base material suppliers' datasheets show X, Y and Z thermal conductivities. In most cases, a single value is given, moreover determined with a generic methodology, and not necessarily adapted to the reality of glass-reinforced composites with a strong anisotropy.

After reminding the fundamentals in thermal science, this paper gives a short overview of the state-of the art in terms of thermal conductivity measurement on PCB base materials, and some typical values. It finally proposes an innovative method called transient fin method, and associated test sample, to perform reliable and consistent in-plane thermal conductivity measurement on anisotropic PCB base materials.

Introduction

Observed on a long enough time scale, electronic systems behave like living species; they obey the laws of evolution. To be successful, they have to adapt to their environment, which means to market requirements, and thus to consumer expectations. Any system with a new, more powerful functionality naturally surpasses the previous generation. As consumers, we normally prefer smaller, lighter, faster, more reliable and cheaper electronic systems. This has led the electronic industry since its beginning.

The PCB progressively becomes a little bit more than just the backbone of electronic systems. At the beginning, the printed circuit board was providing essentially an electrical function, by interconnecting electrically components together, and a mechanical function, by supporting mechanically the components and holding them into a defined volume. Progressively, evolution towards microwave applications brought electromagnetic functionalities to the PCB. In addition, the constant increase of power density made the PCB more and more capable of providing solutions for efficient thermal management strategy.

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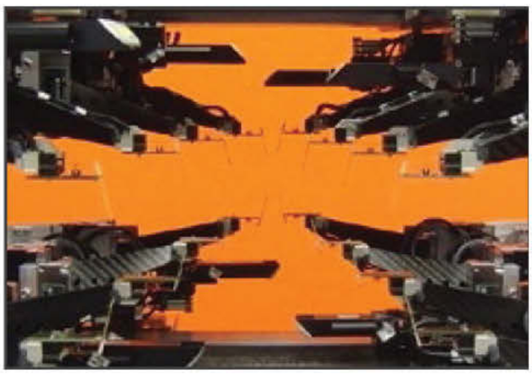

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Heat transfer is the exchange of thermal energy between physical systems. It always occurs from a region of high temperature to another region of lower temperature. The fundamental modes of heat transfer are conduction, convection and radiation. In a PCB, the predominant mode is conduction, for which thermal conductivity of the material is a good indicator. Therefore, to accompany PCB evolution, base material suppliers improved the thermal conductivity of their laminates and prepregs. Early PCBs were made of bakelite, having around 0.2 $W.m^{-1}.K^{-1}$ thermal conductivity. Nowadays, it is possible to find dielectric materials compliant with printed circuit board manufacturing process and product specifications exhibiting a higher thermal conductivity, typically in the range of 2 $W.m^{-1}.K^{-1}$, when copper is almost 400 $W.m^{-1}.K^{-1}$.

Nowadays, most of the critical parameters of PCBs have reached some limits. Improving the overall performances of the electronic system often means to look for some percent. This is true for PCB thickness, via size, copper thickness, or etched features. This is also true for thermal behavior. Designers are looking for some Celsius for the system operating temperature. In this context, it becomes more and more important to have reliable thermal models, and therefore to feed these models with consistent physical properties, including thermal conductivity.

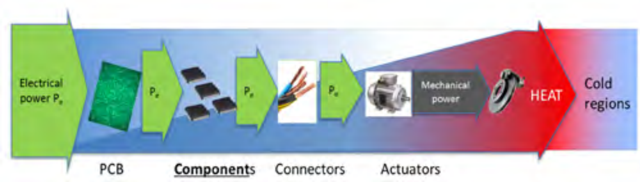
Many methods exist to measure thermal conductivity. Most of them are adapted to isotropic and homogeneous materials, but there is not one single easy method to measure thermal conductivity of composite anisotropic materials, especially dielectrics used in the printed circuit board industry. Therefore, this paper aims at proposing a method for consistent and reliable thermal conductivity measurement, adapted to anisotropic dielectric materials.

Thermal Science Fundamentals

To understand how to optimize thermal efficiency of a PCB, and why thermal conductivity of dielectric materials is important, this section gives an overview of some aspects of thermal science.

Standard physic model says that heat propagates according to three modes: conduction, convection and radiation. Heat transfer always occur from hottest region to coolest region.

The first law of thermodynamics says that the total *quantity* of energy in the universe remains constant. This is the principle of the conservation of energy. The second law of thermodynamics states that the *quality* of this energy is degraded irreversibly. This is the principle of the degradation of energy, and systems powered by electricity respect these laws.



Heat is generated all along the chain. At electronic system level, the main contributors are often components. The printed circuit board, supporting and interconnecting them, is also very helpful to avoid their excessive heating. Indeed, excessive temperatures degrade overall system performance, from speed to long term reliability. Therefore, electronic system designers take great care of operating temperatures. Equations managing thermal exchanges can be easily found in the literature.

Thermal Management of a PCB

A multilayer PCB is usually a sandwich mixing copper and glass-reinforced composites. This is an environment where the predominant heat transfer mode is conduction. Inside the material, convection and radiation can be neglected. To optimize thermal efficiency of a PCB, it is therefore important to maximize heat conduction.

In physics, thermal conductivity is the property of a material to conduct heat. It is evaluated primarily in terms of Fourier's Law for heat conduction. Heat transfer occurs at a lower rate across materials of low thermal conductivity than across materials of high thermal conductivity. This is why high thermal conductivity materials are preferred for heat sink applications, while materials of low thermal conductivity are used for thermal insulation.

Using dielectric materials having a high thermal conductivity to build a PCB will make the whole structure more thermally conductive, and will help to transfer heat generated by the components to a colder region. This is generally the strategy to maintain both the PCB and the components to an acceptable operating temperature. Thermal conductivity is probably the most interesting characteristic, when it is about to compare different base materials in order to optimize a printed circuit board thermal management, or simply to assess the operating temperature of a system. This is why suppliers indicate usually thermal conductivity properties in their dielectric base materials' datasheets.

There are a number of possible ways to measure thermal conductivity, each of them suitable for a limited range of materials, depending on the thermal properties and the medium temperature. Two classes of methods exist to measure the thermal conductivity of a sample: steady state and non-steady-state (or transient) methods. In general, steady-state techniques perform a measurement when the temperature of the material measured does not change with time. The transient techniques perform a measurement during the process of heating up.

Thermal Diffusivity

In heat transfer analysis, thermal diffusivity is the thermal conductivity divided by density and specific heat capacity at constant pressure. It measures the ability of a material to conduct thermal energy relative to its ability to store thermal energy.

In a material with high thermal diffusivity, heat moves rapidly through it, because the material conducts heat quickly relative to its volumetric heat capacity or 'thermal bulk.' It characterizes the heat propagation velocity in a material, without information on its intensity.

Thermal diffusivity is often measured with the flash method (this is the case for ASTM E1461 and IPC-TM-650-2-4-50). It involves heating a strip or cylindrical sample with a short energy pulse at one end and analyzing the temperature change (reduction in amplitude and phase shift of the pulse) a short distance away. Thermal diffusivity is usually denoted . The following formula explains the relationship between thermal conductivity λ, the density ρ, and the specific heat C_p.

$$a = \frac{\lambda}{\rho C_p}$$

Where
a: thermal diffusivity ($m^2.s^{-1}$)
λ: thermal conductivity ($W.m^{-1}.K^{-1}$)
ρ: density ($kg.m^{-3}$)
Cp: specific heat capacity ($J.kg^{-1}.K^{-1}$)
NB: ρCp is called volumetric heat capacity ($J.m^{-3}.K^{-1}$). When ρCp is known, measuring thermal diffusivity is very interesting to assess thermal conductivity.

Current PCB Base Material Thermal Conductivity Measurement Situation

There are a number of possible ways to measure thermal conductivity, each of them suitable for a limited range of materials, depending on the thermal properties and the medium temperature. Every field of application, from building to semiconductor industry have its own nature of materials, performance expectations, and range of temperatures. Most of printed circuit board materials are made of woven glass-fiber impregnated with resin. Glass and resin do not have the same properties. Therefore, thermal conductivity in the XY plan (along the glass fibers) cannot be the same as thermal conductivity along the Z-axis (thickness of the PCB).

Glass E	1
Standard epoxy	0,2 to 0,3
Copper	390

Table 1: Thermal conductivities of normal PCB base materials main components (orders of magnitude, $W.m^{-1}.K^{-1}$).

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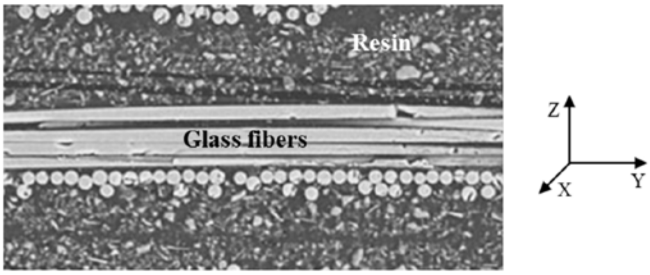

Figure 1: Thermal transfer representation in a glass-reinforced material.

As represented on the figure above, the XY plane is the plane of the woven glass fibers, while Z is the axis of the thickness of the base material. When examining various datasheets of major dielectric base materials (typ. high Tg glass-epoxy materials), it appears that base material suppliers use a wide range of methods to measure the thermal conductivity of their products. In most cases, it is also visible that anisotropy of materials is not considered.

Supplier	Type	Name of the parameter in the datasheet	Unit	Value	Method claimed
A	Glass-polyimide	Thermal conductivity	$W.m^{-1}.K^{-1}$	0,20	ASTM E146
I	Glass-PTFE	Thermal conductivity	$W.m^{-1}.K^{-1}$	0,23	not specified
E	Glass-epoxy	Thermal conductivity	$W.m^{-1}.K^{-1}$	0,30	not specified
B	Glass-epoxy	Thermal conductivity (-100-250°C)	$W.m^{-1}.K^{-1}$	0,32	ASTM F433
J	Glass-PTFE ceramic	Thermal conductivity	$W.m^{-1}.K^{-1}$	0,49	ASTM C518
H	Glass-epoxy	Thermal conductivity	$W.m^{-1}.K^{-1}$	0,53	Laser flash
J	Glass-hydrocarbon ceramic	Thermal conductivity	$W.m^{-1}.K^{-1}$	0,60	ASTM F433
E	Glass-epoxy	Thermal conductivity	$W.m^{-1}.K^{-1}$	0,79	not specified
D	Thermally improved glass-epoxy	Thermal conductivity-Z-Axis	$W.m^{-1}.K^{-1}$	2,00	ASTM E146
		Thermal conductivity-X-Y-Axis	$W.m^{-1}.K^{-1}$	3,50	ASTM E146

Table 2 : Some supplier's datasheet extract.

This table gives an overview of the range of thermal conductivities of typical existing dielectric base materials, and thermally improved glass-epoxy. Because of this specificity, only supplier D considers anisotropy, and specifies thermal conductivity according to the direction of measurement. All others provide a single value.

Thermally improved dielectrics are more expensive than standard products, and more difficult to process. Therefore, a good knowledge of thermal conductivities in all directions may be important for the designer to optimize their products, from a pure technical prospective, but also from a cost efficiency prospective. Indeed, heat can be transferred to colder regions laterally, on component side, on opposite side, or combination of these three options.

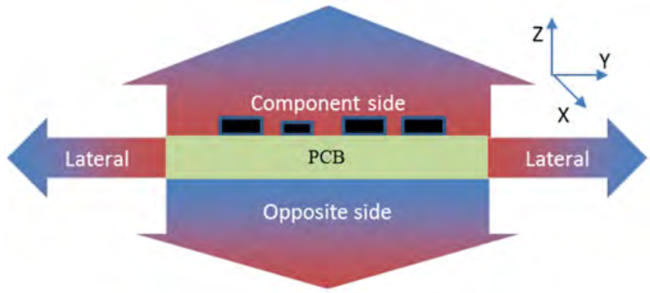

Figure 2: Printed circuit board thermal management possibilities.

Thermal Conductivity Measurement Methods Used by Material Suppliers

ASTM E1461: "Standard Test Method for Thermal Diffusivity by the Flash Method"

"[...] this test method covers the determination of the thermal diffusivity of primarily homogeneous **isotropic solid materials.** Thermal diffusivity values ranging from 0.1 to 1000 $mm^2 s^{-1}$ are measurable by this test method from about 75 to 2800 K. [...]This test method is applicable to the measurements performed on essentially fully dense (preferably, but low porosity would be acceptable), homogeneous, and **isotropic** solid materials that are opaque to the applied energy pulse. [...]"

ASTM F433: "Standard Practice for Evaluating Thermal Conductivity of **Gasket** Materials"

[...] This practice covers a means of measuring the amount of heat transfer quantitatively through a material or system.

This practice is similar to the Heat Flow Meter System of Method C 518, but modified to accommodate small test samples of higher thermal conductance.

ASTM D5930: "Standard Test Method for Thermal Conductivity of Plastics by Means of a Transient Line-Source Technique"

[...] This test method covers the determination of the thermal conductivity of plastics over a temperature range from -40 to 400°C. The thermal conductivity of materials in the range from 0.08 to 2.0 W/m.K can be measured covering thermoplastics, thermosets, and rubbers, filled and reinforced. [...] There is no known ISO equivalent to this test method."

ASTM C518: "Standard Test Method for Steady-State Thermal Transmission Properties by Means of the Heat Flow Meter Apparatus"

"[...] This test method covers the measurement of steady state thermal transmission through flat slab specimens using a heat flow meter apparatus [...] Applicable to the measurement of thermal transmission through a wide range of specimen properties and environmental conditions. The method has been used at ambient conditions of 10 to 40°C with thicknesses up to approximately 250 mm, and with plate temperatures from -195°C to 540°C at 25 mm thickness [...]. To meet the requirements of this test method the thermal resistance of the sample must be greater than 0.10 $K.m.W^{-1}$ in all directions [...]"

Laser Flash: "Method to measure thermal diffusivity"

The laser flash method is used to measure thermal diffusivity of a thin disc in the thickness direction. This method is based upon the measurement of the temperature rise at the rear face of the thin-disc specimen produced by a short energy pulse on the front face. With a reference sample, specific heat can be achieved, and with known density the thermal conductivity is calculated.

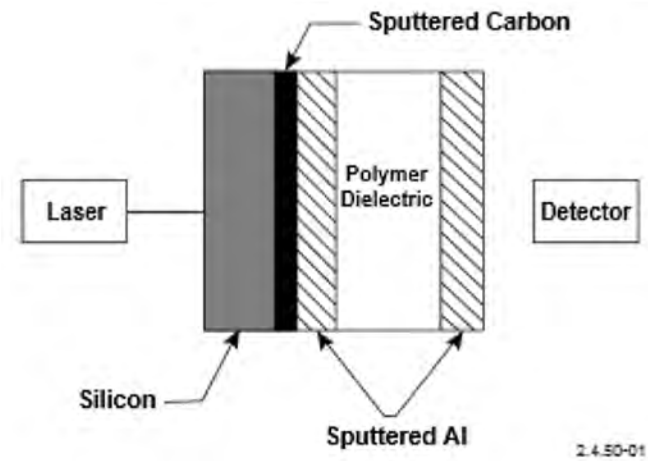

Figure 3: IPC-TM-650-2-4-50: Laser is flashed and the heat rise is measured on the back Al by the detector.

IPC-TM-650 2.4.50: Thermal Conductivity, Polymer Films

"[…] This test method defines the procedure for determining the Thermal Conductivity of polymer coatings on inorganic substrates, such as polyimide on silicon wafer […]".

First Conclusion

Base material suppliers use many different methods, making difficult to compare the relative performances of their products or to check the actual properties. Some methods are clearly not adapted to anisotropic materials. The flash method, described in both IPC-TM-650 2.4.50 and in ASTM E1461, is claimed to be adapted to measuring thermal diffusivity of only isotropic material (which could be discussed in reality). In any case, it does not allow to determine the XY plane thermal diffusivity of a thin anisotropic sample.

Proposed Method to Measure XYZ Thermal Conductivity: Transient Fin Method

The proposed method is called transient fin method. It aims at measuring the thermal diffusivity in the XY plane, with a simple setup and a sample easy to produce. Associated with differential scanning calorimetry and the flash method, it allows to have thermal conductivity values along the Z-axis and in the XY plane.

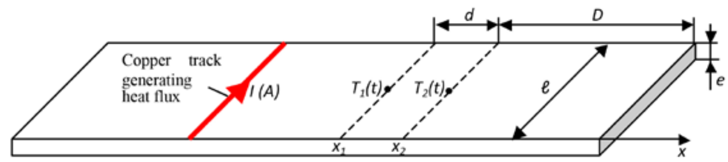

Figure 4: Transient fin method principle.

The method is based on heat generation by a copper conductor patterned on the dielectric material to analyze, and temperature measurement by optical sensor (infrared). The copper pattern is easily produced by a PCB manufacturer. It does not request particular capabilities. Typically, starting from a laminate with copper on both sides, the pattern is produced by direct photolithography.

When it is preferred to analyze the temperature variation on the opposite side, in order to ease the centering of the optical sensor on this opposite side, some fiducials can be added also by photolithography of a copper pattern. However, this copper pattern should be far enough of the analyzed zone, not to disturb the measurement.

The principle is to inject a step of current between the two extremities of a copper track to generate heat, and to measure the temperature variation in two distinct points at a defined distance from the heating track, by placing an optical sensor (infrared camera) either on the same or on the opposite side of the test sample.

Some Physics...

At first, the mathematical model of has to be determined. Once this done, the transient fin method consists of recording thermograms (output of the IR sensor), and find the best parameters values to make the model stick to the experimental curves (thermograms).

This model developed is based on the following assumptions:

- The sample is considered as initially at a uniform temperature, equal to ambient air temperature Ta. A step of current is supplied to the copper track, and generates heat flux $\Phi(t)$. Very interesting for the transient fin method: it is not necessary to know intensity or time variations of the heat flux.

The thermal gradient in the thickness e is negligible with regards to the other dimensions. This is verified if thickness is less than one tenth of the other dimensions, which is clearly the case for our test sample. In other words, when distance x_1 between the heating track and the first line, and the distance $d = x_1 - x_2$ are large enough with regards to the sample thickness, the heat transfer is considered as mono-dimensional (no heat gradient along Z). As an order of magnitude, the typical PCB sample to analyze is ~100 to 200 µm thick, while x_1 and d can easily be around 10 mm.

• The test sample is large enough to be considered as semi-infinite during the measurement time.

The evolution of temperatures $T_1(t)$ and $T_2(t)$ at respective distances x_1 and x_2 from the copper track edge, is recorded by the IR sensor (could be also thermocouples or any other temperature measurement system, with appropriate time constant and accuracy). The output of this process is the experimental curves (in time domain).

With Laplace transform formalism, $\theta_2(p)$ and $\theta_1(p)$. are the Laplace transforms of $T_1(t)$ and $T_2(t)$.

H(P) is the transfer function between $\theta_2(p)$ and $\theta_1(p)$.

$$H(p) = \frac{\theta_2}{\theta_1}$$

To determine H(P), we use the quadrupole formalism:

$$\begin{bmatrix}\theta_1 \\ \Phi_1\end{bmatrix} = \begin{bmatrix}A & B \\ C & D\end{bmatrix}\begin{bmatrix}\theta_2 \\ E\sqrt{p}\theta_2\end{bmatrix}$$

With

$$A = D = cosh(qd)$$
$$B = \frac{1}{\lambda q} sinh(qd)$$
$$C = \lambda q\, sinh(qd)$$

And:

$$q = \sqrt{\frac{p}{a} + \frac{hP_e}{\lambda S}}$$

Where:

Pe = 2(e + l) is the perimeter

S = el is the heat flux flow section

λ is the thermal conductivity, a is the thermal diffusivity and $E = \sqrt{\lambda\rho c}$ is the thermal effusivity

We can write:

$$\theta_2 = \frac{\theta_1}{A + BE\sqrt{p}} = \frac{\theta_1}{cosh(qd) + \frac{E}{\lambda q} sinh(qd)\sqrt{p}}$$

With $\frac{E}{\lambda} = \frac{\sqrt{\lambda\rho c}}{\lambda} = \sqrt{\frac{\rho c}{\lambda}} = \frac{1}{\sqrt{a}}$

It shows that θ_2 is only a function of θ_1, p, a and $\frac{hP_e}{\lambda S}$, and thus:

$$H(p) = \frac{1}{cosh(qd) + \frac{E}{\lambda q} sinh(qd)\sqrt{p}} = \frac{1}{cosh(qd) + sinh(qd)} = exp(-qd)$$

With $q = \sqrt{\frac{p}{a} + \frac{hP_e}{\lambda S}}$

To come back in the real space (time domain) and find $T_2(t)$ function, we have to make the convolution product of $T_1(t)$ by the inverse Laplace transform of H(p):

$$T_2(t) = T_1(t) \otimes L^{-1}[H(p)]$$

NB : L^{-1} [H(p)] is the inverse Laplace transform of H(p).

From above, the model (shape of the curve) of $T_2(t)$ is known. With appropriate parameters, it can be adjusted to the experimental curve. An optimization algorithm is then used to determines the best a and h values minimizing the difference between the experimental and theoretical curves. The next graphs represent this optimization.

Note: Everything done under Matlab®.

Measurement System Setup

The transient fin samples have to be prepared first. A square shape, approximately 100 x 100 mm² is sufficient, with the heating cop-

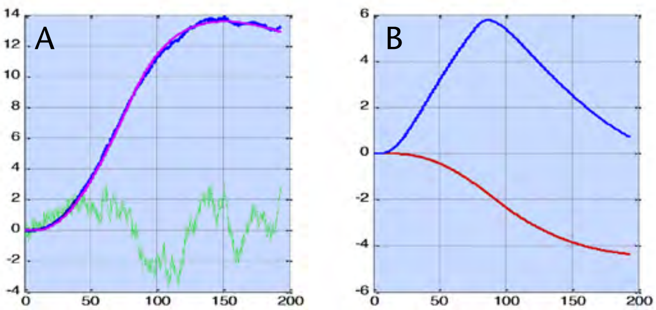

Figure 5: a) Example of experimental and optimized theoritical curves $T_2(t)$; b) Reduced sensitivities of $T_2(t)$ to a (blue) and h (red).

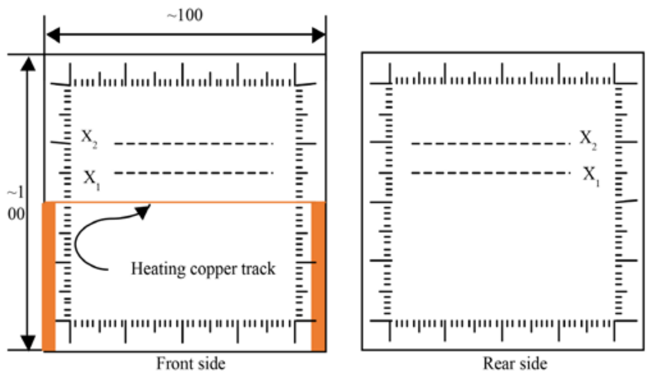

Figure 6: Transient fin sample design.

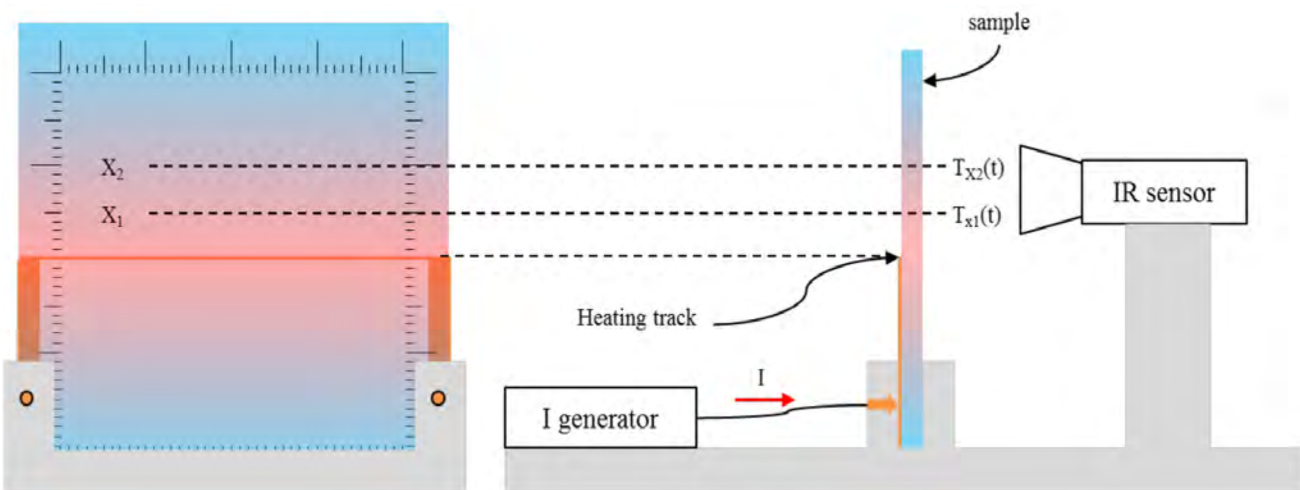

Figure 7: Transient fin sample method apparatus example.

per track in the middle, and power supply bars on one side. There is no other specific treatment required. Temperature variation can be recorder on front side or rear side. In order to ease the centering of the optical sensor on this opposite side, fiducials can be added by etching (photolithography). In that case, the resulting copper fiducials should be far enough of the analyzed zone, not to disturb the measurements.

The transient fin sample has to be connected to a current source, and placed in front of an IR sensor, which will record temperature over time variations, at defined distances from the copper track. To make the measurement easy and repetitive, an apparatus is suggested on the next figure.

Method to Get XY and Z Thermal Conductivities

Step 1

Density and specific heat have to be measured first. Specific heat is measured by differential scanning calorimetry (DSC). Together, density and specific heat give volumetric heat capacity ρC_p, considered as isotropic. As this is quite standard, and measuring equipment is commercially available, this will not be developed here. For DSC and density measurement, depending on the equipment and specified method for DSC and density measurement, no specific samples are required, usually only a small piece of material.

Step 2

Flash method is then used to measure a_z, thermal diffusivity along Z axis (thickness of the base material). Combining a_z and volumetric heat capacity ρC_p gives thermal conductivity along the Z-axis. Here again, flash method is well documented and standards exist (cf. ASTM E1461, IPC-TM-650 2.4.50). Samples have to be prepared according to standard method, for instance ASTM1461. It will not be developed here.

Step 3

In a third step, the proposed transient fin method is used. The specific transient fin samples have to be made. With an electrical step stimulus, the copper track is heated-up while an optical thermal sensor (IR detector) records top surface temperature. The mathematical process described above is used to find the best a and h values to make the model stick to the experimental curve. It allows to get the thermal diffusivity in the XY plane, and later on, combined with the volumetric heat capacity (isotropic), it gives XY thermal conductivity value.

Results

In this case, glass-reinforced dielectrics have been measured as an example. Measurements were performed on two different prepregs of thermally improved base materials. Test samples have been manufactured with these prepregs. For the transient fin method, test samples were manufactured by hydraulic vacuum lamination, photolithography, and routing, in standard printed circuit board industry process conditions.

- Sample 1080 = made of thermally optimized glass-reinforced epoxy 1080 type prepreg
- Sample 106 = made of thermally optimized glass-reinforced epoxy 106 type prepreg

Step 1: Volumetric heat capacity

Measured by Differential Scanning Calorimetry (model mdSc3 from SETARAM).

	T (°C)					Density
	20	30	40	50	60	ρ (kg.m^{-3})
Cp of **1080** (J.kg^{-1}.K^{-1})	887	915	945	977	1006	2249
Cp of **106** (J.kg^{-1}.K^{-1})	884	911	939	970	998	2201

Table 3: Specific heat capacity Cp of 1080 and 106 prepregs measured by DSC.

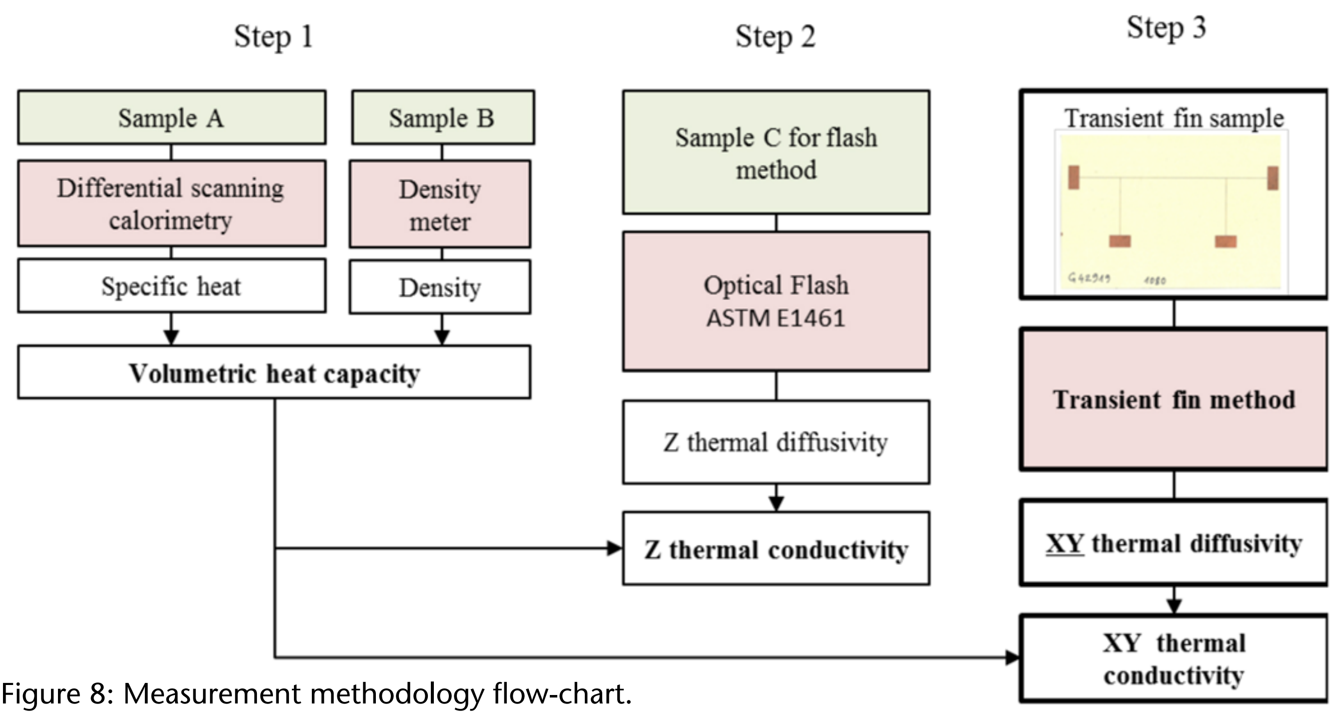

Figure 8: Measurement methodology flow-chart.

From the above,

- Specific heat capacity for 1080 is given by: C_p = 825.6 + 3.001T (J $kg^{-1}K^{-1}$) with T in Celsius.
- Specific heat capacity for 106 is given by: Cp = 825.6 + 2.8683T (J $kg^{-1}K^{-1}$) with T in Celsius.

With density ρ,

- volumetric heat capacity for 1080 (at 30°C) is $\rho C_p = 2.058 \times 10^6$ (J m^{-3} K^{-1})
- volumetric heat capacity for 106 (at 30°C) is $\rho C_p = 2.005 \times 10^6$ (J m^{-3} K^{-1})

Step 2: Z Thermal conductivity by flash method

Note: To perform such an optical flash method measurement, one side of the sample has to be black. To do that, one side is covered with an appropriate black paint instead of the carbon sputtering. It was verified by a separate complex method (simulation under COMSOL software) that this black paint does not affect the results.

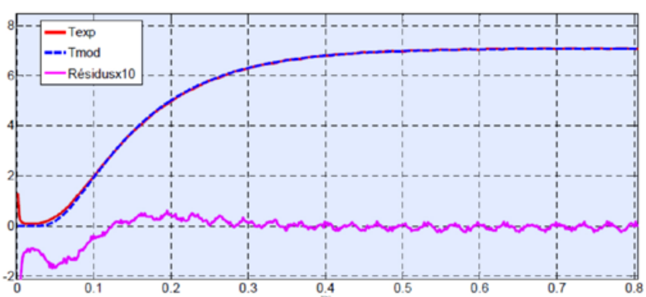

Figure 9: Example of theoretical and experimental thermogram by flash method.

The measured Z thermal diffusivities have been extracted in the following table.

Material	$a_z (m^2.s^{-1})$
1080	8.20×10^{-7}
106	7.80×10^{-7}

Table 4: Z thermal diffusivity measurements by flash method.

Step 3: XY Thermal diffusivity by transient fin method

As described previously, the copper track designed on the sample is connected to a generator to produce a linear heat flux. An infrared camera is placed to measure the temperature of the two distant points and of the sample. Identifying the transfer function allows to compute the thermal diffusivity.

Sample preparation

Using a standard PCB fabrication process, the samples were manufactured with the relevant 1080 or 106 prepregs. A stack-up approximately 200µm thick was built. Hereafter is a picture of the realized sample.

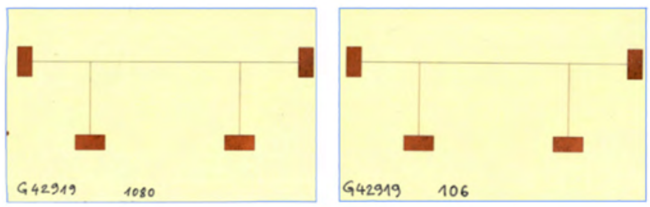

Figure 10: 106 and 1080 test samples for transient fin method.

Thermal Conductivities Determination

The transient fin method is used to determine XY thermal diffusivity. The thermograms (recorded by the IR sensor) give the temperature variation at and distances from the heating

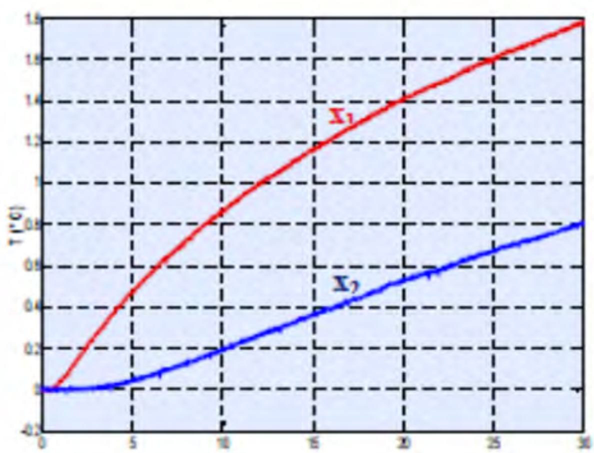

Figure 11: Example of thermograms at x_1 and x_2 distances.

Material	a_{xy} ($m^2.s^{-1}$)
1080	1.23×10^{-6}
106	1.32×10^{-6}

Table 5: XY thermal diffusivity measurements.

line, as a function of time. Using the appropriate mathematical equations described above, it allows to determine the thermal diffusivity. Results are in Table 5:

Using the previously measured specific heat capacities and densities, it is now possible to compute the thermal conductivities in the XY plane and along the Z-axis:

Results

In this particular case, the base material manufacturer's datasheet differentiates the thermal conductivity along Z or in the plane but does not indicate specific values for 106 or 1080 prepregs, nor onto which laminate (thickness and composition in terms of glass-content) measurements were made. As indicated in the datasheet: *"Results listed above are typical properties, provided without warranty, expressed or implied, and without liability. Properties may vary, depending on design and application."*

Transient fin measurements gave lower values than the typical values indicated in this datasheet. A quick look at the resin content of the 1080 and 106 indicates respectively 85% and 90% resin content. As seen before, glass is a better heat conductor than "normal" epoxy resin, but this improved material does not contain "normal" epoxy resin. It has been filled with ceramic particles, precisely to improve its thermal conductivity, bringing it significantly above the ~1 $W.m^{-1}.K^{-1}$ of the glass fibers. Therefore, it is normal to obtain a lower XY thermal conductivity for 1080, containing more glass than 106.

Conclusion

In the PCB ecosystem, there is currently no unique and common standard method to measure thermal conductivity. However, modern applications require an accurate knowledge of base material properties for thermal optimization of electronic systems. Thermally improved dielectrics become more and more popular in various printed circuit board applications. These copper-clad laminate products and corresponding prepregs are usually glass-reinforced, and therefore quite strongly anisotropic. Significantly expensive to buy and to process, the benefit brought by their use should be accurately known or at least easy to assess when designing a new product. 3D thermal models are nowadays common tools for system designers, but to provide consistent simulation results, these tools need accurate thermal properties to provide good simulations.

Transient fin method presented in this paper is at its beginning. At this stage, it seems suitable and efficient enough to help suppliers and manufacturers to complete thermal conductivity information on most of dielectric base materials used in the printed circuit board industry. It requires to manufacture a dedicated but simple test sample, to use a measurement chain with a current step generator, an IR sensor, and appropriate engineering skills. It can be improved by building a dedicated device, comprising the current source, the sample holder,

Material	Datasheets		Measurements	
	λ_z ($W.m^{-1}.K^{-1}$)	λ_{xy} ($W.m^{-1}.K^{-1}$)	λ_z ($W.m^{-1}.K^{-1}$)	λ_{xy} ($W.m^{-1}.K^{-1}$)
A	2	3.5	1,7	2,5
B	2	3.5	1,6	2,6

Table 6: XYZ thermal conductivities calculated.

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the IR sensor, and the appropriate digital signal analysis to output automatically the XY thermal diffusivity. Sample shape and size can be easily standardized.

This method, combined with the existing ones to measure specific heat, density and thermal diffusivity in the Z-axis, allows getting the often missing data about thermal conductivity in the XY plane, along the glass fibers. It also gives the possibility of discriminate more precisely X and Y thermal conductivities by rotating the sample, in case base materials have also an anisotropy between yarn and chain of the woven glass mesh. It will be continued, improved, and deployed on a large range of printed circuit board dielectric base materials to help manufacturers and designers to optimize thermal management of printed circuit board and more generally electronic system performances and efficiency. **PCB**

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This paper was originally presented at IPC APEX EXPO 2016 and published in the proceedings.

François Lechleiter is R&D manager for Cimulec Group.

Yves Jannot is a research engineer at LEMTA CNRS.

Computer Improves Automated Sports Broadcasts

An automated camera system was able to learn how to better film basketball and soccer games—and smoothly recover from mistakes—by watching human camera operators, scientists at Disney Research report.

The result was footage without much of the jerkiness that plagues automated cameras, said Peter Carr, senior research engineer at Disney Research.

Carr, along with colleagues at Disney Research and the California Institute of Technology, will describe the theoretical underpinnings of their new approach June 19 at the International Conference on Machine Learning (ICML) in New York City. The Disney Research and Caltech researchers, joined by colleagues at the University of British Columbia, will describe their field experience at the IEEE Conference on Computer Vision Pattern Recognition (CVPR) 2016 in Las Vegas.

“This research demonstrates a significant advance in the use of imitation learning to improve camera planning and control during game conditions,” said Jessica Hodgins, vice president at Disney Research.

Current optical tracking technology can’t reliably follow the ball automatically for the duration of a match, but the automated camera system can follow the general flow of the game by studying detected player positions. Because of imperfect sensing, automated cameras generate jittery footage—especially when incorrectly anticipating how the game is about to unfold.

Researchers developed new machine-learning algorithms to ensure automated cameras could strike the right balance between smoothness and closely following the action. Unlike established learning algorithms, the proposed approach repeats multiple times, and learns by analyzing the deviations it makes from the human operator at each iteration.

The Evolution and Revolution of Impedance Control in PCB Production

by Renato Peres
CIRCUIBRAS

The PCB industry in Brazil has gone through several changes over the last decade. Our customers have been demanding better quality and higher-reliability products more than ever before, but few things have changed as much as impedance control. PCBs with impedance control requirements have become the engine of the market, and finding solutions to fit the customer's needs is extremely challenging.

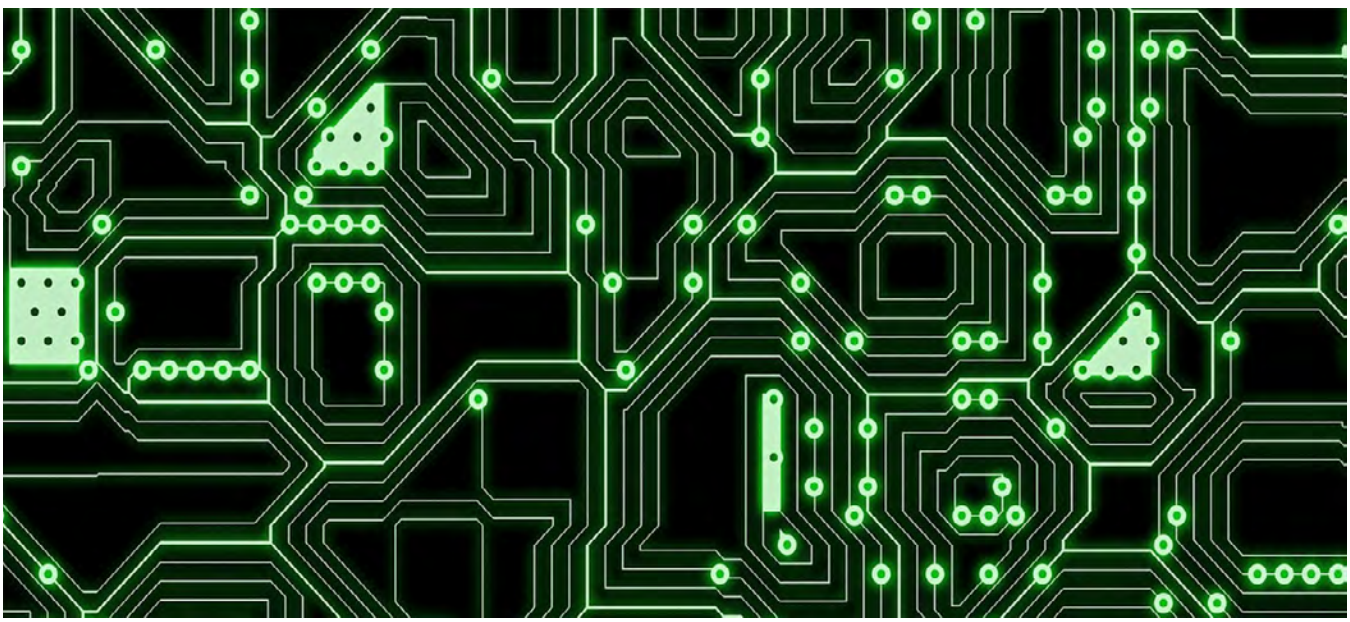
Ten years ago, the Brazilian PCB industry was a little vague on this subject, and very few PCB shops were doing impedance testing. About five years ago, with the evolution of the national PCB industry, customers started producing prototypes requiring impedance control and the market started to develop. However, it seemed to me that neither the customers nor the PCB shops really knew what to order and to deliver at that time.

There always were differences between the specs for the board, the coupon measured, and the simulation software. As a best practice, many PCB shops used to appeal to a cross-section analysis to verify the PCB build up. In the end, impedance simulation software was more reliable than the TDR measurements.

I remember I felt a bit normal last year when I read the article written by Dan Beaulieu and Bob Tarzwell for *The PCB Design Magazine*, Controlled Impedance: A Real-World Look at the PCB Side. Coupons that don't fit the specs of the customers, cross-section analyses, differences in resin flow during lamination, copper thickness variation, and many other issues described in the article were very similar to the problems we faced daily.

Nevertheless, the industry in Brazil has gone further, pressing the suppliers to develop new controls, not yet usual to the national market.

The real challenge right now is to measure the impedance on a board, and make these results similar to the coupon results, so that the coupon becomes useful.



But how in the world could it be possible with so many variables and so much uncertainty? What are the challenges to get this done? The following are a few gleaned from my experience in this field.

1. Relentless pursuit of improvement

There is a need to pursue perfection when dealing with on-board impedance testing. Copper plating distribution, prepreg thickness, lamination flow, etching compensation and line formation, both on coupon and on board, can be exhaustively analyzed by process engineers and controlled in the production. It might sound basic, but there is a need to set patterns or controls all over the production steps, so that one may find a trend. Boards cannot be etched or developed or even plated in a random way. There must be a standard definition of how boards flow into each and every line in the factory, otherwise data will be irrelevant.

> "There must be a standard definition of how boards flow into each and every line in the factory, otherwise data will be irrelevant."

Once, during a presentation to a customer who was very concerned about impedance control, I showed him some results that were quite good at that time. There was a difference in copper thickness between the coupon and all the points of impedance control on the board of about 5–7 microns, but there was a pattern in the deviation. We had never achieved such good results, but the customer looked at us and said, "It needs improvement." I started laughing, and for my surprise and amazement, I learned one of the most important lessons a process engineer could ever learn. He said, "What is data for if not for improvement?"

When it comes to impedance, every single product is different, and although there are some rules to be followed, it is not guaranteed that the results will be the same.

2. Cross-section analyses

Analyze 15 or 20 cross-sections.

3. AOI

AOI became a critical process during fabrication. Every single panel with impedance control needs to go through this inspection, and defects that once were imperceptible will start flourishing in the factory.

It dramatically changes the flow of the boards, and also makes a huge impact on operators' training and understanding of process.

As lines' integrity are a major concern on impedance, focusing on the impedance lines must be a common practice. Also, it is important to state that AOI does not guarantee impedance and it is not a measurement inspection machine, so the process as a whole must be under control.

4. TDR equipment

One of the real challenges is finding equipment that can fit on-board testing and coupon testing and still be robust enough to be used in the production line.

There are many suppliers of impedance equipment in the market, some of them with breakthrough promises but still unknown, and others that have been well-established for years that are trying to keep up with the new trend of on-board testing.

When choosing the equipment, one needs to keep in mind that bandwidth and rise time are important characteristics for on-board testing.

Basically, all TDR equipment can test coupons, because they are about six inches or so in length. However, it is not uncommon to see lines in circuits of just about one-inch length with impedance control that cannot be tested with the same "standard" equipment.

The bandwidth is one of the characteristics that will determine how short the trace can be. Simply saying, the higher the bandwidth and the lower the rise time, the shorter the line to be tested.

Another aspect that has changed is that, when doing on-board testing, it is impossible to know what the pitch of the test points is going to be. In order to do that, suppliers have developed groundless variable pitch probes that can be used on circuit without damaging the pads. This is a huge advance in the industry that has gradually become common.

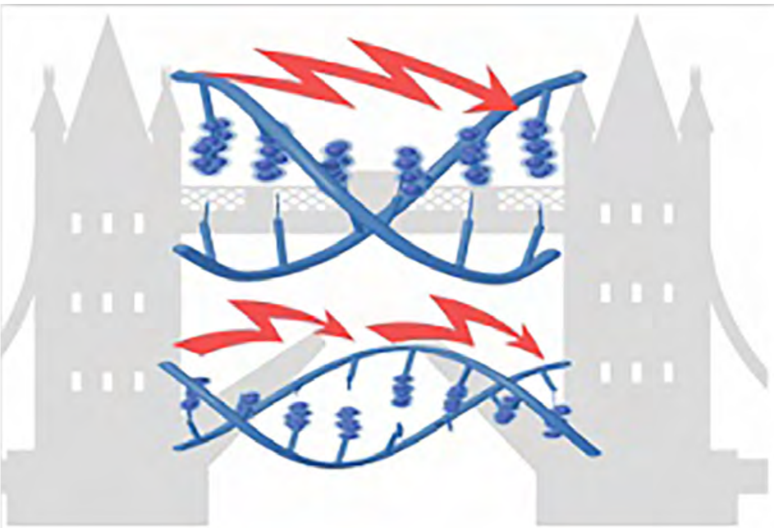
5. Coupon and board design

In order to have similar impedance measures on board and on coupon, the design of the coupon should be similar to the design on board. If there is a large area of copper surrounding the impedance lines on board, there must be an area similar to that on coupon for better copper distribution. We know this is never easy when we deal with better usage of the panel, but this is the challenge for the CAM engineers. Sometimes, coupon and circuit must have different etch compensations to achieve the same results.

Impedance has been changing the whole process of PCB fabrication, especially inspection and data analyses, and it has challenged companies to pursue their best. Surely nobody will have the perfect solution, but if you pursue it you will improve a lot. Even without achieving perfection, you will find a better solution than the one you had. **PCB**

Renato Peres is an industrial engineer and production coordinator with Circuibras Circuitos Impressos Profissionais.

Ultra-thin Solar Cells Easily Bend around a Pencil



Flexible photovoltaics made by researchers in South Korea could power wearable electronics.

The ultra-thin photovoltaics are flexible enough to wrap around the average pencil and could power wearable electronics like fitness trackers and smart glasses. The researchers report the results in the journal Applied Physics Letters, from AIP Publishing.

Thin materials flex more easily than thick ones—think a piece of paper versus a cardboard shipping box. The reason for the difference: The stress in a material while it's being bent increases farther out from the central plane.

"Our photovoltaic is about 1 micrometer thick," said Jongho Lee, an engineer at the Gwangju Institute of Science and Technology in South Korea.

The researchers made the ultra-thin solar cells from the semiconductor gallium arsenide. They stamped the cells directly onto a flexible substrate without using an adhesive that would add to the material's thickness. The cells were then "cold welded" to the electrode on the substrate by applying pressure at 170° and melting a top layer of material called photoresist that acted as a temporary adhesive.

By transfer printing instead of etching, the new method developed by Lee and his colleagues may be used to make very flexible photovoltaics with a smaller amount of materials.

The thin cells can be integrated onto glasses frames or fabric and might power the next wave of wearable electronics, Lee said.

MilAero007 Highlights

Global Technology Development: HDP User Group European Meeting 2016

Delighted and honoured to be invited again to attend the open session of the High Density Packaging User Group (HDPUG) European Meeting, I made my way to the picturesque Grand Duchy of Luxembourg, a tiny principality bordered by Belgium, France and Germany, and ranked among the world's top-three nations in both wealth and wine consumption.

What You Probably Don't Know about NASA

While at Maker Faire 2016 in San Mateo recently, I met with George Gorospe of NASA's Ames Research Center to discuss his group's recent findings and projects, NASA's CubeSats and microsatellites, and what the commercialization of space travel means for the near future.

IPC Standards Committee Reports, Part 2—Assembly and Joining, Component Traceability, Flexible Circuits, High Speed/High Frequency

These standards committee reports from IPC APEX EXPO 2016 have been compiled to help keep you up to date on IPC standards committee activities. This is the second in a series of reports.

Illinois Researcher Receives DARPA Contract to Design a Hybrid Robot

Illinois researcher Hae-Won Park has been awarded a Robotics Fast Track contract from the Defense Advanced Research Projects Agency (DARPA) to design a hybrid robot that can glide, land, and walk.

International Partners Provide Science Satellites for America's Space Launch SLS Maiden Flight

NASA's new Space Launch System (SLS) will launch America into a new era of exploration to destinations beyond Earth's orbit. On its first flight, NASA will demonstrate the rocket's heavy-lift capability and send an uncrewed Orion spacecraft into deep space.

Saab Receives Order within AEW&C Segment

Defence and security company Saab has landed an order within the Airborne Early Warning and Control (AEW&C) segment worth about SEK 1.1 billion.

American Standard Circuits Enhances Via Fill Capabilities with Double Systems

Anaya Vardya, CEO of American Standard Circuits, has announced that his company recently enhanced their via fill capabilities with the installation of a MASS VHF300 horizontal hole filling system with full chamber vacuum capability, accompanied by a MASS ES10 double-sided Scavenger unit.

Record-breaking $65B Global Defense Trade in 2015 Fueled by Middle East and Southeast Asia

"The global defense trade market has never seen an increase as large as the one we saw between 2014 and 2015," said Ben Moores, senior analyst at IHS. "2015 was a record-breaking year." Markets rose $6.6 billion, bringing the value of the global defense market in 2015 to $65 billion. IHS forecasts that the market will increase further to $69 billion in 2016.

BAE Systems Harnesses Pioneering Technology to Power Land Rover BAR's America's Cup Bid

BAE Systems has revealed that it is adapting cutting-edge bone conduction technology for Land Rover BAR's world class sailing team, as it seeks to boost the team's bid to bring the America's Cup home to Britain in 2017.

Global Military Radars Market to Reach $13.04B by 2020

The global military radars market was valued at USD 11.02 billion in 2015 and is projected to reach USD 13.04 billion by 2020, at a CAGR of 3.42% from 2015 to 2020.

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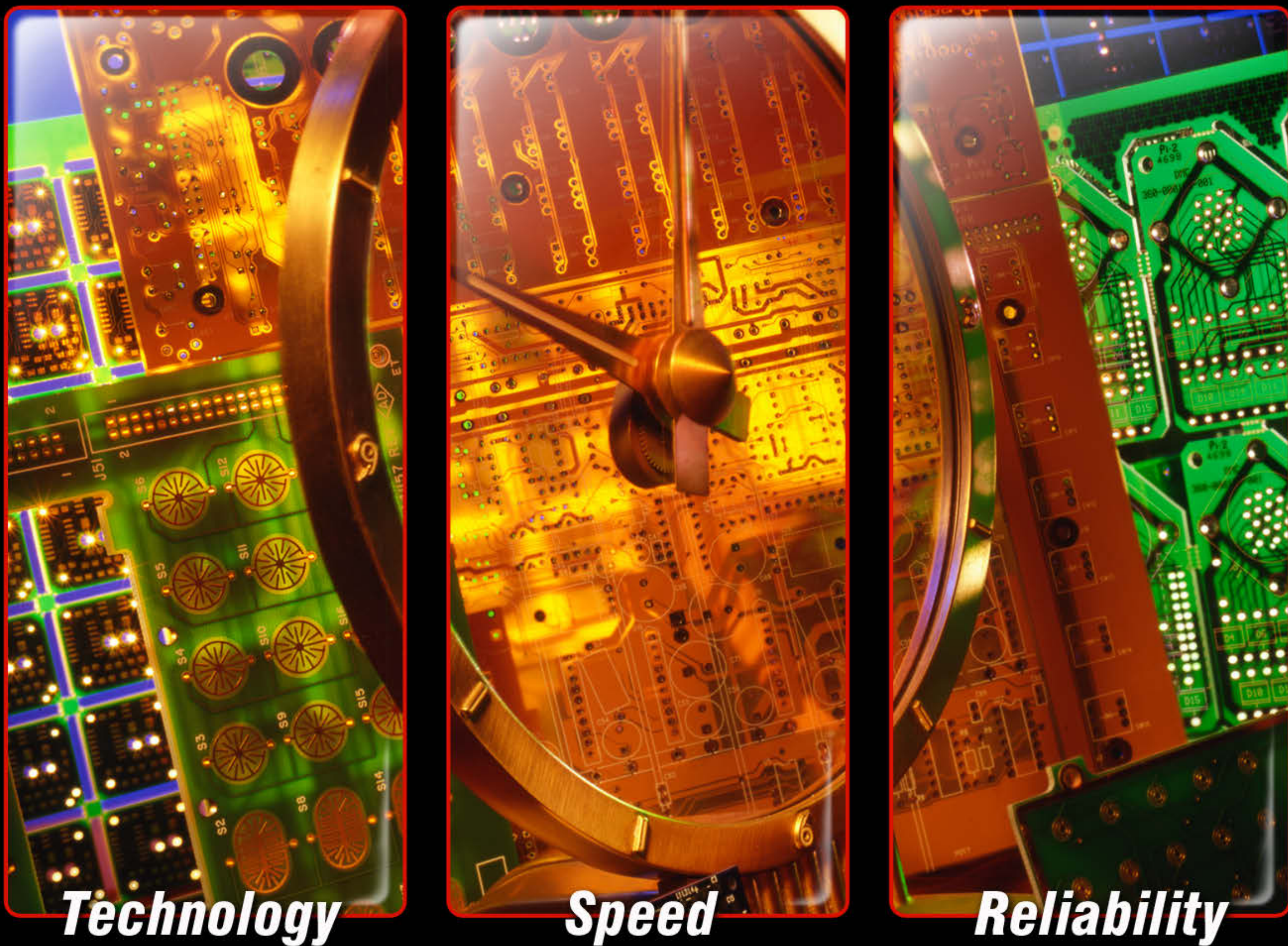

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Building Reliability into the PCB, Part 1

by Michael Carano
RBP CHEMICAL TECHNOLOGY

Introduction

Sometimes there is confusion among PCB engineers and quality managers as to what constitutes reliability. Some may say that reliability refers to avoiding PTH failures such as corner cracks or interconnect defects. Or there are those who subscribe to a wider range of failure criteria to determine whether or not the final product is reliable for long-term service. Regardless, the term "reliability" can be defined as:

"The probability that a functioning product at time zero will function in the desired service environment for a specified amount of time."

With respect to printed circuit boards, the biggest concerns involve thermally driven failures. Thermally driven failures result in PTH defects including:

- Innerlayer separation (ICD)
- Foil cracks
- Barrel cracks
- Corner cracks

Figure 1 shows a schematic of thermally induced PTH failures.

When a printed wiring board or assembly is under a thermal load (soldering, thermal cycling, etc.) the PTH is stressed in the z-axis direction. This stress is caused (due to the thermal excursion) by the difference in CTE (coefficient of thermal expansion) of the resin system (used for the printed board) and the PTH. The resin is prevented from expanding in the x/y planes by glass reinforcement of resin material. Due to this restraining in the x-y directions, resin is not restrained sufficiently in the z-axis direction, unfortunately. The result of this is that the resin expansion will occur at a much greater rate in the z-axis direction. The plated through-hole barrel is clearly stressed under these conditions. As this is occurring, the plated copper-to-innerlayer connections experience severe tension. If the tension is severe enough, the copper-to-innerlayer connection can separate leading to ICD (interconnect defect). In addition, if the copper-to-innerlayer connection is sufficiently robust and does not separate, much of the stress and strain will be redistributed through the barrel of the PTH, leading to barrel cracking.

Taking this a step further, one can surmise that there is a hierarchy of failure that ensues under thermal shock and thermal cycling con-

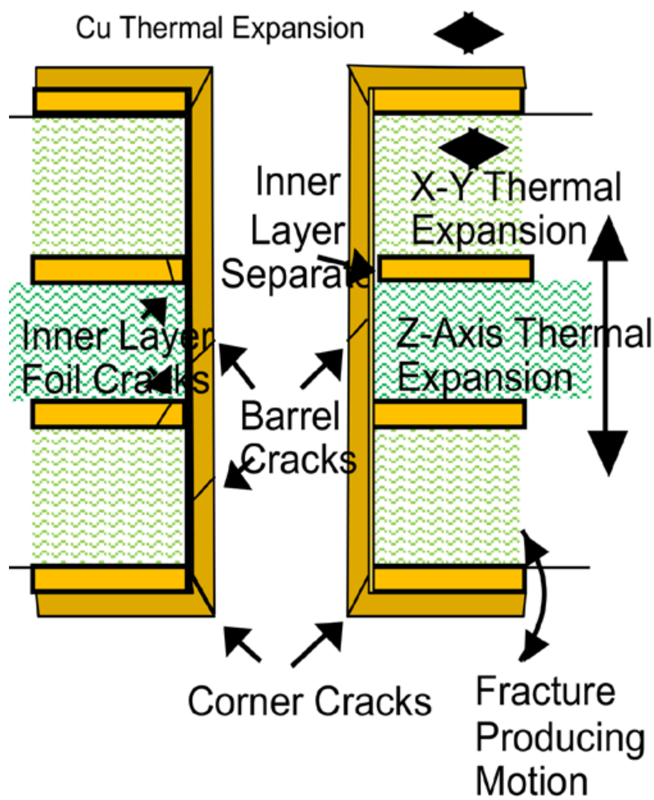


Figure 1: Failure mechanisms in PTH barrel (Source: Coombs' Printed Circuits Handbook, Chapter 59, 2006).

Figure 2: Barrel cracks in PTH subjected to thermal cycling. Note that the copper-to-inner-layer connections remain intact.

Figure 3: Interconnect defect (Source: IPC 9121).

ditions. According to Bill Birch of PWB Interconnect Solutions, "The failure hierarchy of the interconnect plays an important role in establishing whether the foil (or post interconnect) becomes a dominant or latent failure mechanism. The basis for the hierarchy is determined by the reliability of the PTH barrel."[1]

Thus the stress was shifted through the barrel of the PTH, increasing the opportunity for failure. Turning the tables a bit, Figure 3 shows a second failure mode, namely ICD. In this case the adhesion of the plated copper to the interconnect is less than robust. Here the weakest link appears to be the copper-to-copper bond. There are several possible reasons for this including:

- Excessive electroless copper thickness on the post interconnect
- Drill debris at post interconnect surface
- Excessive dwell time in the palladium catalyst
- Poor grain structure of the copper deposit leading to stress
- Poor overall plating practice
- Electroless copper solution out of specification

Stress and Strain in the PTH

Most organic resin matrix substrate materials are highly anisotropic, with a much higher CTE above the glass transition temperature Tg in the through-thickness (z) direction than in the plane of the woven matrix cloth (the x-y plane of the board). Since above Tg the CTE climbs sharply, aggressive thermal cycles can result in large strains in the z direction and, consequently, on the PTHs. The PTH acts like a rivet, which resists this expansion, but the copper barrel is stressed and may crack, causing electrical failure. There is increasing strain on the barrel associated with a high temperature excursion. Failure may occur in a single cycle or may take place by initiation and growth of a fatigue crack over the course of a number of cycles. For high-aspect-ratio through-holes subject to repeated thermal shocks from room temperature to solder reflow temperatures (220–250°C) during board fabrication (e.g., hot-air solder leveling) and assembly (reflow, wave soldering, rework), it is not unexpected to experience failures after 10 or fewer of these thermal cycles.

This raises even more concerns with respect to lead-free assembly. Multiple lead-free assembly cycles with higher peak reflow temperatures (245–260°C) places even greater thermal strain on the PTH when compared to conventional tin-lead assembly. In addition, the laminate resin material chosen for the fabrication may contribute to PTH failure. Why? Consider the property of Td (temperature of decomposition). Td is not the same as Tg. Temperature of decomposi-

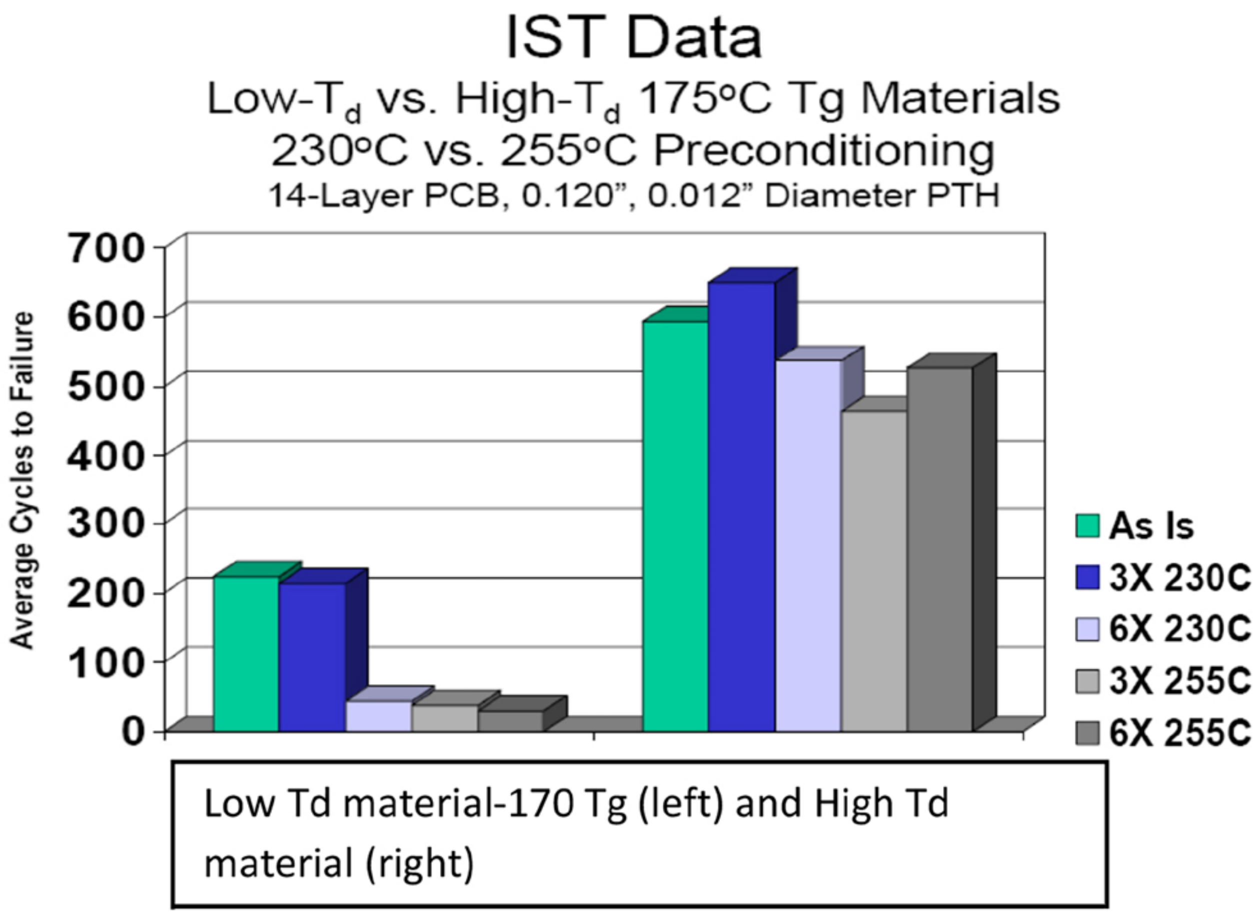


Figure 4: IST comparison of two resin systems—similar Tg but different Td.

tion is that temperature at which the resin material loses 5% or more of its weight. The weight loss may have deleterious effects on the performance and reliability of the PTH. This author suggests that for high-reliability performance requirements, choose a resin material with a Td of 340°C or above. An IPC test method has been developed to determine Td[2].

Certainly there are other factors that contribute to PTH reliability. And these will be the subject of a future column. But for now, Figure 4 shows that there are stark differences in IST failure results when comparing low Td material with higher Td.

Summary

Understanding and controlling the many factors that influence PTH reliability is a complex and often not absolute process. Part 1 of this column provided some background into failure mechanisms in the PTH. The concept of Td was introduced, as well as how that resin property impacts PTH reliability. **PCB**

References

1. Correspondence with Bill Birch, PWB Interconnect Solutions.

2. IPC Test Methods Manual TM-650, www.ipc.org.

Michael Carano is VP of technology and business development for RBP Chemical Technology. To reach Carano, or read past columns, click here.

Digital Imaging Update

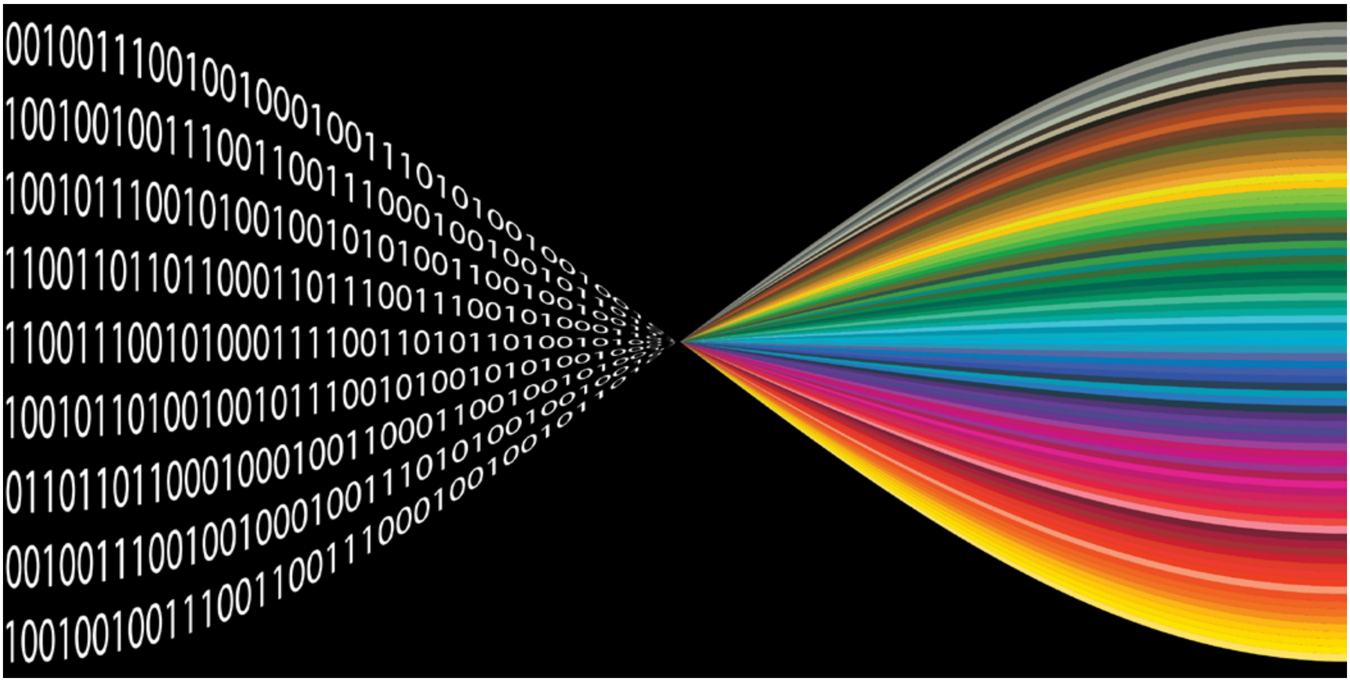
by Karl Dietz
KARL DIETZ CONSULTING

Through the years, I have repeatedly covered and updated digital imaging in this column, from as far back as 1997 in *CircuiTree,* through a column in this magazine in November 2015. Several reasons for this extended coverage include the fact that technology had a slow, long incubation time that eventually led to accelerated improvements and acceptance for mass production. It might also be argued that, next to the development of microvia technologies, digital imaging is probably the most innovative technology to achieve high-density interconnects in acceptable yields.

It is worth mentioning that digital imaging is a more appropriate term to refer to this technology than laser direct imaging (LDI) because LDI is just one example of digital imaging, albeit its pioneering version.

The advantages of digital circuitization techniques have been described in detail by suppliers of equipment and photoresist. Since phototool generation and conditioning are omitted, there is the advantage of shorter lead time. Small lots can be customized at no extra cost (e.g., with added date and lot number information). Maybe the biggest advantage is the ability to scale (i.e., to change the dimension of each individual exposure for best fit to reference points on an underlying pattern of a multilayer structure). However, early digital imaging systems had substantial drawbacks, such as Orbotech's DP100 which used an argon ion laser with limited radiation power, high power usage, and high cooling requirements.

For years, laser direct imaging (LDI) was synonymous with digital imaging. While most early, commercially successful digital processes involved the use of lasers, other more recent processes use non-laser light sources such as LEDs (light emitting diodes) that consume less power, last longer, and have higher light intensity output. Alternatively, various types of mercury lamps are employed, with more than one wavelength used for imaging. Others use inkjet technology to build digitally imaged patterns such as legend print, soldermask or etch resist. They



all have in common the building of a pattern, pixel by pixel, and they employ digital on/off switches to form the pattern. The switch might be an optical modulator as in laser direct imaging, or an array of LCPs (liquid crystal polymer cells) that can be rendered translucent or opaque by addressing it with an electrical pulse. Or the switch might be micro-mirrors on a chip, such as Texas Instruments' Digital Micromirror Device™ (DMD), whereby tiny mirrors are addressed with an electric pulse so that the mirror is either tilted to direct the light to the substrate or away from the substrate.

The following is an overview of developmental and commercial digital imaging systems introduced more recently:

The French supplier of imaging systems Altix-Automa-Tech introduced its ADIX-System. It is based on an advanced high-power LED radiation source (ALDS), a dual multi-wavelength UV-LED (365, 385, 395, and 405nm), and Digital Micromirror Devices™ (DMDs). The system is available with two, four, or six light heads. The system is suitable for rigid and flex substrates and has automatic handling options. Earlier systems using DMDs include:

- ORC's DI-Impact (formerly by Pentax)
- Hitachi DE imagers DE-H, DE-S, and DE-F series
- MIVA Technologies GmbH, Germany, Miva 2600X Direct Imager
- Maskless Lithography's DMD-based system (USA), using a mercury arc light source, and
- Aiscent Technologies Inc. (Canada)

The Korean company AJUHITEK entered the market with its EP digital imager series that is using a laser diode radiation source with the wavelength of 405 nm.

HAN's Laser is the only Chinese supplier of direct imagers to the best of my knowledge.

The Japanese direct imager suppliers ADTEC, DNS, ORC and Via Mechanics continue to introduce improved systems.

The Swiss supplier PrintProcess introduced its Appollon-DI-F10 (manual single frontload) and the Apollon-DI-A11 (auto double-side reverse inline). Line width resolution is 30 to 20 micron depending on photoresist type. There are 1–7 recording heads (8 optional). The light source is UV-LED, multiple wavelengths in the range of 350 to 420 nm.

KLEO Halbleitertechnik GmbH, Germany, has supplied direct imagers since 2009, with systems in production in Germany and Switzerland. The KLEO-LDI-System CB20HV-Twinstage uses a 405 nm wavelength laser diode. The 405 nm radiation source is dominant in Asia. Photoresists (dry film and liquid) suitable for exposure at 405 nm are available from Hitachi, DuPont, Atotech, Eternal, Kolon and Elga Europe.

Orbotech has installed over 1000 direct imagers. Its Nuvogo DI System is designed for mass production of advanced HDI/flex and rigid flex applications, according to Orbotech. The Nuvogo™ 800 is compatible with nearly all resist types. Its resolution is capable of 18-micron lines and spaces. Nuvogo makes use of Orbotech's well-established Large-Scan-Optics technology (LSO). The MultiWave Laser Technology™ uses a multi-wavelength laser beam of high intensity so that lower cost resist with standard photosensitivity can be used for high throughput (up to 7,000 panels/day/line) with optimal line structure.

Manz, a supplier of wet processing chemistry modules, has diversified into digital imaging with its SpeedLight 2D system. It features a twin stage, allowing imaging of the first panel while a second panel is being registered. The imager consists of 288 laser diode beams that are modulated by nine polygon mirror modules.

Limata GmbH, the German supplier of laser direct imaging systems used in small lot PCB production and photochemical machining, has developed its established UV-P models into the advanced UV-R Series. It makes use of the latest UV diode lasers with multiple wavelengths and a long lifetime. Both models are equipped with 1–8 laser heads. Resolution down to 25-micron lines and spaces is being achieved. A pre-registration module can address up to 64 registration targets. Soldermasks can be imaged using up to three different wavelengths for maximum intensity to accommodate less photo-sensitive masks. A robotic load and unload station can be added for enhanced throughput and optimal interface with other processing equipment.

Aiscent Technologies, Inc., a Canadian supplier, has done research and development in digital imaging for more than 15 years. Its systems use DMD® based photolithography and a proprietary high power laser. Double-sided models currently offered are suitable for the production of PCBs, high-resolution photomasks, digital screen imaging, and other customized industrial uses.

Schmoll Maschinen, the well-known supplier of mechanical and laser drilling machines, is now also offering a DDI (digital direct imaging) system, ideal for prototyping innerlayer, outerlayer, and soldermask images. It is based on semiconductor laser diodes and large (wide) optics. The imager is equipped with two to eight diode lasers and can handle a maximum panel size of 610 x 535 mm. Schmoll also offers MDI (micromirror digital imaging) systems. The systems are available as a single-table unit or with a double stage for higher throughput. The units use high-power LEDs and DMD® with multiple waverlengths from 365 to 405 nm.

The Swiss company First EIE SA supplies photoplotters, inkjet printers and direct imagers suitable for quick-turn, small-lot size shops. Its direct imager is named EDI500. The light source technology is based on TI's DMD® devices with an advanced UV lens and very high pressure mercury arc lamp. Panel registration is done with a built-in CCD camera or by manual pin registration. Maximum panel size is 610 x 660 mm.

Visitech is a Norwegian company that supplies optical modules (optical subsystems) for direct imagers. The Luxbeam Lithography System (LLS) is based on TI's DLP® (micromirrors) and multiwavelength LED light source, emitting in the range of 350–440 nm. Three modules are available with different resolution capabilities: LLS 10 (10–12 micron line/space), LLS 25 (25 micron line/space), and LLS 50 (50 micron line/space). Optical multiplexing allows to achieve the very fine resolution.

There have been advances in photoresist photospeed to reduce exposure time with lasers, but there are potential drawbacks with high speed photoresists with regard to yellow light sensitivity, shelf life, and resolution. High photospeed is not so much an issue with LED light sources and the use of multiple wavelengths, so that standard dry film photoresists can be used. **PCB**

Karl Dietz is president of Karl Dietz Consulting LLC. He offers consulting services and tutorials in the field of circuit board and substrate fabrication technology. To view past columns or to reach Dietz, click here. Dietz may also be reached by phone at (001) 919-870-6230.

New Robot Mimics Vertebrate Motion

EPFL scientists invented a robot that mimics a salamander's gait with unprecedented detail. It features 3D-printed bones, motorized joints and electronic circuitry as its "nervous system." Inspired by the species *Pleurodeles waltl,* "Pleurobot" can walk and even swim underwater. The results are featured in the Royal Society journal *Interface.*

Auke Ijspeert and his team at EPFL's Biorobotics Laboratory have built salamanderrobots before, but this is the first robot that's based on the 3D motion of the animal's skeleton. The scientists used X-ray videos of a salamander from the top and the side, tracking up to 64 points along its skeleton.

Give Your Literature Some Lovin'

by Barry Lee Cohen
LAUNCH COMMUNICATIONS

Collateral is such an ugly word. As the late, great Rodney Dangerfield would have put it, brochures, sell sheets, process manuals, and other sales support tools often get no respect in our digital world. Even the convenience of downloading a PDF is scoffed at by today's millennials who rely on the "Almighty App" and the "All-Knowing Cloud" to view, digest and store information.

Whatever twisted mind came up with the word "collateral" to denote support literature is not giving this critical content the high credibility it deserves. Today, the label "collateral marketing" spreads this cancerous term by including compelling white papers, case studies, video, and web content, thereby further demeaning the importance of the information. I've always half-joked that you may as well call the literary masterpieces that I and others slave over "collateral damage."

Collateral damage: injury inflicted on something other than an intended target[1]

I've actually witnessed the embarrassment on the face of a young, super-smart colleague, as if he was apologizing for admitting that he downloaded the PDF because it was easier to follow and read. Why, the shame of it all! May he drop his head in despair and walk the halls of industry tech conferences wearing the collateral letter "C" on his chest! All should succumb to the sanctity of the Cloud and the absolute authority of the App!

But seriously...

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There are few in our industry that have his experience and expertise in just about every aspect of the business. Dan knows what works, and perhaps more importantly, what doesn't.

When additional expertise is needed, or when senior management just needs an independent opinion, companies large and small alike get the guidance of Fein-Line Associates, especially in the areas of New Product Market Entry and M&A Due Diligence.

In our business, there's a lot on the line, not just sometimes, but every time. The line between success and the alternative can be razor thin. That's why winning companies choose Fein-Line time after time.

Dan (Baer) Feinberg
Fein-Line Associates

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graphic, advertisement or social media posting. Ensuring that literature is composed in a tone that conveys your organization's vision with the text and images that "speak the voice" of the targeted readership is essential. Literature, when constructed correctly, consistently communicates the meaning and relevance of the company's brand.

Given the time and thought you devote to generating documentation to support your company's product or service, literature takes no back seat to the fancy-schmancy digital world. It may not have the dynamics of digital, however, the "deep-dive" contents contained in brochures, case studies and selection guides (to name a few) continue to be highly coveted by customers and prospects. Literature is equally used as strategic follow-up by sales and marketing teams to reinforce site visits and showcase technical and applications expertise. And—news alert—that collateral (ouch!) is often repurposed for other editorial and promotional purposes.

So, go ahead—give your literature some lovin' and the respect that it deserves. It may be deemed old-school by some, but it can and should become a powerful part of an integrated program or a singular objective. **PCB**

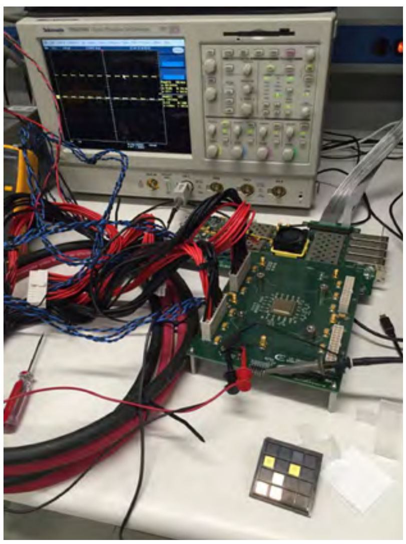
References

1. Merriam-webster.com

Barry Cohen is president and managing director of Launch Communications. He can be reached by clicking here.

World's First 1,000-processor Chip

A microchip containing 1,000 independent programmable processors has been designed by a team at the University of California, Davis, Department of Electrical and Computer Engineering. The energy-efficient "KiloCore" chip has a maximum computation rate of 1.78 trillion instructions per second and contains 621 million transistors. The KiloCore was presented at the 2016 Symposium on VLSI Technology and Circuits in Honolulu on June 16.



"To the best of our knowledge, it is the world's first 1,000-processor chip and it is the highest clock-rate processor ever designed in a university," said Bevan Baas, professor of electrical and computer engineering, who led the team that designed the chip architecture. While other multiple-processor chips have been created, none exceed about 300 processors. Most were created for research purposes and few are sold commercially. The KiloCore chip was fabricated by IBM using their 32 nm CMOS technology.

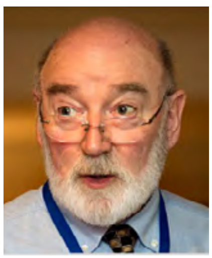
Each processor core can run its own small program independently of the others, which is a fundamentally more flexible approach than so-called Single-Instruction-Multiple-Data approaches utilized by processors such as GPUs; the idea is to break an application up into many small pieces, each of which can run in parallel on different processors, enabling high throughput with lower energy use, Baas said.

Applications already developed for the chip include wireless coding/decoding, video processing, encryption, and others involving large amounts of parallel data such as scientific data applications and datacenter record processing.

The team has completed a compiler and automatic program mapping tools for use in programming the chip.

Recent Highlights from PCB007

1 Institute of Circuit Technology Annual Symposium



On June 1, Technical Director Bill Wilkie introduced the 42nd Annual Symposium of the Institute of Circuit Technology, at the Motorcycle Museum in Birmingham, UK, commenting upon the success of the recent Foundation Course and acknowledging the sterling efforts of his course tutors, although recognising that some of his longest-standing experts were now retiring.

2 Weiner's World

Gen Consulting Company (GCC) has issued the Radiant Insights report "Global HDI Printed Circuit Board Market Forecast and Analysis 2016–2021." The report provides a detailed analysis of worldwide markets for HDI printed circuit boards from 2011–2016, and provides market forecasts for 2016–2021 by region/country and subsectors.

3 EIPC Summer Conference 2016, Day 2: Strategies to Maintain Profitability in the European PCB Industry


Professor Martin Goosey

Delegates awoke to a gloomy Scottish morning on the second day of the EIPC Summer Conference 2016. One or two who maybe overindulged in the whisky on the previous evening had some difficulty in finding time for breakfast before the conference proceedings, but the atmosphere in the meeting room was brighter than the weather outside, as Professor Martin Goosey introduced the day's programme.

4 Happy's Essential Skills: Learning Theory/Learning Curves

Learning is not instantaneous. Nor is progress made in a steady manner, but at a rate that is typified by one of two basic patterns. In some cases, plateaus will be seen in learning curves. These are caused by factors such as fatigue, poor motivation, loss of interest, or needing time to absorb all the material before progressing to new.

5 Graphic PLC... Are the Rumors True?

During a visit to Europe recently, I-Connect007's Barry Matties met with Rex Rozario to get to the bottom of the rumors and speculation regarding the sale of his company, Graphic PLC.

6 EIPC Summer Conference 2016, Day 1: Strategies to Maintain Profitability in the European PCB Industry

Resplendent in the kilt, EIPC chairman Alun Morgan welcomed a large and enthusiastic gathering of printed circuit professionals from all over Europe and as far afield as the USA, Canada and Russia, to the EIPC Summer Conference 2016 in Edinburgh, Scotland's cosmopolitan capital city.

7 It's Only Common Sense: Elevate the Conversation to get Closer to your Customers

So we all think we are doing a pretty good job getting to know our customers, right? We think because we know what market they are in and what they build, and have some sort of idea of what they need we are in pretty good shape, right?

8 All About Flex: Flexible Circuit Fabrication and Cleanroom Manufacturing

Facility cleanliness is a vital part of process control for flexible circuit fabricators. As higher density requirements continue a relentless drive toward finer traces and spaces, particles and foreign material can cause problems in a number of operations.

9 Standard of Excellence: LED and Metal-Backed Technology—Today and in the Future

Probably one of the hottest, or should I say coolest, technologies today is LED. I would also venture to say it is one of the fastest growing as well. All you have to do is look around you can see evidence of this everywhere from holiday lights in your home and Jumbotrons at sports arenas, to highway and business signage. The lighting industry is now dominated by LED technology.

10 Flexible Electronics Market to Reach $87.2 Billion by 2024

The global flexible electronics market was $20.85 billion in 2015, which is estimated to reach $87.2 billion by 2024, according to a new report by Grand View Research, Inc.

GRAND VIEW RESEARCH

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Events

For IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar of Events, click here.

For the complete PCB007 Calendar of Events, click here.

IPCA EXPO 2016
August 18–20, 2016
Delhi, India

Medical Electronics Symposium
September 14–15, 2016
Marylhurst, Oregon, USA

24th FED Conference
September 15–16, 2016
Bonn, Germany

IPC India/electronica India 2016/ productronica India 2016
September 21–23, 2016
Bengaluru, India

IPC Fall Committee Meetings
September 24–30, 2016
Rosemont, Illinois, USA

SMTA International 2016
September 25–29, 2016
Rosemont, Illinois, USA

electronicAsia
October 13–16, 2016
Hong Kong

TPCA Show 2016
October 26–28, 2016
Taipei, Taiwan

Electronica
November 8–11, 2016
Munich, Germany

FUTURECAR: New Era of Automotive Electronics Workshop
November 9–10, 2016
Atlanta, Georgia, USA

International Printed Circuit & Apex South China Fair (HKPCA)
December 7–9, 2016
Shenzhen, China

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SEPTEMBER—
A close look at the **Military/Aerospace electronics industry**