PCB007 PRESENTS

June 2014

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FLEX

Substrates:
Polyester Film for the Flexible Electronics Industry

by Scott Gordon, et al

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Flex Circuitry

This month, *The PCB Magazine* feature contributors examine the realm of flex circuitry, from the basics of polymer thick film flex circuits, to hybrid stretchable circuits on silicone substrates.

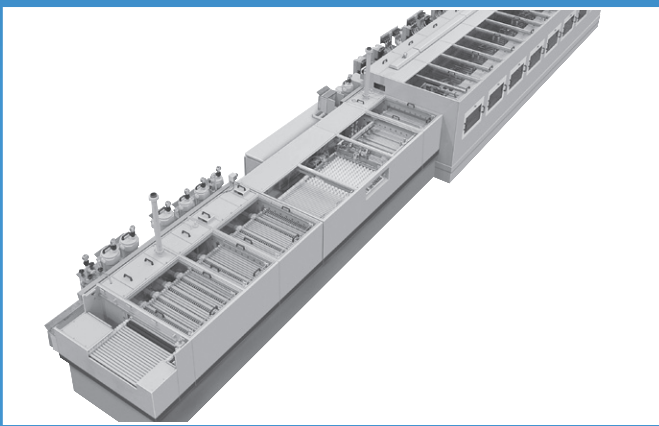
Electronics

Systems Technology

UTS-xs – The Universal Transport System for Horizontal Processing of Flex and Ultra-Thin Material

Flexible PCB

Rinse with UTS-xs features



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FLEX CIRCUITRY

We Saw This Coming

by Ray Rasmussen
I-CONNECT007

There have been quite a few predictions and studies, along with plenty of wishful thinking, about the cost of manufacturing in the U.S. The onshoring/re-shoring movement has gained a lot of attention from media like ours over the last couple of years. IPC even issued a report last year providing their take on the movement, which garnered a lot of interest from the industry.

Now, The Boston Consulting Group (BCG), a global management consultant, has released new research on the "dramatic" change of manufacturing cost competitiveness around the world. BCG's press release is entitled, "Study Reveals Striking Shifts in Global Manufacturing Costs over the Past Decade." I found the use of the word "striking" to be interesting. It almost leads me to believe they were surprised by the trends in manufacturing costs.

For those of us watching the shift over the last few years, it isn't striking at all. It's been coming for some time. As I've said in the past, all things come back into balance. The rising costs in Asia, and China in particular, have made it very clear that you can only sustain dirt-cheap manufacturing for so long. At some point, lax or non-existent labor and environmental standards, ridiculous lending policies, manipulated currencies, etc., will yield a day of reckoning. People get tired of breathing bad air and drinking polluted water. Trading partners say "enough is enough" and demand fair currency valuations. And banks struggle to survive under the weight of bad loans made during the heady days of unbridled growth.

With its success, China has opened the door to all kinds of ills associated with modern, democratic societies: regulations to improve the quality of the air and water along with some basic standards for worker safety and income. The government has had to loosen controls over the populace as well, to keep order and to sustain the illusion of a free society for most of their people. The Chinese people are getting smarter. They're starting to travel the world for business and pleasure. They want the freedoms associated with a modern, democratic society. This illusion has helped perpetuate growth by

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placating their international trading partners and through the continued success of a growing middle class. Being part of the WTO has its advantages. I do believe the leadership in China wants to have a more open, democratic society, really. They're getting there. I don't want to condone their absolute, dictatorial control and lack of personal freedoms, but they have been able to pull off an economic miracle with the help of the West, which has lifted some of their people out of poverty. It ain't all bad, if you're one of those middle-class Chinese.

The release goes on to state that the UK is the low-cost producer in Western Europe, which isn't surprising. They've held a top spot for some time. They've had very friendly business policies since the Margaret Thatcher days. French government activist Olivier Cadic, the founder of PCB007, moved from Paris to the UK to take advantage of the lower costs, in part to strengthen the competitiveness of his businesses, but more likely, to send a message to the French government.

Mexico now has lower manufacturing costs than China. This news does a couple things for the U.S. First, it potentially brings manufacturing closer to home, to the same time zones and to a culture Americans are more familiar with. Second, it takes the pressure off of the border with Mexico. As more Mexicans find work in their own factories, there is less need to seek employment in "El Norte."

A Few Surprises

The cost of manufacturing in Brazil was a surprise and doesn't seem to make sense. They now call Brazil "one of the highest-cost countries." Another report from the World Economic Forum said this: "Brazil's manufacturing competitiveness is expected to strengthen over the next several years. Driven by ongoing investment in infrastructure in preparation for the 2014 World Cup and 2016 Olympic Games, relevant changes in the energy sector, and other recent policy reforms, Brazil appears to be favourably positioned for the future regarding manufacturing competitiveness." There seems to be a disconnect between these two organizations.

A pleasant surprise was that U.S. manufacturing is now on par with costs in Eastern Europe. Here's another quote from BCG: "Overall costs in the U.S., meanwhile, are 10–25% lower than those of the world's ten leading goods-exporting nations other than China." Energy: that's the ticket. We have the market; we have low-cost and very reliable sources of energy, a stable currency, great trading partners, a well-educated, hard-working labor force and a solid infrastructure to reliably produce and move goods to market.

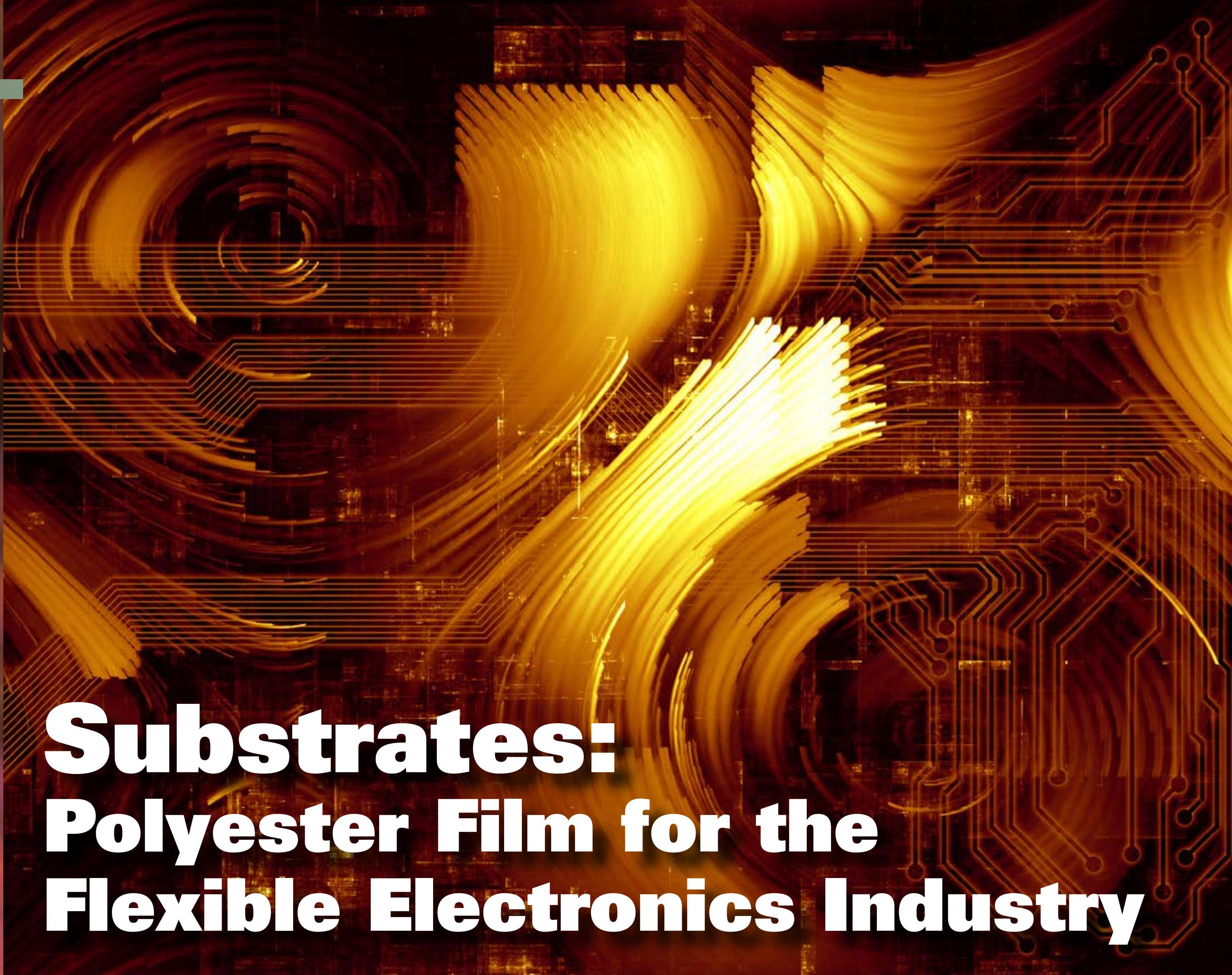
BCG's study looks at four direct economic drivers of manufacturing competitiveness: wages, productivity growth, energy costs, and currency exchange rates. Harold L. Sirkin, a BCG senior partner and a co-author of the analysis said this:

"Many companies are making manufacturing investment decisions on the basis of a decades-old worldview that is sorely out of date. They still see North America and western Europe as high cost and Latin America, eastern Europe, and most of Asia—especially China—as low cost. In reality, there are now high- and low-cost countries in nearly every region of the world."

Based what we've seen as the economies of those low-cost producers improve, costs climb, as well. There are no more "Chinas" as far as I can see so we won't experience that phenomenon again, anytime soon. Those emerging low cost producers will take business from China, Mexico and elsewhere, in small bites here and there, serving mostly local and some international markets. I see the shift to automation removing most of the cost advantages associated with low-cost producers overseas in the not-too-distant future. With that, economies will continue to equalize as we move into the next decades.

That's the way I see it. **PCB**

Ray Rasmussen is the publisher and chief editor for I-Connect007 Publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuiTree Magazine.* To read past columns, or to contact Rasmussen, click here.



Substrates: Polyester Film for the Flexible Electronics Industry

by Scott Gordon, William MacDonald, Robert Rustin, Duncan Mackerron, John Flett, Valentijn von Morgen, Robert Eveson and Karl Rakos
DUPONT TEIJIN FILMS

Introduction

Polyester film substrates have been widely used in making membrane touch switches and other flexible and printed electronic devices for more than 30 years. However, the early 2000s brought about an explosion of interest in additive printed electronics to replace subtractive etched circuitry in terms of materials development and device technologies aimed at defining new business opportunities. The opportunity to exploit flexible substrates in roll-to-roll production has gained the interest of the plastic films and associated film processing and coating industries. This next generation of flexible electronics technologies has required materials suppliers to deliver improved functionalities to the device developers in fields as wide as electrophoretic displays, backplanes, barrier films, photovoltaics, sensors, and more.

The terms flexible and printed electronics can be defined in many ways, but these definitions will not be debated here. It is commonly understood that commercial polyester film substrate technology provides a key cost-effective building block for devices requiring deposition of functional materials. However it is less commonly known that there are many varieties of polyester film, and that the polymers and film coatings can be tailored to meet the end user's evolving film requirements.

It is now possible to compare and contrast the vision of what the early thoughts on material requirements were and how the technology might be exploited, with what has emerged.


"No great thing is created suddenly."
-Epictetus

Physical Form/Manufacturing Route

Initially, the potential to prepare displays based on a flexible substrate opened up the possibility of thin, robust, rollable, color displays based on OLED technology, but the technical difficulties in developing a high barrier on a flexible substrate has limited the development of flexible color displays. The prototype rollable and flexible displays sampled to the market have been based on electrophoretic black and white displays, which were superseded by the introduction of the smart phones and tablet based devices. The consumer now expects the sophistication of full color displays, and the public acceptance of the tablet form has mostly negated the desire for a rollable display concept. Despite this and the fact that present day glass-based displays remain largely flat, ruggedness and light weight remain desirable attributes that displays on flexible substrates can offer. In terms of manufacture, the vision of a roll of film at one end and devices emerging at the other end was postulated. Although R2R is used extensively for specific steps in substrate production including film manufacture, conductive coatings and barrier coatings, device manufacture is still largely batch based, partly because this fits best with the semiconductor industry's existing manufacturing tooling equipment.

Film in Use

Films now find use in a much broader range of application areas than the OLED displays that were originally envisioned (e.g., printed circuitry, printed memory, electrophoretic displays, sensors, OLED lighting and flexible PV devices). In addition, flexible film is used extensively in rigid electronic devices (e.g., touchscreen) and in light management films in LCD displays.

These evolving trends have influenced flexible substrate development throughout the past decade, so this article will take a high-level overview of the substrate evolution for flexible electronics, exploring the issues associated with substrate development and selection. We will then discuss the latest polyester film developments in support of the flexible electronics and PV industry.

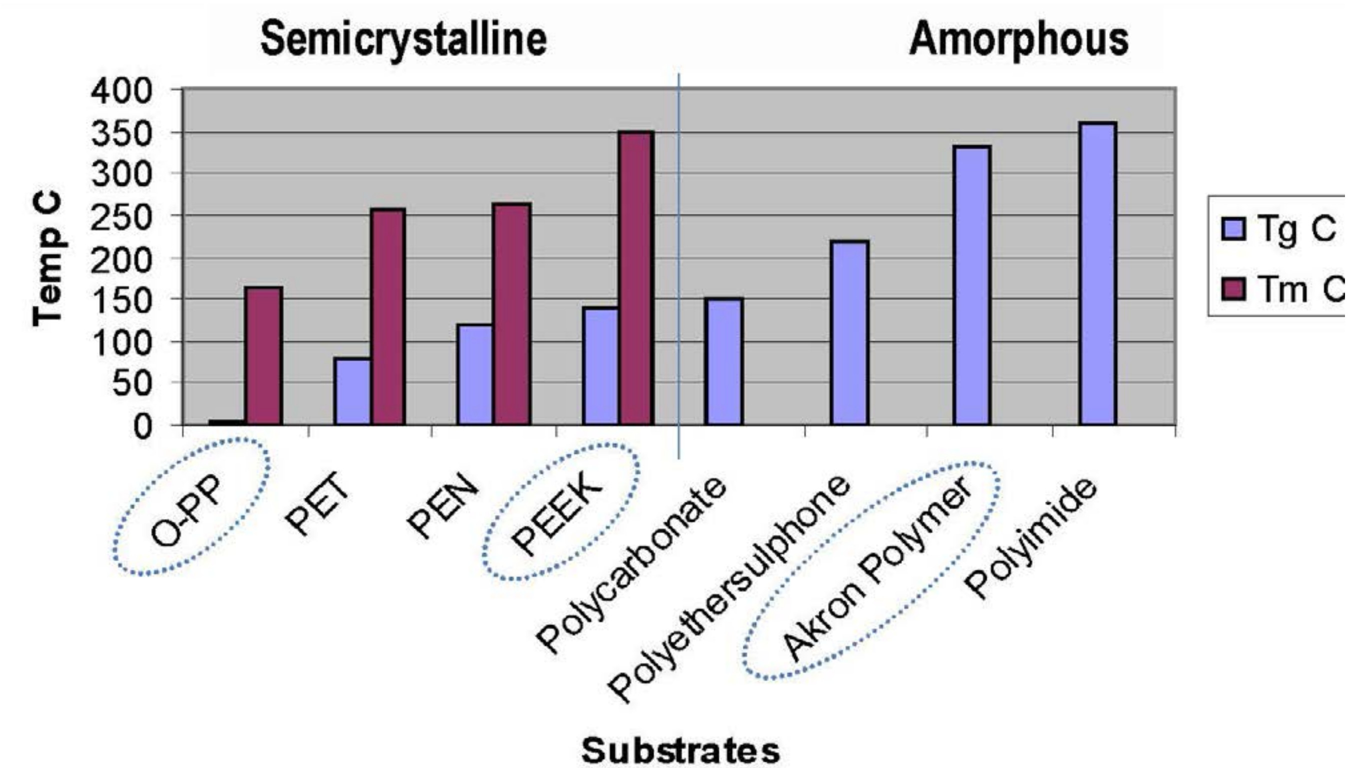


Figure 1: Common substrate films for flexible electronics.

The Flexible Substrate Property Challenge

Over a decade ago, the film's dimensional reproducibility at processing temperatures, surface smoothness, high barrier, and inertness to the chemicals used in processing were highlighted as the key property requirements for film substrates. Cost and commercial availability have emerged as further film requirements as device manufacturers have moved from demonstrators to prototypes to commercial manufacture with the realization that only film manufactured at a commercial scale is likely to meet the consistency and quality required for volume manufacturing. Figure 1 shows the main plastic film types currently under consideration by the flexible electronics industries.

Films can be categorised into semicrystalline and amorphous. The combination of dimensional reproducibility, surface quality , chemical inertness, cost, and commercial availability have given biaxially oriented, semicrystalline, heat-stabilized polyester films a leading position in these emerging markets. The films that are circled have emerged as substrates of interest over the past decade. Oriented polypropylene film (O-PP) is finding use in "simple" printed electronic applications where processing and performance at higher temperatures is not required. Polyether ether ketone (PEEK) is the premier high performance semicrystalline engineering polymer and offers an excellent high temperature, chemical inertness property set. The amorphous high T_g resin developed by Akron Polymer Systems offers high temperature processing. However new polymer and or film developments have the issue of the prohibitive costs of scaling up to a commercial quality film line for what remains at present a low-volume market. Other materials such as stainless steel and flexible glass have also been worked on. Stainless steel finds use in PV devices, but is not being actively used in flexible electronics. Flexible glass offers transparency and excellent barrier properties, but faces the challenges of scale up to a commercial scale, plus other technical and processing issues including edge cracking.

Experience over the past decade has shown that "off the shelf" material is unlikely to have the complete desired property set required, but good progress may be achieved when the device manufacturer and the substrate supplier work together to match process capability to an optimized substrate property set. Taking the property set highlighted earlier and using the biaxially oriented polyester films polyethylene terephthalate (PET) and polyethylene naphthalate (PEN) as examples, it is possible to review the progress that has been achieved.

1. Flexible Transparent High Barrier

Considerable progress has been made in developing high barrier films, and commercial products are now available. However, achieving a cost effect barrier of $>10^{-5}$ g/m2/day for moisture and $>10^{-5}$ mL/m^2/day remains a key challenge and a rate-limiting step in developing commercial quality flexible OLED displays. A pristine film surface is one of the key enablers to achieving this and progress towards this will be discussed later.

2. Dimensionally Reproducibility

The Melinex® (PET) and Teonex® (PEN) family of polyester films exhibit dimensional stability up to approximately 150˚C and 200˚C respectively, and PEN films have been shown to survive solder reflow temperatures >230˚C. The dimensional reproducibility of the films can be enhanced further by the use of a rigid carrier, the use of process technology that allows for predictable dimensional change, and the control of moisture in the processing atmosphere. Once a certain level of shrinkage is achieved, the consistent dimensional reproducibility is more important than further reductions in shrinkage. Companies such as Plastic Logic, Polymer Vision and the Flexible Electronics and Display Center at Arizona State University have demonstrated the successful manufacture of thin film transistor (TFT) backplanes on polyester film, proving that the required dimensional reproducibility can be achieved.

3. Surface Quality

Defects on the surface of the film are clearly undesirable and can lead to pinhole defects in subsequent barrier coatings, or line outs and spot defects in displays. It is probably impossible to achieve glass-like perfection in terms of surface smoothness with a plastic film; however, it can be argued that perfection is not actually required. What is important instead is to understand what defects are critical to a device manufacture, and to target and eliminate those defects where possible in a cost effective manner. Film makers and users continue to research surface quality, and experience over the past decade has shown that external debris (dust, externally introduced debris, scratches, etc.) rather than internal contamination is the major issue. One accepted approach to overcome this has been to cover any defects or marks on the surface with a planarizing coating, and it has been demonstrated that the introduction of such coatings significantly reduces the defect count on the film's surface.

White light interferometry has been used extensively to character the surface of the films, but the use of roughness average (Ra) and root mean square roughness (Rq) can be misleading as they tend to be measured over a small sampling area and do not capture the occasional peaks that occur on the sample size of a display. Recent efforts have led to the development of a large area metrology (LAM) tool—the first of its type. This device has the capability to defect map the surface of film fast and precisely, achieving the optimum lateral resolution obtainable from white light interferometry. The equipment was designed to help distinguish between both intrinsic (polymeric based) and extrinsic (external, air borne debris) defects.

Typical output:

- Sampling area = 35 x 35 cm
- Map of intrinsic and extrinsic defects, precise locations registered for compositional analysis
- Full X'Y'Z measurements of the surface defects, enabling significance testing

Such output can then be used to identify defects critical to device manufacture, and help determine the impact on the effectiveness of removal strategies. An example of this is where the LAM tool was used in support of a UK government funded program (HighQSurf), the aim

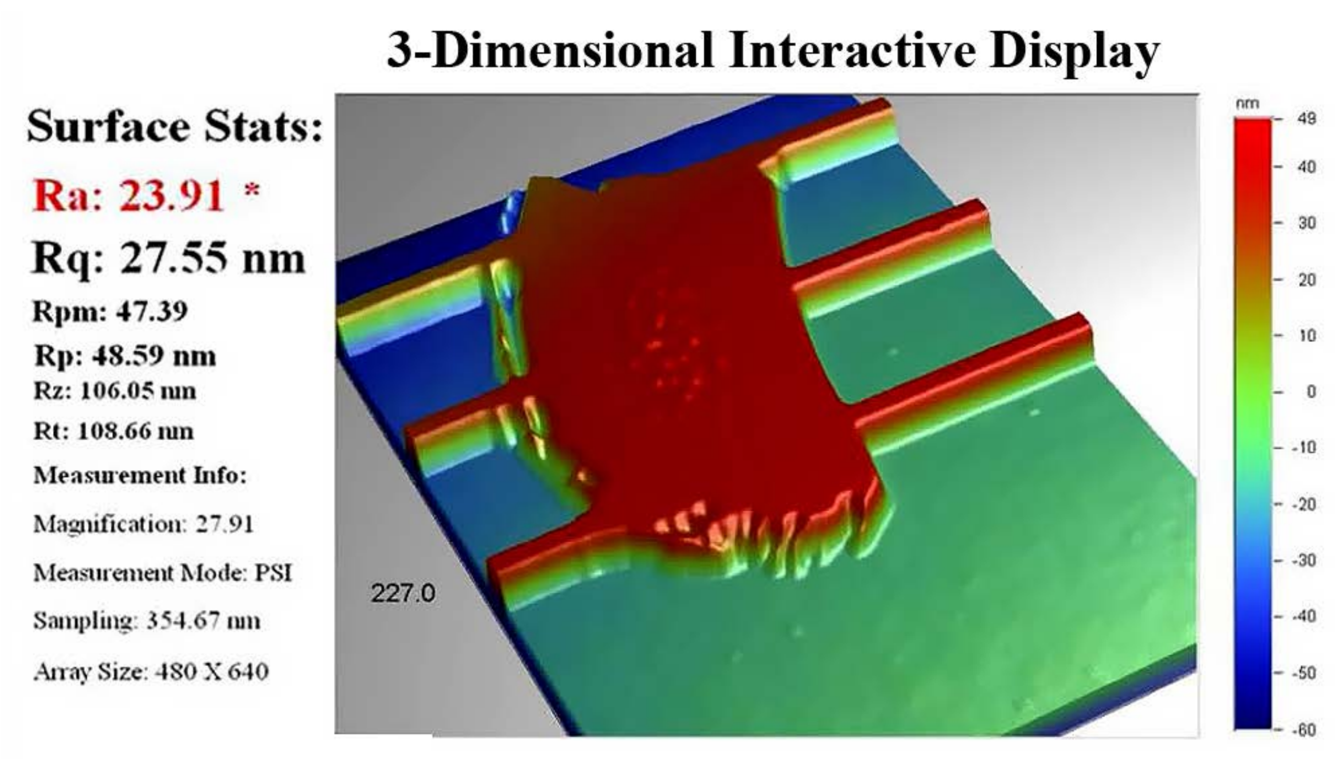
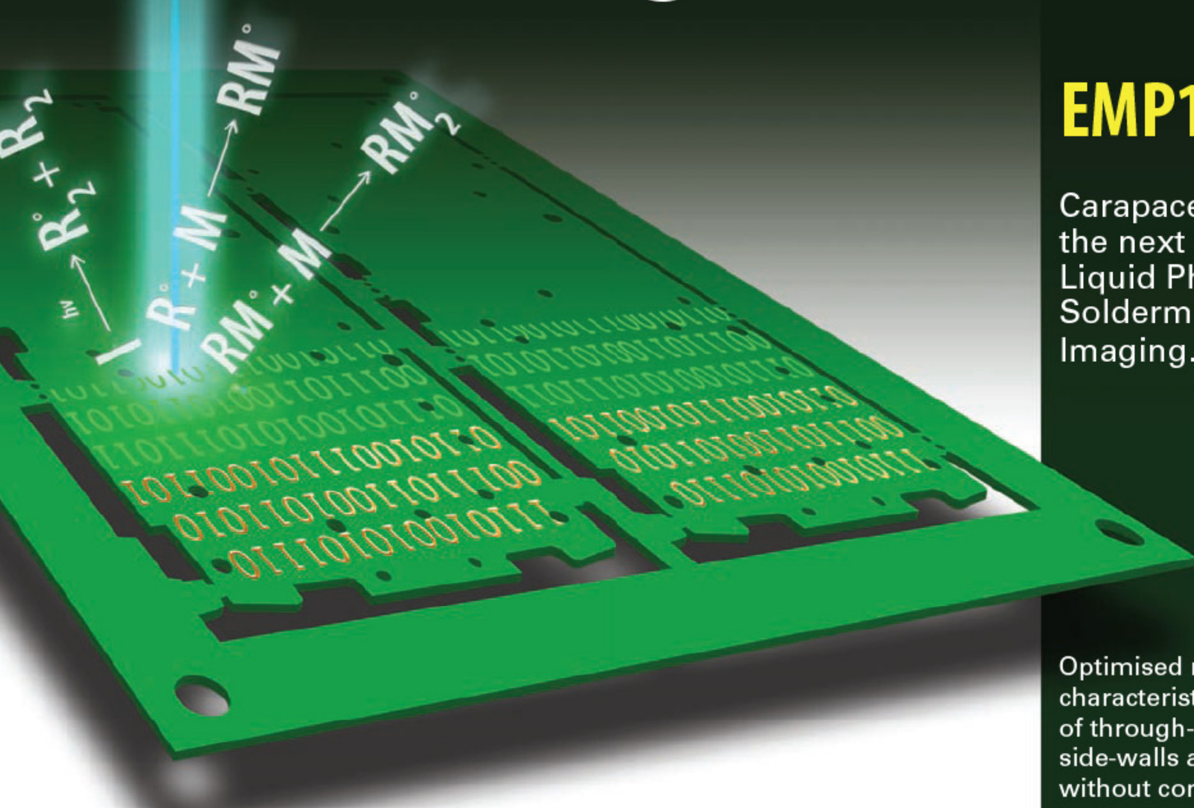


Figure 2: LAM image of Plastic Logic (PL) device mask showing debris.

Direct Image Solder Mask



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of which was to achieve a defect reduced surface by

a) Characterizing the effectiveness of substrate cleaning techniques
b) Identifying the defects critical to device manufacture and tracking where the defects were introduced in the manufacture of the film and subsequent handling and transport of film into a device manufacturers facilities
c) Identifying and applying strategies to reduce defects and improve device manufacturing yields

Working with one of the project partners to identify defects with the potential to cause shorts and line outs, etc., an attempt was made to work back through film handling to identify where the defects were introduced.

The image in Figure 2 was taken from a Plastic Logic device "mask,"—comprising an array of circuit lines 40 µm apart, 10 µm wide and 50 nm high. The mask plate was then electrically tested with an X Y grid array to locate the short regions, which were studied using the LAM. In this case, a particle of extraneous debris gave rise to a short. The defect regions were first quantified in terms of height significance; further analysis was then carried out to determine the composition of the defect. This particular study revealed that virtually all shorts were due to externally introduced detritus.

Within this same "HighQSurf" program, a major audit was performed of the film as it was entering the manufacturer's clean rooms. In summary, this audit revealed that the debris on the surface was derived from human, packaging and post-process interactions and not the initial film manufacture. The primary conclusions suggest there is considerable scope for improving the surface film quality by addressing hygiene factors. Attention to detail is one aspect of this, but given that film handling and transport is unavoidable, improved methods of surface cleaning become important. Trials involving program partner Teknek led to their development of their Nanocleen roller technology with the composition and configuration of rollers designed to remove sub-micron as well as larger particles. Improvements in static control and the provision of a protect film on the surface of the planarized films have led to further improvements in film surface quality and the adoption and exploitation of techniques such as described above have taken Plastic Logic to the stage where they now achieve the same yields on polyester film as they have achieved on glass.

New Film Developments

In addition to the above, new films are being developed to make further improvements targeting surface cleanliness, but also to address additional film requirements. These include:

1. "On Demand" Clean Film

The polyester film surface on manufacture is almost glass smooth, but as discussed above the surface becomes compromised during the subsequent handling and transport processes. One approach currently under development is to exploit coextrusion technology. As shown in Figure 3, a sacrificial film layer is coextruded onto the surface of the film substrate during the film manufacture. The polyester film surface be-

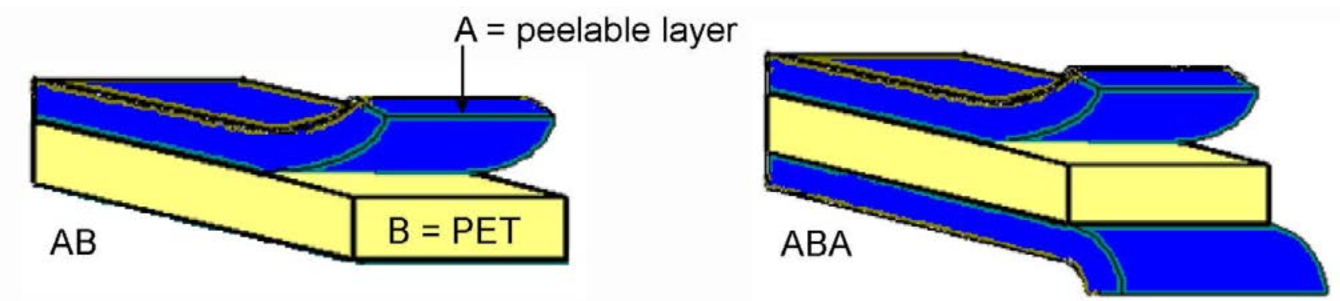


Figure 3: Schematic view of "On Demand" clean film (A = peelable layer).

comes an internal layer, which is only exposed to the environment when the sacrificial film layer is removed, ideally at the point of device manufacture. The sacrificial layer has the added benefit of protecting the surface of the film from contact damage during film handling and transport.

The impact of the sacrificial coextruded layer on subsequent processing has been studied by the TNO-Holst Centre within a European funded FP7 program CLEAN4YIELD. A version of the calcium test was used to study and compare the decay of the calcium on a barrier film utilizing a regular film surface, and on a film surface after the sacrificial layer has been removed. Although multilayers are normally employed, for demonstration purposes a proprietary single layer inorganic barrier material was deposited on the surface of the film. Qualitatively, Figure 4 show that relative to the Regular Melinex® control, the calcium decays (test squares become lighter) at a much slower rate with the On Demand Clean Melinex® film indicating the impact of the sacrificial protect film in preserving the polyester film's surface quality.

A further advantage is that the sacrificial coextruded layer protects the PET surface from defects that may arise by contamination build up at the die lip edge and/or when the film passes over rollers during the manufacturing or slitting processes. Molten polymer flowing over any debris build up at the die lip edge can lead to lines of scratches with high-aspect ratio. These are absorbed within the sacrificial coextruded layer leaving the PET film surface undamaged.

2. Low-Bloom Film

PET film contains ca 1.4 weight % cyclic oligomer and a portion of these oligomers can migrate to the surface if the film is held at elevated temperatures for tens of minutes, as can be seen in Figure 5. This "blooming" effect gives rise to haze. PEN with 0.3% cyclic content has significantly lower cyclic oligomer content compared with PET, and there is significantly less "bloom" associated with PEN film.

Planarizing coatings or hard coats act as a barrier to cyclic oligomer migration and offer one strategy to reduce the haze associated with this blooming effect. Careful control of the filming process offers another strategy to a "low bloom" film. These low bloom films typically have a haze less than or equal to 1% after aging at 150°C for 30 minutes. As a further refinement on the low bloom films, refractive index (RI) matching coatings are being developed, which reduce optical iridescence. The undesirable "rainbow" effect can be observed following the deposition of hard coat layers commonly used to manufacture transparent conductor films for touch panel and appliance applications. Therefore, end users are seeking clear film with both a RI match and a low surface haze after processing.

3. Light Outcoupling Films

As an alternative to the familiar microlens array technology, a range of volume scattering films have been developed which will outcouple light trapped in the glass structure when applied as an overlaminate to a rigid OLED. This

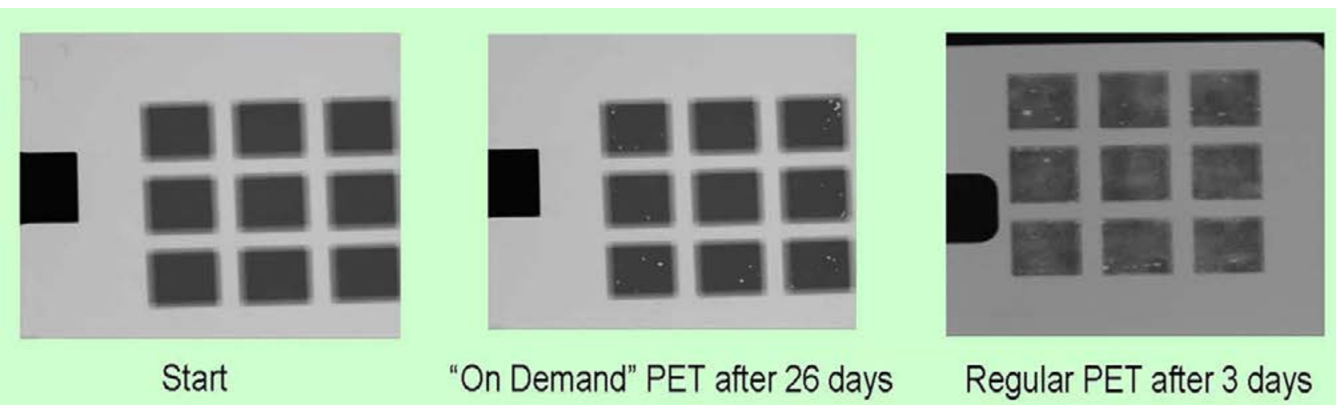


Figure 4: Calcium test pieces aged at 20°C and 50%RH.

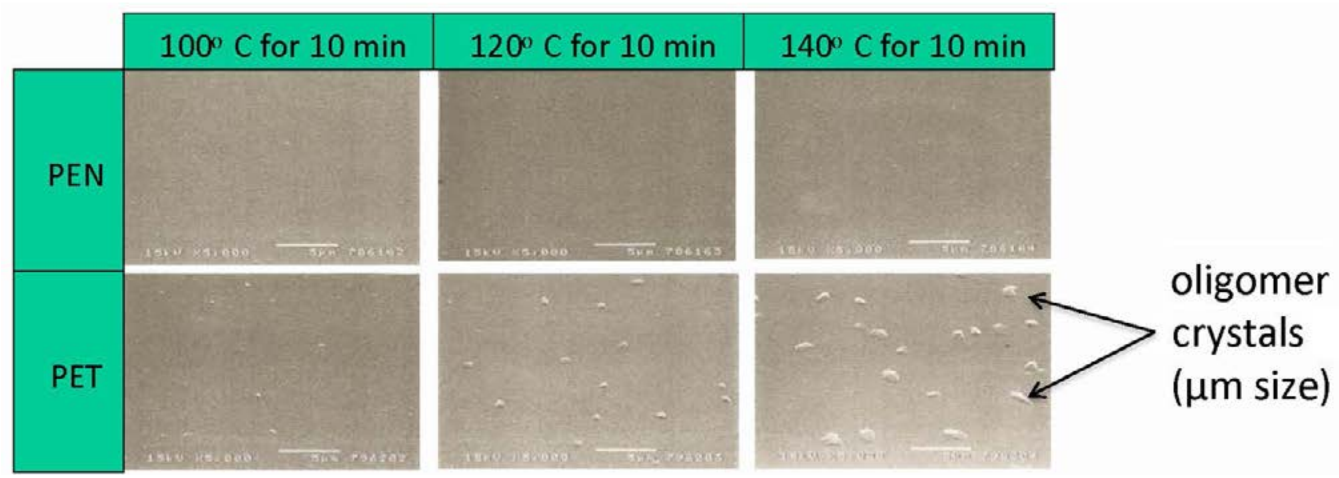


Figure 5: Cyclic oligomer "bloom" on typical PET and PEN film surfaces after aging.

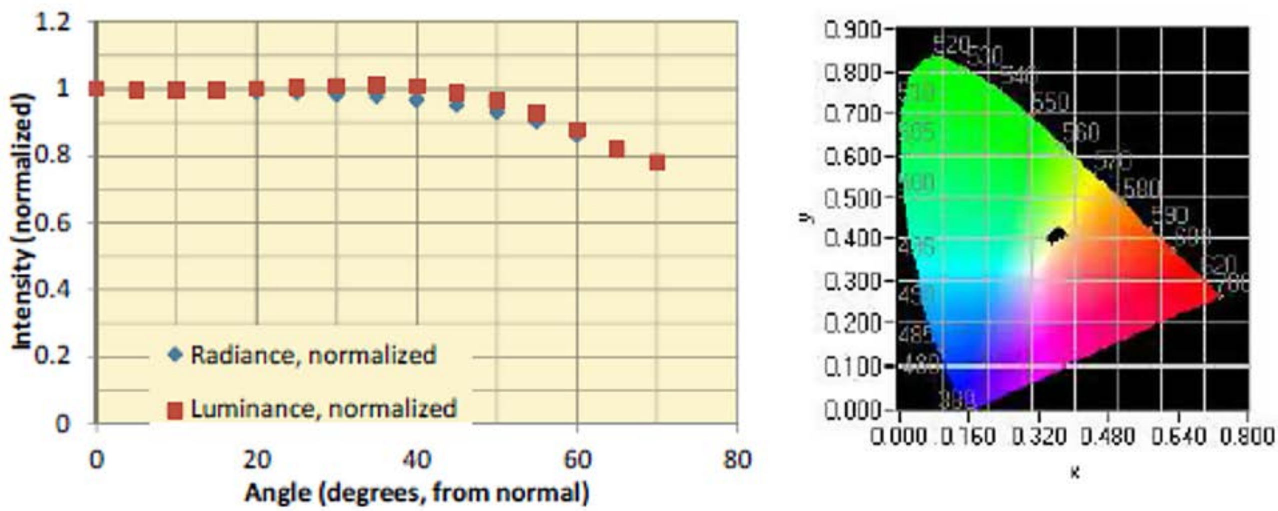


Figure 6: Angle dependent color/emission from glass OLED using outcoupling overlaminate (courtesy of Holst Centre, Eindhoven).

approach offers advantages in practical areas of surface performance, appearance and viewing angle distortion.

Participation in the European funded FP7 programme FLEX-o-FAB has brought optical outcoupling and clean substrate technology to the other participants with a goal of developing a cost-effective R2R process route to flexible OLED lighting. The principle of emission enhancement for flexible OLED using a flexible polyester substrate with integrated volume scattering features has already been demonstrated. The efficacy increased from 30 lm/W to 42 lm/W by using barrier foil with integrated outcoupling enhancement.

4. Weatherable Films

Polyesters such as PET and to a lesser extent PEN are inherently susceptible to degradation by hydrolysis. However, the hydrolysis behaviour of PET film can be improved significantly by control of variables such as molecular weight, the crystallinity developed during the filming process and by control of

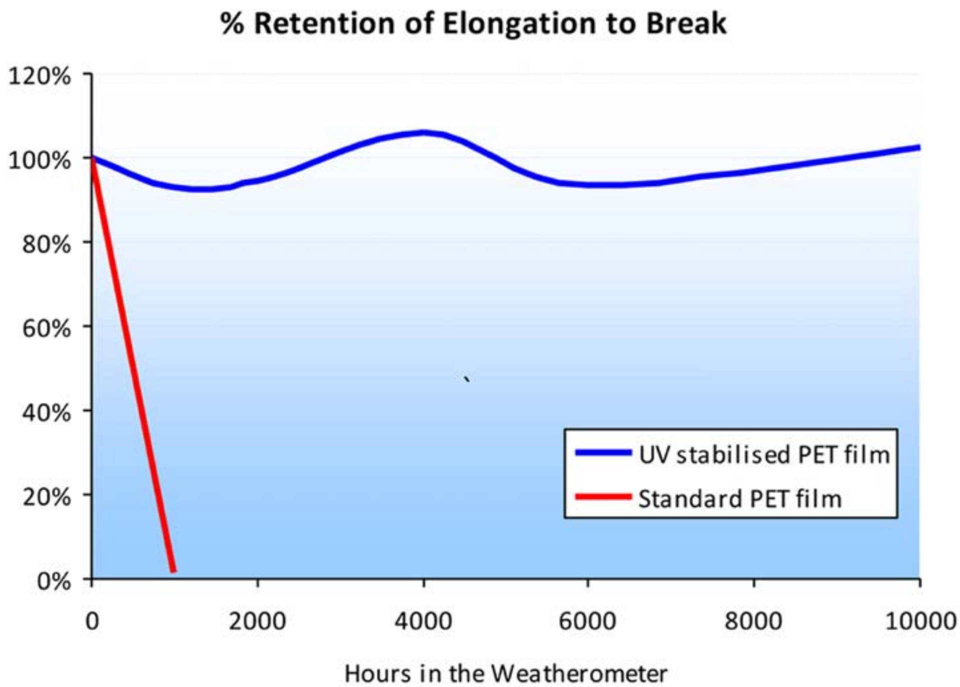


Figure 7: Change in elongation to break vs. hours in a Weather-Ometer® for PET.

end groups. The relative susceptibility of different films to hydrolysis is often studied using a damp heat test (DHT) in a climatic chamber set at 85˚C/85%RH. By using strategies such as those outlined above the lifetime to failure in DHT can be pushed from ca 1000 hours for a standard PET film to 2000–3000 hours for a hydrolysis stabilised film.

Similarly, a standard, unstabilized PET film will show poor stability to UV in outdoor use, and thus PET is often used misleadingly in comparison with other film types. PET film can be very effectively protected against the effects of UV irradiation by the addition of well-established UV stabilizers. Figure 7 shows results that illustrate how the addition of a UV stabilizer will have a significant effect on the retention of mechanical properties of PET as measured by elongation to break (ETB) on accelerated aging. (Aging at 10,000 hours in a Weather-Ometer® equates to approximately three years/1000 hrs for Northern Europe, two years/1000 hrs for Southern Europe and one year/1000 hrs for Australia.) Ongoing development work is extending the lifetime of PET film further.

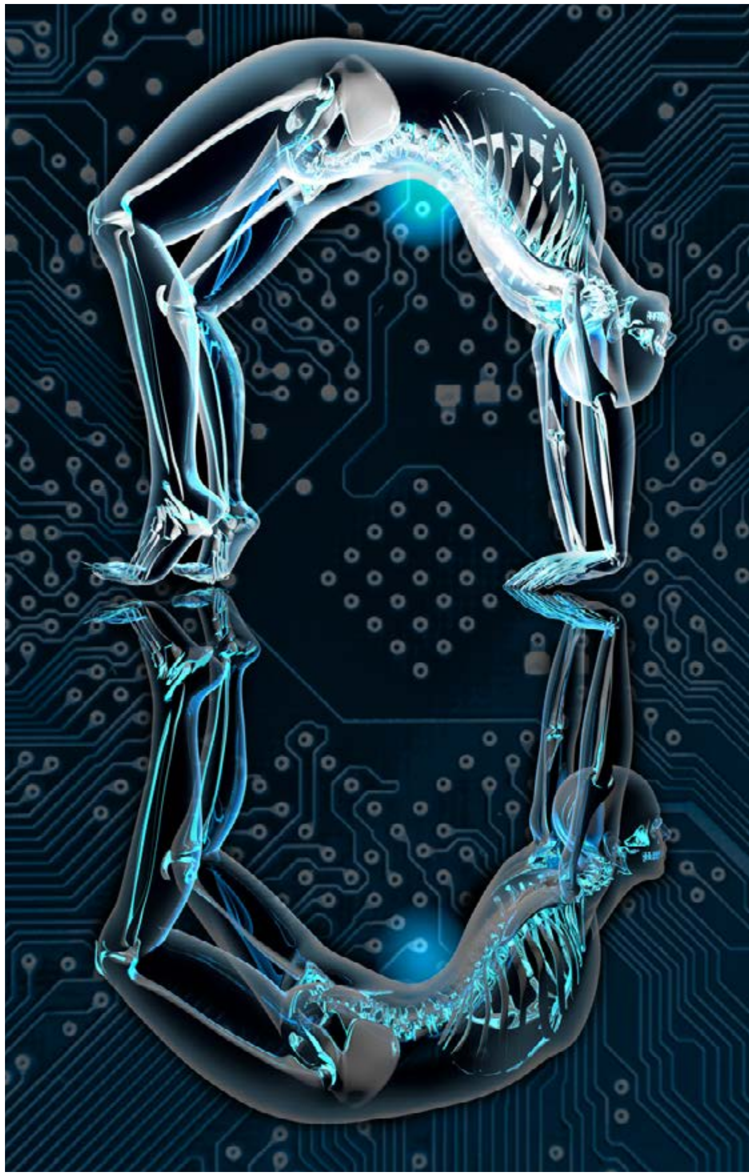
Conclusion

The understanding of the required property set for films used in flexible electronics applications has moved considerably over the past decade, and significant progress has been made in developing films appropriate for use. Rather than awaiting further inventions or scale-up investments for new engineered polymer film substrates, the flexible electronics industry has been seeking to drive the processing conditions of their products to the point where they can utilize extensions of commercial polyester film substrate technology. Polyester film manufacturers must continue to work with the flexible electronics industry to drive innovation that will meet the future performance and cost requirements of the flat panel display industry, as well as other flexible electronic, PV and OLED lighting markets. **PCB**

Scott Gordon is business development manager at DuPont Teijin Films.

Hybrid Stretchable Circuits on Silicone Substrate

by A. Robinson, A. Aziz, Q. Liu, Z. Suo, and S. P. Lacour



Abstract

When rigid and stretchable components are integrated onto a single elastic carrier substrate, large strain heterogeneities appear in the vicinity of the deformable-non-deformable interfaces. In this paper, we report on a generic approach to manufacture hybrid stretchable circuits where commercial electronic components can be mounted on a stretchable circuit board. Similar to printed circuit board development, the components are electrically bonded on the elastic substrate and interconnected with stretchable electrical traces. The substrate—a silicone matrix carrying concentric rigid disks—ensures both the circuit elasticity and the mechanical integrity of the most fragile materials.

Stretchable electronics is a fast emerging field that provides radically new form factors to electronic circuits[1]. Some of the most exciting applications include novel human-machine interfaces in the form of skin-like[2–6] or epidermal circuitry[7,8] and bioelectronic monitoring[9]. The main requirement for stretchable circuits is that the electronic devices and circuit performance do not, or only predictably, change with the applied mechanical loading.

One approach to manufacture stretchable circuits is to produce a stretchable circuit board onto which standard, off- the-shelf components may be mounted[10,11]. Rigid component islands are distributed on the surface of an elastomeric substrate and interconnected with elastic wiring. This hard-on-soft integration however suffers from large mechanical strain concentration at the interface between the rigid (PCB-like) islands and the stretchable substrate. Because interconnects must run across these interfaces, early electrical failure of the stretchable circuit is often observed[12].

This paper presents a simple solution to this challenge and demonstrates a functional hybrid stretchable circuit fabricated on an engineered stretchable circuit board. The latter is designed so that non-deformable regions are embedded within the elastomeric substrate (rather than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on top of the substrate), and the strain within the elastic wiring, (i.e., the top surface strain) smoothly increases across the rigid-to- elastic interface with the applied strain and does not exceed the applied strain. Non-deformable regions are prepared by embedding two concentric disks of stiff plastic foil within an elastomer matrix. We demonstrate the dual disks design is a straightforward way to keep the strain above the smaller disk to 0% and suppress the strain peak across the hard-soft transitions. We monitor the surface strain within elastic wiring prepared with stretchable thin gold film interconnects and highlight minimal mechanical fatigue in the metallic conductors upon cyclic stretching to 20% uni-axial strain. Packaged components (i.e., an operational amplifier, or op-amp) LED, and resistors, are subsequently mounted and interconnected on the stretchable circuit board to form an oscillating circuit, which frequency is designed to linearly decrease with the applied strain. The electromechanical integrity of the circuit is maintained over repeated stretch cycling demonstrating the potential of our stretchable circuit boards.

II. Overview of the Hybrid Stretchable Circuit Board

Stretchable substrates may be formed as (i) a homogeneous elastomer membrane, (ii) a mechanically graded elastomer, or (iii) an elastomeric membrane carrying embedded rigid platforms. A bulk elastomer membrane stretches uniformly so large strains appear across its surface. Macroscopic strain applied across a mechanically graded elastomer (prepared, for example, with photo-patternable PDMS14) is distributed through the polymer so that the stiffest, patterned regions stretch less than the softest ones. Yet, truly rigid regions (i.e., non-stretchable) cannot be prepared with this approach. Embedding stiff platforms within the thickness of the stretchable substrate can provide "zero-strain" zones on the surface of the substrate [12,15]. The strain profile on the surface of such engineered substrates may present a sharp peak close to the edge of the platform and the effective "zero-strain" surface area depends strongly on the geometry and density of the embedded rigid platforms material. Here, we propose the use of concentric rigid disks embedded in the elastomeric substrate to maximize the no-strain surface area and modulate further the surface strain across the soft-hard boundary.

Figure 1 presents a schematic cross-section of the hybrid stretchable circuit board. It consists of a millimetre thick PDMS substrate within which two concentric discs of polyi- mide (PI) foil (50 lm thick) are embedded. The upper disk is the smallest and is positioned towards the PDMS surface. The second disk has a bigger diameter than that of the first one and is embedded deeper in the PDMS membrane. The top disk ensures the strain at the PDMS surface immediately above

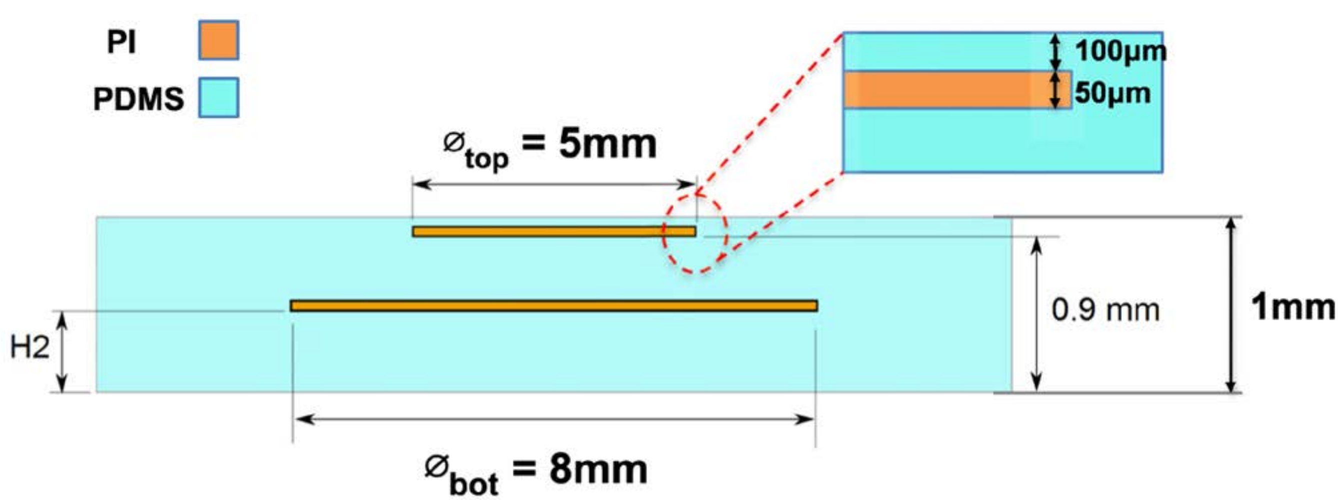

Figure 1: Schematic cross-section of the double-disk stretchable substrate.

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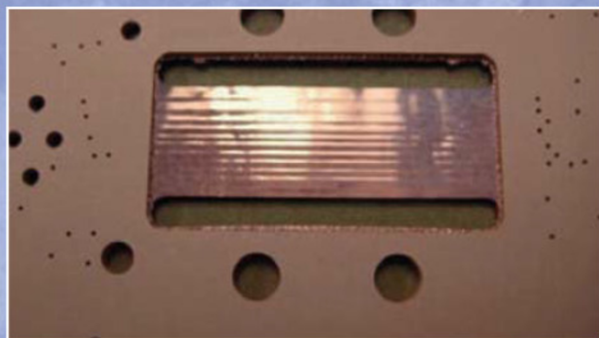

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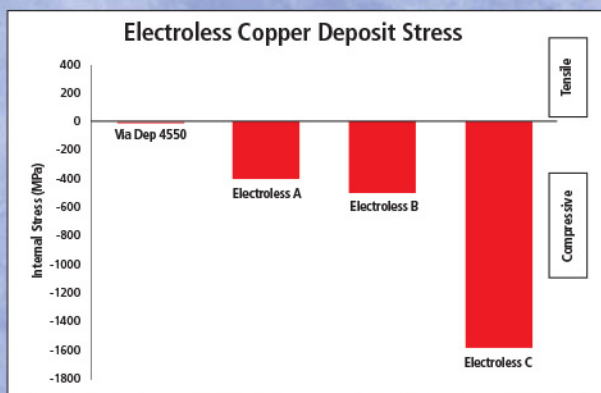

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it is pinned to zero while the bottom disk guarantees the surface strain to be zero across the complete surface area of the small disk[12] and suppresses any sharp peak strain across the non-deformable to deformable surface[15].

We compare the effects of embedding one disk and two disks by using a combination of finite element simulations and experimental measurements.

Let us first consider embedding a single disk close to the surface of the substrate. Since the plastic disk is much stiffer than the elastomeric substrate, such a construct is highly non-symmetric. When the substrate is stretched, the thin disk bends into a concave shape (Figure 2a). Far away from the disk, the substrate becomes flat. To make a transition from the concave shape above the disk to the flat shape far away from the disk, the substrate bends into a convex shape right off the edge of the disk. Consequently, the convex region of the substrate develops a large strain (Figure 2b). This high strain may cause failure of the interconnects[12].

To reduce the strain on the surface of the substrate, we embed a second, larger, disk, roughly at a depth about half of the thickness of the substrate. Because this large disk is placed in the mid-plane of the substrate, when the substrate is stretched, the two disks no longer bend significantly (Figure 2c). Consequently, the surface of the substrate above the edge of the bottom disk no longer develops a high peak of strain (Figure 2d). Furthermore, because the top disk is embedded close to the surface of the substrate, the strain on the surface of the substrate rapidly decays near the edge of the top disk, giving a large area for active devices. The strains determined from the finite element simulation agree well with experimental data. The strain in the two-disk

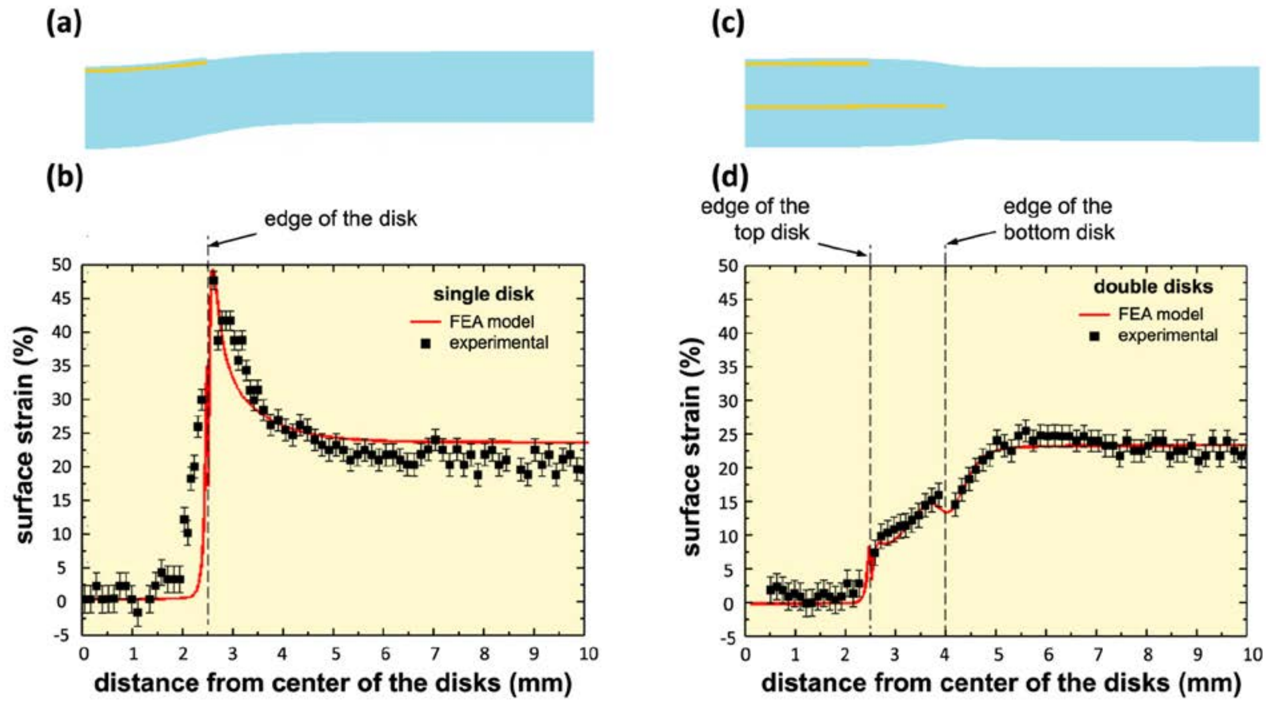

Figure 2: Surface strain profiles across the non-deformable to deformable interface when the substrate is stretched to 20% strain. (a) and (c) are the deformations of the finite element simulation in the case of a single disk and double disks embedded within the elastomer. The top disk is 100 lm from the surface and the bottom disk is half way through the substrate. The top and bottom disks are 5 mm and 8 mm in diameter, respectively. The scale in vertical direction is magnified 50%. (b) and (d) Solid lines are the surface strain calculated from the finite element simulations. Data points are the experimentally measured data.

case is much smaller than that in the single-disk case (Figures 2b and 2d).

We further illustrate our concept with experimental recording of the strain across the surface of the substrate (Figures 2b and 2d). We introduce an ordered matrix of PDMS microposts distributed all over the top PDMS substrate. The PDMS substrate was moulded against a silicon wafer patterned with cylindrical holes, 2 µm deep and 2 µm in diameter, arranged in a square array with a pitch of 12 µm. These microposts are small enough compared to the thick PDMS substrate not to affect the mechanical properties at its surface. They are used as visual markers to measure the local surface strain of the PDMS. While stretching, the distance variation between the microposts on the PDMS surface was measured with an optical microscope, and the local strain profile along the stretch direction was calculated. Each strain value was calculated by measuring the distance between ten adjacent pillars. We assumed the error in determining the position of the edge of each micropost should be approximately the same as the micropost diameter (2 µm), giving ±1 µm for each micropost and a total of ±2 µm for the row. The error was then calculated assuming a ±2 µm uncertainty for each strain value.

Figures 2b and 2d display the recorded strain across the single and double disk sample when a 20% strain is applied along the X-axis. The double disk sample is made of a 5 mm diameter PI disk embedded 100 µm below the top surface and a second PI disk (8 mm diameter) embedded at H2 = 0.5 mm. The single disk sample has the 5 mm diameter disk embedded 100 µm below the top surface. The experimental data concur with the finite element model. At 20% applied strain, a large peak reaching ~40% is observed at the edge of the single disk while it is suppressed in the case of the double disk design. Furthermore, the strain is locked at 0% across the complete surface of the top disk and the strain increases from 0% to 20% in the region above the second larger disk is very gradual. Vertical lines mark the position of the edge of the 5 mm and 8 mm diameter disks. Disks of this size were studied as they provide a rigid region large enough to hold a standard rigid electrical component. The strains determined from the finite element simulation remarkably agree with the experimental data.

III. Electrical Interconnects

Thin-metal film interconnects are patterned on the top surface of the hybrid stretchable substrate and define a stretchable electrical network between the non-deformable areas of the substrate. Their electromechanical performance is presented Figure 3a as a function of applied strain and for both substrate designs. Gold thin-film stripes were evaporated on top of the single and double disk substrate, and their electrical resistance was recorded as a function of applied strain and number of cycles. The interconnect is a 2 mm wide and 1.5 cm long stripe of Cr(5 nm)/Au(50 nm) bi-layer evaporated on the PDMS substrate through a shadow mask.

Both substrates can carry highly stretchable interconnects but interestingly the double disk design allows for a much smaller change in resistance with cycling. After 1000 cycles, the interconnect resistance of the stripe running above the double disk design increases by a factor of seven (at 20% applied strain), compared to a factor 30 for the single disk design. This suggests reduced mechanical damage in the gold thin film on the double disk design. Note that the evolution of the R (strain) profile with cycling from a triangular to a box-like profile is typical of evaporated thin gold film on PDMS13.

We further observed the surface of the gold interconnect patterned on a "double disk" substrate using scanning electron microscopy. We monitored its topography as a function of applied strain in a FEI/Philips XL30 Environmental Scanning Electron Microscope (ESEM). For ease of surface tracking, the top surface of the PDMS is covered with the same PDMS microposts as described above. Figure 3b shows a series of micrographs taken above the rigid platform, at the edge of the 5 mm diameter disk and on the stretchable PDMS region after 1000 stretch cycles to 20% strain. Row (a) displays the gold surface at the edge of the 5 mm disk at 0%, 5%, 10%, 15%, and 20% strain. The dotted line indicates the approximate position of the edge of 5 mm diameter disk. Row (b) shows the gold surface above the rigid region. There is no sign of strain or cracking in the gold film, even after 1000 stretch cycles. Row (c) shows the highest strain regions around the edge of the smaller

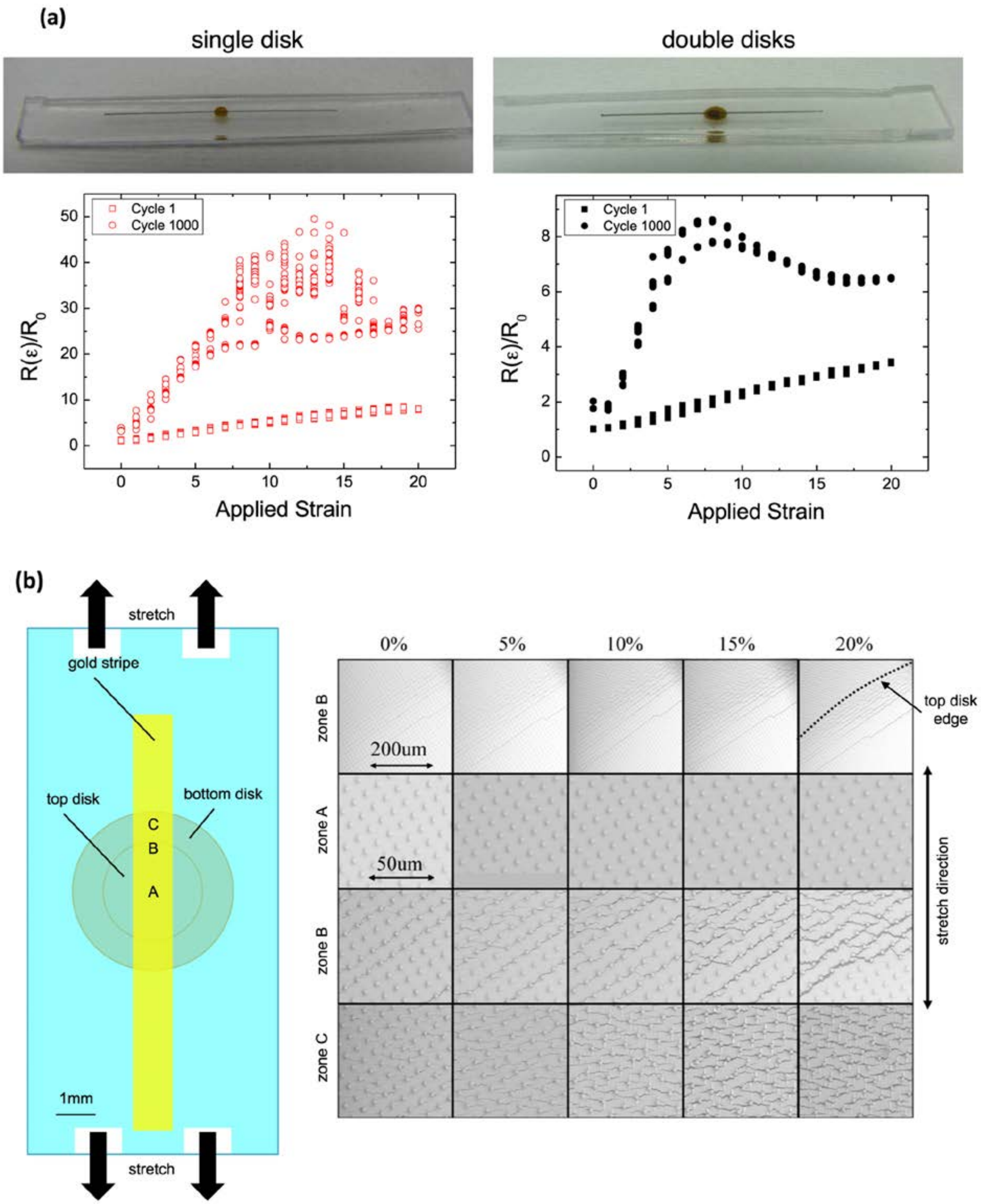

Figure 3: Stretchable interconnects. (a) Optical micrographs of a stretchable metallic stripe patterned above a single disk (left) and double disk (right) embedded in the silicone substrate. Corresponding electrical resistance change as a function of applied macroscopic strain and cycle number. (b) Series of scanning electron micrographs taken across the interconnect surface as a function of the applied strain and location above the rigid disks.

disk. A gradual increase in the size of the cracks with increasing strain is observed. After about a thousand stretch cycles, these cracks may merge to a length that may be as long as the width of the gold stripe leading to electrical failure. The nature of the cracks' progression at the disk edge is different than that of the cracks on the region above the bigger disk, where they originate at the pillars but terminate after a short distance between the pillars, as shown in row (d). Poisson compression, normal to the stretch direction, can also be very clearly seen at 10%, 15%, and 20% stretch in row (d), and results into a small buckling the gold layer originating from the microposts. The wrinkles run from one post to the immediately adjacent one. Investigation of series of ESEM images shows however that the main mechanical failure still occurs at the edge of the smaller disk but its occurrence is delayed thanks to the presence of the larger PI disk.

IV. Stretchable Hybrid Circuits

A multivibrator circuit with a flashing LED was then implemented combining the stretchable circuit board and discrete electronic components (Figure 4). The circuit is operating so that the rate of a flashing LED decreases when the circuit is stretched. The oscillating frequency is defined as

$$f = \frac{1}{2\ R_4\ C_1 \ln\left(\dfrac{1+\beta}{1-\beta}\right)} \quad \text{with} \quad \beta = \frac{R_2 + R}{R_2 + R + R_3}, \quad (1)$$

where R2, R3, R4, and C1 are discrete resistors and capacitance while R is a variable serpentine resistance patterned with stretchable thin gold film on the PDMS substrate.

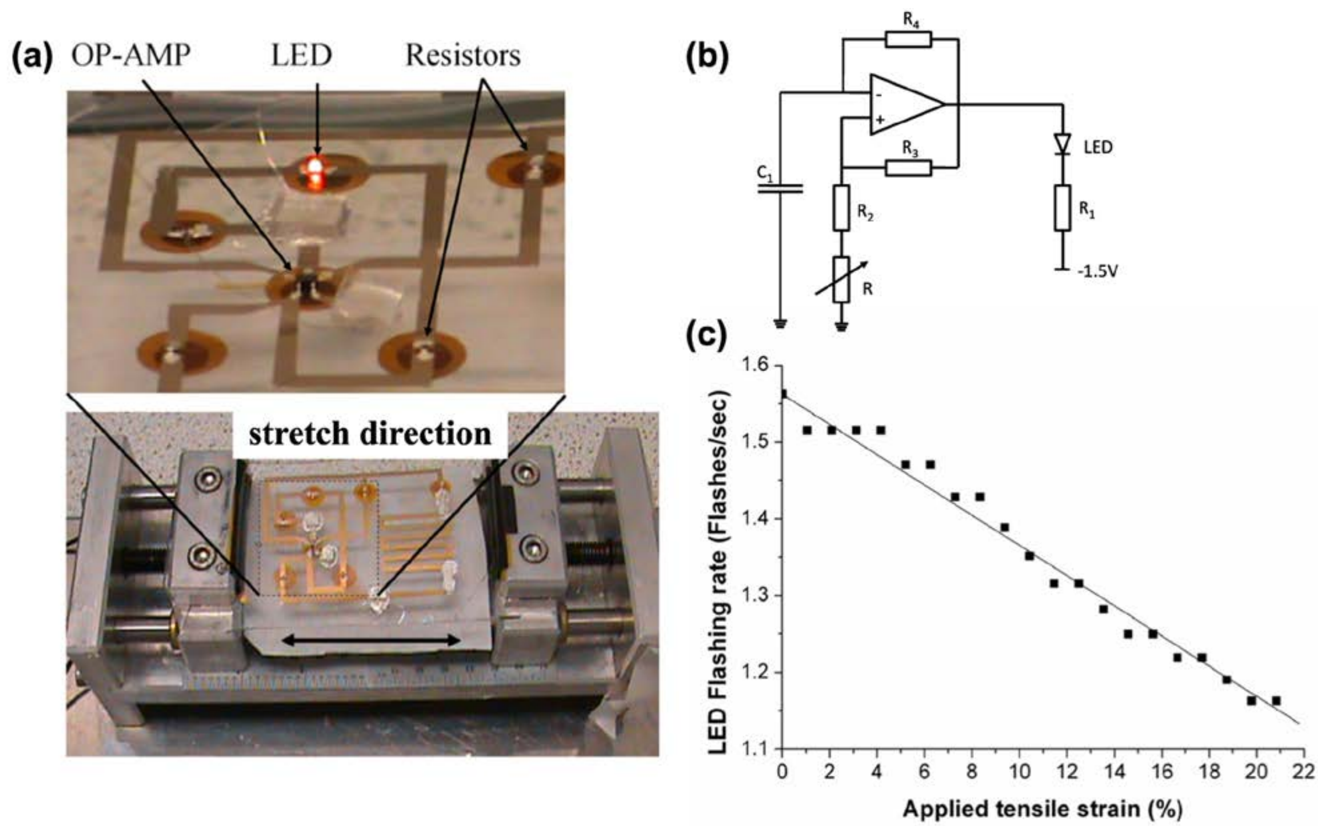

Figure 4: Hybrid stretchable circuit. (a) Pictures of the hybrid multivibrator prepared on the stretchable circuit board. The larger polyimide disks are 8 mm in diameter. Close up of some components (top); circuit mounted in the uniaxial stretcher (bottom). (b) Electronic diagram of the multivibrator circuit. (c) Flashing rate of the LED as a function of applied uniaxial strain.

The stretchable circuit board includes seven double disks areas distributed across the stretchable elastomer matrix to host each of the seven discrete components (four resistors, one capacitance, and one op-amp). Stretchable thin gold film interconnects are patterned on the top surface of the elastomer membrane to complete the circuit. The components are positioned above the rigid areas and electrically connected with the stretchable wiring using silver paste.

When the circuit is stretched, the resistance of the meander is increased, decreasing the flashing rate of the LED. Graph 4c shows the flashing rate of the LED, which linearly decreases with the applied tensile strain. The stretchable resistance increases by about a factor of four when stretched to 20% strain leading to a frequency decrease from 1.55 to 1.15, corresponding to the theoretical variation of f.

Conclusion

This paper provides a solution to a very common problem faced in fabricating stretchable circuits. When non-stretchable regions are created in a stretchable media, for example, PDMS, high-strain regions are created while stretching. For practical circuits, electrical wiring between components must run across the stretchable and non-stretchable regions, where large tensile strain may occur and lead to poor reliability of the electrical circuit and early electromechanical failure. The "double disk" design proposed in this paper provides a simple, yet efficient strategy to integrate disparate electrical components on a stretchable substrate. The proposed stretchable circuit boards will allow for straightforward manufacturing of stretchable electronics.

Acknowledgements

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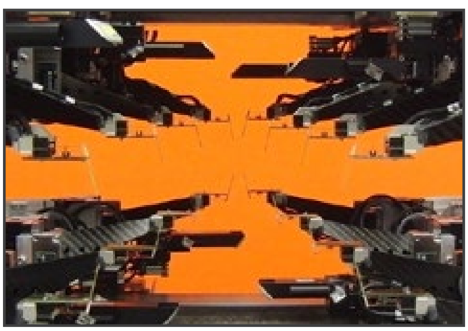

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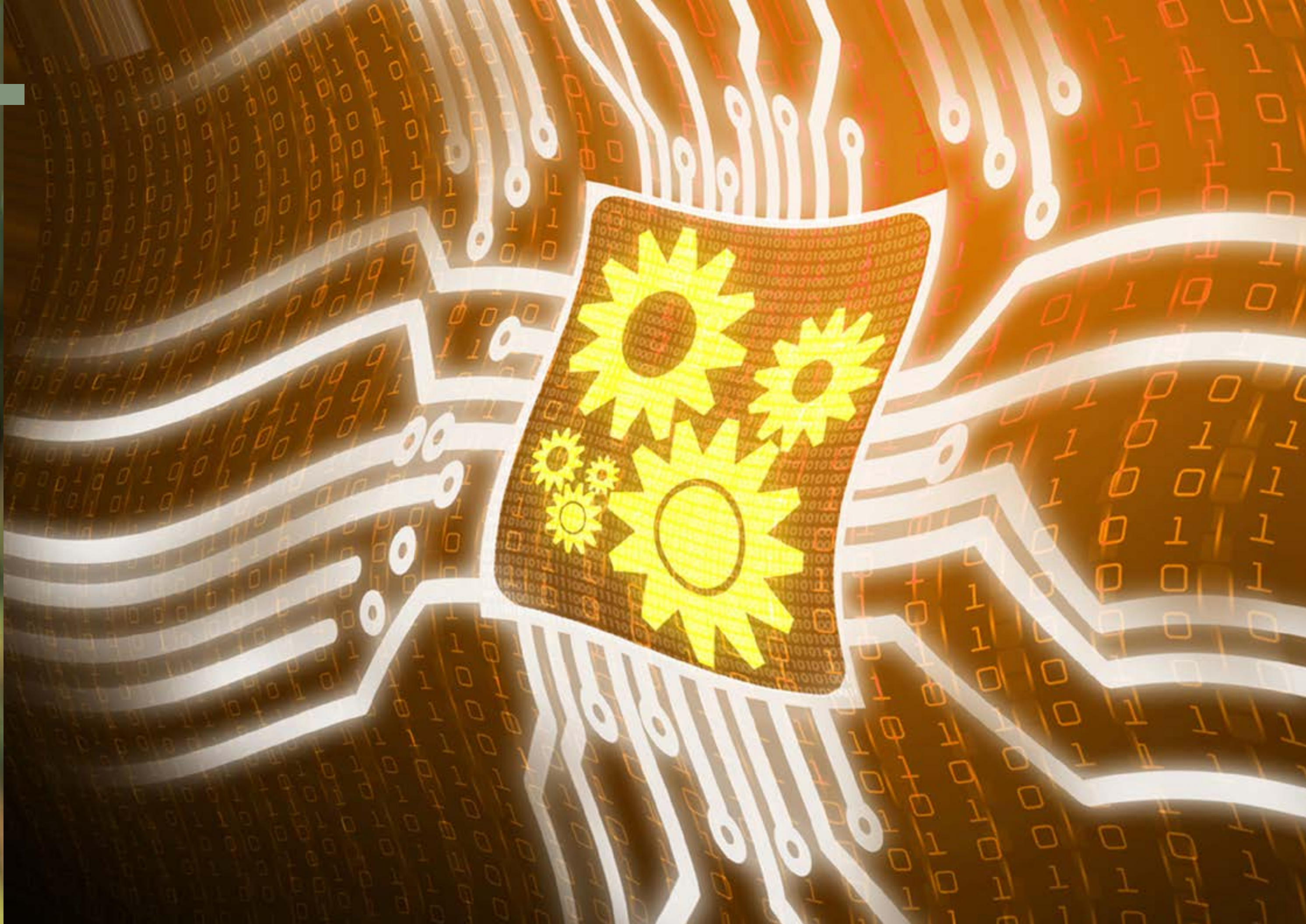

Basic Principles of Polymer Thick Film Flexible Circuits

by Joe Fjelstad
VERDANT ELECTRONICS

Polymer thick film (PTF) technologies have been used to manufacture printed circuits for decades. In fact, some of the very first circuits ever produced in volume were made by printing conductive inks patterned on an insulating substrate using a stencil. While the versatile nature of the materials used and the simplicity of the manufacturing process have made possible its continued use for more than six decades. In more recent decades, the technology has seen extensive use in the manufacture of inexpensive, polyester film-based membrane switches for electronic devices of every imaginable type, from hand-held calculators and computer keyboards to household appliances including microwave ovens and washers and dryers and beyond. An example of such a prospective construction is shown in the cross section in Figure 1.

Polymer thick film circuits are similar in many ways to their rigid and flexible counterparts; however, because of the materials and processes, they have their own very specific design rules. Because most PTF processing is most commonly based on screen printing technology, the limits of design are intrinsically linked to the printed ink's processing considerations and limitations. For example, there are the unique processing properties for conductive and resistive as well as insulating inks in terms of their thixotropy, which influence their printability. There is also the important consideration of the

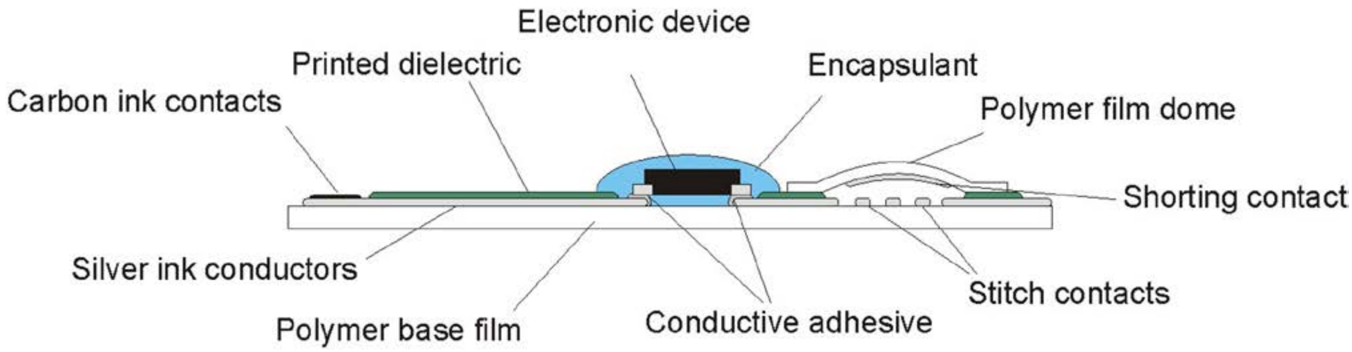

Figure 1: The list of materials used in the manufacture of PTF circuits is a short one and a primary factor in their being one of the lowest cost of current flexible circuit solutions.

final values for the conductivity and/or resistivity of the ink used when cured. In addition, there are also the limits of the screen printing materials and the processes used. Traditional screen printing methods are typically limited to the production of relatively course features (e.g., 250 µm). However, very fine-featured screen printed circuit technology has been reported down to ranges closer to 125 µm. For the foreseeable future, screen printing will remain an important technology for the manufacture of PTF circuits, both rigid and flexible. That said, inkjet printing is well positioned to augment time honored screen print methods. It also opens the door to realizing the possibility of producing circuits economically at a run unit of one, which has been one of the ideals of manufacturing.

With respect to PTF inks, the particle size of the included conductor material (historically silver but with other conductor materials coming on line) and the polymer carrier, its rheology and flow characteristics will establish the limits of screen printing. Emerging nanotechnologies being applied to conductive particle production appear poised to greatly boost conductivity, possibly opening the door for much broader use of polymer thick film technology in areas once reserved for copper circuits. While PTF circuits are not generally considered suitable for dynamic applications, they can actually perform quite well in certain types of dynamic applications. Some experimenters have actually reported increases in conductivity with cycling. PTF membrane switches also provided historical witnesses to the efficacy of PTF as a flexing technology in the contact areas of dome switches.

Basic Circuit Design Considerations with PTF

Among the most basic measures of any circuit manufacturing technology are feature sizes. These include circuit feature such as minimum hole sizes, conductor line and space limitations, and the base material's performance limitations. As mentioned above, minimum conductor width and spacing is considered to be in the range of 250–375 µm (0.010"–0.015"). It is possible to produce finer lines and spaces using PTF inks as was also mentioned, however, circuit conductivity can become more of a design performance concern. In that regard, appreciation of ink conductivity is a key concern in designing PTF circuits. The circuits are typically low-power with maximum current ratings of around 1/10 of an amp.

Current generation silver-based polymer thick film inks, under normal conditions can be expected to carry approximately 25% of the current of copper circuits for equivalent line widths and using a nominal PTF ink thickness. However improvements in materials are being made on a regular basis and there has been some suggestion that conductivities approaching that of copper metal are on the horizon. From a conductivity standpoint, values presently are nominally in the range of 5–20 mil-

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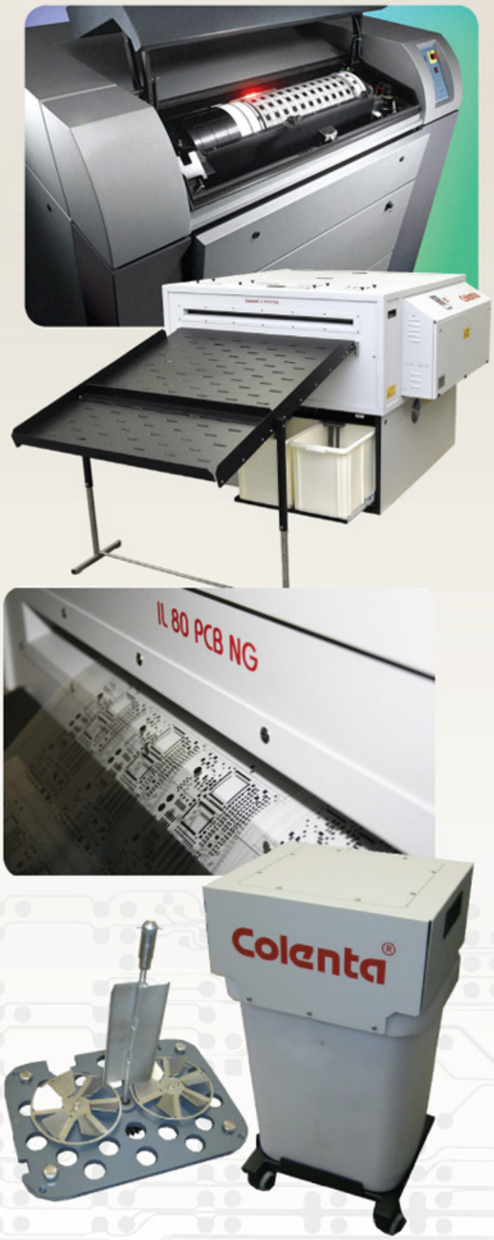

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liohms/square/25 µm of ink thickness, however, patent literature reports values of 0.100 ohm/square/25 µm for copper particles plated with silver. While conductive ink prices may run high owing to the price of silver, the overall processing cost should reduce the overall cost of production. That aside, care should be used when attempting carry higher currents with metal filled polymers. Hot spots within the conductor/polymer matrix can cause rapid degradation of the conductor and possible failure. Also in general, the operating temperature of the circuit should not exceed 90°C and the base material choice may suppress that limit even further depending on what material is used.

Screen printed resistors are familiar and fundamental devices commonly found incorporated into many PTF circuit designs. When planning to use them in a design, the resistors should be kept to a minimum of one or two bulk resistive values to facilitate processing. In general, resistors can be printed to within ±20% of desired value without trimming, however if tighter control of the tolerance of resistor value is required, laser or mechanical trimming of the resistor can be employed. It is also possible for the producer to mix resistive and conductive inks to tune the resistor value if desired, but this takes time and care to assure consistency.

“In general, resistors can be printed to within ±20% of desired value without trimming, however if tighter control of the tolerance of resistor value is required, laser or mechanical trimming of the resistor can be employed.”

When considering terminations, the design rules for circuit pads or lands for PTF circuits are similar to those used for rigid printed wiring boards, however, the termination features should be discussed with the manufacturer. Also while polymer thick film inks are not directly solderable, conductive adhesives can be successfully used to surface mount components. In such cases the component land design for surface mounting is basically the same as it is for traditional PCBs. Device attachment must be accurate, however, because the components will not center themselves in the same way that soldered components do when the solder melts during reflow.

As is the case with other more standard type flexible circuits, PTF flex circuits such as those used for membrane switches often have need for edge contacts which allow them to be plugged into connectors or mated to another surface. The finish of choice for PTF is commonly carbon. The thin graphite coating is both low friction and sufficiently conductive to carry power and signals at the higher voltages that are typically used where PTF technology can serve and it works well with the ZIF-type connectors that are commonly used with other types of flexible circuits.

Summary

Polymer thick film technology is a very useful solution for the manufacture of flexible circuit designs which can take advantage of its benefits while tolerating its more limited abilities. It facilitates the production of highly cost-effective assemblies using simple processing methods and low cost materials. While PTF may not be suitable for every application, it should not be overlooked or automatically ruled out without having given it at least a moment of consideration whenever cost consideration is a high-level concern. **PCB**

Joseph (Joe) Fjelstad is the founder and president of Verdant Electronics and a four-decade veteran of the electronics industry, as well as an international authority and innovator in the field of electronic interconnection and packaging technologies. Fjelstad has more than 250 U.S. and international patents issued or pending and is the author of Flexible Circuit Technology.

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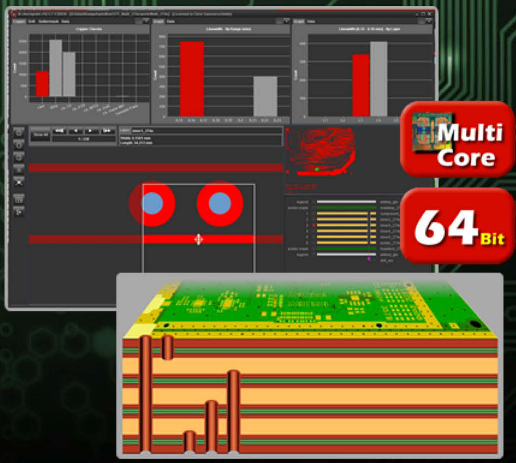

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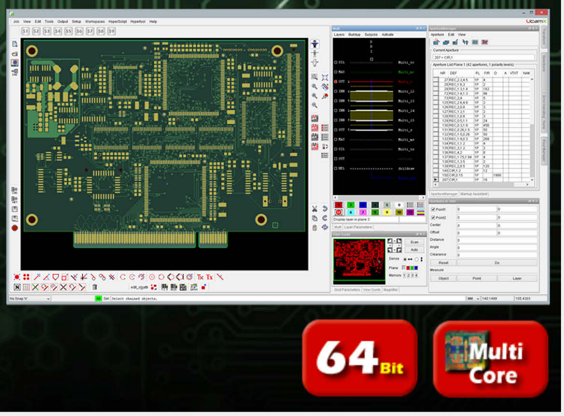

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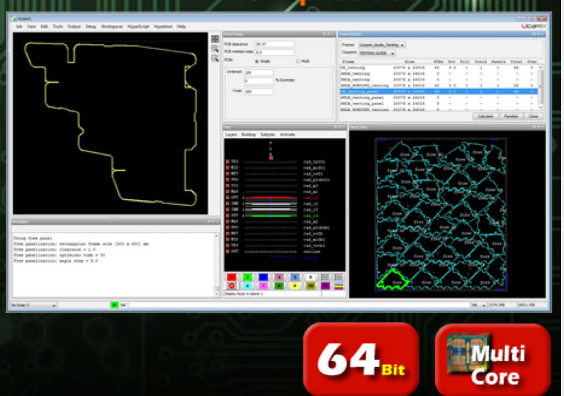

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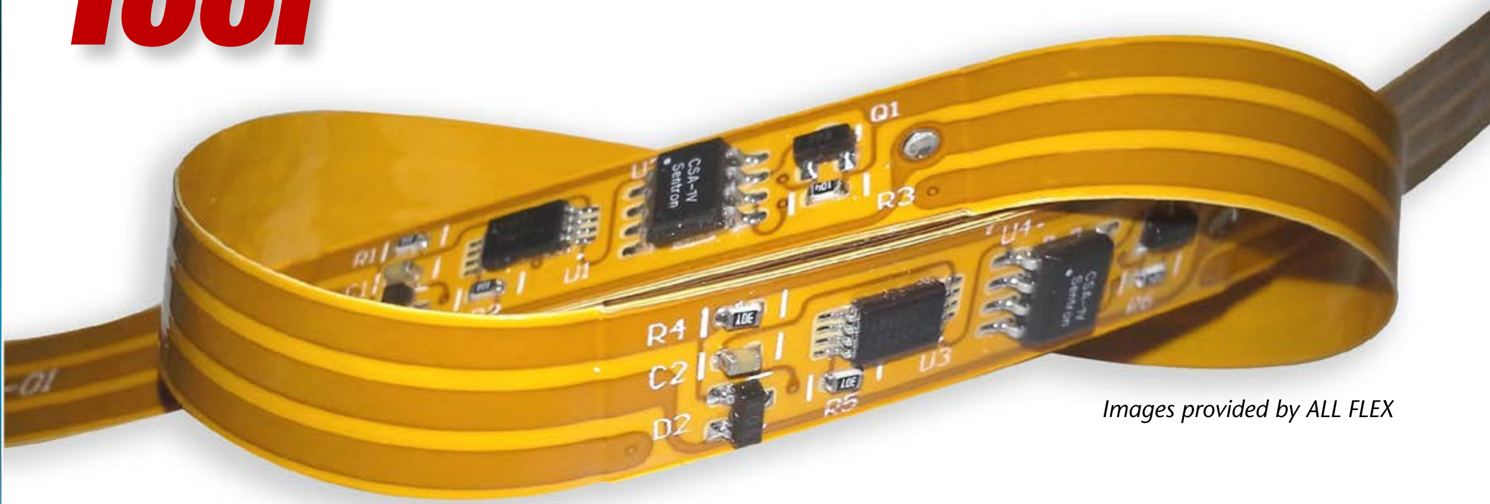

Images provided by ALL FLEX

by Dave Becker
ALL FLEX

The Market

The global market for flexible circuits is currently estimated to exceed $13 billion, with an estimated annual growth rate exceeding 10% as electronic devices continue to become smaller, lighter and more personal. Markets include medical, avionics, industrial, cell phones, military, and consumer among others. It is a technology an electronics designer should understand...and know when to consider adoption of the technology. Borrowing the words of Humphrey Bogart from the movie Casablanca, “Maybe not today, maybe not tomorrow, but soon and for the rest of your life.”

Moving Parts?

When most people think of flexible circuits, they imagine component parts moving within an electronic application. Clamshell cell phones, notebook computers, printers and hard disc drives are often mentioned as examples of products requiring moving parts with flex circuit interconnection. Questions such as “How many times can a flex circuit flex?” are best answered by “It depends.” Moreover, it depends on a lot of things. This political reply should be followed by a comment about several well-known design guidelines to be adopted when designing circuits for use in a “dynamic” flex application. In most cases, the fabricator will incorporate design practices intended to maximize flex life. Feature and construction recommendations include:

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• Copper traces should be in the "neutral" axis (i.e., equivalent amounts of dielectric on each side of the traces). This prevents the copper from being in either a tension or compression mode during flexing.

• Thinner circuits are better than thicker circuits. A good design will use .5 or 1 ounce copper with either .5 or 1 mil polyimide.

• Rolled annealed copper should be used for dynamic applications (the rigid PCB world uses electrodeposited copper) with a consideration for grain direction. The flexing motion of the circuit should be parallel to the copper grain direction. This is a critical consideration when the fabricator does their panelization.

• A gentle bend radius is best. An accepted guideline for dynamic flexing is the bend radius should be at least 10x the thickness of the material. Since single-sided circuits are quite readily designed at .005" thickness, a flexing radius of .050" is safe. In static applications, a guideline for single-sided circuits is that it can be folded on itself three times with a radius equal to its thickness if rolled annealed copper is used.

• When double-sided circuits are required, the circuits should be fabricated without electroplated copper plated on the surface of traces in bend regions. This practice is known in the industry as "pads only plating." Bend regions should be single layer copper to allow neutral axis flexing.

• Copper features are usually modified to "flexize" the circuit design. This includes radiusing traces through corners and adding fillets to solder pads. These feature upgrades not only improve flex life, they also improve the overall reliability of the design. Expect the flex supplier to provide these recommendations and file upgrades as part of their service.

The above guidelines are good rules of thumb. Some applications are only required to flex a few times, others thousands, while some might require millions. It is always a good practice to flex test an individual circuit design with prototype parts with an assembly that mimics the final application. And make sure the circuit supplier knows the product is going to be used in a dynamic application so that proper grain direction is chosen during panelization!

Flex to Install

So while it is certainly true flex circuits are used successfully in a wide range of dynamic

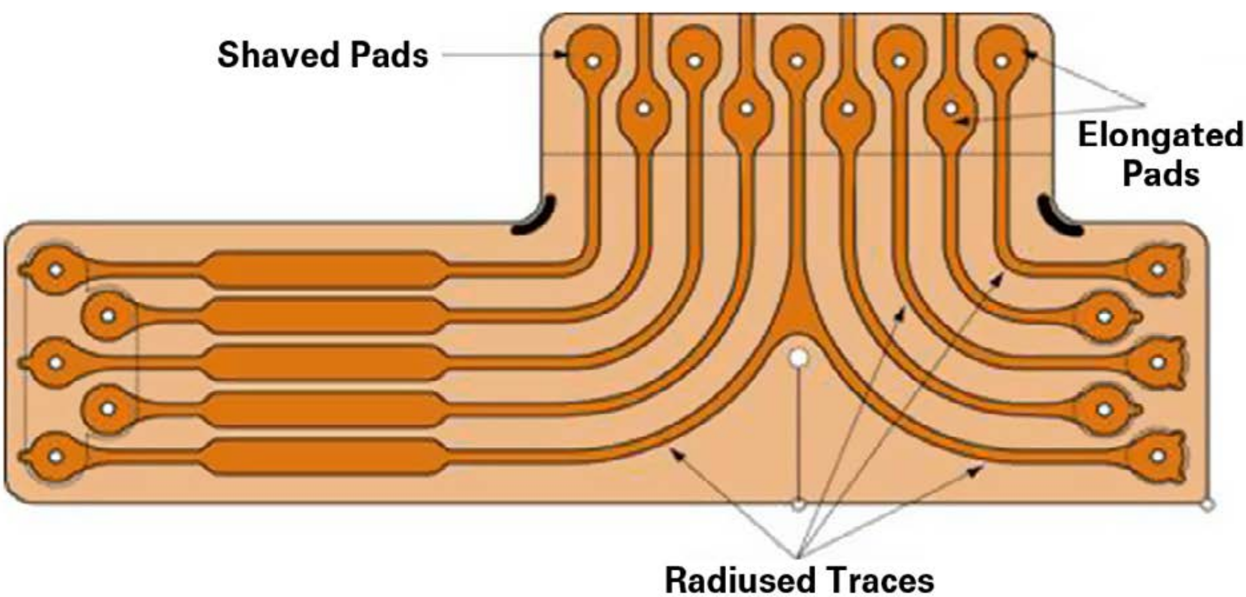

Figure 1: Flexized design.

flexing applications, the vast majority of flex circuits do not bend, fold, or flex once they are installed. This obviously begs a few questions, such as: What are all those other applications? Why do they use flex circuits? When should a flex circuit be used rather than a rigid PCB?

The answers vary as diversely as the applications themselves. Answering these questions requires an examination of why past products have incorporated flex circuits. What utility is offered by this novel interconnection packaging option? Answers include space savings, weight reduction, high-performance cable design, multi-planar interconnection, and cost.

Cost vs. Hardboard

One of the questions I field most frequently is "How does flex circuitry compare in cost to a rigid printed circuit?" And my honest answer is generally is that it is more expensive. The specific premium paid for flex circuitry is a multidimensional factor and a function of material costs, handling requirements, applications engineering support, volume, and the construction. I generally advise that, if a design doesn't take advantage of the bending characteristics or the thinness of a flex circuit, it is likely that a rigid PCB will be a lower-cost solution. But taking advantage of a flexible circuit's characteristics involve considerations for multiplanar interconnections while eliminating connectors or hand soldered wires, simplified assembly, improved reliability, or providing a pre-tested component/subassembly. Applications adopting flex circuits have cleared the hurdle of looking at total cost of ownership and decided the technology is cost effective. In fact, the market for flex circuits is estimated to be about 10% of the overall printed circuit market. It is a pervasive technology.

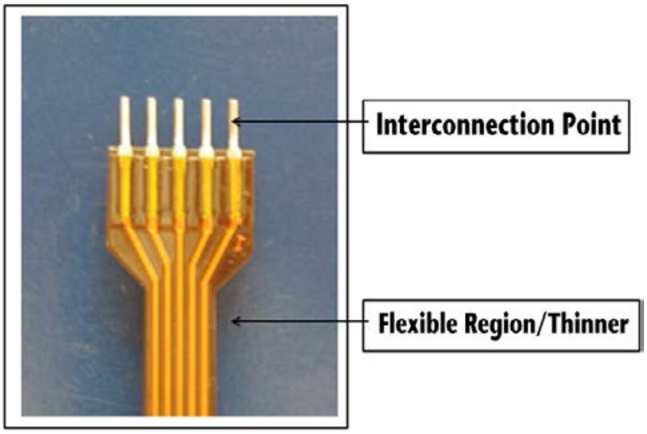

Figure 3: Circuit with integrated pins.

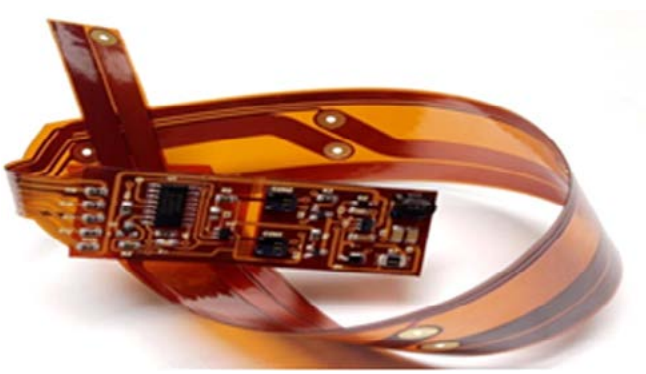

Figure 2: Folded circuit with components.

Power Circuits

A less well known segment of the flex circuit market is found in high-power applications.. Most applications utilize .5 or 1 ounce copper (.0014" = one ounce) but some products require considerably more current-carrying capacity than can be reasonably designed in with these copper thicknesses. One option is to consider thicker copper. Copper thicknesses of .010"–015" thick are not uncommon but flexibility is dramatically reduced with these materials. Using polyimide thicknesses of .001" (dielectric strength at 6000volts/mil per ASTM D149) does allow a considerable thickness reduction in applications with space constraints. And the materials do remain bendable if necessary.

Current carrying capacity is a function of a copper traces cross sectional area and the following chart (Table 1) provides a quick reference for design considerations.

Circuit features with integrated pins are sometimes favored in applications with high current requirements. The thicker copper creates robust pins that are not easily bent or damaged during handling. These integrated pins are often used in high reliability applications serving as jumpers from one PCB to another, eliminating the need and cost of connectors. Cir-

CURRENT CARRYING CAPABILITIES FOR EXTERNAL TRACES IN AIR

COPPER WEIGHT								
AMPS	1/2 OZ. (.0007")	1 OZ. (.0014")	2 OZ. (.0028")	3 OZ. (.0042")	4 OZ. (.0056")	5 OZ. (.007")	6 OZ. (.0084")	8 OZ. (.0112)
CONDUCTOR WIDTH IN INCHES								
0.5	.013"	.008"	N/A	N/A	N/A	N/A	N/A	N/A
1.0	.028"	.017"	.013"	N/A	N/A	N/A	N/A	N/A
1.5	.040"	.027"	.020"	N/A	.012"	.005"	.003"	N/A
2.0	.053"	.040"	.030"	.0235"	.020"	.018"	.016"	.013"
2.5	.080"	.060"	.042"	.0325"	.0285"	.024"	.023"	.018"
3.0	.100"	.083"	.057"	.045"	.0387"	.035"	.030"	.024"
4.0	.160"	.120"	.088"	.066"	.055"	.048"	.043"	.037"
5.0	.225"	.158"	.118"	.09"	.074"	.065"	.059"	.048"
6.0	.285" (off chart)	.195"	.153"	.117"	.094"	.082"	.074"	.062"
7.0	N/A (off chart)	.250"	.187"	.145"	.124"	.105"	.0905"	.075"
8.0	N/A (off chart)	.307"	.232"	.180"	.1485"	.130"	.122"	.095"

This chart gives recommendations for width of conductor needed to carry current on different copper thicknesses. For informational purposes only.

PCB Trace Width Calculator

Table 1.

cuits with this feature require a multi-step etching process to produce a flexible circuit having thinner and more flexible finished conductors in regions that are bent, but with thicker copper pins for the soldered connections.

High-Speed Cables

High-performance cables with controlled impedance requirements can also be created with flexible printed circuits. These cables are designed for use in high-speed digital applications. A common microstrip circuit, easily constructed with PCB materials and requiring controlled impedance, uses a flat conductor over a ground plane. The conductor and ground plane are separated by a dielectric—usually polyimide and adhesive. The surface microstrip transmission line also has free space (air) as the dielectric above the conductor. Stripline designs with two reference planes are also easily designed with circuit board materials and processes. There are several options on the Internet for finding design assistance when calculating controlled impedance. One option is located here.

Component Assembly

Component assembly on flex circuitry is common and similar to methods used for rigid PCBs. More than 50% of flex circuits are sold with value-added component attachment. This can be done with hand soldering techniques or hand placement of SMT components for low volume. Both traditional tin/lead solders and lead-free solders (used to meet RoHS requirements) are common as polyimide constructions are very robust at high temperatures. With higher-volume parts there is custom fixturing used which can get complicated as it is adopted to accommodate the handling nuance characteristic of thin, flexible materials. Both high-volume wave soldering and surface mount soldering are common assembly techniques. Selective stiffeners are attached with either thermoset or high temperature pressure sensitive adhesives on regions of the circuits supporting components. The stiffeners are often glass epoxy materials and prevent bending the circuit at a solder joint. Fracturing traces can occur absent adequate mechanical support from a stiffener.

Additionally there is some process preconditioning recommended when soldering flex circuits, especially if they are stored in a modestly humid environment. Polyimide is considered quite hydroscopic as it absorbs up to 2% of its weight in moisture. This absorption can cause circuitry to delaminate or blister when exposed to solder temperatures. Prebaking flex circuitry at 105°C for an hour eliminates this issue and is a good general recommendation prior to solder temperature exposure.

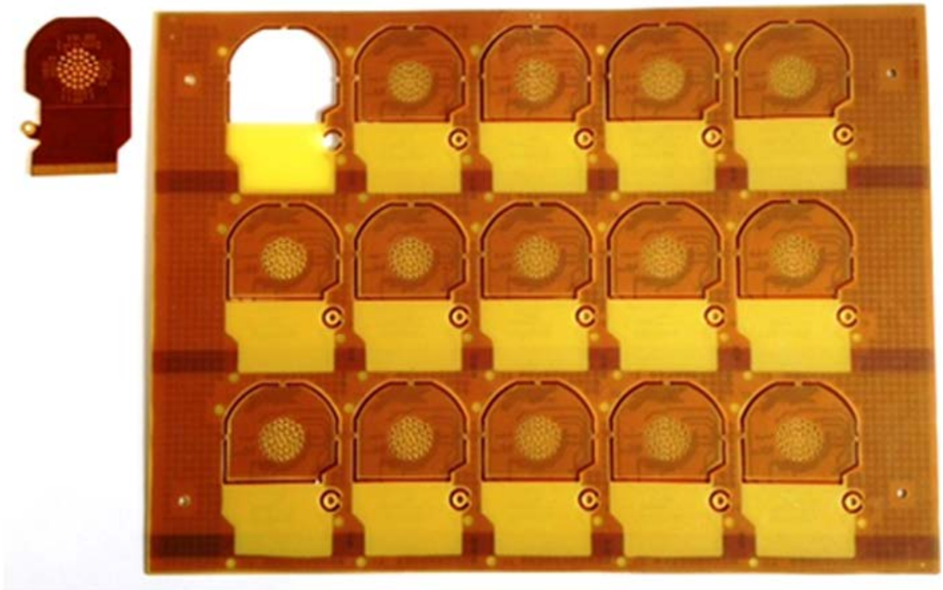

Figure 4: Circuits with stiffener carrier.

As volumes increase beyond prototype quantities, fixturing becomes a requirement for both wave soldering and SMT soldering. This fixturing will be custom and design depends heavily on the individual parts and assembly required. With wave soldering, FR-4 glass epoxy is often used to mechanically support a soldered connector. This glass epoxy can also be used as a carrier fixture with individual parts broken from the panel after component soldering. Carrier plates are also used with cavity openings allowing access to reflowed solder in a wave soldering machine.

Fixturing for SMT assembly is often done with vacuum assist or by bonding the flex panel to a low tack carrier plate. Both methods allow the panel to be held in place through processes including solder stencil, SMT placement and reflow. Pre-cutting or routing the individual parts prior to assembly allows them to be easily removed from the panel post assembly. The myriad of individual parts and variety of assembly requirements leads to a wide variety of fixture options. There are companies specializing in this type of tooling that can also assist with ideas and custom fixtures.

Summary

Flexible PCBs are used extensively throughout the electronic market for a wide variety of reasons, including their ability to move in an application, their light weight, and extreme thinness. They can also be used in high current-carrying applications and are often populated with components with assembly processes typical of rigid printed circuits. There are certain important design, processing, and handling considerations that separate flex circuits from their rigid cousins. Many suppliers offer printed design guides and early involvement of a flex supplier is recommended as a design unfolds. This early involvement will help insure proper tolerances, costs, and constructions are considered for a robust and reliable adaptation of the technology. **PCB**

Dave Becker is the V.P. of sales and marketing at All Flex Flexible Circuits and Heaters, which specializes in low to medium volume flexible circuits and flex circuit assembly.

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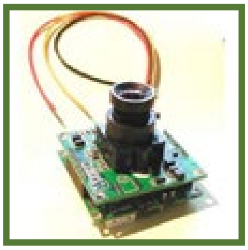

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PCB007 Market News Highlights

Employment Gains Buoyed by Professional & Business Services

In April, the unemployment rate fell from 6.7% to 6.3%, and the number of unemployed persons, at 9.8 million, decreased by 733,000. Both measures had shown little movement over the prior four months. Over the year, the unemployment rate and the number of unemployed persons declined by 1.2% and 1.9 million, respectively.

Wearable Electronics to be a $70B Business in 2024

Wearable electronics is a fragmented industry when it comes to manufacturers. Even mature sub-sectors have no clear leaders in what will be a $70 billion-plus business in 2024, with 12,000 developers and manufacturers, as recently calculated by analysts IDTechEx.

Global Smartphone Shipments Reach 267M Units in 1Q14

"The Q1 momentum came mostly from the emerging market sectors and China," noted Avril Wu, assistant vice president of TrendForce. "The Chinese smartphone manufacturers' increased 4G production is key to the smartphone industry higher than anticipated Q1 growth."

What's Driving the Global Diagnostic Imaging Market?

Some factors, such as increasing investments and funds by government bodies worldwide, investments by public-private partnerships, increasing number of diagnostic procedures and diagnostic centers, rising number of cancer patients, and technological advancements, are driving the global diagnostic imaging market.

China Plays Vital Role in U.S. Economy; Exports Hit $120B

"Exports to China play an essential role in the U.S. economy and job growth," said USCBC President John Frisbie. "With China's large population, rapidly growing middle class, and a long list of economic development goals, American companies of all sizes are sending a variety goods and products to an ever growing consumer and business marketplace in China."

Wireless M2M Devices to See CAGR of 21.4%

According to a new research report from the analyst firm Berg Insight, the number of devices with cellular or satellite connectivity deployed in oil and gas applications worldwide was 423,000 at the end of 2013. Growing at a compound annual growth rate (CAGR) of 21.4%, this number is expected to reach 1.12 million by 2018.

Eco-friendly Electronics Drives PE Market Growth

Analysts forecast the global printed electronics market to grow at a CAGR of 20.6% over the period 2013–2018. One of the key factors contributing to this market growth is the increased need for eco-friendly electronics products. The market has also witnessed the miniaturization of electronics devices.

Small Business Owners Optimistic About Growth in 2014

In a survey of small and mid-sized business, the Pepperdine Private Capital Markets Project 2014 Economic Forecast shows that business owners are optimistic about growth opportunities, both nationally and personally, for the remainder of 2014. More than half of respondents (56%) are more confident about business growth prospects compared to a year ago.

PE Market to Reach $40.2 Billion by 2020

The printed electronics market is estimated to grow at a CAGR of 33.8% from 2014–2020 and it is estimated to reach $40.2 billion by 2020, according to a report published by MarketsandMarkets. Rising energy costs, coupled with climate change, are driving the increase of renewable energy sources such as solar photovoltaic technologies.

Global Semiconductor Industry Hits Record Sales in Q1

The Semiconductor Industry Association (SIA) announced that worldwide sales of semiconductors reached $78.47 billion during the first quarter of 2014, marking the industry's highest-ever first quarter sales. Global sales reached $26.16 billion for the month of March 2014, an increase of 11.4% from March 2013 when sales were $23.48 billion.

ECWC13: "Connecting the World"

The Keynote Presentations

by Pete Starkey
I-CONNECT007

First held in London, UK, in 1978, and triennially since then, the 13th Electronic Circuits World Convention came to Nuremberg, Germany on May 7-9 2014, running in parallel with the SMT Hybrid Packaging Exhibition.

Alun Morgan, chairman of EIPC and also of the ECWC13 Committee, welcomed an enthusiastic international audience to a superbly organised and managed event that offered a programme of 123 papers in 26 sessions, presented by leading experts from industry and academia keen to share their knowledge and experience in printed circuit technology and market trends. His welcome was echoed by David Lai, WECC secretary general, who acknowledged the support and cooperation of WECC members CPCA, EIPC, HKPCA, IPC, IPCA, JPCA, KPCA and TPCA, and extended his gratitude to Mesago for their efforts in coordinating the event, and to Isola, Ventec and Somacis for their sponsorship. Dr. Stefan Mengel added his welcome on behalf of the Federal Ministry of Education and Research, emphasising the importance and significance of cross-border collaborative research and European cooperation.

Representatives of all of the WECC members assembled for a grand ribbon-cutting ceremony, with stirring musical accompaniment from a traditional oom-pa band.

"Where would we be without the PCB?" The opening keynote presentation was delivered by Dr. Marc Schweizer, CEO of Schweizer Electronics. He described how innovative PCBs would form an integral part of customised solutions to enable the future technological, environmental and cost-efficiency demands of the automotive industry to be met. The automotive industry contributed 190 billion euros to the German export market; electronics represented 25% of its manufactured cost and supported 800,000

jobs in Germany. And it was electronics that was driving innovation in automotive development, taking over from mechanical engineering as the dominant force. Future automotive electronics would make major contributions to safety, autonomy and connectivity, and the value of automotive electronics was forecast to increase to 430 billion euros by 2025, largely as a consequence of major developments in alternative drive systems.

He commented that, of the present $60 billion world market for PCBs, the top 100 PCB fabricators now supplied 80% of the total requirement. "The big ones are getting bigger and the smaller ones must become more focused!" His message was that the PCB industry must consolidate further in order to secure the resources to support future capital and operating expenditure requirements as the PCB progressed from being a component carrier to becoming an integrated part of a system solution as automotive electronics technology continued a rapid evolution along a route analogous to that of the mobile phone. And as cars needed to manage more and more electrical power, the power-electronics PCB, offering lower cost than its ceramic equivalent, had enormous growth potential.

PCB and semiconductor were growing together. No longer was the PCB "the semiconductor for poor people." Miniaturisation, the demand for maximum performance in minimum space, was being achieved by techniques such as module embedding, motherboard embedding, power embedding and ceramic replacement. "Nothing is as consistent as change!" The PCB had become an integrated part of customised solutions. An interesting statistic: of over 25,000 PCB manufacturers in the world, 15 served the requirements of 75% of the automotive market, characterised by its special needs and long design cycles.

Dr. Stefan Mengel

Looking to the future, Dr. Schweizer predicted that the electronics value chain would react to the need to integrate active and passive components into PCB-based systems by forming partnerships. "Let's take off our old shoes and look at new ways of management!" He considered the transition from management by control to managing partnerships to be vital to future success. "We must be adaptive to change and ready to question our management styles. Partnership models offer the most promising solutions."

Electronic System Enhancements with Advanced Packaging and Substrate Technologies was the title of the second keynote presentation, from Dr. Mike Ma, Vice President of Siliconware Precision Industries Limited, the world's largest IC packaging and testing company, based in Taiwan and part of a substantial and comprehensive electronics industry infrastructure that included wafer foundries, IC packaging, EMS and ODM companies and PCB fabricators. Seven of the world's top-twenty PCB companies were Taiwanese, and there was strong growth in flexible PCB manufacture.

"What is next after mobile computing?" he asked, referring to a growth curve progressing through zones labelled 'mobile computing,' 'context-aware computing' and 'ubiquitous computing' towards 'smart everything' and 'ambient intelligence,' and went on to explore and explain the contribution that packaging and PCB technology would make to the enhancement of electronic systems.

Small form factor was the driving force for the packaging industry. He used as an example the continuing evolution of the mobile phone, getting progressively thinner and, because a large proportion of available volume was taken up by the battery, the electronic systems had to be squeezed into progressively smaller spaces whilst constantly increasing functionality demanded of them. Flexible circuits were becoming available with cores as thin as 14 microns, copper as thin as nine microns and lines and spaces down to 25 microns. System

Dr. Alun Morgan

performance was being enhanced by embedded passive components, with embedded actives in prospect, and cost savings were being achieved by roll-to-roll processing and automated coverlay application. There was increasing industrial collaboration in flex-rigid manufacture.

So "thin" was the significant keyword when it came to describing packaging trends: multichips in thin single packages, thin system-in-package and thin package-on-package. Copper-pillar bumping gave the dual benefits of being completely lead-free and offering higher current-carrying capacity, and fine-pitch bump-on-trace techniques enabled cost reduction through greater functionality per unit area. Lines as fine as two microns had been demonstrated in embedded-trace IC substrates. Via diameters were approaching 10 microns as the packaging and PCB industries worked closely together. Through-silicon-vias presented no technology challenge, but the overall cost was too high and fan-out technology offered a viable low-cost alternative. An important message was that whatever might be achieved in maximising the system performance whilst miniaturising the packaging, cost was always the over-riding consideration: "New technology can't exceed the product cost budget!"

Dr. Ma commented that the demand for continuous enhancement of electronic systems never stop, focusing on miniaturisation, optimised system performance and, most critically, continuous cost reduction. The PCB industry would provide its own solution in flexible circuits and, as PCB and IC substrate technologies continued to converge, would continue to work closely with the packaging industry to provide advanced substrates to enable electronic system improvement. Some new technologies would become mainstream and induce a shifting of roles and responsibilities within the supply chain of electronic hardware manufacturing, the impact of which remained to be observed.

Dr. Ma's presentation provided a most appropriate context for Prismark's Phil Plonski to consider how creative designs and new manufacturing technologies would shape the future of the PCB industry. "There's a lot more to come!" His figures indicated that more than two-thirds of global electronics industry production was presently based on networked communications, and forecast that this share would be maintained over the coming five years as the industry continued to expand with an annual growth rate of 3.8%. He did comment that the eventual growth rate in cash terms might not be as big as forecast, simply because things were getting less expensive!

In mobile electronics, the trends towards thinner and lighter were being supported by robust and thin enclosures, integrated displays and touch panels, and thin packages, substrates and components. Cloud-access-anywhere-anytime was facilitated by faster cellular standards on more frequency bands. Faster multi-core processors and faster memory access enabled faster computing. There was increasing use of sensors at the user interface for navigation, gaming and virtual reality, and software developments kept pace with the hardware.

The global PCB market could be segmented in many ways, by geography, application, layer count, laminate type or fabrication methodology. Over the past decade, the fastest growing technology segments had been IC substrates, flex and microvia HDI. Presently, the growing segments were flex and microvia HDI, largely due to progress in smartphone and tablet markets. Another growth area was commodity products based on CEM materials used in LED lighting applications. And all technologies were

relevant to the ongoing progress of the world market for PCBs.

To illustrate how designers were challenging the PCB and packaging industries to meet the goals of higher performance, smaller performance and lower cost, Plonski showed a series tear-down cross-sections of components, modules and packages from currently available smartphones, demonstrating their amazing complexity and ingenuity. As a contrast a white-label Chinese smart-phone that could be purchased very cheaply from the grocery store was based on a relatively simple 6-layer board and five basic modules—not the latest technology, but an example of the intelligent integration of available low-cost building blocks to produce an attractive-looking device with a surprising level of functionality.

RF modules had undergone a substantial module size reduction by integration of multiple functions in the same die, multiple functions within the same package and tighter assembly within the package. "You no longer have to be an RF engineer to buy a pretty sophisticated device!" Incredibly complex hybrid multi-mode, multi-band power amplifier modules could be bought for less than $10, and as an example of form factor reduction a 128Gb disk drive could now be made the size of a postage stamp.

With many more illustrative examples, Plonski demonstrated the convergence of PCB assembly and semiconductor packaging, with designers working together and thinking in three dimensions. The standard recipes of the past were giving way to new methods of innovation. Advanced packaging technology and rapidly maturing fabrication technologies were becoming generic, enabling many creative designs and lots of crazy applications, for example activity monitors that modified behaviour, like the Japanese intelligent fork that tells you when you're eating too fast, and serious ones like medical tricorders, previously Star Trek science fiction but now subject of X-Prize competition. There would be a revolution in clinical diagnostic equipment trends as the cost of these tools began to fall dramatically. The concept of the Google driverless car, an example of making a whole lot of sensors work together, was becoming accepted, and Google glass was a good example of clever packaging technology.

He envisaged that electronics would continue to play a role in our lives in many ways, with micropackaging providing tools to increase functionality per unit cost and create positive economic value. Technology innovation was alive and well, but increasing R&D and capital costs would force consolidation to only a few main players with many outsourcing partners. **PCB**

Based in the UK, Pete Starkey joined I-Connect007 as its technical editor in 2008. Most recently, Starkey was products editor and Europe editor for CircuiTree and has more than 30 years experience in the PCB industry, with a background in process development, technical service and technical sales. To contact Starkey, click here.

PCB007 Supplier/New Product News Highlights

Fineline Enhances Euro Support as Key Viasystems' Rep

"We are confident that the cooperation with Viasystems will enable Fineline to offer our customers the best possible support for their PCB requirements. With Fineline's capabilities in terms of global presence, technological expertise, and excellence in service, we'll be able to enhance our market support to PCB customers in Europe," said Orna Kleinman, president of Fineline Global.

Isola's I-Speed Endorsed as Laminate Choice for PCBs

Isola Group S.à r.l. announced that I-Speed has been endorsed by two leading companies as the laminate of choice for PCBs using sequential lamination technology, requiring high conductive anodic filament (CAF) reliability and improved, cost-effective signal integrity.

Nordson MARCH Launches New MaxVIA-Plus

The new MaxVIA-Plus plasma treatment system accommodates larger panel sizes within a small footprint during electronic circuit board fabrication for desmear, etchback, and landing pad cleaning operations.

Rogers' PCB Materials Hits Record Q1 Sales of $58.5M

Printed Circuit Materials reported all-time record net sales of $58.5 million for the first quarter of 2014, an increase of 34.4% from the $43.6 million reported in the first quarter of 2013.

Orbotech's Revenue Falls in Q1

"While the PCB industry experienced a low level of production utilization in certain segments during the first quarter, our FPD business experienced a very strong quarter, with over $65 million in new bookings for our recently introduced products, expected to be delivered mainly in late 2014 and early 2015," says Asher Levy, CEO.

Rogers Opens Innovation Center in Massachusetts

Rogers Corporation held a ribbon-cutting ceremony to dedicate the company's new Innovation Center in Burlington, Massachusetts. More than 125 government officials, community leaders, technology company representatives and other guests were on hand to celebrate and tour the Center located in Northeastern University's George J. Kostas Research Institute for Homeland Security.

Gardien Japan is Now Exclusive Polar Distributor

Gardien Japan Co., Ltd. has become the exclusive distributor for Polar and PWB products and services in Japan. Sales and support efforts will ramp up during the month of May, and will allow for significantly expanded and reliable product distribution and after-sales support throughout the Japan market.

Ohmega Forms Process Support Group

The Group's charter is to lend technical and logistical support for PCB shops interested in processing OhmegaPly embedded resistive technology.

Siber Circuits Earns UL Cert for Aismalibar IMS Materials

Siber Circuits has received their UL listing for Aismalibar's Cobritherm line of Insulated Metal Substrate materials. The certification allows Siber to UL stamp their products using the entire line of Cobritherm materials, which includes ALCUP-G 1.3w, ALCUP 1.8w, HTC 2.2w and HTC 3.2w.

Uyemura to Provide Solutions to eSurface Licensees

eSurface Technologies the developer of the eSurface manufacturing process for PCBs, has confirmed that Uyemura, USA, has become an eSurface Certified Supplier, effective immediately. Uyemura will support the eSurface licensee's needs for products in the facilitation of the eSurface process.

The Degrees of Nickel Hyper-Corrosion and Mitigation Strategies

by Michael Carano
OMG ELECTRONIC CHEMICALS

Introduction

In previous columns, I presented information on electroless nickel-immersion gold and possible concerns with black pad and brittle fracture. I am a firm believer (as well as a stickler) for tight process control. In addition, this also means that understanding the root cause or causes of defects must be pursued with vigor! As a case in point, in this month's column, I will present additional information about nickel hyper-corrosion by further defining the five degrees of hyper-corrosion. This implies that certain levels of the attack on the nickel are more detrimental than others. It should be noted that for purposes of this writing, I define hyper-corrosion as a spike or fissure in the nickel deposit evident after immersion gold plating. Finally the root causes of such attack on the base nickel will be presented along with strategies to mitigate these effects.

The Five Degrees of Hyper-corrosion

As the title of this column implies, we have identified five degrees of hyper-corrosion. While somewhat arbitrary, the extent of the corrosion spikes or fissures are responsible for the rating given. We found it necessary to provide this input to the industry as we found that, all too often, the OEM sees a tiny fissure in the nickel deposit and makes the false assumption that the PCB will fail in some way. That is categorically false, and I will explain why. First, however, let's review the definition of each of the degrees of hyper-corrosion:

1. Level 1: Only a few spike-type defects and not on every pad observed.
2. Level 2: A few spike-type defects observed on most pads.
3. Level 3: More than a few spike-type defects and some spreader/spike defects on most pads observed. At this activity level, more than 99% of the solder surface has not degraded or shown signs of increased phosphorus and as such should not inhibit intermetallic formation.
4. Level 4: More spreader/spike defects and some area black band defects on most pads observed. This activity level may degrade solder joint integrity.
5. Level 5: Mostly large areas of continuous black band on many pads observed. This level of defect activity will affect solder joint integrity.

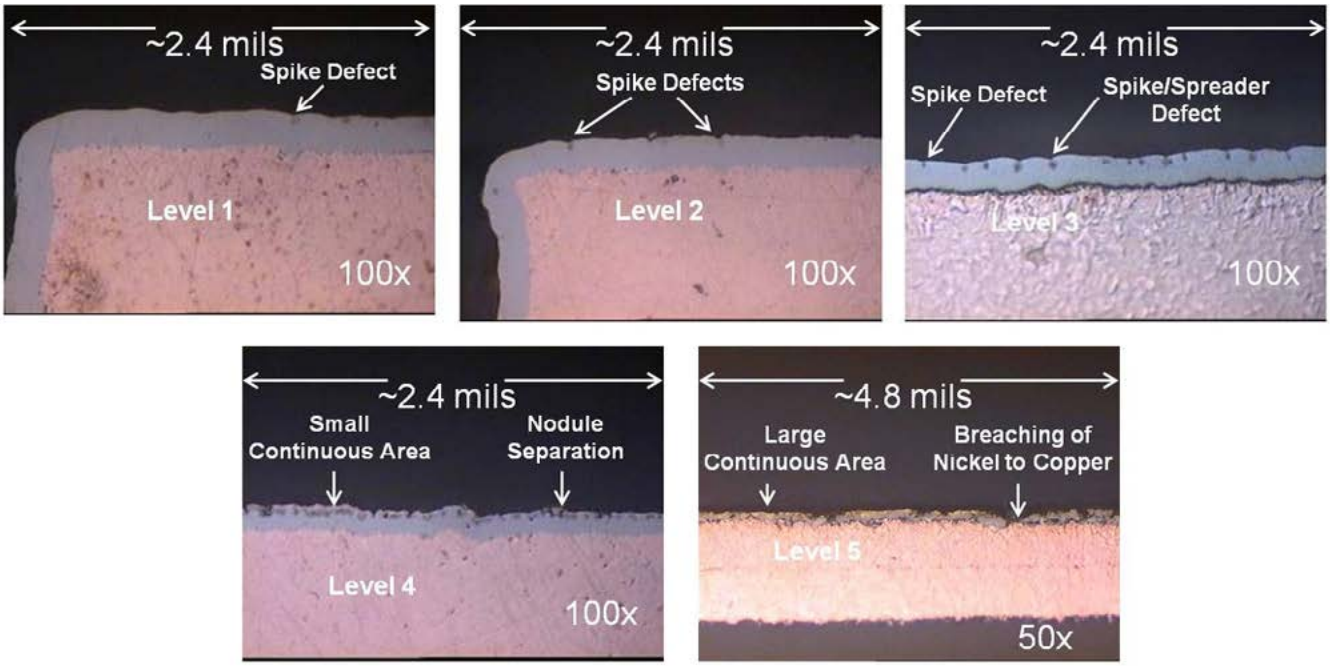


Figure 1: Degrees of hyper-corrosion.

Actual sections showing the levels of hyper-corrosion are shown in Figure 1.

Due to extensive wetting balance and solder spread testing (along with BGA shear testing), Level 1 and Level 2 conditions did not result in failures. Wetting forces and solder joint strengths continued to meet criteria for acceptability. Certainly, Levels 3–5 are cause for concern. Although Level 3 spikes do not lead to wetting failures, this condition would be an indicator for future reference. So again, be vigilant with respect to categorically rejecting parts for very minor imperfections. If that was the case, the entire IPC-600 document would be re-written where even the most minor imperfections would fall in the non-conformance category.

So what would you do with the following? Figure 2 shows Level 2 corrosion spikes (left) and on the right a section with Level 3 spikes. Note there is no issue with solder wettability in either of the soldered sections.

Again, it is important to recognize that on occasion there will be minor corrosion spikes visible within the nickel deposit. And one should not rush to judgment and categorically reject the circuit boards without first studying solderability data. Regardless, there are numerous strategies and process control techniques that can be employed to eliminate any of these issues. Some of the most critical controlling the phosphorous and gold contents.

Control the Phosphorous Content

Yet it stands to reason that the lower the phosphorous content in the nickel deposit, the greater the possibility of corrosion. So one may decide to (by design) utilize an EN process that tends to co-deposit a higher phosphorous content upwards 10–11% by weight. While this level of phosphorous will certainly minimize the chance of hyper-corrosion, there are also two negative impacts. The first is the possibility of a thinner gold deposit. This stands to reason since the gold deposition mechanism relies on the electromotive force to drive the reaction. The more corrosion resistant the nickel, the thinner the immersion gold deposit. Thus the IPC ENIG spec could easily be violated. The second concern is that the higher phosphorous content of the nickel will negate proper solderability of the nickel (reduced wetting).

I suggest that in order to optimize the thickness of gold (within spec) and enhance solderablity without excessive corrosion, engineers

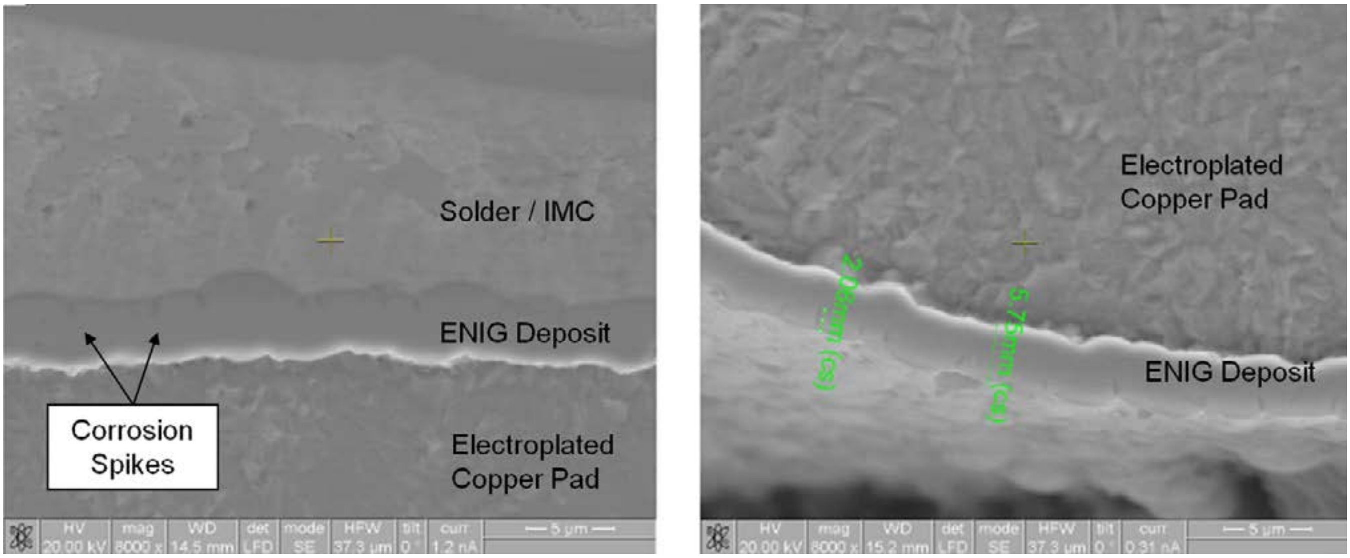


Figure 2: Level 2 (L) and Level 3 (R) corrosion spikes. Section shows excellent wettability and solder joint formation.

should control the phosphorous content of the nickel to 8.3 ±0.5%. Again, consult with the chemical supplier to ensure proper controls exist to insure the consistent phosphorus content through five metal turnovers of the electroless nickel plating solution.

Control the Gold Content

One does not have to be a metals trader or buyer to know that gold metal pricing has flirted with the $2000 per troy ounce level in early 2012. Thus, gold cost is a significant driver in the total cost of the ENIG process. Fabricators are looking for ways to reduce the impact of gold. One way to accomplish this is to lower the concentration of the gold metal in the working solution. While many immersion gold processes require a gold metal concentration range of 1.0–1.5 grams per liter, it is suggested that lower gold concentrations may be beneficial. Of course, this is only valid if the lower gold does not lead to hyper-corrosion of the nickel. One way to ensure that this is effective is to build a first article and inspect the boards after ENIG. In addition, some suppliers have made sufficient improvements in the gold plating solution itself. These improvements have allowed for lower gold concentrations (0.4–0.75 grams/liter) to be employed with significant savings

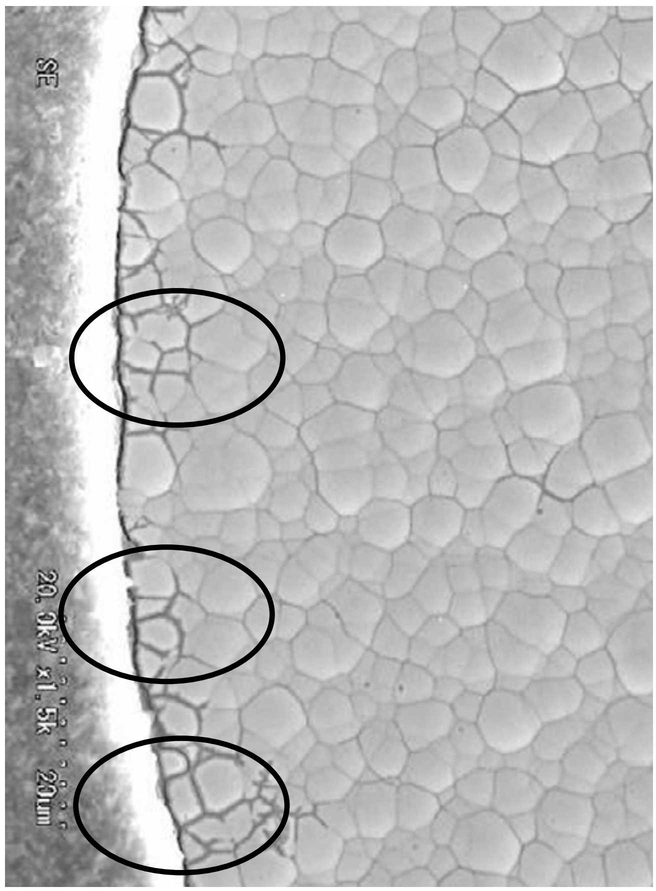
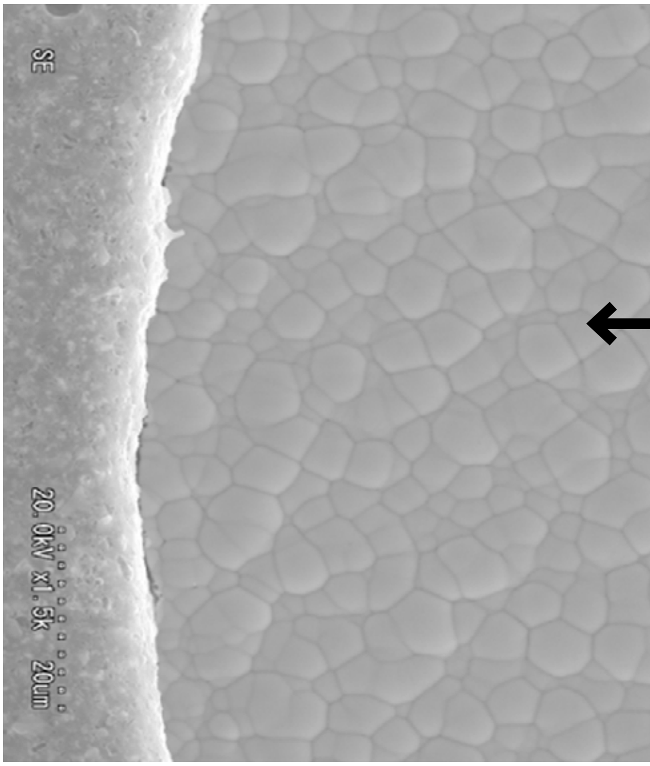


Figure 3: Conventional Immersion gold at 1.0 gram/liter. Note circles around the area of severe hyper-corrosion.



realized. However, attempting to use lower gold concentrations without an improved process in general will lead to disaster.

There are other factors that influence the potential for corrosion spikes. These will be presented in a future column of *Trouble in Your Tank*. **PCB**

Figure 4: Lower gold content solution with electroless nickel process with tighter phosphorous content range. Note: no corrosion spikes.

Michael Carano is with OMG Electronic Chemicals, a developer and provider of processes and materials for the electronics industry supply chain. To read past columns, or to contact the author, click here.

VIDEO INTERVIEW

Supplying Unusual Flex to Meet Customers' Needs

by Real Time with...IPC APEX EXPO 2014

Joe Fjelstad interviews Pete Uka, Director of Technology at Q-FLEX Inc about the challenges of supplying unusual flex circuits and specialty products, such as a recently completed 15-ft long flex and a flex circuit smaller than a grain of rice!

CLICK TO VIEW

realtimewith.com

Mil/Aero007 News Highlights

Saab to Acquire ThyssenKrupp, Inks MoU

ThyssenKrupp Industrial Solutions AG, a subsidiary of ThyssenKrupp AG, and Saab AB have signed a non-binding Memorandum of Understanding concerning the sale of the Swedish shipyard ThyssenKrupp Marine Systems AB (formerly named Kockums) with operations in Malmö, Karlskrona and Muskö to Saab AB.

Celestica Earns Supplier Award from Rockwell Collins

The company was presented with the 2014 Assemblies Supplier of the Year Award from Rockwell Collins during the recent Annual Supplier Conference held in Cedar Rapids, Iowa. The award is an acknowledgement of significant contributions made during the year by suppliers and is based upon quality, delivery, total cost of ownership, lead time, and customer service.

Sypris' Electronics Group: 16% Revenue Increase in Q1

The company reported revenue of $84.2 million for the first quarter compared to $78.4 million for the first quarter of 2013. Revenue for the Electronics Group expanded 16%, to $8.4 million in the first quarter, an increase of $1.1 million from $7.3 million in the comparable prior year quarter.

Ducommun Posts 2.2% Sales Increase in Q1

"The first quarter of 2014 showed the diversity of Ducommun's product portfolio and strength of our operating leverage," said Anthony J. Reardon, chairman and CEO. "Top line growth was driven by gains across our commercial aerospace business, including a further pickup in revenue with Airbus and on Boeing's 787 platform. Operating margins expanded year-over-year reflecting higher revenues and an improved product mix."

Digicom Electronics Earns ITAR Registration

"Our attention to quality and detail and our ability to handle low-volume, high-end products has enabled us to prototype and manufacture many military, aerospace, and government-related projects," explained GM Mo Ohady. "Receiving ITAR certification expands the base of projects we can accept and gives more flexibility to our customers."

OnCore Implements E2open's Supplier Collaboration Solution

OnCore Manufacturing LLC, a global supplier of EMS, has implemented E2open's supplier collaboration solution. E2open enables OnCore to offer more effective customer service, given the real world of unpredictable demand.

Cal Quality to Support Boeing's CSEL Program

The company announced a multi-year, multi-million dollar contract signing with The Boeing Co. to support the Combat Survivor Evader Locater (CSEL), a major government program that is the U.S. Department of Defense (DoD) Program of Record for Joint Search and Rescue.

API Nets $1.6M Filter Solutions Order

"Our customers in the electronic warfare arena demand products that address a broad set of technical requirements with unparalleled performance and reliability," said Bel Lazar, president and CEO, API Technologies. "As a supplier to both emerging and existing EW platforms, our products are helping save the lives of warfighters from our armed forces and allies around the world every day."

Probe Order Backlog Rises to $3M; To Meet Target

Kam Mahdi, CEO, commented, "Our order backlog puts us in excellent position to meet our revenue target of 20% year-over-year growth by the end of 2014. We strongly believe that manufacturing for small- to medium-sized businesses is coming back to the U.S. We have witnessed businesses of this size become adversely affected by the subsequent increase in costs, unmanageable processes, and intellectual property protection concern of manufacturing abroad."

Nortech: Modest Growth in Q1; Continues Improvements

"We're pleased to see our pretax profits rise 13% on a slight sales increase," said Rich Wasielewski, president and CEO. "While the mixed economic recovery is impacting each of our customers differently, we continue focusing on improving our operating performance by managing the areas under our control and actively working on building a qualified sales pipeline."

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Here's what one of our customers had to say about Prototron...

"I have been using Prototron for more than two decades. This includes working for four different companies and a few more as a consultant. Throughout this time period, Prototron has never let me down and has always made me look good as an employee and a consultant. I have never gotten a single board error in the hundreds of different boards I have ordered. This includes simple two layer boards, complicated 12 layer boards and everything in between. They are extremely consistent in delivery times. They can handle large quantity jobs and extremely fast turn around if you need it.

Over the years I have had a variety of difficult and unusual mechanical issues on my boards. Recently I have had a board set with unusual hole patterns that needed to be routed in half. They were very helpful with DFM consultation on this project and have again been very consistent with perfect quality. Many board houses would not even quote this job and the one time I ordered the identical board from another "production-only" vendor, it was a disaster. Late delivery and poor quality.

The entire staff is very friendly and even though they do a very large volume of business, you feel as if it is the "little board house around the corner". My current company does a fair amount of business in Denver and I was impressed when I was talking to an assembly shop in Denver and without knowing anything about me or where I lived, they waxed on about the unique abilities of Prototron.

Great attitude, good prices, fantastic service, 100% perfect quality...what's not to like?

Bill Barnard
Principal Engineer and All Round Good Guy
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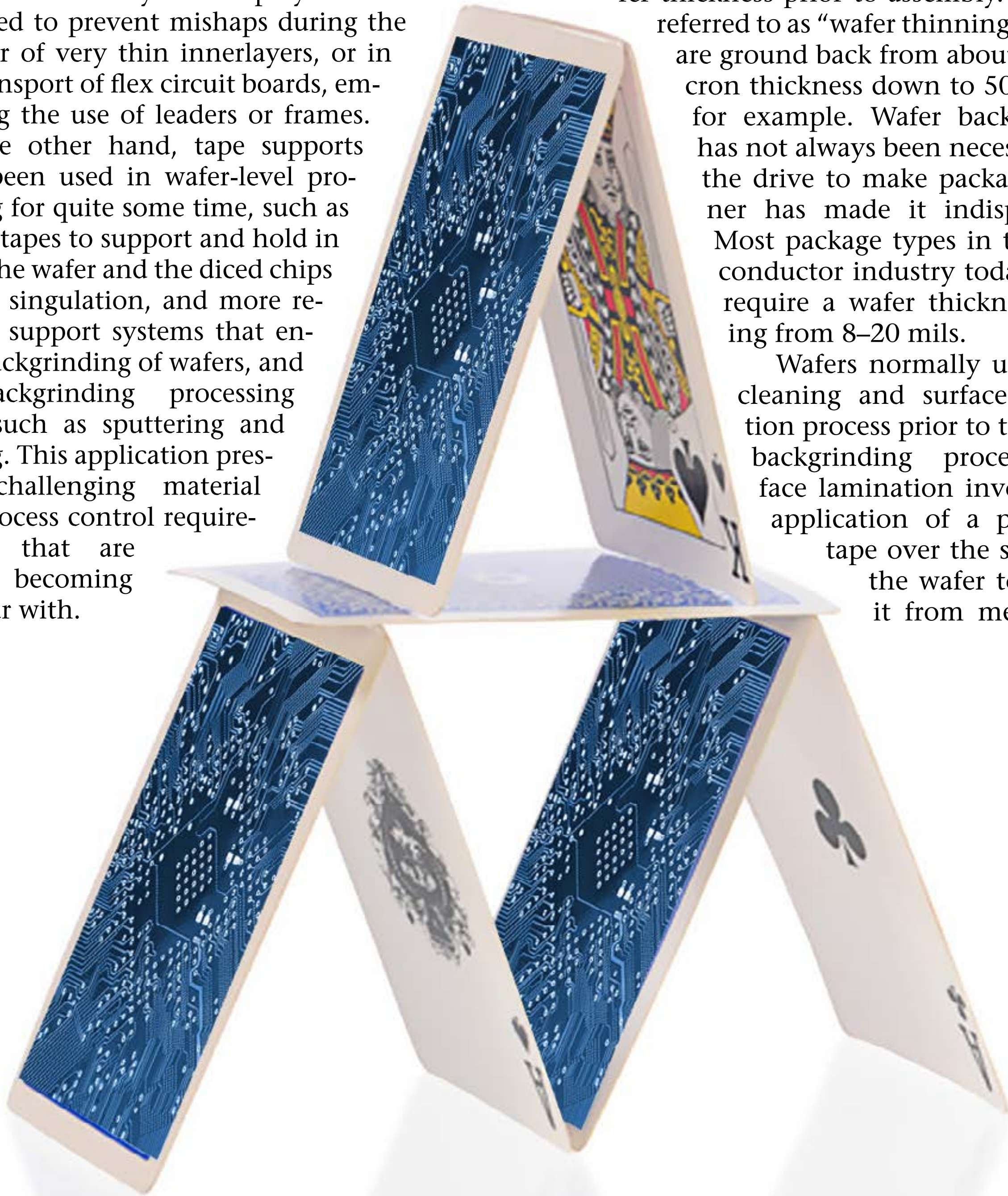
Supporting Thin Structures

by Karl Dietz
KARL DIETZ CONSULTING LLC

In the world of PCB fabrication, there are few examples of special support features for thin substrates. But they do exist in the form of assist features in conveyorized spray modules designed to prevent mishaps during the transfer of very thin innerlayers, or in the transport of flex circuit boards, employing the use of leaders or frames. On the other hand, tape supports have been used in wafer-level processing for quite some time, such as dicing tapes to support and hold in place the wafer and the diced chips during singulation, and more recently, support systems that enable backgrinding of wafers, and post-backgrinding processing steps such as sputtering and plating. This application presents challenging material and process control requirements that are worth becoming familiar with.



Background Information

Wafer backgrinding is the process of grinding the backside of the wafer to the correct wafer thickness prior to assembly. It is also referred to as "wafer thinning." Wafers are ground back from about 300 micron thickness down to 50 micron, for example. Wafer backgrinding has not always been necessary, but the drive to make packages thinner has made it indispensable. Most package types in the semiconductor industry today would require a wafer thickness ranging from 8–20 mils.

Wafers normally undergo a cleaning and surface lamination process prior to the actual backgrinding process. Surface lamination involves the application of a protective tape over the surface of the wafer to protect it from mechanical

damage and contamination during backgrinding.

The surface-laminated wafers are then loaded into cassettes that will go into the cassette holder of the backgrinding machine. The machine picks up the wafer from its backside (untaped side) with a robotic arm, which positions the wafer for backgrinding. The process is automatically accomplished by a grinding wheel, following a precise set of parameters to ensure proper backgrinding.

To remove debris from the wafer, it is usually washed continuously with D/I water while undergoing backgrinding. Once the wafer has been background, the wafer is returned to the cassette, and the cycle is repeated for the next wafer.

Parameters set for backgrinding include spindle speed, spindle coolant water temperature and flow rate, D/I water temperature, initial and final wafer thickness, and feed speeds.

Problem areas:

- Die cracking/chipping: occurrence of fracture or chipout anywhere in the die. Common causes in the context of backgrinding: incorrect backgrind parameters resulting in excessive stresses on the wafer
- Die scratching: inducement of any mechanical damage on the die, as when an operator scratches a die with tweezers due to mishandling. Common causes: insufficient operator training, use of improper tools
- Die metallization smearing: depression or deformation of any metal line on the die surface. Common causes: foreign materials on the backgrind tape, wafer mishandling
- Die corrosion: corrosion of the metallic parts of the die as a result of prolonged exposure to water during backgrinding

“*After thinning, there are several processing steps on the backside of the wafer, involving challenging physical and chemical environments that the handle-wafer and its bond layer have to survive. These include high-temperature and low pressure processes such as chemical vapor deposition, sputtering, plating, and etching. In particular, it is the polymeric bonding layer that is vulnerable to chemical degradation and stress cracking.*”

Most tapes rely on UV-curing to “de-tackify” the tape. Some tapes are not UV-cured and may rely on pressure-sensitive adhesives.

UV curable tapes differ from non-UV tapes in that they must be exposed to a UV light source prior to removal. This makes it possible to achieve a higher tack during processing while ensuring ease of removal after exposure.

Backgrinding and TSV Formation

Through-silicon via (TSV) formation is the key enabling technology for 3D packaging of chips, notably of memory chips. While there are several processes for forming TSVs, the following process sequence seems to dominate: After CMOS processing has been completed on the device wafer, vias are dry etched (e.g., by the Bosch process) from the active side of the wafer down to the inactive side of the wafer to form blind vias, which are then metallized. A “handle wafer,” covered with a bonding layer, is then brought in contact with the active side of the wafer. Then follows the backgrinding step that removes silicon all the way to the bottom of the blind vias to open them up and form through-silicon vias.

After thinning, there are several processing steps on the backside of the wafer, involving challenging physical and chemical environments that the handle-wafer and its bond layer have to survive. These include high-temperature and low pressure processes such as chemical vapor deposition, sputtering, plating, and etching. In particular, it is the polymeric bonding layer that is vulnerable to chemical degradation and stress cracking. Thermoplastic resins appear to be more suitable in this application than are thermoset resins[1]. After completion of its support function, the support wafer with its bonding layer needs to be removed, either by dissolving the bonding resin, for which process the support wafer needs to be porous to allow for solvent penetration, or by heating and softening the bond layer and sliding off the support structure ("thermal slide process").

Permanent Wafer Bonding

These technologies are all temporary bonding techniques for support of a thin wafer through demanding processing steps. It should be mentioned that there are quite a few wafer bonding applications that have in common that the bond is intended to be permanent. There are two types of such permanent bonding processes: bonding techniques that make use of an intermediate layer and those that don't use an intermediate layer. Examples of bonding without an intermediate layer are anodic bonding and direct silicon bonding. Examples of bonding with an intermediate layer are glass frit bonding, solder bonding, and adhesive bonding. These bonding techniques find applications in MEMS fabrication. **PCB**

References

1. 3D IC Thin-Wafer Handling Materials Requirements, Mark Privett, Chip Scale Review, Nov./Dec. 2012, pg. 24.

Karl Dietz is president of Karl Dietz Consulting LLC. He offers consulting services and tutorials in the field of circuit board & substrate fabrication technology. To view past columns or to reach Dietz, click here. Dietz may also be reached by phone at (001) 919-870-6230.

Flying Probe: Indirect Testing vs. Military

by Todd Kolmodin
GARDIEN SERVICES USA

Introduction

The use of flying probe testers has become increasingly popular in recent times, mainly due to the affordability of the equipment and also the reduced cost of testing, as no dedicated or "bed of nails" fixture is required. When using flying probes to test military product, one must be diligent to make sure the test method is allowable. Table 1 below outlines the military specifications and whether indirect testing is performed on a flying probe vs. a grid test machine. Grid test machines provide full net to net testing for isolation of all nets and full continuity of individual nets. This is referred to as full simultaneous test. When a flying probe is used there are two modes of operation: direct or indirect.

Direct Testing

When a direct test is used the machine will test every board in resistance mode, meaning that every net will be resistively tested for both opens and shorts. Each board will take the same time to test. When the isolation (shorts) test is performed, nets will be tested using an adjacency window. This is different than a bed of nails whereby which each net is tested simultaneously to all other nets using the voltage and isolation resistance thresholds. With a flying probe only nets within the adjacency window are tested to others. Industry accepted practice for this adjacency window is .050" (1.27 mm). Also to be considered is the type of adjacency used. Standard practice is X,Y adjacency or "line of sight," meaning only on the same layer. If Z-axis adjacency is added, the adjacency window becomes three- dimensional and isolation testing is done not only on the same layer but within the adjacency window on layers above and below.

		Military Specifications			Indirect IPC-9252A - Am 1		
Specification	Revision	Voltage Minimum*	Isolation Minimum	Continuity Maximum	Class 1	Class 2	Class 3
MIL-PRF-31032	B	40 VDC Minimum	>2 Meg Ohm	10 Ohms	-	-	-
Mil-PRF-31032	/1C	40 VDC Minimum	>2 Meg Ohm	10 Ohms	Yes	Yes	Yes*
MIL-PRF-31032	/2B	40 VDC Minimum	>2 Meg Ohm	10 Ohms	Yes	Yes	Yes*
MIL-PRF-31032	/3B	40 VDC Minimum	>100 Meg Ohm	10 Ohms	Yes	Yes	Yes*
MIL-PRF-31032	/4B	40 VDC Minimum	>100 Meg Ohm	10 Ohms	Yes	Yes	Yes*
MIL-PRF-31032	/5A	40 VDC Minimum	>100 Meg Ohm	10 Ohms	Yes	Yes	Yes*
MIL-PRF-31032	/6A	40 VDC Minimum	>100 Meg Ohm	10 Ohms	No	No	No
MIL-PRF-50884	F	40 VDC Minimum	>10 Meg Ohm	20 Ohms (Qual) 10 Ohms Production	Yes	Yes	Yes
MIL-PRF-55110	G	40 VDC Minimum	>2 Meg Ohm	20 Ohms (Qual) 10 Ohms Production	No	No	No

Table 1: Indirect Military & IPC.

TEST LEVEL	A	B	C
Performance Class	1	2	3[5]
Source Data	CAM, CAD	CAM, CAD	CAD[1]
TEST METHODS			
Resistive Continuity Testing	≤ 100Ω	≤ 50Ω	≤ 10Ω[4]
Resistive Isolation Testing	≥ 500kΩ	≥ 2MΩ	≥ 10MΩ
Indirect Isolation & Continuity Testing by Signature Comparison	Yes	Yes	AABUS
Adjacency (for isolation testing)[2,3]	Yes	Yes	AABUS
Required Testing of Accessible Midpoints[6]	No	No	Yes

Note 1. See 5.1.2
Note 2. Default minimum of 1.27 mm [0.050 in] or AABUS.
Note 3. Includes horizontal and/or line of sight adjacency; vertical adjacency is not required unless specified.
Note 4. For referee purposes, 0.5 maximum for each 25.0 mm [0.984 in] of circuit length **shall** apply.
Note 5. For Class 3/A Performance Requirements, see IPC-6012.
Note 6. Conductors not covered with solder mask or via plug material.

Table 2: IPC-9252A amendment 1.

Indirect Testing

Indirect testing however uses a reference plane or planes to develop a "signature" or capacitive master. This is why you will see the term "indirect testing by signature comparison." When this methodology is used the first board tested will go through the capacitive gather and then a full continuity and isolation (using adjacency) test against the set threshold parameters. Once this is complete the signature or master is written. On the second and subsequent boards the capacitive gather is done and then compared to the "signature" or master. Only nets that are identified as "outside" of the signature or master comparison will be retested under resistive parameters for either opens or shorts. The entire board does not receive the full resistive test for opens and shorts as provided by the direct test method. Capacitive scanners also fall into the arena of indirect testing. The UUT is placed on the scanner and two passes are made. This is the same as the capacitive gather on the flying probe but thousands of probes are used rather than the limitation of arms on the flying probe. This eliminates up to 90% of the test that a general flying probe would use. Then, using a flying probe, the resistive retest is performed. The end result is the same, but time in testing using this combination is reduced significantly.

IPC and Military Considerations

Now the question arises as to when one can safely test using indirect testing by signature comparison? In general, IPC-9252A amendment 1 (Table 2) does allow the use of indirect testing across all performance classes A–C. However, the caveat here is that with Class 3 (C) this must be agreed upon between the manufacturer and end user, known as AABUS (as agreed upon between user and supplier). Also what must be agreed upon is the use of adjacency (isolation) testing on Class 3 (C) product. One should always review the procurement document or fabrication drawing as many Class 3 (C), Class 3/A (aerospace and military avionics) and high-reliability medical products will not allow the use of flying probe at all.

Further it must be understood that not all remaining military product can be tested using indirect testing by signature comparison. Although the defense logistics agency (DLA) has released updated revisions to MIL-PRF-31032, MIL-PRF-50884 and MIL-PRF-55110, one cannot assume that any test method can be used on military product. Although the DLA uses IPC-

9252A amendment 1 as a test guideline there are limitations in each specification. With MIL-PRF-31032 only the build requirement sheets /1 through /5 allow the use of indirect testing. The /6 build requirement sheet does not (Table 1 and 2). Additionally, the MIL-PRF-55110 specification does not allow indirect testing at all. Full continuity and indirect (or sometimes called field measurement) does not satisfy the MIL requirement when indirect testing is not allowed.

Conclusion

Always review the fabrication and/or procurement document to ascertain what specification the product is being manufactured/tested to. This will always override the industry specification. Be careful with military product as it cannot be assumed that it can be processed on flying probe equipment using indirect testing. Further, when indirect testing can be used on Class 3 (C), Class 3/A, and military product, such use of indirect testing and adjacency must be agreed upon between the manufacturer and end user.

In these instances the allowance of indirect testing must be AABUS, as noted in IPC9252A amendment 1. This means that it must be stipulated up front via the PO or procurement document. Although the military specifications noted allow this, it is not inferred or allowed without the written consent of the manufacturer requiring such test. It shall be the directive of the individual test center via its duly appointed director or sales representative to solicit this information. **PCB**

Todd Kolmodin is the vice president of quality for Gardien Services USA, and an expert in electrical test and reliability issues. To contact Kolmodin, or to read past columns, click here.

PCB007 News Highlights This Month

1 Viasystems' Sales Up 8.4%; Q2 Growth Expected

"While the markets we serve did not demonstrate any significant strength, and in some instances declined both year-over-year and sequentially, we were able to generate net sales and earnings in line with our first quarter expectations," said CEO David M. Sindelar. "In terms of our end markets, our automotive, telecommunications, and military and aerospace sectors performed as expected."

2 Speedy Circuits Looks West for More Business Prospects

Speedy Circuits has seen a marked increase in output of prototype PCBs at its board fabrication facility in Taiwan lately due to strong demand from numerous ICT companies. Demand for HDI PCBs in particular has been strong since it beefed up its board fabricating capabilities two years ago with the acquisition of several advanced processing equipment that include Orbotech InCAM systems, Mitsubishi laser drill, Orbotech LDIs, and more.

3 IPC: N.A. PCB Book-to-Bill Shows Positive Growth

"The book-to-bill ratio's climb and positive year-on-year sales growth in March are encouraging signs of a recovery ahead," said Sharon Starr, IPC's director of market research. She cautioned, however, that "the book-to-bill ratio has just reached positive territory after six consecutive months below 1.00. Economic indicators are positive for 2014, but the PCB industry's recovery is developing slowly."

4 HEI Suffers 53% Q1 Sales Drop

HEI, Inc. has announced unaudited financial results for the first quarter of 2014, which ended March 29, 2014. Sales in the first quarter of 2014 were $5,944,000, compared to $12,516,000 in the first quarter of 2013. The company generated a net loss of $896,000 in the first quarter of 2014, compared to a net income of $636,000 in the first quarter of 2013.

5 Graphic PLC Ups North American Presence

Scott Kohno, president of Graphic USA announced that Graphic PLC has begun its strategic penetration of the North American market. Graphic PLC bought CalFlex USA last summer with plans to increase its market reach into North America.

6 Advanced Circuits Marks 25 Years in PCB Industry

"Advanced Circuits has experienced consistent growth since its establishment in 1989 and currently occupies a dominant market position with the industry's largest customer database," said President and CEO John Yacoub.

7 MFLEX Sees Net Sales Drop 32%

Commenting on the company's business outlook, Reza Meshgin, CEO, noted, "Based on the timing and breadth of new programs expected to ramp across our customer base, we continue to anticipate a significant increase in net sales and a return to profitability, excluding impairment and restructuring, in the fiscal fourth quarter."

8 Despite Loss, TTM Meets Guidance; Sees Demand in Q2

Net sales for the first quarter of 2014 were $291.9 million compared to $366.1 million in the fourth quarter of 2013, and $325.4 million in the first quarter of 2013. First quarter 2013 included $23 million of revenue from TTM's SYE plant, in which TTM sold its controlling equity interest during the second quarter of 2013.

9 Sunstone Named Among Healthiest Oregon Employers

The company earned this award by launching a formal wellness program to encourage healthy lifestyles. By implementing a health incentive, employees who obtain biometric readings, undergo a health risk assessment, and participate in the "Wellness BINGO" challenge have the ability to receive a reduction in their health insurance premiums each month.

10 WUS, Schweizer Collaborate on HF PCB Production

WUS Printed Circuits Co., Ltd. and Schweizer Electronic AG concluded an exclusive long-term agreement on the cooperation for the production of high-frequency PCBs for the global automotive and industrial market.

EVENTS

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar of Events, click here.

For the complete PCB007 Calendar of Events, click here.

MEDTEC Europe 2014
June 3–5, 2014
Messe Stuttgart, Germany

RAPID Conference & Exposition
June 9–12, 2014
Detroit, Michigan, USA

IPC SE Asia Workshop on Soldering of Electronics Assemblies
June 9, 2014
Penang, Malaysia

MedTech MD&M East
June 9–12, 2014
New York, New York, USA

IEEE ICC 2014
June 10–14, 2014
Sydney, Australia

CES Unveiled Warsaw
June 17, 2014
Warsaw, Poland

Upper Midwest Expo & Tech Forum
June 18, 2014
Bloomington, Minnesota, USA

CE Week
June 23–27, 2014
New York, New York, USA

Symposium on Counterfeit Electronic Parts and Electronic Supply Chain
June 24–26, 2014
College Park, Maryland, USA

Ohio Expo & Tech Forum
July 17, 2014
Cleveland, Ohio, USA

SusTech 2014
July 24–26, 2014
Portland, Oregon, USA

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