I-Connect007 Presents

November 2017

the pcb magazine

HDI: Today, Tomorrow and the Future

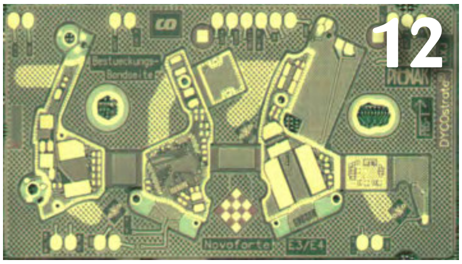
FREE SIGNAL INTEGRITY eBOOK

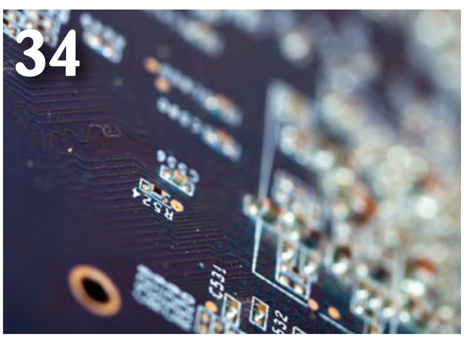
I-007e Books

I-Connect007 Presents
the pcb magazine

November 2017

Featured Content





HDI: Today, Tomorrow and the Future

This month, we cover the wide-ranging topic of HDI: from the latest technology developments and manufacturing challenges, to HDI strategies that include design, fabrication, and assembly perspectives. As one of our feature contributors, Happy Holden, says, in North America, there is a growing need for more HDI capability. Find out why in this issue!

FEATURES:

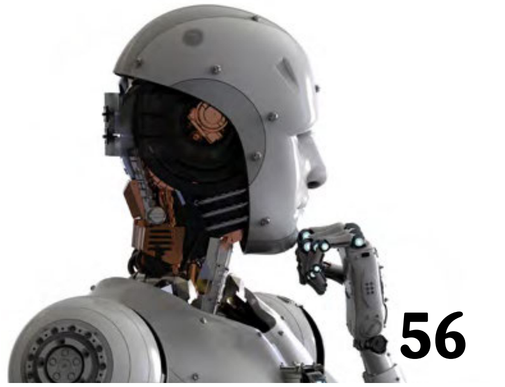
FEATURE COLUMNS:

IConnect007 Presents

the pcb magazine

November 2017

More Content

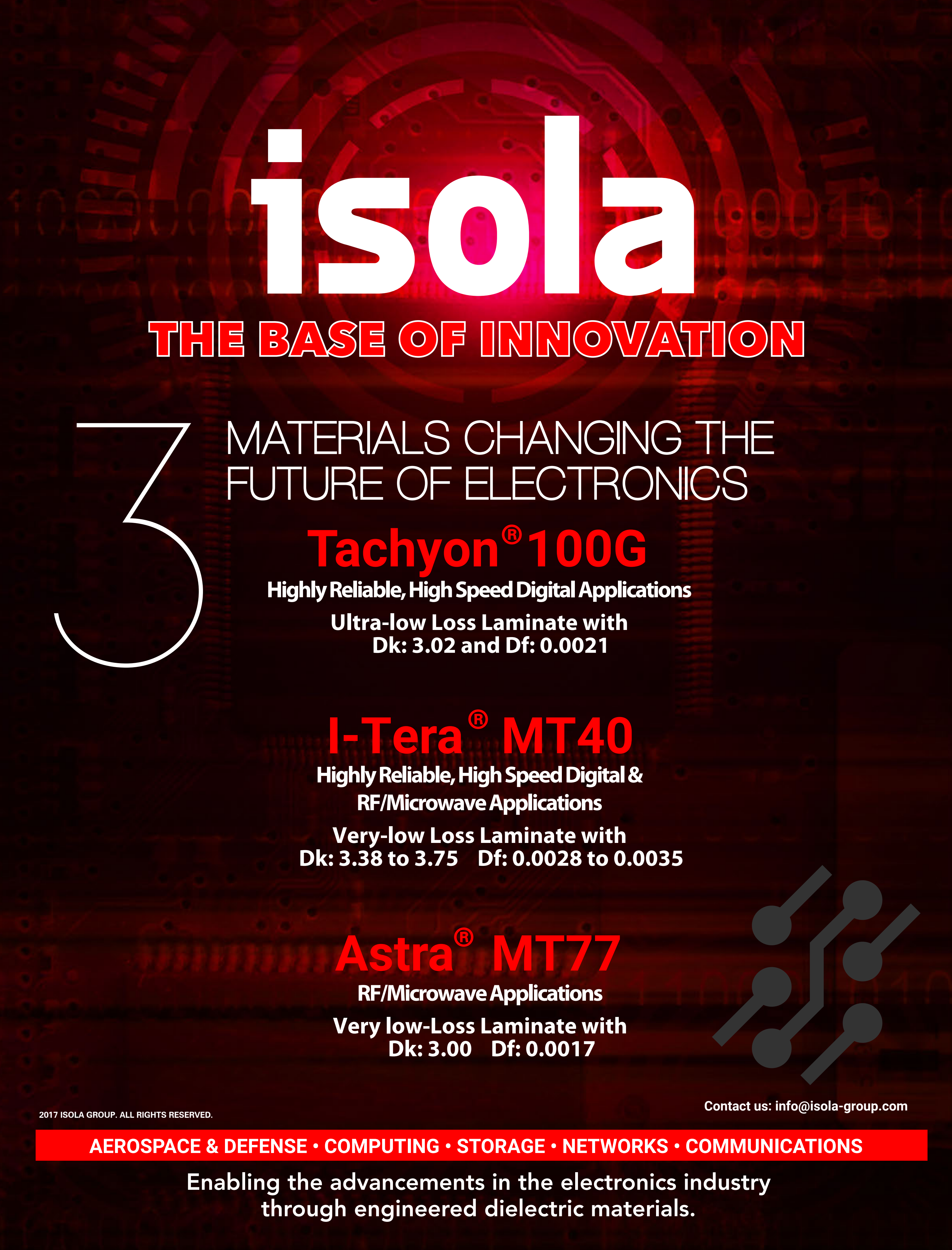


COLUMNS

HIGHLIGHTS

DEPARTMENTS

SHORTS


isola
THE BASE OF INNOVATION
3 MATERIALS CHANGING THE FUTURE OF ELECTRONICS
Tachyon® 100G
Highly Reliable, High Speed Digital Applications
Ultra-low Loss Laminate with Dk: 3.02 and Df: 0.0021
I-Tera® MT40
Highly Reliable, High Speed Digital & RF/Microwave Applications
Very-low Loss Laminate with Dk: 3.38 to 3.75 Df: 0.0028 to 0.0035
Astra® MT77
RF/Microwave Applications
Very low-Loss Laminate with Dk: 3.00 Df: 0.0017
Contact us: info@isola-group.com
2017 ISOLA GROUP. ALL RIGHTS RESERVED.
AEROSPACE & DEFENSE • COMPUTING • STORAGE • NETWORKS • COMMUNICATIONS
Enabling the advancements in the electronics industry through engineered dielectric materials.

HDI: Born in the USA and Making a Comeback

by Patty Goldman
I-CONNECT007

There is no denying that high-density interconnect (HDI) has been around a long time—over 25 years, believe it or not. From almost the moment of its conception in the U.S., the technology was adopted by and used almost exclusively in Asia. It was a puzzlement—and a frustration—as to why the quick move to Asia, and why the U.S. did not pick up on this technology and start making these boards. However, Taiwan, et al., were making most of the consumer products such as cellphones and camcorders, and HDI helped pack the necessary computing power into these devices.

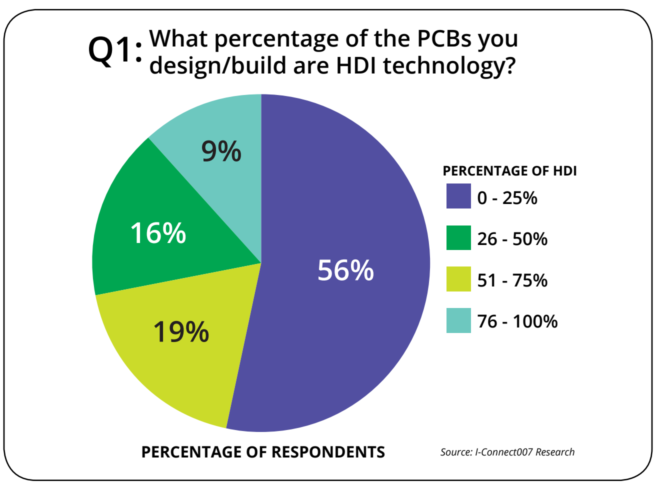
But HDI is back! In this month's reader survey, we learned that while half of the respondents have less than 25% of their production in HDI boards, for some 28% it accounts for more than half their business, and a for a third of those, HDI is their main technology (Question 1). In addition, 30% of all respondents expected their percentage of HDI work to grow to at least 25% and 45% expected it to represent more than half their business (Question 2).

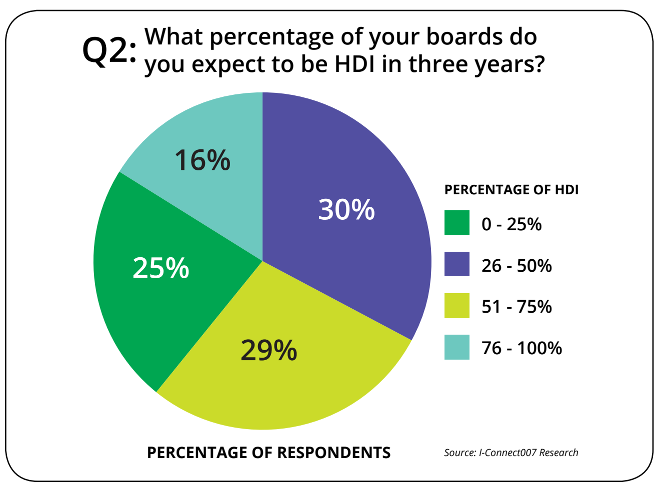
According to our respondents, the three main industry segments using HDI were telecommunications, automotive and consumer electronics. We then asked about market trends: What market trends are driving your HDI work? Obviously, a multi-answer question, but note that many of the answers have to do with density on the board (Question 3).

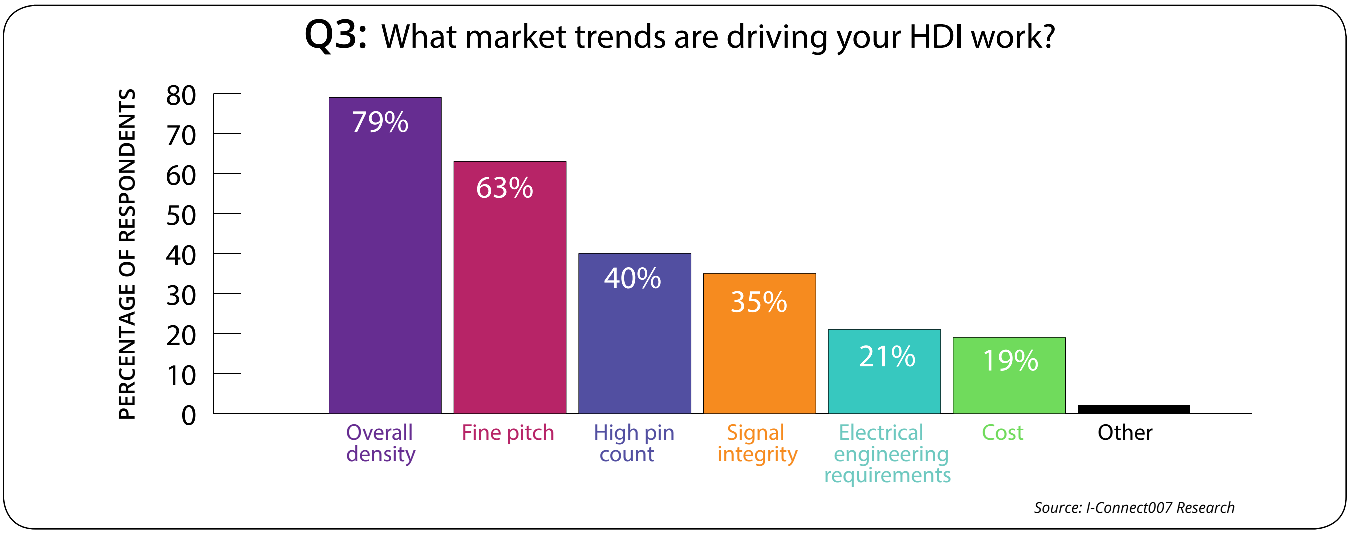
Now, think back 25 years and you realize that fine features on a PCB were certainly not the same as they are now, and neither were the chip packages being used. Drilling, imaging and other PCB processes have made significant advances as you can imagine. And today's densely-packed semiconductor packages are making HDI a necessity for many types of boards for many more applications—think electronics in cars, medical electronics and your incredible smartphone—all making use of components with many, many more I/Os and finer pitches (imagine what Moore's Law has done in 25 years!). How to fit all those connections into a finite area on a PCB? So, it's with all this in mind that we delve into this month's issue on HDI, which is not for the faint of heart or the light reader!

Of course, we can't talk about HDI without first hearing from the acknowledged "Father of HDI," Happy Holden. And Happy has put together our intro article on the subject. He provides the proverbial wakeup we need to move all the faster into it. He points out concerns and obstacles and what needs to be done to overcome them.

Continuing in this theme, Mike Carano, RBP Chemical Technology, discusses in his col-







umn the practical competencies needed by a PCB fabricator to be a successful manufacturer of HDI boards.

Consultant Vern Solberg continues with a more design-focused view—or perhaps explanation—of the rather recent surge in HDI. He not only thoroughly explains the need for HDI based on the increased package density, but also discusses both imaging and via formation. This is a heavy-duty column for the PCB manufacturer, but definitely something you should read.

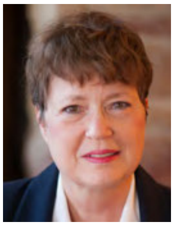
As usual, we pulled together some experts who could intelligently explain some of this to us, as well as our readers. Our group consisted of Finisar's Steve Bird, APCT's Tony Torres, and several technologists from MC Assembly: Steve Jervey, Mike Smyth and Paul Petty. We learned a great deal about the latest technology, manufacturing challenges and strategies for design, fabrication and assembly—and you will too.

OK, let's take a break and talk about something else. Elmatica's Andreas Lydersen makes the case for a common PCB language called CircuitData. This open source standard was conceived to help prevent insufficient and erroneous article specifications that occur far too often between designer and manufacturer, often due to the many ways to describe even simple items like solder mask. This project sounds like a very good idea and one you should consider participating in.

Next, Tara Dunn, Omni PCB, writes about FlexFactor, a NextFlex program to help grow the next generation of advanced manufacturing workforce. She starts by listing several interesting electronics-based products that have been conceived by high school students and goes on to describe the four-week program and some of its encouraging results.

IPC's John Mitchell also writes along these lines, covering the nationally recognized Manufacturing Day, which occurs on the first Friday in October. This day gives manufacturing companies the opportunity to present their company to their communities by inviting businesspeople, students, teachers and other community members, into their companies. It serves as a perfect venue to inform on career options in manufacturing, including the electronics industry.

OK, everyone. This issue is definitely required reading, so get on it. You need this technology and you need to read about it here. Next month we've got a hot one for you: an issue devoted to thermal management. We want you to learn and thrive in our industry and we're doing our best to help you do that. If you haven't already put yourself on our waiting list, what are you waiting for? Subscribe now and get a leg up on your competition. Move! **PCB**



Patricia Goldman is managing editor of *The PCB Magazine*. To contact Goldman, click here.

35 Years of HDI Fabrication Processes and Obstacles for Implementation

by Happy Holden

I-CONNECT007

Introduction

The electronics industry is the world's largest and most robust market. It is also a bulwark of American creativity, with Silicon Valley as its origin and fortress. The SIA Roadmap is still pushing the size of wafer transistors smaller and smaller, with the resulting faster rise times and need for finer pitch. *But* silicon needs a mounting platform and the printed circuit and organic IC package will be needed to create working products.

For North America, there is a growing need for more HDI capability. Some of the reasons for the slower adoption of HDI fabrication in N.A. may rest with four obstacles: Defining density needs; EDA tools not providing increased functionality; process controls for fabricating reliable microvias; and bare-board/ICT solutions once HDI is assembled.

A wakeup call may be too strong a term, but it is time to seriously consider what you are going to do about HDI. The adage "offshore can't handle our technology" is out of date. Offshore (or Asia) can now do 24-layer multilayers, laser-drilled HDIs, fine lines (2-mil traces and spaces), flip chip packages, pure gold, hard gold, low loss materials, RF, buried capacitance, mixed dielectrics, etc. The current production analysis of HDI technology released by TechSearch International in "High-Density Microvia Substrates: Markets, Applications and Infrastructure–Updated" shows that Asia had 86% of the HDI business in 2016–2017[1]. As you can see in Figure 1, North America is a mere 5% of the total. TechSearch predicts that HDI will grow to $18.6 billion by 2020.

Now you might ask, why is this so? The two main uses for HDI are for portable products like

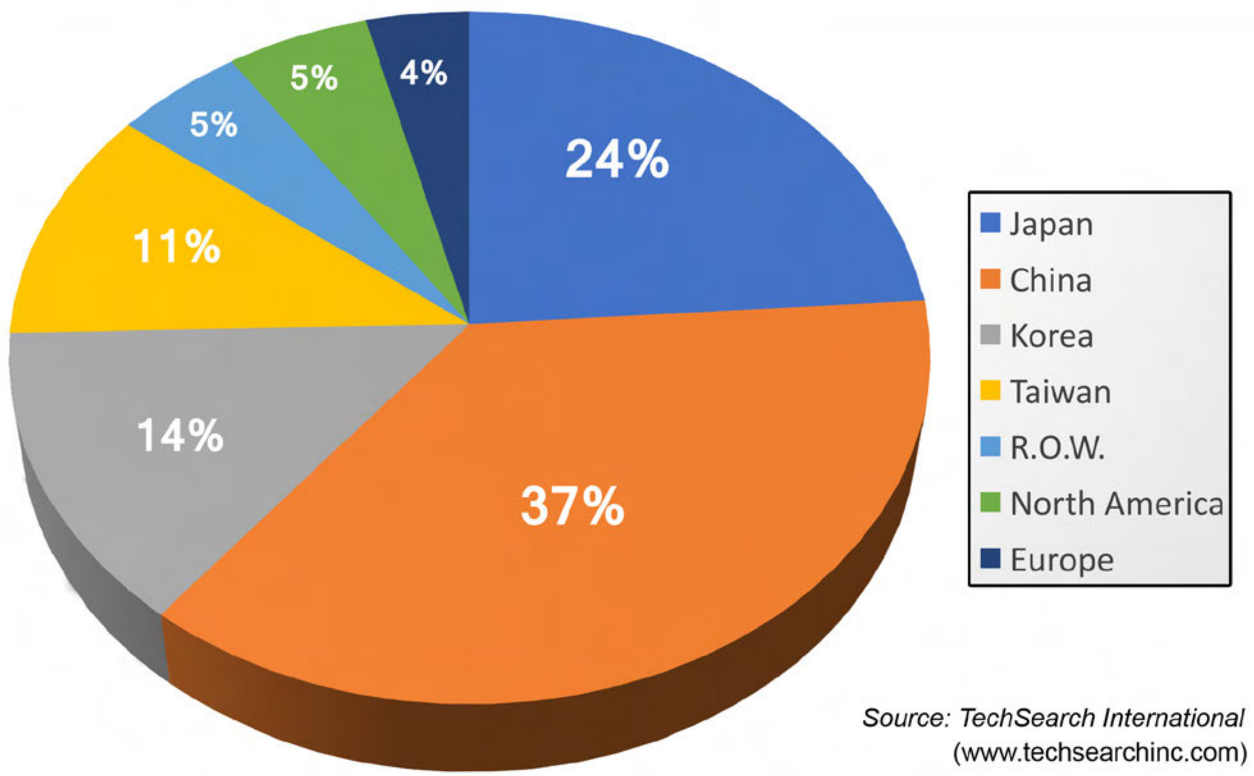


Figure 1: HDI production worldwide for 2016–2017.

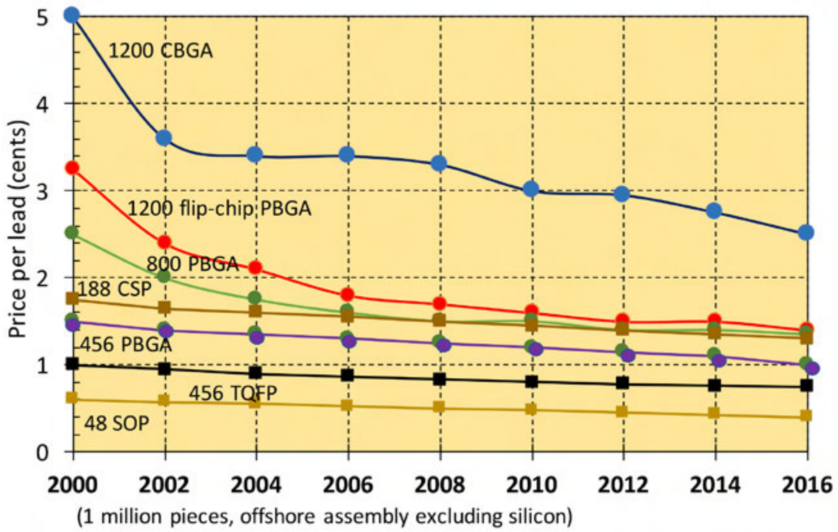


Figure 2: Assembled array packaging prices from Prismark survey[2].

cellular phones and camcorders and for fine-pitch IC packages. It just happens that Japan, Korea and Taiwan make a lot of these products and we don't. In fact, at the Electronics Circuits World Conference 14, companies like Samsung have been working on new lower-cost laser HDI technologies using thermoset resins. This eliminates the need for lamination presses and lowers the material costs in the production of microvias.

Lately, my time has been monopolized by OEMs asking about the most cost-effective way to use the new 0.5 mm BGAs. Many of these are digital signal processors (DSP) and custom ASICs in the 457 to 1384 I/Os range. These are being produced in the millions now and are going into all sorts of sophisticated servers, networking and telecom products. These industrial products will now form the *third platform* for HDI. These products also make up a majority of the high value-added electronics produced in North America.

The reason for the increase in fine-pitch BGA activity can be seen in Figure 2. In 2016, BGAs are approaching the costs of quad flat packages and complex (high pin count) packages now cost less than one cent per pin. With package prices like that, all OEMs are considering how to use them in their new products.

I'm not going to talk about making microvias; that's the easy part (but expensive). There are now laser drilling job shops that you can subcontract to. No, the real issues are metallization, registration and plating. When dealing with small blind vias, getting a reliable, completed blind connection takes more than just wetting a small hole.

The one issue they don't talk a lot about is the assistance OEMs need when first dealing with microvias. Their first questions are, "How small can you make this with microvias?" and "How much will it cost?" The questions are obvious, but the answers aren't. For the first time, we know more about building the HDI product than we do about designing it or pricing it. Yet, this is where the OEMs are going to start asking their questions. Be prepared! One way to help the OEM is to provide him with the new *HDI Handbook* (Volume II) scheduled for publication in December 2017 by I-Connect007[3]. It will also be available at IPC APEX EXPO in San Diego. This free and downloadable eBook will have nearly 19 chapters to give any OEM or fabricator a thorough understanding of HDI, including how HDI can make assemblies smaller and/or thinner. These issues will be important as you decide your future; with or without HDI.

Defining Density Needs

I would like to introduce all of you to some of the measures of performance or *metrics* for the HDI Value Delivery Chain (VDC). Figure 3 is what I call a Packaging Technology Map. The Packaging Technology Map was first displayed by Toshiba in January of 1991 in the paper "New Polymeric Multilayer and Packaging" at the Printed Circuit World Conference V in Glasgow, Scotland[4]. So, I didn't invent this chart, but I have been unsuccessful since 1991 in finding the person or persons who did. No one in Japan seems to know about this chart!

In the chart, I saw for the first time the interrelationship between component packaging, SMT assembly and printed wiring boards. Like the triangle in the figure, these three vital chains of the HDI VDC are linked. This makes the chart an ideal technique to analyze packaging, as it captures the three elements of interconnection:

- Assembly complexity: A measure of the difficulty to assemble surface mounted components; measures in parts per square inch and leads per square inch
- Component packaging: The degree of sophistication of a component, measured by its average leads (I/Os) per part
- Printed wiring board density: The amount of density (or complexity) of a printed circuit as measured by the average length of traces per square inch of that board, including all signal layers; the metric is inches per square inch

When the chart is used to analyze surface mount assemblies, three major zones show up on the packaging chart, which is why I call it a map. The first is products with a high content of discreet components. Typical products are camcorders, pagers and cellular telephones. They have the highest assembly complexity, up to 300–400 leads per square inch (47 leads per square centimeter). The second group is products with a high degree of digital components and some mixed discretes. Notebook computers, desk tops, instruments, medical equipment and telecom routers are examples. The last group has a highly integrated use of ICs. PCMCIA, flash memory, MCMs and other modules are typical of this group. This group has the highest PWB wiring density of over 160 inches per square inch (25 centimeters per square centimeter). Figure 3 loosely shows the three regions.

By charting products of a type over time, an analysis will show how the packaging technology is changing, its rate of change and the direction of those changes. This is the exercise in road-mapping. But now, the exercise will have some data behind it.

A second valuable feature of the map is the area I call the "Region of Advanced Technologies." This is where calculations and data have shown that it is necessary to have an HDI structure. So, this is the barrier or wall of HDI. Cross this and it now becomes cost-effective to use HDI. Move too far and it becomes a necessity.

To create the packaging map, an assembly is measured for its size, number of components and the leads those components have. The area is the laminate, not the surface area. The components include both sides of an assembly as well as edge fingers or contacts. By the simple division of leads by parts and parts by area of the assembly, the X- and Y-axes are known. By plotting the components per square inch (or components per square centimeter) against av-

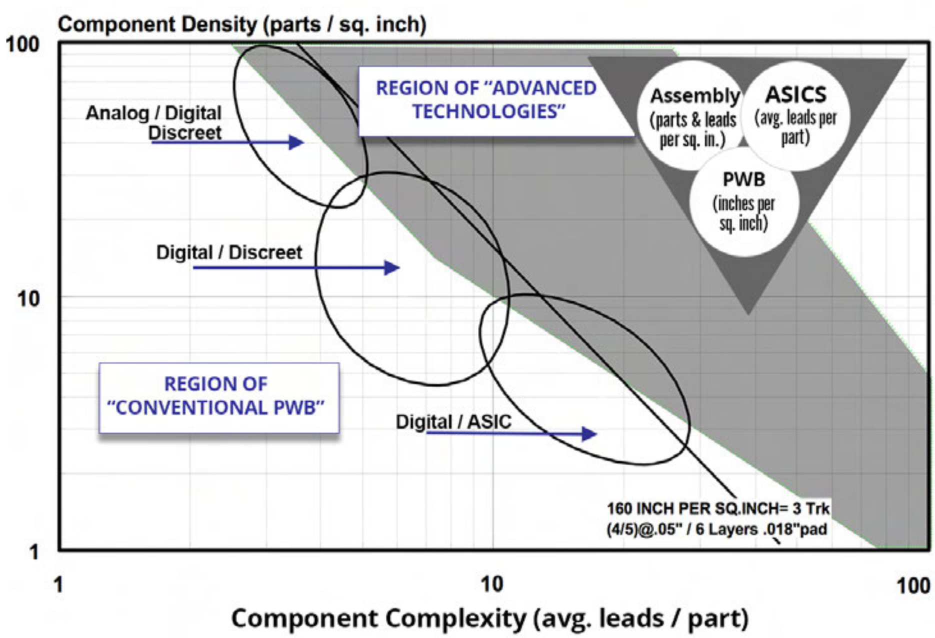


Figure 3: The Packaging Technology Map for printed circuits, created by Toshiba.

erage leads per component on a log-log graph, the PWB wiring density in inches per square inch (or centimeters per square centimeters) and assembly complexity (in leads per square inch or leads per square centimeter) can be calculated. The assembly density is just the X-axis times the Y-axis. The PWB density was derived by assuming an average of three electrical nodes per net and that the component lead was a node of a net. The result was an equation that says the PWB density is β times the square root of the parts per square inch times the average leads per part. β is 2.5 for the high analog/discreet region, 3.0 for the analog/digital region and 3.5 for the digital/ASIC region:

PWB Density = β √[parts per sq. in.] x (avg. leads per part)

In Figure 3, the assembly complexity lines cross the wiring density lines. At high discreet levels, less wiring is required for the amount of assembly density. At high ASIC (and low discreet) levels, much more wiring is required to connect the components. This makes assembly metrics like leads per square inch a good indicator, but not adequate to substitute for the PWB wiring density.

Metrics are an important part of solutions creation. If we can't measure something, it's very difficult to improve it.

EDA Tools Need Additional Functionality

Current design tools do not provide the analysis and advice on the challenges of fine pitch and increasing density. This forms a real obstacle for implementation of high density interconnects. One reason may be the absence of density metrics. Performance measures are needed for: the difficulty to assemble surface mounted components with fine-pitch; the amount of density required on the printed circuit to mount all these fine-pitch devices in the area provided; and the degree of sophistication of new components with faster rise-times.

Maybe the problem is that I am approaching my 50th year in printed circuits. It's been fun and I look forward to what each day may bring. For the last 35 years I have been involved in the PCB design process. I have used CAD systems to design boards, provided advice for designers on their boards and worked on CAD tool development. Currently, I am involved in the development of prediction tools to allow the accurate estimation of design rules, board structures and costs from schematic and part information before the board is physically designed. This, along with new design metrics, allows for the optimization of the board.

This optimization follows a major theme for many electronics companies—that of Total Quality Management (TQM). TQM can be applied to the PCB design process by acknowledging that the next step in the process after design is PCB fabrication and assembly. These, then, are the customers of the design process. And a major measure of performance by those customers is *quality.* Quality of design is interpreted by manufacturing as producibility. Unfortunately, for CAD tools, producibility is not one of their features! When I once asked a CAD company executive about his definition of "quality of design," he talked of the number of software bugs per 1,000 lines of code. He refuted the idea that CAD tools had any responsibility for the TQM process.

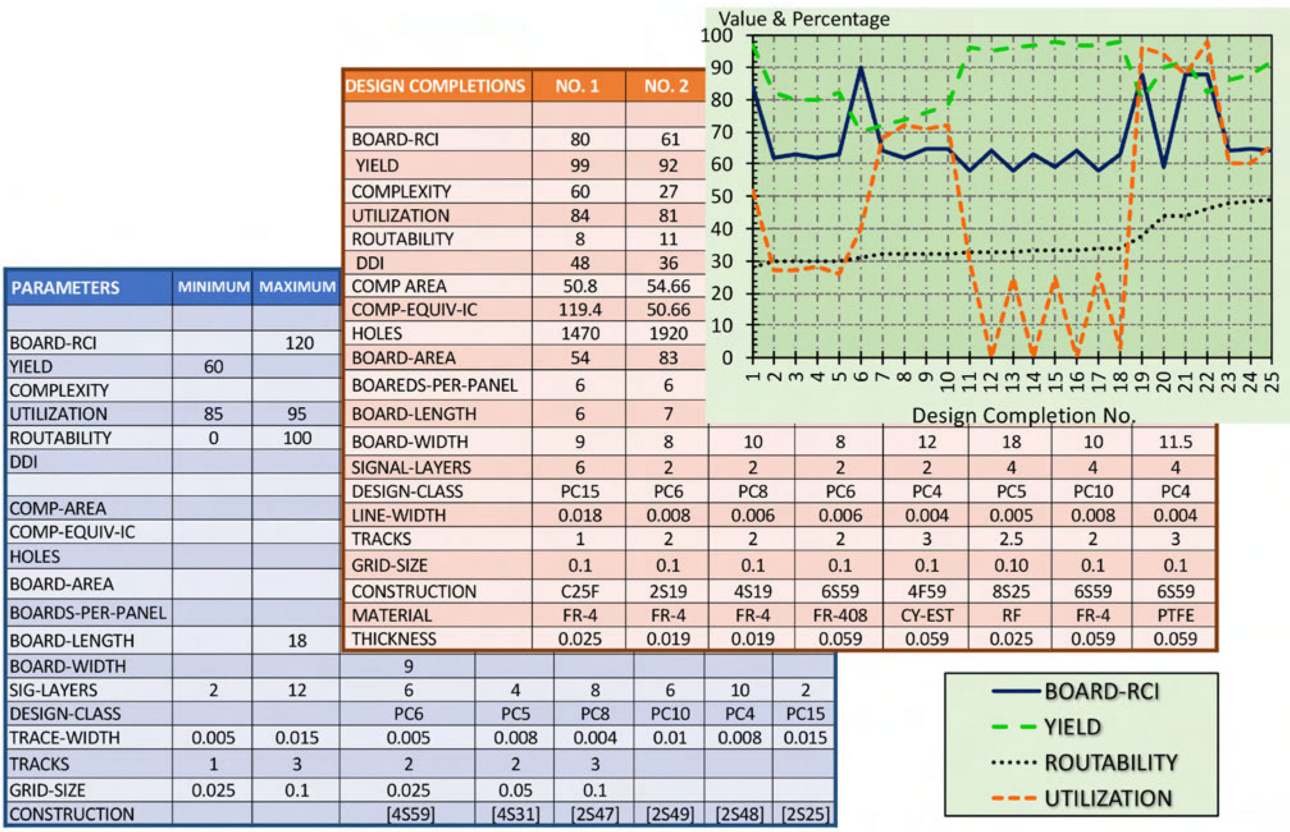
In the last 35 years, my opinion of the PCB design process is, *never has so much been done by so few, to build so many electronics products, to such little recognition!* It's like looking at a chasm between two thriving plateaus. On one side are the areas of engineering excellence, concurrent engineering, CAE and state-of-the-art components. On the other side of the gulf is progressive manufacturing (PCB fabrication, assembly and test). Bridging them takes a leap of faith by PCB design. Falling short means plummeting into the abyss.

We need to build sturdy, reliable, predictable "bridges" over the chasm. But I don't see anyone doing it. Having faster, cheaper CAD tools with more features is a necessary piece of the bridge, but in itself will not create those bridges. In fact, if they continue to increase in complexity, they may become a part of the problem. The last papers I read on predicting wiring were written in 1990. I have not come across any more current work. I have read papers on the CAD tools, on their autorouters and on the software architecture, but nothing on the process and planning of PCB design.

In 1995, I was involved with helping Hewlett-Packard's Laboratory in Palo Alto develop exploratory software for PCB design and DFM. Their first creation was a software tool called the Board Construction Advisor (BCA) (Figure 4). From a paper the creators wrote for an internal HP design technology conference in 1990, they described the tool as "... to help specify the detailed physical design after schematic capture and component selection have been completed ...to answer questions about the cost and [mfg.] yield implications of design alternatives, the electrical characteristics of materials and geometry choices, and the availability of features at manufacturing sites." The software worked perfectly; I loved the ease at which designs could be optimized. But one problem came to the surface. It could quickly give answers and create graphs and figures about a proposed PC board, but what if you did not know the questions? Tested on most engineers and novice PC designers, they kept asking, "What questions do I ask it now?" So the lab went back to work and created Explorer.

Explorer was a totally new approach to optimizing a PCB design. It was a self-learning, artificial intelligence that had an expert system as its engine. The inputs were specifications of design tasks directly in terms of constraints and goals, the schematic and parts library. The software would automatically search for and generate realizable physical designs and judge them against the constraints and goals. It would then use its interactive multi-criteria, multi-objective optimization and trade-off algorithms to create a different and hopefully better design.

After nearly 250,000 different designs it would signal that it had finished and would display the top 25 designs against the goals and constraints given it. The results were stunning. You had only to decide about what was important for the trade-offs. How important is it to have the lowest board manufacturing and assembly costs versus all the signal integrity goals



DESIGN COMPLETIONS	NO. 1	NO. 2						
BOARD-RCI	80	61						
YIELD	99	92						
COMPLEXITY	60	27						
UTILIZATION	84	81						
ROUTABILITY	8	11						
DDI	48	36						
COMP AREA	50.8	54.66						
COMP-EQUIV-IC	119.4	50.66						
HOLES	1470	1920						
BOARD-AREA	54	83						
BOAREDS-PER-PANEL	6	6						
BOARD-LENGTH	6	7						
BOARD-WIDTH	9	8	10	8	12	18	10	11.5
SIGNAL-LAYERS	6	2	2	2	2	4	4	4
DESIGN-CLASS	PC15	PC6	PC8	PC6	PC4	PC5	PC10	PC4
LINE-WIDTH	0.018	0.008	0.006	0.006	0.004	0.005	0.008	0.004
TRACKS	1	2	2	2	3	2.5	2	3
GRID-SIZE	0.1	0.1	0.1	0.1	0.1	0.10	0.1	0.1
CONSTRUCTION	C25F	2S19	4S19	6S59	4F59	8S25	6S59	6S59
MATERIAL	FR-4	FR-4	FR-4	FR-408	CY-EST	RF	FR-4	PTFE
THICKNESS	0.025	0.019	0.019	0.059	0.059	0.025	0.059	0.059

PARAMETERS	MINIMUM	MAXIMUM						
BOARD-RCI		120						
YIELD	60							
COMPLEXITY								
UTILIZATION	85	95						
ROUTABILITY	0	100						
DDI								
COMP-AREA								
COMP-EQUIV-IC								
HOLES								
BOARD-AREA								
BOARDS-PER-PANEL								
BOARD-LENGTH		18						
BOARD-WIDTH			9					
SIG-LAYERS	2	12	6	4	8	6	10	2
DESIGN-CLASS			PC6	PC5	PC8	PC10	PC4	PC15
TRACE-WIDTH	0.005	0.015	0.005	0.008	0.004	0.01	0.008	0.015
TRACKS	1	3	2	2	3			
GRID-SIZE	0.025	0.1	0.025	0.05	0.1			
CONSTRUCTION			[4S59]	[4S31]	[2S47]	[2S49]	[2S48]	[2S25]

Figure 4: Results of multiple design runs with HP Lab's BCA + Explorer.

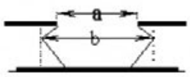
Item	Spec	Measurement	Sample Size	Control Limit
1. Overhead 	Class A: a/b ≥ 0.95 Class B: a/b ≥ 0.90, a/b<0.95 Class C: a/b<0.90	Cross section inspected by microscope	1. First piece of Per Part 2. One of per 10 lots.	a/b = 0 a/b ≤ 0.9
2. Roughness 	Class A: R < 0.1 mil Class B: R ≥ 0.1, P ≤ 0.5 mil Class C: R > 0.5 mil	Cross section inspected by microscope	1. First piece of Per Part 2. One of per 10 lots.	R = 0 R ≤ 0.5 mil
3. Taper angle 	Class A: 5° Class B: 10° Class C: 15°	1. Cross section inspected by microscope 2. Z-check	1. First piece of Per Part 2. One of per 10 lots.	θ = 0° θ ≤ 20°
4. Voids 	Class A: No Voids Class B: Voids	Cross section inspected by microscope	1. First piece of Per Part 2. One of per 10 lots.	No Voids
5. Wicking 	Class A: L ≥ 0, L ≤ 0.1 mil Class B: L > 0.1, L ≤ 0.5 mil Class C: L > 0.5 mil	Cross section inspected by microscope	1. First piece of Per Part 2. One of per 10 lots.	L = 0 L ≤ 0.5 mil
6. Resin remains 	Class A: t ≥ 0, t ≤ 0.2 mil Class B: > 0.2, t≤ 0.5 mil Class C: t > 0.5 mil	Cross section inspected by microscope	1. First piece of Per Part 2. One of per 10 lots.	t = 0 t ≤ 0.5 mil
7. Cracks 	Class A: No Cracks Class B: Cracks	Cross section inspected by microscope	1. First piece of Per Part 2. One of per 10 lots.	No Cracks

Figure 5: Laser hole drilling quality and check sheet.

versus the smallest size versus the ease of manufacture? With the numbers in front of you, you only had to activate that design and the job was finished. Many calibration runs (55 boards) were then done on already existing HP PC boards. In all cases, the computer needed only a few hours (this was a 1995 computer) to complete its design optimization. In all cases, it had designed superior PC boards. Not only that, but signal integrity was better and the manufacturing costs of the boards and assembly were 15% to 60% lower.

HP Labs had finished its work—it had proved the feasibility of an automatic PCB design system. Now the tragedy sets in; no HP Division wanted to make it into a supported product, as HP had sold its EDA tools to Zuken. Manufacturing did not have software resources to rewrite the LISP code into C++ and, when demonstrated to two of the large CAD companies, they were not interested in marketing a software system that would eliminate the need for thousands of CAD seats and the support revenues that they generated. After all, who wants a car that could run on tap water! So, the software collects dust on the shelves of HP Labs. The only trace of its existence, the design, are the six PhDs that created it published a paper on the expert system in the *Cambridge Journal of Artificial Intelligence*[5]. The irony: When I read the article, no mention was made of the fact that its job was to design PC boards! The tragedy: For 22 years I have seen the “bridge” but it is still unattainable.

Process Controls for Fabricating Reliable Microvias

The small blind vias we call microvias present a unique challenge to printed circuit fabricators. Unlike through-holes, the small microvias can be extremely difficult to drill, desmear, metallize and plate. Laser drilling can be quite challenging and is much more difficult that mechanical through-hole drilling. There are seven fundamental quality issues, as seen in Figure 5. Unfortunately, all can only be known by micro-sectioning. Thus, panel coupons dedicated to the fabrication of perfect microvias become a necessity.

Bare Substrate Testing

The testing of HDI PCB prototypes can be accomplished with flying probe electrical testers, but volume production is still relegated to bed of nails type custom fixturing. Multiple-head flying probe testers do have more throughput, but even those models with twelve heads have only limited production capacity. It is the bed of nails fixture that will have to handle the production load. Unfortunately, the very high-density nature of HDI boards make custom fixtures very expensive. Gridded fixtures work with modifications, but their 0.1-inch by 0.1-inch pin grid can handle only an average of 100 test points per square inch. HDI boards are usually in the 75–200 average test points per inch with area array land pattern pitches down to 16 mils (0.4 mm).

Non-contact and limited contact testing is the new area of product development. Capacitance of nets to detect opens and shorts has been used for at least 15 years. I saw my first at Bull in France in 1982. They were using HP plotters outfitted with probes attached to HP high speed capacitance meters. By memorizing the capacitance of a known good board, the computer measured production boards very rapidly, looking for higher or lower capacitance, indicating open nets or shorted nets. Non-contact electrical testing machines have been developed and used in Japan for the last couple of years. Foremost of the Japanese is Nidec-Read Corporation. Their automatic test systems for BGAs, PLGAs, PGAs, MCMs and HDI boards have belt conveyor handling, index tables and step & repeat test heads. Their newest is the TRL electrical tester. TRL stands for Transient Link technology, a signal stimulus injected by spring probe or non-contact transducer that is detected by a non-contact capacitive sensor. It can test a small HDI substrate with 0.06mm pitch in ~4.5 seconds, 7.5 seconds if auto-alignment is required.

Panel Coupons

Special artwork designed into the panel edges or in unused space on the panel is essential. For additional traceability, if the artwork shared common features on the assembly sub-panel, then there is continuity to whomever does the SMT assembly. Figure 6 shows a small coupon I designed that can be used on fabrication panels as well as assembly sub-panel carriers. The coupons are detachable and can be tested by production personnel during the fabrication process. These coupons test for (and test method):

- Desmear-metallization-plating quality (10 immersions of 10 seconds each in 288°C solder pot-inspection)
- Layer-to-Layer registration and movement directions (continuity and cross-section)
- Daisy chain electrical reliability (four immersions @ 288°C of 10 seconds each followed by 4-wire Kelvin measure)
- First drilled hole of multiple diam.-last drilled hole of multiple diameter (inspection if present)
- Layer-order windows (inspection if present)
- CAF reliability (CAF test chamber)

4-Wire Kelvin Testing

Electrical test companies need to do further research into the micro-resistance of small blind vias. Using the concept of multiple flying-head probes, they should be able to perfect either DC or AC 4-wire Kelvin measurements that tell us if there are any imperfections in the fabrication of small laser drilled vias. The CAD files make trace widths, thicknesses, vias and net lengths available, to calculate these elements' contribution to a Kelvin resistance measurement. These calculations can be subtracted from the readings to measure the resistance of individual microvias.

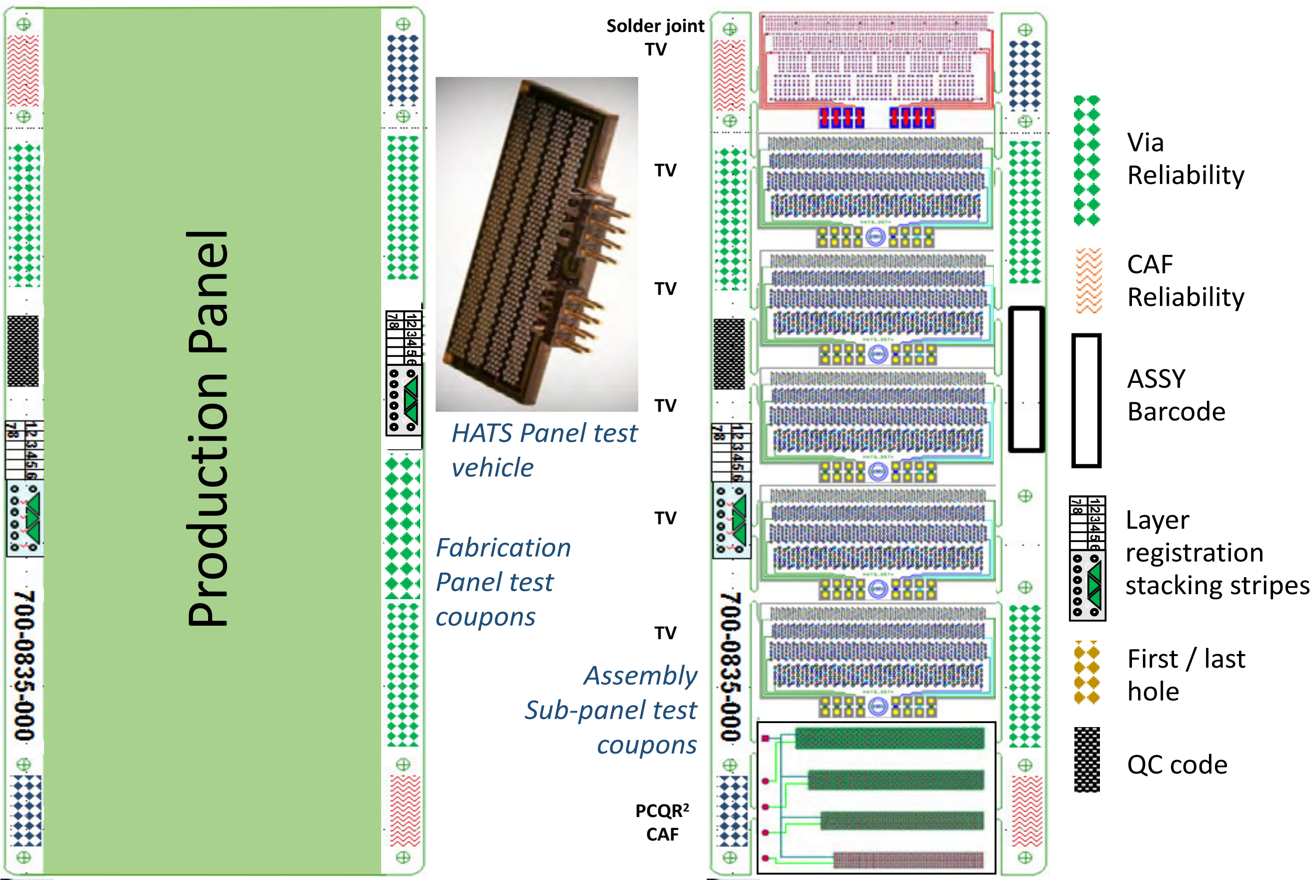


Figure 6: Small process test coupons used on fabrication panels and assembly sub-panels providing traceability and reliability continuity.

Such devices from two to twenty heads should offer fabricators the assurance of proper and reliable microvias.

AOI for Tiny Blind Vias

It seems possible, in today's age of solid-state laser diodes and sensitive multi-wavelength imaging chips, that an AOI machine can be created that can scan newly created microvias for many of the defects shown in Figure 5. We have LED bar printers with the same resolution (300 dpi) as laser printers. The wavelengths can be adjusted to allow the detection of resins or epoxies remaining on the copper at the bottom of these tiny vias. Our sensor and camera technology is superb, along with tremendous computing capability, such that creating a piece of equipment for the inspection of microvias a reality.

Bare-Board/ICT Solutions for HDI

Once these challenges have been overcome, how will we test the resulting assembly? Not everyone has the time or space to implement boundary scan or "built-in-self-test." Other cost-effective solutions need to be found to make sure we have a functioning product.

In 2011, I completed a tour of European and Chinese PWB shops. The amount of HDI substrates in prototype and on a production ramp was heartening. I also had an opportunity to talk with several large semiconductor packaging firms about their use of HDI organic packages. The semiconductor companies are planning to fill the demand for finer pitch BGAs and chip scale packages, all of which require HDI substrates. This is good news for all those fabricators who have invested in HDI production processes. Only one problem (well, one of many, but the biggest) still presents an issue and that is *electrical testing*. Contacting fine pitch devices is still a problem for the bare substrates as well as the populated assembly.

HDI Assemblies

If you think high-density bare substrate testing is difficult, it is nothing compared to testing the populated substrate. Two of the HDI driving forces are area array packages and via-in-pad. When used on a HDI assembly, just these two eliminate the normal via breakout pattern that assembly level testing uses for probing. Assembly level testing for HDI assemblies must be considered and a solution provided while the product is being created and designed. This is now called design for test (DFT) and many CAE/CAD software systems are beginning to provide this function. For large OEMs and companies that can design their own integrated circuits, limited access peripheral testing can be used like boundary scan or built-in-self-test (BIST). For the rest that create their product from standard ICs, other testing options will have to be considered.

Sub-Panel Testing

One of two innovative ways to test HDI assemblies is to put the test points external to the assembly, in the carrier sub-panel. This is best illustrated by the Figure 7. You will notice that, after assembly and assembly test, if the circuit is performing correctly, it is excised out of its carrier. This is also the technique used to electroplate pure gold on the bonding pads of BGAs. The excising can be break-away, punched or routed.

Embedded Test Structure

On one HDI design project I was involved in, the final assembly was a 4-layer IPC Type II Structure (1+2+1). It was a high-volume module for portable computers and could be tested after assembly with just limited access to peripheral I/O connections. Since it employed fine-pitch BGAs and via-in-pad wiring, the various data busses and data streams could not be accessed from the surface. In this case, we designed two additional, redundant build-up layers over the existing four layers to provide data access and troubleshooting. The resulting 6-layer HDI substrate (2+2+2) was only used for prototyping and initial production ramp. Once assembly and test diagnostics stabilized, the two outer, redundant test HDI layers were removed and only the 4-layer HDI structure was continued. Today, if you were to reverse engineer this module, it would be impossible to figure out how it had been developed. Figure 8 shows a cross-section of the six-layer HDI structure with the two test layers applied.

Electrical testing will try our patience. But when it is all over and we will finally have our cost-effective solution, I'm sure that it will also provide us with a new testing technology, including design for test and overall lower test costs in general.

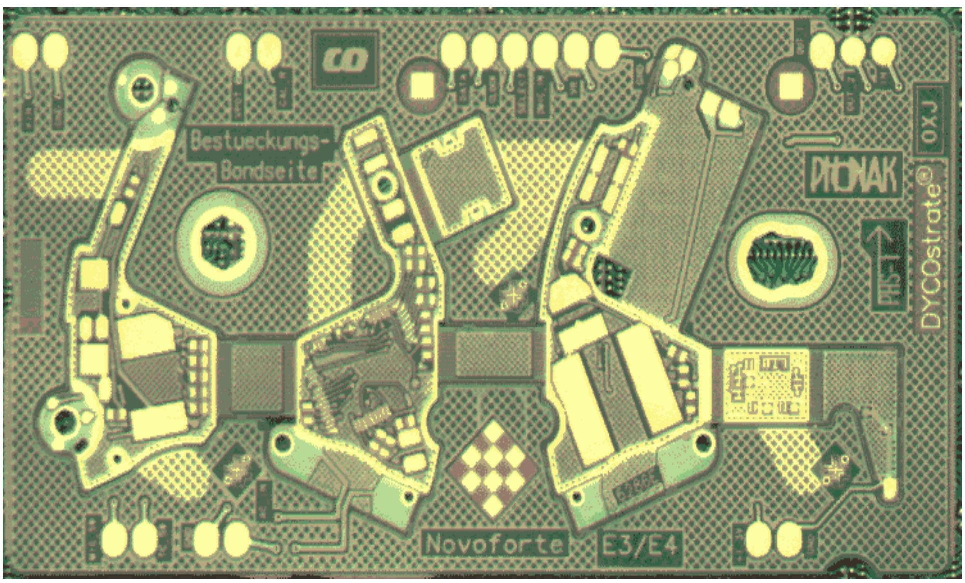


Figure 7: Test contacts designed to be external to the board. (Source: Dyconex)

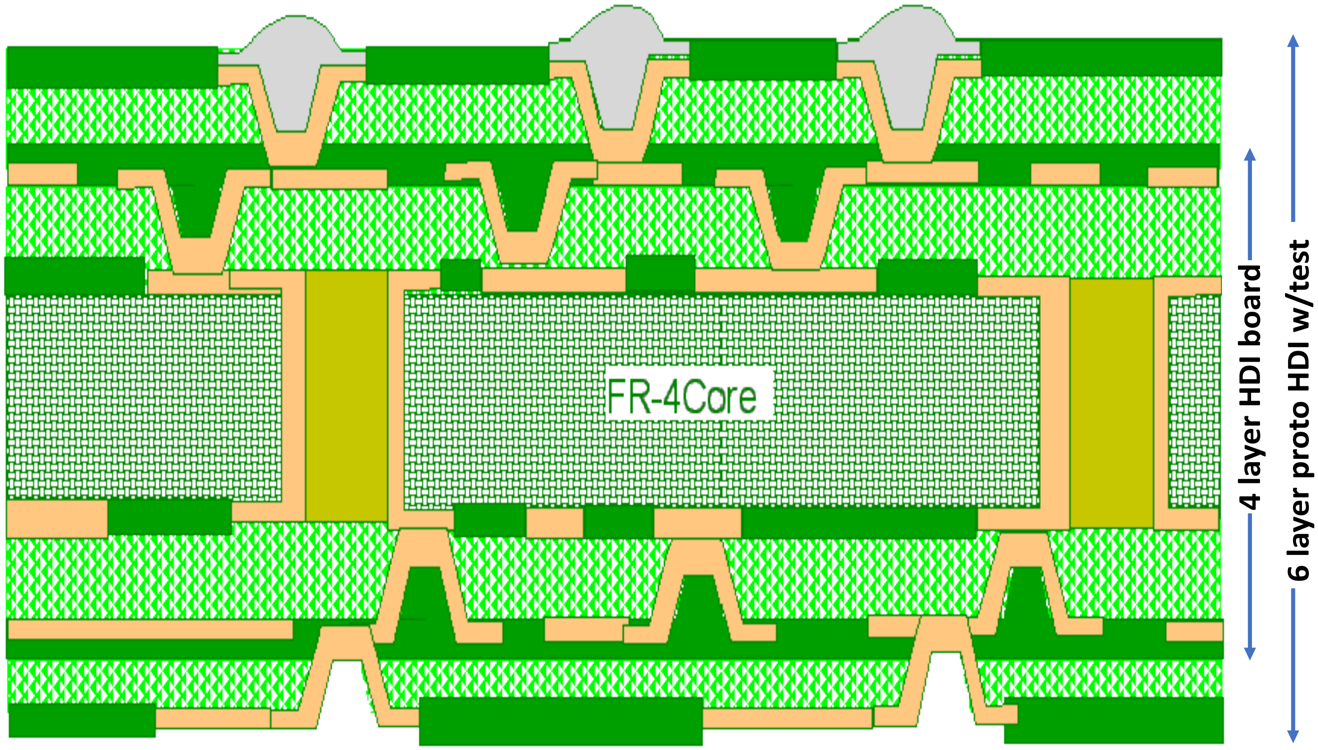


Figure 8: Assembly testing and prototype debugging provided by two extra HDI layers that are later removed.

Conclusion

HDI technology continues to grow and become integrated into new products. But obstacles are still present for the use of this technology in applications more complex than mobile phones and camcorders. Solutions need to be developed for the four remaining areas of manufacturing: defining density needs; EDA tools not providing increased functionality; process controls for fabricating reliable microvias; and bare-board/ICT solutions once the HDI is assembled.

The opportunities for innovation abound, with ample rewards for those looking to solve some of today's HDI manufacturing issues. **PCB**

References

1. Vardaman, Jan, TechSearch International, acquired via private communication. Report updates available by subscription.

2. Prismark Partners, The Semiconductor and Packaging Report, August 2017.

3. Holden, H., The HDI Handbook, I-Connect007, August 2008 (free download).

4. Toshiba Inc., "New Polymeric Multilayer and Packaging," Conference Proceedings, Printed Circuit World Conf. V, January 1991, Glasgow, Scotland.

5. Frayman, Felix; Kuokka, Daniel, "A Tool for Exploring the Solution Space of a Parameter Selection Problem," Journal of Artificial Intelligence for Engineering Design, Analysis and Manufacturing, Cambridge University Press, April 1995, pp 135-144.

Happy Holden has worked in printed circuit technology since 1970 with Hewlett-Packard, NanYa/Westwood, Merix, Foxconn and Gentex. He is currently a contributing editor with I-Connect007. To read past columns or to contact Holden, click here.

Supply Lines
Highlights

Institute of Circuit Technology Hayling Island Seminar 2017
This year's event had a well-chosen and varied programme featuring presentations on process chemistry and R&D consortia, a discussion of controversial standards proposals and a review of the experiences of commissioning new technology in a start-up factory.

New Highlights and Innovation to be Displayed at 2017 HKPCA & IPC Show
In addition to the return of the PCB industry's leading players, the 2017 International Printed Circuit & APEX South China Fair (2017 HKPCA & IPC Show) will feature many new elements: first-time exhibitors, innovative products and services and the entirely new Hong Kong Pavilion.

Ventec's Thermal Management Material Driving Today's Automotive Lighting Technology
Ventec International Group, a world leader in the production of insulated metal substrates, thermally conductive, polyimide & high reliability laminates and prepregs, will be exhibiting its latest thermally conductive material innovations at the Ford Advanced Lighting Innovation Expo (ALIE) on October 3-4, 2017 in Dearborn, Michigan.

Process Engineering & Defect Prevention
Defects may "manifest" or be detected in or after a specific operation within the printed circuit board manufacturing process, but the underlying root cause may have occurred earlier (perhaps much earlier) in the process.

CAC, Inc. Announces the Acquisition of ABC Assets from Oak Mitsui
CAC, Inc., manufacturer of CAC (copper-aluminum-copper), has announced the acquisition of the assets used to manufacture ABC (aluminum-bonded-copper) and sheeted copper foil.

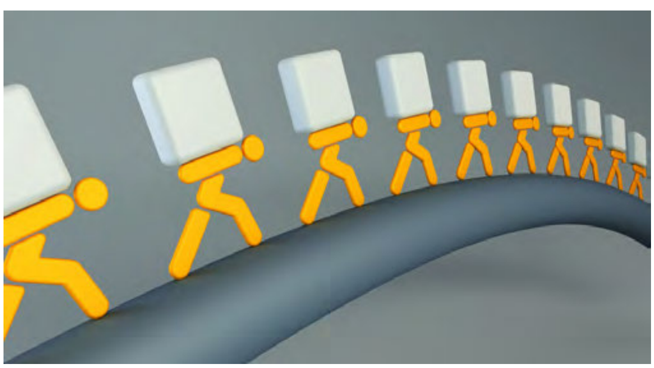
Strategies for Developing Copper Plating Systems
I-Connect007's Patty Goldman met with Dr. Albert Angstenberger, global technology manager for metallization with MacDermid Enthone Electronics Solutions, while at SMTA International. He presented an interesting paper on copper pillar plating systems that we hope to publish in The PCB Magazine sometime in the future.

Taiyo America Opens Office in the Dallas/Ft. Worth Area
Taiyo America Inc. officially opened a new office in the Dallas/Fort Worth area on October 1, 2017. This expansion is the first step in Taiyo's plans to expand technical support and new business development.

Camtek Finalizes Sale of PCB Business
Further to its announcement on July 19, 2017, Camtek Ltd has completed the sale of its PCB business to an affiliate of Principle Capital, a Shanghai-based private-equity fund.

Sun Chemical Enters into License Agreement to Introduce New Screen Printable Molecular Inks
Sun Chemical has entered into a license agreement to introduce a new family of molecular inks for the printed electronics market with Groupe Graham International (GGI) and the National Research Council of Canada (NRC).

CBT Announces Improved Print Speeds with New DI Solder Mask
Chime Ball Technology (CBT), Taiwan, announced today that they achieved print speeds between 30-32 second per side on an 18 x 24 panel size using their Phoenix and Raptor DI models and a new DI solder mask from Electra Polymer LTD, England.



Moving into Microvias: The Interaction of Materials and Processes, Part 2

by Michael Carano
RBP CHEMICAL TECHNOLOGY

Introduction

For the fabricator to successfully implement an HDI strategy, several new competencies must be acquired. These competencies include:

- Material selection
- Small diameter via formation
- Fine line imaging and etching
- Via filling technology
- Improved registration
- Enhanced bonding strength for the sub-laminations
- Metallization technology

These topics will be presented in more detail in this and future columns. But first, a short discussion on materials for HDI is warranted.

Materials

Most of the dielectric materials that are used to make printed circuit boards incorporate reinforcement into the resin system. Reinforcement usually takes the form of woven glass fiber. Woven fiberglass is just like any other cloth, made up of individual filaments that are woven together on a loom. By using different diameter filaments, different yarn bundle sizes and different weave patterns, different styles of glass cloth are created. Woven glass fabric adds both dimensional stability and thermal durability to the dielectric, but it does present some problems when used in HDI constructions.

Materials selection is equally as important, especially due to the higher temperatures of lead-free assembly and their subsequent effect on laminate delamination and reliability. Important new capabilities to embrace are[2]:

- Impedance calculations and stackups for high-frequency boards using coplanar waveguides and coplanar stripline models
- Characteristics and scaling/feature compensation for the newer phenolic-epoxy and halogen-free FR-4s
- Ability to add local fiducials to align laser drilling CCD cameras
- System to store laser drilling parameters based on diameter, depth, and material types
- Characteristics of via-plugging to determine if placement of buried vias will create problems

Via Formation

When lasers are used to create vias, the difference in ablation rates between the glass fiber and the surrounding resin can cause poor hole quality. Also, the fiberglass cloth is not uniform due to having areas with no glass, areas with one strand, and the intersections of strands (also known as knuckles), making it difficult to set up drilling parameters for all these varying materials. Usually the drilling is set up for the hardest to drill region which is the knuckle area. Figure 1 shows some examples of poor hole quality due to laser ablation of glass fiber-reinforced dielectrics. It seems many fabricators opt to not employ a glass etch in these types of conditions. A properly controlled glass etch will aid in removing the protruding glass fiber bundles and enhance overall plating uniformity.

When migrating HDI manufacturing over to laser-drillable prepregs, improvement in via quality is achievable. These laser-drillable prepregs are made using spread yarns in both the warp and fill directions. Thus the reinforcement is more uniform helping to minimize the areas with no glass fiber, as well as the knuckle area[1].

Mechanical drilling is a proven technology that covers a large range of via diameters with high aspect ratios (depth to width). It is most economical for through vias and blind vias larger than 200 µm (8 mils) in diameter. To bridge the gap to microvias, special techniques are used to achieve depth-controlled drilling of small via sizes. High-speed spindles are combined with

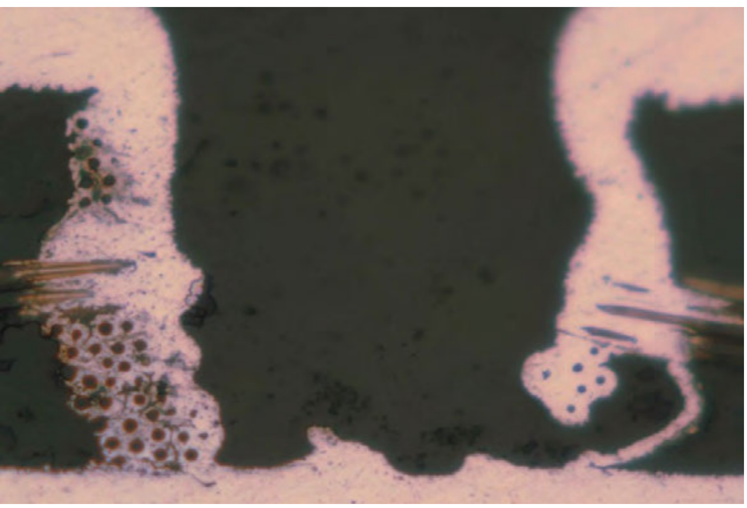


Figure 1: Via formation with glass fibers protruding.

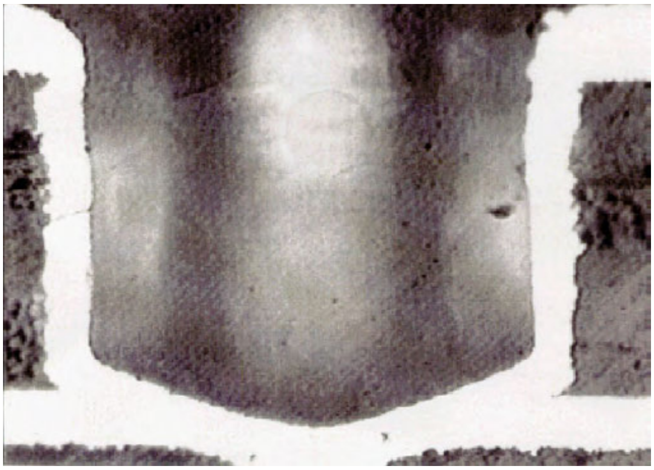


Figure 2: Mechanically formed via—note lack of taper.

different kinds of depth sensors. Thanks to a technique called electric field sensing (EFS), a very high-precision blind via can formed. EFS is based on a simple antenna theory where the pressure foot is flooded with a low power microwave field. The drill bit is used as an antenna to sense this field and monitor the output signal. The drop of the signal indicates the drill bit touching a metal surface such as a copper surface of the board. From this "ZERO" position, the Z-axis drills with an accuracy of I5 µm (0.2 mil) into the board without the use of mechanical parts which are prone to wear and tear or optical elements which are prone to debris[3].

With improvements in software and drill bit quality, it is possible to manufacture blind vias mechanically. Generally, one must recognize that there are limitations as to the depth and minimum via diameter that are attainable. Yet, the capital cost for a mechanical drilling tool maybe already be fully depreciated, making the move to HDI fairly easy from a capital equipment standpoint. This may allow for a cost competitive solution to via formation. The use of existing mechanical drilling equipment for microvias offers a great opportunity to start manufacturing microvias. Some of the depth control systems are even available as upgrades for existing machines. With very limited capital expense, the cost model for mechanical drilling is very simple and is reduced to the cost of operation. An example of mechanically formed blind vias are shown in Figure 2.


How important are your connections?
Plasma to improve reliability – no bad connections!
> Desmear
> Etchback
> Panel Cleaning
Plasma treatment in PCB Manufacturing:
• Removing resin smear
• Removing carbon byproducts from blind vias
• Efficient, economical and environmentally benign
Contact us now to learn more.
+1-800-326-1151
+1-925-827-1240
info@nordsonmarch.com
nordsonmarch.com
Nordson MARCH
VIA™ Series
Plasma System
productronica 2017
Hall A2 Stand 345
Nordson
MARCH

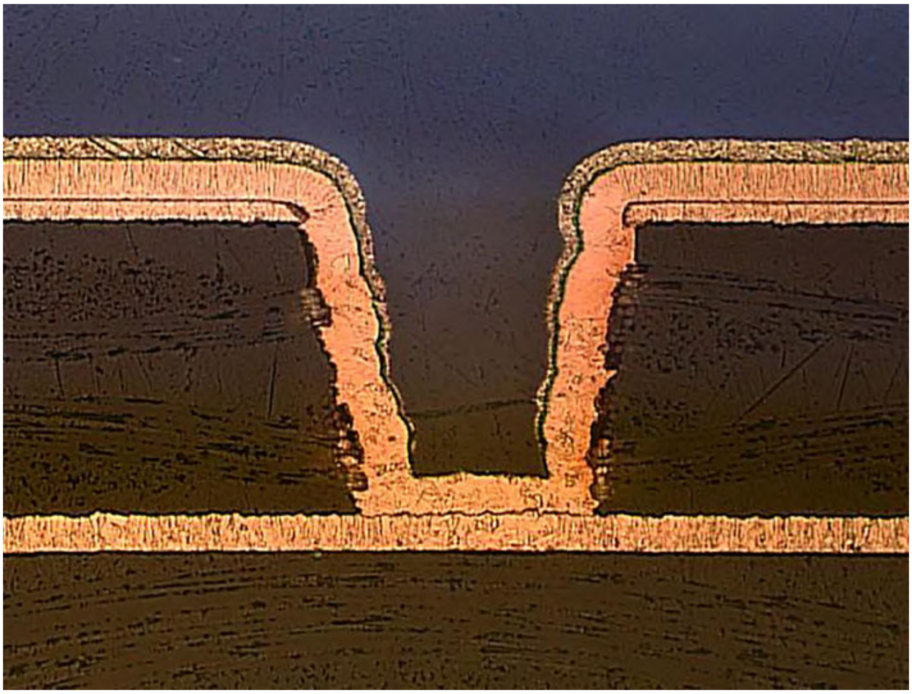


Figure 3: Blind via formed by UV-YAG laser drill with optimal parameters.

A concern with via shape as shown in Figure 2 is fluid dynamics as related to the various plating processes. One of the reasons that laser via formation may be preferred over mechanical drilling is the via shape. Laser via formation provides a shape that is shaped more like a "V" with a wider opening at the top of the via. This aids in promoting more uniform plating along the via wall and capture pad (Figure 3).

The advantage of a smooth transition from traditional drilling to microvia formation on existing equipment is also significant. Transition costs, resulting from downtime while fine-tuning upstream and downstream processes (plating, innerlayer alignment, etc.), can be limited. Having the processes under control will make the adoption of other microvia formation technologies much more rapid.

So, why consider laser drilling at all and just use mechanical drilling for all microvia production? Although the capital cost may be very low for mechanical drilling, the operating cost may not be. The costs per via are mainly determined by the drill bit costs that are strongly dependent on the bit (i.e., via) diameter. Worn and broken drill bits increase the cost of operation significantly. The cost of drill bits is dependent on the price of tungsten and cobalt. During the last year or so, both metal prices have increased significantly. With advances in laser via formation equipment, one must consider its implementation as via diameters decrease for certain applications. Carefully weigh all costs including capital expense, mechanical drill costs, and via quality and productivity.

Summary

Moving into microvias and HDI technology is a critical step for any PCB fabricator. But the market exists and is growing and profitable. Contrary to popular belief, HDI is not just for smartphones. There is an entire market that even small fabricators can exploit and establish a profitable niche. **PCB**

References

1. Holden, Happy, "HDI Handbook," available for free download here.

2. Author discussion with Happy Holden.

3. Burgess, Larry. "Blind Microvia Technology by Laser," IPC APEX EXPO, 1999.

Michael Carano is VP of technology and business development for RBP Chemical Technology. To reach Carano, or read past columns, click here.

Strategies for High-Density PCBs

by Vern Solberg

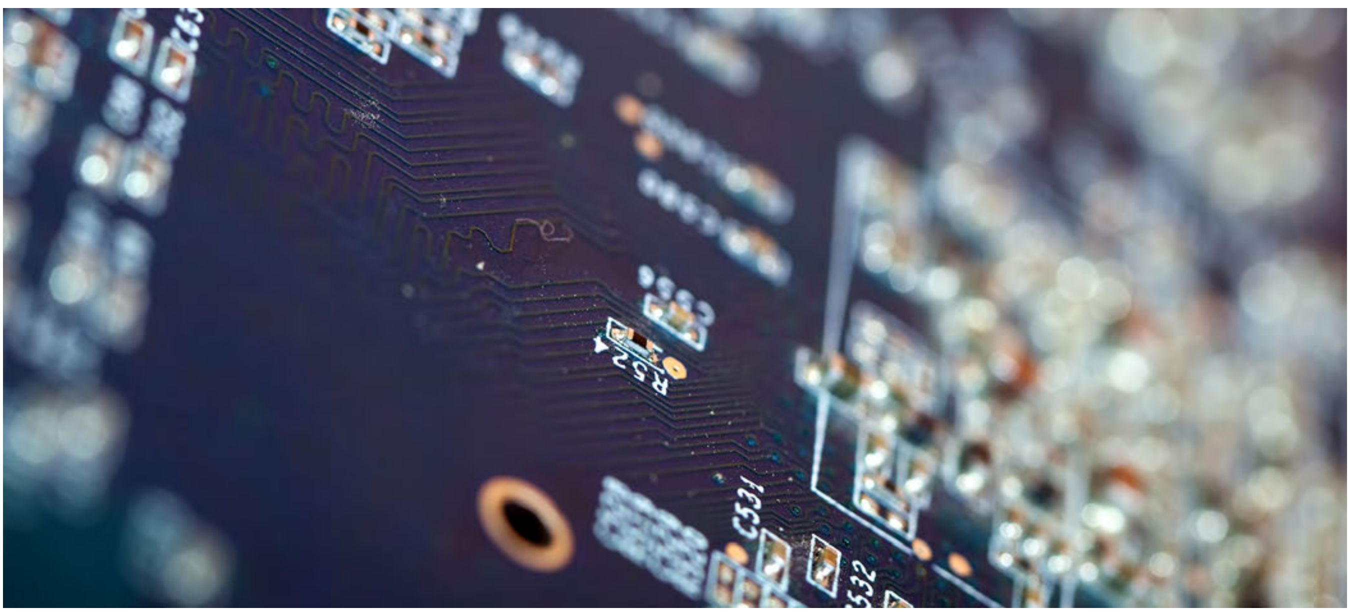
As hand-held and portable electronic products and their circuit boards continue to shrink in size, the designer is faced with solving the physical differences between traditional printed board fabrication and what's commonly referred to as high-density interconnect (HDI) processing. The primary driver for HDI is the increased complexity of the more advanced semiconductor package technology. These differences can be greater than one order of magnitude in interconnection density.

Semiconductor Packaging

Although the development of array-configured packaging for ICs has alleviated circuit routing difficulty somewhat, product miniaturization and performance goals are not easily achieved. To further complicate the PCB design process, many companies furnishing multiple die or multi-functional semiconductor packaging are forced to significantly increasing I/O while reducing both contact size and pitch. This higher I/O and finer pitch evolution is due in part to the OEM need for more capability in an ever-shrinking space. Further complicating traditional PCB design, some companies are doing away with some or all traditional semiconductor packaged semiconductors.

System-in-package (SiP) for example, whether die stack or package-on-package, has rapidly penetrated most major market segments. This includes consumer electronics, mobile, automotive, computing, networking, communications, and medical electronics. The benefits of SiP will differ for various market segments but they can share some very common elements: shorter time to market, smaller size and lower cost. Area efficiency (more functionality in a single package footprint) has resulted in the strongest initial penetration in consumer electronics. These mixed function SiP solutions have become commonplace in small form factor systems, such as mobile phones, memory cards, and other portable electronics products and the number has been increasing rapidly.

In contrast, it has become common for developers to procure bare, uncased die elements that are configured for facedown (flip-chip) mounting. Although flip-chip was originally considered for relatively low I/O die, the redistribution of the peripheral located contact sites to a more uniform area array format



has enabled the commercial use of larger and much higher I/O die elements. Regarding flip-chip mounting, interconnection from die element to the PCB is commonly achieved with alloy bumps, spheres or, for very fine pitch applications, raised copper pillar contacts that, although very small, are compatible with a conventional reflow soldering processes.

Achieving Higher Circuit Density

For many applications, the cost of high-density printed circuit boards has remained a detractor. Although PCB complexity has increased, however, the prices for HDI have declined and analysts expect this trend to continue to decline further each year. This is due in part to increased competition but the trend can be attributed to diligence in refining fabrication process methodology and controlling material utilization. Process refinement includes the development of more efficient imaging capability, improved etching and plating chemistry and refinement in base materials and lamination methods. Many user companies have already established a business relationship with these key suppliers and have qualified their level of expertise and capability. Regarding specifying narrow copper conductor width and spacing, the IPC-2226 has defined three HDI complexity levels for both external and internal locations (Table 1).

Some companies can produce copper conductors as narrow as 25 µm (1 mil) but they likely rely on using dielectric materials that have a very thin copper foil or utilize base materials prepared for a semi-additive copper plating process. But, before committing to adopting any level of HDI technology, the designer should confirm that the PCB suppliers selected are able to meet the required complexity level with acceptable process yields at the anticipated production quantity.

A key contributor to enabling higher density circuits is in the advances made in circuit pattern imaging. Circuit pattern imaging traditionally relied on first digitally imaging the circuit pattern onto polymer-based film masters then, using contact imaging to transfer the circuit pattern onto photo-resist emulsion applied to the copper-clad panel surface. Many fabricators have streamlined their processes by transferring the circuit image directly from the CAD file onto the panels resist coating using laser technology. Both laser direct imaging (LDI) and digital imaging (DI) systems have become mainstream technology for a wide segment of the PCB fabrication industry. Direct imaging eliminates extensive process steps required in preparing the film masters and avoids physical distortions attributed to varying thermal conditions and humidity on the polymer-based film masters.

Hole and Via Forming Methodologies

Mechanical Drilling

Drilling systems are manufactured by a broad number of companies worldwide and can range from a single spindle head system for low volume applications to multiple spindle head configurations to accommodate very high-volume fabrication requirements. Mechanical drilling is the most economical and efficient method for providing holes in circuit boards. The current generations of precision NC drilling systems are designed for accuracy and high throughput and many systems support post lamination profile routing capabilities.

Regarding specifying via hole size, mechanically drilled and plated vias can be furnished as small as 100 µm to 150 µm (4–6 mils) by some,

Conductor L/S	Level A	Level B	Level C
Internal conductor width	127µm (.005”)	75µm (.003”)	50µm (.002”)
Internal conductor spacing	127µm (.005”)	100µm (.004”)	50µm (.002”)
External conductor width	127µm (.005”)	75µm (.003”)	45µm (.0017”)
External conductor spacing	127µm (.005”)	100µm (.004”)	45µm (.0017”)

Table 1: Complexity levels for HDI technology as outlined in IPC-2226.

Laser Via Diameter	Target Land Diameter	Stop Land Diameter
50 µm (2 mils)	150 µm (6 mils)	150 µm (6 mils)
75 µm (3 mils)	180 µm (7 mils)	180 µm (7 mils)
100 µm (4 mils)	200 µm (8 mils)	200 µm (8 mils)
150 µm (6 mils)	330 µm (13 mils)	280 µm (11 mils)

Table 2: Via diameter to land diameter ratio variations.

however, the drill bit selected to furnish a finished hole size of 200 µm (8 mil) diameter will be more practical, less prone to breakage and, because they can be sharpened, facilitate a longer life.

Laser Ablation

When a circuit board design requires hole diameters smaller than 150 µm (6 mils), fabricators will generally adopt the CO_2 laser ablation process to form the vias, however, alternative laser technologies may be employed to initially ablate the copper foil. There are five common variations of laser-ablated and plated vias: through-via, blind via, buried via, stacked via and staggered via. Laser-ablated and plated through-via holes are used for general interconnect applications that connect conductors on the outer surfaces of the board as well as connecting to layers within the multiple layer circuit structure. In addition to through-via applications, laser-ablated and plated blind vias will furnish interconnect from either outer surfaces of the board to conductors on designated innerlayers. These vias may be placed in lands that are only slightly larger than the initial via diameter. Designers can also position the plated blind via within the component's land pattern geometry; however, these via holes must be specified as 'plated closed' and flush with the outer copper surface of the board. This is because any remaining depression within the land pattern's surface can result in void propagation with the solder interface, especially a concern for array-configured components.

The buried via may be mechanically drilled or laser-ablated on one or more inner or core layers of the multilayer board structure. These vias will be specified as plated and filled prior to the lamination of additional build-up layers. Multilayer boards can be designed using vertically stacked via processing. This process is used for more complex structures requiring circuit layers to be processed and laminated sequentially, ablating and plating vias in the copper foil and chemically etching the circuit features before laminating the next layer. A variation of the stacked via process is the staggered via where via lands are slightly offset from one layer to another.

A key issue is the aspect ratio of via diameter to the overall thickness of the copper and dielectric. Via diameter to land diameter ratio requirements may differ from one supplier to another but the following table may be referenced as a base for discussion (Table 2).

Regarding stacked vs. staggered via reliability, some experts acknowledge that, although the small layer-to-layer interconnecting vias will furnish a robust interconnect solution, stacked vias are said to be less robust than the staggered via alternative. As always, the designer is advised to establish dialog with the PCB fabricator early in the design stage of the program. They will be the designers' best source regarding guidance in material selection and fabrication process planning. **PCB**

Vern Solberg is a technical consultant specializing in surface mount technology and microelectronics. He has served the industry for more than 30 years in areas related to both commercial and aerospace electronic product development and holds several U.S. patents for 3D semiconductor packaging innovations. To read past columns or to contact Solberg, click here.

Electronics Industry News
Market Highlights

Smart Bandage Could Promote Better, Faster Healing
Researchers from the University of Nebraska-Lincoln, Harvard Medical School, and MIT have designed a smart bandage that could eventually heal chronic wounds or battlefield injuries with every fiber of its being.

Additive Manufacturing—a Revolution in Production Engineering
Additive manufacturing processes are the major topic for the future of production engineering. Applications range from producing machine parts of metal through to 3D printing of concrete.

Western EU IT Spending Highlights Interest in Next-Gen Technologies Across Vertical Markets
According to a new study from IDC, IT spend in Western Europe will total $453.8 billion in 2017, a 2.7% increase compared with 2016. IT spending will continue to grow at a 2.0% five-year CAGR in 2021.

Novel Circuit Design Boosts Wearable Thermoelectric Generators
Using flexible conducting polymers and novel circuitry patterns printed on paper, researchers have demonstrated proof-of-concept wearable thermoelectric generators that can harvest energy from body heat to power simple biosensors for measuring heart rate, respiration or other factors.

Industrial Control and Factory Automation Market Worth $240B by 2023
The market is expected to be valued at $239.11 billion by 2023 from $155.26 billion in 2017, at a CAGR of 7.4% between 2017 and 2023.

Electrodeposited Copper Foils Market Driven by Hybrid and Electric Vehicles
The global electrodeposited copper foils market is estimated to be valued at $6.6 million by the end of the year 2017 and is poised to touch a value of $16 million by the end of the year 2025, registering a CAGR of 11.6% during the assessment period.

Quantum Computers Demand New Encryption
Data that is confidential today will no longer be secure when quantum computers arrive. However, researchers have a solution ready in advance—quantum cryptography.

Automotive Telematics Systems Revenue to Reach $6.7 Billion Globally in 2023
Global revenue from automotive telematics systems will grow at a compound annual growth rate (CAGR) of nearly 17% to more than $6.7 billion by the end of 2023, according to new research from business information provider IHS Markit.

1.7 Million New Robots to Transform the World's Factories by 2020
By 2020 more than 1.7 million new industrial robots will be installed in factories around the world. Today, the strongest growth in the robotics industry is in Asia—lead by China as the world´s number one marketplace.

ALCF Supercomputers Help Address LHC's Growing Computing Needs
Particle collision experiments at CERN's Large Hadron Collider (LHC)—the world's largest particle accelerator—will generate around 50 petabytes (50 million gigabytes) of data this year that must be processed and analyzed to aid in the facility's search for new physics discoveries.

by the I-Connect007 Team

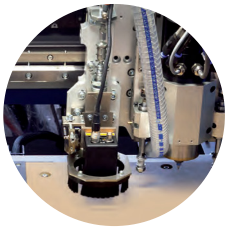
For this month's issue, our editorial team interviewed some of the top HDI experts in the PCB supply chain. Joining us on the conference call were Steve Bird, PCB/flex technology manager at Finisar, and Tony Torres of APCT. Also on the call were several technologists from MC Assembly: Vince Burns, quality engineer; Steve Jervey, director of Test Engineering; Mike Smyth, SMT engineer; and Paul Petty, product engineer. This wide-ranging conversation covered the latest technology developments, manufacturing challenges, and HDI strategies, from the design, fabrication, and assembly perspectives.

Andy Shaughnessy: Why don't we start with design? Steve, you're an HDI technology manager, so you're driving this whole thing. Why don't you tell us where you guys are with HDI?

Steve Bird: Sure. I'm wearing two hats. One is technical lead for the EEs and the CAD designers here at Finisar, and the second one is organic substrate roadmapping and development. Maybe 18 months or two years ago, we were working with a fabricator. We started cheating on the FR-4 design rules, and to their credit they built over 1,500 of these over a period of a year or so and finally gave it up and said, "No bid." So of course, the upper management team came to my group saying, "You're violating the design rules." And I said, "Yes, but not without an engineer sitting next to the CAD designer. And yeah, we did, but what we have here really is not a design rule violation, but a technology limitation."

That spun off an effort to find a substrate that could support the design rules that we're cheating to. Our PCB technology team was tasked with the effort. We got one new substrate developed and released, but now those new design rules are being violated; we have to continue development. For that previous generation, once we got off FR-4 and onto alternate materials, we were still in the subtractive process. Now we're looking very heavily at the semi-additive process. Our trace with normal FR-4 is going from 4 mil trace and space down to say, 3.5 mil,

MULTIPLE PLATFORMS



Drill/Rout/Optimizer
X-Ray Vision

MORE INFO

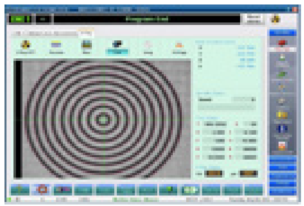
Drill/Rout Multi-Spindle
CCD/RGB Vision

MORE INFO

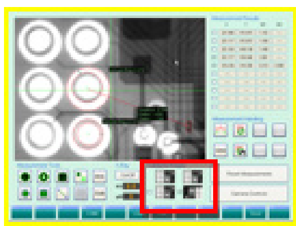
Dual Spindle All in One
Vision System

MORE INFO

SEEING IS BELIEVING



X-Ray - 8X Faster!
with NEW concentric target



See inside your PCB
measure your results!

Drill/Rout/Optimize
Entry level *"Smart Drill"*

MORE INFO

TIME-TESTED FEATURES

Vision Simplifies

Post Etch Slot/Drill

X-Ray Optimization

CCD Camera Optimization
"Smart Drill"

BarCode Job
Data Management

Panel Marking/Serialization

1700 Tool Library per spindle

Control Depth Drilling and
Routing to 15 µm

Lights out Automation

Up to 6 Spindle
Configurations

Automated Panel Prep
(Flash Routing, Edge
Beveling, Corner Champer,
Panel Thickness Measuring)

pluritec

www.pluritec.com | info@pluritec.com

roughly, and that's what earned us the no-bid. Now we're at two mil trace and three mil space, and that's still not good enough.

So, we're continuing to increase the density, and for us, our whole game is no vias, no stubs, and no parasitics. Everything's predictable: no glass weave, etc. So what we're looking at is thinner and thinner laminate, and hybrid stack-ups. We can certainly do all our power delivery and control signal distribution on FR-4 layers, but what lies on that surface is important to us. We can do small modules, system-type modules for our ICs and such, our chip-on-board and so on, but really what we need is a full system-level surface layer that can support those types of densities and mount chips.

Steve Bird

That's really what we are working towards right now. We're now looking at 20–25-micron traces and 25–40-micron gaps, and seeing if we can't do that. If we can, then we can support all our chip mounting technologies. We can support our system-level traces that get from the origin to the destination and so on. When we do that, then of course these traces get very lossy, and that becomes a huge concern. So our antidote to that is keep them short. Get them shorter. And so that's kind of our roadmap in a nutshell. We're starting with surface density, because the propagation is the fastest, keeping it stubless, and then making the net as short as possible. We run everything that's important differentially for noise immunity. So, you can imagine the types of stackups we're looking at in terms of hybrid stack-ups and so on.

Shaughnessy: What sort of materials are working out best for you?

Bird: When we first started this effort, my boss asked me, "What would you use? What's the first step that you would do?" My response was, "Thin, glass-free laminates. Something that's just as thin as you can make it." Let me put it this way: There is a slide that shows FR-4 with traces and spaces in the 4 mil range. With the help of HDI, we then took the through-hole off the surface and stacked the blind and buried vias. We call this technology level modified FR-4. This got us to 3.5 mil trace/space. There is another slide called the constant impedance funnel for differential pairs. You can imagine this funnel that starts out in the FR-4 at 4 mil trace/space and goes all the way down to be something like chip-on-glass or ceramic at 0.6 mil trace/space. One can place a large bracket in the gap with a label saying "This gap is too large. This gap is responsible for chewing up real estate because things are not scalable." The things that you do on an IC or on glass, you have a lot of overhead in terms of the splay angle, trying to get the signals out (escaped) and getting them routable.

We are trying to solve that. Because once you solve the trace to be similar to the pin or pad pitch, then your channels become much more scalable on the surface. By the way, as we're going up in frequency, we're also going up in channel count. We're getting whacked from both sides. We need to step back and look at what design rules we need. If we're at 25-micron trace and 40-micron gap, things such as channel count and speed become much more manageable. Now the trace has become much shorter. From a signal integrity standpoint, the first thing to do is get rid of all your parasitics, get rid of all your stubs, trace, tie-bars, etc., as well as your parallelism and propagation delay; get rid of everything that will kill a signal, and then go for improved material. That's where we're at right now. We're searching the world for the best material with the best copper with the best adhesion, which means the best processes in terms of subtractive, additive or semi-additive.

Then of course the vias stick out like a sore thumb, and even 25-micron vias stick out like a sore thumb to us. So it's very important that we go vialess for all our high-speed traces. If we do that, then we can get to where we want in organic material. My whole point is, let's be organic if we can, and I don't think we're done being creative here.

Happy Holden: Sounds like RF in the digital environment.

Bird: That's exactly what it is. It's a mix of RF- and IC-level packaging. We've become a packaging company. If you really think about what we're doing, we're reinventing our schematic into smaller and smaller packages with each generation, because we know that's the only way that the speed is going to scale. So, yes, exactly that. We're at the point with a coplanar waveguide that you either use all of it, from end to end, or you use none of it. Because if you terminate a coplanar waveguide early, it will show up in the sims and in the EMI behavior, it will also show up in the bit error rate tests. So, we can discern a 50-micron movement in a via, in terms of the return path. We're revising our boards just based on pad shaving, artwork shaving. No net list changes; we're just shaving the artwork.

Barry Matties: You mentioned that you're on a material search. Have there been any surprises in that search?

Bird: Yes, we've had a couple of surprises. First, the first generation was well at hand. If we don't do a lot of chip mount on PCB, then a lot of the polyimides would work for as long as we keep them on the top or bottom layers. But in the semi-additive process and the additive process, there are a couple of materials that are starting to show up as promising, which is probably the best way to say it. We're working out a deal where one of the suppliers is actually looking at pre-drilling the blind vias and pre-seeding the FCCL, so that we can use a fab house that would normally do just the subtractive process and get them into semi-additive without a lot of work.

Holden: Sounds like shades of via ply, where the polyimide was prebuilt with 1 mil holes and then vacuum-metalized and then plated up to 5 microns thick.

Bird: That's exactly the region we're in.

Holden: You didn't have to drill or metallize any holes because the via holes were already in the substrate. You just ended up with a lot of holes in the board because you didn't use those vias and they got etched away.

Bird: Got it. Now, what we're doing is we're sending our blind via drill chart to the FCCL (flex copper clad laminate) provider so they're customized. By the time they get over to the fab shop, our blind vias are pre-drilled and pre-seeded, including the via barrels. So, it's not the only path that we're taking. We're scouring the Earth for inorganic solutions as well. We're looking everywhere we can to stay competitive and our mantra here is that we have to explore every path, because if we don't our competitors will.

We're just now starting to explore the pre-drilled and pre-seeded layer idea. We're actually right in the middle of looking at particular fab shops saying, "Is there a traveler that you could put together that would yield these types of trace, space and via features?"

Stephen Las Marias: Tony, what HDI challenges is APCT facing right now?

Tony Torres: My title is director of marketing, so I'm not going to pretend that I'm an engineer. But what I can tell you is that, when this design goes to our DFM team, besides looking at lines and spaces, annular ring and hole to copper, one important issue that we review is the materials to be used. I was very interested in listening to the discussion on what's coming. The first thing that we must do to satisfy customer needs is to come through with quality and high-reliability product. We give a lot of feedback about what materials to use. We would be very, very open in that conversation.

> **"The first thing that we must do to satisfy customer needs is to come through with quality and high-reliability product."**

If a customer has the design already in hand and wants us to use a certain type of material, if we think that the design will be better and go through easier with a different type of material, we'll certainly suggest that. We have partnered with different material suppliers and we often go out with our sales force, with our supply partner at our shoulder, and start the design discussion of HDI work with material. It's very important that the materials work for both the OEM and the printed circuit board manufacturer. That's critical.

Secondly, we want to try to help them and guide them in design, so getting us involved early is just a tremendous help. Then we can confirm the design, confirm the manufacturability, and we're off and running. But everything is becoming thinner, smaller and tighter. Back in the day, the question was, "Can you get the hole smaller and smaller and through this board?" Now with laser drills, the issue is not about drilling the hole and getting perfect registration. Now the issue is how to get solution through the darn thing. I think more importantly, from a printed circuit board standpoint, the large departments are now in upfront engineering, being a teammate to all the customers who call in. I think the niche in the marketplace is not to simply take the Gerber files and build it, but to really be a partner to the end-customer. Be a help to them and talk out the design and get something that is not only reliable, but manufacturable.

Matties: Tony, what percentage of your customers are doing true HDI?

Torres: It's unbelievable. Just two short years ago, in 2015, we were doing 20% HDI work. Our facility in Santa Clara now does 85–90% HDI work. We're a company whose mantra is to say yes to the customer's needs, in technology and in delivery. We were forced to really learn how to build HDI work because that was their very first question: Can you build this product? Then they want to know how fast we can get it to them.

Vince Burns

Matties: Was that market demand or was that a capability that you carried out to your customers and swayed them to go in that direction?

Torres: It was market demand. The demand came from, as Happy knows, all those IPC meetings that we would attend monthly. Now the numbers in North America said that single-sided, double-sided and multilayer boards were all flat at best; HDI technology was the only growth model. Over the last three-year period, flex circuits and rigid-flex had a little bit of growth, but as far as percentage of the business, it was very, very low. The bulk of the business was HDI and so the writing on the wall was clear. That's why we made the shift in equipment and in upfront engineering, and it's paid off.

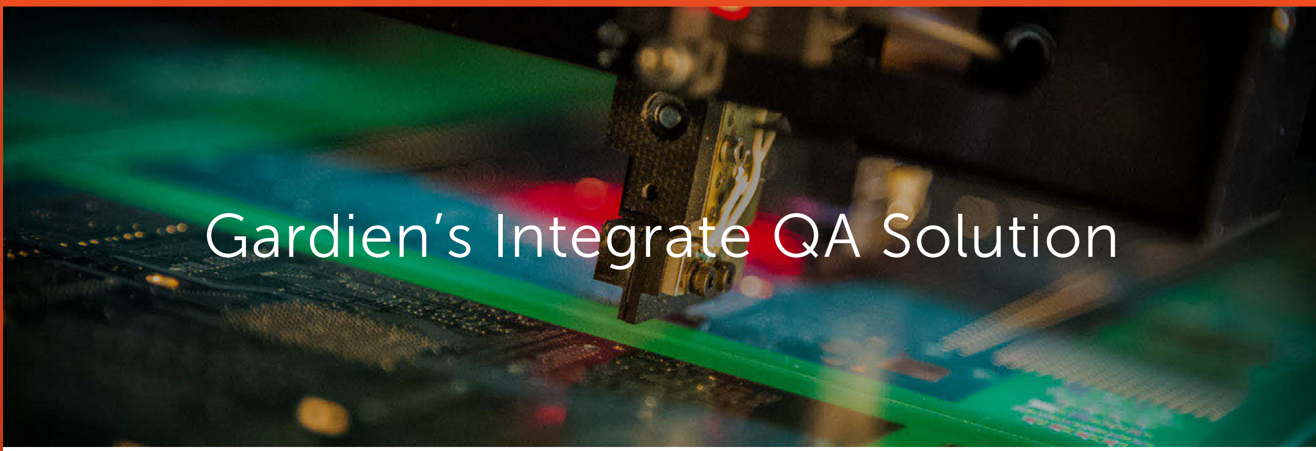
Matties: One of the advantages for HDI is that ultimately your customers wind up with a lower cost for their boards. Is that the result that your customers are reporting?

Torres: It is a mixed bag. Moving to HDI technology and keeping layer count down will ultimately wind up with a lower cost for our customer. However, there are times that, with standard through-hole technology and lower layer counts, simply adding two more layers may be more cost-effective than moving to an HDI design.

Las Marias: Thank you, Tony. Let's go to the assembly side. Vince, from your perspective at MC Assembly, what are the challenges when dealing with HDI boards?

Vince Burns: We're listening to the designer and the fabricator talk about getting layers thinner and smaller. But one of the things that we're all discussing here is the temperature cycles. Just starting out, everything that we build here must go through a reflow oven. It has to go through a reflow profile. We have to melt the solder so that we can get the parts to stick to the board, so the thinner the layers and material get, the more we're

Gardien



Gardien's Integrate QA Solution

WHAT IS INTEGRATE?

Integrate is a new approach to bare board PCB quality assurance. We address and are responsible for 100% of your tail end QA needs, whether it's AOI, testing, final inspection, or a combination of all three. We can provide the service in one of our service centers or fully integrate within your facility.

WHAT MAKES IT DIFFERENT?

Partnership pricing. Payment is based on product that actually passes quality assurance, not on panels produced or tested. Our success is built entirely on how successful we can help you become.

7000 jobs tooled per month

18100 orders processed per month

24,500,000 boards processed per month

Find out if our Integrate solution is right for you!

www.gardien.com/why-integrate

concerned about the adhesion of the layers, of the copper to the substrate, and the internal adhesion of the substrate layers. What I've seen in the past with boards that aren't HDI is that you'll get issues with moisture in the boards and then you'll get issues with delamination as we run through the reflow process at the surface metal level, and at the wave solder and through-hole level. And that's not even mentioning the rework.

Unfortunately, the way that the systems work is that they go through the reflow or the SMT process, and parts don't always go where you want them to go, and so you end up with rework. When we rework these things, now we're applying a 700°F soldering iron to a pad and you're more likely to have that glue that's holding the boards together come apart on you, so a big concern that we have are our thermal profiles and how these things are going to stick together. Another concern is that the smaller these parts get, the more difficult it gets for us to put solder paste on the board and have things that we can see, like the bottom side underneath the BGA. When things flow in there, we must look at it with X-ray. If we're talking about micro BGAs, we don't have a whole lot of clearance for the solder to reflow and hopefully not bridge.


Mike Smyth

Matties: How are you facing those challenges?

Burns: We're starting to use a lot more nanocoating on our stencils; we're focused in on different designs. Instead of typical round BGA pads, we're doing the square with the rounded corners, and we have to have carriers. A lot of the times, we're running boards through the reflow oven or an exterior that gives it more rigidity. It goes through reflow so you don't have any warping of the board, which can also damage it.

Matties: This of course adds cost and cycle time.

Mike Smyth: Right, and we also have an inline SPI which we are definitely checking.

Matties: For the solder paste, is jetting the solution for the solder paste in this application?

Paul Petty: It's something that we can look at. We do not have that capability at this time. We have looked at different equipment that could do that, but right now what we do is we rely on our SPI a lot. That monitors our height, volume, size. It keeps all the pads in check so that we can ensure that everything is meeting spec. I was also going to say we're sometimes constrained by our customers on which solders we can use. We have a variety of tin-lead solders and we have the RoHS-compliant solders, so we'll have a variety of the SAC solders and some others. For one customer, we use a low-temperature solder that has a high bismuth content, so we've got a huge variety of solders. Some of our customers don't allow high- or even medium-activity fluxes. We have to use ROL0 fluxes, which again creates other additional issues.

Matties: How often do designers come to you prior to designing the boards to discuss the best layout for assembly?

Burns: In about 12 1/2 years that I've been in this industry, I've had one company come to us and talk to us actively about the design of the board prior to them bringing it to us for manufacturing, and that was an interesting journey. It ended up working really well. They went through a lot of iterations of the board design before we finally got one that would work, but the vast majority come to us with a product and say, "Here, we're ready for you to start building this."

Matties: Obviously having the designer come talk to you first would be your preference, I would think. How do we get more designers to do that?

Burns: We have to convince them that there's value to be added. It's not just designing the perfect circuit, but it has to be manufacturable, and that's where our input comes in.

Matties: One of the things that Happy mentioned in a more recent conversation is design for automation. Happy, why don't you talk a little bit about that.

Holden: Well, with design for automation, when you start investing in very expensive automated equipment, you can't afford to replace that equipment over time because designers keep trying to innovate and doing anything they want. Instead, if you've got to get payback and have a cost-effective product, this is the capability of the automated equipment. You somehow have to design within the constraint of that; otherwise you can't run it down this really great automated line. We're back to hand-crafting it which is not going to be inexpensive. Automation is great, but it's not like humans. You can't reprogram it with a training course or a set of instructions. You're now constrained by the boundary condition of that automated equipment.

Matties: Do you all overhear designers talking about design for automation at all?

Torres: If I could put in my two cents from a fab standpoint, I would have the same comments as everyone else: Suppliers very rarely get involved early. If I can be so bold, I see it as a comment on business in general that everybody is just concerned with their own responsibility, their own expertise. You've got to start acting like partners, not only with suppliers, but with your internal customers as well. If that designer understood the cost problems of the purchasing department, one phone call to the fab manufacturer before the design is completed could save a lot of time and money. If you design something for manufacturability, it's going to be more cost-effective for their company, and obviously if you go one step further and design for automation, that's even better.


Paul Petty

I think the companies that embrace teamwork in all facets are going to win. When you start talking about the designers, do they know that the prototype is going to go into big production? In some cases, they do, but if they had a system to always call the fab house to have that relationship, why not call the assembly house and get all the feedback before the design is completely made? Then you have a winner in all facets and you're not chasing your tail after the fact. You're saving time and money upfront. The goal is to work together as a team and share our expertise with one another.

Matties: That's a great vision. One of the things that we started talking about some years ago was DFP, design for profitability. If it's a smart design, everybody makes money. What do we do to solve that?

Bird: I've been in this industry since '79 when Happy and I worked together at HP, and the things that we care about now are so different from the things we cared about then. For instance, who cared about the height of a trace or a trapezoidal shape back then? Now we're trying to squeeze gaps down, and all a sudden, we get this metallic bathtub where we are hitting the spacing limits because we can't etch out the gaps cleanly. We use ENEPIG a lot. But now we're getting to a point where nickel, the thickest metal in the stack, is too lossy. It just goes against our density and performance goals. Therefore, we are going to be evaluating EPIG, actually more accurately EPAG (electroless palladium/autocatalytic gold). We're looking at metal thicknesses and trace features that I never thought we would see during my career.

Also, as PCB technologists, we have to be willing to go out and scour the globe, not just within our approved vendor database, for what's up to date and then next year do it again and then do it again, because things are changing so quickly. The best thing we can deliver to the engineering community? Put together a package that is properly vetted, that you know is stable, all the delamination and via micro-cracking, etc., address all the reasons that people say why we shouldn't do it (challenge all paradigms). This means that we have to have DOEs going continually to make sure that we didn't just jump off the cliff. I'm always jumping off the cliff; Happy knows that. You really need to own it, and owning it is doing the look-aheads that you talked about—talk to your assembler, talk to your fabricator, and talk to the guy on the plating line. Talk to the guy who's running the laser drill. So this position two years ago did not exist and it does now, and the reason was because we were failing some of our substrates. Now, with proper vetting in place, we can explore just about anything that makes sense to us, as long as we qualify it before production. At this advanced level, PCB and flex technology roadmapping, PCB reliability, and the DFM process cannot be separated.


Steve Jervey

Matties: Tony, from your point of view and your role in marketing, just give us a quick overview of what you see in the marketplace. What's the feeling out there right now?

Torres: From a marketing standpoint, the goal is to keep your company "top of mind" to your customer or prospect. Because the industry had been close to flat over the past few years, I've noticed companies pulling back on their marketing efforts, when in fact I believe you should increase those efforts during challenging times. However, now in 2017, the industry is showing slow growth and more companies are coming back into the marketing arena.

What's interesting from my perspective is that the message being sent to the industry is what I see as the "standard" message: "These are my capabilities, these are my capacities, these are my cycle times, this is my equipment list and I have the lowest price!" Few, if any, talk about their people. And that's where APCT is different. Yes, you have to have the tools and equipment and the technology to be successful; however, it's the people that make the difference and I believe APCT is among the very best in that category.

From a marketing perspective, I think the feeling is wait and see. If the overall industry is showing growth, more companies will invest in marketing; if there's a downturn, companies will cut back. I strongly disagree with that perspective. The job of the marketing manager is to keep their company top of mind. Always invest in that philosophy to stay strong through upturns and downturns.

Holden: I have a question for Vince and his team. One of the problems HDI brings is limited access for in-circuit tests. Have you worked out solutions to help people who use HDI in terms of being able to use it for assemblies?

Steve Jervey: That's a big concern of ours. As a contract manufacturer, our in-circuit test traditionally has been a big part of our test solution. Over the last couple of years, I see that dying out very quickly. Our response to that in the immediate mode was to transition a lot of our work into flying probe with very small-pitch flying probe leads down to three mils on the point of the probe. We're doing a lot of flying probe work. The obvious extension to a physical test is to utilize boundary scans where we're capable of using vectorless type tests or physical access isn't there to test things. It's going to be a challenge. As things get smaller and smaller, ultimately you have to touch it somewhere to test it in some fashion and it's a challenge every day.

Holden: Technologies would help that where instead of looking for a via hole, you make an opening in the solder mask to touch any particular trace that may be available.

Jervey: Right, so that technology was pioneered by HP, I think, in the HP3070 (tester) days. They used to call it beads, where they would just eliminate the mask and put a little solder paste


Innovation:
it's what leaders do.
For over a decade, the world's top flex PCB processors have relied on ESI's advanced laser processing solutions to drive innovation and stay ahead.
Can you afford to make the wrong decision? Future-proof your investment in flex PCB with ESI's family of laser processing solutions, and maintain your innovation advantage.
Align yourself with the industry leader and let ESI take care of your flex PCB drilling needs.
esi®
ESI's family of FPC laser processing solutions.
5335™ GemStone™
Flex5335™ LodeStone™
5335xi™ RedStone™
For more information, visit us at www.esi.com

on the trace itself. Of course, as speeds get higher you probably don't want to put the paste on there. Probing just the trace is certainly an option, although sometimes probing the trace will deform the trace, so now you're introducing another aspect of altering the circuit.

Las Marias: Vince, from an EMS provider standpoint, what do you think our readers should consider when it comes to HDI assembly?

Burns: Honestly, I think one of the best comments I've heard today was just more communication and better communication up front. So for the design and the fab end of it, the readers should consider contacting not just the OEMs but some EMS manufacturing facilities and ask them up front what their capabilities are. If we go smaller and smaller, what do we need to do as an industry to be able to manufacture things at that level? This also goes to the component manufacturers because now we're also looking at components that have to be mounted on these boards.

We need the designers and the fab guys to understand the conditions that these boards are going to go through when they get to our end and a lot of it is heat. We're concerned about the number of heat cycles we can run a board through, and how we can keep from damaging things as we go through the heat cycles. From the material aspect, we need to make sure that the materials are robust enough to withstand the things that we're going to put them through at our end.

Matties: All right then. Thank you, everybody. This was great.

Burns: Yeah, that was good.

Bird: Thanks.

Torres: Thanks, I appreciate it. **PCB**

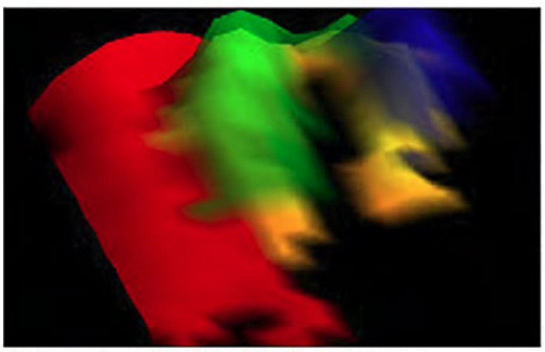
Electroplating: Birth of a Single Nucleus Caught 'In Camera'

Electroplating, or electrodeposition, is one of the most important processes in chemistry. A metal cation in solution can be reduced to its elemental form by applying an electrical potential to an electrode. This enables electrical contacts to be made in integrated circuits with nanometric precision.

Despite decades of research worldwide, visualising the early stages of electrodeposition—the formation of the first nucleus—remains a formidable challenge. A collaborative work involving the University of Bristol's Schools of Chemistry, Physics and the Bristol Centre for Functional Nanomaterials CDT has come up with an entirely new approach to monitoring the process leading to the birth of a nucleus in real time.

Writing in the journal *Nature Communication,* the team show how detecting very small local perturbation of the water structure near the surface, the complex dynamics of early stages of electrodeposition can be tracked. David Fermin, professor of electrochemistry and lead author of the work, said: "This is a very exciting development which pushes the boundaries of spatio-temporal resolution of electrochemical processes.

"There are highly sophisticated methods which allows monitoring phenomena at the atomic scale, but compromising the dynamics of the process, while other methods can follow very fast dynamics, but we can't see where they happen in space."



An artistic impression of the birth of a nucleus
Image credit: University of Bristol

Employing Lateral Molecular Force Microscopy, developed by the team of Professor Mervyn Miles at the School of Physics, the team could spot the formation of a metallic nucleus by following perturbations of visco-elastic properties of hydration layers with nanometer resolution.

MilAero007 Highlights

Cloudy with a Chance of Radiation: NASA Studies Simulated Radiation

In each life a little rain must fall, but in space, one of the biggest risks to astronauts' health is radiation "rain". NASA's Human Research Program (HRP) is simulating space radiation on Earth following upgrades to the NASA Space Radiation Laboratory (NSRL) at the U.S. Department of Energy's Brookhaven National Laboratory.

Sensible Design: Thermal Management—The Heat is On

Thermal management materials are designed to prolong equipment life and reduce incidences of failure. They also maintain equipment performance parameters and reduce energy consumption by reducing operating temperatures, and minimising the risk of damage to surrounding components.

Update on IPC's Validation Services and Hints of What's to Come

SMTA International is the perfect time to get updates on IPC happenings. One that I'm always curious about is the Validation Services programs. At the busy show, I managed to find a quiet spot so Randy Cherry, IPC's director of Validation Services, could fill me in on the latest.

Developing New Magnetic Device Materials

Assistant Professor of Electrical Engineering Luqiao Liu is developing new magnetic materials, known as antiferromagnets, that can be operated at room temperature by reversing their electron spin and can serve as the basis for long-lasting, spintronic computer memory.

American Standard Circuits Upgrades to ISO 9001:2015

American Standard Circuits has recently upgraded their ISO quality management certification to the latest standard, ISO 9100:2015.

Developing Sensors to Defend Aircraft Against Lasers

MIT Lincoln Laboratory team is working on ground-based cameras that detect sources of laser beam attacks on aircraft and may lessen dangers for pilots.

Drones to Grow Mind of Their Own

The use of drones is gaining popularity among environmentalists and law enforcement officials alike due to the robots' ability to reach far-flung locales not easily accessible to humans. A person typically sets the drone on a pre-determined path to collect data.

New Radar Sensor Provides Clear Vision in Any Weather

DARPA's Video Synthetic Aperture Radar (ViSAR) program recently completed flight tests, successfully demonstrating a new sensor that can capture real-time video through clouds.

Global Defense Spending Momentum will Provide $771 Billion Opportunity for Industry

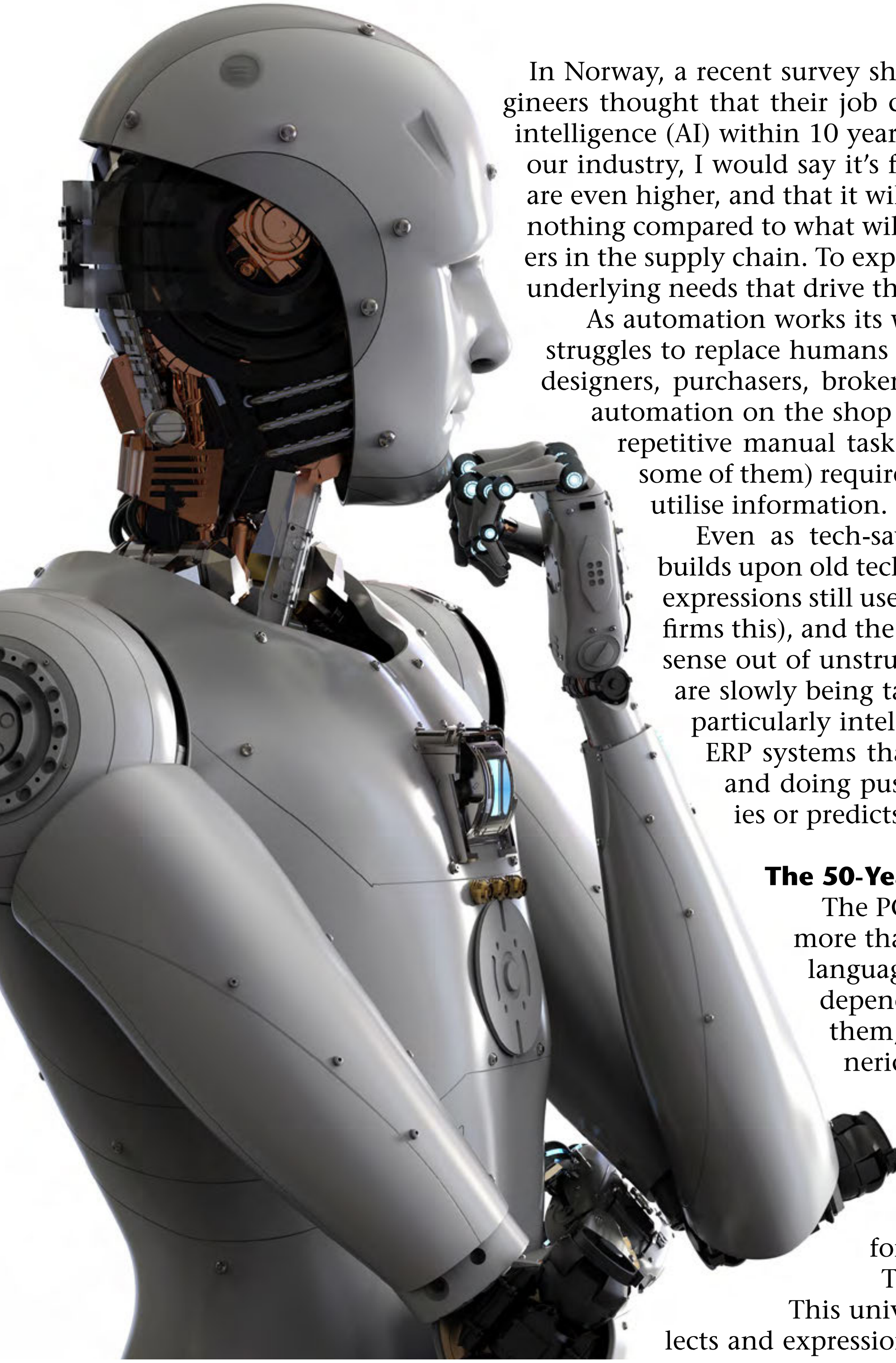
The Strategy Analytics Advanced Defense Systems (ADS) service report, "Global Defense Spending Outlook 2016-2026," forecasts the global defense budget will grow to $2.41 trillion in 2026, with the opportunities available to industry growing at a CAGR of 3.5%, to reach $771 billion.

Rockwell Collins' Cabinconnect™ Wireless Offering Addresses the Growing Trend Toward Bring Your Own Device

Rockwell Collins is addressing the growing passenger demand to be connected on their own devices while flying with its CabinConnect™ inflight wireless connectivity and entertainment solution.

Industry 4.0, AI and CircuitData

by Andreas Lydersen
ELMATICA



In Norway, a recent survey showed that one out of seven engineers thought that their job could be performed by artificial intelligence (AI) within 10 years. If we look at the engineers in our industry, I would say it's fair to assume that the numbers are even higher, and that it will happen faster. But that will be nothing compared to what will happen to the rest of the players in the supply chain. To explain why, we need to look at the underlying needs that drive the supply chain itself.

As automation works its way onto the shop floors, it still struggles to replace humans in the supporting roles, such as designers, purchasers, brokers, and back-office staff. Where automation on the shop floor replaces humans in doing repetitive manual tasks, the supporting roles (at least some of them) require intelligence to understand and utilise information.

Even as tech-savvy as our industry is, it still builds upon old technology (just a quick look at the expressions still used, like screens and stencils, confirms this), and the human brain is great at making sense out of unstructured information. Some tasks are slowly being taken over by machines, but not particularly intelligent ones. One example is the ERP systems that are automating procurement and doing push and pull requests on deliveries or predicts needs and place orders.

The 50-Year-Old Legacy

The PCB industry carries the legacy of more than 50 years of development and language. To be manufactured, PCBs depend on people who understand them, compare them with their generic requirements, and find partners for assembly or manufacturing. Add to that the secrecy needed and the different formats used, and humans are pretty much your only option, for now.

This is where AI comes into play. This universe of formats, languages, dialects and expressions is complex, but still operates

productronica
Visit us! Hall B3, Booth 471
Excellon
Manufacturers of precision Micro-Machining Solutions for over 50 Years
COBRA II
Hybrid laser system
689
6-station precision drilling and routing system
HS-1L DS
Single-station, dual spindle high-speed system
136L
High accuracy and speed
154L
Large panel applications
HS-2L
2-station, high-speed
129
Single-station precision system
Move into the future with the latest innovations in Fabrication Technology from the Industry Leader!
www.excellon.com

within a set of rules. As AI slowly learns these rules, it helps humans to make sense of it. Gradually, as the intelligence expands, it replaces humans altogether. Integr8tor by Ucamco is an example of this. Although it could be argued that this is not actual intelligence—just a set of algorithms and code—it replaces humans in building understanding. There are a number of other examples of software tools that do the same thing or performs related tasks; there will be more and they will become better. They won't take your job, but instead, they will simply allow you to be more efficient. For them to replace humans, they need to step it up and integrate with other systems, and the confidence in them needs to grow. This will happen; hundreds of developers are already working on it.

"For them to replace humans, they need to step it up and integrate with other systems, and the confidence in them needs to grow. This will happen; hundreds of developers are already working on it."

In this chaos of formats, languages and dialects, AI is not the only path to choose, and it is not an "all or nothing" choice. CircuitData is an open source project that uses standardisation to replace brain power.

A Substantial Challenge

My colleague, Jan Pedersen, senior technical advisor, has more than 40 years in printed circuits, receiving each week numerous files with manufacturing data. The pattern is quite repetitive, and not in a good way. There is one substantial challenge that keeps coming back: insufficient—or even totally wrong—article specifications.

When he receives manufacturing data from 10 customers, he often gets 10 different ways to present and explain what's asked for. Tolerances are expressed differently. Fabrication drawings are explained differently. Solder mask is called green mask or even green oil. Component notation is called legend, silk-screen, silk layer or something else. We can live with a different word, but not a missing requirement!

We have decided to challenge the world and improve this issue. We have started to create a standard PCB specification, a new language to share information. We are offering this new standard—or language—as an open source to the PCB industry. It is free of charge and will be a valuable source of information for any PCB designer, user or not.

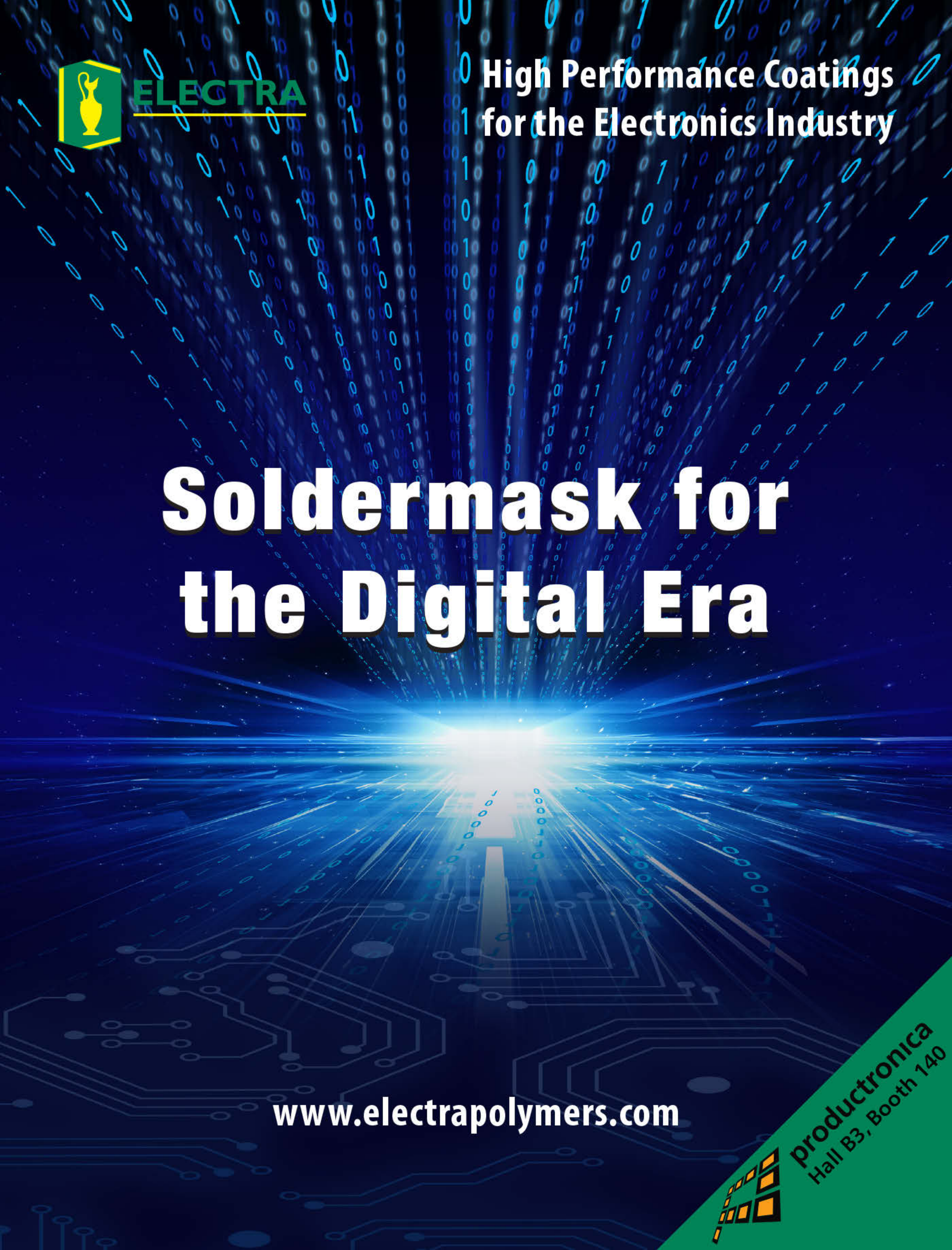
A Language in Addition to, not Instead of

So, what does CircuitData do? To begin with, it aims to be a supplement to the files that are currently used, such as Gerbers, ODB++ and IPC-2581, so that all aspects of manufacturing not provided are resolved. As the standard evolves, we want it to replace the need for transmitting the files throughout the supply chain. This can be done by providing the different parties with only the information they need, and leave the exchanging of files to the first and last part of a set supply chain—the OEM and the manufacturer.

But, as with all free and community-driven projects, the value of the language increases simultaneously as the number of contributors and users rises. It needs to be developed, maintained and fueled like an old and beloved sports car. Because communicating PCB specifications is a dialog, not a monolog. It requires several pieces of information to come together so that all the facts are presented correctly. But the specifications are just part of what is needed; they need to fit with profiles (requirements) and capabilities.

To use the format, you start out by reading the documentation. Then you prepare your internal systems to be able to send and receive this kind of information. Over time, we believe that there will be several systems available that will help you utilise the format.

Another way to use the language is to specify profiles. Profiles are meant to replace the current way of exchanging PDFs with "requirements." The current method involves


ELECTRA
High Performance Coatings
for the Electronics Industry
Soldermask for
the Digital Era
www.electrapolymers.com
productronica
Hall B3, Booth 140

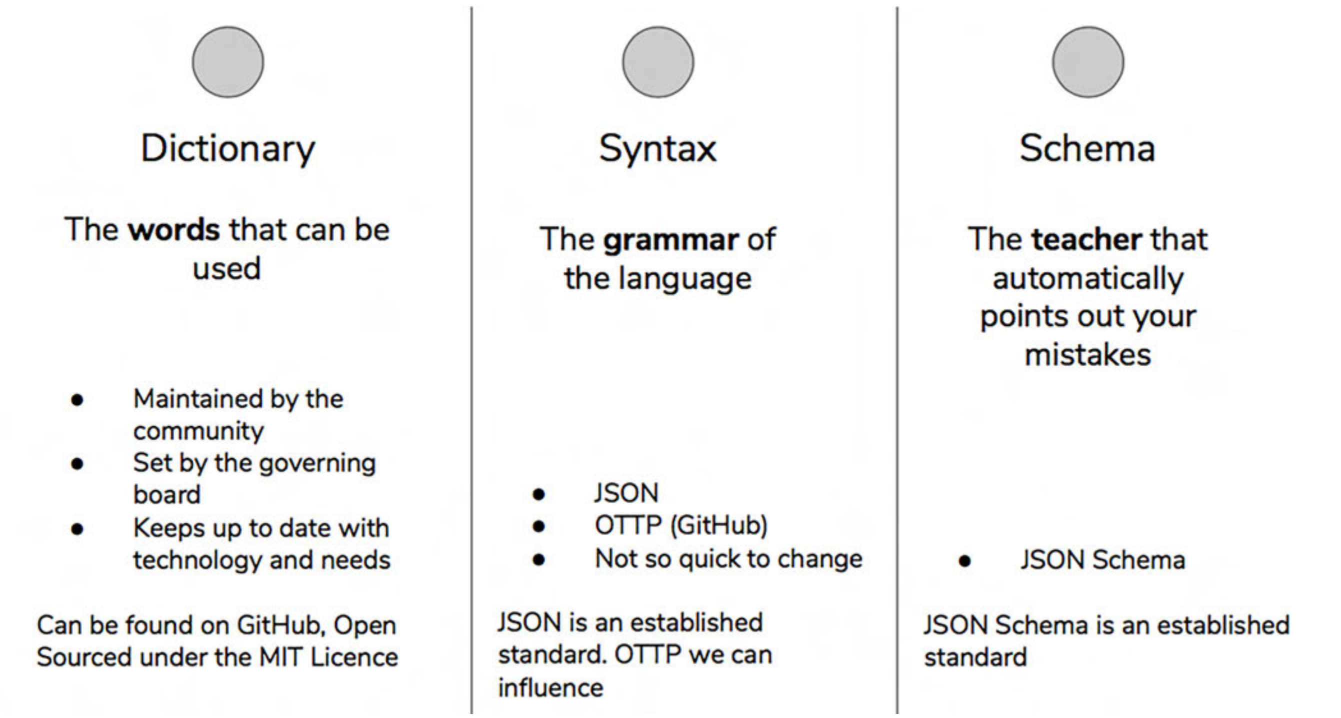


Figure 1: To make the "language" more understandable, Lydersen has divided it into three parts: the Dictionary, the Syntax, and the Schema.

noting in your own words the defaults, "dos" and "don'ts" that everyone in the supply chain needs to know. With this format, you can set your requirements in a machine-readable format that ensures compliance.

The third way of using this is to specify a capability. This allows you to send out a set of manufacturing capabilities to your clients. The goal is to minimise the number of RFQs that are sent out to non-capable suppliers, to benefit both the suppliers and the clients.

The Strict Teacher

So, what does the language consist of? To make it easier to understand, we can divide it into three parts: the dictionary (the words themselves); the syntax (the grammar); and the schema (the strict teacher) as shown in Figure 1.

At this point, and thinking of automation and AI, you might wonder: What's in it for me? Because in the end, that's everyone's main concern.

What's in It for Me?

Let me briefly give you some thoughts around this. You would get a computer-readable PCB specification, a language and tools that you easily can link with your existing software. Files can be added on-the-go from design, through OEM, EMS, broker to PCB factory but will seamlessly fit together. It is all community driven—we would all own it together—a common language developed and maintained by the industry.

There would be no need of PDFs or other spec files that must be re-typed manually. It can easily be imported into existing ERP systems—in your own language! The best part, and my favourite, is that it would save us all lots of time and money. And, we would avoid issues late in the supply chain.

Sounds like something we see in futuristic movies, where robots take over systems and make the world better? It's not.

Automation will keep on happening, driven by standardisation and AI. It is the obvious choice in a supply chain where people are the most expensive asset. As companies are finding their place in this new ecosystem, I'm sure that we will see both companies and software have great rises and massive falls. The focus needs to

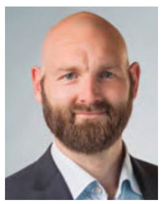

UCE WET PROCESS LINE
Etchers
Scrubbers
Developers
PTH
Oxide Replacement
THIN CORE HANDLING • PC CONTROL • RELIABLE • LOW COST
CLICK TO VIEW OUR UCE WET PROCESS LINE
The leading European PCB Equipment and Parts Supplier
www.vikingtest.com
sales@vikingtest.com
productronica 2017
Visit us! Hall B3, Booth 444
Viking

stay outwards: How am I contributing to a better supply chain? Are our products making life less complicated for whomever receives them? Self-centred companies will lose out in the long run.

Technology Changes Everything

So, what does Industry 4.0 have to do with all this? The fourth industrial revolution is about computers talking to computers. As they are simply better than us at keeping track of products through the flow of a supply chain, they can automate processes between partners. This allows orders to be made and rescheduled, needs to be analysed and reacted upon, whole production processes to speed up or slow down. In the PCB industry, this means that the goal is to be an interconnected part of the supply chain. Fabricators will have to adjust their shop floor setup automatically based on customer needs and focus on robotics beyond each station on the floor. Product owners must understand that the old approach of product life cycle management is a thing of the past; there will be no traditional path from prototype to volume. The agile players in this industry will realise that by focusing two ways—outwards to their partner and inwards to each product and what is to its best interest—they are contributing to a successful supply chain. The traditional game of margins is a losing game. The new game is making your contribution count in an industry where products never move out of prototype.

Technology changes everything and often exponentially. Both AI and standardisation projects like CircuitData have amazing potential to contribute, but are not goals in themselves. The goal is to work smarter, have less impact on the environment and move in tune with demand. In my mind, this is Industry 4.0. **PCB**

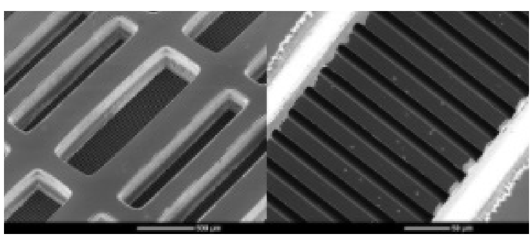


Andreas Lydersen is CTO at Elmatica, a printed circuit broker since 1971 that operates globally in all industries.

'Intrachip' Micro-Cooling System for High-Performance Radar, Supercomputers

Researchers have developed a new type of cooling system for high-performance radars and supercomputers that circulates a liquid coolant directly into electronic chips through an intricate series of tiny microchannels.

Conventional chip-cooling methods use finned metal plates called heat sinks, which are attached to computer chips to dissipate heat. Such attachment methods, however, do not remove heat efficiently enough for an emerging class of high-performance electronics, said Suresh V. Garimella, principal investigator for the project and the Goodson Distinguished Professor of Mechanical Engineering at Purdue University.



New advanced cooling technologies will be needed for high-performance electronics that contain three-dimensional stacks of processing chips instead of a single, flat-profile chip. Too much heat hinders the performance of electronic chips or damages the tiny circuitry, especially in small "hot spots."

"You can pack only so much computing power into a single chip, so stacking chips on top of each other is one way of increasing performance," said Justin A. Weibel, a research associate professor in Purdue's School of Mechanical Engineering, and co-investigator on the project. "This presents a cooling challenge because if you have layers of many chips, normally each one of these would have its own system attached on top of it to draw out heat. As soon as you have even two chips stacked on top of each other the bottom one has to operate with significantly less power because it can't be cooled directly."


Get the spark you need to tune up your sales team.
When an engine doesn't fire on all cylinders, performance is limited. The same goes for your sales team. We provide the spark to get your sales to the next level ...and beyond.
We've helped dozens of companies big and small improve their bottom line.
db MANAGEMENT GROUP
Learn how we can help YOU
207-649-0879
danbbeaulie@aol.com

FlexFactor™: Faith in the Future

by Tara Dunn
OMNI PCB

Take just a minute and read through this list of new product ideas. Can you identify the common thread? Yes, they are all enabled by advanced technology, but would you believe that these products were all pitched in the last year by high school students?

Drive Alert:

Problem – Drowsy driving.

Solution – A patch placed on the temple can detect if the user is drowsy and wakes up the user.

Technology – Circuits form a flexible patch with sensors detecting theta brain waves indicating if the user is drowsy or daydreaming.

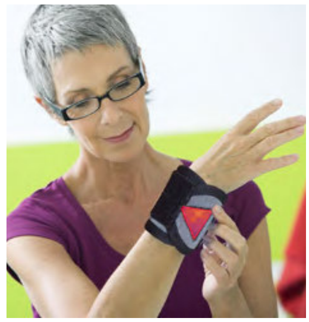
Fast Asleep:

Problem – In 2015, there were nearly 4,000 Sudden Unexpected Infant Deaths (SUIDS) in the U.S., with 1,600 of those being attributed to Sudden Infant Death Syndrome (SIDS). Because of this, 59% of working parents do not get enough sleep.

Solution – A small wristband fits snugly around sleeping baby's arm and measures movements, oxygen, and heart rate, to let you know the baby is safe and sound asleep.

Technology – Mounted flexible hybrid electronic wristband connected to device via Bluetooth.

RA Solutions:



Problem – RA is a chronic, inflammatory disease that causes mild to severe joint pain and stiffness, which can lead to a wide variety of damaged body systems including skin, eyes and lungs.

Solution – The Relieve Sleeve, a pain reliever that administers heating sensations and applies electric pulses tailored to a user's needs. The functions are embedded in a compression sleeve for easy application around joints and muscles.

Technology – Flexible battery, micro-coiling embedded in the compression fabric, Bluetooth chip to connect to the app, electrical pulses produced from thin wires, wireless charging hub for battery.

Asthmex:

Problem – According to CDC, 25.7 million Americans suffer from asthma. Between the years 1996–2012, 8% of Olympic athletes suffered from asthma. 11.8% of the 7.8 million high school athletes in the U.S. have asthma.

Solution – A chest band with a smart patch to detect asthma symptoms, which triggers and administers medication via auto-injector.

Technology – Smart fibers within the band detect symptoms of an attack specific to the individual.

Just to reiterate, these creative new product ideas have all been pitched by high school students! These students have all participated in the NextFlex FlexFactor™ program. Growing the next generation of advanced manufacturing workforce is a key component of the NextFlex mission of developing technologies for commercial adoption while supporting a sustainable manufacturing ecosystem.

What is FlexFactor?

This program is designed to enable youth to engage with next generation technology through entrepreneurial immersion. Over the course of this program, students work in teams to conceptualize a flexible hybrid (FHE) electronics-based hardware device that solves a human health issue or performance monitoring program, develop a business model around the opportunity, and pitch "Shark Tank" style to a panel of industry representatives. In the process, students become immersed in advanced technology and entrepreneurship, are inspired by the advanced manufacturing industry segment, and gain a deeper understanding of the education and career pathways for the future.

This four-week program kicks off in the classroom where students break into teams, are given the mission, the building blocks of flexible hybrid technology, and can define the problem and research hypothesis. Throughout the program, students interact with assigned technical mentors as they develop their product idea. The next week, students take a field trip to tour an advanced manufacturing facility that provides a deep dive into the world of hybrid and flexible technology and gives the students the opportunity to interact with manufacturers, technicians and engineers to get a sense of what is like to work in these environments. The third week is a field trip to a local community college where students sit in on two, 90-minute entrepreneurship lectures and experience the feel of college life. The final week each team pitches their product idea, including target market analysis and cost vs. revenue projections, to industry experts. Through this program, each student is enrolled in the community college and receives college credit upon completion.

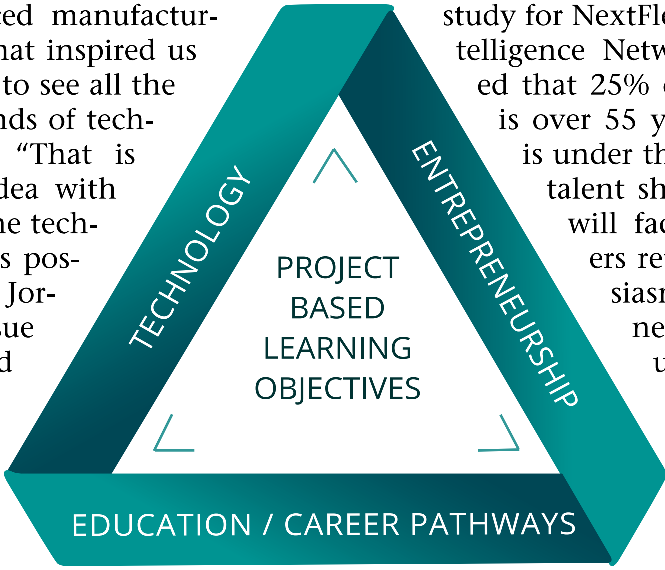
How much fun would that be! With enrollment skyrocketing, the program is obviously engaging students and sparking interest. Brynt Parmeter, director of Workforce Development at NextFlex, explained that the first session started in the fall of 2016 with eight students participating. Following its fourth session the spring of 2018, the program will have had over 2,000 participants. That is amazing growth and speaks volumes about the program.

I had the opportunity to speak to Jordan Tachibana, who was part of the group responsible for the Asthmex product. Jordan had been taking business classes with a marketing major focus and was introduced to this program through a teacher describing the program as an entrepreneurship program with an emphasis on advanced manufacturing.

RESEARCH

DESIGN & DISCOVERY

PRODUCT IDEA PITCHES



"Touring the advanced manufacturing facility is actually what inspired us the most because we got to see all the cool applications and kinds of technology," he explained. "That is what slingshotted my idea with my group. After seeing the technology, we saw what was possible and said, 'Let's go.'" Jordan is continuing to pursue the Asthmex product and has enrolled in the program for a second time.

Through FlexFactor's collaborative approach to education, entrepreneurship and technology, NextFlex is helping students identify and engage in career pathways in advanced manufacturing, while actively increasing the interest and talent in the U.S.-based STEAM pipeline. The FlexFactor program creates a win for all stakeholders. High schools expose youth to real-world problems, blend STEAM and entrepreneurship in a project learning environment, and students further develop personal and professional skills. Community colleges expand enrollment, create additional educational and career pathway opportunities, and link community college STEAM focus to a Manufacturing USA Institute.

Government facilitates the creation of a nationally competitive talent pool prepared to tackle society-wide technology challenges, increase student awareness in STEAM occupations, motivate students to purse STEAM education, and provide students a government-sponsored activity that develops disciplinary based knowledge and promotes critical thinking, reasoning and communication skills. Our industry benefits by the expanded awareness and interest in advanced manufacturing, reduced hiring expenses via a direct channel to qualified resources for both internship and long-term workforce requirements, and increased community exposure through relationships with local high schools and community colleges.

A talent pipeline shortage is looming across all flexible hybrid electronics (FHE) manufacturing occupations. This was validated in a 2016 study for NextFlex[1] by the Workforce Intelligence Network. This study reported that 25% of the workforce in FHE is over 55 years old, while only 6% is under the age of 24, indicating a talent shortage that the industry will face as experienced workers retire. There is also enthusiasm in the industry to connect with students that are unsure of career opportunities in advanced manufacturing sectors and are unaware of new technologies now in development that will impact lives in meaningful ways. The FlexFactor program is working to bridge the gap, connect students and organizations, and bring excitement about advanced manufacturing to young people.

What isn't there to be excited about: mouth guards that could detect an athlete's hydration level; non-obstructive patches that could detect blood glucose levels for Type 1 diabetics; an allergen medication patch that can administer the exact amount of epinephrine needed based on inflammation detected in the blood; and a device that can detect the levels of leptin hormone to evaluate sleep quality. Yes, these and many more cool applications are coming from the FlexFactor list of products that have been pitched. If these ideas are generated from a four-week program, I am excited to see what these students will develop in the future, and have renewed faith in the future of our industry and the role that advanced manufacturing and flexible hybrid electronics will play. **PCB**

Reference

1. Report available from www.nextflex.us.

Tara Dunn is the president of Omni PCB, a manufacturer's rep firm specializing in the printed circuit board industry. To read past columns or to contact Dunn, click here.

UPCOMING Programs

November 7, 2017
IPC Day
Networking Event
Raleigh, NC, USA

November 7, 2017
IPC Technical Education
held in conjunction with PCB Carolina
Workshop
Raleigh, NC, USA

November 7–9, 2017
The Pb-Free Electronics Risk Management (PERM) Council Meeting No. 34
Philips Innovation
Meeting
Andover, MA, USA

November 8, 2017
Wisdom Wednesday
Competitive Innovation: Best Practices
IPC Members Only
Webinar

November 14–17, 2017
IPC Committee Meetings
held in conjunction with productronica
Meeting
Munich, Germany

November 14–17, 2017
IPC Hand Soldering Championship
held in conjunction with productronica
Competition
Munich, Germany

December 6–8, 2017
HKPCA International Printed Circuit and Exhibition & APEX South China Fair
Conference
Shenzhen, China

December 13, 2017
Wisdom Wednesday
Strategies for Reducing Product Warranty and Liability Risk in Manufacturing Services Agreements
IPC Members Only
Webinar

February 24–March 1, 2018
IPC APEX EXPO 2018
Conference & Exhibition
San Diego, CA, USA

March 1–2, 2018
The Pb-Free Electronics Risk Management (PERM) Council Meeting No. 35
held in conjunction with IPCAPEXEXPO
IPC Members Only
Meeting
San Diego, CA, USA

For more information, **visit www.IPC.org/events**

Connecting the Dots Between Manufacturing and Community

by John Mitchell
IPC–ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES

Across the United States, the first Friday in October represents the annual celebration of Manufacturing Day. On this date, manufacturers and supporters come together to celebrate the longevity and success of our industry. Since 2012, Manufacturing Day has served as a chance to learn about the businesses that thrive in our communities and contribute greatly to the economy.

The manufacturing industry has proven vital to the success and growth of our communities, and our communities are essential to the success of manufacturing. From printed circuit boards to cellphones, chances are there is a manufacturing facility near you, creating products that you may not even realize you use.

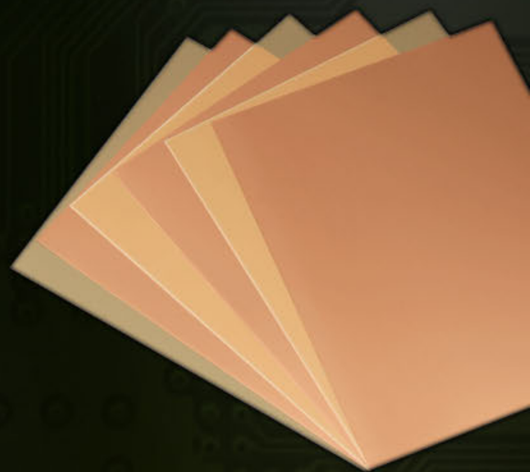
Manufacturing Day began with a goal to invite students, educators, businesspeople, media, and politicians to facilities across the country to educate them on the ins and outs of our industry. It has since evolved into an opportunity to inform visitors of the numerous career options in the manufacturing sector and the public policy issues that affect our success.

For example, manufacturers across the country have expressed concern over the perennial shortage of skilled talent. Leading into Manufacturing Day, IPC offered a letter of support for the Apprenticeship and Jobs Training Act (S.1352)[1], which was introduced in the U.S. Congress by Senators Susan Collins (R-ME) and Maria Cantwell (D-WA). The act would create a $5,000 tax credit for up to three years for companies that hire and pay employees enrolled in a federal- or state-registered apprentice program, as well as allow senior employees near retirement to draw from pensions early if they're involved in mentoring or training new employees. Additionally, this act will help veterans get into skilled jobs that match their mili-

Panasonic

Ultra-low Transmission Loss Multi-layer Circuit Board
Materials for ICT Infrastructure Equipment

MEGTRON7



Laminate **R-5785(N)**
Prepreg **R-5680(N)**

H-VLP2 Cu and Low Dk
Glass-Cloth Specifications

Features

- H-VLP2 copper foil and Low Dk glass-cloth allows for 30% loss improvement than MEGTRON 6
- Glass transition temperature (Tg): 200°C (DSC)
- Reduce process cost (Improve drill processability and ENIG (Electro-Nickel Immersion Gold))

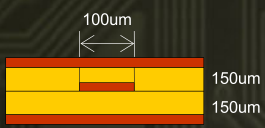
	Dk	Df
R-5785(N) + H-VLP2 Cu	3.4	0.002 @ 12GHz
R-5775	3.6	0.004 @ 12GHz

Applications

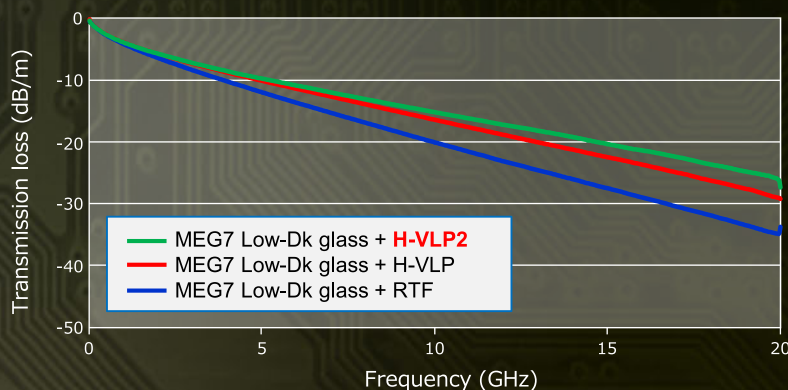
- High-end servers, High-end routers, Supercomputers, and other ICT infrastructure equipment, Antenna (Base station, Automotive millimeter-wave radar), etc.

Trasmission Loss

- Evaluation Sample



Line Length	1000 mm
Impedance	50 Ω
Copper Thickness	18 μm
Inner Cu Treatment	No-surface Treatment
Core Type	#1078 (RC67%) x 2ply
Prepreg Type	#1078 x 2ply



Contact us

More information

tary experience sooner by allowing credit in apprenticeship requirements from previous military training.

As an official endorser[2] of Manufacturing Day, IPC also reached out to several state governors requesting proclamations on the importance of this annual celebration. Govs. Greg Abbott (R-TX), John Hickenlooper (D-CO), Bruce Rauner (R-IL), and Tom Wolf (R-PA), each offered proclamations recognizing the contributions of the advanced manufacturing industry in communities across the country.

Similarly, on Manufacturing Day, President Donald Trump convened manufacturers from across the country for a White House ceremony. During the service Trump signed a presidential proclamation recognizing the importance of the country's manufacturing history.

Meanwhile, several IPC member companies joined the growing list of Manufacturing Day local events as they opened their doors to the public to show what advanced electronics manufacturing looks like.

IPC member company STI Electronics hosted local school groups, including a group of female engineers, to tour their manufacturing facility in Madison, Alabama.

Bay Area Circuits offered a presentation on importance of manufacturing and an overview of the PCB manufacturing process. The company also conducted a tour of its manufacturing facility, highlighting many key processes.

Power Design Services gave a tour of their 10,000-square-foot facility, where attendees saw the printed circuit board assembly process. The event included a career fair and a brief presentation on assembly technology and flow.

Each year Manufacturing Day continues to exemplify the contributions our industry makes nationwide. If you missed the chance to celebrate the date this year, mark your calendar now for 2018! **PCB**

References

1. IPC Supports Apprenticeships and Jobs
2. MFG Day Sponsors and Endorsers

John Mitchell is president and CEO of IPC—Association Connecting Electronics Industries. To read past columns or to contact Mitchell, click here.

Recent Highlights from PCB007

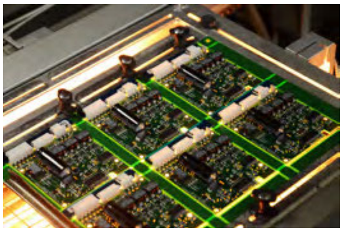
1 EPTE Newsletter: Can Toshiba Survive?

Toshiba was the leader in the electronics industry, and developed and marketed many types of electronic equipment and devices that included word processors, printers, VCR cameras, tape recorders, hard disc drives, transceivers, laptop computers, facsimiles, cellular phones, and more.

2 The Right Approach: Navigating Process Change? TPC is the Key

Change is a given. While this adage may be quite true and normally a good thing, it can wreak process engineering havoc in a printed circuit operation. Change is good, but the operative word phrase is controlled change relative to the complex processes involved in manufacturing a printed circuit board.

3 Flex Talk: The Man Behind the Curtain



"Pay no attention to the man behind the curtain." This famous quote from The Wizard of Oz conjures up the image of Dorothy, the Tin Man, the Cowardly Lion and the Scarecrow discovering that the great Wizard of Oz isn't as grand or as magical as he seems.

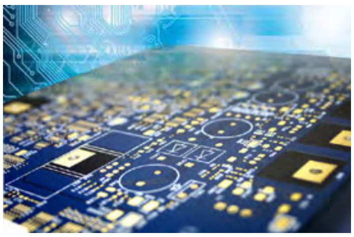
4 Catching up with FineLine Global

With locations all over the world and technology offerings covering all technologies, I wanted to see for myself what this "broker on steroids" was all about—how they got started and how they grew. So I was delighted to have a conversation with Eli Ikan, Fineline Global's General Manager.

5 RTW SMTAI: Prototron Continues its Growth

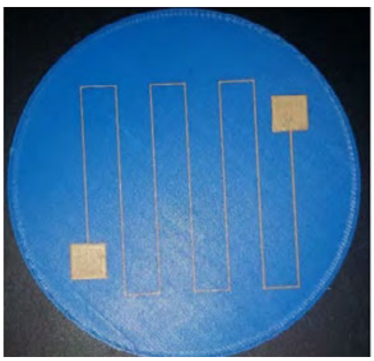
Dave Ryder and Russ Adams of Prototron Circuits discuss the firm's 30th anniversary and their continued growth. Prototron recently hired several new staff members, and the company still has one open position to fill.

6 American Standard Circuits Upgrades to ISO 9001:2015



American Standard Circuits has recently upgraded their ISO quality management certification to the latest standard, ISO 9100:2015.

7 3D Printed Electronics for Printed Circuit Structures



Printed electronics is a familiar term that is taking on more meaning as the technology matures. Flexible electronics is sometimes referred to as a subset of this and the printing approach is one of the enabling factors for roll-to-roll processes.

8 Bay Area Circuits Celebrates Manufacturing Day 2017

"Manufacturing Day continues to be an opportunity for us to connect with engineering students and introduce high-technology manufacturing to them as a viable career path," said Brian Paper, chief operating officer at Bay Area Circuits.

9 All About Flex: Flexible Circuit Failure Analysis

Design reviews and early involvement by a circuit board fabrication house can minimize the possibility of field problems, but despite best efforts, there remain occasions when diagnosis of a poorly performing design is required.

10 A Guide to IPC Survey and Report Season

IPC Director of Market Research Sharon Starr found time to discuss the recently conducted and published surveys and research reports and a few others still in the works. These reports are free to survey participants, which is certainly a great incentive for taking the time to complete them. (Hint: That's a call to action for those of you sitting on the sidelines.)

For the latest PCB news and information, visit: PCB007.com

SALESPERSON WANTED • MAINLAND SOUTH CHINA

Work where you live!

The I-Connect007 China team is seeking an experienced salesperson to generate and manage a revenue stream for our Chinese publications.

Key Responsibilities include:

- Sell advertising contracts for monthly magazine
- Develop and cultivate new business
- Keep timely and accurate records
- Generate and follow up on all leads
- Manage contract renewals
- Account management: work with local and international team to provide customer support
- Phone and email communications with prospects
- Occasional travel

Qualifications

Successful candidates should possess a university degree or equivalent, experience with managing and cultivating leads, projecting, tracking and reporting revenue. We are looking for positive, high-energy candidates who work well in a self-managed, team-based, virtual environment.

Compensation

This is a base salary-plus-commission position. Compensation commensurate with experience.

Requirements

- Must be located in China Mainland, South China area preferred
- Good command of Chinese language, proficient with English speaking and writing
- Able to follow established systems and learn quickly
- Able to maintain professional external and internal relationships reflecting the company's core values
- 2-5 years' sales experience
- Experience with Microsoft Office products
- Must be highly motivated and target-driven with a proven track record for meeting quotas
- Good prioritizing, time management and organizational skills
- Create and deliver proposals tailored to each prospect's needs
- Experience in the electronics industry desirable

QUALIFIED CANDIDATES: CLICK HERE TO APPLY

I-Connect007
GOOD FOR THE INDUSTRY

I-Connect007 pcb007中国 线上杂志 CHINA MAGAZINE

I-Connect007 pcb007中国 每周通讯 WEEKLY NEWSLETTER

WWW.ICONNECT007CHINA.COM

ACE
ACCURATE
CIRCUIT
ENGINEERING

PCB Assembly Supervisor—full time Accurate Circuit Engineering—Santa Ana, CA

Position Summary: Responsible for all assembly processes to ensure continued growth as directed by management.

Essential Job Functions:
- Create, implement, and supervise in-house manufacturing facility
- Recruit, hire, train, and supervise assembly floor personnel
- Extensive hands on experience with all aspects of PCB assembly
- Understanding of IPC-A-610 standards
- Research and acquire additional assembly resources
- Gather data on product shortages, lead times, price changes, etc.
- Coordinate the assembly activities with sales to ensure 100% on-time delivery
- Create, implement, and supervise daily quality processes to ensure 100% accuracy
- Document, monitor and review progress of the business unit
- Respond to internal and external customers in a timely manner
- Coordinate walk-through, site audits, etc.

Qualifications:
- Minimum 3 years as operations supervisor of electronics assembly house
- 5+ years' experience in the electronics industry
- Previous experience as a quality or operations supervisor preferred
- Ability to solve practical problems using pre-established guidelines
- Strong facility in Microsoft Office applications
- Excellent verbal and written communication skills
- Ability to work with people of diverse backgrounds
- Highly organized/excellent time management skills
- Ability to perform at the highest level in a fast-paced environment
- Valid California driver's license.

apply now

ACE
ACCURATE
CIRCUIT
ENGINEERING

PCB Process Planner

Accurate Circuit Engineering (ACE) is an ISO 9001:2000 certified manufacturer of high-quality PCB prototypes and low-volume production for companies who demand the highest quality in the shortest time possible. ACE is seeking a skilled individual to join our team as a PCB process planner.

Responsibilities will include:
- Planning job travelers based on job release, customer purchasing order, drawings and data files and file upon completion
- Contacting customer for any discrepancies found in data during planning and CAM stage
- Consulting with director of engineering regarding technical difficulties raised by particular jobs
- Informing production manager of special material requirements and quick-turn scheduling
- Generating job material requirement slip and verify with shear clerk materials availability
- Maintaining and updating customer revisions of specifications, drawings, etc.
- Acting as point of contact for customer technical inquiries

Candidate should have knowledge of PCB specifications and fabrication techniques. They should also possess good communication and interpersonal skills for interfacing with customers. Math and technical skills are a must as well as the ability to use office equipment including computers, printers, scanners, etc.

This position requires 3 years of experience in PCB planning and a high school level or higher education.

apply now

ventec
INTERNATIONAL GROUP
騰輝電子

Ventec Seeking U.S. Product Manager for tec-speed

Want to work for a globally successful and growing company and help drive that success? As a U.S.-based member of the product and sales team, your focus will be on Ventec's signal integrity materials, tec-speed, one of the most comprehensive range of products in high-speed/low-loss PCB material technology for high reliability and high-speed computing and storage applications. Combining your strong technical PCB manufacturing and design knowledge with commercial acumen, you will offer North American customers (OEMs, buyers, designers, reliability engineers and the people that liaise directly with the PCB manufacturers) advice and solutions for optimum performance, quality and cost.

Skills and abilities required:

- Technical background in PCB manufacturing/ design
- Solid understanding of signal integrity solutions
- Direct sales knowledge and skills
- Excellent oral and written communication skills in English
- Experience in making compelling presentations to small and large audiences
- Proven relationship building skills with partners and virtual teams

This is a fantastic opportunity to become part of a leading brand and team, with excellent benefits.

Please forward your resume to jpattie@ventec-usa.com and mention "U.S. Sales Manager—tec-speed" in the subject line.

www.venteclaminates.com

apply now

ARLON

Arlon EMD, located in Rancho Cucamonga, California is currently interviewing candidates for **manufacturing** and **management positions.** All interested candidates should contact Arlon's HR department at 909-987-9533 or fax resumes to 866-812-5847.

Arlon is a major manufacturer of specialty high performance laminate and prepreg materials for use in a wide variety of PCB (printed circuit board) applications. Arlon specializes in thermoset resin technology including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, high density interconnect (HDI) and microvia PCBs (i.e., in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001: 2008 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customer's requirements.

more details

Altium

Application Engineer

The application engineer is the first contact for our customers who have technical questions or issues with our product. We value our customers and wish to provide them with highest quality of technical support.

Key Responsibilities:

- Support customer base through a variety of mediums
- Log, troubleshoot, and provide overall escalation management and technical solutions
- Create various types of topic based content, such as online help, online user guides, video tutorials, knowledge base articles, quick start guides and more
- Distill complex technical information into actionable knowledge that users can understand and apply
- Continually develop and maintain product knowledge

Requirements:

- Understanding of EDA electronic design software, schematic capture and PCB layout software
- Bachelor's degree in electronics engineering or equivalent experience
- Sales engineering and/or support engineering experience
- Circuit simulation and/or signal integrity experience
- Understanding of ECAD/ MCAD market segments
- Understanding of micro controllers, SoC architecture and embedded systems market
- Database experience preferred (i.e., MySQL, PostgreSQL, Microsoft Access, SQL, Server, FileMaker, Oracle, Sybase, dBASE, Clipper, FoxPro) etc.
- Experience with PLM/PDM/MRP/ERP software (Program Lifecycle Management) preferred
- Salesforce experience a plus

Salary based upon experience. Comprehensive benefits package and 401k plan. Openings in USA, UK, and Germany.

For more information, contact Altium.

apply now

CHEMCUT

BOUNDLESS INNOVATION | UNBEATABLE PRECISION

Field Service Technician

Chemcut, a leading manufacturer of wet-processing equipment for the manufacture of printed circuit boards for more than 60 years, is seeking a high-quality field service technician. This position will require extensive travel, including overseas.

Job responsibilities include:

- Installing and testing Chemcut equipment at the customer's location
- Training customers for proper operation and maintenance
- Providing technical support for problems by diagnosing and repairing mechanical and electrical malfunctions
- Filling out and submitting service call paperwork completely, accurately and in a timely fashion
- Preparing quotes to modify, rebuild, and/or repair Chemcut equipment

Requirements:

- Associates degree or trade school degree, or four years equivalent HVAC/industrial equipment technical experience
- Strong mechanical aptitude and electrical knowledge, along with the ability to troubleshoot PLC control
- Experience with single and three-phase power, low-voltage control circuits and knowledge of AC and DC drives are desirable extra skills

To apply for this position, please apply to Mike Burke, or call 814-272-2800.

apply now

BLACKFOX
Premier Training & Certification

IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

apply now

Prototron Circuits

Experienced PCB Sales Professional

With more than 30 years of experience, Prototron Circuits is an industry leader in the fabrication of high-technology, quick-turn printed circuits boards. Prototron of Redmond, Washington, and Tucson, Arizona are looking for an experienced sales professional to handle their upper Midwest Region. This is a direct position replacing the current salesperson who is retiring after spending ten years with the company establishing this territory.

The right person will be responsible for all sales efforts in this territory including prospecting, lead generation, acquiring new customers, retention, and growth of current customers.

This is an excellent opportunity for the right candidate. Very competitive compensation and benefits package available.

For more information, please contact Russ Adams at 425-823-7000, or email your resume.

apply now

Process Engineer (Redmond, Washington)

With more than 30 years of experience, Prototron Circuits is an industry leader in the fabrication of high-technology, quick-turn printed circuits boards. We are looking for an experienced PCB process engineer to join the team in our Redmond, Washington facility. Our current customer base is made up of forward-thinking companies that are making products that will change the world, and we need the right person to help us make a difference and bring these products to life. If you are passionate about technology and the future and believe you have the skills to fulfill this position, please contact Kirk Williams at 425-823-7000 or email your resume.

apply now

Events

IPC Calendar of Events, click here

SMTA Calendar of Events, click here

iNEMI Calendar of Events, click here

PCB007 Calendar of Events, click here

productronica 2017
(IPC Committee meetings held in conjunction with productronica)
November 14–17, 2017
Munich, Germany

HKPCA/IPC International Printed Circuit & South China Fair
December 6–8, 2017
Shenzhen, China

47th NEPCON JAPAN
January 17–19, 2018
Tokyo Big Sight, Japan

DesignCon 2017
January 30–February 1, 2018
Santa Clara, California, USA

EIPC 2018 Winter Conference
February 1–2, 2018
Lyon, France

MD&M West
February 6–8
Anaheim, California, USA

IPC APEX EXPO 2018 Conference and Exhibition
February 27–March 1, 2018
San Diego, California, USA

China International PCB and Assembly Show (CPCA)
March 20–22, 2018
Shanghai, China

KPCA Show 2018
April 24–26, 2018
Kintex, South Korea

Thailand PCB Expo 2017
May 10–12, 2017
Bangkok, Thailand

Medical Electronics Symposium 2018
May 16–18, 2018
Dallas, Texas, USA

JPCA show 2018
June 6–8, 2017
Tokyo, Japan

PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

SALES: **ANGELA ALEXANDER**
(408) 489-8389; angela@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

EDITORIAL:
MANAGING EDITOR: **PATRICIA GOLDMAN**
(724) 299-8633; patty@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

CONTRIBUTING TECHNICAL EDITOR: **HAPPY HOLDEN**
(616) 741-9213; happy@iconnect007.com

MAGAZINE PRODUCTION CREW:
PRODUCTION MANAGER: **SHELLY STEIN**

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **MIKE RADOGNA, SHELLY STEIN, TOBEY MARSICOVETERE**

INNOVATIVE TECHNOLOGY: **BRYSON MATTIES**

COVER: **SHELLY STEIN**
COVER IMAGE: **© ROLFFIMAGES, ADOBE STOCK**

I-Connect007 Presents the pcb magazine

The PCB Magazine® is published by BR Publishing, Inc., PO Box 50, Seaside, OR 97138

November 2017, Volume 7, Number 11 • The PCB Magazine© is published monthly, by BR Publishing, Inc.

ADVERTISER INDEX

Coming Soon to *The PCB Magazine:*

DECEMBER:
Thermal Management
Keeping off the hot seat.

JANUARY:
Equipment
Choosing the right equipment for your current and future needs, with a special IPC APEX EXPO 2018 pre-show section.

FEBRUARY:
Who's Your Customer
Knowing who your customers are, both internal and external.