I-Connect007
AUGUST 2018

PCB007 MAGAZINE


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PCB007 MAGAZINE

Walking the Fine Line of Reliability

Electronics are no longer an occasional luxury, they are an integral and constant part of our daily lives, from automotive, medical and aerospace electronics to cellphones and alarm systems. Reliability has become ever more critical, and our industry wants to deliver. This month, our experts provide their perspective on the evolution of reliability across sectors.

PCB007 MAGAZINE

COLUMNS:

HIGHLIGHTS:

DEPARTMENTS:

SHORTS:

IT-988G SE / IT-988G

IT-988G

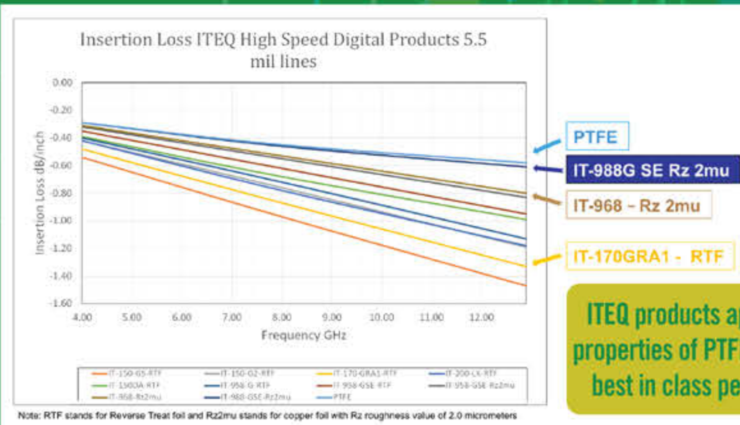
- Halogen Free
- Tg = 190° C
- Td = 405° C
- Dk = 3.46 @10GHz*
- Df = 0.0025 @10GHz*
- Available with low Dk Glass - IT-988G SE

IT-988G SE

- Halogen Free
- Tg = 190° C
- Td = 405° C
- Dk = 3.24 @10GHz*
- Df = 0.0014 @10GHz*

Ultra high speed > 56 Gbps per channel, NRZ (PAM2), PAM4 applications

Insertion Loss - Measured



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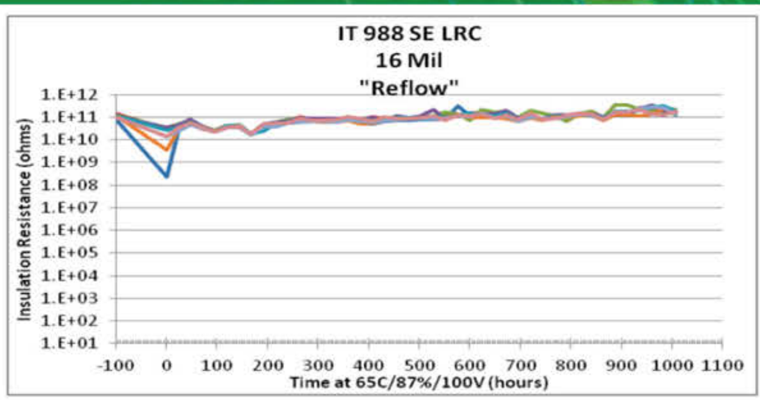
Sequential Lamination

7 Lamination cycle data

Lamination	DMA	DSC	TMA	T300 with CU	Solder Dip PCT: 1h @ 121°C	Td 2wt% / 5wt%
1	213	187 / 187	182	> 60	> 60	408 / 435
2	216	194 / 199	193	> 60	> 60	41 7/ 438
3	214	186 / 192	185	> 60	> 60	417 / 442
4	216	193 / 194	184	> 60	> 60	424 / 443
5	217	194 / 199	190	> 60	> 60	418 / 442
6	218	191 / 197	188	> 60	> 60	405 / 436
7	218	190 / 197	194	> 60	> 60	425 / 444

No themal degradation observable after 7 lamination cycles

HDPUG MRT-6 LRC CAF Data



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Reliability Takes on a New Urgency

Patty's Perspective
by Patty Goldman, I-CONNECT007

In the last year or so, I believe our industry definition of reliability has changed. Consumers wanted a reliable car that wouldn't break down on the road; a computer that wouldn't crash; a phone network that wouldn't drop our calls; the plane we were hurtling across the sky in to stay in the air and land safely, with the wheels down. In retrospect, those seem rather simple wants, and the industry certainly wants to deliver.

But with the advent of the autonomous vehicle and all that has been written and discussed about it—from the "computer on wheels" concept to hacking concerns and who's responsible in a crash—I believe this has made us stop and think deeply about what reliability really means. As one of our authors points out this month, a PCB can be of highest quality, meeting the most stringent specs, but in the end the machine it goes into may not be reliable and in fact the board itself may fail down the road. How can we ensure that the PCBs we make are reliable and how can we feel confident that reliability will carry through to the final product—for the lifetime of that product? This month, our experts provide the latest information to help with that.

We begin this month with a discussion on reliability with Colonial Circuits, a PCB manufacturer that builds mostly military boards. Increasing demands regarding feature sizes, material types and preciseness only highlight the need for more communication between designer and fabricator, as well raw materials suppliers, to ensure reliability.

Next, Denny Fritz, recently retired from SAIC, brings a DoD perspective to the reliability discussion. He enlightens us on the workings within the defense community and the need for updated measures of reliability.

Dovetailing with Fritz's article is an in-depth report by Happy Holden on the IPC High-Reliability Forum for Mil-Aero and Automotive Sectors, held in Baltimore, Maryland in May. Several companies reviewed their testing of failed HDI microvias while other speakers discussed the state of the PCB industry in the U.S. This is important information that Happy has brought back to our readers.

Getting down to the nitty-gritty, Super Dry's Rick Heimsch provides practical and useful guidelines on bake-drying of PCBs based on the type of laminate. His information is based on the updated IPC guidelines and includes cautions regarding various final finishes.

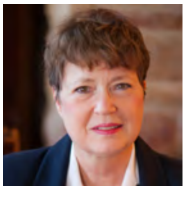
I-Connect007's old friend, Uyemura's George Milad, returns this month with his clear understanding of the mechanism for nickel corrosion in deposits of the ENEPIG final finish, along with the best ways to prevent it and ensure a reliable final finish.

Regular columnist Mike Carano, RBP Chemical Technology, brings us a cautionary "tale" relating to zinc treatment on copper foil, which enhances the copper-resin bond strength. The protruding "tail" of zinc after desmear can be a potential cause of PTH failures. Read on to get the whole tale.

Taking an overview approach, PNC's Sam Sangani provides a primer on reliability and quality in the PCB facility. He reviews critical areas or components to building a reliable product.

And lastly, Tara Dunn, Omni PCB, enlightens us on Mina, an advanced surface treatment for soldering to aluminum. This may not sound like something for PCBs…or is it? As the various segments of electronics begin to converge towards ever-smaller features, more unusual applications, and ever-more complicated thermal requirements, who is to say where this will fit into the PCB portfolio? At any rate, it is worth learning about.

Next month we will be exploring another up-and-coming subject: mSAP and SLP. Or, modified semi-additive processes and substrate-like PCBs. I'm still learning about these myself and looking forward to what our authors will reveal. See you then! Oh, yes… Subscribe! **PCB007**



Patricia Goldman is managing editor of *PCB007 Magazine.* To contact Goldman, click here.

Smarter, Safer Bridges with Sandia Sensors

Along with flying cars and instantaneous teleportation, smart bridges, roads and subway lines that can send out warnings when they're damaged are staples of futuristic transportation systems in science fiction.

Sandia National Laboratories has worked with Structural Monitoring Systems PLC, a U.K.-based manufacturer of structural health monitoring sensors, for over 15 years to turn this science fiction into science fact. They outfitted a U.S. bridge with a network of eight real-time sensors able to alert maintenance engineers when they detect a crack or when a crack reaches a length that requires repair.

Sandia Senior Scientist Dennis Roach will present his team's work at the ninth International Conference on Bridge Maintenance, Safety and Management. His presentation will include data on this trial bridge, a general assessment of the sensors used and his proposal for how to make structural health monitoring more routine in transportation infrastructure.

Source: Sandia National Laboratories

Photo: Mechanical engineer Stephen Neidigk positions a Comparative Vacuum Monitoring sensor on a bridge. In his other hand is the control system that periodically checks the sensor and a wireless transmitting device to autonomously alert the maintenance engineers if it detects a crack. (Photo by Randy Montoya)

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Building a Better Board: It Always Comes Back to Communication

Feature by the I-Connect007 Editorial Team

For our experts meeting on this month's theme of reliability, we reached out to Colonial Circuits and asked them to participate in a conference call with our I-Connect007 editorial team consisting of Dan Feinberg, Andy Shaughnessy, Patty Goldman, and Happy Holden. Joining the call from Colonial Circuits was Mark Osborn, president and CEO, Kevin Knapp, quality manager, and Rodney Krick, manufacturing manager.

Dan Feinberg: Gentlemen, we really appreciate your participation. Mark, you and I have talked about the optimism of the industry with things that are going within it. There seems to be more optimism and general optimism in business that I've seen perhaps since the late '60s, early '70s.

Mark Osborn: I agree. We saw a slight dip in business last year, mainly because a key customer's program ended. The new design switched from rigid to flex, and due to the quantity needed, the customer required the flex to be supplied on reels, something we are unable to do. Fortunately, today's market is one where new opportunities are presenting themselves daily.

Feinberg: That's great to hear. You never like to turn work away.

Patty Goldman: Does that mean you can kind of pick and choose your customers now?

Osborn: We're getting quite a mix from the same customer. It's the technology that's taking so much time to fabricate.

Feinberg: Mark, I know you have had some issues with regard to reliability and materials, as well as counterfeit components. So, my question for you is, what reliability trends are you seeing regarding requirements from customers, especially over the last few years?

Kevin Knapp: I'm in the quality world here. We're seeing a lot of dimensions going out

Figure 1: Colonial Circuits is located in Fredericksburg, Virginia.

four and five decimal places, where three was about it in the past. It's getting to be a lot more particular. We're also seeing parts from several years ago that have been in stock for two to three years, and then I'll scrutinize them and find that what was acceptable then may or may not be today. I think it's changed that much. And the other thing we are seeing is more customers sending parts out for third-party testing, just like you would for space flight prior to being accepted.

Osborn: Most of that arises when they've had a manufacturing problem, not necessarily with our boards, but with one of the other suppliers.

Feinberg: I think that going from two decimal places to five decimal places, or three to five, that's huge. That's a quantum jump in specs.

Osborn: It is. But as you know, the trend is to build smaller, and it must meet certain criteria, and with the new components, features have really shrunk. But we're here taking on huge challenges every day knowing that next week a whole new set of challenges will materialize.

Feinberg: I know reliability trends relate to specs on what customers are demanding of you as a fabricator, but what are you seeing as far as raw material challenges, and what are you then passing on to your suppliers of raw materials as far as demands?

Osborn: The answer to that question is the ability to get laminate. In many cases we can, and I'm sure you have heard of the horror stories with Rogers. When they're out to 30, 40, or 50 days on delivery and you're in a quick-turn market, that makes it extremely difficult to compete. We just tried a new material at a customer's suggestion called Astra, sold here in the states by Isola. But as we're learning, it has its own set of issues that we were totally unaware of because we had never used this laminate before.

As you know, Dan, the grain direction of the material plays a role in potential warpage. Colonial, for the past five years, has only purchased material with the grain in the long dimension. This time period has allowed us to build an extensive library of data on dimensional stability surrounding our standard laminates. Unbeknownst to us, the Astra is only available with the grain in the short direction, meaning we were unable to predict the outcome! After two or three unsuccessful fabrication attempts, we finally nailed it.

Even the ability to obtain regular material has proven difficult, particularily with flight work. Polyimide-aramid-NT is a popular laminate used for this application, but the 4-5 week lead time on delivery is not appealing to our better customers.

Feinberg: Where is the Astra material made?

Osborn: China.

Feinberg: Any indication that, with the demand going up, there might be some made in the U.S. again at some point?

Osborn: I hope that some of that comes back, but at this moment we're not hearing anything from our supplier.

Rodney Krick: The only thing I can offer as far as materials and what we've seen over the short term, particularly with RF, is that we have a tremendous number of different materials and the designers, I believe, don't have a good working knowledge of board manufacturing. Because we do a lot of combinations: FR-4 and Rogers; FR-4 and PTFE; and FR-4 and rigid polyimide and flex—we just get all kinds of stuff. And we make it work. We certainly go through a learning curve on some of these materials just like the Astra that Mark mentioned. It sounds as though it is a competitive material to the Rogers 4000 series, which obviously is a benefit to the board guys because right now Rogers basically has everybody stretched out, delivery-wise.

You're at their mercy to say, "Well, if we can't get it for 30 days ..." which again hurts us, but it certainly hurts the end customer as well. I think one of the other things with being a relatively small board shop is that you don't carry the muscle and the might of some of the big guys. So you don't always necessarily get that treatment and you may be dealing with drop. Earlier today when we were talking about this Astra material, and how if it's not supplied in the 24-inch grain direction we need, then we must buy full sheets of this material. I'm assuming 36 x 48 or 48 x 48. We buy it from China, freight it in, and now we have to cut it down to the size we can use. And if we do that and we only need one piece of material, but there's a lot charged for 15 pieces; you're dropping $2,500 on materials for a $1,000 order that you're trying to turn.

Feinberg: Well, that is an issue because just this one problem of raw material of laminate can actually destroy what's left of our industry in the U.S., and then what happens? Our military is going to buy circuit boards from China and who knows what's really in them, right?

Krick: Exactly.

Feinberg: The biggest challenge you're facing seems to be supply more than anything else. Is that what I'm hearing?

Osborn: Correct. From a supply standpoint, let me give you an example of the financial impact the dwindling supplier base is having on Colonial. Two months ago we were notified by our chemical supplier that we would have to replace our existing ENIG line because they were no longer going to support that particular chemistry. After shelling out over $41,000 and taking precious start-up time out of our production schedule to validate this new chemistry, I realized that this is just the beginning of changes yet to come. We are being forced to change and the word "choice" is no longer in our vocabulary. The other thing is that our supplier base doesn't have the people in the field to go into the shops anymore.

We are being forced to change and the word "choice" is no longer in our vocabulary.

Feinberg: It's not like the old days where we had salesmen who were process engineers in the field.

Osborn: Correct. Or at least if they didn't know, they had access to the information and would get it for you. But being forced to change your chemistries because your suppliers have consolidated and they're no longer going to carry the one that you've been using for 15 years, and to put that kind of money out all at one time, it's a killer and it hurts.

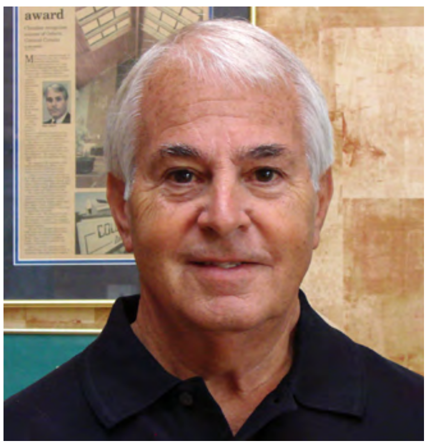
Krick: That's another one of the issues with a small shop. We have been in a couple of situations just in recent months, and to get somebody on the phone who is a knowledge base, like an applications engineer is like pulling teeth. We're kind of on the convenience tour. We're about 40 miles away from TTM Sterling, and if an AE happens to be in that facility, they may swing past for a cordial visit here but, again, we don't really carry the clout where a drill bit supplier or a chemistry supplier is going to put somebody on a plane to come in and help us out with a problem.

Feinberg: Of course, the big product that we had was dry film resist. Well, dry film resist is now selling for less than what it used to cost us to make it, and it used to be a very, very high-profit product. Now, from what I'm understanding the prices that are being paid on the retail side are far less than the manufacturing cost back in the day. So you've got to wonder how they're doing that and how they're dealing with it. Of course, the suppliers are very different and I'm sure the raw materials are different and it's just a totally different world.

Osborn: It is a different world.

Feinberg: What other reliability challenges do you have with raw materials?

Krick: To the best of my knowledge, at least for consumables coming in the door, the quality is there. They're repeatable. Thicknesses are good. Copper quality is good. The typical stuff that you used to see, such as handling scratches and packaging, I am assuming it is so automated now you generally don't see that. It comes in in a nice pretty package and it's vacuum sealed. Other than not getting it as quickly as we need to get it, I think the quality of the material has gotten tremendously better. It's a little difficult dealing with the smaller population of suppliers. It's kind of like with Insulectro buying everybody. You're dealing with a giant and being able to flex a little muscle with somebody that big. They don't always respond.



Mark Osborn

Knapp: You're talking about a lot of laminates. I was a process guy for 35 years, chemical engineering. I was on the chemistry side of things and, if we look back, we used to have a lot of options. It was a lot of 'me too,' but you had a lot of options. You remember the dry film business; there was DynaChem, Hercules and DuPont. But they're gone. You don't have a lot of options, and, as Mark alluded to earlier, it looks to me like there's not a tremendous amount of R&D going on in the process world from our vendors. Although, occasionally, they come out with a solution desperately searching for a problem.

Feinberg: Let's swing off just a little bit off from the raw materials. The finished parts that you sell are 100% circuit boards but not assembled devices. Obviously, the quality of the circuit board you send customers is good, but what about the quality of their finished device? Mark, you and I have had some discussions with various customers and various agencies about counterfeit components. Are you hearing any more about that?

Osborn: No, it has kind of died down.

Feinberg: Three years ago, that was not what we were hearing. So, I think that's probably good news.

Osborn: There was a lot of hype and I know it was going on, but I don't believe it was really to the degree that was expressed at that time, or at least not with our customer base.

Feinberg: What can the designers do to help improve reliability?

Osborn: If our engineering manager were here right now he would tell you that he'd like all the designers to come here and spend a week with him working on one of their designs so that he could show them exactly where they are making our life difficult. That to me is probably the biggest obstacle in getting good product out the door: getting it out of engineering right the first time on time. We're finding that we have to go back and educate the designers who are using great software but have no knowledge of how boards are built. That's a big obstacle right now.

Andy Shaughnessy: In light of that, what advice would you have for the designers?

Osborn: They need to come visit the board shops, not the contract manufacturers. The designers need to sit down and look at, first, what we can build or what that board shop is capable of, and then let the board shop critique their designs. This lack of communication is the big issue here, and nobody has time or money in their budgets to change this culture.

This lack of communication is the big issue here, and nobody has time or money in their budgets to change this culture.

Shaughnessy: Is it just the data coming in? We always hear that most of the time when you get a new customer, the data that comes in is a mess, until you get them trained.

Osborn: Sometimes, but not all the time. Depends on what kind of rush they are in; if they know you can fix it, they'll continue to send it to you that way knowing that you are going to fix it. That's not the right approach, in my opinion.

Krick: I'll add to Mark's comments as to what I have seen here. I think designers tend to not live in the real world, and I qualify that because even internally here, when you look at a high-resolution monitor that has a one-mil space or a one-mil line, you think, why can't we do that? Well, the reality is that out in the real world that's not doable. I think, when the designers look at what they're developing, it's based on their theoretical end unit, not necessarily what it takes to get there. We've done some pretty crazy stuff here that was pretty far outside of the box.

We have some customers that enjoy the feedback and learn from the feedback, but—I've been building boards for years and I know how to build them—for the life of me, I don't know why they do what they do. It would be a benefit to me to see how the designers come up with their designs. I think the same thing is true with the designers and board shops because they don't really have an idea of what manufacturability really equates to.

Knapp: Just to piggyback on that, there's no manufacturing tolerance to variation built-in to the high-resolution monitor on a desk. There is manufacturing tolerance built in these boards that may not be understood.

Krick: That's a great point. I was just having that dialogue with some of our internal people here, trying to educate, and even to Kevin's point, the thought is that when you've spent big money on that CNC drill and that drill program tells that hole to go to X1Y1, that's where you expect it to be. Well, you don't live in that true-position world. There's always some degree of variability, and I don't think the designers see that either. We've seen designs that have six-mil holes that are spaced on a three-mil grid or something and they don't understand why we can't do that. Oh, and it's a 100-mil thick board.

Feinberg: I think getting this word out is of great value.

Krick: I agree. One other comment I would like to make goes back to being a small shop. We don't have the resources to afford the half a dozen method engineers to be able to take raw data, clean it up, go through designer manufacturability rules, go back to the customers, make sure that they know what they've got, make sure we know what we've got, and, oh yeah, "We need the parts delivered in two days." That's kind of where we end up hitting the brakes.

If we were talking 20-mil vias, 10 x 10 (line/space) double-sided stuff, then this conversation is a moot point, but some of the jobs that we take, and we've hit it out of the park, take a lot of what I agree with Kevin is tribal knowledge as to being be able to build this stuff. But it's hands-on by everybody in the building to get it through with kid gloves. It's not just throwing it to the floor and go.

Osborn: And the bottom line is that the R&D is being done in-house now at our expense.

Patty Goldman: And it only works for that job?

Krick: That is correct. Usually you're right. What you learn on one part may not necessarily apply on another.

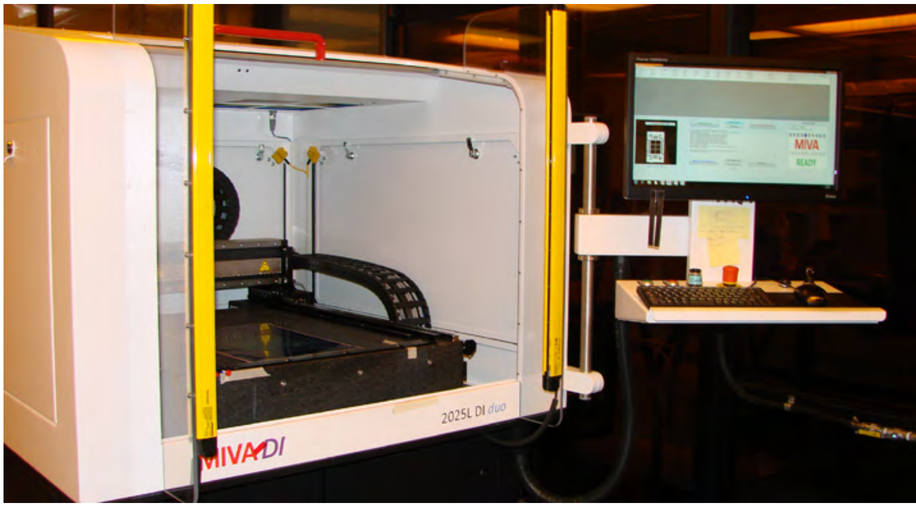


Figure 2: Colonial's new Miva Quad wave LED direct imager is capable of imaging down to 1 mil (25 µm) with conventional or LDI photoresists. Throughput has been greatly enhanced with innerlayers, outer layers and solder mask without sacrificing printing quality.

Osborn: But I still go back to communication. As a matter of fact, I was told this morning we have an engineering group that wants to come down and tour our facility next week. And the reason that they want to come down is that they are experiencing some of these problems with some of their other suppliers, and since we are their closest board shop, they want to visit to discuss the likes and dislikes of their supplied data. This bit of openness unfortunately is not common across the customer base.

Krick: I think we're hitting some degree of limitation of equipment and materials. We've seen that this week doing sub-three and three repeatedly and robustly with good yields. We've got reasonably state-of-the-art drills. We've got state-of-the-art printers. We've got state-of-the-art etchers. We've got what I certainly consider state-of-the-art capability and yet, you sit here and go through the art and data Mark was alluding to and it's a failure and a failure and a failure. At some point, you must go back to you suppliers and say, "Two-mil resist ain't cutting it anymore" or again, the designers don't understand.

Knapp: We're also trying to run state-of-the-art work with materials that are the same materials that we were using 10 years ago to do what was state-of-the-art then.

Osborn: And we're always looking for state-of-the-art employees.

Feinberg: That's true. If you think about it, back in the day there were 25 circuit board companies within 100 miles of you. How many are there now?

Osborn: Within 100 miles? Maybe four. It's a changing world, and it's still a lot of fun, but it is a challenge.

Feinberg: One of the definitions of fun is meeting a challenge.

Osborn: Right. That sense of satisfaction that you get at the end of the week after shipping good product on time. The customers are happy, and one thing you can count on is that this cycle will repeat intself the following Monday. When things go south, the customers will let you know. That's where the communication comes in.

Feinberg: Before we wrap up a little bit on reliability, reliability combined with quality are kind of different. You can meet the quality spec. Quality is meeting the requirements of the customer, but it still may not give you a reliable product. So how do you see the quality specifications that you're getting from your customers, and how does that compare to what they should be specifying to get the reliability that's needed? And it could be either way. It could be that they're specifying too high a quality to make something that's a 15- or 20-mil line and space battery charger, or where they're not specifying enough quality to meet the 2-mil line and space for an 8K monitor.

Osborn: Right off the bat, I'm going to say communication; unless you know what those circuit boards are going into and what the product is, you have no idea about reliability other than you have the spec that you built it to. And that goes back to the lack of communication. This information is not generally shared, particularly with the contract manufacturers. They prefer not to tell you who the end customer is. They throw up all kinds of roadblocks and excuses for why they are unable to assist once you discover that their files are corrupt, incomplete, or poorly designed. Perhaps a better word to explain it is Trust, or lack of! Colonial does have a few customers who are contract manufacturers that are willing to work closely with us to take care of the customer.

Krick: I've asked certain designers and customers what these parts go in and Mark is correct. Literally it's a "Well if I tell you, I'd have to kill you" type of an environment. We also know here that we deal with mostly military and it could be guidance systems for missiles or going up in space. If I was an end user that was putting my signature on the approval for this part in a $35 million satellite that got off the launch pad and blew up, I'd scrutinize it pretty heavily too. This isn't 10 x 10 going in a transistor radio. This is pretty high-end stuff that has people's lives and potentially innocent people's lives resting in your hands to provide a reliable product.

Can it go too far? We deal with some space flight folks where you stand back and say, "Really? A tenth of a mil in etch factor and you're going to shoot me down for that?" If this is going up in a shuttle or something similar, I would like to know that the shuttle is going to make it to destination, not necessarily turn around and come right back down to earth.

Knapp: I have a lot of thoughts on this from the quality point of view. The first one is, and I've had this conversation with Randy Cherry from the IPC, in many cases the soft specs have not kept up with board technology. IPC-6012 is silent or very vague on several things that are not middle-of-the-road technology. Another issue that we see, and I am sure every other board shop sees too, is what the print notes say and what the engineer meant may not be quite the same thing. There needs to be standardization in terminology. A recent example is a board that wanted 0.062 plus or minus 10%. We kind of judged that over laminate. He judged it overall. Neither one of us was probably 100% right or 100% wrong. We didn't talk to each other, which goes back to Mark's point. We're going to have that corrected now, but we both learned something.

One of the other things that occurs is there's not necessarily universal buy-in to using the

Figure 3: Colonial's newest electrical tester, an atg A7a, utilizes eight flying probe test heads for a wide variety of advanced, high-speed electrical test techniques, with an auto-load/unload system for true "lights-out testing."

soft specs as they're currently written, and the best example is that there's a lot of work that we do for space flight. We're up to IPC-6012DS, with an S for space flight addendum. But I'd say close to half of the space flight work that we do is specified to 6012B. That's about two generations back. And they're brand new designs. There's obviously some discomfort out there with the specs, with the requirements, and with the designs. Ultimately, quality is: what does the customer need? But conveying exactly what he needs may not be universal here.

Osborn: Just to add to what Kevin said, even though the via fill process has been around for several years, not all designers are on the same page. We still see new designs specify via fill holes with no mention of cap plating. In the past that is exactly how we manufactured the boards until the customer experienced massive fallout during assembly and suddenly we're open to discussion. It is amazing how much progress can be made when you sit down and talk.


Kevin Knapp

Feinberg: Mark, that brings up a very good point. Standards and specifications, gee, don't we have the IPC for that? Do we need a standard or specification on things like filling the via?

Goldman: Remember that IPC is just a facilitator for standards; it's the people from companies in those meetings and who are developing the standards. But the lag time in specifications is not a new or unrecognized problem. The trouble with industry standards, though, is they take time to develop and review, and in the end, everybody must agree, there needs to be a consensus.

Feinberg: I have two other basic questions for you guys. We're seeing a tremendous advancement in computerization of process control, computerization of manufacturing with quantum level computing coming. Are you starting to see any higher role in computerization of process control at your own company?

Knapp: Computerization makes process control a whole lot easier in the fact that usually there is a key or a password that the guy setting up the process set it up that way and nobody else has a chance to change anything. In days gone by, everything had knobs and toggle switches and you had to rely on the operator to be enough of a craftsman and have enough integrity to do things correctly. You don't have a lot of those people anymore. You must basically use computerization to lock out the happy fingers which allows you to have process control. It doesn't necessarily enhance it. It just allows you to have it.

It's the consistency. Back in our younger days, I remember if you had three shifts, you had three etchers. They would all give you an adequate product, but they would all go about it just a little different. If you had three shifts, you had three copper platers. They all gave you a decent product but they all may have gone about it a little differently. But there was a craftsmanship there. It isn't here anymore. You must maintain that consistency. And what we considered consistent 20 years ago is going to give you nothing but scrap today. It's just so much tighter, but you must have that, and I don't think you can rely on that from an individual point of view anymore.

Krick: I think that for the volume that we do here and the small fortune we avoid in having processes and/or equipment that requires that level of technology, I'd rather have 25 well-trained craftsmen to build it. We're not a bathtub shop, by any means, but we pull off what we pull off because of time and tenure from the people on the floor. Even our plating line is controlled by a program, but they still need to rely on that operator to follow the program. CNC drills have been around 100 years, but everybody knows that it's easy enough to hit the cycle start button and change the bit. We don't have that level of automation here. We're more of a human-based than machine-based operation.

I can say I don't think we can compete technologically with the big guys, but we pull off some pretty good stuff for what we do. And that's kind of a nice tip of the hat to the people. We're very good at understanding our technological boundaries and investing in equipment that we need to get the job done. We've spent many years here using contact printers and I couldn't even tell you the difference that a direct imager made when we bought that machine. And now we have two.

Knapp: Let me take this just down a little different path, although it's still process control. Right now, there's not a place you can go in our shop that an operator doesn't have at his fingertips access to any production control information he needs, information regarding what his procedure tells him to do, and pretty much any information that he needs. He doesn't have to go hunting down the production control guy to ask about this job. He doesn't have to hunt down the supervisor to ask, "How am I supposed to do this?" All that information is right there at his fingertips. There is a lot of time saved and a lot of misinterpretation avoided.

Feinberg: What do you see are the major roadblocks for a company like Colonial Circuits to continue to be a contributing and key part of the American circuit board fabrication industry? What do you see as the major roadblocks to continuing and growing a little bit?

Osborn: I think finding the right qualified people with the right attitude. We need to get through to our youth that a career in manufacturing could be a great lifetime move. I've got a junior in college working here for the summer. He's going to be an engineer and he happens to be a personal family friend. He's been working with Rodd's son, back in manufacturing for nearly three weeks and yesterday I asked him how he liked it and I was amazed at how he responded. He said, "You all do a lot of neat things here. I really enjoy this job." I realize this is just a summer internship but receiving his positive response gives me hope about our industry's future.

Colonial is only 50 miles south of Washington, D.C. I believe about 60% of the people who live in our area work for the government in one way or the other. They're either in the military or they work in Washington, which means they commute. This makes it difficult at times to find that craftsman or that candidate for craftsman to bring into the board shop. But when you do find them, you want to keep them. That to me is the biggest obstacle. But on the other hand, if you don't have any laminate to make the boards with, it's a moot issue (laughs).

Krick: Certainly, from the manufacturing perspective, we have had many people come in and interview and we have hired many. Some come in right off the street and show initiative and they now have pretty good tenure here, multiple years of tenure. I think even with this area, if we were to hire people off the street and what they would be willing come in and do manufacturing work for, we'd go out of business. There's so many people that come in the door and in some cases, they're asking $16 or $20 an hour to start with no education, with no background, with no nothing. There's a McDonalds up the street and they're paying people $15 an hour. How do you compete and remain profitable?

Again, kids just aren't as hungry as we were 40 years ago. There's a few. You'll find them but it's rare now. I think it's changed dramatically just in what level of income they feel they need to be satisfied. These kids are coming in the door and they want six figures a year. They want an office. They want a chair. They want a PC. They want their phone. The less than glamorous days of getting your hands dirty and smelling chemistry and all the rest of it, they're just not interested in something like that.

Knapp: I've been here almost 25 years and I'd like some of that stuff. If you think back to the days where we got into this business, there were some older folks up at the top. They had supervisory engineering positions, process positions, and that was something that a lot of us aspired to. There was always a young crop of hungry, in Roddy's terms, engineers, just good people wanting to move up. Suddenly, there's not that crop any more waiting to come right in behind folks like us that are getting toward the end of the train ride. There's a problem with all the tribal knowledge walking out the door and there aren't any people to convey that knowledge to, that are all that interested.

Osborn: I would like to add to that. One of the things I've been a real proponent of is training. As you're aware, at the federal and state level now they have programs for training, improving your skills. But unfortunately to get some of this grant money they want to funnel it through the community colleges and then the colleges will train the student. I've been fighting to have that grant money go directly to the company that's hiring these newbies and use that to facilitate their salary for a trial period, whether it's 90 days, six months or a year. And then once that trial period is over, if they cut the mustard, then the company takes on the total financial obligation and even gives a raise!.


Rodney Krick

Krick: When I was climbing up through the ranks there were so many opportunities to go up the ladder, and that's how you did it. It was time and tenure. The more you learnt, if you kind of hit a top ceiling at the place you were at, pull your resume around and throw a dart at a state. There were places you could go that you never even would have thought about. It's so limited now and trying to encourage kids to look at this as a career, certainly a 35-40-year career, that's a hard sell.

Knapp: They begin to equate manufacturing to their dad and granddad who worked in the factory, or in the coal mine, and there's a difference.

Krick: There's just not a hunger there, not for this type of an environment, and I don't if anybody could really change it. I've told many people coming in here for interviews that to build boards you don't need to be a road scholar. You need to get it, take it in and if you understand it you can have a very good career doing it whether it's here at Colonial, TTM, or any of the other ones that are out there. But a lot of younger people don't get it. They look at it as just kind of a medial task, maybe one notch above cleaning restrooms but not much more than that.

Knapp: There is such a wealth of knowledge and information and just creativity that's available in this business if you want to just reach out and grab it. We still do things here that we're told can't be done, even when people are watching us do it and it's not like that everywhere.

Holden: Well, that's great. I've got a couple questions before we run out of time. I was just at the IPC reliability forum for milaero and automotive in Baltimore. One of the things that came out is the new reliability test that they put in place last September. The TM 650 2.6.27A in which the boards must pass six reflows at a peak temperature 260°C but being monitored by a four-wire Kelvin bridge while the thing reflowed. Are you doing that test, or have you seen that requirement?

Osborn: No, but I was also at that conference and heard the same discussion.

Knapp: This takes us almost full circle to where we began this. How does that test line up with the capabilities of that material to begin with?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Does it exceed the capabilities of the material? Now we go to UL. We're not allowed to do that under UL.

Holden: It has nothing to do with the material. It has everything to do with soldering and the number of reflow cycles a board is going to see, and the consensus was that you can throw away all the MIL-spec thermal cycling and the IST and the other thermal cycling—they don't find a defect on these microvias. But at least six passes at this 260°C peak, unless you're using bismuth solder and then the spec is 230°C peak instead of 260°C for lead-free, but you have to be monitored by a four-wire system because a crack and a split can occur and then it self-heals itself and then will only fail in the field a couple years later.

We put out a white paper called IPC-WP-023. Have you seen that or read that white paper? It's about 30 pages. It's about the hidden reliability threats in microvias.

Osborn: To be honest with you, no. Unless it's required by our customers, we really wouldn't explore that on our own.

Holden: It's funny, even one level deep microvias are failing the test. The data is bad because as much as 40% of milaero boards are now being thrown away because they are failing the reliability testing. The reason we called the conference was because the fabricators can't afford to have an overage of 40% to meet the quality today, but we still don't have a root cause as to why these microvia boards fail so often.

Osborn: It doesn't play in our arena. It's not something our customers have brought to our attention.

Krick: We have done a very small handful of microvias and stack microvias here, none of which has been military. I believe it's all been commercial level.

Osborn: Almost all the military, though, are running under the IPC specs.

Knapp: And, we've heard no complaints with internal or field parts that we've sent. We had one that was a suspect IST coupon or a D coupon, but other than that we haven't heard of any.

Holden: Appendix A from IPC-2221 about the D coupon has a whole new generation of D coupons to better test the finer geometries as well as drilled or laser-drilled blind vias. A couple of the talks at that conference were on that.

Krick: I still personally believe that until the laminate suppliers can control the Z-axis expansion, or you can come up with a more robust dynamic of hole creation, I don't think it's going to hold up. I don't think that you can subject laminate to that number of cycles nor plating integrity for that matter, particularly when you're looking at sub five-mil microvias and sub five-mil dielectric. I certainly don't know technology-wise of where it is to that or where you could go with it today. I mean we certainly see the axis here and we toggle cycle all the stuff that we do but you certainly can't expect the Z-axis expansion to be less than a few mils before it's going to end up pulling a four-mil stacked via apart. That's mechanical.

Osborn: But when it cools down, it works.

Krick: Then it heals right back. That is correct.

Knapp: Again, specs don't necessarily reflect reality.

Osborn: It goes back to communication.

Feinberg: Well, I want to thank everybody. This has been a very interesting call.

Osborn: This was fun. You're welcome. PCB007

Supplier Highlights

Trouble in Your Tank: Surface Preparation and Cleaning, Part 2 ▶

Some type of cleaning and surface structuring is required in virtually every step of the printed circuit manufacturing process, from preparing the raw laminate for etch or plating resist to final assembly board cleaning before shipment. I will attempt to cover most of the general cleaning problems that can occur in any of these steps.

MIVA Technologies' Explosive Growth Shows no Signs of Slowing Down ▶

MIVA Technologies is a leading equipment builder for direct imaging technologies. The company's head of its business development group, Brendan Hogan, provides some background and explains where the company's specialties lie.

MacDermid Enthone Appoints Roger Fontaine to Eastern Region Commercial Team ▶

MacDermid Enthone Electronics Solutions has announced the appointment of Roger Fontaine to the Eastern Region Commercial team. Roger will take over account management responsibilities for the New England, New York and Toronto Territory, working closely alongside Nate Dobrzynski.

Atotech's Future Is Pointing Upwards; Unveils New Logo ▶

Over the past year, the company has transformed into a stand-alone organization and just completed a company-wide re-organization in order to increase its customer support levels. The new logo perfectly represents Atotech as the driven and forward-thinking company it is and will help to reach the next goal of increasing customer engagement and satisfaction.

Ventec Names Peter Coakley Sales Director for UK ▶

Ventec International Group Co., Ltd. has appointed Peter Coakley as sales director UK. Effective July 1, Peter takes over the responsibility for the strategic leadership of UK sales activities that will contribute to the overall growth strategy of the company.

Flying Probe Testing: It's about Speed and Stability Says MicroCraft ▶

The I-Connect007 team and Takayuki Hidehira discuss where flying probe testers currently stand in the market and MicroCraft's observation of the rise of captive PCB shops in Japan.

Excellon Installs Laser System at Coast to Coast Circuits ▶

Excellon has installed a COBRA-II Hybrid Laser System at Coast to Coast Circuits Inc.'s facility in Rochester, New York. Coast to Coast is a US-based company specializing in the manufacture of bare printed circuit boards, flex and rigid-flex circuits, and IC packaging substrates.

atg Luther & Maelzer Extends Range of Flying Probe Test Systems ▶

atg Luther & Maelzer GmbH extended its range of Flying Probe test systems by launching a line for test areas of up to 40'' width. The oversized systems complement the standard line which can load boards with sizes of up to 27'' width.

China CCL Suppliers Raising Prices ▶

China-based CCL suppliers led by Kingboard Copper Foil have raised their quotes starting July. Rising costs of copper foil and other raw materials were the key factor behind those China-based firms' upward adjustments to their CCL prices.

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Reliability Thoughts at the Department of Defense

Guest Columnist
Feature Column by Dennis Fritz, FRITZ CONSULTING

Obviously, the Department of Defense is very interested in reliability. The DoD has been designing and using weapon systems since before the B-52 bomber became operational 63 years ago. Reliability must be a prime consideration in defense design and manufacture.

But just how does reliability get specified and designed into defense systems? Contrary to public belief, the DoD has no central engineering department watching reliability—just handbooks and/or guidelines for the various programs, prime contractors, and engineers. Central to DoD is the Defense Standards Program Office (DSPO). However, authority for system reliability does not rest with the DSPO; authority rests with the weapons program offices. A program executive officer (PEO) may be responsible for a specific program (e.g., the Joint Strike Fighter), or for an entire portfolio of similar programs.

However, one metric of reliability within the DoD is obtained from using Handbook MIL 217—Reliability Prediction of Electronic Equipment, Revision F, note 2. That document dates originally to 1962 and was revised about every five years until 1995. Handbook MIL 217 contains 17 chapters on various IC/discrete components, and Chapter 16 concerns "interconnection devices." Section 16.1 deals with through-hole mounting (remember that?) and section 16.2 for boards using surface mount devices.

Various complicated Handbook 217 formulas give failures per million operating hours or inverting to one-over failures gives "mean time between failures – MBTF."

Autonomous unmanned Squad Mission Support System, or SMSS (Photo Credit: U.S. Army)

To get a feel for the factors influencing Mil Handbook 217 MTBF prediction, the following information is necessary:

- Thirteen various environments where defense electronics will be deployed
- Whether the construction obeys IPC Class 3 or lower IPC class construction
- The number of board layers from one to 18 (an 18-layer board was complicated in 1995)
- A quality factor for whether the assembly is to be machine soldered or hand soldered

So, why has there not been an update of Handbook MIL 217 since 1995? The book "Reliability Growth, Enhancing Defense System Reliability" contains an explanation[1]. The lack of an update is something of a "hot potato" within the DoD, for the following reasons:

1. The general methodology of MIL 217 is to analyze field failures to compile the important reliability factors and derive a formula for their influence. However, there is not really a good mechanism for collecting field failure data across the various programs within the DoD. Failure data is hard to accumulate.
2. There is little precise information about the operating conditions of deployed defense electronics. Sometimes a weapon system has different environments—storage temperature, humidity, operating temperature when active, etc. Consider the operating conditions of a fighter aircraft: storage at various land or sea locations, operating at elevated desert or frigid high-altitude temperatures, standby for days but then extreme stress conditions for a one-hour mission, and so on.
3. The formulas are statistically based—whereas there is frequently an understanding of the influence of operating conditions. The latter was traditionally called physics of failure (PoF), but has recently been given the more positive name "reliability physics analysis" and has come to be a highly developed branch of reliability engineering.

Within the DoD, the original critic of MIL Handbook 217 was the U.S. Army. That dates to 1995, when Assistant Secretary of the Army Gilbert Decker noted in "Policy on Incorporating at Performance-Based Approach to Reliability in Requests for Proposals" that Army systems reliability should include:

- Quantified reliability requirements and allowable uncertainties
- Failure definitions and thresholds
- Life-cycle conditions

That is, reliability of Army systems should not be derived just from mathematical formulas but should try to understand the conditions that influence failure.

MIL 217 is still in use today, mainly for spare parts purchases at the start of, and during the useful life of weapons systems. The formulas, when use data is gathered, will generate failure numbers for spare parts purchases. The purchase of new weapons systems can be defined with required spare parts and the whole deployment going forward—with a best estimate of how to keep the weapons system operational for 20, 30, 40, or even 63 years.

Is MIL 217 dead? The pioneering work on MIL 217 was done at the Rome Air Defense Center near Utica, New York. As recently as 2010, there has been a Defense Standards Program Office effort to generate MIL 217 Handbook Revision G. However, Naval Support Activity–Crane, Indiana has been designated now as the "preparing activity" for any revisions that would be directed by the DoD. While there is still some hope to incorporate some physics reliability analysis into MIL 217, the effort is minimal.

So, how is the defense community to deal with reliability in the future? Recent advances in computer-based modeling now allow a reasonable prediction of assembled systems life. This modeling has moved beyond prediction of solder joint life and now includes other stresses such as vibration and various mechanical shocks, properties of laminates, final board finishes, and plating properties of the copper board conductors. Great strides are being tak-

en in the "prognostics and health" prediction for new electronics systems.

One of the emerging challenges for high-reliability boards, especially ones for defense, is outlined in IPC WP-23 "Via Chain Reflow Continuity Test: The Hidden Reliability Threat—Weak Microvia Interface." This is evidenced in boards with multiple levels of stacked microvias, which are increasingly needed for mounting high-density boards for large I/O count integrated circuits.

While this stacked microvia reliability activity is currently focused within the IPC Technology Solutions committee, it is expected that more information will be forthcoming at both SMTAI in Rosemont, Illinois, and IPC APEX EXPO in San Diego. For a synopsis of the recent high-reliability forum held in Maryland, see the article by Happy Holden on page 36 of this magazine[2]. **PCB007**

References

1. National Research Council of the National Academy of Science, copyright 2015.

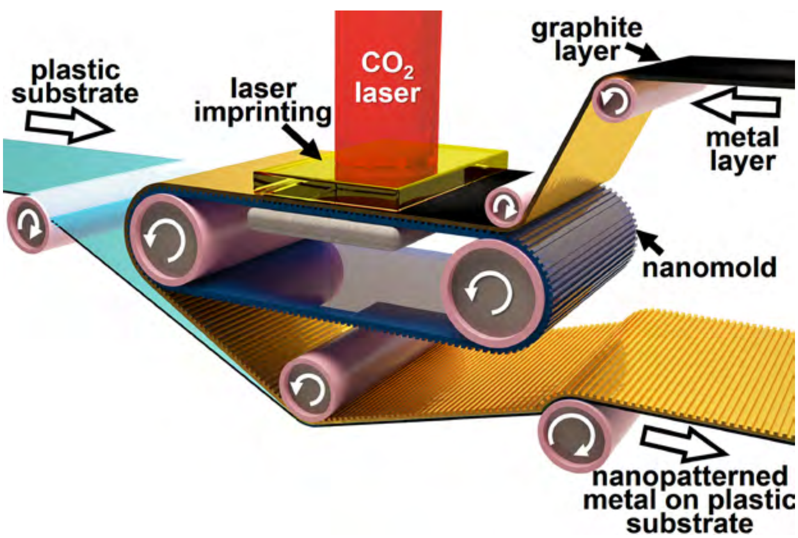
2. "The IPC High-Reliability Forum for Mil-Aero and Automotive Sectors" by Happy Holden, *PCB007 Magazine*, August, 2018.

Dennis Fritz was a 20-year direct employee of MacDermid, and has just retired after a 12 years as a senior engineer at SAIC, Inc, supporting Naval Surface Warfare Center, Crane, Indiana. He was elected to the IPC Hall of Fame in 2012.

Future Electronic Components to Be Printed Like Newspapers

A new manufacturing technique uses a process similar to newspaper printing to form smoother and more flexible metals for making ultrafast electronic devices.

The low-cost process, developed by Purdue University researchers, combines tools already used in industry for manufacturing metals on a large scale, but uses the speed and precision of roll-to-roll newspaper printing to remove fabrication barriers to making electronics faster than they are today.



Cellphones, laptops, tablets, and other electronics rely on their internal metallic circuits to process information at high speed. Current metal fabrication techniques tend to make these circuits by getting a thin rain of liquid metal drops to pass through a stencil mask in the shape of a circuit, like spraying graffiti on walls.

"Unfortunately, this fabrication technique generates metallic circuits with rough surfaces, causing our electronic devices to heat up and drain their batteries faster," said Ramses Martinez, assistant professor of industrial engineering and biomedical engineering.

Future ultrafast devices also will require much smaller metal components.

"Forming metals with increasingly smaller shapes requires molds with higher and higher definition, until you reach the nanoscale size," Martinez said. "Adding the latest advances in nanotechnology requires us to pattern metals in sizes that are even smaller than the grains they are made of. It's like making a sand castle smaller than a grain of sand."

This so-called "formability limit" hampers the ability to manufacture materials with nanoscale resolution at high speed.

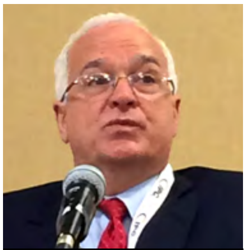
Source: Purdue University

The IPC High-Reliability Forum for Mil-Aero and Automotive Sectors

Feature by Happy Holden
I-CONNECT007

I had the pleasure of attending IPC's High-Reliability Forum (HRF) in Baltimore in May. As the IPC scripted it, it was a "Technical Conference with a Focus on Electronics Subjected to Harsh-Use Environments."

HRF included a half-day tutorial on "Achieving Improved Reliability with Failure Analysis" taught by Bhanu Sood, commodity risk assessment engineer, NASA Goddard Space Flight Center.



Michael Carano

Michael Carano, the forum moderator, opened HRF at 9 am. Attendance topped 80, with pre-registration at over 90. Michael introduced the keynote speaker for the forum, American Standard Circuits CEO Anaya Vardya, whose keynote highlighted the North American overview of the PCB industry's challenges. Specific points included:

- Pricing erosion
- Higher technology
- Cost of doing business
- Demanding customers
- Competition
- Hiring the right people

Anaya Vardya

The growth of China as a PCB manufacturing center has eroded North America's PCB facilities from a high of over 1,000 in 2000 to the most current (2016) count of 255. Of those, only six had revenues of over $50M USD and most were under $6M (~150). The total of $5.4B worth of shipments were distributed into seven major markets (Table 1).

Anaya used his own company's philosophy and milestones to highlight their approach to people, equipment, software, product capabilities, demanding customers and competi-

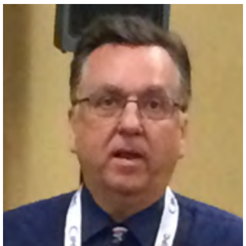
Military/Aerospace	27%
Communications	24%
Instruments/Medical	18%
Computers	14%
Industrial	9%
Automotive	4%
Consumer	4%

Table 1: The seven major markets that U.S. PCB manufacturers supplied into. (Source: WECC)

tion. He concluded with a summary of the key "Global Strategy" for success.

The second presentation was by J.R. Strickland and Jerry Magera of Motorola Solutions: "How MSI Applied Technology Beat the Microvia Hidden Threat." This was a summary and report on their research into stacked-microvia failures that were escaping into products. This report was the main substance of the recently released IPC White Paper, IPC-WP-023 "IPC Technology Solutions White Paper on Performance-Based Printed Board OEM Acceptance—Via Chain Continuity Reflow Test: The Hidden Reliability Threat—Weak Microvia Interface."


J.R. Strickland


Jerry Magera

Starting in 2010, stacked microvias begin exhibiting field failures and steps were taken to understand why. The product failures were intermittent in nature but more often at hot temperatures. This led to their unpredictable reliability. Existing quality controls and reliability testing was not showing up these defects. Various experiments were conducted to find a fool-proof method of quality control. By 2011, an in-situ reflow test of six passes through the SMT reflow oven while instrumented with a 4-wire Kelvin resistance circuit was finalized and contained the problem. The problem was a weak microvia interface to the prior plated copper on stacked vias. Communication and consulting with industry colleges indicated they were having similar problems. All new microvia designs were to use staggered microvia chains until the root cause was thoroughly understood. A board coupon was established of the microvia chain and this proved to be effective to screen each board before assembly. IPC TM-650 2.6.27A was released in September 2017 as a standard for this Pb-free reflow oven acceptance test. MSI has had zero product failures since implementation. The reflow coupon consists of six daisy chains to test each board:

- S1 chain of staggered microvias
- SX2 chain of stacked microvias
- S3 smallest finished hole size PTH via
- S4 & S5 daisy chain of constructed of via features used in the corresponding PWB
- S6 FHS of greatest number of PTH, PIH component via

They concluded with promises to share their data as they search for the root cause of this microvia problem, as stacked microvias are inevitable in future high-reliability designs. Additional work is needed by industry to identify root cause and implement corrective actions.

The third presentation, "HDI Microvia Reliability for any Temperature Extreme," was presented by Kevin Knadle of I3 Electronics. Kevin, formerly of IBM, gave an excellent history of PTH reliability testing at IBM and the use of current induced thermal cycle (CITC) testing. Covered as IPC-TM-650 2.6.26 Method B, this small, single-net coupon of 100 vias is only 1.75" x 0.3" and designed by IBM to be used many times on a panel and easily adapted to in-line process monitoring. The test uses current to heat the coupon at three degrees per second to 245°C for a dwell time of 40 seconds and repeats the cycle for 200-700 cycles per day. The temperature coefficient of resistance (TCR) is measured continuously and used to determine the coupon's temperature. A 4-wire resistance bridge monitors the via daisy chain.


Kevin Knadle

The CITC cycles were verified by FEA modeling, TMA, and Moiré and has been used by IBM for 25 years. The rapid nature of the test and the small size of the coupons has lead IBM and I3 to be able to characterize many important steps in the PCB manufacturing process like basic laminates, drill bit design, lamination temperature cycles, drill hit count, copper plate chemistry, etchback process, hole filling materials and ENIG process control.

This testing technique has led to the discovery of PTH barrel and corner cracks as well as microvia cracks. The efficient and inexpensive CITC test vehicle (TV) was used to monitor and continually improve the microvia process including the use of high-stress stacked microvias. Kevin utilized many graphs and diagrams illustrating how to create and prevent microvia failures from field studies and design alternatives, which led to his final slide: "Conclusion: Reflow is the cause of assembly and field via failures."


Jimmy Baccam

The fourth presentation was by Jimmy Baccam of Lockheed titled "Microvia Reliability." Jimmy is a product designer and designed the microvia boards that failed. This is his story:

"Microvias are not bulletproof and there are few design rules that have been verified and are consistent from vendor to vendor. Further industry studies are required to understand what makes a robust microvia. There are many complex variables in designing with microvias, but this I have found:

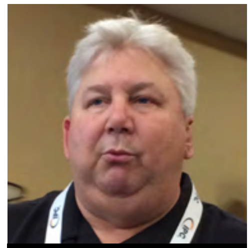
- It is hard to pinpoint any one thing as the perpetrator of microvia failure
  - Is it laser drilling?
  - Is it materials?
  - Is it chemistry?
  - Is the target pad surface cleanliness?
  - Is it something else or all the above and more?
- Microvias that have passed electrical test after fabrication can still fail post assembly
- Microcracks at the target pad and electroless copper interface are observed in failing microvias
- A more robust screening method that measures resistance during reflow is required to verify microvia reliability in a PCB
- Depending on the function of the circuit, a microcrack in the microvia doesn't necessarily mean the circuit will fail. Sensitive analog signals of less than 5 mA of current had performance failures, while the digital signals on the same board which had greater than 5 mA of current didn't have any performance problems even though the microcracks were present"

Lockheed did extensive testing to discover where the microvias had failed. SEMs and focused-ion-beam (FIB) helped locate the microcracks in microvias. To test for these failure modes, a new IPC-2221 D-coupon has been designed by Lockheed containing two daisy-chained microvias with/without buried through-via structures. These coupons then are reflowed a minimum of 6X times using one of two different reflow profiles (230°C or 260°C) and monitored with a 4-wire resistance sensor. The results from OM testing indicate that the coupon and test procedure does in fact find the weak microvia structures and those that pass are good to assemble. Lockheed will be doing more experiments on large fabrication 12-layer panels during 2018 and 2019 using this new D-coupon (but modified into six different sets of design rules and via structures) to find what are the root causes of failure during the fabrication process and what design rules produce the most robust microvia structures. The six D-coupons are summarized:

- D-coupon 1
  - Net 1 has a microvia L01-L02 stacked on top of buried microvia L02-L03
  - Net 2 has offset microvias L01-L02 and L02-L03
  - Net 2 has different offset pad to pad distances of tangent, 2 mil, 6 mil and 10 mil
- D-coupon 2
  - Net 1 has stacked microvias of L01-L02, L2-L11, and L11-L12
  - Net 2 has offset microvias and buried vias of L01-L02, L02-L11 and L11-L12
  - Net 2 has different offset pad to pad distances of tangent, 2 mil, 6 mil and 10 mil

- D-coupon 3
  - Net 1 is a single stack microvia with traces used in the daisy chain on layer 2
  - Net 2 is a single stack microvia with mini-planes used in the daisy chain on layer 2
- D-coupon 4
  - D-Coupon 4 simulates 0402 discretes with via-in-pad and fanned out microvias
  - Net 1 has via in pad as well as offset microvias and buried via with varying offset microvia to buried via distances
  - Net 2 has fanned out microvias and the microvias are offset from the buried via with varying offset microvia to buried via distances
- D-coupon 5
  - D-Coupon 5 simulates 0.5 mm pitched BGA with via-in-pad
  - Net 1 has via in pad as well as stacked microvias L01-L02 and L02-L03
  - Net 2 has via in pad and only a single stack microvia from L01-L02
- D-coupon 6
  - D-Coupon 6 simulates SOIC with via-in-pad and fanned out microvias
  - Net 1 has via in pad as well as offset microvias and buried via with varying offset microvia to buried via distances
  - Net 2 has fanned out microvias and the microvias are offset from the buried via with varying offset microvia to buried via distances
  - Peel strip coupon
  - Peel strip coupon anchored with microvias

Testing to be complete by December 2018 and results will be reported at next year's IPC High-Reliability Conference 2019.


Doug Jeffrey

Our fifth presenter Doug Jeffrey of Electrotek discussed their process of drilling blind vias in "Reliability Findings of Mechanically Drilled Complex Via Structures." Doug went into their process of drilling blind vias and the results of testing these blind vias. They use 0.006" and 0.008" drills for the drilled blind vias and 0.008" and 0.010" for buried vias depending on the aspect ratios. The IPC-2221 D-coupon was used as the test vehicle, as a 14-layer design (1 + 12 + 1) with four microvia structures, a buried via set of 2 to 13 and a filled via through via 1 to 14. The two nets consisted of:

- Net 1 consists of 800 microvias
  - Chain 1 is a daisy chain of single layer vias
  - Chain 2 is a daisy chain of 2 layer stacked microvias
- Net 2 consists of 103 buried/through vias and 80 microvias
  - Chain 1 uses a through via and microvia single-layer daisy chain
  - Chain 2 consists of a daisy chain of buried vias

Testing was done on 1549 coupons from 41 builds conducted from May 2017 to Apr 2018 with four coupons per panel using the new IPC-TM-650 2.6.27 (260°C lead-free profile). Additional reflows were conducted on those that pass for up to 24 such cycles. The test resulted, of the 41 builds, in the failure rates shown in Table 2.

A special guest speaker was Stamen Borisson, of the U.S. Dept. of Commerce, who presented the "Results from DOC Study on U.S.

	1–6 Cycles	7–24 Cycles	>24 Cycles
Net 1	5.9% going to 0	3.5% going to 2.6%	7.8% going to 9.1 %
Net 2	9.1% going to 0	23.5% going to 17.4%	52.2% going to 60.9%

Table 2: Failure rates of the two nets in the 41 test builds.

Printed Board Industry." Stamen had several slides that showed the status of the U.S. bare board industry, especially, the defense end use market where fabricators indicated their customer base:


Stamen Borisson

- Electronics—18.5%
- Aerospace—17.2
- Command, control, communication, surveillance—16.0%
- Missiles—12.5%
- Marine—11.1%
- Space—10.8%
- Ground vehicles—9.2%
- Homeland Security—4.5%

One of the interesting statistics they collected was the number of facilities with negative net income in one or more years. From 2012 to 2015, the number small facilities (<$10M) was more than 50, growing to 57 in 2015, while there was only one in the large >$40M group. Another stat was the facility utilization percentage, which is the average rate for each as a percentage of production possible under 24/7 operation. The small shops averaged about 40%, while the large facilities averaged around 62%.

Respondents indicated their top priorities for investment and capital:

- Equipment for new technologies—34.4%
- Equipment for existing technologies—31.3%
- IT/computers/software—14.6%
- Expanded facility—10.4%
- Other—8.3%

This corresponds to their list of needs and concerns:

- R&D and capital investments
- Manufacturing limitations due to equipment
- Supply chain disruptions
- Workforce challenges
- Retention issues
- Aging equipment and facilities
- Healthcare costs
- Competition
- Working with DoD-MIL certification

Borisson concluded his presentation with an overview of the U.S. PCB facilities' various manufacturing capabilities.

The final two speakers of the day addressed reliability coupons. The first was by Phil Henault of the Raytheon Company, "Reliability Coupons." This was an overview of IPC-2221 Appendix A—Conformance Coupons. Phil explained each of the new Appendix A coupons: AB/R; A/R; H; P; S; E; G; W; Z; D; Propagated D & Propagated B (Table 3). These coupons are newly redesigned by the IPC Committee to be smaller and reflect the higher density used today. Of interest is the new 'D' and 'Propagated D' coupons for HDI. The Figures x and y show the old "Legacy D" and the new "D" coupons.


Phil Henault

Phil concluded with an overview of the new IPC-2221B Gerber Coupon Generator, including screen inputs. Currently available automated coupon designs are: AB/R, H, P, S, D, Propagated D and Propagated B with the IPC 1-1-c subcommittee working to include coupons E, G, and W. Additional work is being done on Coupon K.

The second coupon talk, and the last of the day, was on "Reliability Coupons Test Coupon Improvement" by Lance Auer of Conductor Analysis Corp. This was a continuation on the IPC's efforts to update reliability topics and standards. Lance was talking about and explaining the various IPC Committees:


Lance Auer

- 1-10c committee for Conformance coupons
- D-32 committee for Reliability test methods

Coupon	Description	Purpose	Use
AB/R	General purpose AB coupon for through features	Plated hole/via evaluation, feature size and spacing, annular ring, thermal stress and rework simulation	Lot Conformance
A/R	General purpose A coupon for use when B features are not present	Plated hole evaluation, feature size and spacing, annular ring, thermal stress and rework simulation	Lot Conformance
H	Surface insulation resistance coupon	Surface insulation resistance	When Specified
P	Peel strength coupon	Peel strength/Plating adhesion	Periodic/Lot Conformance
S	Hole solderability coupon	Hole solderability	Lot Conformance
E	Moisture and insulation resistance coupon	Moisture and insulation resistance, Dielectric Withstanding Voltage	Periodic Conformance
G	Solder mask coupon	Solder mask adhesion	Lot Conformance
W	Surface mount solderability coupon	Surface mount solderability, finish plating thickness verification by XRF	Lot Conformance
Z	Controlled impedance coupon	Controlled impedance	When Specified
D	General purpose AB daisy-chain via coupon	Plated hole/via reliability	When Specified
Propagated D	D coupon for non-through (propagated) via features	Plated structure reliability	When Specified
Propagated B	B coupon for non-through (propagated) via features	Plated hole evaluation, annular ring and thermal stress	Lot Conformance

Table 3: IPC-2221, Appendix A Coupon Table.

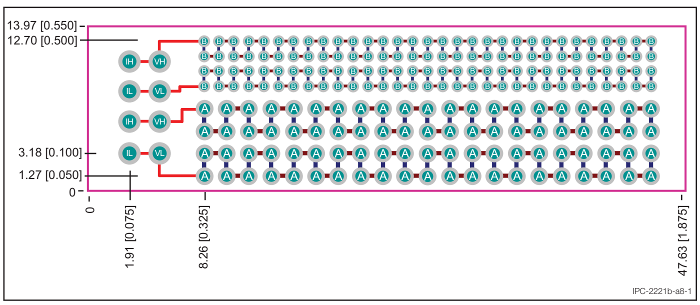


Figure 1: D coupon layout. (Source: IPC-2221 Appendix A)

Design Features

- Coupon D is used to evaluate plated hole and through via reliability by thermal stress. The coupon is designed to have a sufficient number of plated holes or vias in a chain to obtain a precise resistance measurement.
- Overall size: 1.875 x .550
- Legacy coupon: 1.378 x .550
- Daisy Chain traces n Layers 2 and n-1 to capture both post separation and barrel crack failures.

- D-33a committee for Performance specifications (IPC-6012)
- D-22 committee for Performance specification (IPC-6018)

These new efforts will address the early detection of microvia defects using the new coupons, resistance monitoring during reflow (or simulations) and thermal stress/thermal shock. This includes the PCQRR Program and IPC-6012 QML Program, where entirely new parametric panel artwork has been created to include HDI staggered and stacked microvias and complex constructions up to 24-layers.

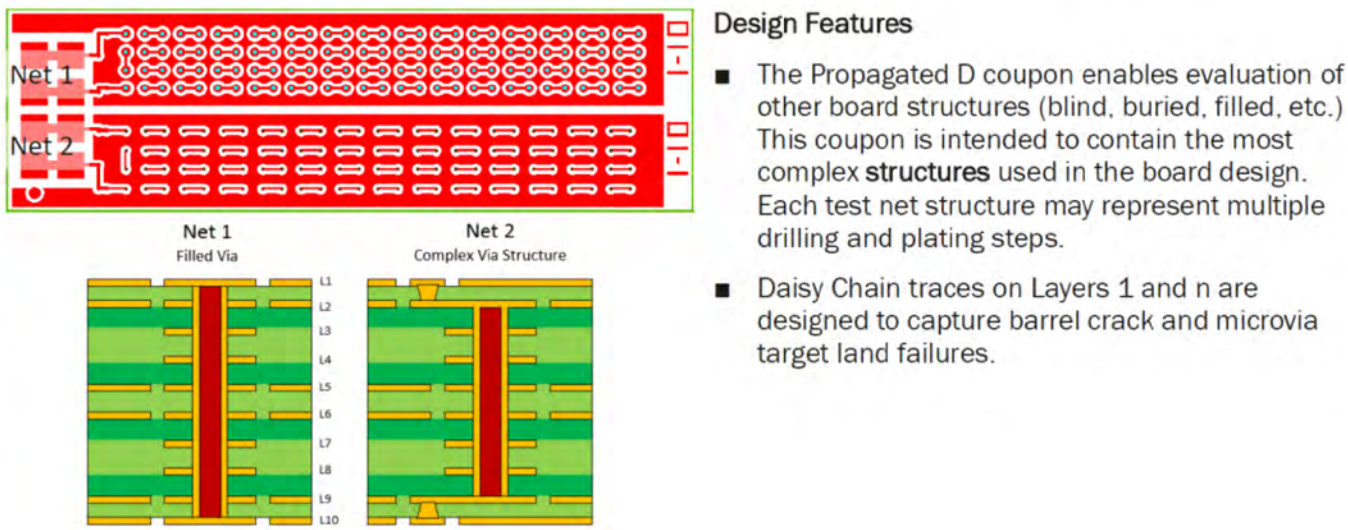


Figure 2: Propagated D coupon layout. (Source: IPC-2221 Appendix A)

IPC High-Reliability Forum for Mil-Aero and Automotive Sectors–Second Day

The first presentation of Day 2 was a panel discussion on "forgotten tribal knowledge." The panel members were Don Dupriest, Lockheed Martin; Denny Fritz, SAIC; and Doug Jeffrey of Electrotek (Figure 3).

What is Tribal Knowledge? The panel defined it as, "A set of unwritten rules or information known by a group of individuals within an organization but not common to others that often contributes significantly to overall quality. Tribal knowledge may be essential to the production of a product or performance of a service but may also be counterintuitive to the process."

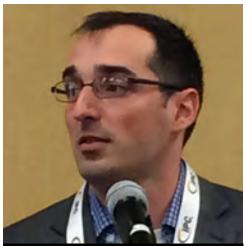
Figure 3: Panel on "Forgotten Tribal Knowledge," (left to right) Don Dupriest, Denny Fritz and Doug Jeffrey.

To get the discussion going, the panel had some general questions for all:

- What methods are you or your company using to prevent loss of tribal knowledge?
- Can you provide an example of when tribal knowledge loss caused a design or production issue?
- What actions would you recommend a new employee take to combat the loss of tribal knowledge?
- In this bimodal era of our industry what means can management take to facilitate knowledge sharing?
- What areas of our industry do you see the biggest potentials for knowledge loss?
- Do you have any creative ideas for how to backfill these gaps?
- How are you or your companies making a conscious effort to include younger and newer employees in industry activities/meetings?

The next presentation was "System-level Effects on Solder Joint Reliability" by Maxim Serebreni of DfR Solutions. Maxim discussed the simulation of the "Wear-Out Failure

Mechanism" of solder joints arising from board-component interactions under complex loading conditions. The system level effects can be complex and included:


Maxim Serebreni

- Effect of PCB glass style and pad size
- Influence of PCB mounting conditions
- Thermo-mechanical effects on constrained assemblies
- Vibration at elevated temperatures-vibration fatigue
- Mitigating system level effects-like underfill

By using test vehicles, microsections, Weibull charts and comparisons to FEA and model correlations, Dr. Serebreni made a compelling presentation about the usefulness of model predictions from simulations.

The third talk of the day was by David Pinsky of Raytheon on "Tin Whisker Mitigation by SMT Reflow." Tim covered the work Raytheon has been doing to prevent tin whisker growth by using the SMT assembly process to create a "self-mitigation" condition where all exposed tin is covered with tin-lead. The DOE matrix for the study was composed of four experimental factors (Table 4):


David Pinsky

- Each of the seven assembly locations were provided with a kit containing eight bare boards (four types, two replicants) and all the components necessary to populate them. Each assembler chose process conditions as they would deem appropriate to achieve compliance with J-STD-001, Class 3 requirements
  – HASL finish/large pads
  – HASL finish/small pads
  – OSP finish/large pads
  – OSP finish/small pads
- Components used: 0603 chip, TQFP100-14 mm, SSOP28-5.3 mm, A-TQFP44-10 mm-.8 mm, SO14G-3.8 mm, SO14G-3.8 mm, SSOP28-5.3 mm, DO-216AA, QFP44-0.8 mm, LQFP32-7 mm-0.8 mm, SO14G-3.8 mm, SOT223, LQFP48-7 mm-0.5 mm, LQFP100-14 mm-0.5 mm & 0612 chip
- Assembly process details (Table 5)

The analysis was complex and thorough. The summary of the results indicated:

- Pad finish was not significant
- Pad size was significant but had a very minor effect
- Soldering process was very significant to self-mitigation
- Package geometry is the most significant factor
- Some components were nearly certain to self-mitigate under all process conditions (0603 chips, SO14Gs)

Experimental Factor	Settings
Component packages	Sixteen different part numbers
Board finish	OSP and Sn Pb HASL
Pad size	Per initial study and 25% smaller
Manufacturing process	Seven different locations

Table 4: The four experimental factors in Raytheon's Tin Whisker Mitigation reflow study.

Setting	Process A	Process B	Process C	Process D	Process E	Process F	Process G
Reflow type	Vapor phase	Convection oven	Convection oven	Convection oven	Convection oven	Convection oven	Convection oven
Flux	ROL0	ROL0	ORM0 63/37	ROL0	Sn62 RMA No-clean	No-clean	No-clean
Stencil thickness	5 mil	5 mil	5 mil	4 mil	Laser 5 mil	5 mil	5 mil
Stencil aperture	1:1	1:1	1:1	1:1	1:1	1:1	1:1
Time above liquidus	90 s	60-75 s	66 s	90 s	45 s	60 s	70 s
Peak temperature	218 °C	215 °C	220 °C	225 °C	220 °C	213 °C	220 °C
Atmosphere	Air	Nitrogen	Nitrogen	Nitrogen	Nitrogen	Nitrogen	Nitrogen
Number of reflow cycles	1	1	1	1	1	1	2
Rework	None	None	None	None	None	None	Yes

Table 5: The settings for the seven reflow conditions used in the DOE matrix for Tin Whisker Mitigation study. (Source: Raytheon)

- Some components exhibited a moderate probability of self-mitigation within the range of 0.6 to 0.9
- One component exhibited a very low probability of self-mitigation (0612 chip)
- XRF is an effective technique for evaluation of self-mitigation
- Aging of parts to 14 months did not compromise self-mitigation but aging to five years did
- There is a difference in self-mitigation depending on reflow process and peak oven temperature
- Lead geometry affects self-mitigation probability of QFNs

The afternoon presentations started with "Solder Interconnect Challenge and Modeling for High Performance Electronics" by Dr. Michael Osterman of CALCE-University of Maryland. Osterman gave a compelling lecture on the physics of failure (PoF) for complex electronics units, including:

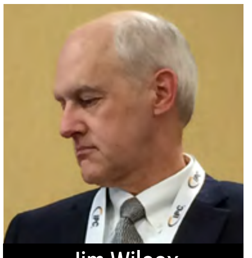

Dr. Michael Osterman

- Microelectronic components
- Conductive filament formation
- Dendritic growth
- PFH barrel cracking
- Trace fracture
- Solder fatigue
- Lead wire fracture

He explained the PoF simulation-based life assessment with models and FEA demonstrations. Lead-free solders were a focus with review of their history from the first generation to the present third generation solders.

He concluded with the effect of underfilling components and the important role simulation of the modeling life under complex temperature cycles has to life predictions.

The next talk was "Assembly Tests for Solder Joint Reliability" by Jim Wilcox of Universal Instruments. Jim is a member of


Jim Wilcox

the AREA Consortium (Advanced Research in Electronics Assembly). This is a comprehensive evaluation program for assembly processing including lab research, text vehicles, metallurgical evaluations and reliability evaluations, including a full scope of environmental stress testing (ATC, drop shock, vibration, thermal shock and corrosion). He relayed to us many of their findings after doing extensive assembly level testing for solder joint reliability that included:

Mechanical robustness
- Isothermal shear fatigue
- Drop shock testing
- Vibration testing

Thermomechanical reliability
- Environmental thermal cycling
- Thermal shock (air-to-air, liquid-to-liquid)
- Power cycle

Included were the effects of various PCB surface finishes and various components like BGAs, LGAs, TBGAs and QFNs of various pitches and ball configurations and sizes. The number of slides was impressive and numbered over 50. Suffice it to say, the AREA Consortium is testing most of the variables that are used in lead-free assembly today for their effect on SMT reliability.

The last talk of the conference was by Richard Bellemare of MacDermid Enthone Electronics on "A Review of Metallization Interfaces on Microvia Reliability."

Rich entertained us with a compelling talk on factors affecting reliability of microvias and the interfaces encountered in microvia processing. There are numerous factors contributing to microvia reliability:


Richard Bellemare

- Number of vias, stack/staggered, and level of the via within panel
- Via size, aspect ratio and shape
- Drilling and microvia shape
- Cleanliness of the target pad and desmear
- Type of primary metallization
- Quality of the primary metallization
- Quality of the secondary metallization
- Plating processes
- Via filling
- Test methods—thermally induced stress

Bellemare then went on to discuss how critical the understanding is of each process and the underlying steps of each process. Although he could not pin down the 'root cause' we were talking about over the last two days, it certainly educated us as to the complex nature of finding such a root cause. It was a fitting end to two days of presentations and discussions about microvia failures and other SMT failures. **PCB007**

Happy Holden is technical editor with I-Connect007. To read past columns or to contact Holden, click here.

Robots Are Racing Through Our Blood to Cure Disease

Dr. David Zarrouk, director of Ben-Gurion University of the Negev's Bio-Inspired and Medical Robotics Lab carefully places the tiny robot into a cleaned-up pig intestine on his table and flips on the switch. About the size of a thumb, the miniature robot comes to life and starts worming through the intestine, all the way through the other end.

The BGU researcher draws his inspiration from the 1960s movie "Fantastic Voyage." In the movie, a shrunken submarine swims through a scientist's bloodstream to repair his brain. "You can call it a gut bot," says Dr. Zarrouk.

Source: Ben-Gurion University of the Negev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Electronics Industry News and Market Highlights

Scientists Unlock Signal Frequency Control of Precision Atom Qubits ▶

Australian scientists have achieved a new milestone in their approach to creating a quantum computer chip in silicon, demonstrating the ability to tune the control frequency of a qubit by engineering its atomic configuration.

Bacteria-Powered Solar Cell Converts Light to Energy, Even Under Overcast Skies ▶

UBC researchers have found a cheap, sustainable way to build a solar cell using bacteria that convert light to energy. This innovation could be a step toward wider adoption of solar power in places like British Columbia and parts of northern Europe where overcast skies are common.

Flexible Hybrid Electronics: NextFlex Awards $12M ▶

NextFlex has announced funding for seven projects, fueling development of FHE projects that include epidermal sensors for robotic knees, a sensor network to monitor and communicate the status of industrial systems and infrastructure, and more.

Ecology and AI ▶

It's poised to transform fields from earthquake prediction to cancer detection to self-driving cars, and now scientists are unleashing the power of deep learning on a new field: ecology. A team of researchers demonstrated that the artificial intelligence technique can be used to identify animal images captured by motion-sensing cameras.

Electron Spectrometer Deciphers Quantum Mechanical Effects ▶

Electronic circuits are miniaturized to such an extent that quantum mechanical effects become noticeable. Using photoelectron spectrometers, physicists and material developers can discover more about such electron-based processes.

Traditional PC Market Grows 2.7% in Q2 of 2018 ▶

The second quarter of 2018 (2Q18) showed shipments of traditional PCs (desktop, notebook, and workstation) totaled 62.3 million units, recording solid year-on-year growth of 2.7%, according to the International Data Corporation (IDC). The results exceeded forecast of 0.3% and marks the strongest year-on-year growth rate in more than six years.

'Elegant' Design Could Lead to More Powerful, Safer Lithium Metal Battery ▶

If the dendrite breaks through the separator and reaches the cathode, short-circuiting and fire can occur. Solid electrolytes have been shown to suppress dendrite growth mechanically, but at the expense of fast ion transport.

Quantum Computer Becoming Reality ▶

A billion-dollar research effort will make Sweden a world leader in quantum technology. Chalmers researchers have begun work on developing a quantum computer with far greater computational power than today's best super computers.

Engineers Develop Efficient Semiconductor Material for Thermal Management ▶

Working to address "hotspots" in computer chips that degrade their performance, UCLA engineers have developed a new semiconductor material, defect-free boron arsenide, that draws heat away from hotspots much faster than current materials, which could lead to dramatic improvements in computer chip performance and energy efficiency.

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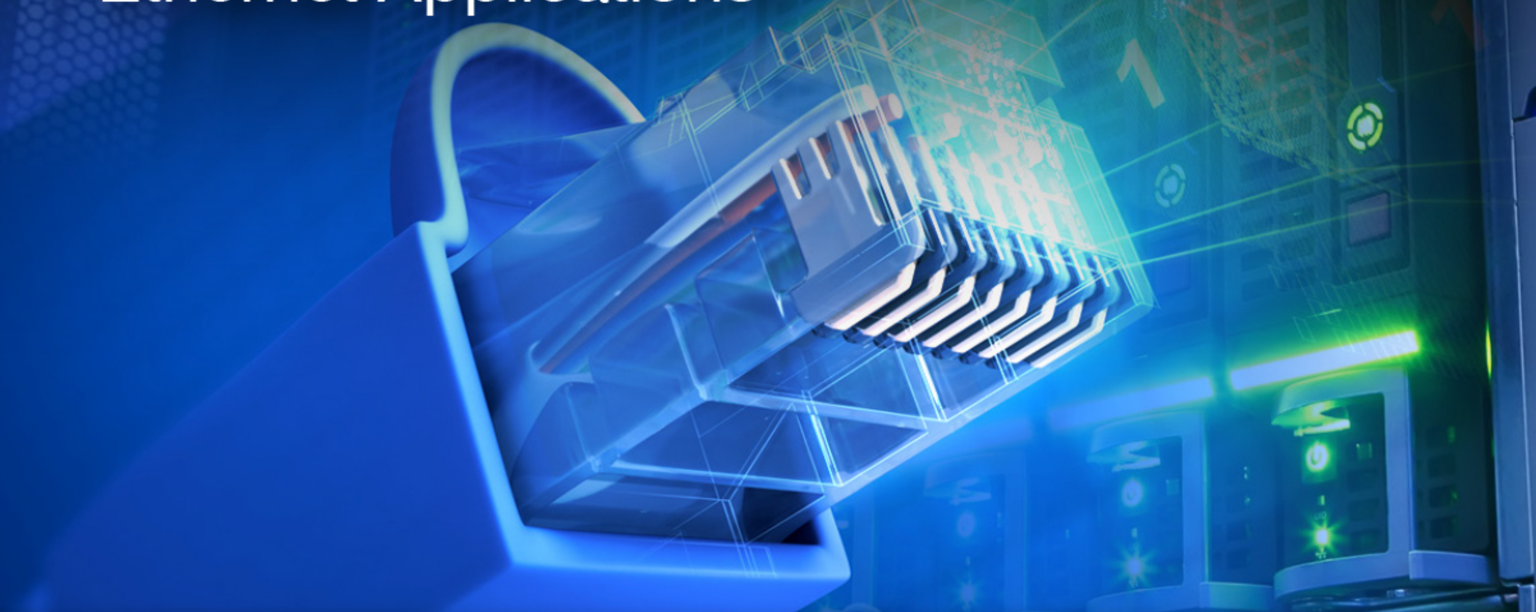

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PCBs Are Moisture-sensitive Devices

Feature by Richard Heimsch
SUPER DRY

Guidelines for the proper storage, handling and moisture protection of electronic components can be found in the standards IPC/JEDEC J-STD-033C. Though these date back to 1999, there were no published standards for storage and moisture protection for printed boards until 2010, and their proper handling is still often overlooked. But with the correct storage control and the use of suitable drying methods, considerable manufacturing advantages can be gained: PCBs will remain solderable for much longer and damage during reflow due to moisture can be eliminated.

Historically, the printed board industry relied on military specifications and guidelines to define the packaging methods used to preserve the quality and reliability of PCBs during shipment and storage. Over time, of course, many of these documents became obsolete, were found to be incomplete, didn't address lead-free assembly, or did not provide guidance for newer laminates or final finishes. Additionally, the proliferation of alternative final finishes has produced concerns and requirements for printed board packaging and handling to preserve the finish and assure good solderability.

For instance, IPC-1601A (2016 revision) Printed Board Handling and Storage Guidelines, states: "Baking is not recommended for OSP coatings, as it deteriorates the OSP finish. If baking is deemed necessary, the use of the lowest possible temperature and dwell time is suggested as a starting point."

Organic solderability preservative (OSP) coatings are among the leading surface finish options in lead-free soldering because they provide an attractive combination of solderability, ease of processing and low cost. Compared to alternatives, however, they tend to be the most prone to oxidation. The cause for this lies in the pure copper surface protected only by the OSP coating layer. Under normal climatic conditions in a manufacturing process, after only a few minutes there will be a separation of a water film at the surface (3-5 atom layers). This then starts a diffusion process which leads to a vapor pressure balance through the

OSP coat. Baking also accelerates solid diffusion between metals and increases intermetallic growth. This can lead to a "weak knee" or other solderability issues if the intermetallic layer reaches the surface and oxidizes. Effects upon other finishes (immersion tin, immersion silver, ENIG) are further detailed in the guidelines.

IPC-1601A (2016 revision) also states: "If process controls are ineffective, and printed boards have absorbed excessive moisture, baking is the most practical remedy." It goes on to state, "However, baking not only increases cost and cycle time, it can also degrade solderability of the printed board which requires extra handling and increases the likelihood of handling damage or contamination. In general, both the printed board fabricator and the user should strive to avoid baking by practicing effective handling, packaging, storage, and process controls..."

In addition to moisture management at key steps in the fabrication process, IPC-1601A also makes clear that boards should be protectively packaged to limit their exposure to ambient humidity during processing and storage. And, importantly, packaged only after determining that their moisture content is below the maximum acceptable moisture content (MAMC) level, which is typically between 0.1% and 0.5% moisture weight to resin weight.

Just as with components, 125°C baking temperatures degrade the solderability of PCBs. IPC-1601A warns that as little as 4-6 hours at that temperature can render HASL finished boards unsolderable. Over the decades that passed since the J-STD-033 standard was created, new technologies were developed and proven to safely reset component floor life using low temperatures and ultra-low humidity without requiring extensive time. These 40-60°C and <1% methods were first adopted in Europe, and their recognition and use has now spread to North America.

The same methods were applied to PCBs, and engineers from the company SMT and Hybrid GmbH published their findings in "Production of Printed Circuit Boards and Systems"[1]. They

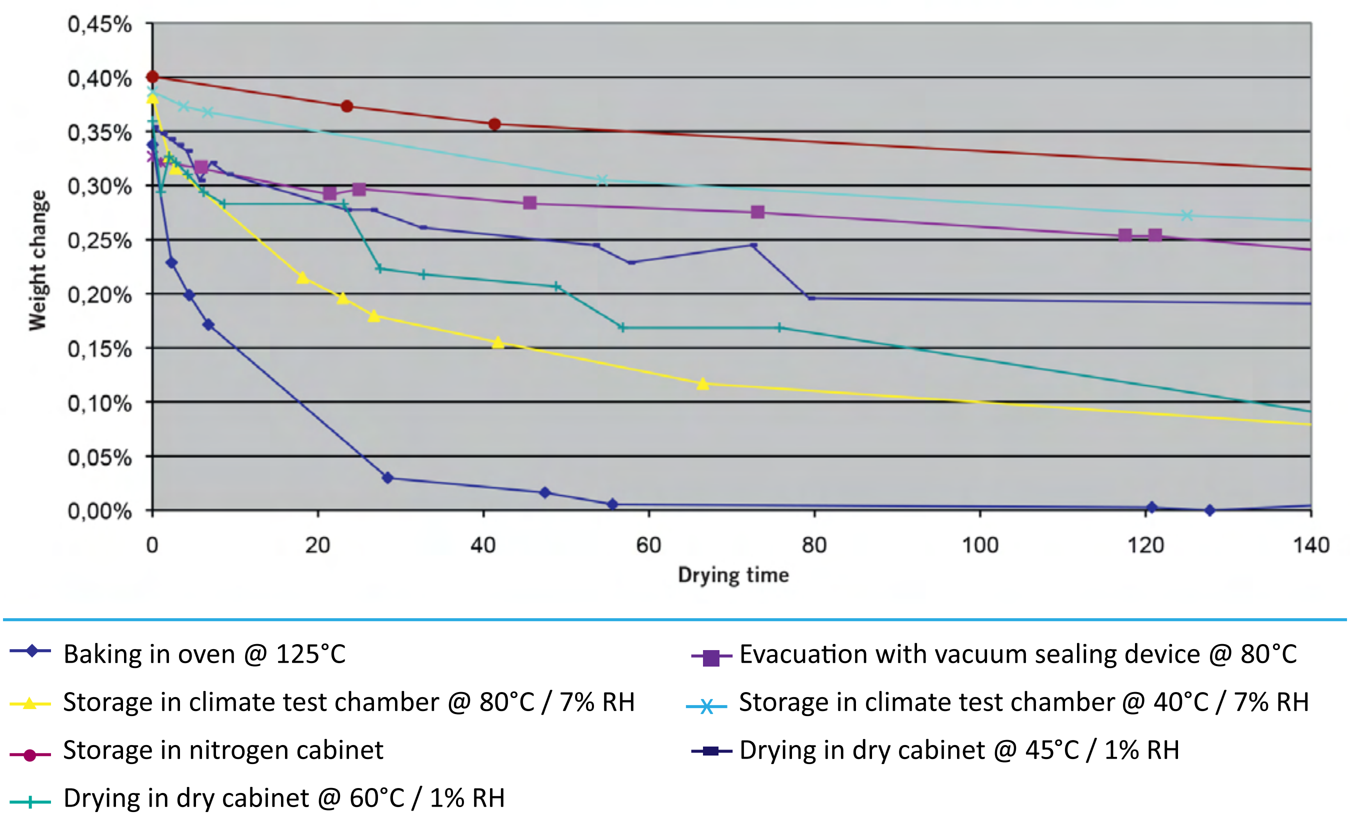

Figure 1: Comparison of the various drying processes using QFP100 as an example.

stated, “Circuit board manufacturers are extremely hesitant at providing instructions on drying their circuit boards. Information from the ZVEI[2] should also be regarded critically. The cardinal problem is the high temperature which is recommended for tempering. If this is applied, the result is often delamination and distortion of the circuit boards. Corrosion and the formation of intermetallic phases of the metallic surfaces are also to be expected.”

The research investigated “whether gentle drying at 45°C or 60°C and at low relative humidity achieves the same result as tempering at high temperatures.” They began first with QFP components which were saturated and then dried in seven different environments, referencing J-STD-033 standards in their report. These were charted in comparison of the various drying processes and are outlined in Figure 1.

The researchers then selected four PCB types and repeated the same procedures of saturation then drying and weighing to 0.1% water weight. This was done using 60°C at <1%, 45°C at <1%, and 125°C at 5%. Their summary results were that “125°C demonstrates the shortest drying time; however, oxidation of the soldering pads and board warpage make it unsuitable for the particular board types tested.” These comparisons are charted in Figure 2.

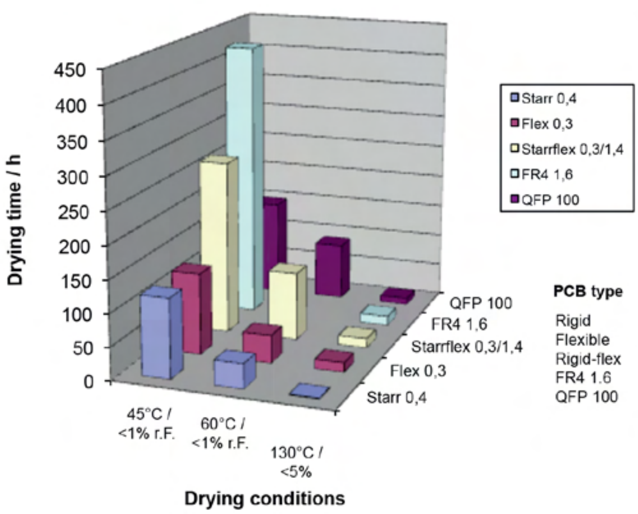

Figure 2: Comparison of four PCB types at various drying conditions.

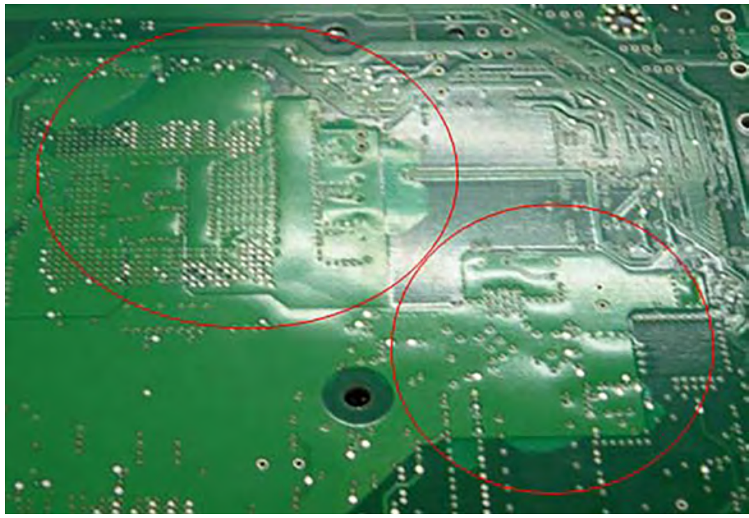

Figure 3: In addition to extending the safe storage time, defects and damage such as popcorning and delamination during the reflow process caused by moisture can be avoided.

Conclusion

Research by SMT & Hybrid GmbH (now SMT Elektronik) was conducted just prior to the original publication of IPC-1601, which now provides detailed guidelines for the packaging and storage of PCBs, both from the PCB manufacturer and at the assembler’s manufacturing floor. It also describes the solderabilty risks associated with high-temperature baking. Ultra-low RH and low temperatures can significantly mitigate those risks while preventing moisture damage during reflow. Examples of such PCB damage are illustrated in Figure 3. **PCB007**

References

G. Schubert, Th. Schonfeld, A. Friedrich, SMT & Hybrid Gmbh, “Drying Printed Circuit Boards,” Production of Printed Circuit Boards and Systems, September 2009.

Richtwerte/Empfehlung des ZVEI, Fachverband der Leiterplattenindustrie.

Rich Heimsch is director at Super Dry.

Mechanism and Mitigation of Nickel Corrosion in ENEPIG Deposits

Feature by George Milad, Jon Bengston and Don Gudeczauskas
UYEMURA INTERNATIONAL CORPORATION

Abstract

Nickel corrosion in ENEPIG (electroless nickel/electroless palladium/immersion gold) deposits has been reported on multiple occasions. This was originally observed in cases where the desired gold thickness was in excess of 2.0 µin (0.05 µm). The boards were left in the gold bath for an extended dwell time until the desired gold thickness was achieved. In those cases, the gold ion reaches through micro-pores, that are common in thinner palladium deposits, below the palladium substrate to the underlying nickel and continues to deposit, corroding the nickel.

This article is an attempt to reproduce the defect, and to determine the necessary mitigation action to avoid nickel corrosion in the ENEPIG finish.

Introduction

Nickel corrosion, also referred to as black pad, has been associated with the electroless nickel/immersion gold (ENIG) surface finish. Nickel corrosion occurs during the immersion gold deposition step. It occurs when the nickel deposit is compromised (uneven with deep crevices) in combination with an extended dwell time in an immersion gold bath, particularly if the bath is run beyond its intended life and outside the specified operating parameters such as temperature, pH and chemical concentrations. The expectation with ENEPIG is that these conditions would not be available due to the presence of the electroless palladium layer. However, nickel corrosion was observed in some instances with ENEPIG. Excessive nickel corrosion in an ENEPIG compromises the solderability of the surface finish and can give rise to wire bond lifts at the nickel interface.

The immersion gold reaction is an exchange reaction between the gold ions in solution and the substrate basis metal. The substrate metal (Ni or Pd) is oxidized to the respective metal ion, giving up electrons. The gold ion picks up electrons and is reduced to the gold. The driving force for these reactions follows the electromotive series.

The electromotive series is a list of metals whose order indicates the relative tendency to be oxidized, or to give up electrons. The electromotive series begins with the metal most easily oxidized (i.e., the metal with the greatest electron-donating tendency) and ends with the metal least easily oxidized. The tendency to be oxidized is called the oxidation potential and expressed in volts. The more negative the oxidation potential, the more readily oxidation takes place. The series is also called the replacement series, since it indicates which metals replace, or are replaced by, other metals. In general, a metal will replace any other metal lower in the series and will be replaced by any metal higher in the series.

The tendency to be oxidized is not an absolute quantity; it can only be compared with the tendency of some other substance to be oxidized. In practice, it is measured relative to a standard hydrogen electrode, which is arbitrarily assigned an oxidation potential of zero. Table 1 shows select common metals and their oxidation potential, which is a measure of their tendency to undergo the half reaction, in which some metal M loses n electrons e^-, and acquires a positive charge of M^{+n}, as in:

$$M \rightarrow M^{+n} + n\,e^-$$

Metal-Metal ion Equilibrium	Electrode Potential (v) vs Hydrogen
$Au - Au^{+2}$	+ 1.498
$Pd - Pd^{+2}$	+ 0.98
$Ag - Ag^{+}$	+ 0.799
$Cu - Cu^{+2}$	+ 0.337
$H_2 - H^{+}$	0.000
$Ni - Ni^{+2}$	- 0.250
$Fe - Fe^{+2}$	- 0.440
$Zn - Zn^{+2}$	- 0.763
$Al - Al^{+3}$	- 1.662

Table 1: Select metals and their oxidation potential.

The driving force for the reaction is the difference between the two half reactions (Equation 1).

The immersion gold reaction on nickel proceeds at a much faster rate than on palladium. The immersion gold reaction on palladium proceeds at a lower rate and can only achieve limited gold thickness. Immersion gold thickness on palladium is in the order of 1.2–2.0 µin (0.03 – 0.05 µm).

Immersion Gold on Nickel:

$$Ni \rightarrow Ni^{+2} + 2e \qquad -0.250v$$

$$Au^{+2} + 2e \rightarrow Au \qquad +1.498v$$

$$\text{Driving force} = 0.250v - (+1.498) = -1.740v$$

Immersion Gold on Palladium:

$$Pd \rightarrow Pd^{+2} + 2e \qquad +0.987v$$

$$Au^{+2} + 2e \rightarrow Au \qquad +1.498v$$

$$\text{Driving force} = +0.987v - (+1.498) = -0.511v$$

Equation 1.

The expectation is that nickel corrosion would not occur in ENEPIG as the gold ions have no direct access to the nickel. This would be true if the palladium layer is impervious to the gold ions. If the Pd layer is thinner (< 4 µin/ 0.1 µm), it is not totally impervious, and the gold ions may have access to the underlying nickel offering an easier path to immersion gold deposition. Nickel corrosion would occur. A thicker Pd layer (6–8 µin/0.15–0.2 µm), would go a long way towards preventing nickel corrosion.

The effect of the following attributes in creating nickel corrosion were investigated:

- Thickness of the electroless palladium layer
- Type of electroless palladium (phos vs non-phos)
- Type of immersion gold (standard immersion vs reduction assisted immersion gold)

Experimental and Results

The test vehicle (Figure 1) used in this study consisted of a double-sided, copper-clad laminated substrate which was copper plated to a thickness of 20 µm using an acid copper electroplating process. ENEPIG was deposited on the test vehicle using two different types of electroless palladium with two different types of gold. The nickel deposit (7-8 % phosphorous) was a single source and was deposited at a fixed thickness of 225-275 µin (5.6–6.9 µm). The electroless palladiums were a phos Pd with ~4.0% P in the deposit and a non-phos Pd (0% P). Two different gold baths were chosen for this investigation; the first was a standard immersion gold bath that ran at a mildly acidic pH of ~5.5 at a temperature of 180°F, the second gold bath was a "reduction-assisted immersion gold" bath also known as a "mixed reaction" bath. This bath is both an immersion and an autocatalytic (electroless) bath. The bath composition includes a reducing agent; the deposition of gold does not depend on substrate oxidation. All the plating was done using plating chemicals commercially available from C. Uyemura & Co.

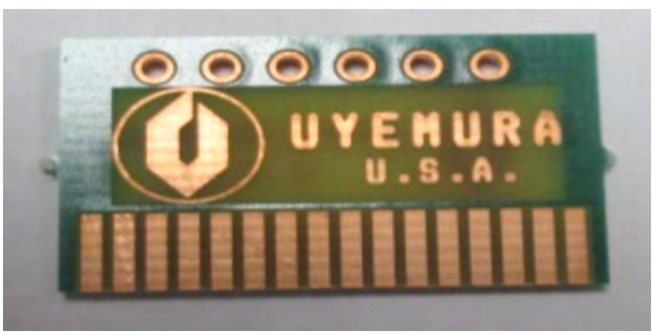

Figure 1: Test vehicle (2.4 x 1.5 cm).

The thickness of the palladium deposit was varied by changing the dwell time in the baths. The rate of deposition over time was recorded. The different thickness Ni-Pd layers were individually placed in the immersion gold bath for an exaggerated dwell time of 30 minutes. The exaggerated dwell in the gold bath was by design, to ensure that some level of nickel corrosion would occur and there would be a way to evaluate the difference that the thickness of the Pd layer would play in Ni corrosion.

Test #1: Varying thickness of phos palladium with standard immersion gold

Test #2: Varying thickness of non-phos palladium with standard immersion gold

Test #3: Varying thickness of phos palladium with reduction-assisted immersion gold

After each test, cross-sections through the ENEPIG layer at different palladium thickness were evaluated for Ni corrosion using a Seiko SEA-5120 Element Monitor MX XRF. The cross-section images of the pads were observed using a JEOL JSM-6010LA SEM.

Test #1: Phos palladium/immersion gold

Test #1 followed the process sequence outlined in Table 2. Six solder test coupons were plated in electroless nickel to fixed dwell time and nickel thickness. This was followed by electroless phos-palladium. The dwell time in the palladium bath was 1, 2, 4, 6, 8, and 10 minutes, giving rise to thickness that varied from 2-8.8 µin. The holes were cross-sectioned and examined.

Process Step	Dwell Time minutes	Test #1	Test #2	Test #3
Cleaner	5	O	O	O
Microetch	1	O	O	O
Activator	2	O	O	O
E'less Ni	20	O	O	O
E'less P-Pd(1)	1,2,4,5,6,10	X	O	X
E'less Pd(2)	1,2,4,5,6,10	O	X	O
IG Standard(3)	30	X	X	O
IG Mixed Rxn(4)	30	O	O	X

Process Sequence

1. Electroless Phos Palladium
2. Electroless Non-phos Palladium
3. Standard Immersion Gold
4. Reduction Assisted Immersion Gold

Table 2: Process Sequence.

Minutes In EP bath	EN µin/µm	EP µin/µm	IG µin/µm 30 mins
1	272/6.8	2.0/0.05	4.0/0.1
2	272/6.8	3.2/0.08	3.2/0.08
4	272/6.8	4.8/0.12	2.8/0.07
6	272/6.8	5.2/0.13	2.4/0.06
8	272/6.8	6.4/0.16	2.0/0.05
10	272/6.8	8.8/0.22	2.0/0.05

Table 3: Palladium thickness at different dwell times and the corresponding thickness of immersion gold for the different coupons for Test #1.

Figure 2 is a graphic presentation of the data from Table 3. The data shows that the gold thickness at the lower palladium thickness was as high as 4.0 µin (0.1 µm) and continued to diminish as the thickness of the layer increased and was limited to 2 µin (0.05 µm), when the thickness of the palladium was 8 µin (0.20 µm) or greater. The explanation is that the gold ions, at the lower thickness, had access to the underlying nickel and proceeded to deposit at an accelerated rate, producing nickel corrosion. In absence of availability of the underlying nickel, the immersion gold reaction with phos palladium becomes self-limiting to 2 µin (0.05 µm).

Figures, 3, 4 and 5 are SEM micrographs depicting the level and type of corrosion at different levels of phos palladium thickness. Figure 3 shows shallow extensive corrosion and a thicker gold deposit; Figure 4 shows intermittent deep corrosion spikes and a gold thickness of 4.8 µin (0.12 µm); and Figure 5 has no corrosion spikes, however the gold thickness was limited to 2 µin (0.05 µm).

Test #2 Non-phos palladium/immersion gold

Test #2 followed the process sequence outlined in Table 2. Six solder test coupons were plated in electroless nickel to fixed dwell time

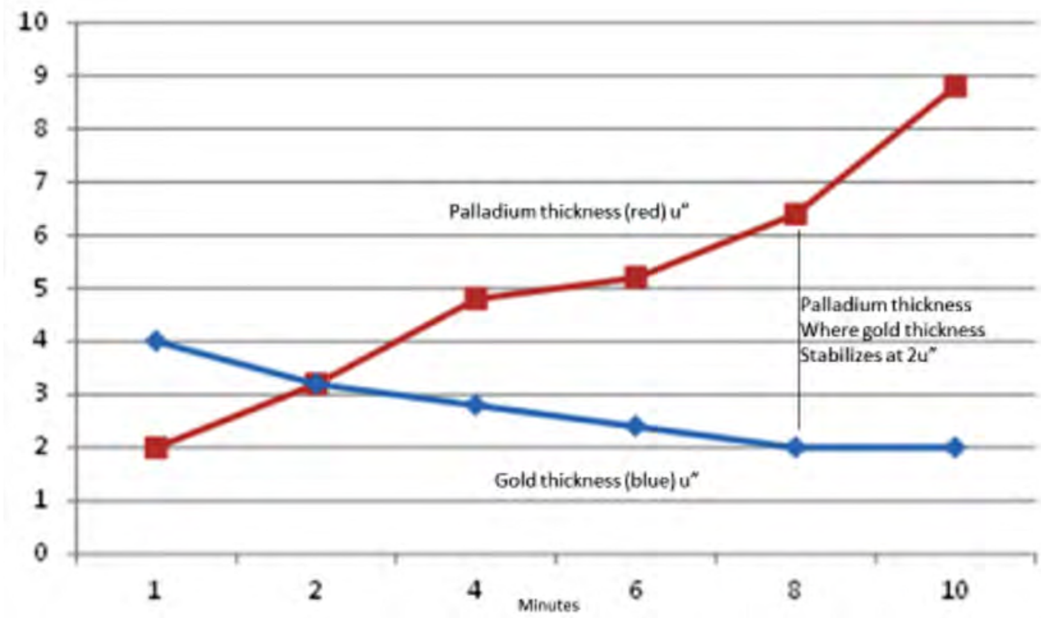

Figure 2: Chart of phos-palladium and gold thicknesses vs. time in the palladium bath.

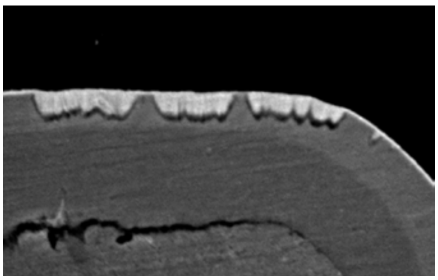

Figure 3: Nickel corrosion at 2 µin (0.05 µm) of phos palladium. Corrosion was extensive and shallow.

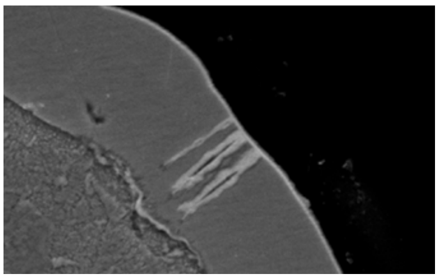

Figure 4: Ni corrosion at 4.8 µin (0.12 µm) of phos palladium. Few intermittent deep corrosion spikes.

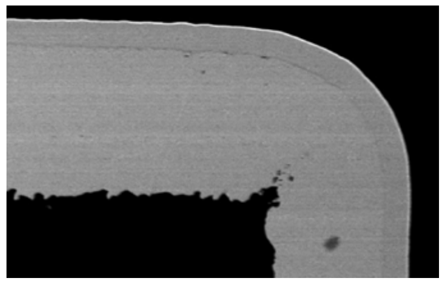

Figure 5: No corrosion at 8.8 µin (0.22 µm) of phos palladium. No corrosion was found.

and nickel thickness. This was followed by electroless non-phos palladium. The coupons' dwell time in the palladium bath was 1, 2, 4, 6, 8, and 10 minutes, giving rise to thickness that varied from 2–10 µin (0.05–0.25 µm) of palladium. All six samples were then immersed into the immersion gold bath for 30 minutes at 180°F. The holes from each coupon were then cross-sectioned. Using the SEM, twenty corners were evaluated for nickel corrosion at 5000 and 1000X.

Figure 6 is a graphic presentation of the data from Table 4. The data shows that the gold thickness at the lower palladium thickness was as high as 3.2 µin (0.06 µm) and continued to diminish as the thickness of the palladium in-

Minutes in Non- Phos Palladium	EN µin/µm	EP µin/µm	IG µin/µm 30 mins
1	272/6.8	1.6/0.04	3.2/0.08
2	272/6.8	2.4/0.06	2.8/0.07
4	272/6.8	3.6/0.09	2.0/0.05
6	272/6.8	5.6/0.14	1.2/0.03
8	272/6.8	7.6/0.19	1.2/0.03
10	272/6.8	9.2/0.23	1.2/0.03

Table 4: Thickness of the different coupons for Test #2 with non-phos palladium.

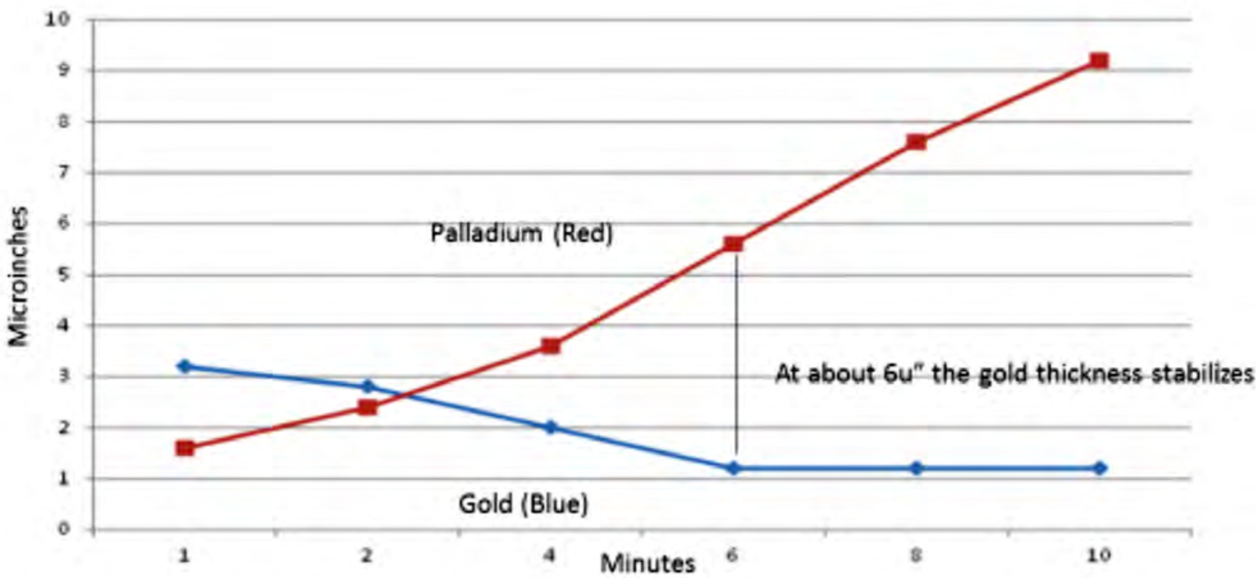

Figure 6: Chart of non-phos palladium and gold thicknesses vs. time in the palladium bath.

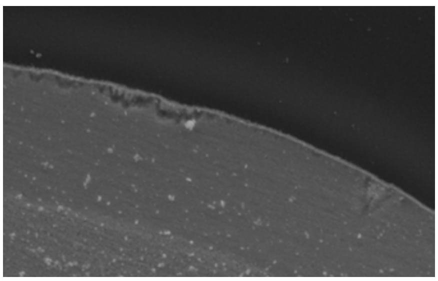

Figure 7: Non-phos palladium at 1.6 µin (0.04 µm). Corrosion was extensive and shallow.

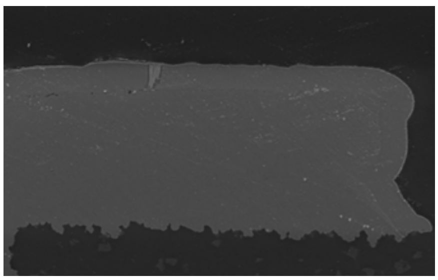

Figure 8: Non-phos palladium at 3.6 µin (0.09 µm). Very intermittent deep corrosion.

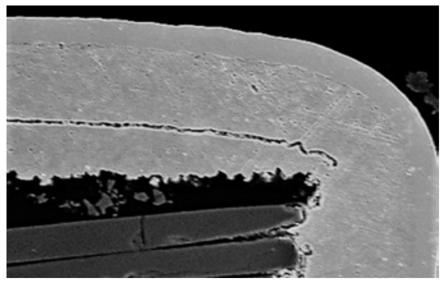

Figure 9: Non-phos palladium at 7.6 µin (0.19 µm). No corrosion.

creased and was limited to 1.2 µin (0.032 µm) , when the thickness of the EP was 5.6 µin (0.14 µm) or greater. The explanation is that the gold ions, at the lower palladium thickness, had access to the underlying nickel and proceeded to deposit at an accelerated rate, producing nickel corrosion. In absence of availability of the underlying nickel the immersion gold reaction with non-phos palladium, becomes self-limiting to 1.2 µin (0.03 µm).

Figures 7, 8 and 9 are SEM micrographs depicting the level and type of corrosion at different levels of non-phos palladium thickness. Figure 7 shows extensive very shallow corrosion and a thicker gold deposit, 3.2 µin (0.08 µm); Figure 8 shows intermittent deep corrosion spikes and a gold thickness of 2.0 µin (0.05 µm); and Figure 9 has no corrosion spikes, however, the gold thickness was limited to 1.2 µin (0.03 µm).

Under the conditions of the test (the 30 minutes extended dwell time in the gold bath) the data from the non-phos palladium shows similar trends as the phos-palladium data. At the lower thickness corrosion of the nickel will occur, and at a thickness greater than 6.0 µin (0.15 µm) no corrosion occurs and the gold thickness is limited to 1.2 µin (0.03 µm).

Figure 10 is a graphic presentation of the data from Table 5. The data shows that the gold thickness of the reduction-assisted or mixed-reaction immersion gold was virtually independent of the phos-palladium thickness. Gold continued to deposit at a high rate when

Nickel Corrosion in ENEPIG

TEST #3 Deposit Thickness

TEST #3
Phos palladium thickness at different dwell times and the corresponding thickness of "Reduction Assisted" immersion gold for the different coupons for Test #3

Minutes in Non-Phos Palladium	EN µin/µm	EP µin/µm	IG µin/µm 30 mins
1	255/6.4	1.5/0.04	8.73/0.22
2	255/6.4	2.1/0.05	8.05/0.20
4	255/6.4	3.6/0.09	7.28/0.18
6	255/6.4	4.9/0.12	7.24/0.18
8	255/6.4	6.5/0.17	7.30/0.18
10	255/6.4	7.7/0.19	6.96/0.17

Table 5: Phos-Pd with reduction-assisted immersion gold.

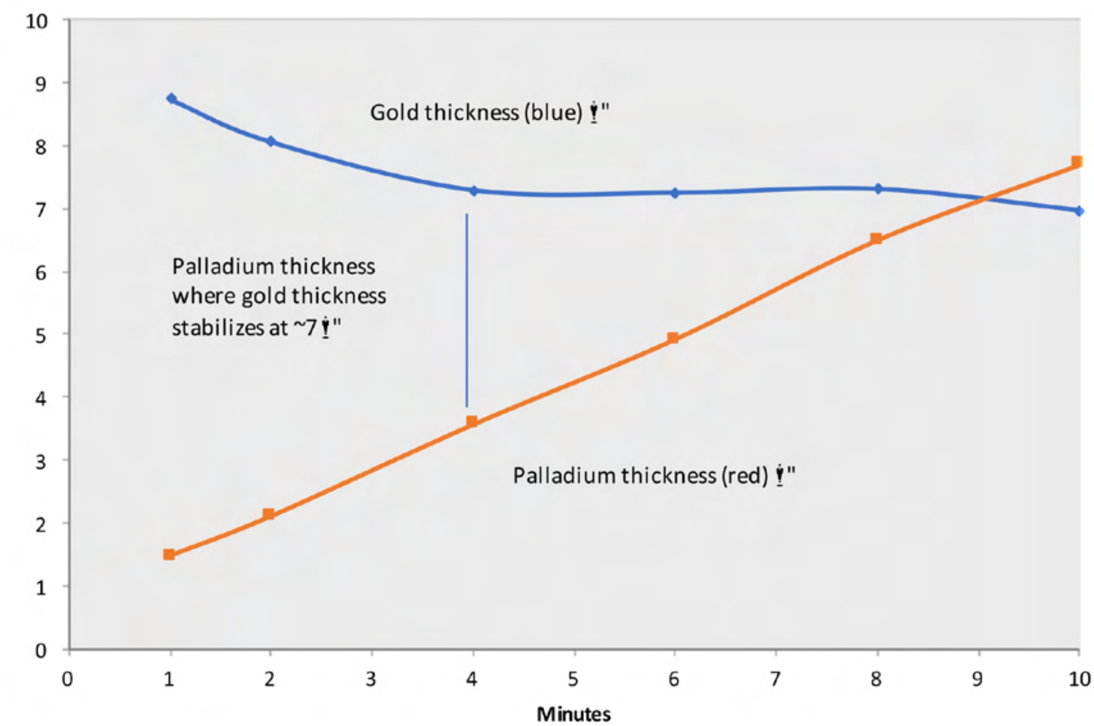

Figure 10: Chart of phos palladium with reduction-assisted immersion gold vs. time in the palladium bath.

the phos-palladium thickness was as high as 7.7 µin (0.19 µm). No signs of nickel corrosion were found at any level of palladium thickness (Figure 11).

Mitigation of Nickel Corrosion

The data clearly indicates that increasing the thickness of the palladium layer in the range of 6-8 µin would go a long way towards minimizing nickel corrosion in ENEPIG. Presently, the IPC-4556 specification for ENEPIG specifies for 2–12 µin (0.05–0.3 µm) for the EP layer and 1.2-2.8 µin (0.03–0.07) µm for IG. The authors of this paper recommend increasing the lower limit of EP thickness to 7 µin (0.18 µm).

The increased dwell time in the immersion gold bath, to achieve higher thickness of the IG, will create a level of nickel corrosion, par-

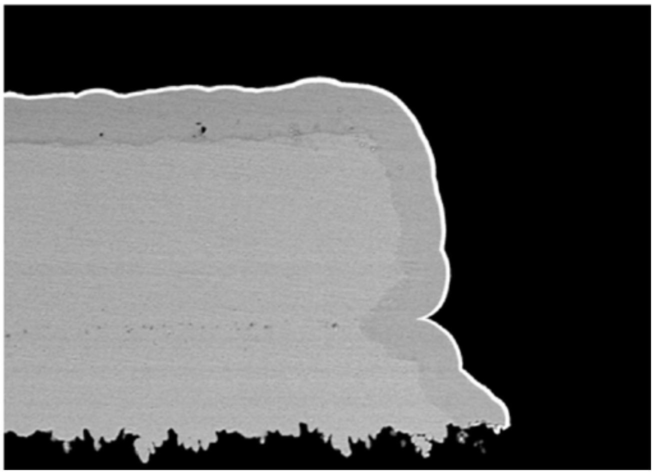

Figure 11: Phos palladium with reduction-assisted immersion gold.

ticularly at the lower EP thickness. The IG gold bath should be run per vendor specification as far as gold concentration, temperature, pH, dwell time and age of bath or MTOs (metal turnovers). If a thicker layer of immersion gold is a design criterion, immersion gold should be substituted for “Reduction Assisted” immersion gold. This type of gold bath will deposit gold up to 8 µin (0.2 µm) without any Ni corrosion in an ENEPIG deposit.

Conclusion

Nickel corrosion in ENEPIG was reproduced using exaggerated dwell time in the immersion gold bath. Nickel corrosion will occur at the manufacturing site if there is an attempt to plate thicker (> 2.8 µin (0.07 µm) gold with standard immersion gold chemistry.

The gold thickness in the ENEPIG surface finish is specified (IPC-4556) at 1.2–2.8 µin (0.03–0.07 µm). Meeting this specification using standard immersion gold should not create any nickel corrosion.

A different gold bath specifically “Assisted Reduction Immersion Gold” was shown to be capable of depositing higher thickness of gold without compromising the nickel substrate. **PCB007**

This article was originally presented at SMTA International 2017 and published in the proceedings.

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Army Researchers Teaching Robots to Be More Reliable Teammates for Soldiers

Researchers at the U.S. Army Research Laboratory and the Robotics Institute at Carnegie Mellon University developed a new technique to quickly teach robots novel traversal behaviors with minimal human oversight.

The technique allows mobile robot platforms to navigate autonomously in environments while carrying out actions a human would expect of the robot in a given situation.

The experiments of the study were recently published and presented at the Institute of Electrical and Electronics Engineers’ International Conference on Robotics and Automation held in Brisbane, Australia.

ARL researchers Drs. Maggie Wigness and John Rogers engaged in face-to-face discussions with hundreds of conference attendees during their two-and-a-half-hour interactive presentation.

According to Wigness, one of research team’s goals in autonomous systems research is to provide reliable autonomous robot teammates to the soldier.

Source: U.S. Army

MilAero007 Highlights

It's Time to Retire ROSE Testing ▶

The transition from predominantly water wash processes to "no clean" has meant the advent of very different flux compositions. The question has been posed as to whether the ROSE test is still a viable option for evaluating PCB and PCBA cleanliness.

Global Electronic Warfare Market to See CAGR of 6.2% from 2017-2026 ▶

The Global Electronic Warfare market is accounted for $22.19 billion in 2017 and is expected to reach $38.31 billion by 2026, growing at a CAGR of 6.2%.

Compass Call Electronic Warfare System Moving to Modern Business Jet ▶

BAE Systems has begun work to transition its advanced Compass Call electronic warfare (EW) system from aging EC-130H aircraft to a modern, more capable platform that will improve mission effectiveness.

Solving the Challenges of 'Flying Microgrids' ▶

As the role of satellites for communications, navigation, research and defense continues to grow, researchers say there is a need to address a number of unique challenges faced by satellite power systems.

Nano Dimension Partners With AURORA Group for China Distribution ▶

Nano Dimension has entered the Chinese market with a strategic partnership with the AURORA Group. The AURORA Group will market and sell Nano Dimension's award-winning DragonFly 2020 Pro 3D printer for electronics to customers in China.

Digital Transformation Key to Survival in Aerospace & Defense ▶

Despite solid profits in recent years and a decade of stock market outperformance, the global aerospace and defense (A&D) industry cannot afford to be complacent in the face of an increasingly dynamic business environment.

Electronics Industry Supports Senate Bill to Advance Workforce Education ▶

IPC—Association Connecting Electronics Industries, representing the $2 trillion global electronics industry, applauds a U.S. Senate committee for its work in advancing a workforce education and training bill.

Lyncolec Receives prEN9100:2016 (AS9100D) Certification ▶

SCL PCB Solutions Group announced that its manufacturing subsidiary Lyncolec has been awarded with certification for prEN 9100:2016 (technically equivalent to AS9100D and JISQ 9100:2016) and ISO9001:2015.

Cirexx Achieves AS9100D Certification ▶

Cirexx International has acquired AS9100D Standard Certifications in only four months. The AS9100 Quality Management System (QMS) is a rigorous standard for organizations that design and manufacture products for the defense and aerospace industries.

Collaborative Robots and Digital Technology Signal Creation of the 'Factory of the Future' ▶

The cobotic workstation, a key feature of the factory of the future, is fitted with a range of digital technology and will be piloted at the company's Warton, Lancashire site.

Panasonic

For Millimeter-wave Band Antennas NEW Material replacement of PTFE

Halogen-free Ultra-low Transmission Loss Circuit Board Material

R-5515

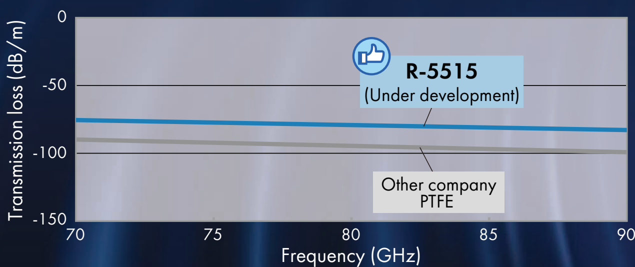
Under Development

Features

- Low transmission loss (Equality or Better than PTFE)
- Dk 3.0 Df 0.0019@10GHz
- Reduce PCB process cost (vs. PTFE)

Transmission Loss

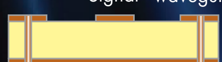
- **Frequency dependence by Transmission loss (70-90GHz)**



- **Transmission loss at 79GHz**

Material	Transmission loss (dB/m)	Dk (Design)
R-5515	79	3.22
Other company PTFE	96	3.14

- **Construction**



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A Tale of Zinc Tails

Trouble in Your Tank
Feature Column by Michael Carano, RBP CHEMICAL TECHNOLOGY

Introduction

Copper foil used in the fabrication of printed circuit boards is subjected to a plurality of copper layer treatments, including a roughening treatment followed by a locking or gilding treatment to form a matte surface on the copper foil. The matte surface is then coated with a thin layer of zinc and heated to produce a brass layer that provides the copper foil with sufficient bonding sites to enhance the interlaminar bond strength between the resin and the copper foil. This brings me to a tale—a zinc "tail"—but what exactly is a zinc tail?

Origin of the Zinc Tail

An electrodeposited copper foil to be laminated on a substrate for a PCB is treated with either a brass or zinc coating. This barrier layer serves several purposes, including improving the adhesion of the foil to the laminate resin materials and acting as a diffusion barrier. How does this play into the creation of the zinc tail?

The mechanism, while not well understood, is believed to have its origins after the use of plasma for desmear/etchback. In particular, the zinc tail is prominently visible if plasma provides a three-point connection (Figure 1).

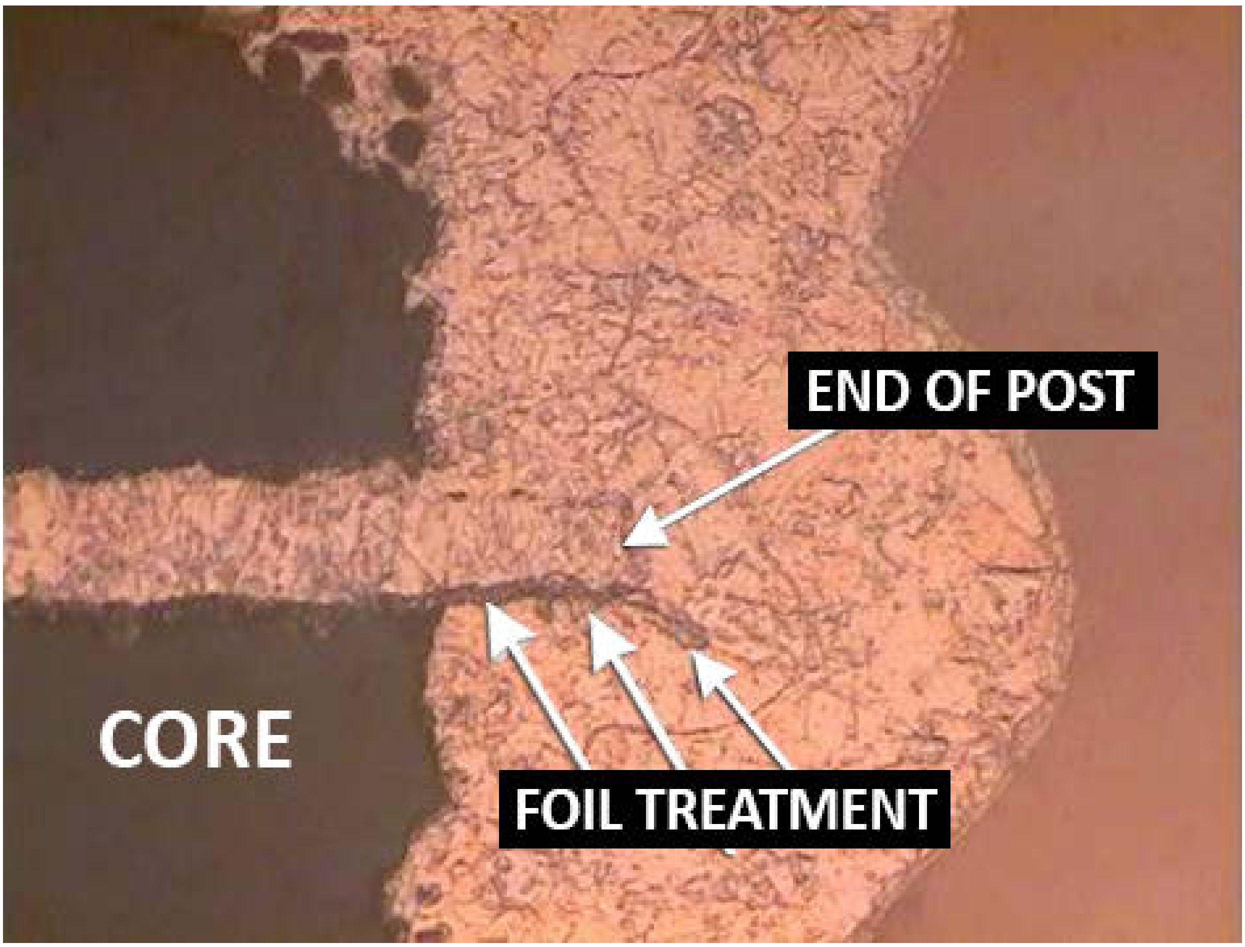
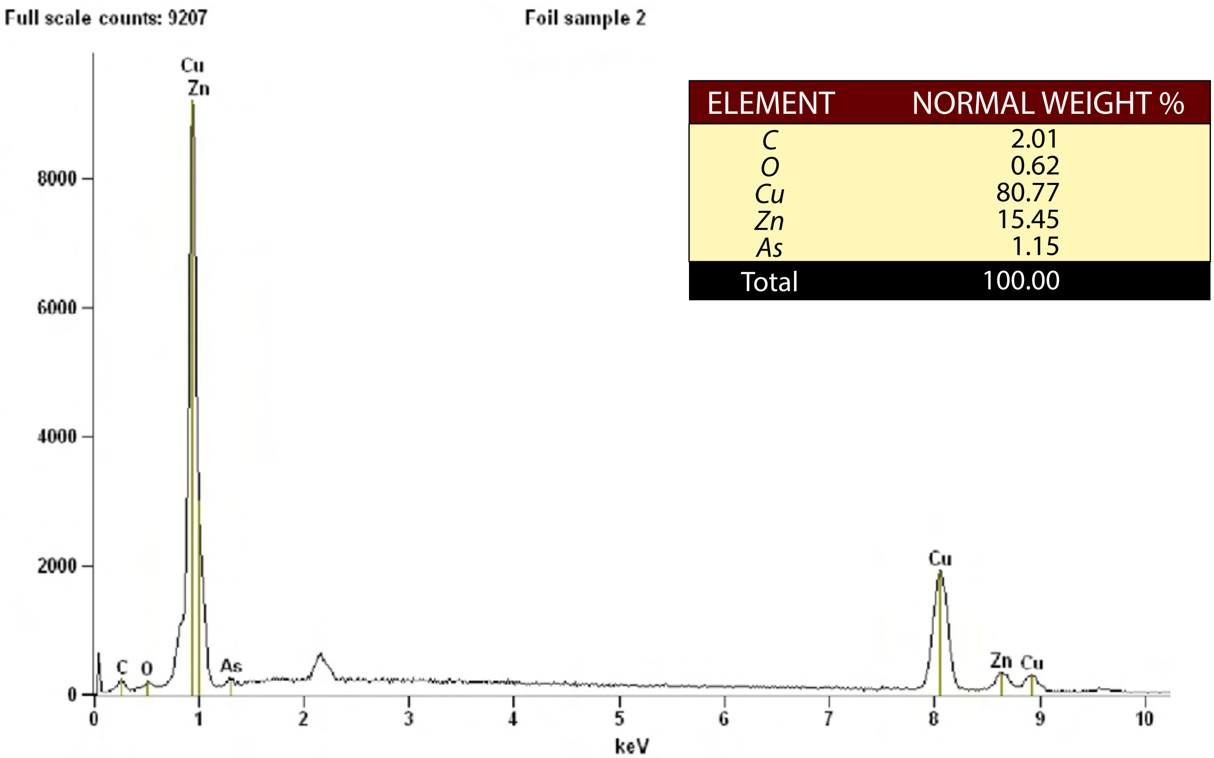


Figure 1: Zinc tail at C-stage to copper interface.



ELEMENT	NORMAL WEIGHT %
C	2.01
O	0.62
Cu	80.77
Zn	15.45
As	1.15
Total	100.00

Figure 2: SEM/EDAX results of protruding area and foil treatment shown in Figure 1.

In Figure 1, the protruding foil treatment (tail) extends from the foil into the electrolytic copper. Several fabricators have documented this condition and the subsequent degradation of PTH reliability after thermal excursions. It is easy to see why the zinc tail left unremoved would act as a fulcrum causing weakening in the plated through-hole (PTH). Another issue is that the tail may be misinterpreted as poor adhesion of the electroless copper deposit.

Figure 2 shows the results of the SEM/EDAX of the protruding tail. One can easily see the high level of zinc present.

Figure 3 shows another example of the zinc tail as it protrudes into the via. Subsequent metalization is forced to plate around the tail.

Zinc Tail as a Possible Cause of PTH Failures

Thermal cycling leads to the majority of failures in the plated through-hole. It is also critical to put in perspective the environment in which the circuit board will be used. A harsh-use environment (HUE), such as automotive applications under the hood or on an engine, qualifies as the most severe of environments. Reliability testing should simulate the thermal excursions of a PTH throughout its life. This would include thermal cycling at temperature extremes of -40°C to +125°C. In addition, the most severe thermal cycles are experienced during assembly and rework. Thus, simulating assembly reflow and rework cycles will provide a more in-depth understanding of the board's long-term reliability. More to come on this topic in a future column.

As previously mentioned, the concern is that the protruding zinc tail, if not removed prior to metalization, will lead to stress points within the electrodeposited copper at a minimum. If one clearly studies the failure hierarchy within the PTH, one surmises that the plated-through via expands quite rapidly in the Z-axis at a temperature above the Tg of the resin material. During these temperature excursions, the PTH acts as a rivet working to resist expansion. However, when there are various anomalies in the PTH, including protruding glass fiber bundles and zinc tails, stress points are introduced. Remember, the weakest link in the

Figure 3: Zinc tail evident on C-stage.

chain breaks first. If the chain's weakest link is thin-plated or brittle copper, then one can expect the failure to occur at this point. Keep in mind that the number of thermal cycles to failures is affected by the strain imposed on the PTH during each cycle. Thus, the concern with additional strain created by the protruding zinc tail.

Regardless, it is a given that the zinc tail can have a negative impact on PTH thermal reliability. Therefore, it is best to understand how to minimize its formation, or at least provide a means to mitigate the negative effects of the zinc tail.

One way to remove zinc is to be somewhat aggressive with the microetch prior to electroless copper plating. Strong acids, such as hydrochloric acid, will also remove the zinc without etching the copper interconnects. I recommend that if zinc tails become an issue, testing of acid soak cleaners, such as hydrochloric acid-based and persulphate-based microetchants, be evaluated. **PCB007**

Michael Carano is VP of technology and business development for RBP Chemical Technology. To reach Carano, or read past columns, click here.

Factors of Reliability

The Sum of All Parts

Feature Column by Sam Sangani, PNC INC.

A popular definition of reliability is "The quality of being trustworthy or of performing consistently well." Upfront engineering is of utmost importance in developing a design that will endure its intended life cycle. On the other hand, the manufacturing of that design is just as critical. Both processes go hand in hand and are equally as important. As a PCB manufacturer and a PCBA assembler, I take a look this month into some of the critical areas of manufacturing that play a role in determining a reliable product. There are four specific areas—quality suppliers, SPC, in-process verification and testing, and preventive maintenance—that will help increase the reliability of end user electronic parts (Figure 1).

Quality suppliers are the backbone of any manufacturer to achieve continuous reliability. End-user reliability often starts with its manufacturer's suppliers when it comes to quality, on time delivery of raw materials, defect-free materials, technical support, and responsiveness to issues. Sub-par materials or counterfeit parts will adversely affect reliability and must be safe-guarded by continually assessing your supply chain. Monitoring and measuring suppliers is a necessity to maintain consistency and quality control within the process flow. Suppliers need to be monitored through the Key Performance Indicators that are most critical to manufacturing, and they need to be periodically reviewed to ensure each supplier is performing to specific quality standards.

The electronics industry is constantly changing, with trends toward smaller parts and new materials. This creates a possible need to add new suppliers to your approved supplier list. In saying that, it's imperative that they go through an assessment. This assessment may consist of a standard audit survey, onsite audit, or meet a specific certification such as ISO, AS9100, MIL-Spec, etc., which will identi-

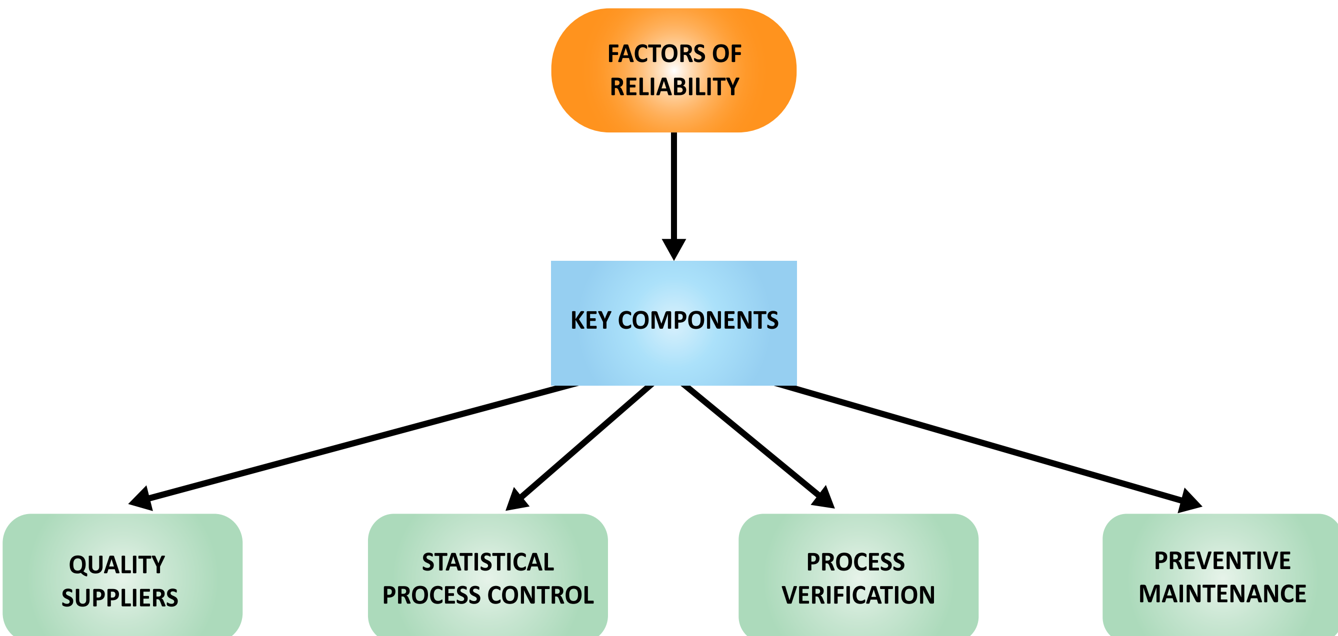


Figure 1: Critical areas for determining a reliable product.

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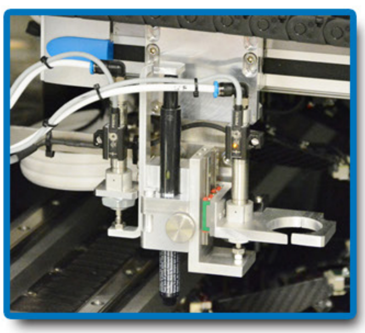

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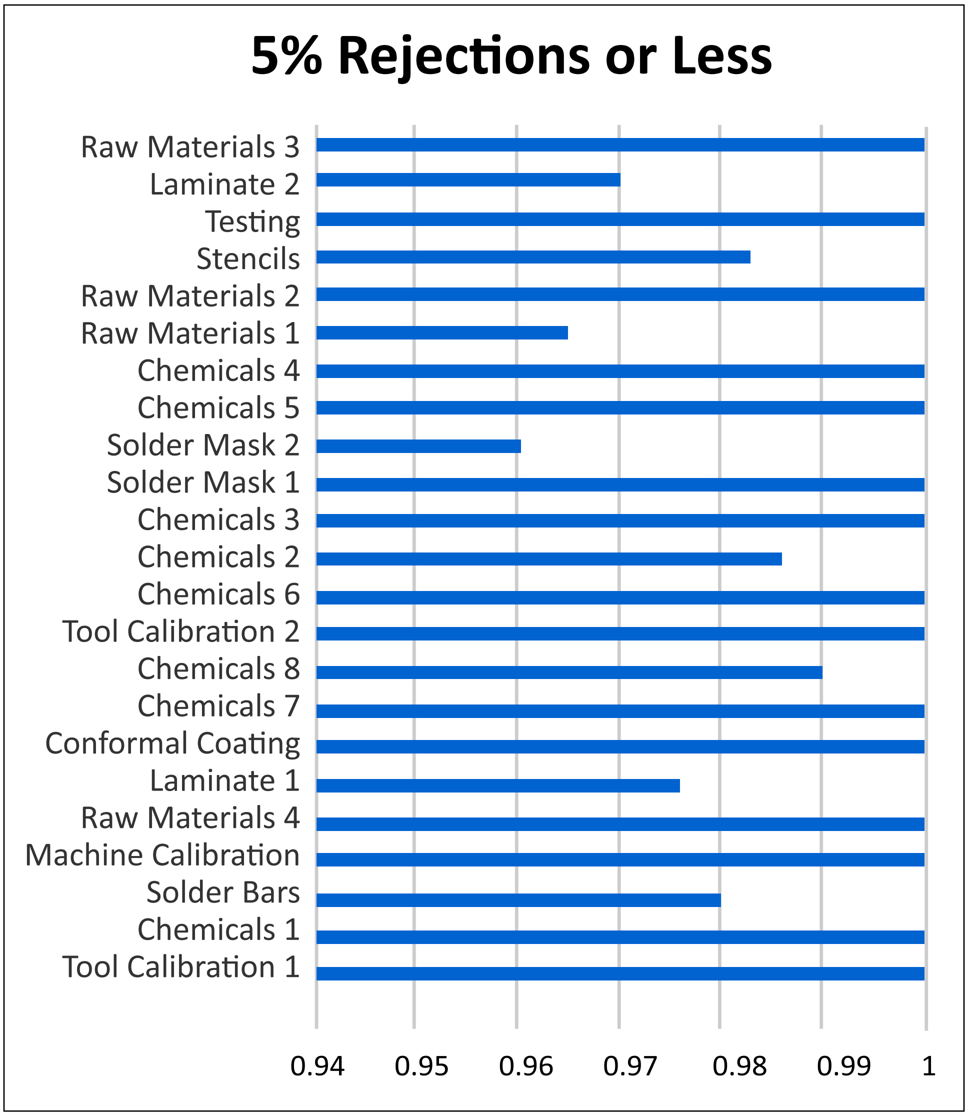


Figure 2: Sample supplier list.

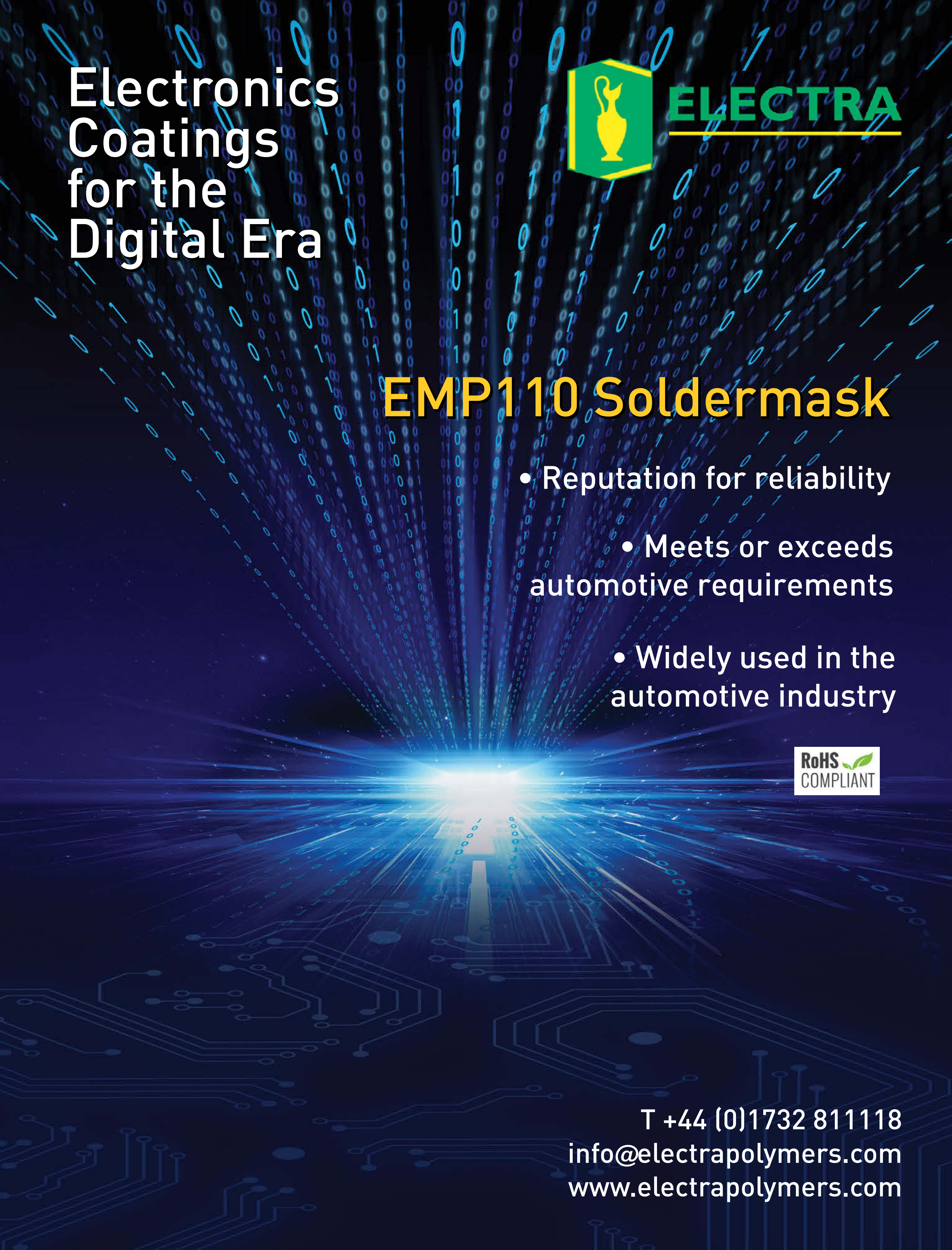
fy their commitment to their product. Product reliability starts with a good base of material suppliers (Figure 2).

Statistical process control is the number one factor that drives quality, which in turn derives a reliable product to its customers. Each departmental process should be broken down into specific process defects. Those defects should be noted and documented for every piece that makes its way through the manufacturing process, whether it be bare board manufacturing or electronic assembly. A defect analysis matrix for all departments should also be reviewed daily, to recognize spikes or leading defect contributors in that department process. Whether a spike or leading defect contributor, they must be analyzed and measures put in place to reduce the defect which also requires monitoring by continuous tracking.

An actual example taken from PNC Inc. showed that 20% of all defect scrap was being generated from electrolytic copper plating line due to pitting and mouse bites (Figure 3). With combined technical support from their chemical suppler, along with their inhouse lab and engineering staff, it was determined that the acid cleaner being used was not cleaning the panels sufficiently prior to the plating process. Continuous tracking from September of 2017 shows the defect rate from the plating line has been reduced to less than 3%, with the addition of a new acid cleaner.

In-process verifications and testing through the manufacturing process flow is highly recommended to maintain not only product quality, but product reliability. In-process verifications can be broken down into two categories: part verification at each process step and the process step itself. Testing is typically a standalone process step.

Part verification at each process step can be monitored in various ways, such as a first piece article check, or part AQL checks. For example, the routing process (of a PCB from a panel) would most likely be an FAI check. The FAI will indicate that the part is dimensionally correct within the stated tolerances. An example of an AQL may be to dimensionally check the same routed pieces in the final inspection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DEFECT ANALYSIS				
Defect		Boards Scrap	Panels Scrap	Percent
FF1	EXPOSED COPPER	659	29.90	3.89
EH1	OVER ETCHED	557	30.01	3.29
RT4	ROUTE (ROUGH EDGES)	382	14.01	2.26
P1	PITTING	306	17.90	1.81
AO1	Opens	282	44.88	1.67
FL7	HAL PLUGGED HOLES	255	22.80	1.51
IM3	DEVELOPING	250	45.27	1.48
DR9	DRILL REGISTRATION	215	24.36	1.27
FL2	DIMENSIONAL REJECT	71	3.18	0.42
P2	MOUSE BITES	35	3.17	0.21
L4	SOLDERMASK ON PADS	33	2.90	0.20

Figure 3: Sample defect analysis.

step to ensure the repeatability from the routing step.

An example of part verification during the assembly process step of pick and place would require an FAI. The FAI will indicate whether parts are missing, skewed, misplaced, proper polarity, correct rotations, etc. This is a very critical step that needs attention prior to reflow to eliminate rework. Rework can be a major contributor to end-product reliability.

When it comes to PCB testing, be sure that your PCB manufacturer is 100% electrical testing your parts. Standard continuity testing is typically 100 V, 50 mA, 10 ohms (low resistance), and 10 megaohms (high resistance). The testing should also be documented and supplied with your PCBs as verification.

Assembly testing can be performed at various levels depending on your requirements. Full functional burn-in testing is obviously the best method for reliability purposes, but again, depending on the design, the assembled part may only require some voltage input/output testing. Partial functional tests may be sufficient for reliability based on the function of the design. For mass production assembly runs, flying probe tests are a cost-effective and highly reliable means of testing for end-product reliability.

Preventive maintenance within a manufacturing facility is extremely crucial to quality and ultimately, for product reliability. This is an area that can be often overlooked and difficult to schedule due to day-to day operations and constant work flow. Along with employees, equipment is the heartbeat of the company. Imagine if you never maintained your etcher and half the conveyor rollers are bound up with crystalized ammonia and you're running an impedance control job. Most likely the impedance control traces will be under-etched causing impedance readings either out of spec, or on the edge of their tolerance. There are 35 different process steps when fabricating a simple two-layer PCB; if no PMs were performed at those process steps, I think it's obvious what the result would be.

These three examples are just a microcosm of things to be checked, monitored, and analyzed during and after the manufacturing process of electronic parts. Other process controls such as employee training, calibrations, and inventory control all pertain to product reliability in one way or another. When choosing a PCB manufacturer or PCB assembler, be sure it's the right fit for your company. I have found that a company's web page says a lot about the nature their business. Take the time to ask questions, maybe even visit or audit their facilities, don't just rely on the lowest price, as price can certainly be a contributor to end-product reliability. **PCB007**

Sam Sangani is president of PNC Inc.

Mina: RFID, LED and What Else?

Flex Talk

by Tara Dunn, OMNI PCB

"The science of today is the technology of tomorrow." This Edward Teller quote is an apt description of the Mina product. This advanced surface treatment, recently developed to enable low-temperature soldering to aluminum in the RFID market, is not only finding success in that market, but quickly finding a home in other markets, including the LED market, where the incentive is both cost and improved LED performance. I recently had the opportunity to speak with Divyakant Kadiwala, from Averatek, to discuss the development of Mina and potential applications for this surface treatment.

The science behind the ability to solder to aluminum can be summarized as the battle against aluminum oxide. Removing the oxide is easy but keeping it from reforming is extremely hard in ambient conditions. Development was focused on coming up with a surface treatment that removes this oxide at the correct temperature—the temperature at which solder reflows (Figure 1). This would ensure the formation of a strong bond between the bare aluminum and molten solder as it cools down. This advanced surface treatment is enabling technology across more than one market.

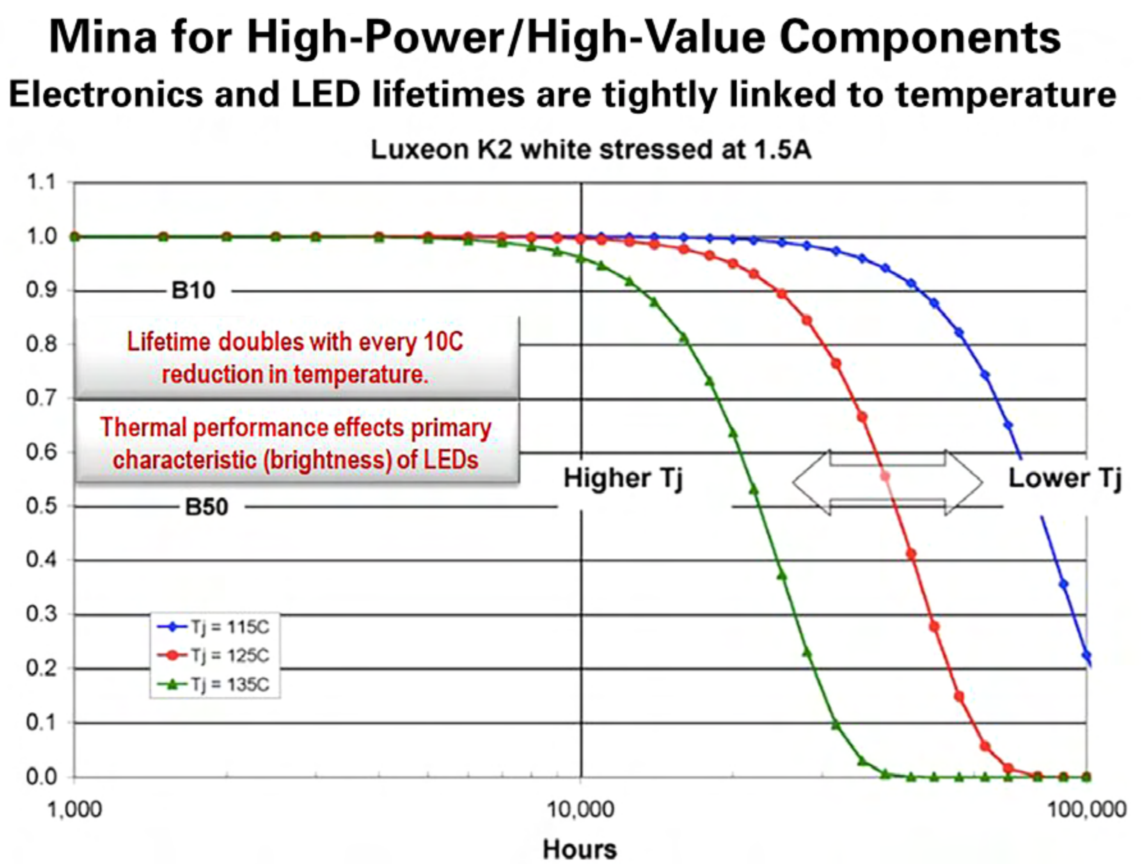


Figure 1: LED performance improvement per 10°C drop in temperature. (Source: Averatek)

RFID Tag Market

This surface treatment was originally designed for the high-volume RFID tag market. For cost reasons, aluminum-polyester (Al-PET) materials are a preferred choice, but this material does present some challenges. Aluminum is difficult to solder to at lower temperatures and PET cannot withstand high temperatures. Soldering to aluminum is difficult because of the presence of a thin layer of aluminum oxide that is present when Al-PET is exposed to air. The oxide can be removed with extensive wet chemistry but adds cost and makes this material cost prohibitive in high volume. Anisotropic conductive paste (ACP) is a common solution to this challenge and is widely used for attaching components to aluminum-based RFIDs. It is applied to the face of the chip, which is attached to the antenna using heat and pressure. However, ACP has its own challenges. It is typically syringe applied, requires longer cure times, has pot-life issues and is electrically inferior to conventional solders. In addition, it must be stored at low temperatures in special freezers to control the polymerization of the epoxy.

LED Market

As Mina is entering the market and people are learning more about it, discussions of applications in other industries are happening and other potential uses are being explored. One prominent market also poised to benefit from Mina is the rapidly growing LED market. According to a study from Zion Market Research, the LED market is predicted to have a 13% CAGR from 2107 to 2022, with an estimated market of $54 billion in 2022.

In the LED market, Mina can both lower cost and improve performance. The underlying goal for better performance in the LED market is keeping the LED cooler. One segment of the LED market, using thinner aluminum and less expensive materials, has similarity to the RFID tag market. Currently, base materials vary between copper-PET laminate and aluminum-PET laminate. Applications using Al-PET materials also typically bond to aluminum using the conductive epoxy method mentioned earlier. The use of Mina in these applications results in a true metal-to-metal bond that improves both the electrical performance and the thermal conductivity (Figure 2). As a result, the LED stays cooler.

Oftentimes in this segment of the market, copper-PET materials are being used when the conductive epoxy approach to assembly does not provide the needed performance. Mina would enable the adoption of the Al-PET materials which can reduce the cost of the base materials by 80%. Once Mina is applied, the traditional soldering process used on copper-PET circuits can be performed.

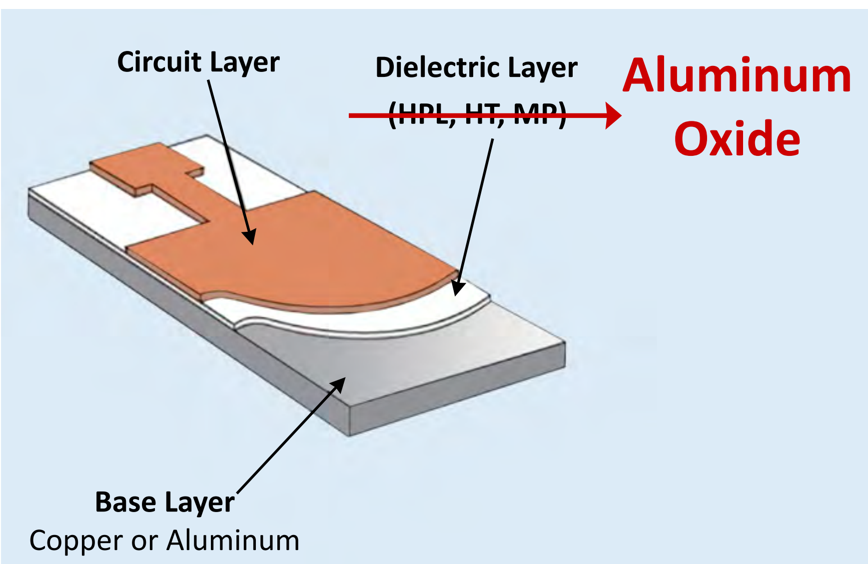


Figure 2: Aluminum oxide as a dielectric layer.

In the high-power LED segment of the market, thicker copper with a polymer dielectric is most commonly used. This dielectric does provide some thermal performance. The introduction of Mina has provided another option for consideration and improved performance of LEDs. LED systems typically consist of a package, board and heat-sink. The package consists of the LEDs with two leads, and a separate thermal pad in case of high power LED systems. The traditional board can be eliminated by

the combination of Mina and Averatek's ALD additive circuitry process. Alumina, the anodized layer of aluminum, is a thermally conductive, electrically insulated dielectric layer. From a 10,000-foot view, Averatek's ALD ink additive circuitry process generates the copper traces directly on the alumina or dielectric layer. Mina can be used to solder both leads that need to be electrically grounded and the thermal pads, directly to the aluminum. This can be done by masking the bonding areas when anodizing the aluminum prior to building the copper traces and then applying Mina to those previously masked areas allowing soldering to the aluminum. This provides better thermal management and significantly improves performance.

Mina has been developed to work with standard screen printing, baking and assembly equipment. This allows a simple adoption without incurring significant capital equipment costs. As a new with benefits to two markets, I have to wonder which industry will be next to discover Mina. Hard disk drives? Connectors? Shielding wire and cable? Mina is an excellent example of innovation and technology development benefiting multiple segments in the rapidly changing electronics industry. **PCB007**

Tara Dunn is the president of Omni PCB, a manufacturer's rep firm specializing in the printed circuit board industry. To read past columns or to contact Dunn, click here.

Sensor Technology to Improve Safety and Health in Aged Care

Flexible sensors developed at RMIT will be integrated into new health monitoring technology to improve aged care, in a project supported through a $1.7 million Federal Government grant.

The $1.7 million Cooperative Research Centre Projects (CRC-P) grant has been awarded to Melbourne-based research and advanced manufacturing company Sleeptite, which is leading the development of the non-invasive health care monitoring program. Assistant Minister for Science, Jobs and Innovation Senator Zed Seselja, announced the CRC-P grant at RMIT's Micro Nano Research Facility.

The Sleeptite collaboration brings together a multi-disciplinary team in sensing, micro-technology, health data analytics and bedding manufacturing that will deliver new Australian-made products for the aged care and assisted living sectors.

RMIT researchers led by Associate Professor Madhu Bhaskaran will work to integrate their flexible, unbreakable electronics into bedding products to enable the real-time monitoring of health and sleep.

Bhaskaran said while some technologies existed to improve monitoring, they were either too expensive for wide implementation or unreliable.

"What we're developing is a cost-effective way to improve the supervision and monitoring of people living in aged care and assisted living facilities, especially at night," she said.

The new technology is designed to give nurses and aged care facility managers greater insight into the health and well-being of patients. By alerting health care workers to movements, the technology aims to minimise night time disruption and deliver better quality of life for residents.

Source: RMIT University

Recent Highlights from PCB007

1 EIPC 50th Anniversary Conference Day 1: The Past, the Present and the Future, Pt. 1 ▶


John Ling and Michael Weinhold

Just like old times—meeting with John Ling, with whom I had previously travelled to industry events for over two decades, and who still carries the role of EIPC marketing manager, to fly together from Birmingham UK to Dusseldorf in Germany for the EIPC 50th Anniversary Summer Conference.

2 EIPC 50th Anniversary Conference Day 2: The Past, the Present and the Future, Pt. 1 ▶

The sun was shining in Dusseldorf as delegates returned to the conference room for the second day of the EIPC 50th Anniversary Conference. There were very few empty chairs as Paul Waldner opened the proceedings with Session 5, on a theme of future PCB design, material, and processes for the PCB supply chain.

3 Graphic Plc Continues to Prosper at 50 ▶

Graphic Plc was formed on 21st June 1968 by Rex Rozario OBE. Rex worked with Dr Paul Eisler, the inventor of the Printed Circuit Board, at Technograph-Telegraph in the 1950s. In 1972 Rex moved the factory to Crediton and operated from a number of buildings on the Lords Meadow Industrial Estate.

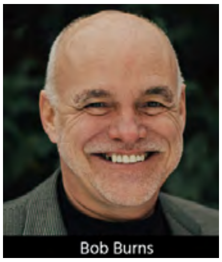
4 Punching Out! Dealing with Family Businesses ▶

Some families may have spent this past Father's Day discussing family business issues, including when, how or whether to pass the baton. There are several issues to consider when dealing with a family business.

5 The Right Approach: The Value of Coopetition ▶

As our industry continues to evolve and shape-shift, PCB manufacturing continues to shrink through consolidations and attrition. In a global economy, partnering with world-class suppliers is mandatory, and excluding a sub-set of this dwindling supply base because they also happen to be in a crossover business will severely hinder this effort.

6 Flex Time: Why is Rigid-Flex So Expensive? ▶



Bob Burns

One question that I hear fairly often, particularly after an initial quotation, is "Why is rigid-flex so expensive?" In this article I'll share with designers the cost drivers in rigid-flex relative to standard rigid boards and flex circuits with stiffeners.

7 RMAs: Negative Experience or Valuable Opportunity? ▶

Non-conforming material that is sent back by the customer can easily be interpreted as a negative experience. However, if it is perceived as an opportunity to learn and support the customer it becomes a much more pleasant and satisfying endeavor.

8 It's Only Common Sense: Love What You Sell ▶

Raise the perceived value so high that our customers will feel guilty even haggling about the price. To do this, you must love your products—love them as much as my dad, the Coke man, loved his.

9 PCB Material Toolbox for Today's 3G and 4G Networks and Future High-Speed Needs in 5G ▶

Stig Källman

The material toolbox idea first came up when I saw the IPC appendix list for standard one-ply stack-ups. The idea is to make a very simple bill of materials, specifications and notes, and possibly use the same prepreg/resin in the laminate and in the core.

10 American Standard Circuits Names Mohammed Khan Director of Operations ▶

American Standard Circuits has recently appointed Mohammed Khan to the position of director of operations. In this new position Mr. Khan will be overseeing all production, engineering and quality operations for the West Chicago based PCB fabricator.

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Career Opportunities

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Candidate Profile:
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- Experience in change management
- PCB background appreciated, but not mandatory
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- Savvy in standard office software (Word, Excel and Power Point)

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About Gardien Group - Gardien is the world's largest international provider of independent testing and QA solutions to the PCB industry with a global footprint across 24 service centres in five countries and we cater to a whole range of customers, from small family owned PCB shops to large international fabricators. Gardien's quality solutions and process standards are trusted by leading high-tech manufacturers and important industries including aerospace, defense, and medical technology.

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- Assist in resolving customer complaints and queries
- Meet deadlines and financial goal minimums
- Make recommendations to the customer
- Maintain documentation of customer communication, contact and account updates

Job requirements:

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For more information, click below.

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The successful candidate is expected to have solid experience within the PCB assembly industry and the ability to represent the Valor solutions with authority and credibility. A solid background in PCB Process Engineering or Quality management to leverage in day-to-day activities is preferred. The candidate should be a good "storyteller" who can develop relatable content in an interesting and compelling manner, and who is comfortable in presenting in public as well as engaging in on-line forums; should have solid experience with professional social platforms such as LinkedIn.

Success will be measured quantitatively in terms of number of interactions, increase in digital engagements, measurement of sentiment, article placements, presentations delivered. Qualitatively, success will be measured by feedback from colleagues and relevant industry players.

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- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Produce service reports
- Cooperate with technical team and share information across the organization
- Assist with the crating and uncrating of equipment

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- Three to five years of experience with SMT equipment, or equivalent technical degree
- Strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Organizational skills, detail orientated and capable of multitasking
- Good written and oral interpersonal skills with an ability to work under minimum supervision
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Job Duties:

The Mentor printed circuit board (PCB) technical writer/content manager will:

- Write and produce high-quality content for various properties (blogs, product collateral, technical white papers, case studies, industry publications, etc.)
- Gather research and data, interview subject matter experts, and transform complex information into clear, concise marketing communications
- Manage projects across multiple PCB product teams (high-speed design/analysis, advanced packaging, board design) within a deadline-driven environment

Job Qualifications:

The ideal candidate should possess:

- Strong writing and editing skills with experience in PCB design technologies
- Desktop publishing skills (InDesign) using project templates and knowledge of online publications and social media
- A technical background (B.S. in electrical engineering or computer science preferred; this role works closely with the PCB division's technical marketing engineers and managers
- Solid project planning and management skills; appreciation for adhering to deadlines; creativity for turning technical information into compelling content; teamwork and strong interpersonal communications skills; ability to be a self-starter

apply now

Events Calendar

PCB West 2018
September 11–13, 2018
Santa Clara, California, USA

IPC E-Textiles 2018 Workshop
September 13, 2018
Des Plaines, Illinois, USA

electronica India & productronica India
September 26–28, 2018
Bengaluru, India

electronicAsia 2018
October 13–16, 2018
Hong Kong

SMTA International
October 16–17, 2018
Rosemont, Illinois, USA

TPCA Show 2018
October 24–26, 2018
Taipei, Taiwan

electronica 2018
November 13–16, 2018
Munich, Germany

IDTtechEx Show
November 14–15, 2018
Santa Clara, California, USA

HKPCA/IPC International Printed Circuit & South China Fair
December 5–7, 2018
Shenzhen, China

48th NEPCON JAPAN
January 16–18, 2019
Tokyo Big Sight, Japan

IPC APEX EXPO Conference and Exhibition
January 26–31, 2019
San Diego, California, USA

DesignCon 2019
January 29–31, 2019
Santa Clara, California, USA

Additional Event Calendars

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Coming Soon to PCB007 Magazine:

SEPTEMBER 2018: mSAP and SLP
The Effects on the PCB industry

OCTOBER 2018: Lights Out
The Fully Automated Factory