I-Connect007

JUNE 2019

PCB007 MAGAZINE

Everything Starts With Design

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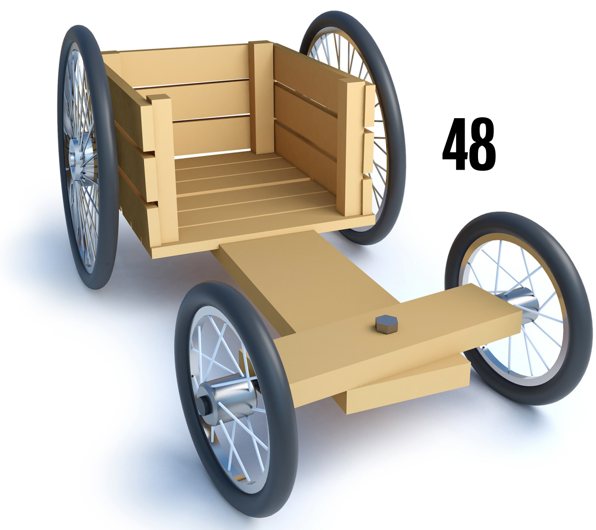
As OEMs drive electronics manufacturers to improve processes to simultaneously build a product at two orders of magnitude more reliability, where does a fabricator even begin to concentrate its efforts to get the best improvement in output? Some will tell you that getting the best possible quality on the input is where you should start.



IT-170GRA1

IT-170GRA1 Value Proposition

- Halogen Free
- Best in class performance in its space
- Best in class CAF performance
- Very attractive price to performance ratio
- Pass MRT-6 requirements
  - -CAF > 1000 hours
  - -0.65mm pitch equivalent, no thermal issue
- Available with RTF and 2μ copper which provides additional performance on a very solid platform
- Df = 0.0075 @10GHz

Intel Purley Mid-Loss Solution – IT-170GRA1

Futures

Halogen free mid loss, Df < 0.01
Tg 180ºC by DSC, low CTE

Applications

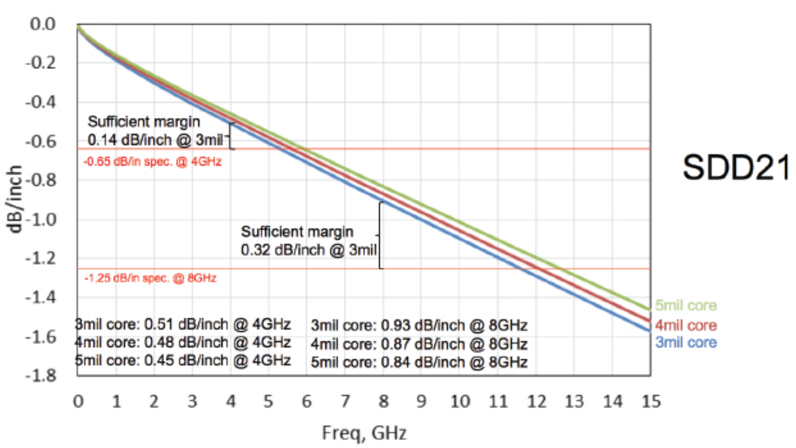
Server/Storage/Switch (10G, 40G)
Backplane, Telecom
Base station

Feature *Purley Platform Mid-Loss Solution – Hi Tg*

General Properties

Items	Methods	IT-170GRA1
Tg (℃)	DSC	180
T-288 (w/ 1 Oz Cu, min)	TMA	60+
Td-5%(℃)	TGA 5% loss	380
CTE (%), 50-260℃	TMA	2.4
Peel strength (lb/inch)	1 oz	7.0
Water absorption	D-24/23	0.1
Dk: 2-10 GHz	Bereskin	3.96 – 3.99
Df: 2-10 GHz	Bereskin	0.0073 - 0.0075

IT-170GRA1 Insertion Loss



ITEQ

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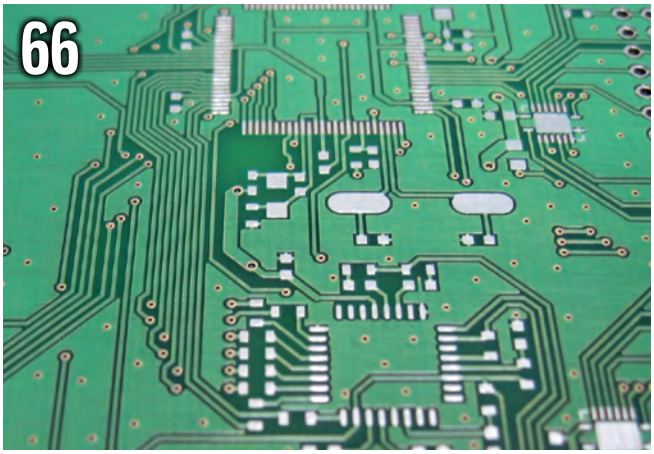


ARTICLES:

SHORTS:

COLUMNS:

DEPARTMENTS:

HIGHLIGHTS:

Quality by Design

Nolan's Notes
by Nolan Johnson, I-CONNECT007

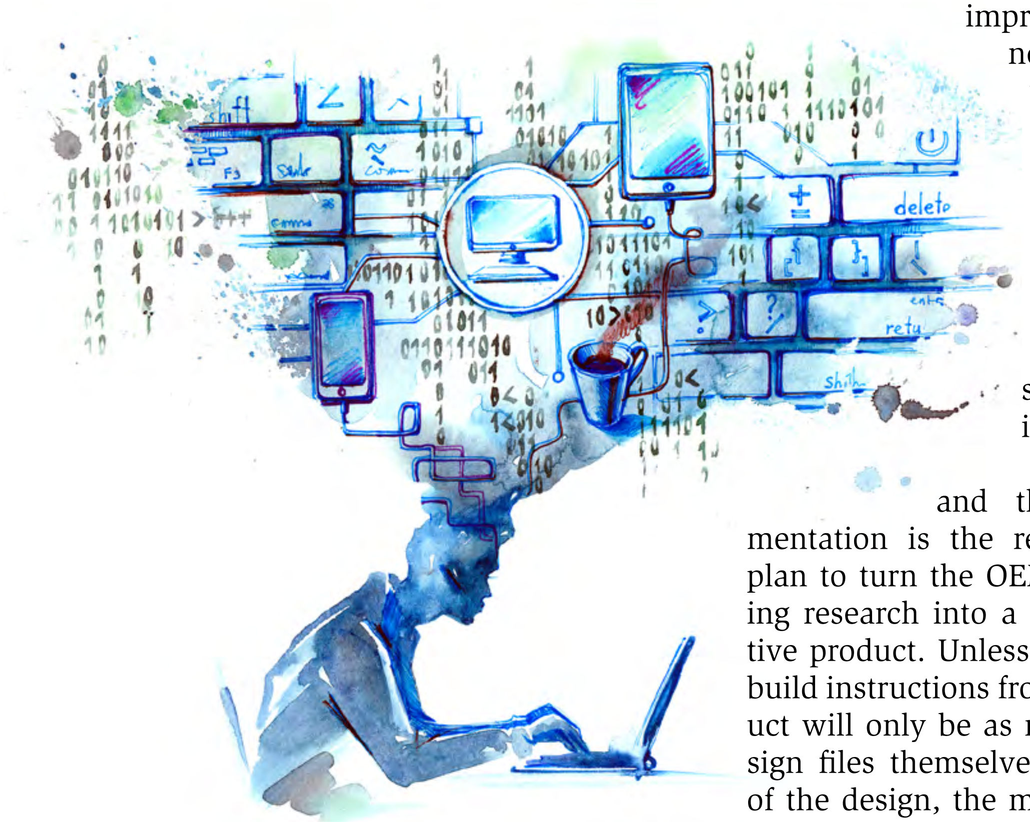
"Quality is never an accident. It is always the result of intelligent effort." –John Ruskin

Though he wasn't writing about printed circuit board design at the time, Ruskin's wisdom suits us very well. Quality is, well, qualitative. Output quality can be affected by processes, people, product specifications, and raw materials. In our industry, ongoing hot topics include the skills gap, filling jobs, emerging technology, Industry 4.0, and so forth. Ultimately, these topics can make or break your company's quality.

According to a press release published by SCORE on May 23, 2019, "98.6% of American manufacturing companies are small businesses, and 75.3% of those businesses have fewer than 20 employees." SCORE is an organization that mentors to America's small businesses. The report continues, "Last year, manufacturing businesses generated 11.6% of the U.S. economic output and employed 8.5% of the U.S. workforce, but 89% of manufacturers report that they cannot fill all job openings."

This report looks at all manufacturing, but it's clear that the electronics industry trends are consistent with manufacturing in general. There are also a large number of small businesses in our sector.

Our topic this month, however, is "Everything Starts With Design," so what does that have to do with quality, staffing shortages, or small business? Pretty much everything.



As OEMs drive electronics manufacturers to improve processes to simultaneously build a product at two orders of magnitude more reliability, where does a fabricator even begin to concentrate its efforts to get the best improvement in output? Some will tell you that getting the best possible quality on the input is where you should start.

The design team's files and the accompanying documentation is the real-world implementation plan to turn the OEM's concepts and marketing research into a viable, physical, competitive product. Unless manufacturing defies the build instructions from the designers, the product will only be as manufacturable as the design files themselves. The higher the quality of the design, the more robust the contingencies specified in the bill of materials, and the more materials tolerances have been thought through and expressed in the build notes, the better the end result will be coming through fabrication.

And given all of the simultaneous challenges facing PCB fabricators with respect to staffing, new equipment, environmental impact, etc., making the communication process with your OEM customers efficient seems like the logical first step in stepping up to new challenges.

This month's conversation kicks off with Happy Holden's feature on "Digital Twin Drives Design in the Smart Factory." Then, we bring you an excerpt from Mark Thompson's book *The PCB Designer's Guide to… The Perfect Data Package*. If you're involved on either side of the job file transfer from design teams to manufacturing, Mark's book will be valuable to you.

Next, IPC President and CEO Dr. John Mitchell introduces the Emerging Engineer Program.

San Diego Circuits' Mike Creeden contributes to the discussion in an interview. Mike talks with me about material selection and the effect on design performance later.

Tara Dunn heads even further upstream in her column "Spark an Idea" to explore some great examples of design brainstorming.

Next, Barry Matties files an interview with Vladi Kaplan, marketing and technical director at CIMS. Barry and Vladi discusses the Virtual Verification Station and trends that Vladi sees in laser via inspection.

The PCB Norsemen weigh in on the importance of design in their column, "From Wooden Huts to Homemade Go-karts: It All Starts With Design."

We wrap up with some deeper technical topics. Contributor Brandon Sherrieb submitted a piece on 4-wire Kelvin testing titled "Kelvin Characterization to Accurately Predict Copper Thickness." Nikolaus Shubkegel also joins the lineup with his article titled "Conventional Exposing: Direct Imaging Solder Mask."

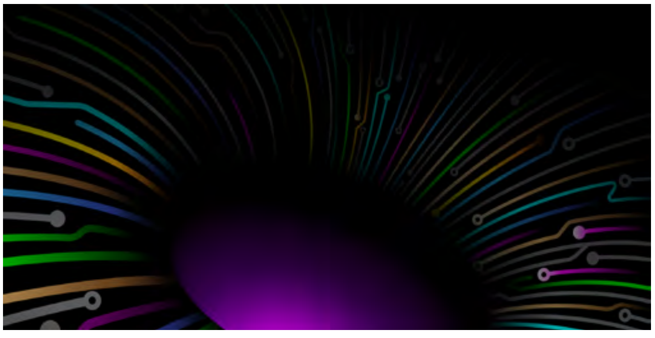
Completing the hat trick, Joan Tourné returns with the second in his series on VeCS, concentrating on micromachining.

As always, we welcome your feedback on our coverage. Questions, comments, and story ideas and submissions can be sent to *PCB007 Magazine* at editorial@iconnect007.com. **PCB007**

Nolan Johnson is managing editor of *PCB007 Magazine*. Nolan brings 30 years of career experience focused almost entirely on electronics design and manufacturing. To contact Johnson, click here.

XNC Format: Gerber Takes Data Into the Future

Gerber is the world's favorite data exchange format for PCB image data: it's easy to use, crystal clear, and gives designers and engineers a language with which to communicate with each other. And this grand old man of the PCB industry has remained at the forefront, powered by ongoing developments that add capability and functionality without ever compromising its characteristic simplicity and ease of use.



But the majority Gerber file set creators are still transferring routing and drilling coordinates using NC formats, which were never designed for data transfer, and more often than not create confusion and waste time. So, why are CAD developers and their users still stuck on NC formats? It's most likely a question of inertia or tradition.

Denis Morin, Karel Tavernier, Jean-Pierre Charras, and Marius Matioc explain how the new XNC format serves as an improvement over, and replacement for, NC formats.

To read this entire article, which appeared in the April 2019 issue of *Design007 Magazine*, click here.

Digital Twin Drives Design in the Smart Factory

Feature by Happy Holden
I-CONNECT007

New product realization and design for manufacturing and assembly (DFMA) has now started to become more visible as a program that can improve a company's time to market and lower product costs. This is one of the main focuses of Industry 4.0 for the smart factory. Many programs are underway by numerous companies, and what is now needed is a framework to coordinate the application of these programs.

This article will cover the interactions of DFMA and the need for the development of a new framework to coordinate the trade-offs provided by digital twin simulations.

Concurrent engineering has been the basis for electronics design. Its one-way interactions with manufacturing constitute the "old way" of thinking. This article will also propose a new framework—digital twin—patterned after the manufacturing software framework of concurrent manufacturing. This framework will provide the interoperability for manufacturing capabilities and characteristics to be planned into electronic assemblies before the traditional CAE/CAD processes. As part of this framework, the basis for trade-offs will be the basic DFMA metrics that have been developed by different companies. Digital twin is complementary to the growing application of Industry 4.0, smart factory software, and product data management (PDM) software used in electronics manufacturing (Figure 1).

We have all seen how electronics technologies are increasing in capability at an ever-increasing rate. Unfortunately, those of us in manufacturing have also seen a corresponding increase in the complexity of packaging. Modern EDA tools and concurrent engineering are the primary driver of this phenomena. What we have not learned to do in this era is to de-

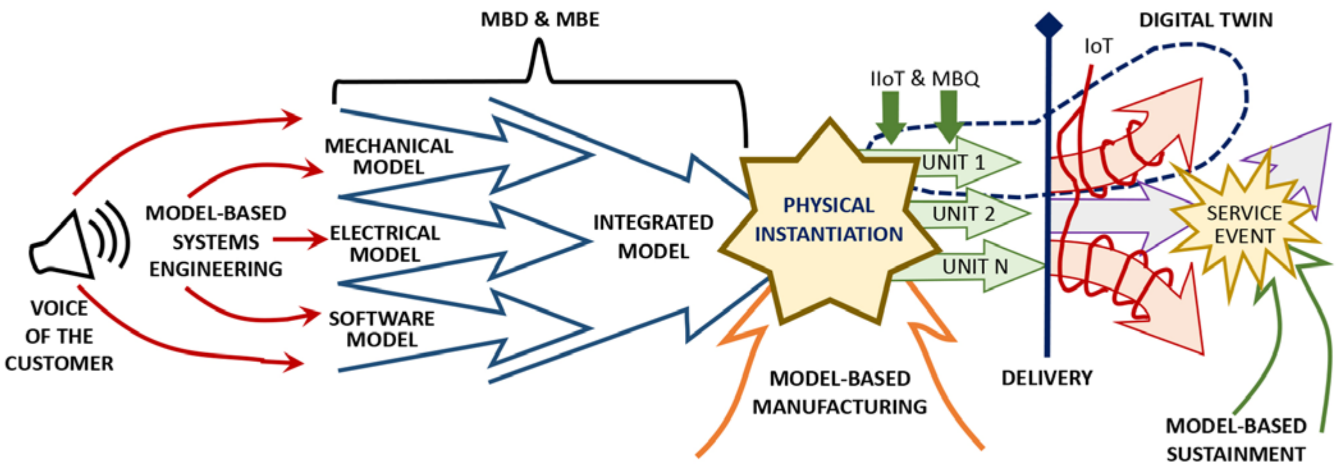


Figure 1: Digital twin evolved from conventional simulation and electrical models to combine with the manufacturing twin models and the performance twin as well as other features of the smart factory. (Source: *Machine Design*, March 2019)

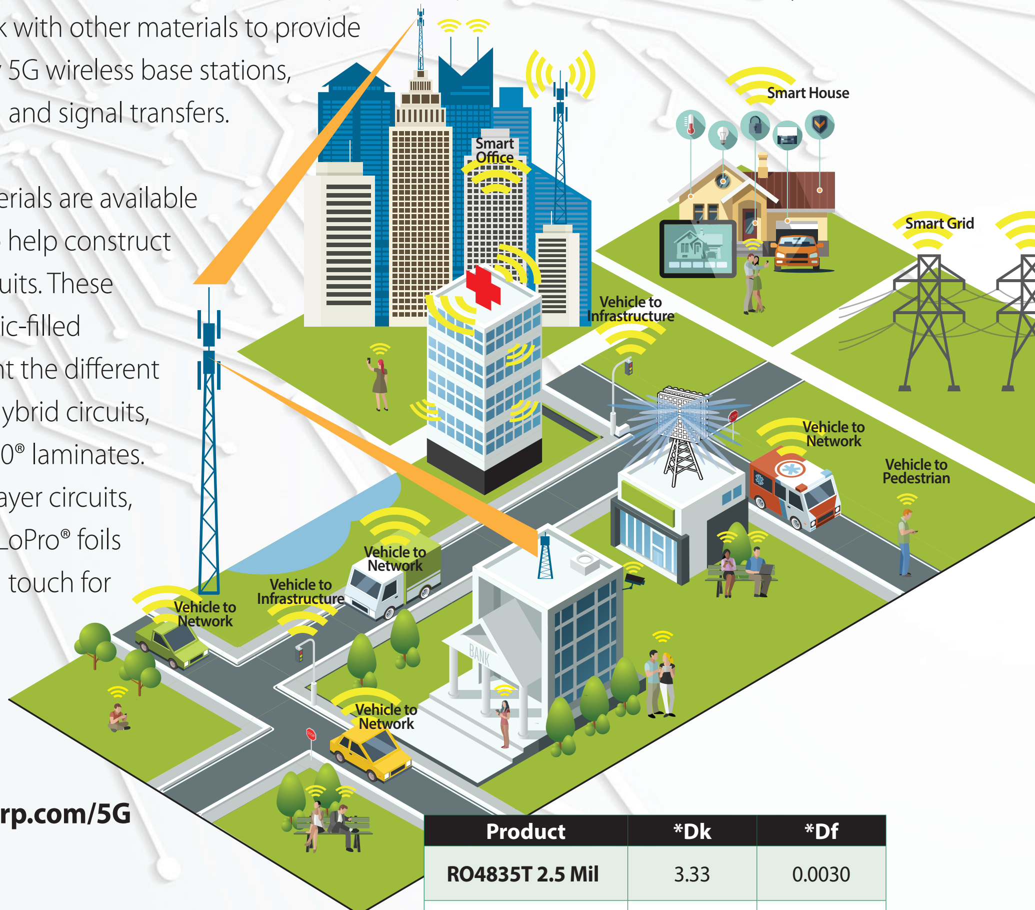
5G: Higher Frequencies!

Do you have the **right** circuit materials?

Frequencies at 28 GHz and higher will soon be used in Fifth Generation (5G) wireless communications networks. 5G infrastructure will depend on low-loss circuit materials engineered for high frequencies, materials such as RO4835T™ laminates and RO4450T™ bonding materials from Rogers Corporation!

Rogers RO4835T spread-glass-reinforced, ceramic-filled laminates are low-loss materials in 2.5, 3.0, and 4.0 mil thicknesses. They are well suited for millimeter-wave frequencies as part of the inner cores of 5G hybrid multilayer PCBs. They can work with other materials to provide the many functions needed by 5G wireless base stations, including power, signal control and signal transfers.

Rogers RO4450T bonding materials are available in 3, 4, and 5 mil thicknesses to help construct those 5G hybrid multilayer circuits. These spread-glass-reinforced, ceramic-filled bonding materials complement the different materials that will form these hybrid circuits, including RO4835T and RO4000® laminates. And for many 5G hybrid multilayer circuits, Rogers CU4000™ and CU4000 LoPro® foils will provide a suitable finishing touch for many hybrid multilayer circuit foil lamination designs.



5G is coming! Do you have the right circuit materials?
Learn more at **www.rogerscorp.com/5G**

Product	*Dk	*Df
RO4835T 2.5 Mil	3.33	0.0030
RO4835T 3.0 Mil	3.33	0.0034
RO4835T 4.0 Mil	3.32	0.0036
RO4450T 3.0 Mil	3.23	0.0039
RO4450T 4.0 Mil	3.35	0.0040
RO4450T 5.0 Mil	3.28	0.0038

** IPC TM-650 2.5.5.5 Clamped Stripline at 10 GHz - 23°C*

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velop an effective technique to feed back manufacturing experiences and wisdom. The data flow is all one direction from DFM.

Opportunity Provided by the IC Design Model: Design Planning for PCBs

There are five compelling reasons that digital twin is essential to the design of electronic products. First, products have become increasingly complex. Not only must products meet increased expectations from customers but they must be environmentally friendly, energy-efficient, and conservative of resources. All of this is done in ever-shrinking product life cycles. Second, minimizing cost is imperative. DFMA has been shown in benchmarking and case studies to reduce assembly costs by 35% [1] and PWB costs by 25% [2].

Third, 75% of the manufacturing costs of a product is determined by all the design drawings and specifications. Fourth, in the electronic product design process, 60% of the manufacturing costs are determined in the first stages of design when only 35% of the design cost has been expended. As shown in Figure 2, the product definition process includes specifications and partitioning. This is a technology trade-off analysis of the balance of loss and gain in various domains' performance versus costs. Fifth, a common language needs to be established that links manufacturing to design and R&D. This common language should define producibility as an intrinsic characteristic of design. It is not an inspection milestone conducted by manufacturing. Producibility scores form a non-opinionated basis that allows for a team approach that results in a quality, cost-competitive product.

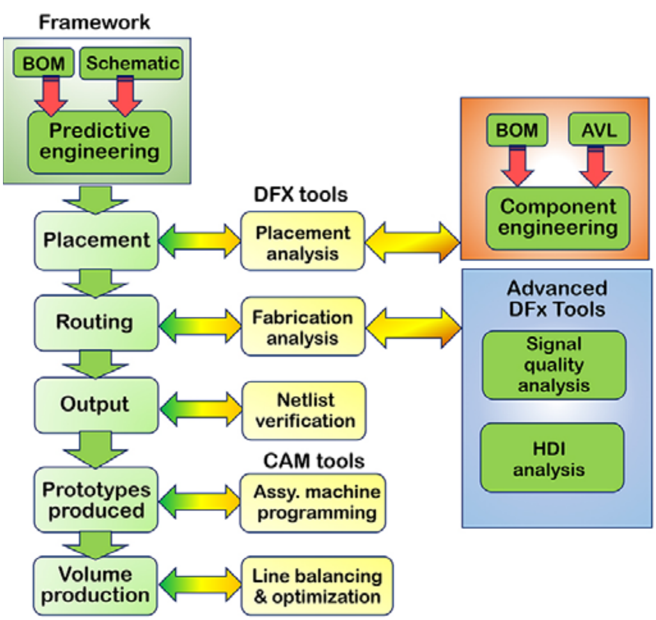

Figure 2: Digital twin contains more than just density modeling; it provides caution on failure-prone components and suitability for testing as well as optimizing electrical performance and minimizing signal integrity problems.

The Nature of the Problem

The current practice is that design data travels in only one direction: toward manufacturing. As shown in Figure 3, there is no provision for the capabilities, experiences, and wisdom gained in manufacturing to flow back to the design environment. Hence, many companies use concurrent engineering to bring experienced manufacturing personnel into the design process to try and impart some of that wisdom. Unfortunately, these experienced manufacturing people are becoming rarer, and it takes far too long to gain that experience. The difficulties don't just end there; most of the time, the manufacturer is far away. Under the best of circumstances, the wisdom and experience must be imparted as opinion, and opinions are difficult to defend.

This might be a working solution for small, vertically integrated companies with vast experience in manufacturing. But in the last few years, printed circuit packaging has taken a jump in sophistication. Not only is surface mounting now very fine pitch, but ball grid arrays (BGAs) and flip-chip and chip-scale packages have entered the picture. Take all of this and the many high-density interconnect structures (microvia or buildup PCBs in Figure 4) [3] available on the market, and design has be-

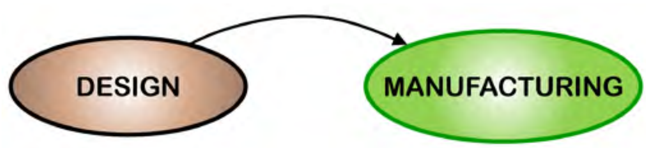

Figure 3: Current product data movement.

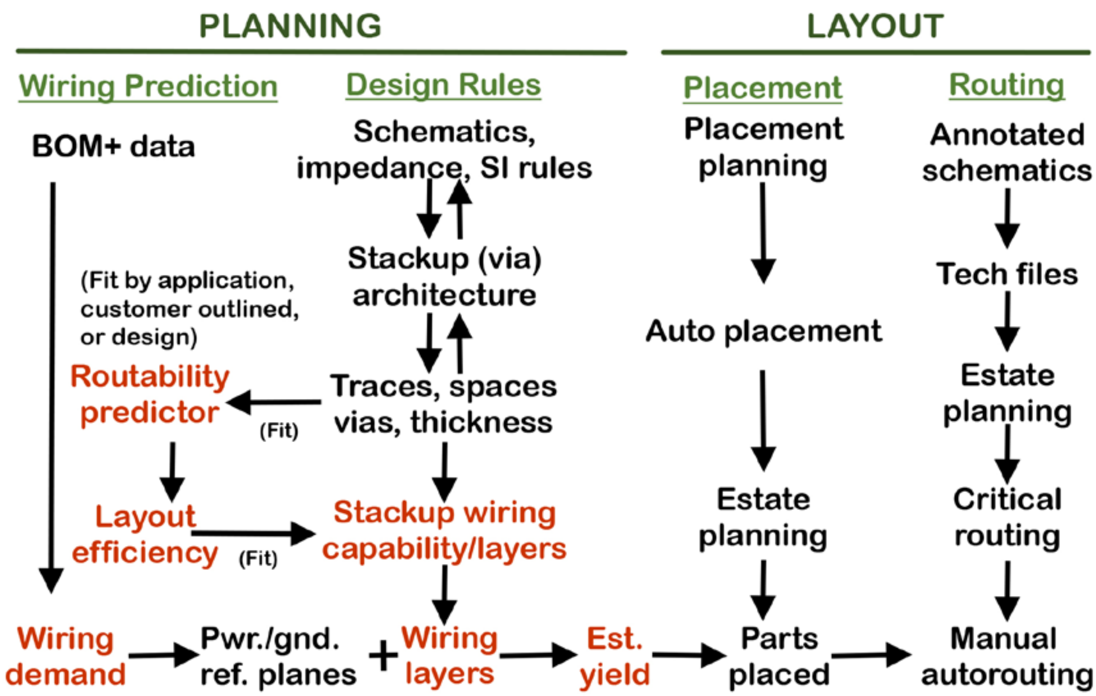

Figure 4: Process flow for the design planning of a printed circuit.

come extremely complex. Many companies are working on this problem through DFMA. The focus is on six key design topics, including:

1. Optimization of PC design grids and layout [4]
2. Minimization of PC substrate costs [2]
3. Minimization of assembly costs [1]
4. Use of preferred parts [5]
5. Analysis of test coverage [6]
6. Partitioning of ASIC pinouts

What they all have in common is metrics, but the design community is suspicious when the entire system is not being considered. They are afraid of suboptimization where the cost of a particular domain is lowered but the total system cost increases. The design community needs a software environment to integrate all of these separate programs.

Common Metrics of DFMA

The metrics that have been developed for DFMA occur in three domains:

1. PWB layout
2. PWB fabrication
3. SMT assembly and test

1. PWB Layout

The standard (and not so standard) metrics used before PWB layout include a packaging technology map. A simple technique exists to predict a printed wiring board's wiring factor (W_F) and its assembly complexity. The technique is the packaging technology map [7]. By plotting parts per square inch against average leads per part on a log graph, the wiring factor (inches per square inch) and assembly complexity (leads per square inch) can be calculated.

2. PWB Fabrication

The metrics for PWB fabrication deal with trade-offs between the performance objectives and the PWB prices. This is where producibility came in since prices need manufacturing yields before it can be estimated accurately. Two key metrics were developed to bring about these price/performance trade-offs:

1. Complexity index (CI) to characterize the complexity of physical characteristics (size, layers, holes, traces, etc.) of this particular PWB so that first pass yield can be calculated

2. Relative cost index (RCI) is an artificial currency that indicates the magnitude of price changes between two or more design alternatives

3. SMT Assembly

The major metric of SMT assembly is the assembly report card—a predictive, comprehensive set of metrics. The 10 factors are based on a total point scheme derived from assembly costs. The points affect quoted prices to the following extent:

- 0–45 points: +20%
- 46–60 points: +10%
- 61–75 points: -10%
- 76–100 points: -20%

A second typical metric is assembly complexity [8 & 9]. This is defined as leads per square inch (LPI). The listed references provide the data for a regression model of the average cost per lead versus assembly complexity.

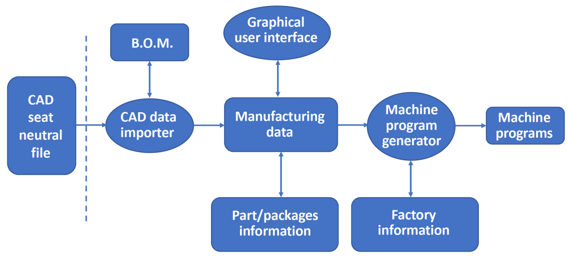

Figure 5: Concurrent manufacturing framework.

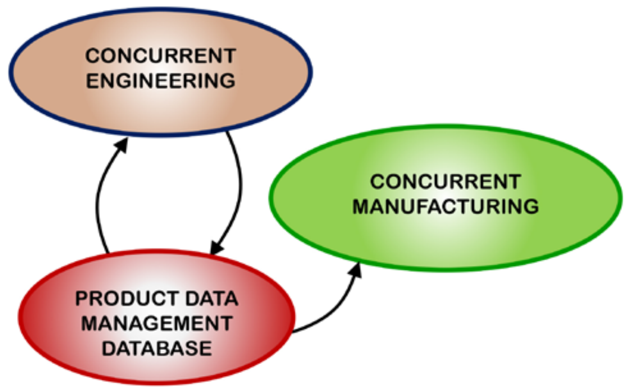

Figure 6: Emerging data transfer environment.

Proposed Approach

Emerging assembly and fabrication smart digital systems—such as CFX, CAD Master, CAMStar, CADMaster, and individual software solutions—offer a new opportunity to implement DFMA. As mentioned earlier, I call these modern frameworks concurrent manufacturing to differentiate them from concurrent engineering. The framework of concurrent manufacturing is shown in Figure 5.

The important role concurrent manufacturing plays in DFMA is illustrated by the module product information exchange (PIX). Its role is to:

- Communicate information between design engineering to manufacturing, manufacturing to design engineering and other manufacturing, and subcontractors
- Automate CAD data exchange and revision archiving
- Provide product data tracking and packaging completeness checking, and support standard industry networking
- Design for Assembly to analyzes party placement, support multiple machine configuration, analyze machine capacity, and provide production engineering documentation

The emerging data transfer environment is from the enterprise's central database called product data management [10]. Figure 6 illustrates this new data movement condition. PDM software integrates all data required to design, manufacture, and support a product, such as:

- Simulation and models
- CAD and CAE data files
- Materials, processes, and characteristics
- ECOs, revisions, parts, etc.

Digital Twin

Digital twin is the activity of doing trade-offs and simulations. It focuses on:

- Product definition and system partitioning (technology trade-off)

- Layout and CAD system setup
- PWB fabrication design rules, yield optimization, and cost trade-offs
- SMT assembly process, packaging component, and test trade-offs
- Specifications and documents
- Standards and regulations

Over the years, I have taken various predictive models and coded them into Excel spreadsheets. This allowed me to see the effects of various parameters on events. Eventually, by using macros, I have linked these 34 spreadsheets into one predictive system that allows me to prototype a proposed schematic and look at its performance and costs without ever actually designing it or building it. As shown in Figure 7, this allows the user to improve on any product development or product change process.

One key element is missing from this list: the global assignment of custom ASIC pin locations. This would help to reduce PWB and assembly complexity and costs while assuring better system performance and the best time to profits. The DT framework imports critical metrics and data from manufacturing through the PDM database (Figure 8) [10]. Since concurrent engineering has such a short product focus, the wisdom and experience acquired in concurrent manufacturing can be archived in PDM.

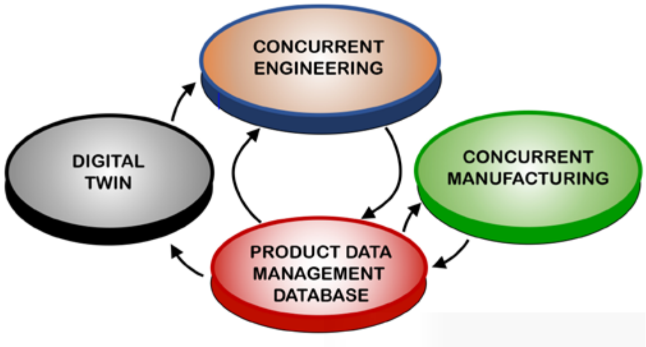

Figure 8: Proposed digital twin framework.

The DT software architecture of trade-off models and supporting software provides the user with global information (Figure 9). As

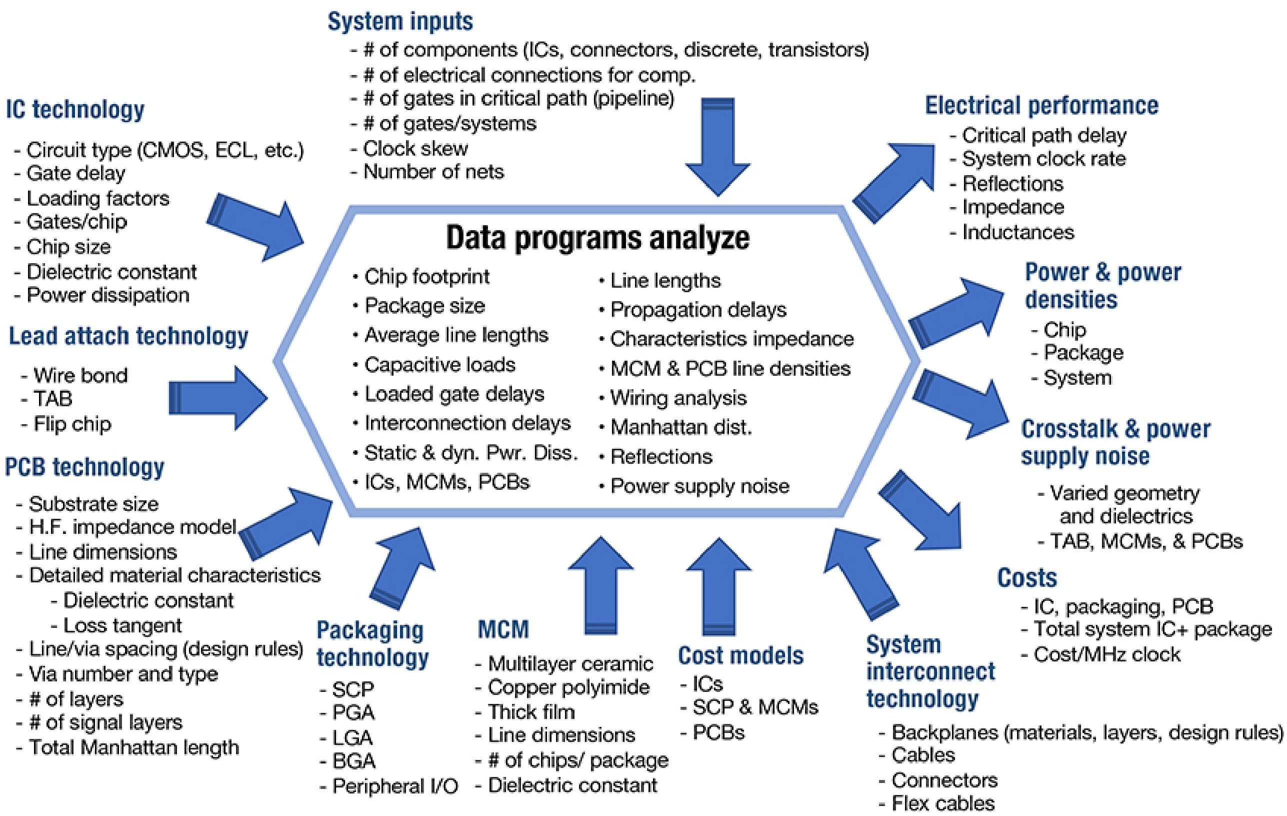

Figure 7: For digital twin of a PCB, there should be simulations and trade-offs that cover all the domains that a user finds critical, including costs, manufacturability, density, signal integrity, and reliability.

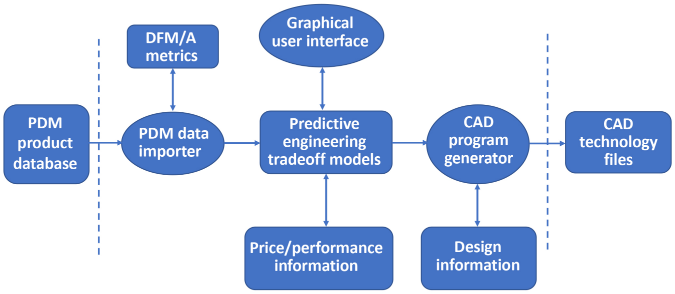

Figure 9: Proposed digital twin architecture.

features are selected, they can be placed back in the PDM database. Selection of layout factors, sizes, and design rules can be used to create technology files that drive modern CAD programs.

Conclusion

If companies want to reduce product generation time to market and development and production costs, then DFMA needs to be integrated into a product generation framework. Concurrent engineering and manufacturing, product data management, and digital twin all are essential elements. The tools, software, and elements of such a vision are shown in Figure 10. All that remains is to find a software environment to add digital twin. **PCB007**

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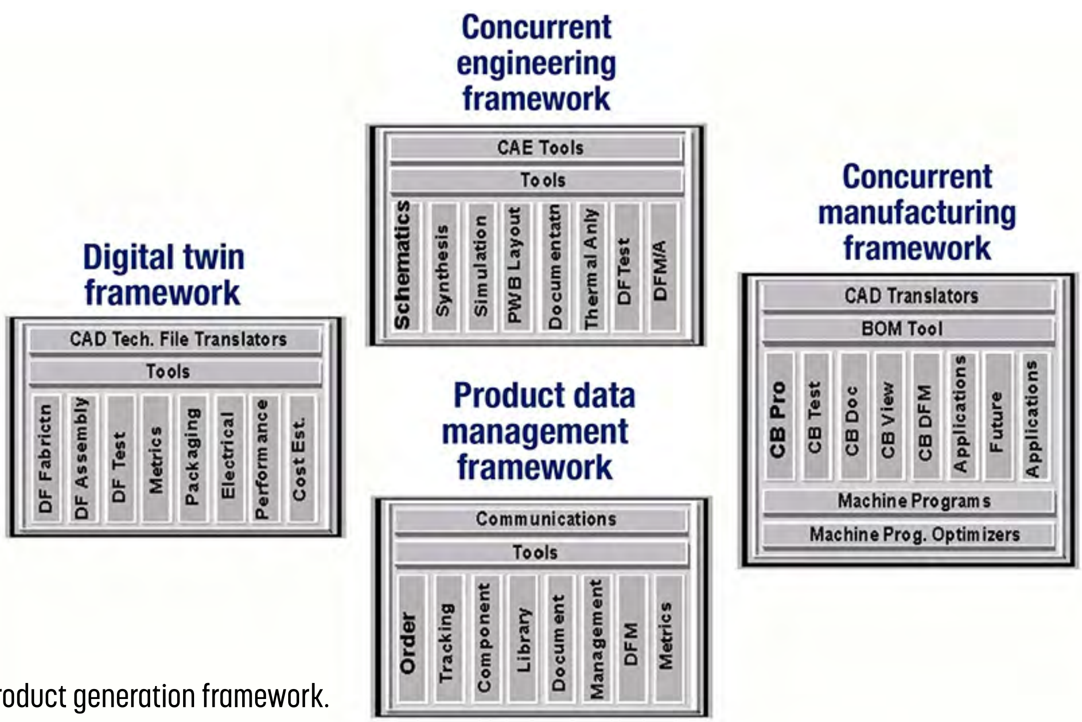


Figure 10: Product generation framework.

Identifying Product Board Class and Pre-quote Software

Editor's note: The following is an excerpt from Chapter 1 of ***The Printed Circuit Designer's Guide to... Producing the Perfect Data Package*** written by Mark Thompson of Prototron Circuits.

Deciding on the class of the final product will determine what files are needed for fabrication and assembly. It is critical to note that for a product to be built to any class level, it must be designed to that class level from its inception.

Standards and Specifications

Let's review the various PCB classes as defined by IPC—Association Connecting Electronics Industries. IPC is the trade association for the electronics industry that provides standards, training and certification, market research, education, and public policy advocacy to support all facets of the industry, including design, PCB manufacturing, and electronics assembly.

First, understand that IPC has different specifications depending on the PCB type. This book will address rigid and rigid-flex PCBs. The industry standards for these PCB types are:

- IPC-6012: Qualification and Performance Specification for Rigid Printed Boards
- IPC-6013: Qualification and Performance Specification for Flexible Printed Boards
- IPC-6018: Qualification & Performance Specification for High Frequency (Microwave) Printed Boards
- IPC-6012DS: Space and Military Avionics Applications Addendum to IPC-6012D: Qualification and Performance Specification for Rigid Printed Boards

There are three different board classes as defined by IPC-6012 and IPC-6013. The appropriate class will be defined by the criticality of the product the PCB will be integrated with.

Classes

Class 1 is for "general electronic products" and is the lowest reliability class. Therefore, it requires the least amount of additional information in a fabrication package to meet product reliability. For instance, a Class 1 or Class 2 PCB does not require a netlist compare, whereas Class 3 and Class 3A do require it. Thus, for

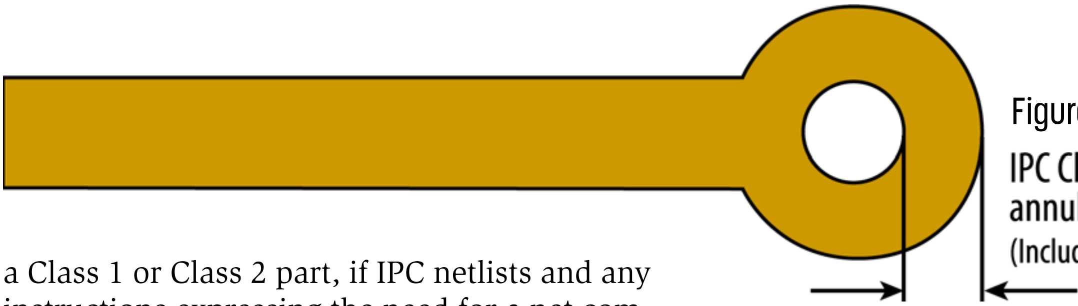


Figure 1.1
IPC Class 3 external annular ring min. 2 mils. (Includes hole wall copper.)

a Class 1 or Class 2 part, if IPC netlists and any instructions expressing the need for a net compare are not provided, a separate netlist file is not required in the output package.

Class 2 is for "dedicated service products" and requires a little more information to be provided, as continued performance and extended life cycle are required. Uninterrupted service is not mandatory for Class 2 PCBs. It is important to note that while a Class 2 PCB does not require an IPC netlist be provided to do a design versus exported image data comparison, it is highly recommended as part of the output package.

Class 3 is specified for the highest reliability and continued high performance in segments where equipment failure simply cannot be tolerated, such as the medical or aerospace industries. For IPC 6012 Class 3 an IPC netlist comparison is required. Netlists typically follow IPC-D-356, IPC-D-356A, or a Mentor neutral file. Other older forms of IPC netlists can be used if a fabricator has the ability to use raw computer-aided design (CAD) data, but by far the most common formats for fabrication are the three previously mentioned.

As a fabricator, we constantly see PCBs called out as IPC-6012 Class 3 that have not been designed to meet Class 3 requirements, such as minimum annular ring or clearance (Figure 1.1). If the PCB was not designed to meet Class 3 requirements, the fabricator does not have a chance to provide the customer with a Class 3 PCB. Designers should use the IPC-2220 series of documents concerning board design and fabrication to ensure a design-to-fabrication match.

Part sizes are shrinking while part densities are growing, which reduces space and makes it increasingly difficult to have enough supporting annular ring or clearance. One way to minimize delays in the fabrication quote or manufacturing process is to qualify this by saying the product is to be built to IPC-6012 Class 3 with an allowance for annular ring and clearance to Class 2. This may preclude a phone call from your fabricator to tell you the quote is on hold because the design does not meet Class 3 minimum annular ring requirements (Figure 1.1).

Pre-quote Software

Many PCB fabricators have some type of pre-quote analysis software that can quickly tell them if the PCB meets certain design rules, such as whether spaces on a given design do not support the copper callout specified on the drawing or stackup detail, or if the annular ring is insufficient for the specified hole sizes. As a cautionary note, these are quoting tools the fabricator uses to catch obvious concerns. They are not intended to take the place of a full-blown computer-aided manufacturing (CAM) design rule check (DRC) tool.

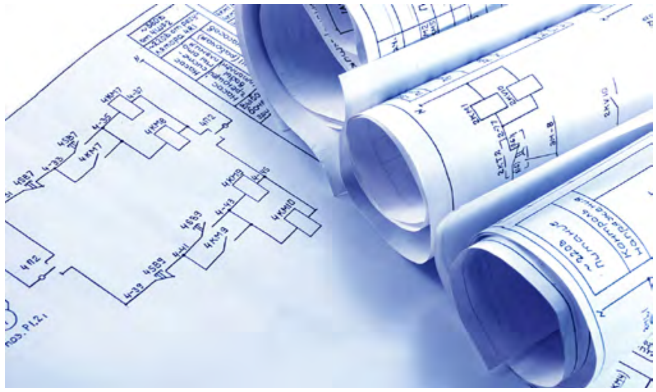
Pre-quote software is typically a quoting tool for managing and assessing the customer's incoming PCB data files. Depending on the

Fun fact: The term "annular ring" comes from the reliable indicator of yearly tree growth.

system in place, this can include automatically retrieving design information and generating precise summary reports that identify potential risks and challenging design features. These tools allow sales and quoting personnel, who typically do not have a technical engineering background, to work more independently from engineering and provide a highly accurate quote.

Many of the fabricators using these software packages offer them as an online check prior to submitting a quote. However, they typically have a support person run the files through the software for the customer. If you are utilizing any of these services, you can do yourself a favor and minimize quote response times by standardizing your file names to avoid sending any conflicting information. These quote software packages do not have the ability to read and interpret drawings. If your file names are not readily recognized to prepare the layer stack, the system may pause to allow the user to enter this missing or misinterpreted information and continue to process the job.

Incoming files are placed into a "hopper" with some type of naming convention that establishes which files go to which quoting person (presuming your fabricator has more than one). The files are then loaded into the system, and the software runs an analysis of your data; in some cases, it will even run your provided IPC design netlist against the provided customer image data. The benefit of using a pre-quote software solution is identifying potential manufacturing problems early during the quote stage without tying up engineering resources.



Fun fact: The process of printing blueprints is now obsolete; however, the term continues to be used informally to refer to various digital images known as "prints" or "drawings."

Visit I-007eBooks.com to download *The Printed Circuit Designer's Guide to… Producing the Perfect Data Package* as well as other free, educational titles. **PCB007**

Albert Gaines: It All Comes Down to Documentation

During SMTA Atlanta, Andy Shaughnessy spoke with Albert Gaines, founder of the design bureau HiGain Design. They discussed Albert's belief that everything starts with design and the fact that too many engineers and designers focus solely on the final board at the expense of the documentation. It may not be PCB designers' favorite part of the process, but documentation, in many ways, is their most important product of all.

To read this entire article, which appeared in the June 2019 issue of *Design007 Magazine*, click here.

Albert Gaines

Emerging Engineer Program: A Unique Opportunity Offered by IPC

One World, One Industry

by Dr. John Mitchell, IPC—ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES

One of the most rewarding parts of my job is being able to offer new engineers a leg up early in their career, and I am especially thrilled when I can do it personally. Often, this can be as simple as connecting them with an industry leader. Wonderfully, this was something I was able to do IPC APEX EXPO this past January.

After speaking at the First-Timers' Welcome Reception, I met an engineer from Blue Origin named Christina Handewith-McCallum who mentioned that it was her first visit to IPC APEX EXPO. She was taking it all in (the exhibition on the show floor, standards meetings, professional development courses, etc.) and was eager to learn about the opportunities available to a newcomer like herself.

That gave me the perfect opportunity to talk to her about IPC's Emerging Engineer Program, which launched in 2016 (Figure 1). The program provides engineers early in their careers the opportunity to learn about the industry from dedicated IPC volunteers participating in standards development. Emerging engineers receive:

- Mentoring and training to assist in their professional development
- Recognition for themselves and their company
- An all-access package registration to IPC APEX EXPO for three years
- Complimentary registration to IPC SummerCom, featuring Panelpalooza

This all sounded great to Christina, and by the time she left the show, she was signed up

Figure 1: Emerging engineers and their mentors.

as a new IPC emerging engineer complete with a mentor, and we helped her find on location. I know she's glad she attended the First Timers' Welcome Reception, and I am too!

How else will you find out the nitty gritty about engineering if you don't talk to those in the field? Career engineers and IPC volunteers provide invaluable knowledge by participating in mentorships for our emerging engineers. And I don't know who is having more fun—the new engineers who have a front-row seat to decades of knowledge or the dedicated mentors who enjoy sharing their skills and expertise with the future of our industry.

Melby Thelakkaden, a process engineer at Raytheon Missile Systems and a year-one emerging engineer, said this about her Emerging Engineer Program experience (Figure 2):

"I became interested in the Emerging Engineer Program because I wanted to participate and be more closely involved in the development of IPC standards. Early in my career, I frequently found myself referencing various IPC documents. My mentor, Kathy Johnston, encouraged me to enroll in the program, and after attending a couple of conference sessions, it became clear that being involved will help raise industry awareness. It's such a great opportunity to represent Raytheon at this international platform."

It feels good to give back. It is clear to me that the electronics industry has a great future and that we are doing our best to put it into good hands. If you are interested in becoming an IPC emerging engineer or a mentor, visit www.ipc.org/emerging-engineer or email careerdevelopment@ipc.org. **PCB007**

Figure 2: Melby Thelakkaden talks with her IPC Emerging Engineer Program mentor, Vijay Kumar, at IPC APEX EXPO 2019.

Dr. John Mitchell is president and CEO of IPC—Association Connecting Electronics Industries. To read past columns or contact Mitchell, click here.

The Bare (Board) Truth

by Mark Thompson, CID+, Prototron Circuits

Mark Thompson writes in his column, "It's a fact: Great board design is the key to a great PCB. I'm even more certain of this after spending two days in a wonderful class presented by Rick Hartley."

In his column, "Fabrication Starts With Solid Design Practices," Thompson shares some of his takeaways from one of Rick Hartley's training courses. Mark is a subject matter expert on this topic himself, having authored *The Printed Circuit Designer's Guide To: Producing the Perfect Data Package.*

To read this entire article, which appeared in the June 2019 issue of *Design007 Magazine*, click here.

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Halogen-free Ultra-low transmission loss Multi-layer circuit board materials

Halogen-free MEGTRON6

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Prepreg R-5370(N)* R-5370(E)
*Low Dk glass cloth type

Features

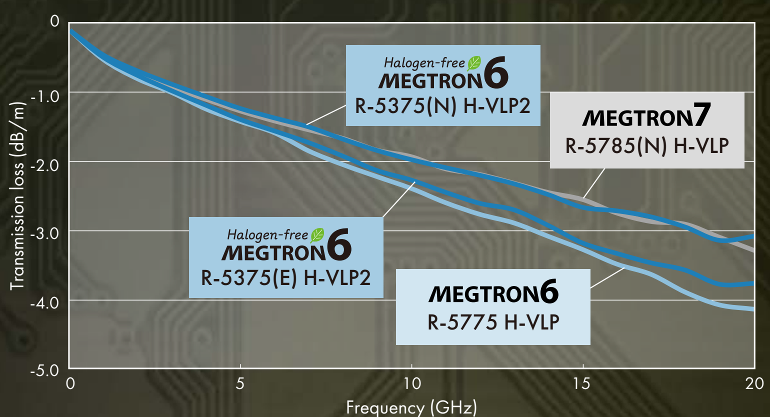
- Excellent HDI and thermal performance **with Halogen free**
- High speed and ultra-low loss material
- Low transmission loss

@10GHz	Dk	Df
R-5375(N)	3.3	0.003
R-5375(E)	3.8	0.005
R-5775	3.8	0.005

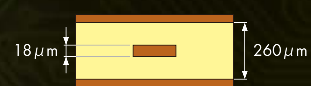
Applications

- ICT infrastructure equipment, High speed networking(High-end server/ router, Optical network, switch), High layer count PCB, etc.

Transmission Loss



- Construction



Line length	200mm , 100mm
Line width	125μm
Impedance	50Ω
Inner Cu treatment	No-surface treatment
Core	0.13mm
Prepreg	#2116 56% x 1ply

Contact us

More information

Technically Appropriate Material Choices Are Key to Success

Feature Interview by Nolan Johnson

Materials are no longer a passive part of the design; they play an active role in the manufacturability, reliability, and speed of a PCB. I-Connect007's Nolan Johnson and Mike Creeden, founder of San Diego PCB Design, discuss several key characteristics that designers should consider in their material selection process.

Nolan Johnson: Mike, could you introduce yourself and tell us about what you're working on?

Mike Creeden: I'm the founder of San Diego PCB Design, and I had the opportunity to sell the company to Milwaukee Electronics/Screaming Circuits, so we've joined the Milwaukee Electronics family of companies. I also serve as an EPTAC instructor for the IPC CID and CID+ programs as an MIT (master instructor).

Johnson: When in the design cycle should PCB development people consider material selection?

Creeden: That's a great question. It should be within the first days of starting your project because that's the best time to establish that things will be designed "correct by construction." I do not want to design a product and then consult my fabricator in the last days of development. If the material is not in stock, we may be delaying the procurement of what is probably a late design, anyway. You'd want to make sure that it's in stock, and you'd also want the coaching from your fabricator and supply chain to make sure that you're making correct selections. When you do this late in the process, selections may happen quickly, and there may not be enough time to ensure that it's an appropriate material selection. There's always a material technology decision, and it should be made early in the design process. The earlier, the better because this allows time to change it if that is required.

Johnson: You're making the point that material is becoming increasingly important. With that in mind, and especially for anybody who's newer to this, why is material important?

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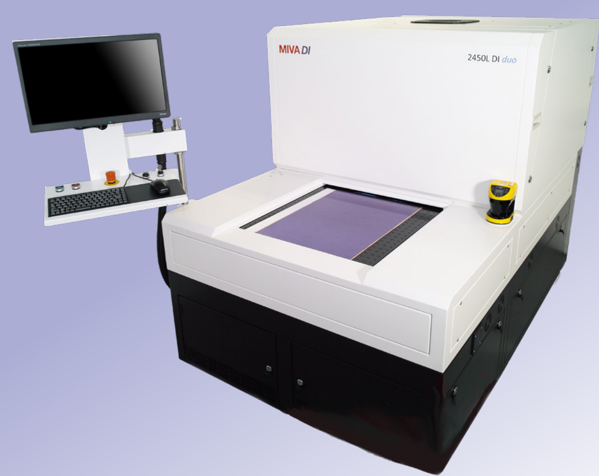

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Creeden: If you've ever seen lightning strike in the air, you're probably seeing it from the cloud to the ground. Or if you've ever seen static electricity, when the lights are low, you can see the spark fly. That's a good visualization to understand every time you're routing a trace. Historically, circuitry traces were DC in nature, and their environment didn't matter as much. Now, you are managing an electromagnetic field. The field is capacitive, and that's best (high capacitive) when a trace is close to its return path. It's also magnetic, which is inductive. That is how a signal propagates (low inductance) down the line. You're also managing an EM energy field; you're not just connecting two points with a trace. The energy field is not in the trace. Rather, the trace and it's return path—typically a GND plane—serve as reference points; thus, the energy exists in the dielectric material between them. Therefore, the material with all of its parameters are an integral part of the performance of the circuit.


Mike Creeden

The material's electrical properties are measured by the dielectric constant (Dk) denoted as ϵr. This measures how well energy will permeate through the material at different frequencies. Also, they are measured by the dissipation factor (Df) also known as loss tangent. This measures how much energy can be dissipated or lost into the material. The energy field travels within the dielectric material. The material can resist the flow of energy, and each material has a known measured rate. As a reference, air has a dielectric constant of $\epsilon r = 1$. Your average FR-4s have a dielectric constant of approximately $\epsilon r = 4$. Faster circuitry requires less resistance and less energy loss, so you see high-speed material go down to the range of $\epsilon r = 3$.

With circuitry achieving increasingly faster speeds, most people equate speed to the circuit's frequency, but it must be understood that the burst of energy delivered in every pulse as measured in the rise time (Tr) as related to voltage/frequency. That is when the signal transitions from zero to its voltage and that burst of energy defines its field. To manage that, you must understand that the material selection is an integral part of the function of the circuitry. These are all factors that engineers and designers must take into consideration from day one.

Material plays an important factor, but the designer must practice good design skills to ensure that signal integrity issues are not created by violating a signal's return path, impedance matching, or crosstalk to another signal. Another electronic consideration is the consistency of the weave pattern because of the Dk difference between weave and resin, so as a solution, they have what's known as spread weave. They spread the weave out to get a consistent Dk, which is essential for the performance of differential pairs of traces.

Mechanical and physical properties affect the structural integrity and manufacturing process. With the glass transition (Tg), the material's resin will transition from a hard to a rubbery state as a factor of temperature. That's imperative when you're considering high layer count boards. The dielectric material typically is comprised of a glass weave, which expands in the X-Y axis, and a resin that expands in the Z axis. The Z-axis expansion is measured as the coefficient of thermal expansion (CTE), which threatens the structural integrity of the via plating, and the vias are the most vulnerable entity on a PCB. The other physical property to be considered is the thermal decomposition temperature (Td) when you start doing HDI boards where you have multiple lamination (thermal) cycles to accomplish the construction. The material can breakdown due to the excessive amount of heat from thermal excursions during all phases of manufacturing, test, and environmental stresses.

Do your research and make sure you understand, based on your application, whether the material's physical and mechanical properties suit your requirement and the manufacturing process. Fabrication is where the material will probably see its first and worst thermal excursions. The amount of weave plays a part in the drilling in some of the HDI laser vias too.

Johnson: Are there other specifics in materials that designers should be considering?

Creeden: Absolutely. Another major consideration nowadays is thermal properties. There are many different market spaces where the end user will place their circuit board in a high-temperature environment. For thermal concerns, we're seeing a lot of people using different polyimide materials, such as automotive or military under the hood where the temperatures are extremely high.

We've talked about the dielectric material, but the other major part of circuit material is the copper. Copper has been our conductive metal of choice going way back. The metal comes in two forms. There's an electrodeposited type of copper both in the holes and on the surface, but there's also a base copper, which is either rolled on to prepreg or clad right onto the core laminate itself. Copper is used because it is highly conductive with low resistivity and will transmit voltage/current. It's affordable, available, and relatively easy to manufacture. The base copper comes in different thicknesses. When you feel it, you're amazed at how easily you can distinguish the weight by holding a couple of sheets of different weight. And copper has an ability for thermal dissipation, which is helpful. If you put a power and ground plane layer next to each other (close so that they couple well) and they're both thick layers of copper, you can typically carry more current, so that's another property it would have.

But when the copper is put onto the prepreg, it needs to bond. When it's laminated, the resin needs to adhere to the metal. Usually, the metal has a smooth side and a rough side, and the rough side gives you that adhesion required to bond to the material, which will hold it down. And that's measured as a peel strength. This could be realized if you need to do solder rework, especially if the pads/lands are small, they'll have the potential to peel right off the board, which would destroy it. So, they have this rough side to hold it down.

If you look at it in a cross section under a microscope, you'll see how rough it is, which is problematic from a high-speed perspective. And when I explained how the field goes between the bottom side of a trace and the ground plane underneath it, most of the energy is on the bottom side of the trace, which is the rough side. Therefore, the topology of that rough copper is not good for what's known as the skin effect where the electrons are bumping on the surface of the copper facing the ground plane. As a solution, the industry has produced very low-profile copper, but it's threatened by that adhesion and peel strength challenge. I'm seeing engineers consider putting the ground plane opposite the smooth side of the copper, trying to guide the wave towards the smooth side. Not all circuits can do that, but that is one way to get around it if you're stuck with the rough side of the copper. Again, getting low-profile copper with good adhesion is the advancement that we need with materials today.

Getting low-profile copper with good adhesion is the advancement that we need with materials today.

In addition, the devices and circuitry are getting smaller and smaller. The standard pin pitch of BGAs are 1.0 mm, but BGA pin pitch keeps getting smaller (0.8, 0.65, 0.5, 0.4, 0.35, 0.25 inches, and smaller). Consequently, high-definition and rectangular, square-edge traces are important. The traditional fabrication process is subtractive where you etch in, resulting in an interconnect with a trapezoidal geometry. However, it is difficult and inaccurate to create a microtrace that is less than roughly 88 µm (0.0035 inches) with a trapezoidal geometry. The definition becomes imperative and should have well-defined, squared edges. This is accomplished using some additive or semi-additive methods. Some of the dry-film photoresist materials are used for that, and we're going to see that become more and more prevalent as people must use microtraces and microfeatures. Ormet's sintering paste is one of the best innovations for any-layer HDI vias along with innovations with DuPont's conductive inks, which will help define the printed electronics needs that are now happening.

Johnson: That's very comprehensive, Mike. Is there anything else you'd like to mention?

Creeden: There's always something else to consider. The inquisitive mind of a design engineer is always trying to look and consider everything, and that's where diligence pays off. It's a relentless profession where the pursuit of excellence is what makes us move forward. And ensuring your materials are appropriate for your circuit is no longer a thing of the future. It's our present challenge, and we should make it our success story.

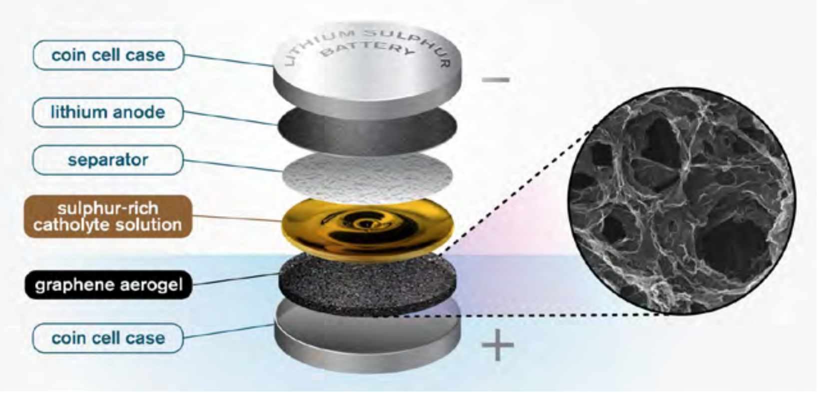
Johnson: Thank you, Mike.

Creeden: Thank you, Nolan. I appreciate this opportunity to serve. **PCB007**

Graphene Sponge Helps Lithium-sulphur Batteries Reach New Potential

Researchers at Chalmers University of Technology in Sweden recently unveiled a promising breakthrough for lithium-sulphur batteries, using a catholyte with the help of a graphene sponge.

The researchers' novel idea is a porous, sponge-like aerogel made of reduced graphene oxide that acts as a free-standing electrode in the battery cell and allows for better and higher utilisation of sulphur. They previously experimented with combining the cathode and electrolyte into one liquid—a "catholyte." The concept can help save weight in the battery as well as offer faster charging and better power capabilities.



Compared with lithium-ion batteries, lithium-sulphur batteries offer several advantages, including a theoretical energy density of approximately 1,000-1,500 Wh/kg compared to lithium-ion batteries' 350 Wh/kg.

The problem with lithium-sulphur batteries so far has been their instability, and consequently, their low cycle life. But the new prototype from Chalmers researchers demonstrated an 85% capacity retention after 350 cycles. The new design avoids the two main problems with the degradation of lithium-sulphur batteries–one, that the sulphur dissolves into the electrolyte and is lost, and two, a "shuttling effect" where sulphur molecules migrate from the cathode to the anode. In this design, these undesirable issues can be drastically reduced.

The researchers note that there is still a long journey to go before the technology can achieve full market potential. New manufacturing processes will need to be developed to make them commercially viable.

The research was published in the *Journal of Power Sources.*

(Source: Chalmers University of Technology)

Spark an Idea

Flex Talk

Feature Column by Tara Dunn, OMNI PCB

"Everything you imagine is real," is a well-known, inspirational quote by Pablo Picasso often interpreted in the context of the power of the imagination. This phrase parallels something I find true in flex and rigid-flex design. Often, the applications for flexible circuits are simply limited by our imagination. One of the favorite parts of my job are the days when I meet with a group of engineers and designers to talk about flex and rigid-flex. We might do a "lunch and learn" with a general overview of the technology or address a specific challenge. It is always helpful to bring samples to pass around and show different features. Usually, looking at a sample will spark an idea and the comment, "I wonder if we could do something like this." From there, the brainstorming begins.

Knowing this month's theme was going to be "everything starts with design" made me wonder if I could make something similar happen by looking at pictures rather than holding flex and rigid-flex in your hands. If these pictures help generate an idea for a new design, I would love to hear about it. If not, I will point out some of the best practices being utilized in these designs that should be beneficial to those new to flex and design—and maybe a good reminder to those more experienced.

Let's start with a basic flex design. Figure 1 is a straightforward, single-sided design connecting two components. I imagine this could replace wire and save space and weight. It could also replace a rigid board and solve a packaging issue. The FR-4 stiffeners are important here to support the weight of a heavier component and prevent damage to the flex circuit.

Figure 2 is a double-sided flex, using a combination of through-hole and SMT components. In this image, you can see the polyimide stiffener in the tail area. Zero insertion force) (ZIF) connectors are a common termination method for flex and require tight tolerances for both the outline and the overall thickness. Polyimide stiffeners are commonly used to increase the thickness to meet this specification.

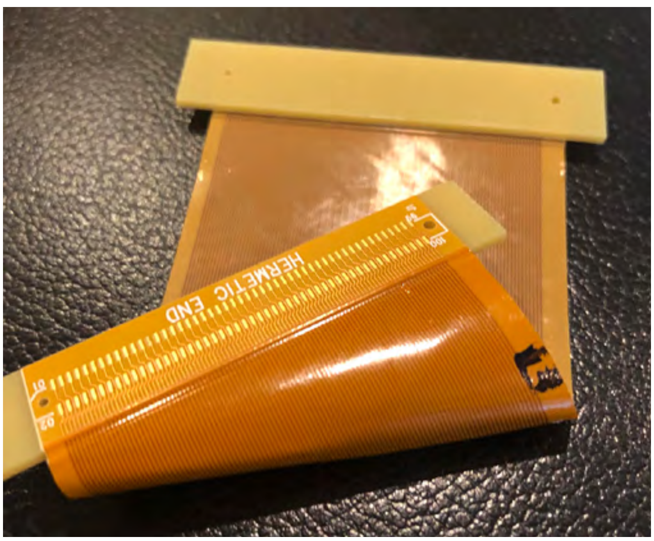


Figure 1.

Figure 2.

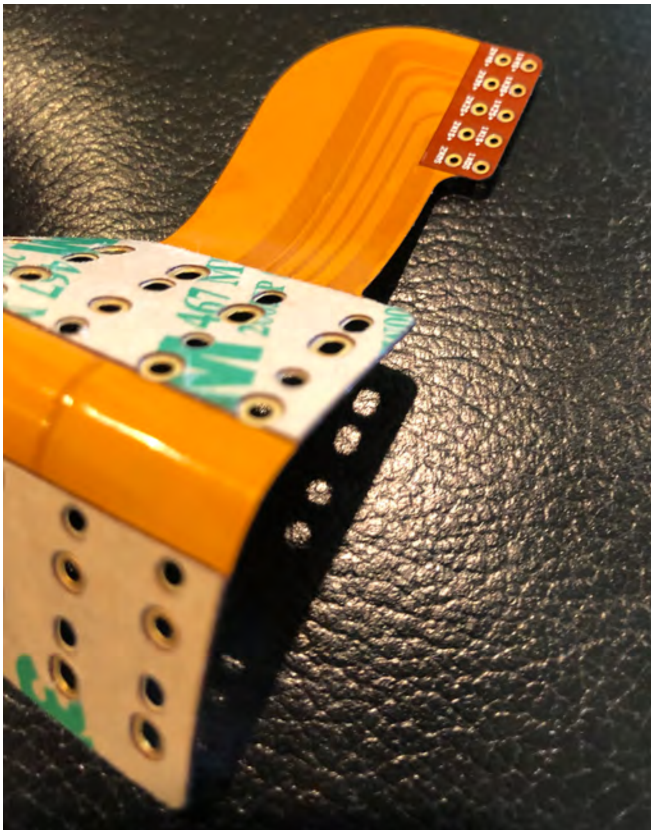


Figure 3.

Figure 4.

Figure 3 is another example of a double-sided flexible circuit. You can see from the photo that this design also uses a polyimide stiffener. In this case, the stiffener is functioning as a support for that component area, adding a bit of thickness. The other interesting thing to note about this sample is the use of pressure sensitive adhesive (PSA). This is something that doesn't really make its way into design guideline discussions but is commonly used to mount the flex inside of the unit either to be sure it remains in place through the life of the product or to help anchor a section that is going to have a lot of flexing in end use. This is one of those items that calls for imagination.

Figures 4 and 5 are images of a double-sided flex that does an excellent job of taking advantages of packaging benefits of a flexible circuit. The shape of a flex interconnect truly allows for creativity and imagination. In Figure 4, you can imagine how this will simply drop into the unit, eliminating wire and assembly. In Figure 5, you can also imagine how that tail breaks off from the main flex area. What you can't see is the PSA being used to guide and secure that during installation.

Figure 6 shows an example of a simple rigid-flex. In this case, the FR-4 stiffeners have plat-

Figure 5.

Figure 6.

Figure 7.

ed through-holes both mechanically supporting and electrically connecting with the flex layers. This particular design required heavier copper for shielding and was in danger of not being flexible enough for the end application. To solve that problem, a loose-leaf construction was used. In this case, the layers were split into two sections.

Figure 7 is also a rigid-flex design, having circuitry included in the rigid areas. This sample gives one of my favorite views of the power of loose-leaf construction. This design did not have heavy copper but did have 10 flexible layers that if all bonded together, would never allow for the flexibility required in end use. Something that isn't shown well in the photo is the use of crosshatch shielding in the flexible layers, which is also added to the flexibility of each of these layers.

Figure 8 displays a common rigid-flex construction with two rigid areas connected by flexible layers. I wanted to include this for two reasons. First, it's simplicity. This type of design is one that many start with when they first move into rigid-flex. The concept is simple, and

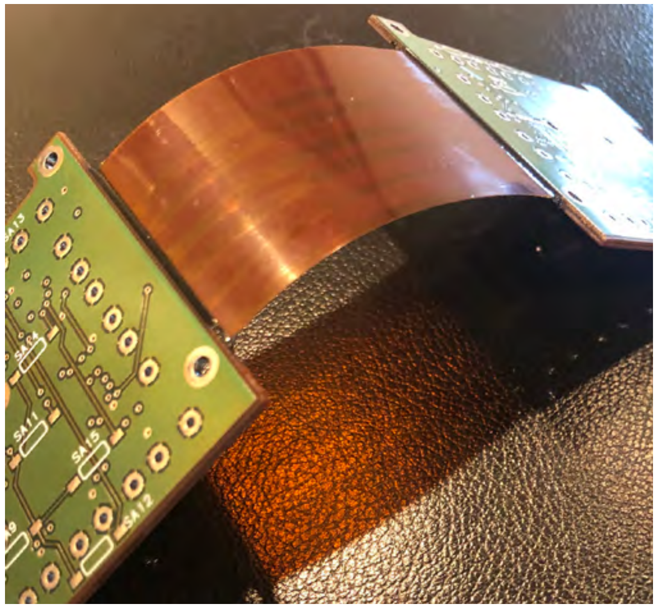


Figure 8.

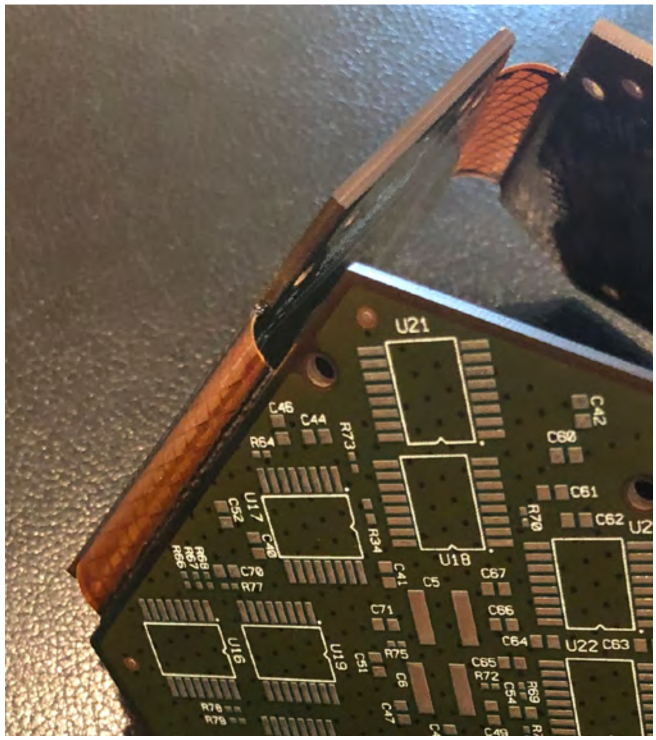


Figure 9.

this is one of the lowest cost forms of rigid-flex design. The second thing I wanted to point out with this image is the use of strain relief with a simple bead of epoxy where the flex and rigid layers meet. This prevents damage to the flex in that critical area.

Figure 9 is another example of a rigid-flex construction and demonstrates how the flex-

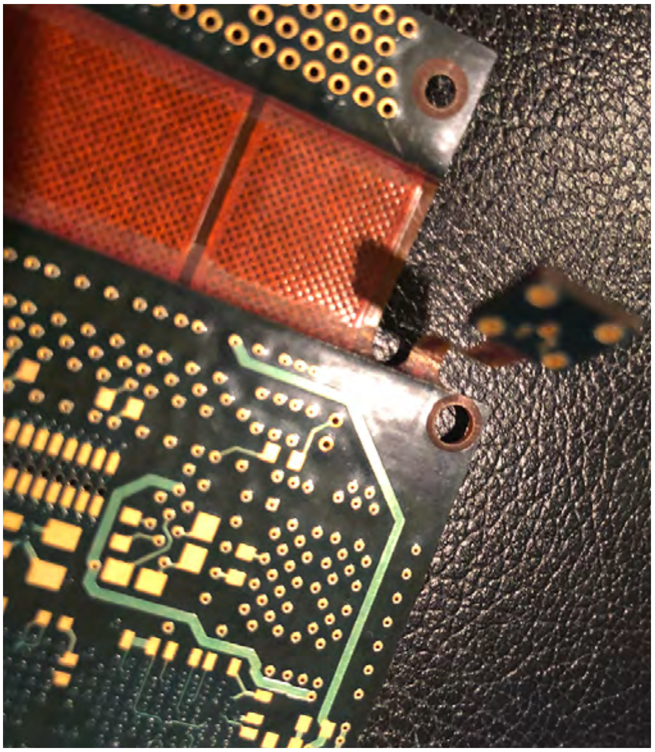


Figure 10.

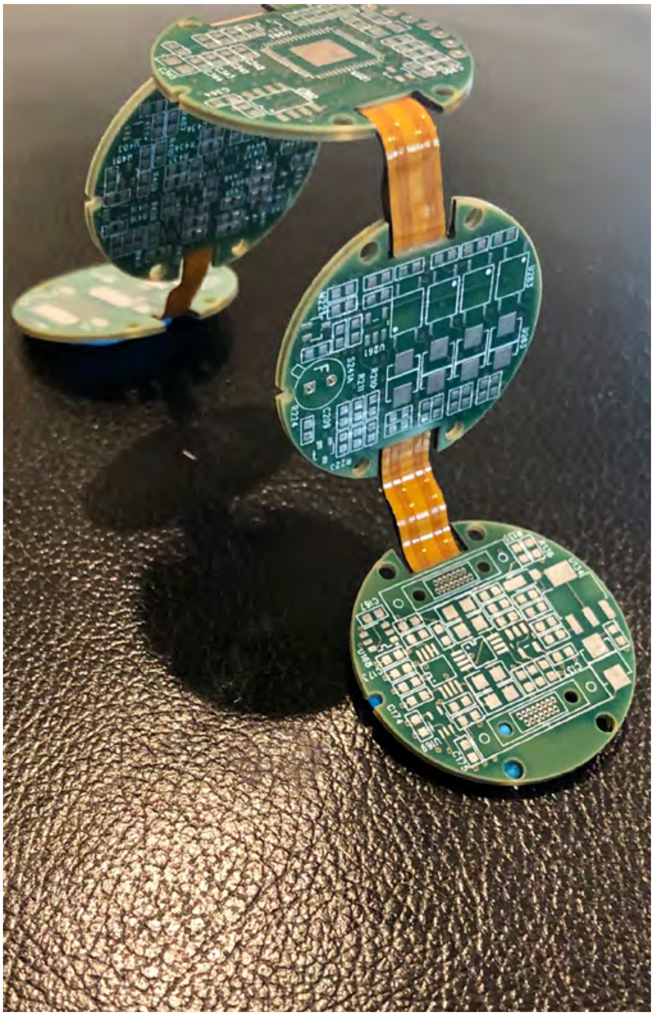


Figure 11.

ible tail areas aid in packaging. This is becoming more and more important as we are challenged to fit more sophisticated electronics into smaller and smaller spaces. This sample also shows the crosshatch copper pattern in the bend areas to improve the flexibility of the design.

Figure 10 is also a rigid-flex design, which is a little more complex with various tails splitting off from the main flex area. This is an excellent use of imagination and fits well with rigid-flex capabilities. Again, you can again see the crosshatch copper pattern to improve flexibility in the photo. What you cannot see in is the strain relief added to each section area that has a flex tail or the fact that this design will ultimately be packaged with four different bending and folding areas and the tail being routed in all directions.

Figure 11 is one final rigid-flex design that also shows the power of flex and the potential for packaging solutions. You could imagine this rigid-flex moving up and over a fixed piece in the unit while connecting complex electronics. This is an excellent use of rigid-flex to solve a packaging issue.

Flex and rigid-flex design is one of those things that allows engineers and designers to be both creative and science-driven at the same time. Hopefully, seeing some of these samples will help spark some new and creative options for solutions that need flex and rigid-flex to solve their space, weight, and packaging constraints. **PCB007**

Tara Dunn is the president of Omni PCB, a manufacturer's rep firm specializing in the PCB industry. To read past columns or contact Dunn, click here.

Electronics Industry News and Market Highlights

N.A. Smartphone Market Plunges to Five-Year Low But Samsung Rallies with Galaxy S10 ▶

Smartphone shipments in North America plummeted 18% year on year in Q1 2019 to a five-year low of 36.4 million units, down from a record high of 44.4 million in Q1 2018.

Texas Instruments Widens Its Lead As World's Top Analog IC Supplier ▶

TI's 2018 analog sales rise to $10.8 billion; Infineon moves into third position, ST posts strongest annual increase as top-10 suppliers collectively account for 60% of total analog market.

Shipments of Connected Wearables Will Reach 239 Million in 2023 ▶

Shipments of connected wearables reached 116.8 million worldwide in 2018, according to a new report by Berg Insight. Growing at a compound annual growth rate (CAGR) of 15.4%, total shipments of smartwatches, smart glasses, fitness & activity trackers, smart clothing, mobile telecare and medical devices as well as other wearable devices are forecasted to reach 238.5 million units in 2023.

Frost & Sullivan Reveals Top Internet of Things Platforms Poised for Growth ▶

With over 60 billion connected devices expected globally by 2024, IoT is a complex ecosystem that integrates Information technology (IT) with operations technology (OT) to generate data that can be analyzed to increase revenues and improve business productivity.

EU Wearables Market Hits Record Values in 2018 ▶

Shipments of wearable devices in Europe grew 30% year over year to 28.3 million units in 2018, according to data from International Data Corp. Worldwide Quarterly Wearable Device Tracker.

Worldwide Telecomm Services Market Prepares for 5G Impact ▶

Worldwide spending on telecom services and pay TV services totaled $1.6 trillion in 2018, an increase of 0.8% year over year, according to the International Data Corp. Worldwide Telecom Services Database. IDC expects for the worldwide spending on Telecom and Pay TV services to reach $1.66 trillion in 2023.

Hardcopy Device Shipments Continue in Line With 1Q19 Forecasts ▶

According to research by International Data Corp., the Western European printer and multifunction market decreased by 5.8% in unit terms in 1Q19 compared with the same period a year ago.

Digital Technologies Driving Growth in the India IT & Business Services Market ▶

The India IT & Business Services market is expected to grow annually by 8.8% to reach US$ 13.1 billion by December 2019, according to the IDC Asia/Pacific Semiannual Services Tracker—2H 2018.

Mobile Services Market in APAC to Increase Focus on B2B and B2B2C Segments ▶

The mobile services market in Asia-Pacific (APAC) is expected to focus more on business models for the business-to-business (B2B) or business-to-business-to-consumer (B2B2C) segments as a result of declining revenue from traditional services.

Virtual Verification Station From CIMS Enhances AOI Capabilities

Vladi Kaplan

Interview by Barry Matties
I-CONNECT007

CIMS is a company well-known in the PCB industry for its automated optical inspection (AOI) solutions. At this year's CPCA Show, Marketing and Technical Director Vladi Kaplan spoke to Barry Matties about a number of add-ons CIMS designed to further enhance their AOI capabilities and systems. Vladi described their Virtual Verification Station (VVS)—a server that pulls images of defects from the AOI as well as additional defect data collection, metrology, and classification capabilities—CIMS Quality Center (CQC), and Software Development Kit (SDK) as well as trends he sees with laser via inspection.

Barry Matties: Vladi, you are introducing a new product at the 2019 CPCA Show. Can you tell us about that?

Vladi Kaplan: Yes, our product is the Virtual Verification Station (VVS), and it is designed to reduce physical verification. The idea is to look at the images as seen by AOI in an intermediate stage before the board goes to physical verification on the verification stations and remove most of the false calls. In many cases, the image can easily tell the user if there's oxidation, something that looks like dust, or defects in areas that you're less concerned about. Then, you can remove them from verification, and everything that goes to physical verification will be either real defects or defects that you want to have a closer look at or you're unsure about based on an AOI-grabbed image.

We've also built it to show you simulated color images that are almost indistinguishable from video images of verification stations, although it is still a grabbed image from AOI. It's not straightforward colorization like taking a black and white picture and making it colored; this process is much smarter than that. We use complex AI-based algorithms to make the images look natural, making it easier to figure out if it's a real defect or a false call. This technology relies on many factors that enable the VVS to find the most optimal way to colorize various images. If you look at those images, you can't tell if either they're video or simulated.

Another thing I want to highlight is the automatic classification. At this stage, we can classify critical defects, such as opens, shorts, etc. The next generation of the software will

be able to go further and classify more types of defects, such as small nicks, protrusions, or false calls. The biggest challenge is to classify false calls because they can appear in many different ways, which is why we need to employ AI. We'll have to see how far it can take us because it's still a developing field. Will it be able to completely replace physical verification? That's still an open question. I don't believe it's possible in the near term. There's still going to be some physical verification, but that's where we're going and what customers are asking from us. Everybody wants to reduce physical verification, so that's the idea.

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Another product is CIMS Quality Control, or sometimes we call it the CIMS Quality Center (CQC). The idea is to display aggregated live quality information from AOI—for example, how many opens and shorts we detected, where the defects are located, and what's the yield. The live data as it comes out of AOI is displayed in one configurable dashboard. In this example, you can see only one type of information but the user can set as many dashboards as they want. For instance, you can have utilization in real time and see how many panels you've already scanned, how many panels have been verified, what the yield is, and if it goes up or down. If your shorts go up, it can trigger an alarm, so you know in real time that you have to fix something within the process and so on.

We want to make it very visual and feed this information in real time so that you can have it on your laptop or big monitor in the AOI room, for example, so that anyone can look at it. You can set up different types of graphs or charts that are most relevant for you. If you're a production manager, you may be more interested in utilization, and quality control personnel will be more interested in types of defects, their location, and where they're coming from.

Matties: What do you mean when you said it's in "real time?" Because this isn't an inline process.

Kaplan: It's AOI in real time, so as information comes out of AOI or verification, that's typically where you capture it. That's when you know for sure what type of defect it is, so as soon as you make that decision, information is displayed immediately. It's accumulating and you can have it for a day, for the last hour, for even for the last 30 days, but you get the most value if it's live.

That's why we call it the Quality Control Center; it provides the quality data as it comes in rather than waiting until electrical test, for example, when it would be too late the fix the process. And it's a pretty simple program that can run on any computer; you don't need specific hardware to run it. All of the data comes out of our server. We centralize the data collection from our AOI and VVS systems. Everything goes into one server, and this program pulls out the data and extracts all of the information that you're interested in.

Matties: Is there a server at the customer's location or a server at your location?

Kaplan: There's a server at the customer's location where all of the data is consolidated.

Matties: So, you're an equipment builder, but you're also developing a lot of software.

Kaplan: Absolutely. All of the equipment today is becoming smarter and more software heavy than hardware. At the end of the day, hardware is quite simple. You eventually build everything with some off-the-shelf component, so the expertise comes from software. Eventually, everything will become software.

Matties: And now, with the move to Industry 4.0 smart factories, when this data becomes

available to the customer, is this something that they're going to be able to plug in and have it optimize their systems automatically?

Kaplan: That would require the type of server that oversees the entire process, so we already have built-in abilities to change parameters based on the input, but it's not done automatically yet. Now, that comes down to automating the entire process. We also have a tool that we give to our customers that enables them to extract any data that they want from the AOI process and everything that runs in our databases.

The risk with database access is it's not something that you can just go in and extract information from because that can break it. There must be a safe way to do that, which is another tool that we developed—the Software Development Kit (SDK). It's a programming environment that allows a third party, which could be the customer or someone hired by them, to extract the data, analyze it further, etc. We believe that all of the data that we generate belongs to the customer; it doesn't belong to us. Therefore, our goal is to provide full and safe access to such data while ensuring integrity if the database.

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Again, making this kind of data extraction safe is the first priority and is exactly what our SDK tool is designed for. Using this tool, anyone who's familiar with the databases, including IT personnel on the customer side or third-party suppliers, will be able to figure out how to get the data out. Everything that we collect—types of defects that the system detects, utilization rates, yield data, how many panels it scanned, etc. —can be safely extracted from the database using this tool.

Matties: Regarding the software, is this something that they can purchase and add to their existing equipment?

Kaplan: Yes. As long as they're running the latest version, they have this ability. We don't even charge anything for SDK access, so we can give it for free to whoever's interested, so they can build their own tools on top of it.

Matties: Nice. How many users are currently taking advantage of this?

Kaplan: We have quite a few. They're still finalizing the whole concept and want to make sure that we have this capability. Large companies have been the most interested in this type of tool. They have a lot of equipment, so they're more forward-thinking in terms of integration and Industry 4.0 compliance for all of their equipment. Last year, we did a series of training for the most advanced customers. We brought our top software engineers from headquarters and R&D to train those customers and their IT personnel. Our people went from customer to customer, teaching them what's possible, what kind of tools they need, and what the tools can do.

Matties: For people using the VVS, what benefits have they reported back to you?

Kaplan: The most obvious benefit is that they reduce a lot of false calls before going to physical verification.

Matties: Have they said they've reduced it by a certain percentage?

Kaplan: They're still in the evaluation stage. As I said, it's very different from customer to customer, and it depends on how many false calls you have. If you have a lot of oxidation—maybe 70% of what the AOI reports is oxidation—so you can get rid of pretty much all of it. Some customers have a much cleaner environment and don't have a lot of dust that leads to false calls. Most defects are real, so you maybe get less benefit from it because you don't have a lot of false calls to begin with. Thus, it really depends on the customer. On average, you will save 50–70% in reduction of the whole verification cycle.

Matties: That's pretty substantial.

Kaplan: Right now, the most typical ratio is 1:2, meaning one AOI machine for two verification stations (VRS); if you go below that, you'll win. If there's just one AOI machine and one VVS, there's not much room for you to go from there, but if you have 10–20 AOI machines and 40 verification stations, then you can reduce to 30 or maybe even below that. So, you're already winning.

Matties: To shift gears into Industry 4.0, you have equipment at GreenSource Fabrication, and when I looked at it last year, it wasn't fully up and running with all of the automation aspects. How is all of that equipment configured?

Kaplan: We are the exclusive supplier of AOI to GreenSource. They also take advantage of our metrology capabilities built into AOI. GreenSource is probably the first one to take the metrology data and use it to correct the process, so it's an essential part of their entire concept.

Matties: Being at GreenSource, which is one of the world's most advanced PCB factories if not the most advanced factory, what lessons have you learned from that experience so far?

Kaplan: We're still going to learn more once it's up and running, but so far, what we've understood is what type of information and data they're going to need. So, we'll have some implication on future design—especially for metrology—what type of data they need to take out of the AOI, and what's important for their process. We've already learned a lot, but I think most lessons are going to come after they start running.

Matties: And fingers crossed it happens sooner rather than later. Everybody is excited to see this factory. Well, congratulations. You're doing a great job with your company. Being at GreenSource is quite a victory for you.

Kaplan: Thank you.

Matties: Is there anything we haven't talked about that you think we should let the industry know about?

Kaplan: One of the key trends that we see is laser via inspection. Companies have been inspecting laser via for a long time but usually just for sampling. Now, what we see with many companies is that their end users, such as Apple, are pushing for 100% inspection rather than sampling, so it's a big market that is opening up not only for us but for everyone, and we're definitely taking advantage of it. We have four new systems for laser via inspection. The one that we are presenting here is suitable for a 20-micron drill size. We have a system that can then inspect down to 12-micron laser drill size, which is probably still ahead of the market, so when it comes, we will have the capabilities to do that.

One of the key trends that we see is laser via inspection.

On top of that, we generate all types of statistical data that we can output, and everything can be integrated with all of this software that I just discussed, including the VVS, CQC, and SDK. So, our customer will have all their quality data in one place: traditional AOI data, laser via inspection data, and metrology output with everything integrated into one database and compliant with Industry 4.0. We believe that it's going to be one of the biggest markets for us in years to come.

Matties: Okay, thank you very much.

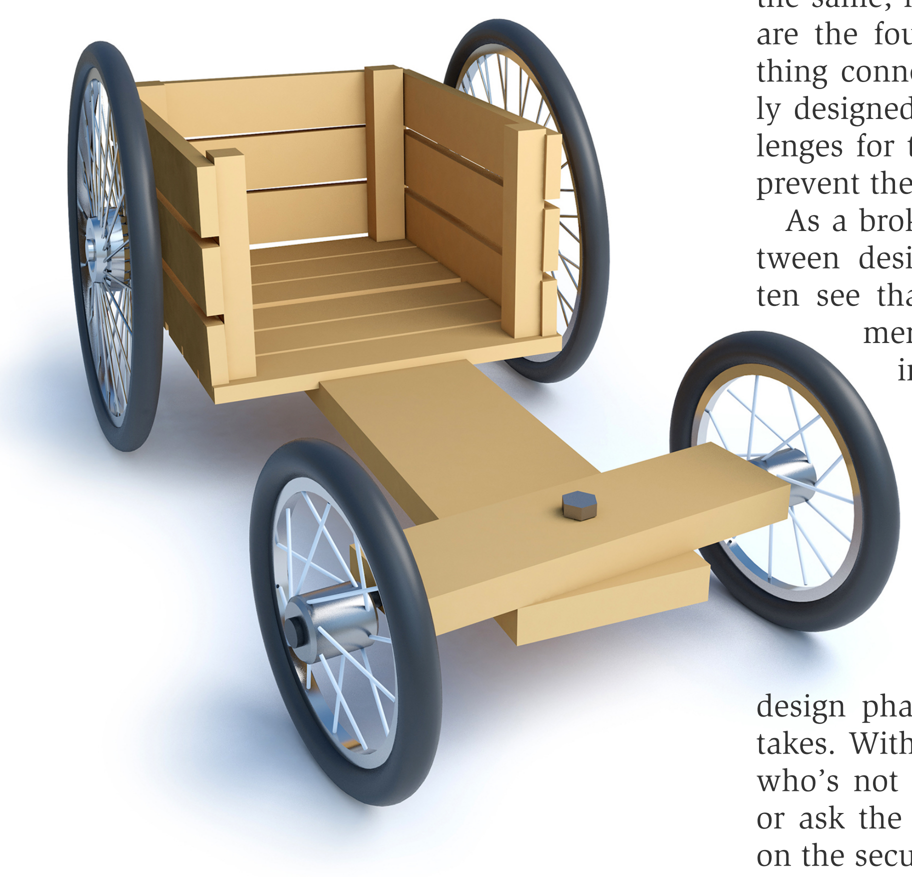
Kaplan: No problem. Thank you. PCB007

From Wooden Huts to Homemade Go-karts: It All Starts With Design!

The PCB Norsemen

Feature Column by John Steinar "Josse" Johnsen, Didrik Bech, and Jan Pedersen, ELMATICA

When we were kids, we valued the possibility to design, create, and build—the ambition to create something special over hours spent drawing or building things. The quest for making a wooden go-kart that would make you the coolest kid in the street. Sometimes, the design fits the purpose. Other times, there might not even be a plan—just pure luck to succeed, or even better, win the heart of the most popular girl with your homemade vehicle.



As adults, the situation is slightly different. For some of us, the ability to design and create withers. Some keep this creativity and create fantastic products. As technology accelerates and the toolbox develops, it opens up a whole new set of tools and inventiveness.

An Important Foundation

For printed circuits, we gave up building the coolest go-kart a long time ago, but the story is the same; it all has to start with design. PCBs are the foundation for the product—the one thing connecting the bits and pieces. If poorly designed, it might cause unnecessary challenges for the EMS putting it all together and prevent the product from working optimally.

As a broker of printed circuits—the link between designers and manufacturers—we often see that early involvement and commitment between all the involved parties in a product development process diminishes the risk for mistakes and misunderstandings. Several times, we have seen the unfortunate result of inadequate planning and execution in the early phase of the product development process. Early involvement of an experienced partner in the design phase can save you from costly mistakes. With a knowledgeable partner onboard who's not reluctant to share their know-how or ask the challenging questions, you can be on the secure side when planning.

Five Tips to Start Your Product Development Design

What tips should you provide when designing a new product? Here are five for you to consider.

1. Ask the Right Questions

When starting a product development process, you need to ask all of the important questions—why, how, where, what, when? What is possible, cost-effective, legal, and smart? Find the best solution for the heart of your electrical product—the PCB!

2. Do Your Research

When the concept is set, research and analysis begin. Involve an experienced partner to help you identify challenges, growth potential, and compliance.

3. Do Not Skip Steps

If PCB design is not your strength, involve someone with the skills. This will save you from costly mistakes. The same goes for the choice of the manufacturer.

4. Know Where You Produce

Make sure to have a trusted partner for production, offering transparency, documentation, and audited manufacturers.

5. Do Not Forget Documentation

When your product is ready for launch, use a partner with a global delivery platform and experience. You do not want your product to face trouble on the finishing line.

Product Development Process

At Elmatica, we have split the product development process into six steps from idea generation to launch. We have supported the development of thousands of products throughout the years. Even if the process is more or less the same in 2018 compared to 1971 when we started, some things have changed. Outsourcing part of the supply chain is more frequent, and the products have increased in complexity. What is the result of this? The involvement of the right competence and knowledge in every step is more important than ever.

Designing PCBs Is an Art

Often, we see a design that is not feasible or possible to produce. Sometimes, the improvements needed are either time-consuming or difficult. You just need to know what to look for and how to solve it. Designing PCB is a bit like art; there are holes, pads, and wires that need to connect. While the painting might end up on the wall inspiring many, the perfect PCB drawing might end up saving you lots of challenges later in the process. However, an artist might not always start with a set purpose for their design, but a PCB designer aims to fill a very specific one with strict schematics as the base. Because we all know that PCBs are not shelf goods.

As with anything else in life, PCB design follows the same rules: The more you know before you start, the better. What environment will the printed circuit be in? Will it fit into a box? Will tall components need to be laid down flat to fit? Will flex-rigid be the best solution? Will this affect the cost of the PCB or the final product? How many PCBs are ideal to fit into one panel? Can a different design optimize panel utilization?

Important "Dos" to Remember

No matter where your product will end up, the better you plan and design, the better the end product will be. What we often preach when it comes to PCB designing is the following points:

- Consider early cost planning, which might prevent unnecessary surprises later
- Involve the supplier as early as possible, and make sure the right capabilities are available
- Do you possess the needed PCB knowledge? If not, involve a partner who does
- Consider risk vs. cost and reliability, as this can affect both choices of technology and capability

The following statement says it all: "It's unwise to pay too much, but it's worse to pay too little." Of course, it's unnecessary to pay too much. But if a higher cost is equal to better reliability, transparency, and security, then paying too little is just the beginning of the trouble that might come. Because when it comes to PCB design or design in general, there are always some parameters to follow and adapt the design. You need to have important discussions and answer crucial questions, such as:

- **Hardware design:** What mm and tolerance requirements are there?
- **Environment restrictions:** Are there any?
- **PCB technology:** Which one is best suited for the product?
- **Material restrictions:** What is needed, and what environment will the product and PCB face?
- **Reliability level:** What is expected and mandatory?
- **Test and qualification:** How, when, and by whom?
- **Standards and regulations:** What standards does the product apply for, and are there any regulations that you need to handle?

Planks, Blocks, and Legos: Designers Evolve

Childhood in the '60s and '70s encouraged designing through planks, blocks, Legos, or whatever else we found by stacking, assembling, disassembling, sorting, or molding. We pushed the boundaries we had and developed design skills and thinking. Whether Josse's incredible PCB design skills and knowledge started with him designing a treetop hut, we will not say for sure, but it all started with the design. We have learned that even if designing has evolved since then, the tools to facilitate it have been through an even steeper inventiveness.

A good example is a previous column Jan Pedersen wrote about how the unfinished printed circuit was tested before computer-based 3D simulations were a possibility. How did they do it? Simple! They took a piece of paper, scissors, and started to cut the paper into the shape of the flexible PCB to be designed. Next, they glued this to samples of the rigid PCB and started to simulate the application. Not only did they examine how it fit into the application, but they also checked the manual assembly process and found areas where the paper was torn. Then, the model was improved, and the process started again until the sample hit perfection. It was rough, honest, handcrafted work.

As for Josse's treetop hut, Didrik's wooden go-kart, or Jan's paper models, we all want our design to hit perfection each time. However, to make that happen, we know that working thoroughly in the beginning. Involving the right parties to the table and setting the right parameters is a good start. As we say at Elmatica: What is your product or design challenge, and how can we assist you? PCB007

John Steinar "Josse" Johnsen and **Jan Pedersen** are senior technical advisors and **Didrik Bech** is CEO at Elmatica. To read past columns or contact the PCB Norsemen, click here.

John Steinar Johnsen

Jan Pedersen

Didrik Bech

MilAero007 Highlights

IPC's D.C. Focus: Chemicals Regulations, Lead-Free, Export Controls ▶

From North America to Europe, Asia, and beyond, the future of the electronics manufacturing industry is shaped in many ways by government policies. That's why IPC maintains an active, multifaceted government relations program, including leadership and networking opportunities for member company executives.

BAE Systems' Joint Strike Fighter Underpins Advanced Manufacturing Growth in South Australia ▶

BAE Systems Australia has celebrated the production of the 15,000th titanium part produced at Edinburgh Parks in South Australia for the world's largest defence program, the F-35 Joint Strike Fighter.

Wearable Sensors Could Leverage Biotechnology to Monitor Personal, Environmental Data ▶

In an effort to enhance Soldier lethality, Army researchers are developing biorecognition receptors capable of consistent performance in multi-domain environments with the ability to collect real-time assessments of Soldier health and performance.

DARPA Tests Advanced Chemical Sensors ▶

DARPA's SIGMA program, which began in 2014, has demonstrated a city-scale capability for detecting radiological and nuclear threats that is now being operationally deployed.

Incoming CEO Steve Pudles on the Acquisition of Zentech ▶

Nolan Johnson talks to Steve Pudles about the recent acquisition of Zentech Manufacturing Inc. by BlackBern Partners LLC and Zentech management. Steve, also an investor in Zentech, steps in as the incoming CEO of the new organization and discusses the deal, his new role, changes to management, and the company's plans post-sale.

Electronics Industry Endorses US-Mexico-Canada Pact ▶

Top executives from electronics companies across the United States are in Washington, D.C., this week to endorse the proposed U.S.-Mexico-Canada Trade Agreement (USMCA) and call on the Trump Administration and Congress to support policies that will drive advanced manufacturing.

Saab to Open U.S. Site for Advanced Manufacturing ▶

Saab announces a new site for advanced manufacturing and production in West Lafayette, Indiana, United States of America. The site will be located at the Purdue University-affiliated Discovery Park District. Saab intends to invest $37 million over the coming years from 2020.

Beyond the Metal: Investigating Soft Robots at NASA Langley ▶

Into the Spiderverse's newest crew of villains include a brilliant scientist named Doctor Octopus who uses flexible robotic arms to commit her dastardly deeds. Her bionic arms can throw objects, aid her in moving quickly in fight scenes, and a host of other functions.

U.S. Air Force to Launch Fifth Lockheed Martin-Built AEHF Satellite ▶

The U.S. Air Force is gearing up to launch the fifth global, anti-jam, protected communications satellite after its arrival in Florida.

Kelvin Characterization to Accurately Predict Copper Thickness

Article by Brandon Sherrieb
INTEGRATED TEST CORPORATION

Background

A few years ago at Integrated Test Corporation, we found that the reaction plan for void fallout at electrical test was ineffective and not standardized. Like many PCB manufacturing facilities (including a Sanmina shop that I used to work at), the reaction plan consisted of cross section analysis to determine the void type. Then, based on the type of void, we would either thermal stress and cross section coupons from passing boards or process passing boards through reflow simulation and retest electrical continuity for disposition.

In addition to these reaction plans, another that I have experienced at Sanmina included one where circuit boards would be processed numerous times through a micro-etch process and retested for electrical continuity if voiding was found within unfilled holes.

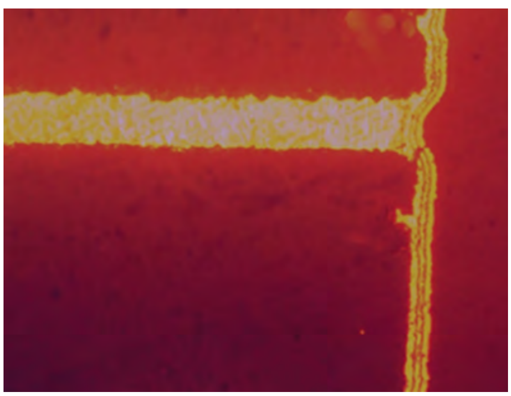


Figure 1: Example of low copper discovered during Kelvin testing.

If the panels withstood that, they should be okay, right? Unfortunately, none of these disposition methods are robust enough to ensure that vias with marginal connection are caught before shipment. As we all know, a few holes within a coupon is hardly representative of the thousands of holes within a circuit board, and processing production orders through a reflow simulation or micro-etch before assembly will negatively impact the life of that PCB.

Therefore, the only way to ensure that marginal products are not being shipped to the customer is to perform an electrical test on those suspect vias at a low enough resistance where minor differences between vias can be observed. A method that was evaluated and proven successful would be four-wire Kelvin testing; if characterized properly for your process, it can distinguish differences in copper thickness between holes. A failure discovered by this testing method is depicted in Figure 1.

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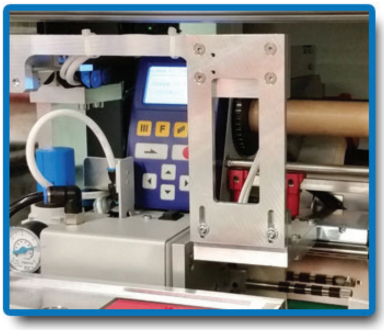

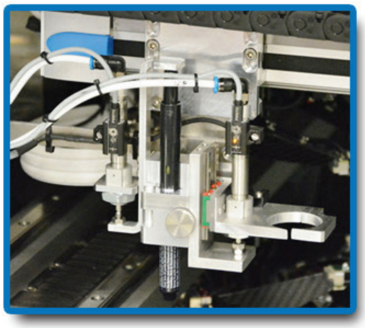

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At the time, Integrated Test Corporation did have Kelvin probes and a flying probe tester that was capable of performing the testing process. However, it had not been properly set up to accurately predict what the resistance measurements should be based on the aspect ratio of the via and the amount of copper in the hole. The first few times the process was used, all that was accomplished was to indicate which holes had resistance measurements outside of the normal distribution of results. These were then sectioned, and it was found that they would have met the minimum copper criteria. After a few instances of performing destructive analysis on nondiscrepant products, it was decided that this process required testing for proper characterization.

A quick search of articles and white papers yielded comprehensive descriptions of the process itself but not guides on how to set it up in production. Most of the papers available described building a baseline of resistance measurements with known good panels. Ultimately, the process that we desired was to accurately predict the resistance measurements based on drill aspect ratio and copper thickness. This would require a correlation between these measurements and a set of equations. These equations could then be used to set the maximum resistance specification during testing or to determine the copper thickness within plated through-holes without destructive analysis.

Characterization

At Integrated Test Corporation, very high aspect ratio vias are common in production. So, we decided to design a test panel that was 0.300” that could be drilled with coupons including 0.010”, 0.012”, 0.015”, and 0.020” vias to characterize the process for aspect ratios up to 30:1. For each diameter, via coupons were included that were copper plated with 0.0002”, 0.0004”, 0.0006”, 0.0008”, and 0.001”, respectively. To ensure that the proper amount of copper plating was deposited in the holes, boards were processed through many different plating cycles, covering and uncovering coupons with resist during each cycle. This was found to be more cost-effective than building panels exclusively for each copper plating thickness. However, doing the characterization in this manner would simplify the plating and imaging operations.

After the copper plating and etching processes were completed on the test panels, they were processed through four-wire Kelvin testing. Resistance measurements were graphed based on drill diameter (Figures 2 and 3).

After reviewing the results and observing that there was little variation in the resistance measurements with respect to aspect ratio and cop-

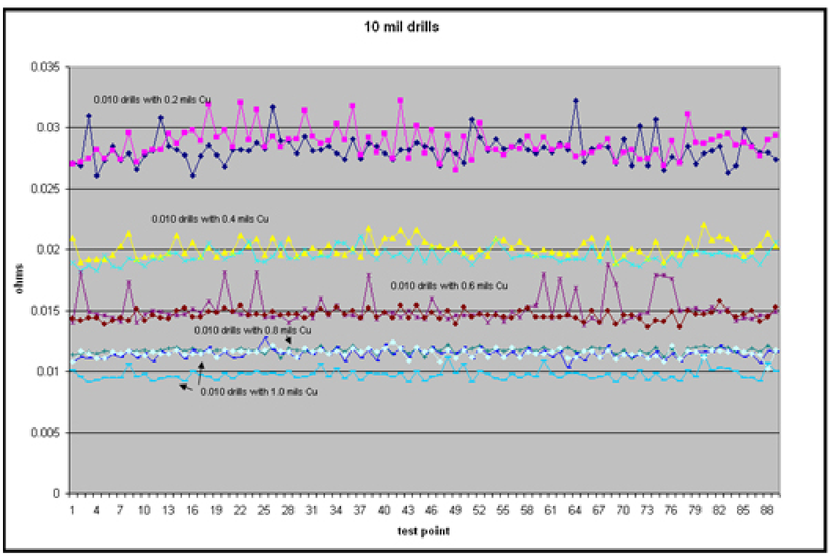


Figure 2: Resistance measurements (0.010” drill and 30:1 aspect ratio).

Figure 3: Resistance measurements (0.020″ drill and 15:1 aspect ratio).

per thickness, the average, minimum, and maximum resistance values for each test coupon were graphed based on the copper thickness for each aspect ratio (Figure 4). A second-degree polynomial trendline was added to the data and strongly correlated for each of the given aspect ratios (R^2 = 0.996 (15:1), 0.993 (20:1), 0.995 (25:1), and 0.999 (30:1)). Given a known resistance Y and solving for X would determine the copper thickness; conversely, given a known copper thickness and solving for Y would determine the resistance measurement.

These trendlines would accurately predict the four-wire resistance measurements if there were only plated through-holes at these precise aspect ratios to consider. But what if copper thickness needed to be determined on a via at an aspect ratio that fell outside of this range or was within the range but not one of the tested aspect ratios? Then, it would be necessary to extrapolate from the data to generate the curves to predict at these other aspect ratios.

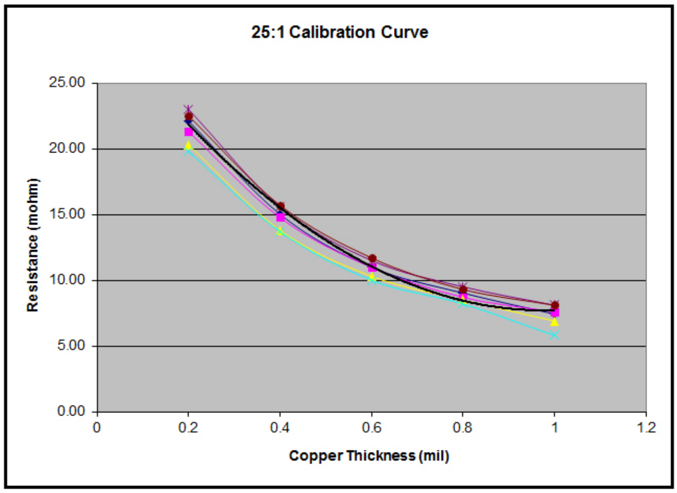


Figure 4: Resistance measurements for 25:1 aspect ratio (average, minimum, and maximum).

To do this, the second-degree polynomial trendlines that were created for each aspect ratio (Table 1) were reviewed and the quadratic

Aspect Ratio	Equation	Second-order Coefficient	First-order Coefficient	Intercept
15:1	$11.5x^2 - 23.1x + 15.6$	11.5	-23.1	15.6
20:1	$16.4x^2 - 32.1x + 21.1$	16.4	-32.1	21.1
25:1	$23.4x^2 - 45.7x + 30.1$	23.4	-45.7	30.1
30:1	$24.6x^2 - 52.1x + 37.5$	24.6	-52.1	37.5

Table 1: Resistance trendline equations by aspect ratio.

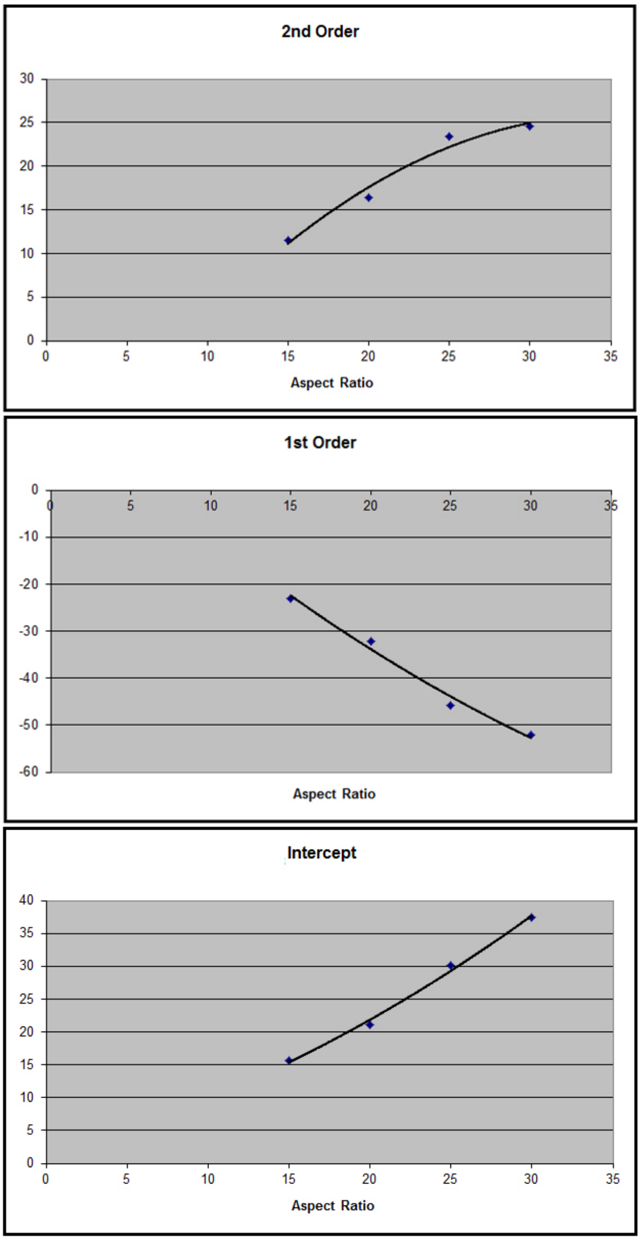


Figure 5: Quadratic equation coefficients with trendlines.

Aspect Ratio	Resistance by Copper Thickness (Mils)
10.0:1	$2.85\ x^2 - 9.76x + 9.86$
12.5:1	$7.23\ x^2 - 16.26x + 12.50$
17.5:1	$14.62\ x^2 - 28.30x + 18.50$
22.5:1	$20.15\ x^2 - 39.03x + 25.47$
27.5:1	$23.83\ x^2 - 48.45x + 33.41$
32.5:1	$25.67\ x^2 - 56.57x + 42.32$
35.0:1	$25.89\ x^2 - 60.14x + 47.14$
37.5:1	$25.65\ x^2 - 63.39x + 52.20$
40.0:1	$24.95\ x^2 - 66.31x + 57.50$

Table 3: Resistance equations by aspect ratio.

coefficients for each equation were plotted. A trendline was again added to each of the graphs (Figure 5).

Again, second-degree polynomial trendlines strongly correlated to the plotted coefficient data (R2 > 0.974). The trendline equations (Table 2) for these coefficients would help determine the coefficients for unknown aspect ratios.

The variable X in these equations represents the aspect ratio. Therefore, any aspect ratio that is desired can be substituted into each of these equations to determine the first- and second-order coefficients and intercept for the quadratic equation that will ultimately determine the resistance of a plated through-hole based on copper thickness. Table 3 shows the equations that were derived from this information.

Graphs of resistance versus copper thickness at aspect ratios ranging from 8:1 to 40:1 generated from these equations are depicted in Figure 6.

These graphs and equations were used to create a simple calculator in Excel that would output a maximum resistance value based on a given aspect ratio and minimum copper thickness. This value is then used as an upper specification limit when processing boards through four-wire Kelvin testing. Plated through-holes that failed this specification limit (resistance measurements higher than this limit) would have copper thicknesses that are lower than the user-defined minimum. Conversely, the calculator can also output the copper thickness given a known resistance and aspect ratio.

Coefficient	Equation	Coefficient of Correlation
Second Order	$-0.037\ x^2 + 2.587x - 19.318$	R2 = 0.974
First Order	$0.026\ x^2 - 3.19x + 19.533$	R2 = 0.986
Intercept	$0.019\ x^2 + 0.618x + 1.745$	R2 = 0.995

Table 2: Quadratic coefficient trendlines by coefficient.

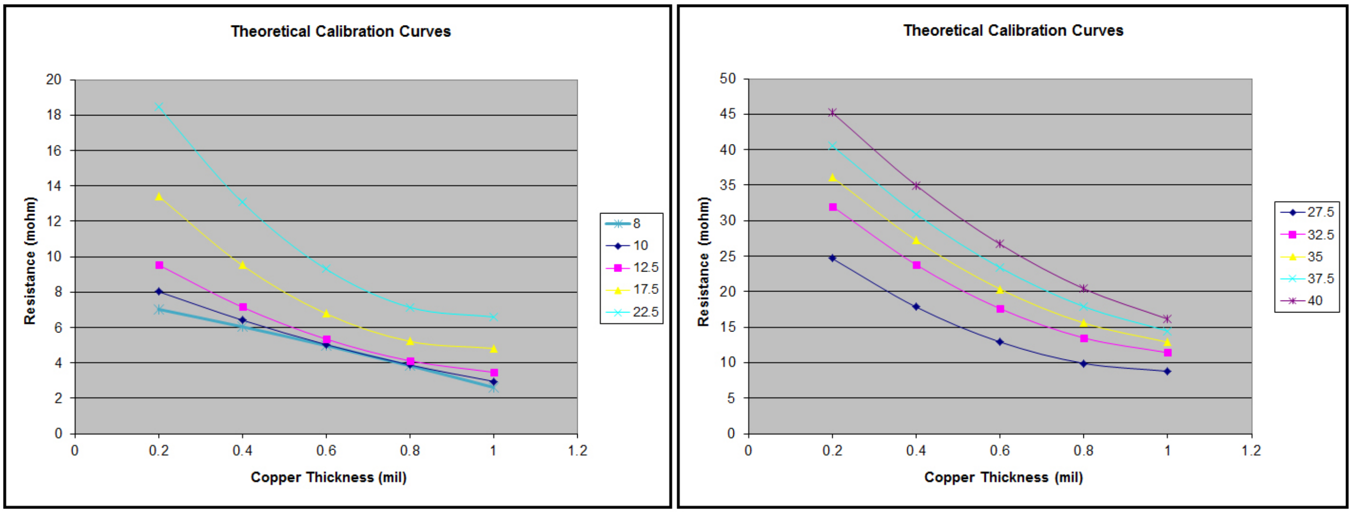


Figure 6: Resistance versus copper thickness.

Applications

The main area where we observed benefits utilizing this process was dispositioning orders where there was fallout for voiding. We still completed failure analysis for corrective action and process improvement but utilized four-wire Kelvin testing to disposition the nondiscrepant product that was processed at plating during the same time. This ensured that products with low copper that could potentially lead to field failures were not shipped to the customer. Examples of copper voiding that were dispositioned using four-wire Kelvin testing are shown in Figures 7 and 8.

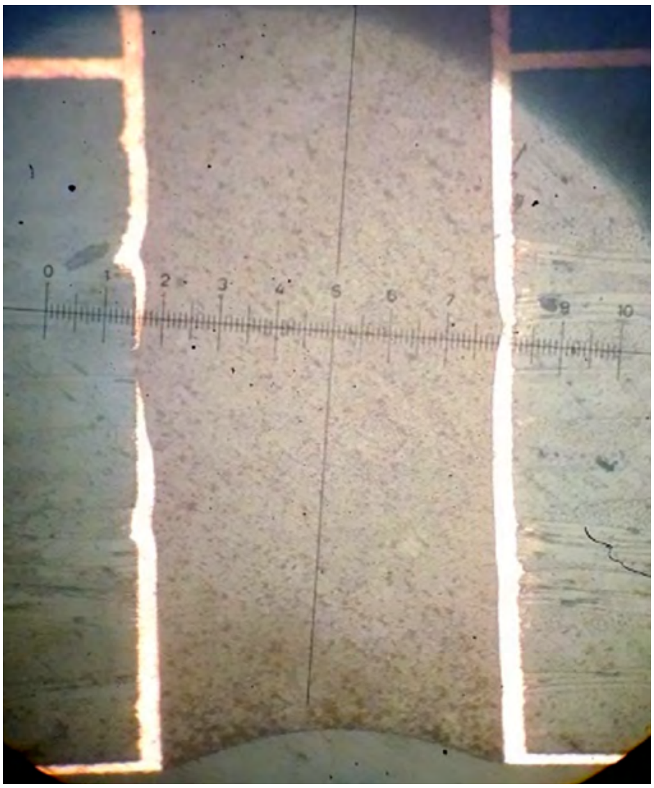


Figure 7: Copper voiding dispositioned by four-wire Kelvin testing.

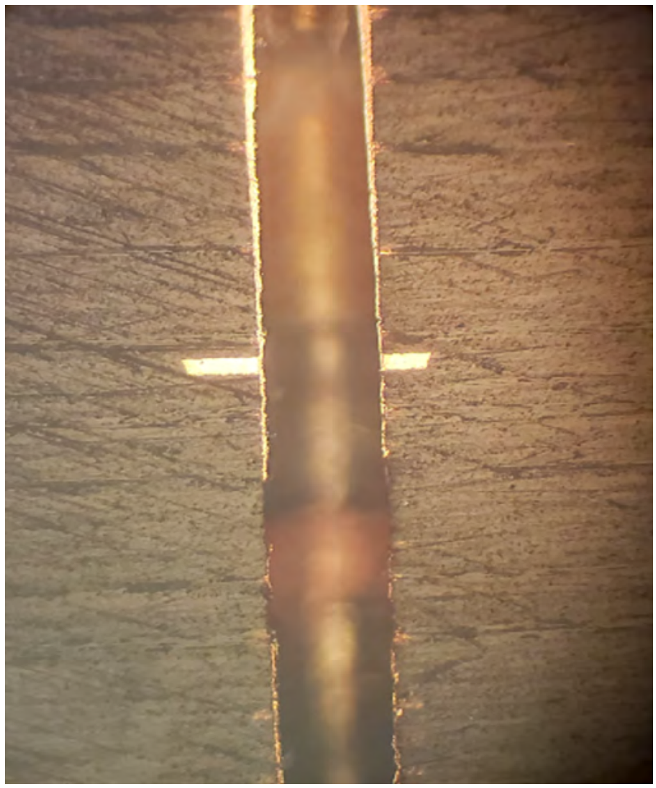


Figure 8: Copper voiding dispositioned by four-wire Kelvin testing.

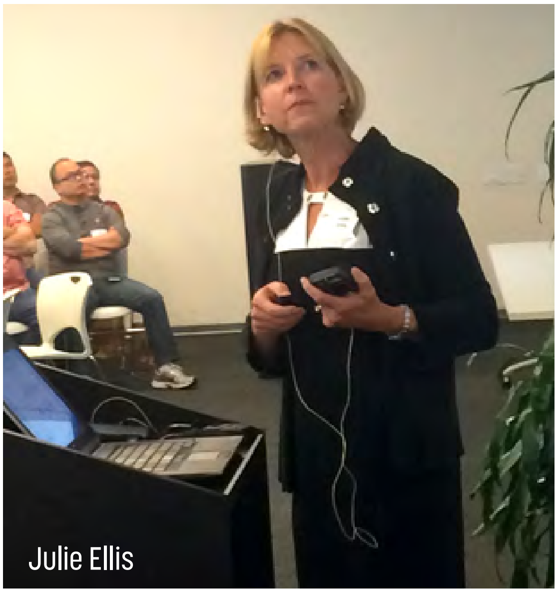
This process can also be utilized to pinpoint the through-hole vias that fail customer specification for plating thickness. Theoretically, these vias could then be processed through rework plating cycles and retested to determine the efficacy of the rework process. Since this is a non-destructive process, products would then be viable for shipment. There are cases where we have customer-finished hole diameter requirements where the PTH to inner layer spacing prohibits oversizing the PTH drill as much as our design guidelines indicate we should. This limits our drill diameter and the amount of plating that we can plate in the via and still meet the finished requirements. Since our plating window is drastically reduced, we utilize Kelvin resistance measurements to disposition the copper thickness in the final product so that we are certain that the minimum plating thickness criteria are met.

Finally, we utilized this process to improve the reliability of a conductive bonding process that we use. We baselined our current process before and after component assembly and made improvements to the manufacturing and assembly processes by comparing the impact that these changes had on the Kelvin resistance measurements. In addition, Kelvin testing assisted our company in qualifying a more thermally robust dielectric material to use in this process. Different materials were tested, and the percent change in the Kelvin resistance measurements was reviewed and compared through the assembly reflow process.

Conclusion

Four-wire Kelvin testing can provide significant benefits to your plating and testing processes provided that it is adequately set up to your process. Following the steps that have been outlined, this testing process will be set up properly and have the ability to accurately predict the copper thickness in plated through-holes. This allows you to adequately disposition plating voids without costly cross section analysis. It also allows you to determine exactly which holes do not meet specifications and may require rework and ensures that there are no escapes to customers, which may result in costly field failures. Overall, Kelvin testing provides an excellent way to characterize, baseline, and improve your process. **PCB007**

Brandon Sherrieb is currently the process engineering manager at Integrated Test Corporation in Dallas, Texas. He has a degree in mechanical engineering and 15 years of process engineering experience in the industry with a focus on mechanical and thermal processes.



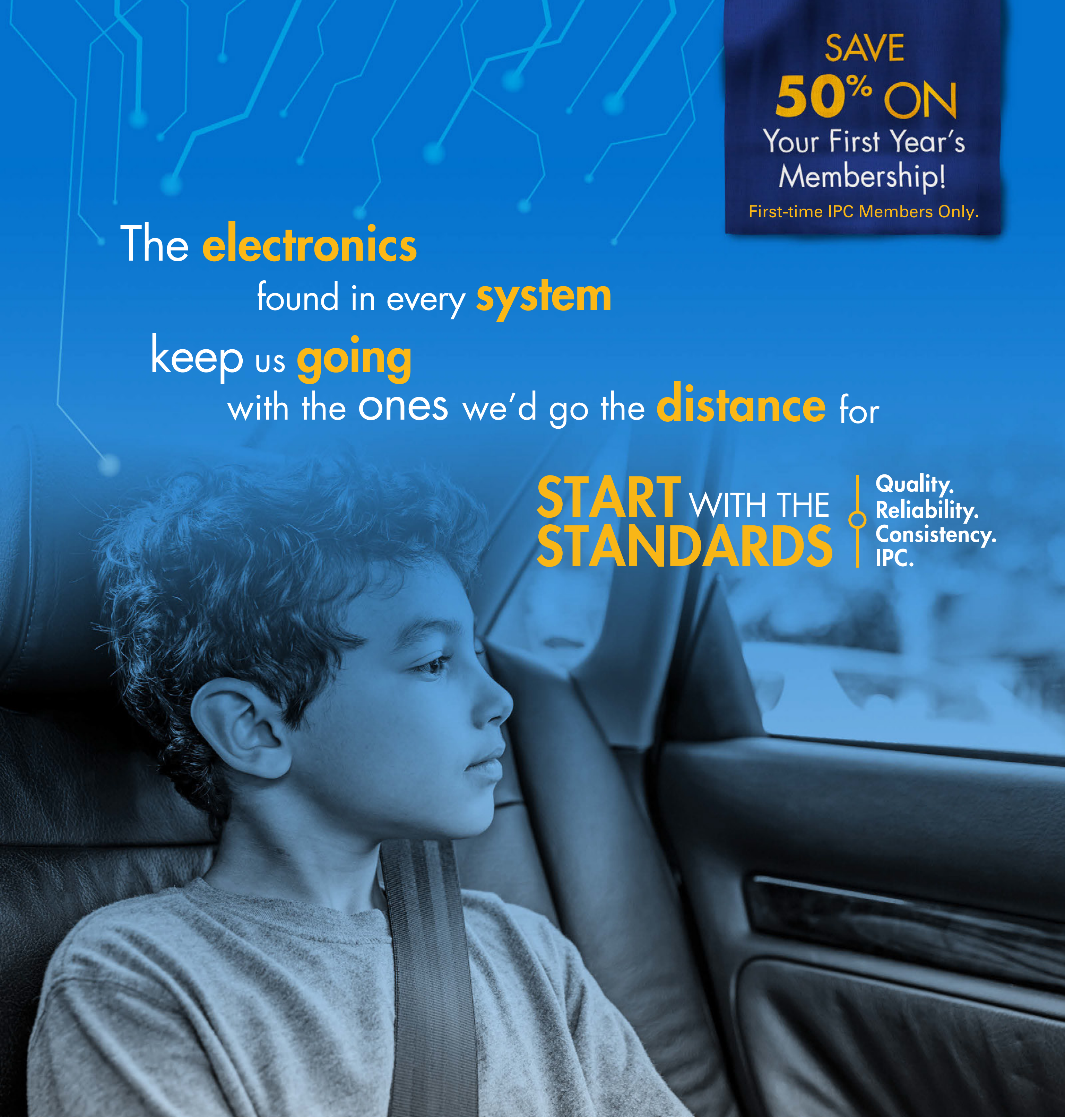
Julie Ellis

Design Is a Pivotal Piece of the Puzzle

by Andy Shaughnessy

As a field applications engineer at TTM Technologies, which has fabrication and manufacturing locations around the world, Julie Ellis sees a wide variety of customer design requirements. In this interview with the I-Connect007 Editorial Team, Julie explains how PCB designers can influence the development of the PCB. She shares a variety of tips and tricks that designers can implement early in the design process to help optimize fabrication and assembly later on and keep small issues from becoming big problems downstream.

To read this entire article, which appeared in the June 2019 issue of *Design007 Magazine*, click here.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PCB007 Supplier Highlights

Averatek on the Future of Additive and Semi-additive Processing ▶

Averatek's President and COO Mike Vinson talks with Barry Matties about the benefits semi-additive and additive processing can bring to the shop floor as well as some of the current challenges and limitations that continue to leave many manufacturers hesitant to implement the technology.

Alun Morgan on the Future of PCB Materials ▶

The I-Connect007 editorial team asked Alun Morgan, technology ambassador for Ventec International Group, to discuss materials at a high level. Our conversation delivered a detailed overview of the current state of the electronics industry.

DuPont on New Beginnings and Empowering the Industry ▶

Andy Kannurpatti gives the I-Connect007 team an overview of the latest news from DuPont Electronics and Imaging. Including investments toward the new production assets in Ohio, Silicon Valley Technology Center, and other facilities. He also details how the company is engaging OEMs and PCB fabricators and design teams, as well as some exciting business updates coming this spring and summer.

Making Materials Succeed: Past, Present, and Future Trends ▶

Tony Senese—manager, business development group, Panasonic EMBD—gives Nolan Johnson an overview of materials and components as well as changing business models and methods to make materials succeed and how to stay profitable.

Nano Dimension Reports 2019 First Quarter Financial Results ▶

Nano Dimension reported revenues of $1.69 million for the first quarter of 2019, compared to $1.7 million in the fourth quarter of 2018, and $635,000 in the first quarter of 2018. The increase compared to the first quarter of 2018 was attributed to higher commercial sales of DragonFly Pro systems.

Rogers Comments on Commerce Dept. Designation of Huawei ▶

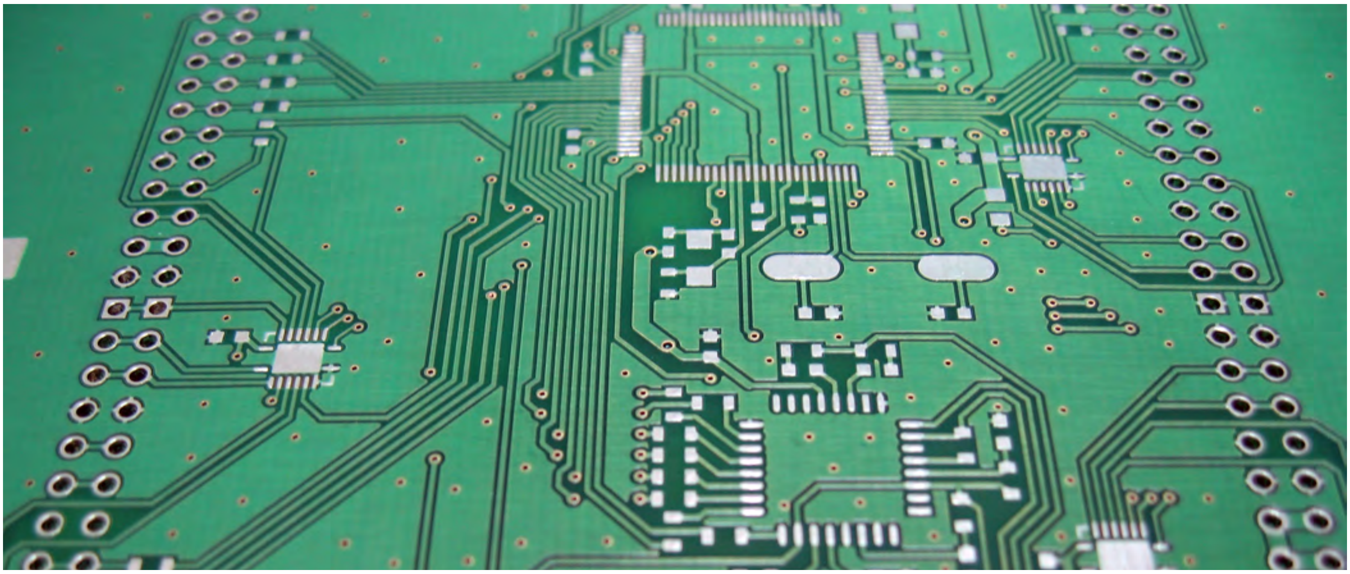
Rogers Corporation commented that it has evaluated the recently issued U.S. Department of Commerce export control restrictions relating to Huawei Technologies Co. Ltd. and its affiliates and is implementing additional compliance processes for sales to Huawei's fabricators and converters, which are Rogers' direct customers.

Orbotech Celebrates Success of Orbotech Diamond and Discusses Future Trends ▶

Barry Matties caught up with Meny Gantz—VP of marketing for Orbotech's PCB division—to talk about the drivers behind the success of Orbotech Diamond systems, the future, and Industry 4.0.

Flexium Revenues to Surge on PI Board Shipment Growth in 2H19 ▶

Taiwan-based Flexium Interconnect expects its revenues and profits to improve quarter by quarter on more shipments of PI (polyimide) boards for antenna use, after hitting the bottom in the first quarter of 2019 on weak demand for smartphones.



Conventional Exposing: Direct Imaging Solder Mask

Article by Nikolaus Shubkegel

When you compare direct imaging of solder mask with contact exposure of solder mask, the positive aspects and the advantages are clear. Without a doubt, direct imaging shortens the throughput time and eliminates artwork production. It also eliminates the costly measurement of the panels and manufacturing of artwork with different scaling factors.

In this article, I present seven of these defects. These defects occur rarely on contact exposing and only when the process is not well balanced. The occurrence of these defects can be explained by the fundamental differences between contact exposure and direct exposure. But first, let's review the direct imaging processes.

The biggest advantage of direct imaging is the ability to scale and change the dimension of each individual exposure for the best fit. With direct imaging, it is possible to expose different cards on the same panel with different spreads. The scrap rate due to misregistration tends toward zero. This is because, with artwork, you need to produce photo tools with different scaling factors, making nonlinear scaling impossible.

Direct exposure solder mask, however, does have its own set of unique defects that occur. Thankfully, these defects are well known. Due to the increased use of direct imaging of solder resists, these defects occur more often. These defects depend on the solder mask chemical composition and the photoinitiator package (a compound that reacts to light, initiating or catalyzing a chemical reaction), so they can be a bit different from solder mask to solder mask. How the defects appear depends on the direct imaging unit, the wavelengths of the system, the general process parameters, the drying conditions, and the developing parameters. Even the pre-cleaning process can sometimes have an influence.

These direct exposure defects occur early on during implementation of a direct exposure unit. Once the process is optimized, the defects no longer occur. In general, there are also possibilities to prevent these defects; in other words, they are manageable.

Four Fundamental Differences Between Direct Exposure and Contact Exposure

1. Oxygen Inhibition of Surface Crosslinking

First, a fundamental difference is the oxygen inhibition of surface crosslinking. Contact exposure occurs under vacuum. A side effect of this is that oxygen adsorbed on the solder mask surface is desorbed. This low oxygen concentration does not interfere with the crosslinking of the solder mask. With direct imaging, rather, the exposure happens in the air and under normal pressure. The oxygen inhibition effect strongly depends on the photoinitiator package. Some solder resists are very sensitive to oxygen inhibition while other systems are insensitive to the presence of oxygen.

Exposure transforms certain photoinitiators from the solder resist into free radicals. These free radicals start the crosslinking of the solder resist. A portion of the free radicals stabilizes by a reaction with atmospheric oxygen. These stabilized radicals are no longer available for crosslinking. As a result, the crosslinking on the solder mask surface is disturbed by the loss. When crosslinking is incomplete, the solder mask surface will be sticky, dull, and porous. Some photoinitiators start the polymerization via a cationic photopolymerization. In this case, oxygen inhibition generally does not occur, but there are exceptions.

2. Narrow-band Light Frequencies for Direct Imaging

The second problem with direct imaging happens because light in the 200–350 nm range is missing. Contact exposure relies on mercury vapor lamps, short arc lamps, ultra-high-pressure lamps, etc., for its radiation sources. These lamps radiate throughout the UV range (200–400 nm), in the visible range (400–760 nm), and far into the infrared range.

In contrast, direct-exposure light sources emit a few discrete wavelengths in the 355–420 nm range. This radiation penetrates deep into the solder resist and starts the crosslinking in the entire mask. But these light sources do not penetrate into the solder mask because the solder mask resin absorbs strongly in this area. The solder mask starts a massive crosslinking on the solder mask surface, creating a protective skin. The surface is sealed, the chemical resistance is improved, and the moisture absorption is reduced.

3. Quantum Yield Mismatches Due to Wavelength and Solder Mask Not Being Compatible

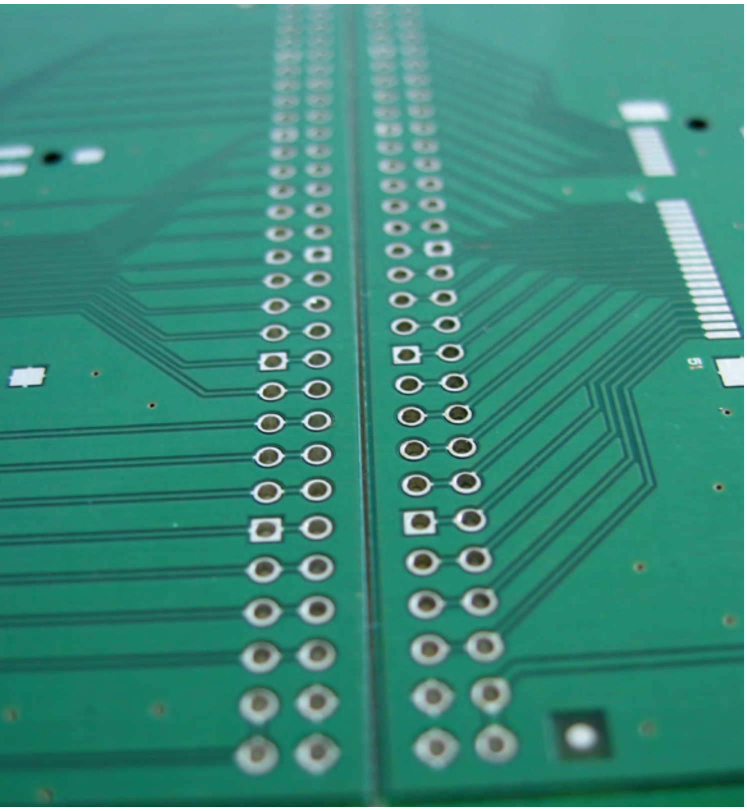
A third difference is the quantum yield in the formation of radicals at different wavelengths. In contact exposure, the difference in the quantum yield between the individual wavelengths does not play a major role. The whole UV range is available. Conversely, in direct exposure, one or more wavelengths are used, which form free radicals with a certain yield. Some wavelengths are very efficient with some solder resists while other wavelengths are very ineffective, which explains the different results when exposing a solder resist on different direct imagers.

4. Longer Exposure Times in Direct Imaging

The fourth problem with direct imaging is the need for longer exposing times compared to contact exposure. This is not a defect, but it does make implementation more difficult. Presently, more and more companies are switching entirely to the direct imaging of the solder mask. Some companies have maintained contact exposing and partly switched to direct exposure for reasons of capacity. However, contact exposure is still the first choice for other companies.

Since the exposing times are long, solder mask manufacturers have responded to the requirements of PCB shops by optimizing coatings for direct exposure. Existing solder masks have been modified so that all qualifications remain. It should be noted that these are still more traditional coatings and are not developed purely for direct exposure.

There are also solder masks available that have been developed specifically for direct imaging. These products require an unbelievably low exposing energy. In most cases, this means the introduction of a new solder mask with all of the necessary qualifications. In an extreme case, a coating for direct exposure might mean



designing a product for a specific machine. This is feasible but means introducing a new solder mask onto the manufacturing floor that, most likely, does not work optimally on any other direct imaging systems at that facility.

The direct imaging systems in the market can vary greatly. Available wavelengths start at 355 nm and go up to 420 nm. Some systems may feature just one wavelength, and others may have as many as four wavelengths. Generally, the light sources used include UV diodes or UV laser diodes. Alternately, some machines may feature solid-state lasers or special mercury vapor lamps. Additionally, the exposure optics vary from brand to brand.

Seven Defects

Practically speaking, these seven defects may be observed during direct exposure but generally do not occur during contact exposure.

1. Solder Mask Surface Is Dull

The solder mask surface could be more matte instead of shiny or satin due to missing wavelengths, oxygen inhibition, or the surface of the resist not being sealed.

2. Solder Mask surface Is Sticky After Development

This defect could be due to oxygen inhibition.

3. White Stains on the Mask Surface

This defect occurs after ENIG and HASL or after wave soldering and cleaning. One side can be affected or both sides over the entire area. Sometimes, there are white spots of different sizes visible. These stains are due to moisture absorption because of the missing wavelengths of 200–360 nm that seal the resist surface. By drying the PCBs at 100–120°C for 15–20 minutes, the spots generally disappear almost completely. In some cases, the defect can be avoided by better drying of the solder mask. Another option is a UV bump after developing. Higher exposure energy is also helpful.

4. Spontaneous ENIG on the Solder Mask

This defect is well-known and generally due to an overactive nickel bath. It also occurs in areas with poor rinsing. Due to the porous surface of the solder mask, palladium nuclei can remain behind and lead to nickel deposition even during good rinsing and normal activity of the nickel bath.

5. Solder Residues on the Resist Surface After HASL

On the porous surface, more solder balls and solder spiders can be left. The defect is known but rarely occurs during contact exposure. Certain configurations of solder mask, flux, and HASL parameters tend to form tin spiders. In a well-optimized HASL process, the defect does not occur.

6. Increased Ionic Contamination

This defect highly depends on local conditions. If demineralized water is used throughout for rinsing, it is generally not a problem. If city water is mostly used, it can be a problem.

7. Solder Mask Residues on Soldering Surfaces

This defect is observed when the solder mask is applied by spray coating on certain machines or curtain coating. When coating by screen printing, the defect does not occur. By curtain coating and spraying, two opposite edges of a panel are coated over the edge. Mask accumulations can also occur in the edge area, by contact of two panels at the edge, or by contact of the edge with a rack. In this area, the drying of the mask is insufficient and sticky.

During contact exposure, this area is fully exposed and the mask remains on the panel. During direct exposure, a circulating area of about 2–5 mm is not exposed. Sticky mask accumulations might remain in this area and pollute the developer. The developer is not designed to remove mask accumulations. These solder mask accumulations can be transferred by the rollers on soldering surfaces.

Conclusion

To meet the requirements of the PCB shops, the solder mask manufacturers have optimized some solder mask types for direct exposure. With products that are more light-sensitive, the exposure time on direct exposing units is reduced. The second advantage is that oxygen inhibition now plays a minor role and usually can be ignored thanks to the increased levels of photoinitiator, ensuring enough free radicals for a good crosslinking. The mask surface is less porous, however, so moisture absorption remains an issue.

The formation of condensation during thermal curing is enhanced. But the service lifetime of nickel baths in ENIG plating might be reduced due to the out-leaching of photoinitiators and degradation of products that affect the bath's service life. These decomposition products might interfere with the nickel deposition and lead to a lower height of the deposit at the corners. It should be noted that the whole process can be improved if a UV bump is added right after developing. By adding the UV bump step, excess of photoinitiator is destroyed and blown out. Consequently, the contamination of the curing oven is lower, and the nickel-gold process is less error-prone depending on the specific ENIG and solder mask process parameters in your facility.

The results of solder mask direct imaging depends on the solder mask itself, the local conditions, and the type of direct exposing unit. Direct imaging is an elegant challenge, but the seven defects described in this article are all manageable. **PCB007**

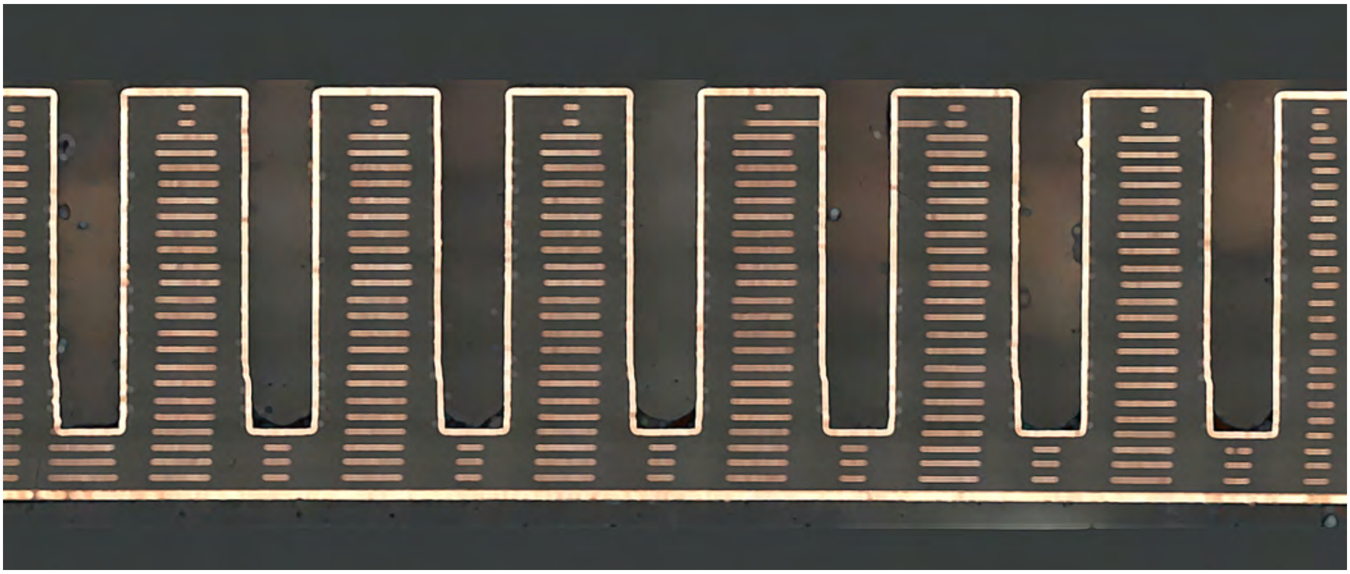
Nikolaus Schubkegel retired in February 2019. For the past 12 years, Schubkegel worked at Umicore Galvanotechnik GmbH in Germany as a technical service engineer for Taiyo products. Before that, he worked as a process engineer in the solder mask department at the former IBM-PCB plant (later STP) in Albstadt, Germany. Schubkegel obtained an M.Sc. degree in chemical engineering from the Polytechnic Institute in Timisoara.

Reversible Chemistry Clears Path for Safer Batteries

Researchers at the University of Maryland (UMD) and US Army Research Lab (ARL) have taken a critical step on the path to better high energy batteries by improving their water-in-salt battery with a new type of chemical transformation of the cathode that creates a reversible solid salt layer, a phenomenon yet unknown in the field of water-based batteries.

Building on their previous discoveries of the water-in-salt electrolytes, the researchers added a new cathode material which, lacking transition metal, operates at an average potential of 4.2V with excellent cycling stability, and delivers an unprecedented energy density higher than non-aqueous Li-ion batteries.

Leveraging the reversible halogens intercalation in graphite structures, enabled by a super-concentrated aqueous electrolyte, the team generated an energy density previously thought impossible. The researchers found that the super-concentrated solution of the water-in-salt battery, combined with graphite anode's ability to automatically build and reform a protective layer within the battery, gave a stable and long-lasting battery with high energy. The report was published in *Nature*. (Source: University of Maryland)



Vertical Conductive Structures, Part 2: VeCS and Micro-machining

Article by Joan Tourné
NEXTGIN TECHNOLOGY

Micro-machining is used every day in circuit board manufacturing with both drill and routing bits. Micro-machining is a very broad term for techniques used to shape an object. I introduce this term because micro-machining, in combination with the fabrication and processing of objects in 2.5D and 3D is not commonly used in circuit board manufacturing. But vertical conductive structure (VeCS) technology will change that.

Today, the industry has available to it the infrastructure needed to shape circuits in a different way and to create new functions and applications, such as higher density connections between internal and external layers and tuned connections that minimize signal distortion. VeCS is a multi-depth slot element currently achieved with CNC machines (part of today's infrastructure) using drill and router bits to create the shapes (Figure 1). The objective is to create a new structure that makes the vertical connections using the board real estate differently so that we do not comprise isolation.

CAF/electron migration are the primary constraints in reducing the distance between vertical connections (via hole, microvia, etc.). By using micro-machining, we can create structures that are less–or not at all–sensitive to these isolation defects. VeCS-1, as described in the first article of this series, is a slot going through the circuit from top to bottom. In this article, I will focus on VeCS-2 technology (blind slots) as more micro-machining techniques are required for VeCS-2 than VeCS-1.

Note that the examples in this article all focus on slots with the same depth. In a later

Figure 1: The basic VeCS element shown from the bottom side using two traces and a power connection at the far end of the slot. Terms for the wide structures are cross route and bottom route.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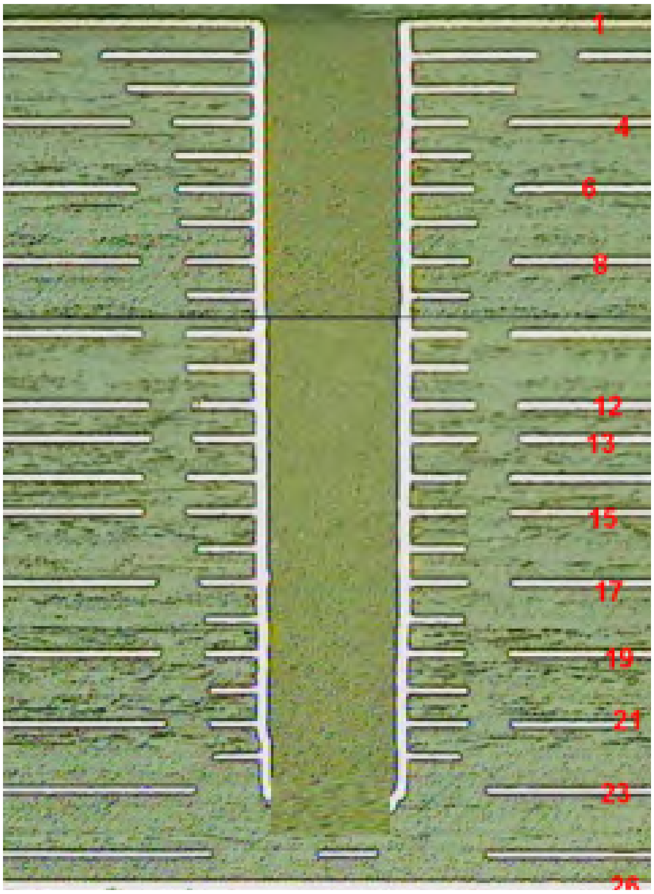


Figure 2: Basic high aspect ratio VeCS-2 element.

article on VeCS, we will see multi-depth slots connecting signals, not only connecting the signal from the outside layers to the internal layer but from, for example, layer 3 to layer 10 creating an internal layer transition. Also in future articles, we will address transparent layer transitions where more micro-machining techniques will come into play to define the different depths as well as the sequence of processing. It would be preferred to have machine codes defined that determined the depths and sequence of the processing. CAM systems need to accommodate the rules and process sequences to minimise the potential for error in engineering and fabrication.

The VeCS slot shown in Figure 2 is close to a 2.7 mm depth in a 3.0 mm product. The plating is split at the bottom of the deep slot creating two potentials. This particular slot is part of a test coupon, and therefore, has a connection on every layer. This would not be representative of a typical design.

If we use the VeCS for an internal layer transition (no connection at the top layer) we micro-machine the vertical trace away in the same process step as we do the cross route. Building on part one of this series where I introduced the VeCS slot, I will introduce some additional features under the topic of micro-machining.

Power VeCS

Electronics design applications constantly need more power and current, which opposes the need to make the features smaller, increasing resistance. These opposing constraints still apply to VeCS. With Power-VeCS, the vertical copper trace is shaped so that the cross section is larger, giving it a lower conductivity. Figure 3 shows the use of a half round cylinder extending from the side wall of the slot on the top layers (adding this construct on every layer compromises the routing channel).

We create the lower resistance connection by a combination of the vertical trace shapes with a stackup where Layer 2 (green) and Layer 3 (red) are a power/ground layer. In this manner, we create a lower resistance connection while keeping the connection to all ground and power in the same position. This prevents the

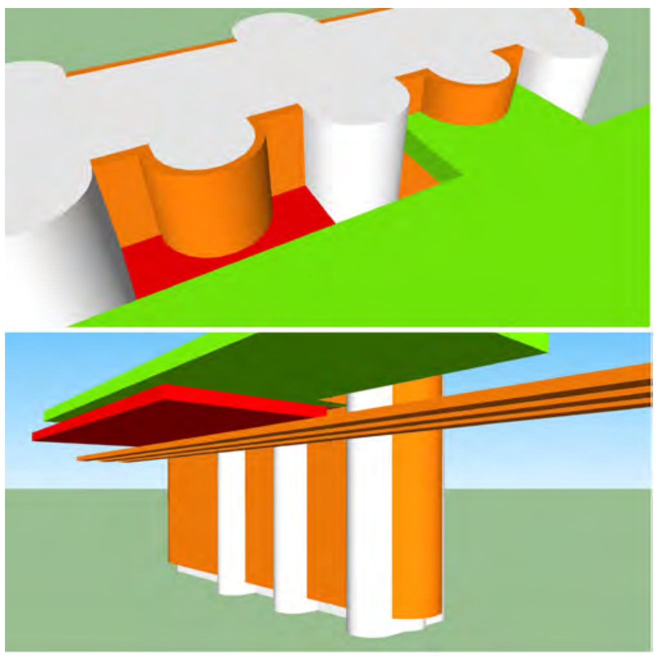


Figure 3: Micro-machined power-VeCS application to be applied to positions where lower resistance is required.

shifting of ground and power. And at the same time, we keep the CAF bridge in place.

Data Size

One difference between using micro-machining and the traditional PCB data sets can be the number of lines of machine-code/G-code required. For some designs, the amount of programming code can easily exceed the memory capacity of the current generation CNC machines. To reduce the number of lines of CNC code required, one could always write a specific machine code that defines a slot using a sequence of numbers for slot length and depth. Naturally, this makes the process more complex in that data files need to be cut up with correspondingly increased potential for error.

Micro-machining Experiences

Depth control is one of the challenges in setting up the VeCS-2 slots process. Dielectric tolerances are a critical parameter when setting the depth. Dielectric measurement across the panel needs to be performed to set the correct depth. The layer below the slot needs to have isolation thick enough to accommodate the tolerance of the Z-axis on the CNC machine. This tolerance needs to be in the region of ±0.02 mm. It should be noted also that the type of pressure foot as well as resetting the Z-axis counter through contact with the surface are important in achieving good depth tolerances.

Later in this series, I will introduce layer detection. This technique prevents what would otherwise be a complex, time-consuming, and somewhat inaccurate depth-setting process. Similar techniques will also be used for back drilling and depth-control drilling.

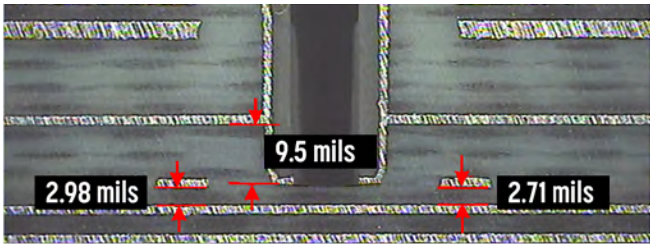


Figure 4: Critical dimensions at and around the bottom of the slot.

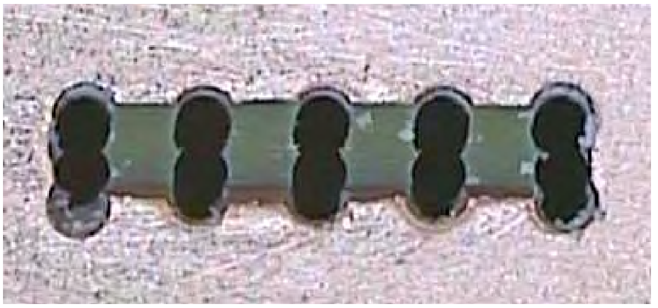


Figure 5: Cross route results using a standard bit.

Figure 6: Alternative bit from HPTec.

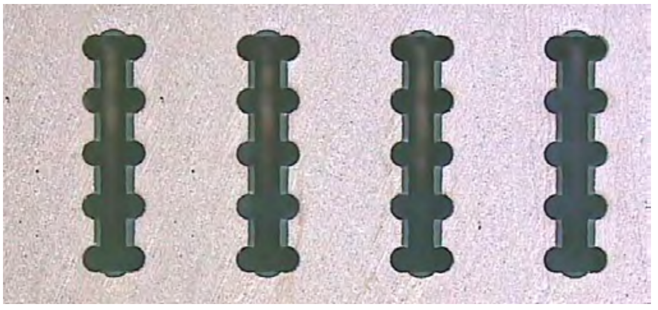


Figure 7: Clean cross routes using alternative bits and parameters.

The development of the techniques for cross-routing took some time. For example, forming the cross route initially had problems with bit wander (Figure 5). Note that a prerequisite to the routing process is to fill the slot with traditional via filling materials. This embeds the vertical trace and keeps it protected from the routing process.

With the assistance of HPTec, we addressed the bit wander by switching to an alternative bit (Figure 6). We saw a major improvement using these alternative bits, and after adjusting the parameters, we achieved straight and well-positioned cross routes (Figures 7-9) with little to no burring. Additionally, we achieved vertical trace widths of 0.1 mm.

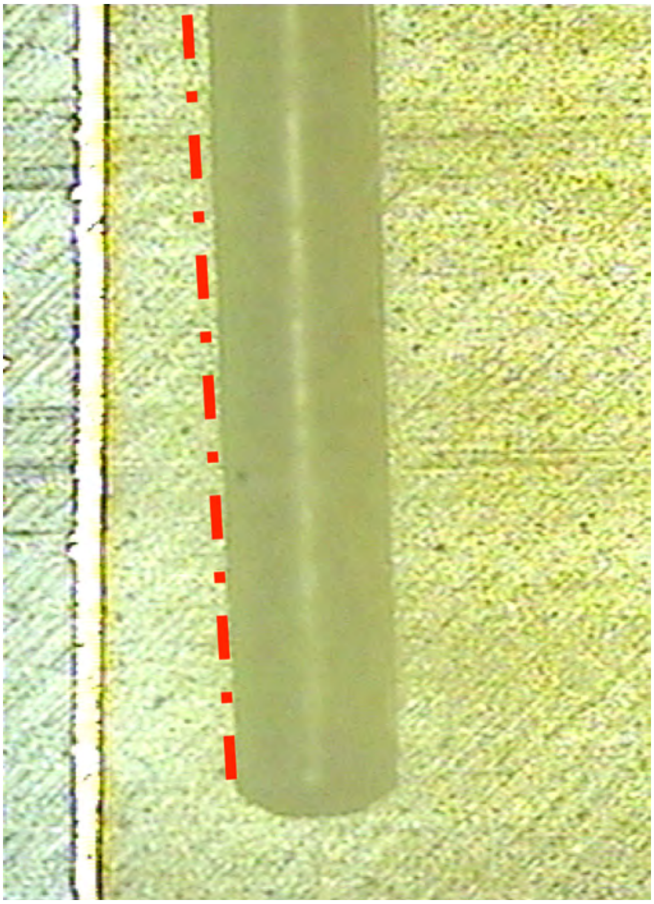


Figure 8: Typical drill bit; slot wandered on this particular drill hole.

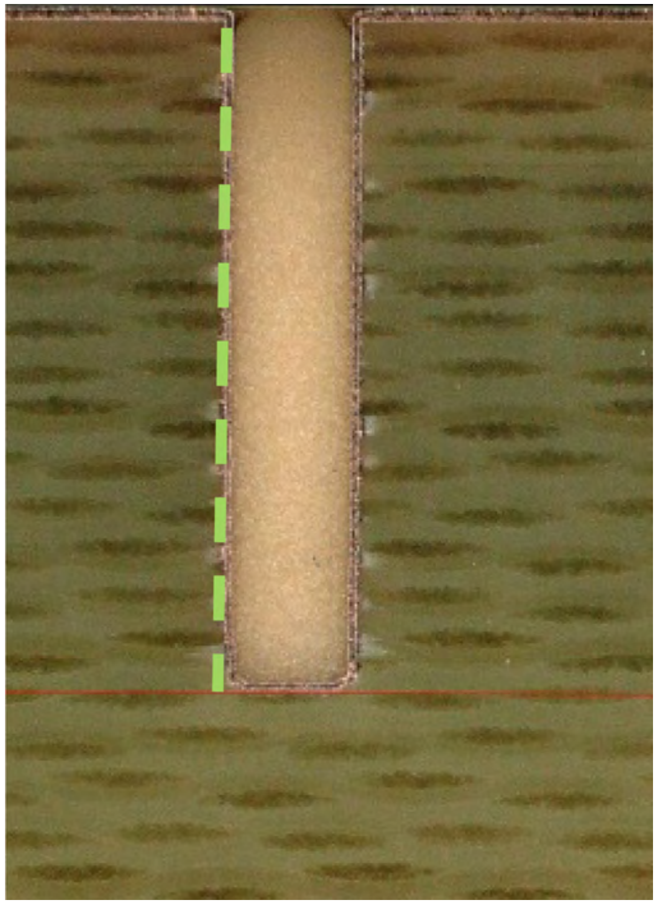


Figure 9: Alternative bit created straight slot a medium to high depths (2.8 mm).

For micro-machining, a proper process setup is spindle stability and drilling from drill bit selection to RPM, so there's one more item in setup to discuss, route planning. So far in this article, all of our examples use 0.5-mm slots. Making smaller slots with smaller bits is not a problem. Router bits with ball tips of 0.02 mm are used in the metal industry and have been for many years.

The strength in these small bits is that you do not put pressure on the side of the bit but only on the tip in line with the direction of the shaft. The bit is much stronger when a constant pressure/load is applied on the tip (axial) compared to applying only a radial load. Contact your tool bit supplier for help selecting the correct bit and setting the right parameters.

Measurement and Inspection

In addition to micro-machining, it is important to check the dimensions of the structure.

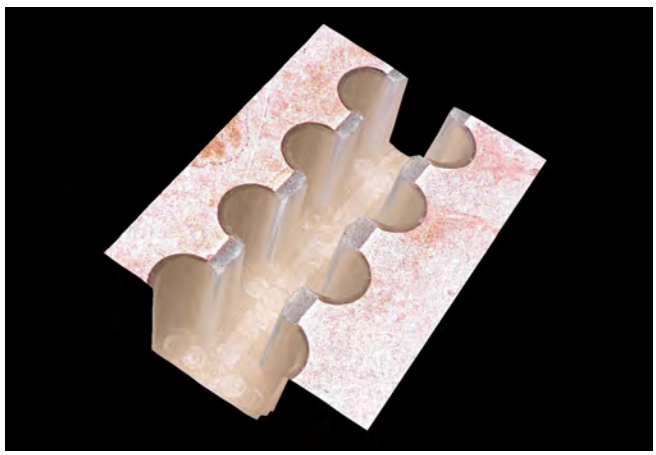


Figure 10: Laser profiling is highly accurate; even with the scoring lines, the bit created at the bottom of the slot is visible.

Figures 10–12 were generated using a laser profiler. The data from the laser profiler is processed, and sections from different planes can be made for analysis. This is not only faster

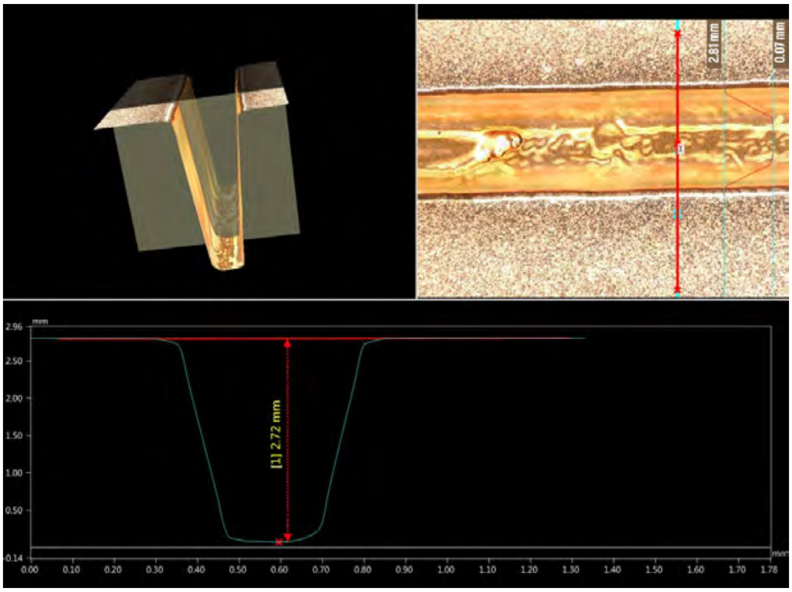


Figure 11: Measurements can be taken on the scanned profile in any direction, and the data is rendered in a 3D model (this image was taken after plating and before cross route).

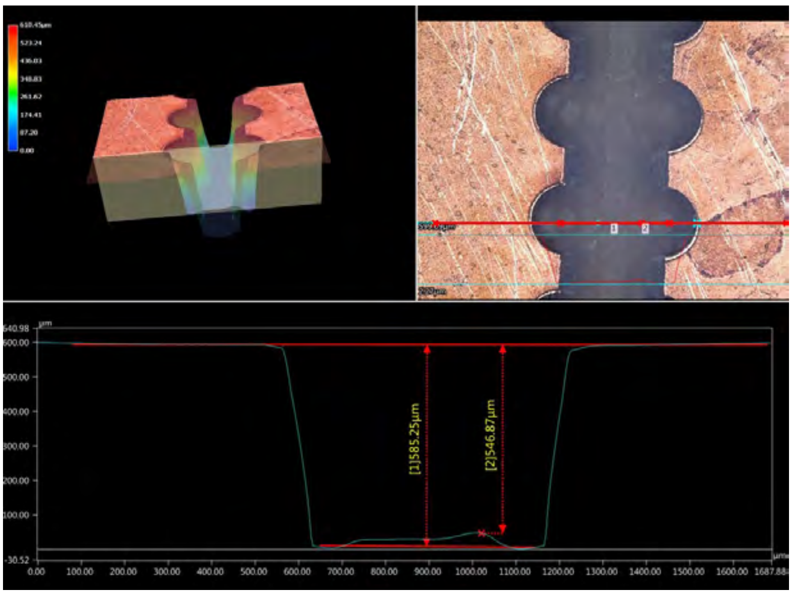


Figure 12: After cross route, we can check the flatness of the bottom surface. Any anomaly can be picked up, and debris from the process will be registered as well.

than cutting microsections or using a scanning electron microscope (SEM), but also nondestructive. The laser profiler can be applied to a panel without cutting any holes into it. While laser-profiling may not give you details, such as plating thickness, it is still a very effective tool for checking slot widths, depth, roughness, etc.

Micro-machining offers a lot of opportunities. As stated at the beginning of this series, we limited ourselves to using only the equipment currently available in the industry to develop VeCS technology. When new equipment allows us to step beyond this limit, we will be able to create structures that look very different from what we know today—holes and slots that are curved or angled, for example. For now, though, we limit ourselves to the 2D type application in keeping with the processes available today.

Acknowledgments

NextGIn wants to thank WUS PCB China for performing the work in fabricating the sample and making the cross section results available. WUS has been a VeCS development partner over the last few years, demonstrating the capabilities of this new approach. NextGIn also wants to thank HPTec for supporting the development work in developing and supplying special router bits as well as supporting the WUS PCB team.

I also want to thank HDP User Group International for allowing use of the cross section pictures in this article. HDP is running a test program that evaluates VeCS technology.

About NextGIn Technology

NextGIn Technology is a fabless company that develops and engineers solutions for the interconnect industry. It works with designers and fabricators in solving industry problems and will sell or license the technology to the industry. **PCB007**

Joan Tourné is CEO of NextGIn Technology BV.

Editor Picks from PCB007

1 EPTE Newsletter: Global Electronics Industry Continues to Decline ▶

Sales from consumer electronics are expected to slip this year, continuing a decline that began in December 2018. The Taiwanese PCB industry was first to signal stormy days ahead, and data from the global semiconductor industry for the same month backed up this gloomy forecast.

2 Trouble in Your Tank: OSP Performance—Effect of Film Thickness and Microetch ▶


Michael Carano

Two often overlooked performance attributes for organic solderability preservatives (OSPs) are the organic film thickness and the topography of the copper after microetch. Film thickness up to an extent is critical. However, the copper topography and surface preparation also play a role. Thus, you should not overlook the critical nature of the overall OSP film thickness. Read on.

3 Super PCB's Jessica Zhang on LEDs and Other Trending Business Areas ▶


Jessica Zhang

In an interview with I-Connect007 at the recent West Penn SMTA Expo, Super PCB Program Manager Jessica Zhang provides an overview of the company and shares new business trends they're seeing, including LEDs, wearable devices, and more.

4 Creating Smart Surfaces with Electronic Functionality ▶


Pete Starkey

Of all of the technical user presentations I attended at the AltiumLive design summit in Munich, the one I found most fascinating introduced an innovative technology that encouraged a bit of lateral thinking and appealed to my creative side: the IMSE, or injection-moulded structural electronics.

5 Flex Talk: Old-fashioned Networking ▶

We live in a connected world. Information is collected at an astonishing rate. But I sometimes wonder what is going to happen to the good, "old-fashioned" networking. Not networked devices, but the act of going out and meeting people in our industry, learning about their story and expertise, and sharing yours—mutually beneficial sharing of information and resources.

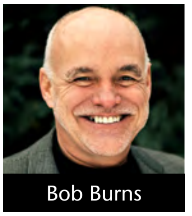
6 IPC Study: How PCB Makers Meet Technology Demands ▶

PCB Technology Trends 2018, a new global study published by IPC, is now available. The survey-based study shows how printed circuit board (PCB) manufacturers are meeting today's technology demands and looks at the changes expected by 2023 that will affect the whole industry.

7 It's Only Common Sense: Take All the Help You Can Get ▶

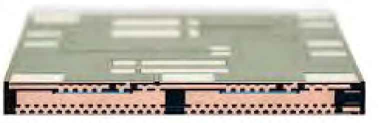
The best way to become great at anything is to learn everything you can from anywhere that you can. I have been fortunate enough to have had a number of mentors in my career—people who took the time to teach me, foster me, and help me move forward.

8 Flex Time: Alternative Constructions in Rigid-flex Designs ▶



In his last column, Bob Burns discussed how manufacturers of rigid-flex boards use techniques similar to those used by manufacturers of hard boards and flexible circuits, and how techniques vary. That column's discussion was for a standard, straightforward rigid-flex design. This column will talk more about non-standard designs, which can present process difficulties and require extra care for effective yields.

9 Continental Leverages Schweizer, Infineon Tech for 48V Systems ▶



Schweizer Electronic AG and Infineon Technologies AG have developed a new technology for the mild-hybridization of cars: chip embedding for Power MOSFETs.

10 Substrate-like PCB Demand Looks Promising ▶

With more smartphone vendors looking to adopt substrate-like PCBs in their high-end models, and more other mobile devices including notebooks and tablets set to incorporate SLPs, SLP demand is expected to be bullish.

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Insulectro, the largest national distributor of printed circuit board materials, is seeking a talented sales superstar for a Technical Account Manager role based out of either our Chicago or Minneapolis office. This role will focus on maintaining the existing customer base and developing new business within the assigned territory in both the printed circuit board and printed electronics industries. We are looking for the perfect fit of education, experience, and attitude that matches our company culture and enhances the service level to our customers.

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APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

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- Coordinate travel arrangements to realize significant transportation savings
- Respond to and write email messages
- Write monthly reports
- Prepare agendas for customers, detailing goals and objectives
- Must comply with all OSHA and company workplace safety requirements at all times

OTHER DUTIES:
- Other duties as assigned from time to time

REQUIRED EDUCATION/EXPERIENCE:
- College degree preferred with solid knowledge of chemistry
- 10 years of technical work experience in the printed circuit board (PCB) industry
- Computer knowledge
- Good interpersonal relationship skills

WORKING CONDITIONS:
- Occasional weekend or overtime work

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Career Opportunities

Career Opportunities

Career Opportunities

Career Opportunities

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Kindly note only shortlisted candidates will be notified.

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- Florida
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- Washington
- Los Angeles

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Contact Mike Fariba for more information.

mfariba@uscircuit.com

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GOOD FOR THE INDUSTRY

Events Calendar

IPC SummerCom ▶
June 15–20, 2019
Raleigh, North Carolina, USA

2019 FLEX Korea ▶
June 19–20, 2019
Seoul, South Korea

NEPCON Thailand 2019 ▶
June 19–22, 2019
Bangkok, Thailand

eSMART Factory Conference ▶
June 20–21, 2019
Dearborn, Michigan, USA

PCB Pavilion @ LCD EXPO Thailand ▶
June 27–29, 2019
Bangkok, Thailand

NEPCON South China 2019 ▶
August 28–30, 2019
Shenzhen, China

C3Bio Conference on Biosensors, Bioelectronics and Biodevices ▶
September 9–10, 2019
Bath, United Kingdom

C3Bio Training Workshop on Lab-on-Chip ▶
September 11–12, 2019
Bath, United Kingdom

EIPC PCB Pavilion @ WNIE Exhibition ▶
September 18–19, 2019
Warwickshire, UK

Additional Event Calendars

Coming Soon to *PCB007 Magazine:*

JULY: Failure & Reliability
The pressure to improve failure and reliability performance is increasing. We look at the latest developments in reliability improvement for PCB fabrication.

AUGUST: Wet Processes
Wet processes are the core of printed circuit fabrication. What's new? Are there new offerings down the road to make your wet process capabilities sharper? Faster? Greener? Easier to operate? Find out in this issue.

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