THE pcb design MAGAZINE

AN I-CONNECT007 PUBLICATION

August 2014

MATERIALS

Material Selection for Digital Design

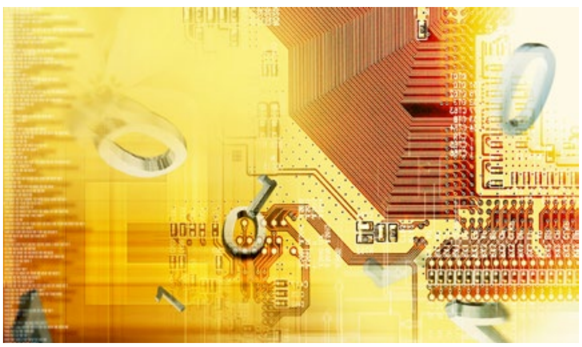
by Barry Olney, page 12

THE PCB DESIGN MAGAZINE™
August 2014

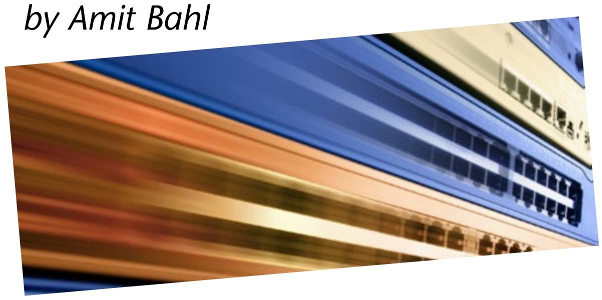
This Issue: MATERIALS

FEATURED CONTENT

The universe of PCB materials continues to expand: FR-4, low Dk, polyimide, halogen-free, phenolic cured, thermally conductive metal substrates…the list goes on, and evolves constantly. This month, we look at the effect of various PCB laminates on the PCB design process, with articles from expert contributors Barry Olney, Martin Cotton, John Andresakis, Amit Bahl, and John Coonrod.



FEATURE COLUMNS



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CONTENTS

Goodbye, Dieter

by Andy Shaughnessy
I-CONNECT007

A lot of people love their jobs; I do, and I bet you feel the same way. But Dieter Bergman was different. He devoted most of his adult life to IPC, and to PCB design. His heart belonged to Bannockburn.

Many of you knew Dieter, or knew of him and his history, so I don't need to rehash his biography. He was in on the ground floor of the modern PCB and EDA industries, and he helped shape IPC into what it is today. All of this made him a rock star among PCB designers. Designers always wanted a piece of Dieter, and he did his best to accommodate them.

I didn't know Dieter that well, but I always enjoyed talking to him, and, more importantly, listening to him. It was a good idea to pay attention when Dieter was speaking; you could learn quite a bit from his stories. And what a storyteller he was.

And he told some of the funniest jokes, both clean and dirty, that I've ever heard. He was a child when his family moved from Europe to Philadelphia in the 1930s, and his first words of English were curse words. He loved to tell the story about a store owner who paid him to stop cussing in front of her store. The more he swore, the more money he made.

I first met Dieter at a trade show when I started covering the industry in the 1990s. I mentioned that I was still learning about the technology. He laughed and said, "So am I!" He was so down-to-earth about himself, and barely impressed with his dozens of awards and industry accolades. I think he found the "living legend" badge mildly amusing.

No, Dieter was usually much more interested in talking about an upcoming DFM presentation. He enjoyed working with PCB designers, identifying their challenges, and helping them stay ahead of the game. That's what really animated him.

I last interviewed Dieter a few years ago on the last day of IPC APEX EXPO. We were supposed to talk after his Design Forum keynote speech on the morning of the first day of the show. Unfortunately for me, he was surrounded by designers after his presentation and entertained questions until he was late for his next meeting, so he took off at a trot.

I finally found Dieter on the last day of the show, rolling his bag down the hall, trying to get to the airport. I tried to catch up to him, walking, then power-walking, but to no avail. He may have been 30 years older than me, but Dieter was pulling ahead! After a week at a trade show, I was exhausted, but Dieter seemed

Dieter Bergman with Bob Neves at the 2011 IPC Midwest Show.

GOODBYE, DIETER *continues*

energized. He was walking faster and faster, as if he had eyes in the back of his head, and he really didn't want to be interviewed. I finally ran and caught him, and then, of course, he did a great interview.

It's hard to believe Dieter's gone now, because he seemed to defy the laws of aging. He shook your hand like he was 50 years younger. He was always quick-witted, always on the ball, and very sharp, even after a week at a trade show.

Dieter moved fast because he always had somewhere to go. One year, I saw Dieter at APEX, and a few weeks later I ran into him at a conference in Quebec. He was everywhere. Who wants to travel that much? He even joked about how he might keel over in an airport one day.

I see this a lot in the PCB community, especially in the design world. People just keep on working well after they reach 65. Some things just get into your blood and become part of your DNA.

The design world needs more people like Dieter, people who are willing to devote their lives to PCB design, and to IPC. We'll miss him. **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 15 years. He can be reached by clicking here.

The Passing of an Industry Icon: Dieter Bergman

It is with great sadness that IPC announces the passing of Dieter Bergman, IPC staff member for more than 40 years.

Decorated with countless awards over his lifetime, Bergman's name will forever be synonymous with IPC, and he leaves a legacy of friendships, lasting memories, and what is affectionately treasured by IPC staff and close friends as "Dieter-isms," such as a 45-minute answer to a 10-second question.

Bergman began his career in 1956 as a designer for Philco Ford in Philadelphia, Pennsylvania. He assumed the position of supervisor of the printed circuit design group in 1967, and joined the company's advanced technology group where he specialized in printed circuit computer-aided design. Before that, however, 1962, he became Philco's official representative to IPC and received the IPC President's Award in 1968, the same year he assumed chairmanship of the IPC Design Committee.

Bergman was elected Chairman of the IPC Technical Activities Executive Committee in 1974, and later that year joined the IPC staff as Technical Director. In that role, he was responsible for a number of things: the coordination of standards, specifications and guidelines development; round robin test programs; establishment of workshops and seminars; government and inter-society liaison; and initiating IPC activities in Europe and Asia.

In 1984, Dieter became Director of Technology Transfer to help foster the interchange between design and manufacturing and he continued to serve as a leader in the identification of future technologies and industry needs.

While Bergman had a special place in his heart for the design community, his contributions to the industry as a whole earned him IPC's highest honor, the Hall of Fame Award, in 1985.

Most recently, Bergman chaired the IPC Ambassador Council, a group of IPC Hall of Famers who provide advice and guidance to IPC, and encourage active participation in IPC activities by all of its members to enhance the electronics industry.

"The staff and I feel very fortunate to have known Dieter, and have benefited from his knowledge and his passion for the industry," said IPC President and CEO John Mitchell. "He will be missed, but always remembered as an icon, pioneer and friend."

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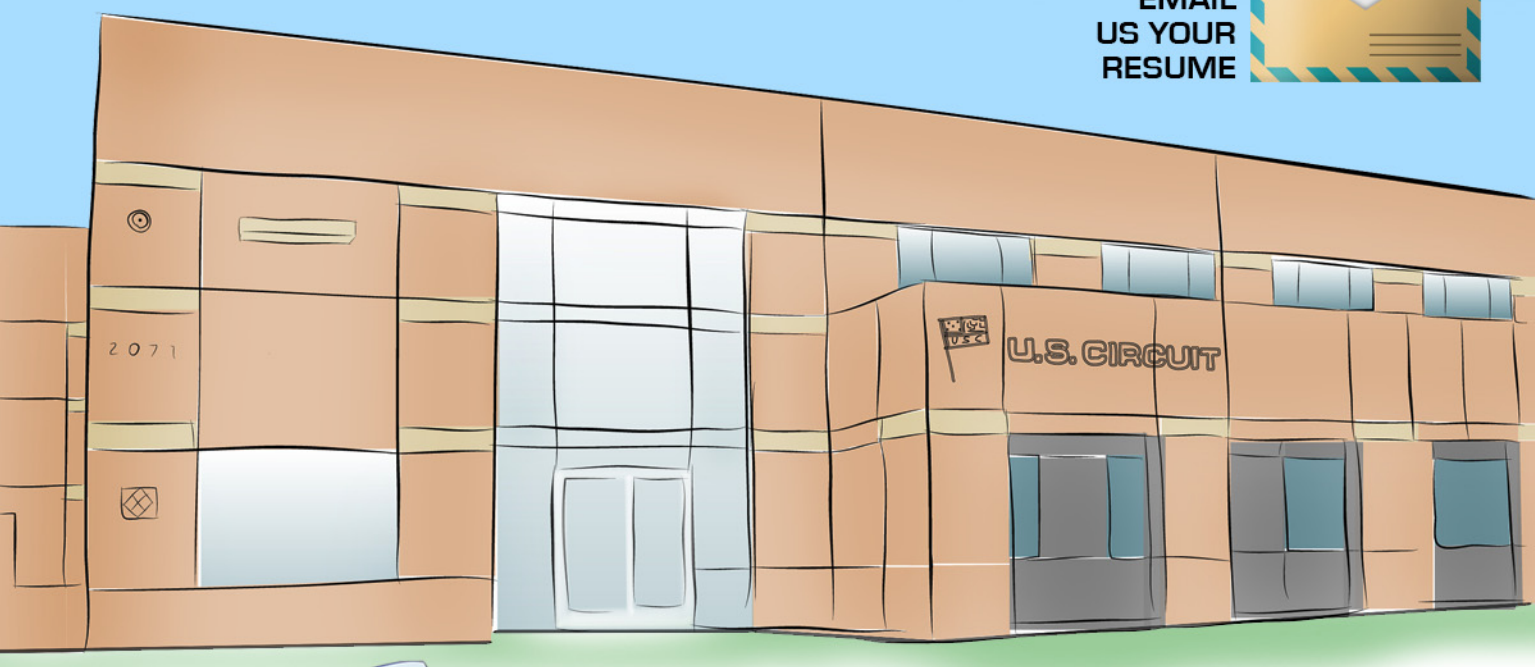

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Material Selection for Digital Design

by Barry Olney
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In a previous column, Material Selection for SERDES Design, I pointed out that materials used for the fabrication of the multilayer PCB absorb high frequencies and reduce edge rates and that loss, in the transmission lines, is a major cause of signal integrity issues. But we are not all designing cutting-edge boards, and sometimes we tend to over-specify requirements that can lead to inflated production costs.

In this column, I will look at what types of materials are commonly used for digital design, and how to select an adequate material to minimize costs. Of course, selecting the best possible material will not hurt, but it may blow out the costs.

Signals propagate in a vacuum or air at approximately the speed of light. But, as the electromagnetic energy is enveloped in a dielectric material, sandwiched between planes in the PCB medium, it slows down. Figure 1 illustrates a signal propagating through a curved waveguide. This is representative of a typical stripline configuration of a PCB. What needs to be understood is that the signal traces on a PCB simply guide the signal wave, as the electromagnetic energy propagates in the surrounding

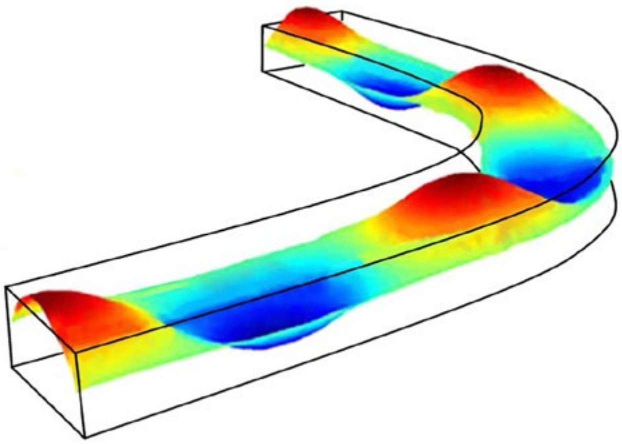


Figure 1: Simulated signal propagating through a curved waveguide[2].

dielectric material. It is the dielectric material that determines the velocity (v) of propagation of the electromagnetic energy:

$$v = \frac{c}{\sqrt{Er}} \quad \text{Equation 1}$$

Keep in mind that c is the speed of light (in free space) and Er is the dielectric constant of the material (FR-4 is ~4.0). By contrast, the Er of air is 1. Therefore, the velocity of propagation in FR-4 is about half the speed of light or 6 inches per ns. The important concept is that it is the electromagnetic energy that propagates down the transmission line—not electron flow. Electrons flow at about 0.4 inches per second, a snail's pace by comparison.

The electrical properties of a dielectric material can be described by two terms:

1. The dielectric constant or relative permittivity (Er or Dk) is the ratio of the amount of electrical energy stored in a material by an applied voltage. It describes how the material increases the capacitance and decreases the speed in the material.
2. The dielectric loss or dissipation factor/loss tangent (Df) is a parameter of a dielectric material that quantifies its inherent dissipation of electromagnetic energy.

Dielectric constant and dielectric loss are not a function of the geometry of the transmission line—they are a function of the dielectric material in which the signal propagates, their distribution in the PCB stackup, and the applied frequency. These mechanisms contribute to the frequency dependent loss and to degrade the speed of the signal. The signal quality transmitted through the medium, and picked up at the receiver, will be affected by any impedance discontinuities and by the losses of the dielectric materials. The glass epoxy material (FR-4) commonly used for PCBs has negligible loss for digital applications below 1 GHz. But, at higher frequencies the loss is of greater concern.

So if you have a fast rise/fall time, high frequency signal, then the wave needs to propagate at higher speed and therefore the Er needs to be low to enable this. If a material with a high dielectric constant is placed in an electric field, the magnitude of that field will be measurably reduced within the volume of the dielectric. Therefore, a lower Er is desirable for high-speed design.

It is best to use the value of the dielectric constant applicable at the highest frequency of interest. For digital signals, the highest frequency of interest (f) depends on the rise/fall time (Tr) and is approximated by:

$$f = \frac{0.5}{Tr} \quad \text{Equation 2}$$

Therefore, for a 1-ns rise time signal, the frequency of interest will be 500MHz. But then, the maximum bandwidth also needs to consider the 3rd or 5th harmonic of the fundamental—1.5 GHz to 2.5 GHz—in this case. The bandwidth is an indication of the highest data rate that can be transmitted by an interconnect. So for a 1 ns rise time signal, we should look at about a 2 GHz material.

Also of importance is the glass transition temperature (T_g), which is the point at which a glassy solid changes to an amorphous resin/epoxy. If the reflow temperature exceeds the T_g for an extended period, the material rapidly expands in the Z-axis. Plus, mechanical material properties degrade rapidly—strength and bonds in the material. A high T_g guards against barrel cracking and pad fracture during reflow. Standard FR-4 has a T_g of 135–170°C, whereas the high-speed materials are generally over 200°C.

There a basically two types of dielectric material:

1. Woven fiberglass reinforced dielectric
2. Fiberglass free dielectric

At high frequencies, a non-uniform dielectric in the substrate can cause skew in differential signals. The inconsistency of the dielectric material comes from the fact that the fiberglass and the epoxy resin, that make up typical PCB core (laminate) and prepreg materials, have a different dielectric constant. And because the fabricator cannot guarantee the placement of the fiberglass with respect to the location of the traces, this results is uncontrolled differential skew. A fiberglass-free material can be used to eliminate differential skew. However, fiberglass-free materials come at a price. So for a cost-effective solution, let's eliminate the fiberglass-free dielectric.

Close attention should also be paid to the skew associated with the fiber weave effect. For high-speed data rates of 5 Gbps and above, this skew significantly cuts into the available jitter unit interval (UI) budget and leads to a reduction in the observed eye width at the receiver. If the flexibility exists, specify a denser weave material (2113, 2116, 1652 or 7628) compared to a sparse weave (106 and 1080). Figure 2 compares the different types of fiberglass weaves to a 4/4 mil differential pair. Notice that one side of the pair can be routed over the fiberglass and the other over the gap (resin), depending on the placement. The different dielectric constants create skew. However, routing the differential signals diagonally across the weave can reduce this skew considerably.

Typically, when the impedance of a substrate it first calculated, "virtual materials" are used as the basis. In other words, we choose a round number to represent the dielectric constant, dielectric thickness, and the attributes of the trace thickness and width to establish a solution. However, these are not the attributes, of the actual materials, used by the fab shop to manufacture the board and are inherently inaccurate. I'm not saying that the use of virtual materials should be avoided but rather, the numbers need to be in the ball park to begin with.

In order to select the correct dielectric materials and variables for your substrate, you need to consider the following:

1. Dielectric loss needs to be low.
2. Dielectric constant needs to be low.
3. Glass transition temperature needs to be high (= >180°C).
4. Dielectric thickness needs to be low.

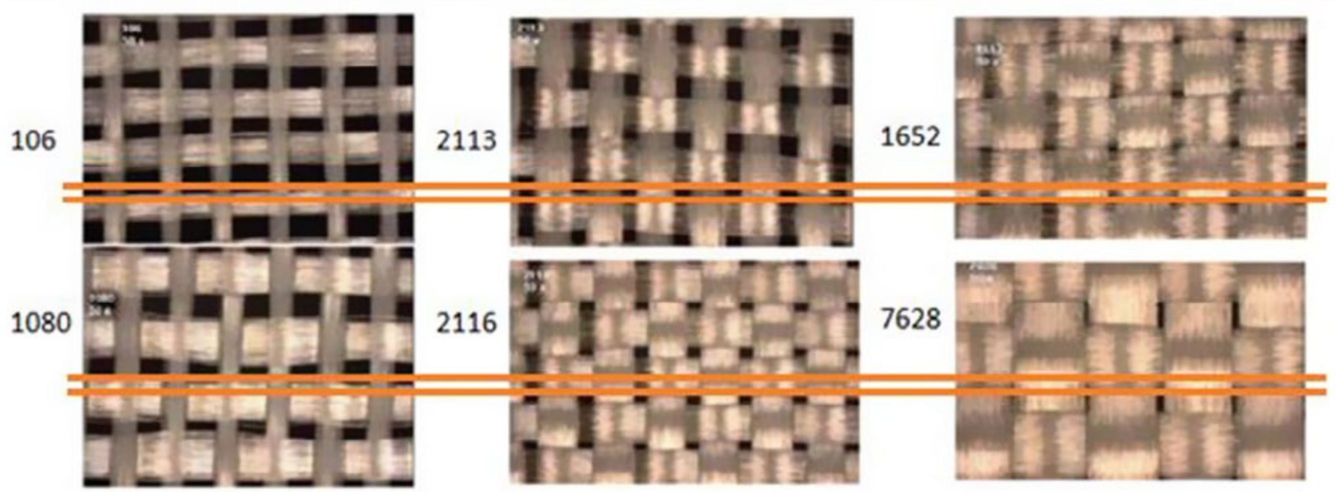


Figure 2: Different types of fiberglass weaves compared to a differential pair. (Source: Altera)

5. Trace thickness, width and separation need to be above the manufacturable limits. Trace width/clearance should not go below 4/4 mils to minimize costs.
6. And most important of all, the price needs to be low.

All of the above need to be considered, to establish the right material without over-design.

Once the ball park, virtual material numbers are established, the material needs to be selected for 2 GHz operation. This I suggest you do in consultation with your preferred fab shop, as choosing the materials that they stock will result in up to 5% better accuracy. Obviously, what you select is based on what is available at a reasonable price. (The ICD Stackup Planner features 8,800 materials up to 40 GHz to choose from.) Boolean searches can be done in order to reduce the select list as Illustrated in Figure 4. Look for a 2 GHz material with Er<4, Df<0.02 and Tg = >180C. In Figure 5, I have chosen ITEQ IT-180A which fits the specs.

Prepreg materials are only available up to 8–9 mil thick, so in order to attain the desired thickness, multiple prepregs must be stacked together to give the required 10 mils. In this case, I have used 2 x 2.8 plus a 4.6 giving 10.2 mils total. Make sure these are symmetrical, about in the center, otherwise there will be a slight offset in impedance due to the field solver seeing an imbalance in dielectric constant.

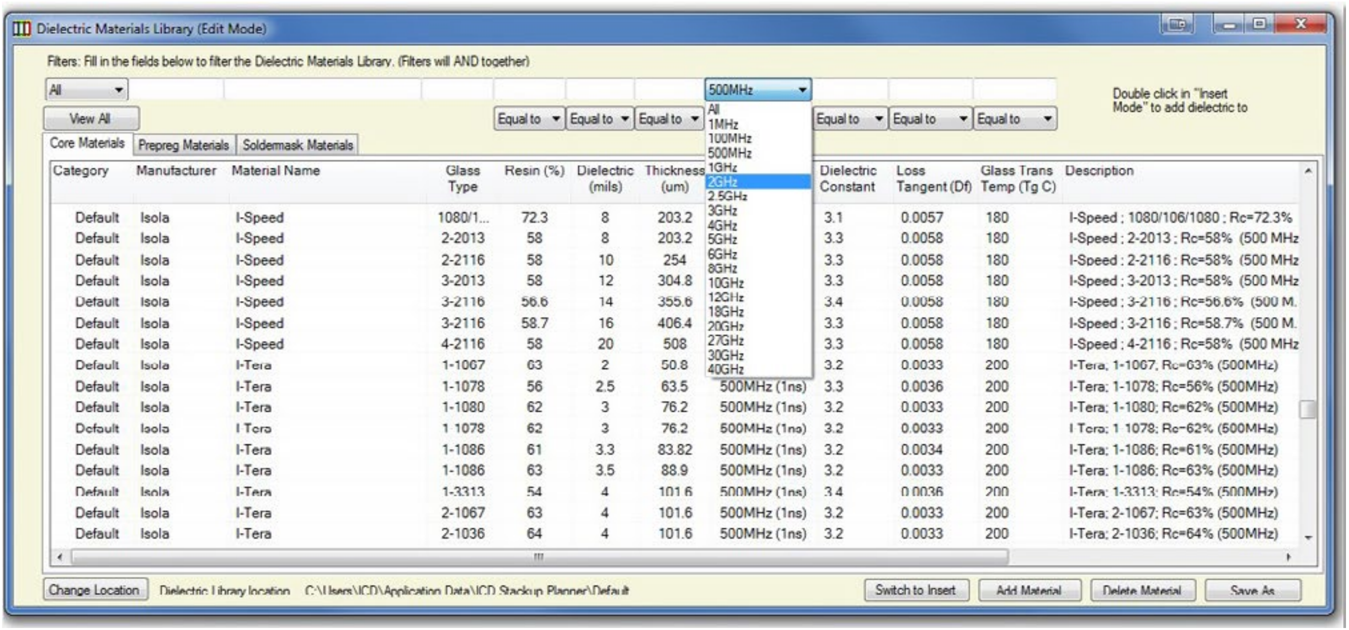
In conclusion, selecting an adequate material for the project will minimize the cost. The

UNITS: mil   7/3/2014   Total Board Thickness: 62 mil

Differential Pairs > 50/100 ohms | USB 90 ohms

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
1	8	Plane	GND	Conductive			1.4						
		Core		Dielectric	3.9	4							
2		Signal	Inner 3	Conductive			1.4	10	4	0.31	54.05	99.19	86.89
		Prepreg		Dielectric	3.9	10							
3		Signal	Inner 4	Conductive			1.4	10	4	0.31	54.05	99.19	86.89
		Core		Dielectric	3.9	4							
4		Plane	VDD	Conductive			1.4						

Figure 3: Stripline configuration using "virtual materials."



Category	Manufacturer	Material Name	Glass Type	Resin (%)	Dielectric (mils)	Thickness (um)		Dielectric Constant	Loss Tangent (Df)	Glass Trans Temp (Tg C)	Description
Default	Isola	I-Speed	1080/1...	72.3	8	203.2		3.1	0.0057	180	I-Speed ; 1080/106/1080 ; Rc=72.3%
Default	Isola	I-Speed	2-2013	58	8	203.2		3.3	0.0058	180	I-Speed ; 2-2013 ; Rc=58% (500 MHz
Default	Isola	I-Speed	2-2116	58	10	254		3.3	0.0058	180	I-Speed ; 2-2116 ; Rc=58% (500 MHz
Default	Isola	I-Speed	3-2013	58	12	304.8		3.3	0.0058	180	I-Speed ; 3-2013 ; Rc=58% (500 MHz
Default	Isola	I-Speed	3-2116	56.6	14	355.6		3.4	0.0058	180	I-Speed ; 3-2116 ; Rc=56.6% (500 M.
Default	Isola	I-Speed	3-2116	58.7	16	406.4		3.3	0.0058	180	I-Speed ; 3-2116 ; Rc=58.7% (500 M.
Default	Isola	I-Speed	4-2116	58	20	508		3.3	0.0058	180	I-Speed ; 4-2116 ; Rc=58% (500 MHz
Default	Isola	I-Tera	1-1067	63	2	50.8		3.2	0.0033	200	I-Tera; 1-1067; Rc=63% (500MHz)
Default	Isola	I-Tera	1-1078	56	2.5	63.5	500MHz (1ns)	3.3	0.0036	200	I-Tera; 1-1078; Rc=56% (500MHz)
Default	Isola	I-Tera	1-1080	62	3	76.2	500MHz (1ns)	3.2	0.0033	200	I-Tera; 1-1080; Rc=62% (500MHz)
Default	Isola	I-Tera	1-1078	62	3	76.2	500MHz (1ns)	3.2	0.0033	200	I-Tera; 1-1078; Rc=62% (500MHz)
Default	Isola	I-Tera	1-1086	61	3.3	83.82	500MHz (1ns)	3.2	0.0034	200	I-Tera; 1-1086; Rc=61% (500MHz)
Default	Isola	I-Tera	1-1086	63	3.5	88.9	500MHz (1ns)	3.2	0.0033	200	I-Tera; 1-1086; Rc=63% (500MHz)
Default	Isola	I-Tera	1-3313	54	4	101.6	500MHz (1ns)	3.4	0.0036	200	I-Tera; 1-3313; Rc=54% (500MHz)
Default	Isola	I-Tera	2-1067	63	4	101.6	500MHz (1ns)	3.2	0.0033	200	I-Tera; 2-1067; Rc=63% (500MHz)
Default	Isola	I-Tera	2-1036	64	4	101.6	500MHz (1ns)	3.2	0.0033	200	I-Tera; 2-1036; Rc=64% (500MHz)

Figure 4: Material selection in the ICD Stackup Planner Dielectric Materials Library.

MATERIAL SELECTION FOR DIGITAL DESIGN *continues*

UNITS: mil — 7/3/2014 — Total Board Thickness: 62 mil

Differential Pairs > 50/100 ohms | USB 90 ohms

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
1	8	Plane	GND	Conductive			1.4						
		Core		IT-180A, 1-2116, (2GHz)	3.8	4.0							
2		Signal	Inner 3	Conductive			1.4	10	4	0.31	54.45	99.73	87.82
		Prepreg		IT-180A; 106; Rc=62%; (2GHz)	3.9	2.8							
		Prepreg		IT-180A; 106; Rc=53%; (2GHz)	4	4.6							
		Prepreg		IT-180A; 106; Rc=62%; (2GHz)	3.9	2.8							
3		Signal	Inner 4	Conductive			1.4	10	4	0.31	54.45	99.73	87.82
		Core		IT-180A: 1-2116: (2GHz)	3.8	4.0							
4		Plane	VDD	Conductive			1.4						

Figure 5: Virtual materials substituted with ITEQ IT-180A material.

designer should calculate the highest frequency of interest, taking the bandwidth into account, then choose a dielectric material with the lowest Er (Dk) and Df with a Tg about 180°C. And remember, choosing the materials that are stocked by your fab shop will result in up to 5% better accuracy.

Points to Remember

• Selecting the best possible material will not hurt—but may blow out the costs.

• Signals propagating in the dielectric material of a PCB slow down.

• Signal traces on a PCB simply guide the signal wave, as the electromagnetic energy propagates in the surrounding dielectric material.

• The velocity of propagation in FR-4 is about half the speed of light or 6 inches per ns.

• Dielectric constant and dielectric loss are not a function of the geometry of the transmission line—they are a function of the dielectric material in which the signal propagates, their distribution in the PCB stackup and the applied frequency.

• A low Er is desirable for high-frequency design.

• It is best to use the value of dielectric constant applicable at the highest frequency of interest. However, the maximum bandwidth also needs to consider the 3rd or 5th harmonic of the fundamental.

• A high T_g guards against barrel cracking and pad fracture during reflow.

• A fiberglass-free material can be used to eliminate differential skew but is costly.

• In order to select the correct dielectric materials and variables for your substrate, you need to consider dielectric constant and loss, glass transition temperature, trace thickness, width and separation and of course cost.

• Choosing the materials that are stocked by your fab shop will result in up to 5% better accuracy.

• The ICD Stackup Planner features 8,800 materials up to 40GHz. **PCBDESIGN**

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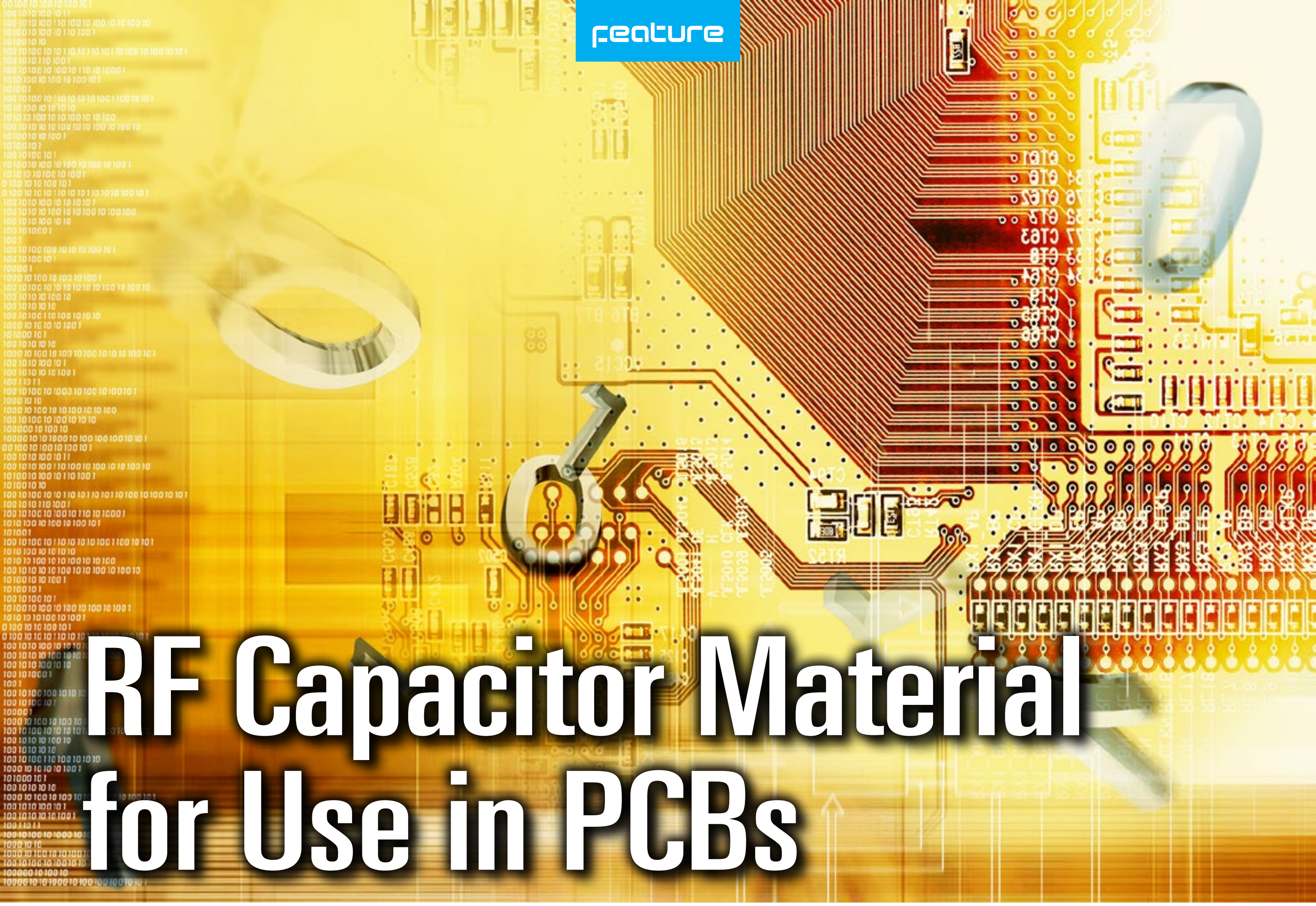
Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, click here.



RF Capacitor Material for Use in PCBs

by Jin-Hyun Hwang, John Andresakis, Ethan Feinberg, Bob Carter, Yuji Kageyama, and Fujio Kuwako
OAK-MITSUI TECHNOLOGIES

Abstract

A novel ceramic-functional-particle-filled polymer composite material has been developed for use in discrete elements on the PCB or embedded within the packaging substrate for high-frequency circuit applications. This material provides the desired properties such as low loss at high frequencies (about 0.002 or less up to 10GHz) and high dielectric strength, among other improved properties. The electrical properties were influenced significantly by the ceramic-functional-particle (type and particle size/distribution in the polymer matrix). Their contributions to the electric strength and temperature stability of capacitance (an important material issue for practical device application) will be discussed. In addition, capacitance tolerance for manufacturing an embedded RF capacitor will be presented in terms of etching uniformity to minimize the variation of the capacitor electrode areas.

I. Introduction

Organic-based dielectric materials have been explored for the use either in discrete passive components on the PCB or in being embedded within the packaging substrate as part of RF/microwave circuits[1–4]. Using ceramic-functional-particles (fillers), filled polymer composite material is merely a convenient and inexpensive way (to compete with ceramic chip capacitors) achieving low ESR (equivalent series resistance), high SRF (self-resonant frequency) for RF capacitor application that can support frequencies well above 1GHz. Besides, embedding fillers into the polymer enhances properties of dielectric materials (by optimizing filler chemistry and its distribution in the polymer matrix) such as temperature stability of capacitance for high-precision RF circuit and dielectric strength (the maximum DC electric field strength applied across the dielectrics in RF capacitor) for a high-

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voltage rating which is essential especially for servers, pico cell and femto cell in the base station market space. Generally, fillers are widely accepted in various applications because of their advantage in addressing several limitations of polymers, making its way onto benefits such as better dimensional stability for polymer composite membrane, lower coefficient of thermal expansion (CTE) for build-up layers, increasing thermal conductivity for thermal interface materials (TIM), and improved stiffness for underfill materials. As for the fillers in RF capacitor application, it is presently based almost entirely on the simple perovskite $BaTiO_3$ (barium titanate), but there is strong demand on the class of materials known as paraelectrics, mainly due to the fact that their dielectric properties are much more stable with regard to most operating conditions such as frequency, temperature and DC bias[5].

Well dispersed fillers in the polymer composite matrix play a crucial role in achieving RF capacitor requirements as described earlier, and thus factors that determine fillers distribution should be controlled and optimized. Any existence in the particle agglomerates is accompanied by the formation of possible defects such as trapped porosity that make the dielectrics vulnerable under practical operating conditions. Figure 1 shows a typical example of severe filler agglomerates clearly visible, concentrated on the coating surface as discrete protuberances and appearing to be in greater numbers. Filler agglomeration is easy to observe by improper usage of dispersion agents and their mismatching to a solvent composition in formulation. It could degrade electrical properties, in particular dielectric strength and temperature stability of capacitance (both will be described in next section). Various types of coupling agents can be added to the polymer compositing to take advantage of the absorption of a functional polymer to the particle surface to modify the filler/polymer interface chemistry, giving rise to complete de-agglomeration of the fillers and subsequent elimination of the air void[6]. It is also necessary to adjust the solvent composition combined with the coupling agents, which is associated with coupling, adhesion and dispersion. In this study, a titanium-based coupling agent and a typical solvent mixture were selected and formulated with a paraelectic filler and a phenylene-based polymer. The optimum amount of the coupling agent was determined by the viscosity response for various levels of the application of the coupling agent. The de-agglomeration effect was pronounced when significant reduction in suspension viscosity was observed. Optimal combination was formulated to make RF capacitor laminate that used thin dielectrics having thickness range of 12–25 µm.

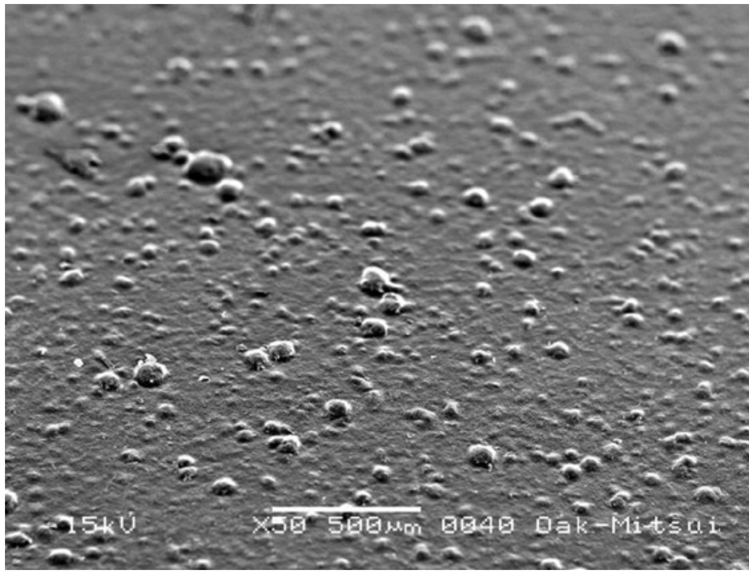

Figure 1: SEM image (at tilt angle) of the typical filler agglomerates of ceramic filled polymer composites (on the coating surface).

II. Results and Discussion

A. Effect of Ceramic Functional Particles (Fillers)

For practical device application, the contribution of the filler to the dielectric strength and the temperature stability of the capacitance are of greatest interest. The dielectric strength was examined by measuring dielectrics breakdown voltage (BDV) of the samples having fillers with different size (Figure 2). A circular pattern with 0.5 inch diameter was placed on a bottom electrode grounded to the DC tester. A probe was placed on the center of a circle and subjected to the voltage. The electrode material was made

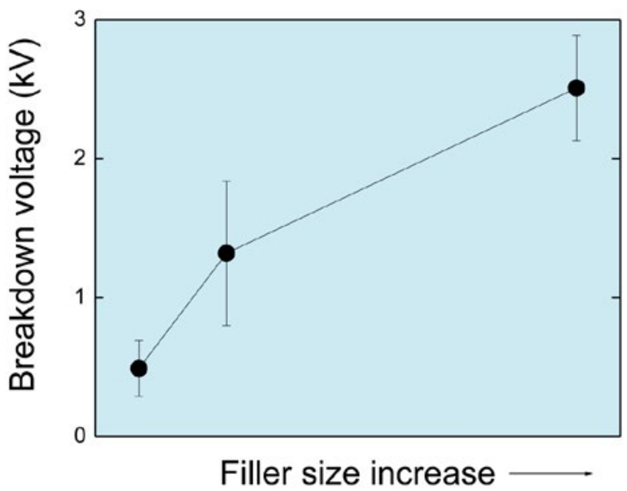

Figure 2: BDV variation of polymer compositing with the filler size.

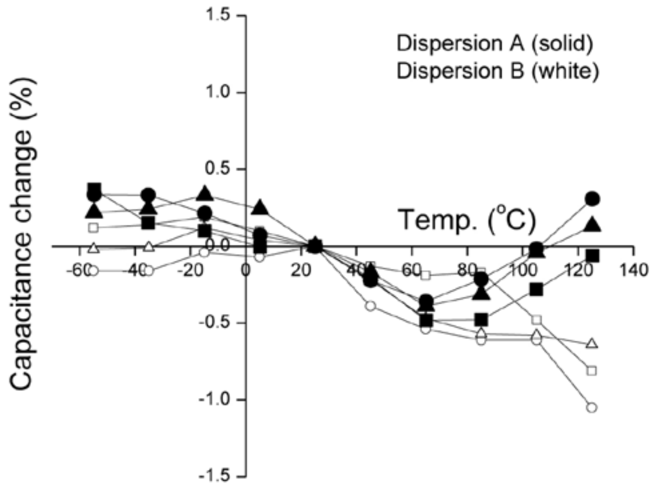

Figure 3: Temperature stability of capacitance of two samples prepared by different suspension preparation routes.

on one side of the copper of a RF capacitor laminate. The dielectric thickness was set to 25μm for all samples. As shown in Figure 2, the effect of the filler size on the BDV was clearly detectable, and the BDV of the dielectrics composed of the larger size filler revealed a considerable improvement in BDV compared to the case of formulating with the smaller size filler. Lower BDV may result from non-uniform dispersion of the filler and it may induce the charging of the weak interface chemistry, probably representing the filler agglomerates. We continue to work on improving the material to achieve relatively high BDV even with small size filler by controlling the suspension chemistry.

Indirect evidence for the improvement of the filler distribution was sought by measuring capacitance change with temperature for samples fabricated with different suspension preparation routes. Temperature coefficient of capacitance (TCC) is an important material parameter to meet the tighter RF/microwave design tolerances. (Details on TCC were described previously[7]) Figure 3 shows that the TCC was rotating counterclockwise (in the direction of the positive TCC) toward the end of each curve at high temperature region. We mixed fillers with the polymer in an arbitrary way. Thus, in this physical construction of the polymer compositing, the dielectric is comprised of filler and polymer with the filler occupying the majority of the dielectric. The filler selected ended up slight positive TCC and the plain polymer (without filler) showed negative TCC. The filler contribution to the net composite TCC is dependent on its volume fraction and distribution. Therefore, it is assumed that the filler can control complete TCC by compensating for negative TCC of the polymer and positive TCC at higher temperature could be regarded as being responsible for the uniform filler distribution in the polymer matrix. SEM photos in Figure 4 support this with different level of dispersion of the filler in polymer between two samples.

B. Characteristics of RF Capacitor Laminate

Figure 5 shows frequency stability of Dk (dielectric constant) and DF (dielectric loss) of our developed RF capacitor laminate product using the ceramic-particle-filled polymer composite. As for the method for checking Dk and DF, the first point in Figure 5 used the lower-frequency method (LCR meter) and the remaining three used the split post resonator cells, which are useful to measure Dk for isotropic mixtures (when

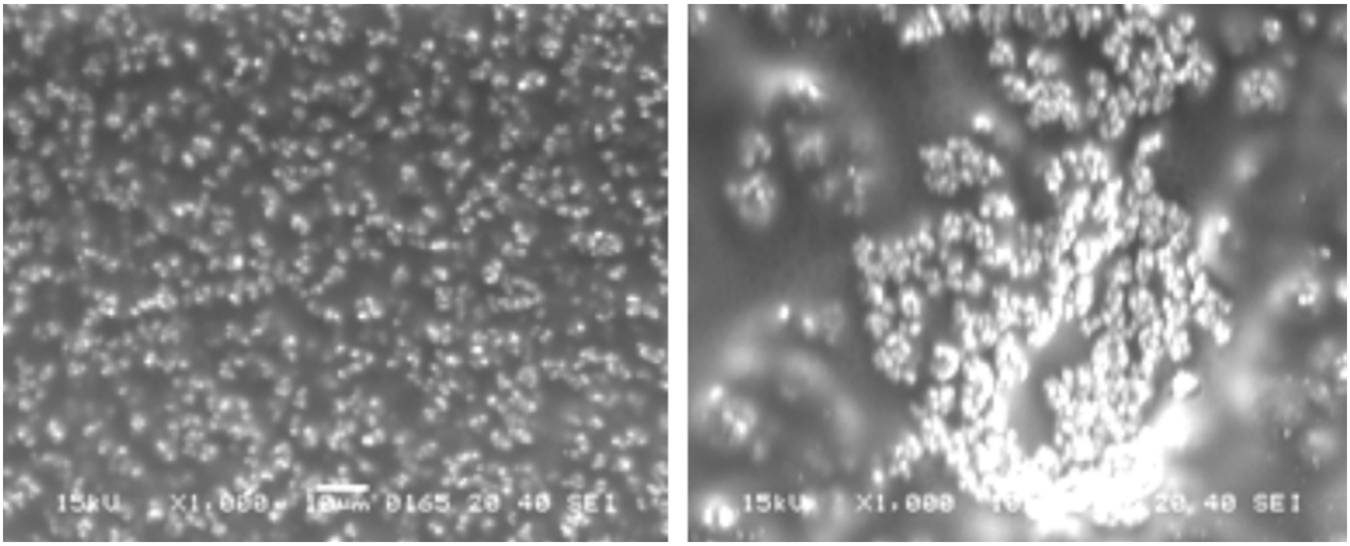

Figure 4: SEM images (on the coating surface) of samples with (a) dispersion condition A and (b) dispersion condition B.

fillers are randomly oriented)[8,9]. The product is the copper clad laminate (CCL) with a standard panel, 18 x 24 inches. It was composed of two sheets of copper foils on both ends with organic based composite dielectrics having fillers dispersed into polymer in between. Copper foils are available in various thicknesses, 0.5 ounce and 1 ounce being the dominant thickness, but thinner copper foil would help to minimize the variation in capacitance during etching process in PCB manufacturing. The typical Dk and DF of the RF capacitor laminate at 1GHz were measured, 7.8 and 0.0022, respectively. We are expanding the product's capacitance density range up to 670 pF/cm^2 thinning dielectrics and process optimization. The standard reliability tests including solder shock, solder float, time to delamination and THB (temperature, humidity and bias) testing were performed and all these tests passed.

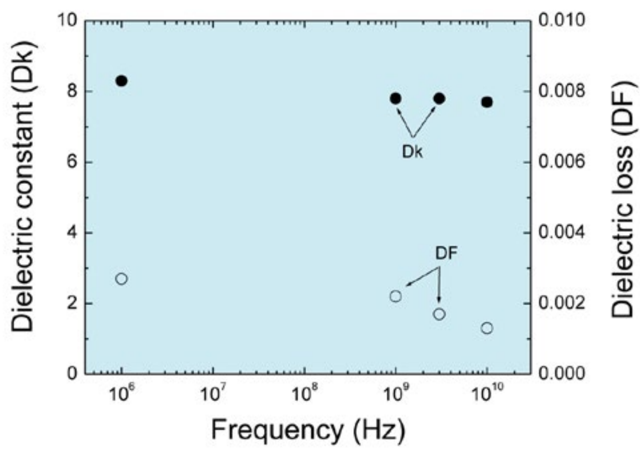

Figure 5: Frequency dependence of Dk and DF of the developed RF capacitor laminate.

C. Uniformity of Capacitance

Capacitance tolerance for the organic-based RF capacitor laminate is critical for the application of forming discrete type embedded capacitors inside the organic packaging substrate. In this case, capacitance tolerance can be expressed as 3 sigma in the form of (mean of capacitance) ± (3 sigma) for the footprint size of the capacitor. Smaller tolerance in capacitance is desirable to achieve better yield performance of the RF device in manufacturing[2]. However, when forming discrete embedded capacitors inside the organic substrate for RF module, the materials and processes don't currently allow for the tight tolerances due to the material and the process variation. The dispersion techniques for the ceramic fillers in polymer and the right

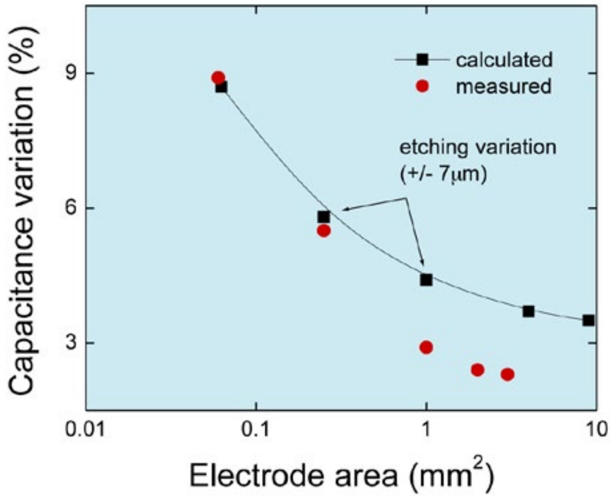

Figure 6: Capacitance variation with electrode area: calculation vs. measurement result.

coating method for putting the ceramic-filled polymer composite material on the copper can minimize the material variation. In addition to the material variation, the process variation (mainly etching variation) in formation of the electrodes by the etching process in PCB manufacturing will add to the tolerance. In order to understand the capacitance tolerance of the capacitor laminate, uniformity of capacitance was investigated as a function of various capacitor electrode areas (0.25 mm square ~ 3 mm square) which were prepared by the standard etching on the test board. Figure 6 is a typical result, showing the measured capacitance tolerance and calculated tolerance (expected) of capacitance. Actual measured uniformity of capacitance in the smaller footprint of the capacitor showed a good correlation with an assumption that the etching variation is around ±7µm. Small footprint capacitors with tight tolerance are still being challenged, but the result in Figure 5 indicate that we can still achieve fairly uniform capacitance values with proper process optimization and control that will result in functional RF circuits.

III. Conclusion

The ceramic filled organic-based composite material has been used to make RF capacitor laminates (to compete with ceramic chip capacitors). Using this material, we successfully achieved low DF of ~0.002 at GHz frequencies (up to 10GHz), higher dielectric strength and better TCC by optimizing size of the filler and controlling its distribution in the polymer matrix. This material can be applicable for the use either in discrete RF components or in being embedded within the packaging substrate as an embedded RF capacitor material. **PCBDESIGN**

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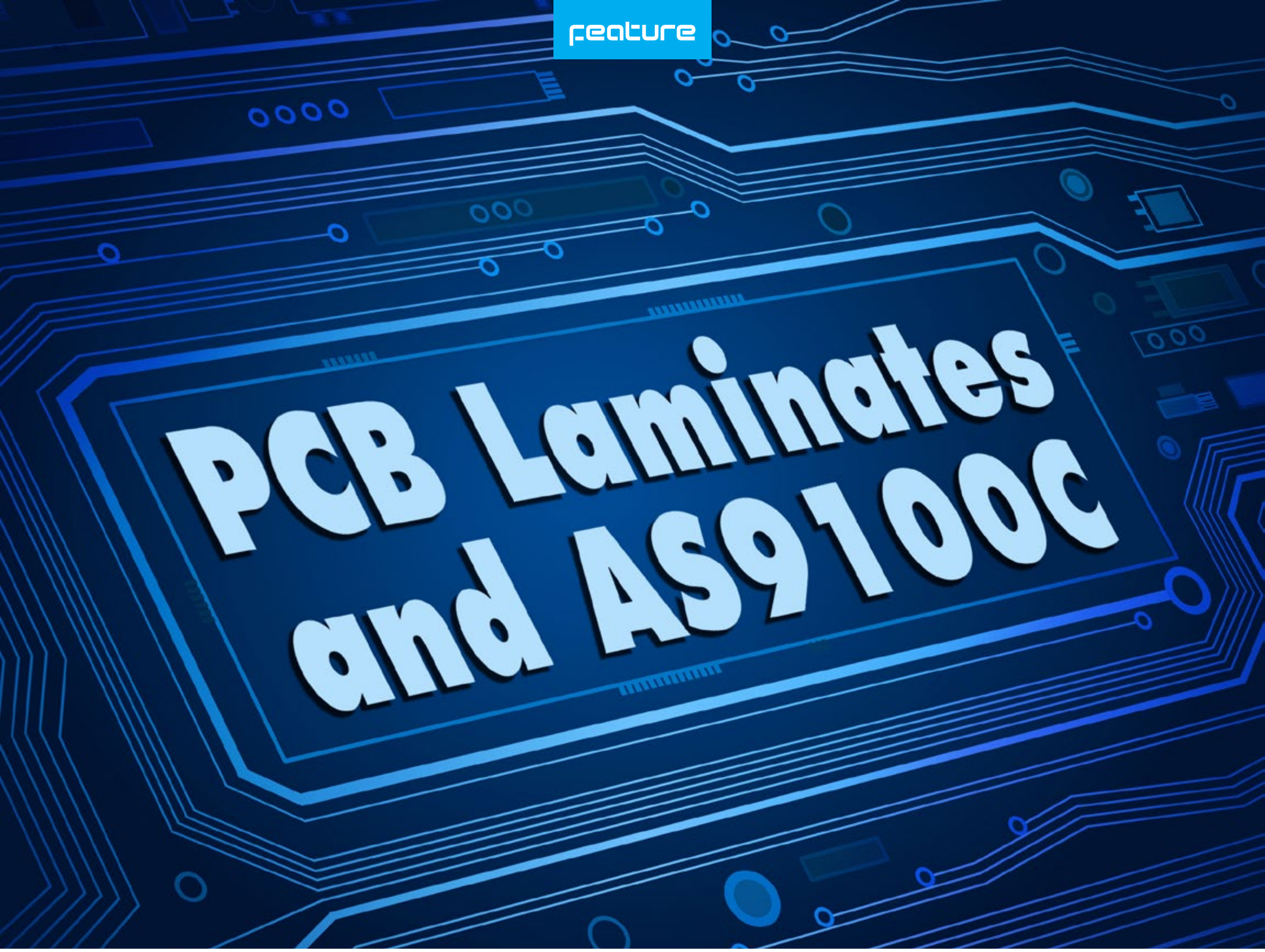


by Martin Cotton and Mark Goodwin
VENTEC INTERNATIONAL GROUP

Legislation at the factory level, by way of procedures, can assist in reducing failures by making sure not to introduce a failure mechanism into the product. Laminators and PCB suppliers must share the responsibility for fostering a culture of cleanliness and quality.

Additionally, good processing is a must to avoid introducing faults into the laminate or printed circuit board. It is preferable that the whole supply chain from the laminator to the PCB manufacturer and the EMS providers are all covered by the same accreditation. In the aerospace segment, all involved share the burden of making the supply chain compliant with AS9100C.

It therefore makes sense to have accreditation in all camps. As the recipient of the final product, the OEM should demand this certification. But how complete is the actual coverage of any accreditation, including AS9100C? The procedure for tracking product quality and delivery is a good model to review, because it considers concepts from source to destination, the whole pipeline. So, why not apply a similar model when applying AS9100C? It is a thought!

The PCB manufacturer must come under the same accreditation rules to comply with the ideal of lowest-cost manufacture, which means highest yields and no-failure introduction. The processes must be correct, so aerospace OEMs will benefit from partnering with PCB manufacturers who have AS9100C accreditation. As I revisit the concept of pipeline accreditation, it becomes obvious that, with so many variables and opportunities for introducing faults, any fault-reduction methodology is welcome. AS9100C typifies how the avionics industry leads the way in supply chain accreditation; compliance leads

to a cascading effect downwards into other market sectors, and it also shows leadership in quality ideals.

While OEMs are often presented as the main barriers to material change, the bottleneck is more likely to be the PCB fabricator. The complex nature of manufacturing materials and processes—chemistry, etching, plating, material preparation, etc.—requires standards and specifications to control the output. This has many levels, from single process steps to corporate specifications and regulatory requirements. Compliance with a standard indicates that you, as an organisation, have taken the time to understand the supply chain.

Remember that laminates follow the same basic process manufacturing steps as a PCB. Glass, resin and copper are processed to create laminates, and process steps similar to that of PCBs can introduce faults and lead to material failures. The selection of materials is usually left to the manufacturer, who usually receives a print with very open options regarding material type and composition.

Typically, the Tg is given as the basic information on material type. As circuit speeds rise, a more critical selection of material takes place, with Dk and Df also selected as material guidance criteria. Thermal reliability, along with electrical performance, becomes more of a driver for specific materials or a particular group of materials, but this is, in the main, left to the PCB fabricator. The fabricator supplies that information to the OEM design department, who then place it on the drawing. Selecting high-speed materials, for example, is something that the OEM design departments are being drawn into, and it is perhaps here that the selection processes become important to the OEM. Having made the basic selections to fulfil design functionality, choosing a material supplier is often more difficult. Manufacturability is key. How easy is the material to process?

This is where the fab shop steps in and tells the OEM which "approved" materials are available for the design. This is based on many things: cost, a strong supply chain, or even specific accreditations. If your material selection process includes suppliers that have regulatory approval or accreditation, then you can usually be assured of quality and reliability. Having your laminate supplier and fabricator accredited is vital to demonstrating that your supply chain pipeline is controlled. The OEM typically owns the quality culture for the product. Why not request the same from all of its suppliers?

You cannot test faults out of a laminate, because a fault causes a failure. It is this failure

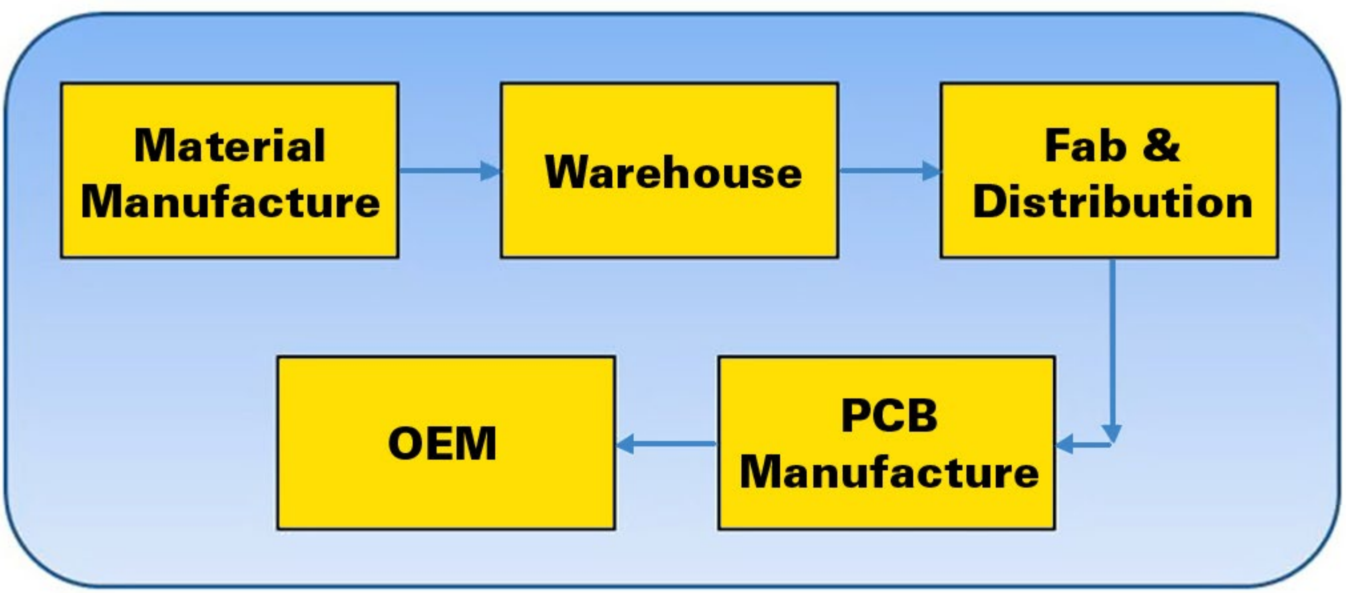


Figure 1: Chart showing how AS9100C covers the entire supply chain.

that shows up during testing. This raises the question: How much should you test? Should you even test at all? If the processes are correct, then there should be no failures, and no need to test. Testing is an overhead expense. Yes, we know that the industry will keep on testing, but it always raises the question of why we tested in the first place when we found no faults.

After all of this, you do not want to be let down by having distribution systems or methodologies that introduce faults. So, you need your clean, no-fault culture to follow you out to laminate distribution, directly from the manufacturing plant.

Advanced laminate manufacturers with AS9100C accreditation such as Ventec foster a cleanliness culture. This means that less checking is required to ensure that the laminate is fault-free, and that faults will not be introduced into the material.

Even OEMs outside the aerospace segment can benefit from partnering with AS9100C-accredited companies. Often, the cultural effects of this standard pervade the working methodologies and practices throughout the company, along with stricter policy elements of standard.

OEMs may find standard accreditation, particularly AS9100C, to be a useful measure of quality when qualifying potential partners, both laminate providers and fabricators. **PCBDESIGN**

Martin Cotton is OEM Technology Director for Ventec International Group.

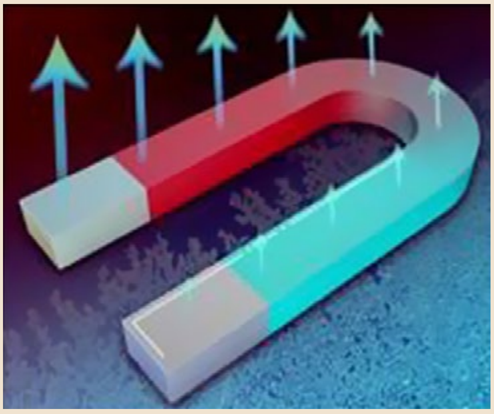
Mark Goodwin is the COO USA & Europe for Ventec International Group.

Magnets May Act as Wireless Cooling Agents

The magnets cluttering the face of your refrigerator may one day be used as cooling agents, according to a new theory formulated by MIT researchers.

The theory describes the motion of magnons — quasi-particles in magnets that are collective rotations of magnetic moments, or "spins." In addition to the magnetic moments, magnons also conduct heat.

"You can pump heat from one side to the other, so you can essentially use a magnet as a refrigerator," says Bolin Liao, a graduate student in MIT's Department of Mechanical Engineering. "You can envision wireless cooling where you apply a magnetic field to a magnet one or two meters away to, say, cool your laptop."



In theory, Liao says, such a magnetically driven refrigerator would require no moving parts, unlike conventional iceboxes that pump fluid through a set of pipes to keep things cool.

Liao and his colleagues recognized a similar "coupled" phenomenon in magnons, which move in response to two forces: a temperature gradient or a magnetic field. Because magnons behave much like electrons in this aspect, the researchers developed a theory of magnon transport based on a widely established equation for electron transport in thermoelectrics, called the Boltzmann transport equation.

"There's still a long way to go for thermoelectrics to compete with traditional technologies," Liao says. "Studying the magnetic degree of freedom could potentially help optimize existing systems and improve the thermoelectric efficiency."

PCB007 News Highlights

Schweizer CEO Reappointed Board Member of ZVEI

At the general meeting of the Zentralverband Elektrotechnik und Elektronikindustrie (ZVEI), the German electrical and electronic manufacturers association, in Munich, Germany, Dr. Marc Schweizer, CEO of Schweizer Electronic AG, was reappointed a member of the board of ZVEI.

Electronics Industry Leaders Meet with Policy Makers in D.C.

A healthy electronics industry is critical to the economy and national security of all nations. That's why 17 IPC member-company executives gathered in Washington, D.C. to meet with senior policy makers as part of IMPACT 2014: IPC on Capitol Hill. Through a series of meetings, the executives educated lawmakers about the needs of our industry.

IPC: PCB Industry Growth Slows in May

"While sales growth is slowing, declining orders pushed the book-to-bill ratio below parity after just two months of positive ratios," said Sharon Starr, IPC's director of market research. "This setback in the industry's recovery is likely to be short-lived, given the positive economic outlook for North America this year," she added.

Newbury Begins Redevelopment Program

Newbury Electronics has begun the initial phase of its redevelopment program early this month. West Berkshire MP Richard Benyon recently visited Newbury's premises to learn more about its redevelopment of the site, which will ultimately provide increased production space, new offices, and deliver savings in both water and electricity consumption.

PCBs Enumerated at Category XI of USML

The U.S. Department of State published a final rule that enumerates PCBs in Category XI for Military Electronics of the United States Munitions List (USML). This is a significant win for IPC which has advocated for the enumeration of PCBs on the USML.

Sunstone Circuits Names Hammer QA Manager

Sunstone Circuits, the leading PCB prototype solutions provider, has named Dennis Hammer as quality assurance manager. In this position, he will play a vital role in the management of product quality, continuous improvement, and process analysis.

Global, China Advanced Rigid PCB Industry Report

The PCB industry is fairly mature, with the growth rate generally not more than 6%. The output value of rigid PCB vendors has long been declining—the year 2012 witnessed hard times for rigid PCB vendors at a time when the smartphone and tablet PC market showed unexpectedly rapid growth. This sent rigid PCB vendors into a fierce price war, leading to a drop in profit and revenue.

TTM Shanghai Earns Zero Defect Award from Spansion

TTM Technologies, Inc. announced that its Silicon Platforms facility in Shanghai received the World Class Supplier—Zero Defect Award from Spansion Inc. on June 16, 2014 for supplying top quality, zero defect substrate products in 2013.

Merlin Circuit Installs Latest ITC Via Plugging Machine

Flintshire-based Merlin Circuit Technology has completed the installation and testing of the latest via plugging machine supplied by ITC. The THP35 is the most advanced system currently available and gives the ability to reliably fill all via types by way of its vacuum head.

Colonial Committed to IP Safeguarding; Earns IPC-1071QML

IPC's Validation Services Program has awarded its first IPC-1071 Qualified Manufacturers Listing (QML) to Colonial Circuits Inc., a full-service printed board manufacturer in Fredericksburg, Virginia. The facility underwent an intensive audit based on IPC-1071, Best Industry Practices for Intellectual Property Protection in Printed Board Manufacturing.

High-Speed Networks Drive New Material Choices

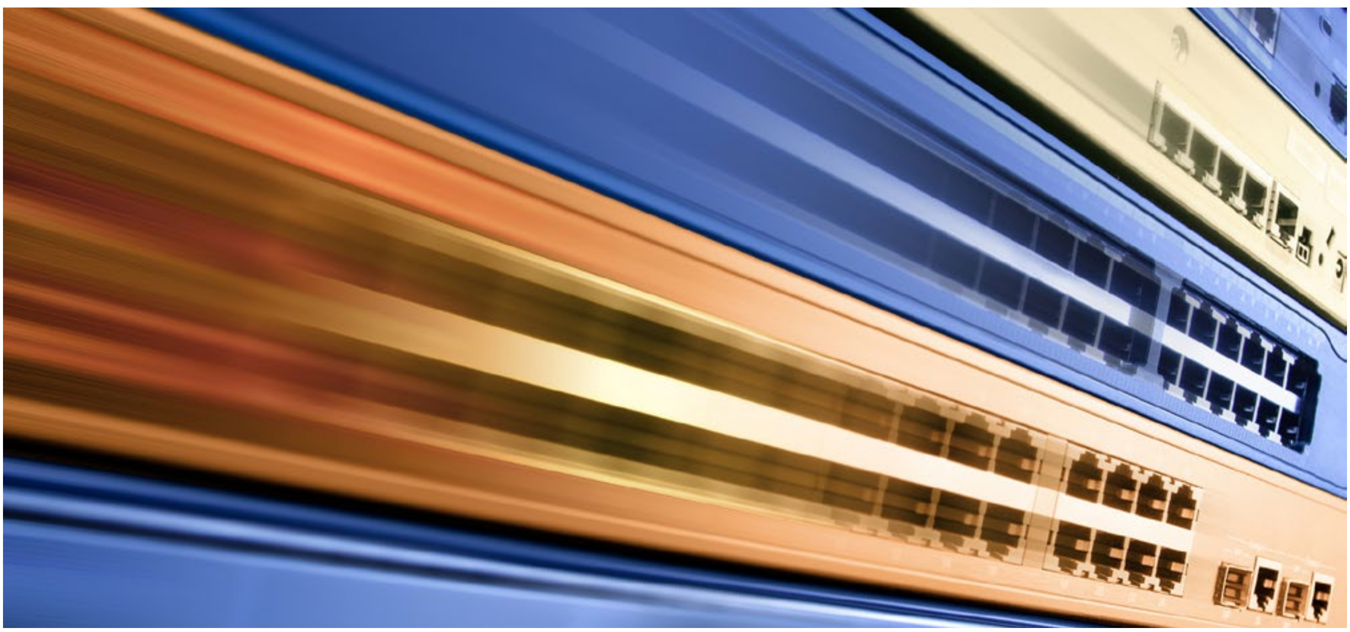
by Amit Bahl
SIERRA CIRCUITS

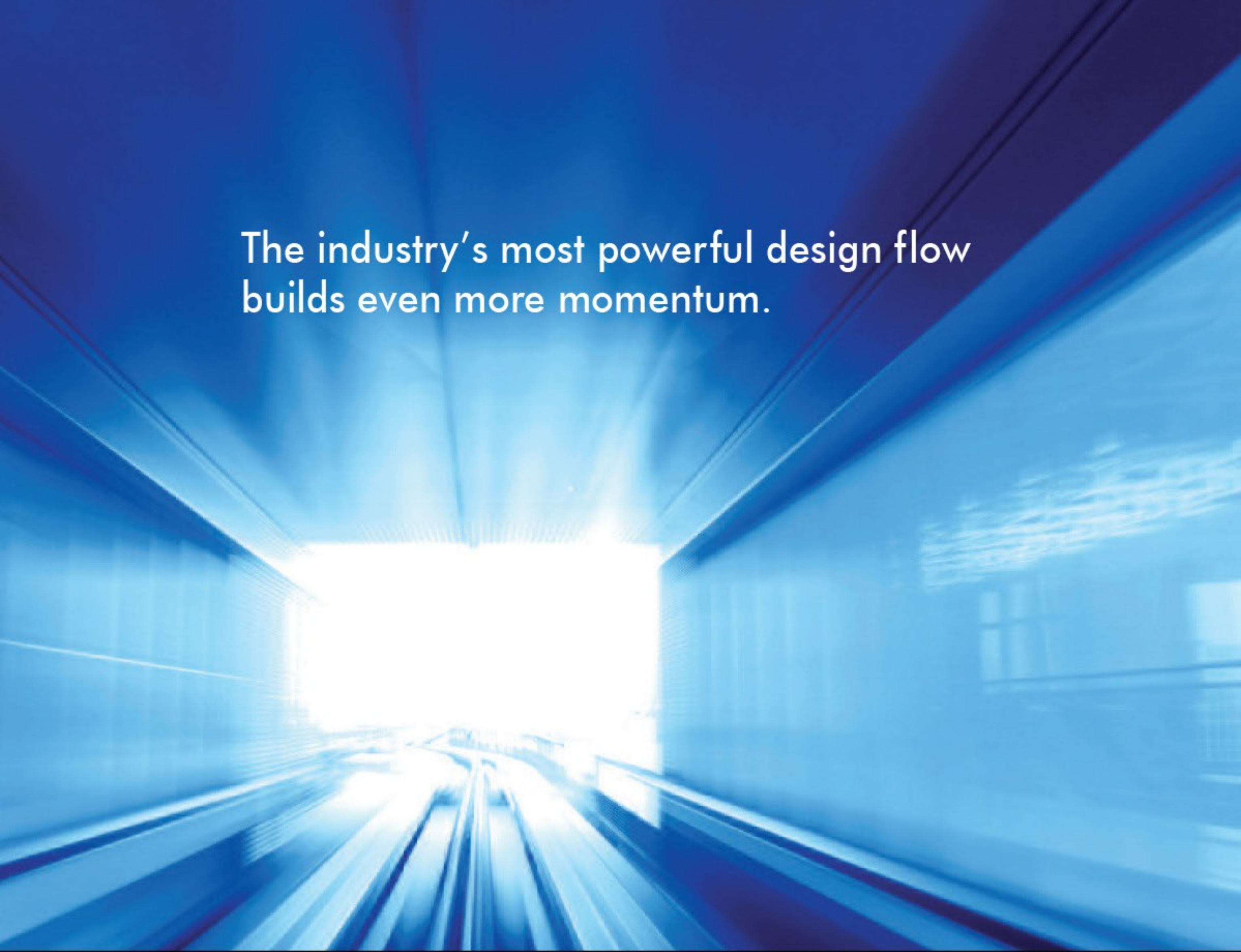
One third of the entire human population uses the Internet, according to the International Telecommunication Union, the United Nations agency for information and communication technologies. And access to the network is burgeoning, especially in developing countries. Not only is the sheer number of people online soaring, but demand for video services and other data-intensive applications is compounding burdens on network bandwidth. Likewise, data-intensive business applications are straining the bandwidth of corporate IT infrastructures. Every sector of the electronics industry is being driven by the need to provide greater network capacity, yet improve the efficiency of network communication equipment in terms of bits per second per watt. This includes the manufacturers of laminates for printed circuit boards.

Cisco Systems presented a roadmap for the company's laminate requirements through 2015. The company's top priority for high-end network routers and line cards is a material that has half the Df of Megtron 6 at 10 GHz and requires no unusual processing during PCB fabrication, as do PTFE laminates, which are difficult to drill, desmear, and plate. It also emphasizes resistance to CAF and thermal reliability for lead-free assembly operations for such a material.

I recently met with Leena Guila, who manages product marketing to OEMs and other customers for Isola, and her colleague Michael Miller, senior manager for OEM marketing. Close relationships with laminate suppliers are, of course, imperative for such PCB manufacturers as my company, which specializes in prototype fabrication and assembly. We had a far-ranging discussion, but concentrated on the material requirements for high-speed digital systems, especially network routers and line cards. They differentiated between the properties needed for high-speed network line cards and those for router backplanes.

Backplanes for carrier-class routers comprise many layers, may span distances of 30 inches




The industry's most powerful design flow
builds even more momentum.

or so, and must possess loss characteristics low enough to support succeeding generations of increasingly faster line cards without attenuating signals beyond budget as frequency climbs. These passive interconnects that tie together the press-fit connectors, into which the modules for line communications plug, can stave off the need for redesign as data rates increase, provided the Df of the laminate is low enough to provide a wide safety margin.

Line cards to support 100-Gb/s Ethernet communications also call for PCB materials with loss characteristics lower than that of Megtron 6. Such cards could have upward of 20 layers with very dense routing, many thousands of plated holes packed very tightly, and many expensive, highly integrated devices packaged in BGAs that have complex contact matrices on a tight pitch. These cards can involve multiple lamination cycles during fabrication and their assembly entails the high temperatures required for lead-free solder. Beyond the transits through the assembly oven and wave soldering, some cards could require rework to remove and replace a BGA, for example, and that repair would involve heat to remove the device and then another heat cycle to attach the replacement. Such designs and circumstances are ripe for CAF growth unless a laminate is thermally very stable and robust, the bond between resin and fabric is void-free from the start, and care is taken during drilling and desmear to preclude wicking. There is also the possibility that the thermal cycling can change the Dk and Df of a material, thereby compromising signal integrity.

"Such designs and circumstances are ripe for CAF growth unless a laminate is thermally very stable and robust, the bond between resin and fabric is void-free from the start, and care is taken during drilling and desmear to preclude wicking."

Cisco Systems and the other manufacturers of high-speed network equipment have developed extremely stringent internal procedures and standardized test vehicles for qualifying laminates to ensure the materials will survive conditions far more severe than would ever be encountered during manufacture. These are tall hurdles. Materials that pass would also be prime candidates for a wide spectrum of other high-speed digital applications, provided the price is right.

The Isola representatives pointed to two laminates, the second of which was just introduced in late June 2014, Tachyon and Tachyon-100G, respectively, which they recommend for building router backplanes, line cards, and PCBs for other very high-speed digital applications. The two laminates have identical electrical characteristics, including a Df of 0.002 and a Dk of 3.02 that is invariant up to 40 GHz.

Tachyon-100G was introduced to target very high-speed line cards (think 100-Gb/s Ethernet) because of its thermal stability, in particular a very low co-efficient of expansion in the Z-axis, suiting it especially to such high-layer-count constructions. Both the materials use spread glass along with very low-profile copper foil (2 µm Rz surface roughness) to help minimize weave-induced differential skew, cut signal rise times, and reduce jitter and intersymbol interference.

The materials come in a wide range of prepreg and core thicknesses and are processed in the same manner as typical FR-4 laminates. They can be used as either a core or prepreg in hybrid FR-4 builds.

Any materials with the sort of dielectric and thermal performance as described are welcome additions to a PCB manufacturer's catalog of laminates, especially since they do not involve the complications inherent in processing PTFE-based materials. I'll provide comparisons with other laminates in the near future. **PCBDESIGN**

Amit Bahl directs sales and marketing at Sierra Circuits, a PCB manufacturer in Sunnyvale, California. He can be reached by clicking here.

i-connect007 panel discussion video

Printed Electronics

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This panel, moderated by Ray Rasmussen, covers the current state of printed electronics, and offers a look at what the future holds for this new technology. Panelists include John Andresakis, VP of strategic technology for Oak-Mitsui; Scott Gordon, business development manager at DuPont Teijen Films; and Josh Goldberg, marketing specialist for Taiyo America.

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Device Uses Lasers, Sound Waves for Melanoma Imaging

A new hand-held device that uses lasers and sound waves may change the way doctors treat and diagnose melanoma, according to a team of researchers from Washington University in St. Louis. The thicker the melanoma tumor, the more likely it will spread and the deadlier it becomes, says dermatologist Lynn Cornelius, one of the study's coauthors.

Because skin scatters light, high-resolution optical techniques don't reach deep enough. "None are really sufficient to provide the two to four millimeter penetration that's at least required for melanoma diagnosis, prognosis or surgical planning," says engineer Lihong Wang, another coauthor on the Optics Letters paper.

Recently, researchers including Wang have applied an approach called photoacoustic microscopy, which can accurately measure melanoma tumors directly on a patient's skin--thus allowing doctors to avoid uncertainty in some circumstances.

Wang, Cornelius and their colleagues previously built a similar desktop device, which shines the laser directly onto the tumor. But so much light is absorbed that very little penetrates to the tumor's lower layers. The latest version, however, is not only hand-held, but it also delivers light around and below the tumor, which generates a bright image of the tumor's bottom and an accurate measurement of its depth.

The researchers tested their device on both artificial tumors made of black gelatin and on real ones in live mice, showing that the instrument could accurately measure the depths of tumors—and do it in living tissue.

Initially, this tool will be mainly used for improving how doctors plan and prepare for surgeries, Cornelius says.

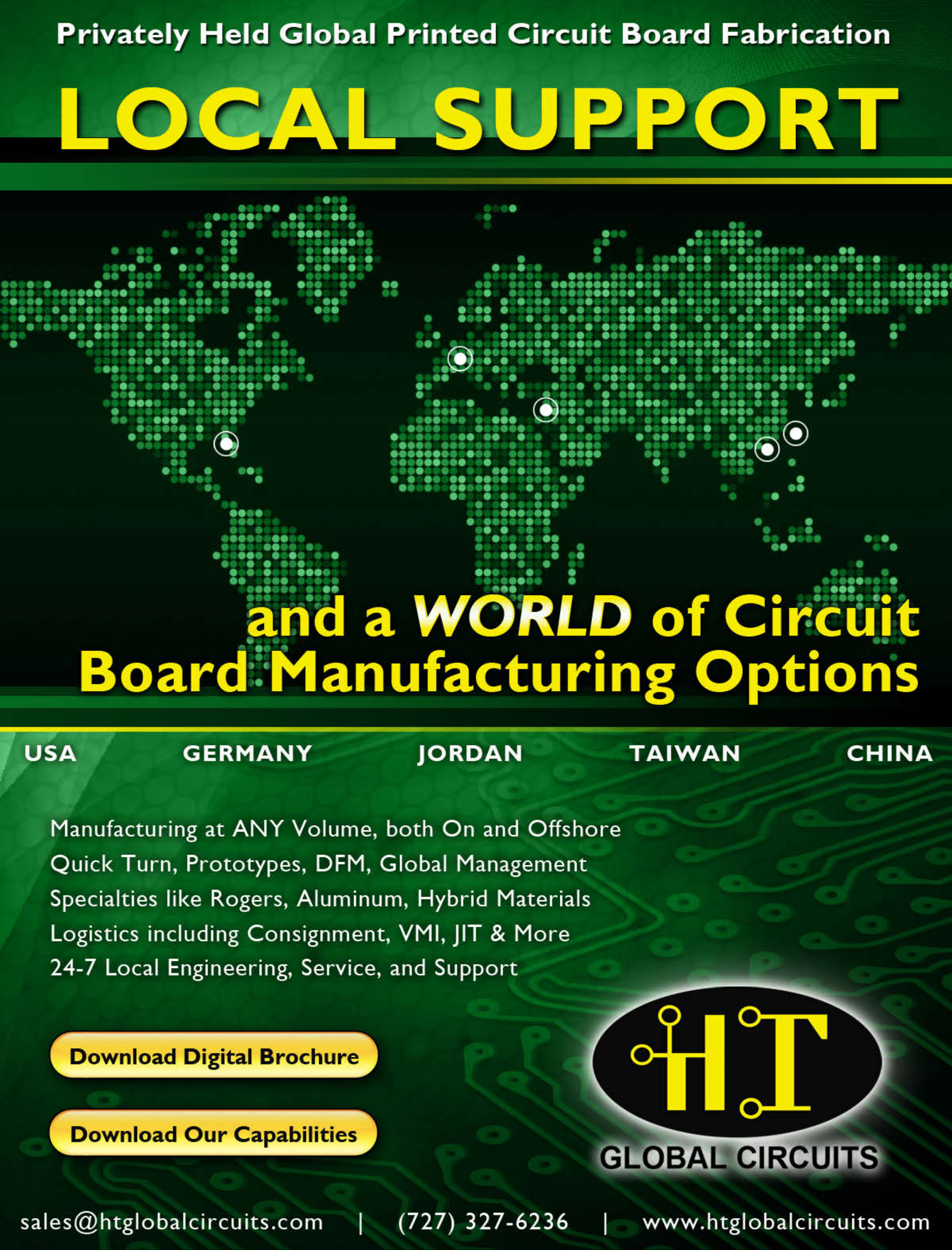
Environmental Effects on High-Frequency Material Properties

by John Coonrod
ROGERS CORPORATION

PCBs can be subjected to a variety of environmental conditions, which can cause changes in the material and alter how a PCB operates. For those who are less familiar with circuit material properties, there is often an unrealistic expectation that material shouldn't change electrical performance when subjected to different environments. Actually, all circuit materials will change some properties when evaluated within a changing environment. Some properties may change more than others and some materials may have more change than others, but they all do change.

The materials formulated for use in high-frequency PCB applications are formulated so that critical electrical properties have minimal change when subjected to a changing environment. In the material development process, it is always a juggling act to allow some properties to change more so other properties will change less. All engineers typically struggle with difficult tradeoffs on just about any complex engineering task, and it is no different when formulating circuit materials.

One material property which is often overlooked until a field unit failure demands attention is TCDk (thermal coefficient of dielectric constant). This property is innate to all circuit materials; however, materials not formulated for high-frequency applications often have an extremely poor TCDk. Conversely, high-frequency laminates are formulated to have good



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TCDk properties and as a general statement, a good value would be 50 ppm/°C or less and this value would be an absolute value in the mathematical sense. Of course, the closer the material is to zero for TCDk the better.

The comment about a field failure attracting attention to TCDk is valid, because unaware engineers may fine-tune the application in a controlled environment, such as a lab, only to find that it will change electrical performance as the unit goes through normal temperature cycling in the field. TCDk describes how much the material will change dielectric constant with a change in temperature; the TCDk value varies among the different types of high-frequency PCB materials. In general, PTFE-based laminates have excellent electrical performance for loss but suffer from high (poor) TCDk. This is one reason why some PTFE laminates are filled. With the proper filler, the TCDk can be adjusted to a good, low level. For example, a nearly pure PTFE laminate may have a TCDk value of 200 ppm/°C whereas a PTFE laminate with ceramic filler can have a TCDk of 20 ppm/°C.

Satellite applications are sensitive to TCDk. The change in temperature which the PCB is subjected too can be extreme and if the dielectric constant (Dk) changes significantly, the PCB will not operate in the manner for which it was designed. A common material used in satellite applications for its consistent and low TCDk is the Rogers TMM laminate. However, as mentioned earlier, in the formulation process of a material, there are many tradeoffs. The TMM materials are excellent for TCDk properties, but require extra attention during the PCB fabrication process. A good understanding of the PCB manufacturing properties helps fabricators adjust their processing conditions, allowing them to manufacture a robust circuit using these materials.

“*The TMM materials are excellent for TCDk properties, but require extra attention during the PCB fabrication process. A good understanding of the PCB manufacturing properties helps fabricators adjust their processing conditions, allowing them to manufacture a robust circuit using these materials.*”

Another material property to consider which is related to change in operating environment is TCDf, the temperature coefficient of dissipation factor. This is the property of a laminate where the Df changes with a change in temperature. In many applications, the TCDk is much more important than TCDf but there are some designs which are more sensitive to TCDf. Typically, TCDf is important in PCB configurations where it is critical that loss performance remains consistent. As with TCDk, the TCDf property is often very different when comparing one type of high-frequency circuit material to another.

In general, the materials with high Df values typically have a higher TCDf. As another real-life example, a nearly pure PTFE laminate has a very low Df of about 0.0009 and the TCDf is also low at 20 ppm/°C, as compared to a ceramic filled hydrocarbon laminate where the Df is about 0.004 and has a TCDf of about 50 ppm/°C. Even though 50 ppm/°C is not considered bad, the difference between these material TCDf properties is more than double.

If a designer is not familiar with material attributes, ensuring consistent electrical performance of high-frequency PCBs can be more complicated than expected. Due to this concern, it is always recommended that the designer consult their high-frequency materials manufacturer for advice on proper materials when considering a new design. **PCBDESIGN**

John Coonrod is a market development engineer for Rogers Corporation, Advanced Circuit Materials Division. To read past columns, or to reach Coonrod, click here.

Part 1: Taking Control

by Charles Pfeil
MENTOR GRAPHICS CORP.

This article is part one of a three-part series that will discuss a new routing tool that allows PCB designers to “sketch” the routing of traces and then routes along the path of the sketch (Figure 1). The articles discuss the core elements of effective PCB routing—control, quality, and performance—and how the sketch routing environment empowers the designer to succeed with each of these elements.

In the past, one of these three was always missing from routing capability; yet without all three, the functionality falls short of being the truly useful and desirable solution that designers want. This first article describes the kind of control over routing that is expected.

As designers, we often envision topology forms in our minds as we organize the rough component placement and as we refine it within the context of each particular design. Of course, there are exceptions that make this visualization difficult, such as emulation or network boards where nearly every BGA I/O is connected to every other of the 8, 16, 32 or more BGAs on the design. And to our horror, the netline display is so dense that it appears as a solid color.

With those types of designs, something beyond the normal approach is needed. Normal designs feature an organization of ASICs and/or FPGAs with interfaces, various functional circuits, and power supplies, which are grouped and positioned during placement.

With that so-called “normal” design, a plan, a flow of the routing, and a solution to the interconnect complexity forms in our imagination, which is coupled with the graphic feedback of netlines, classlines, coloring, and filtering. Designers want tools that enable control of the actual routing so that it matches this vision.

The control needed is three-fold: location, constraints, and route style. This is what a designer needs to manage for successful routing of the design as intended. This control needs to be easily applied without abusive setup maneuvers.

Location

Location is not only related to the layer(s) where the routes are to be placed, but also the path or channel where the traces run. River routing is a term that applies to much of today’s routing, because there is a desire for the

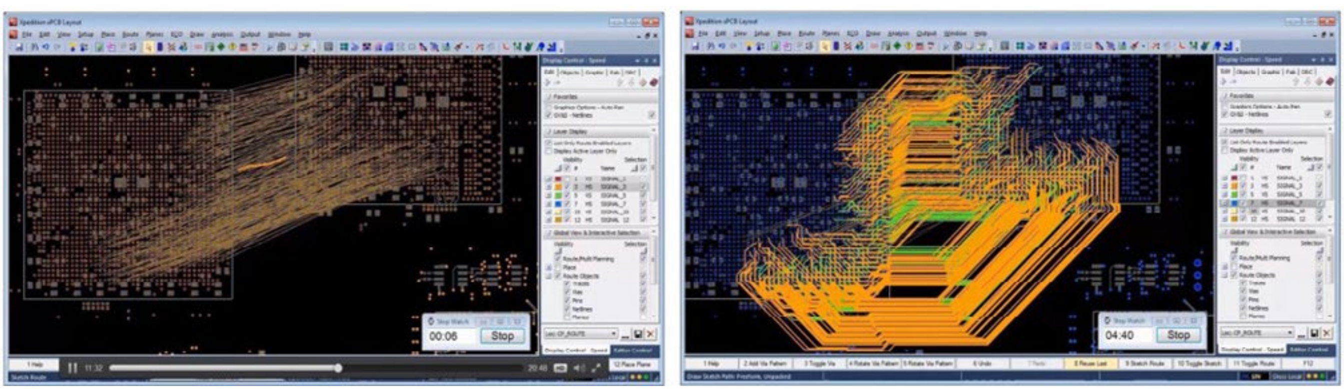
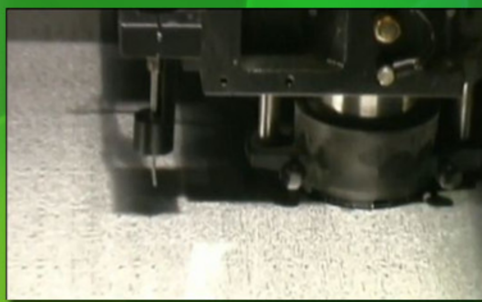


Figure 1: With sketch routing, the designer looks at the netlines and then draws a sketch (left), directing the router as to how they should be routed. On the right, the completed routing is shown.


Multilayer
Technology



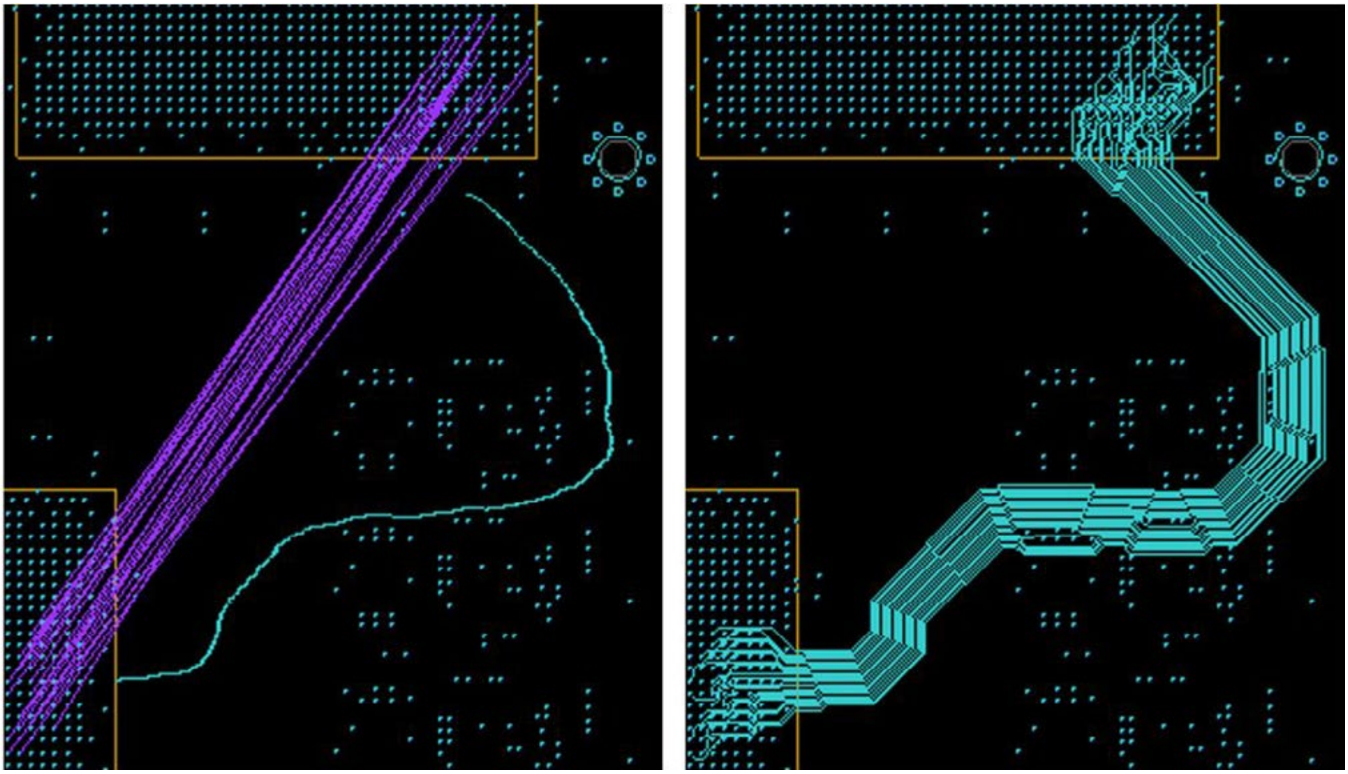


Figure 2: Meandering path location described by a sketch and after routing.

routing to flow in the most efficient path, without X/Y bias, through the channels available between components. Often the routing of one set of traces needs to be done while recognizing that one or more additional sets of traces need to be in the same area. Controlling the routing location, while leaving enough room for other routes, is essential. Advanced design tools such as Mentor Graphics' Xpedition Layout use a freeform or angled line sketch path that enables the designer to maintain this kind of control (Figure 2).

Constraints

Routing needs to be controlled in ways that enable the designer to fulfill the signal integrity and fabrication requirements. This is accomplished by following the constraints that are setup prior to routing. For example, setting appropriate physical constraints between objects enable higher yield during fabrication. Trace widths and clearances also allow managing impedance and avoiding crosstalk. The sketch routing environment follows the physical rules set in the constrain manager, which has a hierarchical structure to define general and very specific rules. The signal integrity rules are also very detailed along with the means to define pad entries and Z-axis clearances. A hierarchical matched length definition, including phase matching, enables control of the tuning algorithms.

There is one particular object in PCB routing that needs to be restricted and avoided: the through-via. Designers need the ability to minimize the use of vias. Vias used to be considered undesirable primarily due to fabrication costs—reduce the number of vias, reduce the cost. While that is still true, it is a less significant factor compared to the negative impact that vias have on signal integrity. There are enough problems created by the through-via that a paper could be written just on that subject. Since I don't want to bore your with through-via condemnation in this article, can we simply agree that through-vias should be avoided with high-speed signals? A successful routing methodology must give the designer the ability to pre-

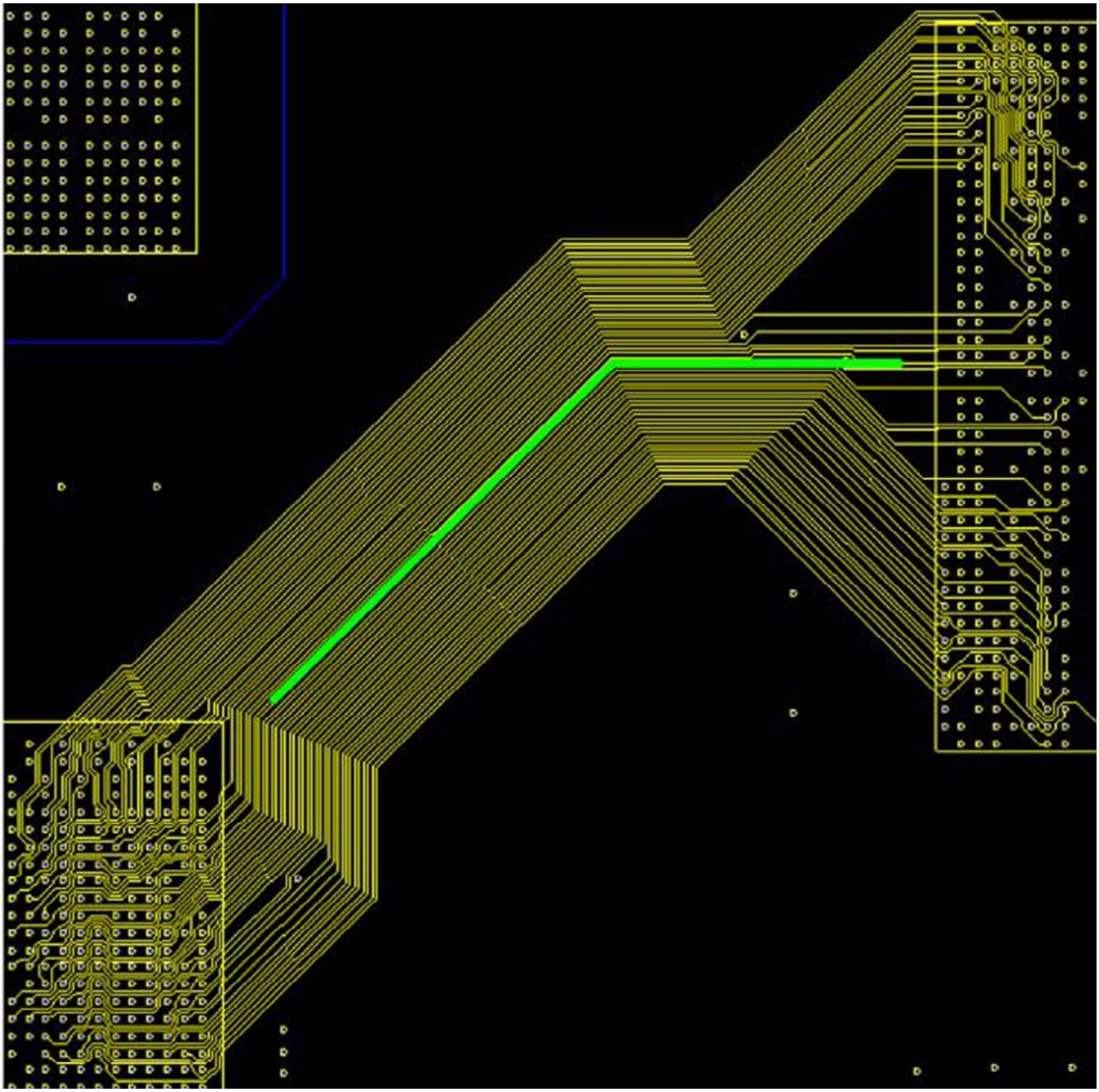


Figure 3: Packed-style routing groups traces for dense situations.

vent vias, yet if they are necessary, control their location.

By default, the sketch router does not add vias except in two cases. First, if the fanout vias are needed and they do not exist, it will put them in. Secondly, when drawing a sketch path, the designer can specify a via pattern for transitioning to another layer. There are four styles, with control over the direction of routing in and out of the pattern, and eight rotations of each.

Route Style

In the context of control, route style is a matter grouping the traces together or spreading them out. Assuming the rules are followed

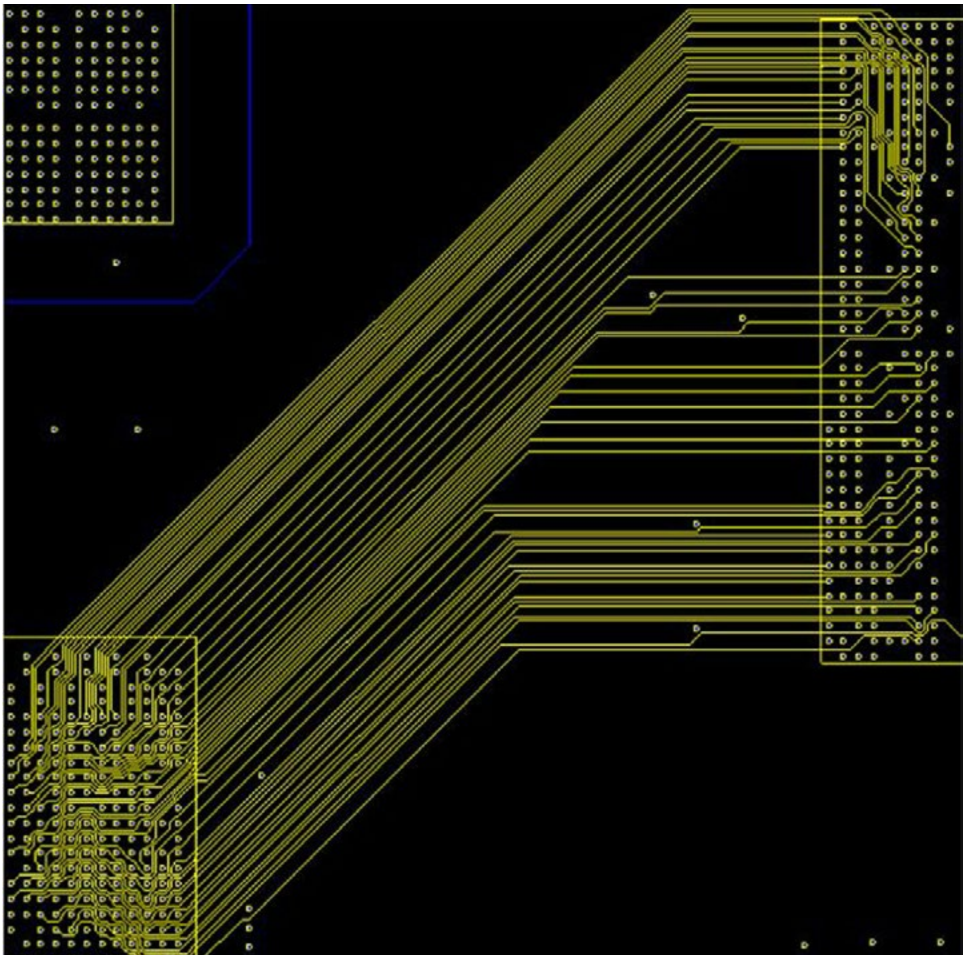


Figure 4: Routing using an unpacked style.

to provide optimal spacing in order to minimize crosstalk, designers want to pack the traces together in dense areas and spread them out in more open areas. Considering again the visual comprehension that a designer has for the routing, the dense areas are known; and during the routing task, it is clear which groups of signals need to be packed together to maximize the density of the routing channels. Style and quality are similar; however, the second part of this series will go deeper into all the aspects of what constitutes quality.

The sketch router allows the designer to route either a packed or unpacked style. The packed style will group the traces together and is very useful in dense situations (Figure 3).

The unpacked style (Figure 4) routes in a direct and efficient manner, which naturally will spread the traces apart compared to the packed style. In both cases, the tuning algorithms will work just fine because in both cases, the existing traces are pushed and shoved to allow enough space for the serpentines, trombone or sawtooth patterns.

Sketch routing is one of those things that is better demonstrated with video than still images. For a quick video of what sketch routing looks like, click here.

Summary

You could say that allowing the designer to control location, apply restrictions and choose a style is exactly what occurs during common interactive routing. Yes, this is true. Manual routing provides the control and quality, but is often slow and significantly slower on large designs. Automatic routing provides the performance and a certain amount of control, but it lacks the quality. But advanced sketch routing technology provides designers with this desired control, along with quality and high performance. **PCBDESIGN**

Charles Pfeil is an engineering director in the Systems Design Division at Mentor Graphics. He was the original product architect for Expedition PCB and an inventor of XtremePCB. Pfeil has been in the PCB industry over 40 years as a designer, owner of a service bureau, and has also worked in marketing and engineering management at Racal-Redac, ASI, Cadence, PADS, and VeriBest. To contact him, click here.

Mil/Aero007 News Highlights

Murrietta Circuits Nets Raytheon Five Star Supplier Award

Andrew Murrietta, CEO and co-owner of Murrietta Circuits, announced that his company has been awarded Raytheon's Five Star Supplier Recognition Award for the second year in a row. He says, "This is truly overwhelming for me and the rest of the Murrietta team. I know we have all worked hard to make this happen and we are so pleased and proud we were recognized again this year."

IPC Lauds U.S. Rule on Military-related PCBs

Following years of advocacy work to clarify the treatment of printed circuit boards (PCBs) under International Traffic in Arms Regulations (ITAR), IPC is applauding the U.S. Department of State's final rule for Category XI for Military Electronics of the United States Munitions List (USML). Published today, the new rule states that PCBs "specially designed" for defense-related purposes will be controlled under USML Category XI. Additionally, any designs or digital data related to "specially designed" PCBs will be controlled as technical data.

FTG's Aerospace Segments Show Dramatic Q2 Improvements

"FTG's momentum has continued through the first half of 2014 with strong results across the company, particularly at our two new aerospace facilities in Tianjin and Chatsworth where we continued to see progress on qualification activities, strong orders, and increased shipments," stated Brad Bourne, president and CEO.

Merlin Flex Earns SC21 Bronze Award

Flexible and flex-rigid PCB manufacturer Merlin Flex Ltd., based in the Northeast of England, has been awarded a prestigious SC21 Bronze award. The SC21 programme has become a benchmark for supply chain excellence evaluating current business practices against rigorous international standards in quality, service, and business management.

Multilayer Technology Completes AS9100 Audit

Multilayer Technology of Irving, Texas is pleased to announce it has successfully completed a scheduled AS9100C + ISO9001: 2008 conducted in May 2014.

FTG Tianjin China Ships 10,000th Flight Deck Product

Firan Technology Group Corporation has shipped its 10,000th aircraft flight deck product from its facility in Tianjin, China. "It has been amazing to watch the development and growth of our new facility in Tianjin. The team there has learned so much and has developed world-class skills in illuminated cockpit products," stated Brad Bourne, president and CEO, FTG Corporation.

NASA Launches Mission to Monitor Earth's Breathing

NASA's Orbiting Carbon Observatory-2 (OCO-2) aims to locate Earth's sources of and storage places for atmospheric carbon dioxide, the leading human-produced greenhouse gas responsible for warming our world and a critical component of the planet's carbon cycle.

DoD Spending Driven by Geospatial Tech Innovation

The DoD is leveraging innovations in geospatial technologies to ensure commanders at every level have a deeper understanding of evolving operational environments. "After engineering and integration, improvements in dissemination and targeting will command the most attention, with spending in 2018 likely to stand at $712.6 million and $579.4 million, respectively," said Industry Analyst John Hernandez.

Power GaN Market to See 80% CAGR through 2020

Overall, 2020 could see an estimated device market size of almost $600 million, leading to approximately 580,000 x 6 wafers to be processed. Ramp-up will be quite impressive starting in 2016, at an estimated 80% CAGR through 2020, based upon a scenario where EV/HEV begins adopting GaN in 2018–2019.

Global Commercial Satellite Imaging Market Forecast

This report analyzes the commercial satellite imaging market on a global basis, with further breakdown into various sub-segments. It provides thorough analysis and market growth forecast of the global commercial satellite imaging market, based on its applications, end-use industry, and geography for the period from 2013–2019.

column

TIM'S TAKEAWAYS

There Are no Stupid Questions

by Tim Haag
INTERCEPT TECHNOLOGY

Are there really any stupid questions?

Well, of course there are. Try asking your high school graduate whether he would prefer a new car or a hearty "well done" as a graduation gift, and you will get a look that tells you that you've just asked a really stupid question. In fact, just asking if there are really any stupid questions proves the point. But now that I've gotten your attention, let's take a deeper look.

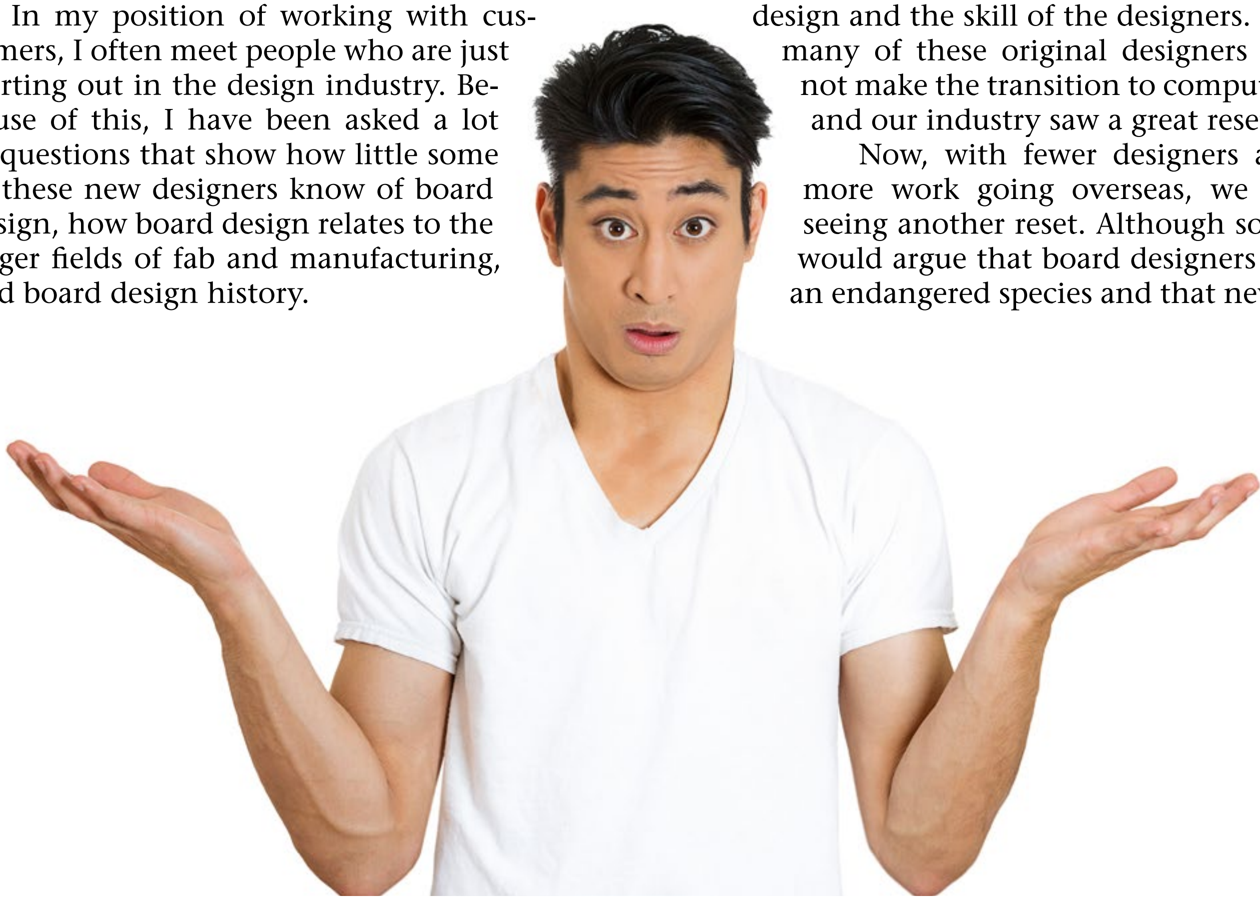
Many of us who have been designing boards for years have had to deal with annoying questions from "the kids." You know who I mean: the rookies, newbies, greenhorns or puppies just starting out in their design careers. We've all had to answer questions like, "Why is library development so important?" or "Why is solder mask green?"

In my position of working with customers, I often meet people who are just starting out in the design industry. Because of this, I have been asked a lot of questions that show how little some of these new designers know of board design, how board design relates to the larger fields of fab and manufacturing, and board design history.

Try telling one of these kids, "Back in the day, we used to lay out tape-up boards by first sticking down dollies," and you will get a very strange look in return. So, I understand the temptation to ignore questions that seem trivial, but I believe we do ourselves a great disservice by doing so. I'm sure that we can all remember times when those who were older and wiser helped us out when we were just puppies in this business.

Our PCB design industry has changed a lot through the years. When I first started designing boards in the '80s, many designers still created tape-up designs on drafting boards. These people were artists and the fact that some of these tape-up designs are still being fabricated today is a testament to the durability of the design and the skill of the designers. But many of these original designers did not make the transition to computers and our industry saw a great reset.

Now, with fewer designers and more work going overseas, we are seeing another reset. Although some would argue that board designers are an endangered species and that newer



THERE ARE NO STUPID QUESTIONS *continues*

tools and automation negate the need for the skills of an experienced board designer, I disagree. I believe that now, more than ever, our industry is in need of young people that excel in the latest technology and methods of board design to become the experienced designers of tomorrow. Technology will advance, but the need for experienced people will never disappear. And in order for people to grow and become the experienced designers that our industry needs, we need to be willing to invest a little of ourselves to help them.

A few months ago, I was walking my dog through the grounds of the local elementary school and I paused for a moment to watch a little girls' softball game. One of the balls lobbed in by the pitcher landed on the ground six feet or so in front of the plate. When the batter didn't swing at this pitch, her coach encouraged her by calling out, "Good eye, good eye!"

At first this seemed ridiculous to me. After all, the ball hit the ground long before it even came close to the plate. But then I looked at it through the eyes of an eight-year-old child and realized that from her perspective, the situation was very different. From where she was standing, that huge softball almost came over the plate. After all, it was ONLY six feet away. Whew! To those of us who are older and have had some experience playing ball, this would not be a situation that would concern us. But to an eight-year-old batter, it was a huge moment. And her coach did the greatest thing that he could do by encouraging her and telling her that what she had done was correct.

When we old salts of the design world get asked annoying questions by the greenhorns, shouldn't we treat those questions in the same way?

Years ago, a friend of mine told me that he used the philosophy of "holding a crown a few inches over an employee's head and watch them grow into it." This is actually tougher than it seems. The key is to give someone enough responsibility that they can grow with it without being overwhelmed by those same responsibilities. For this style of management to be successful, we need to stay engaged with newbies that we are mentoring and not leave them hanging. We have to be patient as they suffer through occasional failures while at the same time celebrating their victories.

> *"So, when these new designers ask questions that show how new they really are at this, let's do our best to help them to grow. After all, these are the people who are going to inherit this industry."*

It also means being supportive, helpful, and, yes, even answering the occasional annoying questions. Although this encouragement won't work with every person and in every situation, it is amazing how often it does work. So, when these new designers ask questions that show how new they really are at this, let's do our best to help them to grow. After all, these are the people who are going to inherit this industry. By making them successful now we help guarantee that the circuit board design industry will stay strong.

While I was working on this article I found out that one of my first bosses had passed away. As a young man I had just gotten my feet wet in the design world when my company had a layoff that unfortunately included me. Without much in the way of experience I started looking for design work and eventually found a small service bureau run by a gentleman named Darrel Pfeifer. Considering my slim résumé at that time, I don't know why he hired me.

But Darrel took a chance on me and over the next seven years of working with him, my skills as a designer truly grew. I worked on everything from wrist-watch sized designs to industrial-strength power boards and some of the first PC motherboards, and just about everything else in between. I think that it is safe to say that without my tenure at Darrel's service bureau, I wouldn't enjoy the career that I have today. Darrel led us by example, often working late into the night to finish up a design and then being back in the office early in the morning to manage the company.

Besides being an astute businessman he also led us by showing us the importance of family and a balanced life. All of us who worked there enjoyed the company parties at his house with our kids playing in his pool, competitive volleyball matches, and an abundance of food and conversation. And no one will ever forget him strolling through the design area during the work day and in his deep baritone voice issuing the command "Darts!" This was the signal to drop what you were doing and go into the back room for a quick game of darts.

I will forever be grateful to Darrel for all that he taught me about design, business, family and life. And it has made me wonder: For all of those who are new in our industry, who will be the Darrel in their lives? Just look in the mirror. Yes, we are the mentors. So let's do our best to help these newbies.

Just think, the next time one of these greenhorns asks you a really annoying question, you might just be helping to lay the foundation of someone who revolutionizes the business, creates new design technologies, or even designs the control circuits for the first starship. You never know.

And why is it that solder mask is green? There are a lot of different theories ranging from the natural resulting color of the original base resin and hardener used, to the color green being the most visible under different lighting conditions as specified by the military. As for me, I just prefer to tell the rookies that solder mask is green because all the other colors were busy at that particular time. **PCBDESIGN**

Tim Haag is customer support and training manager for Intercept Technology.

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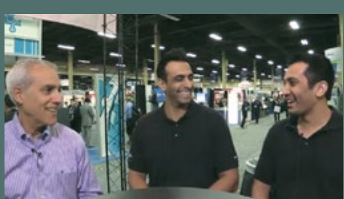
video interview

Dragon Circuits Expands Beyond PCBs

by Real Time with... IPC APEX EXPO



Dragon Circuits' Gunny Babaria and Rajan Babaria discuss their work with new partners, and the firm's move into new markets, including drones for non-military uses, such as search-and-rescue.

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Spacing is Irrelevant Below 270 Volts

by Bob Tarzwell and Dan Beaulieu

Dan Beaulieu: I have been friends with Bob Tarzwell for many years now. He and I met when he lured me to his shop in Carleton Place, Ontario, by telling me about all of the amazing things he was doing in that little shop of his. He claimed (and this was 1997, mind you) that he was building boards with 18 ounces of copper on a routine basis. He also told me that he producing lines down to 2 mils without any special equipment. My first reaction, which is pretty much the same as anyone who hears about Bob for the first time, was that this guy was full of it; there was no way he was doing what he claimed he was doing. So I had to go see for myself.

It turns out that Bob was doing all of these things, and more. He was operating a truly amazing little shop up there in the middle of nowhere. It was then I realized that Bob Tarzwell was not your average PCB engineer.

Just to give you an idea of what Bob is like here is a little story for you.

A True Tarzwell Tale

The day Bob came in, Director of Operations Mike Driscoll was late getting back from lunch. So Bob and I waited in the conference room with a number of Rockwell Collins engineers who were anxious to meet him. Thanks to Mike, everyone had already heard about Bob, and they planned to do everything they could to discredit him.

We had already been through the introductions, and now we were just killing time while


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waiting for Mike to show up. There was not much left to say or do until he got there. Outside, a thunder storm raged, and we could hear the thunder even though we were in an inside room without windows.

It was at this point that Bob, quite bored sitting around, said, "Did I ever tell you about the time I was struck by lightning twice in one afternoon?"

I was stunned! I looked around the room, hoping that no one had been paying attention. But that was not the case at all; instead, everyone was looking at Bob like he had snakes coming out of his ears.

I thought, Great! I bring this guy in, wanting him to back up and explain some of the technology claims that he is making, and here he is telling a lame-brained, incredible story like this. And these guys are all here to prove him not only wrong, but certifiable to boot. To make matter worse, Mike had just walked into the room in time to hear Bob's claim.

Without skipping a beat, Mike walked right up to Bob, held out his hand, and with a huge grin on his face said, "You have to be Bob Tarzwell. I've heard a lot about you."

Bob smiled and shook his hand.

And then Mike said, "Well, are you going to tell us how you were hit by lightning twice in one afternoon or what?"

Now Bob had the full attention of everyone in the room. Meanwhile, I was trying to disappear under the table, pretending that I was not the guy who had brought him here.

Completely unfazed, Bob told the story of how he had been struck by lightning twice in the same afternoon:

It was at our house in Canada. We were just finishing lunch when a thunderstorm hit. Man, it was a big one, worse than the storm going on outside now. I remembered that I had a car part in the back of the truck that I didn't want to get wet, so I ran out in the yard, got the part and took it to the garage. Just when I reached for the side door to the garage, I got hit by lighting. This was one of those all-metal buildings, so the lightning went right through it and into the doorknob and up my arm and knocked me down.

When I woke up a few minutes later, all of the hair on my arm was gone. Since there was still lightning, I went into the garage to get out of the rain. When I got inside, a lightning bolt hit the electrical pole outside. The lightning traveled down the wires, into the garage along an extension cord on the garage floor, which I was standing on. Zap! I got hit again. The funny thing was that, except for a few scratches I must have gotten from flying across the room, I was fine. Missing some hair, but OK.

I looked tentatively over at Mike to see his reaction. I thought that he was going to signal me to follow him out into the hall and tell me to get my nut-case friend out of there. But instead, Mike laughed his ass off. Bob did his job, saved them a lot of money, and showed them how to make heavy copper boards.

So, over the years, Bob and I have worked together on a number of projects: developing indestructible boards at Sierra Circuits and Taiyo America, as well as focusing on printed electronics. It has always been an adventure.

I thought it might be fun to challenge Bob by writing a series of columns in which I ask Bob questions about technology and he answers them. We decided to present this to The PCB Design Magazine, because designers are always on the lookout for information about PCBs, from the very basics to bleeding-edge technology. Best of all, you, the readers, are invited to send Bob questions as well. Maybe we'll all learn something. So I contacted my friend, Editor Andy Shaughnessy, and here we are.

For this first column (and it's a doozy), I asked Bob to talk about something that would shake up the industry. I wanted something really earthshaking, and Bob delivered. Take it away, Bob!

Bob Tarzwell: Under 270 volts, there is no self-arcing, no matter what the spacing! You don't believe me? Check it out.

New information (at least for me, after 50 years in the business) shows that there is no difference in spacing requirements for situations below 270 volts, because 270 volts will not self-arc regardless of spacing. Designer and engineer friends have all been laboring under the same belief as mine: As voltage increased from 5 volts on up, you had to add more spacing to prevent arcs.

This revelation came about through consulting contracts I've had with large companies over the past year. All involved working with trace spacing to help stop PCB assemblies from failing. One big surprise that resulted from my research: Based on physics from Paschen charts and voltage arcing formulas, it is impossible to have a self-generating arc at sea level in normal humidity at less than about 330 volts, and, correspondingly, less than 270 volts in high-altitude applications.

So, all the spacing charts and worry about voltage-based line spacing was incomplete without adding these important environmental conditions to the chart. I researched as many spacing charts as I could, and studied the physics of arcs and corona, leakage, dust and moisture. My findings changed the way I looked at circuit line spacing. The conclusion was that for 95% of PCBs, the line spacing used has almost nothing to do with the circuit operating voltage, but almost 100% with environmental conditions.

Now, I can hear the uproar. "What? No! The IPC charts are the Bible, and we can't think of looking at spacing in any other way."

But the Paschen charts and physics show that it is impossible to generate an arc between two sharp points in normal air at sea level with one millionth of an inch spacing while applying 350 volts. I need not remind you that 350 volts is below the majority of PCB voltages used. So, why do we need spacing charts for less than 350 volts if the voltage is not the cause of shorts and arcs? And why do spacing charts show voltages down to 5 volts?

My conclusion: Over time, we have learned that specific spacing is required to stop PCBs from failing in operation, but I believe we were seeing voltage as the guilty party when moisture, dust, dendrite growth and other environmental conditions are the bad guys in town.

To relate this to another industry, let's look up 5 volts in our PCB design charts. These charts mandate 50 microns of minimum spacing, yet trillions of integrated circuits run at 5 volts with spacings down to 50 nanometers. What's the difference? It comes down to a sealed package that eliminates all environmental conditions vs. an open PCB with moisture-absorbing epoxy with glass fibers, surfaces exposed to moisture, nasty air quality, dust build-up and surface resistance.

One good example for not following the standard spacing charts can be found in a failing flexible circuit in a kitchen appliance. In this case, the designer followed the spacing rules and added more spacing for safety. The circuit was a trace of more than 20 volts and a ground trace at .075" spacing between traces with solder mask. This circuit was failing in large numbers, and I was hired to find out why. Research showed it was excessive moisture on the flex causing dendrite growth right under the solder mask, causing shorting between the two traces. The standard spacing charts failed to address higher moisture situations with silver ink.

To fix the spacing information problem, we need more spacing variables, different charts for specified conditions, because a single voltage spacing chart with a few simple environmental conditions cannot even come close to properly relating to all situations that PCB designers and engineers may encounter.

Shameless plug: My soon-to-be-released e-Book will provide new information about spacing requirements and voltage, as well as more new information on PCB design and manufacturing for increased reliability. It should be available soon at www.dmrpcb.com.

Dan and I will have more information in upcoming issues, so stay tuned. **PCBDESIGN**

Bob Tarzwell is a PCB consultant who has spent 50 years in the PCB industry, inventing technology and building almost every type of PCB. He is the co-owner of DB Publishing, the publisher of the PCB 101 and Quality 101 handbooks.

Dan Beaulieu is a well-known industry consultant and co-owner of DB Publishing. His column It's Only Common Sense appears Monday mornings in the I-Connect 007 Daily Newsletter. He can be reached at danbbeaulieu@aol.com.

News Highlights from PCBDesign007 this Month

1 Joe Fjelstad Remembers Dieter Bergman

"Sometimes, not often enough, a force of nature graces this planet for a time making it a better place than it would have been without its presence. Dieter Bergman was such a force of nature," writes Joe Fjelstad.

2 Patty Goldman Reflects on the Life of Dieter Bergman

Goldman comments, "I think it probably never occurred to any of us who worked with him that Dieter would ever die. Heck, it was only in the past few years that he even slowed down. So this is sad news indeed."

3 Mentor Graphics Debuts New xDM Product Suite

Mentor Graphics has announced its next offering in the new Xpedition platform, the Xpedition Data Management (xDM) product suite. It provides a flow-wide information hub that manages the PCB design data that is created, reused, imported, or released from the Mentor Graphics Xpedition Enterprise platform.

4 Zuken Boosts Global Competencies in Transportation

Zuken plans to extend its global competencies in transportation and to provide electronic architecture and wiring harness tools to meet the future challenges of OEMs and their suppliers.

5 Cadence Q2 Revenue Rises Year on Year

Cadence reported second quarter 2014 revenue of $379 million, compared to revenue of $362 million reported for the same period in 2013. On a GAAP basis, Cadence recognized net income of $23 million, in the second quarter of 2014, compared to net income of $9 million in the same period in 2013.

6 Exception PCB's Neil Day Awarded CID Certificate

Exception PCB Solutions' Design Manager Neil Day has completed the IPC CID training course and attained CID Certification. Plans are already in place for Neil to complete the CID+ certification and for the other members of the design team to complete their CID training.

7 New CadSoft EAGLE Update Announced

CadSoft Computer has launched Version 7 of its award winning EAGLE PCB software. The update to the popular software brings a modern design environment with increased flexibility, enabling users to develop custom schematics using commercial standard software at a fraction of the cost.

8 Zuken Reports 10.5% Sales Increase in FY 2014

Jinya Katsube, chief operating officer, said, "This has been a good year for Zuken as we significantly surpassed last year's results. Our success has been achieved, in part, by the introduction of CR-8000 Design Force to new and existing customers, and strong acceptance of our data management solution DS-2 and IT solutions such as visual BOM, with a sales increase of 24.4% this year.

9 EDA Industry Rises 4.6% in 1Q14; PCB up 1.6%

According to the EDA Consortium Market Statistics Service, EDA industry revenue increased 4.6% for Q1 2014 to $1.746 billion, compared to $1.668 billion in Q1 2013. But PCB & MCM revenue of $159.7 million lagged, increasing only 1.6% compared to Q1 2013.

10 Cadence Targets Emerging Design Challenges

The new OrCAD products include OrCAD Engineering Data Management (EDM), a comprehensive collaboration and management environment for OrCAD Capture; OrCAD Library Builder, a rapid automated part builder; and OrCAD Documentation Editor, an intelligent, automated PCB documentation environment.

events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out *The PCB Design Magazine's* event calendar.

West Penn Expo & Tech Forum
August 14, 2014
Monroeville, Pennsylvania , USA

IPC Southeast Asia High Reliability Conference
August 20, 2014
Penang, Malaysia

NEPCON South China
August26–28,2014
sHenzHen,CHina

Vietnam Manufacturing Expo
August 27–29, 2014
Hanoi, Vietnam

Electronics Assembly
August 27–29, 2014
Hanoi, Vietnam

Assembly Technology Vietnam
August 27–29, 2014
Hanoi, Vietnam

World Engineering Expo (WEE)
September 1–3, 2014
Singapore

IMTS 2014
September 8–13, 2014
Chicago, Illinois, USA

Capital Expo & Tech Forum
September 9, 2014
Laurel, Maryland, USA

PCB West
September 9-11, 2014
Santa Clara, California, USA

Hybrid & Electric Vehicles Forum 2014
September 17–18, 2014
Munich, Germany

Medical Electronics Symposium 2014
September 18–19, 2014
Portland, Oregon, USA

FUTURA
September 18–21, 2014
Salzburg, Austria

MEDIX Osaka
September 24–26, 2014
Osaka, Japan

SMTA International 2014
September 28–October 2, 2014
Rosemont, Illinois, USA

Standards Development Meetings
September 28–October 2, 2014
Rosemont, Illinois, USA

CEA Innovate!
September 30–October 2, 2014
Phoenix, Arizona, USA

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