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August 2015

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THE WAR ON PROCESS FAILURE

Kelly Dack and Mark Thompson Unite in the War on Failure

by Andy Shaughnessy, page 10

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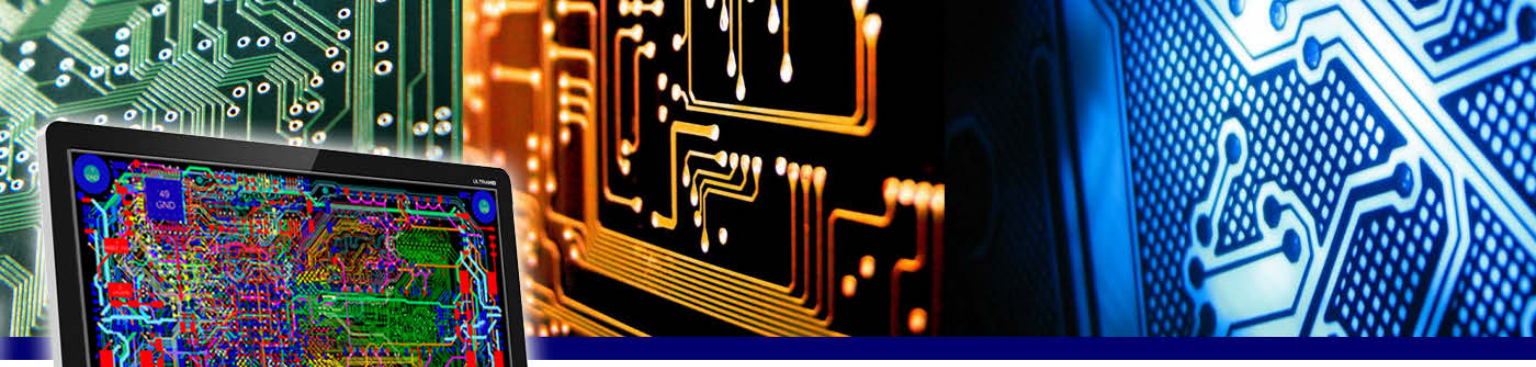

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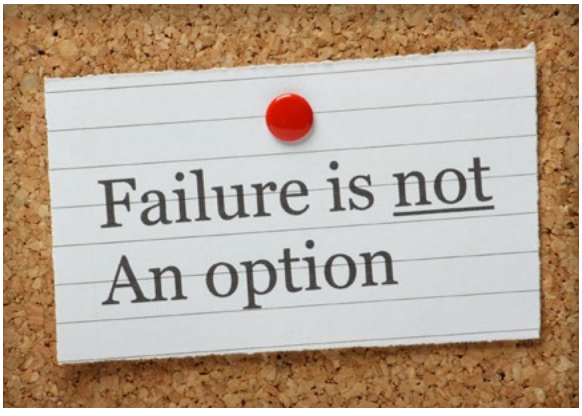
August 2015

This Issue: THE WAR ON PROCESS FAILURE

FEATURED CONTENT

Attention! You may not realize it, but PCB designers are in a veritable war zone, day in and day out. This month, our cover story is an interview with two "soldiers" in this war on failure, Kelly Dack and Mark Thompson of Prototron. We also have feature columns by Paul Reid and Tim Haag, as well as an interview with Per Viklund and Alex Caravajal of Mentor Graphics.

FEATURE COLUMNS



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Df @ 10 GHz	0.0028 - 0.0036	0.0028, 0.0031 & 0.0034	0.0031*	0.0030*	0.0017
CTE Z-axis (50 to 260°C)	2.90%	2.80%	2.80%	2.90%	2.90%
T-260 & T-288	>60	>60	>60	>60	>60
Halogen free	No	No	No	Yes	No
VLP-2 (2 micron Rz copper)	Available	Available	Available	Standard	Standard
Stable Dk & Df over the temperature range	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C	-40°C to +140°C
Optimized global constructions for Pb-free assembly	Yes	Yes	Yes	Yes	Yes
Compatible with other Isola products for hybrid designs	For use in double-sided applications	Yes	Yes	Yes	Yes
Low PIM < -155 dBc	Yes	Yes	Yes	Yes	Yes

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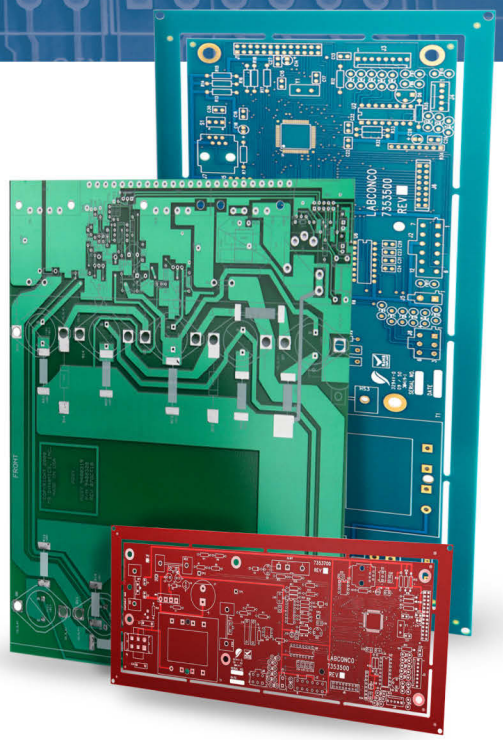

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Fighting the War on Failure

by Andy Shaughnessy
I-CONNECT007

In this issue, we focus on the "War on Failure," a war that your company is likely already prosecuting. The big question is this: Can we ever win this war?

No one in this industry sets out to fail, except failure analysis test engineers. But failure is a part of life for designers and manufacturers of electronics. Our reader surveys show that failure affects nearly everyone in the PCB industry: designers, fabricators, assembly providers, OEMs, and suppliers.

And failure itself is difficult to define; everyone has a different definition.

Even the meaning of "failure" seems to evolve over time. Think about this: The PCB design process of the past would be considered a failure today. Decades ago, many PCB designs went through multiple design iterations and board re-spins. No one labeled those actions as failures; it's just the way the process worked back then.

There was no hand-wringing about it, no post-mortem meetings full of downcast faces, wondering what went wrong. That was the accepted practice. I bet design managers included these multiple steps in their department's flow charts.

Multiple iterations and board re-spins weren't an issue until price and time-to-market made them an issue. Once high-speed PCBs became the norm, doing redesigns and building prototype after prototype was no longer financially feasible. Design teams began using simulation and analysis, the "right the first time" movement took off, and now we look at the old way as a failure.

The same holds true for PCB fabrication and assembly providers. The scrap rates of the past would run a company out of business today. Now, manufacturers are adopting processes like Lean and Six Sigma to help eliminate as much waste as humanly possible. Six Sigma's 99.997% rate of perfection is no longer considered an unattainable dream.

What Does Failure Mean to You?

That was one of the first questions I posed in our cover story interview, "Kelly Dack and Mark Thompson Unite in the War on Failure." Kelly and Mark come from design and CAM backgrounds, respectively, and they've teamed up in this ongoing battle. In this interview, they discuss their definition of failure, some of the more common failures they see from their perspectives, and a variety of ways to keep failures to a minimum. But as they point out, we'll probably never eliminate failure completely from the PCB industry.

Paul Reid's feature column, "Failure Mode: Hole Wall Pullaway," details how stress-relieving and stress-inducing HWPA can cause copper plating in a plated through-hole to be pulled away from the dielectric of the hole wall. As usual, Paul brought along a few of his super cool cross-section animations that show these defects as they happen.

In Tim Haag's feature column, "Failure May Not be an Option, But Sometimes it's a Reality," he discusses some of the mistakes, miscues, and missteps that are common among PCB designers. Working off the famous line by Ed Harris' character in Apollo 13, "Failure is not an option," Tim explores everything from not using all of your EDA tool's inherent capabilities to using far too much automation.

In "Mentor Graphics Helps Bridge Gap between PCB and RF," Barry Matties interviews Per Viklund, director of IC packaging and RF product lines for Mentor, and Business Development Manager Alex Caravajal. Per and Alex explain how Mentor is helping bring together the RF and PCB design worlds, and their plans to accelerate the RF design cycle.

We also bring you the latest in columnist Barry Olney's continuing series, "Stackup Planning, Part 3." This month, Barry looks into

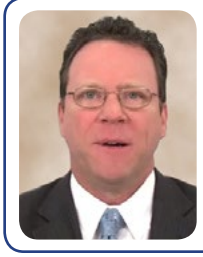
stackup configurations for high layer-count, high-speed PCBs, with some stackup tricks for eight-layer designs.

Columnist John Coonrod offers a "Brief Overview of High-Frequency Laminates," explaining their moisture absorption challenges, thermal properties, and thickness control. He also addresses the use of special fillers to achieve good CTE values and greater stability.

DfR Solutions' Tom O'Connor offers an update on the ongoing shortage of engineers graduating in North America in "Training the Next-Generation Engineer: When Does it Begin and End?" Tom focuses on the efforts to attract more smart young students to the STEM disciplines, and the need to jump-start these efforts right now, before it's too late.

This month, our sister magazines The PCB Magazine and SMT Magazine also focus on the war on failure from their perspectives, so don't forget to check them out.

I'll see you next month, when we devote the September issue to automotive electronic design. Enjoy the last of your summer—show time is around the corner! **PCBDESIGN**



Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 16 years. He can be reached by clicking here.

Kelly Dack and Mark Thompson Unite in the War on Failure

by Andy Shaughnessy
PCBDESIGN007

There's been a lot of talk about fighting the war on failure in the PCB industry. But what strategies should our generals follow to prosecute this war? What exactly constitutes a failure in the first place? Is this war even winnable? I recently spoke with longtime designer Kelly Dack and CAM support veteran Mark Thompson of Prototron Circuits about the best battle plans for beating failure, and why designers and manufacturers must team up against this common enemy.

Andy Shaughnessy: *Kelly, you recently said, "Failure wins when it leverages the guerrilla warfare tactic of divide and conquer to confuse and disorient the product development community. Designers and manufacturers must unite to fight this war."*

Why don't you start off by saying what failure means to each of you at the design stage and at the board shop stage?

Kelly Dack: Andy, failure is defined as not meeting the intended objective. But I think the concept is easily confused if coming from isolated design and manufacturing perspectives. Meeting the intended objective successfully can only come from allied efforts. Designers need to describe or define objectives for their projects in terms of concise orders in order to make successful products, but this will only come about if the folks giving orders are also able to follow orders.

Mark Thompson: Absolutely, I agree with Kelly entirely. I'd say from the fabrication side, following orders is easy if the orders are given from time-proven, industry standard speci-

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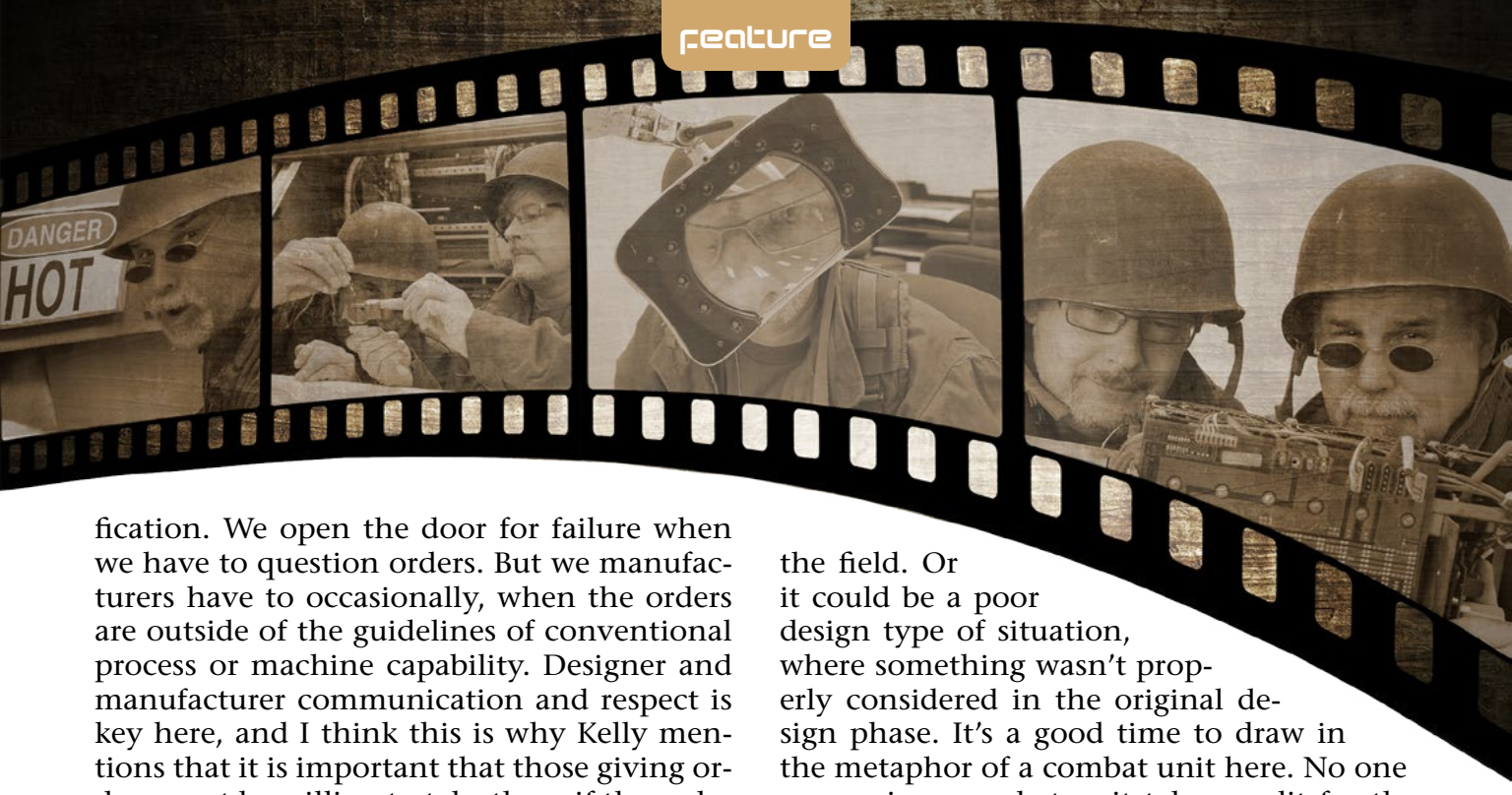

fication. We open the door for failure when we have to question orders. But we manufacturers have to occasionally, when the orders are outside of the guidelines of conventional process or machine capability. Designer and manufacturer communication and respect is key here, and I think this is why Kelly mentions that it is important that those giving orders must be willing to take them if the order would put the part at risk of failure.

Shaughnessy: ***Is failure always someone's fault or is it the fault of a bad process, or is it a combination of both?***

Dack: I'm not comfortable pointing fingers at individuals. The causes for success and failure can be attributed to people, but it can also be caused by unforeseen conditions or even acts of God. A good strategy is to identify performance requirements and operating conditions. The "battle plan" needs to identify constraints: design constraints, manufacturing constraints, performance constraints, even cost constraints. Knowing the enemy and anticipating every possible way a design could possibly fail is crucial, but it can't happen in a vacuum. It must occur through open communication with the allies – stakeholders of the product who are connected through the process steps.

Thompson: If you're asking if every failure is someone's fault, I would say yes, at the most base level. It will always turn out to be someone's fault either due to negligence or lack of vigilance. But, as Kelly said, there are extenuating circumstances. There can be dynamic situations where environmental, human or mechanical conditions create a failure in the field. Or it could be a poor design type of situation, where something wasn't properly considered in the original design phase. It's a good time to draw in the metaphor of a combat unit here. No one person in a combat unit takes credit for the unit's success or failure. They are a team!

Dack: Oh, yes. I like that analogy! A combat unit trains and rehearses their craft to work with other units successfully on the battlefield. A big part of their success is adherence to standards. Standard equipment, weapons and communication is so important! Without standards, orders are non-effective SNAFU. Mentioning standards at this point at least helps to move the question from who failed to how it failed, which is much more important from a process perspective.

Shaughnessy: ***In your positions, you've both had the experience of seeing a lot of things fail over the years. I wonder if you guys can talk about some of the more prevalent types of failures that you've seen in design and fab. By the way, in our recent survey, we asked our design readers what they thought was the No. 1 cause of failure in the field. A good chunk of the readers said, "Solder joint failure," and an equal number said, "Bad design techniques."***

Thompson: I think the survey results are telling. When you ask about what are some of the more common failures in design and fab, and you find that the results vary from bad design to solder failure with a good smattering of both, that really tells you something

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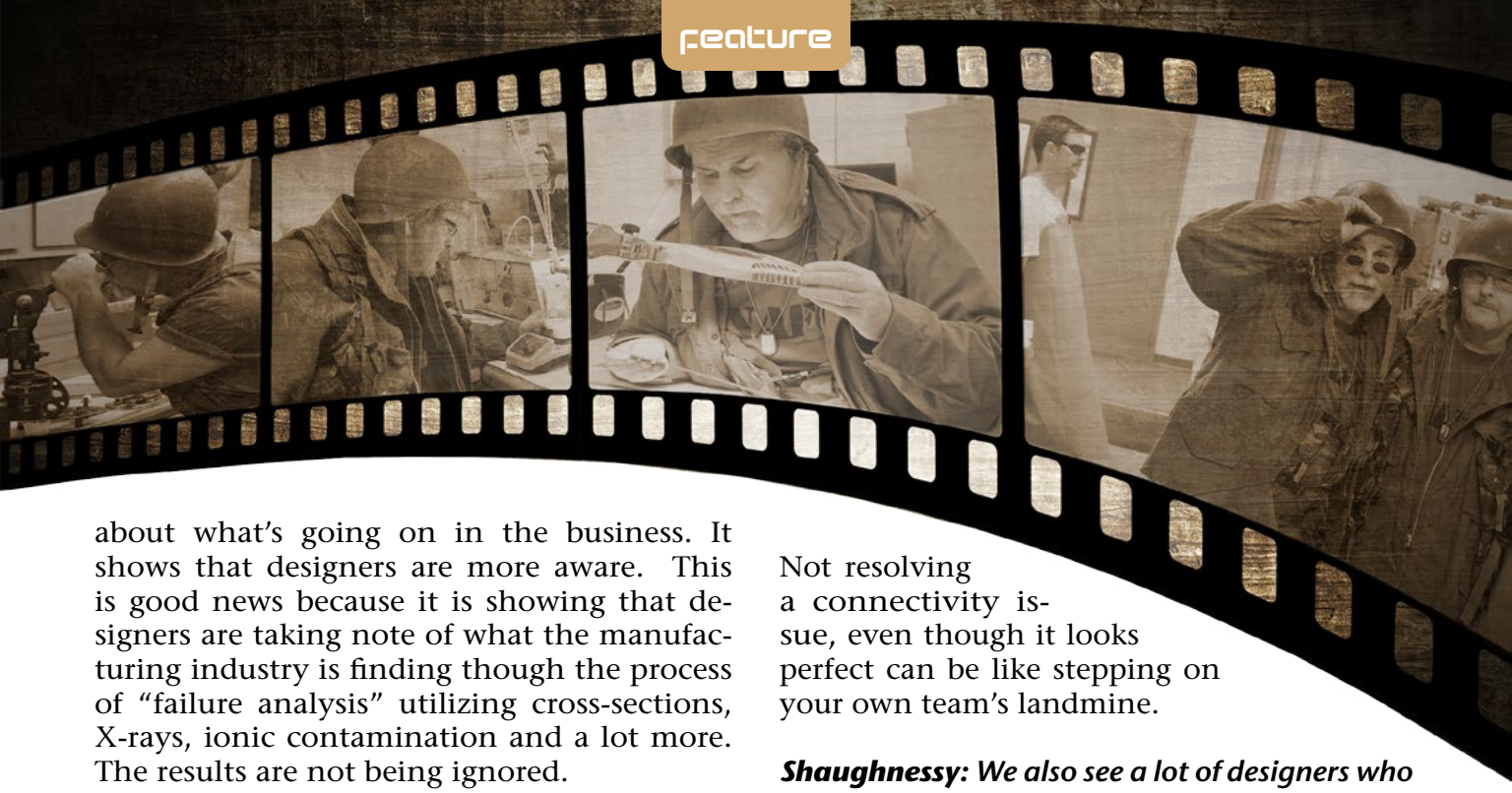


about what's going on in the business. It shows that designers are more aware. This is good news because it is showing that designers are taking note of what the manufacturing industry is finding though the process of "failure analysis" utilizing cross-sections, X-rays, ionic contamination and a lot more. The results are not being ignored.

Dack: On the front-end, the cause of many common failures can easily be caught by checking. There are so many failures that can be attributed to poor design checking. Discontinuity between the schematic and netlist in the layout; failure to edit nodes properly; forgetting to change a solder mask color; forgetting to flood a power plane could cause a huge failure. But a lot of these common problems are easily prevented by a check process.

Thompson: I definitely agree. I see that people are making more progress in this respect. A lot of our customers, for instance, are now supplying an IPC netlist when they didn't in the past. This form of communication helps our war on failure by comparing the design connectivity orders with exported, graphical Gerber data orders prior to making any edits whatsoever. So, let's bring in another military metaphor: friendly fire. A lot of people, when they're brand new at generating netlists, will do silly things like assign fiducials as net points or non-plated holes as net points. Some do not realize that the design may have half-plated pads at the part edge that are creating a connection with a metal post at some point later in its life. Having to interpret and resolve design dicontinuities without a code talker, is like dodging friendly fire. Not resolving a connectivity issue, even though it looks perfect can be like stepping on your own team's landmine.

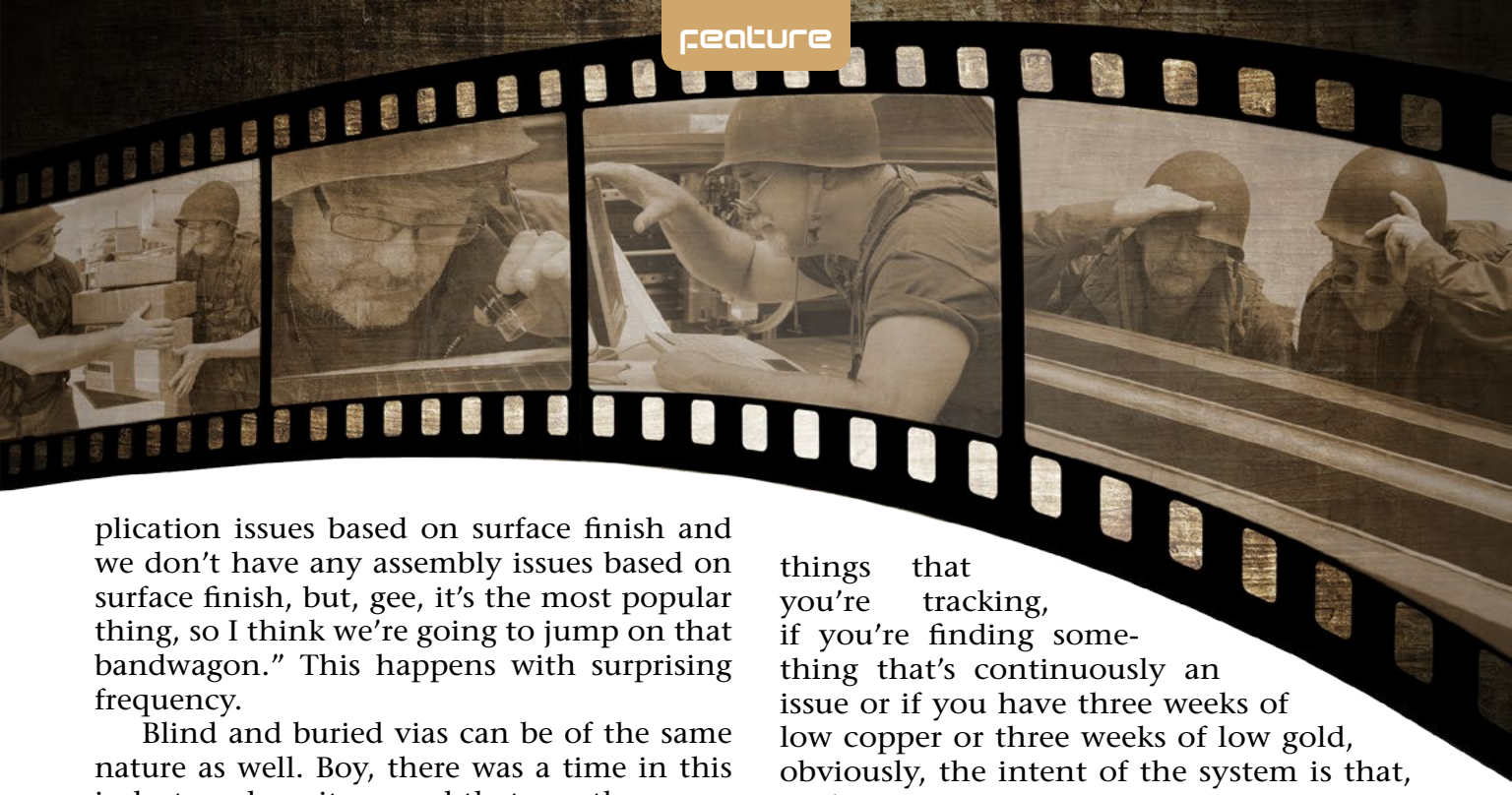
Shaughnessy: ***We also see a lot of designers who are over-constraining their designs and making them too high-tech.***

Thompson: Absolutely. Many people rope themselves in with these specifications. I've seen so many drawings that will call out very specific material types, very specific dielectric values and even very specific dielectric constants. This is really a problem. If you go to shop X, they may have a flavor of 4101/126 that has a different dielectric constant, a different environmental condition, and a different lamination process and parameter that's different from shop X, shop Y, and shop Z, all the way down the road. If you make a drawing and you roped yourself into a specific material type or a specific dielectric constant, you're really doing yourself a disservice.

Dack: What Mark is talking about is overspecifying. Overspecifying can cause failure at the front-end manufacturing process by limiting sources who can manufacture the part.

Thompson: Kelly and I did a tour yesterday and we brought up that very point. We were talking about how sometimes people go on a tangent because it's the new thing to do.

I hear customers saying, "We have to have ENEPIG because we have to have ENEPIG. We don't really care about the surface finish. We don't have any constraints or ap-



plication issues based on surface finish and we don't have any assembly issues based on surface finish, but, gee, it's the most popular thing, so I think we're going to jump on that bandwagon." This happens with surprising frequency.

Blind and buried vias can be of the same nature as well. Boy, there was a time in this industry where it seemed that was the vogue way of dealing with tight-pitch areas and breaking out of very fine-pitched land patterns. The "only" solutions were blinds and burieds. Now, people are realizing, "Well, that's not necessarily true." Now, we can have the best of all worlds on the same board and still be able to deal with fabrication constraints. They don't have to go down to the absolutely crazy 2x2 mil design pitch limiting them to only a very few manufacturers here in the United States.

***Shaughnessy:** So, how do we prevent failure? Does it start with communication?*

Dack: Yeah, most definitely. As design and manufacturing allies, we need to provide a united front against failure. This needs to be done through communication, with everyone speaking the same code. Our communication vehicles are design data, documentation along with manufacturing and inspection data. These are the only proven methods to check and verify our manufacturing result meets our design intent.

Thompson: I think, very simply, it comes down to due diligence and continuous quality improvement. As you evolve in your continuous quality improvement plan, one would hope that any violations or consistent things that you're tracking, if you're finding something that's continuously an issue or if you have three weeks of low copper or three weeks of low gold, obviously, the intent of the system is that, at that point, you can issue a corrective action, permanently correct that and then move forward.

Ultimately, what we're looking for when we're talking about charting and tracking these things is, if I could look at a year's worth of data and everything was very sporadic and few and far between, I'd say we're probably doing pretty well with our quality system. If I have three weeks of the same type of anomaly, clearly we have some issues.

Dack: Mark comes from a manufacturing background. I'm always very impressed by manufacturers and the data that they keep regarding their processes. If a failure occurs, a manufacturer is expected to be able to point to their travelers and inspection reports and tell a customer exactly where and how the failure occurred. I think we as designers need to take note the next time we request that corrective action report. Do designers have design processes in place where we check and verify that our design and layout meets the intended design constraints and design specifications? Do we check for those before we ever send design data to the manufacturer? If we don't, isn't that a lot like being really good at giving orders without being able to take them?

I'd like to give a nod to a wonderful group manager I worked for over the past couple

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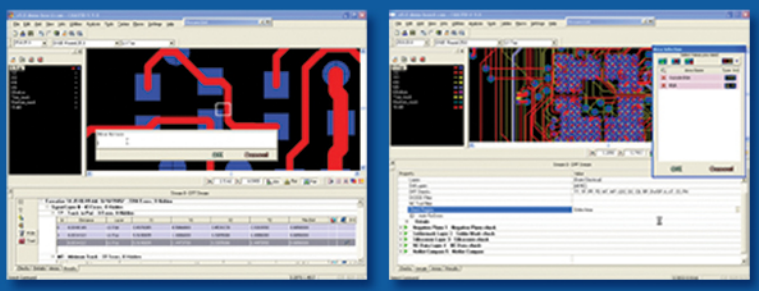

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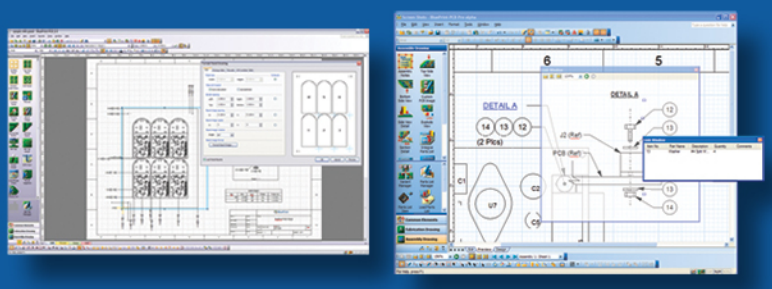

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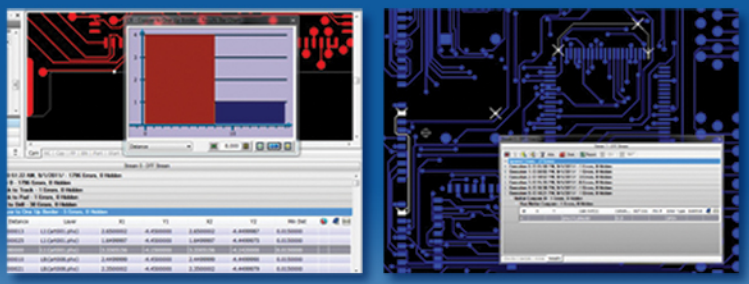

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of years at IGT in Reno, Mark Taylor. He's a four-star general in the war on failure. He introduced our PCB design workgroup to a book by Franklin Covey called "The 4 Disciplines of Execution," or the 4DX Methodology. Our group had a really extensive checklist that was so long and time-consuming it was rarely being used. Needless to say, design problems found their way onto our manufacturing assembly line. For a good year, our assembly folks tracked these errors and many more. But without an ally, the data was useless. Mark suggested we solve our ineffective checklist problem by formulating a new one based on the data collected by the assembly group. His leadership and 4DX skills helped us to win this battle. As the designers and assemblers allied together to eliminate designer induced failure, they found only five major show-stoppers that were slipping through the design process. The designers revamped their checklist to check for only those five things, kept score with the assembly team, and met each week to report on progress. Victory against failure was won in this case, by great leadership and team alliance.

***Shaughnessy:** Is it all about process control? Is that the key?*

Thompson: Yes, at all levels. Process control at the design and engineering phases all the way through to fabrication and assembly. As a designer or a company going to fabrication, are you sometimes giving them too much? Is there too much for them to deal with? Are there too many caveats? Is everything 3x3, and does it need to be? Were you just ingressing and egressing out of a fine pitch part and then, all of a sudden, you decided to run the remainder of the board at 3x3?

That's where the proof is in the pudding. That's when, ultimately, your design goes into the product and they do the initial product testing and you have to go through your first set of revisions. That's when you're really starting to see what sorts of things you need to address through that process. Certainly, there are process issues on the fabrication level. They happen all the time, anything from, as you said, solder failures at an assembly due to low copper barrel cracking, heat considerations, etc. Any number of things can happen in a fabrication environment that could affect the actual physical board.

One example that we talk about in our facility tours is how various fabricators could do the customer a disservice. Let's say you've got an impedance control job and you're at the initial testing phase and you're running high. You're running at 55 or 56 ohms for 50 ohms, so you're just out of tolerance. Now, your solder mask guy is going to say, "Give me those boards back. I can throw another coat on that and I can take it back down to 50 ohms." That is true. Now, the board comes through as another rev, it's the same impedance, and you build it right this time. You have no etching issues and you don't have to put a second coat on it.

The customer has two sets of boards in their hands. They both meet 50 ohms performance, but they have slightly different performance characteristics. Why? Because the shop played that little trick. Again, you need to be diligent about that kind of stuff. How do we do that? Mainly through site

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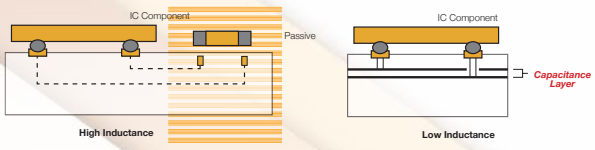

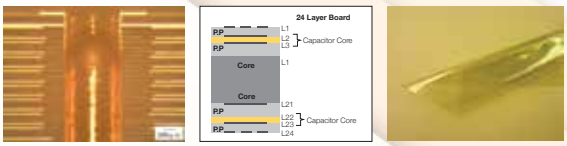

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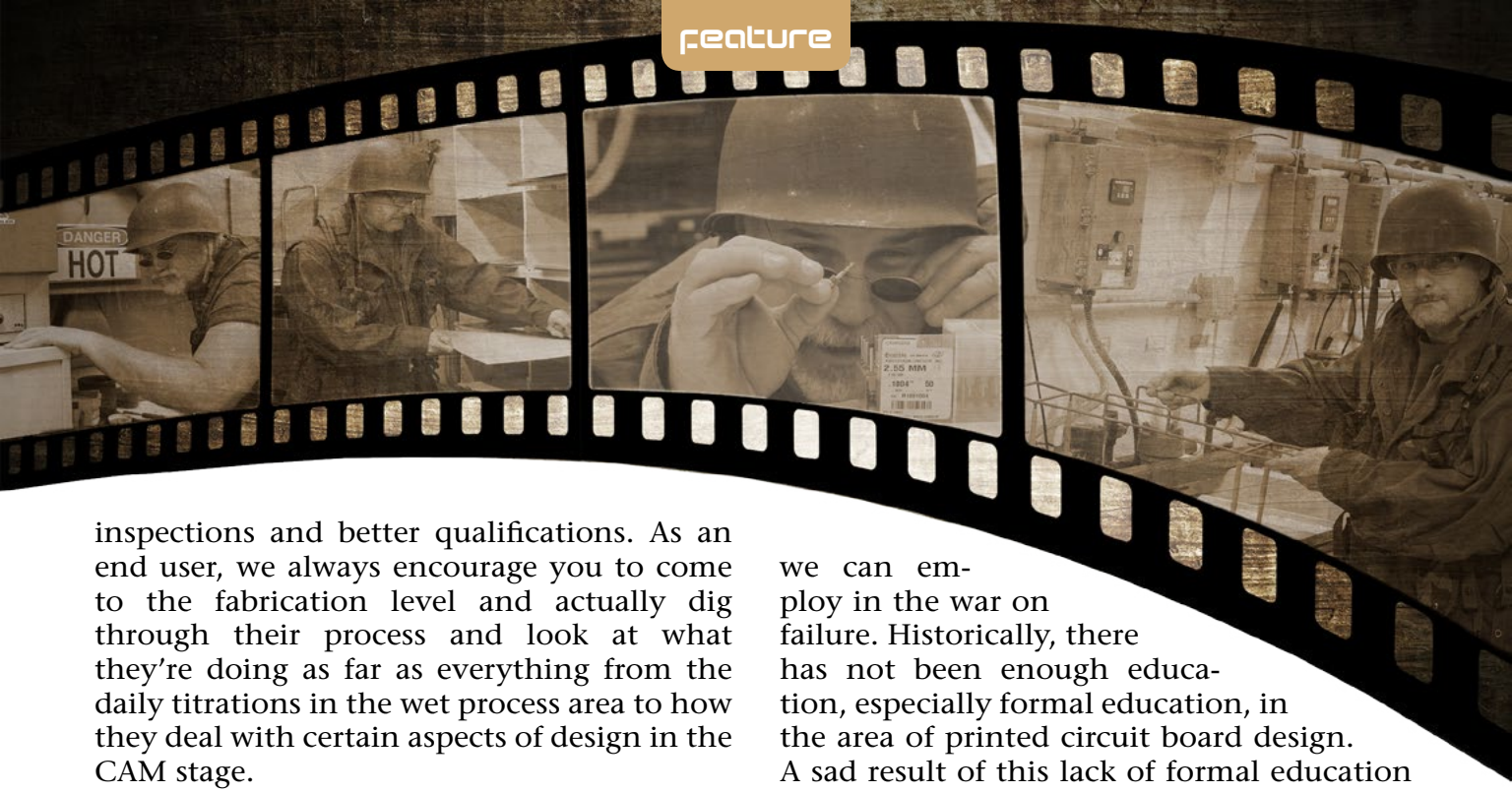

inspections and better qualifications. As an end user, we always encourage you to come to the fabrication level and actually dig through their process and look at what they're doing as far as everything from the daily titrations in the wet process area to how they deal with certain aspects of design in the CAM stage.

Shaughnessy: *It's funny you mentioned site visits. I ask designers all the time when they last visited a board shop. About half of them say, "20 years ago," and the rest say, "Never."*

Thompson: It's been too long. The gentleman we had in yesterday for a tour is a great example. He's an old dog, an owner of four local companies that we've built boards for all these years. He came in and he'd never been on a tour. At the end of the tour, he said to me, "You know, things haven't really changed in the last 20 years. It's the way you deal with them." That was a very critical statement. That's absolutely true. How do we deal with defined geometries, 0.1 millimeter lines and spaces? Everything five years ago was 8x8 and dealing with 14 mil holes. There was a whole lot of tolerance involved. Now, you have so much less tolerance.

Shaughnessy: *Right. Are you seeing that people seem to be a little more educated now because there are so many classes and webinars and seminars and all these things that are available in design and manufacturing? Are you seeing that people are a little more informed now than they used to be?*

Dack: Education—or metaphorically, intelligence—is one of the defense strategies that we can employ in the war on failure. Historically, there has not been enough education, especially formal education, in the area of printed circuit board design. A sad result of this lack of formal education is designer failure due to intellectual inbreeding within a company culture. This happens in an engineering department when "good ol' boy knowledge" is passed on from designer to designer with a process methodology of "that's the way we've always done it." Well, the technology is changing fast and without outside knowledge about how everyone else is doing it, good ol' boys will not keep up! Designers are doomed to fail if they design in a vacuum.

In the war on failure, communication and education are critical. There are many sources for education that have evolved and have come about over the years. IPC has been key in educating and organizing designers in the ways of process, design and manufacturing specification through the Designers Council. There are training companies which exist — like the widely known EPTAC organization, who is in the business of training and certification in the areas of these specifications, including designer certification or CID.

Shaughnessy: *It's also a good networking opportunity to go to any of these conferences like DesignCon, PCB West or the design forum at APEX.*

Thompson: Absolutely, we've seen huge value in the things like Kelly was talking about, like IPC's Certified Interconnect Designer

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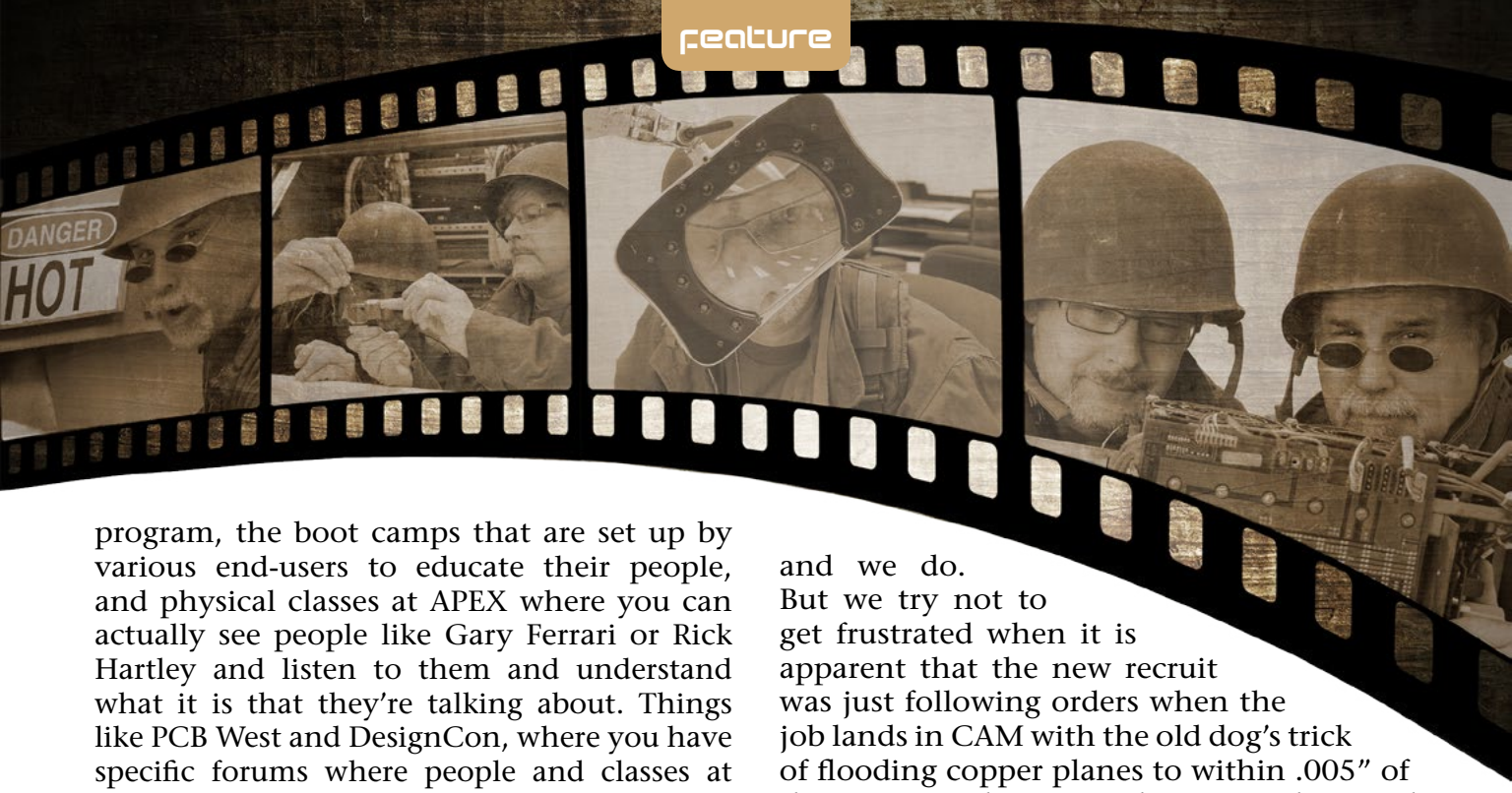

program, the boot camps that are set up by various end-users to educate their people, and physical classes at APEX where you can actually see people like Gary Ferrari or Rick Hartley and listen to them and understand what it is that they're talking about. Things like PCB West and DesignCon, where you have specific forums where people and classes at those shows deal with this kind of stuff.

I would also add things like my blog "The Bare Board Truth" on LinkedIn, our very own LinkedIn forum that is used for networking, and also your local IPC Designers Council. We highly encourage anybody to get an IPC Designers Council started in their area because, at some point, it takes on a life of its own, and problem solving is within the group. It's very, very helpful and certainly mitigates failure.

Shaughnessy: *I guess the war on failure, from our standpoint, is never really over, is it? I mean, you're not going to win the war, but you can manage it.*

Thompson: The fact that we've got some new people in the industry and there are training issues at that level is certainly part of this. Let's not forget that right now, in our industry, we're looking at a lot of young fresh, recruits. Young EEs from the universities. Some of them are starting with large design bureaus and being mentored by old dogs who have methodologies from old times. I can't tell you how many times a new recruit will call and say, "I've got an 8-layer board. I want impedances on layers 1, 3, 6 and 8. They're 50 & 100 ohms. Send me your calculations and send me a stack up." Now, we are glad to send the stackup based on the orders given, and we do. But we try not to get frustrated when it is apparent that the new recruit was just following orders when the job lands in CAM with the old dog's trick of flooding copper planes to within .005" of the traces, inducing coplanar coupling and messing up all of our given stackup calculations. So we manage the war first by showing respect to our veterans. If they will listen, we take every opportunity to give them the information they need to be able to continue with their board.

Dack: It's a great topic. The war on failure has so many metaphors relating to design and manufacturing. What we are about are our defense strategies. Like we said before, failure wins only if the allied strategies of communication and education obliterate the axis tactics of division and isolation in the design and manufacturing cultures.

Shaughnessy: *At least if the designers communicate with fabricators and with the assembly guys, and if everybody communicates, you may not eliminate all the failures, but you'll certainly be able to manage it better.*

Dack: The war on failure is inevitable because failure will not relent. Failure is a force.

Thompson: Losing the war on failure is not healthy for designers, manufacturers and other living things.

Shaughnessy: *All right. Thanks so much for joining me today guys.* **PCBDESIGN**

Failure Mode: Hole Wall Pullaway

by Paul Reid
CONSULTANT

Hole wall pullaway (HWPA) is an insidious defect that is not usually a cause of electrical failure. What happens with HWPA is that the copper plating in a plated through-hole (PTH) is pulled away from the dielectric of the drilled hole wall. The hole must not be filled with any sort of a hole fill in order to see HWPA.

There are two distinct types of HWPA: stress-relieving and stress-inducing. In stress-relieving HWPA, the condition appears to distress the PTH, allowing it to survive hundreds or thousands of thermal cycles without failure. In stress-inducing HWPA, the stress appears to greatly increase, causing the PTH to fail in just a few thermal cycles. What we consider a failure is an increase greater than 10% in the overall resistance in the circuit. A crack that partially bridges the copper at the internal interface is enough to cause a failure.

This column is based on my experience in test reliability of interconnect stress test (IST) coupons. I am addressing HWPA that has moderate to severe outgassing. There may be HWPA due to thermal stressing of the board without any significant outgassing, but this type of HWPA is subtle, and it presents as a dark line between the plating and the dielectric of the hole wall. This type of HWPA is rarely detected.

Stress-Relieving HWPA

Stress-relieving is the most common type of HWPA. It appears that the adhesion of copper plating to the dielectric is reduced most likely due to problems with the application of electroless copper plating adhering to the dielectric of the hole wall. At the same time, the adhesion is strong at the copper's internal interconnection. In fact, experience suggests that the adhesion of the electroless copper is stronger than the copper plating. This process frequently produces strong interconnections to copper inner layers.

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FAILURE MODE: HOLE WALL PULLAWAY *continues*

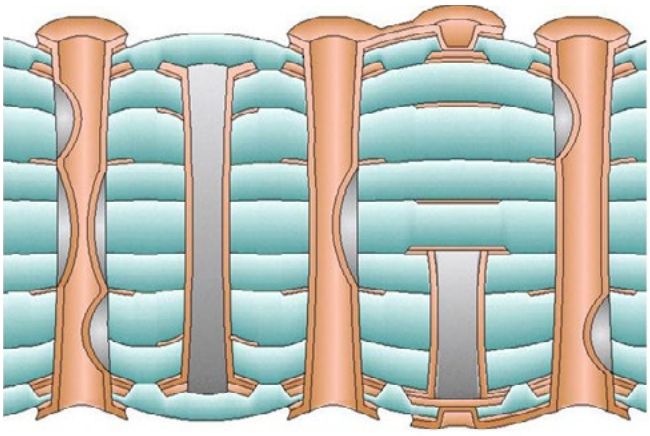

Figure 1: Graphic of stress-relieving HWPA.

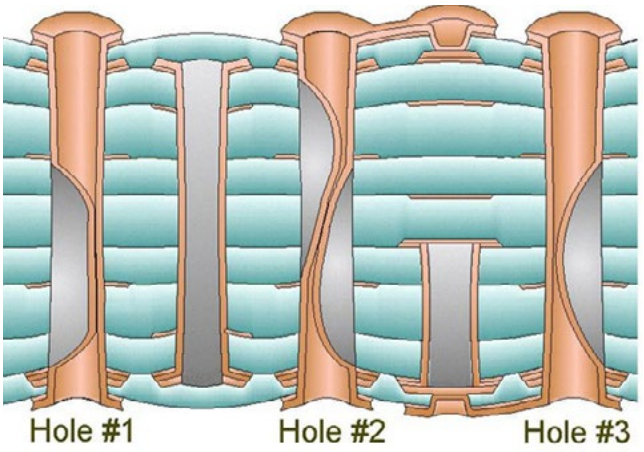

Figure 2: Graphic of stress-inducing HWPA.

This condition may result in a hole wall that looks like a stack of forward or backward "Ds" running the length of the hole where the top and the bottom of the "Ds" is at a internal interconnect (Figure 1).

I have tested holes with HWPA that have survived for thousands of thermal cycles tested from ambient to 150°C. It appears that 99% of the time this HWPA stress relieves the copper plating in the PTH, making the hole more robust to thermal cycling types of failures.

Now, when I say that HWPA stress relieves the copper plating in the PTH, thus making the hole more robust to thermal cycling types of failures, what I mean is this: When the samples are tested and the thermal cycles to failure are compared, coupons with HWPA typically outperform coupons without HWPA. This is with coupons that are from the same process that happen to have HWPA vs. those without HWPA. It appears that the coupons without HWPA have wear-out failures, while those with HWPA don't succumb to wear-out type of failures. What I think happens is that the majority of the wear-out failures propagate from a glass fiber. The crack forms slowly, starting from a glass fiber, and works its way across the copper of the barrel, with each successive thermal cycle. With HWPA we do not have the glass fibers constrained in the copper and the hole wall is free to expand and contract without encumbrances, and because of this no wear-out type of failures ensue.

Stress-Inducing HWPA

We rarely see HWPA cause an electrical failure, but on occasion this condition may cause a catastrophic failure. I call this condition stress-inducing HWPA. If it is severe enough the HWPA may put enough stress on the interconnect to cause it to pull away from the copper plating in the hole. The result is a break between the internal interconnection and plating in the hole. A crack develops between the internal interconnection and the copper plating that widens in to an open. On this rare occasion, the bond is weak between the internal interconnection and the copper plating of the hole wall, or there is extreme out-gassing that causes the internal interface to crack. When HWPA is severe, it usually goes open within 100 thermal cycles.

Note that in the graphic of stress-inducing HWPA the copper in the hole wall is not deformed uniformly. In hole No. 1, the pullaway is from the wall on the left side of the hole and bridges the gap so that it is pressed against the right side of the hole. In hole No. 2, the deformation is equal from both sides and in hole No. 3, the right side of the hole is deformed to touch the left side of the hole. The question becomes, what is going on in this section? To understand what was happening, we decided to do a horizontal cross-section.

What we found was surprising. The hole walls were deformed into three or four cusps. It appeared that the three or four cusps roughly aligned with the wrap or weft of the glass bun-

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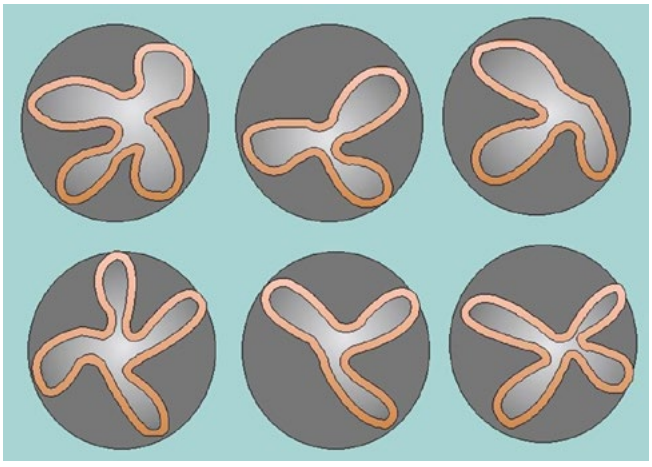

Figure 3: Horizontal cross-section of stress-inducing HWPA.

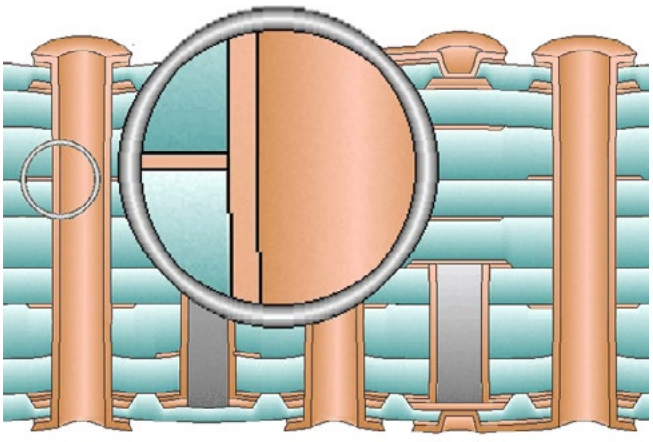

Figure 4: Animation depicting stress-relieving HWPA. Click to view animation.

dles. The angle of the grind would determine what was presented in the cross-section.

I once experienced this type of out-gassing. When I worked for a board shop in New England (which will not be named), we had a special team that was supposed to move critical orders through the shop quickly. The team had a critical job, but they wanted to go to lunch when the boards were in the middle of the wet process line. They figured that it would be all right to hold the board in the sulfuric acid bath while they went to lunch. They were gone about an hour.

This worked well for the copper because a mixture of sulfuric acid can reduce copper oxide and will not attach metal copper, but it was not so good for the dielectric. The team returned and finished the process. The next day the boards were delivered to the customer. During assembly, they noticed that when the boards were soldered, a geyser of white smoke would push up through the solder and continue to smoke for as long as the soldering iron was applied to the hole. I'll never forget this condition because, under a microscope, these holes looked like little erupting volcanos.

The two animations in Figures 4 and 5 depict both types of HWPA. Figure 4 shows a stress-relieving HWPA forming. Please note that the outgassing is not as severe in this type of HWPA and the coupons survived for hundreds of thermal cycles.

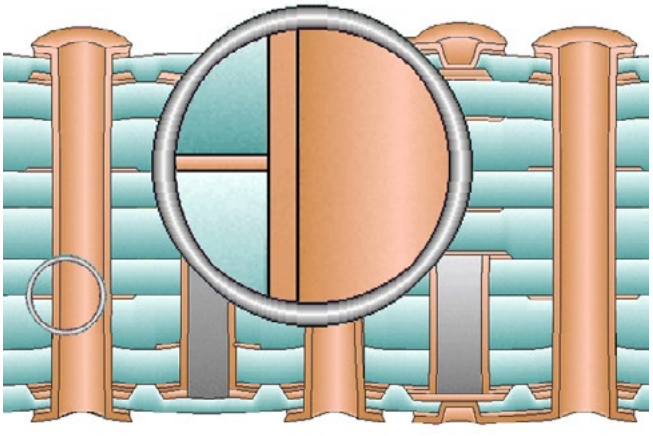

Figure 5: Animation showing out-gassing due to stress-inducing HWPA. Click to view animation.

The animation in Figure 5 shows the severe out-gassing of stress-inducing HWPA. The hole wall is deformed to the point that the copper is pushed all the way to the other side of the hole. The failure is an interconnect type of failure. These coupons failed in fewer than 100 thermal cycles. **PCBDESIGN**

Paul Reid is retired, but open to suggestions. To contact him, click here.

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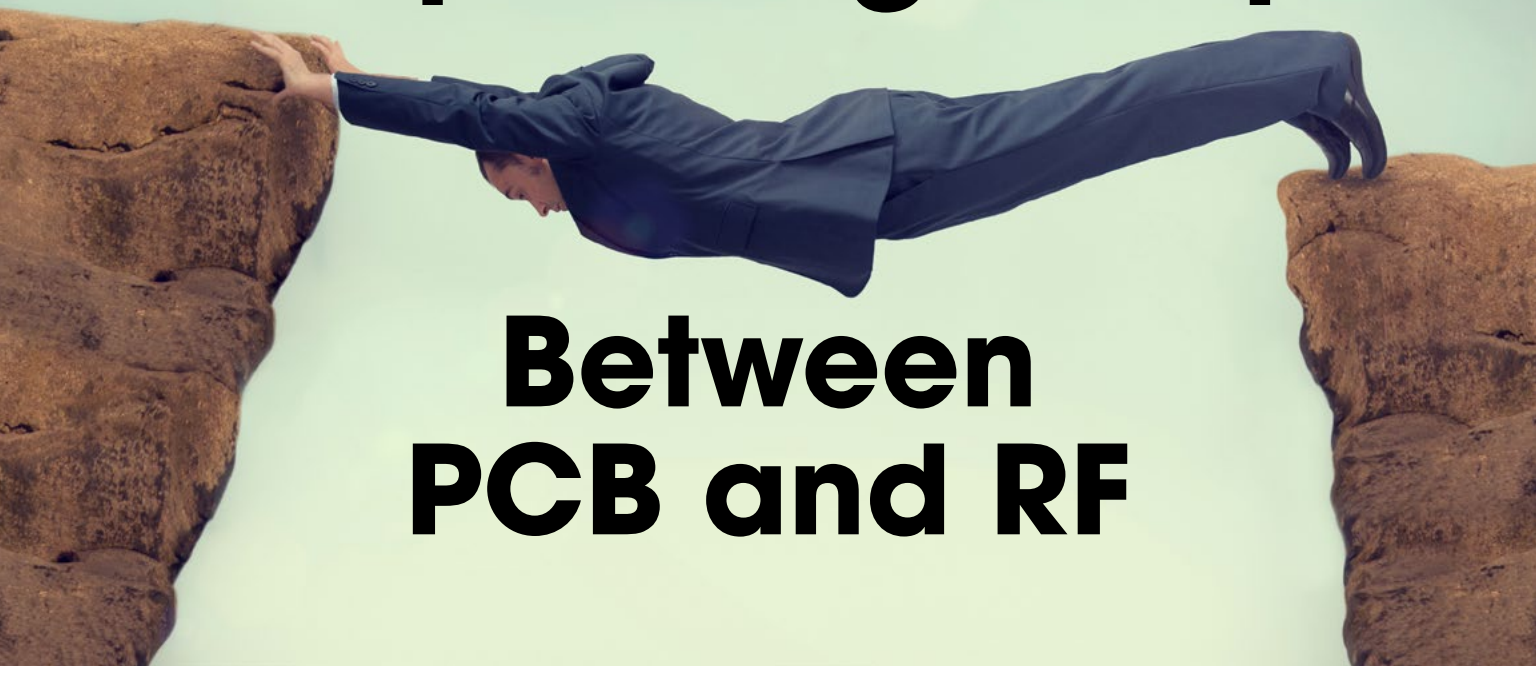


by Barry Matties
I-CONNECT007

I recently attended IMS 2015, a show that focuses primarily on RF and microwave technology. During the show, I met with Per Viklund, the director of IC packaging and RF product lines at Mentor Graphics, and Alex Caravajal, business development manager with Mentor Graphics. We talked about the challenges facing PCB designers working with RF and microwave technology, and Mentor's efforts to help reduce the RF design cycle time.

Barry Matties: *Per, please begin by giving a quick overview of what Mentor Graphics is featuring here at IMS.*

Per Viklund: Specifically for this show, we're focusing on the RF. Our customers have told us for a long time that it takes too long to develop RF circuits, especially when RF is going to be a piece of a bigger system. It's not so often that RF engineers have told us that. It's the PC board integrators who receive the RF circuit for integration and the management who sees long engineering times, lots of re-spins, that clearly says it can't be real to have these long cycles, or it can't be correct to have to do five or six iterations. There's got to be a different way. Not often will the entire engineering organization admit that there is a better way.

Matties: *When we talk about cycles, what sort of cycle times are we talking about?*

Viklund: It could be different depending on if you're doing a simple project or a larger one. But we have some cycle times that can be over two months long, say, if you are doing a board for a satellite communication link or something like that. They could have very long cycles.

***Matties:** As you were saying, there are many iterations.*

Viklund: There are many iterations, because first you try to simulate, and it doesn't work so you try again. And that intricate process takes a long time because every time you have to send data back and forth between RF design tools and board tools and integrate and simulate and so on. It just takes a long time. You might be surprised how many people still use the ASCII files that transfer RF circuits from, for example, ADS or National Instruments Microwave Office into board tools. And when they do it that way, it becomes a dumb metal blob that the tool cannot make anything smart out of. It's just a blob; you can place it and it comes out in your fabrication data. But the problem is, every time something changes, they have to do that entire process again because there is no intelligence.

So what we try to help these companies with is to say, "Well, if you have intelligent data in your ADS or Microwave Office tool, let's try to maintain that intelligent data in a round trip." So that you can send that data into our tools and implement it into a bigger system, bigger context, but still maintain all the parametric shapes and programmable shapes that you have. You're able to set up things like tuning expressions and then, by just a push button, send the data back into ADS or Microwave Office again to analyze and make adjustments, optimize and then just send the adjustments back into our tools again. But that loop has actually proven to shorten this design cycle by more than 50% in most cases. It's significant.

***Matties:** People must be pretty excited about that.*

Viklund: They are very excited about it. But it's hard sometimes to adapt a new methodology. If you've been doing one thing for 20 years and now suddenly we tell you to do something different, and you won't see the benefit until the middle or end of your project rather than immediately, that's challenging to people. They say, "I know I have a pretty good project. You're telling me to use a little bit of time up front." Yes, I am, and you're going to gain it back. People are more and more adapting to this.

Figure 1: Per Viklund, director of IC packaging and RF product lines at Mentor Graphics.

***Matties:** Cycle time is still the focus.*

Viklund: It is. Cycle times and more importantly number of cycles. If you can do one cycle and you're done, that's what everybody wants to do, but there could be various reasons why you can't. Sometimes there are legit reasons that you have to do multiple things. But you don't want it to happen because you didn't understand the design from the beginning and you don't realize it until the end. You want to make sure the tools talk the same language and the design keeps its intelligence so that you don't have to redesign because you lost something in translation.

***Matties:** If you were looking at creating the most efficient process, what advice would you give your customer?*

Viklund: It has to be an intelligent process where your data maintains design intent and intelligence of the circuit itself. You cannot translate it into dumb graphic and then go back again, because then you've lost all the intent. So that has to be maintained.

Matties: That's what you were just talking about, maintaining the access into the data.

Viklund: Yes, it's actually access into the data and intelligence of the data at all points. It has to be done that way. That's very important, and the other thing is that we cannot just dump the file, give it to somebody and tell them to import it. Because what we would be seeing is that every time you have file-based interfaces, one time or another a user will import the wrong version of the file and there's no way to see on the file that it's the wrong version, unless somebody realizes that the part is missing or something. You typically discover it once you build the board, and that's really extensive.

Matties: Dammit.

Viklund: Exactly, dammit. We're done with that, we don't use files anymore. We open the tools and we have them talk on an Internet channel between them. The tools are basically communicating back and forth live without files. Then they can use all the data management tools you have on either side to make sure that what you have opened is the right version.

Matties: Would this be considered a cloud-based situation?

Viklund: No, it's not really cloud-based. It works over the Internet but it's only the two tools involved in the communication, and it's kind of important because a lot of the times the users work with classified equipment and cannot use clouds. The cloud would have to be built inside their own organization like a mini cloud. But we don't see any advantage in this because it is two sides of the same design that need to talk for a limited period of time and then they don't need that communication anymore. So the cloud really is not that beneficial.

Matties: So it's residing on multiple computers at whatever step in the process it's living in, but it goes back and forth immediately?

Viklund: It goes back and forth. Typically you have a data management solution that makes sure you have the right version of the assigned database. That manages the work-in-progress data.

Matties: When a customer comes to you, what's the greatest challenge that they're placing on you?

Viklund: The greatest challenge is to really cut down the design time and get rid of iterations.

Matties: Are they looking for more autorouting tools?

Viklund: Not for RF and microwave. For high-speed digital, definitely, because designs are getting so complex that even if you can route them by hand it takes too long. We have a new router that we call the sketch router, which basically allows the designer to sketch his intention on the board and the router will allow it to magically follow those guidelines so that the end-result looks hand-routed. That's very powerful.

Matties: In my mind, it's like when the calculator came out. We really didn't need to know math as much as we needed to learn how to input into the machine to get the result we wanted. When I look 10 years down the road, is that what circuit design is going to look like? Calculator operators. Not to take away from the experience and expertise of a designer in any way, but it seems to me that we put in parameters and there's a lot of intelligence compiled in the database.

Viklund: It's definitely similar, because you have the problem now with having enough designers who have broad enough skill sets to manage these designs, so the tools will help the designers not get spread too thin. But I think we're still going to need intelligent and well educated designers. We have to outman the designer more than replacing him.

Figure 2: Alex Caravajal, business development manager at Mentor Graphics.

Matties: *I think there's a transition, because one of the things you mentioned is that designers have been doing it for 20 years. That's indicative of the age group of a lot of designers. We've done surveys and we see a lot of them are closer to retirement years, so is there a new group of designers coming in that's going to think differently?*

Viklund: I hope so. We're starting to see it a little bit.

Matties: *Alex, what are your thoughts on this?*

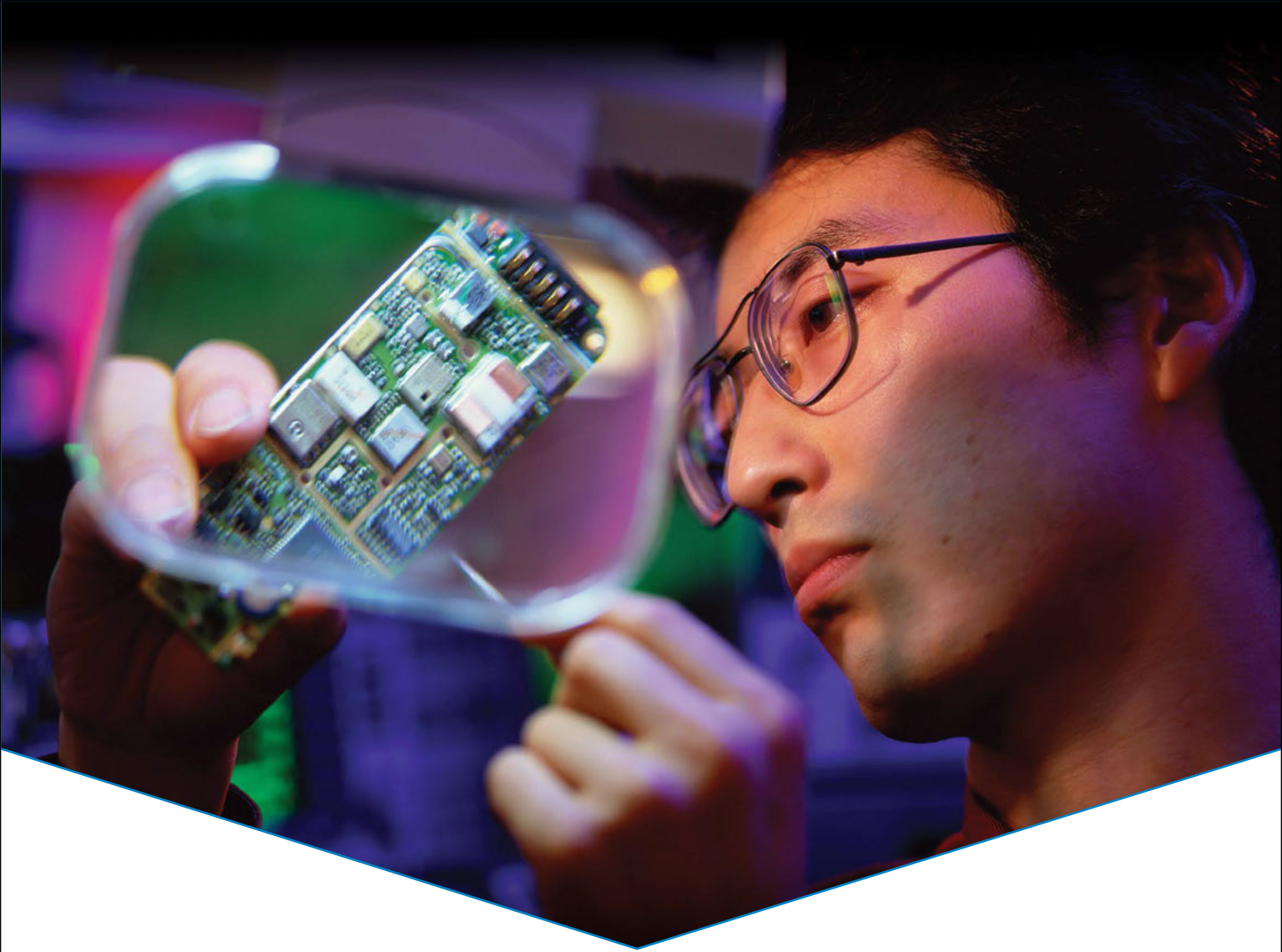
Alex Caravajal: Going back to that calculator discussion, I don't know if you've ever seen this kind of diagram. This is the system implementation diagram. Everything starts off with a concept and an application. The real issue is that you go from a spec sheet, a back of napkin, and a brainstorming session, and know we have an idea. That idea needs to be implemented, so I called it the de-aggregation process. The de-aggregation process takes the concept, the idea, and now implements it in terms of software/hardware. Yes, you can build constraints, you can make specifications, and then the engineers and programmers have to interpret that. This process kind of walks you through that.

It's sort of like when you said it is kind of like a calculator, if you understand what needs to be implemented and how it needs to be tested. As we work our way in the de-aggregation from the concept through software, through the hardware, system modeling—does it meet the right cost? The right performance, the right size, and form factor? How do we define that? Then we start implementing that in PCBs, ICs, maybe some chips. When we work back, now I have chips, I have boards, and now I have to reassemble it to represent the original concept into a system. This is really what this process is. This is where the engineers live down in here.

Matties: *This is a process regardless of what tool you're using.*

Caravajal: This is a process for engineering, and we layer it back to you. In the real world, it goes from the architectural implementation into the hardware implementation, and the whole supply chain that supports it. You buy chips, and you buy EDA tools from Mentor Graphics or any of our partners or our competitors for hardware implementation. This process, one way or another, has to be implemented to get from concept to a real working product, whether it's a large computer system, a smartphone or whatever.

Matties: *Recently, we surveyed the PCB design community to ask what the greatest challenge is, and many designers said that data was their No. 1 problem. They say they don't get the data soon enough. Someone says what they need, but there's no concurrent engineering, and this looks like what you're talking about. You start at that level.*



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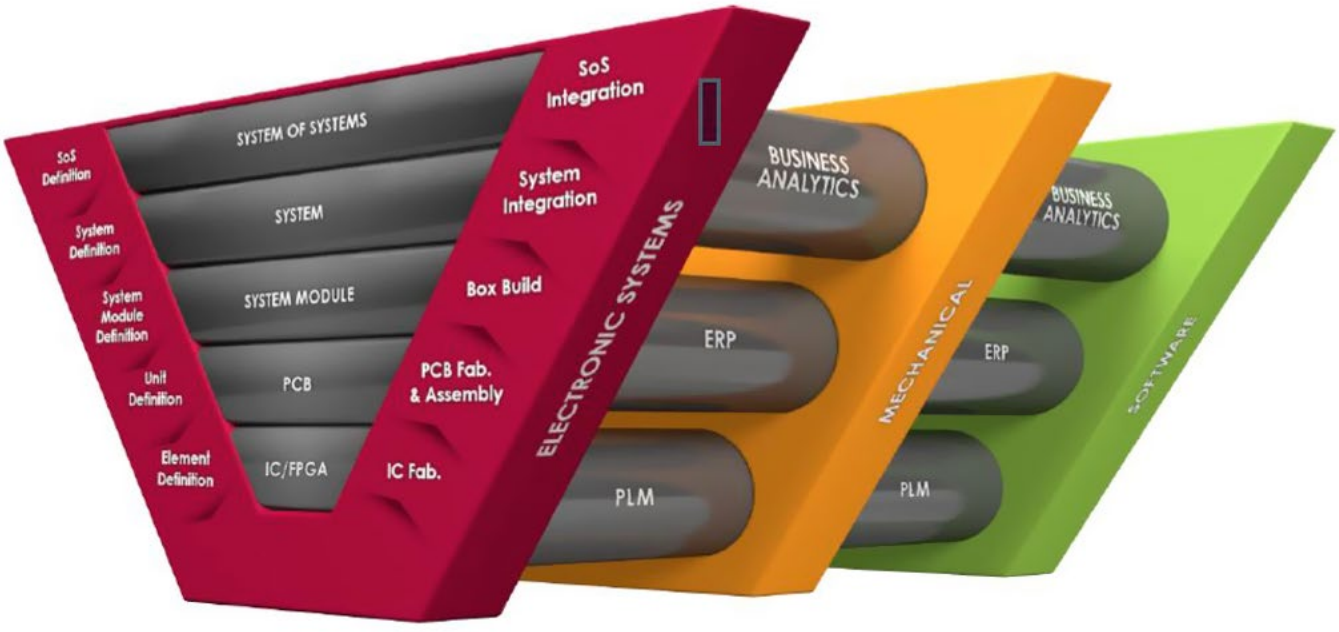


Figure 3: Graphic showing integration of software, mechanical, and electronic systems.

Caravajal: Right, we start at that level, and part of what Per was talking about is a version of RF concurrent designs. Some of our most strategic partners in RF design, like Keysight Technologies, formerly Agilent and HP with the Ansys HFSS software, need these things for their engineers. They produce data, but it has to be implemented. So that connection is critical. Sometimes it's over the wall, and sometimes it's highly automated. What Per was talking about was highly automated co-design to support RF designers in a Mentor PCB flow. Then there are people who implement FPGAs, people who implement a whole system in a package. We need to be able to support concurrency across domains and different disciplines. That is a constant ongoing data and integration issue.

Matties: Another big issue designers cited was not having enough real estate for the functionality requirement that's being placed on them.

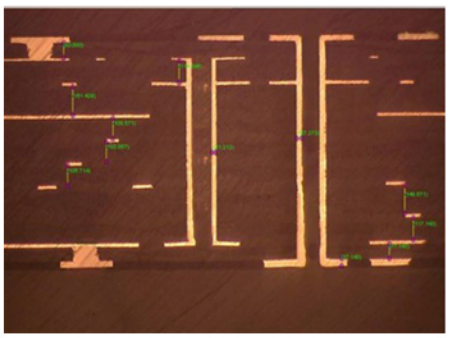
Caravajal: You have the concept. But let's say if I wanted to use an SoC for more functionality, I could put the design functionality on a single large SoC, if possible, or a couple of SoCs, such as processor, memory, and IO, and assemble this on a system-in-package for a targeted PCB form factor like a PC. You may also want to explore other form factors for automotive, tablets, phones and wearables. What you're really talking about is where we're going and being able to integrate the cost and performance domains from RFIC/package/board. That's kind of disruptive technology, because traditionally these design considerations are thrown over the wall.

PCB system design methodology is running into limitations going over the wall—time to market, being able to design it cost-effectively and achieve performance goals that you want. What is needed is a way to capture IC-package-board that could have a processor, memory, RF, IO and other IP blocks. Then collect the electrical data for consideration, get it into a "design cockpit" where I can do my trade-offs and optimization. That's what we call our Mentor Xpedition Package Integrator.

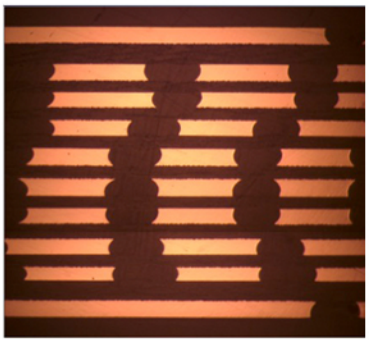
Again, it's a form of concurrent design or co-design. You don't want to build something that no one can afford, so you have to think about the cost of the package. The other really burning issue that's impacting the semiconductor guys is that it's very costly to build higher-density chips, meaning millions to hundreds of

EXTRAORDINARY

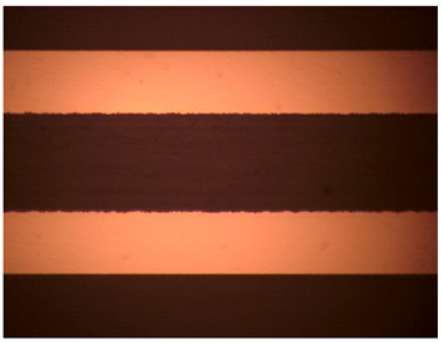
Heavy copper PCB – Microsection



Via in Pad Technology (Micro-via)



10 Layers: 140µm copper finished in each layer (4oz cu) with Buried via (L2- L9) and PTH (L1- L10)



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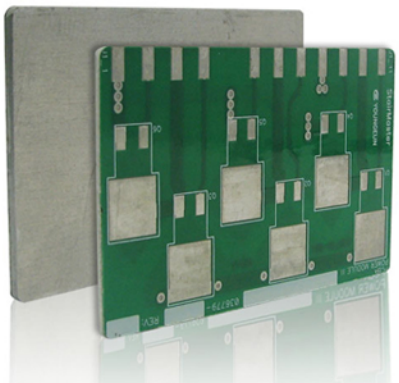

Multi-layered aluminum board
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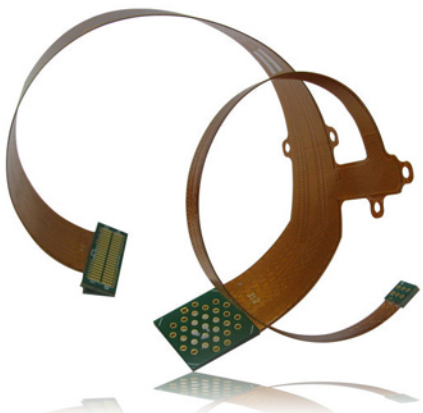

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millions of gates. Do we really need to do it that way? Can we possibly get the same results but kind of slice and dice it? I really could bring the memory in as a separate chip, the processor as a separate chip, and put it into a small package and accomplish the same goal at a price point, reliability point, and thermal point that we want. It's all spec-driven. If somebody comes with a concept and says, "Here are my thermal constraints. I don't want it to burn my hip or my face, and I want it to last on a battery three days." All these things have to be gathered together, optimized, and affordable. Part of affordability is manufacturability. So we addressed that even from a manufacturing aspect. We went from concept to product going out the door and hitting the enterprise system for PLM systems.

***Matties:** That's exactly what we're talking about, right?*

Caravajal: Yes, and I'm using it right now for ICs, package, and boards. Per could be using this from the RF designers for the RF implementation, it's the same concept. Today we have a lot of great tools. They are domain-oriented, domain IC, package, and board. This is about breaking down whether you want to do Internet of Things. You want more stuff in a little package and wearable and to hit all these constraints. We've got to break these walls down. Really it is exchanging data and not just pushing it one way and waiting.

"Today we have a lot of great tools. They are domain-oriented, domain IC, package, and board. This is about breaking down whether you want to do Internet of Things. You want more stuff in a little package and wearable and to hit all these constraints. We've got to break these walls down. Really it is exchanging data and not just pushing it one way and waiting."

***Matties:** It's reciprocating. But you guys deal with these guys all the time. Why don't more people get this?*

Caravajal: Very large companies that build processors and phone chips do get it. Right now, I would call it the early adopters stage. They know they have to do this because otherwise the product they get out the door might cost too much, or may not work as well as possible.

***Matties:** If you're managing a supply chain of partners, that creates a whole different set of challenges. Are we seeing the landscape change where companies are bringing in more engineering and more manufacturing in a captive environment just to accomplish this sort of process?*

Caravajal: It's another form of that, right? It's concurrency and engineering data with your supply chain. Yes, all these things are trying to be optimized by what I would call world-class leaders in the semiconductor marketplace. When you think about world-class semiconductor companies, they just don't build a chip for the fact of building a chip. Intel doesn't build a processor and say, "Who wants to use this?" They build a whole ecosystem—how it fits on a board, how it thermally models, how it electrically models, and what performance level their customers need. People who build phone chips do the same thing. No more ordering it from a catalog of chips. They have a co-design environment with their partners and their customers.

***Matties:** How does Tier 2 fit into all of this? We understand Tier 1 has the resources, but Tier 2 may not.*

Caravajal: Tier 2 probably will look for more on-call programmable fabric. I mentioned Altera and Xilinx, and those guys have the concept to make this for the masses—the Tier 2, Tier 3 players. What they can do is take a processor, an FPGA, and a memory and say, "I'm not going to tell you what software to put on this, and I'm not going to tell you what application to put on it. It has a processor, a DSP and some I/O for

wireless." This is probably a good platform for a network. So let's make it flexible vs. fixed. You pay a little more money for that, for the Tier 2, but the volumes are not the same. Those particular guys that have programmable fabric are implementing new technology like processors, memory, and specialized communications like wireless and Bluetooth in one package. It's like, "Here, you have the concept, I'm giving you all the tools, and you build it."

***Matties:** Now the RF market is a booming market, with automobiles really driving a lot of it.*

Viklund: The interesting thing is that it's a new market, but RF used to be military, satellites, and space. Now RF is everywhere. Everything needs to be wireless, even if it's just data communication. You have automobiles now with tracking, cruise control, and radar that can scan objects, the perimeter of the road, stuff like that. And it's coming online more and more. We know that type of design needs to be really cheap; otherwise it's not in the range for normal people to buy them. That has been going on for some time. When we presented our RF product for the first time, we got some boards from a company who was doing back-up radars for SUVs. Their radar board, which was complete radar, was $280 in fabrication costs. This is already happening. I bet there are going to be even more new markets coming into play just like automotive, and they will have the same drivers—faster designs, higher performance and cheaper products. That's what's driving it.

Caravajal: It's still an ecosystem that's worldwide, because if you think about the chips model I just told you about, the packaging is actually designed here, assembled overseas, sent back and tested here. The chips could be designed here and made there; the package could be designed here, tested here and then mass made overseas. You really don't see one hot spot. I'd say it's an ecosystem.

***Matties:** I see it globally, too. But it's interesting because we almost see this fervor for product made in USA or even made in China. They have a nationalistic approach now where they're really looking at the internal markets as much as they are the external markets. India has the same tone. I saw an ad in USA Today that said, "Walmart looking for US-made products to sell."*

Viklund: How interesting.

Caravajal: A long time ago, Walmart had a "Made in America" sign on the outside of the door. And then that dissolved over the last 25 years and now you see it pushed back. If you could do it cost-effectively, that's what it's all about. A very interesting thing you mentioned about radar. Early adopters who needed it were mainly mil/aero, and the really late adopters are automotive consumers.

Viklund: But it's also technology, because it was expensive to build a radar 20 years ago, and today, any student can build a simple radar on a circuit board and it will be $100 or so in parts. Technology has driven the market.

Caravajal: Moore's law does drive more capability every year. And by the way, this is an extension of Moore's law. Moore's law used to say it could double your performance every 18 months. Well, they're running into cost issues and this extends it. What you're doing is integrating in a package and just thinking of the best cost performance and integrating it through a whole process. So we covered the RF integration, which is part of co-design, and then I covered the integration of the IC, the package, the boards. Then of course the next level integrates that package into a board, and then the board into a system. If you think about it, it's all co-design.

***Matties:** It's all co-design. You've got to start end-to-end and work all the way through.*

Caravajal: If you close your eyes and just throw it over the wall, poor planning will produce poor products.

***Matties:** Well, gentlemen, thank you so much.*

Caravajal: Appreciate you dropping by. Glad to see you. **PCBDESIGN**

PCB007 Highlights

Kelly Dack Discusses His Recent Move

It's no secret that Prototron is one of the fabricators to watch in the US. I've known the Prototron staff for years, and worked with them for a number of years as well. So, when I heard they had hired Kelly Dack, a longtime PCB designer and guest editor for PCBDesign007, I wasted no time meeting with Kelly.

Catching Up with Vector Fabrication's Quang Luong: Here Comes Vietnam!

I have known Quang Luong, the owner of Vector Fabrication, for many years now, and I have always been interested in his business and how it operates, especially since he is the only PCB shop owner I know of who has a company both in the U.S. and in Vietnam.

TTM: Consult Fabricators Early for PCB Designs

Recently, I attended the Designers Council "Lunch and Learn" at Broadcom's office in Orange County, California. One of the speakers at this event was Julie Ellis, a field applications engineer with TTM Technologies. She sat down with me to discuss her presentation and some of the ways fabricators can assist PCB designers.

Coated Ultra-Thin Copper on Printed Circuit Laminates

Nanocopper based copper foil has great promise for high-density microcircuits. Utilizing conventional coating capability, volume production is easily scalable and cost-effective.

Institute of Circuit Technology 41st Annual Symposium

The Institute of Circuit Technology continues to grow its membership, and the Annual Symposium is a major occasion that attracts most of the leading names and faces of the UK PCB industry. This year's event was not only a platform for exchange of knowledge and ideas, but another great opportunity for building networks and collaborative relationships.

EIPC Summer Conference: Day 2

Refreshed after an excellent conference dinner, and for most, a good night's sleep, delegates returned for the second day of the EIPC Summer Conference in Berlin, continuing the theme of improving profitability through technical leadership and innovation to meet future market requirements, with sessions on materials and processes for high performance PCBs and advanced material testing strategies to meet OEM and ODM needs.

EIPC Summer Conference, Berlin: Day 1

Berlin, capital of Germany and a world city of culture, politics, media and science, was the venue for the 2015 EIPC Summer Conference, which attracted delegates from sixteen countries, including Russia, Hong Kong, Japan, Israel, USA and Canada, as well as the European Union, to experience a programme of 21 technical presentations over two days. Also included was a visit to the Berlin laboratories of Fraunhofer Institute, Europe's largest application-oriented research organisation.

IPC Releases PCB Industry Results for May 2015

Total North American PCB shipments decreased 4.2% in May 2015 from May 2014, and year-to-date shipment growth declined to -1.8%. Compared to the previous month, PCB shipments were down 3.5%.

IPC Promotes Philip Carmichael to IPC President, Asia

IPC has promoted Philip Carmichael to IPC president of Asia. Carmichael has served as president of IPC Greater China since January 2013 and will now expand his responsibilities to include member acquisition and support in Japan, Korea and ASEAN member states including Cambodia, Indonesia, Malaysia, Philippines, Singapore, Thailand and Vietnam.

iPhone 6S Series Drives Sales of Flex PCBs

The upcoming release of Apple Inc.'s iPhone 6S series, which will feature Force Touch technology, is expected to drive demand for flexible PCBs (FPCBs) as Apple is set to increase its orders from Taiwanese firms Zhen Ding Technology and Flexium Interconnect, according to a Digitimes report. This is expected to boost sales of both Zhen Ding and Flexium for the second half of 2015.

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Failure May not be an Option, but Sometimes it's a Reality

by Tim Haag
INTERCEPT TECHNOLOGY

On the surface it seemed like such a great idea: Grill up a bunch of chicken for a huge feast that would leave lots of leftovers while my wife was out of town. But I didn't realize when I pulled them from the freezer earlier that morning that there were four pieces of chicken in every package instead of just two.

"What the heck. Now I'll have even more leftovers and I won't have to cook for a week," was my bachelor-mode thinking. But I had completely forgotten that with all of that chicken comes all of that grease, and soon my barbecue was engulfed in flames.

Fortunately, I got the fire out before any major damage was done (except for my singed hair), but the charred chicken that I was left with wasn't very appetizing—not even to the dog. And this wasn't some silly mistake from my youth; it was just a couple of months ago. In a word, failure!

A famous line was spoken by actor Ed Harris, who portrayed NASA Flight Director Gene Kranz in the movie *Apollo 13:* "Failure is not an option!" It was a motivating and inspirational thing to hear. Sadly, though, sometimes failure is a reality that we have to deal with. Let's face it: If life has its ups, then it follows that there will be some downs as well. And in the world of PCB design, those of us sitting at a computer are no stranger to the occasional failure.

One of the most prevalent failures that designers have to deal with is the general misunderstanding about what we do. When I was designing full-time, I can't begin to tell you how many times I would try to explain what I did only to get a blank look in reply. My wife got so exasperated trying to explain my vocation to people that she eventually resorted to simply saying that I played video games all day long. That answer would usually still get the same blank looks, but at least the gamer crowd suddenly started treating me as an equal (which I'm not really sure was a step in the right direction).

I was explaining my job to some construction contractors one day, and after my lengthy explanation one of the guys simply asked, "Yeah, but can you roof it?" In my opinion, having your vocational zeal and enthusiasm abruptly dismissed like that is a classic form of failure.

But it's not just the "great unwashed" who have no idea what circuit board design is all about. Sometimes, those who should know better can be a problem too. How many of you designers have ever been in a situation where an

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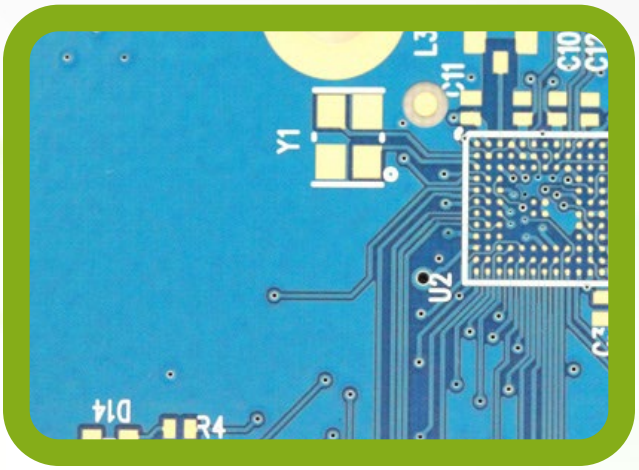

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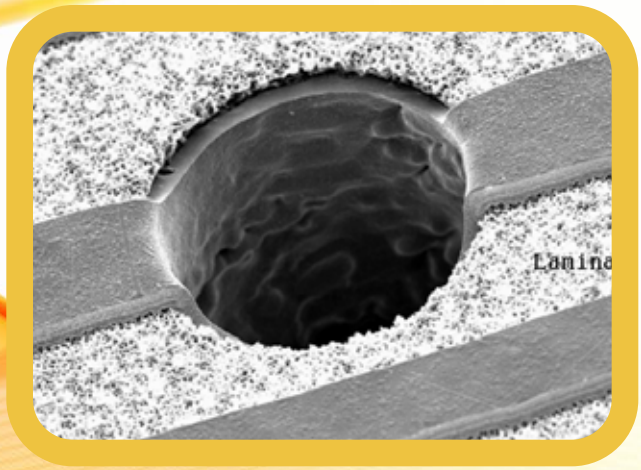

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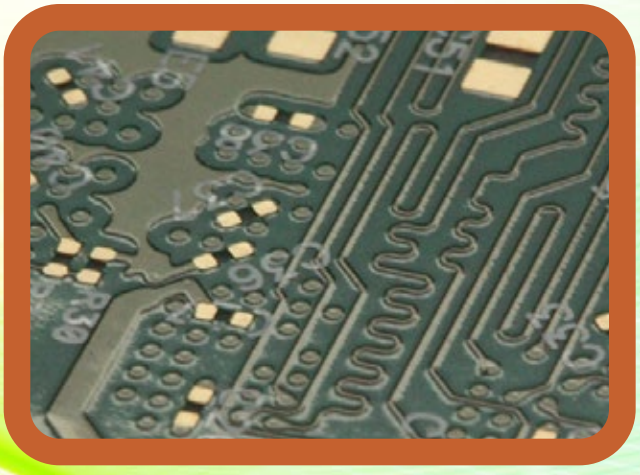

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FAILURE MAY NOT BE AN OPTION, BUT SOMETIMES IT'S A REALITY *continues*

engineer puts demands on you that prove that he doesn't understand what you actually do? I've certainly run into that.

I've had mechanical engineers question why we are bothering with circuit boards instead of designing the circuitry into the plastic housing of the device. I've had manufacturing engineers demand that I shelve the electrical considerations in order to meet manufacturing requirements, and electrical engineers who could care less if the product could actually be built. I've had engineers hover over my shoulder watching each and every stroke of the mouse that I make, and others who are never available for important questions, which ultimately brought the whole project to a grinding halt. And then like some of you, I've had my share of moments where, after the job was completed and the engineering team got their recognition, my efforts were completely ignored.

"I've had engineers hover over my shoulder watching each and every stroke of the mouse that I make, and others who are never available for important questions, which ultimately brought the whole project to a grinding halt."

It can really be tough to not look at this sort of treatment as a complete failure. Of course it isn't a failure on our part, but it can sure feel that way.

Have any of you ever been working on a design only to have your work station suddenly shut down because someone else was fooling around instead of working? I did, and boy was I mad! I'm not sure how long it had been since I had done a save, but all that time was lost just because this guy thought that he was being clever by logging into my machine and pulling the plug—on purpose. And in case you were wondering, yes, shortly after that stunt this person no longer had a job.

Back in those days I also remember talking to a designer at another company who used the same software that I was using. He had a crash and wanted some help in recovering his work. The problem is that he hadn't saved his work for many, many days. He was in the habit of always keeping his design open, and every now and then he would do a little work on it. But because he would never save it, he didn't have anything to go back to. Thank goodness now for the ability to schedule auto-saves and replaying the transcripts of our work to avoid those kinds of failures.

Now that I am working in the customer support arena, I have seen a greater variety of failure scenarios. One of the biggest failures that I see involves users who don't understand what their software is capable of. I will find people doing manual operations and getting really frustrated with how much time it is taking and how many errors they are dealing with, simply because they didn't know that the same process was already available in the core application as an automated function. To avoid this type of failure, please spend time in your user manual, look at the tutorials, and talk with other users. And if you can, look into taking a refresher course in your software from time to time, too.

Another failure that I have seen is almost in the opposite direction. Users will sometimes rely too much on automation for something that they should just do themselves with the functionality provided in the core application. I had one user call me for help after he switched companies because his original company had created a whole set of automated scripts for post-processing, and now he didn't know how to create a simple Gerber file. I've also seen users introduce design errors because they tried to do something that the software just isn't able to do. Again, knowing what your software can and can't do is the key to avoiding these kinds of failures.

I started this column by mentioning the movie Apollo 13, when the flight director said that failure was not an option. But later on in the movie, when it was suggested that this could be the worst disaster NASA had ever faced, Ed Harris' character responded with this: "With all due respect sir, I believe that this will be our finest

hour." I don't believe that this was blind faith on the part of this character; after all, these people were trained and experienced in the world of space flight and they knew the risks. Instead I believe that this was the confidence of a man who was in essence saying, "No matter the failure and the eventual outcome, we will prevail, despite the difficulty or personal cost."

That is a good mindset for us to strive for as well. We are always going to run into failures, whether they are of our own making, or software and hardware glitches that are ganging up on us, or obstacles put in our path by others. But it is how we navigate these difficulties that show what we are truly made of.

A smooth, beautiful pebble found on the beach gets its polished look by the continual pounding of the surf. The failures we experience in life are the pounding surf that shapes us into better designers, and ultimately better people. And the lady who cuts my hair is still laughing at the amount of singed hair she had to repair.

By the way, former NASA Flight Director Gene Kranz is now 81 and still flying the aerobatic plane he built when he retired. He discusses the nail-biting Apollo 13 flight in his autobiography, "Failure is not an Option." **PCBDESIGN**

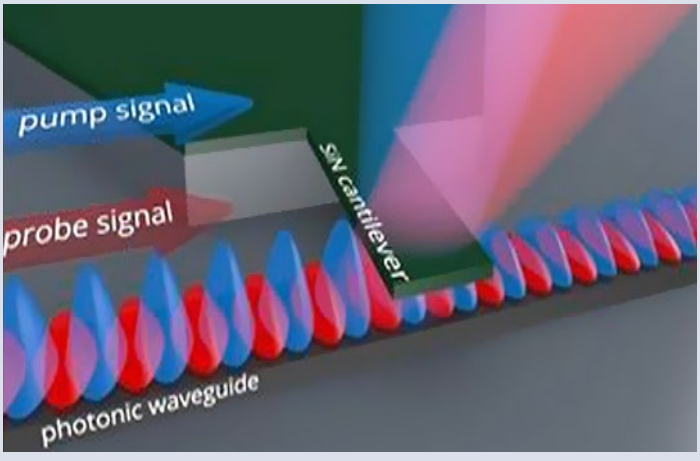
Tim Haag is customer support and training manager for Intercept Technology.

Physicists Develop Ultrasensitive Nanomechanical Biosensor

Researchers at the MIPT Laboratory of Nanooptics and Plasmonics, Dmitry Fedyanin and Yury Stebunov, have developed an ultracompact highly sensitive nanomechanical sensor for analyzing the chemical composition of substances and detecting biological objects, such as viral disease markers.

The sensitivity of the new device is best characterized by one key feature: according to its developers, the sensor can track changes of just a few kilodaltons in the mass of a cantilever in real time. One Dalton is roughly the mass of a proton or neutron, and several thousand Daltons are the mass of individual proteins and DNA molecules.

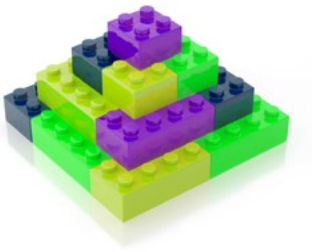
A cantilever, or beam, is a long and thin strip of microscopic dimensions (5 micrometers long, 1 micrometer wide and 90 nanometers thick), connected tightly to a chip. To get an idea how it works, imagine you press one end of a ruler tightly to the edge of a table and allow the other end to hang freely in the air. If you touch the latter with your other hand and then take your hand away, the ruler will start making mechanical oscillations at a certain frequency.



The difference between the oscillations of the ruler and the cantilever is only the frequency, which depends on the materials and geometry: while the ruler oscillates at several tens of hertz, the frequency of the cantilever's oscillations is measured in megahertz.

One chip, several millimeters in size, will be able to accommodate several thousand sensors, configured to detect different particles or molecules. The price, thanks to the simplicity of the design, will most likely depend on the number of sensors, being much more affordable than its competitors.

Stackup Planning, Part 3



by Barry Olney
IN-CIRCUIT DESIGN PTY LTD

Following on from the first Stackup Planning columns, this month's Part 3 will look at higher layer-count stackups. The four- and six-layer configurations are not the best choice for high-speed design. In particular, each signal layer should be adjacent to, and closely coupled to, an uninterrupted reference plane, which creates a clear return path and eliminates broadside crosstalk. As the layer count increases, these rules become easier to implement but decisions regarding return current paths become more challenging.

Given the luxury of more layers:

- Electromagnetic compliancy (EMC) can be improved or more routing layers can be added.
- Power and ground planes can be closely coupled to add planar capacitance, which is essential for GHz plus design.
- The power distribution networks (PDNs) can be improved by substituting embedded capacitance material (ECM) for the planes.
- Multiple power planes/pours can be defined to accommodate the high number of supplies required by today's processors and FPGAs.
- Multiple ground planes can be inserted to reduce the plane impedance and loop area.

Although power planes can be used as reference planes, ground is more effective because local stitching vias can be used for the return current transitions, rather than stitching decoupling capacitors which add inductance. This keeps the loop area small and reduces radiation. As the stackup layer count increases, so does the number of possible combinations of the structure. But, if one sticks to the basic rules, then the best performing configurations are obvious.

Figure 1 illustrates the spreading of return current density across the plane above and below the signal path. At high frequencies, the return current takes the path of least inductance. As the frequency approaches a couple of hundred MHz, the skin effect forces the return current to the surface (closest to the signal trace).

I previously mentioned that it is important to have a clearly defined current return path. But it is also important to know exactly where the return current will flow. This is particularly critical with asymmetric stripline configurations where one signal layer is sandwiched between two planes as in Figure 2. Now obviously, if the distance to the closest plane (h1) is the same distance as the far plane (h2) then the return current distribution will be equal on each plane (given the same inductance for each path). However, in order to force the current onto the ground (GND) plane of an unbalanced stripline configuration, h2 needs to be at least twice h1, and three times is better.

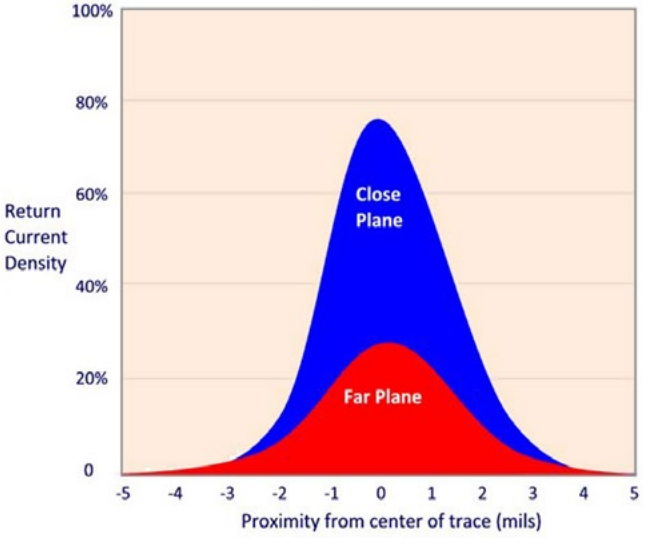


Figure 1: Return current density for asymmetric stripline planes of ratio 3:1.

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Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)
1	8	Plane	GND	Conductive			1.4					
		Core		Dielectric	4.3	5	Close plane (h1)					
2		Signal	Inner 3	Conductive			1.4	12	4	0.31	54.2	102.11
		Prepreg		Dielectric	4.3	15	Far plane (h2)					
3		Plane	Power	Conductive			1.4					

Figure 2: Close plane is h1 (5 mils), far plane is h2 (15 mils).

$$Iclose = \left(1 - \frac{h1}{h1 + h2}\right).I \quad \text{Equation 1}$$

$$Ifar = \left(\frac{h1}{h1 + h2}\right).I \quad \text{Equation 2}$$

Equations 1 and 2 define the relationship between the ratio of the thicknesses of the dielectrics to the close and far planes and the resultant return current distribution. Table 1 simplifies the calculations presenting the percentage of return current, in each plane, for different ratios of h2:h1. If the configuration is dual asymmetric stripline (two signal layers between the planes), then these ratios still apply and can be calculated by adding the two (or more) dielectric thicknesses to the far plane representing the h2 value.

Ratio h2:h1	Close Plane	Far Plane
1:1	50%	50%
2:1	67%	33%
3:1	75%	25%
4:1	80%	20%
5:1	83%	17%
6:1	86%	14%
7:1	88%	12%
8:1	89%	11%
9:1	90%	10%
10:1	91%	9%

Table 1: Percentage of return current in the close and far planes of asymmetric striplines.

Eight-Layer Stackup

An eight-layer board with six routing layers is not recommended. If six routing layers are required, then a 10-layer board should be used. For that reason, an eight-layer board can be thought of as a six-layer board with optimum EMC performance and should not be utilized to improve routability. Although there are many possible configurations of eight layers, I will only focus on the two that I consider to possess superior performance. Having said that, there are a total of four signal layers and four plane layers to consider in the each configuration.

1. The stackup of Figure 3 is the standard eight-layer configuration. This stackup has many good attributes including:

- All signal layers are adjacent to, and closely coupled to, an uninterrupted reference GND plane, which creates a clear return path and eliminates broadside crosstalk.
- Stripline return current is biased toward the GND planes.
- There is good planar capacitance (4 mils VDD to GND spacing) to reduce AC impedance at high frequencies.
- ECM could also be substituted for the center planes, further improving the PDN performance.
- Crosstalk is minimized by closely coupling the signal to plane layers.
- EMI is minimized by routing critical signals between the planes.
- The substrate can accommodate a number of different technologies. For example: 50/100 ohm digital and 90 ohm USB.

Differential Pairs > 50/100 ohms | USB 90 ohms

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)
		Soldermask		Dielectric	3.3	0.5						
1	8	Signal	Top	Conductive			2.0	10	4	0.4	51.61	97.17
		Prepreg		Dielectric	4.3	3						
2		Plane	GND	Conductive			1.4					
		Core		Dielectric	4.3	5						
3		Signal	Inner 3	Conductive			1.4	10	4	0.31	54.16	99.48
		Prepreg		Dielectric	4.3	15						
4		Plane	VDD	Conductive			1.4					
		Core		Dielectric	4.3	4						
5		Plane	GND	Conductive			1.4					
		Prepreg		Dielectric	4.3	15						
6		Signal	Inner 6	Conductive			1.4	10	4	0.31	54.16	99.48
		Core		Dielectric	4.3	5						
7		Plane	GND	Conductive			1.4					
		Prepreg		Dielectric	4.3	3						
8		Signal	Bottom	Conductive			2.0	10	4	0.4	51.61	97.17
		Soldermask		Dielectric	3.3	0.5						

Figure 3: Standard eight-layer stackup with central planar capacitance using virtual materials.

Differential Pairs > 50/100 ohms | USB 90 ohms

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)
		Soldermask		PSR-4000 HFX Satin / CA-40 HF LPI (1GHz)	3.5	0.5						
1	8	Signal	Top	Conductive			2.0	12	4	0.4	51.42	98.53
		Prepreg		IT-180A; 1080; Rc=62%; (2GHz)	3.9	2.8						
2		Plane	GND	Conductive			1.4					
		Core		IT-180A; 1-2116; (2GHz)	3.8	4						
3		Signal	Inner 3	Conductive			1.4	12	4	0.31	52.2	99.69
		Prepreg		IT-180A; 7628; Rc=43%; (2GHz)	4.0	7.4						
		Prepreg		IT-180A; 7628; Rc=43%; (2GHz)	4.0	7.4						
4		Plane	SPLIT POWER	Conductive			1.4					
		Core		Dielectric	4.3	4						
5		Plane	SPILT POWER	Conductive			1.4					
		Prepreg		IT-180A; 7628; Rc=43%; (2GHz)	4.0	7.4						
		Prepreg		IT-180A; 7628; Rc=43%; (2GHz)	4.0	7.4						
6		Signal	Inner 6	Conductive			1.4	12	4	0.31	52.2	99.69
		Core		IT-180A; 1-2116; (2GHz)	3.8	4						
7		Plane	GND	Conductive			1.4					
		Prepreg		IT-180A; 1080; Rc=62%; (2GHz)	3.9	2.8						
8		Signal	Bottom	Conductive			2.0	12	4	0.4	51.42	98.53
		Soldermask		PSR-4000 HFX Satin / CA-40 HF LPI (1GHz)	3.5	0.5						

Figure 4: Alternate eight-layer stackup with central split power planes using ITEC IT-180A 2GHz material.

Probably the only negative, for this configuration, is that it will not accommodate multiple power supplies on the lone power plane. Today's high-speed processors and FPGAs require more than six or seven different high current power sources. So if you are pushing the envelope then this configuration is probably not right for you. A recent complex layout that I completed had a total of 13 individual power supplies. As this is becoming the norm, additional power planes need to be exploited and these need to be split to accommodate all 13 supplies plus GND.

2. The alternate configuration of Figure 5 alleviates the multiple power supply issue but does this by sacrificing planar capacitance. So in order to compensate, for this shortcoming, the PDNs need to have multiple decoupling capacitors with self-resonances close to the fundamental clock frequency. Also, lower mounting inductance can be achieved by placing these decaps on the top layer so that the fanout vias connect to planes 2 and 5 rather than transverse the total layer span. This also helps lower the high-frequency AC impedance.

STACKUP PLANNING, PART 3 *continues*

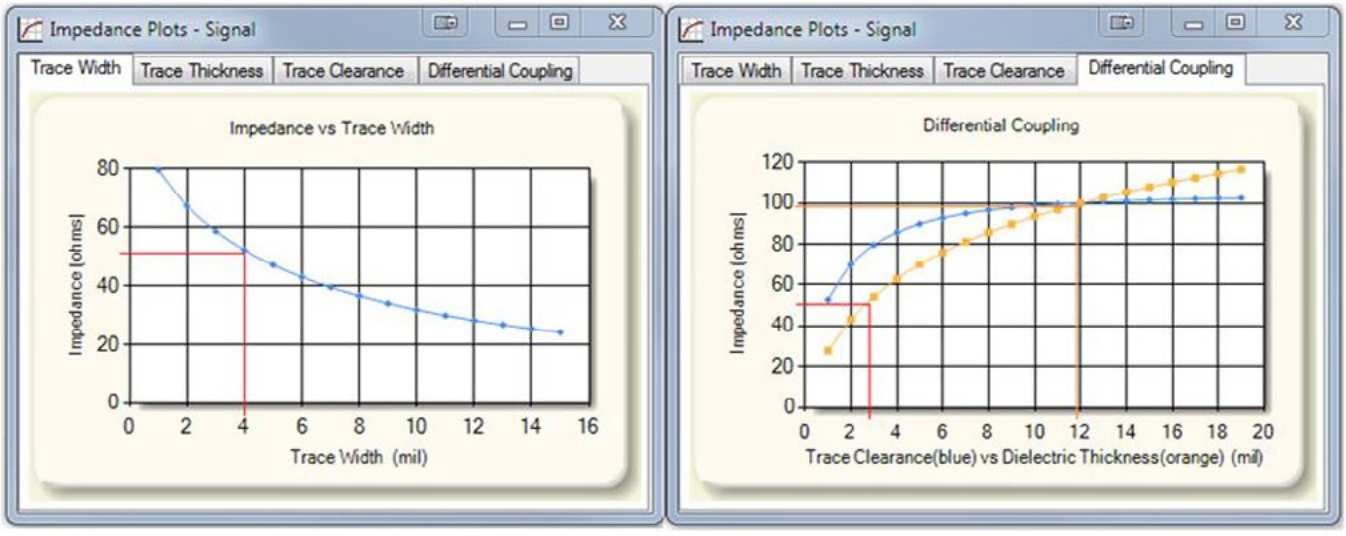


Figure 5: Impedance plots for the microstrip layers.

I have mentioned in previous columns that planes should not be split. This mainly refers to having one continuous GND plane for all supplies including analog. But since, in this case, the return current path has been forced into the GND planes then the path is not interrupted. Looking at the asymmetric stripling configuration between layers 2 and 4 of Figure 4, we have a ratio of 14.8:4. This means that at least 79% of this current will flow in the GND plane. However, if you also take into account the increased inductance, of the alternate return path, this almost totally eliminates the power plane. It is important to place GND stitching vias close to each signal layer transition to ensure there is a low inductance path between GND planes.

Figure 5 incorporates ITEC IT-180A 2GHz materials. This material is very common in Asia and is suitable for low-cost, high-speed applications. It has a low dielectric constant and low dielectric loss of just 0.015 with a glass transition temperature of 180C. Since the "real" values are quite different to the "virtual" values, I have used to initially construct the stackup, the variables must be adjusted to provide the correct impedances for the design.

The impedance plots of Figure 5, project the correct values of trace width (4 mils), trace thickness (2 mils), trace clearance (12 mils) and dielectric thickness (2.8 mils) given the dielectric constant (3.9) for the ITEC IT-180A 2GHz material to achieve the target single ended and differential impedance. This also provides the differential coupling point whereby increasing the trace spacing has little effect as the impedance rolls off. In this case, 12 mils is ideal for 100 ohms differential impedance.

Next month, Part 4 of the Stackup Planning series will continue detailing the construction of 10+ stackup layer configurations. Once the basics are defined, the pattern for higher layer-count structures becomes evident.

Points to Remember

- Each signal layer should be adjacent to, and closely coupled to, an uninterrupted reference plane, which creates a clear return path and eliminates broadside crosstalk.
- Although power planes can be used as reference planes, ground is more effective.
- At high frequencies, the return current takes the path of least inductance.
- In order to force the current onto the ground (GND) plane of an unbalanced stripline configuration, h2 needs to be at least twice h1; three times is even better.
- An eight-layer board can be thought of as a six-layer board with optimum EMC performance and should not be utilized to improve routability.

- Additional power planes need to be exploited and these need to be split to accommodate all supplies plus GND.
- The impedance plots project the correct values of all variables for the chosen material to achieve the target impedance. **PCBDESIGN**

References

1. Barry Olney Beyond Design columns: Material Selection for SERDES Design, Material Selection for Digital Design, The Perfect Stack-up for High-Speed Design, and Embedded Signal Routing.

2. Henry Ott: Electromagnetic Compatibility Engineering.

3. To download the ICD Stackup and PDN Planner, visit www.icd.com.au.

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. The company developed the ICD Stackup Planner and ICD PDN Planner software, is a PCB Design Service Bureau and specializes in board level simulation. To read past columns, or to contact Olney, click here.

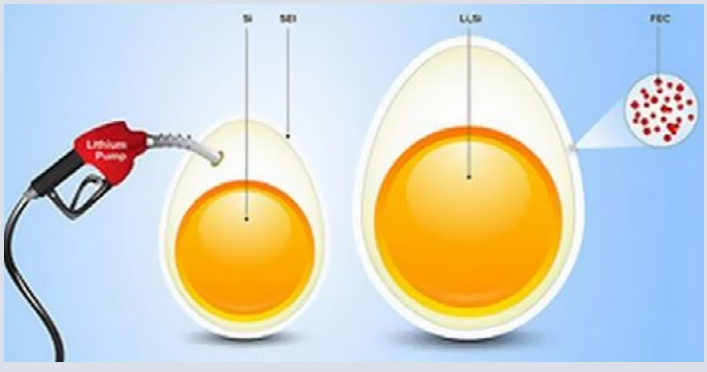
Protective Shells May Boost Silicon Lithium-ion Batteries

Imagine a cell phone that charges in less than an hour and lasts for three to four days, or an electric car that runs for hundreds of miles before needing to be plugged in.

Researchers at the U.S. Department of Energy's Argonne National Laboratory are working to make this dream a reality by developing lithium-ion batteries containing silicon-based materials. The most commonly used commercial lithium-ion batteries are graphite-based, but scientists are becoming increasingly interested in silicon because it can store roughly 10 times more lithium than graphite.

There's just one problem: current batteries based on silicon materials don't last long.

The problem lies in the battery's chemistry. The electrolyte inside the battery transports lithium ions back and forth between positive and negative electrodes as the battery charges and discharges.



Lithium ions react with the negative electrode to form a new compound, causing the electrode to expand, while the electrolyte produces a protective coating called the solid electrolyte interphase.

"The ideal solid electrolyte interphase should halt the reaction between the electrode and electrolyte, while allowing the lithium to come through," said Ilya Shkrob, a chemist in the Chemical Sciences and Engineering Division.

But the coating also needs to expand and contract with the electrode, or else it will crack and the battery won't work.

"When the protective layer cracks, the electrode surface reacts and consumes the electrolyte," Shkrob said. "If the electrolyte is completely consumed, then the battery won't work."

In today's graphite-based lithium-ion batteries, the electrode expands about 10%—a small enough change that cracks in the coating aren't an issue.

But the electrode in a silicon-based lithium-ion battery expands up to 300%. These batteries need a different electrolyte in order to produce an elastic shell.

The researchers found that when fluorine is added to ethylene carbonate, the resulting electrolyte forms a coating that can stretch and accommodate the volume changes in the electrode.

MilAero007 Highlights

Avoid Overbuilding your RF Printed Circuit Board

Today, many companies are overbuilding and "overmaterializing" their RF printed circuit boards. In this interview, James Hofer of Accurate Circuit Engineering (ACE) shares some strategies to avoid doing both, which will help lower the total cost of your PCB and improve the overall product quality. Hofer also discusses some of the challenges in the laminate supply chain.

A Look at the High-Reliability Interconnect Market

I-Connect007 Publisher Barry Matties recently met with Mark Cormier of Miraco Inc. to discuss the latest trends and drivers in the high-reliability segment, and their customers' increasing demand for quality.

Changing the Face of Displays… One Button at a Time

Incom produces fused fiber optics with a new polymer process that replaces traditional glass fiber optics. This allows the creation of new applications, and for OEMs it changes the way they can build human control interfaces. Emilijo explains how Fairlight is incorporating this technology into their famous products for the recording and broadcast industries, along with other applications such as elevator control panels.

Exception PCB Solutions Design Service Boosts CID+ Qualifications

Exception PCB Solutions growth and development in 2015 continues with a focus on service including additional investment in Exception's Integrated PCB Design Service which is proving to be highly popular. This has resulted in increased growth not only from existing customers, but also from many new customers across a range of sectors.

NASA, DRS Technologies Collaborate to Create Mid-Infrared Detector

NASA scientist Xiaoli Sun and his industry partner have created the world's first photon-counting detector sensitive to the mid-infrared wavelength bands—a spectral sweet spot for a number of remote-sensing applications, including the detection of greenhouse gases on Earth, Mars and other planetary bodies, as well as ice and frost on comets, asteroids and the moon.

FTG Circuits' Sales Up $1.8M or 15% in Q2

"The second quarter of 2015 saw record sales for FTG with all sites participating in the growth," stated Brad Bourne, president and CEO. He added, "These record sales are enabling us to report strong earnings while still investing in our future."

Multilayer Technology Passes AS9100 Surveillance Audit

Multilayer Technology (MLT), located in Irving, Texas has passed its AS9100C surveillance audits. The audit consisted of 2.5 days (20 hours) of intense auditing by our registrar. All departments were completely audited to ensure compliance to the AS9100C Certification.

All Flex Flexible Circuits & Heaters Achieves AS/ISO Re-certification

All Flex, manufacturer of flexible printed circuits and heaters announces re-certification to AS9100C and ISO 9001:2008. AS9100 is an international aerospace standard for quality assurance requirements of aerospace companies.

Satellite Project to Clean Up Space Debris Orbiting Earth

The Clean Space One Project has passed a milestone. The space cleanup satellite will deploy a conical net to capture the small SwissCube satellite before destroying it in the atmosphere. It's one of the solutions being tested for eliminating dangerous debris orbiting the Earth.

Alone in the Darkness: Mariner 4 to Mars, 50 Years Later

July 14 marks 50 years of visual reconnaissance of the solar system by NASA's Jet Propulsion Laboratory (JPL), beginning with Mariner 4's flyby of Mars in 1965. Among JPL's first planetary efforts, Mariners 3 and 4 (known collectively as "Mariner Mars") were planned and executed by a group of pioneering scientists at Caltech in partnership with JPL.

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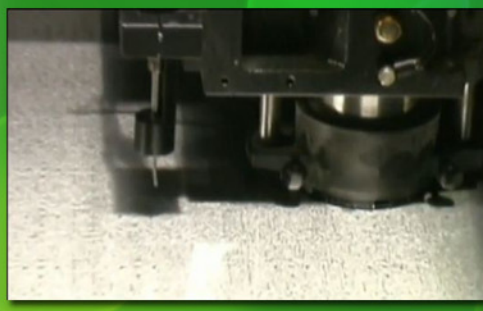

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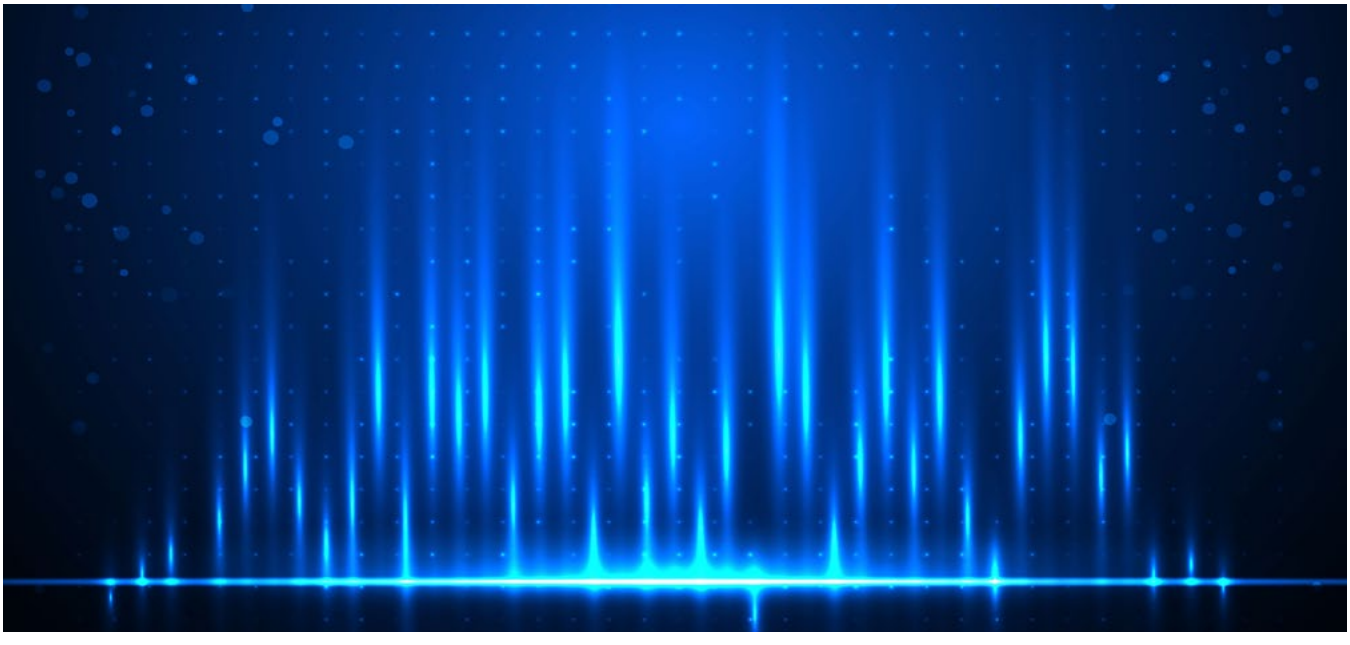
A Brief Overview of High-Frequency Laminates

by John Coonrod
ROGERS CORPORATION

The PCB laminates used for high-frequency applications possess several unique attributes that are distinctly different than FR-4 types of materials. Obviously, the electrical properties are better for high-frequency laminates than FR-4, however there are many other beneficial characteristics which may be less obvious for those unfamiliar with these specialty laminates. These other properties are the reason why sometimes, high-frequency laminates are used for applications that are not high-frequency.

Moisture absorption can be problematic for high-frequency circuits (and other applications) for several reasons. When a circuit absorbs moisture from its environment, some water content becomes part of the material matrix on a molecular level. Water has a high dielectric constant, with a value of approximately 70. Most components that make up a laminate have dielectric constant values in the range of about 2–10, so if an appreciable amount of the material matrix has a component of 70, the overall laminate dielectric constant will increase significantly. A change in dielectric constant will cause a change in impedance, propagation velocity, phase response and other circuit issues. Additionally, the change due to moisture is typically a variable based on the environmental conditions in which the circuit is operating.

The amount of moisture absorption that can impact circuit performance is unique to the circuit design and application. Some applications are nearly unaffected by moisture absorption issues and others will have electrical performance that is greatly affected. The amount of moisture absorption which is considered low for high-frequency applications is somewhat subjective, but as a general rule a value of 0.3% or less is considered good. Moisture absorption also increases insertion loss, and as another general rule, the applications that are higher frequency or higher speed are more susceptible to moisture effects.



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A BRIEF OVERVIEW OF HIGH-FREQUENCY LAMINATES *continues*

Other issues that are critical to many high-frequency applications and also environment-related is TCDk and TCDf. All circuit materials have these attributes: TCDk is the temperature coefficient of dielectric constant (Dk) and TCDf is analogous in regards to dissipation factor (Df). Basically, this is the property of material which will change Dk or Df with a change in temperature. Many times this becomes an issue when an application is fine-tuned in a lab environment and it then performs different in the field as the temperature fluctuates. The amount that TCDk or TCDf impacts circuit performance is very design and application specific. Some applications will be unaffected by these changes and others may see dramatic shifts of electrical performance. An ideal TCDk or TCDf would be 0 ppm/°C, which gives no change in Dk or Df with a change in temperature, but this is typically not realistic. A general rule for a good TCDk is an absolute value of 70 ppm/°C; however, there are many applications which could tolerate 200 ppm/°C or even more.

Other thermal properties related to laminates are pretty well known in the PCB industry such as coefficient of thermal expansion (CTE), glass transition (T_g) and decomposition temperature (T_d). These properties are related to high-frequency applications in a manner similar to most other applications, where these issues are typically a concern for assembly and long-term reliability. However, some high-frequency laminates, due to the nature of their formulation, have very good CTE, T_g or T_d. Some of the ceramic-filled hydrocarbon laminates, such as RO4350B™ substrates used at high frequency, have good CTE and extremely good T_g and T_d.

Another material property which is common for all laminates is thickness control and high-frequency laminates excel with this concern. Because impedance and other circuit properties are sensitive to the substrate thickness, high-frequency laminates generally have better thickness control than FR-4 type laminates. It is common to have high-frequency laminates with a thickness control of ±7% or better. The tightly controlled thickness combined with the fact that high-frequency laminates also control the dielectric constant strictly, allows the designer to have much tighter control over impedance and other electrical properties of a circuit. This combination of laminate properties control is why high-frequency laminates are sometimes used in applications where impedance control is critical, but it may not be a high-frequency application.

Lastly, many high-frequency laminates that use special filler to achieve good CTE values and stable electrical properties often have much higher thermal conductivity. In general, PTFE based substrates have a relatively low thermal conductivity and it is typically in the range of 0.25 W/m·K. However when the proper filler is added to PTFE, to formulate a high-frequency laminate, the thermal conductivity can increase significantly and values of 0.5 W/m·K or more, are common. The ceramic-filled hydrocarbon high-frequency laminate mentioned previously also has the benefit of high thermal conductivity filler and that substrate has a thermal conductivity value of 0.64 W/m·K. A special formulation of a high-frequency laminate, RT/duroid® 6035HTC material, is a PTFE based substrate with unique formulation to achieve a thermal conductivity figure of 1.44 W/m·K. Again, these laminates are sometimes employed in applications where high-frequency is not a concern, but where thermal management is a critical issue.

It has been shown that high-frequency laminates have many attributes which make them attractive for applications that are not necessarily high-frequency, but can be used when other concerns are important. Obviously, when an application is high-frequency or high-speed digital, then these specially formulated laminates are the proper choice. However, when a designer or PCB fabricator is working with a new design, which may or may not be high-frequency related, they should consider all material options. **PCBDESIGN**

John Coonrod is a senior market development engineer for Rogers Corporation. To read past columns, or to reach Coonrod, click here.

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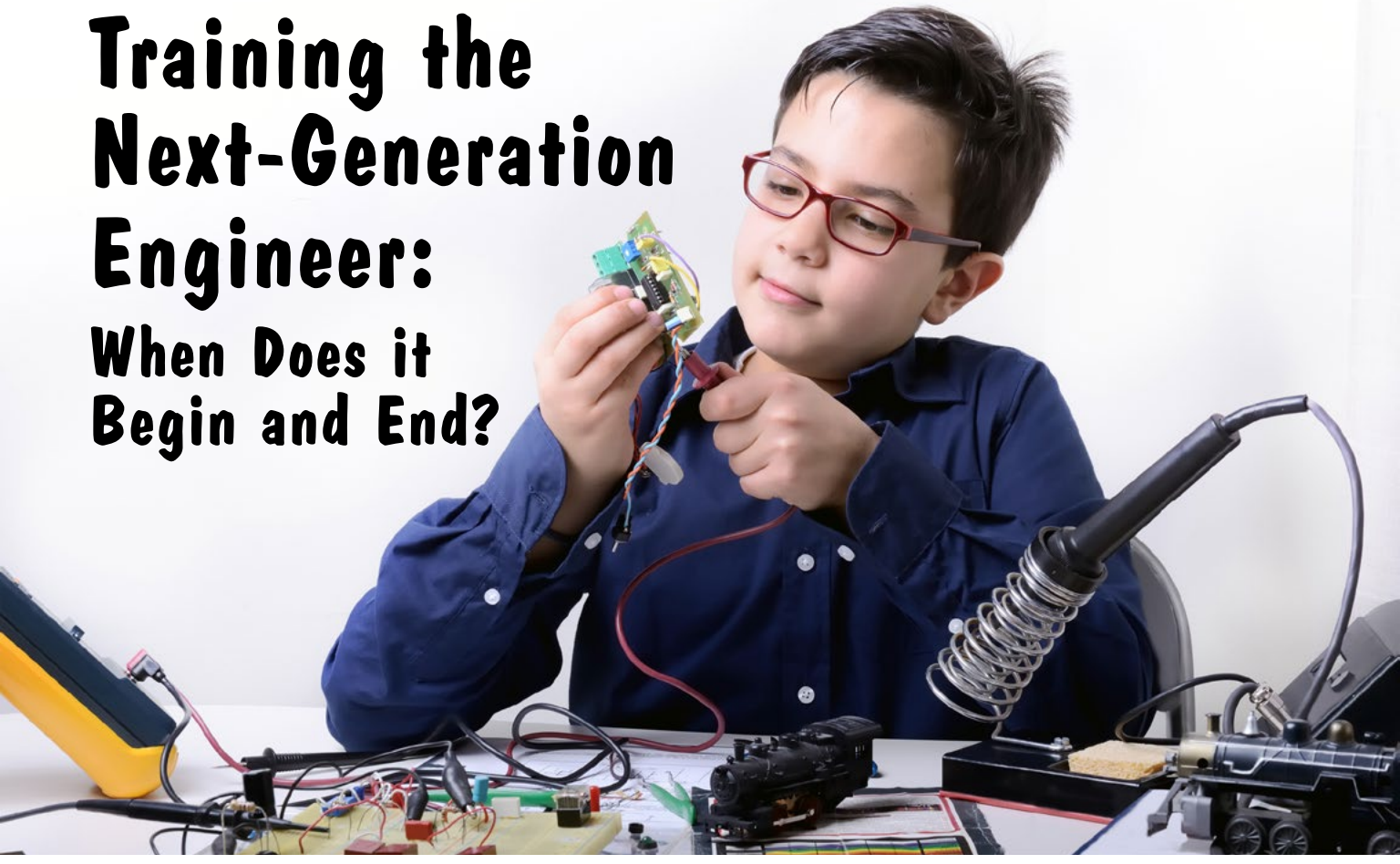

by Tom O'Connor
DFR SOLUTIONS

American engineering companies are seeing a severe shortage of the homegrown engineers required to compete globally. Just go into any company today and you'll notice that increasingly, the engineers are foreign-born. Our local universities are seeing fewer and fewer American engineering students each year. Universities are also seeing a growth in female students. Over 50% of college student are now female, and women traditionally are not attracted to science and engineering majors.

What is causing this imbalance? Why is the U.S. unable to train as many engineers as it needs? How is the U.S. going to fill its engineering requirements? Today, the answer is importing engineers who have an education and an H-1B visa. But is this a long-term answer? Probably not. As foreign countries catch up with the U.S. in technical capability and manufacturing abilities, these engineers will want to stay home as the pay in their home countries increases. Any of those who did come here to work will be able to bring their experiences home to help speed this transformation.

Another way companies avoided filling their engineering need was by offshoring, first with the manufacturing and then the engineering functions. This created hollow companies that are devoid of manufacturing and engineering. These companies are controlled by marketing and accounting staff, with just a few manufacturing engineers whose only function is to interface with the offshore contractors. This model works very well for high-volume, low-risk consumer product companies, whose goal is to make the products as cheaply as possible with just the right amount of functionality. The communications between OEM and contractor is not the critical item in these cases; cost is the critical factor. More and more companies are finding that all products do not meet this definition and foreign, low-cost suppliers are not always the right answer to their design and manufacturing needs.

Today, we are reading more and more about onshoring products. Companies may not be starting their own manufacturing facilities, but

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they are keeping their cost low by using North American contractors. They are weighing the cost of doing business due to longer logistics lines that cross multiple time zones and languages. Many of these companies are bringing the design and manufacturing back in house. One company that recently announced this move is General Motors. Earlier this year, GM announced that they would be closing some of their design centers in Asia, and the company is now planning to rebuild that capability in Michigan. Many have speculated that this move was brought on by all of GM's recalls. GM cannot afford any more bad publicity.

One avionics company set up a R&D center in Asia to cut engineering costs. They now are seeing higher costs because of poor quality work and the need to redo many designs. Their customers are now starting to feel the difference and the supplier is now wondering if the move was correct and is bringing more critical work back to the US.

How can the engineering community attract good young engineers? It starts at the K-12 level. Scientists, technologists, engineers and mathematicians (STEM) need to be seen as the cool kids once again. (I'm showing my age now.)

In the '50s and '60s, when the U.S. was in the race to beat the USSR to the moon, science was cool. All the boys wanted to be an astronaut or a rocket scientist. Universities were graduating STEM-related majors left and right. After we landed on the moon and the USSR did not, interest waned and the perceived need for STEM graduates diminished. Marketing and accounting became the hot majors in the '70s and '80s, and these graduates took over corporate America. By the '90s, the move to subcontracting manufacturing was well on its way. Since the beginning of the century, offshore contracting has taken over.

A Way Forward

Since 2006, there has been a realization that the STEM-related majors need more emphasis. Politicians are touting STEM programs in K-12 education. The good news is that it is starting to work. The other good news is that more and more young women are getting into STEM majors due to these new policies.

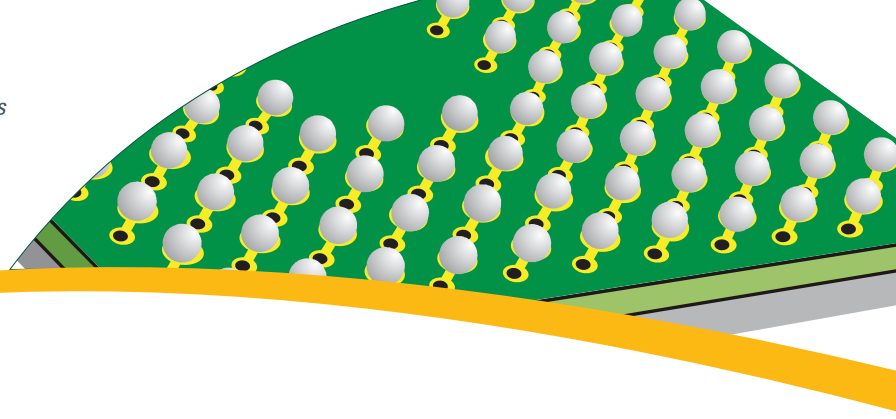
So how do we keep these young engineers interested in staying engineers? First, start with good pay. Companies need to realize they are not competing against other engineering companies. Young STEM graduates are attractive to Wall Street, marketing, and law firms. If you want the best you have to compete for the best. It is not just a cost of doing business; it is the cost of survival. Engineering companies do all the heavy lifting to generate STEM graduates. Why just let these other industries pick off the cream of the crop? A good competitive starting pay will pay many dividends later in their careers.

"If you want the best you have to compete for the best. It is not just a cost of doing business; it is the cost of survival. Engineering companies do all the heavy lifting to generate STEM graduates. Why just let these other industries pick off the cream of the crop? A good competitive starting pay will pay many dividends later in their careers."

Treat these young people as the adults they are, but recognize that they are not 45 years old with two kids and a mortgage. Know what keeps the interest of millennials. This is very important. Recently, a young aerospace engineer whom I know left a Fortune 100 aerospace company and then a small engineering company for a young management software company. Why wasn't the big Fortune 100 Company able to keep this engineer? He didn't see his usefulness at the big company and didn't see being compensated in the near term. He saw he was worth more to the young upcoming software company and now he is being compensated for his worth.

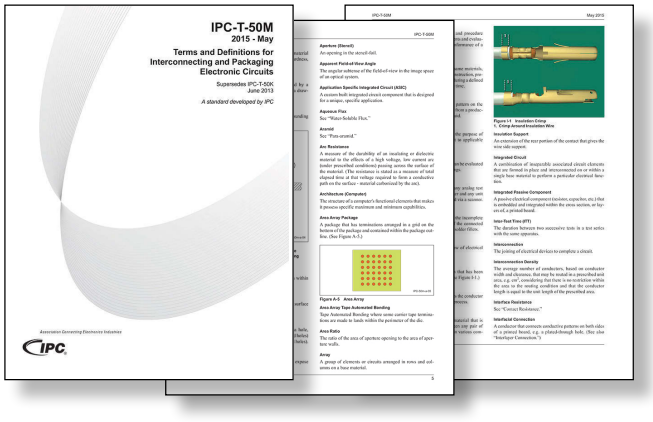
Once the engineer is hired, the way to keep them is to talk to them. Not just the HR manager, but his immediate manager and his boss should get to know the young engineer. This should not be just a one-time meeting, but a

Association Connecting Electronics Industries



T-50M: Defining the Language of an Industry

What's relevant for today's OEM, EMS or ODM Company?



Each year, a new slew of terms and definitions become common place in the manufacturing process. To meet these needs, T-50 Revision M, *Terms and Definitions for Interconnecting and Packaging Electronic Circuits*, delivers users the most up-to-date descriptions and illustrations of electronic interconnect industry terminology. It is a dynamic standard that adapts to the industry to provide the most thorough dictionary in the industry.

T-50M brings 150 new terms, while eliminating out-of-date terminology in order to provide a streamlined standard that focuses on the trending language of the electronics industry. This revision includes terms often cited in other standards, here is a sneak peek at some of the newly added terms for T-50 Revision M:

- **Backfill (Liquid)**
  The act of sealing the edge of a component with an adhesive or encapsulate to prevent intrusion of liquids or other contaminants.

- **Glob-Topped Encapsulation**
  A localized application of a viscous compound to a printed board assembly, other substrate or component/wire, which is then fully cured to provide mechanical support and environmental protection.

- **Microsection (Mount)**
  The polymer encapsulation of a sample for support during destructive cross-sectional view preparation. Without this support, the sample would be unacceptably deformed by grinding and polishing, such that it could not be examined. It is commonly used for the microscopic examination of printed board features.

Stay up to date with the trending terms covering the newest emerging technologies. Prepare for tomorrow's discussions by downloading T-50M today.

series of one-on-one and group meetings. These meetings should have a two-way dialogue. The basic ground rule: Nothing the young engineers can say is negative. These engineers are the future and life blood of your company.

Next, young engineers should be assigned a mentor outside of their immediate group. This person needs to understand his or her roll. Training by HR should be a requirement. The mentor should be selected to match the personality and interests of the mentee. You want them to hit it off and become friends.

I remember my days at Texas Instruments. There was no mentor program; you were on your own to discover the right way to get a project done. I was fortunate. I'd spent seven years as an officer in the Army, so I knew how to get things done. I'll never forget the number of recent college graduates who would ask me how I knew to do something. Nobody would tell them until it was too late, when they would hear it from a program manager whose program was lagging behind. A mentor program would have paid major benefits then. Meanwhile, TI had a high turnover rate.

Finally, young engineers should be encouraged to join engineering groups like SMTA, IPC, the American Society for Quality (ASQ), and Women in Engineering. Once they join these groups they should be given time (even encouraged) to participate with the local chapters and attend the conventions and symposiums.

Finally, young engineers should be encouraged to join engineering groups like SMTA, IPC, the American Society for Quality (ASQ), and Women in Engineering. Once they join these groups they should be given time (even encouraged) to participate with the local chapters and attend the conventions and symposiums. Too often I hear, "Only my boss gets to go to this or that event." Young engineers are sponges, and the opportunity to learn should be made available.

It is amazing how much information is transferred as a manager and a junior engineer walk the aisle of a trade show. While attending conferences, young engineers should be assigned to attend a couple of presentations during a symposium and required to report back to teammates what was learned.

Local chapter meetings offer even more to help the young engineer's education. First, he learns there are other engineers having the same issues. He also quickly learns that this community is very supportive; he can talk freely with his peers without any repercussions. For the company, the local chapter meetings give the engineer the biggest bang for the smallest commitment, time and local travel. The engineer's education gain easily outweighs the value of an hour or two of lost labor every few months.

Again, retention is the goal. The cost of losing an engineer is very high, not only for his present company, but probably for the STEM community if the engineer decides to move to a different industry that promises to treat him better.

In conclusion, high-tech companies will be hiring more and more engineers in the next couple of years. These companies should do everything they can do to attract and retain the best and the brightest STEM graduates. First, they should offer salaries that are competitive with other industries. Second, they should establish effective mentoring programs. Finally, they should encourage continuing the young engineers' education by encouraging active participation in industry organizations. **PCBDESIGN**

Tom O'Connor is the outside sales manager with DfR Solutions. Tom has over 30 years of experience in the electronics industry. He began his career as a manufacturing engineer at Texas Instruments, building the first airborne FLIR systems.

TECHNICAL SALES MANAGER

(Midwest Territory)

Taconic, a leader in the manufacture of PTFE coated fiberglass fabric, belts, tapes and circuit board laminates is seeking a **Technical Sales Manager** to grow our Advanced Dielectric Division (ADD) market. Responsibilities will include servicing existing accounts and developing new markets and customers in assigned territory for microwave circuit laminate product line.

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Recent Highlights from PCBDesign007

1 Fast Interconnect: Engineering Services for the Masses

Gary Griffin and Ana Rosique are co-founders of Fast Interconnect, an Arizona-based product engineering company designed to serve an underserved market: the small product developers, inventors, and anyone with an idea for a "cool gadget." I caught up with Griffin recently to discuss the new company, its innovative business model, and the challenges facing smaller OEMs and product developers.

2 EDA Analyst Gary Smith Dead at 74

Longtime EDA analyst Gary Smith died July 3 in Flagstaff, Arizona at the age of 74. He had been ill with pneumonia. He knew more about the EDA market than anyone I've ever known. I once asked Gary, "How many PCB design seats do you think are in China?" He sent me numbers for all of Asia and broke them down by country. He really loved EDA.

3 Avoid Overbuilding your RF Printed Circuit Board

Today, many companies are overbuilding and "overmaterializing" their RF printed circuit boards. In this interview, James Hofer of Accurate Circuit Engineering (ACE) shares some strategies to avoid doing both, which will help lower the total cost of your PCB and improve the overall product quality. Hofer also discusses some of the challenges in the laminate supply chain.

4 Mentor Graphics White Paper: 10 Key Challenges in Electronics Thermal Design

Miniaturization of electronics is continuing to increase power densities at all packaging levels. Without cooling, most electronics products would fail in a matter of minutes. How, then, should engineering managers in organizations that develop high-power electronics ensure the thermal performance of their products while meeting other design criteria?

5 Max Maxfield Looks at the Future of Electronics

Clive "Max" Maxfield has worked for decades in this industry, and in a variety of capacities: Engineer, author, editor, columnist, blogger, and keynote speaker, just to name a few. I caught up with my former columnist recently and asked him what he'd been doing to stay out of trouble, and what sort of technology and futur-

istic electronic gadgets were piquing his interest right now.

6 Rigid-Flex PCB Right the First Time—Without Paper Dolls

The biggest problem with designing rigid-flex hybrid PCBs is making sure everything will fold in the right way, while maintaining good flex-circuit stability and lifespan. The next big problem to solve is the conveyance of the design to a fabricator who will clearly understand the design intent and therefore produce exactly what the designer/engineer intended.

7 The Art of Bending and Forming PCBs

Flexible circuits are designed to be bendable, but bending rigid PCBs is a little unusual. However, many applications that do not use flex circuit technology will also require bending and forming the circuit. Some of these applications use high-frequency circuit materials to create a circuit in a form that enables improved antenna functionality. Another application involves wrapping a circuit around a structure, which sometimes functions as an antenna as well.

8 DownStream Releases New Versions of Industry-Leading Products

DownStream Technologies has released new versions of their industry-leading PCB post-processing solutions, BluePrint-PCB, CAM350, and DFMStream. The releases include many new features and performance improvements designed to help users post-process PCB designs and create and distribute all the deliverables required for a complete PCB assembly release package.

9 Cirexx Installs UCAMCO Integr8tor Software

Cirexx International has acquired and installed the UCAMCO Integr8tor pre-CAM software. This software package affords the user faster and more accurate information for quoting and front-end engineering. With the Integrator tool, Cirexx is not only able to process more quotes, more quickly, but with a greater degree of confidence in having identified all of the challenging attributes of printed circuit fabrication build.

10 The Past, Present, and Future of IPC-A-610

Since 1983, IPC-A-610, Acceptability of Electronic Assemblies, has been the standard used by organizations interested in understanding the acceptability criteria for electronic assemblies around the world. To understand the ultimate power of IPC-A-610, you need to first understand what is at the core of this standard. IPC-A-610 is a collection of visual quality acceptability requirements for electronic assemblies.

events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out *The PCB Design Magazine's* event calendar.

7th Annual SMTA Vendor Show
August 21, 2015
Penang, Malaysia

NEPCON South China 2015
August 25–27, 2015
Shenzhen, China

Capital Expo & Tech Forum
September 1, 2015
Laurel, Maryland, USA

electronica India
September 9–11, 2015
New Delhi, India

productronica India
September 9–11, 2015
New Delhi, India

PCB West
September 15–17, 2015
Santa Clara, California, USA

Medical Electronics Symposium 2015
September 16–17, 2015
Portland, Oregon, USA

SMTA International 2015
September 27–October 1, 2015
Rosemont, Illinois, USA

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October:
Accelerating the Design Cycle

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