THE pcb design MAGAZINE

January 2014

AN I-CONNECT007 PUBLICATION

2013: A Look Back
by Steve Williams
p.16

The Wrap-Up
by Ray Rasmussen
p.22

A LOOK AT 2014

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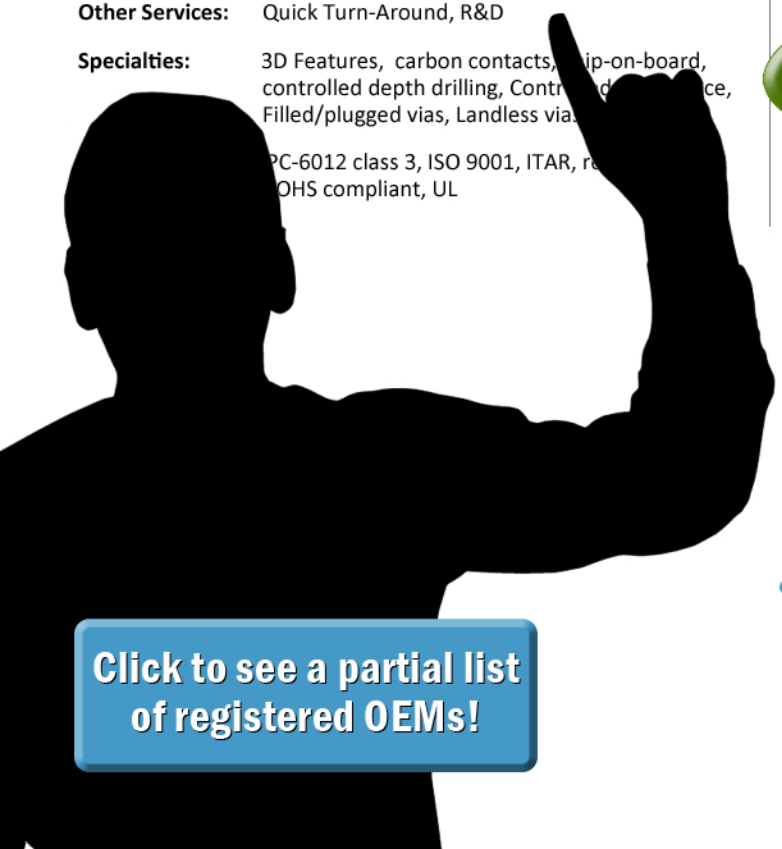

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This Issue: A LOOK AT 2014

FEATURED CONTENT

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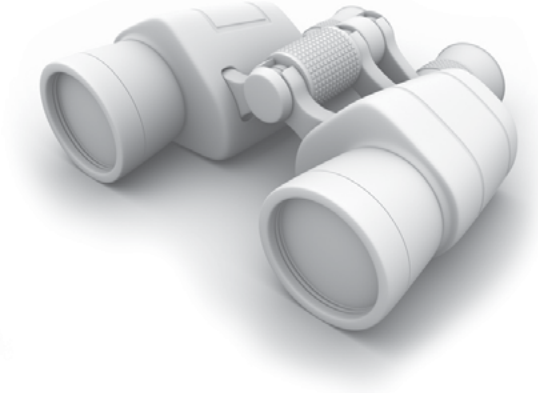

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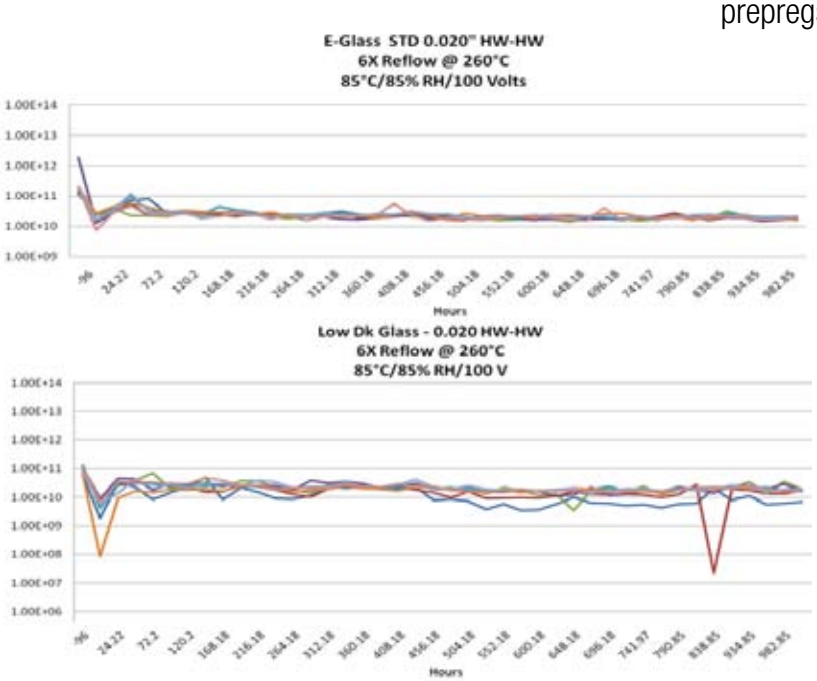

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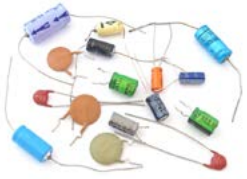

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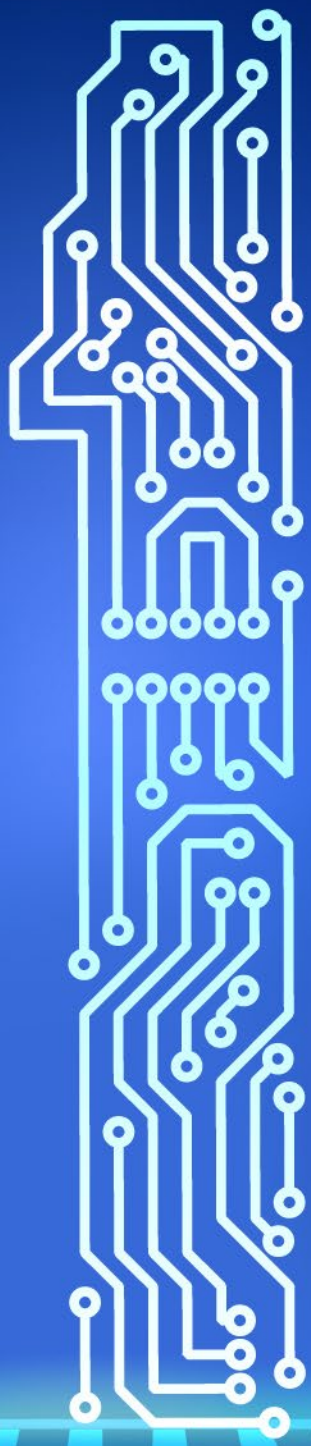

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THE SHAUGHNESSY REPORT

The Old Guard Moves On

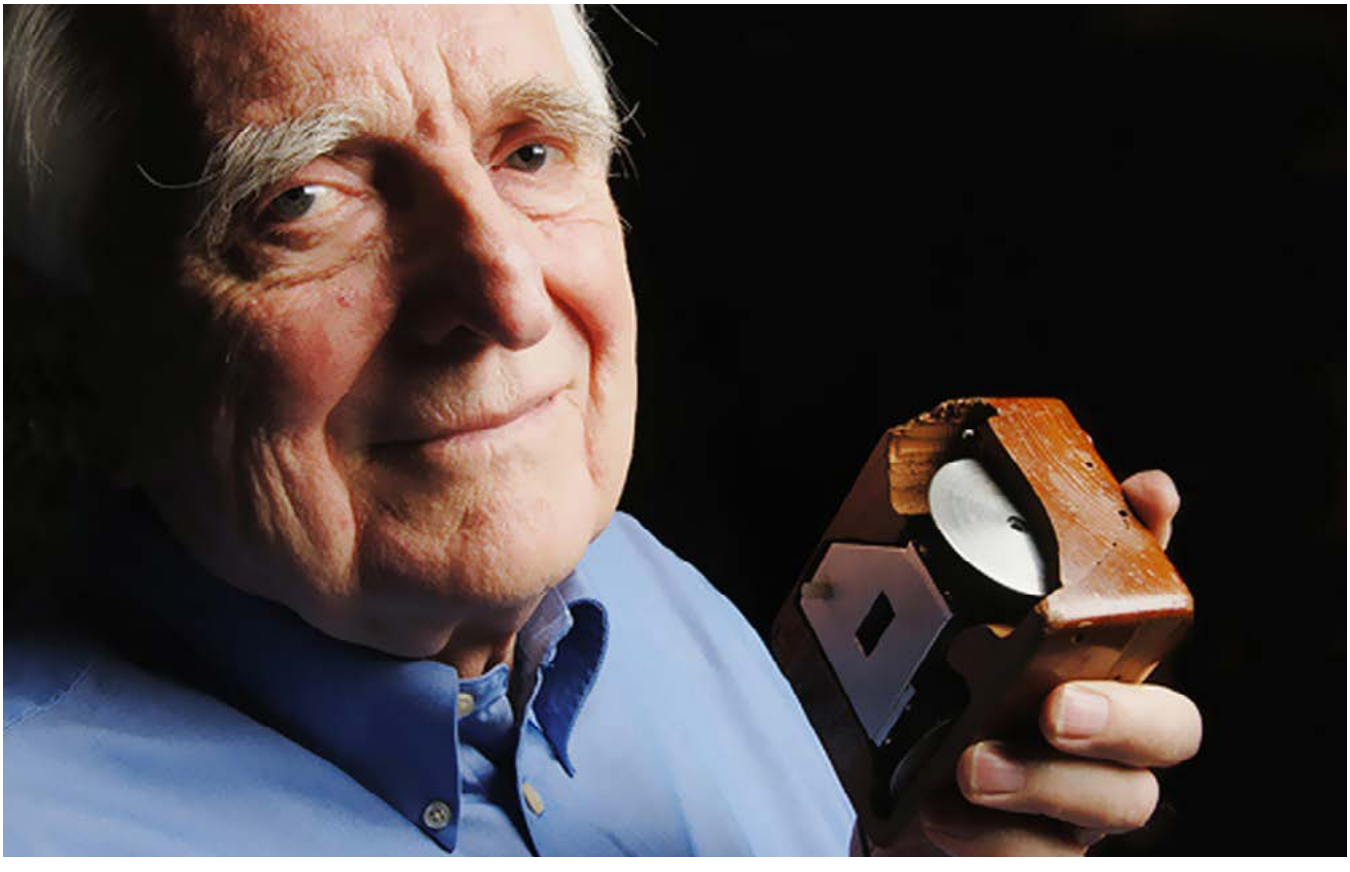
by Andy Shaughnessy
I-CONNECT007

We've officially entered 2014. How can that even be possible? If you look back at the year in terms of trade shows, it seems like we just left IPC APEX EXPO in San Diego. But now, we're gearing up for trade show season again.

The year ahead is ripe with promise. The jobless rate recently dropped to 7%, the lowest in five years, and more jobs were added to the economy in December than analysts expected. And, surprisingly, the U.S. government hasn't shut down in nearly three months! Did the Democrats and Republicans secretly agree to quit calling each other names and actually work together? Probably not, but we can hope.

But before we get caught up in 2014, let's look back at the truly great innovators we lost in 2013. Doug Engelbart, inventor of the computer mouse, died at 88. He served in WWII as a Navy radar technician, and later went to work at the Stanford Research Institute, where he developed the computer mouse in the 1960s and was awarded a patent in 1970.

At first, even his peers wondered why anyone would need such a thing. It wasn't the most technologically advanced idea; it was a wooden box with two wheels and a red button. (It wasn't even called a "mouse" in the patent paperwork.) But it revolutionized the way humans interact with computers, not to mention how we all work and communicate. Engelbart was also a pioneer in the creation of the Internet predecessor ARPANet, hypertext, and video-



Doug Engelbart, inventor of the computer mouse.

conferencing technology, among a long list of accomplishments. But he'll always be remembered for the mouse.

William Lowe passed on at 72. He led the IBM team that developed its first PC in one year, a feat that no one—including IBM—thought possible. IBM was a behemoth, and not known for its quick turnaround time. But Lowe bypassed the firm's usual years-long proprietary development model by using existing technology: The IBM 5150 incorporated Microsoft's MS-DOS 1.0 operating system and an Intel 8088 microprocessor. In 1981, Lowe's idea put IBM at the top of the tech mountain, if only for a while.

Ray Dolby died at 80, with 50 patents to his name, not to mention a few Oscars for his work with movie audio. As a child, he studied the vibrations of clarinet reeds. He got his Ph.D. in physics, launched Dolby Laboratories, and changed sound forever. If you're my age or older, you may remember how music sounded back in the pre-Dolby days, especially guitar-driven rock and roll.

Back then, total harmonic distortion (THD) ratings were a big consideration when buying a stereo. There was so much hiss that I hated to turn up the volume too loud, which made it tough to enjoy the music. But then stereos started appearing with this magical button marked "Dolby," and that was the beginning of true high-fidelity, at least in my mind.

I remember looking at my new Panasonic cassette/turntable stereo and thinking, "When would I ever not want to use the Dolby button? Why not just build Dolby into the system?" The first generation of Dolby wasn't perfect—it cut out some of the middle and treble frequencies. But it allowed us to turn the music up louder than we ever could before, and for that, we audiophiles owe Ray Dolby a great debt.

Eiji Toyoda, the creator of the Toyota Way, passed away at 100. He joined his uncle's car company and pioneered the development of Lean manufacturing, kaizen, kanban, zero defects, and a host of other production concepts used by PCB assemblers today. Toyoda had an uncanny ability to spot inefficiencies in any type of operation, and he prodded his engineers to study W. Edwards Deming so they could learn to increase productivity and quality. He also pushed Toyota to start manufacturing cars overseas, and to enter the luxury car market.

And Yvonne Brill, creator of a variety of innovations in rocket propulsion, died at 88. Possibly the only woman working as a rocket scientist in the 1940s, she holds a patent for her electrothermal hydrazine thruster (EHT), which to this day helps keep communications satellites in geosynchronous orbit.

When she was denied entry into an engineering program because of her gender, Brill earned a mathematics degree instead, graduating at the top of her class. Brill worked for Douglas Aircraft, RCA Astro Electronics, and NASA, and took home a slew of honors. President Obama presented her with the National Medal of Technology and Innovation in 2011.

Yes, the old guard—people who made huge, disruptive contributions to technology—are slowly moving on. But the innovation continues, and we're all a part of it, in one way or another. That's the great thing about the electronics industry.

It's Show Time

It's that time again. We'll be bringing you *Real Time with…* video coverage of the industry's hottest trade shows, starting with DesignCon, January 29-30, 2014, at the Santa Clara Convention Center. The exhibition has been moved back one day, so the show runs Wednesday and Thursday instead of the usual Tuesday and Wednesday.

Then we move on to the CPCA Show in Shanghai, March 18-20, followed almost immediately by IPC APEX EXPO March 25-27 at Mandalay Bay in Las Vegas. Who needs sleep? It's an exciting time, and we hope to see you on the road.

Happy New Year! **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 13 years. He can be reached by clicking here.

New Year's Resolution: Validate Your Model Data

by Todd Westerhoff
SISOFT

***SUMMARY:** As we begin 2014, remember: Signal integrity simulations are only as good as the models that go into them. But how thoroughly do we really validate simulation models before we use them?*

Sure, you'll have plenty to worry about in the upcoming year. But here's an idea to consider that might save you some time and money in 2014: Do you test and correlate simulation models, or do you just take someone else's word for it?

When we do take someone else's word for it, is there written evidence of that testing and correlation, and do we take the time to review it? Let's be honest—we all want fast, accurate simulation models with plug-and-play simplicity. Testing simulation models is difficult, time-consuming and a general pain in the neck. We know that if we really take a close look at most of the models we use, we'll likely raise questions that take time to resolve—time that most of us don't have in our project schedules.

There are two types of models involved in SI simulation: interconnect and semiconductor models. Interconnect models include transmission lines, vias, connectors and passive components. They may be represented in the simulation as individual elements or they may be combined together and provided as S-parameter data. Semiconductor SI models can be a type of SPICE (there are multiple variants), IBIS, IBIS-AMI, or a model that is designed to run in a par-

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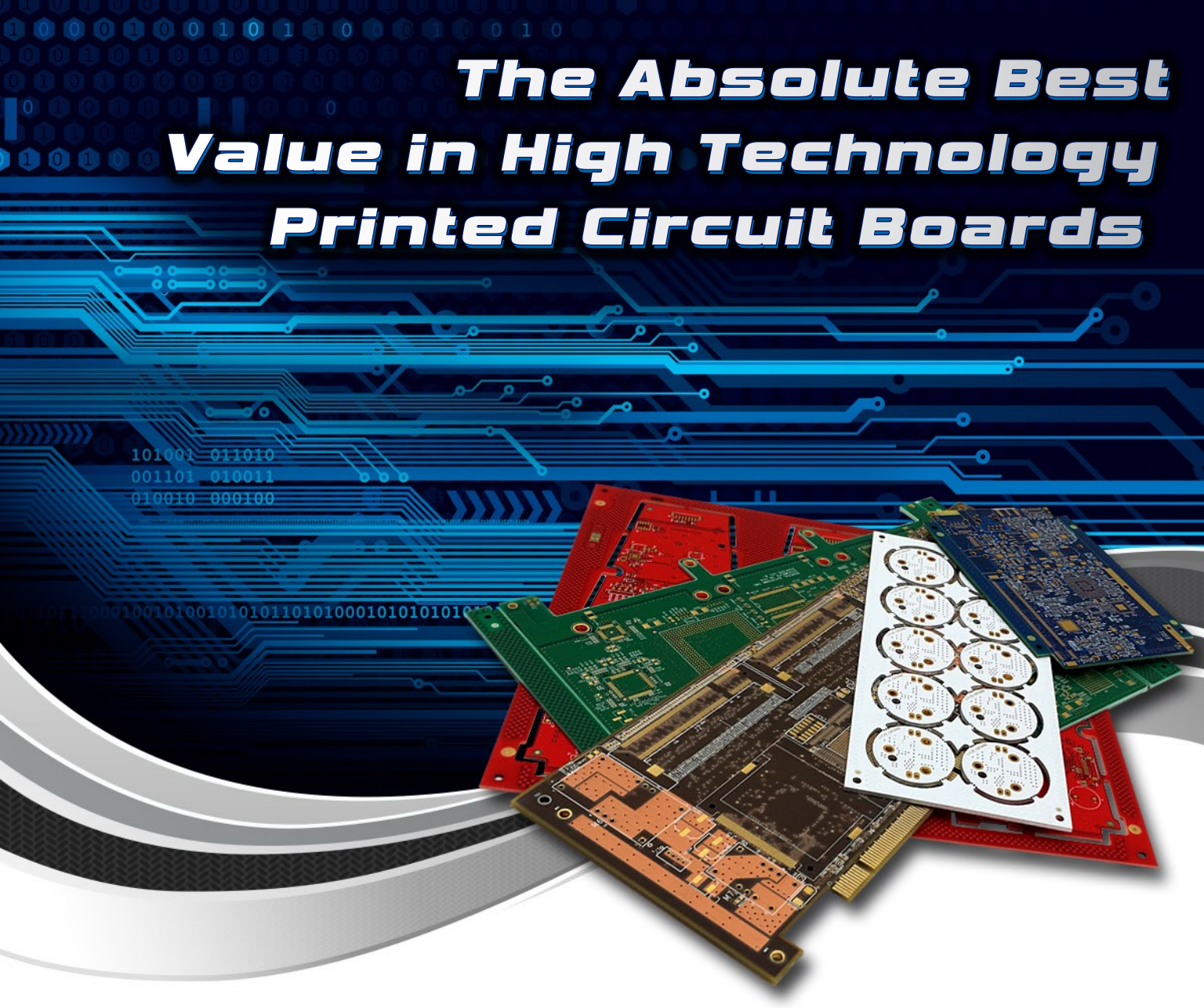

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ticular semiconductor vendor's simulator. There are other types of models as well, but these are the types that most users have to contend with. Each type of model has its own unique characteristics, limitations and typical quality problems. If you spend enough time working with a particular class of model, you'll probably develop techniques for verifying those models before use in system simulations.

Why should you care? Well, if you're using the results of system simulations to make design decisions, you should care a lot. A prototype board run for a high-end system can cost $100,000, plus the time it takes to get assembled boards back and running in the lab. Bad design decisions that result from poor models can delay a product's ship date by months and the lost sales could probably pay off your house. So, model quality matters, but the real question is whether users are in a position to do anything about it or not.

For example, let's look at S-parameter models, which are useful for all sorts of applications. In practice, there are limits as to how accurate most S-parameter models are. Since they are frequency-based models, they should specify how energy is transferred all the way down to 0 Hz, or DC. S-parameters can be created either analytically (often through the use of 3-D field solver software) or empirically (derived from measurement). Both techniques often have trouble generating the DC portion of the S-parameter file accurately. Why does it matter? It matters because many simulators perform a steady-state (DC operating point) solution before beginning transient (waveform) analysis. If the DC characteristics of the circuit are off, the operating point will be off, and the quality of the transient analysis may be compromised as a result.

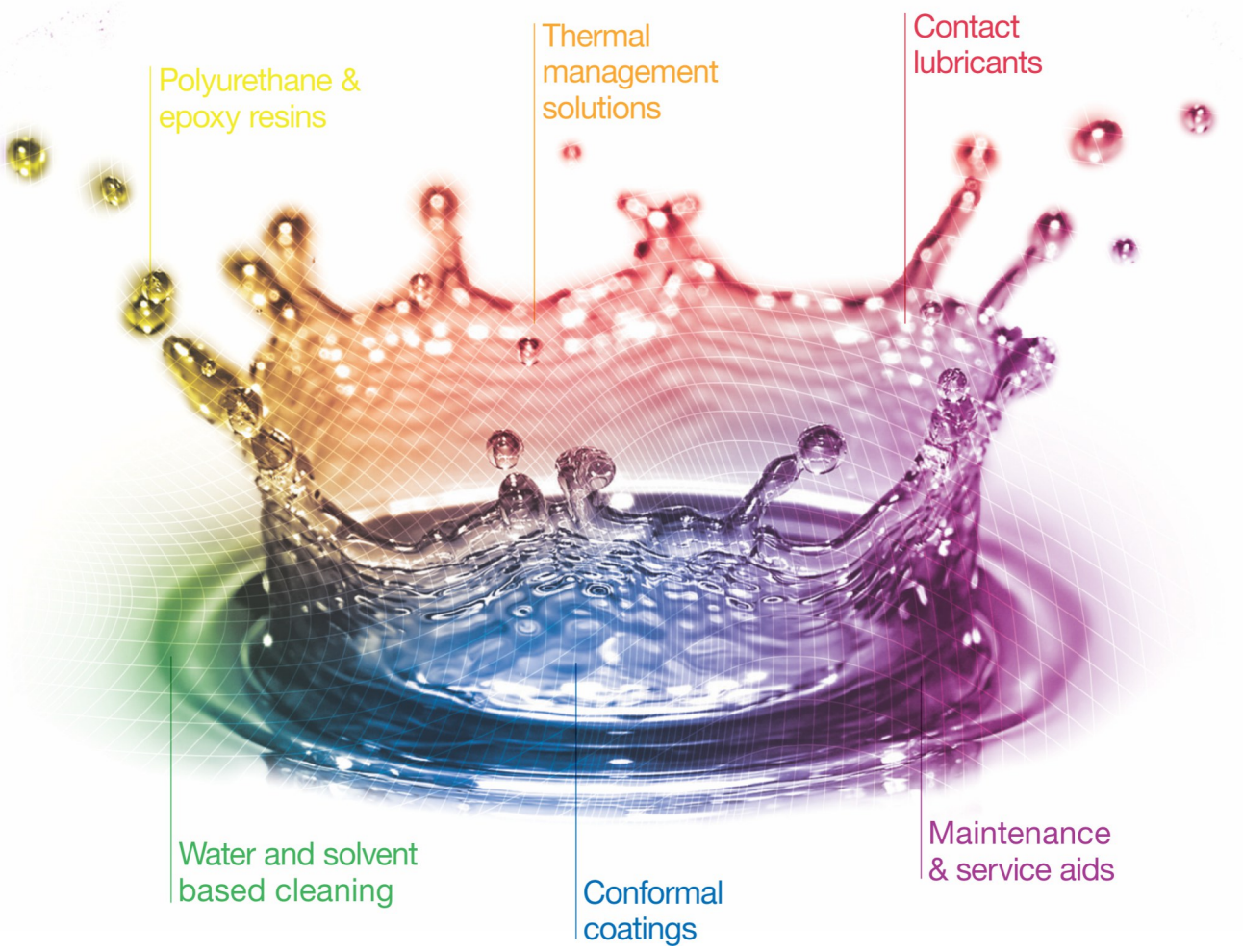
A prototype board run for a high-end system can cost $100,000, plus the time it takes to get assembled boards back and running in the lab. Bad design decisions that result from poor models can delay a product's ship date by months and the lost sales could probably pay off your house.

What's a user to do? While there are numerous programs that claim to "detect and correct" issues with S-parameter data (causality and passivity being two of the most popular issues), we maintain that users should take a close look at S-parameter data before letting a computer program change it. This means developing techniques to evaluate the quality of S-parameter data. Dr. Michael Steinberger's article TDR: Reading the Tea Leaves outlines the use of TDR techniques to do just that. Designers can use these techniques to understand the topology that the S-parameter data describes and its key characteristics. If those characteristics don't reasonably match the circuit being modeled, then there's really not much point in worrying about whether the data is passive and causal and how it might be corrected.

The same is true for semiconductor models. Basic characteristics of the I/O circuitry—output and termination impedance, voltage swing, ESD capacitance, slew rate, non-linearity, equalization and more—can be observed by exercising a model under the right test conditions. If the model meets reasonable expectations, great—it's time to start running system design simulations. If not, it's time to figure out what's going on with the model before running simulations that will have to be rerun later anyway.

As I write this, I can't help but think that I'm coming across as a spoilsport. I imagine the grumpy old man sitting on his front porch, yelling at kids who walk across his lawn, except that he's saying, "Mind your S-parameters, young man! Test your I/O models to make sure they accurately represent return loss!"

As I've already conceded, testing simulation models is neither quick nor enjoyable. And



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based on conversations with customers, it's not terribly popular either. So why do I keep going on about it? Because it's important, and because I've been burned too many times. In my former job, the scenario would repeat itself: We'd put together a project schedule that was too aggressive to begin with, and then the models would show up late.

Instead of running the tests we planned, we'd run quick tests to make up time, and the models would look good (they always looked good at first). Then we'd use them for a week or two before we noticed some discrepancy in simulation results, trace it back and realize the model had been bad all along. The scenario repeated itself so many times that we finally compiled a list of all the ways we had been burned, defined an incoming model inspection process and stuck to it. It didn't solve all our problems, but things did get better.

If this were a sales pitch, I would pull out the magic answer to the problems I've posed. "Do you have problem SI models that are difficult to test? No problem! Try new SI TestAll with Borax! Your simulation models have never been so fast and so clean!"

Of course, that's the exact opposite of what I'm trying to say. I'm saying that we, as designers, need to do the hard work of understanding whether we can trust our models before we start using them to make design decisions. That message isn't glitzy and it isn't exciting, but it is critically important if we want to use SI simulations to create high quality products.

Welcome to 2014, and stay off my lawn!

PCBDESIGN

Todd Westerhoff is vice president of semiconductor relations for SiSoft, has over 34 years of experience in the modeling and analysis of electronic systems, including 17 years of signal integrity experience. He can be reached by clicking here.

video interview

Dragon Circuits: Old Company, New Name and Ideas

by Real Time with... SMTAI

Raj and Gunny Barbaria acquired North Texas Circuit Boards and began rebuilding the failing company. After shedding some longtime employees and investing in new equipment, the two say they are ready to make Dragon Circuits into a 21st century technology company. They also discuss their drive to make PCBs attractive to the next generation.

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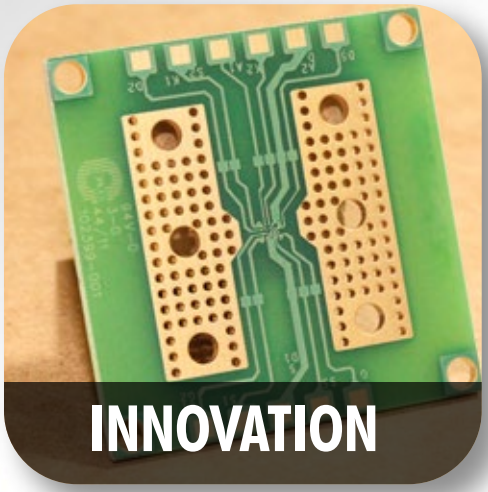

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POINT OF VIEW

2013: A Look Back

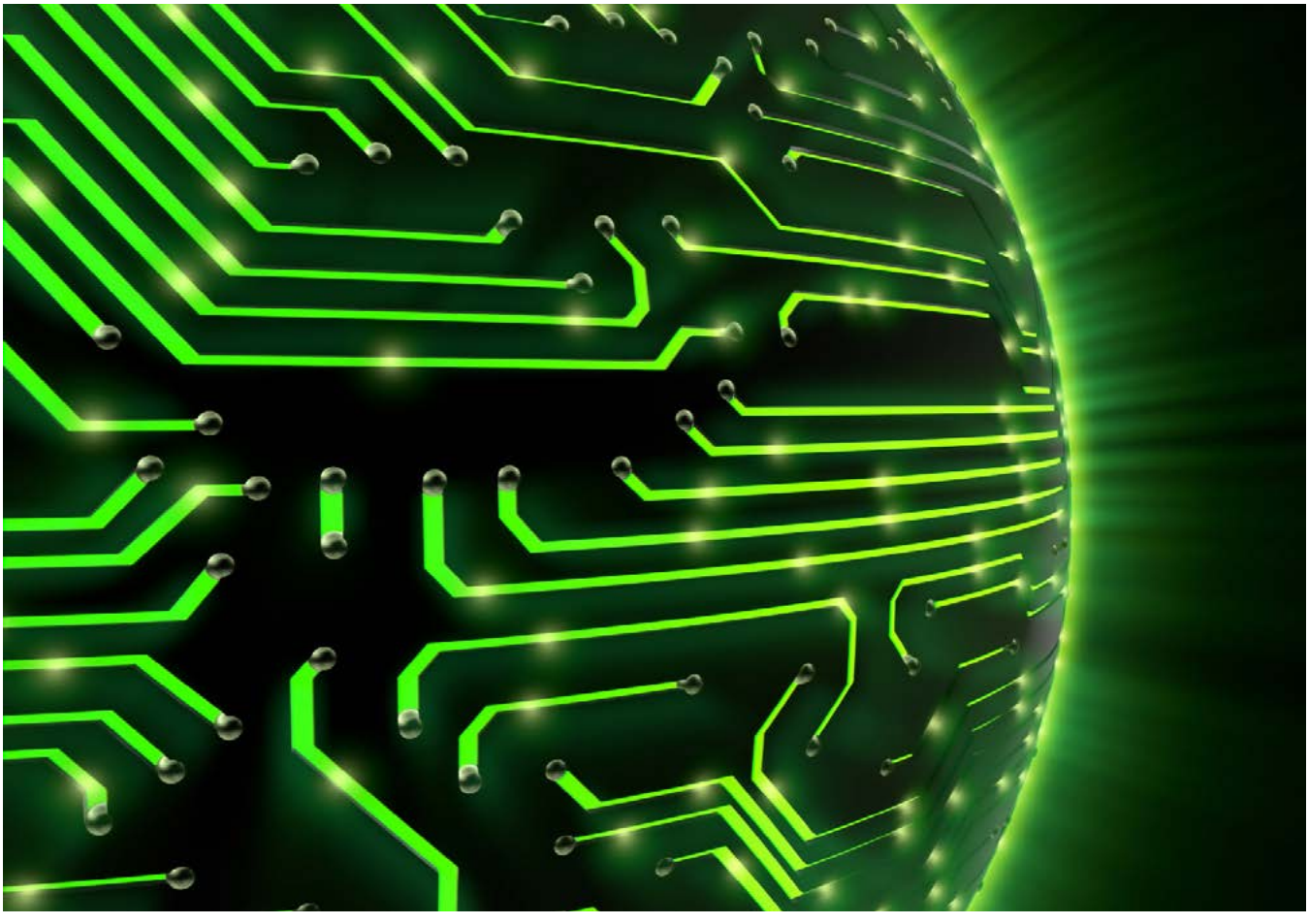
by Steve Williams

After a very challenging year for the domestic PCB industry, global business conditions are slowly improving. Let's take a look back at 2013 and also a look forward to what we can expect as we move into the New Year.

Like many of you, I grew up in this business. I cut my teeth (and more than a few body parts) in this industry working for my dad in the family business. At the risk of dating myself, this was well before the advent of CNC machines, CAD/CAM and automatic plating equipment. Throughout the past three decades, I have been proud to see this business grow into the professional industry it has become. I am vested in the success of our industry; it matters to me.

2013 News Flash: The U.S. economy is still not working!

After a number of false starts, missteps and failed technologies in the renewable industry, solar/photovoltaic demand is beginning to recover. Europe's tighter fiscal policies have squeezed consumer purchasing power and increased sovereign-debt tensions, which has an impact on global business. U.S. consumer confidence has not improved and is still hovering around 80%. The unemployment rate is 7.2% (published), which is bad enough, but after factoring in the millions of people that are no longer counted because they have flat-out quit looking, the "real" unemployment number



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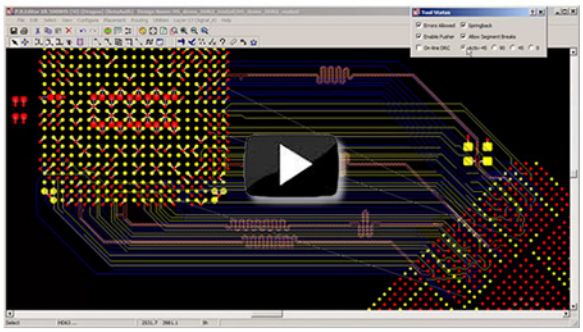

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2013: A LOOK BACK *continues*

is somewhere north of 14% (Forbes/BLS). The U.S. is dead last in the world for Gross Domestic Product growth in 2013 at 1.7%; forecasts for 2014 are only slightly better, at 2.8%, pulling ahead of only Japan and the EU.

Whether it is RoHS, conflict minerals or the EPA, restrictive legislation continues to make it harder for PCB manufacturers to not only make a profit, but survive. Look for the biggest to get bigger through acquisitions both domestically and globally.

In 1990 there were roughly around 1,000 U.S. printed circuit board manufacturers; in 2000 there were 700, and in 2010 the number of domestic shops had fallen to only 365. Unfortunately, I fear this number will be less than 300 by the end of 2015,a short two years away. Where the U.S. market needs to continue to compete are QTA/proto business, advanced technology and short run orders.

> ***Apple plans to move $100 million of Macintosh computer manufacturing back to the U.S. While this may be a public relations move on Apple's part, it is still $100 million worth of work coming back.***

Global PCB Snapshot

The global printed circuit board industry's total available market is currently at a little more than $60 billion, with Asia still dominating world production. There are a little over 2,900 printed circuit board manufacturers globally, and the United States held onto its fifth-place rank with just under a 5% share, which may look encouraging. However, this is extremely misleading as the top four countries are responsible for 89% of the total global PCB pie. People much smarter than me are only forecasting single-digit growth of the industry for the next five years.

Bright Spots Looking Forward

There are a few positive signs looking forward: Leading indicators are rising in some regions and new product designs are starting to show some life. The overall world PCB production is increasing (100% growth over the past 10 years), which will continue to present more opportunities for the U.S. market.

Much of the talk at April's IPC APEX EXPO was how to bring manufacturing back to the U.S. *Onshoring* (the preservation of existing manufacturing in America) is increasing as a result of U.S. companies becoming more globally competitive through efforts such as Lean, product design, reduced labor cost through increased efficiencies, and improved customer responsiveness. *Reshoring* (the return of work to America that had been previously lost to offshore competition) is also on the uptick. China's rising labor costs, political unrest and weaker exports are driving this trend. Apple plans to move $100 million of Macintosh computer manufacturing back to the U.S. While this may be a public relations move on Apple's part, it is still $100 million worth of work coming back.

Smart Connected Devices

"I think there is a world market for maybe five computers."

—Thomas Watson, chairman of IBM

"There is no reason for any individual to have a computer in his home."

—Ken Olsen, founder of legendary minicomputer company DEC

"So we went to Atari and said, 'Hey, we've got this amazing thing, even built with some of your parts, and what do you think about funding us? Or we'll give it to you. We just want to do it. Pay our salary; we'll come work for you.' And they said, 'No.' So then we went to Hewlett-Packard, and they said, 'Hey, we don't need you. You haven't got through college yet.'"

—Apple Computer Inc. founder Steve Jobs, on attempts to get Atari and HP interested in his and Steve Wozniak's personal computer.

Fortunately, these three boneheaded visions couldn't have been more wrong; printed circuit boards are the backbone of electronic technology and have taken us to a place that none of these "prophets" could have imagined in their wildest dreams. The smartphone market is approaching a billion units a year with tablets adding another 400 million to this number. Every one of these devices has at least one printed circuit board that needs to be redesigned and replaced with each new generation launch.

Keep Your Chin Up

Process equipment manufacturers are growing at a solid rate, which is a positive indicator for the PCB industry as a whole. Laminate and other material suppliers are also showing slight growth. So 2013 was a bit of a wash, but in this economy that is a win and with any luck, 2014 looks to be a little better. **PCBDESIGN**

This column appeared in the December 2013 issue of The PCB Magazine.

Steve Williams is the president of Steve Williams Consulting LLC (www.stevewilliamsconsulting.com) and the former strategic sourcing manager for Plexus Corp. He is the author of Quality 101 Handbook and Survival Is Not Mandatory: 10 Things Every CEO Should Know About Lean. To read past columns, or to contact Williams, click here.

Graphene Sees the Light

Graphene, a one-atom-thick sheet of carbon that is extremely strong and conducts electricity well, is the thinnest material ever made. Researchers believe that it could be used as a transparent electrode in photovoltaic cells, replacing a layer of indium tin oxide (ITO) that is brittle and becoming increasingly expensive.

Wee Shing Koh of the A*STAR Institute of High Performance Computing in Singapore and co-workers have compared these two materials. They found that graphene outperforms ITO when used with solar cells that absorb a broad spectrum of light.

Square sheets of graphene produced by today's chemical vapor deposition technology have an electrical resistance roughly four times that of a typical 100-nanometer-thick layer of ITO. Although adding more layers of graphene reduces its resistance, it also blocks more light. Koh and his co-workers calculated that four layers of graphene stacked together had the best chance of matching ITO's performance.

Graphene has one key advantage over ITO: it allows more than 97% of light to pass through to the solar cell beneath, regardless of its wavelength. In contrast, ITO tends to block certain wavelengths more than others.

"With the refinement in the graphene manufacturing process, it would be possible for the sheet resistance of graphene to be an order of magnitude lower than the current state of the art," says Koh. This would allow just one or two sheets of graphene to beat ITO on both conductivity and transparency, making graphene transparent electrodes much more widely applicable.

PCB007 News Highlights

IPC: October PCB Sales, Orders Up; Book-to-Bill Dips

"Although both sales and order growth are trending up compared to last year, sales have outpaced orders in the past three months, causing the book-to-bill ratio to dip," said Sharon Starr, IPC's director of market research. "Year-on-year sales growth has been improving for the past six consecutive months and finally turned positive in October."

Viasystems Opens World-class Factory in California

Designed to consolidate the sprawl of 13 buildings that used to represent DDi's PCB business, the new factory is housed in an ex-MFLEX site and was constructed from scratch. This enables the company to service its very high-end customers, both military and commercial OEMs, who are looking for the latest in HDI, high-reliability PCBs for their products.

PCBs for LED Lighting: The Times They Are a-Changing

BPA forecast that the market for PCBs providing enhanced thermal and power management will reach over $3.2 billion by 2020. BPA discusses some of the research in their report "Metal in the Board—Opportunities for Printed Circuits Providing Thermal and Power Management 2012-2020."

Wurth Elektronik: HDI Microvia PCBs Now Available

The HDI specialist Würth Elektronik has set new standards in the PCB industry: HDI microvia PCBs are now available in its online shop, WEdirekt. With just a few clicks, your HDI PCB is calculated and the price is shown immediately online. Ordering prototypes is considerably simplified and faster.

Canadian Circuits Acquires Oxford CMI 900 Unit

Praveen Arya, president and owner of Canadian Circuits Inc., announces that his company has acquired a new Oxford CMI 900 X-ray fluorescence coating thickness measurement system as part of the company's complete equipment upgrade.

PCB Solutions Offers Expanded Stocking Program

Effective in December 2013, PCB Solutions is pleased to announce offering enhancements to their stocking program. PCB Solutions is now offering a complete stocking program that enables customers to take advantage of volume pricing, but assists them with cash flow and inventory relief.

SOMACIS Receives Innovation Award from JDSU

At the 2013 JDSU Global Supplier Day SOMACIS received the "Excellence in Value Innovation" Award. This recognition confirms SOMACIS' focus in delivering innovative solutions through high-tech PCBs combined with co-design services.

Cicor Realigns from Four Divisions to Two

Cicor, an international high-tech industrial group and leader in the fields of PCBs, microelectronics, and electronic solutions, headquartered in Boudry, Switzerland, is optimizing its existing organizational structure to better align with customers' future needs.

Integral's Zeta Certification Awarded to Eagle Circuits

Integral Technology Inc., a manufacturer and distributor of HDI electronic materials for the PCB industry, has announced that Eagle Circuits of Dallas, Texas, has received the prestigious Zeta® Certification allowing them to produce circuit boards using Integral's revolutionary dielectric films.

AT&S: EmPower Consortium Aims to Optimize Energy Use

Targets include the improvement of processes for semiconductor manufacturing, development of new concepts for component packaging, and design of products for optimum management of energy.

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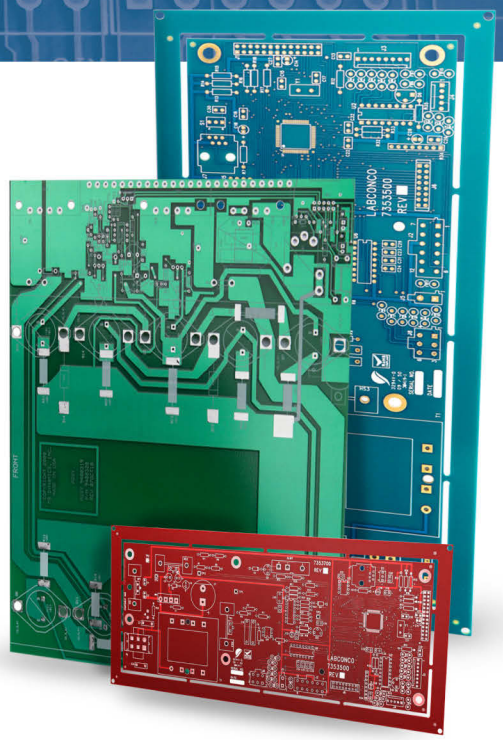

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THE WAY I SEE IT

The Wrap-Up

by Ray Rasmussen
PUBLISHER, I-CONNECT007

Good Riddance

Tying up 2013 into a nice, tight bow, tossing it over my shoulder and then dusting off my hands comes to mind when trying to wrap up the year. I didn't much like the year that was.

Politics seemed to take center stage for most of us as those we elected to keep us on track did nothing to improve the economy.

A few changes should be noted. On the PCB side of things, we lost Endicott Interconnect Technologies to bankruptcy and in August, Hitachi Via Mechanics sold to the Longreach Group. Hitachi has claimed the global top spot over the last decade, filling Chinese factories with their drilling equipment. The reliance on that low-margin sector, even though they sold a ton of machines, may have cost them their business.

TTM COO Shane Whiteside left the company "to pursue other opportunities," and a few months later, his boss, Kent Alder, retired. Those two built one of the world's largest PCB companies, but it makes you wonder. Their departures were so close together, it almost feels like they were jumping ship, although there aren't any indications that there's anything wrong with the company. The stock is doing fine. But it makes you think.

Other notable M&A activity includes Kyocera buying NEC Toppan Circuit Solutions; Graphic Plc buying Calflex; Elga Europe entering into a joint venture with Eternal Chemical;

Mentor Graphics

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THE WRAP-UP *continues*

Eltek joining with Nistec, an Israeli EMS provider; R&D Circuits acquiring PCB design company Altanova; EPEC and Suncoast Digital joining forces (EPEC also purchased UPE back in January to enhance its extreme copper technology); China's Fastprint picked up eXception's PCB business; SMG and Global Circuits merged operations; Yash Sutariya's management team purchased Alpha Circuit Corp; Zutron acquired Teknoflex; andAll Flex started off the year acquiring Tri-C Design.

On the EMS side of things, CirTran finally got out of the EMS business and is now putting all of their focus on beverages. I have not spent time figuring out how and why they made the switch from electronics manufacturing to playboy energy drinks. Not a big loss, I guess. CTS also left the industry, selling its EMS capabilities to Benchmark Electronics so that they could focus on their sensors and components business. I guess focus is good. Hunter Technology acquired NBS's design assets; Natel bought EPIC Technologies, while assembly equipment supplier Essemtec sold its operations to a private investor group. GE bought Imbera Electronics to advance its capabilities into advanced embedded electronics packaging. LTX-Credence bought Dover's Multitest and ECT, while Molex bought FCT Electronics, only to be acquired by Koch one month later.

Flextronics made a few acquisitions, picking up RIWISA to strengthen its position in medical. They also picked up a couple of factories from Motorola Mobility (Google), one in Brazil and the other in China. Sparton bought Creonix to strengthen its mil/aero offerings and also picked up Aydin Displays. They bought Onyx at the end of 2012.

Jabil bought Nypro; OSI bought Briton EMS; Season Group acquired OEL; ENRI merged with Abotron; eXception Group sold to TPG, Goldman Sachs; Probe bought Trident; JUKI and Sony merged their SMT equipment businesses.

Moving On

China's been sucking wind most of the year. Seems like things are improving but it's anybody's guess. China's official numbers are suspect at best.

Europe is finally coming out of recession, which is good, but it will take some time for things to get moving again.

In the U.S., we've had to deal with the repercussions of the budget sequestration (artificial slowing of the economy) and the government shutdown by a few radicals (another artificial slowing of the economy). It's been painful. We need to pull out all the stops and allow the economy to grow at full speed. We can work on the structural stuff later, once we have full employment and tax revenues flowing in. We take two steps forward then one step back. It's crazy.

> ***"As one gentleman from Raytheon said at the recent tin whiskers conference, they haven't seen any increase in failures due to whiskers, but he also acknowledged they are spending a ton of money to ensure that."***

Market news is getting the most reader interest from our websites. Anything with market information seems to be of great importance these days. Leading indicators from The Conference Board captured the most attention. Those indicators have been climbing for most of 2013, which is a good thing, just not fast enough. All economists believe economic growth is being hindered by partisan politics in the U.S. Congress.

IPC continues to evolve and along with it, some more personnel changes. We've lost Susan Filz (conference coordinator) and Mary MacKinnon (APEX show sales). IPC has also added PERM into the stable of groups under its control. PERM is a group working to help high-reliability companies move to lead-free. Driven mostly by mil/aero suppliers, they're working hard on a solution for tin whiskers. They made some good, but rather expensive progress. As one gentleman from Raytheon said at the recent tin whiskers conference, they haven't seen any increase in failures due to whiskers, but he also acknowledged they are spending a ton of money to ensure that.

IPC also broke bread with SMTA by co-locating their fall meeting in conjunction with the SMTAI show. It seemed to work well for both groups. Let's hope for more cooperation and, ultimately, the merger of these groups.

A bright spot for me in 2013 was the new Viasystems factory in Anaheim. I liked that. It's good to see what may be a taste of things to come. Let's hope so.

Looking ahead

What can we expect in 2014? I'm optimistic. It sure seems like the market is ready to roll if politics can stay out of the way. That's the only area of real concern I have. When you look at the raft of new technologies under development, conventional and alternative energy, printed electronics, 3D, new products based on exciting materials like graphene, the U.S. and Europe are in pretty good position to capture serious market share. Those innovations will translate into some type of electronics, which will drive our industry forward. The U.S. now has a pretty solid and reliable energy supply. Huge improvements to the energy infrastructure will keep energy prices relatively stable for years to come—a huge benefit for our manufacturers. This gives companies confidence that the costs of manufacturing will be fairly stable as they expand their businesses., Infrastructure and rule-of-law (IP protection), proximity to customers, and low levels of corruption are advantages we have over most of the developing world.

As a result, I think we'll see some surprising on-shoring initiatives in 2014 as companies make the move back to North America. China will continue to lose its luster. Things are beginning to come back into balance.

Another change we're starting to see and will continue to see expand in 2014 is the number of talented young people entering the industry. It has been a cry heard for years at industry events: *Where are all the young people? How can we get them involved in the industry?* Actually, these engineers, product designers, and entrepreneurs have discovered our industry because of printed electronics and 3D printing. They're going to rock our world. They don't have the mindset we all have. They're going to develop the systems to build the electronics of the future, not based on what we know with traditional PCBs but on PE and 3D platforms. So for those of you who've been wondering where all the young people are, ask no more.

What will we see from the PE and 3D sectors in 2014? No big gamechangers, really. Just lots more low-cost prototyping systems. In a recent PCB assembly association survey, printed electronics scored highest as the area of greatest interest for its members. Just a couple years ago, PE was hardly on anyone's radar.

The link below is an example of the kinds of efforts being made by GenZ (get it, Z axis, third dimension) of circuit manufacturers.

Circuit-printing startup reaches 30-day kickstarter fundraising goal in 5 hours

And to help us get a glimpse of the kind of energy going into this, Oak Ridge National Lab is giving 35,000 3D printers to U.S. schools. Again, the lack of young people in our industry won't be an issue for long. It's just not going to be the industry we're used to. Read more about this initiative here.

Tremendous opportunity awaits all those who grab it, and 2014 holds a lot of promise for our industry. You have to open your eyes, though, to see it. I'll leave you with a few famous quotes on the topic. **PCBDESIGN**

The reason a lot of people do not recognize opportunity is because it usually goes around wearing overalls looking like hard work.

—Thomas A. Edison

A pessimist sees the difficulty in every opportunity; an optimist sees the opportunity in every difficulty.

—Winston Churchill

Ray Rasmussen is the publisher and chief editor for I-Connect007 publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuiTree Magazine.* To read past columns, or to contact Rasmussen, click here.

An Introduction to Rigid-Flex Design Best Practices

by Ben Jordan
ALTIUM

SUMMARY: ***Once considered too costly by many designers, rigid-flex circuits are becoming more prevalent every day. Now designers are learning how to deal with this seemingly schizophrenic product format.***

Designers increasingly face project requirements for densely populated electronic circuits, including pressures to reduce manufacturing times and costs. To meet these requirements, design teams have increasingly turned to 3D rigid-flex circuits to meet their project's performance and production requirements. As a first step, rigid-flex designs require closer collaboration between the designer and fabricator than traditional board-and-cable designs. The trade-offs required to produce a successful rigid-flex design translate to a set of design rules the designer can develop with the fabricator's input. These considerations include the number of layers in the design, materials selections, recommended sizes for traces and vias, adhesion methods, and dimensional control.

In the past, seasoned PCB designers bypassed rigid-flex circuit design by connecting two rigid PCBs with a flexible cable. This approach worked well for short-run designs. However, this approach adds the cost of connectors on each board, the cost of assembling the connectors to the board, and the flexible cable. In Figure 1, the chart maps the cost trade-off between a traditional rigid PCB-and-cable assembly and a 3D rigid-flex design.

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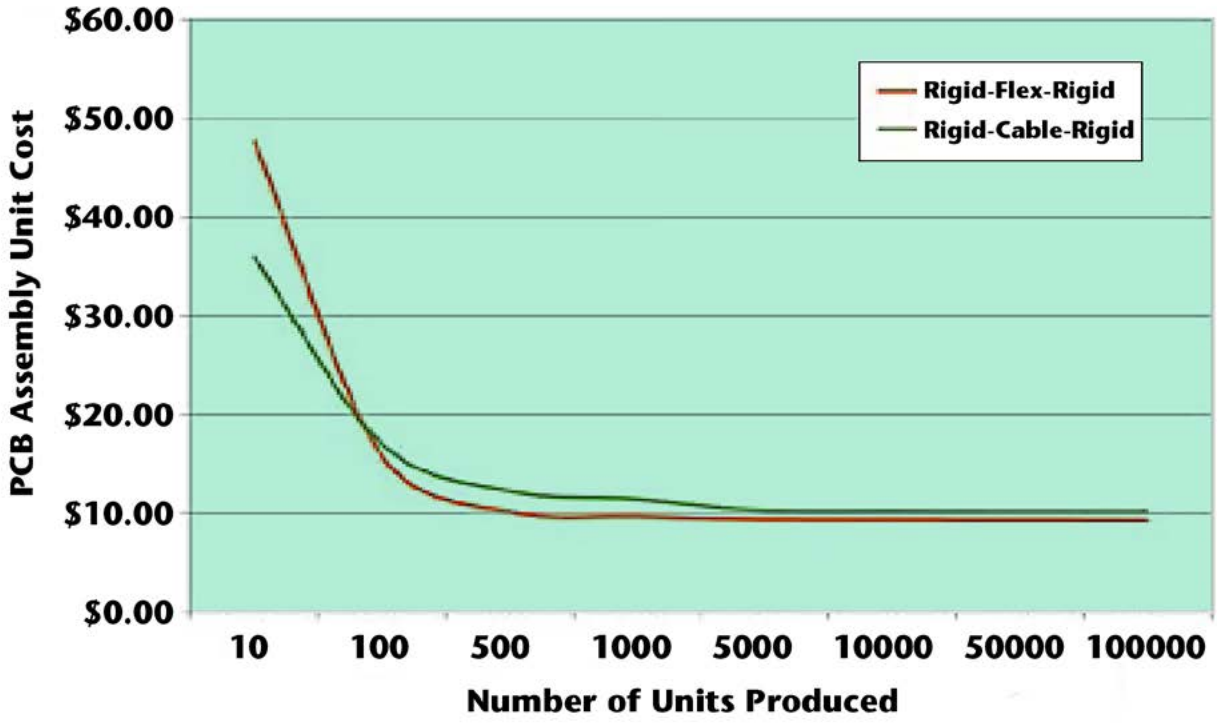

Figure 1: Quote-generated cost comparison of rigid-flex design vs. rigid-cable-rigid PCB assembly.

This chart relies on simulated manufacturing costs based on real PCB fab quotes for a four-layer PCB with two inner flex layers in a rigid-flex board. The alternative, rigid boards using flexible cable and connectors between them, is also based on quotes from PCB fabricators. In the latter case, the calculation totals the costs of two separate four-layer boards plus the costs of connectors and cable including assembly costs for both alternatives. This calculated "what-if" scenario does not take into account the improvements in reliability and overall higher product quality of the rigid-flex circuit. Among other reasons, the individual boards with flexible connectors and cable can form electrically "cold" joints, causing malfunction. By comparison, the rigid-flex circuit obviously eliminates these joints.

Surprisingly, as soon as the project involves any volume over 100 units, a rigid-flex circuit design becomes the obvious choice. Why? Because rigid-flex designs eliminate connectors, connector assembly, and increase reliability and process yields.

Until recently, when a traditional PCB designer first tackled a rigid-flex design, the available PCB design tools did not support board design in 3D. Existing tools also did not support defining and simulating bends and folds in the flex portion of the design. Worse yet, they didn't even support defining different layer stacks in different parts of the design or even what areas constituted the flex part of the design.

As a result, rigid-flex designers had to manually determine how to translate a 3D design of the rigid and flexible sections into a flat, 2-D representation suitable for fabrication. This further required them to manually document all areas that were flexible. They also had to double-check to ensure that they did not place components or vias near the transitions between rigid and flexible portions of the design. This also included many additional rules which were mostly not supported in the PCB design software at the time.

As suggested earlier, any successful rigid-flex design requires that the design team work closely with the fabricator. The following Golden

Rules for the project aim for successful production and eliminating preventable re-spins.

Golden Rules

- Communicate with the fabricator!
- Qualify the fabricator's capability to build the planned rigid-flex design.
- Involve the fabricator as early as possible in the design process.
- Collaborate so the design's layer stack matches the fabricator's processes.
- Use IPC-2223 as the common point of reference with the fabricator. Otherwise, communication in the form of documentation can cause errors and misunderstandings resulting in costly delays.
- Graduate from delivering Gerber files to the fabricator. Instead, deliver files in ODB++ (v7.0 or later) or in a format that meets IPC-2581 because either format identifies specific layer types for clear documentation.

For a successful rigid-flex design, the design team must also select the materials that balance, as always, cost versus performance. Most conventional PCB boards start with a rigid fiberglass/epoxy substrate. Although termed "rigid," fiberglass/epoxy substrates exhibit some flexibility, but not enough for more complex applications that involve movement.

For 3D rigid-flex designs, dimensionally stable, flexible and heat-resistant polyimide (PI) film is the most common choice. It remains reasonably stable due to low thermal expansion and contraction (relative to PET) while also tolerating multiple reflow cycles. Polyester (PET), also commonly used, but does not tolerate high temperatures well and is less dimensionally stable than PI. As well, thin fiberglass/epoxy cores also find application in rigid-flex circuits. Besides substrates, the design will require additional films (usually PI or PET, but sometimes flexible solder mask ink) for coverlay. The coverlay protects the outer surface components and conductors from damage and corrosion and insulates the conductors as well.

By definition, rigid-flex circuits impose additional requirements when selecting conductor materials. Electrodeposited (ED) copper foils used in traditional PCB designs fall short of the necessary flexibility and toughness properties needed in a rigid-flex design. Rigid-flex designs utilize a variety of higher-performance conductor materials and methods. However, the two most common are medium-priced high-ductility electrodeposited (HD-ED) and higher-cost rolled-annealed (RA) copper foils.

In the early stages of the process, the rigid-flex design team members face a balancing act. They must define the mechanical challenges of the projected use cases balanced against the electrical performance requirements. These two considerations often butt heads, requiring the designer to balance and resolve the two. As a first step to arriving at the optimal design, the design team can gain considerable insight by producing a physical "paper-doll" mock-up of the circuit. The mockup pinpoints potential form and fit problems early in the design process. As modern CAD tools progress, they include 3D modeling of rigid-flex designs. The most up-to-date add animation. However, developing a 3D computer model involves considerable design steps, so an initial paper mock-up still proves to be informative.

Rigid-Flex Design Best Practices

The term "rigid-flex" points to one of the most significant design details. Rigid-flex circuit designs involve multiple elements that, when combined, result in a high level of complexity. For designers who develop rigid-flex designs, the biggest challenge remains: "How do I define all of the areas, layers, and stacks?" The answer: Use a table to define the stack layer design. As a general characteristic, most rigid-flex designs exhibit different layer stacks in different areas of the design.

One simple way: Copy the design outline on a mechanical layer. Then create a fill-pattern that to identify the rigid and flexible portions of the design that contain a different layer stack as shown in Figure 2.

The simplified design in Figure 2 uses the matching graphic fill patterns (the two columns on the right of the table) to identify the flexible and rigid areas of the board, respectively. For example, the layer named "Dielectric 1" is an FR-4 core. With the different layer stacks defined, any rigid-flex design team now confronts

Layer	Name	Material	Thickness	Constant	Flexible	Rigid
1	Top Paste					
2	Top Overlay					
3	Top Solder	Coverlay (PI)	0.50mil	4		
4	Top Layer	Copper	1.40mil			
5	PIBase	Polyimide	1.40mil	4.8		
6	Dielectric 1	FR-4	12.00mil	4.2		
7	Bottom Layer	Copper	1.40mil			
8	Bottom Solder	Coverlay (PI)	0.50mil	4		
9	Bottom Overlay					
10	Bottom Paste					

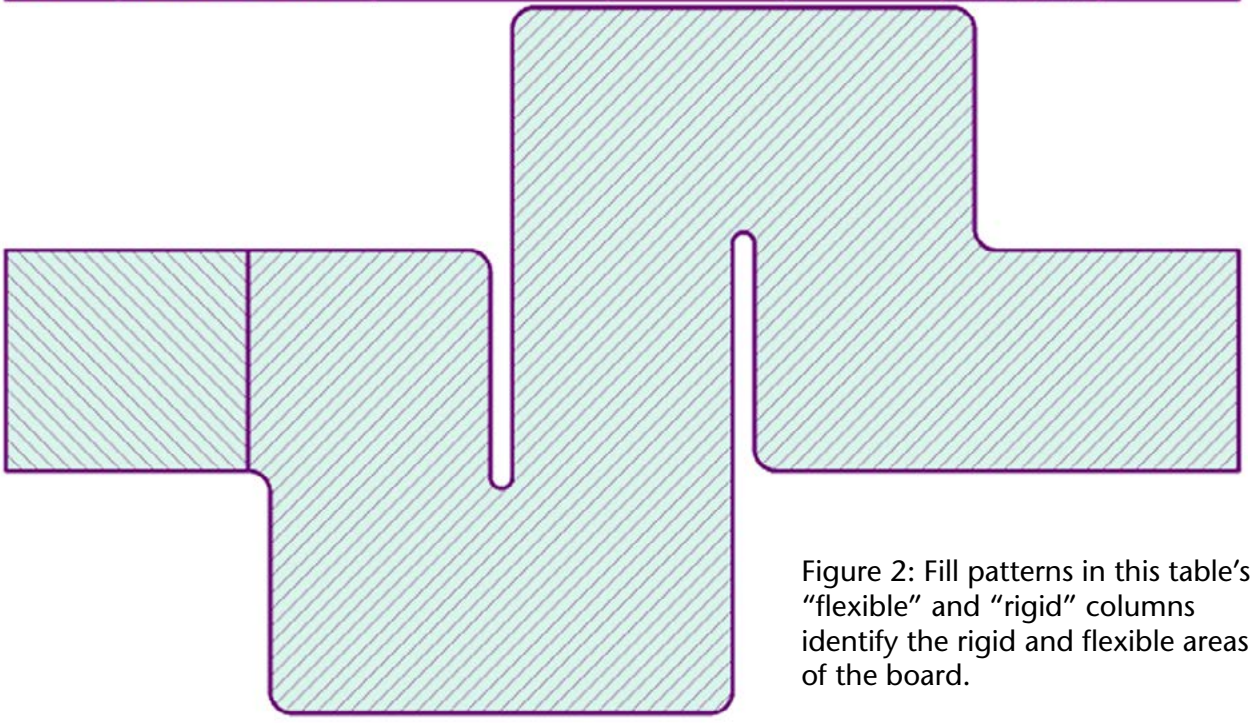

Figure 2: Fill patterns in this table's "flexible" and "rigid" columns identify the rigid and flexible areas of the board.

specifying bends and folds in 2-D space. This means that every rigid-flex designer must document where critical design elements cross the boundaries between rigid and flexible sections.

Keeping the Flex in Rigid-Flex: Staggered Length Circuits

This design practice, also called bookbinder construction, adds a small amount of length layer by layer, moving outward from the bend radius. This method allows the circuit to bend in only one direction. A common rule of thumb is to add additional length to a subsequent layer, roughly 1.5 times the thickness of the individual layer. But that value varies depending on the tightness of the bend and the number of layers. This is another instance where a paper-doll mockup can provide an informative quick check. Bookbinder construction relieves tension produced during bending and also prevents buckling of the inner layers near the bend radius.

More Golden Rules

- **Avoid bending at the corners.** Copper traces perform best when placed at right angles to the flexible circuit bend. In cases where bending is unavoidable, one alternative is to use conical radius bends.
- **Use curved traces.** Avoid hard right angle traces and even 45° hard corners because they increase stresses on copper traces during bending.

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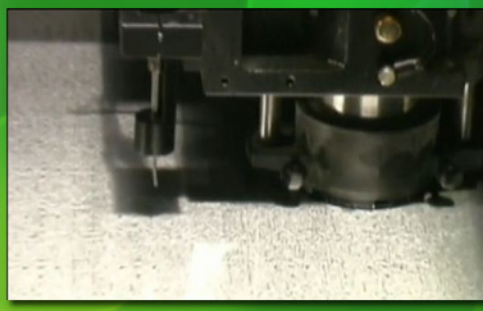

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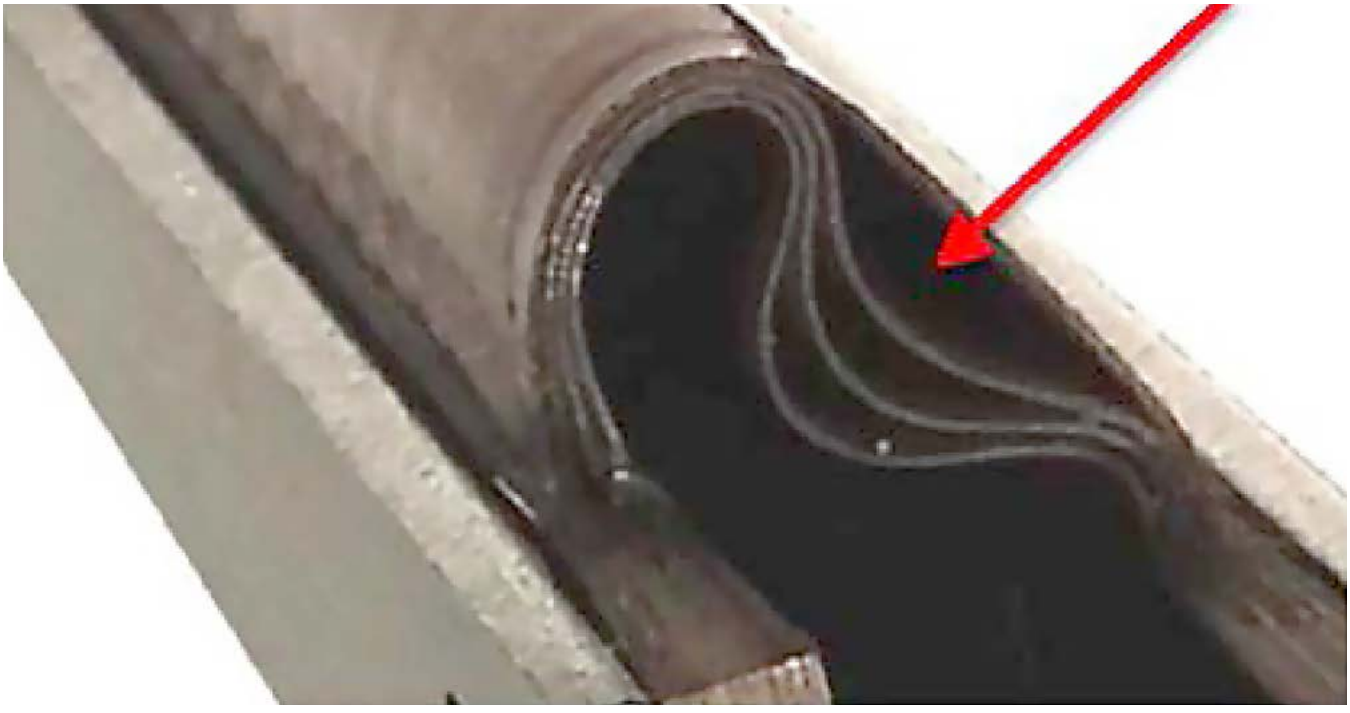

Figure 3: In this commercially produced design, the designers obviously did not apply bookbinder construction, resulting in additional stress on the separated layers (red arrow).

• **Do not abruptly change trace widths.** When traces enter a pad, often in alignment, an abrupt change in trace width creates a weak spot. As a good design practice, use a teardrop pattern to gradually change the width of traces connecting to pads and vias in the flex circuits.

• **Use hatched polygons.** A normal rectangular pour still retains heavily biased stresses in 0°, 45°, and 90° directions. A hexagon, by comparison, statistically provides a more optimal hatch pattern.

• **Add pad support.** Compared to FR-4, copper on a flexible PI substrate is more likely to detach due to repeated stresses involved in bending plus lower adhesion. Consider surface mount pads and non-plated through-holes to be unsupported. Many fabricators recommend additional through-hole plating and recommend additional SMT pad support such as anchoring stubs and reduced coverlay openings.

• **Stagger double-sided flex traces.** Running traces over each other in the same direction distributes tensions between the copper layers unevenly. Staggering the traces reduces or eliminates the problem.

In harmony with the clear trend of increasing rigid-flex PCB manufacturing, updated PCB CAD tools now include the necessary features needed to design rigid-flex circuits. These include multiple layer stack management, components mounted on "inner" flex-circuit layers, and 3D visualization and simulation of the flex circuit portions. Figure 4 demonstrates these capabilities.

In addition to the layer stack management and 3D visualization, clearance checking of the components on the flex substrate is also possible. The design rule check engine provides early warning for rigid-flex designs whenever the final bend radii results in mechanical interferences. See Figure 5.

Electronic design is becoming a 3D world. And as more rigid PCB designers face technological pressure, many are turning to rigid-flex circuits to help them meet these requirements. Fortunately, EDA companies are incorporating

Figure 4: An example rigid-flex PCB design in Altium Designer's 3D mode, showing intended bends in the flex circuit areas.

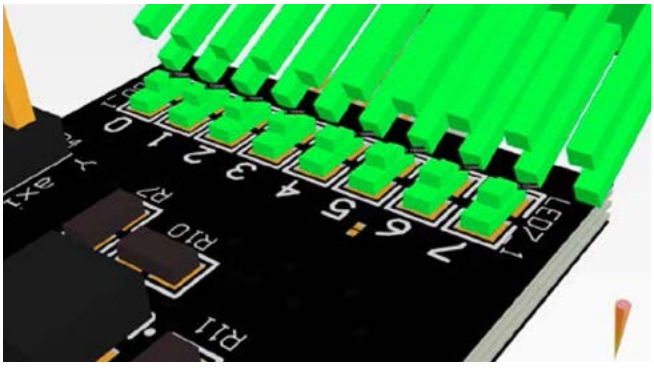

Figure 5: Simulated bending of a flex circuit reveals a clearance violation between a flex-mounted pin-header and SMDs on the main rigid board. The violating components are highlighted green.

improved rigid-flex design capabilities into existing PCB design tools. **PCBDESIGN**

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Ben Jordan has more than 20 years of electronics experience, including PCB design and embedded computing and FPGA hardware and software, and has research interests in signal processing, audio electronics, and PCB design. Ben Jordan has worked as an account engineer, field account engineer, and in marketing and management roles at Altium since 2004.

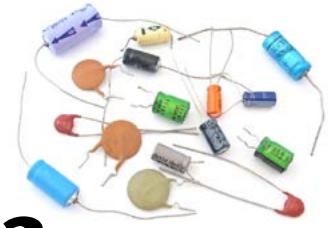
Group Hopes to Produce Electricity On the Moon at Night

Researchers from the Polytechnic University of Catalonia and U.S. collaborators have studied two options for storing energy on the moon during the day for use at night.

"The first system consists of modifying fragments of regolith or lunar soil, incorporating elements such as aluminium, for example, such that it becomes a thermal mass," says study co-author Ricard Gonzalez-Cinca.

The second system incorporates a more sophisticated series of mirrors and a heat engine. The mirrors are Fresnel reflectors, which concentrate solar rays upon a fluid-filled tube.

This heat converts the liquid into a gas, which heats the thermal mass. At night, heat is transferred to a Stirling engine to produce electricity.



PDN Planning and Capacitor Selection, Part 2

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD | AUSTRALIA

In last month's column, PDN Planning and Capacitor Selection Part 1, we looked closely at how to choose the right capacitor to lower the AC impedance of the power distribution network (PDN) at a particular frequency. We also examined capacitor properties and types of capacitors that are readily available and touched on the target frequency approach for analyzing a PDN. This month we will continue on from there looking at the one-capacitor-value-per-decade and optimized value approaches.

Figure 4 shows the effect of using the one-value-per-decade approach where capacitors from each decade are added in parallel. Now to be fair, I have added three of each value from 100uF to 1pF to total 27 capacitors as the target frequency approach, in Figure 2, had a total of 29 capacitors. In this case, the impedance is below the target impedance from 10KHz to 110MHz.

Notice how the combination of capacitors causes anti-resonant (parallel resonant) peaks where the higher frequency capacitor goes capacitive while the lower frequency capacitor is inductive. This occurs as the LC network produced by the combination is effectively a tank circuit that has parallel resonance at the crossing frequency. This happens each time a different value of capacitor is added. These peaks exceed

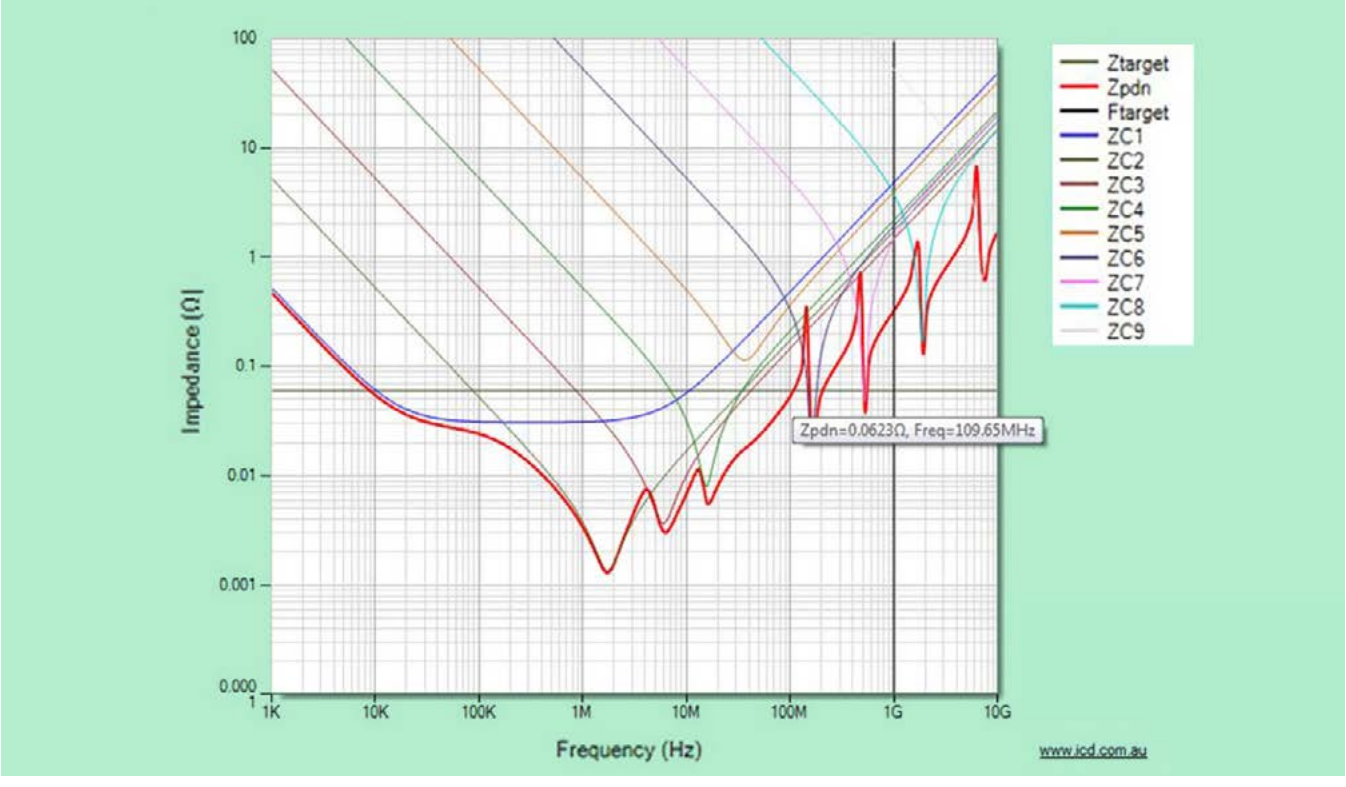


Figure 4: One value capacitor per decade approach.

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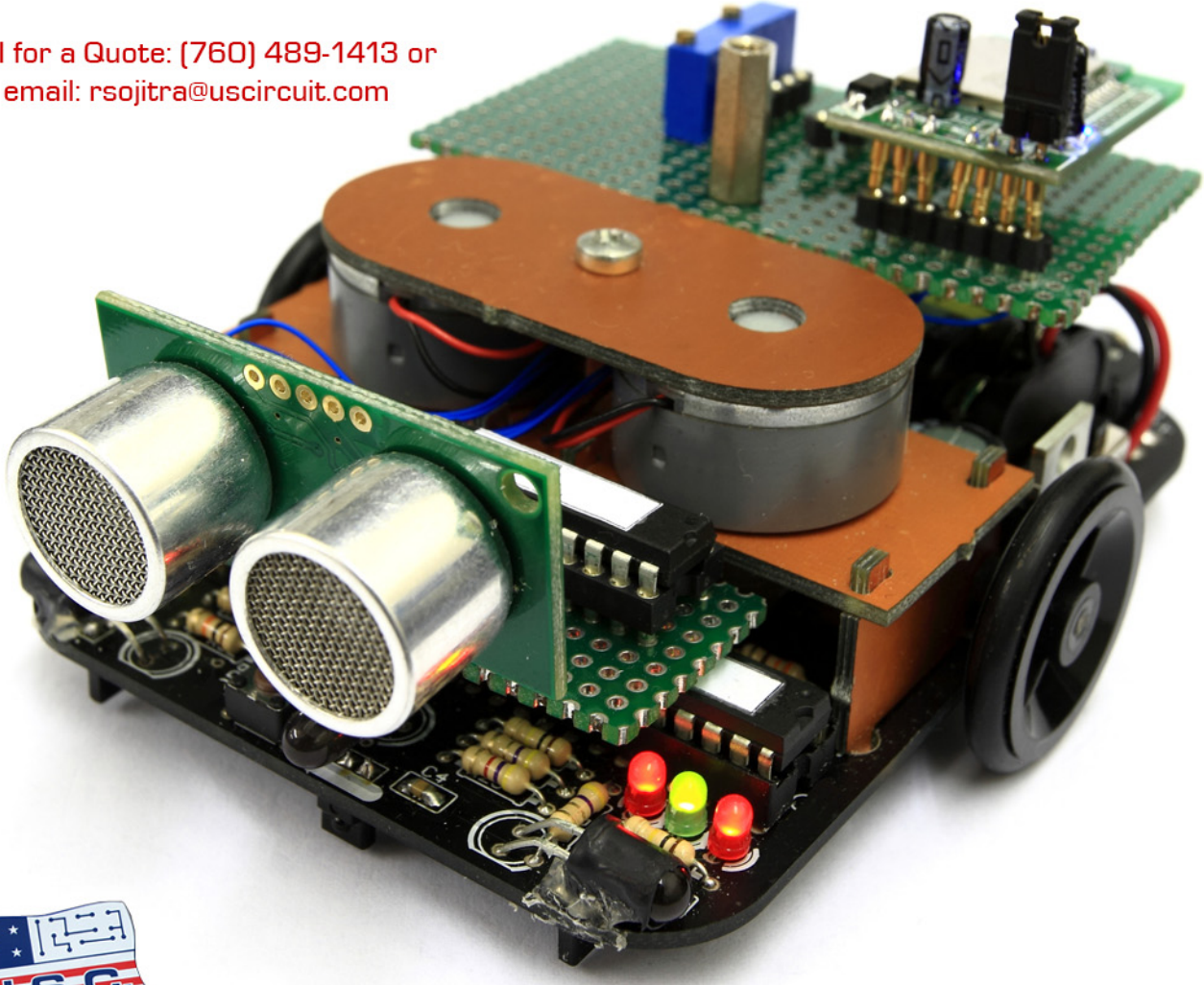

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PDN PLANNING AND CAPACITOR SELECTION, PART 2 *continues*

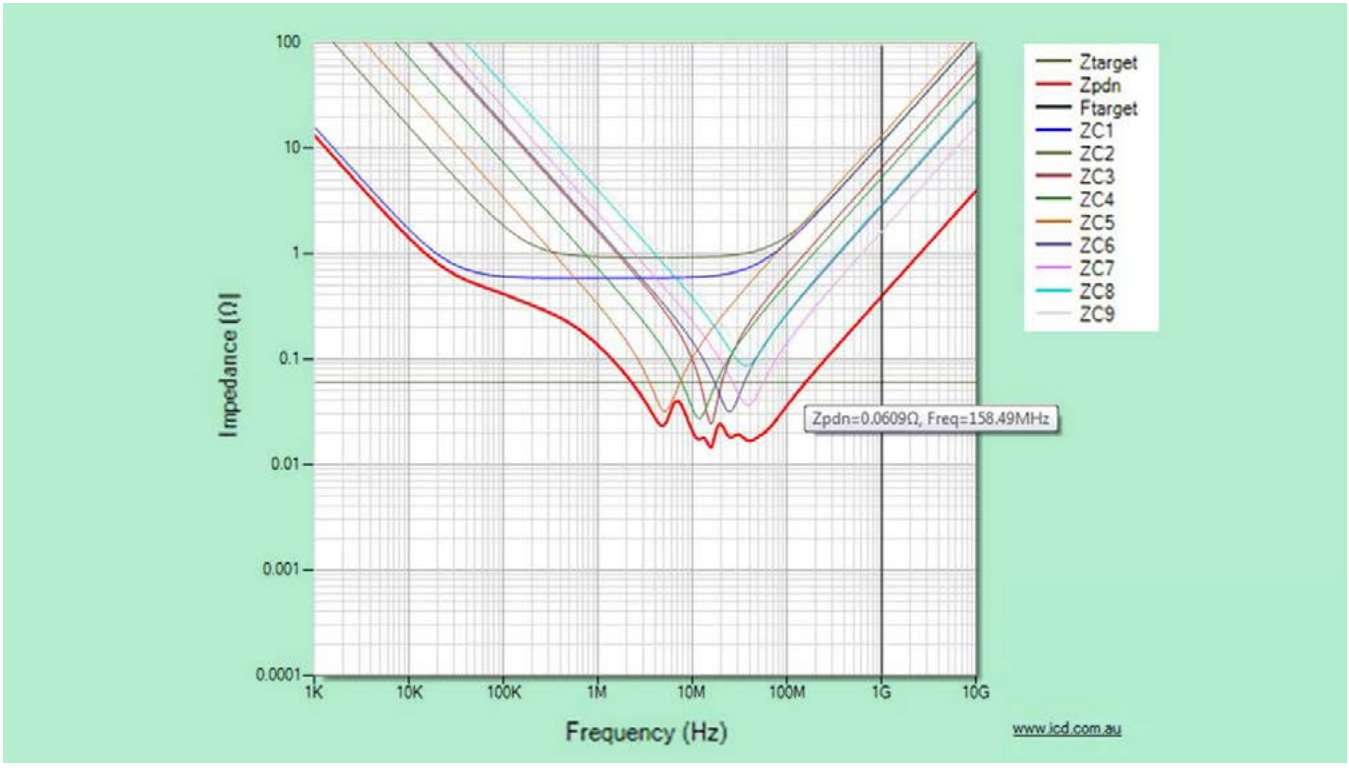


Figure 5: The optimized value approach with 21 capacitors.

the 60mΩ impedance of the V shape of the target frequency approach—some as high as 800mΩ below 1GHz which is 13 times higher than the target impedance. If an odd harmonic was to fall on that particular frequency, then emissions would also be very high at that frequency. From extensive simulations, I have noticed that there is a direct correlation between AC impedance peaks and electromagnetic radiation. In fact, if a board fails electromagnetic compliancy, emissions can be dampened by changing the capacitors to ones that have a self-resonant frequency (SRF) close to the radiating frequency.

The optimized value approach, illustrated in Figure 5, has 21 capacitors of different values and numbers to optimize the overall AC impedance. In this case, 21 capacitors from 10uF to 4.7nF are used. This approach gives a response below the target impedance from 2MHz to 158MHz. The low end is of little consequence, as the operating frequency of concern is much higher. And you will also note that there are no anti-resonant peaks, in this case, because the values are so close together the overlaps dampen the peaks. When the SRFs are spread, the parallel resonant impedance sets the limits to the PDN performance. There are a few ways to reduce the anti-resonant peaks:

1. Adjust the capacitor values so that the SRFs are closer to the anti-resonate peaks.
2. Add a capacitor with a SRF at the anti-resonant peak.
3. Add more ESR by increasing the number of capacitors.
4. Increase the capacitance of the planes by using thinner plane to plane dielectrics.

The resonant and anti-resonant peaks of the bypass and decoupling capacitors have now been taken into account but we also need to deal with the plane resonance. Ideally the planes, a perfect lumped element capacitor of this size, should provide a very low impedance between power and ground at very high frequencies (several hundred MHz and higher). But planes, left open at the edges, behave like wide un-terminated traces, from a signal integrity point of view,

reflecting at the ends creating resonances in the transmission line. As the frequency increases to half wavelength, the series resonance builds up a standing wave pattern reflecting from the open edges of the plane. Fortunately, this happens above 1GHz.

Also, the mounting inductance of each capacitor needs to be taken into account. The mounting inductance is comprised of three components: Capacitor footprint and fanout, capacitor height above or below the plane and power plane spreading inductance. These three elements describe the loop in which current must flow—the bigger the loop, the more the inductance. The footprint (land pattern) for a capacitor dominates the total ESL. It consists of via placement with respect to the pad, the length and width of traces connected to the pad, and the way the vias are connected to the power and ground planes. The location of the power/ground planes in the PCB stackup controls the height of the via. Inductance directly depends on the magnetic field, so reducing the energy associated with the loop area reduces overall inductance.

The inductance associated with current spreading, into the power/ground planes, also contributes to the total mounted inductance. Current in the planes becomes concentrated in the vicinity of the vias. This current creates a high magnetic field and therefore contributes to inductance.

With the continuous trend to smaller feature sizes and faster signal rise times, planar capacitor laminate or embedded capacitor materials (ECM) is becoming a cost-effective solution for improved power integrity. This technology provides an effective approach for decoupling high-performance ICs whilst also reducing electromagnetic interference.

Planar capacitor technology allows for a very thin dielectric layer (0.24 – 2.0mil) that provides distributive decoupling capacitance, of 20nF/in^2 in this case. This also increases real estate (space), reduces the number of vias and opens up routing channels. Unfortunately, standard decoupling capacitors have little effect over 1GHz and the only way to reduce the AC impedance of the PDN above this frequency is to use ECM or alternatively on-die capacitance. These ultra-thin laminates replace the conventional power and ground planes and have excellent stability of dielectric constant and loss up to 15GHz.

In Figure 6, the ICD PDN Planner shows the one value per decade approach including the voltage regulator module (VRM) which is mainly inductive, the total loop inductance of each capacitor, via spreading inductance and the plane capacitance. The plane resonance can be seen on the right. In each case, a 0.24mil, 3M ECM, that provides 20nF/in^2, was used to drop the PDN to below the simulated target impedance up to 1.3GHz. By comparison, the target frequency and the optimized value approached in Figure 7, also have the VRM, loop inductance and plane capacitance of 3M ECM included.

> ***This technology provides an effective approach for decoupling high-performance ICs whilst also reducing electromagnetic interference.***

So which approach is best?

1. The target frequency approach gives a clean "V" shape with just one small anti-resonant peak at 40MHz and is below the target impedance up to 1.3GHz;
2. The one value capacitor per decade approach has one peak at 23MHz and is also below the target impedance up to 1.3GHz; and
3. The optimized value approach is also good from 2.3MHz to 1.3GHz with a peak at 1MHz.

But, in reality, only plane capacitance, on-die capacitance or changing the plane size (area) can reduce the impedance beyond several 100MHz.

So, it is really six of one and half a dozen of the other! Personally, I prefer the target frequency approach, as it is less time-consuming to analyze and requires fewer parts; this means that the BOM count is reduced, holding stock is reduced and assembly equipment setup and placement times are greatly reduced. This all leads to reduction in cost and time to market and of course a more reliable end product. Also,

PDN PLANNING AND CAPACITOR SELECTION, PART 2 *continues*

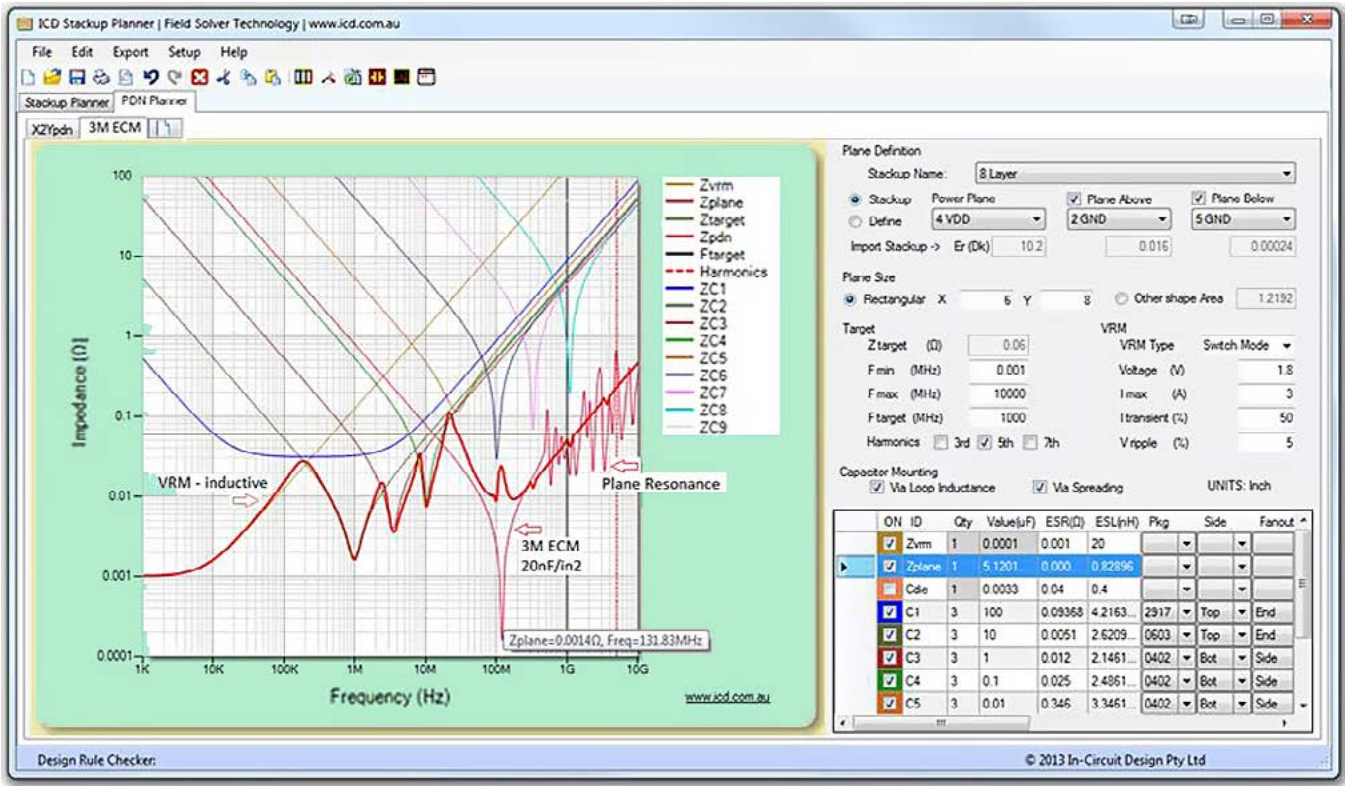
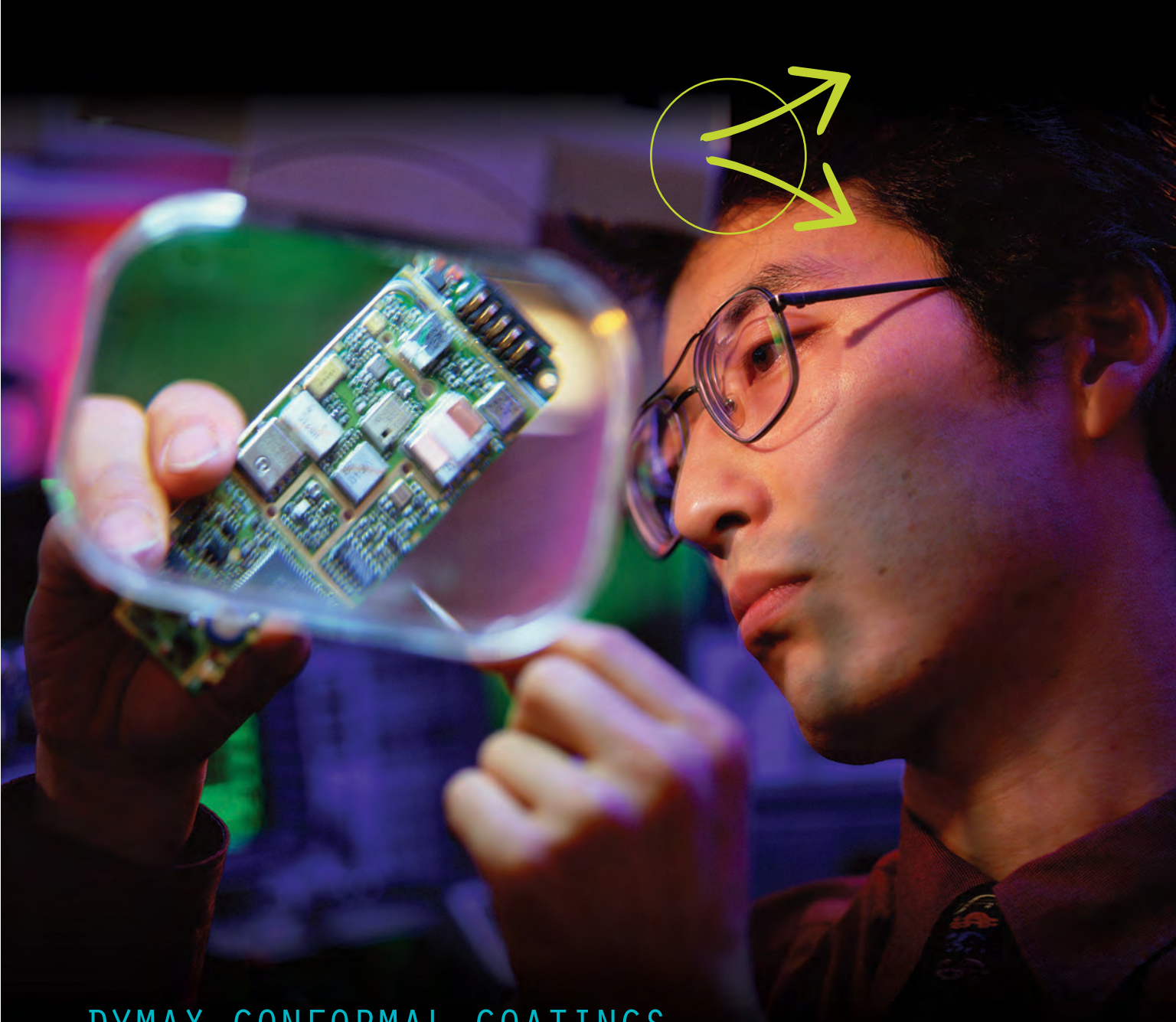


Figure 6: One value capacitor per decade approach including VRM, loop inductance and plane capacitance of 3M ECM.

this method can be used to dampen electromagnetic emissions at a particular frequency. Either way, each PDN on the board should be analyzed to give confidence in the final product.

Points to Remember

- There are three approaches to analyzing the PDN: target frequency, one value capacitor per decade or optimized value.
- Poor PDN design can result in unusual, intermittent signal integrity issues including high crosstalk and excessive emission of radiation.
- The integrity of the PCB stackup and the PDN are the basis for a stable product.
- Decoupling is not the process of placing a capacitor adjacent to the IC, but rather it is the process of placing an L-C network adjacent to the IC to supply the high transient switching current.
- Decoupling capacitors supply instantaneous current—at different frequencies—to the drivers until the power supply can respond.
- For bulk decoupling at the supply level, tantalum is usually preferred, due to the availability of high capacitance ratings.
- Large capacitance value ceramics provide effective decoupling at about 25% of the nominal capacitance value compared to standard tantalums.
- The capacitance of a capacitor is determined by three factors. The number of layers in the part, the dielectric constant and the active area.
- The dielectric thickness is inversely related to the capacitance—so the thicker the dielectric, the lower the capacitance value.
- The rating compared to working voltage for multilayer ceramic capacitors is 2:1.
- The dielectric constant depends on the ceramic material used. NP0 has the lowest dielectric constant, followed by X7R and Y5V.
- Dissipation Factor (Df) is the percentage of energy wasted as heat in the capacitor.
- While X2Y MLCCs offer superior performance and space wise, they are about five times the price of standard 0402.



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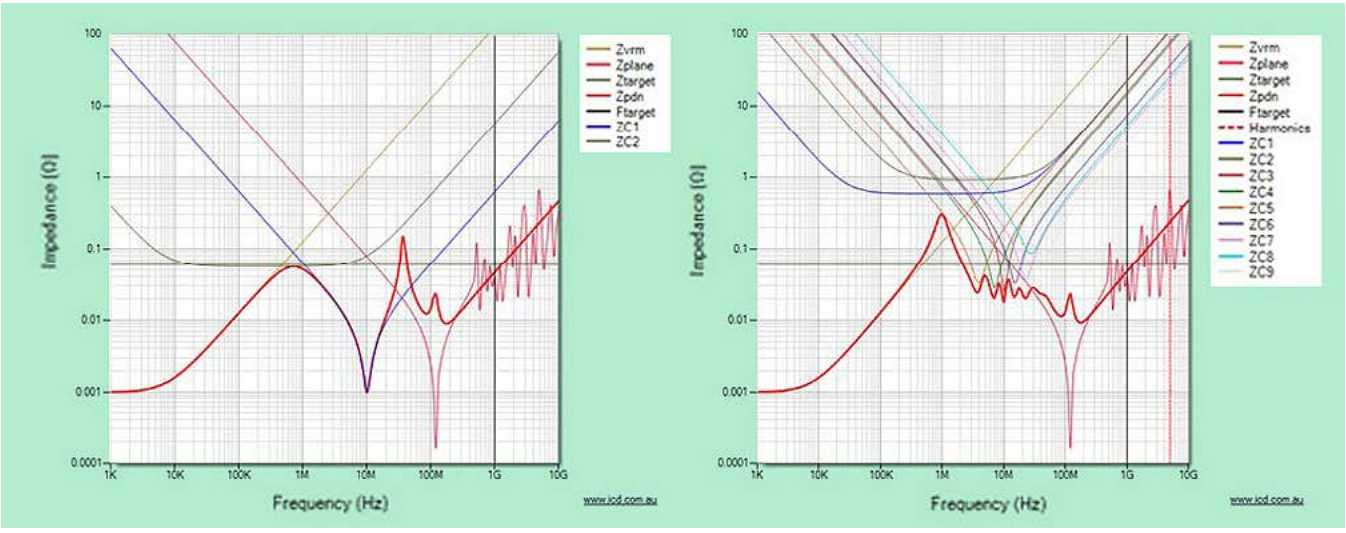

Figure 7: Target frequency and optimized value approaches including VRM, loop inductance and plane capacitance of 3M ECM.

• A capacitor's equivalent circuit is basically a series capacitor, resistor and inductor. These are referred to as the capacitance value, ESR and ESL respectively.

• The downward slope of the capacitor is capacitive, then as the capacitor approaches its SRF it becomes resistive, then as the frequency increases the inductance takes over raising the impedance again.

• To meet the target (low) impedance at a particular frequency, a capacitance value is chosen so that when mounted on the PCB, it will resonate at the desired frequency, and have an impedance that is equal to its ESR.

• The combination of capacitors causes anti-resonant peaks, where one goes capacitive while the other is inductive.

• When the SRFs are spread, the parallel resonant impedance sets the limits to the PDN performance.

• The mounting inductance is comprised of three components: Capacitor footprint and fanout, capacitor height above or below the plane and power plane spreading inductance.

• Embedded Capacitance technology allows for a very thin dielectric layer (0.24 – 2.0mil) that provides distributive decoupling capacitance and takes the place of conventional discrete decoupling capacitors over 1GHz. **PCBDESIGN**

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4. Eric Bogatin, Signal and Power Integrity Simplified

5. Johanson Dielectrics, Basics of Ceramic Chip Capacitors

6. Kemet, SMT Capacitor Comparison

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8. The ICD PDN Planner is available at www.icd.com.au

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. ICD is a PCB design service bureau that specializing in board-level simulation. The company developed the ICD Stackup Planner and the ICD PDN Planner software. To read past columns or contact Olney, click here.

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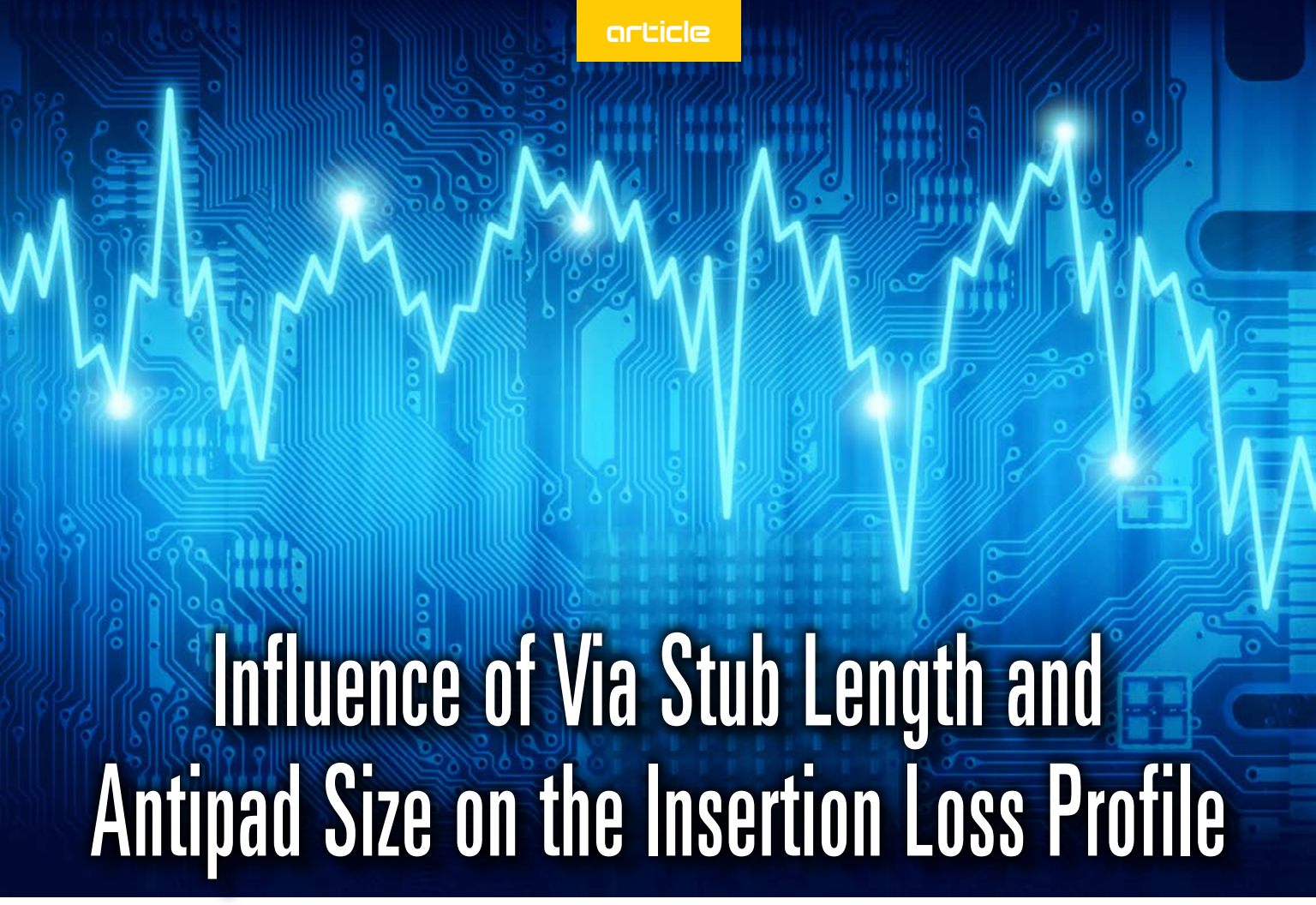

Influence of Via Stub Length and Antipad Size on the Insertion Loss Profile

by Alexander Ippich
MULTEK INC.

SUMMARY: What effect do via stub length and antipad size have on resonant frequency and insertion loss profile? This article focuses on an investigation into these issues and offers recommendations for optimum via stub length.

Abstract

The growing transmission speed and volume of digital content increases the pressure on reduction of overall insertion loss of printed circuit boards permanently.

In today's circuit boards, it is not only the transmission line itself, but also the via structure that impacts the insertion loss profile. To optimize the via, the stub length needs to be reduced by methods like backdrilling the copper out of the unused portion of the PTH.

In this article, the influence of remaining stub lengths, varying between a couple of mils and 100 mils, on the insertion loss profile is evaluated. As a second variable, the size of the antipad is chosen and a two-factor, multiple level DOE is performed.

Both, single-ended and differential insertion loss is investigated and an "analysis of variance" approach is used to determine the level of influence of the variables stub length and antipad size at various frequencies up to 40 GHz.

The frequency of the quarter-wave-length-resonance is correlated to the stub length, and the increase of the insertion loss well below the resonance point is discussed.

The test vehicle and the performed measurements are detailed, and the article discusses the electrical performance characteristics of the various test cells. Later, a recommendation for an acceptable stub length is given.

Introduction

Driven by steadily increasing bandwidth demand for networking infrastructure and the amount of data handled in ever-enlarging server installations, the transmission characteristics of the transmitting channel must be optimized.

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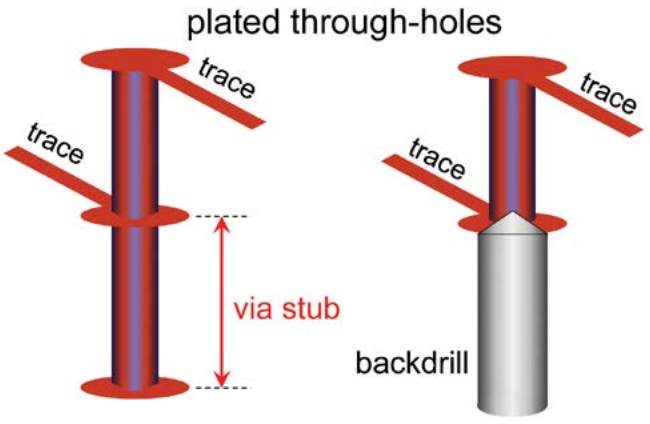


Figure 1: Backdrill principle.

Best performance would be reached with a signal path without distortion and zero attenuation. In the imperfect reality, the insertion loss of the transmitting structures needs to be as small as possible and should not show large non-linearities.

For insertion loss reduction, the dielectric loss needs to be minimized by using low-Df materials. The second important parameter is the copper loss, which is influenced significantly by the roughness of the signal trace. The application of both adequate oxide replacement and copper foil quality is key[1, 2].

However, there is another element in the transmission channel that needs to be evaluated. The via structure connecting the integrated circuit or connectors to the traces on the inner-layers of the printed circuit board has a huge negative impact on the insertion loss profile, especially if the via extends significantly beyond the layer that needs to be electrically connected.

As discussed in Eric Bogatin's Practical Analysis of Backplane Vias[3], the via stub creates a large notch in the insertion loss profile at the "quarter-wave frequency." A commonly used method to reduce the via stub is to backdrill: A second drilling step after electroplating of the through-holes removes the copper in the unused portion of the via (Figure 1).

Since this is a mechanical operation, improving the depth accuracy is not simple and very often complicates the process significantly, which in turn increases cost. It is important to understand how much stub is still acceptable in a given application to avoid excessive strengthening of the via stub specification.

To get real data on the effect of the via stubs, single ended and differential channels were created with stub lengths varying from practically zero to close to 100 mils. As a second parameter, the sizes of the antipads on the reference layers have been modified. Two-port and 4-port S-parameters were collected on these test structures and an "analysis-of-variance" (ANOVA)[4, 5] approach was used to evaluate the effect of these parameters on the magnitude of the insertion loss as well as on the quarter-wave resonance frequency.

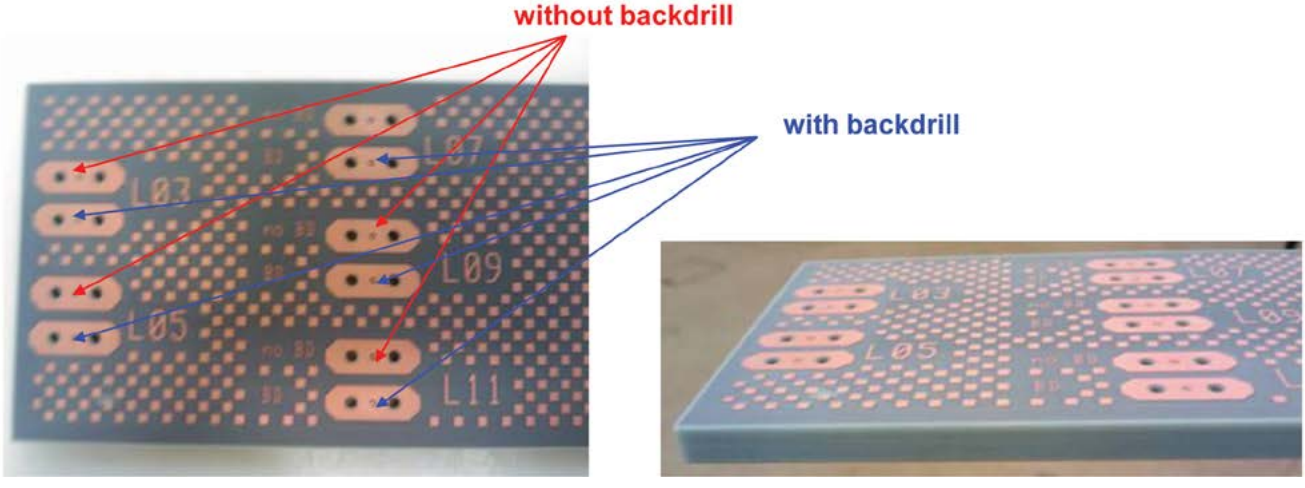


Figure 2: A board 0.220" in thickness.

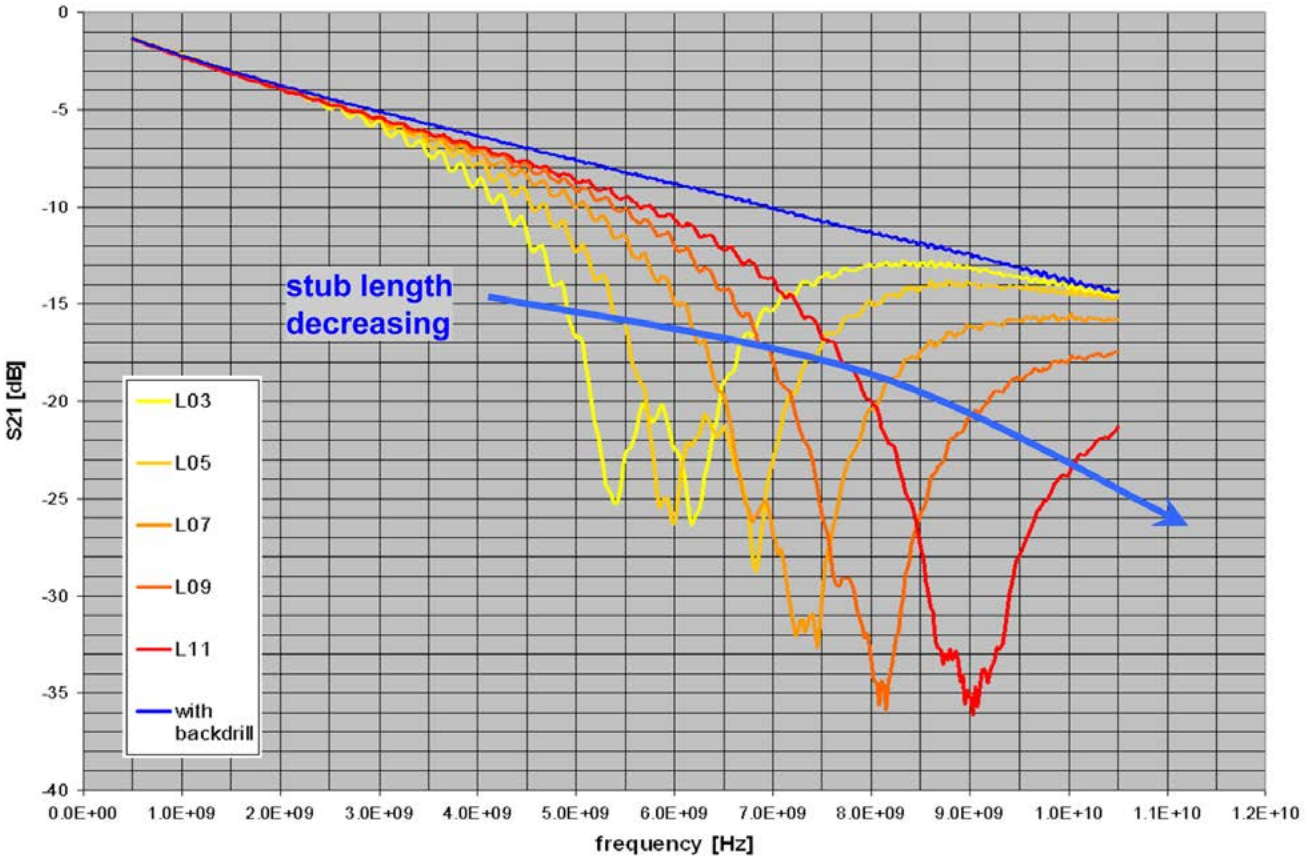


Figure 3: Influence of stub length on insertion loss profile.

Measurement Results that Prompted the Investigation

During a routine measurement of insertion loss over frequency on a 0.220" board (Figure 2), significant differences were found, depending on the measured layer. Testing the same layers with backdrilled vias eliminated the differences and resulted in a straight insertion loss curve without the deep resonances (Figure 3). This finding initiated a thoroughly investigation into the influence of via stubs on electrical performance.

The Test Vehicle

An 8-layer stackup was used for the test vehicle, with one offset stripline on layer 3 (referencing to ground layers 2 and 4). Layer 6 was an unused layer and layers 5 and 7 were also ground layers. The outer layers provided the landing patterns for probing. The probing was performed from the top side, which in turn generated maximum via stubs for the layer 3 features.

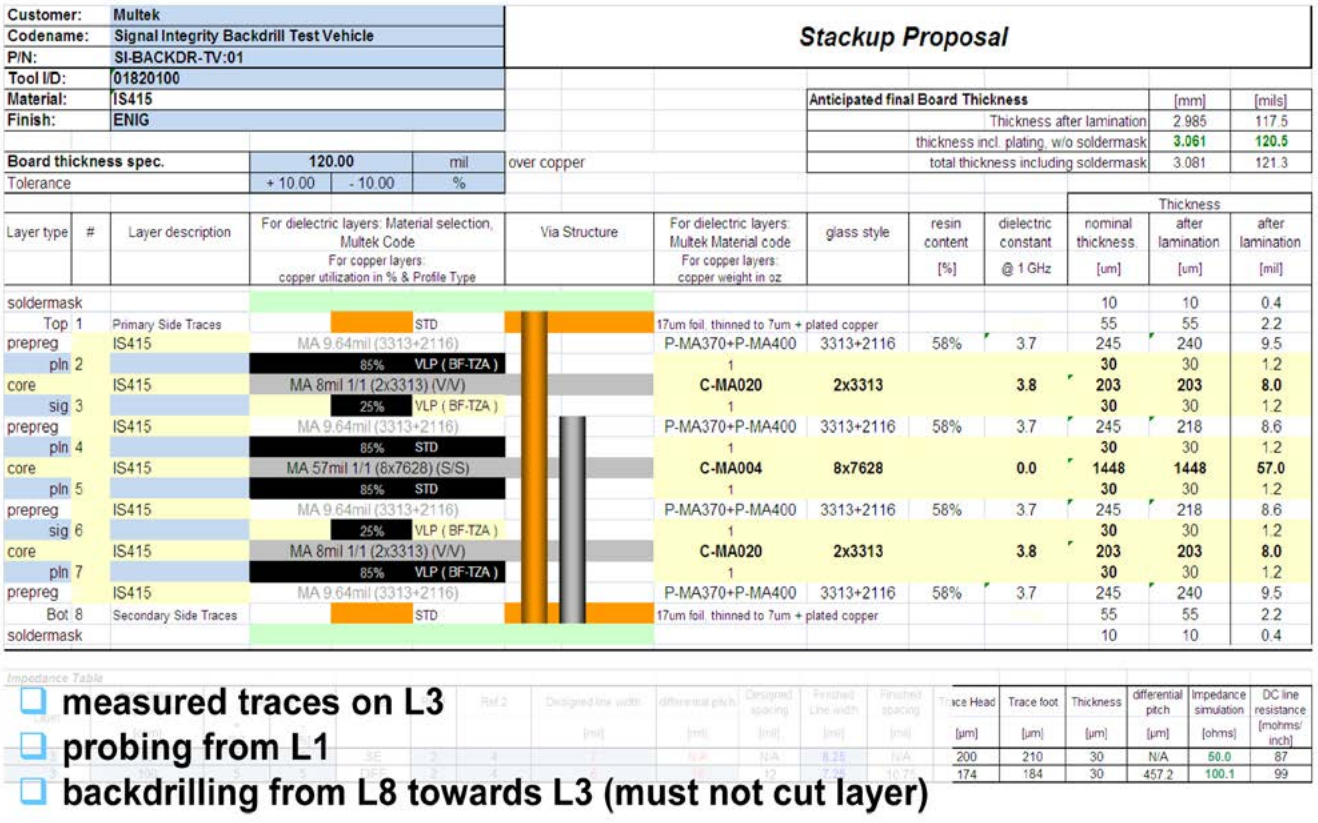
A mid-loss material has been applied for the DOE, as many designs in the range of 3.125 – 10Gbs+ are using them. Similar glass styles and thicknesses were used for the cores and prepregs to get a relatively balanced stripline design. A rather wide line width in combination with 1 oz. copper delivered minimum DC resistance.

Together with a smooth copper foil, these design attributes were resulting in a relatively small insertion loss. The complete stackup details can be found in Figure 4.

The design consisted of single-ended and differential transmission lines on layer 3, with a via connecting the lines to the outside at each end of the traces. In addition, single-ended and differential impedance test coupons were placed on the panel.

The size of the antipads on the plane lay-

INFLUENCE OF VIA STUB LENGTH AND ANTIPAD SIZE ON THE INSERTION LOSS PROFILE *continues*



Customer:	Multek
Codename:	Signal Integrity Backdrill Test Vehicle
P/N:	SI-BACKDR-TV:01
Tool I/D:	01820100
Material:	IS415
Finish:	ENIG

Stackup Proposal

Anticipated final Board Thickness	[mm]	[mils]
Thickness after lamination	2.985	117.5
thickness incl. plating, w/o soldermask	3.061	120.5
total thickness including soldermask	3.081	121.3

Board thickness spec.	120.00		mil
Tolerance	+ 10.00	- 10.00	%

over copper

Layer type	#	Layer description	For dielectric layers: Material selection, Multek Code / For copper layers: copper utilization in % & Profile Type	Via Structure	For dielectric layers: Multek Material code / For copper layers: copper weight in oz	glass style	resin content [%]	dielectric constant @ 1 GHz	Thickness: nominal thickness [um]	Thickness: after lamination [um]	Thickness: after lamination [mil]
soldermask									10	10	0.4
Top	1	Primary Side Traces	STD		17um foil, thinned to 7um + plated copper				55	55	2.2
prepreg		IS415	MA 9.64mil (3313+2116)		P-MA370+P-MA400	3313+2116	58%	3.7	245	240	9.5
pln	2		85% VLP (BF-TZA)		1				30	30	1.2
core		IS415	MA 8mil 1/1 (2x3313) (V/V)		C-MA020	2x3313		3.8	203	203	8.0
sig	3		25% VLP (BF-TZA)		1				30	30	1.2
prepreg		IS415	MA 9.64mil (3313+2116)		P-MA370+P-MA400	3313+2116	58%	3.7	245	218	8.6
pln	4		85% STD		1				30	30	1.2
core		IS415	MA 57mil 1/1 (6x7628) (S/S)		C-MA004	8x7628		0.0	1448	1448	57.0
pln	5		85% STD		1				30	30	1.2
prepreg		IS415	MA 9.64mil (3313+2116)		P-MA370+P-MA400	3313+2116	58%	3.7	245	218	8.6
sig	6		25% VLP (BF-TZA)		1				30	30	1.2
core		IS415	MA 8mil 1/1 (2x3313) (V/V)		C-MA020	2x3313		3.8	203	203	8.0
pln	7		85% VLP (BF-TZA)		1				30	30	1.2
prepreg		IS415	MA 9.64mil (3313+2116)		P-MA370+P-MA400	3313+2116	58%	3.7	245	240	9.5
Bot	8	Secondary Side Traces	STD		17um foil, thinned to 7um + plated copper				55	55	2.2
soldermask									10	10	0.4

Impedance Table

Trace Head [µm]	Trace foot [µm]	Thickness [µm]	differential pitch [µm]	Impedance simulation [ohms]	DC line resistance [mohms/inch]
200	210	30	N/A	50.0	87
174	184	30	457.2	100.1	99

- measured traces on L3
- probing from L1
- backdrilling from L8 towards L3 (must not cut layer)

Figure 4: Stackup of the test vehicle.

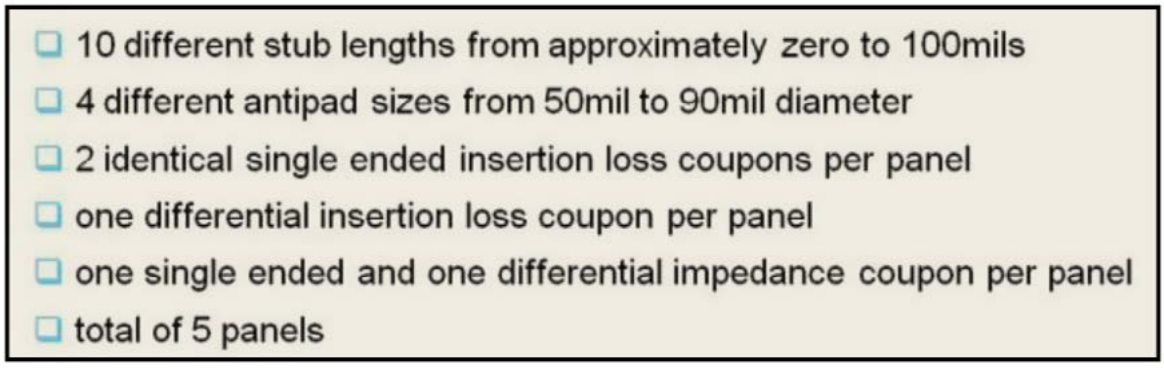


Figure 5: Design features.

ers was identical on L2, L4, L5 and L7, but they were modified between 50 mil and 90 mil in diameter for the various coupons. The primary drill (plated through-hole) was backdrilled from the bottom side of the test vehicle to different depths, resulting in nominal stub lengths between around 100 mil down to practically no stub at all (Figure 5). Some of these stub lengths can be seen in Figure 6.

An overview of the test panel with the various backdrill and insertion loss coupons is given in Figure 7 and an example of one of the coupons populated with the flange mount connectors is shown in Figure 8.

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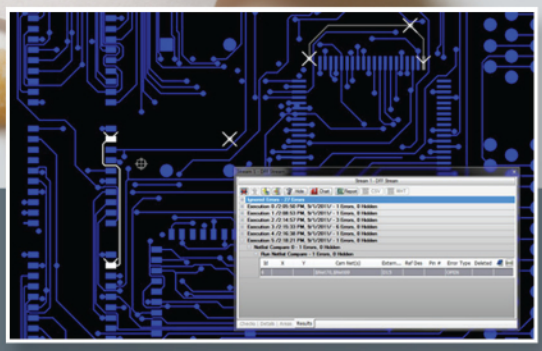
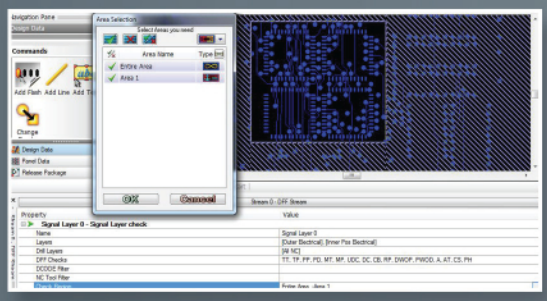


Netlist errors are quickly validated in DFMStream



Define DFM checks by area so components such as BGAs can be verified with unique rules different from rest of design

DownStream Technologies

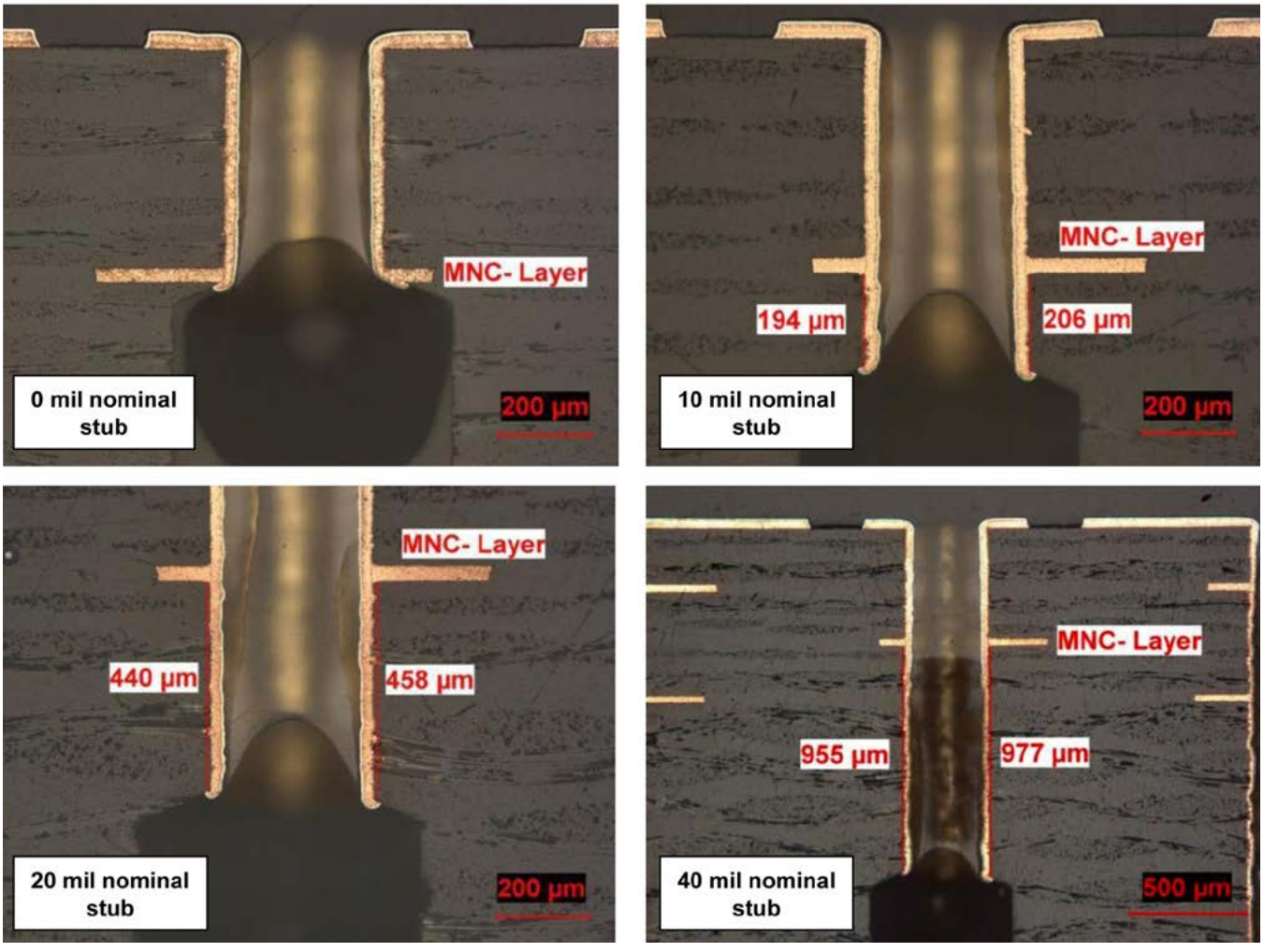


Figure 6: Different stub lengths.

Impedance Control

To assure good matching of the transmission lines to the measurement equipment, the single ended and differential impedance of the traces was measured on each test panel. For ease of testing, dedicated impedance coupons (Figure 7) were used in conjunction with handheld probing heads and a standard, volume manufacturing impedance test system.

The impedance testing confirmed that both the differences between the panels and between the two produced work orders were minimal. The absolute values were slightly below nominal, with an average single ended impedance of 47.6 ohm and an average differential impedance of 97.2 ohms on layer 3. The detailed readings can be found in table 1.

Single-Ended Insertion Loss Testing

Measurement of single ended and differential insertion loss of the transmission lines including the effect of the via stubs was performed on a 4-port vector network analyzer capable of going to 40 GHz. High-quality coaxial cables with 2.92 mm connectors with a frequency rating of 40 GHz were used.

A minimum warm-up period of two hours was ensured prior to calibration of the vector network analyzer. For this purpose an electronic calibration module, connected directly to the end of the coaxial cables was used. After completion of the calibration, the cables connected directly to the compression mount connectors on the test boards, without any additional adapters needed.

INFLUENCE OF VIA STUB LENGTH AND ANTIPAD SIZE ON THE INSERTION LOSS PROFILE *continues*

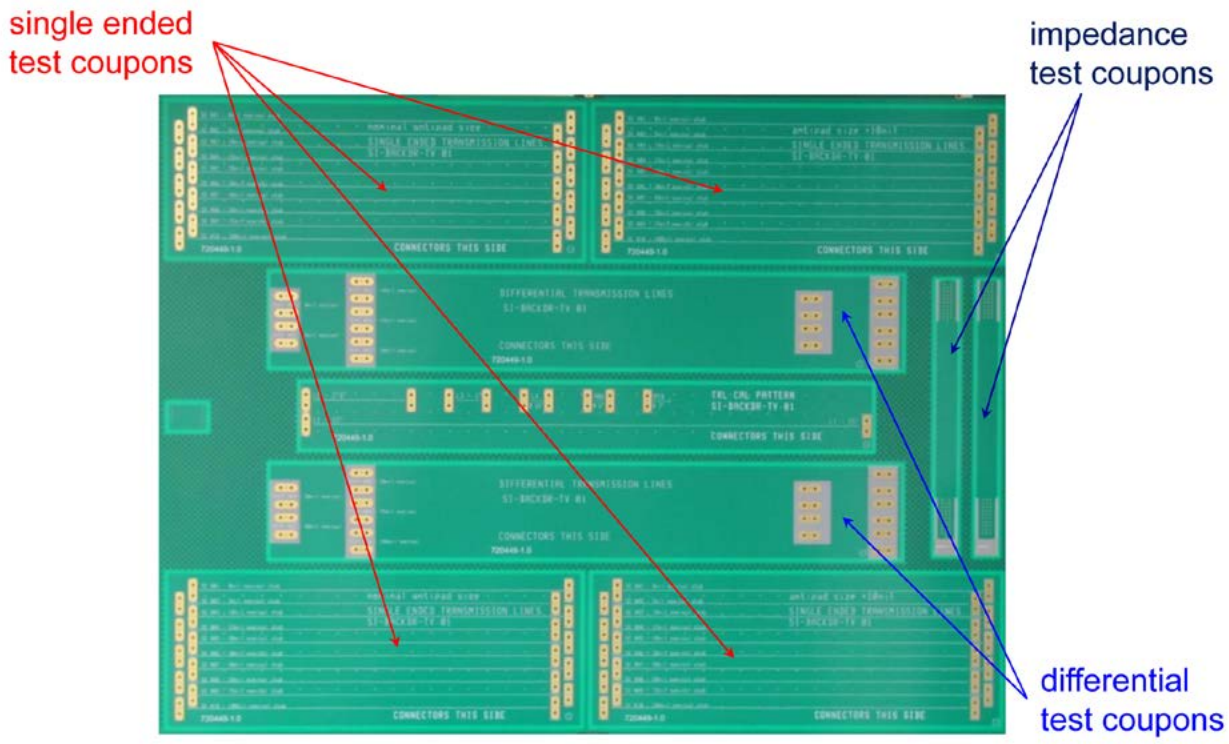


Figure 7: Test panel layout.

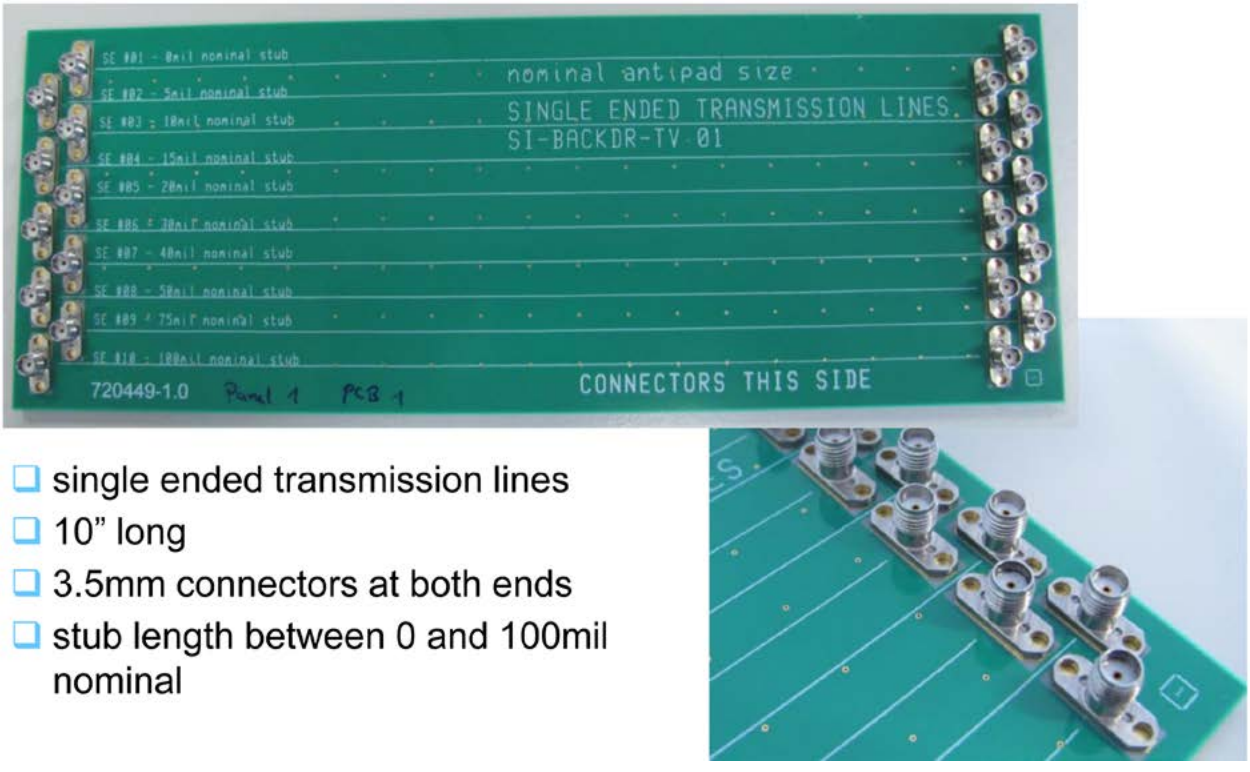


Figure 8: Single-ended coupon with connectors mounted.

INFLUENCE OF VIA STUB LENGTH AND ANTIPAD SIZE ON THE INSERTION LOSS PROFILE *continues*

average							47.56	48.23	97.19
stds							0.87	0.81	0.91
min							45.80	47.12	96.09
max							48.47	49.89	98.41
cpk							0.98	1.33	2.64
target							50.00	50.00	100.0000
lower spec limit							45.00	45.00	90.00
upper spec limit							55.00	55.00	110.00
tool#	**date**	**time**	**part#**	**serial#**	**workorder**	**datecode**	**sig3 -8.25mil**	**sig6 - 8.25mil**	**sig3 -7.25mil**
Polar3	4/20/2012	21:41	SI-BACKDR-TV	1	720449-1	1612	48.29	49.89	97.48
Polar3	4/20/2012	21:44	SI-BACKDR-TV	2	720449-1	1612	46.89	47.75	97.75
Polar3	4/20/2012	21:44	SI-BACKDR-TV	3	720449-1	1612	45.80	48.94	97.93
Polar3	4/20/2012	21:43	SI-BACKDR-TV	4	720449-1	1612	46.81	48.44	98.41
Polar3	4/20/2012	21:43	SI-BACKDR-TV	5	720449-1	1612	48.47	47.12	98.39
Polar3	5/22/2012	12:52	SI-BACKDR-TV	2	720513-1	2012	48.06	47.51	96.41
Polar3	5/22/2012	12:54	SI-BACKDR-TV	1	720513-1	2012	47.30	47.64	96.09
Polar3	5/22/2012	12:54	SI-BACKDR-TV	3	720513-1	2012	48.46	48.60	96.72
Polar3	5/22/2012	12:55	SI-BACKDR-TV	4	720513-1	2012	48.00	48.44	96.23
Polar3	5/22/2012	12:55	SI-BACKDR-TV	5	720513-1	2012	47.52	48.00	96.45

Table 1: Impedance results.

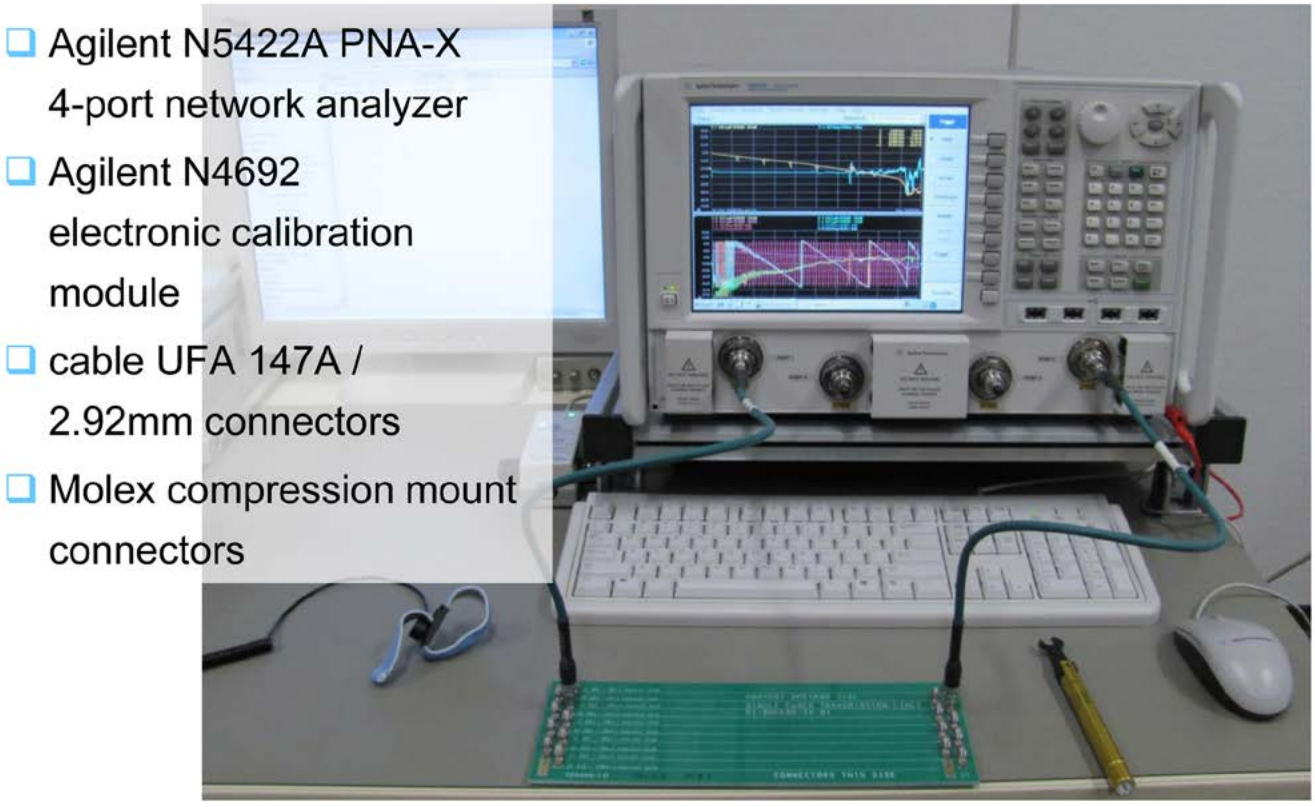


Figure 9: Single-ended insertion loss test setup.

Full 2-port and 4-port S-parameters were measured on all test boards. The data was transferred into a spreadsheet and statistics software to allow plotting of the parameters and further evaluations, like the analysis-of-variance (ANOVA) to find the 'vital few' parameters. The setup for single-ended insertion loss testing can be found in Figure 9.

Figure 10: Screen shot of single-ended insertion loss testing.

A screenshot of typical measurement data is shown in Figure 10. The orange trace in the upper portion of the display is the magnitude of insertion loss over the full frequency range for a coupon with a very short stub, where the yellow trace is for a long stub. The lower part of the screenshot shows magnitude and phase for all four single ended S-parameters.

For single-ended structures, four different antipad sizes and 10 different stub lengths were measured on five panels with two identical coupons each. This resulted in 400 full 2-port S-parameter matrices, spanning the frequency range from 10 MHz up to 40 GHz with 2048 points. To exclude odd readings in the data, the magnitude of the insertion loss was plotted for each of the 400 measurements in one chart, (Figure 11).

To get a less noisy picture of the influence of the stub length and the antipad sizes, the data of the five panels and two identical coupons for each stub length/antipad size combination were averaged and plotted (Figure 12). The via stubs cause a large resonant dip, with the longest stubs creating the notches in the insertion loss curve at lower frequencies than the shorter stubs. The antipad size generates some small changes, but with less of a clear effect than the stub length. To evaluate the influence of the antipad size, an ANOVA was performed, with results presented in Figures 17, 19, 20.

To answer the question of the maximum acceptable stub length, the additional insertion loss caused by the via stubs is extracted from

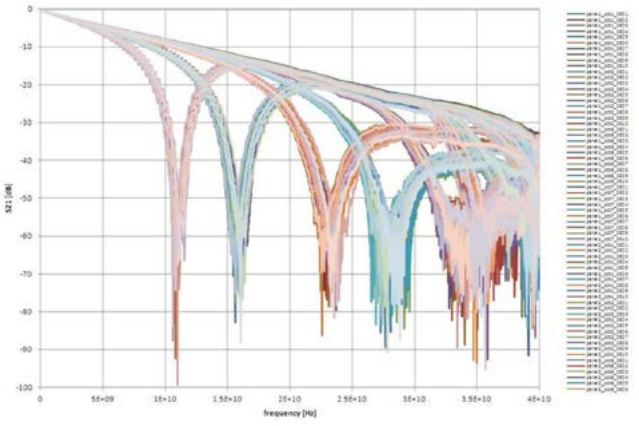


Figure 11: Raw data for S21 magnitude.

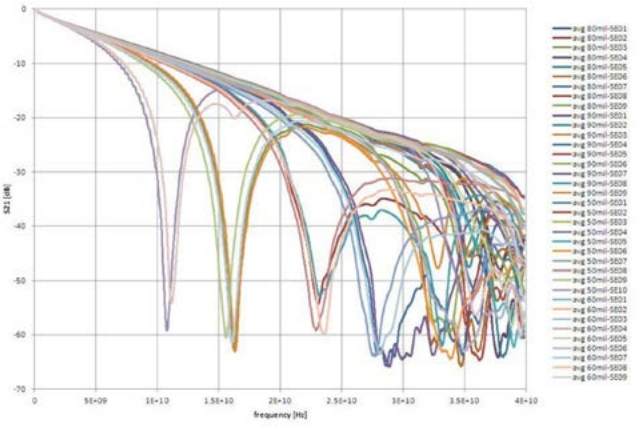


Figure 12: Average data for S21 magnitude.

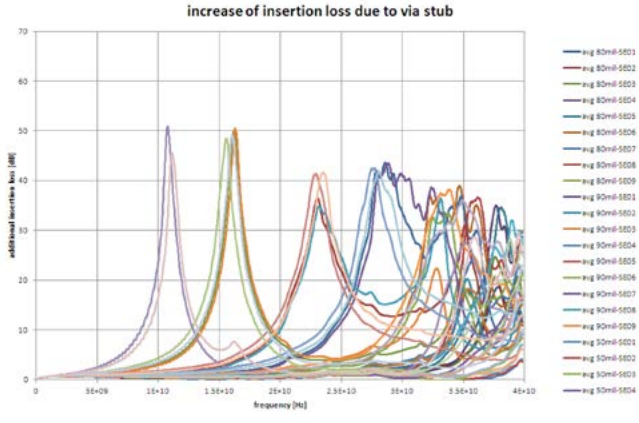


Figure 13: Additional loss caused by the via stubs.

Figure 14: Maximum acceptable stub length.

this data with a de-trend operation and plotted in Figure 13.

As an example, a maximum additional insertion loss of 5 dB might be acceptable at frequencies up to 20 GHz. Using the chart in Figure 13 and adding a forbidden zone (red hatched box), it can be found that the stub lengths SE08, SE09 and SE10 are too long and therefore add too much insertion loss. The stub length SE07 is barely acceptable in this example, whereas all shorter stub lengths pass the requirement (Figure 14).

Beside evaluating the magnitude of insertion loss, the return loss was also plotted (Figure 15). Obviously, the effect of stub length and antipad size is much less pronounced than in the insertion loss charts.

Because of the wide maxima at the resonance frequency in the return loss chart, no numerical evaluation was performed here. However, plotting the insertion loss and the return loss in one chart confirmed the expected alignment of the dips in insertion loss (IL) and maxima in return loss (RL) regarding frequency, which is shown in Figure 16 for the longer stubs.

The charts provided a good overview about the influence of the stub length and the antipad sizes, but to get quantitative data on the level of influence, ANOVA evaluations were performed. The first ANOVA shows the influence of the pa-

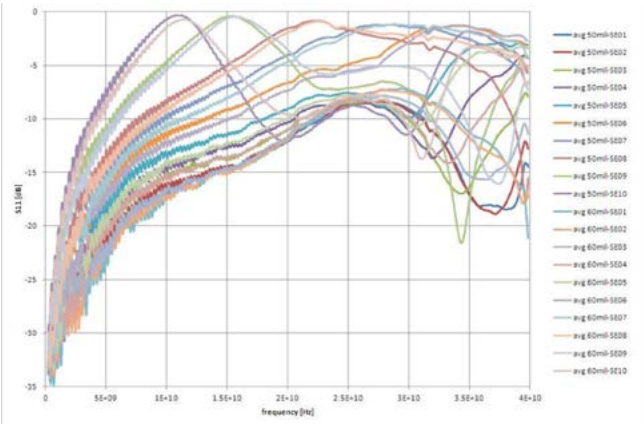


Figure 15: Averages for single ended return loss.

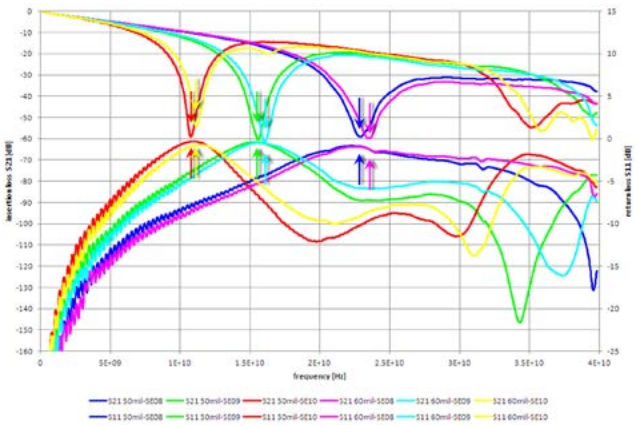


Figure 16: Alignment insertion loss and return loss.

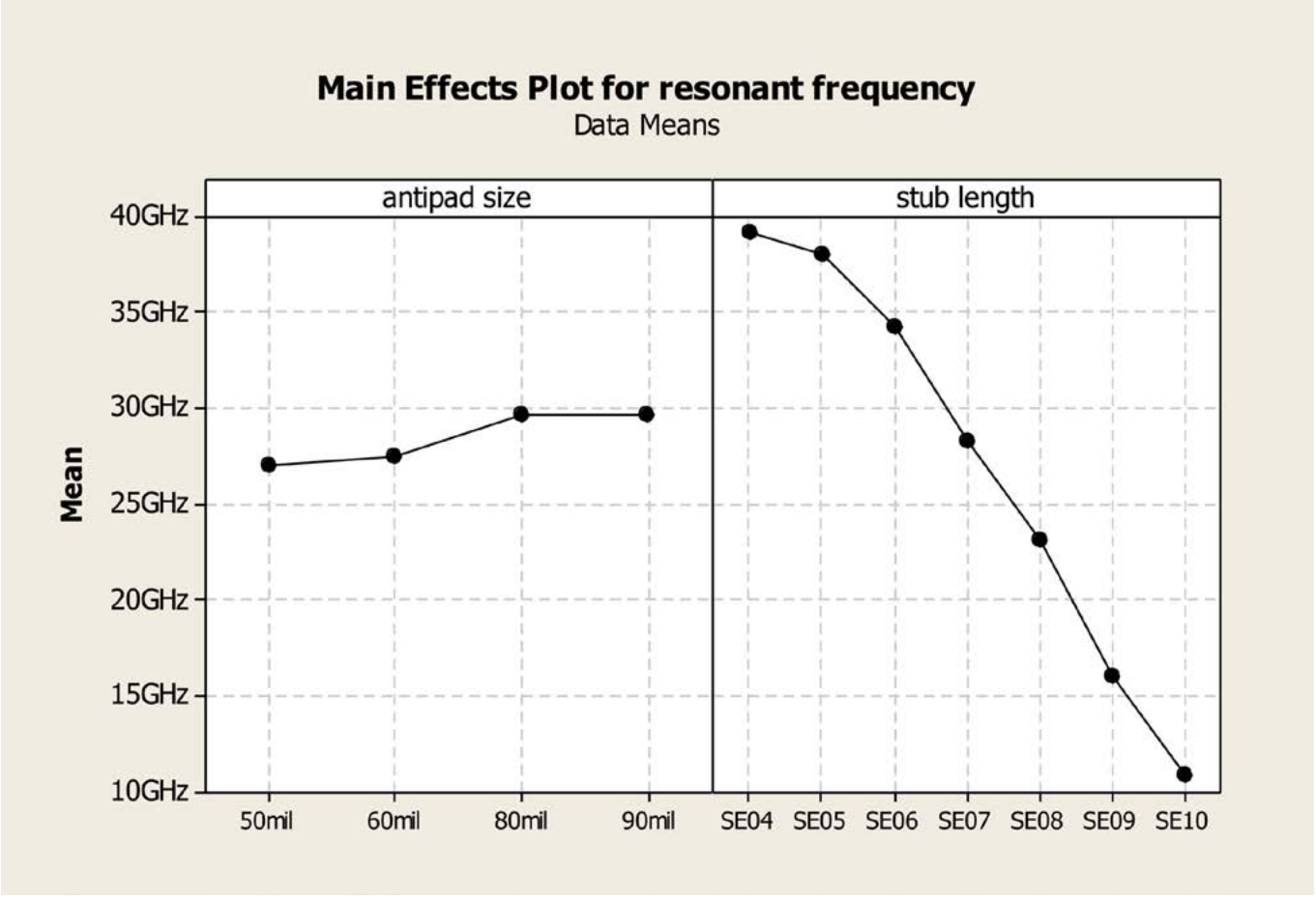


Figure 17: ANOVA chart for resonance frequency.

rameters' stub length and antipad size on the resonance frequency (Figure 17).

The main effect plot demonstrates, that larger antipad sizes increase resonance frequency slightly. The main driver however is the stub length, with the short stub length SE04 resulting in a resonance at close to 40 GHz, whereas the longest stub (SE10) creates a resonance only

INFLUENCE OF VIA STUB LENGTH AND ANTIPAD SIZE ON THE INSERTION LOSS PROFILE *continues*

```
General Linear Model: resonant frequen versus antipad size, stub length

Factor        Type   Levels  Values
antipad size  fixed       4  50mil, 60mil, 80mil, 90mil
stub length   fixed       7  SE04, SE05, SE06, SE07, SE08, SE09, SE10


Analysis of Variance for resonant frequency, using Adjusted SS for Tests

Source        DF       Seq SS       Adj SS       Adj MS       F      P
antipad size   3  3.83060E+19  1.42535E+18  4.75118E+17    0.84  0.492
stub length    6  2.26578E+21  2.26578E+21  3.77629E+20  666.95  0.000
Error         16  9.05929E+18  9.05929E+18  5.66205E+17
Total         25  2.31314E+21


S = 752466163   R-Sq = 99.61%   R-Sq(adj) = 99.39%
```

- **antipad size accounts for 1.7% of the variation → minor influence**
- **stub length accounts for 98% of the variation → major influence**
- **less than 0.5% in the error term**

Figure 18: ANOVA general linear model for resonance frequency.

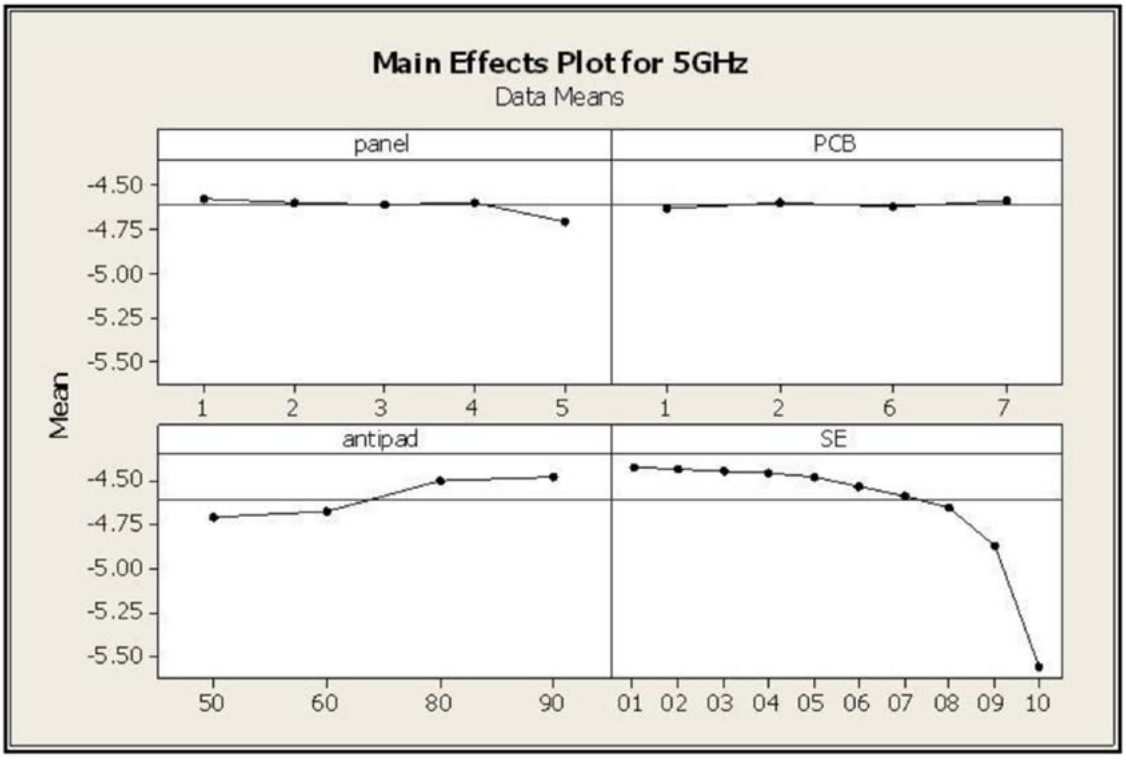


Figure 19: Main effect plot for insertion loss at 5 GHz.

marginally above 10 GHz.

To quantify the effect of the two parameters' antipad size and stub length, the numeric output from the ANOVA evaluation is used. The data show, that the stub length accounts for 98% of the variation in the resonance frequency, where the antipad size has an effect of less than 2% (Figure 18).

Another ANOVA was performed to investigate the influence of panel number, PCB number, antipad size and stub length on the absolute insertion loss value. This can be done for every frequency in the captured data (10 MHz to 40 GHz). Here only the data for 5 GHz and 10 GHz are presented as an example.

For both frequencies, there is hardly any variation over the PCB number/location of the coupon on the panel. Some variation can be seen between the five manufactured panels.

Again, the antipad size has a small influence, with the larger clearances causing less insertion loss. The main contributor is the stub length, causing an increase in the single ended insertion loss from around 4.5–5.5 dB at 5 GHz. The ANOVA main effect plots for 5 GHz and 10 GHz are shown in Figure 19 and Figure 20.

Using the numeric output of the ANOVA at 5 GHz (frequency chosen as one example), shows the panel to be a minor influence causing only 1.8% of the variation. The antipad size is a second order influence with an effect of 11.3% and the stub length is again the major influence, being the cause of 83.2% of the variation, as shown in Figure 21.

Differential Insertion Loss Testing

The setup for the differential insertion loss testing can be found in Figure 22. A 4-port vector network analyzer was calibrated at the connector interface to the device-under-test with an electronic calibration module. The use of the eCal module lead to a significantly faster, easier and virtually error proof calibration process, especially for the 4-port calibration. On the test board, the interface to the VNA was provided with flange mounted compression type connectors.

Figure 23 shows a screenshot of two different stub lengths superimposed. The upper por-

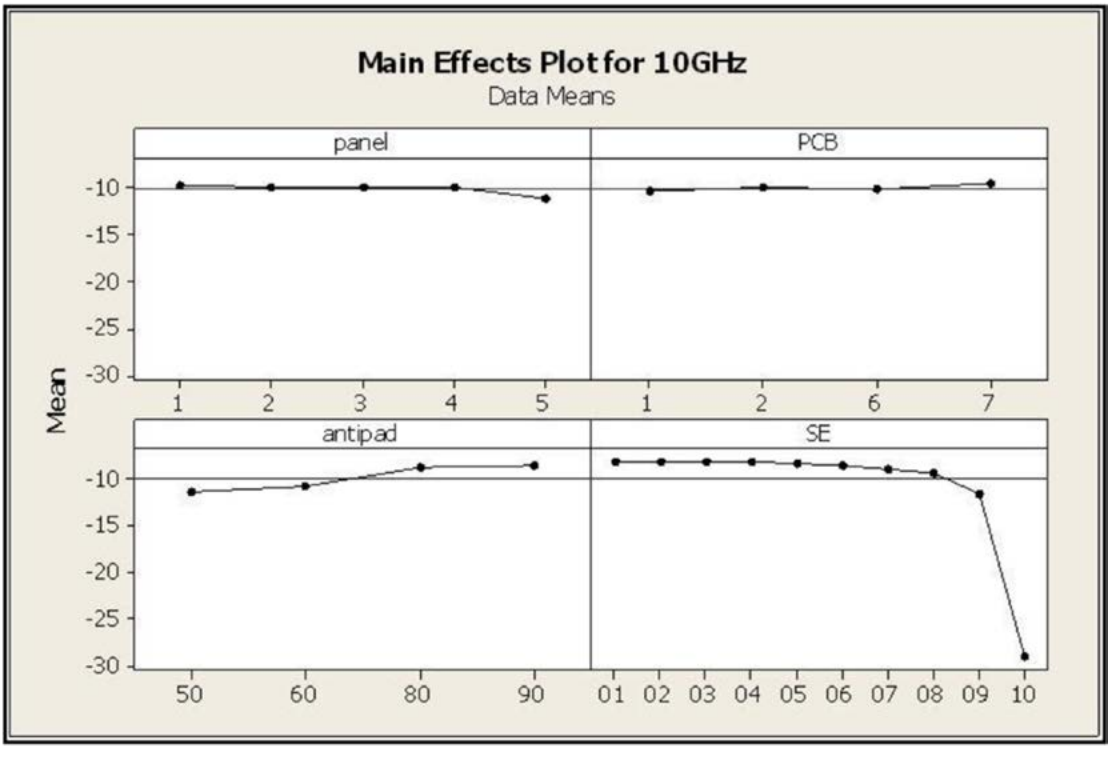


Figure 20: Main effect plot for insertion loss at 10 GHz.

INFLUENCE OF VIA STUB LENGTH AND ANTIPAD SIZE ON THE INSERTION LOSS PROFILE *continues*

```
General Linear Model: 5GHz versus panel, antipad, SE

Factor   Type   Levels  Values
panel    fixed       5  1, 2, 3, 4, 5
antipad  fixed       4  50, 60, 80, 90
SE       fixed      10  01, 02, 03, 04, 05, 06, 07, 08, 09, 10


Analysis of Variance for 5GHz, using Adjusted SS for Tests

Source     DF   Seq SS   Adj SS  Adj MS       F      P
panel       4   0.4770   0.0701  0.0175    5.41  0.000
antipad     3   3.0815   0.8301  0.2767   85.45  0.000
SE          9  22.6476  22.6476  2.5164  777.07  0.000
Error     316   1.0233   1.0233  0.0032
Total     332  27.2293


S = 0.0569063   R-Sq = 96.24%   R-Sq(adj) = 96.05%
```

- **panel accounts for 1.8% of the variation → minor influence**
- **antipad size accounts for 11.3% of the variation → second order influence**
- **stub length accounts for 83.2% of the variation → major influence**

Figure 21: ANOVA general linear model for insertion loss at 5 GHz.

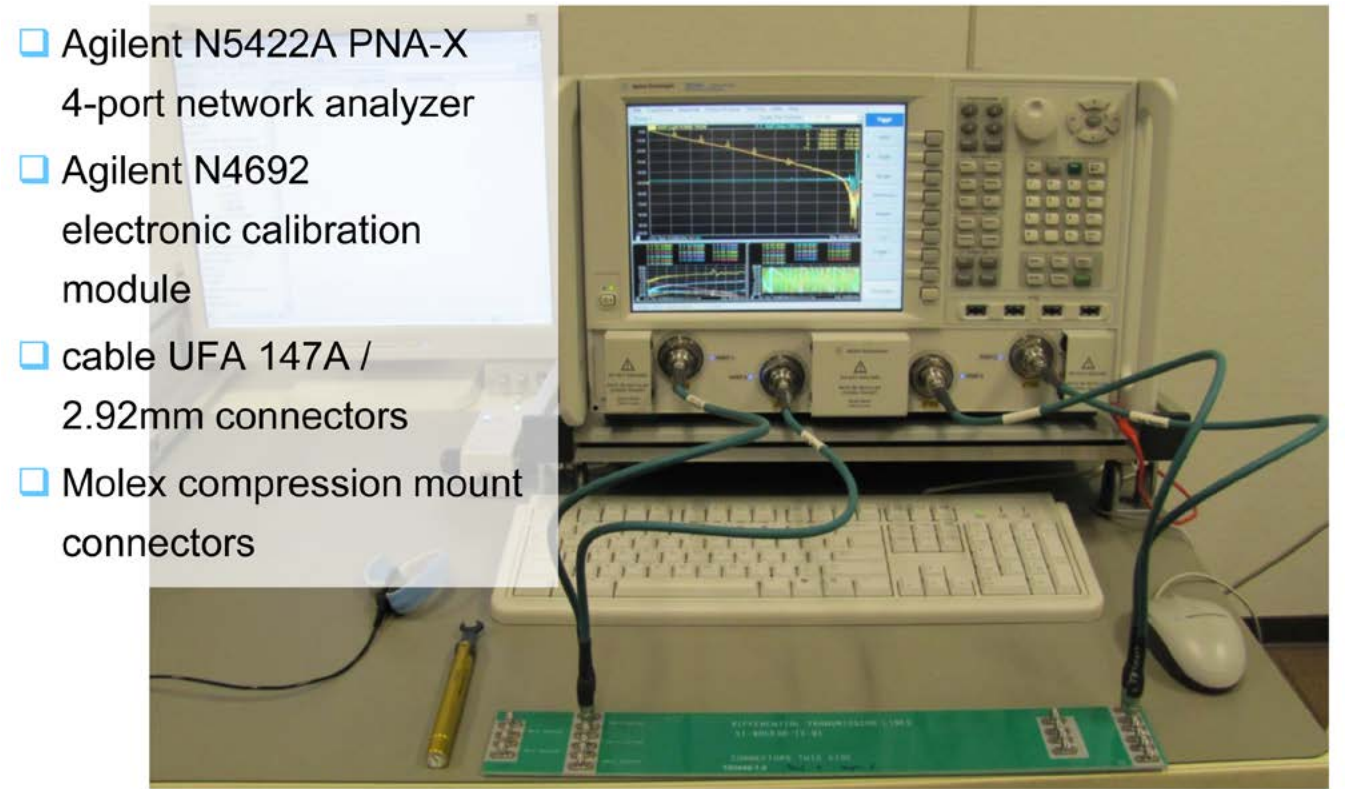


Figure 22: Differential insertion loss setup.

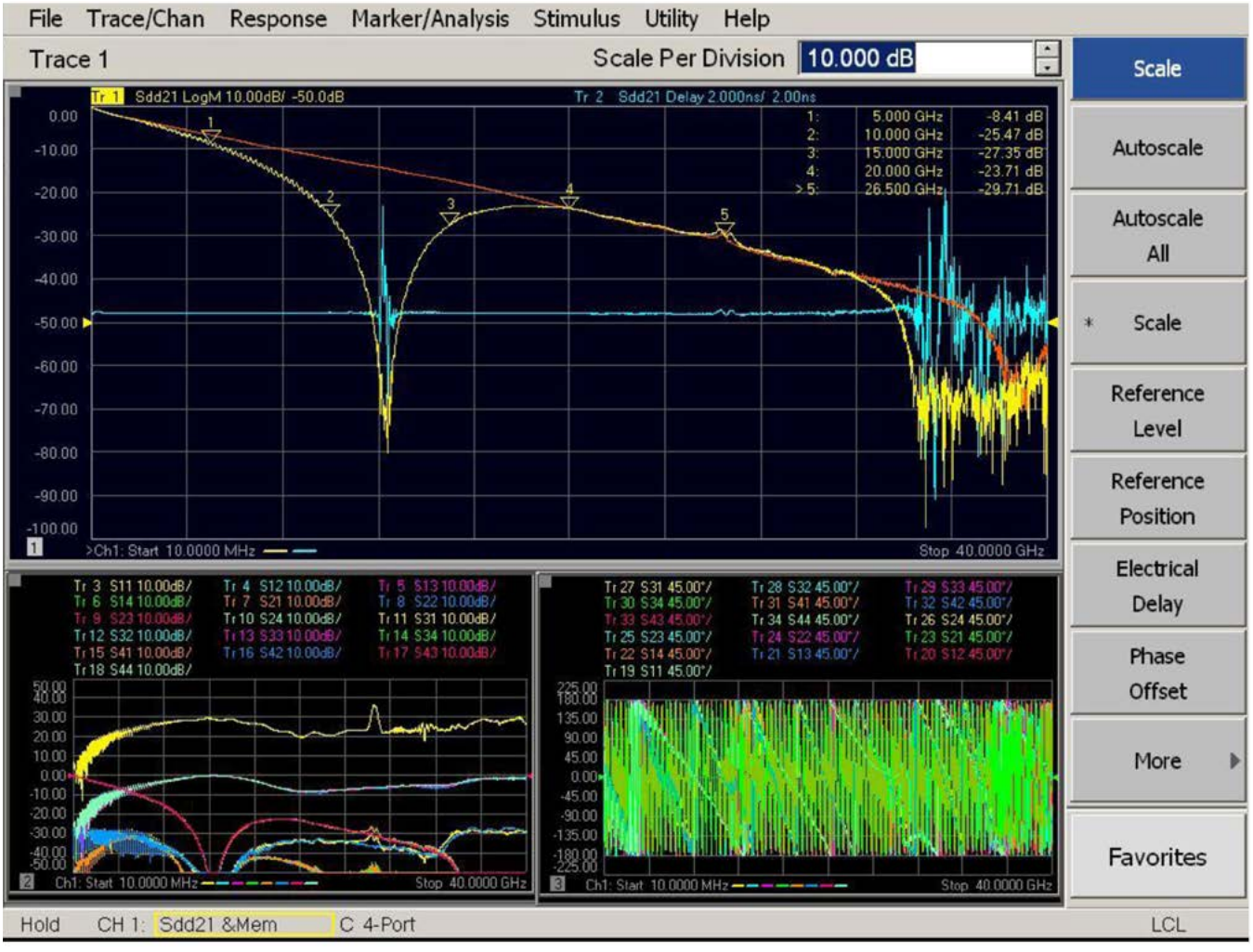


Figure 23: Screen shot of differential insertion loss testing.

tion of the display shows the amplitude of the differential insertion loss SDD21. The orange trace is for a coupon with nearly optimum backdrilling (minimum stub), with the yellow trace showing SDD21 for a differential pair with long via stubs. The bottom portion of the screenshot displays the amplitude (left) and phase (right) of all 16 mixed mode S-parameters.

For the differential testing, mixed mode S-parameters were measured on 10 different stub lengths, two different antipad sizes and five panels, testing from 10 MHz to 40 GHz with 2048 points. Similar as with the single ended data, the magnitude of the differential insertion loss was plotted for all 100 differential pairs to check for unusual readings (Figure 24). The averages over the five panels were plotted for the 10 stub lengths and two antipad sizes, to visualize the impact of the parameters (Figure 25).

Figure 25 clearly demonstrates the increase of the resonant frequency for shorter stub lengths and also some smaller changes caused by the antipad size. To get the full picture on the influence of the panel, the antipad size and the stub length, an analysis-of-variance on the magnitude of SDD21 was conducted for various frequencies. Figure 26 shows the main effect plot of this ANOVA for a frequency of 5 GHz.

The main effect plot confirms a very small panel-to-panel variation. The effect of the antipad size is slightly larger, but the main influence clearly is the stub length. To get quantita-

INFLUENCE OF VIA STUB LENGTH AND ANTIPAD SIZE ON THE INSERTION LOSS PROFILE *continues*

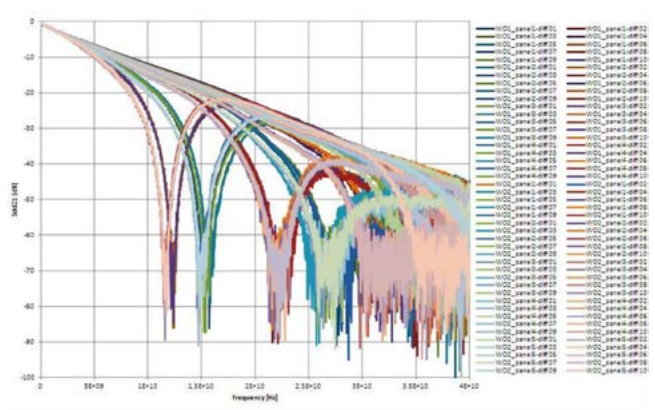


Figure 24: Raw data of SDD21 magnitude.

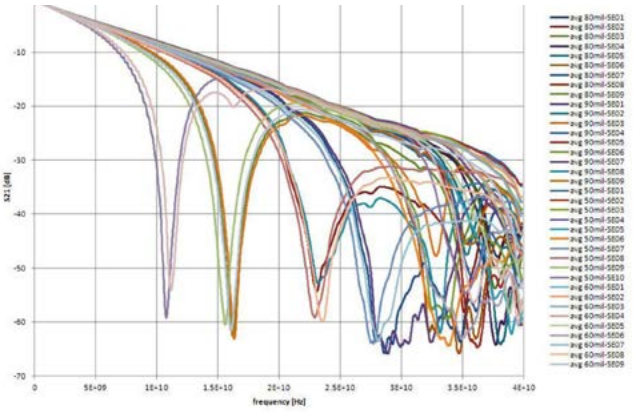


Figure 25: Average data for magnitude of SDD21.

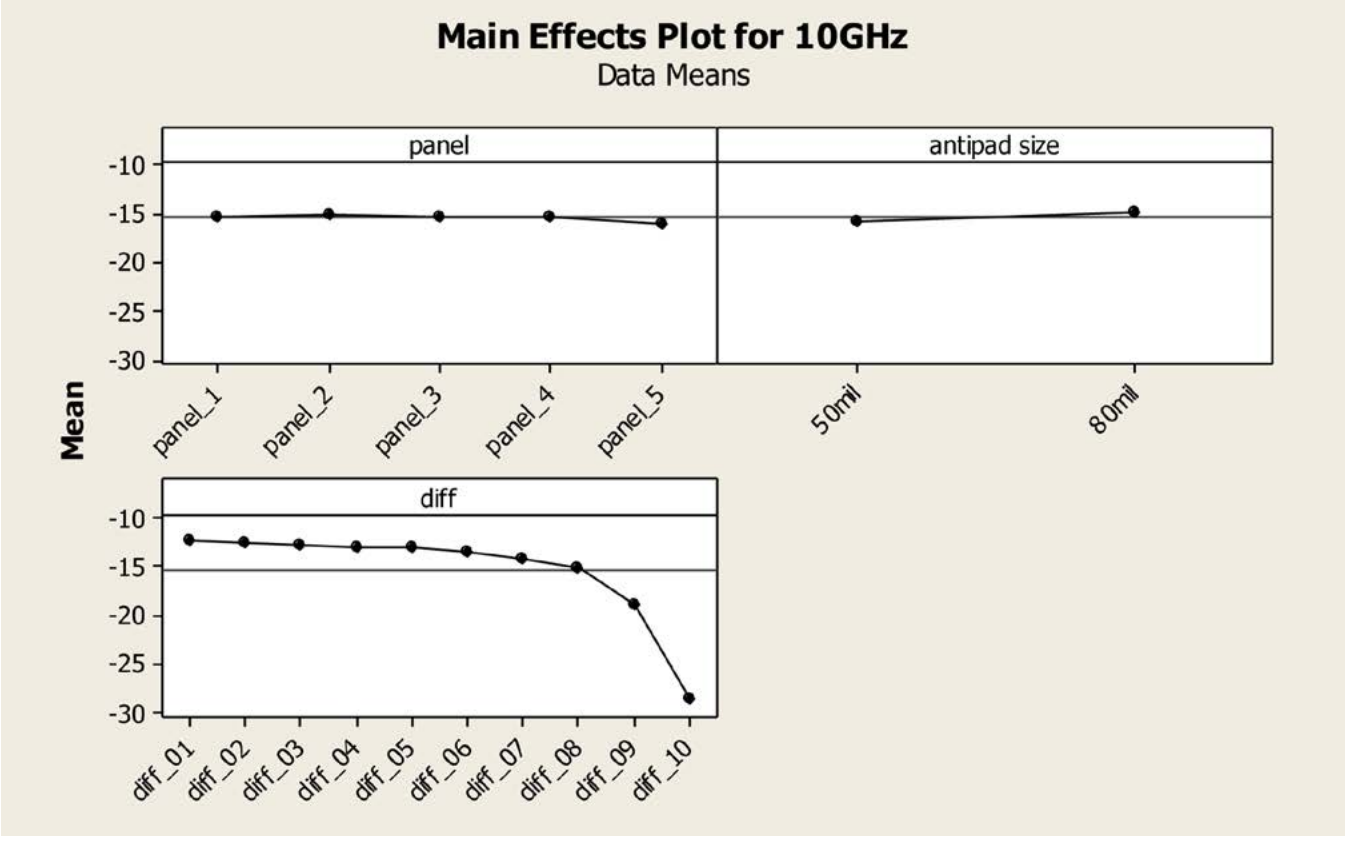


Figure 26: Main effect plot for magnitude SDD21 at 5 GHz.

tive data on the effects, the numerical ANOVA data is evaluated, showing the panel to have only a 0.7% variation and the antipad size to account for 3.5% of the variation. The stub length causes 91.3% of the variation, which therefore has by far the largest influence (Figure 27).

Cross-Section Evaluation

After completing the TDR and VNA evaluation, actual stub length measurements of the launch vias have been made using cross sections. Figure 28 shows examples of the depths, between "SE01," which was virtually no stub at

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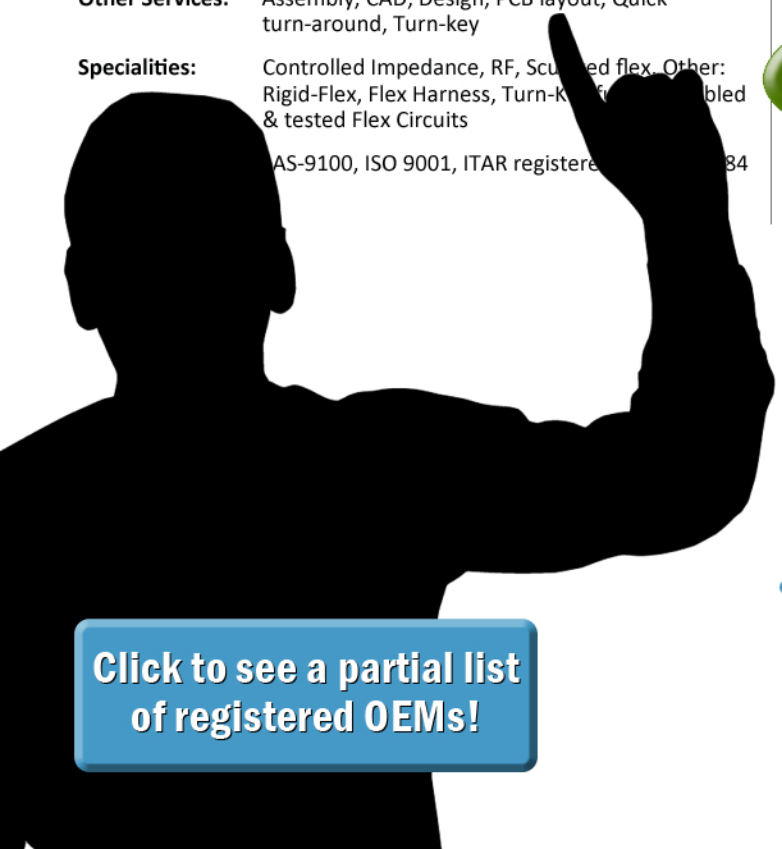

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INFLUENCE OF VIA STUB LENGTH AND ANTIPAD SIZE ON THE INSERTION LOSS PROFILE *continues*

```
General Linear Model: 5GHz versus panel, antipad size, diff

Factor        Type   Levels  Values
panel         fixed       5  panel_1, panel_2, panel_3, panel_4, panel_5
antipad size  fixed       2  50mil, 80mil
diff          fixed      10  diff_01, diff_02, diff_03, diff_04, diff_05,
                             diff_06, diff_07, diff_08, diff_09, diff_10


Analysis of Variance for 5GHz, using Adjusted SS for Tests

Source        DF   Seq SS   Adj SS  Adj MS       F      P
panel          4   0.2908   0.0467  0.0117    0.48  0.753
antipad size   1   1.4273   1.8685  1.8685   76.33  0.000
diff           9  36.7577  36.7577  4.0842  166.83  0.000
Error         72   1.7627   1.7627  0.0245
Total         86  40.2385

S = 0.156465   R-Sq = 95.62%   R-Sq(adj) = 94.77%
```

- panel accounts for 0.7% of the variation → minor influence
- antipad size accounts for 3.5% of the variation → second order influence
- stub length accounts for 91.3% of the variation → major influence

Figure 27: ANOVA general linear model for differential insertion loss at 5 GHz.

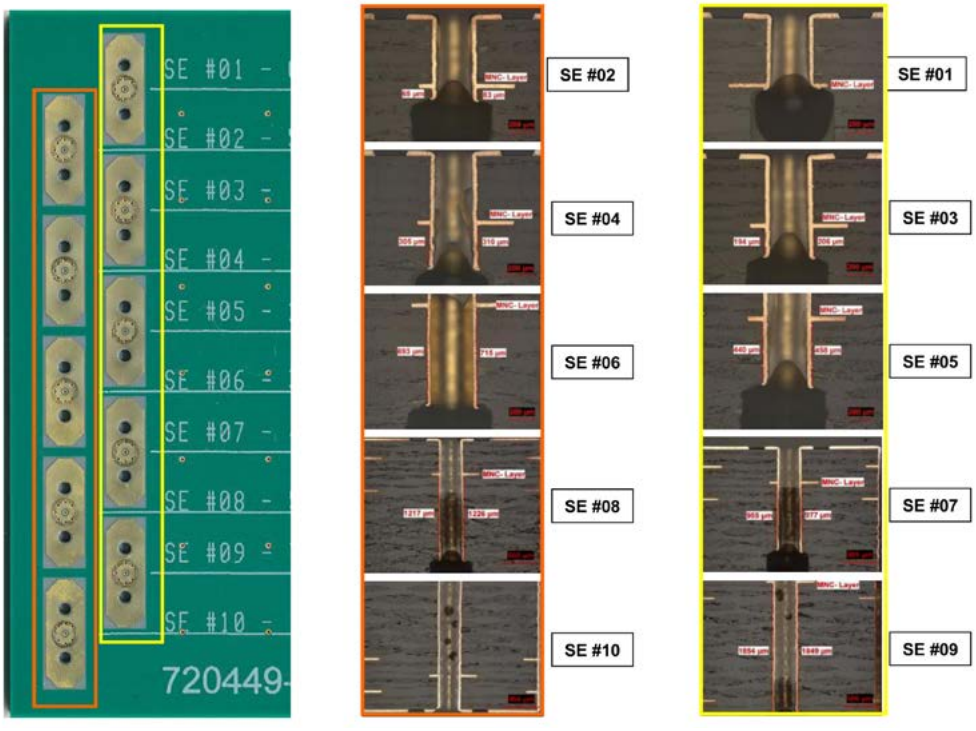

Figure 28: Cross-sections of via stubs.

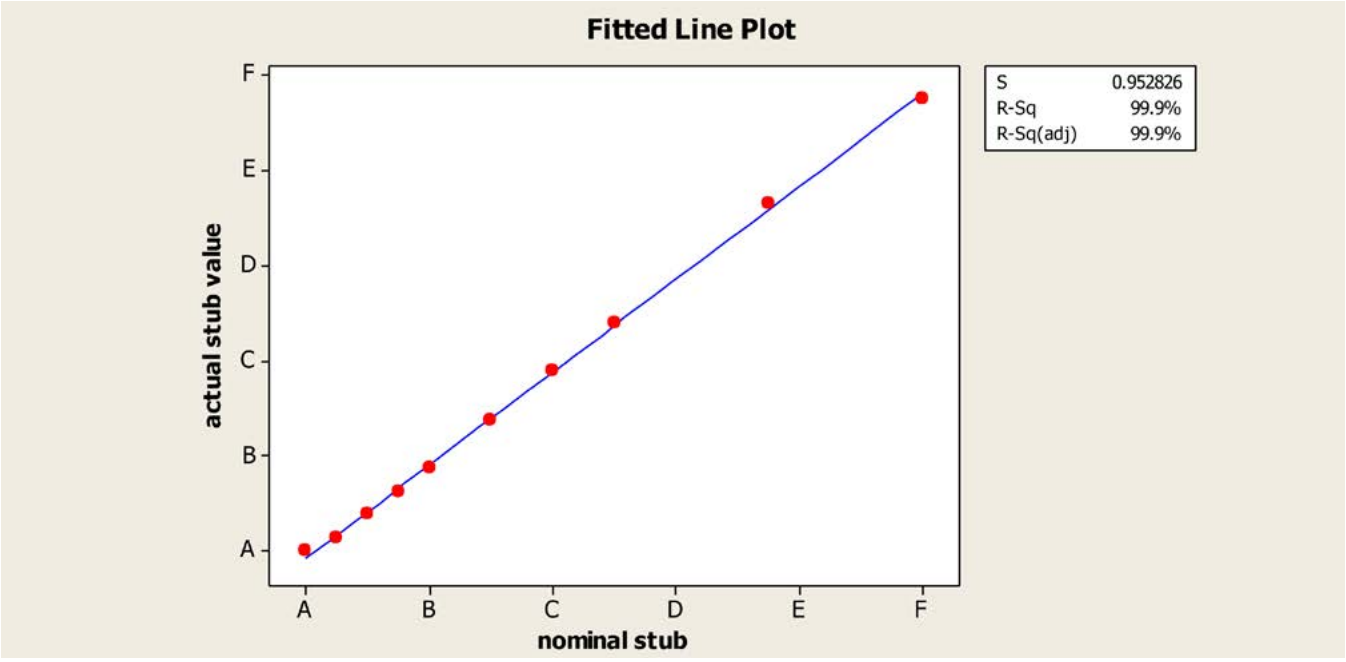

Figure 29: Fitted line plot for actual versus nominal stub length.

all to "SE10," the maximum stub length.

The measured stub length was plotted against the nominal stub length (Figure 29). Obviously, actual stub lengths and target stub lengths correlate tightly. This can be considered as proof that the backdrilling operation was well under control.

Summary

In this investigation, data were generated to predict the additional insertion loss generated by via stubs of the launch vias. The effect on the frequency of the resonant notch in the loss profile was also demonstrated. Both parameters were evaluated over various stub lengths and antipad sizes.

The data confirmed that a larger via stub reduces the resonant frequency and increases the overall insertion loss. It was also demonstrated that a smaller antipad size has the same effect, but to a much smaller degree. **PCBDESIGN**

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Alexander Ippich is a senior signal integrity engineer at Multek. Previously, he held various positions in Application Engineering and R&D. He worked also in the development of thin film TFT matrixes and LCD displays. His PCB manufacturing and engineering experience dates back to 1993. He received his degree in electrical engineering from University Stuttgart, Germany.

Mil/Aero007 News Highlights

Ducommun Gains Major Parker Aerospace Airbus Contract

The company has received a multiyear contract from Parker Aerospace, a unit of Parker Hannifin Corporation, to produce complex PCBs assemblies for use in the fuel management system of the Airbus A350 family of commercial aircraft. The award has a potential value in excess of $20 million over the contract period.

Sparton, USSI JV Nets $2.8M in Subcontracts

Sparton Corporation and USSI, a subsidiary of Ultra Electronics Holdings plc, announce the award of subcontracts valued at $2.8 million from their ERAPSCO/SonobuoyTech Systems joint venture.

Axis Leads 2014 UK Aerospace Youth Rocketry Challenge

Axis Electronics apprentices joined more than 25 MPs who teamed up with aerospace apprentices from all over the UK to take part in a rocket launching competition. The aim was to achieve the greatest vertical distance.

Blackfox, Lockheed Martin Celebrate 'Hire a Veteran Month'

Last month, Denver's 9News featured a segment with Andrew Stone of Lockheed Martin discussing his company's plan to hire nearly 180 veterans for high-tech positions in assembly during "Hire a Veteran Month."

ESCATEC is Founding Member of Swiss Photonics Group

"Being a founding member of this SWISSMEN professional group for the Photonics industry, puts ESCATEC in a very good position to support this growing industry in Switzerland with ESCATEC's outstanding knowledge and experience in research, design, and development," said Dr. Thomas Dekorsy, general manager.

IMET is Philadelphia's Manufacturer of the Year

IMET Corporation, a contract manufacturer providing electronics engineering services and PCB assembly, has received the 31st annual Manufacturer of The Year Excellence Award by The Greater Philadelphia Chamber of Commerce.

NASA, CCAM Partner to Advance Technology & Innovation

NASA and the Commonwealth Center for Advanced Manufacturing (CCAM) in Richmond, Virginia, have joined forces to advance technology and innovation.

U.S. Aviation Industry Poised to Enter Second Golden Age

"Emerging foreign competitors are ramping up their capabilities and technological advancements in their home markets, and are even expanding their manufacturing footprint here in the U.S. in ways that will likely alter the industry's competitive landscape through this decade and beyond," said Scott Thompson, PwC's U.S. aerospace and defense leader.

IDtechEx: Electrics Will Be the Future of UAVs

The total market value for electric unmanned aerial vehicles (UAVs) will reach over one billion dollars by 2023 according to findings in the new IDTechEx report, "Electric Unmanned Aerial Vehicles (UAV) 2013-2023."

Total Avionics Sales to Exceed $1.72 Billion

The Aircraft Electronics Association announced its third quarter Avionics Market Report for this year. In the months of July, August and September 2013, total worldwide avionics sales amounted to $1,721,888,397.14, or more than $1.72 billion, as reported by the 20 aviation electronics manufacturers participating in the report.

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Pulse Laser Wins German Future Prize 2013

Scientists from Bosch, TRUMPF, Jena University, and Fraunhofer IOF have turned the ultra-short-pulse laser into an effective series-production tool. For their collective effort they were awarded the German Future Prize 2013 on December 4, 2013.

Although lasers are an indispensable part of industrial manufacturing, in some areas conventional systems are reaching the limits of what they can do. A laser beam directed at a piece of metal will cause the metal to heat up and partially vaporize and melt. However, controlling the properties of melted materials is extremely difficult--imperfections develop, meaning that manufacturers still have to go to the trouble of re-working the workpiece. This costs both time and money.

Little by little, a USP laser can remove, or ablate, tiny areas measuring just a few millionths of a millimeter (nanometers). At lightning speed, a computer-controlled mirror system makes sure the laser pulses hit the right spot. "Hundreds of thousands of pulses per second lead to a melt-free processing with unparalleled precision," explains Dr. Jens König from technology company Bosch. Using "cold ablation," as it is also known among engineers, it is even possible to engrave incredibly fine structues onto the head of a match without igniting it.

In recognition of their outstanding work, German President Joachim Gauck presented Jens König, Dirk Sutter, and Stefan Nolte with the German Future Prize 2013 on December 4, 2013. The price for technology and innovation honors top scientific work that displays great economic potential. This highly respected prize has been awarded annually since 1997 and comes with 250,000 euros in prize money.

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TOP TEN

News Highlights from PCBDesign007 this Month

① Top 10 Most-read PCB Design Magazine Articles of 2013

When our contributors speak, people listen! We've compiled a list of 10 of the most-read PCB Design Magazine articles in 2013. Take another look and enjoy these gems one more time.

② Top 10 Most-read PCBDesign007 Columns of 2013

It's been a wild year in the PCB design community. Naturally, the top PCBDesign007 columns of 2013 cover a maze of topics, from delamination to routing techniques. So, without further ado, here are the Top 10 most-read PCBDesign007 columns of the past year.

③ Mentor's Capital Tool Adds S1000D Compliance

The Capital suite addresses vehicle electrical system definition, design, manufacture, and service. S1000D support is one of over 60 new capabilities available in the latest version. Users can automatically generate S1000D-compliant information packages directly from their electrical design data using the Capital Publisher tool, reducing the costs and lead times associated with documentation creation.

④ CAM Engineering Easier with Ucamco's Integr8tor 8.2

Ucamco is delighted to announce its release of Integr8tor 8.2. This is the latest generation of a unique suite of tools that support the CAD-to-CAM data transfer process as well as pre-CAM and CAM functions in PCB manufacture.

5 IPC Releases New Document Pricing Structure

On January 12, 2014, IPC will implement a new, simplified pricing structure for standards and technical documents. The new pricing structure is based on the complexity of the document (number of pages, number of images and color), with three distinct pricing levels.

6 PCB West 2014 Dates Announced

UP Media Group Inc. has announced the annual PCB West 2014 will be held September 9-11, 2014, in Santa Clara, California. The event includes a three-day technical conference and one-day exhibition to be held at the Santa Clara Convention Center.

7 IEEE: Stakeholders Want Standards-based Interoperability & Communications

Every year, tens of billions of dollars reportedly slip through the cracks in interoperability and connectivity among medical devices in the United States alone. But now there seems to be interest in closing those gaps in the global web of healthcare, says the IEEE Standards Association.

8 EMA's Simulation Team Welcomes Mike Rogers

"Mike brings a wealth of injection molding experience to our team enabling him to support our Autodesk customers with his application knowledge and expertise," said Manny Marcano, president and CEO. "His experience rounds out our simulation competencies allowing us to cover the full Autodesk mechanical simulation product line."

9 DesignCon Introduces Keynote Speakers & New Tech Director

The 2014 DesignCon program, which comprises the largest educational conference and technology exhibition for chip, board, and systems design engineers in the high-speed communications and semiconductor communities, will provide attendees with an array of in-depth technical education and training opportunities.

10 Nakahara's Japanese PCB Industry Update

The Japanese PCB industry is following N. America's trajectory. Once a $12 billion "domestic output," Japanese PCB production is dropping to $5 billion asymptotically while its overseas production continues to increase. However, profits are declining continuously.

events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out *The PCB Design Magazine's* event calendar.

International Electronic Components Trade Show
January 15–17, 2014
Tokyo, Japan

Microtech Japan
January 15–17, 2014
Tokyo, Japan

Electrotest Japan
January 15–17, 2014
Tokyo, Japan

Material Japan
January 15–17, 2014
Tokyo, Japan

NEPCON Japan
January 15–17, 2014
Tokyo, Japan

PWB Expo
January 15–17, 2014
Tokyo, Japan

15th IC Packaging Expo
January 15–17, 2014
Tokyo, Japan

Lighting Japan
January 15–17, 2014
Tokyo, Japan

CAR-ELE Japan
January 15–17, 2014
Tokyo, Japan

EV Japan
January 15–17, 2014
Tokyo, Japan

DesignCon 2014
January 29–30, 2014
Santa Clara, California

SPIE Electronic Imaging
February 2–6, 2014
San Francisco, USA

Pan Pacific Microelectronics Symposium
February 11–13, 2014
The Big Island, Hawaii

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Next Month in *The PCB Design Magazine:*

High-speed Design

What's the state-of-the-art in high-speed design? And what exactly constitutes high speed in 2014? Find out in the February issue of *The PCB Design Magazine,* when our expert contributors discuss design on the bleeding edge. And don't miss our featured coverage of DesignCon 2014.

See you next month!