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March 2016

an I·Connect007 publication

Strategies to Increase Profit

The Top 10 Ways

Designers Can Increase Profits

by Mark Thompson, pg. 10

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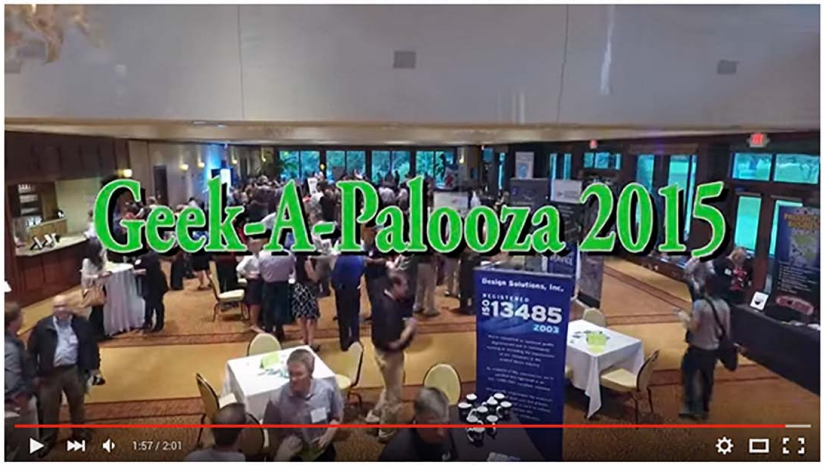

Check out this short drone video of last year's event in Minneapolis where we hosted over 300 attendees.

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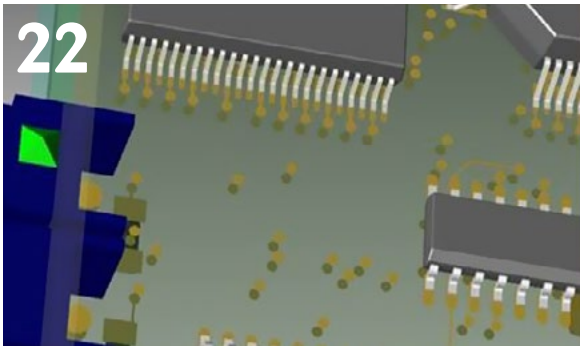
Feature Content

Design Strategies for Success—and Profit

Designers have a plethora of ideas about how to best layout a PCB. But how many designers understand that good design techniques can lead their company to greater success, and even profit? In our cover story, Prototron's Mark Thompson offers 10 design strategies that can help your bottom line. We also feature articles on profitable design strategies by Gary Griffin of Fast Interconnect and Barry Olney of In-Circuit Design Pty Ltd. And we round out this issue with interviews with Nolan Johnson of Sunstone Circuits and Greg Roberts of EMA Design Automation.



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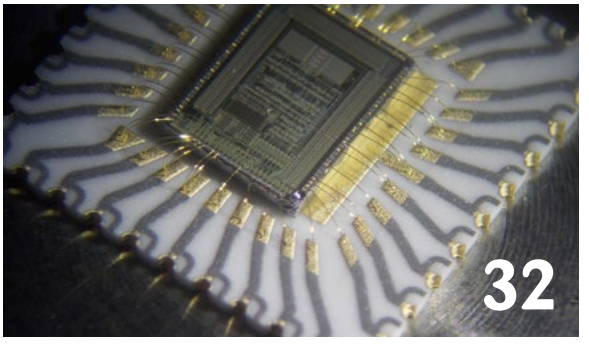


More Content

Back to Vegas

by Andy Shaughnessy
I-CONNECT007

It's almost time to head back to Las Vegas for IPC APEX EXPO, along with my favorite event, the Design Forum. I'm glad to be heading back to the land of Lost Wages, and in a new venue, the Las Vegas Convention Center. The last time I attended a trade show in the convention center was in the summer of 2001 for the Design Automation Conference.

DAC was held in June that year; who had that bright idea? I guess the surface of the sun was booked! That year, I perfected the art of "shade darting," running from one bit of shade to the next. It was 108° the entire week of DAC 2001, and it was so hot that the cab drivers almost turned on their air conditioning. Let's hear some applause for IPC not holding APEX in Vegas during the summer months.

So we're back in Vegas again. But I've heard grumbling from people in the electronics industry who are worried that attendance is going to drop off this year. You've heard the traditional arguments for holding APEX in San Diego vs. Las Vegas: There are hundreds of circuit board companies and defense contractors in and around San Diego, the weather is perfect, and your manager is more likely to sign off on a visit to San Diego than Vegas. IPC knows this, of course, and I understand that they'll be holding APEX in San Diego in 2017 and for several years after that. You can't please everyone.

The I-Connect007 team will get to Vegas over the weekend and start planning our wall-to-wall coverage. I get started early in the week with my coverage of the Design Forum on Monday, March 14. Anne Marie Mulvihill and her accomplices at IPC have set up a solid design program. The subtitle of Dale Parker's keynote speech offers a hint of what you can expect: "Brother, Can You Par-a-Digm?" Parker is the eCAD tools and support manager for Google/Alphabet, and he'll be discussing "Paradigm Shifts Required to Accomplish Next-Generation Technical Innovation."

Next, Gary Carter of Fujitsu, Humair Mandavia of Zuken, and Hemant Shah and Ed Acheson of Cadence Design Systems will present "Seamless Data Transmission from Design through Assembly: Briefing from the IPC-2581 Consortium." Speaking of which, if any of you are using IPC-2581 on a regular basis, I'd like to hear about your experience. Have you ever designed a PCB using this neutral data transfer standard?

Then, Karen McConnell of Northrop Grumman, Dock Brown of DfR Solutions, and Dale Lee of Plexus will discuss "Developing a DFX Program for Your Organization: DRC in a Layout Tool vs. DFX Rules When Checking a Board." That sounds like a great session; Karen is a hoot, as well as a great instructor. Cherie

Figure 1: Kelly Dack, PCB designer, gentleman farmer and novice cattleman.

Litson of Litson Consulting follows with "New Developments in IPC Industry Standards: A Review of Key Issues for Design Teams," and our own columnist and technologist Vern Solberg of Solberg Technical Consulting updates us on IPC-7091 and 7092 with his talk, "2D, 2.5D and 3D Package Technology: Embedded Component and Advanced Semiconductor Package Innovation."

With so much talk about the need for (and lack of) good communication between designers and fabricators, "Making Your Design-Fabrication Collaboration Most Effective" should draw a good crowd. Mike Creeden of San Diego PCB will be joined by contributors Tom Clifford of TJB Associates and Phil Marcoux of the Fab Owners Association. And rounding out the Design Forum is a presentation by Stephen Chavez of UTC Aerospace Systems and Scott McCurdy of Freedom CAD, "Continue Your Professional Development with IPC Design Programs, Technical Education and Networking."

It sounds like a great Design Forum. I'll be there bright and early Monday. Unfortunately, our guest editor and contributor Kelly Dack won't be with us at APEX. Kelly is taking delivery of seven head of cattle next week. No, Kelly does not know anything about cattle; he's from Southern California. He never even lived on a farm until he moved to Spokane, Washington this year. Let's wish Farmer Kelly luck with his efforts at animal husbandry!

Profitable Design Strategies

We have a great issue for you this month. We're focusing on design strategies that can lead your company to success, and profit. Yes, as Mark Thompson of Prototron explains in our cover story, even the "lowly designer" has some control over the company's bottom line. And we have feature articles on profitable design strategies from Gary Griffin of Fast Interconnect and Barry Olney of In-Circuit Design Pty Ltd.

We also bring you interviews with Greg Roberts of EMA Design Automation and Nolan Johnson of Sunstone Circuits, as well as contributions from columnists Tim Haag, Phil Kinner, Doug Brooks and Istvan Novak.

I better wrap it up and get my clothes to the dry cleaner. I hope to see you at IPC APEX EXPO and the Design Forum. If you can't make it, don't worry; we'll be covering the show from start to finish. **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 16 years. He can be reached by clicking here.

The Top 10 Ways
Designers Can Increase Profits

by Mark Thompson, CID
PROTOTRON CIRCUITS

Some of you are probably wondering about the title of this article. "What could Mark possibly mean? How can a lowly PCB designer like me increase our company's profits?"

So can you truly increase profitability through PCB design practices? Yes, you can. And it starts with a philosophy that embraces DFM techniques. Then you must be ready for the initial release to a fabricator by ensuring that you are communicating all of your specifications and needs clearly to the fabrication house so that you get an accurate quote.

Let's dive in, starting with Number 10 and working our way to the most important way a designer can increase company profits.

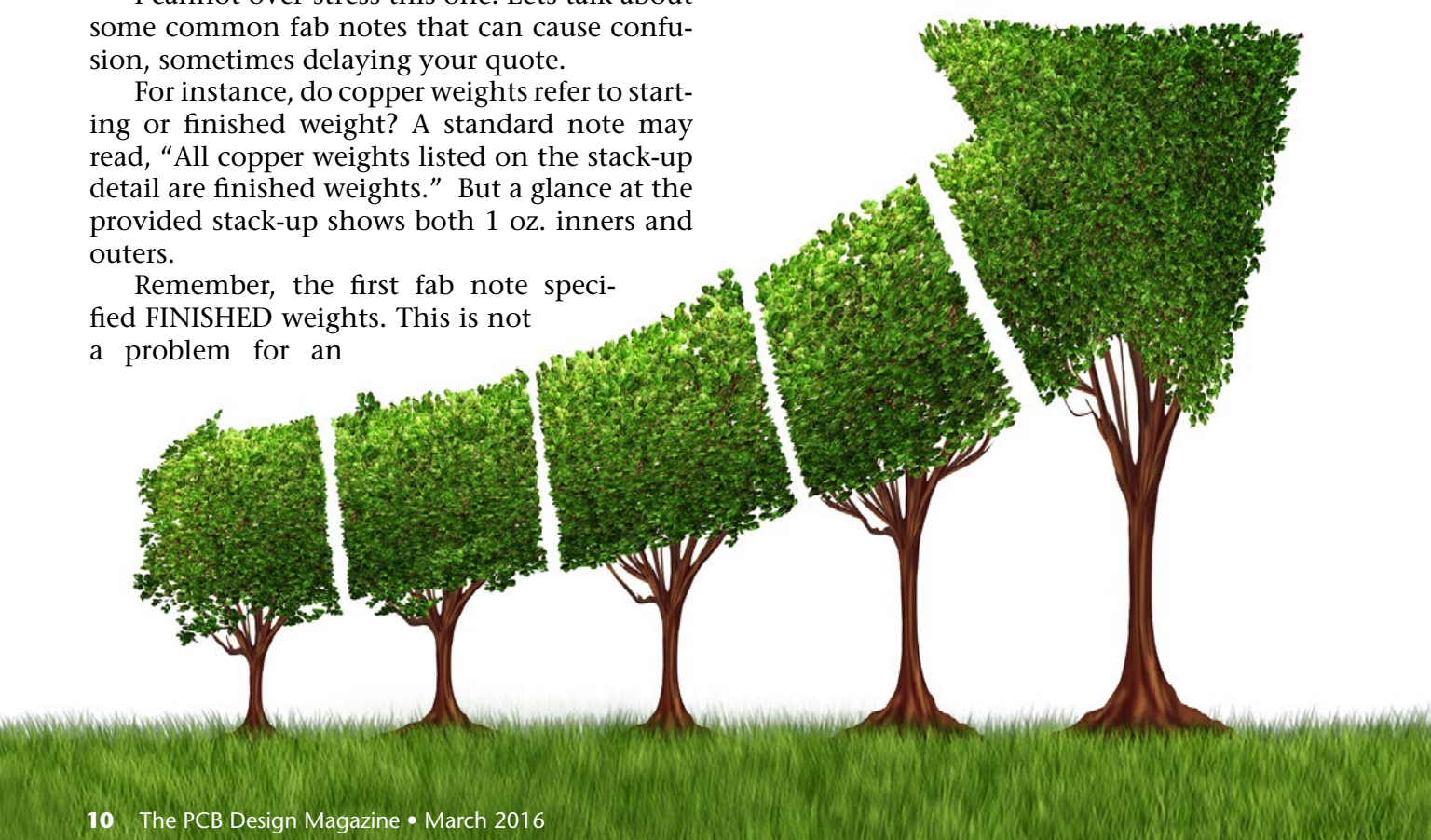
10. Accurate Fab Notes

I cannot over-stress this one. Lets talk about some common fab notes that can cause confusion, sometimes delaying your quote.

For instance, do copper weights refer to starting or finished weight? A standard note may read, "All copper weights listed on the stack-up detail are finished weights." But a glance at the provided stack-up shows both 1 oz. inners and outers.

Remember, the first fab note specified FINISHED weights. This is not a problem for an internal layer, as they are "print and etch" for the most part. Their desired copper features are protected by the photosensitive resist and are simply printed, developed (to remove the resist not hardened by the light source), etched (to remove the unwanted metal) and resist stripped to remove the resist covering your desired copper features. So a 1 oz. callout for an inner layer is not at all uncommon.

The 1 oz. finish for the outer layers, however, is a bit unusual, given the fact that IPC recommends a minimum of 8/10 of a mil of plated copper on the surface and in the barrel of the hole for continuity. So starting on .5 oz. or even .25 oz. copper foils would mean we would have to plate less than what IPC recommends to finish at 1 oz.



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Worse yet, there may be impedance calculations that the customer has based on the 1 oz. finish for outer layers. Increasing the finished copper weight may mean a REDUCTION in your impedance lines. If you have already taken them down to .003" for instance, this may be a problem for the manufacturer.

This clarification about what is needed for desired copper can take additional time at the quote process. I am happy to say we are seeing more and more customers, both old and new, embracing this and creating non-conflicting manufacturing notes that allow for a 1 oz. additional plate.

Now, we see notes that read, "1 oz. inner layers, .5 oz starting copper for outers layers (1.5 oz. finished after plate)." That is a good example of a clear drawing note that does not require additional clarification or send the fabricator down the wrong road for any external impedance calculations.

> "It should also be an obvious point that your notes must reflect the data."

It should also be an obvious point that your notes must reflect the data. If you state "IPC netlist compare required," be sure you include the netlist. Likewise, if you have a specific region for placement of a manufacturer logo or date code based on a flag note, make sure that flag note exists.

Remember, a good review of the fab notes for their accuracy and validity prior to release is always a good thing!

9. Beware of Conversion Errors

Whether it is a conversion error due to format issues or units of measurement rounding, be aware that additional conversion questions can arise at the quote or pre-quote stage.

Example: Lets say your drawing specifies .0055" traces on layers 3 and 6 to be 50 ohms +/-10%.

This is a nice, round, inch unit measurement. Now, let's say your CAD system is metric and it generates a trace width of .005496. Even this slight mismatch can generate questions that take additional time for clarification. In addition, if you have a number of trace widths that are very close, this rounding error can be misinterpreted easily.

Additionally, simply specifying specific Impedance types by either their name or their net names will not always work. Many manufacturers do not have the ability to query a net name for its location to validate impedances, and the same goes for specifying by their type, such as DDR2, SATA, etc. Not all fabricators are familiar with device names. Which leads me to No. 8…

8. Don't Make Assumptions about Controlled Impedances

When running simulations for the purpose of signal integrity, try to be within +/-10% . Yes, I know this is a tough one.

As a PCB designer, your goal is to simulate impedance to within 10% of your goal. The fabricator should be able to take it the rest of the way. How is this done? Well, typically you will get your marching orders from the engineer who tells you what familiy of materials is necessary for the product. If you simply go online and check material PDFs for the purpose of establishing impedances, be aware of at least two things.

First, look at the dielectric that the dielectric constant is based on. Many material PDFs are based on .014" or even .028" core, so if your impedance lines are .005" or less, you won't be using these dielectrics. The thicker dielectrics also have higher Dk values, which may create an impedance issue.

Let me give you an example: Let's say you have done initial calculation to determine trace widths/spaces based on one of these higher Dk numbers. But in reality, the DK of the dielectric required to meet your impedance with your specified line size is vastly lower, which means an ancrease in trace widths.

If your design is .1 mm (.00393") traces and spaces, the fabricator has NO ROOM to increase

traces to meet impedances, and he therefore has to look at altering dielectric. To add insult to injury, should you have a higher copper weight for the inner layers, it may not be an option to reduce dielectric at all!

Our recommendation is to consult your chosen fabricator prior to trace layout for any tight impedances (traces .004" and less) to ensure they can meet your desired impedance.

Next, consider the speed. If the literature is showing 4.5Dk at 1Mhz and you know this product will be running at higher speeds, such as 5, 10 or even 20 Ghz, understand the Dk will be driving WAY down. You may be looking at something closer to 3.8 Dk at 5Ghz. Again, the mismatch will affect the impedance.

7. Panelization Requirements

If you know where your board will be assembled and they have specific panel requirements for tab placement, tooling hole size and placement, fiducial size and placement, additional panel text or targets you or they may provide a sub-panel drawing to the fabricator. If you do not, and it is acceptable for your chosen fabricator to sub-panelize a given part for you, understand this: While fabricators are generally very good at assosciating breakaway rails with standard .125" tooling holes and .040"-.060" fiducials for auto-insertion devices, should there be a part overhang concern or tab placement concern, it should be communicated to the fabricator at the time of quote. No one likes to redo a panelization after "check plots" have been sent by a fabricator; it takes additional time and additional cost to be "re-CAMmed" to add or modify sub panel features.

So if you do have specific locations where tabs cannot be placed based on feature proximity or edge plate concerns or specific fiducial sizes based on your assemblers preferance, be sure to communicate this with your chosen fabricator at the time of quote.

6. Specifying Filled Vias

Many of today's products require via fill with either epoxy, silver epoxy, copper epoxy or sometimes even solid plated copper fill.

It used to be that if you needed the vias in the region of a BGA exposed on one side of the board and covered on the other, at 1 mm and .8 mm pitch, the vias could be plugged with soldermask in lieu of epoxy fill without too much issue.

But today with .5 mm and .4 mm pitch devices, the same vias now need to be either epoxy-filled or conductive epoxy-filled depending on whether or not the vias were being used in any thermal management capacity.

Much like with the impedance statement earlier, you may not want to simply specify the location of filled vias by their component names. Make them a unique size. This way you can specify "All .xxx holes to be epoxy-filled and planarized." Or if you are using that same via size where you DO NOT need epoxy fill, create a separate drill file containing only those vioas to be filled. This eliminates guesswork on the side of the fabricator, again speeding things up, minimizing costly revisions and cutting cost.

5. Let's Talk Tolerances

What are typical drill tolerances? For most fabricators here in the US that use inch measurements for tolerances, we typically say +/-.003" for plated holes and slots and +/-.002" for non-plated holes and slots. Are there situations where these would not be applicable but still possible at a fab level?

Yes. Let me give you an example.

Let's say the plated holes in question are to be used for a "press-fit" device and the literature says you need +/-.002", this does not fall into the +/-.003" that is standard, but is still fairly common in the industry and IS possible at the fab level.

Or let's say the holes are vias. As true vias (not part of a plug-in component), they can be specified as +.003" minus the enire hole size. This is particularly useful if space is limited and tells the fabricator you do not care if they are smaller, as long as they provide good continuity.

4. Avoid Multiple Changes

Whether for a quote or a review, try to avoid multiple changes. If you have decided on a given material family, attempt to stick to a material within that family. If the end-user has not yet decided whether or not a given impedance structure will be co-planar, for example, or even

what thresholds they desire and where they will reside within the stack, soliciting a quote from a fabricator prematurely may make the quote invalid. Consult with your assembler for feedback on any panelization aspects to avoid having to reCAM a panel to add or modify based on assy needs. Lastly, do a thourough product review prior to releasing the fab data to avoid lost time due to incomplete or conflicting notes.

3. IPC Netlists, Their Function, and Typical Net-Compare errors

What is the purpose of the netlist compare? This method is used to compare your design info against your exported Gerber/image data. This is done prior to any fabrication edits.

Required by Class 3 6012, an IPC netlist contains your design info. You may have heard me say this before, but I have been asked by so many of our customers to CREATE an IPC netlist for a class 3 6012 job if they cannot provide one.

This defeats the purpose of the net compare in the first place. Because the idea is to check the customer's design against the customer's exported data, creating a netlist from that data would never catch an actual design-to-export data mismatch.

What are some things you can check for to minimize time lost for IPC netlist issues?

A. AGND to DGND shorts. You may have an analog ground to digital ground short built into the design. You will want to specify that it is a known or expected short, or you may receive a phone call from your fabricator.

B. Castellated holes (plated half holes at a part edge) practically scream that they will make a connection to a metal grounding post sometime later in life. They come up as "broken" nets frequently when running an IPC netlist compare. They show up as broken only because at the time of bare board fabrication, they dis not make connection to the posts.

C. Surface mounts defined as net points, Likewise, sometimes when a surface mount is defined as a netpoint, we can also come up with erroneous broken or open nets. Again, the netlist may think they are to be connected, but they are only connected after assembly.

2. Check Your Edges

For scored parts, do not pour metal any closer to the part edge than .015" for an .062" thick part and at least .009" for an .031" thick part.

1. Get Accurate, Timely Quotes

How do I make sure I get an accurate quote? It's easy. Don't leave anything out. Don't leave anything open for interpretation.

Don't provide a preliminary drawing that you KNOW will change. If the prelim drawing indicates you will have 1,000 vias of a specific size and the final data comes in as 10,000 vias, your price will change.

If you have negotiated impedances and a stack-up over time and the data comes in changed, more time will be involved in revalidating the impedances. Time = money.

If the new board is a revision of an older board and only some constraints have changed, make sure the fabricator knows this so he does not reinvent the wheel for some things they have already covered from a previous rev. This could take additional time and delay the quote.

And of course, if you do everything listed in this article, you should end up with accurate, timely quotes.

As always, I appreciate your time. If you have any comments or feedback I would love to hear from you. **PCBDESIGN**

Mark Thompson is in engineering support at Prototron Circuits. To read past columns, or to contact Thompson, click here, or phone 425-823-7000, ext. 239.

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Design Strategies for Success—and Profit

by Gary Griffin
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In today's economic environment, making money on a project is getting more and more challenging. Those years when businesses like mine were practically printing money are long gone.

The Good Ol' Days

If you are under 30 years old, you probably do not have this point of reference; it's been one downturn after another for your entire adult life. But for us older folks, times were really good back then. So, what happened?

You happened, as well as a million others like you, or so it seems. In other words, the market is a little cramped now and much more competitive, which dilutes our profit per project. And if you're old school and have not grown into the here and now, you will always feel the profit pinch.

There was a time when PCB designers could name their price and people would pay it, primarily because their PCB design choices were limited. This is not true anymore. Now, you can't throw a rock without hitting a PCB designer, or at least someone who thinks he knows how to design a board.

This is the competition we all face, and it's the reason it is so difficult to justify our prices. We're competing with every designer sitting in a home office in his shorts, drinking coffee and eating toaster pastries, while undercutting us by as much as 50%. Customers are driven by their own profit goals, and a low-ball quote is attractive when they really don't understand the real cost of using cut-rate resources.

So how do we make more money while saving money for our customers? After all, the only reason to be in business is to make money, and that is a two-way street. Vendor and customer relationships go both ways. We provide a service that has value so they can provide a product that has value.

OEMs use companies like mine because they don't want the overhead of supporting an in-house design engineering department. That was not the case 15 years ago. Seemed like everyone wanted to capture the engineering in-house. However, when business slowed down, this first thing many OEMs did was push us out the door because they did not know the value of the work we did.

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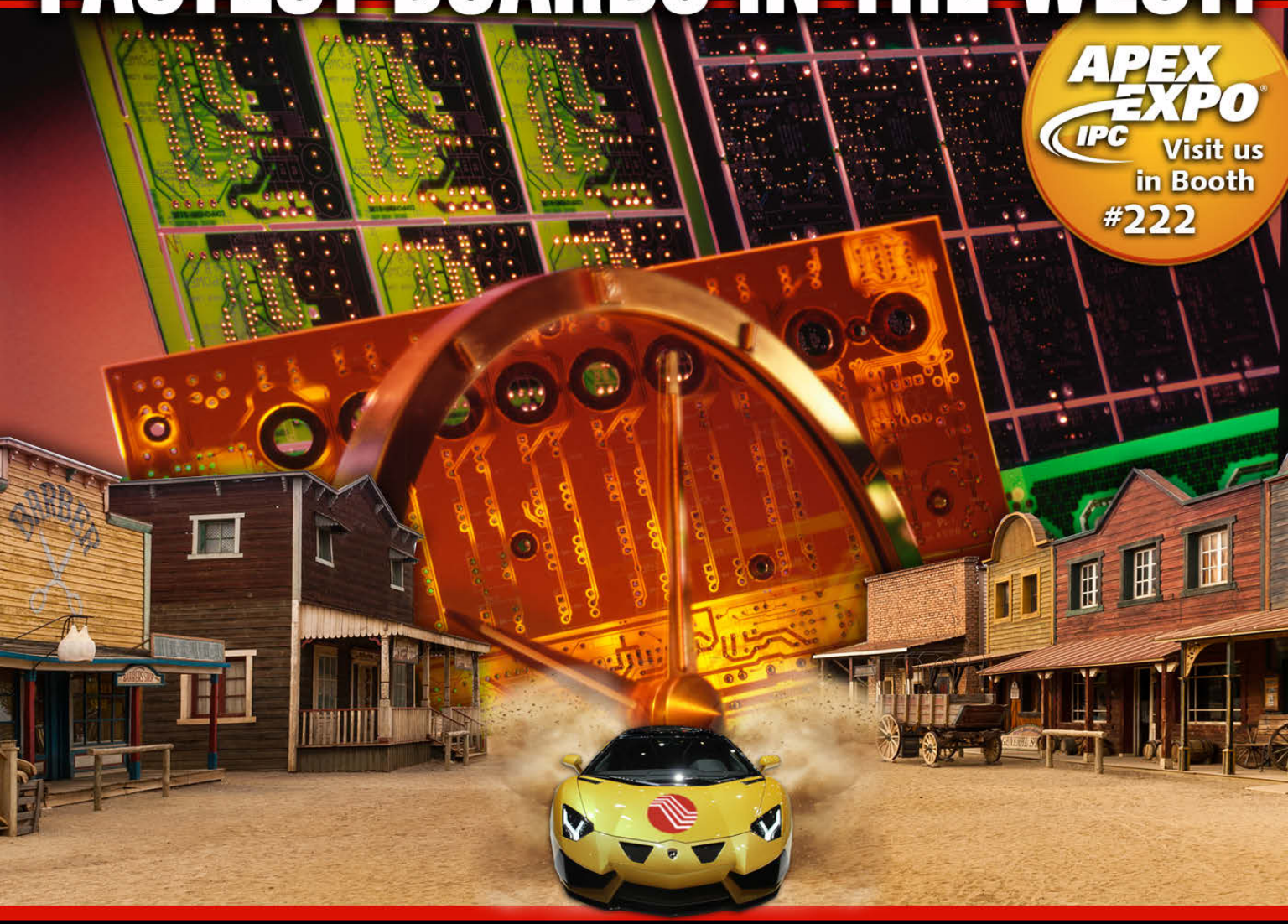

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Today: Focus on Project Management

Fast-forward to 2016. Customers are looking for resources who have both the skills and knowledge to help them get their products developed. What designers have to do is demonstrate the value of our services and capabilities. We don't have to do everything alone; it is good to partner with technologists who have a different skill set than yours, and it's an asset to have a full suite of engineering resources at your disposal. I've found that acknowledging that you may not know the answer to a certain question, but you have access to someone who does, is usually well received and respected. Whether you want to disclose that is your decision, of course.

"I've found that acknowledging that you may not know the answer to a certain question, but you have access to someone who does, is usually well received and respected. Whether you want to disclose that is your decision, of course."

Customers no longer want to manage their PCB design projects anymore. They would rather throw the project over the wall and have us manage it for them. This is where we show our value, and this is worth a lot more to them than just doing a physical PCB layout.

You can see the look of relief on the customer's face when you demonstrate the willingness to manage their project, along with the skills to do so. Customers will keep coming back and more importantly, they will spread the word about your company. This particular knife also cuts the other way; if you screw up their project, the word will spread even faster.

In order for us to manage a project that has many facets, first we need to understand what the customer wants.

Simply put:

1. What is the input?
2. What is the output?
3. What does the customer plan on doing with it?
4. What do they plan to use to generate the inputs?
5. What do they intend to do with the outputs?

These questions open up the conversation and will organically lead you down the path of what they truly want and this will force you to start asking some questions on your own, like the following:

1. Do I know how to do this project?
2. Do I know someone who knows how to do this if I don't?
3. Do I have time?
4. How much time is this going to take?
5. How will this impact my current projects?
6. If I need to get someone else involved, how much are they going to charge me?

Once all these questions are answered, you will be in a good position to create the estimate and a timeline for your customer's project. An important note: Stick to the timeline.

It goes without saying, but I will mention it anyway, when the project starts to change from the original statement of work, there is always the opportunity to renegotiate costs and pricing. Don't be afraid to do this. It is necessary that the client understand that there is value to your time and services and changes are costly in both.

When You Become a Design Customer

Next, I want to discuss the customer's point of view and how you should be addressing the choice of their design bureau. We all may wind up needing to outsource design work from time to time.

Let's face it, choosing the right design engineering company is hard. It is like a blind date. I don't know you and you don't know me. Suspicion and distrust are normal, especially when you will be asked to fork over

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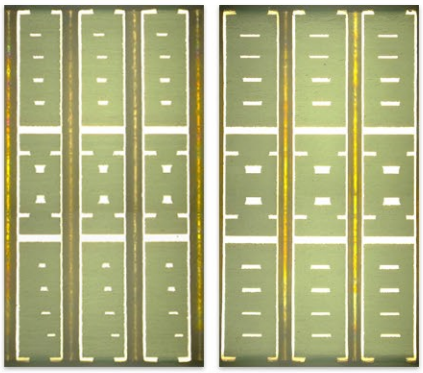

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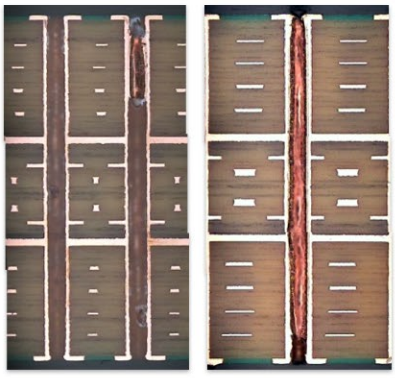

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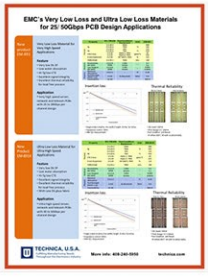

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some of your hard-earned cash to get the project done.

So, one would ask, how in the world do I go about choosing the right company? It really comes down to an interview. Ask the questions that are important to you and to your project, and if you are getting the runaround, then run away as fast as possible.

> **"Ask the questions that are important to you and to your project, and if you are getting the runaround, then run away as fast as possible."**

When you are interviewing a potential partner in your project, you need to understand how that company does business. Keep the following questions in mind when you're considering working with a design bureau:

1. Do they have and maintain the most current revs of the CAD and CAE software suites?
2. Are they willing to spend time with you and outline the process and how it works?
3. Do they have the ability to start and finish your project for you?
   a. Do the research.
   b. Create the schematic.
   c. Create the PCB layout.
   d. Completing a prototype assembly.
   e. Developing the firmware.
   f. Perform debug and test.
   g. Provide a technical guide and test report.
4. Are they able to integrate your ideas into a final product that you can go and sell to the world?
5. Are they willing to protect your ideas and project with a written guarantee and more importantly a legal document?

This process of choosing an engineering partner is a two-way street. The company representative will or at least should be asking you questions and setting expectations on potential costs and potential timelines. They need to understand your ideas, the inputs, the outputs, what you want it to do with them.

Cost is an area of concern. If a company low-balls you on the quote to get your business, caveat emptor, or "let the buyer beware." They ARE going to hit you with additional costs later on, and that is not a good situation at all.

As the customer, you need to understand that if you make changes to the statement of work that was originally agreed upon, cost changes should be expected. After all, their time is worth something too, and this is how they make a living.

Since this may be a long-term relationship, it is important to get to know each other. Talk about the project's goals. Talk about money. Yes, have the money talk. They need to know if you can pay them and HOW you will do so. You need to know what you are going to get for your cash as well as HOW and WHEN.

When they send you the estimate, does it outline the timeline and milestones? It should, and if it doesn't, ask them to provide them for you. If the company cannot give you a timeline and milestones, go somewhere else and start the process all over again.

Finally, a contract is important, because this is your money, your project. You own it, not the design engineering company. Any company should be willing to sign a contract that spells that out.

It's true; the "good ol' days" of electronics design are long gone. But with a little planning, PCB designers can still succeed, and make a good profit too. **PCBDESIGN**

Gary Griffin is co-founder of Fast Interconnect, a product engineering company based in Casa Grande, Arizona.

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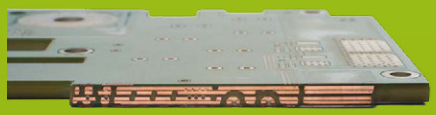

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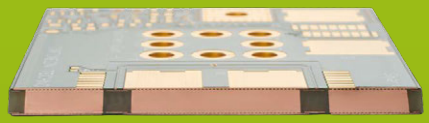

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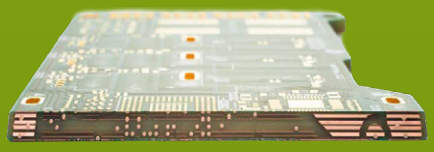

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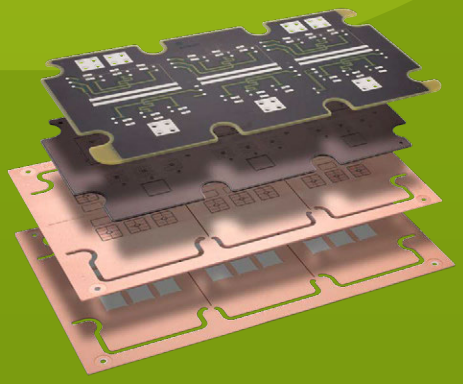

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The Need for Speed: Strategies for Design Efficiency

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD AUSTRALIA

Years of experience with one EDA tool obviously develops efficiency, whether the tool be high-end feature-packed or basic entry-level. And one becomes accustomed to the intricacies of all the good and bad features of their PCB design tool. However, there comes a time, with the fast development pace of technology, that one should really consider a change for the better to incorporate the latest methodologies. This month, I will look at productivity issues that impede the PCB design process.

The choice of PCB design tools, until now, has been limited to either high-end, enterprise-level solutions that are expensive and have the added cost of an extended learning curve and setup time, or entry-level desktop solutions that are fast to pick up but limited in capability and error-prone. Mentor Graphics' new PADS Professional has addressed this by providing the best of both solutions. Based on proven Xpedition technology, PADS Professional focuses on ease of adoption, ease of use and affordability but is still packed with all the features today's designers need for the most complex designs.

Typically, a high-speed computer-based design takes two or three iterations to develop a working product. However, these days the product life cycle is very short and therefore time-to-market is of the essence. One board iteration can be expensive, depending on your overheads.

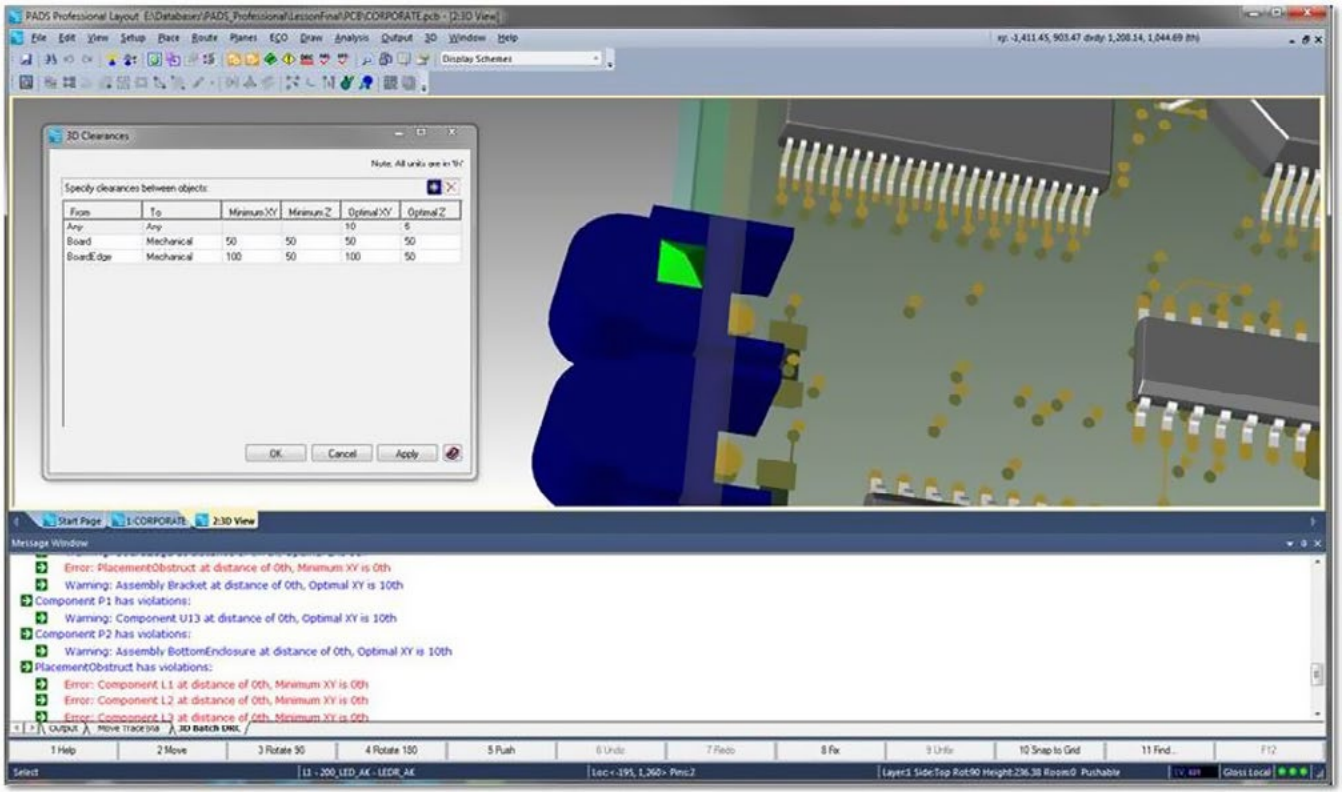

Figure 1: 3D interference validation.

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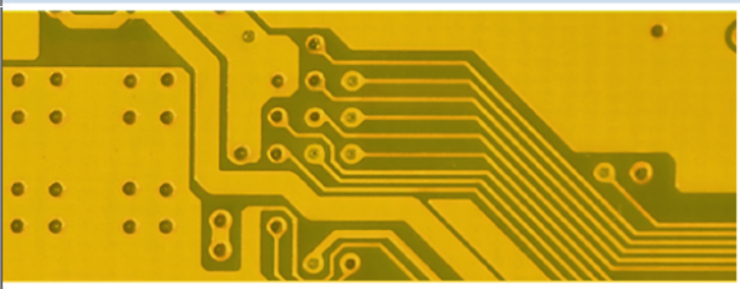

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We should not only consider the engineering time but also the cost of delaying the products market launch. This missed opportunity could cost your company hundreds of thousands of dollars, if not the total loss of market share.

In a previous column, Introduction to Board-Level Simulation and the PCB Design Process, I mentioned that the cost of development is dramatically reduced if simulation is employed during the design cycle. The design changes that occur early in the design process are less expensive compared to those that take place after it is introduced into full-scale production. The cost of the change increases with development time.

Fundamentally, the design changes can be classified into pre-production and post-production modifications. The pre-production changes can happen in the conceptual, design, prototype, or the testing stage. The post-production stage change will happen almost immediately when the product is introduced into production or worse still, be recognized only when the product reaches the market. The later the stage, the more expensive the issue is to fix. The advantage of virtual prototyping is that it identifies issues early in the design process so they can be rectified before they become a major problem.

For years, entry-level tools allowed us to quickly design and build a prototype, some of these based on chip vendor reference designs. Unfortunately, those days are long gone and development teams are finding that they need to employ analysis tools to verify their design before release. One cannot rely on reference designs to actually work in the operating environment. These designs are generally built by R&D teams who have high academic qualifications but little appreciation of design for reliability or manufacturability—the real world.

This in-circuit design, find-and-fix methodology is imperative in today's design environment, where multiple fast rise-time signals propagate at faster and faster speeds with the implementation of each new technology. We no

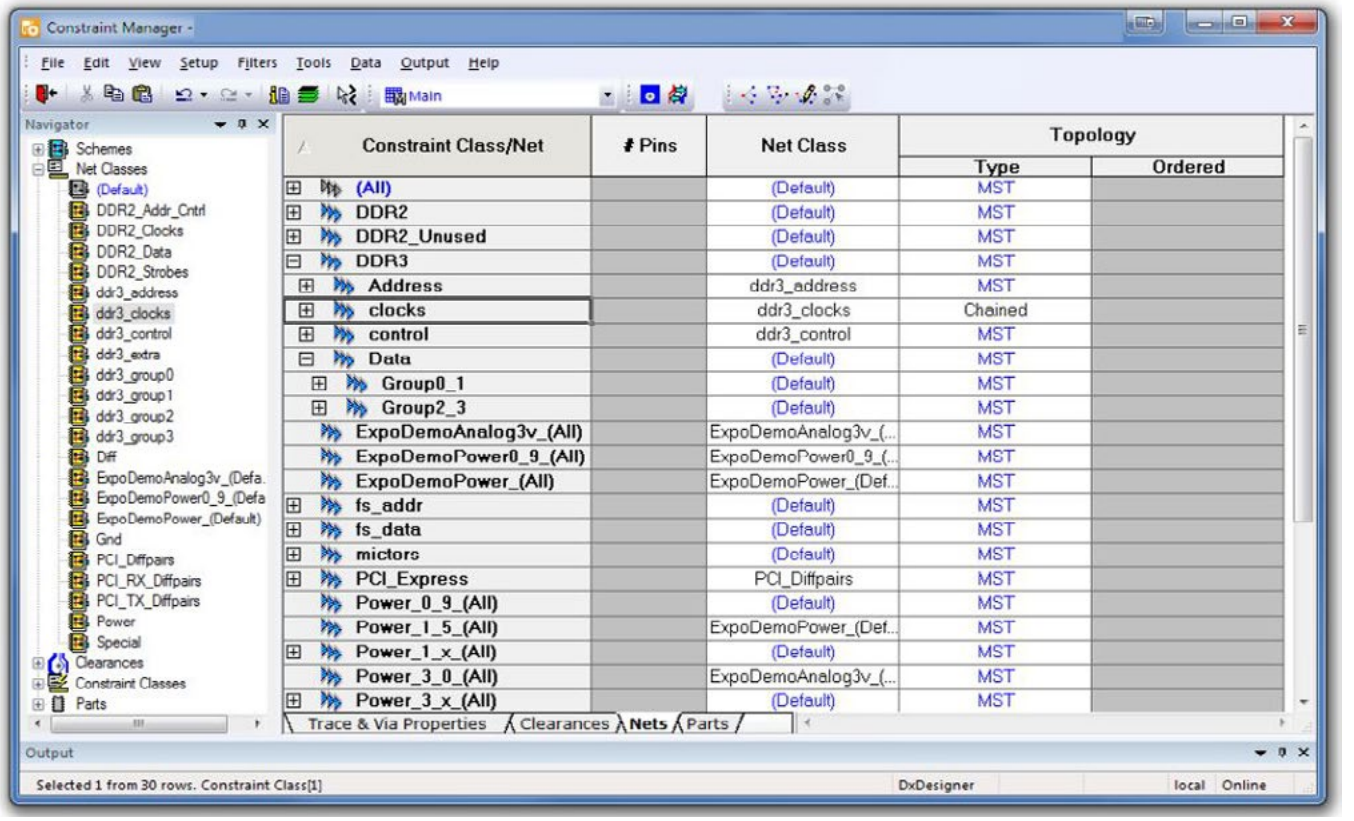

Figure 2: Constraints planning at the schematic level.

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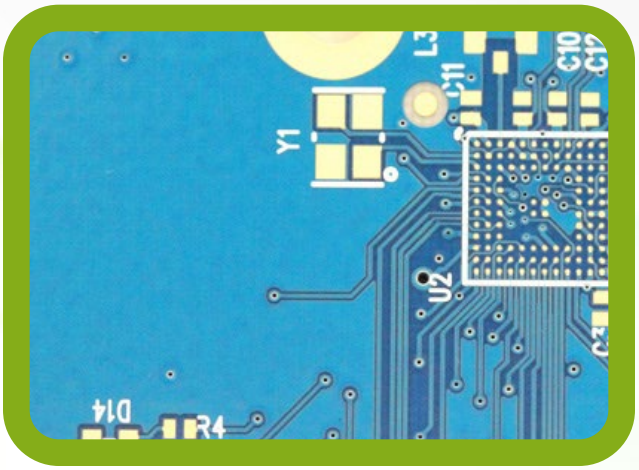

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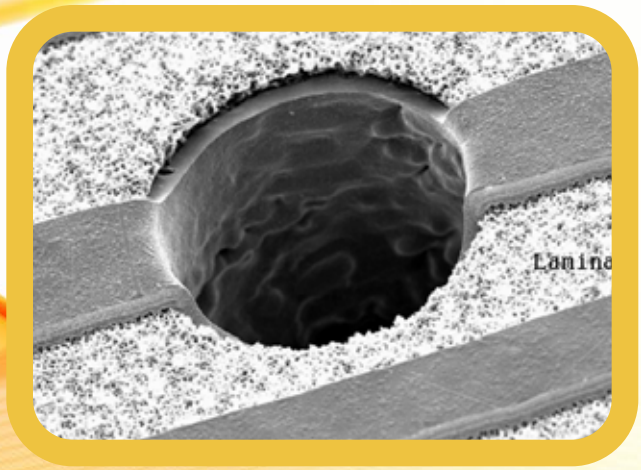

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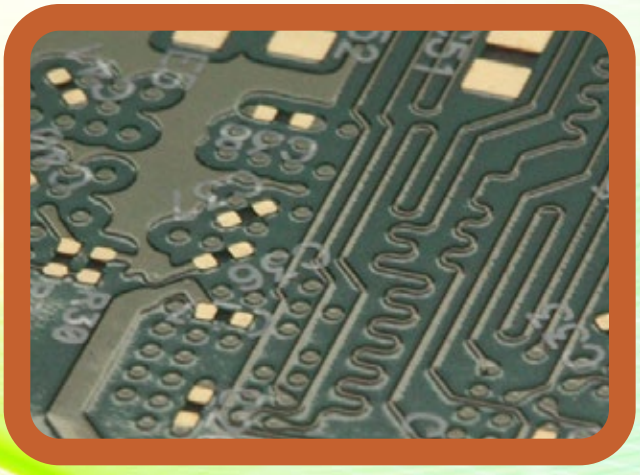

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longer have the luxury of building a prototype, testing and then revising the approach where necessary. Virtual prototyping, including signal and power integrity, thermal analysis, DFM and 3D interference validation, impart fewer design spins and are essential for design efficiency. 3D interference validation is shown in Figure 1. 3D clearances can be setup then the 3D clearance checking displays violations and automatically zooms in on the selected violation.

Entry-level tools tend to rely on the skills of the engineer and PCB designer to detect possible issues as they arise during the design process. However, these days a more constraint-driven, correct-by-construction approach is required for complex designs. Once the rules are established, they will be followed by downstream tools and validated to conform by the various design rule checkers (DRCs).

Figure 2 illustrates typical constraints planning and definition for a high-speed DDR2 & 3 design. The constraints should be defined at the schematic level and flow through to the layout process. The advantage of this approach is that the engineer can convey his intent, to the PCB designer, without misinterpretation. Alternatively, the independent engineer (the guy who does everything) can manage the constraints, throughout the design process, using the same consistent management tool. Also, the reuse of constraints from a previous proven design not only ensures consistent rules but also minimizes the possibility of errors.

Net classes are used to organize and speed-up the definition of routing constraints for nets with similar properties. For each net class, the layers allowed for routing, the corresponding trace width range for these layers, and the via types allowed can be defined. For differential pairs, a layer-dependent differential pair gap can be defined based on the calculated impedance to ensure uniform impedance across all layers.

Proper grouping and definition of net classes and constraint classes in the early stages of the design process simplifies constraint definition and management significantly. Grouped constraints can increase layout efficiency, reducing design time and, ultimately, lower PCB design costs.

Pre-layout simulation allows the designer to predict and eliminate signal and power integrity, crosstalk and EMC issues early in the design process. This is the most cost-effective way to design a board with fewer iterations, rather than starting with the post-layout simulation. One

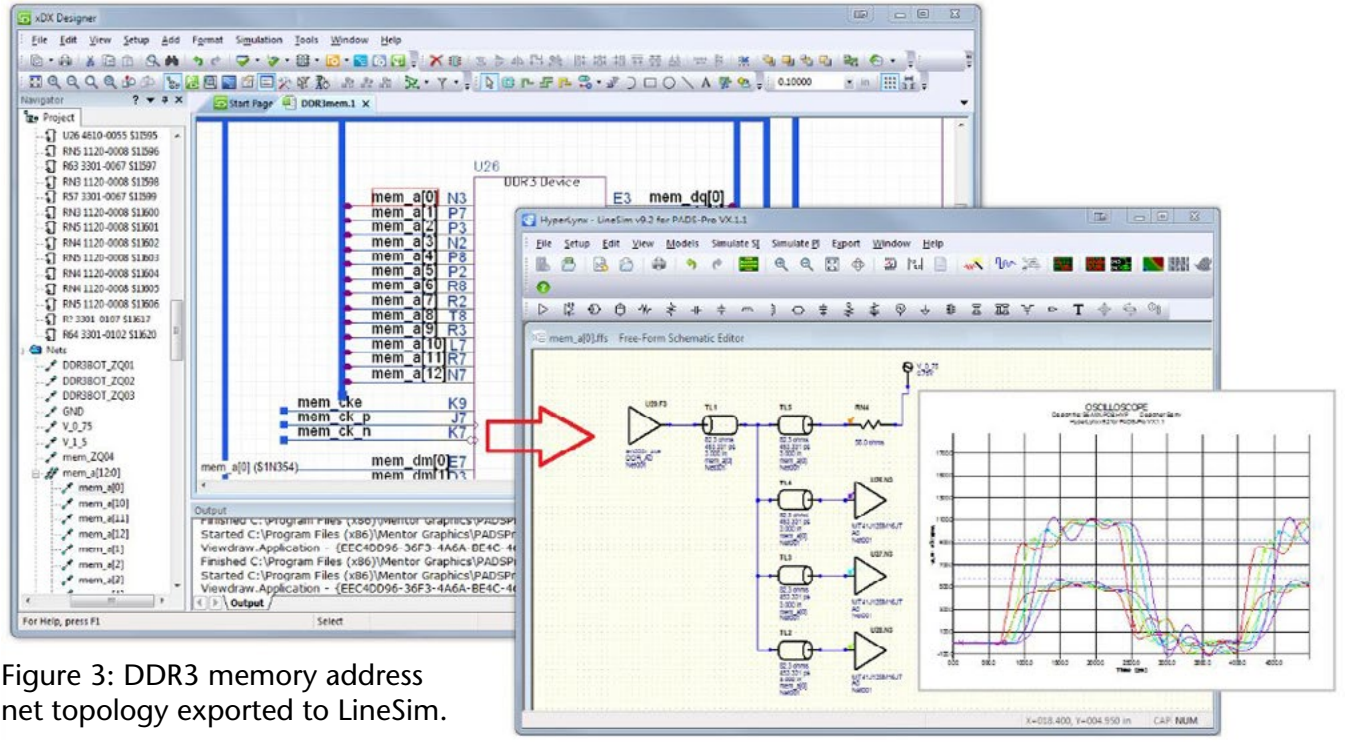


Figure 3: DDR3 memory address net topology exported to LineSim.

can quickly simulate complex interconnect scenarios including ICs, transmission lines, connectors and passive components to identify which scenario is best suited to a particular design.

An integrated correct-by-construction component library also ensures that once a part is defined, the symbol, cell and part mappings will be in sync. This approach eliminates a major cause of design iterations commonly found in netlist driven design paradigms.

Apart from the use of signal and power integrity analysis tools, most designers still rely on eye-balling to pick up many inconsistencies in the layout. HyperLynx DRC, for instance, can verify complex design rules that are not easily simulated, such as EMC constraints. With support for DRCs of such items as traces crossing split planes, reference plane changes, shielding and via checks, one can quickly detect and rectify issues that may later on causes intermittent signal and power integrity issues. The DRCs can also be customized to allow users to create constraints for any check that they may otherwise perform manually eliminating human error.

Today's high-performance processors, with sub-nanosecond switching times, use low DC voltages with high transient currents and high clock frequencies in order to minimize the power consumption and hence heat dissipated. However, fast rise times, low output buffer impedance and the simultaneous switching of busses create high transient currents in the power

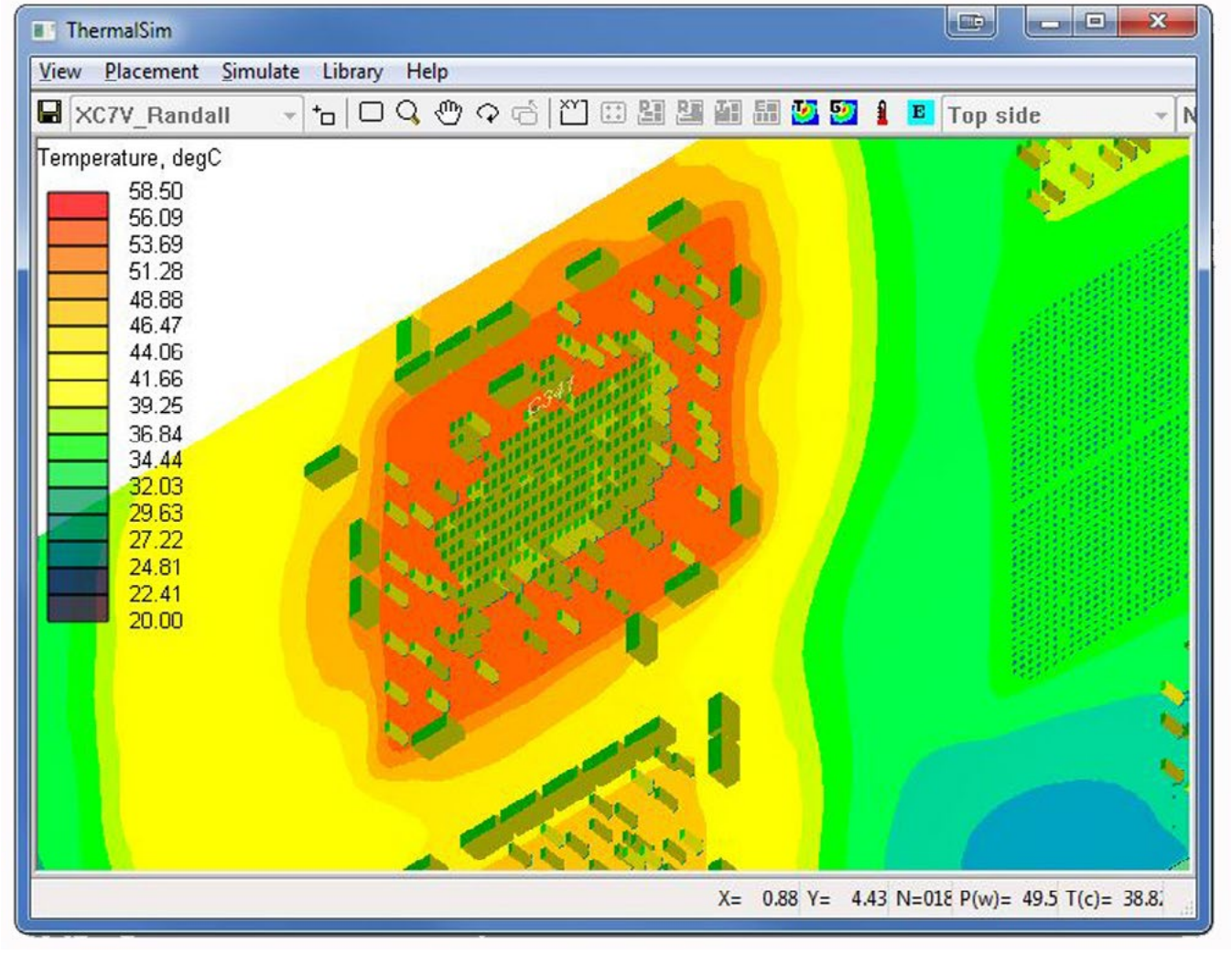


Figure 4: Thermal simulation of hotspots on the bottom of the PCB.

and ground planes. This in turn, degrades the performance and reliability of the product. There is also a high risk of thermal failure in adverse operating environments. Independently from power integrity analysis, thermal analysis can detect hotspots, overheated components and other thermal issues that may degrade the product. Thermal simulation can be run by itself or co-simulated with DC voltage drop. Thermal-only simulation takes into account the heat dissipated from ICs and other components, the environmental air flow and ambient temperature. Thermal/DC drop co-simulation additionally includes the heat produced by current flowing through copper connecting the voltage regulator module (VRM) and DC sink component pin models.

Of course, the use of today's advanced routing technology can provide stunning productivity gains, particularly with the latest high-speed DDR4 memory interfaces requiring your undivided attention to detail. Once set up with constraints defined for all critical signals, routing can be completed and verified in a fraction of the time required using manual techniques.

In conclusion, the use of virtual prototyping including signal and power integrity, thermal analysis, DFM and 3D validation, is now becoming imperative in order to reduce design iterations, meet aggressive schedules and stay ahead of the competition, But, what about the cost? One could choose an enterprise solution that would undoubtedly do the job, or you could consider an affordable bundle of tools that are comparatively priced to desktop solutions, yet provide all the necessary tools required for the most demanding design. Is it time to look at more efficient alternatives?

Points to Remember:

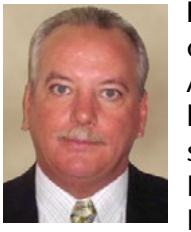
- The choice of PCB design tools, until now, has been limited to high-end, enterprise-level solutions or entry-level desktop solutions.
- A typical a high-speed computer based design takes two or three iterations to develop a working product, costing engineering time and delaying time-to-market.
- The design changes that occur early in the design process are less expensive when compared to those that take place after it is introduced into full scale production.
- Development teams are finding that they need to employ analysis tools to verify their design before release.
- Virtual prototyping, including signal and power integrity, thermal analysis, DFM and 3D interference validation, impart fewer design spins and are essential for design efficiency.
- Entry-level tools tend to rely on the skills of the engineer and PCB designer to detect possible issues during the design process. A more constraint-driven, correct by construction approach is required for complex designs.
- The reuse of constraints, from a previous proven design, not only ensures consistent rules but also minimizes the possibility of errors.
- Net classes are used to organize and speed-up the definition of routing constraints for nets with similar properties.
- Designers still rely on eye-balling to pick up many inconsistencies in the layout. However, DRC tools can verify complex design rules that are not easily simulated, such as EMC constraints.
- Independently from power integrity analysis, thermal analysis can detect hotspots, overheated components and other thermal issues that may degrade the product.
- Today's advanced routing technology can provide stunning productivity gains. **PCBDESIGN**

References

1. Barry Olney Beyond Design columns: Introduction to Board Level Simulation and the PCB Design Process, Design for Profit.

2. Steve Hughes, Mentor Graphics PADS Professional documentation, Why Impose Design Constraints?

3. For information about PADS Professional, click here.



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, click here.

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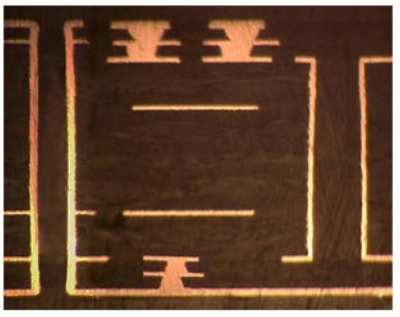

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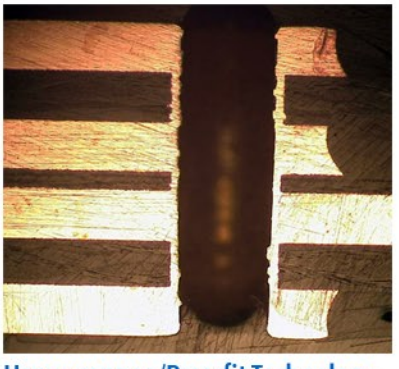

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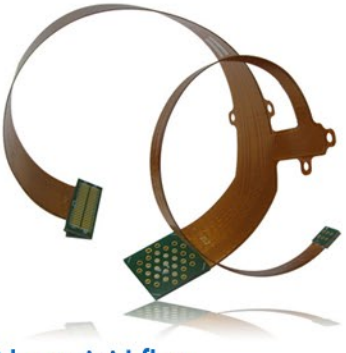

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PCB007 Highlights

Happy's Essential Skills: The Need for Total Quality Control (Six Sigma and Statistical Tools), Part 2

The statistical representation of Six Sigma describes quantitatively how a process is performing. To achieve Six Sigma, a process must not produce more than 3.4 defects per million opportunities. A Six Sigma defect is defined as anything outside of customer specifications.

What a Long, Strange Trip it's Been—and It's a Long Way from Being Over

Harvey Miller has been in the PCB industry for more than 40 years, and he's probably seen it all. I recently sat down with Harvey at a wine bar in Palo Alto to learn more about his history in the industry and where he sees it going forward. Harvey arrived wearing jogging shorts and running shoes. No surprise after what his doctor recently shared with him.

Graphic PLC Receives Training Awards

The awards recognise exceptional training and development in organisations across the South West; celebrating companies that develop their staff through training and have as a result seen exceptional business success.

TTM Technologies Reports Sales Growth in Q4 and FY 2015

"Our solid fourth quarter execution combined with seasonal growth in the cellular phone end market and robust demand in the automotive and aerospace and defense end markets drove our sequential increases in gross margin, operating profit and strong free cash flow generation," said Tom Edman, CEO of TTM.

Conflict Minerals: Negotiations Begin in Europe on Proposed Legislation

Informal negotiations between the EU Council, Commission and Parliament (trialogue) started on the conflict minerals dossier on February 1, 2016. The trialogue is an informal, closed-door process in which the Council and the Parliament try to reach to a compromise on a legislative proposal.

New Year, New Outlook for the Electronics Manufacturing Industry

As an advocate for the electronics manufacturing industry, my job is to educate and encourage policymakers to create a favorable legislative and regulatory environment for advanced manufacturing to grow and succeed. From that perspective, I think we should be proud of the significant progress we made in several areas in 2015.

In Memoriam—Dennis (Denny) J. Cantwell

Long-time IPC member, Dennis (Denny) J. Cantwell, 74, passed away on November 12, 2015. Denny was a very active member of the IPC Flexible Circuits Base Materials Committee until his retirement from Printed Circuits Inc. in 2009.

Robots, Wearables and Implanted Devices in the Age of Bionic Health

If you are an electronics manufacturer and you ask your business bankers where their market research suggests growth will come from, they will almost certainly identify medical electronics as a key growth area.

How North American Fabricators Benefit from Attending HKPCA

Two New Englanders in Shenzhen. It sounds like the title of a play, doesn't it? Headlining the bill is Peter Bigelow of IMI, who explains to me why even small American manufacturers benefit from attending large Chinese shows like the HKPCA. He's joined by fellow New Englander Alex Stepinski of Whelen Engineering, who discusses drill concepts and the transition to zero discharge.

Mr. Laminate Tells All: CEM-3 Reinvents Itself (Again)—or, Atari Game Boards on eBay?

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The Principles of Hybrid Design, Part 1

by Tim Haag
INTERCEPT TECHNOLOGY

The butterflies fluttering around in your gut intensify as you walk down that long hallway to the impromptu department meeting. There have been a lot of rumors, but no one seems to know anything.

You wonder, "Will I even have a job 20 minutes from now?" Then you take your seat for the presentation. But fortunately, the news isn't what you had feared, and instead you find out that your company is merging with Acme Industries. And on top of that, Acme has an urgent need for a new design to be completed, and you've been picked for the job.

So, in front of the VP, your boss, and all your co-workers, this particular hot potato gets handed to you. Congratulations. But as you look through the design data, those annoying butterflies return, because the design requirements are something that you've never seen before. And even though you desperately want to raise your hand when the VP asks if anyone has any questions, you decide to hide your confusion instead. But what you desperately want to ask is; "Just what in the heck is a hybrid design anyway?"

So just what exactly is hybrid design? If the only thing that comes to mind is an image of a car that switches between batteries and gasoline for power, then this column may be just what you are looking for. We are seeing more and more of our customers exploring the world of hybrid design, and we are getting new customers for whom hybrid design is their sole focus. The world of hybrid design is growing and we have lots of hybrid-specific functionality built into our software that helps designers conquer

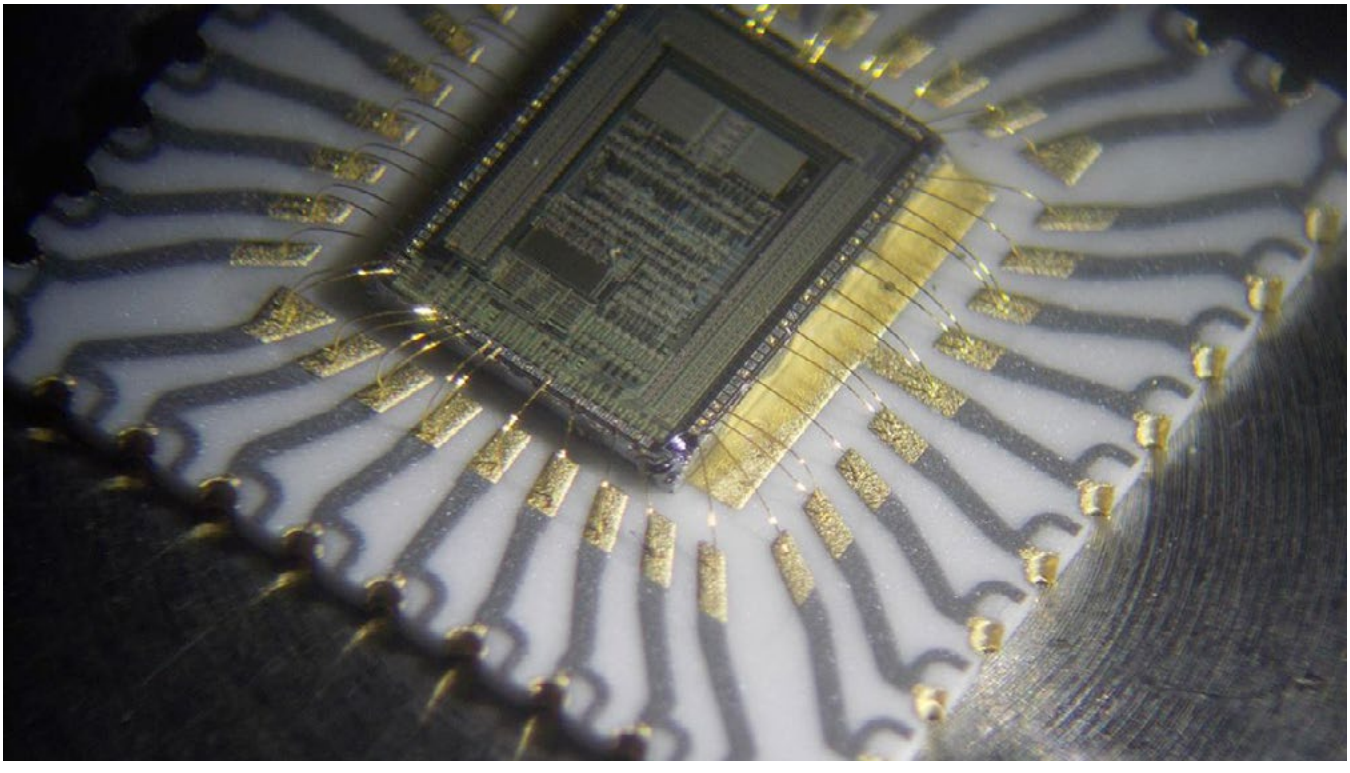

Figure 1: An example of a hybrid design (Image courtesy of Saline Lectronics).

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the unique hybrid design requirements that they are faced with.

And yet many designers out there (and I used to be one of them) have no idea of what is meant when people start talking about hybrid design. It is therefore not uncommon for designers to avoid the subject directly while hoping to pick up little cues and pointers from others indirectly so that they are no longer in the dark. If that description sounds uncomfortably close to where you are today, then read on. My hope is that this three-part series will help you by serving as an introduction into the world of hybrid design.

“And yet many designers out there (and I used to be one of them) have no idea of what is meant when people start talking about hybrid design.”

And before we jump in, I want to give a shout out to my colleague Bernd Pflueger. Bernd has been around the world of hybrid design for a long time now, and he has probably forgotten more about it then I'll ever know. I'm indebted to him for his help and the depth of his knowledge and the valuable insight to hybrid design from the PCB designer's perspective that he brings.

A hybrid design is an alternative to the standard PCB. Components and conductors are attached to or fabricated onto a substrate which can then be completely encapsulated in a protective coating. Hybrids are generally smaller and much more robust than PCBs, making them more adept for extreme environmental conditions. A hybrid design is best if the board is going to be subjected to moisture, excessive vibration, or high temperatures. In other words, if a board is going to be immersed in water, buried in the ground, or shaken to death inside the hot confines of some kind of engine, then a hybrid design would be the better choice over a PCB which may not able to survive under those kinds of conditions.

Hybrid designs will generally have a higher reliability than traditional PCBs. They have fewer solder interconnections, while the other metal interconnections in a hybrid design are more reliable than a solder joint. And with the ability to print ink resistors instead of using standard board-mounted packaged resistors, a hybrid design can realize better precision in their resistors plus save on the cost of stocking and storing these parts for manufacturing. But we are getting ahead of ourselves by talking about ink resistors this early in the game; more about that later.

To start with, let's talk about the basic structure of our hybrid design, which for the purposes of this series we will be referring mostly to an LTCC hybrid design (more on what LTCC means later). As the circuit board designer knows, a standard PCB is a made up of different layers of copper and dielectric material (usually FR-4). The PCB fabrication process etches copper away to form conductors (traces and fills) and all layers are eventually composited together. Therefore the fabrication of a PCB can be considered a subtractive process due to the copper etching. An LTCC hybrid design is the complete opposite. It is built bottom-up from a substrate by printing conductive material for conductors (traces and fills) onto the substrate making its fabrication an additive process.

LTCC stands for low-temperature co-fired ceramics. LTCC designs generally use a ceramic material for their substrate, although depending on the needs of the design, different substrate materials can be used. Stainless steel and titanium are two alternatives for substrates, but these materials are more expensive then ceramic and add another level of complexity to the fabrication process. Each of these would require the application of a thin layer of isolation material to the substrate before adding conductive layers. Therefore, the majority of substrates are ceramic unless the high-temperature environments require the extra cost and weight of stainless steel. Titanium is reserved for those environments where heat flow, weight and sta-

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bility under changing temperature conditions demand the additional increase in cost over stainless steel. Stainless steel and titanium substrates are usually used in HTCC designs, and not LTCC.

The word "co-fired" means that the conductors and the ceramic are all heated (fired) in an oven at the same time. LTCC is fired at a temperature of up to approximately 900°C and when in use these LTCC designs can operate in a design temperature range of up to 225°C. This is one of the main advantages over standard PCB designs which are usually restricted to operating temperature ranges that do not exceed 85°C.

We have also mentioned HTCC hybrid designs, and as you might expect, HTCC stands for high-temperature co-fired ceramics. These designs get fired in ovens up to 1500°C and can support operating temperature ranges of up to 500°C. But these designs are also subjected to higher conductor resistance due to the different type of conductive inks required for the higher temperatures. HTCC designs also have other considerations such as the requirement of different methods of soldering components using different mixtures of metals due to the higher temperature environments. Because of these reasons, HTCC technology is used for hybrid designs only if the advantages it provides are truly required.

There are other hybrid technology types besides LTCC and HTCC in use as well. Greentape technology is a blend of both FR-4 and LTCC technologies for high-precision designs. Greentape stacks several thin ceramic substrates, each printed with only one conductor layer, and presses them into a layered package. This technology lends itself to RF and microwave designs for Bluetooth, radar and transceiver applications. But as we said, for the purposes of this series we will focus primarily on the LTCC hybrid design in our efforts to introduce you to the basics of the hybrid design world.

Unfortunately, just as we are getting started, we have reached the end of Part 1 of this series. We've discussed the basic structure of a hybrid design and talked about their benefits, but there's still so much more. I teased ink resistors with a promise of more information, and that is still to come. And we haven't even touched yet on things like software differences for hybrid design applications, routing conductors, or designing dielectric areas, to mention just a few of the topics that still need to be covered.

Therefore, I hope that next month you will look for Part 2 in this series on basic hybrid design, and we will continue down this path of exploration. See you then. **PCBDESIGN**

Tim Haag is customer support and training manager for Intercept Technology.

Step Towards 'Holy Grail' of Silicon Photonics

A group of researchers from the UK has demonstrated the first practical laser that has been grown directly on a silicon substrate.

It is believed the breakthrough could lead to ultrafast communication between computer chips and electronic systems and therefore transform a wide variety of sectors, from communications and healthcare to energy generation.

The EPSRC-funded UK group, led by Cardiff University and including researchers from UCL and the University of Sheffield, have presented their findings in the journal Nature Photonics.

Silicon is the most widely used material for the fabrication of electronic devices and is used to fabricate semiconductors, which are embedded into nearly every device and piece of technology that we use in our everyday lives, from smartphones and computers to satellite communications and GPS.

Professor Peter Smowton, from the School of Physics and Astronomy, said, "Realising electrically-pumped lasers based on Si substrates is a fundamental step towards silicon photonics. The precise outcomes of such a step are impossible to predict in their entirety, but it will clearly transform computing and the digital economy, revolutionise healthcare through patient monitoring, and provide a step-change in energy efficiency."

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Design and Production: Some Essential Facts

by Phil Kinner
ELECTROLUBE

Well, a month has passed since I last appeared in this column offering advice on the importance of design for manufacture, essentially how to spot those wrinkles that might have an adverse effect on production, and iron them out before you even think about applying conformal coatings to your products. I do hope you found it useful and that it has, at least, started the conversation about the importance of making sound early-stage design decisions.

In this column, I'm going to take a look at some issues you are sure to face—which must be taken into consideration—when you finally apply those conformal coatings. Here are my five essential facts:

Fact 1

Conformal coatings are generally applied in liquid form and are subject to capillary forces and gravity during drying. They are unlikely to yield perfectly straight edges. Often the coating drawing is presented as a rectangular box, and this is likely to cause issues during inspection. Better to specify areas that must be coated and areas that must not be coated. Anything else is a "don't care" area.

Fact 2

The old adage that "if some is good, more is better" doesn't necessarily hold true with conformal coating. Conformal coatings are designed to be applied at the thickness specified

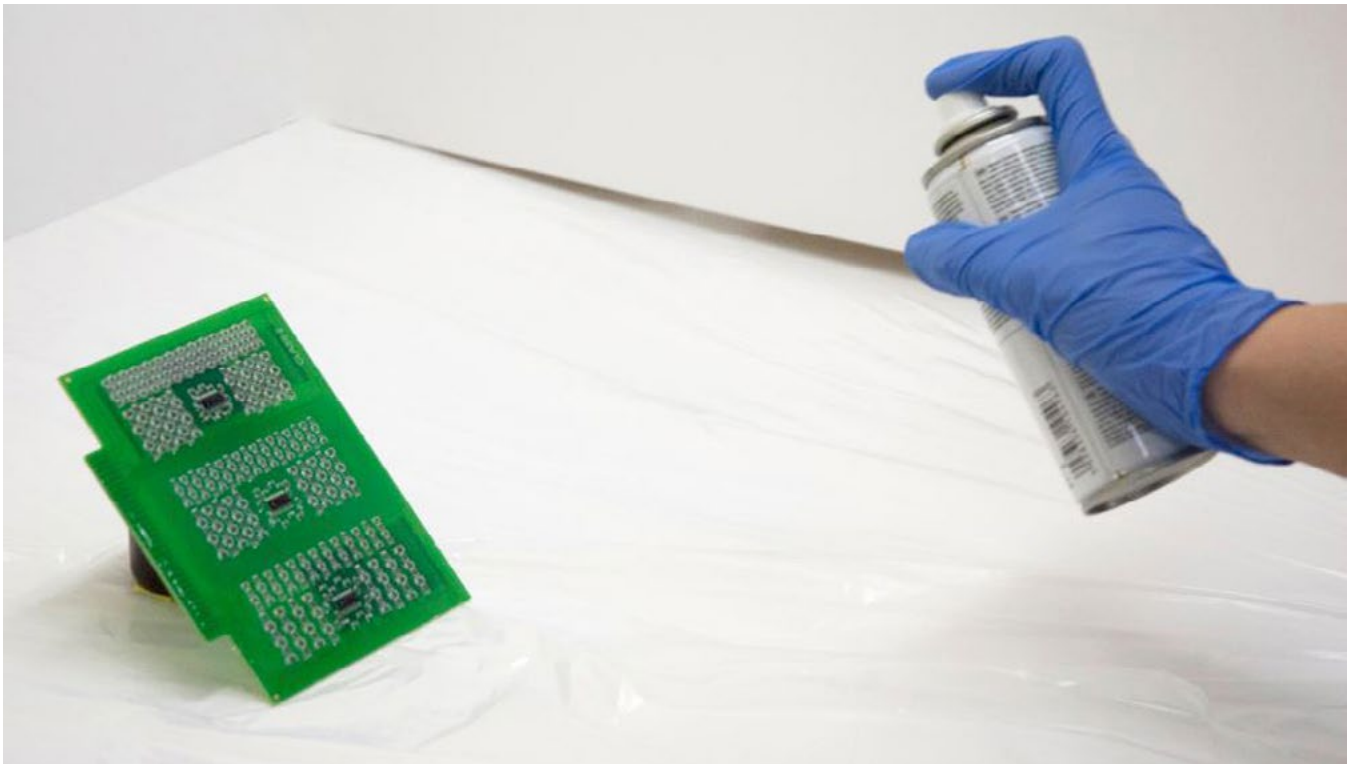

Figure 1.

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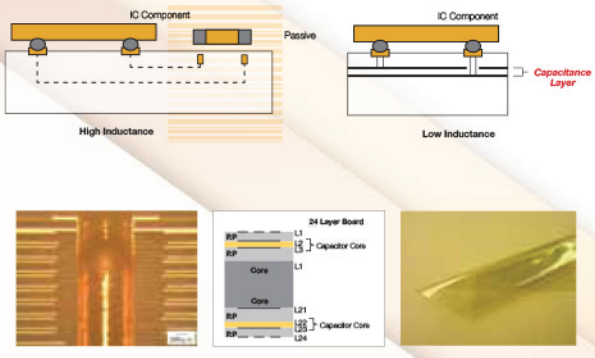

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on the datasheet. Exceeding the recommended thickness is unlikely to provide better protection, but may introduce a range of production issues ranging from dramatically increased cycle time to solvent-entrapment, stress-shrinkage/de-lamination/cracking. If you need a coating on the thick end of the specification, two thin coating applications are better than one thick coating. If you need more thickness than specified, use a coating that is designed to be applied thickly (such as Electrolube's 2K series two-part coatings) or consider a resin product.

Fact 3

Conformal coatings are not under-fill materials. They generally contain no filler and have relatively Z-axis thermal coefficients of expansion. They have been shown to reduce the lifetime of ball grid array (BGA) and quad flat no-lead (QFN) terminations during thermal cycling conditions. If you need to under-fill a device, use one of the many under-fill formulations especially designed for this purpose.

Fact 4

Conformal coatings are available in many generic types. Each has its strengths and weaknesses. Choose the right coating for the intended use and operational environment, rather than one that is used by your subcontractor or qualified on another product line for a different end-use environment. Be sure to test your design to ensure that it is suitably ruggedized for the intended application.

Fact 5

Conformal coatings are not generally waterproof. They will allow moisture to permeate, albeit very slowly, through them. This will eventually react with contaminants from production, such as flux, solder and adhesive residues that could ultimately lead to corrosion beneath the coating. Cleaning is therefore highly recommended prior to the application of conformal coating.

I don't pretend that it's an easy task to choose the correct conformal coating for your product, let alone have certainty that you will have achieved the ultimate goal of protecting your electronics by applying it. It's critical to communicate with your conformal coating supplier, whose technologists can help you address your problems and overcome them at the all-important early design stage.

See you next month. **PCBDESIGN**

Phil Kinner joined Electrolube in May 2014 as technical director for the company's Conformal Coatings Division, which is represented in more than 55 countries across the globe.

Plasma Processing Technique Takes SNS Accelerator to New Energy Highs

A novel technique known as in-situ plasma processing is helping scientists get more neutrons and better data for their experiments at the Spallation Neutron Source at the Department of Energy's Oak Ridge National Laboratory.

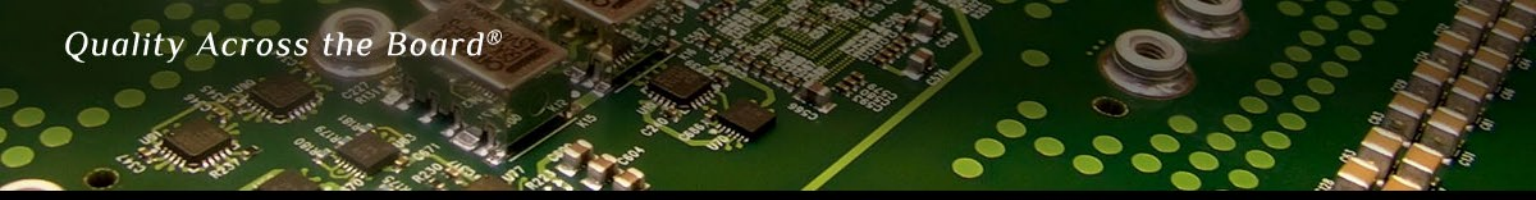
"Plasma cleaning is a well-known technique in electrostatics," said ORNL's Research Accelerator Division Director Kevin Jones, "but it has not been applied before to superconducting cavities, and there are some interesting tricks that you have to develop and apply in order to make it all work."

ORNL staff scientist Marc Doleans and postdoctoral researcher Puneet Tyagi found a better solution.

"Basically, the oxygen gobbles up all the bad atoms off the surface of the niobium, and afterwards everything gets pumped out as a gas," Jones said.

After the trial procedures were complete, the team tested the cryomodule's performance and saw a significant improvement. That gave the go ahead for the team to carry out the in-situ procedure in the accelerator tunnel during the facility's scheduled winter maintenance outage.

The work is already generating a lot of buzz, and it's being viewed very positively, Jones says.



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How Many Vias Does It Take To…?

by Douglas G. Brooks
ULTRACAD

Sounds like the opening words of a bad joke [1]. Well, here's the answer, and it's no joke: One! That's right. No matter how much current you are putting down the trace, all you need is a single via. And a small one, at that.

OK, that last statement might not be true in EVERY single case. But it is true in a LOT more cases than you think. I will explain why in this column.

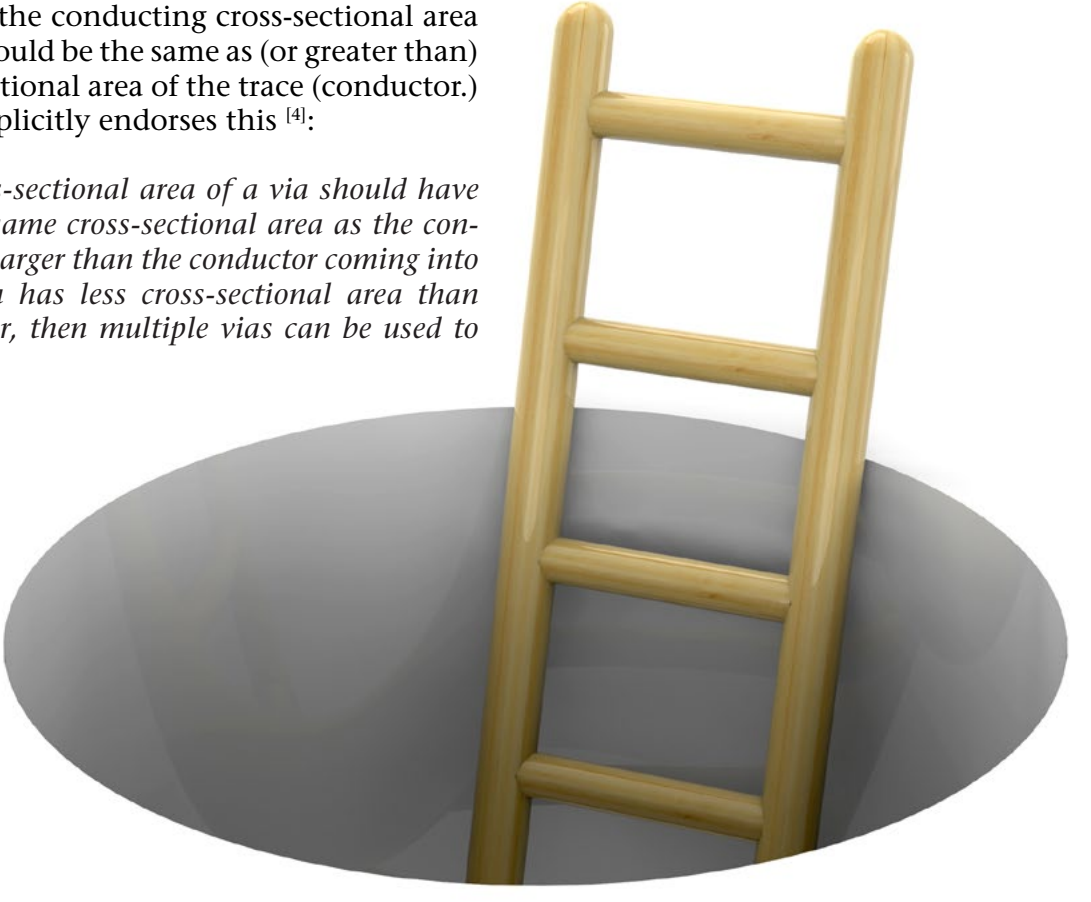
During 2015, I enjoyed a very productive collaboration with Dr. Johannes Adam, from Leimen, Germany. That collaboration resulted in several papers, but one in particular is relevant for this column, "Via Currents and Temperatures" [2]. In that paper, we used a simulation tool, thermal risk management (TRM), developed by Dr. Adam [3], to simulate current flowing through a via and then determine the temperature of the via. The conventional wisdom is that the conducting cross-sectional area of the via should be the same as (or greater than) the cross-sectional area of the trace (conductor.) IPC 2152 explicitly endorses this [4]:

The cross-sectional area of a via should have at least the same cross-sectional area as the conductor or be larger than the conductor coming into it. If the via has less cross-sectional area than the conductor, then multiple vias can be used to maintain the same cross-sectional area as the conductor.

But our results contradicted this; they suggested that the temperature of the via was controlled by the trace, and as long as the trace was sized correctly, any old (single) via was good enough.

If there was ever a result that cried out "show me," this was it.

So I set out on a path to build a test board, test it, and verify the simulation results. This type of study would not have been possible without the cooperation of several people and organizations. In particular, I want to thank my longtime partner Dave Graves (now with Monsoon Solutions in Bellevue, Washington) for helping prepare the final artwork for the test



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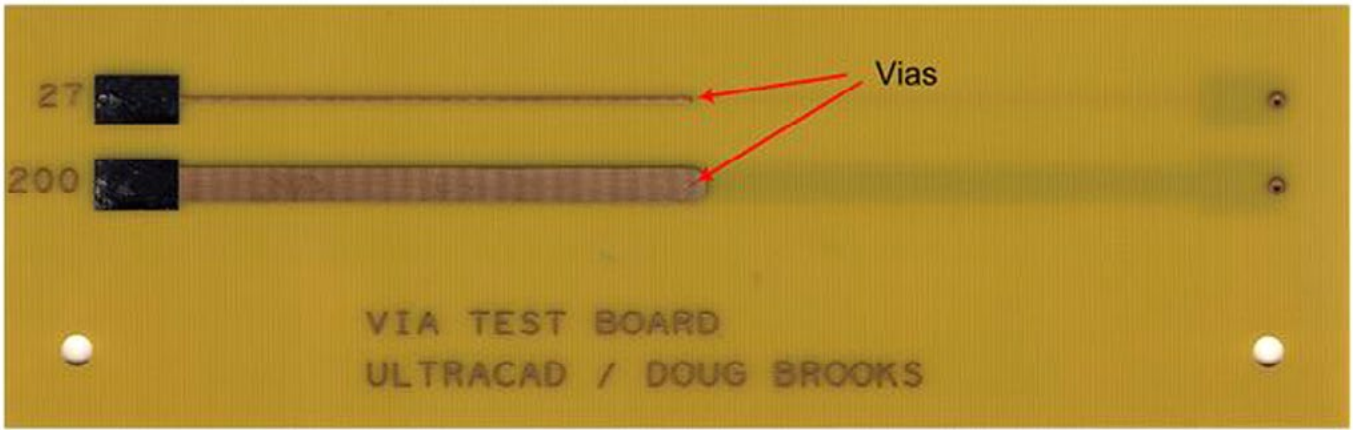

Figure 1: The relevant portion of the via test board.

Measured Results of Via Tests				
Trace width (mils)	Current (A)	Trace Temp. °C	Via Temp. °C	Via T/Trace T
27	6.65	114	109	95.6
200	8.55	40.5	44.5	109.9
Simulation Results of Via Tests				
27	6.65	114.2	108.2	94.7
200	8.55	44.8	48.1	107.4

Table 1: Summary of test results.

board. C-Therm Technologies [5] (Fredericton, New Brunswick) graciously measured the thermal conductivity of the board material to facilitate the simulation. And a special thanks to Prototron Circuits [6] of Redmond, Washington, who provided the test boards and also the microsectioning work and measurements. And my collaborator on trace thermal issues, Johannes Adam, continues to be a great help in evaluating results.

Figure 1 illustrates the relevant portion of the test board. There are two 0.5 oz. test traces, each six inches long, each consisting of two, three-inch segments (top and bottom) connected by a single 10 mil diameter via. The via is plated to approximately one ounce. One test trace is 27 mil wide, providing approximately the same cross-sectional area as the conducting area of the via. The other trace is 200 mil wide. It is important to note that the vias are identical for the two traces.

A controlled current was applied to the traces (8.55 A to the 200 mil trace and 6.65 A to the 27 mil-wide trace) and the temperatures along

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the trace measured with thermocouples. The hottest point on the 27 mil trace was 114°C, measured to the left of the via. The via temperature was 109°C, about 4% COOLER than the trace! The hottest point on the 200 mil trace was 44.5°C, measured at the via. The temperature to the left of the via was about 40.5°C (found by experiment to be the maximum temperature of the trace under similar conditions without a via). It is important to note that:

A 6.6 Amp current through the 27 mil-wide trace results in a via temperature of 109°C, while a higher current of 8.6 Amps in a larger (200 mil) trace results in a much lower via temperature of only 44.5°C. This confirms that it is the trace that is controlling the via temperature.

We wanted to run a simulation of the actual test board, since it had different dimensions than those hypothesized in our first paper. The simulation technique is described in previous papers on the UltraCAD website. The simulation results are provided, and compared to the empirical test results, in Table 1. As can be seen, the simulation results compare quite favorably to the measured results. The thermal profiles for the two simulations are provided in Figure 2.

Two questions come to mind:

Why doesn't the via heat up more?

The answer is that the thermal conductivity between the via and the copper trace is so good that the via can't heat up (much) more than the trace. Any excess heat conducts away from the via into the trace and is then conducted into the board material—the same material that is cooling the trace. So as long as the trace is sized correctly to carry the current, the via can't get much hotter (maybe less than 10% at most) than the board.

Why is the via COOLER than the trace in the 27 mil case?

Since the via and trace conducting areas are the same size, one might expect the via and the trace to be the same temperature. But the via looks something like an internal conductor, completely surrounded by board material. The trace has conducting material underneath it, but air above it. And the board is more efficient at cooling the trace than is the air. This is the same reason IPC 2152 found that internal traces run cooler than external traces, all other things equal.

The conclusion? It would appear that a single, 10 mil diameter via is adequate for conduct-

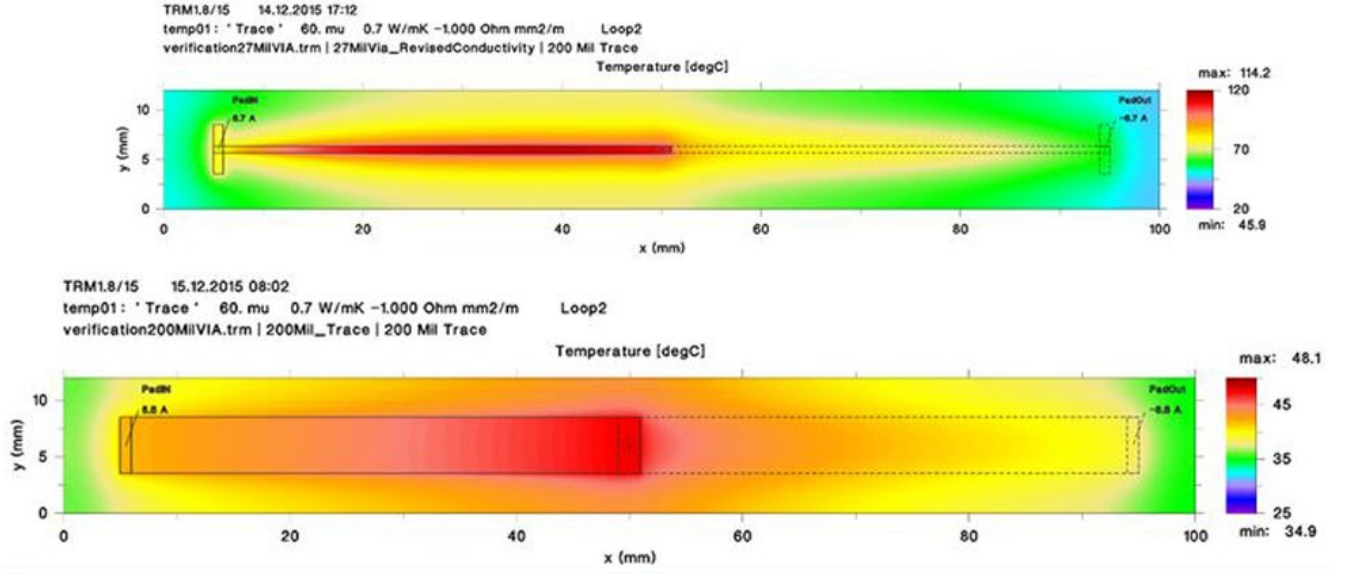

Figure 2: Thermal profiles of a 27 mil trace (top) carrying 6.65 A and a 200 mil trace (bottom) carrying 8.55 A.

ing any amount of current through a via, as long as the respective traces are sized correctly. This has significant implications for some designs in that additional routing channels might now be open for trace routing that were not open before. And to the extent that vias have a cost, reducing their number therefore has improved cost benefits.

(Note: It is assumed here that the problem is managing heat buildup at the via. We do not address the voltage buildup across the vias, and whether a particular circuit might require multiple vias for voltage control. But we know of very few designs where additional vias are needed for voltage control. Nor are we addressing high-speed issues where via inductance might be an issue.) **PCBDESIGN**

References

1. Editor Andy Shaughnessy responds: A current walks into a bar and takes a table. Two voltages are sitting at the bar. One turns to another and says, "So how many vias does it take to drive her home?" OK, don't blame me. Blame Andy!

2. The papers, including this one, are available at www.ultracad.com .

3. Thermal Risk Management (TRM) is designed to analyze temperatures across a circuit board, taking into consideration the complete trace layout with optional Joule heating as well as various components and their own contributions to heat generation. Learn more about TRM at www.adam-research.com

4. IPC-2152, "Standard for Determining Current Carrying Capacity in Printed Board Design," August, 2009, www.ipc.org, page 26.

5. Contact: Adam Harris, C-Therm Technologies, 921 College Hill Rd, Fredericton, NB, Canada, E3B 6Z9, www.ctherm.com.

6. Contact: Dave Ryder, Prototron Circuits, Inc., 15225 NE 95th St., Redmond, WA 98052, www.prototron.com.

Douglas Brooks, Ph.D., is the founder of UltraCAD Design Inc. He has written numerous articles in several disciplines and held signal integrity seminars around the world. He has spent most of his career in the electronics industry in positions of engineering, marketing, management, and as CEO of several companies. Prentice Hall recently published Brooks' latest book, PCB Currents: How They Flow, How They React. Visit his website at www.ultracad.com.

MaXphone to Bridge Handheld Radios and Smartphones

For as high-tech as Department of Homeland Security operations have become, radio communications for the federal agency remain entrenched in the previous century. But researchers from the University of California, San Diego Qualcomm Institute, in collaboration with MaXentric Technologies, are hoping a new technology that bridges legacy land-mobile radio (LMR) and LTE cellular networks will provide the upgrade the Department of Homeland Security needs.

Known as the MaXphone (officially, Multi-Access Extension for Smartphones), the prototype device consists of a plastic sleeve or "MaXjacket" that fits over potentially any smartphone.

"The hardware developed for the MaXjacket runs an open-source software defined radio (SDR) version of P25," said Per Johansson, Vice President of Engineering at MaXentric. "The open-source SDR approach gave us a lot of design flexibility and access to all parts of the radio."

Co-PI Curt Schurgers, director of the Wireless Systems Laboratory at the Qualcomm Institute, likens the MaXphone to a bridge that connects two parallel highways.

"It's been a very interesting and exciting journey working on this project," added Johansson. "The MaXphone is one of the most novel approaches we've seen so far, and it's been an amazingly successful prototype."

Dynamic Models for Passive Components

by Istvan Novak
ORACLE

A year ago, my QuietPower column [1] described the possible large loss of capacitance in multilayer ceramic capacitors (MLCC) when DC bias voltage is applied. However, DC bias effect is not the only way we can lose capacitance. Temperature, aging, and the magnitude of the AC voltage across the ceramic capacitor also can change its capacitance. Finally, the initial tolerance needs to be considered as well. In the worst case, we may lose up to 90% of the capacitance for an X5R capacitor, and even for an X7R capacitor. This column will show you the details and also how the most advanced manufacturers are helping the users with new simulation models to take these effects into account.

As an actual example, let us look at one of the capacitors that was extensively tested [2], where 1uF 0603-size 16V capacitors were tested from various vendors. We further assume that we want to use the part on a 12V supply rail, where the AC noise is low (this will be important later when we take the AC bias dependence into account). Some of the samples were chosen with X5R, some with X7R temperature characteristics. As showed with actual test data [2], X7R capacitors are sometimes worse for DC bias sensitivity than X5R parts.

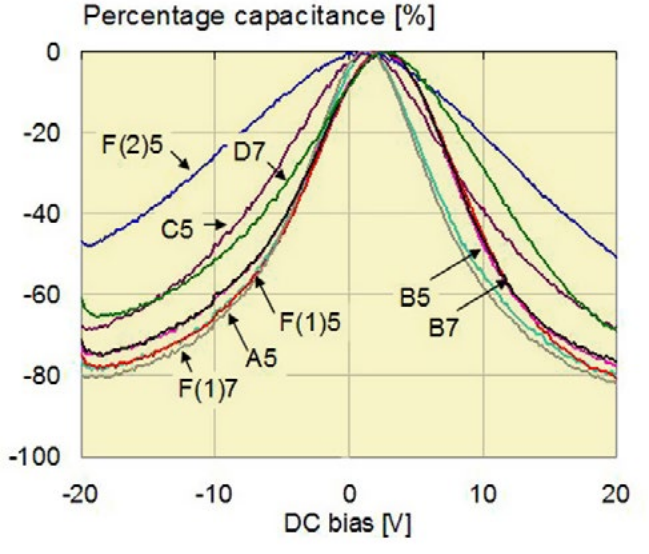

Figure 1: Percentage capacitance as a function of DC bias for all studied 1uF 0603 16V models, measured at 100 Hz and 10 mV AC bias.

If we take the part from Vendor B (labeled B7) in Figure 1 (this was Figure 5 [2]), we see that at 12V DC bias we can lose 60% or 70% of the capacitance, dependent on which way the DC bias changes. But when we need to consider the worst-case capacitance loss, we have to consider the cumulative effect of all of the following factors:

- Initial tolerance
- Temperature effect
- DC bias effect
- AC bias effect
- Aging

The sample had +-10% initial tolerance. The X7R temperature characteristics comes with an additional +-15% tolerance window for the temperature variation.

When the part is used with low AC excitation across the part, the capacitance may be up to 20–30% less than what the standard test procedure provides. Since the vendors use the standard test methods, the AC bias dependence has only a negative range: 0 … -20%, sometimes up to -30%.

The aging in ceramic capacitors creates an exponential decay with a fixed percentage drop of capacitance for every decade of passed time. In case we take -2.5% per decade drop for X7R parts [3] and assume that the initial capacitance is measured 24 hours after manufactur-

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	Percentage range [%]	Relative multiplier
Initial tolerance	+-10	0.9 … 1.1
Temperature effect	+-15	0.85 … 1.15
DC bias effect	+0 -70	0.3 … 1
AC bias effect	+0 -30	0.7 … 1
Aging (over 3 years)	+0 -7.5	0.925 … 1

Table 1.

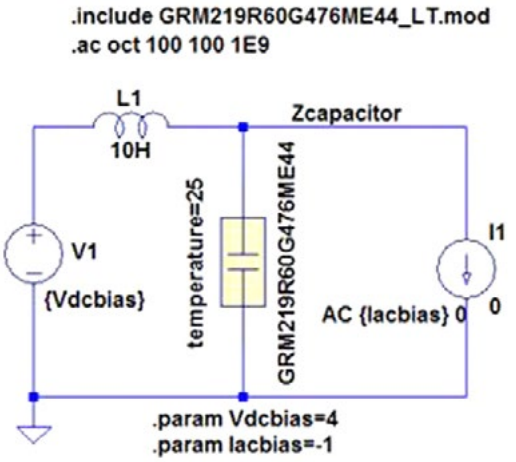

Figure 2: LTSPICE simulation deck to calculate the linearized impedance at the 4V DC bias point.

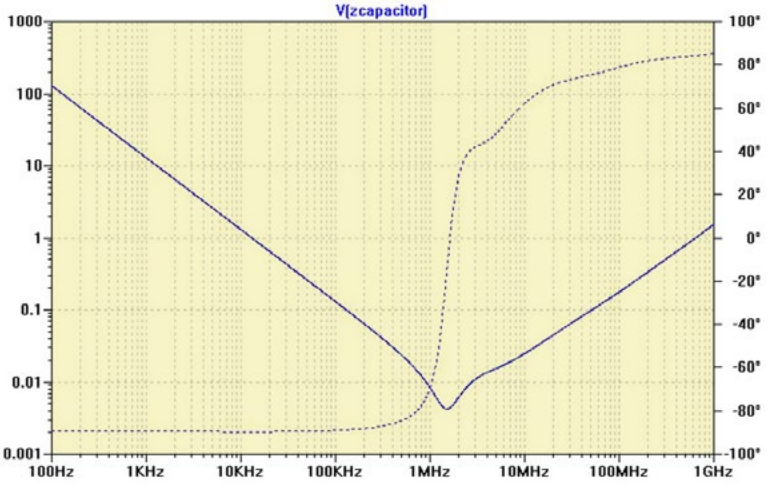

Figure 3: Impedance versus frequency (magnitude, solid line, left axis and phase, dashed line, right axis) of the GRM-219R60G476ME44 capacitor, simulated with its dynamic model.

ing, within an expected life span of three years (26208 hours) this means approximately three decades of time, resulting in a -7.5% capacitance drop. If we consider the worst-case cumulative effect of all of the above contributors, we need to multiply all of the ratios corresponding to these percentage values. In the table below, we repeat the list of contributors together with their worst-case limits for the example part.

When we multiply the worst-case contributors, we get 0.9*0.85*0.3*0.7*0.925 = 0.15, which means instead of 1uF we have only 0.15uF capacitance. From the table we also see that with modern high density ceramic capacitors the biggest possible capacitance drop is due to the DC and AC bias effects. In some applications the loss of capacitance is important to know and therefore users want to simulate it. Until recently, however, simulation models were available only for no-bias conditions.

This has changed with the emerging dynamic models [4], which use controlled sources inside encrypted models to create a true nonlinear response according to the instantaneous excitation across the part. Dynamic models are currently available for a number of popular simulators. The examples shown here were run on Linear Technologies LTSPICE. For the illustrations below we use a GRM219R60G476ME44 part, which is 47uF +-20% X5R 4V capacitor in a 0805-size package. Figure 2 shows the LTSPICE circuit to simulate the impedance of the capacitor with different bias conditions and Figure 3 shows the impedance with 4V DC bias.

The data from Figure 3 can be post processed and we can display impedance magnitude and

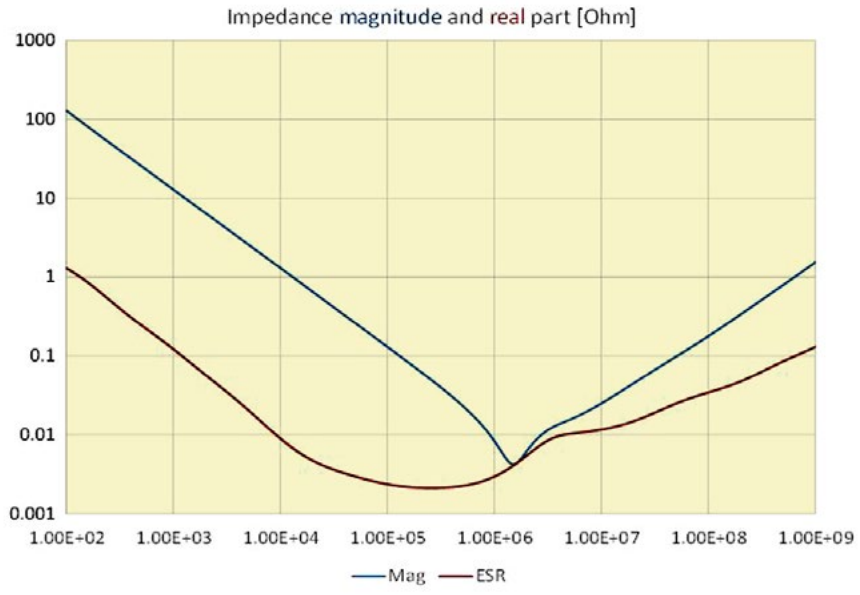

Figure 4: Impedance magnitude and real part as a function of frequency, shown for the GRM219R60G476ME44 part with 4V DC bias.

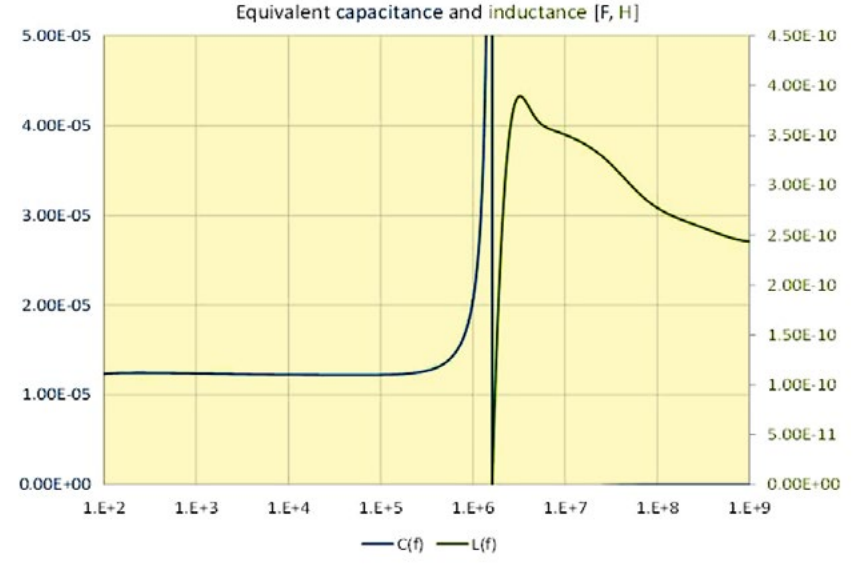

Figure 5: Extracted capacitance (blue trace, left axis) and inductance (green trace, right axis) for the GRM219R60G476ME44 part with 4V DC bias.

We can also run the simulation at different DC bias levels and show the equivalent capacitance at different DC bias voltages and we get a plot as shown in Figure 6. Note that even at 0V DC bias, the capacitance is just 35uF instead of the nominal 47uF. The reason for the difference is the AC bias dependence of the part. This dynamic model is based on measured data, where the excitation level is just a few millivolts, whereas the nominal capacitance is specified with a 0.5Vrms source voltage, and with the larger AC excitation the capacitance is bigger.

The above simulation results used the AC SPICE simulation option, which linearizes the model at the given DC operating point. For this reason the capacitance extracted from the AC simulation result would not change if the test current value (I1 in Figure 1) changes. Of course we would need to scale the result, for instance with I1 = 0.1A, we would need to multiply the result by 10 to get the correct impedance, but beyond this scaling we would get the same result for any value of I1. With time-domain simulations, however, we can expect the capacitor to show different capacitance values dependent on how the instantaneous voltage changes across the part. This best can be shown if we simulate the capacitor model with a linear voltage ramp across the part. The current through the capacitor will be proportional to its capacitance multiplied by the voltage slew rate.

This means as the voltage across the capacitor changes as the ramp moves, the current through the capacitor also changes according to the change of capacitance with voltage bias. To make sure that we capture the DC bias dependence, we need to select a slow enough ramp. The ramp voltage in our simulation changes four volts in four millisecond. This

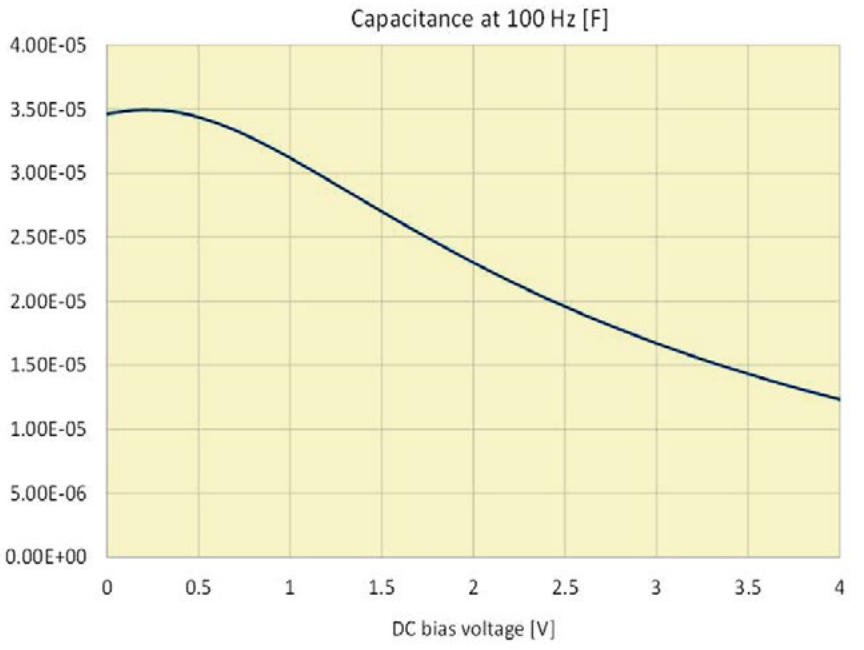

Figure 6: Capacitance of the GRM219R60G476ME44 part at 100 Hz and different DC bias levels.

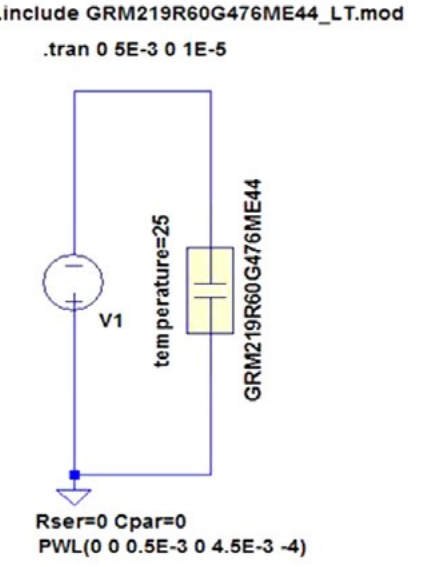

Figure 7: Time-domain simulation deck to measure the voltage-dependent capacitance with a voltage ramp swinging from 0V to 4V.

voltage slew rate across the capacitor approximately corresponds to a bandwidth which matches the 100 or 120 Hz measurement frequency used by component vendors to test their parts. Figure 7 shows the simulation deck, Figure 8 shows the result. The current waveform in Figure 8 shows sharp spikes at the beginning and the end of the ramp. We can ignore those spikes, since they are the result of the ideal piece-wise-linear voltage ramp with sharp corners at those time instances. For the duration of the voltage ramp, the current shows a voltage dependence that is very similar to that which we see in Figure 6. In fact from the current vs. time function of Figure 8 we can

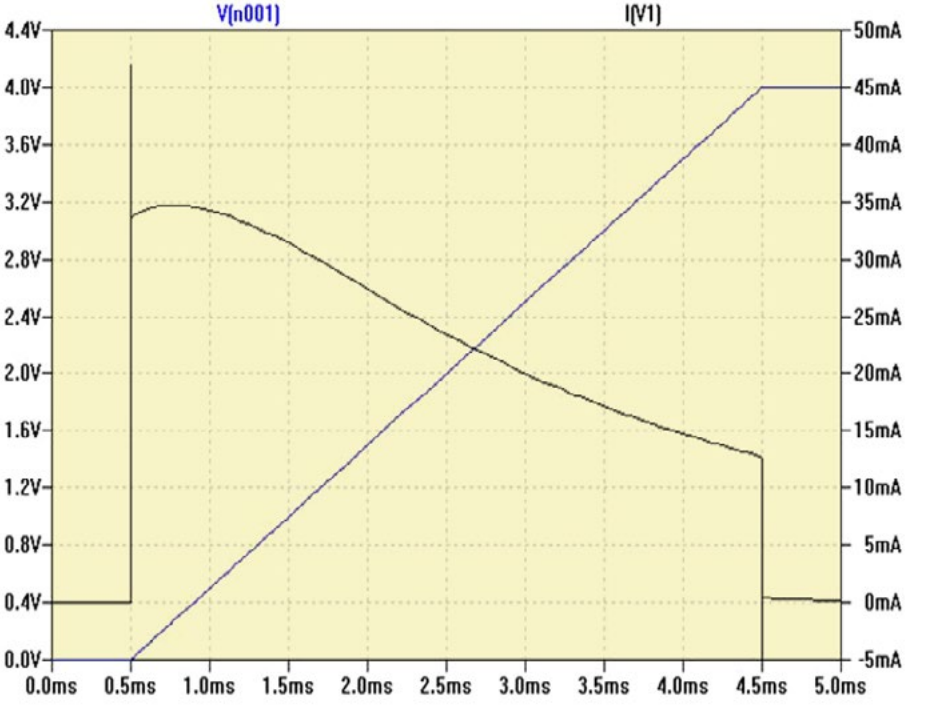

Figure 8: Time-domain simulation results with the simulation deck shown in Figure 7. The blue trace with its axis on the left is the voltage ramp across the capacitor. The black trace with its axis on the right is the resulting current through the capacitor.

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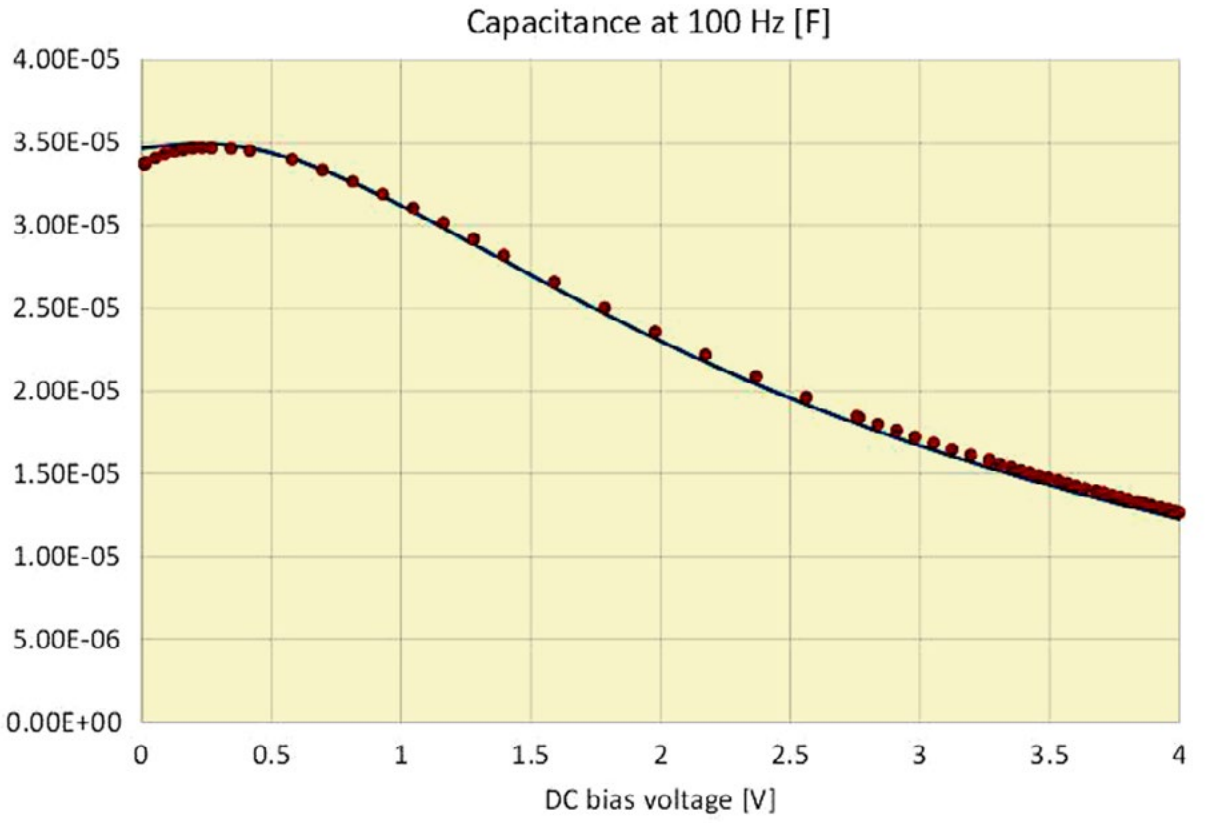

Figure 9: Comparison of capacitance vs. DC bias voltage simulated with AC run vs. time-domain ramp.

back calculate the capacitance and can show it on the same plot together with the AC simulation results, see Figure 9.

The solid blue line is the same data we showed in Figure 6; this was the result of SPICE linearized AC analysis around the DC operating point. The red dots are the capacitance values calculated from the time-domain waveform of Figure 8.

The very good agreement between the two data series in Figure 9 proves that these dynamic models are actually nonlinear and the capacitance changes instantaneously with the voltage. The dynamic models allow us to simulate the effect of bias dependence in LC filters, power circuits and in many other applications. **PCBDESIGN**

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3. Johanson Dielectrics Ceramic Capacitor Aging Made Simple.

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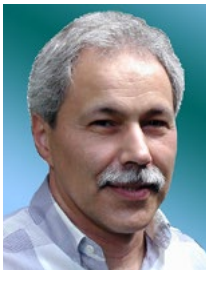

Dr. Istvan Novak is a distinguished engineer at Oracle, working on signal and power integrity designs of mid-range servers and new technology developments. With 25 patents to his name, Novak is co-author of "Frequency-Domain Characterization of Power Distribution Networks." To contact Istvan, click here.

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MilAero007 Highlights

New Made-in-NTU Satellite Technologies Pass Space Tests

Nanyang Technological University, Singapore (NTU Singapore) and BAE Systems have signed a $2.5 million partnership to jointly develop next-generation cybersecurity solutions in an era of rising cyber attacks.

Footsteps Could Power Mobile Devices

When you're on the go and your smartphone battery is low, in the not-so-distant future, you could charge it simply by plugging it into your shoe. An innovative energy harvesting and storage technology developed by University of Wisconsin, Madison mechanical engineers could reduce our reliance on the batteries in our mobile devices, ensuring we have power for our devices no matter where we are.

High-Performance Laminates

High-performance laminates are characterized as base materials that in one or more aspects exceed the performance of FR-4, CEM, or paper/phenolic laminates. In this article, Karl Dietz talks about the different types of laminates, their dielectric requirements, and how they are being manufactured.

Fabrication Drawings and Electrical Test—Reading the Fine Print

When a new PCB design is born, designers envision what the product will provide when completed. Whether the product is for the consumer, aerospace, military, medical or countless other markets, the designers—or more likely, the customers—expect certain deliverables on the commodity they wish to purchase.

FTG Receives New Multi-year Contract Awards for its Circuits Business

Firan Technology Group Corporation (FTG), a leader in aerospace and defense electronics, announced today that it has renewed two long-Term Agreements with a prominent US based Aerospace, Space and Defense Contractor for its Circuits Toronto and Chatsworth facilities.

New Galaxy-hunting Sky Camera Sees Redder Better

A newly upgraded camera that incorporates light sensors developed at the U.S. Department of Energy's Lawrence Berkeley National Laboratory (Berkeley Lab) is now one of the best cameras on the planet for studying outer space at red wavelengths that are too red for the human eye to see.

New Tool Provides Successful Visual Inspection of Space Station Robot Arm

As NASA takes a break in RRM operations, it's looking back on past achievements and celebrating one of its latest accomplishments: the successful inspection of Canadarm2, the International Space Station's (ISS) robotic arm. In time, this visual inspection capability may help future servicing ventures at other orbits inspect for damage and failures on their spacecraft.

Mission Teams Prepare for Critical Days

Moments after Sentinel-3A separates from its rocket, a team of European mission control specialists will assume control, shepherding new spacecraft through its critical first days in space.

Global Defense Industry Business Confidence Report H1 2016

This defense Industry Business Confidence Report H1 2016 presents executives' opinion on the business environment over January 2016–June 2016. Organizations can understand the market by analyzing existing economic conditions, supplier price variations, sales performance, industry and company growth outlook, spending patterns, and key priorities.

Robotic Drones to Print Emergency Shelters for Those in Need

A new research project aims to develop the world's first flying robots capable of autonomously assessing and manufacturing building structures to help areas suffering from natural disasters.

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Ventec Europe Accredited to AS9100 Revision C

We are proud to announce that the quality management system at our Leamington Spa, UK, headquarters is now fully accredited to AS9100 Revision C (the two facilities of our parent company, Ventec Electronics Suzhou Co Ltd, have been fully AS9100C certified since 2012).

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Romania's TIE Design Conference Celebrates 25th Year in April

If you thought all of the PCB design conferences were held in North America, think again. The Tehnici de Interconectare in Electronica (Interconnection Techniques for Electronics) conference will mark its 25th year during this year's event, held April 20-23 in Suceava, a city in Northeast Romania.

Dr. Paul Svasta

The conference is the brainchild of Dr. Paul Svasta, a professor of electrical and electronic manufacturing at Politehnica University of Bucharest – CETTI. Svasta said he's pleased to see the event he founded in 1992 celebrating such a milestone.

"It's nice to achieve, after so many years, normality," Svasta said. "It's important to remember that this education and training is focused on the needs of the industry. This helps bring academia closer to the industry."

The event brings together the leaders of Romania's academia and the electronics industry, culminating in a PCB design contest for college students. Thirteen universities send three PCB designer students each to TIE; the students spend four days in PCB design workshops and compete in a design contest known as "The Olympic Games for PCB Designers." Winners are awarded a "PCB Designer Certificate of Competence."

TIE is sustained by the IEEE CPMT Joint Hungary & Romania Chapter. Svasta was recently awarded the 2015 IEEE CPMT Regional Contribution Award – Region 8 (Africa, Europe, Middle East) for establishing the TIE event and the IEEE International Symposium for Design and Technology in Electronic Packaging (SIITME).

Svasta points out that a number of global electronics companies have facilities in Romania, including Continental Automotive Systems; over 4,500 of Continental's electronics engineers are located in Romania.

He credits TIE with bringing more young people into the relatively mature PCB design community.

"Interest in the contest from high school students has increased," Svasta explained. "In the spring, I will visit some of the high schools that are focused on teaching science and math. I will be going with my students."

Now 74, Svasta said he has no plans of retiring any time soon.

"I am 74 biologically. I love what I do."

For more information, visit www.tie.ro.

EMA is Bullish on Data Management

by Andy Shaughnessy

EMA Design Automation has evolved over the years, from a typical Cadence Design Systems VAR to a distributor that functions more like a part of Cadence. During DesignCon, I met with Greg Roberts, director of marketing for EMA, and asked him to discuss the company's focus on data management tools, and why he's giving away certain OrCAD tools.

***Andy Shaughnessy:** Greg, why don't you start by giving us a little bit of background about EMA.*

Greg Roberts: EMA is Cadence's channel partner for North America—we predominantly sell their PCB tools and cover Canada, the United States, and Mexico. That includes the OrCAD, PSpice, Allegro, and Sigrity product lines.

***Shaughnessy:** And I understand you guys are giving away a tool?*

Roberts: Yes, we've got a new promotion. We have ads all over that say, "Free OrCAD Capture."

***Shaughnessy:** So how does that work?*

Roberts: In the EDA world, you typically buy the software and also pay for maintenance. They're two separate prices and you put them together for the first year. We're giving away the software. You get a perpetual license, but you have to pay for the maintenance.

So a tool that used to be $1,400 for the software and $390 for the maintenance is now just $390. At the end of one year if you don't want to keep paying for the maintenance, you don't have to and the software is still yours. However, we think you will because for the maintenance price you receive a number of benefits, like phone support. You can call our engineers and talk to them about whatever problems you're having—we get pretty good accolades about our phone support.

Additionally, you get access to our engineering resource center where you can find app notes and other information. You get access to Cadence's as well, and as Cadence releases updates to the software, you get those updates for the whole year. We think it's a pretty good value for the maintenance on top of the free software.

Greg Roberts, EMA director of marketing.

We also don't want new users to not be able to use the software. OrCAD Capture itself comes with some training videos built in, but we've enhanced that with our iTrain software. It's basically our classroom training in an online format; you can go through the same classroom exercises and learn the software that way. On top of that we said, "People always have parts they can't find symbols and footprints for," so we're also giving the customer a three-month license of OrCAD Library Builder, which does a number of things like build symbols from data sheets. For instance, you might have a 256 or 512-pin BGA, and you just scrape it right off the PDF, massage it a bit, and it spits out the symbol. Then you can go over to the footprint side and make IPC-compliant footprints. It's quite the deal. Today we sent out an e-mail blast to some of our customers and prospects letting them know about the offer and we're kind of getting inundated by the response.

Shaughnessy: *That's a good model.*

Roberts: It is fun. Apparently, OrCAD back in the heyday did something like this—way back between the DOS and the Windows days. I wasn't aware of that, but people have reminded us. So we're doing it again.

Shaughnessy: *Data management is a big area for you. You all wrote an article about data management for us a few months ago.*

Roberts: We've spent a fair amount of time looking at some of the kinds of problems customers run into. We can do schematics, PCB, and simulation, but a lot of times they're running into things that aren't really design problems, they're management problems. How do you manage all these parts in your library?

We've had CIS and CIP for quite a while, but a big part of it was, "What about all my designs? How do I know the history? How do I track revisions?" And that's what EDM is, engineering data management.

It gives you things like check-in and check-out. So you can check-in your designs, track revisions, check-in libraries, changes, and more. A lot of customers seem to be really interested in that, and it's solving a big problem for them.

Shaughnessy: *Most of our readers know how to design a board. The majority of them are senior designers, but they're just inundated with all this data. They've got all this data they've got to keep track of.*

Roberts: I visit customers and it's kind of interesting. As a tool vendor, you tend to think, "Oh, they're just spending all day in my tool." A lot of times that's not true. They design their board, they design the circuitry or whatever they're doing, and then they spend all this time worrying about this other stuff. They've got Excel spreadsheets, Word documents, different revisions, and all this data. How do you deal with that? This is what we're trying to help them with.

A corollary to that is a lot of companies have PLM. Engineers do a lot of work-in-process, but once you get the first rev now they have to deal with PLM. We've integrated with some of the

PLM systems, and one we've done recently is the Arena PLM integration. That's been very popular with our customer base.

Shaughnessy: *You guys are in a good spot to be, helping designers with their data. As they get more and more productive, it's like the data just grows and it's like an octopus that they can't control.*

Roberts: One thing we hear from customers is the number of designs they're required to do seems to keep going up, the amount of time they've got to do them keeps going down, and there's just so much competition. I was at CES and it was just amazing how many new products and ideas are coming out—everybody's working really hard and really fast to get their stuff to market. We're there to help them get it to market faster.

Shaughnessy: *Right, from Fitbits to hover boards. We had a few of our editors at CES.*

Roberts: And those are some of the big-name things, but there are things to keep track of your dog or your cat while you're away, steering wheel covers that keep track of whether you've got your hands on the wheel or not, just all kinds of things. They're putting circuitry in places I never expected.

Shaughnessy: *Is there anything you would like to add?*

Roberts: We're at DesignCon, so while we're here I'd just say this has been a good show for us.

Shaughnessy: *It looks like they've expanded it since last year.*

Roberts: Yeah, it's a bigger show and there's more traffic as well. It's kind of fun. I talked to a guy just now who downloaded the lite version of our software to do some kind of a wearable. He had never used the software before and he figured it out on his own. He did the schematic design and did the board all the way to Gerber. He's pretty happy, but now he really needs to move up because the lite version only lets you do pretty small designs.

That's the nice thing about this show. He had a question he couldn't figure out, so he came in and got a little free training. We gave him a little tutorial on how to do thermals and connect it to pads and things like that. It worked out pretty well for him, and I think he's going to move up to the next level in the software. It's a great show for people to come and learn about what's available.

Shaughnessy: *Greg, I appreciate you taking the time to talk to me.*

Roberts: I always like talking to you Andy, thank you. **PCBDESIGN**

Robots: Eliminating the First Contact with an Enemy Force

"We should be thinking about having a robotic vanguard, particularly for maneuver formations," said Dr. Bob Sadowski.

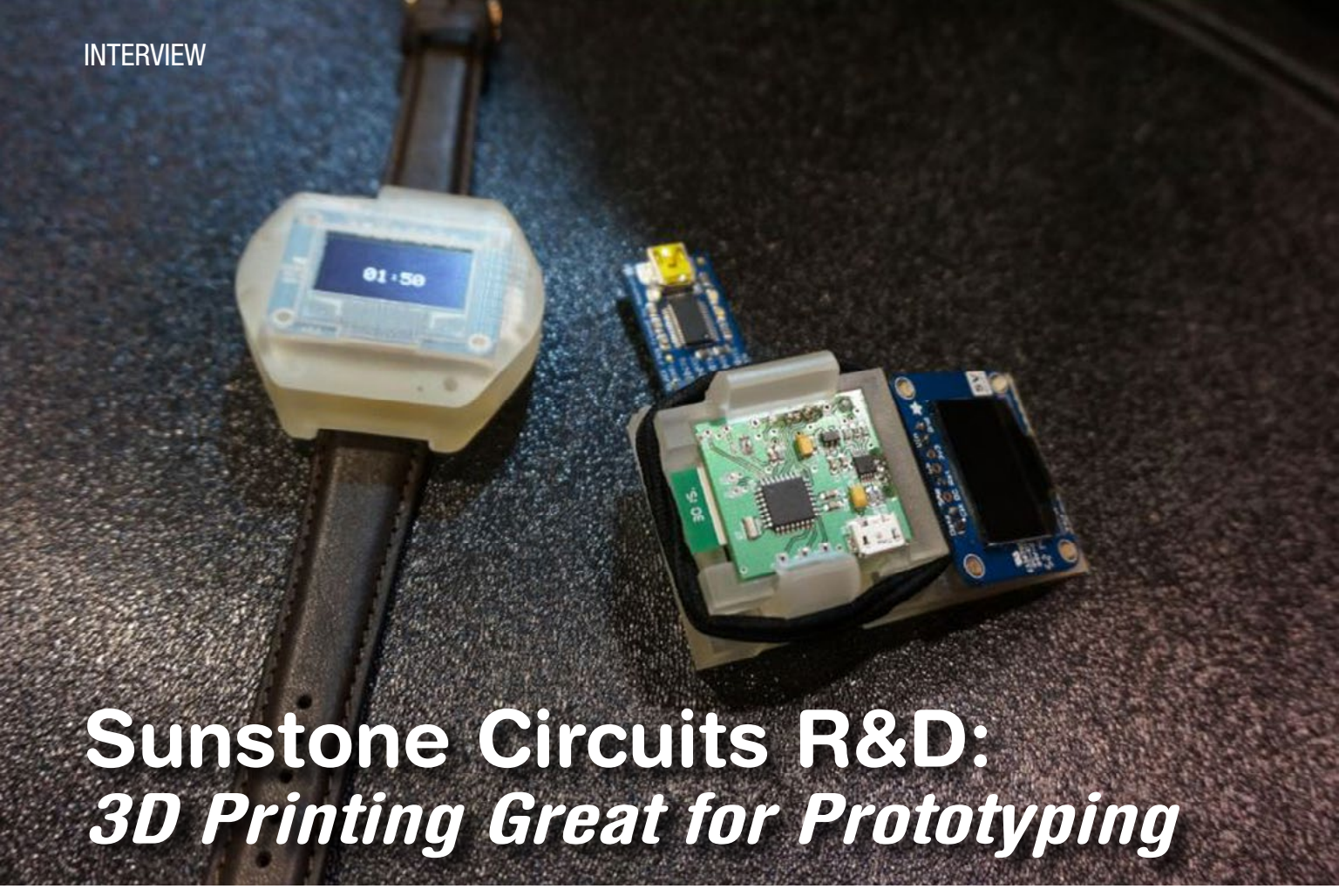
Sadowski, the Army's chief roboticist at U.S. Army Tank Automotive Research Development and Engineering Center, or TARDEC, in Warren, Michigan, spoke at a robotics conference here, March 2.

Over the last 10 years, the Army has focused on logistical challenges in Iraq and Afghanistan, Sadowski said. A lot of soldiers were lost in convoys that encountered improvised explosive devices and the funding and research went into stopping that.

Today, the effort is still in logistics, but current thinking and doctrine is that robots should be more than logistics; they should be in the fight as well, he said.

The Marines tried this with a robot in Afghanistan, a mule-like device that followed a patrol dismounted, he said. It was rated for 1,000 pounds but the Marines loaded it up with 2,000. Then they complained it was too slow.

Currently, testing of vehicles is being done on-road, but off-road is where soldiers fight,he said.



Sunstone Circuits R&D:
3D Printing Great for Prototyping

by Barry Matties

We've been hearing a lot about 3D printing for the past few years. But where does 3D printing fit in with traditional rigid circuit board development? Sunstone Circuits recently completed a project that focused on that very question. Sunstone Product Manager Nolan Johnson explains why 3D printing is a viable option when it comes to jigs and parts of the support infrastructure that are needed when prototyping today's emerging technologies.

Barry Matties: *Nolan, today we're talking about some new technology that you're demonstrating here. Why don't you start by telling us about it.*

Nolan Johnson: Sure. We're here at the IDTechEx printed electronics show where there are a lot of emerging technologies around graphene, printed electronics, energy, IoT, wearable devices, and that sort of thing.

Matties: *Where does the traditional rigid circuit board work fit into that sort of environment?*

Johnson: Well, the story that we're telling here is this: We did a project starting with some open-source designs for a smartwatch, a Bluetooth connection to an Android application, and we started with some off-the-shelf components. We breadboarded together the design, confirmed that it would work, and then we started using our expertise at Sunstone with PCB123® to design a custom single board to hold the Arduino and all the support electronics. We made a single board for the smartwatch, and attached that to an OLED display. Then using our sister company, 3D Fixtures (www.3dfixtures.com), we rapid prototyped a series of watch cases and a jig. The jig has some control circuitry underneath that is a basic circuit board. With this, we can take the board once it's back from manufacturing and assembly, snap it into the jig, program it, make it a functional watch, and put it into the case.

We counted the hours to do this from start to finish including rapid prototyping the jig, concurrently with having the boards manufactured. Everything came together on the workbench on the same day and to go from the start

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to a prototype that we could show off here at the show, took 59 hours. Where the rigid PCB and 3D printing really fit, as we see it, is in the support infrastructure for the manufacturing and finalizing of all of the emerging technologies.

***Matties:** Tell us how the customers are going to win by doing this.*

Johnson: It happens more and more with Arduinos and other microprocessors that are so accessible going onto projects that are getting smaller and smaller all the time. One example is a gentleman we were talking to who has an Arduino-based hummingbird feeder that adjusts, heats and cools the hummingbird feeder to keep the nectar just exactly right for his hummingbirds. These microprocessors are showing up in all sorts of applications. At what point do you program that, boot load that into your consumer device and get that running?

You're going to need some jigs to do that even if you're just a small mom-and-pop shop doing that sort of thing, and that's exactly where 3D Fixtures benefits its customers. You can custom design what you need for doing that part of your work. Get it made in one, two, or three days in quantities of four, five, or six very affordably, and get started. It beats the heck out of trying to do metalwork at a machine shop to fit that sort of a thing.

Nolan Johnson, Sunstone product manager.

***Matties:** Is the idea that they buy the printer?*

Johnson: No, we do the printing for them. All we need to do this is the mechanical design. We can even help with the design, but basically we need the CAD file (STL or STEP), and we run it though the printer. It's just the same exact business model as we've been running at Sunstone with PCBExpress® and ValueProto® for years and years.

***Matties:** This is great, because the cost to buy a printer and all of the associated technology to go with it is a sizable investment for this sort of application.*

Johnson: Absolutely, it's a lot of money, and then the expertise to know how to run it. Machine operation is important. One of the things that we learned in making this particular test jig was that if the printer isn't calibrated, you might end up with a jig that looks right but the piece won't fit.

***Matties:** I liken this to the early days of typesetting when linotype came into use in publishing. There were service centers, but eventually linotype went away. What's the lifecycle of someone needing a supplier to when they're going to be able to buy the printer at an affordable price?*

Johnson: That's a great question. We'll all have to wait and see how that plays out with the dynamics of how 3D printers are going to come down in price. We need to remember, though, that there are still successful print shops due to unique requirements, special formats, and materials. The 3D printer that everyone can afford will not cover every need. We think there will always be a need for specialized 3D printing. It's been interesting to watch what's happened around this too, Barry.

You've got the 3D printers that busted out

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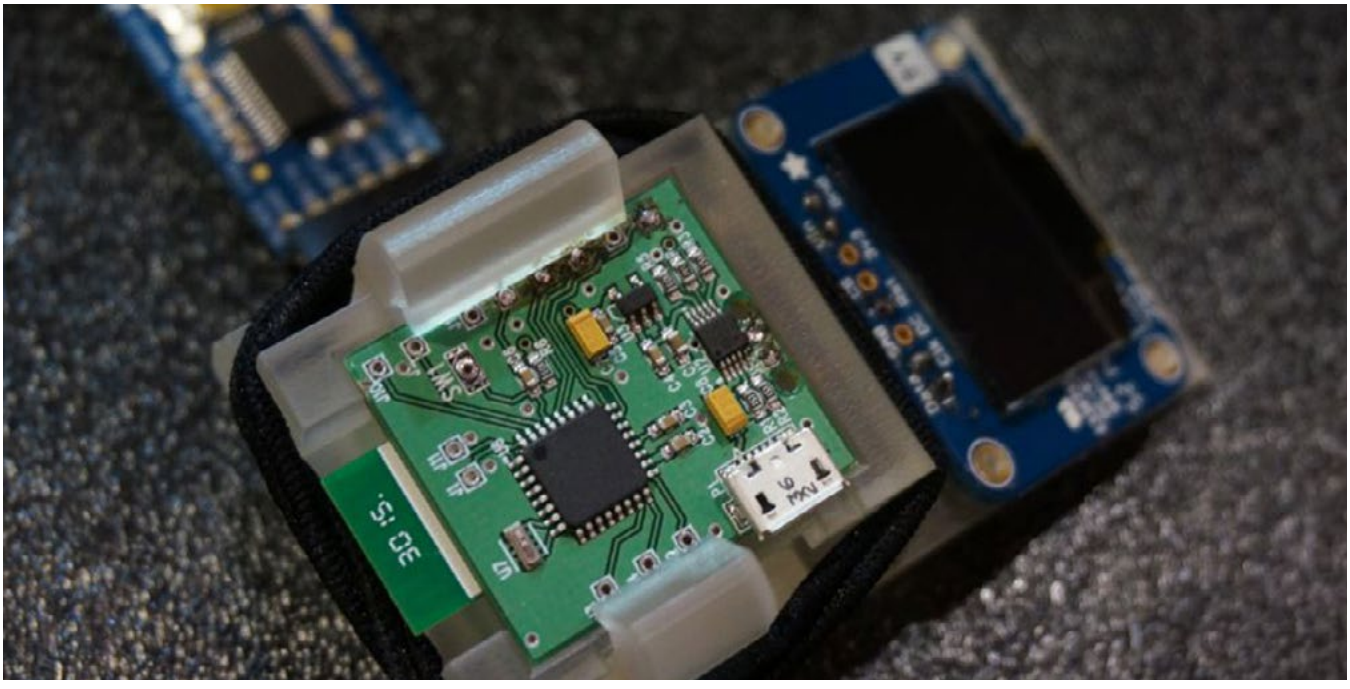


into the consumer sector in 2012. They do all the fun things, but they are mostly a novelty or toy, and not too industrial. Then you see people doing projects like, "Well, can we 3D print a car?" Or "How much of the car can we 3D print?" While conceptually you could actually do that, is it drivable and up to the real-world rigors? At this show, just as an example, there's a car here, the Blade, that's 3D printed, but what they're 3D printing is the key structural components to connect the carbon fiber tubes. That connecting part is being 3D printed and the rest of the car is being done in a traditional way. 3D printing is rapidly finding realistic, achievable applications in the industry and doing the right thing for the right part of the overall industry, but not taking over everything.

I think there's going to be a place that will make business sense for the right customer doing the right thing. Otherwise, they have to invest a lot of time and resource in getting their own in-house expertise for running that equipment.

***Matties:** Is this the same sort of process where they download the files, place the order, and a few days later their product is in their hands?*

Johnson: Absolutely, it's all done online.

***Matties:** Well, thanks so much for sharing. This is really great to see. It looks like this is an explosive market. It reminds me of when the personal computer came out. It was slow, but it empowered so many people and it changed the world, and that's what 3D printing is going to do.*

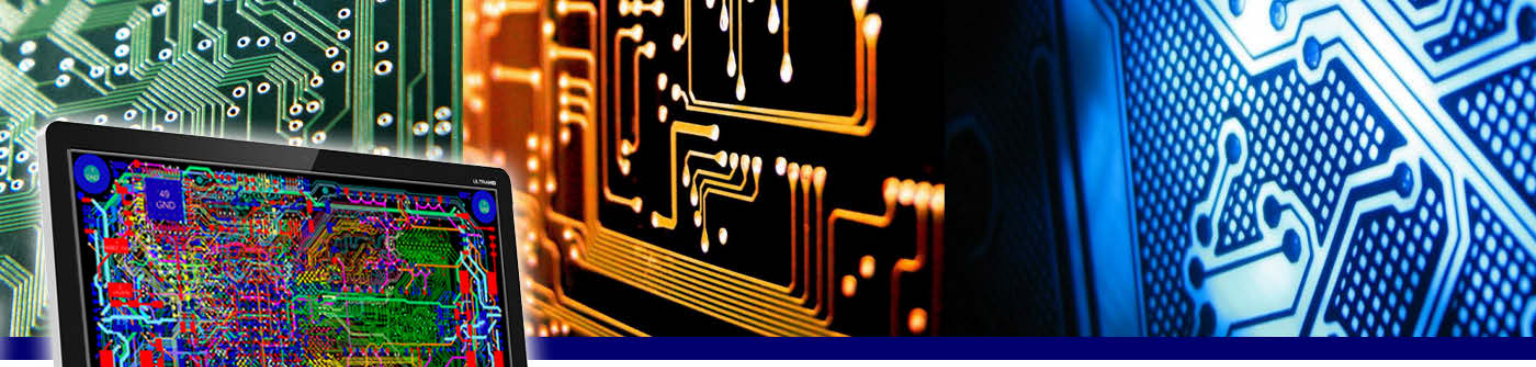
We're going to see a lot of innovation, new products, and new ideas. I think there's a manufacturing renaissance that's going to happen in America because of this and the types of services that you guys are providing.

Johnson: We're having a lot of fun. Just this morning I was talking to someone from a contract manufacturer, and he said they do a lot of different short-lived projects in their contract manufacturing business, and they need something like this.

***Matties:** Perfect, that's what you want to hear. Nolan, thank you so much. It's great to catch up with you again and it's exciting to see what you're doing.*

Johnson: Thank you, Barry.

For more information on the relationship between 3D printing and PCB design, read this Sunstone Circuits case study. **PCBDESIGN**



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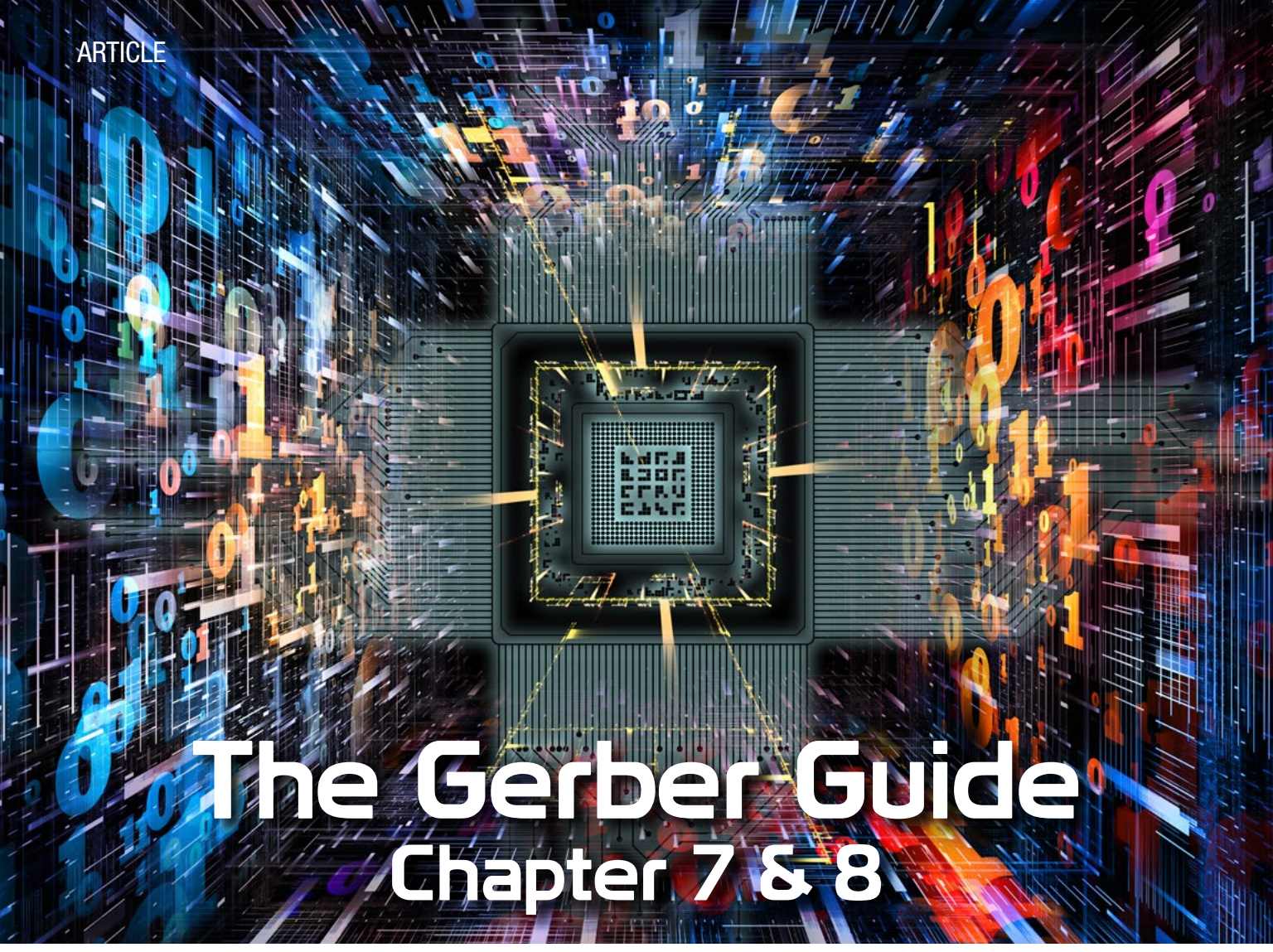

The Gerber Guide
Chapter 7 & 8

by Karel Tavernier
UCAMCO

It is possible to fabricate PCBs from the fabrication data sets currently being used; it's being done innumerable times every day all over the globe. But is it being done in an efficient, reliable, automated and standardized manner? At this moment in time, the honest answer is no, because there is plenty of room for improvement in the way in which PCB fabrication data is currently transferred from design to fabrication.

This is not about the Gerber format, which is used for more than 90% of the world's PCB production. There are very rarely problems with Gerber files themselves; they allow images to be transferred without a hitch. In fact, the Gerber format is part of the solution, given that it is the most reliable option in this field. The problems actually lie in which images are transferred, how the format is used and, more often, in how it is not used.

Each month we look at a different aspect of the design to fabrication data transfer process. In this monthly column, Karel Tavernier explains in detail how to use the newly revised Gerber data format to communicate with your fabrication partners clearly and simply, using an unequivocal yet versatile language that enables you and them to get the very best out of your design data.

Chapter 7: Junk, or the Difference Between Data and Drawings

The core of a PCB fabrication data set is its digital data files. These data files will be read into CAM to recreate a model of the PCB and then used for further digital processing. There must be a digital data file, in Gerber, for each pattern in the PCB: copper layers, drill and route files, solder masks, legends, peelables and whatever other patterned layers are present.

That said, a PCB fabrication data set may contain technical drawings—indeed, a mechanical

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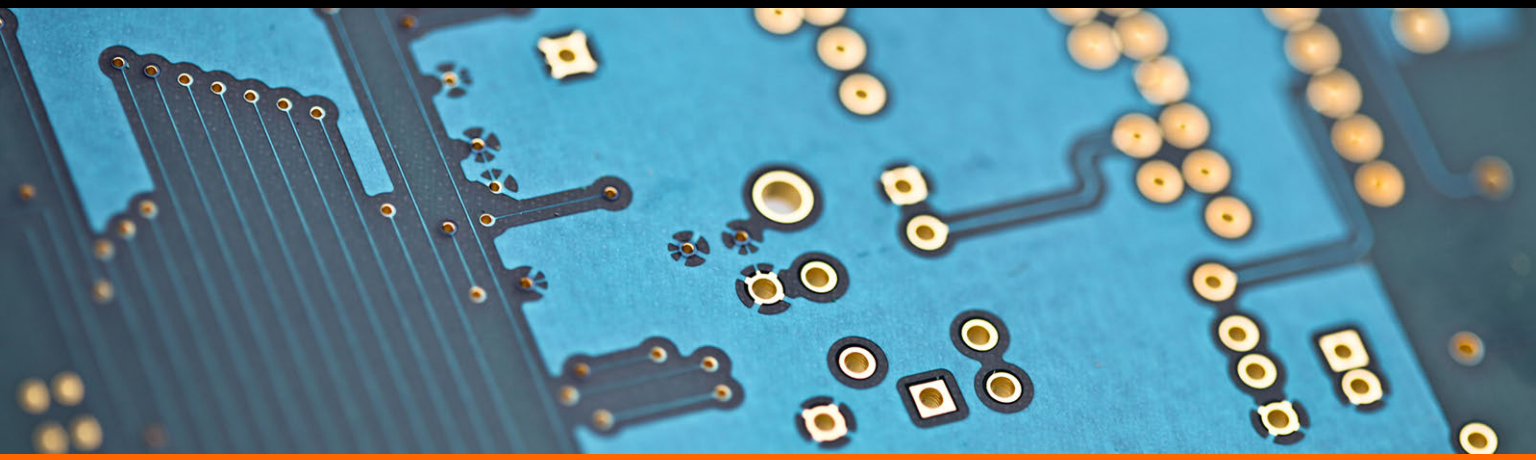

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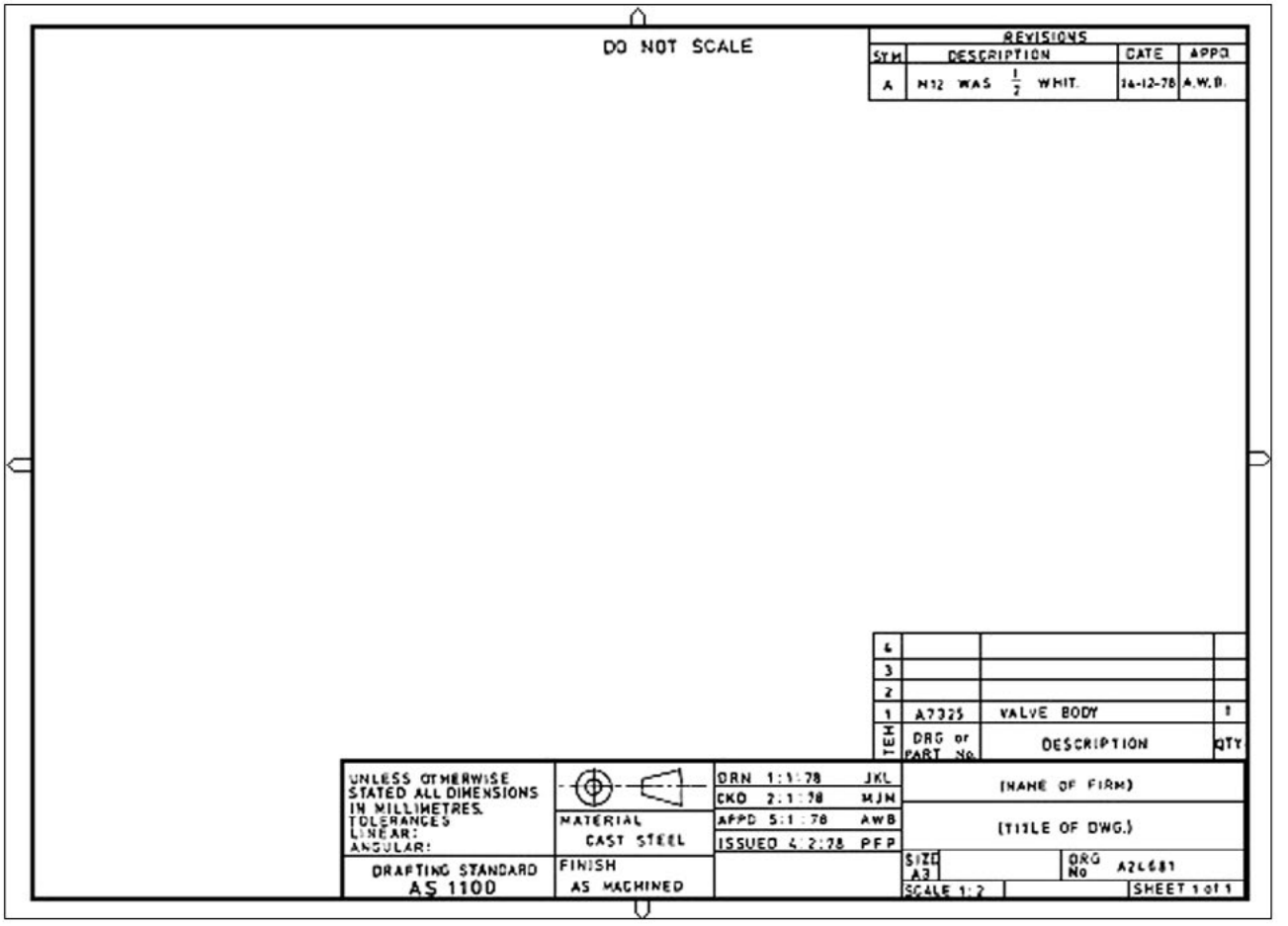


Figure 1: A typical frame for a technical drawing.

drawing is often absolutely essential. A technical drawing is intended not for digital processing, but for humans to look at, and it is made according to time-hallowed rules as shown in Figure 1, and includes a frame, title block, notes and legends.

As drawings are images, they too are best transferred in Gerber (more in Chapter 10). Alas, sometimes digital data and drawings are confused and a drawing frame is added to digital data, resulting in a copper layer (Figure 2).

While the frame is essential in a drawing that is made for people, it becomes junk when added to a digital data file such as a copper layer that is to be digitally processed by CAM software—and this junk must be removed manually by the CAM operator before the data can be used. Digital data does not automatically become a drawing because it represents graphic information. And expressing both drawings and graphical digital data in Gerber does not automatically make them drawings—or purely digital files.

Use only pure data files, without junk or embellishments. You may object that the title block contains useful information. This may well be—if so, the solution is to put that information in a separate text file or a true drawing. The data is then pure and can be used without manual cleanup and the information intended for the human operator is conveniently available in a separate file.

Remember, put only data in data files.

Chapter 8: Always Include the Netlist

Basically, a netlist is a set of nets, where each net has a name and a set of nodes identified by their XY coordinates. Nodes on the same net must be electrically connected. Nodes on different nets must be isolated.

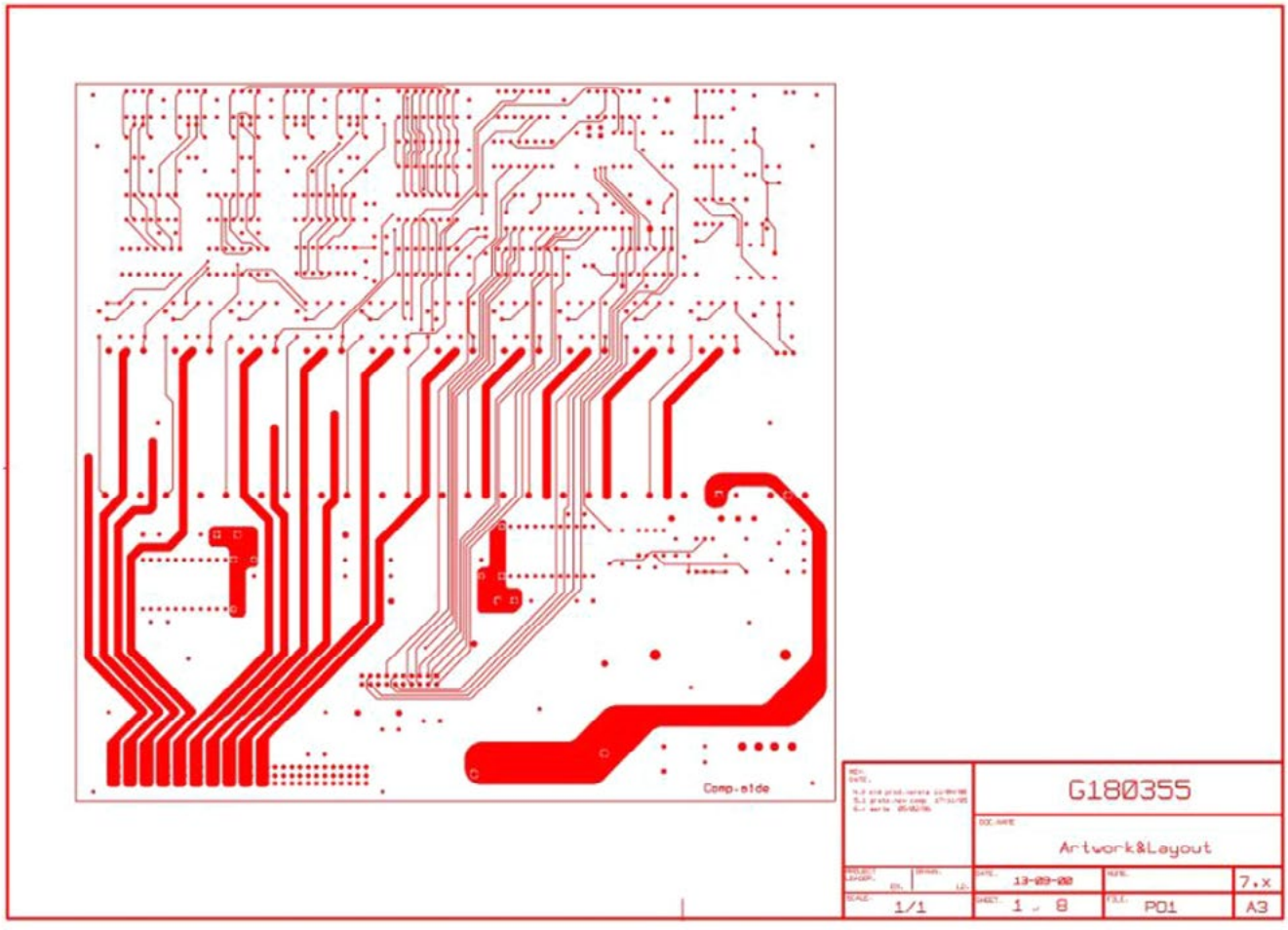


Figure 2: Confusing a drawing and digital data.

Including the netlist in the PCB fabrication data set increases the security of data transfer by an order of magnitude. The first thing a fabricator does after reading a fabrication data set into his CAM system is to generate a netlist—the reference netlist—from the image. During the CAM process the CAM engineer will regularly check the job data against the reference netlist to protect against operator or software errors. When a netlist is present in the incoming fabrication data set, he will also check his reference netlist against the supplied netlist.

Any serious errors in the images or drill files will inevitably result in netlist differences and set off an alarm. The presence of the netlist in the fabrication data sets protects against mistakes in data transfer, whether these are due to software or operator error, in CAD output or CAM input. Adding the netlist to the fabrication data sets extends the regular netlist check performed by the CAM operator to encompass not only the CAM process, but the complete CAD-to-fabrication data transfer.

Now, errors in the transfer of image data from CAD to CAM are rare, but they do happen. And they are very costly when they happen. Without the netlist, the fabricator cannot know he is working from a wrong image. He will faithfully manufacture the wrong PCB, which will pass his electrical test as it is tested against the netlist created from the wrong data. The error will only become apparent after the PCB is loaded with components, at which point the costs are staggering. All deadlines are missed, recriminations fly, and the search for the guilty starts. Simply including a netlist largely protects against such a rare but dramatic event – it is like installing smoke detectors and sprinklers. Fires

do not occur often either but everyone takes steps to protect against them.

The netlist is a powerful check on the image data; it is akin to the checksums that are widely used to make data transfer reliable. Including the netlist is simple. It is sufficient to include an IPC-D-356A file in the data set. IPC-D-356A contains all the necessary information, and more. Virtually all manufacturers can read IPC-D-356A and most CAD systems can output it.

It is sometimes claimed that comparing netlist and image data throws up many false errors. This is largely a problem of the past when implementations were new and buggy. Nowadays most netlist files are OK.

There is another way to view this: the netlist is the basis of any PCB layout, and the essential function of a PCB is to physically implement that netlist. The PCB fabricator is expected to electrically test the fabricated boards and to guarantee that the shipped boards' netlist is correct. It is therefore of paramount importance that the fabricator works from the correct netlist, so it is an obvious requirement that the netlist be supplied to the fabricator rather than leaving him to reverse engineer it from the images.

A professional PCB fabrication data set must include a netlist. Omitting it amounts to a self-inflicted competitive disadvantage.

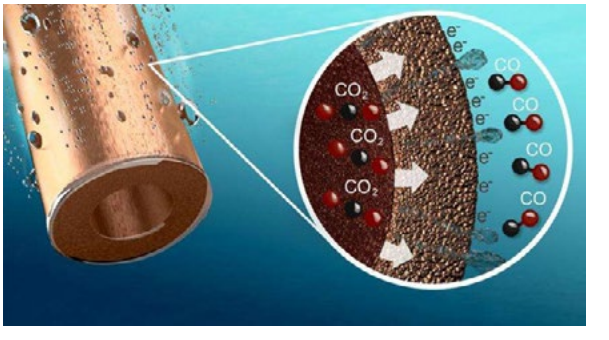
Because the inclusion of a netlist is so simple and is such a powerful security check on the data, Ucamco's position is that if a data transfer error occurs that would have been flagged by checking back to a netlist, the responsibility lies at least partially with the party that has neglected to include a netlist, or that has neglected to use a supplied netlist.

Remember, always include an IPC-D-350A netlist file in the PCB fabrication data set.

This column has been excerpted from the Guide to PCB Fabrication Data: Design to Fabrication Data Transfer. **PCBDESIGN**

Karel Tavernier is the managing director of Ucamco.

Researchers Develop Highly Efficient Hollow Copper Electrodes



Scientists at the University of Twente research institute MESA+ have developed an electrode in the form of a hollow porous copper fibre which is able to convert carbon dioxide (CO_2) into carbon monoxide (CO) extremely efficiently. In principle the invention enables a wide variety of industrial processes, for example in the steel industry, to be made more sustainable.

Researchers have developed a hollow copper fibre which can be used to convert CO_2 into CO with a very high efficiency. The fibre, which serves as an electrode, is provided with countless minute pores. If the fibre is placed in a bath of water, a voltage potential applied, and CO_2 pumped in, the CO_2 is converted into CO as it passes out through these pores.

Small copper particles are added to a polymer solution. This solution is guided through a small, ring-shaped slit in a water bath, in which the polymer solution solidifies into the form of a thin hollow fibre. A thermal treatment is then employed to remove the polymer and partially fuse the copper particles. The result is a copper oxide fibre.

The researchers particularly envisage an important area of application for these copper electrodes to be in the steel industry, where large volumes of CO_2 are produced and CO is needed to convert iron ore into iron.

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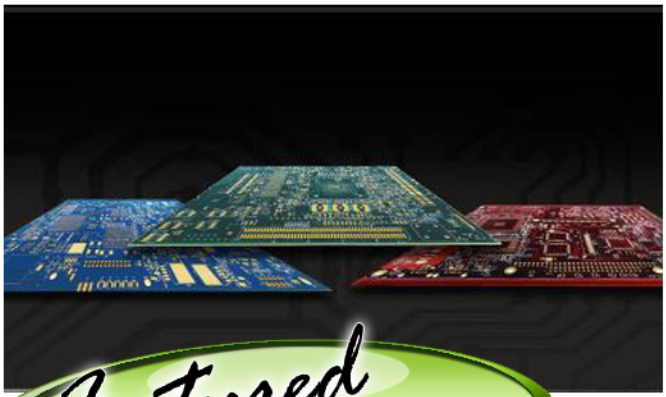
Certifications:	AS-9100, IPC-6012 class 3, ISO 9001 registered, MIL-PRF-55110, UL



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TOP TEN

Recent Highlights from PCBDesign007

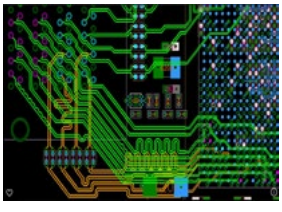
1 Digi-Key Updates Free Design Tools

Global electronic components distributor Digi-Key Electronics has announced key updates to Scheme-it and PCBWeb, two influential design tools in its portfolio. "Digi-Key is continually striving to provide engineers the most up-to-date and innovative design tools in order to support any design needs they may have, from concept to production," said David Sandys, director of digital marketing.

2 Justifying the Need to Outsource Design Work

They work while you sleep? That's just one of the benefits of outsourcing design work to a company like India-based Entelechy Global. Barry Matties met with Mehul Dave and H.D. Shreenivasa to discuss the many ways Entelechy helps their customers worldwide and why outsourcing should not be thought of as a four-letter word.

3 Technology Outlook with Mentor Graphics



Mentor Graphics recently announced the winners of its PCB Technology Leadership Awards. Now in its 26th year, this program provides a great barometer for measuring the newest trends in cutting-edge PCB designs. I caught up with Product Marketing Manager David Wiens and asked him to give us an idea of the trends he's seeing in PCB design and manufacturing, and what the industry has in store for us in the next few years.

4 Innovative Circuits Sees Healthy Medical Market

Medical electronics is one of the fastest growing segments of our industry. Alpharetta, Georgia-based Innovative Circuits is at the forefront of fabricating medical PCBs, both flex and rigid. I asked Innovative Business Development Manager Amir Davoud to give us a solid diagnosis of the world of medical PCBs.

5 ICD Releases 2016 Edition of the ICD Stackup Planner

The ICD Stackup Planner is delivered with an extensive dielectric materials library (DML) containing over 23,300 commonly used rigid and flexible core, prepreg and solder mask/coverlay materials up to 100GHz. This is arguably the most comprehensive list of material properties ever compiled. Using the exact materials that are stocked by your preferred fabricator can increase accuracy by up to 5%.

6 Designers Notebook: Flexible and Rigid-Flex Circuit Design Principles, Part 3

Both adhesiveless copper-clad films and materials relying on lamination with high-temperature adhesives will continue evolve. For example, DuPont, a major supplier of polyimide base materials, is said to have developed high-temperature adhesive technology that combines new polymer systems that significantly improves moisture and chemical resistance. The new material is tougher, exhibits better thermal conductivity.

7 SiSoft and MathWorks Present Design Flow to Create AMI Models from SerDes Design Data

"AMI model development typically occurs only after the SerDes design has been finalized," noted Barry Katz, SiSoft's President and CTO. "AMI models are also generally created by a different group, so some knowledge of the original design intent gets lost in translation. This flow lets SerDes engineering create AMI quickly and efficiently. Reusing SerDes design models for AMI development has been a longstanding, but previously unattainable goal for many design teams."

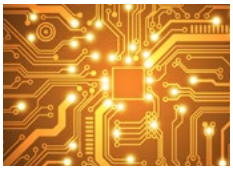
8 The Shaughnessy Report: Doing My Part for Medical Electronics

If you're like me, and most of you are, you've started getting mail from AARP. You exercise, because if you don't, you feel like a fat slob. Your body hurts more often, and you just deal with the pain until it gets bad enough to go to the doctor. This is especially true for men; tough guys like us don't like going to the doctor, unless we've actually severed an artery. Otherwise, we don't need no stinkin' doctors!

9 Cadence's OrCAD Capture Supports Intel Schematic Connectivity Format

Cadence Design Systems' OrCAD Capture now provides export capability for Intel Schematic Connectivity Format (ISCF), targeted at automating Intel-based design reviews. ISCF was developed by Intel to streamline the collaboration process with its customers. Intel worked with Cadence to develop a direct ISCF generation capability in OrCAD Capture to make this collaboration process simpler and more efficient.

10 Enhancing Thermal Performance of CSP Integrated Circuits



In order to meet size and weight requirements, constraints of portable electronic designs often force PCB designers to reduce the size of components and PCB real estate area. To meet these demands, the use of CSP packages to shrink the PCB area needed is a common change in designs. As a result of the reduction of total PCB area, the available options to move heat and route high-power PCB traces is also reduced.

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Events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out The PCB Design Magazine's event calendar.

IPC APEX EXPO 2016
March 13–17, 2016
Las Vegas, Nevada, USA

25th China International PCB & Assembly Show 2016 (CPCA)
March 15–17, 2016
Shanghai, China

2016 Annual Foundation Course (ICT)
April 11–14, 2016
Loughborough, England

Thailand PCB Expo 2016
April 19–22, 2016
Bangkok, Thailand

KPCA Show 2016
April 26–28, 2016
KINTEX, Gyeonggi-do, S. Korea

JPCA Show 2016
June 1–3, 2016
Tokyo, Japan

IPCA EXPO 2016
August, 2016
India

IPC Fall Meetings
September 24–30, 2016
Rosemont, Illinois, USA

SMTA International 2016
September 25–29, 2016
Rosemont, Illinois, USA

electronicAsia
October 13–16, 2016
Hong Kong

Electronica
November 8–11, 2016
Munich, Germany

International Printed Circuit & Apex South China Fair (HKPCA)
December 7–9, 2016
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