THE pcb design MAGAZINE

September 2016

an I·Connect007 publication

John Cardone on Designing Flex for Spacecraft p.12

Flexdude Abides: PCB Design for Satellites p.24

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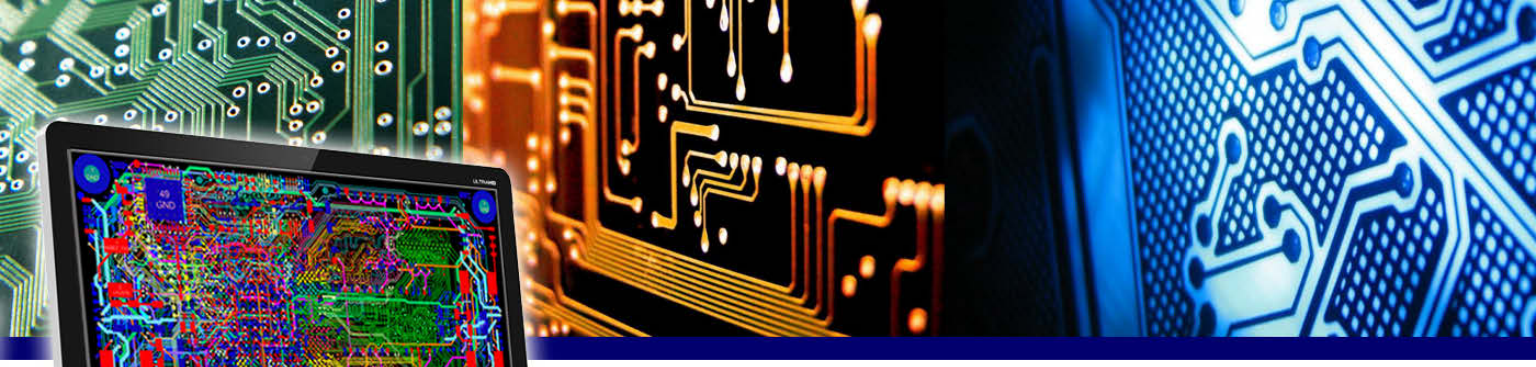

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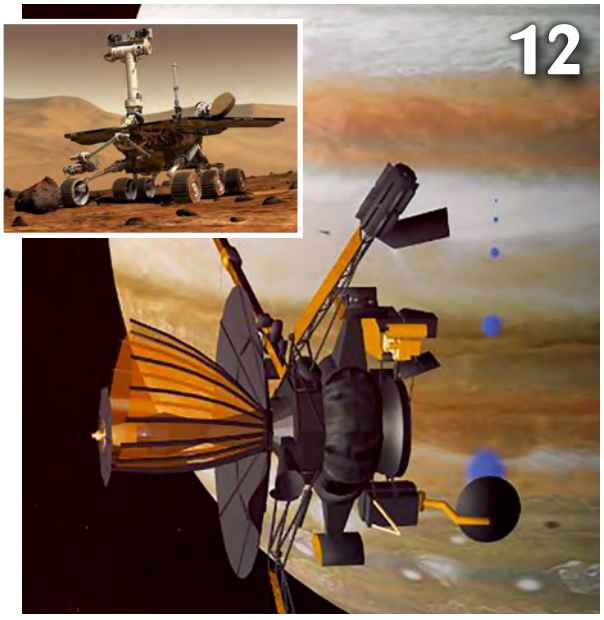
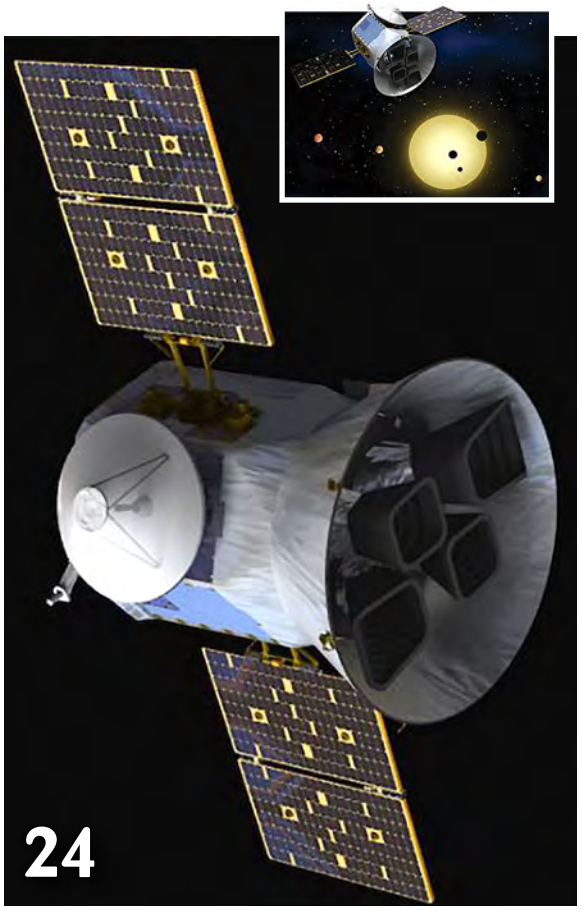
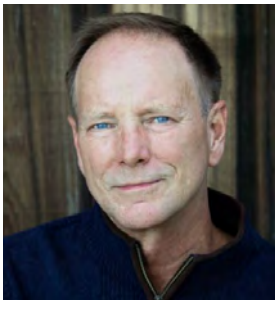


The Aerospace Issue

As *Star Trek* celebrates its 50th anniversary, NASA prepares to map out the rest of the universe, known and unknown. This month, we feature interviews with two veteran PCB designers with spacecraft project experience: John Cardone of JMC Design Services and Tom Woznicki of Flex Circuit Design Company. We also have a great article on thermal PCB design by Continental Automotive's Gabriel Ciobanu and Mentor Graphics' Boris Marovic. Read on!





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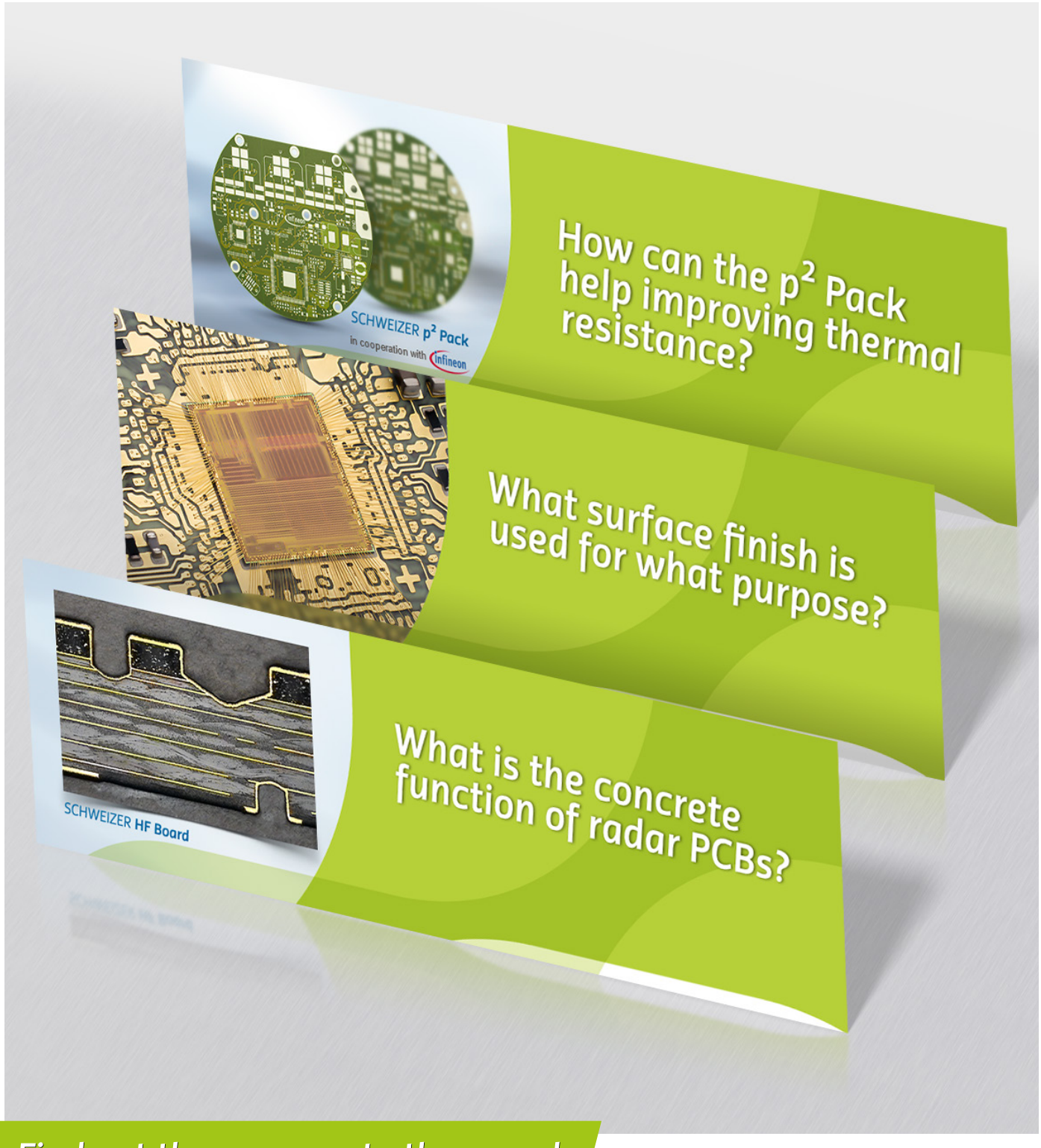

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Space: Still the Final Frontier

by Andy Shaughnessy
I-CONNECT007

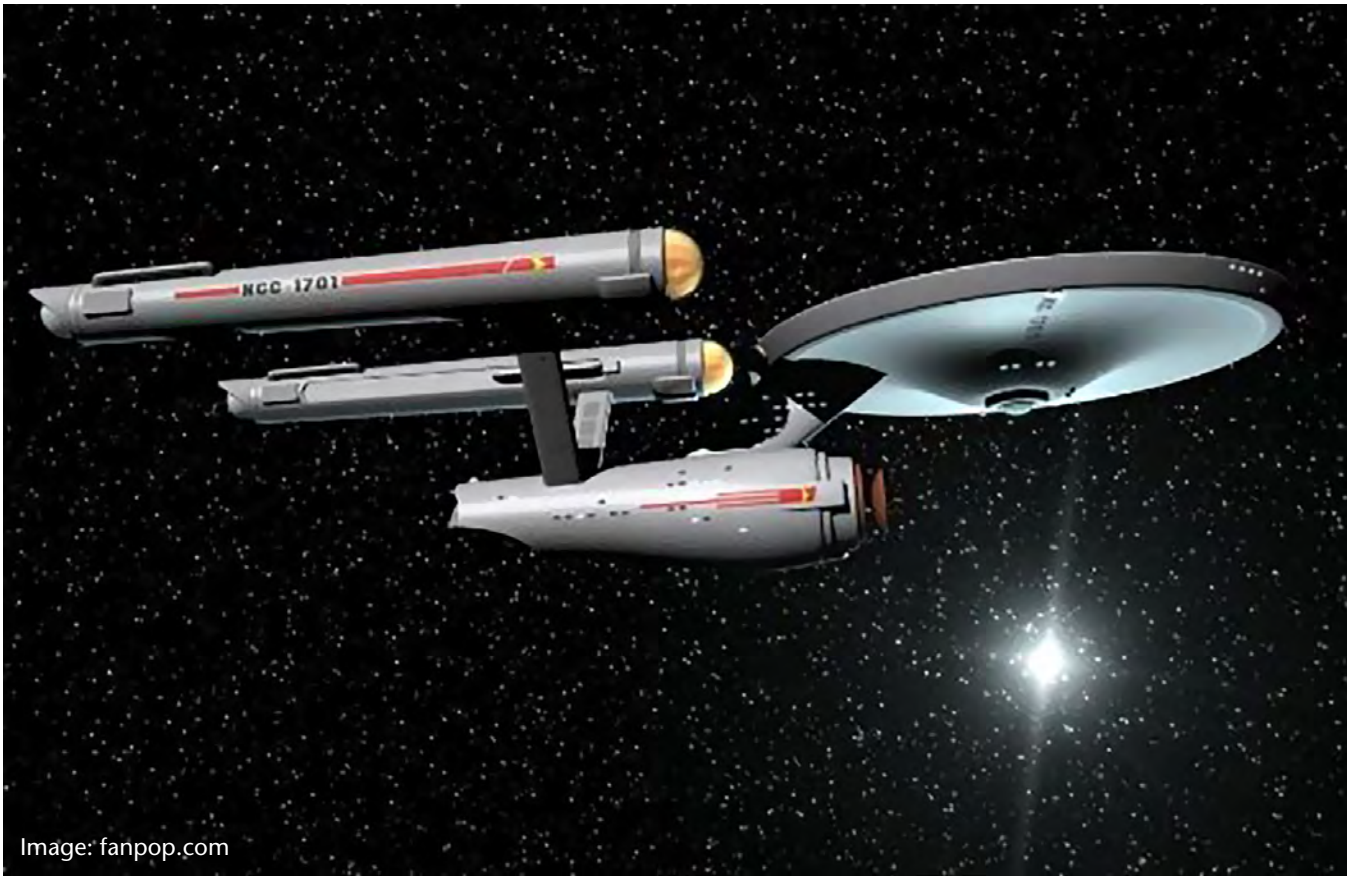
If this doesn't make you feel like a "seasoned citizen," I don't know what will: *Star Trek* first aired 50 years ago, on Sept. 8, 1966. What were you doing at the time? I was probably trying to avoid eating my peas. But I loved *Star Trek;* I thought it was a live TV show that followed a spacecraft.

No one—not even the actors—thought the show would last, and it only ran for three seasons, drawing average ratings. But Captain Kirk and company are more popular than ever on their Golden Anniversary. *Star Trek* tapped into our primal need to know more about our universe.

Much has changed since 1966. Fifty years ago, the U.S. and the Soviet Union were engaged in the Cold War, fighting a proxy war in Vietnam and racing to get the first man on the moon. But later the U.S. partnered with Russia on numerous space missions. I guess you could call our two countries "frenemies" now, which might be the best-case scenario.

Most of the world has abandoned their space programs. But the U.S. plans to keep exploring the "final frontier," even as NASA adjusts to budgetary restraints. NASA is indeed tightening its belt; the agency's $19 billion budget request for the fiscal year 2017 is $300 million lower than the previous year's enacted budget.

That figure still amounts to only about half of 1% of the total U.S. budget. It's difficult to put a dollar figure on the benefits of a space program. Just looking at it from an educational standpoint, I wonder how many young people



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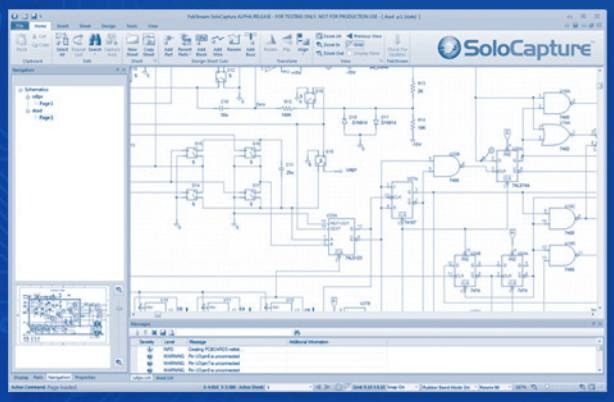

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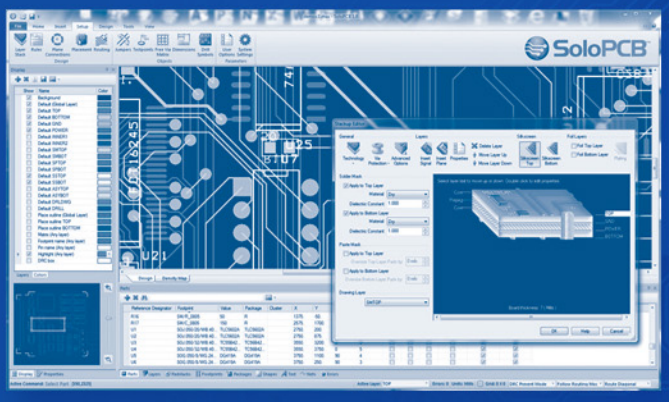

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decided to get a degree in one of the STEM disciplines after following the Mars Rover's progress on NASA's interactive website?

In our own industry, one segment that's evolved in the past 50 years is flexible circuitry. Not too long ago, flex was considered too expensive for most applications. When I first started covering PCB design in 1999, I kept hearing, "Well, flex is cool, but it's just too expensive for us. You don't see flex in many consumer products, except digital cameras and printers."

Now, most PCB design tools include flex design functionality. And flex has turned out to be the perfect circuitry for space applications. It withstands harsh environments, extreme temperatures, and shock, and flex can last a long time.

This month, our first feature is an interview with John Cardone of JMC Design Services. John spent more than 20 years designing flex, rigid-flex, and rigid boards at the Jet Propulsion Lab, and he discusses the flex circuits he designed for a variety of spacecraft, including the Mars Exploratory Rover. Along the way, John gives us a bit of a spacecraft history lesson too. For instance, did you know there are over 4.5 miles of flex circuitry on the rover's robotic arm alone?

Next, Tom Woznicki, also known as the "Flexdude," discusses his recent foray back into the world of rigid PCB design while working on the upcoming TESS satellite. TESS (Transiting Extroplanet Survey Satellite), scheduled to begin its two-year mission in 2017, will monitor more than 200,000 stars, searching for drops in brightness caused by planetary transits. Tom explains how the design team met the shock and temperature requirements without using any unusual materials, and why he doesn't consider rigid design work to be "slumming."

Also on hand is an article by Gabriel Ciobanu of Continental Corporation and Boris Marovic of Mentor Graphics that focuses on improving thermal design, and how proper layout and component placement can have as much effect on thermal properties as thermal vias.

Rounding things out, we've got a couple of great columns by our regular contributors Barry Olney and Istvan Novak, and a new *Sensible Design* column by Electrolube's Alistair Little, who takes the reins from our friend Phil Kinner.

As you probably know, the show season is about to get underway. This month, we are attending PCB West and at SMTA International we will be providing *Real Time with...* video coverage.

If you can't make it to a show, don't worry. We have the coverage you need. See you next month! **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 17 years. He can be reached by clicking here.

Notre Dame Researchers Find Transition Point in Semiconductor Nanomaterials

Collaborative research at Notre Dame has demonstrated that electronic interactions play a significant role in the dimensional crossover of semiconductor nanomaterials. The laboratory of Masaru Kuno, professor of chemistry and biochemistry, and the condensed matter theory group of Boldizsár Jankó, professor of physics, have now shown that a critical length scale marks the transition between a zero-dimensional, quantum dot and a one-dimensional nanowire.

The findings, "Dimensional crossover in semiconductor nanostructures," were published in Nature Communications. Matthew P. McDonald and Rusha Chatterjee of Kuno's laboratory and Jixin Si of Jankó's group are also authors of the publication.

A quantum dot structure possesses the same physical dimensions in every direction while a quantum wire exhibits one dimension longer than the others. Do quantum properties evolve gradually or do they suddenly transition?

Kuno's laboratory discovered that a critical length exists where a quantum dot becomes nanowire-like. The researchers achieved this breakthrough by conducting the first direct, single particle absorption measurements on individual semiconductor nanorods, an intermediate species between quantum dots and nanowires. Single particle rather than ensemble measurements were used to avoid the effects of sample inhomogeneities.

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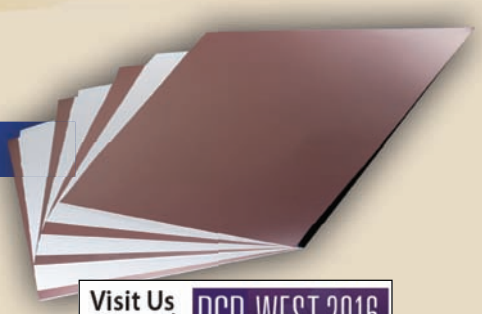

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John Cardone on Designing Flex for Spacecraft

by Andy Shaughnessy

If you watched footage of the Mars rover driving all over the red planet, you're familiar with some of John Cardone's handiwork. He's been designing rigid, flex, and rigid-flex circuitry for spacecraft since he joined JPL in the early '80s, and he's worked on some of the more ground-breaking flex circuits along the way. Now John runs his own design service bureau, JMC Design Services, and he continues to design circuitry for things that blast off. I caught up with John recently and asked him to give us the straight scoop on designing boards for spacecraft.

***Andy Shaughnessy:** John, give us a little bit of background about yourself, and how you got into PCB design.*

John Cardone: My first engineering jobs were with Raypak, where I designed hydronic deicing systems (which looked very much like film heaters on a larger scale), and then Medical Communication & Instrumentation (which coincided with my start at Cal State, Northridge), where I designed my first electronic enclosure, PWBs and flex cable, all on the drafting and light tables with pencil and red/blue tape from Bishop Graphics.

The product I redesigned at MCI (later Biocom Inc.) was a medical communicator, the Biophone 3502, which was a feature of the old '70s TV series "Emergency." You can see the old unit by clicking here. It had miles of wire, stack pole switches, and a gutted Motorola radio behind the front panel. The attached pdf is of the manual for the replacement radio. The second pdf is a copier scan that shows only a portion of the panel flex cable (focal length issue). I took this with me on my CSUN job fair interview with JPL, and as it happens not too many other students had comparable show-and-tell items.

After graduating from CSUN I went to JPL as a mechanical design engineer. At that time JPL was just getting into CAD design and they had three seats of Computer Vision Cadds3 that were kept in a dimly lit closet. My first task (after listening to Cadds3 training tapes, and reading the manuals) was to layout a two-layer PWB used in a PAP smear analyzer. From there I worked in a support role for most of the flight projects that came through our mechanical design group from Galileo on. The drafting tables were slowly replaced by more CAD stations; we transitioned through software revisions, flirted with ProE (until the designer revolt), and settled on Unigraphics NX and Solidworks. PWB design moved from Computervision to Protel, Mentor and Altium. My work focused on electro-mechanical design. This might include light struc-

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ture, electronic enclosures, schematic capture, PWB design (rigid, flex, rigid-flex), and cabling.

John Cardone

***Shaughnessy:** Tell us about JMC Design Services, and what led you to start your own company?*

Cardone: I worked at JPL from 1983-2005. At that time factors all converged to allow my family to make the move to Grenada where we have a small ranch, for the purpose of raising horses. If I could have done that and stayed at JPL I would have, but it's 650 miles away. The next best thing was to contract to them as a remote associate, and this I've been doing for JPL and a number of other clients since 2005.

***Shaughnessy:** So you were at JPL for 22 years, when they were just getting into EDA tools. What were some of the biggest challenges you faced (technical, bureaucratic, etc.) during that time?*

Cardone: When I started at JPL in the design room, they were just getting started in MCAD with CV CADDS3. JPL is a matrix organization, and I am not certain of the state of EDA tools in the sections with an EE focus. It may have been very rudimentary as I do recall creating many schematics and PWBs for the Galileo S/C.

CV was a unique platform because it did it all. You could create an electronics enclosure, add a PWB to it, link the PWB to a schematic net-list from a schematic created in CV, and then place and route the PWB. CV is still being used in the ship-building industry because it is very adept at large assemblies. It was later purchased by ProE, hence its decline and JPL's search for a replacement. I believe that the fact it was being used at the time of my start at JPL fostered my inclination to cross the boundaries that typically exist between mechanical, electrical, systems, thermal, etc. On the MER (Mars Exploration Rover) project I was a member of the mechanical, systems, and electrical engineering teams.

At JPL these were few bureaucratic challenges. It's a marvelous place, and more of a campus environment than a commercial engineering firm. The one challenge I felt is that the vast majority of funding is tied to a specific project, so we could not be a Bell Labs where you have the luxury of playing around until you hit on something. An axiom is that technology used on flight projects must have a high TRL (technology readiness level), and how do you get a high TRL? By being demonstrated on a flight project, of course!

I cannot complain about the progress that EDA tools have made over the years. Having started on a light table, being able to insert or delete a trace with a few clicks is amazing. Even in the early '80s, CV had gate and pin swap, and back annotation. But it was certainly slower. There were many times I babysat a computer overnight as it chugged along. At that time (and today) we were limited in our selection of components because of their fault tolerance and radiation hardness. It was very rare that we spent the mass to radiation-shield a component. It had to arrive at the dock hardened. So, for example, Galileo PWBs were designed with robust CMOS logic in flat packs. We still occasionally use flat packs, and even some DIPS.

The environment: One major concern in both mechanical and EDA design is the severe thermal cycling seen by both earth orbiting and space probes. With mechanical design (which includes printed flex cabling) attention has to be given to the CTE of all dissimilar materials with an interface. This effects bolted joints, necessary machining tolerances, selection and use of potting materials, and on and on. As you know, the X-Y CTE of polyimide has been tuned to be close to that of aluminum, but since it has a ~constant bulk CTE, plated through-holes that see large delta T can crack due to the large difference in the CTE of CU and CTE-Z of polyimide.

Let me focus on PFC (printed flex circuit) for a moment. Its optimal design isn't necessarily the same as in a rigid, or rigid-flex design. Here are a few examples: First, in a PFC, for controlled differential impedance, an off-set broad-

side coupled configuration is much more space efficient, and gives a better transition at the connector interface (less reflection) than using edge-coupled. And in a PWB design edge coupled is most common. This creates challenges that need to be resolved at the PFC-to-PWB interface (it's all about interfaces).

Second, every guide you will see on PFC design will warn that I-beam construction is a no-no. The problem is that a staggered design adds impedance where you may not want it, reduces common-mode noise rejection, and it uses more cable width or allows increased crosstalk between functions. To validate our designs, we conducted life tests with at least 2x needed cycles, under vacuum and temperature extremes. I have five rovers on Mars (one Pathfinder, two MERs and two MSL rovers) and each has far exceeded its required life.

Third, as the Mars rover designs have progressed, the PFC challenges have gotten increasingly more strident. From Pathfinder to MSL, PFC cable lengths have increased to more than 10m, with full end-to-end cable lengths of ~15m. The longest cable runs transition from PFC inside the rover, to round wire outside, to flex over a 5 DOF (degree of freedom) robotic arm, back to round wire for a transition at the arm end, then to flex in a rolling loop on the drill mechanism, to a final wire segment to the motor. In this example of the drill rotation motor, the requirement was <0.8 ohm one-way. We met the requirement, and for the upcoming M2020 project we're on track to improve upon it (and to reduce the trace-to-chassis capacitance which was found to introduce some noise into the encoder reading). Oh, there's another challenge. How do you put noisy motors, heater, brakes (yes there are holding brakes) and quiet encoder, temperature, and data telemetry on the same cable? By the way, there are more than 4.5 miles of printed flexible circuitry in the rover's arm alone.

***Shaughnessy:** Tell us a little more about your work on the MER. What were some of the unique issues you encountered on that project?*

Cardone: To tell you about MER, I'll need to start with MSR (Mars Sample Return). I was part of a small pre-planning team that was outlining the configuration for this mission. At some point NASA decided that returning a sample to Mars orbit, by a rover to be eventually picked up by another spacecraft, was too ambitious. As a side note, M2020 will be preparing and packaging samples, for eventual return to earth. I haven't looked into how they plan to do this but the plan might be up on jpl.nasa.gov.

From that context MER began. A number of mechanical designers were co-located. Designers do little "engineering" and they generally work for many Cognizant Engineers. A CogE would be responsible for an element of a project, attend budget meeting, contract design, analysis, fabrication people, etc., while the designer drives the development of the CAD model and the documentation. I managed the design of all things inside of the Rover body, another managed the rover exterior, another the mobility system, robotic arm, mast cam, etc.

Because I started with the MSR team, I came into the MER project with a viable configuration concept. The MER rover body is essentially an ice chest. Inside it is something like a 6U VME chassis. The front and back of this chassis supports stuff like the UHF and X-band components, the redundant batteries, inertial measurement units, and the cable tunnels. The cable tunnels are insulated serpentine pathways that provided thermal isolation for the rover's wiring between this chassis and the

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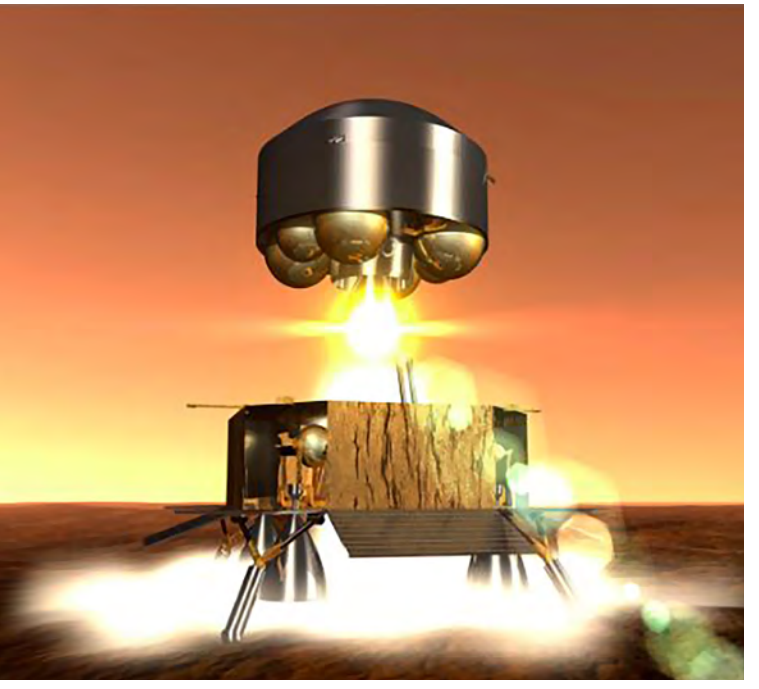

rover exterior. From there the wiring goes to all of the actuators and instruments.

For the rover's internal wiring, I developed a 4-layer printed flex cable construction (two conductors, two Faraday shields) with edge launched micro-d connectors. I think there were 50 flex cables in the front and rear cable tunnels, each about 1m in length. The only round wires exiting the rover were a couple of RF lines to the antenna, ~20 pyrotechnic lines, and a couple of others due to last-minute changes. This saved considerable mass, volume and, most importantly, it reduced our thermal leakage. The thermal leakage related directly to needed heater power and solar panel size, and operational constraints; for example, how long to heat up before we can do science?.

In addition to this, I also created the rover wiring diagram, and the flex cable designs for the robotic arm (seven cables up to 3m in length), panoramic camera mast (seven cables up to 1m in length), high-gain antenna (HGA—three cables up to 1m in length), and the mobility system (six cables up to 1.8m in length). The mast used a COTS twist capsule, the arm and the HGA used its continuous flex in custom twist capsules, and the mobility had a one-time deployment of a rolling fold for the telescoping structure.

The biggest challenges were:

A) There was some bias against flex because it is considered too costly, impossible to modify and comes with a long lead time. Our first big use of flex was two impossibly complicated and expensive 30+ layer rigid-flex circuits that I designed for the first rover, Pathfinder. I still hear the same bias on each successive program, and on each program printed flex cables are an enabling technology that allows them to meet the mission goals.

B) I spent a great deal of time negotiating with instrument and electronic designers over pin-out designs that would enable efficient use of flex. For the 100 ohm differential stuff, it means talking them into broad-side instead of edge-coupled (not a huge deal for them since the electronics generally used wire between the connector and PWB. This gives thermal compliance between the PWB and the chassis, and doesn't overly constrain or stress the solder joints). We also segregated noisy stuff to one edge, and quiet to the other and placed shield line between.

C) Controlled impedance. The flex cables used Dupont AP material and acrylic adhesive. To hit the 100 ohm differential I can reduce trace width, but I need to stop at some point to maintain the robustness of the trace (12 mils), increase the offset distance, but this needs to be kept as small as possible or the coupling will shift to through the shield layer and it eats up finite cable width resources (~24mils), and I can increase the distance between the trace layers and the shield layers, but this increases cable stiffness, increases needed twist capsule diameters, and static bend radii (~12 mils).

D) I created flat patterns for each of the cables by modeling them in their flight configurations, and then flattening each design using the sheet metal module in CV Cadds4.

When it was all done, I think it came together pretty well. Its original mission was supposed to be 90 sol (one Martian day). I don't recall exactly how long they ran them. I think it was over five years, and that they were still mostly operational when they decided to stop the operational funding. You will always need to check me on mission facts. I'm a design mer-

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cenary, and have moved on to a new project by the time something has launched. I'm one of 20 JPL engineers listed on a patent (USD487715) for the "ornamental design" of the MER.

Shaughnessy: *It's interesting that you designed everything inside the Rover body, and your patent is for "ornamental design." Do you have any other patents?*

Cardone: I managed the rover interior design, meaning that I took the designs of others and configured them within the rover. The electronic packaging concept was in a large part mine, but I did not do the detail design of the PWBs, chassis, RF components etc. The only detail design I did inside the rover was the wiring, flex cables, a few pieces of secondary structure, and the cable tunnels. I'm not a lawyer, so don't know the ins and out of patent law, but I think a partial reason for the patent was so that it could be licensed to LEGO.

I'm a co-author of one other patent for a novel electronic packaging method (US 6206705 B1) which I helped develop for a micro-spacecraft study at JPL, and that I used on the JASON spacecraft. There was some interest in it, but I don't think it was ever licensed. At least I never received any checks in the mail. It used AMP elastomeric connectors, which were a piece of flex with parallel conductors on it, which was wrapped around a piece of silicon. All connectors are composed of a spring and a contact. With these the flex was the contact, and the silicon is the spring.

Shaughnessy: *You mentioned a "bias" against flex. It was like that until recently, but now we're seeing flex everywhere. Why do you think flex has become so popular lately?*

Cardone: Projects have review hurdles they all have to cross (early peer reviews, preliminary design review, critical design review, and detail design review), and without fail someone will submit an action item to justify the schedule impaction, cost, etc., of using flex over traditional cabling. The fabrication cycle of a typical JPL PFC is about six months. And on the surface this is longer than a typical round wire harness, but it doesn't account for the downstream time savings. Another weak link for us is the limited vendor pool for fabrication. Because of the panel size needed we get a lot of no-bids. We have one vendor that's been working with us since Pathfinder (that >30 layer rigid-flex I mentioned before), and they have been great. So the bias I mentioned is at a project level where they are looking solely at project risk.

I've been using flex, rigid-flex throughout my career, and I consider it just one tool in the box. If I think it's the right tool I push for it, and if not I don't. If it is becoming more popular then this would have to be due to improvements in fabrication, and resulting cost reductions. Some of it may also be due to reduced end-item assembly costs. Perhaps skilled labor, for end-item assembly, is less available or more expensive.

Shaughnessy: *What were the smallest and largest flex designs you've done? What was the most interesting?*

Cardone: The smallest flex I've designed was an R&D project to interconnect 4 MEMS accelerometers. The line widths were 0.025mm, leg widths are 3mm, and the overall size is about 9mm x 8mm. The three legs allowed the unit to fold up in to a pyramid shape so that it could measure acceleration in all three axes.

The largest flex designs I've done are probably the robotic arm cable for the MSL rover. They are on the order of 10m in overall length, and they are three cables designed to 24" x 85" fabrication panels (limitation of the lamination

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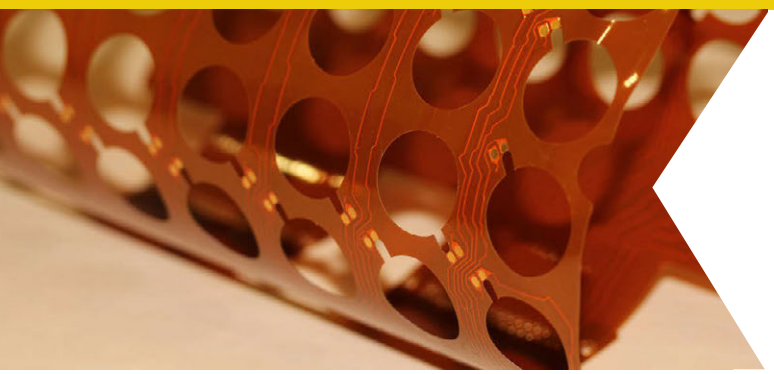

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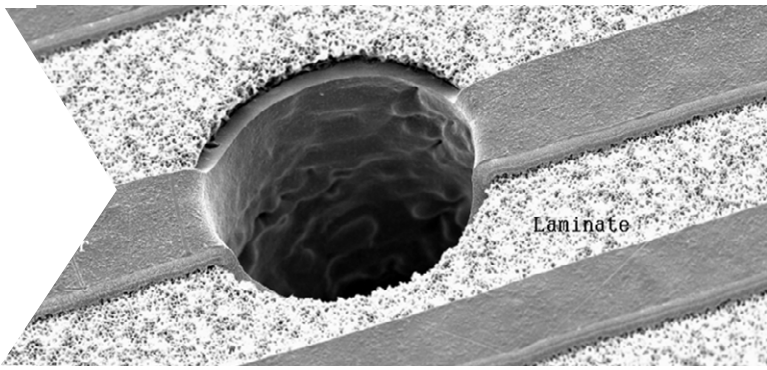

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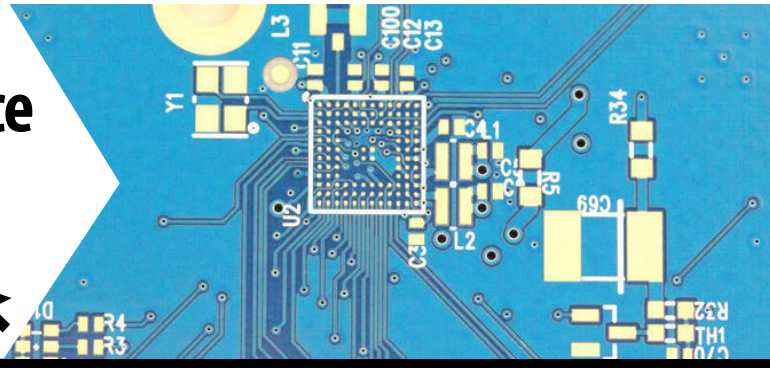

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press) that are spliced together. Another very large flex I did was a phased array antenna that was designed to deploy on an inflatable frame on orbit.

Another large flex circuit design was a prototype heater for HP. It wasn't huge, but it was jam-packed with eight heater zones and over .23 miles of conductors. The goal on this design was to maximize distribution, and then adjust the trace width for the desired resistance.

My most interesting flex design was probably a rigid-flex I did for Panavision. The center segment supported the CCD sensor, and four legs folded down, enveloping the lens stack to support the other electronics. Or it may have been some circular phased patch array antennas I did at JPL. These were about 3m in diameter and were filled with tuned RF elements on about a 1/4" grid. Each element was "tuned" by adjusting the length of the two RF stubs that came out of it. Each element's stub length depended on its location on the array. I designed these with Computervision Cadds4 by constructing an executable file that placed polygons at each location based on an input file from the antenna engineer. It doesn't sound interesting, but when it was done, you could discover some beautiful patterns.

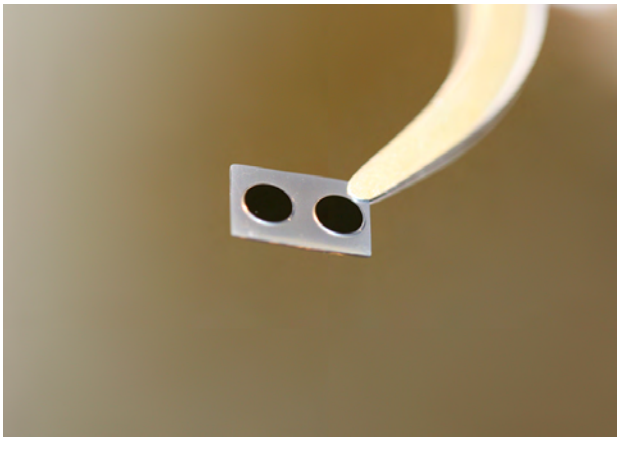
Shaughnessy: *I understand that you may have designed the first flex ever used at JPL. Can you tell us about that?*

Cardone: I am not certain this was the first use of flex at JPL. It is the first one I was aware of. For the Cassini mission we designed a flex that adapted a sub-d connector to surface mount interface at the PWB. Its construction was a 3 oz. layer of Cu or BeCu sandwiched between polyimide layers. The connector interface was through-hole, and the PWB interface was unsupported flying leads of the BeCu that exited the sandwich. The flex exited the connector pin array in both directions to allow maximum trace width, and keep the flex to one layer. The flex leg near the PWB had a 90 degree turn, the leg away from the PWB had a 180, and then a 90 degree turn. The end result was that we only took up about .55" of PWB area, while a round wire interface might have taken twice that.

Shaughnessy: *Thanks for talking with us, John.*

Cardone: Thank you. **PCBDESIGN**

New Breed of Optical Soliton Wave Discovered



Applied scientists led by Caltech's Kerry Vahala have discovered a new type of optical soliton wave that travels in the wake of other soliton waves, hitching a ride on and feeding off of the energy of the other wave.

Solitons are localized waves that act like particles: as they travel across space, they hold their shape and form rather than dispersing as other waves do. They were first discovered in 1834 when Scottish engineer John Scott Russell noted an unusual wave that formed after the sudden stop of a barge in the Union Canal that runs between Falkirk and Edinburgh. Russell tracked the resulting wave for one or two miles, and noted that it preserved its shape as it traveled, until he ultimately lost sight of it.

The microcavities that Vahala and his team use include a laser input that provides the solitons with energy. This energy cannot be directly absorbed by the Stokes soliton—the "pilot fish." Instead, the energy is consumed by the "shark" soliton. But then, Vahala and his team found, the energy is pulled away by the pilot fish soliton, which grows in size while the other soliton shrinks.

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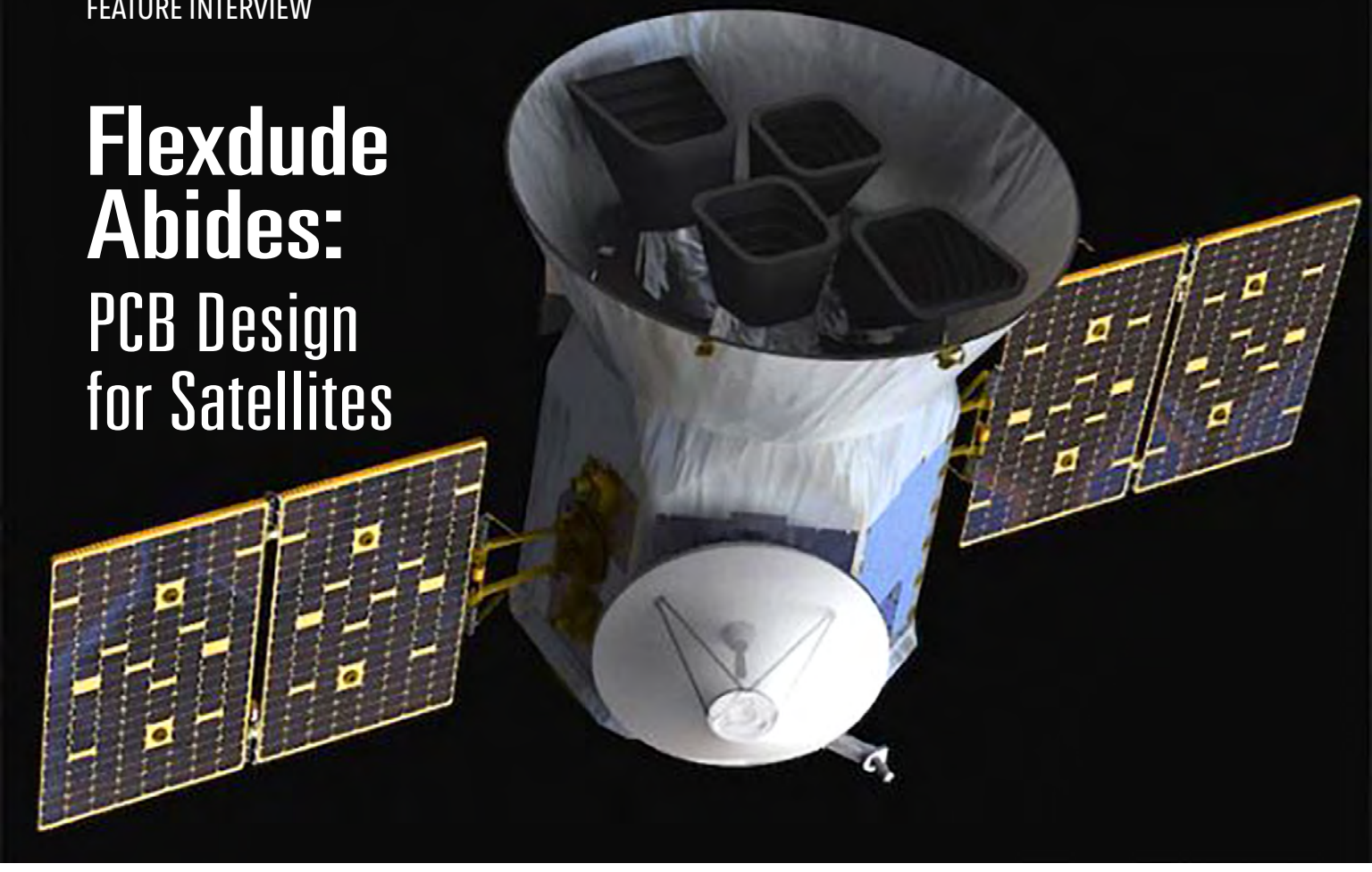
Flexdude Abides: PCB Design for Satellites



by Andy Shaughnessy

Tom Woznicki has made a career out of his love for designing flex circuits. Woznicki, also known as "Flexdude," has focused primarily on flex circuit design since he founded Flex Circuit Design Company in the 1990s, and he designed flex circuits for the Mars rover. But recently, Tom found himself designing rigid PCBs, this time for the TESS satellite. I tracked Tom down via email recently and asked him to discuss his work with TESS, and what it's like switching between flexible and rigid PCBs.

Andy Shaughnessy: ***Tom, give us a quick thumbnail sketch of your background and your company.***

Tom Woznicki: I almost exclusively design flex circuits and rigid-flex circuits. I have been in the flex industry since 1988 and started my company, Flex Circuit Design Company, in 1992, coming up on 25 years ago! I am a mechanical engineer by education, which I believe really helps me understand the intricacies of flex circuits; they are as much mechanical as electrical. In fact, most flex circuits are electrically simple, but mechanically complex.

Shaughnessy: ***Now, you're more identified with flex design, but I understand you designed rigid boards for the upcoming TESS satellite. Tell us about that project.***

Woznicki: Yes, for the past two years I have been part of the team working on the TESS satellite. The principal goal of the TESS mission is to detect small planets with bright host stars in the solar neighborhood. I actually designed the early prototype and development PCBs and worked in a support role in the designing the flight boards that are now assembled and in testing.

How did it happen? Once in a blue moon, my flex circuit customers need me for rigid board design help; they need something fast and their PCB designers are busy, or they don't know any PCB designers and would prefer to work with someone they know. Most times it's small test

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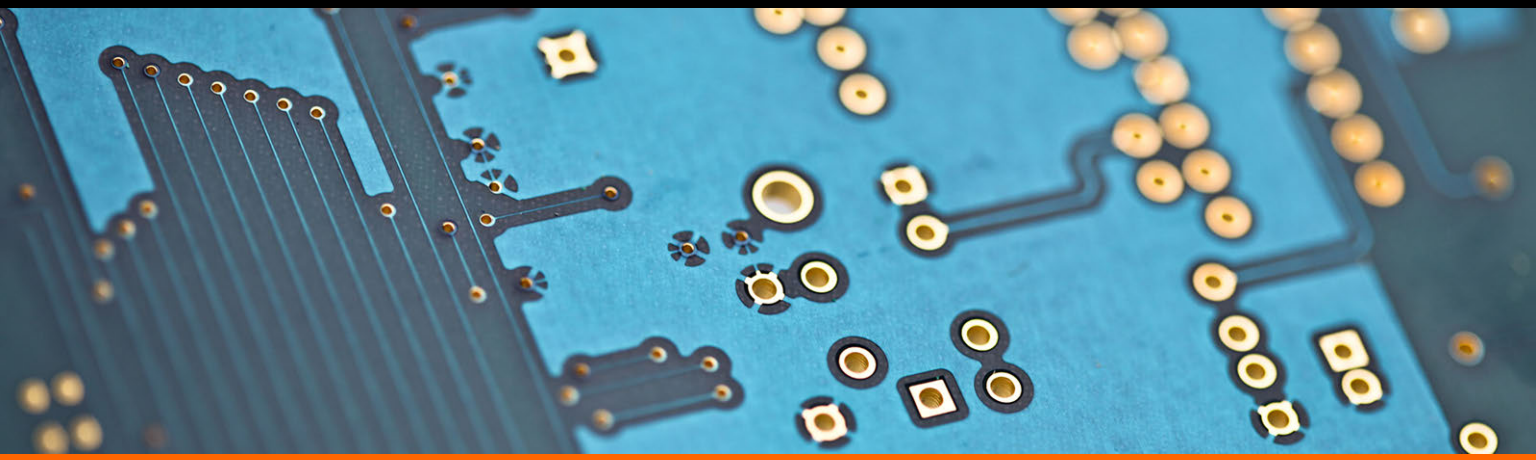

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SUNSTONE CIRCUITS

Tom Woznicki, aka "Flexdude."

boards or interposers, but sometimes it's bigger. As long as we're working with Cadence Allegro or Altium I'm good. (One of the sales reps for Cirexx kids me whenever she sees one of my rigid board designs. "So, you're slumming again, designing PCBs?")

TESS began in a similar way. One of my flex design customer supplies the camera detectors for the project, and they asked if I could help. A TESS scientist had designed the first prototype PCBs on a Mac using a program called Osmond, and they needed someone to bring the design into a mainstream CAD tool and make some changes to that initial design. As I dug into the design changes, it turned out they needed a complete redesign, and of course they needed it in a hurry. I completed that design—it worked fine. Then they asked me to design a microprocessor evaluation board, and after that a spin of the two prototype revisions of the satellite PCBs.

And these satellite boards were very challenging designs—over 1,000 components each and very specific shapes to the copper planes. A whole different world (pun intended) from flex circuits! For the third round of prototypes, the designs were transferred to a service bureau with a lot of experience in mil/aero PCB design and designers that had CID certification. I continued to help as a liaison between the TESS folks and the service bureau, transferring the design information and helping review the finished board designs. I also designed a couple of test boards for the scientists to evaluate the flight boards. The satellite itself is scheduled for launch in 2018.

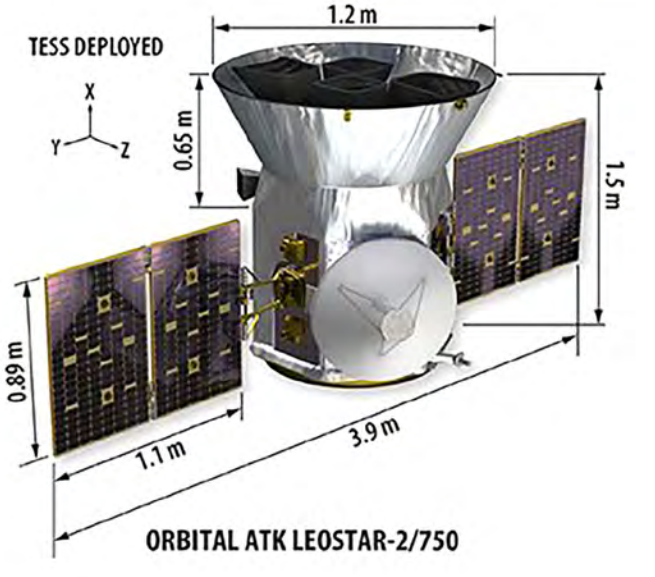
Looking back, it was as if I had taken a nine-month sabbatical from flex designing; it consumed almost all my time from September 2014 to July 2015, and it's been part-time since then. It was definitely a fun experience working with some incredibly smart people.

***Shaughnessy:** What are some of the unique challenges that come with designing boards for space applications?*

Woznicki: The workmanship standards specified was IPC-6012 class 3A, which has very challenging via requirements: 1.5 mils plating in the barrels and a minimum 2 mil annular ring on inner layers. We weren't able to use very small vias, even though we had to fit lots of components onto the board.

***Shaughnessy:** How is a board for a satellite different than any other high-reliability board?*

Woznicki: You have to keep in mind the very cold temperatures of space as well as the shock and vibe of the rocket launch. In many ways, the design techniques we use in flex circuitry apply. I'm always looking at the trace layout to see if there is anything that might cause a trace or solder joint to crack under temperature cycling or actual physical flexing as the board vibrates. So adding teardrops at vias and plated holes and running small traces out the corners of SMT pads where possible so as not to create stress concentrators help the board be more reliable. I also try to do as much signal routing as possible on interior layers to protect them if the board flexes, just like we try to keep traces near the neutral axis in flex design.



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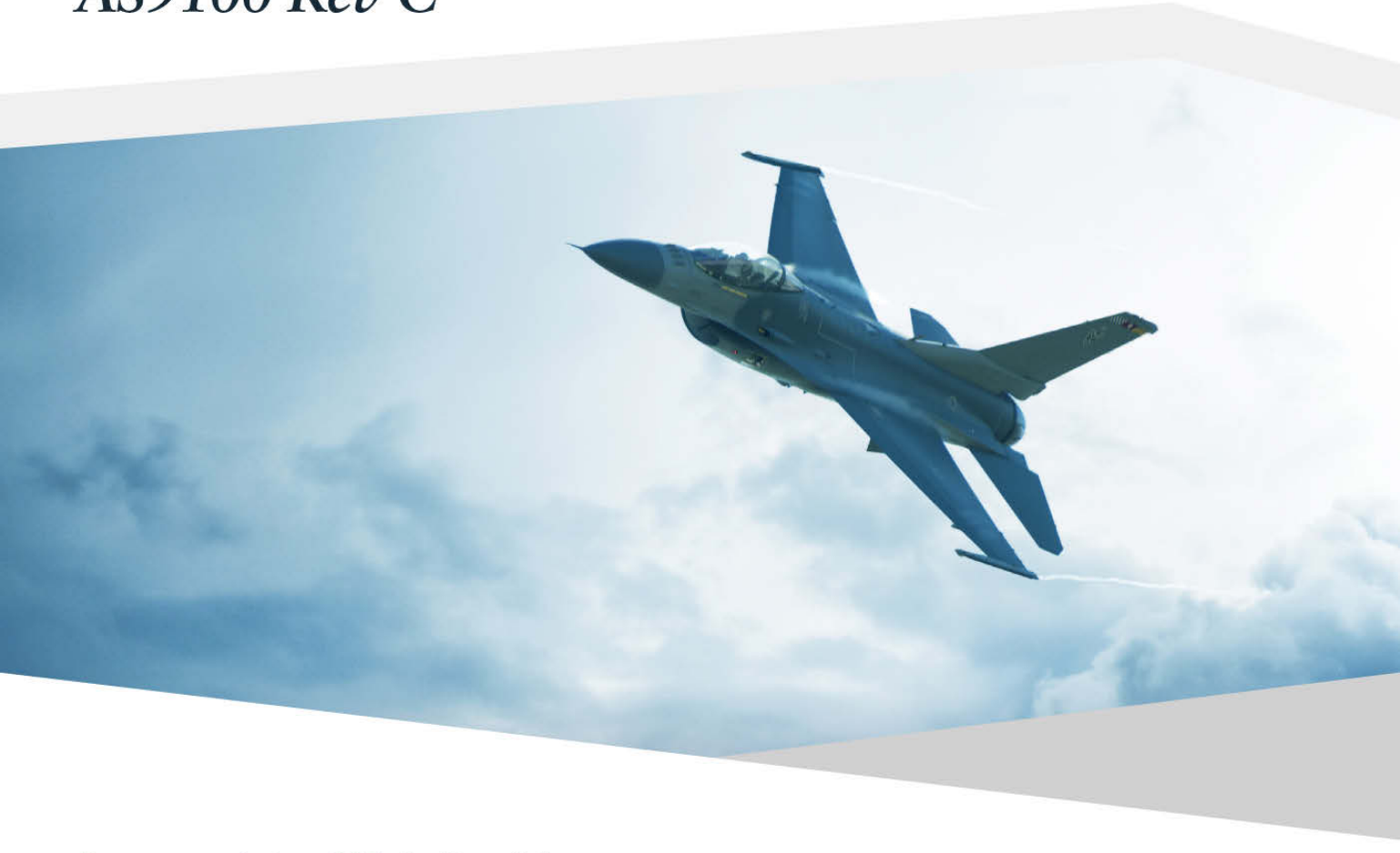

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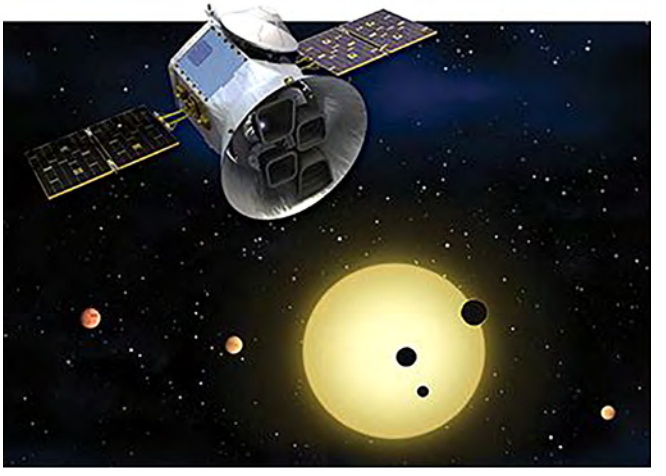


Shaughnessy: *What sort of technologies and materials did you deal with, if you can talk about that?*

Woznicki: Fortunately, we were able to meet the system requirements without any unusual materials or technologies. We did need blind and buried vias, but not stacked vias.

Shaughnessy: *In one survey, our military and aerospace designers said they have trouble with data and specs—inaccurate data, not enough data, confusing specs, and unclear requirements. Did you encounter any of these issues?*

Woznicki: Yes, I did. Flight components sometimes have oddball sizes and packages: 0505 resistors, transistors in UB packages, etc. Spec sheets don't have recommended footprints and the tech support from vendors was slow or non-responsive.

Shaughnessy: *So are you back designing flex now?*

Woznicki: Yes, I'm back to designing flex circuits.

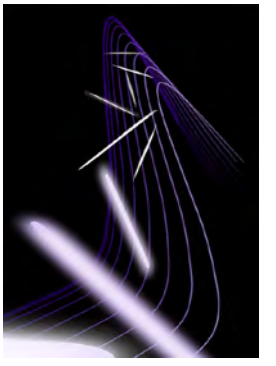
Shaughnessy: *Is there anything else you'd like to add?*

Woznicki: There were many times I'd think, "Can I really do this? I'm not a rigid board designer." But good design techniques work! To build on the experience I got my CID certification last year, and I'll be taking the CID+ test later this month.

Shaughnessy: *Great. I appreciate your time, Tom.*

Woznicki: Thank you, Andy. **PCBDESIGN**

New Perovskite Research Discoveries May Lead to Solar Cell, LED Advances



"Promising" and "remarkable" are two words U.S. Department of Energy's Ames Laboratory scientist Javier Vela uses to describe recent research results on organolead mixed-halide perovskites.

Perovskites are optically active, semiconducting compounds that are known to display intriguing electronic, light-emitting and chemical properties.

Scientists found that depending on how the material is made there can be significant nonstoichiometric impurities or "dopants" permeating the material, which could significantly affect the material's chemistry, moisture stability and transport properties.

The answers came via the combination of the use of optical absorption spectroscopy, powder X-ray diffraction and for the first time, the advanced probing capabilities of lead solid-state NMR.

"We were only able to see these dopants, along with other semicrystalline impurities, through the use of lead solid-state NMR," said Vela.

Another major discovery scientists made was that solid state synthesis is far superior to solution-phase synthesis in making mixed-halide perovskites. According to Vela, the advanced spectroscopy and materials capabilities of Ames Laboratory and ISU were critical in understanding how various synthetic procedures affect the true composition, speciation, stability and optoelectronic properties of these materials.

"We found you can make clean mixed halide perovskites without semi-crystalline impurities if you make them in the absence of a solvent," Vela said.

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PCB007 Highlights

Shane Whiteside and Summit Interconnect: Aspiring to New Heights

A few weeks ago I was privileged to meet with Shane Whiteside in Anaheim, California, at KCA Electronics. Whiteside, former COO of TTM, has helped launch a new company—Summit Interconnect— which encompasses the recent acquisition of KCA Electronics and Marcel Electronics International. Once again assuming an executive role, this time as CEO and president, Whiteside shared his story, strategy and vision for this new chapter.

Karl's Tech Talk: Digital Imaging Update

Through the years, I have repeatedly covered and updated digital imaging in this column, from as far back as 1997 in CircuiTree, through a column in this magazine in November 2015. Several reasons for this extended coverage include the fact that technology had a slow, long incubation time that eventually led to accelerated improvements and acceptance for mass production.

Happy's Essential Skills: Project/Program Management

No matter what your job, you may have to manage, or play an active role in, a project at some point during your career. It takes a great deal of skill to do this well, but the time you invest in building good project management skills can pay off enormously.

A Day with Pete (Starkey)

Usually the one conducting the interviews, I-Connect007's own Pete Starkey recently found himself on the other side of the microphone when I spent time with him in his hometown of Market Bosworth, England. There, between hiking and gardening, we found time to discuss Pete's rich history in the PCB industry and the many changes and surprises he's seen in the manufacturing process over the years.

FTG: Focus to Expand

Firan Technology Group (FTG) is a Canadian circuit board and cockpit product manufacturer. With a newly established global footprint, they look now to grow within that footprint, particularly by way of acquisition. I-Connect007's Judy Warner and Barry Matties met CEO Brad Bourne at FTG's Chatsworth, California facility to learn more about the acquisitions, their success in China, and the overall challenge of working in the aerospace and defense market.

IPC Releases Final 2015 PCB Market Size Estimates and Growth Rates Report

The North American PCB Market Report, published last week by IPC, reported IPC's final estimates of 2015 market size for rigid PCBs and flexible circuits in North America. Although North American PCB production decreased 4.3% in 2015 to $2.9 billion, the PCB market grew 1.4% to an estimated $3.4 billion.

All About Flex: Considerations for Impedance Control in Flexible Circuits

Impedance can be thought of as a system's opposition to alternating or pulsing electronic current. The unit of measurement is ohms, the same unit of measurement in a direct current system. However, the components for calculating impedance are much more complex than DC resistance.

Weiner's World

This month's column has a higher percentage of IC coverage than normal for several reasons. The end of Moore's Law regarding transistor scaling will be dead by 2021 as will be replaced by 3D integration according to the International Technology Roadmap for Semiconductors (ITRS).

Inside Spirit Circuits

I was recently treated to a factory tour with Spirit Circuits' Managing Director Martin Randall, to learn more about their process line and how it has evolved over time. In the discussion following, I learned about Spirit's involvement in the China market and how they've structured their business to handle quick turn prototypes locally and high volume abroad.

Congressman Scott Peters Tours TTM Technologies' San Diego Facility

Today, TTM Technologies Inc. held a town hall-style discussion with Congressman Scott Peters (D-CA-52) on the legislative issues impacting the manufacturing industry. Executives and employees of TTM gave Congressman Peters a first-hand look at the work taking place in their San Diego facility.

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How to Handle the Dreaded Danglers, Part 2

by Barry Olney
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In Part 1 of this series, I deliberated on how dangling via stubs distort signals passing through an interconnect and also decrease the usable bandwidth of the signal. This is due to the via stub acting as a transmission line antenna, which has a resonant frequency determined by the quarter wavelength of the structure. The conventional solution to this problem is to back-drill (or control depth drill) the vias to bore out the via stub barrels, so that the via stubs are reduced in length if not completely removed. This month I will look into all the possible solutions to alleviate this issue.

1. Back-drill the Stub

Back-drilling is a process to remove the stub portion of a plated through-hole (PTH) via. It is a post-fabrication drilling process where the back-drilled hole is of larger diameter than the original PTH. This technology is often used instead of blind via technology to remove the stubs of connector vias in very thick high-speed backplane designs. State-of-the-art board fabrication shops are able to back-drill to within 8 mils of the signal layer, so there will always be a small stub portion attached to the via.

High-speed, SERDES, serial link-based backplanes generally have thick substrates. This is due to the system architecture and backplane to card interconnect requirements such as press-fit connectors. Back-drilling the via stub is a common practice, on thick PCBs, to minimize stub length for bit-rates greater than 3Gbps (1.5GHz). However, at transmission rates >10Gbps (5GHz), back-drilling alone may not be adequate to reduce jitter and bit error rate (BER).

Figure 1 shows the effects of excessively long via stubs on a high-speed differential pair. On the left, the differential pair is simulated using a pseudo random bit stream (PRBS) with lossy transmission lines enabled; note the open eye pattern. However, on the right, I had included via modelling, which enables the via parasitics and highlights the effects of via resonance. The high-frequency harmonics are attenuated, rolling off the signal rise time,

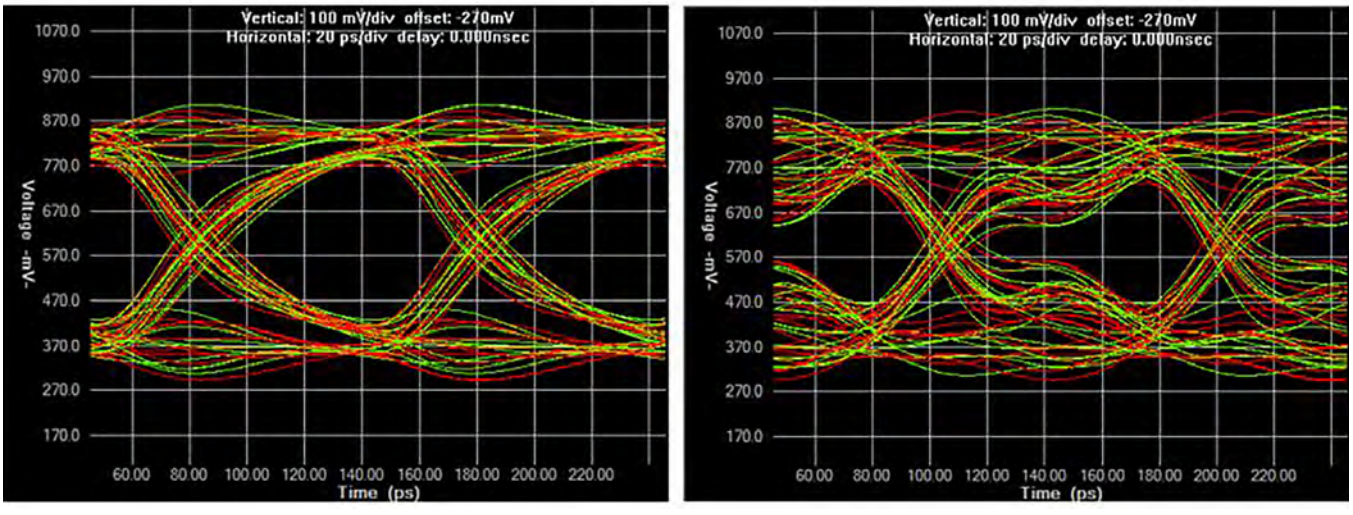

Figure 1: High-speed differential signal with via resonance (simulated in HyperLynx).

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distorting the signal, reducing bandwidth and closing the eye.

Vias can appear as capacitive and/or inductive discontinuities. These parasitics contribute to the degradation of the signal as it passes through the via. At high frequencies and with thick backplane substrates, it is imperative that these issues are addressed.

Back-drilling typically requires specialized equipment, and further requires that the back-drill be precisely located over the vias. As such, the back-drilling process, especially two sided back-drilling, is expensive due to drill breakage and yield issues and is very time-consuming.

2. Blind and Buried Vias

Blind vias connect the outer microstrip layers to one or more inner stripline layers and may have a central reference plane between the signal layers providing a very low inductance return path. The holes are laser drilled and are typically 3-4 mils diameter. Blind vias behave like a lumped capacitor with very little inductance. And because the microvia hole is very small, it has less capacitance than a standard PTH via.

On the other hand, buried vias are used to make connections between the inner stripline layers only and may have short stubs. They have more capacitance than a standard PTH, being typically 8 mils diameter, but may still have a short stub that cannot be back-drilled from top or bottom. They may not be appropriate for high frequency design.

3. Remove Non-Functional Pads

Non-functional pads are pads on internal layers that are not connected to any signal or plane on that layer as illustrated in Figure 2. There is an ongoing debate regarding the influence of non-functional pads on PCB reliability, especially as related to barrel fatigue on PTH vias with high aspect ratios. The primary reason is to improve the fabricators' processes and yields as it helps manage Z-axis expansion of the board due to coefficient of thermal expansion (CTE) stresses. There is also the possibility of a short-circuit, to a plane, due to a gap in the prepreg fill, when no pad is present. However, removing non-functional via pads reduces via capacitance

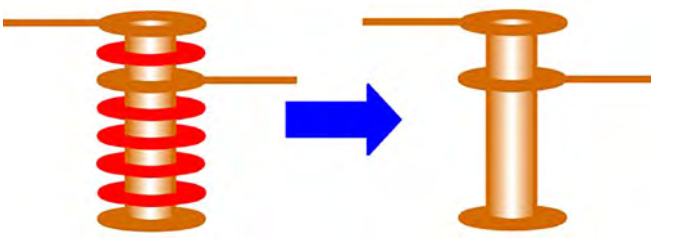

Figure 2: Non-functional via pads are removed on the right.

by approximately half, which in turn, increases impedance. So from a signal integrity point of view, this is a positive. But, check with your preferred fabricator before implementing this.

4. Increase the Antipad Diameter

If you follow the IPC standards, then an antipad should be 20 mils larger that the via pad diameter. However, this is not always possible (in fact very rare) in a densely packed multilayer PCB using fine pitch BGAs. For an 8 mil via hole, the pad is typically 16 mil with an antipad of 26 mil. This allows a 9mil clearance around the pad, resulting in high plane to via capacitance. Increasing the size of the antipad, also reduces capacitance but at the same time, may well make Swiss cheese out of the reference plane. This increases the DC drop and reduces the amount of instantaneous current available to simultaneous switching devices, which is highly detrimental from a power integrity perspective.

Another alternative, that may not be very practical, is to back off the clearance to the plane, on the stub section of the via, reducing capacitance. However, this would have to be implemented manually in the PCB tool and would leave the planes, in the stub section, with wide holes reducing the effect of a solid reference plane.

So if increasing the size of the antipad is not advisable, then creating an oblong antipad may be a compromise. An oblong antipad still reduces the parasitic capacitance significantly. But at the same time, it allows the return current to flow directly between the vias to reduce loop inductance and preserve the continuity of the reference plane. Most PCB design tools will

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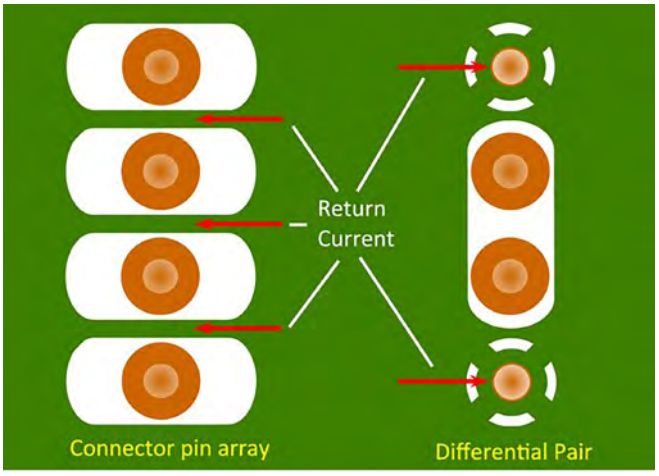

Figure 3: Oblong antipads reduce via capacitance.

allow the definition of an oblong antipad on internal layers.

Where differential pairs are present, an oblong antipad can be placed around both pairs (see Figure 3) to reduce the via-to-plane capacitance. A ground stitching via should be positioned at either end of the oblong antipad to reduce return path inductance. With connector pin arrays, the oblong clearances also preserve the continuity of the current return path in the reference plane.

5. Terminate the Stub

The via stub acts like an unterminated transmission line. If a terminating element is placed at the bottom end of the stub, then the reflection of the stub may be minimized. The impedance terminating element may include one or more resistors, capacitors, and/or inductors between the via stub and a ground layer. Simulation would determine the most appropriate solution. The impedance terminating element may be formed internally to the PCB, or mounted to the PCB surface. For instance, a resistor equal to the characteristic impedance of the via (50 ohms) could be placed from a single ended signal to ground or power or a 100 ohm terminating resistor across a differential pair.

6. Lower the Surrounding Dielectric Constant

Lowering the dielectric constant, of the material surrounding a via, by positioning non-PTHs in proximity to the interconnect is a solution proposed by Bhyrav Mutnury and colleagues, IBM Corporation. Air in the non-PTH has a dielectric constant of 1, whereas FR-4 is approximately 4. This serves to increase the resonant frequency of the via stubs. By increasing the resonant frequency of the via stub, beyond the frequency of the signal, the attenuating effects of the via stub are no longer problematic. But, it may also make Swiss cheese of the reference plane, which is not a good approach for high-speed design.

7. Plate the via Barrel with Lossy Material

Stuart Allen Berke and colleagues, Dell Products, have postulated reducing the Quality (Q) factor of the via stub. The resonance of a via stub can be dampened by plating the via barrel with a material having a low conductivity. For example, a via can be plated with tin, which has a conductivity of approximately 8×10^-6 S/m, while copper has a conductivity of approximately 6×10^-7 S/m. Thus, tin can be referred to as a "lossy" medium as compared to copper. Plating a via barrel with a lower conductivity material, such as tin, reduces the Q factor of the via. Resistance is inversely proportional to the conductivity of the material used to plate the via, thus a lower conductivity material results in a lower Q factor for the via dampening the resonance.

In conclusion, dangling via stubs distort a high-frequency signal and also decrease the usable bandwidth of the signal. Since the via capacitance varies in proportion to the overall size of the hole and the plane clearance of the antipads, vias should be kept small with large clearances where possible. Oblong antipads also reduce capacitance and preserve the continuity of the reference plane. Of the seven solutions put forward to alleviate this problem, using blind vias and back-drill stubs on backplanes combined with oblong antipads are the best, and most economic solutions for high-speed design.

Points to Remember

- Back-drilling typically requires specialized equipment and is expensive.

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• Blind vias behave like a lumped capacitor with very little inductance. And because the microvia hole is very small, it has less capacitance than a standard PTH via.

• Removing non-functional via pads reduces via capacitance which in turn increases impedance.

• Increasing the size of the antipad reduces capacitance but, at the same time, may well make Swiss cheese out of the reference plane increasing the DC drop and reducing the amount of instantaneous current available.

• An oblong antipad still reduces the parasitic capacitance significantly, but at the same time allows the return current to flow directly between the vias to reduce loop inductance and preserve the continuity of the reference plane.

• A terminating element placed at the bottom end of the stub reduces signal reflection.

• Lowering the dielectric constant, of the surround material, and tin plating the via barrel are possible but may not be practical solutions.

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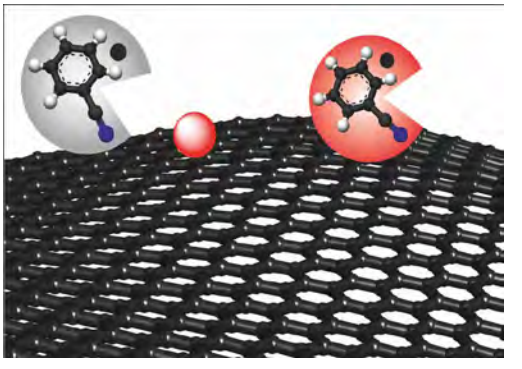
Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD) Australia. The company is a PCB design service bureau that specializes in board-level simulation. ICD has developed the ICD Stackup Planner and ICD PDN Planner software, which is available here. To contact Barry, click here.

Low-cost and Defect-free Graphene



Chemists at Friedrich-Alexander-Universiät Erlangen-Nürnberg (FAU) have now succeeded in producing defect-free graphene directly from graphite for the first time.

Graphene is two-dimensional and consists of a single layer of carbon atoms. It is particularly good at conducting electricity and heat, transparent and flexible yet strong. Graphene's unique properties make it suitable for use in a wide range of pioneering technologies, such as in transparent electrodes for flexible displays.

A common way of synthesising graphene is through chemical exfoliation of graphite. In this process, metal ions are embedded in graphite, which is made of carbon, resulting in what is known as an intercalation compound. The individual layers of carbon - the graphene - are separated using solvents. The stabilised graphene then has to be separated from the solvent and reoxidised. However, defects in the individual layers of carbon, such as hydration and oxidation of carbon atoms in the lattice, can occur during this process. FAU researchers have now found a solution to this problem. By adding the solvent benzonitrile, the graphene can be removed without any additional functional groups forming - and it remains defect-free.

"This discovery is a break-through for experts in the international field of reductive graphene synthesis,' Professor Hirsch explains. 'Based on this discovery we can expect to see major advancements in terms of the applications of this type of graphene which is produced using wet chemical exfoliation. An example could be cutting defect-free graphene for semi-conductor or sensor technology."

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Evaluating Evaluation Boards

by Istvan Novak
ORACLE

Evaluation boards are very helpful. Manufacturers of complex circuits such as DC-DC converters provide boards with those circuits ready to try out, saving us time and effort to design the printed circuit board around them. Evaluation boards are supposed to help us to understand the capabilities of the device. But with the very many potential user applications, what should a particular user expect and look for in an evaluation board? We need to know how to properly evaluate an evaluation board.

My February 2013 Quiet Power column featured an LTM4604 evaluation board. In that column the purpose was to discuss different measurement techniques; the subject was not the regulator itself. In this column we look at an LM20143 evaluation board to explain what may matter during the evaluation.

The LM20143 is an adjustable-frequency synchronous buck regulator with current-mode control loop [2]. The input voltage can be anywhere in the 2.95 to 5.5V range, the maximum continuous output current is 3A. The switching frequency is adjustable in the 500 kHz to 1500 kHz range. The default output voltage setting of the evaluation board is 1.2V. The integrated circuit includes the output switching devices. Figure 1 shows the top view of the evaluation board with no cable attached.

To make the board work, all we have to do is connect a voltage source to the input terminals and pull the enable pin (labeled 'EN' on the board) to logic high.

The first rule in every test and measurement (also true in simulations, by the way) is "Know what to expect." We measure something because we may want to validate a design or we measure something because we are not sure exactly how the circuit behaves. This latter case, however, is no excuse to ignore the rule: we still should have some idea what we expect as a result. If we don't, it becomes a full-fledged exploration and we need to be extremely careful to make sure that accidental mistakes or measurement errors don't mask the correct signature that we are after. In an evaluation board of a DC-DC converter, we can test many different aspects of operation. There are items that require only DC voltage and current meters. This way, for instance, we can check the line and load regulations and efficiency at different input and output voltages and load currents. To test for dynamic parameters, we can use an oscilloscope and transient current source. In the frequency domain, with a frequency response analyzer or vector network analyzer we can test the gain-phase curve or output impedance. These measurements

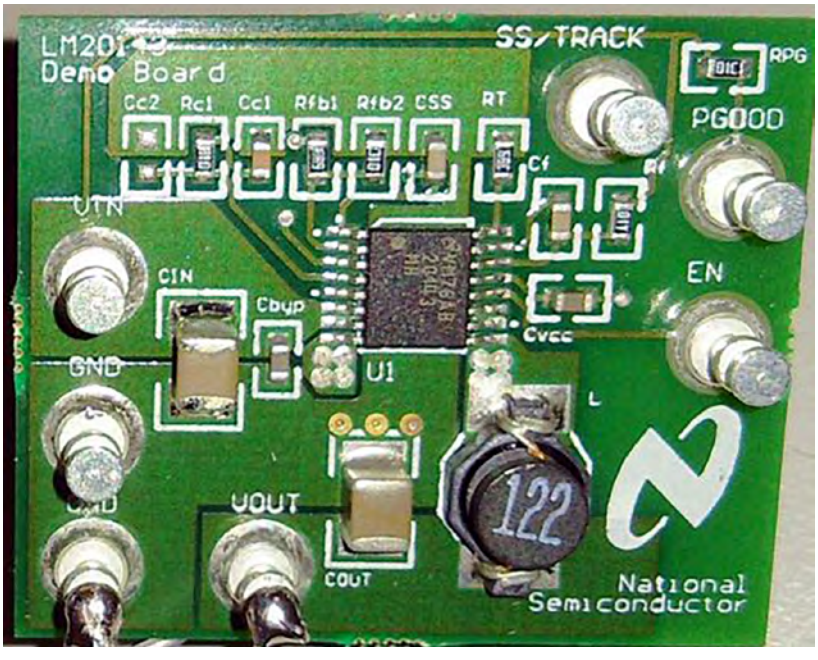

Figure 1: LM20143 evaluation board, top view. Evaluation module courtesy of Texas Instruments.

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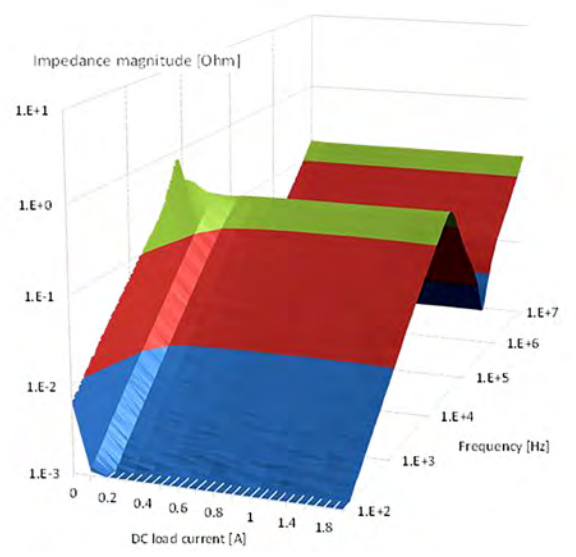

Figure 2: Output impedance as a function of frequency and DC load current.

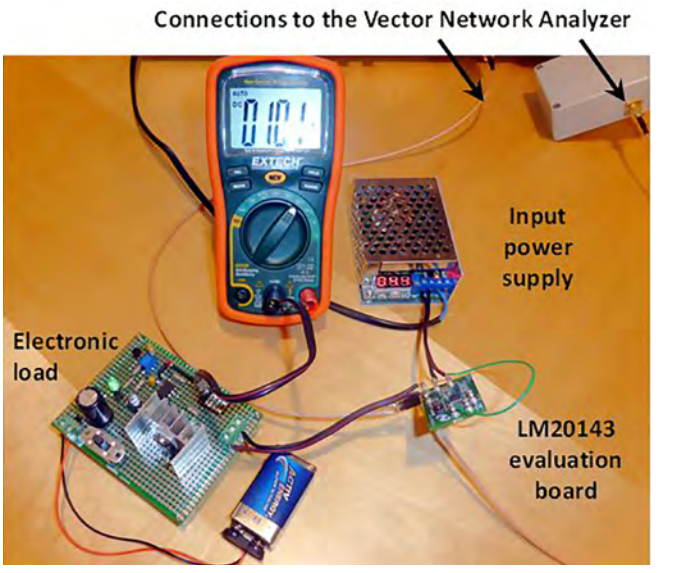

Figure 3: Test setup with input power supply and electronic load.

can be done with small-signal excitation or large-signal excitation. As an example, in Figure 2 we show the output impedance magnitude measured with fixed input and output voltages, with DC load current varied from 0A to 2A. The photo in Figure 3 shows the measurement setup in my basement lab.

The setup has the LM20143 evaluation board connected to a small AC-DC adjustable power supply, serving as the input source. On the lower left there is a small home-made electronic load circuit, which can draw an adjustable constant current. The voltage, proportional to the DC current is shown on the handheld digital multimeter. Two cables connect to the vector network analyzer, not shown on this photo.

When we look at the data on Figure 2, we have to answer the question: Is this close to what we expected? What would be warning signs that something is wrong with our measurement or the evaluation board may not meet our expectations? We can start with items that we know. In case of evaluation boards, we get a schematics and BOM as well, reproduced in Figure 4 [3].

The schematics and BOM show that on the evaluation board the main inductor has 1.2 uH inductance and 17 mOhm DC resistance. There

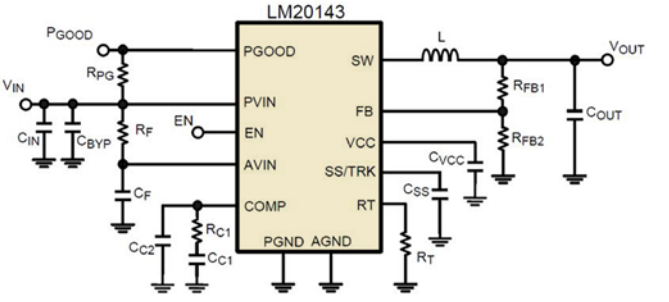

Figure 4a: Schematics of the LM20143 evaluation board used in reference 3.

is a single capacitor on the output, a 1210-size 47uF 6.3V X5R ceramic capacitor. With or without this knowledge about the component values, we can take the measured output impedance and fit to it a simple model. The plot in Figure 5 shows the result of a very quick curve fitting we can do in a spreadsheet in seconds. The measured data is the blue trace, using the data at 1A DC load current from Figure 2. The red line, almost completely behind the blue trace, is the result of a simple three-capacitor model, where the third capacitor is fit around the impedance minimum at 0.5 MHz. The values to get this match come at as C_3 = 38uF, R_3 = 3.5mOhm, L_3 = 3nH. Are these values reasonable? The 38uF capacitance is 80% of the nomi-

Designator	Description	Part Number	Qty	Manufacturer
U1	Synchronous Buck Regulator	LM20143	1	Texas Instruments
C_{IN}	47 µF, 1210, X5R, 6.3 V	GRM32ER60J476ME20	1	Murata
C_{BYP}	1 µF, 0603, X5R, 6.3 V	GRM188R60J105KA01	1	Murata
C_{OUT}	47 µF, 1210, X5R, 6.3 V	GRM32ER60J476ME20	1	Murata
L	1.2 µH, 17 mΩ	DO1813H-122ML	1	Coilcraft
R_F	1Ω, 0603	CRCW06031R0J-e3	1	Vishay-Dale
C_F	100 nF, 0603, X7R, 16 V	GRM188R71C104KA01	1	Murata
CV_{CC}	1 µF, 0603, X5R, 6.3 V	GRM188R60J105KA01	1	Murata
R_{PG}	10 kΩ, 0603	CRCW06031002F-e3	1	Vishay-Dale
R_{C1}	1 kΩ, 0603	CRCW06031001F-e3	1	Vishay-Dale
C_{C1}	4.7 nF, 0603, X7R, 25 V	VJ0603Y472KXXA	1	Vishay-Vitramon
C_{C2}	OPEN	OPEN	0	N/A
C_{SS}	33 nF, 0603, X7R, 25 V	VJ0603Y333KXXA	1	Vishay-Vitramon
R_{FB1}	4.99 kΩ, 0603	CRCW06034991F-e3	1	Vishay-Dale
R_{FB2}	10 kΩ, 0603	CRCW06031002F-e3	1	Vishay-Dale
R_T	49.9 kΩ, 0603	CRCW06034992F-e3	1	Vishay-Dale
Test Points	Test Points	160-1026-02-01-00	7	Cambion

Figure 4b: Bill of materials of the LM20143 evaluation board used in reference 3.

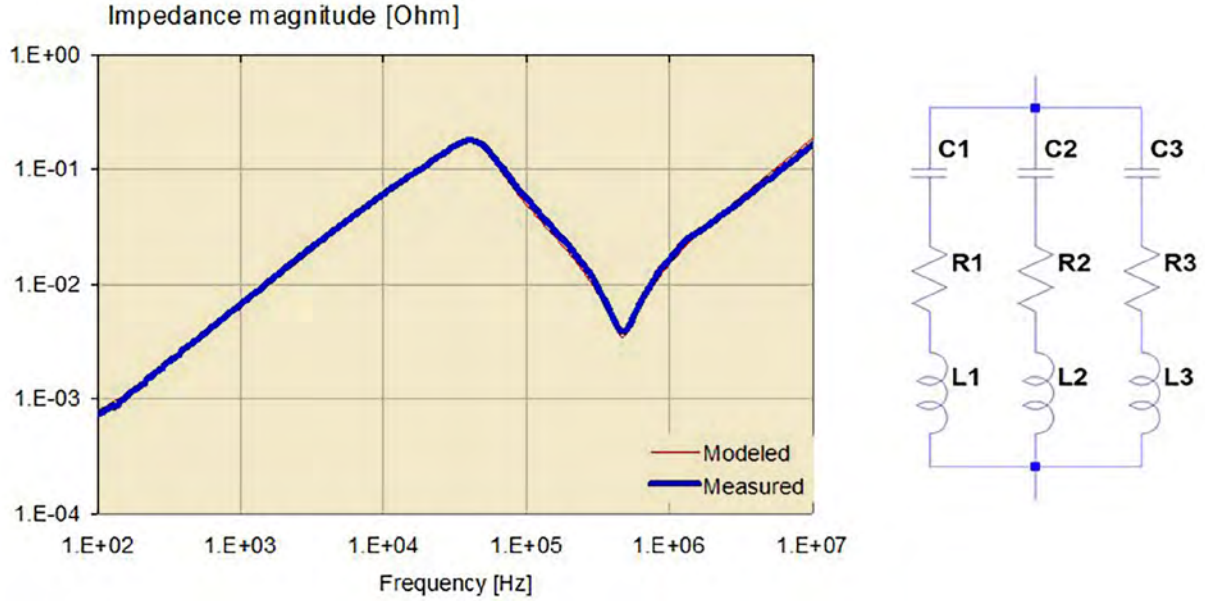

Figure 5: Correlation of measured output impedance to a three-capacitor model at 4.5V input voltage, 1.2V output voltage and 1A DC load current.

nal 47uF value. Considering the 20% initial tolerance rating on the part, plus the additional few percent for DC bias effect and the expected 20-30% capacitance drop due to AC bias effects [4], the 38uF is way within the expected range.

Many capacitors from major component manufacturers also have various models available, from which we can get the typical ESR values. In case this data is not available and we may suspect that the ESR value we got from curve fitting might be wrong, we can continue the testing and collect more data. If we want to check the parameters of the same exact capacitor that we have on the evaluation board, we can for instance measure the output impedance with the converter turned OFF, so that across the out-

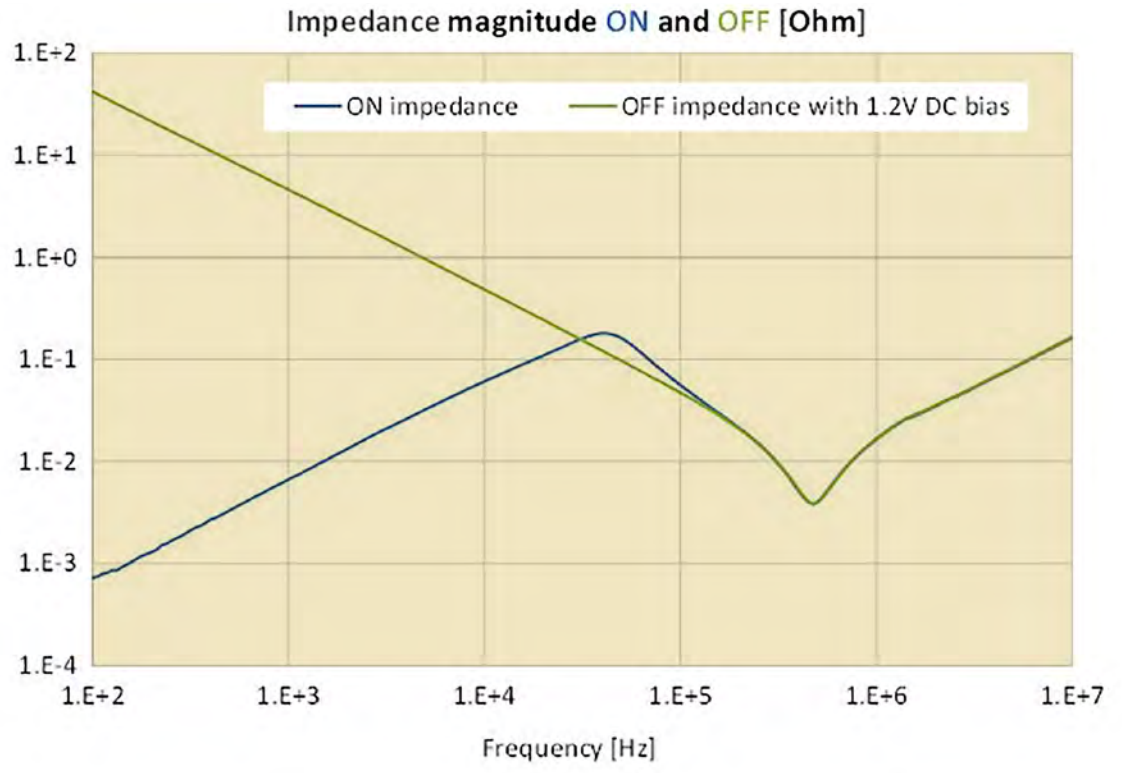

Figure 6: Output impedance of the evaluation board with no input power (green trace) and with input power (blue trace) applied.

put terminals we have only the output capacitor. If we do this, we may need to apply a DC bias we have during normal operation, so that we measure the part with the correct DC operating point. To remove any potential contribution from the evaluation board, we can desolder the capacitor and measure it in a fixture. Ultimately we can obtain samples of the same capacitor model and measure several of them to see how different or how identical their data looks.

For example, in Figure 6 the combined plot of the evaluation board is shown with and without input power. We can see that around 0.5MHz, where the output capacitor's ESR matters, the agreement is quite good, namely the impedance in that frequency range even with the converter running is primarily dictated by the output capacitor. From all the above we can conclude that the ESR of the output capacitor is around 2 to 2.5 mOhms, assuming that the plane resistance on the evaluation board between the location of the output capacitor and the point where we measure the output impedance is in the range of one to one and half mOhms. Finally, we can confirm this by measuring the part in a fixture with the fixture de-embedded.

Once we feel comfortable with the basic results, we can look further and ask again: What did we expect or what are we looking for in the test results? One qualitative feature that we may want to see, especially if we want to use the measured impedance to create simple equivalent circuits for simulations, is the consistency of the impedance plots across the different input parameters, such as load current, input voltage and possibly ambient temperature. Output voltage should also be considered for the list if we plan on using the same device with different output voltage settings. To get a sense of how consistent is the small-signal impedance performance of the converter, Figure 7 shows the impedance surfaces at three different input voltages. We can see that the primary variation is along the frequency axis,

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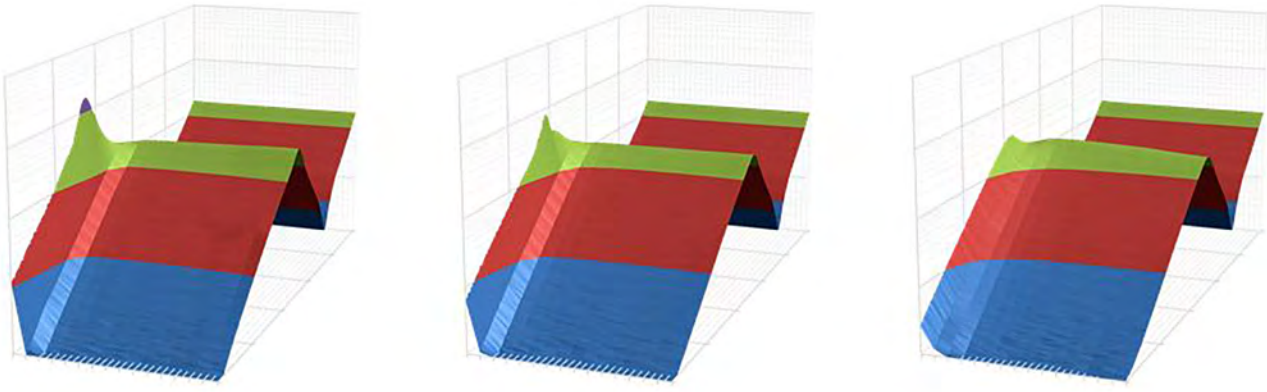

Figure 7: Variation of impedance surface as a function of input voltage. Left plot: 3.5V;middle plot: 4.5V; right plot: 5.5V DC input voltage. For sake of simplicity, axis labels and titles are not shown, but are the same as in Figure 2.

but there is very minimal change with input voltage and load current, especially above 0.2A DC load.

There are many other parameters we may want to test. In the frequency domain we could check the gain-phase plot to assess the stability margin of the converter. In the time domain we can measure the output ripple, high-frequency burst noise and transient response. And finally we could tie all that data back to simulations to see how good correlation we get. We will address some of those items in future columns, and also things that don't make sense to check on evaluation boards.

So next time when you evaluate an evaluation board, be prepared to know what to expect. Double checking the test data always helps to avoid wrong and potentially misleading conclusions. **PCBDESIGN**

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4. DesignCon East 2011 paper, DC and AC Bias Dependence of Capacitors Including Temperature Dependence

Dr. Istvan Novak is a distinguished engineer at Oracle, working on signal and power integrity designs of mid-range servers and new technology developments. With 25 patents to his name, Novak is co-author of "Frequency-Domain Characterization of Power Distribution Networks." To contact Istvan, click here.

KnowMade—Microbattery

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The Little Guide to Resins

by Alistair Little
ELECTROLUBE

Over past months, this column has seen Electrolube's Phil Kinner provide *The PCB Design Magazine* readers with information, guidance and practical tips on the uses and application of conformal coatings. He now hands over the reins to me, and I plan to do the same for resins, starting this month with a "back to basics" piece that questions the core rationale for potting—why and how do we do it, and what are we trying to achieve or protect?

First, a little background. I joined Electrolube as global business technical director for the Resins Division in January 2016. I currently head up a team of chemists developing formulations that encompass epoxy, polyurethane and silicone resin systems for encapsulating or potting electrical devices or electronic components in order to protect them against a wide range of environments.

In my previous appointment at Gurit (UK) I held the position of senior product development chemist, responsible for the development of new epoxy and vinyl ester resin systems for aerospace, automotive, engineering and marine composite systems. Prior to this, I worked for 2K Polymer Systems, where I developed civil engineering and structural adhesives, and at SI Group, where I worked on UV curing and high-performance resins.

I have wide experience working within ISO 9000, 14001 and 18001 accredited systems, and I am an expert in vinyl ester resin systems (for which I am in the process of completing a PhD in Polymer Chemistry at Loughborough University). I am a Chartered Chemist, an active member of the Royal Society of Chemistry, and a member of the Society of Adhesion and Adhesives.

Resins: Why, Where and How?

I would like to start this series of columns by going back to basics, questioning the core rationale for potting and encapsulation with resins, their fundamental chemistries and how each resin type differs one from the other—indeed, how their individual properties can be exploited to maximise performance under a wide range of environmental conditions.

Let's start with moisture, the archenemy of electrical and electronic devices that, quite apart from causing short-circuits, can also lead to premature deterioration of components due to corrosion. Polyurethane resins—usually supplied as two-part products, which, when mixed

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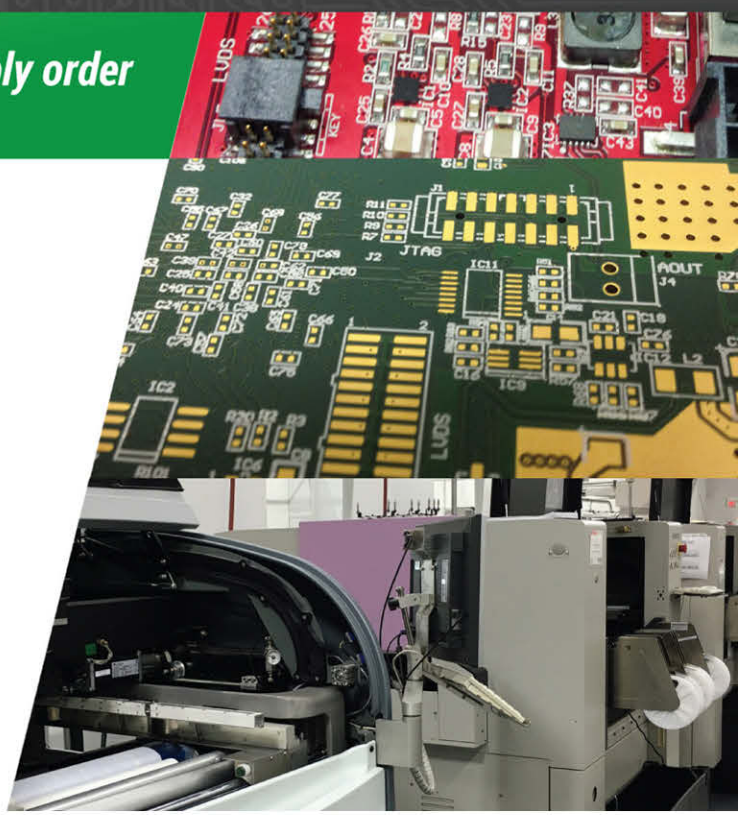

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achieve the desired cure—provide that all-important moisture resistance, as well as excellent electrical insulation, flexibility and good adhesion to most substrates, both metal and plastic. Some polyurethane resin systems provide exceptional resistance to sea water, as well as temperature extremes, making them an ideal choice for marine applications such as sensor encapsulation. A good outdoor example of a polyurethane resin encapsulated component that requires maximum protection against water ingress is an LED lighting unit; these resins are also optically clear and UV stable, making them ideal for the task.

“Some polyurethane resin systems provide exceptional resistance to sea water, as well as temperature extremes, making them an ideal choice for marine applications such as sensor encapsulation.”

There are one-part moisture curing polyurethane resins available, but these are a no-no if you want to achieve moisture resistance, as moisture penetration is necessary in order to obtain full cure on potting or encapsulation. Some epoxy resins, too, offer good moisture resistance, as well as a fast cure, hardness and high stability, particularly in variable temperature environments. These also adhere well to most substrates, even difficult substrates with a very low surface tension, such as PTFE, ensuring a watertight encapsulation.

You might also need to protect electrical or electronic components that are likely to come into contact with chemicals, including acids, alkalis, solvents and a whole raft of other substances that pose a threat to delicate circuits and components. Chemical resistance is very much the province of epoxy resins, though some of the tougher polyurethane products—as well as some silicone based formulations—will provide a degree of protection. Epoxy resin products are available to protect electrical/electronic units that undergo frequent or permanent immersion in solvents such as diesel fuel, leaded and unleaded petrol and cellulose thinners.

Protecting components from mechanical shock and vibration may also be on your must-do list. Here, a more flexible cured product is likely to provide the best solution as it adds a level of compliance which will help insulate the potted components against adverse mechanical movements. In addition to their moisture resistant properties, polyurethane resins also provide this desired level of flexibility and so they are often the first choice for shock and vibration protection. Silicone resins, too, offer excellent flexibility and, in addition, will tolerate high operating temperatures.

One more “shock” that I should mention is thermal shock, which can have a devastating effect on electronic components, shortening their operating lives at best, and destroying them completely at worst. The adverse effects of thermal stress can be ameliorated by using two-part epoxy resins, which are best for those applications that undergo severe temperature cycling or which are likely to suffer thermal shock. Some also provide the added bonus of flame-retardant technology.

Finally, it’s worth mentioning that, quite apart from providing all the protections listed above, opaque potting and encapsulation resins also conceal what lies beneath. This could provide an effective foil against counterfeiters or those wishing to copy a circuit layout, helping you to protect your intellectual property.

When it comes to the choice and applications of resins, there’s a great deal more to discuss, and over the following months I hope to provide some useful tips and design advice that will help you in your quest for reliable circuit protection. **PCBDESIGN**

Alistair Little is global business/technical director for the Resins Division of Electrolube.

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THERMAL DESIGN ISSUES

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MilAero007 Highlights

DoD Announces Groundbreaking Policy to Stop Counterfeits

The Department of Defense (DoD) yesterday issued a new regulation that will greatly reduce the risks of counterfeit microelectronics entering the military supply chain.

Congressman Bill Johnson Visits TTM Technologies Manufacturing Facility in Ohio

Congressman Bill Johnson (R-OH-6) met with executives and employees of IPC-member company TTM Technologies, Inc. at their manufacturing facility in North Jackson, Ohio. Coordinated by IPC, this visit is part of an ongoing effort to help policymakers learn first-hand about legislative and regulatory issues that impact the industry.

Multiple Markets Merge for PCBs at H&T Global

While at the SMTA-Ohio expo I met Rob DiGiovanni, VP of sales and marketing with H&T Global, a printed circuit manufacturer based in Florida. I was attracted to the H&T booth by a large photo of an Army jeep. I wanted to learn what this particular photo had to do with PCBs, and Rob had a ready answer.

Event Review: 7th Electronic Materials and Processes for Space Workshop

This year's Electronic Materials and Processes for Space Workshop discussed a wide range of technology issues and developments when it comes to PCB fabrication and assembly for space applications. From addressing reliability issues to dealing with cracks that may form during thermal cycling, to REACH regulations and their impact on space hardware, and tin whisker growths.

Space Launch System Rocket Gets Updated Adapter for Journey to Mars

NASA's Space Launch System (SLS) rocket is designed to be flexible and evolvable to meet a variety of crew and cargo mission needs, and with an exploration upper stage (EUS) planned for future configurations, the rocket will require a new adapter to connect it to the Orion spacecraft.

American Standard Circuits Now Provides DFM Software

Anaya Vardya, CEO at American Standard Circuits, announces that ASC is now providing free design for manufacture (DFM) software on their website. Customers can simply upload their Gerber files to ASC's server and within approximately 60 minutes they will be emailed a detailed summary in PDF format.

LPKF Equips German Armed Forces with Circuit Board Plotters

LPKF ProtoMats machines conductive patterns out of fully coated substrates by contour milling. Contact and mounting holes are then drilled. The vision system integrated in the ProtoMat E44 helps reliably detect the substrate position on the working surface to ensure that the same area is covered on the front and back sides.

Flex is Where it's at

At the recent SMTA Ohio Expo event, Jack Baculik of Circuits LLC speaks with I-Connect007's Patty Goldman about the latest developments driving demand for flex and rigid-flex circuits.

Smart Weapons Market Worth $15.64 billion by 2021

The report "Smart Weapons Market by Product (Missiles, Munitions, Guided Projectile, Guided Rocket, Guided Firearms), platform (Air, Land, Naval), Technology (Laser, Infrared, Radar, GPS, Others) & Region—Global Forecast to 2021," published by MarketsandMarkets, the market is estimated to reach USD 15.64 billion by 2021, at a CAGR of 6.3% between 2016 and 2021.

Military Satellites Market to Reach $14.37B in 2016

The military satellites market is set to be worth $14.37 billion in 2016, resulting from several major contracts in the United States, Israel and Russia and continuing satellite fleet modernization in China and India, according to a new report by visiongain.

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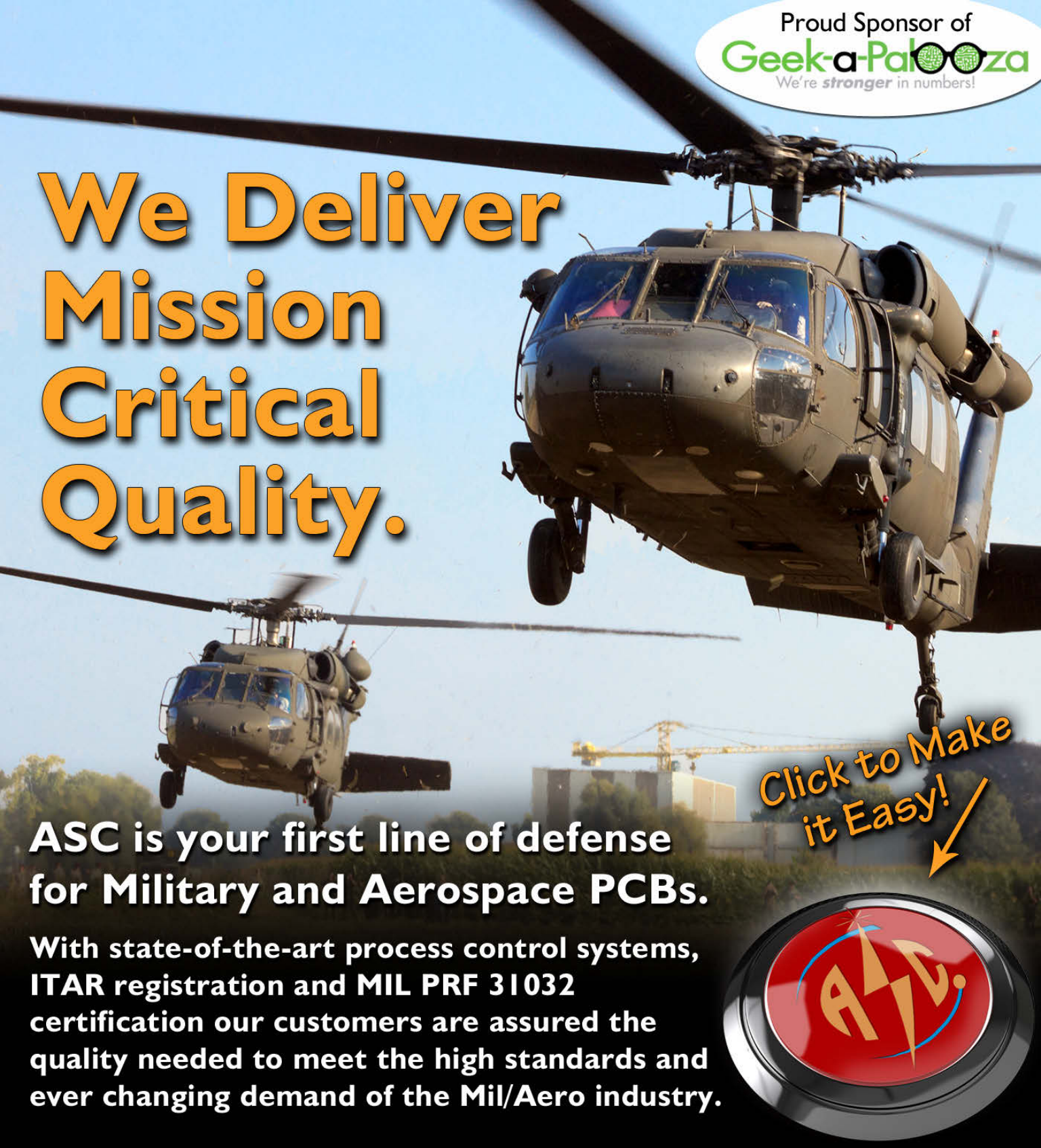

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The Fundamentals of Improving PCB Thermal Design

by Gabriel Ciobanu
CONTINENTAL CORPORATION
and Boris Marovic
MENTOR GRAPHICS

Continental Automobile engineers have many years of experience building critical parts and systems for automobiles, from the chassis and safety systems to the powertrain, interior control systems, and tires. Much has changed in the past decade, and electronic technology has become an important aspect of what the company supplies to OEM and other manufacturers worldwide. Electronics are doing more now than ever to provide safer cars, cleaner power, more mobility, and smarter driving.

Making sure that automotive electronics are reliable, safe, and properly designed begins at the component level. Heat must be addressed early in the design process for these goals to be achieved. The most important thermal resistance for heat, outside the IC package, is the PCB. Continental engineers use 3D computational fluid dynamics (CFD) to simulate and test a PCB's thermal design (Figure 1). Modeling the main heat flow paths in detail is critical to ensure that generated heat in the component flows out to the ambient, either through convection, conduction, or radiation. Knowing the thermal junction resistance allows optimizing a design for more efficient and less costly heatsinks, materials, and ICs.

When building a model to use in simulation, different methods can be used to represent chip packages and PCBs. Chip packages are typically defined as four types (Figure 1). The simple cuboid is a lumped component with some material properties and a heat source applied to it. The 2-resistor model doesn't include any thermal capacitance and is therefore not suitable for transient analysis of component temperatures. The Delphi model is comprised of several thermal resistances and capacitances and thus is more accurate and suitable for transient simu-

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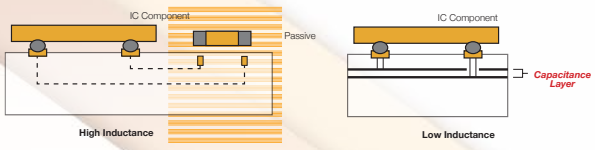

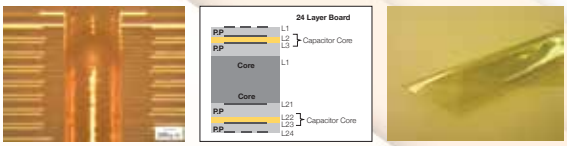

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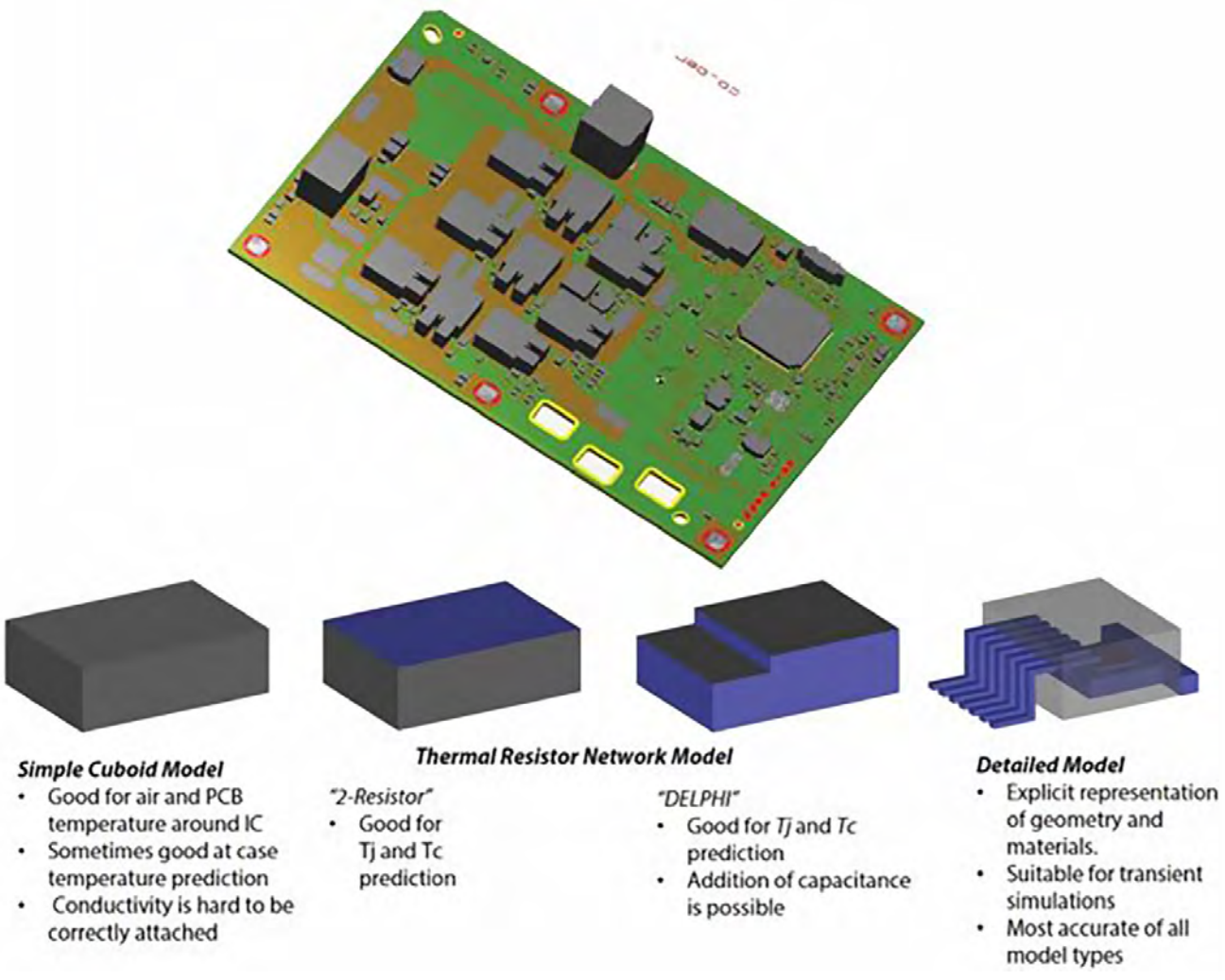

Figure 1: Simulation models for a chip package, from the simplest to more complex.

lations. Finally, the detailed model is modeled explicitly and is the most accurate model; however, it also increases the simulation time and requirements for computing resources.

For the PCB, four detailing levels from simple to complex also are used in simulation: lumped approximation, individual layers' representation, layers modeled with "patches," and copper tracks and areas modeled in detail.

Using lumped approximation (Figure 2), the PCB is represented as a single block with thermal orthotropic thermal conductivity (different in all directions) applied in the x,y (in-plane) and z (through-plane) axes. This method has a fast modeling and solving time. However, the heat-spreading effect is lost for surface-mount devices with high-power losses.

Using individual layers' representation (Figure 3), each layer is modeled as a separate object with individual thermal conductivity. This method is better at capturing in-plane heat-spreading behavior of surface-mount devices and is still low in computational resource demands. It provides optimistic results for some IC that don't have cooling measures (copper areas, thermal vias) implemented.

For state-of-the-art simulation, each individual layer of the PCB can be modeled. Each layer is subdivided into an array of "patches" (Figure 4). For each patch, orthotropic thermal conductivity is calculated from the copper and FR-4 composite distribution within that area. This method provides more accurate results, but takes a long time to model and solve and

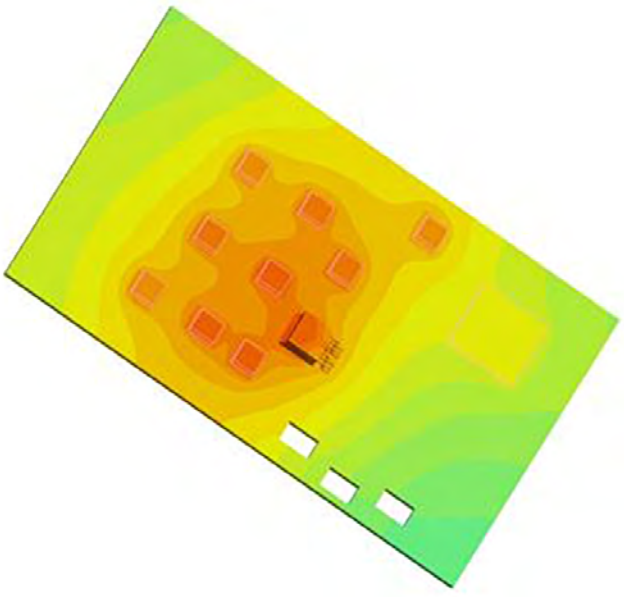

Figure 2: Lumped approximation model.

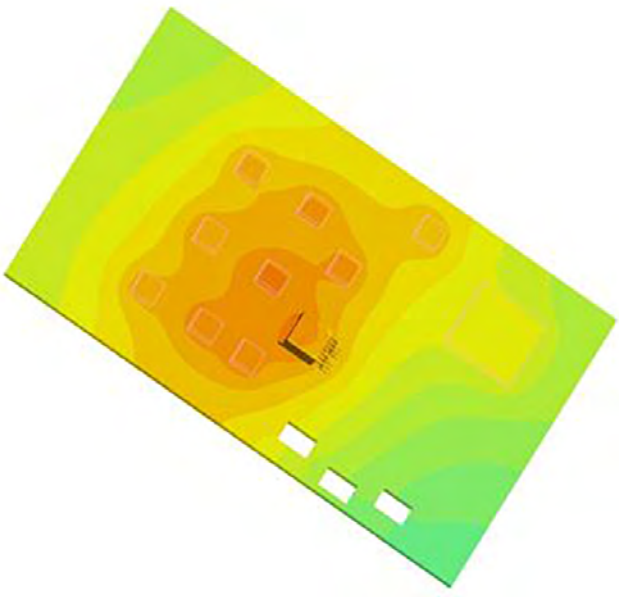

Figure 3: Individual layers' model.

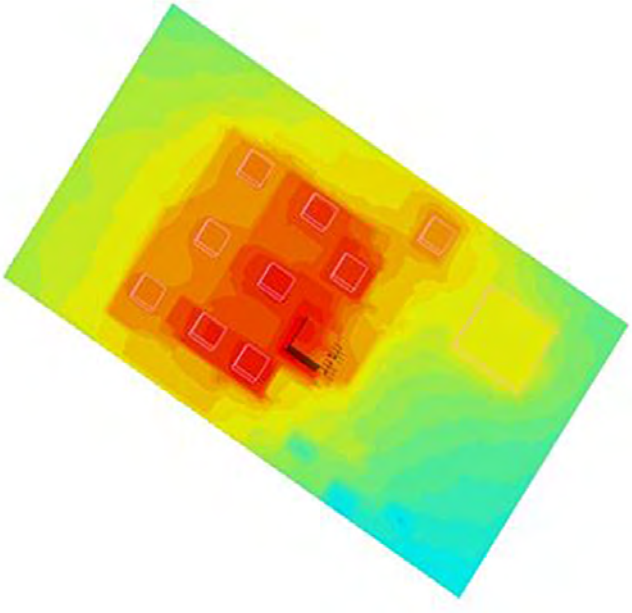

Figure 4: Model of each layer with patches.

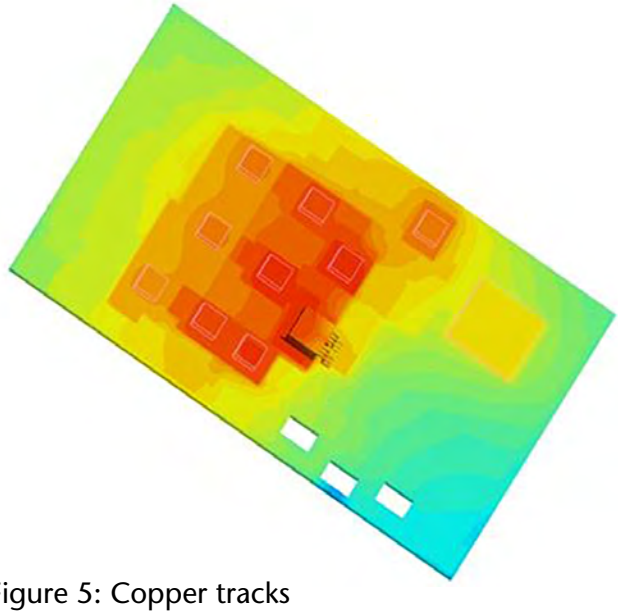

Figure 5: Copper tracks and areas modeled in 3D detail.

uses a lot of computational resources.

Finally, copper tracks and areas modeled can be analyzed in a 3D thermal simulation software for the greatest amount of detail (Figure 5). "Wide" copper tracks and areas are represented individually as parts of the input data. This method has the most accurate results because each layer has a 3D representation.

A detailed 3D model provides an explicit representation of the geometry and materials, and is most accurate. A detailed PCB model should be used when the main cooling path is through the board, and a simpler PCB representation when the board is not the main cooling path. All these models can be used for transient simulations of the PCB.

All aspects of the simulation model should have the same magnitude of details. A model is

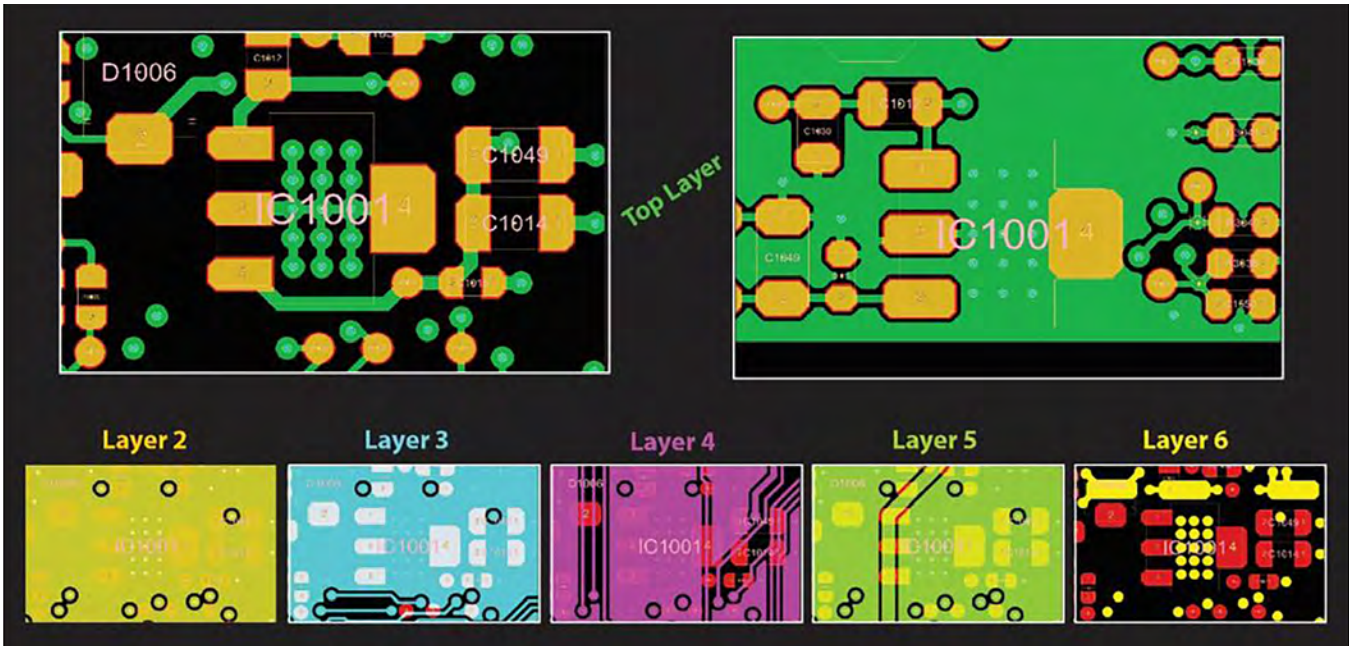

Figure 6: In the IC for which thermal behavior is simulated, only the top layer is different between the two designs.

good if the change from the thermal junction to ambient is within 10% of measurement results.

How do the details represented by the simulation model help to improve a design? Let's look at a detailed analysis of two different designs of an IC onto a PCB where only the top layer and number/position of the thermal vias varies (Figure 6).

The modeled PCB is approximately 1.6 mm thick with six layers (outer layers = 67 µm thick; inner = 95 µm thick) (Figure 7). The IC is an SOT223 (surface mount, 4 pin) package modeled with nominal values. The 15 thermal vias are 300 µm inner hole and 25 µm copper-plating thickness (modeled as square section). It has 1-W power loss at the inside junction and a 25°C ambient and cooling block temperature.

In Figure 6 and 7, the "bad" (left image of top layer) and "good" (right image of top layer) designs can be differentiated by analyzing the detailed models. In this first example of a bad layout, the base has 15 thermal vias. Analysis results shows that the thermal junction maximum temperature is 64.6 °C. 0.69 W is transferred by conduction into the PCB top layer (the rest, 0.31 W, is going outside the junction through pins 1-2-3 by conduction or outside the encapsulant by convection) (Figure 8a). Only 0.40 W is transferred into the thermal interface material (TIM) through the 15 thermal vias (Figure 8b). This is inefficient thermal via use.

The second example of a bad layout uses nine thermal vias instead of 15. Analysis results shows that the thermal junction maximum temperature is 65.1 °C (+0.5 °C). 0.69 W are transferred by conduction into the PCB top layer. The rest, 0.31 W, is transferred outside the junction through pins 1-2-3 by conduction or outside the encapsulant by convection (Figure 9a). Only 0.39 W is transferred into the TIM through the 9 thermal vias (Figure 9b). Removing six of the vias has little affect (ΔT = 0.5 °C).

The first example of a good layout also has a base of 15 thermal vias. Analysis results shows that the thermal junction maximum temperature is 45°C. 0.87 W is transferred by conduction into the PCB top layer by pin 4. The rest (0.13 W) is going outside the junction through pins 1-2-3 by conduction or outside the encapsulant by convection (Figure 10a). 0.60 W is transferred into the TIM through the 15 thermal vias (Figure 10b). This is a much more efficient use of the thermal vias.

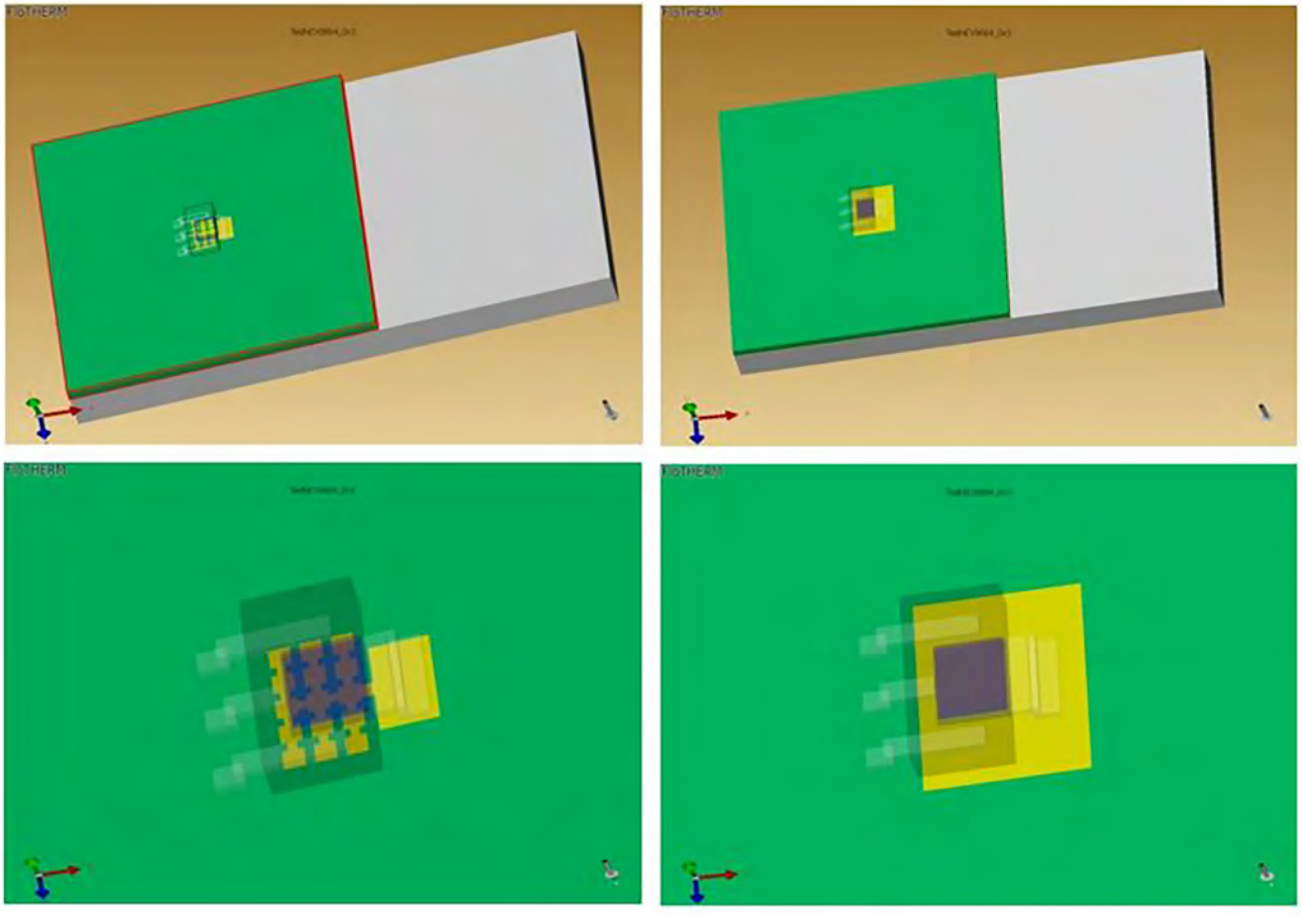

Figure 7: Model of the package in FloTHERM 3D thermal simulation and analysis software.

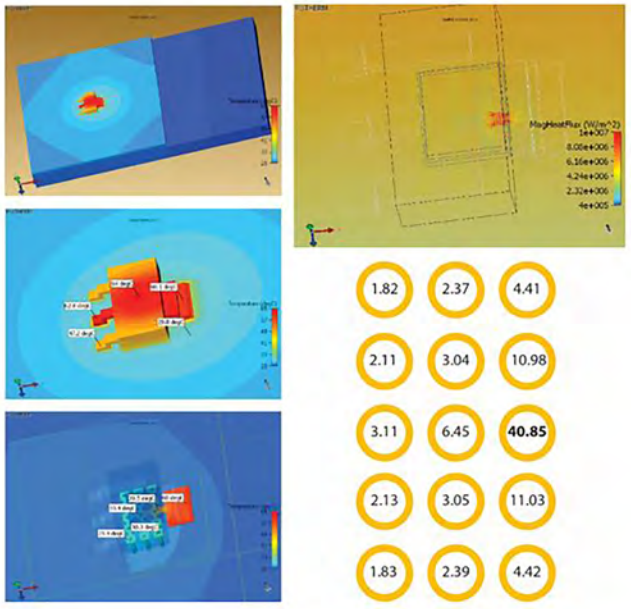

Figure 8: Bad layout with 15 thermal vias, and the percentage of thermal via usage for the 0.4 W transferred by vias.

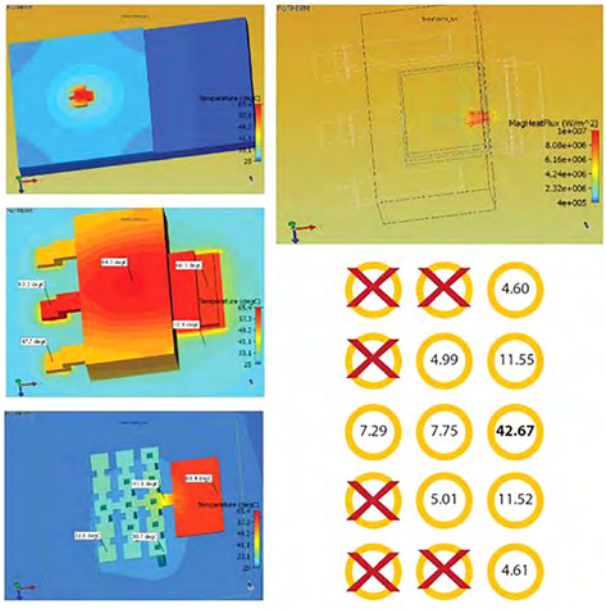

Figure 9: Bad layout with nine thermal vias, and the percentage of thermal via usage for the 0.39 W transferred by vias.

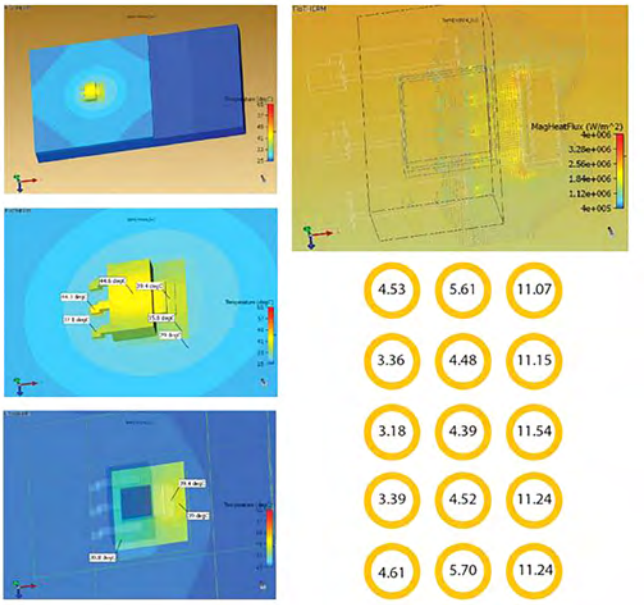

Figure 10: Good layout with 15 thermal vias, and the percentage of thermal vias usage for the 0.6 W transferred by vias.

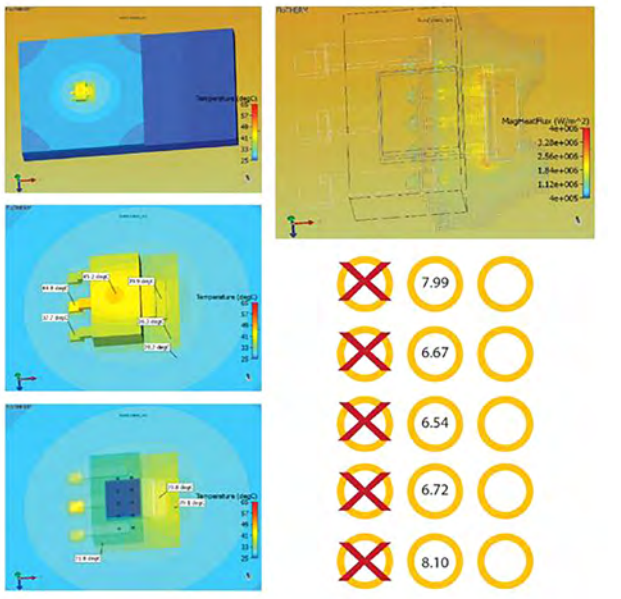

Figure 11: Good layout with 10 thermal vias, and the percentage of thermal via usage for the 0.57 W transferred by vias.

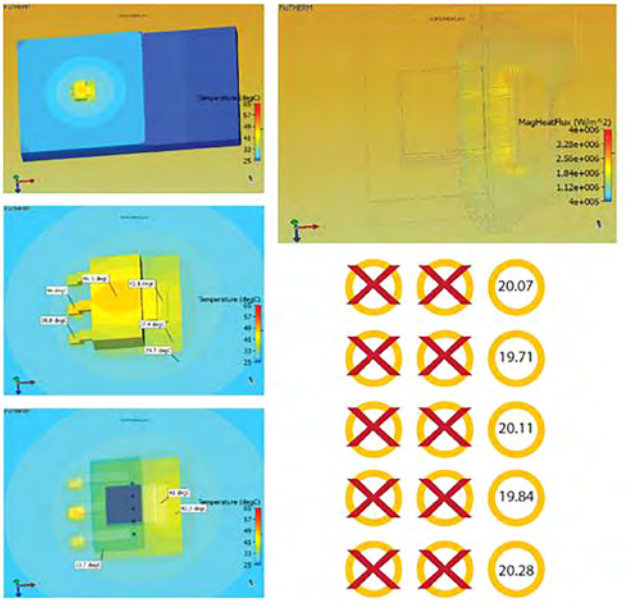

Figure 12: Good layout with five thermal vias, and the percentage of thermal via usage for the 0.48 W transferred by vias.

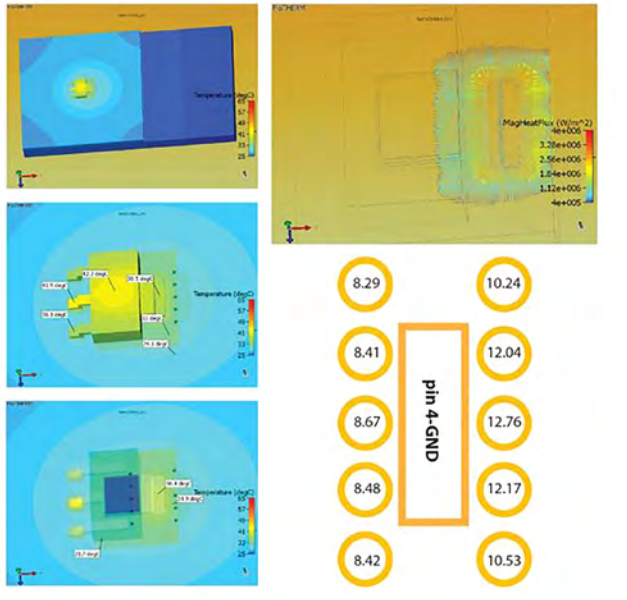

Figure 13: Improved layout with 10 thermal vias, and the percentage of thermal via usage for the 0.71 W transferred by vias.

The second good layout has a base of 10 thermal vias. Analysis results shows that the thermal junction maximum temperature is 45.5°C (+0.5°C). 0.87 W is transferred by conduction into the PCB top layer by pin4. The rest, 0.13 W, is transferred outside the junction through pins 1-2-3 by conduction or outside the encapsulant by convection (Figure 11a). 0.57 W is transferred into the TIM through the 10 thermal vias (Figure 11b). The same benefit

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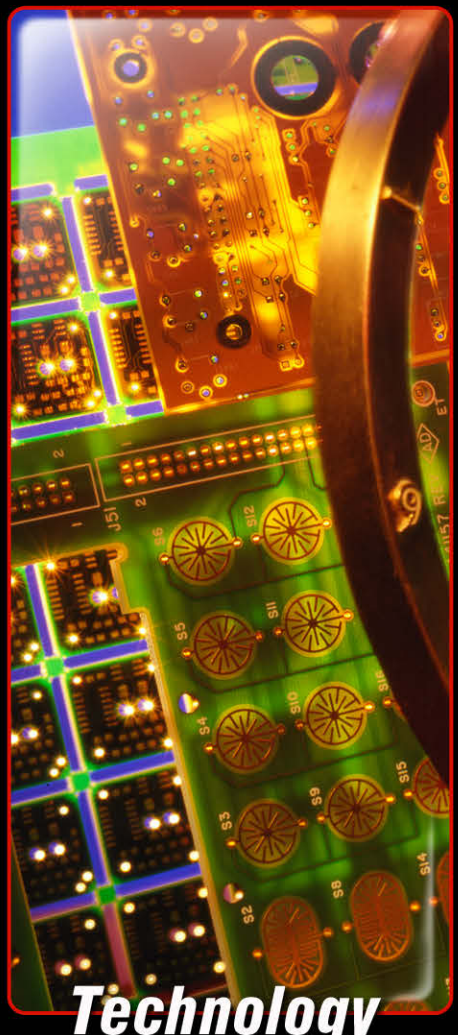
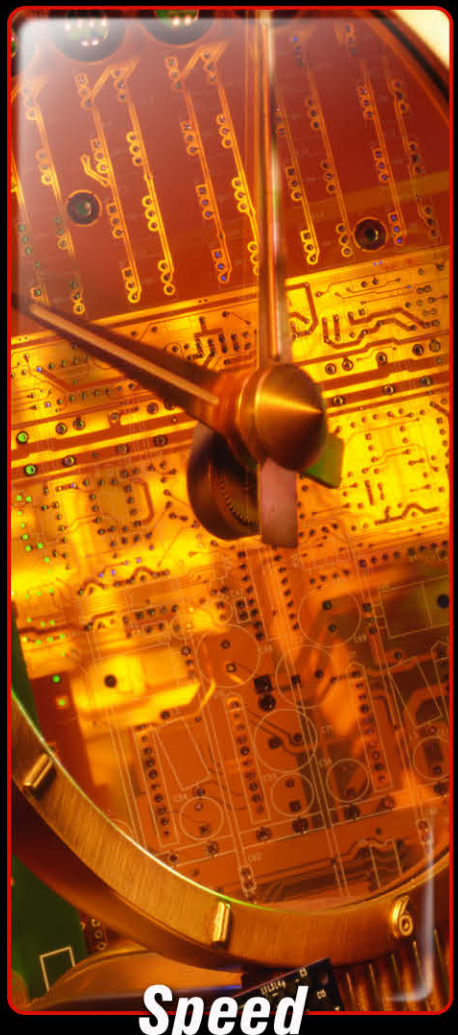
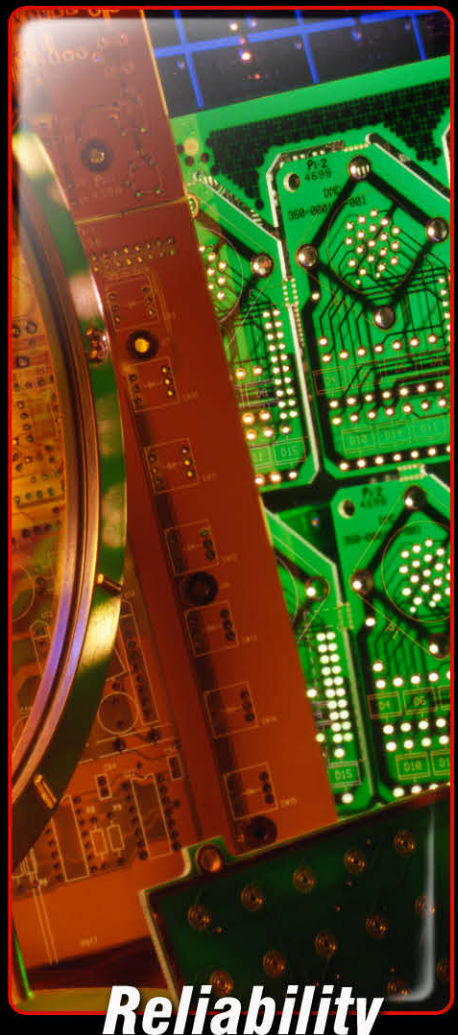


Technology



Speed



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is obtained as the first design but with a smaller number of vias.

We can take the analysis further by reducing the number of vias for this design to five. Analysis results shows that the thermal junction maximum temperature is 46.6°C (+1.6°C). 0.87 W is transferred by conduction into the PCB top layer by pin4. The rest (0.13 W) is transferred outside the junction through pins 1-2-3 by conduction or outside the encapsulant by convection (Figure 12a). 0.48 W is transferred into the TIM through the five thermal vias (Figure 12b). We can conclude that using fewer vias has no benefit.

Now with this information, the good layout with 10 thermal vias can be improved. Analysis results shows that the thermal junction maximum temperature is 42.9°C (-2.1°C). 0.90 W is transferred by conduction into the PCB top layer by pin4. The rest, 0.10 W, is transferred outside the junction through pins 1-2-3 by conduction or outside the encapsulant by convection (Figure 13a). 0.71 W is transferred into the TIM through the 10 thermal vias—improved use of the thermal vias (Figure 13b).

These examples illustrate the importance of using a 3D model in thermal simulation to obtain the best design. The top layer of the PCB has the most effect on cooling the IC; thus, the path from the heat source to the thermal vias must be free of "heat bottlenecks." Thermal vias must be placed as close as possible to the heat source (in this case, pin 4). Overall, our thermal simulation illustrates that the number of thermal vias is less important than the quality of placement and layout. **PCBDESIGN**

Gabriel Ciobanu is a thermal design engineer at Continental Automotive in Romania, where he is involved in the development process of creating virtual prototypes and investigating cooling concepts and materials.

Boris Marovic is the technical manager of FloEFD products for the Mechanical Analysis Division at Mentor Graphics, and is based in Frankfurt, Germany.

Team of Robots Learns to Work Together, Without Colliding

When roboticists create behaviors for teams of robots, they first build algorithms that focus on the intended task. But that's where the problems begin.

"When you have too many robots together, they get so focused on not colliding with each other that they eventually just stop moving," said Georgia Tech roboticist Magnus Egerstedt, director of Georgia Tech's Institute of Robotics and Intelligent Machines. "Their safety behaviors take over and the robots freeze. It's impossible for them to go anywhere because any movement would cause their bubbles to pop."

Egerstedt has created a solution. His team's new algorithms allow any number of robots to move within inches of each other, without colliding, to complete their task -- swapping locations on his lab floor. They are the first researchers to create such minimally invasive safety algorithms.

In technical speak, the bots are using a set of safe states and barrier certificates to ensure each stays in its own safe set throughout the entire maneuver.

"In everyday speak, we've shrunk the size of each robot's bubble to make it as small as possible," said Egerstedt. "Our system allows the robots to make the minimum amount of changes to their original behaviors in order to accomplish the task and not smack into each other."

Egerstedt also said something similar to these algorithms could be used for the next generation of air traffic control. Instead of people directing the flow, planes will be given the authority in airspaces.

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TOP TEN

Recent Highlights from PCBDesign007

1 Brooks' Bits: Your Traces Have Hot Spots!

Your traces have hot spots. At least, those that carry a moderate current do. Surprised? Well, Douglas G. Brooks was a little surprised, too, when he looked at this issue a little more closely. One chapter in Doug's latest book focuses on fusing currents, and this month he breaks out the thermocouple.

2 Mentor Graphics Launches New Xpedition Enterprise Platform

Mentor Graphics Corporation has announced the first phase of the new Xpedition PCB flow to address the increasing complexity of today's advanced systems designs. To efficiently manage the density and performance requirements for advanced PCB systems, the new Xpedition flow provides advanced technologies to enable design and verification of 3D rigid-flex structures, and to automate layout of high-speed topologies with advanced constraints.

3 It's Only Common Sense: Mike Wilson, World's Greatest Design Salesman, Has Died

My great friend and business associate, Mike Wilson, passed away last week after a short illness. Mike was indeed the world's greatest PCB design salesperson. Man, he knew everyone in the design world and everyone knew him. The world will be a little less interesting without Mike. For the 25 years I knew Mike, he was always up to something. Mike would say something like, "There's a guy we have to talk to," or "What do you think about doing this?"

4 Beyond Design: The Rise of the Independent Engineer

With the changing demographics, the old-timers in our industry—the master PCB designers—are about to retire and hand over the exacting job of PCB design to the Gen-X and Ys. These generations, shaped by technology, will tackle the most demanding designs without possessing the experience that we veterans benefit from.

5 PentaLogix Implements Ucamco's Gerber X2 in ViewMate and CAMMaster

PentaLogix has completed its Gerber X2 input and output. Working closely with Ucamco, the developer of the Gerber format, PentaLogix has successfully implemented Gerber X2. The output has been fully verified by Ucamco, who confirm it conforms to the X2 specification.

6 EMA Announces Ultra Librarian for OrCAD

EMA Design Automation has announced Ultra Librarian for OrCAD, providing symbols and footprints for over 7 million parts. EMA is currently enlisting select customers to join the early adopter program. These users will be able to try out the solution and provide feedback on functionality, ease of use, speed, and additional capabilities.

7 The Shaughnessy Report: Voices of the Industry

In a survey, we asked readers like you to share some of your thoughts about PCB design, design engineering, and the electronics manufacturing industry in general. We even provided a few helpful "trigger" statements to get your brains firing right, including, "If they would just do this…" The result is the August issue, "Voices of the Industry."

8 Sisoft to Exhibit and Present at EDI CON USA 2016

SiSoft will be exhibiting at the upcoming EDI CON USA 2016 at the Hynes Convention Center in Boston, September 20-22. SiSoft will also be co-presenting, with MathWorks, the technical session "Leveraging SerDes Design Flows for AMI Model Development" during the event Wednesday at 11:30 AM in Room 202.

9 Altium Acquires Perception Software

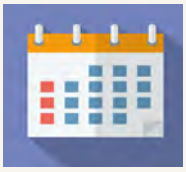
Altium has completed acquisition of Perception Software, a provider of enterprise PLM integration solutions. Perception Software will bring over a decade of enterprise integration expertise and technology to the Altium portfolio.

10 Zuken and Aras Partner to Deliver Ideal EDM/PLM Environment

Zuken and Aras have entered into a partnership to develop a new approach for managing cross-discipline product development processes that include electrical and electronic design data from design creation to manufacturing. The new solution will span enterprise processes across the lifecycle.

PCBDesign007.com for the latest circuit design news and information—anywhere, anytime.

Events



For IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out The PCB Design Magazine's event calendar.

PCB West Conference and Show
September 13–15, 2016
Santa Clara, California, USA

Medical Electronics Symposium
September 14–15, 2016
Marylhurst, Oregon, USA

24th FED Conference
September 15–16, 2016
Bonn, Germany

ICT Evening Seminar
September 20, 2016
Newtown House Hotel, Hayling Island, UK

EDI CON
September 20–22, 2016
Boston, Massachusetts USA

EIPC Workshop on Reliability
September 22, 2016
Tamworth, UK

IPC India/electronica India 2016/ productronica India 2016
September 21–23, 2016
Bengaluru, India

IPC Fall Committee Meetings
September 24–30, 2016
Rosemont, Illinois, USA

SMTA International 2016
September 25–29, 2016
Rosemont, Illinois, USA

Manufacturing Day
October 7, 2016
An annual celebration of modern manufacturing meant to inspire the next generation.

electronicAsia
October 13–16, 2016
Hong Kong

TPCA Show 2016
October 26–28, 2016
Taipei, Taiwan

Electronica
November 8–11, 2016
Munich, Germany

FUTURECAR: New Era of Automotive Electronics Workshop
November 9–10, 2016
Atlanta, Georgia, USA

Printed Electronics USA
November 16–17, 2016
Santa Clara, California, USA

International Printed Circuit & Apex South China Fair (HKPCA)
December 7–9, 2016
Shenzhen, China

DesignCon 2016
January 31-February 2, 2017
Santa Clara, California, USA

IPC APEX EXPO 2017 Conference and Exhibition
February 14–15, 2017
San Diego, California, USA

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