THE PCB December 2012 December 2012 DECEMBER 2012 MAGAZINE

Beyond Design: Interactive Placement and Routing Strategies p.12

Designing for Assembly in Today's Production Environment p.26

The Challenge of Routing High-Frequency Laminate PCBs p.74

ROUTING AND PLACEMENT ISSUE



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FEATURED CONTENT

THE ROUTE TO SUCCESS: There are almost as many placement and routing methods as there are PCB designers. Some designers won't touch an autorouter with a 10-foot pole, while others use them as needed. Many designers take placement and routing preferences to the next level, ensuring that their designs will pass a "beauty contest" every time. If you're in a routing rut, this issue of *The PCB Design Magazine* has the solution!

12 Beyond Design: Interactive Placement and Routing Strategies by Barry Olney

FEATURE SHORT

52 Orange County Designers Council Meeting Draws a Crowd by Andy Shaughnessy



26 Designing for Assembly in Today's Production Environment

by Noah Fenley



FEATURE COLUMN

74 The Challenge of Routing High-Frequency Laminate PCBs



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PCB DESIGN

CONTENTS

AN ONICONNECTOOT PUBLICATION

ARTICLES

36 Designing a PCB Stackup, Part 2 by Lee W. Ritchey



66 Software-Defined Radio: The Driver of Universal Connectivity in the Consumer Space?





SHORTS

19 Agilent Releases **ADS 2012**



- 53 Mentor Graphics Posts Record **Q3** Revenues
- 57 IPC: N.A. PCB Shipments, **Bookings Down in October**

TOP TEN MOST-READ NEWS

- **19 PCB007**
- 53 Mil/Aero007
- 72 PCBDesign007

EXTRAS 76 Events Calendar



77 Advertiser Index & Masthead

COLUMNS

8 2012: The Year in Design by Andy Shaughnessy



- **20** Trace Currents and **Temperature**, Part 2: **Empirical Results** by Douglas Brooks, Ph.D.
- 32 Schematic Diagrams by Jack Olson
- **48** Sexy Software Sells: **User Interface Ranks Higher** than Functionality by Abby Monaco
- 54 How Often Do **You Visit Your Fabricator?** by Amit Bahl



58 The Elements of PCB Library **Construction**, Part 2 by Tom Hausherr



VIDEO INTERVIEWS

- **11 Bay Area Circuits Stresses Design Education**
- 31 PCBs: Not Old-Fashioned **Technology After All**
- 47 Fab and Design Speaking the Same Language
- 71 Intercept's Design Software **Moving Into 3-D**





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THE SHAUGHNESSY REPORT

2012: The Year in Design

by Andy Shaughnessy I-CONNECT007

SUMMARY: Each December, we like to look back over the PCB design news of the past year. The American electronics industry seemed to find more solid ground in 2012, but we're not out of the woods yet. What's ahead for 2013?

Each December, we like to look back over the PCB design news of the past year. What trends were big, and why? Who bought whom?

The American electronics industry seemed to find more solid ground in 2012, but we're not out of the woods yet. What's ahead for 2013? If our leaders in Washington can work out a budget deal (and the world doesn't end in 2012), we just might see real growth next year. There's plenty of pent-up enthusiasm ready to be unleashed.

With that said, we present the PCB design news highlights from January through early December 2012.

January

Mentor Graphics began the year by <u>acquir-</u> ing another CFD software company, the Dutchowned Flowmaster Group. Mentor Graphics also released <u>HyperLynx Version 8.2</u>. This rev added 3D full-wave field solving, and integrated HyperLynx's thermal analysis and power integrity tools.

Was this a good omen? The EDA Consortium reported that EDA industry revenue rose 18% YOY in October 2011, with PCB design tools lagging at 11.6%.

Zuken promoted Steve Chidester to head of international marketing. Patrick Hackney was named senior technical marketing manager for electrical design solutions in Europe and North America, and Aurang Rona was appointed to an international corporate development management role at Zuken. The company also launched a new version of <u>Board Modeler Lite</u> as part of CADSTAR 13.0.



2012: THE YEAR IN DESIGN continues

IPC <u>updated the flex standard IPC-2223C</u>. The new "Sectional Design Standard for Flexible Printed Boards" includes a tutorial and data to help designers of flex circuits.

Bay Area Circuits released a free <u>PCB array</u> <u>calculator and a free desktop Gerber viewer</u> with DFM and quoting capabilities, along with a DXF/DFG-to-Gerber conversion guide.

Joe Fjelstad's newest book, <u>Flexible Circuit</u> <u>Technology, 4th Edition</u>, included a chapter on flex design techniques and guidelines, with plenty of design information contained throughout the book.

February

Intercept Technology <u>launched Pantheon 7</u>, which featured a completely redesigned interface. Pantheon's GUI had not changed since its introduction in the early 1990s.

Zuken released a new version of its E³.WireWorks software, E³.WireWorks Unified.

National Instruments <u>released Multisim</u> <u>12.0</u>, which included analysis functionality developed for NI's LabVIEW system design software.

<u>Mentor Graphics and Altium</u> were among the DesignVision Award winners at DesignCon 2012. Other winners included Molex, Memoir Systems, Akros Silicon, Apache Design and Oscium.

Mikel Williams, president and CEO of DDi and Chairman of the IPC Government Relations Committee, <u>testified before the Commit-</u> <u>tee on Foreign Affairs</u> about the importance of clear and appropriate U.S. export controls on PCB designs for military technologies.

March

Mentor Graphics <u>released PADS 9.4</u>, which featured the ability to associate nets required for DDR interconnect design.

DownStream Technologies <u>released new</u> <u>versions</u> of their PCB post-processing tools, CAM350 and BluePrint-PCB.

AWR Corporation inked a <u>global reseller</u> <u>agreement</u> for AWR to sell and support Modelithics' model libraries.

I-Connect007 provided complete Real Time video coverage of the <u>Designers Forum and IPC</u> <u>APEX EXPO</u> in San Diego.

Altium <u>launched Altium Designer 12</u>, delivered as part of Altium's continuous update model instead of a large software upgrade.

April

I attended the <u>Designers Roundtable at</u> <u>SMTA Atlanta</u>, and I found a dozen PCB designers who were happy to discuss their jobs and answer questions from pesky editors. The biggest takeaway: Despite all the talk about new data formats, every designer used Gerber, though some used Gerber and ODB++, depending on where the design was headed.

The EDA Consortium reported that <u>EDA in-</u> <u>dustry revenue rose 12.8% YOY in Q4</u>, but PCB software revenue fell 15.6% compared to the year-earlier period.

Cadence Design Systems <u>posted first quar-</u> ter 2012 revenue of \$316 million, compared to revenue of \$266 million reported for the same period in 2011.

Zuken joined the ODB++ Solutions Alliance. The company is also a member of the IPC-2581 Consortium.

May

PADS Software founder <u>Gene Marsh died on</u> <u>May 4</u> after a short illness. He was 84.

Cadence <u>expanded its OrCAD Capture Mar-</u><u>ketplace</u>, allowing OrCAD and Allegro users to view and download content through any Webenabled device.

Mentor Graphics posted <u>Q1 revenues of</u> <u>\$247.9 million</u>, and forecast annual revenues of \$1.1 billion.

Australia-based In-Circuit Design Pty Ltd released the <u>FX version of its Stackup Planner</u>, which integrates boundary element method 2D field solver technology into ICD's impedance planning software.

Intercept Technology joined the social media movement, launching sites on YouTube, LinkedIn, Facebook, and Twitter. Does your company use social media?

June

Mentor Graphics <u>released the FloEFD v11.3</u> computational fluid dynamics software for PTC's Creo platform.

My coverage of the Designers Roundtable

2012: THE YEAR IN DESIGN continues

at SMTA Atlanta led to a spirited debate by supporters of Gerber and ODB++. This <u>column by Karel Tavernier of Ucamco</u>, the company that now owns the Gerber format, contains links to previous columns and replies by Julian Coates, Andy Kowalewski, and Jack Olson.

Agilent's collaboration with Thales helped expand X-parameter technology to wideband super-heterodyne receiver applications. Agilent invented X-parameters, a new category of nonlinear network parameters for high-frequency design.

Zuken inked a reseller <u>agreement with Tech-Bridge Solutions</u>. TechBridge will sell Zuken's CADSTAR tools in Massachusetts, Connecticut, Rhode Island, Vermont, New Hampshire, Maine, Washington, Oregon, Idaho, Montana, and parts of Canada. Zuken also named Quadra Solutions European <u>CADSTAR Distributor of</u> <u>the Year</u> for the fourth time.

July

M&A activities continued, with Cadence Design Systems acquiring Sigrity, a provider of signal and power integrity tools. Cadence posted a <u>year-on-year revenue increase</u> for Q2 2012. The company reported Q2 revenue of \$326 million, compared to revenue of \$283 million reported for the same period in 2011.

Zuken released the <u>E³.Series Industry</u> <u>Editions</u>. The E³.series can be configured specifically for the transportation, machinery, mil/aero, power, railway and systems segments.

Mentor Graphics launched a <u>general purpose software</u> solution that combines 1D and 3D computational fluid dynamics.

The EDA Consortium reported that <u>EDA in-</u> <u>dustry revenue increased 6.3% for Q1 2012</u> to \$1.53 billion. PCB design software earnings rose 5.1% year-on-year, to \$147.5 million.

August

In August, I-Connect007 <u>introduced The</u> <u>PCB List</u>, a global directory of fabricators that is searchable by technology, geography, volume, and a variety of other criteria. If you want to have your design built by a fabricator in North America (or anywhere, for that matter), and you'd like to screen companies by materials, surface finishes, average layer count, and delivery time, check out The PCB List. It's free for users.

The <u>ODB++</u> Solutions Alliance exceeded <u>2,000 users</u> and 26 partner members, and developed Japanese and Chinese versions of its website.

Signal Consulting Group launched a <u>soft-</u> ware tool to validate IC vendors' IBIS models. SharkSim allows users to validate IBIS models and build standard CAD model libraries.

Mentor Graphics posted <u>all-time record</u> <u>revenues</u> for Q2 2012, with revenue of \$240.8 million. During the second quarter, Mentor repurchased 1.4 million shares of its stock for \$20 million.

September

Members of the <u>IPC-2581 Consortium</u> <u>fabricated their first-ever PCB</u> by transferring design data in the IPC-2581 format. The 12-layer bare board was designed by Fujitsu Network Communications, and included BGAs, QFPs and SFPs, with components rotated at odd angles.

Cadence <u>released Allegro 16.6</u>, with improved features for CAD team collaboration and increased productivity.

Zuken added <u>support for Xilinx's Zynq-7000</u> <u>All Programmable SOCs</u> within its CR-8000 and CR-5000 tool suites.

DownStream Technologies launched new versions of <u>DFMStream, CAM350, and Blue-Print-PCB</u>.

CadSoft EAGLE PCB design software <u>added</u> <u>Sunstone Circuits</u> as its preferred prototype fabricator.

October

Intercept Technology took home the 2012 <u>New Product Introduction Award</u> at PCB West for its Pantheon design suite. Pantheon received its first GUI overhaul since its introduction in the early 1990s.

SiSoft released three <u>Quantum Channel De</u>-<u>signer design implementation kits</u> for the Intel 89xx Series.

Mentor Graphics held the 24th annual <u>Tech-</u> nology Leadership Awards program. The award

2012: THE YEAR IN DESIGN continues

for Best Overall Design went to Simon Hawkes, Mark Butt, and Kelly Perryman of Selex Galileo in the UK.

In-Circuit Design Pty Ltd (ICD) released a Japanese version of its ICD Stackup Planner. Dynatron Co. Ltd of Tokyo will distribute the Japanese version.

Sunstone Circuits launched its <u>"Share Your</u> <u>Story"</u> contest for PCB designers. <u>Click here</u> to check out some of the stories that designers have posted.

November

Mentor Graphics <u>reported revenue of \$268.8</u> <u>million</u> for the third quarter, a Q3 record.

We <u>launched The PCB Design Magazine</u>. The response from readers has been overwhelming. Isn't it time designers had their own magazine?

ICD released the ICD Stackup Planner and PDN Planner with <u>floating network licenses</u>, available in English, European and Japanese versions. Agilent Technologies released <u>EMPro 2012</u>, its 3-D electromagnetic simulation software.

NBS <u>expanded its design engineering servic</u><u>es</u>. The company began as a PCB design company, and is now an EMS provider.

December

Agilent Technologies shipped <u>Advanced De-</u> <u>sign System 2012</u>, its RF and microwave EDA software platform. ADS 2012 features improved integration with Agilent's EMPro, which enables 3D electromagnetic component designs to be saved for use in ADS.

Have a happy new year! PCBDESIGN



Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 13 years. He can be reached by clicking <u>here</u>.

video interview

Bay Area Circuits Stresses Design Education

by Real Time with... Designers Forum



Bay Area Circuits' Stephen Garcia, VP of operations, and Peter Brissette, sales and marketing, discuss their recent investments in higher technology, including the hiring of their first PCB designer. They also highlight their recent "Pizza, Pop and PCBs" event, which showed local college students how PCBs are manufactured in the "real world," and their dedication to educating the designers of the future.



Beyond Design: Interactive Placement and Routing Strategies

by Barry Olney

IN-CIRCUIT DESIGN PTY LTD, AUSTRALIA

SUMMARY: Cross-probing between the schematic and PCB provides a valuable mechanism for design, review, verification and testing of PCBs, but it is most powerful during interactive placement and routing.

PCB layout is a means to combine your artistic side and your creative skills with the power of automation. I always say that if a PCB design looks good, it will probably work well. However, neatness in routing often leads to unwanted crosstalk as trace segments are routed in parallel for long distances.

Back in the late 1970s, I used Bishop Graphics tape and stick-on pads to create PCB artwork, such as it was. Artwork is still an appropriate name for PCB layout because of the artistic qualities required. Good routing requires the PCB designer to have exceptional 3D spatial skills, a thorough and methodical approach, and a keen eye for detail—and all of the above combined with style.

Interactive Placement

To obtain a high route-completion rate, component placement is extremely important. If the board is difficult to route, it may just be the result of poor placement, slots/gates positioned all over the board, or perhaps the sequence of pins on components are flipped. We need to help the router as much as possible by opening route channels and providing space for vias.

Interactive placement is best done by cross-probing and dragging the components one-by-one from the schematic to place on the PCB—taking functionality and design constraints into account.

During placement, consideration should not only be given to routing, but also to inspection and rework. An 80

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You guys are terrific! I had my proto boards fabricated by you when I worked at Honeywell and you do first class work. Many of those proto designs ended in aircraft from the C-17, Air Force One, to the Presidential Helicopter! Once those designs were proven the production house handled the load. But many of your boards went up 40,000+ feet to start the certification process. Mark, you do great work getting the information we need!

Steve White, Sr. P.C. Designer C.I.D. Verathon Thank you!

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mil minimum clearance is required for rework tools, and an angle of 60 degrees for visual inspection. However, where possible, 45 degrees (i.e., spacing between components = height of tallest component) is a good rule of thumb.

In other words, if a tall electrolytic capacitor is next to a BGA, then the height of the electrolytic is the distance required between components. Along these lines, grouping large, plated, through-hole components together saves board space.

Similar types of components should be aligned on the board in the same orientation for ease of component placement, identification, inspection, and testing. A placement grid of 100 mils is recommended for large components and 25 mils for chip components. Also, similar component types should be grouped together whenever possible, with the net list or connectivity and circuit performance requirements ultimately driving the placements. In memory boards, for example, all of the memory chips are placed in a clearly defined matrix with pin 1 orientation in the same direction for all components. This is a good design practice to carry out on logic designs where there are many similar component types with different logic functions in each package.

On the other hand, analog designs often require a large variety of component types, making it understandably difficult to group similar components together. Regardless of whether the design involves memory, general logic, or analog components, it's advisable to orient pin 1 on all IC components the same, provided that product performance or function is not compromised in the process.

One issue that is always a problem—especially as trace widths and clearance decreaseis the lack of via space. With high-speed design, traces from a BGA fan-out straight to an internal layer to prevent radiation, and this of course requires a via for each BGA ball. This cannot be avoided. But we can open up space for vias on other surface mount devices (SMDs) when using double-sided placement. Figure 2 Illustrates two PLCCs placed on the top of a board with resistor packs on the bottom side. If the lands on the bottom are aligned with the lands on the top, space is cleared for vias and horizontal routing channels are opened. This is not the case when using blind vias, but certainly helps with through-board vias.

A comment regarding autoplacement: One of the most useless features that all EDA layout tools offer is autoplacement. I guess they all have this feature because some bright guy decided to include this in his tools and it then became a checkbox for product comparisons—so everyone has to have it.

Notwithstanding the uselessness for autoplacement's intended purpose, I have found a



Figure 1: Space = height of tallest component.





good use for it—to see if all the components will fit inside the board outline before stating placement. If not, then you can re-evaluate the packaging or reduce functionality to fit the required space.

Cross-probing

Cross-probing, between the schematic and PCB, provides a valuable mechanism for design, review, verification and testing of PCBs, but it is most powerful during interactive placement and routing. Cross-probing is bi-directional, in that you can select parts or nets on the schematic and highlight and identify them on the PCB database, or vice-versa. This feature also gives you the ability to drive the router directly from the schematic design. Figure 3 illustrates a schematic to PCB cross-probe of a component.

Cross-probing can also be used as a powerful search tool—locating parts and nets on the schematic or PCB. And, cross-probing is not limited to schematic and PCB. AutoVue, for instance, allows the cross-probing between PCB and 3D MCAD tools, enhancing mechanical visualization of the product. When an engineer creates the schematic he invokes a logical process, typically, grouping components into blocks or sheets that functionally go together. When the PCB designer then places these components, he should also use a logical, sequential process by placing functional components near each other, optimizing trace cross-overs and lengths, keeping constraints in mind.

In years past, I recall having to place components by select list. This seemed logical but the PCB designer was never to know whether they were placing a trivial static pull-up resistor or a critical terminator. Resistors are just resistors—unless you know what they do. This is the beauty of cross-probing. The functionality of the circuit is displayed and each and every component can be placed by functionality and importance—providing error-free transfer of the intended schematic functionality to the design.

Of course, design rules can also be added to the schematic to pass this information on to the PCB designer, but a picture is worth a thousand words.



Figure 3: Cross-probing between schematic and PCB.

Interactive Routing

Proper component placement is an important aspect of routing. If the board is difficult to route, it may just be the result of poor placement. So before you start routing, it is important to check the placement and design rules to ensure that there are no issues that may prevent the route completion. The easiest way to check this is to turn the autorouter loose and see how it goes. If you do not get at least 85% completion on this first test route, then you may need to tweak the placement, look at more appropriate packaging, adjust the design rules, and possibly drop some functionality to improve routability.

However, there are some important things to do before you commence with the process of formally routing the board:

1. The stackup should be planned to ensure that controlled impedance signals have been calculated correctly and that the return current for each signal layer has a clear return path. The ICD Stackup Planner can be used to analyze the stackup (download from <u>www.</u> icd.com.au), and help you with material selection, along with input from your fabricator. The resulting stackup configuration should then be transferred to the design rules to define the correct trace width and clear-

ance for each layer, and to specify the differential pairs.

2. The power distribution network (PDN) should be planned, and bypass and decoupling capacitors placed in the appropriate positions. The ICD PDN Planner is an ideal sandbox for analyzing this. It is a good idea to color the power nets with individual colors so that they can easily be recognized without having to name the net. Altium has a great feature, which displays the net name for each net, making identification of power nets extremely clear.

3. Design rules and constraints can be passed from the schematic, which automatically sets the design rules in the PCB database—though there is always some adjustment to be done on the PCB side. Via sizes for different net classes need to be defined. This is important for route completion. (Please see my previous article on PCB Design Techniques for DDR, DDR2 & DDR3, Part 1 and Part 2 for a complete list of the appropriate design rules for DDR2 routing.) For rules to properly support the design process, they need to be defined in the correct priority so that the most important rules prevail over rules of lesser importance.

4. Set up the routing options. It amazes me that all the EDA tools that I have used do not come with the router set to the most useful functions straight out of the box. So before

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Example of a Test Scenario



18 layer, .085" thick (2.16 mm), buried and single stack vias. 2 lamination cycles (1+N+1) This design has passed:

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- 10x solder floats @ 288°C (unconditioned)
- 10x reflow @ 260°C (JEDEC std. lead-free cycle) ,
- 6x 260°C preconditioning before 1000 cycles IST @ 150°C followed by 100 cycles @ 190°C
- T260 passed more than 30 min
- (Magnified @ 100x) CTEz (50-260°C) of 3.1%



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routing, one must tweak the route options to get the tool to do what you want. Details vary by tool, of course, but the nuisance is nearuniversal.

Once we have the above set, then it is time to start interactive routing. The real power of cross-probing is driving the router from the schematic. Starting with the most critical nets, cross-probe in the following sequence:

1. Select the components on the schematic and fan-out on the PCB selecting the appropriate pattern. Adjust the fan-out as necessary. The rules should be set such that power traces are routed thick (10 - 20 mils) to reduce inductance. And, each GND and VCC should have its own individual via to the plane—avoid connecting two or more GNDs to the one via.

2. Obviously, matched length, differential pair and critical signals that have specific requirements should be routed first. Fix or lock these traces so they cannot be inadvertently moved.

3. Select the most critical nets, a few at a time, on the schematic and route in the PCB. Adjust the routing as necessary then move on to the next group of nets and so on. In this way you can build up an excellent route in a short time and it is all controlled from the schematic. Feel free to jump in and tweak the routing to your liking.

Once the routing is complete, apart from running design rule checks (DRCs), I like to run a sanity check on the board. I can either do this in the simulation environment or in the PCB database. Simply highlight each net one by one—it is tedious, but gets results. You can quickly see if there are any nets that are longer than the Manhattan length or spiral around the board three times before termination.

Points to Remember:

• Component placement is an important aspect of routing. If the board is difficult to route, it may just be the result of poor placement.

• Components should be placed in functional blocks.

• An 80-mils minimum clearance is required

for rework tools, and an angle of 60 degrees for visual inspection. A good rule of thumb: Spacing between components = height of tallest component.

• Similar types of components should be aligned on the board in the same orientation. A placement grid of 100 mils is recommended for large components, and 25 mils for chip components.

• Align lands on the bottom with the lands on the top to open up space for vias.

• Check the stackup, PDN, design rules and routing parameters before interactive routing.

• Run a test autoroute, targeting at least 85% completion.

• Cross-probing, between the schematic and PCB, provides a valuable mechanism for design, review, verification and testing of PCBs, but it is most powerful during interactive placement and routing.

• Cross-probing can also be used as a power-ful search tool.

• The real power of cross-probing is driving the router from the schematic. Start with the most critical nets—then continue to lower-priority nets.

• Finally, run a sanity check on the board. Simply highlight each net one by one. You can quickly see if there are any nets that are longer than the Manhattan length. **PCBDESIGN**

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1. Advanced Design for SMT—Barry Olney

2. <u>Beyond Design: Intro to Board-Level Sim-</u> <u>ulation and the PCB Design Process</u>—Barry Olney

3. <u>PCB Design Techniques for DDR, DDR2 &</u> <u>DDR3, Part 1 & 2</u>—Barry Olney

4. The ICD Stackup and PDN Planner can be downloaded from <u>www.icd.com.au</u>



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. ICD is a PCB design service bureau specializing in board-level simulation. The company developed the ICD Stackup Planner and ICD

PDN Planner software.



Viasystems' PCB Segment Posts Sales of \$269.5M in Q3

"Our reported net sales of \$327.4 million for the quarter were within our projected range of \$325 to 335 million," noted Viasystems' CEO David M. Sindelar. "The previously-reported fire in our Guangzhou factory late in the quarter had only an estimated \$5 to 7 million adverse impact on the quarter's billings, thanks in large part to the facts that, first, we hold finishedproduct inventories for the benefit of many of our customers and, second, we were able to utilize our other factories to meet customers' demand.

BBG SV Acquires PCB Fabrication Operations of Hunter Tech

Bare Board Group (BBG) is excited to announce the formation of a Silicon Valley-based subsidiary (BBG SV) and the acquisition of Hunter Technology's PCB fabrication operations. This acquisition makes BBG a manufacturer with internal and direct offshore sourcing and fabrication capabilities.

TTM Posts Improved Q3 Results; Q4 Looks Promising

"As expected, third quarter results were affected by the continued challenging demand environment in some of our end markets, including our largest—networking and communications," said Kent Alder, president and CEO of TTM. "Performance in our Asia Pacific segment was less robust than anticipated primarily due to later than expected orders for several customer programs."

RENA Revamps Hoellmueller PCB/PCM Business Unit

RENA has announced corporate structure changes by the acquisition and introduction of a new business

segment—clean and waste water treatment—by integrating SH+E GROUP, as well as via the strengthening of existing segments, including, semiconductor, medical technology, and printed circuit board/photochemical machining (PCB/PCM).

IPC: N.A. PCB Shipments & Bookings Down in September

"PCB sales in September continued below 2011 sales, but improved over the preceding month," said Sharon Starr, IPC director of market research. "Sharp declines in flexible circuit orders over the past three months pushed the overall PCB book-to-bill ratio below parity, but the volatility of the flex business means this effect will probably be short-lived."

Endicott Interconnect Earns Zeta Certification

Integral Technology, Inc. has announced that Endicott Interconnect Technologies, Inc. is the latest PCB fabricator to receive the prestigious Zeta® Certification. This certification allows Endicott to produce circuit boards using Integral's revolutionary dielectric films.

Spirit Circuits Secures LED PCBs Contract

Spirit Circuits is proud to announce their recent business win to supply for LED Lighting Solutions of Southport. The new order will ultimately be used to supply LED PCBs to a major retail chain. This is a significant win for Spirit and will be worth circa $\pounds 1$ million over the three-year period. This is a real triumph for the Waterlooville-based PCB manufacturer who is beginning to be acknowledged in the LED lighting industry for their unique offering of MPCBs.

Agilent Releases ADS 2012

Agilent Technologies Inc. has shipped Advanced Design System 2012, its flagship RF and microwave EDA software platform.

ADS 2012 features new capabilities that improve productivity and efficiency for all applications the system supports and breakthrough technologies applicable to GaAs, GaN and silicon RF power-amplifier multichip module design. New ADS capabilities include an electro-thermal simulator that incorporates dynamic temperature effects to improve accuracy in "thermally aware" circuit-simulation results, as well as updated load pull and amplifier design guides,

which offer mismatch simulation and make it easy to see amplifier performance at a specific output power level.



BROOKS' BITS

Trace Currents and Temperature, Part 2: Empirical Results

by Douglas Brooks, Ph.D.

ULTRACAD DESIGN INC.

SUMMARY: In this second of a four-part series on trace currents and temperature, Douglas Brooks explores various results that have been empirically obtained. Subsequent parts will explore how we can use the melting temperature of a trace to our advantage, and how to deal with vias.

The first part of this series (available here) ended with two models for analysis, Equations 6 and 7, repeated here as Equations 1 and 2. Equations 1 and 2 have been modified slightly from those in Part 1 by the inclusion of a proportionality constant, k. Recall that the difference between Equations 1 and 2 is the inclusion of form factor in the latter, by breaking the area term into its width and thickness components.

$I = k^* \ \Delta T^{\beta 1}$	* Α ^{β2}	[Eq. 1]
$I = k^{\star} \Delta T^{\beta 1}$	* W ^{β2} * Th ^{β3}	[Eq. 2]

Where I = current $\Delta T = change in temperature$ A = area W = trace widthTh = trace thickness



Empirical Testing

I have tested this model with three sets of data. The first is the *original IPC data* we all know and love. Most of us know it by IPC-2221, "Generic Standard on Printed Circuit Board Design." Its curves were also published as IPC-D-275. Mike Jouppi has spent considerable time and effort in reviewing this data and resurrecting significant aspects of its history ^[1]. Perhaps most notable was the following:

- 1. The data were first published in 1955 under NBS Report 4283. It was known that there were some variables that needed further study, so the original charts were labeled "Tentative."
- 2. Further studies were never funded.
- 3. The original charts were redrawn and republished many times through the years, and the word "Tentative" was dropped somewhere along the way.
- 4. Although the original tables included curves for both external and internal traces, data were taken only for external traces. The data for internal traces were derived simply by derating the data for external traces by 50%.

There are several shortcomings to this original data. One in particular is the lack of information contained within the charts reflecting the form factor of the traces under study.

A second set of empirical data was found in an article by Friar and McClurg, published in Design News back in 1968^[2]. There are two reasons to include this data in an analysis. First, there are not many sources of published data to choose from! Second, the data purport to analyze the relationship including the form factor of the traces. This data will be referred to in this column as the *Design News* data or simply by the initials *DN*.

20 The PCB Design Magazine • December 2012





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TRACE CURRENTS AND TEMPERATURE, PART 2: EMPIRICAL RESULTS continues

Finally, IPC has recently published a new (fully revised) standard, IPC-2152 "Standard for Determining Current Carrying Capacity in Printed Circuit Board Design (August 2009)." Mike Jouppi, among others, was very instrumental in creating this new standard. The main body of the standard has a Figure (5-1) which is representative of all traces. Well over 100 charts are included in the Appendix for readers who want to fine tune the results in varying ways. This standard purports to take form factor into consideration (something that can be derived from the charts in the Appendix).

Empirical results will be shown for these three data sources.

Procedure for Analysis

While original, detailed data is difficult to come by; charts are readily available for all three sources. Therefore, it is possible to read data points off the charts. Statistical regression analysis can be used with these data points to estimate and derive the underlying relationships and equations. This would have been somewhat difficult a generation ago, but modern spreadsheets now provide very powerful statistical analysis capabilities that allow us to do things like this easily.

There is the underlying question of whether the charts can be read with enough precision to proceed. While there will certainly be errors in reading the data points, there are three compelling factors that allow us to proceed:

- 1. Errors will be relatively minor.
- 2. More importantly, errors should be randomly distributed, and therefore will not add any bias into the results.
- 3. The magnitude of the errors can be inferred from various statistical measures, in particular the standard errors (and R² values) of the analyses.

These topics are beyond the scope of this column, but people with a statistical background will recognize what is said here and be comfortable with the approach.

Empirical Results

The empirical results for the three data sources are shown in Equations 3 through 8.

IPC 2221:	$I = .065 * \Delta T^{.43} * A^{.68}$	[Eq. 3]
IPC 2221: (expanded	I) I = .065 * $\Delta T^{.43}$ * W ^{.67} * Th ^{.68}	[Eq. 4]
DN	L 040 * AT45 * A 69	[[
DN	$I = .040 \text{ m} \Delta I^{113} \text{ m} A^{103}$	[Eq. 5]
DN (1 oz., 5 oz.)	$I = .028 * \Delta T^{.46} * W^{.76} * Th^{.54}$	[Eq. 6]
(2 oz.)	$I = .034 * \Delta T^{.46} * W^{.76} * Th^{.54}$	[Eq. 6a]
IPC 2152 (air):	$I = .063 * \Delta T^{.50} * A^{.58}$	[Eq. 7]
IPC 2152 (air)(exp):	$I = .070 * \Delta T^{.51} * W^{.57} * Th^{.47}$	[Eq. 8]

Looking first at the results that do not consider form factor, Equations 3, 5, and 7, two things are apparent. First, the exponents for the terms are pretty close for each source. They are not exact, but considering all the variables involved, they are very close. This means we can have a fairly high degree of confidence in the shape of the curves. By that I mean that the curves from each data source seem to have roughly the same slopes and curvatures.

On the other hand, the proportionality factors ("k" in the equations) are, at least in some cases, remarkably different, especially for the DN data. The proportionality factor defines the location of the curves (as opposed to the shape of the curves). The result is that we can have confidence in the shape of the curves, but not as much in the location of the curves.

When we look at form factor information (Equations 4, 6, and 8), we see several things. First, Equations 3 and 4 for the original IPC data are virtually identical. That is, there is no form factor information whatsoever. This is not unexpected, since independent data for form factor was not collected. And this fact is readily apparent in the result.

In the DN data, however, there is a significant difference in the shapes of the curves involving form factor. Thus, the DN data implies form factor is very important. There is also an anomaly in the DN data. The data for 1-oz and 5-oz traces follow almost identical curves (Equation 6), but the 2-oz curves (Equation 6a) have a significantly different proportionality constant. There is no obvious explanation for this, but I suspect it reflects a lack of control over the test procedures for 2-oz traces. More on that later.

The results for the current IPC data seem to follow in between the other two results. The differences between Equations 7 and 8 seem to

TRACE CURRENTS AND TEMPERATURE, PART 2: EMPIRICAL RESULTS continues

suggest that including form factor makes a difference in the results, but the difference is not as pronounced as in the DN case.

Potential Reasons for Differences

There are differences in the test procedures in the three cases. But not all the differences are reported or known. Some of the differences are shown in Table 1.

The test boards were hung vertically in the original IPC study, but placed horizontally in the DN study. I believe the current IPC test procedure follows the early study's procedure. Mike Jouppi has shown that it can take up to five minutes for a trace to stabilize after a change in current ^[3]. Reportedly the early study procedure only allowed the temperature to stabilize for 30 seconds. The time is not reported in the DN study. Interestingly, the DN data is more conservative ^[4] than the early IPC data, consistent with a longer stabilization time for the DN data. The stabilization time for the current IPC data is not reported, but I am told there was "sufficient time" for the temperature to stabilize.

Perhaps the most significant difference in test procedure is the method in which the trace

	Old IPC	DN
Test Board	Vertical	Horizontal
Temperature Measurement	Change of Resistance	Infrared Microscope
Stabilization Time	30 Seconds	??

Table 1: Some differences in test procedures in the three data sources.

temperature measurement is made. The IPC studies infer the temperature by the change in resistance. Refer back to Part 1 of this series for a discussion of the thermal coefficient of resistivity (i.e., how resistance changes with temperature). The DN study reportedly infers the change in resistance using an infrared microscope.

Both approaches are legitimate ways to measure temperature, but they sometimes may measure different things. The change in resistance approach measures the average temperature across the entire cross-sectional area and length of the trace, while the infrared microscope mea-



Figure 1: Differences in temperature measurement.

brooks' bits

TRACE CURRENTS AND TEMPERATURE, PART 2: EMPIRICAL RESULTS continues

sures the temperature at a precise spot along the surface of the trace. One might argue that the infrared approach might result in higher overall measurements than the change in resistance approach. This would also be consistent with the fact that the DN results are more conservative ^[4] than the PC results.

Finally, each temperature measurement approach has its own inherent parameters that must be controlled or calibrated. The change in temperature approach requires a fairly precise knowledge of the thermal coefficient of resistivity for the trace material. This parameter is highly dependent on the particular alloy of copper used. On the other hand, the infrared approach is highly dependent on the reflectivity of the surface of the material being tested. Typically infrared microscopes must be calibrated before each measurement. Errors in adjusting for the reflectivity can significantly impact the results. One might speculate that this might be one reason why the 2-oz DN results are so different from the 1-oz and 5-oz results.

Rationality of the Results

Here is an interesting exercise. Take the results for the form factor equations (Equations 6 and 8), rearrange terms, approximately square both sides (e.g., $(W^{.57})^2$ is approximately W), and recognize that A = W * Th, and that R $\approx 1/A$. The last line in the table shows the results.

The IPC data suggests that the change in temperature is directly proportional to $i^{2}R$ (i.e., heating only). The DN results suggest that the change in temperature is directly proportional to $i^{2}R$ and inversely proportional to the square root of the width (i.e., heating and cooling). The DN results are more consistent with our form factor model introduced in Part 1 of this series.

What is the Truth?

So what is the truth here? Which equations are correct? Those of us in engineering always want to know what the answer is! Well, here's my take: Beats the heck out of me!

Here are some considerations:

- 1. The DN data fit the form factor model better. That is comforting.
- 2. We will see in Part 3 that the DN data also fit the fusing current models better, although there will be some qualifications to that statement when we make it.
- 3. The current IPC data were taken under probably the best controlled conditions

	IPC 2152	Design News
Look at the form of the result:	l ≈ k * ∆T ^{:51} W ^{.57} Th ^{.47}	l ≈ k * ∆T ^{.46} W ^{.76} Th ^{.54}
Rearrange terms:	∆T ^{.51} ≈ k * l / W ^{.57} Th ^{.47}	∆T ^{:46} ≈ k * l / W ^{.76} Th ^{.54}
<i>Approximately</i> square both sides:	∆T≈k*l²/W*Th	∆T≈ k * l² / W¹.5Th
Recognize A = W*Th	∆T≈k*l²/A	∆T≈ k * l² / A*W ^{.5}
Further, $\mathbf{R} \approx 1/\mathbf{A}$	$\Delta T \approx k * l^2 R$	∆T≈ k * l ² *R / W ^{.5}

Table 2: An interesting exercise.

TRACE CURRENTS AND TEMPERATURE, PART 2: EMPIRICAL RESULTS continues

UltraCAD Design Inc. PCB Trace	Calculator
Units, Samesian Trace Distancions Model Oreck to come If English (* Metric Model Solve Solve Model Thick-asse (* Units) * Use decemd fractions GMD? If Sam Effect Temperature Date Fusing Carent If solve Date * Durants Solve Solve Model Current Solve Solve Anget Current Solve Solve Model Tempe rotuce Date Fusing Carent If solve Date * Date Source to be used	der
Thickness **Use decend fractions CMCV* C Units C Units © Dunces Fuseg Caneet Temperature Data Fuseg Caneet Data State Caneet State Tempe OHANSE State Tempe OHANSE State Data Source to be used	7
Temperature Data Puering Current Trace Data * Nite width and thickness taxwel Current Solve S Angen Use Model Temp OHANSE Solve 20.33 oC ? Data Source to be used ? IPC 2152 Air Informal	
Use width and Buckness (sees above) Canneri Solver Same Solver Same Solver Same Solver Same Solver Same Solver Solver Solver	Ohris Law Editolety
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Cosyright 2010 UltraCAD Design. Inc. Ballenve, WA. USA	Regional Settings

Figure 2: UltraCAD's PCB Trace Calculator.

ever, by responsible researchers, with the most resources devoted to this type of investigation. They ought to be the most reliable.

4. Perhaps most importantly, the original IPC data have passed the test of time for over 55 years!

Bottom line: There are many factors that impact the trace temperature relationships. While we can be pretty comfortable with the shape of the relationship, the location of the curves (i.e., the proportionality constant) depends on so many things that there may not be a universal truth. As uncomfortable as that sounds, that may be the practical reality.

Calculator

UltraCAD has released a calculator based on Equations 3 through 8 that can be used to make trace temperature calculations^[5]. Five different data sources can be used for evaluation, the current IPC-2152 data for internal or external traces in air and for traces in a vacuum, the original IPC data (from IPC-D-275) or the Design News data. The user can enter any three of four parameters (width, thickness, current, and temperature change) and the calculator will calculate the fourth. The calculator also has provision for including the skin effect, if that is a consideration ^[6].

In Part 3 of this series we will look at fusing current, the amount of current necessary to just melt a trace. **PCBDESIGN**

References

1. "Current Carrying Capacity in Printed Circuits, Past, Present, and Future," presented at IPC Printed Circuits Expo, March 25, 2003.

2. "Printed Circuits and High Currents," Friar, Michael E. and McClurg, Roger H., Design News, Vol. 23, December 6, 1968, pp. 102 - 107.

3. "Thermal Characterization of Electrical Conductors in Multi-Layer Printed Wiring Boards in Space Environments," Michael R. Jouppi, staff engineer, Lockheed Martin, Denver, Colorado.

4. "Conservative" in this context means that a given change in temperature is associated with a smaller current with the DN data than with IPC data.

5. Available for download at <u>www.ultracad.</u> <u>com</u>. Click on menu item "Calculators."

6. See my column series on skin effect here.



Douglas Brooks has an MS/EE from Stanford University and a Ph.D. from the University of Washington. He has spent most of his career in the electronics industry in positions

of engineering, marketing, general management, and as CEO of several companies. He has owned UltraCAD Design Inc. since 1992. He is the author of numerous articles in several disciplines, and has written articles and given seminars all over the world on signal integrity issues since founding UltraCAD. His book, Printed Circuit Board Design and Signal Integrity Issues was published by Prentice Hall in 2003. Visit his website at www.ultracad.com.



By Noah Fenley ACD

ACD

SUMMARY: The layout designer should create each product with ease of assembly in mind. The easier the product is to assemble, the cheaper the final product. In order to design the best assembly, the designer needs to understand the fabrication limitations of the components and the fabrication shop. The layout designer is a mediator between the requirements of the engineer, the fabrication shop abilities and the needs of assembly.

To build a successful assembly, it is imperative to understand the concept behind design for assembly (DFA). Often, this includes the constant challenge of balancing assembly, fabrication and layout, all of which must cooperate for a smoothly run process. It is necessary also to understand the requirements and limitations of each of the three elements. This is where the layout designer comes into play.

The layout designer should create each product with ease of assembly in mind. The easier the product is to assemble, the cheaper the final product. In order to design the best assembly, the designer needs to understand the fabrication limitations of the components and the fabrication shop. The layout designer is a mediator between the requirements of the engineer, the fabrication shop abilities and the needs of assembly.

The Role of DFA

DFA is more than simply placing components at a safe distance from one another. Today's small-pitch components push the limits of fabrication tolerances. For proper footprint development, it is crucial to understand the fabrication shop's minimum soldermask webbing. Additionally, copper land patterns should take soldermask webbing into account. Oversizing the width of the pin footprint should not eliminate the soldermask webbing. Soldermask ganging combining the pins into one soldermask opening—increases the likelihood of shorts between the pins during assembly. Therefore, it is best to avoid ganging soldermask whenever possible.

Vias are a major factor in testability and DFA. Vias that are too close to a pin do not allow soldermask webbing. The absence of the webbing will starve the solder from the pin. The paste will travel through the via and short components on the opposite board. Vias should be exposed for testability. Adequate clearance from pins allows test probes to reach the via and al-



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Figure 1: Solder bridge caused by an inadequate soldermask between a pad and via on the opposite side of the board.

lows a soldermask web. Vias are a concern for cold solder joints as well. On a multi-lamination board with four or more ground fills, a direct connect via can absorb the heat into the planes and cause cold solder joints.

Figure 1 shows a solder bridge caused by inadequate soldermask between a pad and via on the opposite side of the board. The pin also suffered from solder starvation since the solder was wicked away from the pin. The solder that was wicked away caused a short found under the connector in the image. Shorts of this nature are difficult to find since components must be removed to debug.

Consider connector placement. Allow ample room for mating connection and room to allow removal. Not all connectors are a single plug-in. A common mistake is to place a component too close to a connector. The component blocks the end user from removing the connection. Even placing components on the edge of the board requires space. SMAs and several other connectors require wrenches or other tools to connect them correctly (Figure 2).

Silkscreen is used for orientation and debug. A good silkscreen will indicate the shape of the component, the orientation and any necessary labeling. Labels should be legible and not covered by other components. The end-user needs to be able to identify any connectors, switches, or indicators for debug or configuration. The silkscreen is used during the layout portion to



Figure 2: A tool is needed to correctly connect this component to the edge of the board.



Figure 3: Using silkscreen during layout determines the physical placement of components.

determine the physical placement of the components. Accurate silkscreen will prevent component conflicts during assembly (Figure 3).

Importance of Footprint Accuracy

Footprint inaccuracy is the single most destructive mistake a layout designer or engineer can make. The component specs are not standardized. Footprint drawings are not always to scale. Some specs are drawn from a bottom view as opposed to a top view. Many components do not fit on the manufacturer-recommended footprint.



Figure 4: Pin pitch, shown here, is covered by the DFA check.



Figure 6: Seen here, pin type, component spacing, pin toe and heel are all covered by the DFA check.



Figure 5: DFA check covers row pitch, shown here.

The controlling dimensions are not always clear.

Using a CAD tool built to verify footprints can save schedules and rework. These tools have the ability to build a model to the dimensions of the component. The tool is able to overlay the model of the physical component over the footprint generated in the design tool. Using the latest spec ensures that the component is the latest revision.

The DFA check covers pin pitch (Figure 4), row pitch (Figure 5), pin type, component spacing, pin toe and heel (Figure 6), pin width (Figure 7), as well as providing overall assembly review.

Any one of these items can delay a schedule or cause unattractive rework on a board. Many



Figure 7: DFA check also covers pin width, seen here.

of the issues will scrap a complete lot of fabrication (Figure 8).

Pin pitch mistakes typically are made during the conversion from mils to mm or vice versa. The other error made is not identifying the correct controlling dimensions. The majority of mechanical drawings will include the controlling dimensions. Pin pitch is a cumulative error. On low-pincount items it rarely is a problem. The more pins a device contains, the larger the cumulative error becomes. For example, 0.5 mm converted to mils equals 0.019685". A common mistake is to round up to .020" or 20 mil, with the difference being 0.000315". The difference is not enough in a 6-pin device to cause assembly issues. On a 48-pin de-



Figure 8: Incorrect footprint vs. component selected.

vice, however, the difference grows to .007". Now the pin no longer fits on the intended pad.

Row pitch does not suffer the same ability for cumulative errors except on multi-row/column components. Ball grid arrays (BGA) and connectors should be built in the original dimensions. Row pitch on quads can force a designer to use smaller pads on the corners or increase the toe while decreasing the heel of the solder joint.

Typically, pin type mistakes are made during component look-up or a late BOM change. The manufacturer part specs are accurate between SMT and through-hole pins. The conflict arises on mounting holes. Many manufacturer specs do not indicate if the mounting pins are plated or non-plated. Press fit pins require a tighter tolerance and should be noted in the fabrication and assembly drawings. Component spacing affects the initial placement and the effort level of rework. BGAs require room for rework or the surrounding components will need to be removed before the BGAs can be removed.

Pin toe and heel are critical for a solid solder joint. According to Texas Instruments' solder pad recommendations for surface mount devices, "The criteria for a well-designed solder joint is based on both empirical data and reliability testing. Solder joint strength is directly related to the total solder volume. An observable solder fillet is evidence of proper wetting. Therefore, a



Figure 9: Texas Instruments MicroStar spec illustrates how to create an even solder ball.

positive solder fillet is usually specified. A joint can be described by the solder fillets formed between the device pins and the PCB pads."¹

Pin width also is a factor to consider. The expected assembly process will help determine the width variations for the pin width increase. Wave solder boards will need a wider pad than reflow boards. A major concern when making the pads wider is the soldermask webbing. The soldermask webbing between the pins prevents shorts.

BGA Pin Size

BGA soldermask and routing on the assembled side can destroy assembly yields. The smaller the BGA pin pitch, the more crucial the soldermask becomes. The Texas Instruments MicroStar BGA spec illustrates how to create an even solder ball for the strongest BGA joint (Figure 9).

The majority of the manufacturer's drawings do not show the actual pin diameter, but rather the ball diameter. The MicroStar spec can be used as a guide to design the pin size for BGAs (Figure 10). Some manufacturers have started using the pin size instead of the ball size. These few specs match with the MicroStar spec guidelines. Once the pad is the correct size, the routing must be considered as well for reliable assembly. Gang routing the powers and/or grounds will cause the ball to deform. The shape change will cause shorts and opens on the BGAs. Each pin should



Non-Solder-Mask-Defined Land

Ball Pitch	X DIA.	Y DIA.	Stencil Th	Stencil DIA.
0.5 mm	0.25 mm	0.30 mm	120 µm	0.25-0.30 mm
0.8 mm	0.35 mm	0.50 mm	150 µm	0.35-0.40 mm
1.0 mm	0.40 mm	0.55 mm	150 μm	0.45-0.50 mm

Figure 10: The MicroStar spec can be used as a guide to create the pin size for BGAs.

have a via to allow a low inductive path and to prevent the ball from deforming.²

Conclusion

DFA is a continuous process in which assembly, fabrication and layout must all work together. Understanding the requirements of each is key to creating a successful, smoothly running assembly. The layout designer plays an important role in this, acting as a mediator between the engineer, fabrication shop and assembly needs. **PCBDESIGN** References

¹<u>www.ti.com/lit/an.pdf</u> ²<u>www.ti.com/lit/wp.pdf</u>



Noah Fenley, CID, is a design manager at ACD. Contact Fenley at noah.fenley@acdusa.com.

video interview

PCBs: Not Old-Fashioned Technology After All

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Noted author and blogger Brian Bailey discusses some of the many characteristics that the worlds of ICs and PCBs have in common, and why PCBs should not be considered old technology after all.



CONNECTING THE DOTS

Schematic Diagrams

by Jack Olson

SUMMARY: Last month, the schematic was introduced as the method of recording and sharing electronic ideas. This month, Jack explains the guidelines and conventions that will make schematics easier to interpret.

The Schematic

Over the years, we have developed ways to control the flow of electricity for many useful purposes. These techniques can be recorded and shared by using diagrams called schematics. A schematic diagram is a convenient and informative method for documenting electronic circuitry.

Anyone who understands basic electronic theory can explain the following schematic, no matter what language he speaks:

The basic building blocks of schematic diagrams use a set of standardized symbols to represent different component types. In the schematic shown above, the symbol next to the BT represents a battery, the symbol next to the S represents a switch, and the one next to DS represents a display or a lamp. The letters BT, S, and DS are labels that help identify the

component, and these labels are called reference designators.

Anyone who knows how to interpret the schematic can build the circuit it represents by connecting a battery, a switch and a lamp together with wire or any other form of conductive material.

In addition to reference designators, symbols are also assigned numbers to differentiate components of the same type. For example, if more than one resistor is added to a schematic, they will be labeled R1, R2, R3, etc.

When you are ready to learn more, a more

complete list of symbols and reference designators can be found in the publications IEEE-STD-315 and IPC-2612.

Values and Attributes

In the example schematic, there is not enough information to know what is intended. The components are identified by a reference designator (the letters BT, S and DS), but there is no information about what type or what size the components should be. Consider the fact that there are many different types of batteries available, but nothing in the schematic above suggests which battery would be best. The circuit shown above could be:

- a simple flashlight with a size AA battery, or
- a 9V battery, a doorbell button and a buzzer, or
- a 12V car battery, a rotary switch and a headlamp

Applying the same basic circuit to these different applications illustrates the fact that in the

> real world, a schematic must provide more information. A schematic must include attributes to insure that appropriate components are selected. The same resistor symbol can be used for thousands of different kinds of resistors, so to be useful it

must declare the value, expressed in ohms. The ohm symbol is usually dropped because it is not available in all character sets, so a resistor with

For you trivia fans, the reference designator "U" originally meant "unrepairable."



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SCHEMATIC DIAGRAMS continues

the number 100 next to it would be interpreted as "a hundred ohm resistor." Other types of components are described with different terms; capacitors are differentiated by their value in farads (F), inductors are differentiated by their value in Henrys (H).

Many additional attributes can be added to symbols, such as power ratings or tolerances, to more tightly control the type of component needed for the design.

In addition to visible attributes for each symbol, many CAD systems can also assign hidden attributes such as manufacturer part numbers, cost, revision levels or simulation data. Although a discussion of various CAD capabilities is beyond the scope of this tutorial, sophisticated libraries can be developed with them, and schematics created from them can become very powerful tools.

International Units

Attributes can have a wide range of values, from very small to extremely large. To avoid filling diagrams with long repeating strings of zeros for values like 1,000,000,000 or .0000000001, the world has converged on an <u>International</u> <u>System of Units</u>.

The SI units you are likely to see on schematics are:

SI UNITS

Prefix	Symbol	Value	
tera	Т	1 000 000 000 000	
giga	G	1 000 000 000	
mega	М	1 000 000	
kilo	k	1 000	
	(none)	1	
milli	m	.001	
micro	u	.000 001	
nano	n	.000 000 001	
pico	р	.000 000 000 001	

Some examples:

- a .000027 Farad capacitor would be expressed as 27 microFarads, written as 27 uF
- a .05 Henry inductor would be expressed as 50 milliHenrys, written as 50 mH
- a 10,000,000 Ohm resistor would be expressed as 10 megaOhms, written as 10 M (most CAD systems don't use the ohm symbol)

You can get more information about the International System of Units (SI) from the <u>Na-</u> <u>tional Institute of Standards and Technology</u> (NIST). They maintain a very good website and the document that describes SI in detail can be found in the Bibliography (online publications and citations) as "Special Publication 811."

Schematic Design Guidelines

The schematic provides enough information to select appropriate components and connect them together during the circuit board design phase. Schematics also provide a basic level of documentation for electronic products, and become useful tools during design reviews, testing and debugging, field service, technical manuals, etc. Here are some guidelines for creating good schematic diagrams:

• Lines connecting symbols together represent electrical connections between components. Lines that cross each other are NOT connected.

• A connection dot is used to show connections between lines that touch, but it is better not to have four wires that connect at a point (don't have lines that cross AND connect). In other words, a connection dot will typically have three line segments attached to it.

• In a complex circuit, if every power and ground net were shown connected together with lines, the diagram would be too cluttered, and more difficult to interpret. Instead of showing them connected with lines, we use GLOBAL SYMBOLS. Anything connected with the same global symbol, even across multiple sheets, is assumed to be connected together. • If other connections need to be made without connecting lines together (across multiple sheets, for example) net names can be used. Any net labeled with the same net name is connected.

• All text (pin numbers, net names, polarity, values and attributes) should be horizontal and clearly labeled to avoid confusion. No overlapping text, No lines crossing through text.

• Circuits should flow from left to right and top to bottom. What this means is, try to keep inputs on the left and outputs on the right, and try to keep positive voltage supplies above and ground symbols below.

• Try to design schematic sections in functional blocks. Symbols are placed on the page to facilitate an understanding of the circuit, NOT to show where they are physically located on the board or to show which connections should be long or short.

• Don't try to fill the whole sheet, and don't be afraid to leave empty areas or open spaces.

• Align similar circuit symbols vertically or horizontally. You might not have time to make everything as beautiful as you wish, but schematics should be easy to read and unambiguous. It may be helpful to use a grid if your CAD tool supports it.

• Pin numbers should be on the outside of the symbol graphic. Net names can be placed inside the graphic if practical.

• If sheet connection symbols are used, they should be placed on the extreme left edge or extreme right edge of the page.

• Depending on the conventions of the company or customer, you may have to provide additional information such as an IC Power Table, or a list of spare gates. These are often placed on the last sheet.

• The first sheet should contain a title block in the lower right corner. At minimum it should contain the Part number, Title, Revision Level and the name of the person who created it. Titles should be distinctive enough to differentiate the design from other similar designs. (You don't want to end up with dozens of designs named "Amplifier," for example.) Subsequent sheets may have a reduced title block, but must contain a sheet number and some Definition of the Month: SCHEMATIC DIAGRAM A drawing that shows, by means of graphic symbols, the electrical connections, components, and functions of a specific circuit arrangement.

method of identifying it as belonging to the design (at least the part number and revision level).

Final Advice

None of these guidelines are set in stone, and no two companies do things exactly the same way. Try to learn your customers' preferences as quickly as you can. If you are new, the first thing you should do is study some of their existing drawings. Some companies use "D" as the reference designator for LEDs, while others use "LED." Some use a little circle for test points, but some use that symbol for voltages. Some use a rotated connector symbol for voltages. It doesn't really matter as long as it is clear and consistent. After you have some experience you can suggest ways to standardize if you think it will help.

Finally, if you move to a new company and they do everything differently, don't bother saying, "Well, at my last company, we did it this way." Chances are, they won't care. **PCBDESIGN**



Jack Olson, C.I.D.+, has been designing circuit boards fulltime for over 20 years. He would like to thank the United States Navy for teaching him the basics.

Designing a PCB Stackup, Part 2



by Lee W. Ritchey SPEEDING EDGE

SUMMARY: Designers can no longer rely on the traditional practice of allowing fabricators to design their PCB stackups. In Part 2 of this tutorial on designing PCB stackups, Lee Ritchey discusses laminate thicknesses and methods for calculating and testing impedance, and examines each step of the stackup design process. <u>Click here</u> for Part 1.

Laminate and Pre-Preg: What is the correct thickness?

As can be seen in Figure 5, laminate can be purchased with many different thicknesses, the thinnest being 2 mils or 51 microns for this material. Pre-preg is available as thin as 2.5 mils or 63.5 microns. There are two considerations when deciding how thin either of these should be. The first consideration is minimum breakdown voltage between circuits of different polarity. Virtually all laminates based on epoxy or phenolic have breakdown voltages of at least 1,000 volts per mil of thickness. In almost all products that contain logic circuits, the breakdown voltage requirement is 1,500 volts DC or less. All of the laminates listed in Figure 5 will meet this specification.

The second consideration is associated with pre-preg and the fact that its thickness decreases during lamination because some of the resin in the pre-preg will flow into the voids in the adjacent signal and power layers. As this takes place, the copper features in the adjacent plane and signal layers will be pressed into the resin and glass of the pre-preg, diminishing the final thickness to such an extent that shorts may result if the original thickness is not adequate. From experience I have found that the starting thickness for pre-preg must be at least 3 mils to prevent this type of failure. Some fabricators have learned from experience that a minimum of two plies of the 106 pre-preg are needed to guarantee short-free PCBs. I have found that a single ply of 2113 works very well between adjacent plane layers that are intended to create interplane capacitance for the power delivery system (PDS). Accounting for the thickness decrease in the pre-preg during lamination will be discussed later in this document.
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- Improved Z-axis CTE 2.70%
- I-Speed IPC 4101 Rev. C /21 /24 /121 /124 /129

- Offer spread and square weave glass styles (1067, 1086, 3313, etc.) for laminates and prepregs
 - Minimizes micro-Dk effects of glass fabrics

Servers

- Enables the glass to absorb resin better and enhances CAF capabilities
- Improves yields at laser and mechanical drilling
- A low Df product with a low cost of ownership



Effective Loss @ 4 GHz on a 32 inch line



I-Speed delivers 15-20% lower insertion loss over competitive low Df products.

The data, while believed to be accurate and based on analytical methods considered to be reliable, is for information purposes only. Any sales of these materials will be goveremed by the terms and conditions of the agreement under which they are sold.







Core	Standard	Resin	Dk	Dk	Dk	Dk	Dk	Dk
Thickness	Constructions	s Content	at 100 MHz	at 500 MHz	at 1 GHz	at 2.0 GHz	at 5.0 GHz	at 10.0 GHz
0.0020	1-106	70	3.30	3.29	3.29	3.28	3.24	3.24
0.0027	1-1080	60	3.52	3.51	3.51	3.51	3.47	3.47
0.0030	1-1080 63		3.45	3.45	3.44	3.44	3.40	3.40
0.0035	2-106	66	3 39	3 38	3 38	3 37	3 33	3 33
0.0035	1-2113	51	3.74	3.74	3.73	3 73	3.70	3 70
0.0040	2-106	70	3.30	3.20	3.20	3.28	3.24	3.24
0.0040	1-3070	19	3.80	3.70	3.70	3.78	3.75	3.75
0.0040	1-3313	45	3.00	3.15	2.62	3.00	3.75	3.75
0.0043	106/1080	55	3.64	3.04	3.03	3.65	3.33	3.35
0.0045	106/1080	02	3.40	3.4/ 2.4E	3.47	3.40	3.42	3.42
0.0045	2 1080	63	3.45	3.45	3,44	3.44	3.40	3.40
0.0050	100/0142	57	3.59	3.59	3.58	3.58	3.54	3.54
0.0050	100/2113	55	3.64	3.64	3.63	3.63	3.59	3.59
0.0050	1-1652	43	3,96	3.95	3.93	3.94	3.92	3.92
0.0055	1-1652	47	3.85	3.84	3.84	3.84	3.81	3.81
0.0060	1080/2113	54	3.67	3.66	3.66	3.65	3.62	3.62
0.0060	106/ 1080	70	3.30	3.29	3.29	3.28	3.24	3.24
0.0065	1080/2113	57	3.59	3.59	3.58	3.58	3.54	3.54
0.0070	1080/2116	58	3.57	3.56	3.56	3.55	3.52	3.52
0.0070	2-2113	52	3.72	3.72	3.71	3.70	3.67	3.67
0.0075	2 - 3313	52	3.72	3.72	3.71	3,70	3.67	3.67
0.0080	2-3070	49	3.80	3.79	3.79	3.78	3.75	3.75
0.0100	2-1652	43	3.96	3.95	3.93	3.94	3.92	3.92
0.0100	3-1080	66	3.39	3.38	3.38	3.37	3.33	3.33
0.0100	2-2116	54	3.67	3.66	3.66	3.65	3.62	3.62
0.0120	2-2113/ 1652	48	3.82	3.82	3.81	3.81	3.78	3.78
0.0140	2-2116/1652	47	3.85	3.84	3.84	3.84	3.81	3.81
0.0160	3-1652	46	3.88	3.87	3.87	3.86	3.83	3.83
0.0180	2-3070/2-1652	2 46	3.88	3.87	3.87	3.86	3.83	3.83
0.0210	2-2116/2-1652	2 50	3.77	3.76	3.76	3.76	3.72	3.72
_		ISC	DLA IS 6201 L	AMINATE IN	FORMATIO	N		
Prepreg	Resin	Thickness	Dk	Dk	Dk	Dk	Dk	Dk
	Content	(In)	at 100 MHz	at 500 MHz	at 1 GHz	at 2.0 GHz	at 5.0 GHz	at 10.0 GHz
106	75	0.0025	3.20	3.19	3.19	3.18	3.14	3.14
2113	58	0.0042	3.57	3.56	3.56	3.55	3.52	3.52
3313	54	0.0036	3.67	3.66	3.66	3.65	3.62	3.62
3070	55	0.0046	3.64	3.64	3.63	3.63	3.59	3.59
1652	51	0.0061	3.74	3.74	3.73	3.73	3.70	3.70
	alle de							
Prepreg	Resin	Thickness	Df	DI	Df	DI	Df	Df
106	Content	(in)	at 100 MHz	at 500 MHz	at 1 GHz	at 2.0 GHz	at 5.0 GHz	at 10.0 GHz
1080	65	0.0025	0.0046	0.0050	0.0056	0.0058	0.0066	0.0073
2113	58	0.0042	0.0051	0.0054	0.0058	0.0060	0.0066	0.0071
3313	54	0.0036	0.0052	0.0055	0.0059	0.0060	0.0066	0.0071

ISOLA IS 620I PREPREG INFORMATION

0.0055

0.0051

0.0053

Figure 5: Typical resin information.

3070 2116

A caution about 2 mil laminate: Sanmina owns a series of patents for a material called ZBC[®] which is 2 mils thick, intended to create interplane capacitance for the PDS. When stackups are created with planes separated by 2 mils that don't specifically call out ZBC, there is a potential for legal proceedings initiated by Sanmina for violating their patents. In fact, the patents have been shown to be invalid (Reference 6). My solution to this problem is to design stackups that have pre-preg between plane pairs, thus avoiding the use of 2 mil laminates altogether.

0.0046

0.0061

Laminate Glass Weave Styles

One column in Figure 5 is labeled "standard construction." The numbers in this column refer to particular styles of woven glass cloth. Pictures of these glass cloth styles are shown in Reference 4. It has been shown that certain types of glass weave have an adverse effect on high-data-rate differential signals. The degradation takes the form of differential skew and is described in References 2 and 5. When stackups are being designed for data rates of 2.4 Gb/S and higher, it is imperative that these glass styles be avoided next to signal layers. The three glass styles that have been shown to cause this kind of problem are 106, 1080 and 7628. Two new glass weaves, 1067 and 1086, are "flat weaves" that replace 106 and 1080, respectively. These do not cause skew problems.

0.0060

0.0060

0.0059

0.0066

0.0071

Selecting the Proper Copper Foil Thickness

Copper foils are used as the conductive layers for a PCB. Virtually all copper foil used for this purpose is manufactured by a plating process rather than by rolling out the copper in the manner of aluminum foil. The reason is that it produces superior electrical characteristics, as well as better ductility. Foils are produced in a variety of thicknesses. The primary thicknesses are 0.5 ounce, 1 ounce and 2 ounces. A thickness of 1 ounce is equivalent to 1.4 mils thick. (This odd method of specifying foil thickness has its origins in the gold leaf business, where thickness was specified by the number of ounces of metal spread out over one square foot of area.) Due to process variations, the nominal thicknesses when finally used in a PCB are 0.5 mils, 1.2 mils and 2.6 mils, respectively.

Copper foils are used for two purposes in a PCB: to form plane layers and to form signal layers. The stackup designer must balance foil thickness such that the copper is thick enough to perform properly as a conductor on the one hand, and thin enough to allow accurate etching of features such as traces and plane clearances on the other.

When selecting foils for signal layers, it is desirable to select as thin a foil as possible in order to optimize accurate etching of traces and thick enough to form good signal conductors. Figure 6 is a plot of trace resistance vs. trace width for



Figure 6: Trace resistance vs. foil thickness and width.



Figure 7: Skin depth vs. frequency.

various foil thicknesses. This chart can be used for the trace cross-section calculations required to conduct DC current for traces used for connecting power to loads.

Virtually all transmission lines operate at frequencies where skin effect losses determine the thickness of the copper in a trace. Figure 7 is a plot of skin depth versus frequency. Skin effect loss is defined as the increase in apparent trace resistance as frequency increases due to the fact that the current does not flow throughout the entire conductor, but flows only near the surface. A complete treatment of this phenomenon is contained in several books on microwaves and RF. Skin depth is defined as the depth at which 67% of the current flows. Below this depth only 33% of the current is flowing and at twice this depth 90% of the current is flowing.

From Figure 7, it can be seen that at 100 MHz skin depth is approximately 0.25 mils or 6 microns and at 1 GHz it is approximately 0.075 mils or about 1.8 microns. Since nearly all modern logic features rise times less than 200 pSec, which has an equivalent frequency on the order of 2 GHz, it is easy to see that trace thickness does not need to be more than 0.5 ounce copper or 0.6 mils (15.2 microns) to be thick enough so that skin effect loss dominates over bulk resistance of the trace. So it does not improve signal integrity to use copper thicker than 0.5 ounces in signal layers.

Designing stackups using 0.5 ounce copper in the signal layers has the benefit that trace width accuracy is improved significantly which

results in more precise impedance control because etching can be done with more precision than with thicker copper foils. Trace width control on inner layers using 0.5 ounce copper can be done to an accuracy of ± 0.5 mils.

For the reasons described above, I have been designing PCB stackups using 0.5 ounce copper signal layers for the last 10 or more years with excellent results.

Selecting foil thickness for power and ground layers is a balancing act between providing enough copper to conduct the currents in the PDS and optimizing manufacturability. Chapter 33 of Reference 3 describes how to calculate voltage drops in power and ground planes as a method of determining minimum copper thickness for planes based on expected current flows.

It is likely that planes will be paired backto-back with signal layers across pieces of laminate. Both sides of these pieces of laminate are etched at the same time during the manufacturing process. If the thickness of the copper on the two sides is not the same, it will be difficult to accurately form features on both sides. For example, if a plane layer is one ounce copper paired with a signal layer of 0.5 ounce copper across a piece of laminate, etching long enough to properly form the features in the plane layer will usually result in overetching the signal layer, resulting in impedance errors. Yes, some fabricators claim they have the ability to etch the two sides accurately because their etching equipment sprays etchant on the two sides at different rates. My experience has been that the level of control is not adequate to form features on both sides. The result has been impedance errors.

In order to guarantee good process control and impedance accuracy, it is advisable to design stackups with plane layers that are the same thickness as the signal layers. With modern point-of-load-regulators near their loads, it is reasonable to use 0.5 ounce plane layers.

Calculating Impedance

There are several ways to calculate the impedance of a PCB trace. Among these are various equations that have been developed to allow calculation using simple math and a fixed set of dimensions, as well as a variety of software tools that use Maxwell's Equations to precisely calculate impedance for any trace shape that can be imagined. These software tools are known as field solvers, and they are often an integral part of a signal integrity tool such as Hyperlynx from Mentor Graphics or Allegro PCB Si from Cadence Design Systems.

All of the equations used to calculate impedance were developed by constructing a large number of PCBs, measuring the impedance of their traces and then cross-sectioning the PCBs to determine the dimensions that produced each impedance value. Curve fitting was then used to arrive at an equation that predicted the impedance. These equations are said to have a sweet spot where they are accurate. Outside this sweet spot, results are uncertain.

Field solvers employ precise equations to calculate impedance regardless of the makeup of the transmission line. Figure 8 shows the results of calculating the impedance of surface microstrip, buried microstrip and stripline transmission lines using equations (the square curves) vs. the results using field solvers (the diamond curves).

The conditions used for Figure 8 are: Trace height above the nearest plane – 5 mils (127 microns), trace thickness – 1.4 mils (36 microns) and a relative dielectric constant of 4. SMS denotes surface microstrip, EMS microstrip, and CSL centered stripline.



Figure 8: Impedance results, equations vs. field solvers.

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As can be seen in Figure 8, in most cases the equations predict impedances that are significantly different from that of field solvers. The exception is the stripline equation vs. the field solver. The reason? The stripline equation was developed for the dimensions used in this example.

From experience using field solvers for hundreds of PCB designs and comparing final PCB impedance to that predicted by field solvers, I have observed that the solvers accurately predict impedance within our ability to measure it. Therefore, the difference between what the solvers predict and what the equations predict is an indicator of the accuracy of the equations. Some equations are very inaccurate and should not be used.

Therefore, field solvers should be the only tools used to calculate impedance. If a fabricator or designer uses equations instead of a field solver, the result should be validated prior to using it to construct PCBs.

Measuring Impedance

Impedance is a characteristic of a transmission line. It is expressed in ohms and is a measure of the resistance to the flow of energy along the transmission line. Impedance is different from resistance. Resistance is a DC characteristic, while impedance is an AC characteristic, meaning that it is visible only with an alternating current signal. Therefore, measuring impedance cannot be done with an ordinary ohmmeter as is the case with resistance.

There are a number of ways to measure impedance. Among them are with a TDR (time domain reflectometer), a network analyzer or an impedance bridge. The most common method of measuring impedance is with a TDR, and it is used by virtually all fabricators who make controlled impedance PCBs.

The basic principle behind the TDR is that it sends a fast rising edge pulse down a 50-ohm cable into the transmission line under test and observe how much, if any, of the energy in the pulse is reflected back to the source. If no energy reflects back, the impedance of the transmission line under test is the same impedance as the cable or 50 ohms. If some energy is reflected back and is the same polarity as the



Figure 9: TDR test waveforms.

original pulse, the transmission line impedance is higher than that of the test cable (Figure 9).

If the reflected energy is in the opposite direction of the original pulse, the impedance of the line under test is lower than that of the test cable.

The ratio of the reflected pulse to the original pulse can be used to calculate the impedance of the line under test. This is the basic principal employed by all impedance testing TDR equipment.

Impedance Test Structures

In order to verify that the desired impedance goals have been met in the final PCB, some form of test structures must be provided to allow measuring the impedance of each layer with an impedance specification. One way to do this is to use actual signal traces in each layer. The problem with this method is providing access to traces with a ground via nearby to which the probe is attached. A second problem is indicating the test access location for each layer.

An alternative to this is to provide a test coupon with impedance test traces for each layer. These test coupons are detached from the PCB as it is routed from the panel on which the PCB was built. There are two problems with this method. The trace widths in the coupon may not be the same as in the PCB itself, and the test coupons are often lost and cannot be found when needed.

A way to get around the above problems is to design impedance test traces into the body



IMPEDANCE TEST COUPON DESCRIPTION

Figure 10: Typical impedance test traces.

of the PCB itself. Figure 10 is an example of one way to do this. Notice that there is a ground via next to the via attached to each test trace. The dimensions shown fit the most common test probe systems. It is not necessary to have an access via at the end of each trace. If the design rules for designing differential signal paths in Reference 2 are used, namely that the spacing between members of a differential pair is enough that there is no interaction, it is not necessary to provide differential test structures, because all traces will be the same impedance. Make sure to mark these test points on the silkscreen with the layer numbers to facilitate rapid testing.

Impedance Accuracy

There are three places where impedance accuracy comes into play. These are: calculating initial impedance, measuring impedance and the accuracy of the PCB fabrication process. My experience is that when accurate dielectric values are used with field solvers, the predicted impedance is within the ability of the tools to measure it. The measurement tools can measure impedance to an accuracy of $\pm 0.5\%$. The fabrication process is capable of yielding impedances within $\pm 10\%$ without incurring any premium charges over uncontrolled impedance PCBs. Requesting impedance accuracy tighter than $\pm 10\%$ is possible, but with substantial premiums added to the PCB price.

Steps for Designing a Stackup

From the preceding discussion, designing a proper PCB stackup might seem a bit confusing. These are the steps I go through when designing a stackup. As mentioned early in this paper, I prefer the stackup approach shown on the right side of Figure 4 when the number of signal layers is beyond two. Here are the steps I take:

1. Set the height of the signal layers above their plane partners as thin as is practical to yield good manufacturing results. This is 3 or 4 mils (76 or 102 microns) for most good fabricators.

2. Choose copper thickness for each layer that meets the signal integrity needs and is easy to manufacture.

3. Choose a glass style for these pieces of laminate that will result in uniform impedance and good differential pair performance at high data rates. (This will be laminate that does not include 106 or 1080 glass.)

4. Set the trace width to yield the proper impedance.

5. Set the trace-to-trace separation to meet crosstalk goals.

6. Set the thickness between planes to the thinnest pre-preg that will result in good yields. (Thin is good for power delivery, meaning high interplane capacitance.)

7. Set the thickness between signal layers and between L2 and the surface and Ln-2 and the surface to meet the overall thickness goal. (Variations in the thickness of these pieces of pre-preg have an effect on trace impedance, but it is far smaller than variations in the thickness of the laminate between the trace layers and their nearest planes. See Figure 3 for an example.)

Once you have selected the laminate and pre-preg that meet all of these goals, they must be recorded on the stackup drawing so that multiple fabricators don't build different PCBs. In

Figure 5, notice that there are three different choices for a 4-mil piece of laminate and three for 5 mils. The properties of these can be quite different, so listing only 4-mil or 5-mil dimensions on the stackup drawing is not enough to guarantee two fabricators will build the board the same way. I have had a number of students attend my classes because their fabricator was changed from prototyping to production, and the production PCBs did not work. On investigation, it was determined that each fabricator used different laminate, but all of the same thickness.

Figure 11 is an example of a complete stackup drawing showing all parameters necessary to assure repeatability. It is imperative that the exact glass styles used in each part of a stackup be listed on the stackup drawing.

ayer # 1 2 3 4 5 6 7	Material Name FR-408HR FR-408HR FR-408HR FR-408HR FR-408HR	Material Type Prepreg Core Prepreg Core Prepreg	Material Construction	Material Unpressed Er (at ~2 GHz) 3.7 3.6 3.63 3.7	Material Pressed Er (at ~2 GHz)	Material Unpressed Thickness (mils) 3.7	Material Pressed Thickness (mils) 0.7 3.5	Picture Solder Mask	Copper Thickness (mils) 2 2 0.6	Copper Thickness (oz) 1.5 0.5		Single Ended Trace Width (mils)	Single Ended Imped. (ohms)
1 2 3 4 5 6 7	FR-408HR FR-408HR FR-408HR FR-408HR FR-408HR FR-408HR	Prepreg Core Prepreg Core Prepreg	1 x 3313 RC = 53 8% 1 x 1086 RC = 58% 1 x 2113 RC = 57% 1 x 3313 RC = 53.8%	3.7 3.6 3.63 3.7		3.7	0.7	Solder Mask	2.2	1.5	1	4.5	51.0
1 2 3 4 5 6 7	FR-408HR FR-408HR FR-408HR FR-408HR FR-408HR FR-408HR	Prepreg Core Prepreg Core Prepreg	1 x 3313 RC = 53.8% 1 x 1086 RC = 58% 1 x 2113 RC = 57% 1 x 3313 RC = 53.8%	3.7 3.6 3.63 3.7		3.7	3.5	Solder Mask Prepred	2.2 0.6	1.5 0.5	1000	4.5	51.0
2 3 4 5 6 7	FR-408HR FR-408HR FR-408HR FR-408HR FR-408HR	Prepreg Core Prepreg Core Prepreg	1 x 3313 RC = 53 8% 1 x 1086 RC = 58% 1 x 2113 RC = 57% 1 x 3313 RC = 53.8%	3.7 3.6 3.63 3.7		3.7	3.5	Prepred 2	0.6	0.5	1	4.5	51.0
2 3 4 5 6 7	FR-408HR FR-408HR FR-408HR FR-408HR	Core Prepreg Core Prepreg	1 x 1086 RC = 58% 1 x 2113 RC = 57% 1 x 3313 RC = 53.8%	3.6 3.63 3.7				200 2	0.6	0.5		4.5	51.0
3 4 5 6 7	FR-408HR FR-408HR FR-408HR FR-408HR	Core Prepreg Core Prepreg	1 x 1086 RC = 58% 1 x 2113 RC = 57% 1 x 3313 RC = 53.8%	3.6 3.63 3.7			26						
3 4 5 6 7	FR-408HR FR-408HR FR-408HR	Prepreg Core Prepreg	1 x 2113 RC = 57% 1 x 3313 RC = 53.8%	3.63			3.5	Core			-		
4 5 6 7	FR-408HR FR-408HR	Core	1 x 3313 RC = 53.8%	3.03		-	2	3	0.6	0.5			
5 6 7	FR-408HR	Core Prepreg	1 x 3313 RC = 53.8%	3.7	-	4	3	Prepreg	0.6	0.5	-	_	
5 6 7	FR-408HR	Prepreg	and the second second second				4	Core	0.0				
6	FR-408HR	Prepreg			3	2		5	0.6	0.5		4	49.5
6 7	ED 400UD		1 X 3313 RC = 53.8%	3.7	-	4	3.4	Prepreg	0.0	0.5	-	_	10.5
7	PR. ALDONN	Core	1 x 3313 BC = 53.8%	37			4	6	0.6	0.5		4	49.5
-	Traduorine a	0010	1 x 0010 R0 - 00.070	9.1	-			Core 7	0.6	0.5			1
	FR-408HR	Prepreg	1 x 2113 RC = 57%	3.63		4	3	Prepreg					8 2
8								8	0.6	0.5			
0	FR-408HR	Core	1 x 3313 RC = 53.8%	3.7			4	Core	0.0	0.5			10.6
9	ER.408HR	Drenren	1 X 3313 PC = 53.8%	37		4	34	9	0.0	0.5		4	49.5
10	11-400111	riepieg	17,351510 - 55,57	5.1		4	0.4	Prepred 10	0.6	0.5	-	4	49.5
	FR-408HR	Core	1 x 3313 RC = 53.8%	3.7			4	Core				_	
11	1			C				11	0.6	0.5			
10	FR-408HR	Prepreg	1 x 2113 RC = 57%	3.63	-	4	3	Prepreg	0.0	0.5	-		-
12	ER.408HR	Core	1 × 3313 RC = 53.8%	37		-	4	12	0.0	0.5		_	
13	11-100111	COIC	1 x 001010 - 00.00	0.1			-	13	0.6	0.5		4	49.5
	FR-408HR	Prepreg	1 X 3313 RC = 53.8%	3.7		4	3.4	Prepreg			-		
14							_		0.6	0.5	-	4	49.5
16	FR-408HR	Core	1 x 3313 RC = 53.8%	3.7			4	Core	0.6	0.6	_		
10	FR-408HR	Prepreg	1 x 2113 BC = 57%	3.63		4	3	Dranson	0.0	0.0			
16		rickieg		0.00				Prebled 16	0.6	0.5	-		
	FR-408HR	Core	1 x 3313 RC = 53.8%	3.7	-	2	4	Core	-		1		
17	FD 40014D	0	× 2010 DO - 50 0W	0.7				17	0.6	0.5	_	4	49.5
18	FR-408HR	Prepreg	1 X 3313 RC = 53.8%	3./		4	3.4	Prepreg	<- 06	0.5	-	4	49.5
	FR-408HR	Core	1 x 3313 RC = 53.8%	3.7	2	-	4	Core	0.0	0.0		-	40.0
19	to theme a	1000		-				19	0.6	0.5	-		3
	FR-408HR	Prepreg	1 x 2113 RC = 57%	3.63		4	3	Prepreg					
20		Core	1 + 1088 80 - 588	2.0	-		25	20	0.6	0.5			
21	rn-400mR	Core	T X 1000 RC = 30%	3.0			3.5	Core 21	0.6	0.5	-	45	51.0
	FR-408HR	Prepreg	1 x 3313 RC = 53.8%	3.7		3.7	3.5	Prepreg			-	1.9	
22		-						22	22	1.5	-		
	9	1		-		3	0.7	Solder Mask					2
-				-			76.0	02.4	16.4		-		
				-			Material	92.4	Copper	-			
							Thickness	Total Thickness	Thickness				
	7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 21 22 20 21 22	FR-408HR 8 FR-408HR 9 FR-408HR 10 FR-408HR 11 FR-408HR 12 FR-408HR 13 FR-408HR 14 FR-408HR 15 FR-408HR 16 FR-408HR 17 FR-408HR 18 FR-408HR 19 FR-408HR 20 FR-408HR 21 FR-408HR 22 FR-408HR 23 FR-408HR 24 FR-408HR 25 FR-408HR 26 FR-408HR 27 FR-408HR 28 FR-408HR 29 FR-408HR 20 FR-408HR 21 FR-408HR<	FR-408HR Prepreg FR-408HR Core FR-408HR Prepreg FR-408HR	FR-408HR Prepreg 1 x 2113 RC = 57% 8 FR-408HR Core 1 x 3313 RC = 53.8% 9 FR-408HR Core 1 x 3313 RC = 53.8% 10 FR-408HR Core 1 x 3313 RC = 53.8% 10 FR-408HR Core 1 x 3313 RC = 53.8% 11 FR-408HR Core 1 x 3313 RC = 53.8% 12 FR-408HR Prepreg 1 x 3313 RC = 53.8% 13 FR-408HR Prepreg 1 X 3313 RC = 53.8% 14 FR-408HR Prepreg 1 x 3313 RC = 53.8% 15 FR-408HR Core 1 x 3313 RC = 53.8% 16 FR-408HR Core 1 x 3313 RC = 53.8% 17 FR-408HR Prepreg 1 X 3313 RC = 53.8% 18 FR-408HR Prepreg 1 X 3313 RC = 53.8% 19 FR-408HR Prepreg 1 x 3313 RC = 53.8% 19 FR-408HR Core 1 x 3313 RC = 53.8% 20 FR-408HR Core 1 x 3313 RC = 53.8% 21 FR-408HR	FR-408HR Prepreg 1 x 2113 RC = 57% 3.63 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 FR-408HR Prepreg 1 x 2113 RC = 57% 3.63 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 FR-408HR Prepreg 1 X 3313 RC = 53.8% 3.7 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 FR-408HR Prepreg 1 x 2113 RC = 57% 3.63 FR	FR-408HR Prepreg 1 x 2113 RC = 57% 3.63 8 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 9 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 10 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 10 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 11 FR-408HR Prepreg 1 x 2113 RC = 57% 3.63 12 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 13 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 14 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 15 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 16 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 17 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 18 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 19 FR-408HR Prepreg 1 x 2113 RC = 57% 3.63 <	FR-408HR Prepreg 1 x 2113 RC = 57% 3.63 4 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 FR-408HR Prepreg 1 X 3313 RC = 53.8% 3.7 4 FR-408HR Prepreg 1 X 3313 RC = 53.8% 3.7 4 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 FR-408HR Prepreg 1 x 2113 RC = 57% 3.63 4 FR-408HR Prepreg 1 x 2113 RC = 57% 3.63 4 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 FR-408HR Prepreg 1 X 3313 RC = 53.8% 3.7 4 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 FR-408HR Prepreg 1 x 2113 RC = 57% 3.63 4 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 <	FR-408HR Prepreg 1 x 2113 RC = 57% 3.63 4 3 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 3 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 3.4 FR-408HR Prepreg 1 X 3313 RC = 53.8% 3.7 4 3.4 I0 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 3.4 I1 FR-408HR Prepreg 1 x 2113 RC = 57% 3.63 4 3 I2 FR-408HR Prepreg 1 X 313 RC = 53.8% 3.7 4 3.4 I3 FR-408HR Prepreg 1 X 3313 RC = 53.8% 3.7 4 3.4 I4 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 3.4 I5 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 4 I6 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 4 I6 FR-408HR Core	FR-408HR Prepreg 1 x 2113 RC = 57% 3 63 4 3 Prepreg 8 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 3.4 9 9 FR-408HR Prepreg 1 X 3313 RC = 53.8% 3.7 4 3.4 Prepreg 8 9 FR-408HR Prepreg 1 X 3313 RC = 53.8% 3.7 4 3.4 Prepreg 9 10 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 11	FR-408HR Prepreg 1 x 2113 RC = 57% 3.63 4 3 Precrea 8 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 3.4 Precrea 9 0.6 9 FR-408HR Prepreg 1 X 3313 RC = 53.8% 3.7 4 3.4 Precrea 9 0.6 10 FR-408HR Prepreg 1 X 3313 RC = 53.8% 3.7 4 3.4 Precrea 10 0.6 11 A A 3.63 4 3 Precrea 10 0.6 12 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 3.4 Precrea 11 0.6 13 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 3.4 Precrea 12 13 0.6 14 FR-408HR Prepreg 1 X 3313 RC = 53.8% 3.7 4 3.4 Precrea 14 0.6 15 0.6 15 0.6 15 0.6 15 0.6 15 0.6 16 0.6 17 0.6 17 <td>FR-408HR Prepreg 1 x 2113 RC = 57% 3 63 4 3 Prepred 0 0 8 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepred 0 0.6 0.5 9 FR-408HR Prepred 1 X 3313 RC = 53.8% 3.7 4 3.4 Prepred 0 0.6 0.5 FR-408HR Core 1 X 3313 RC = 53.8% 3.7 4 3.4 Prepred 0 0.6 0.5 FR-408HR Core 1 X 3313 RC = 53.8% 3.7 4 3.4 Prepred 10 0.6 0.5 FR-408HR Core 1 X 3313 RC = 53.8% 3.7 4 3 Preorce -</td> <td>FR-408HR Prepred 1 x 2113 RC = 57% 3.63 4 3 Prepred 0 0.6 0.5 8 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 4 0 0.6 0.5 9 FR-408HR Prepred 1 x 3313 RC = 53.8% 3.7 4 4 0 0.6 0.5 10 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 3 Prepred 1 0.6 0.5 1 11 FR-408HR Core 1 x 313 RC = 53.8% 3.7 4 3 Prepred 1 0.6 0.5 1 12 FR-408HR Core 1 x 313 RC = 53.8% 3.7 4 3 Prepred 1 0.6 0.5 1 1 0.6 0.5 1 1 0.6 0.5 1 1 0.6 0.5 1 1 0.6 0.5 1 1 0.6 0.5 1 1 0.6 0.5 1 1 0.6 0.5 1 1 0.6 0.5 1<td>FR-408HR Prepreg 1 x 2113 RC = 57% 3.63 4 3 Prepreg 0.05 0.05 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 0.66 0.5 4 9 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 0.66 0.5 4 10 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 1 0.6 0.5 4 11 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 1 0.6 0.5 4 12 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 1 0.6 0.5 4 13 R.408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 1 0.6 0.5 4 14 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 1 0.6 0.5 4</td></td>	FR-408HR Prepreg 1 x 2113 RC = 57% 3 63 4 3 Prepred 0 0 8 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepred 0 0.6 0.5 9 FR-408HR Prepred 1 X 3313 RC = 53.8% 3.7 4 3.4 Prepred 0 0.6 0.5 FR-408HR Core 1 X 3313 RC = 53.8% 3.7 4 3.4 Prepred 0 0.6 0.5 FR-408HR Core 1 X 3313 RC = 53.8% 3.7 4 3.4 Prepred 10 0.6 0.5 FR-408HR Core 1 X 3313 RC = 53.8% 3.7 4 3 Preorce -	FR-408HR Prepred 1 x 2113 RC = 57% 3.63 4 3 Prepred 0 0.6 0.5 8 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 4 0 0.6 0.5 9 FR-408HR Prepred 1 x 3313 RC = 53.8% 3.7 4 4 0 0.6 0.5 10 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 3 Prepred 1 0.6 0.5 1 11 FR-408HR Core 1 x 313 RC = 53.8% 3.7 4 3 Prepred 1 0.6 0.5 1 12 FR-408HR Core 1 x 313 RC = 53.8% 3.7 4 3 Prepred 1 0.6 0.5 1 1 0.6 0.5 1 1 0.6 0.5 1 1 0.6 0.5 1 1 0.6 0.5 1 1 0.6 0.5 1 1 0.6 0.5 1 1 0.6 0.5 1 1 0.6 0.5 1 <td>FR-408HR Prepreg 1 x 2113 RC = 57% 3.63 4 3 Prepreg 0.05 0.05 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 0.66 0.5 4 9 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 0.66 0.5 4 10 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 1 0.6 0.5 4 11 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 1 0.6 0.5 4 12 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 1 0.6 0.5 4 13 R.408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 1 0.6 0.5 4 14 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 1 0.6 0.5 4</td>	FR-408HR Prepreg 1 x 2113 RC = 57% 3.63 4 3 Prepreg 0.05 0.05 FR-408HR Core 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 0.66 0.5 4 9 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 0.66 0.5 4 10 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 1 0.6 0.5 4 11 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 1 0.6 0.5 4 12 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 1 0.6 0.5 4 13 R.408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 1 0.6 0.5 4 14 FR-408HR Prepreg 1 x 3313 RC = 53.8% 3.7 4 3.4 Prepreg 1 0.6 0.5 4

Figure 11: A complete stackup drawing for a 22-layer PCB.

Accounting for Resin in Pre-Preg That Flows Into Adjacent Signal and Plane Layers

In Figure 11, two columns labeled "Material Unpressed Thickness" and "Material Pressed Thickness" list thicknesses for the pre-preg layers. The reason for these two columns is that the resin in the pre-preg layers flows into the voids in the adjacent signal and power layers during lamination.

Estimating how much the thickness of each pre-preg layer will diminish during lamination is a necessary part of getting the impedance right as well as getting the overall thickness right. In Figure 11, the internal layers are all 0.5 ounce copper which averages 0.6 mils (15.2 microns) thick when they have been through the cleaning and etching steps involved in creating them. If a conductor layer were etched until it had very little copper left on it (a signal layer), the final pre-preg thickness would be reduced by 0.6 mils. Since there are usually moderate numbers of signals on signal layers, most of us reduce the final pre-preg thickness by this amount.

Plane layers typically have most of the copper in place after etching, so very little resin from the pre-preg flows into the voids in the plane layers. As a result we usually estimate that the pre-preg thickness is diminished by about

	GEN	ERIC 22 I	AYER S	WITCH FABRIC PCB STACKUP	09/03/09	1	-							
	Layer #	Material Name	Material Type	Material Construction	Material Unpressed Er (at ~2 GHz)	Material Pressed Er (at ~2 GHz)	Material Unpressed Thickness (mils)	Material Pressed Thickness (mils)	Picture	Copper Thickness (mils)	Copper Thickness (oz)		Single Ended Trace Width (mils)	Single Ended Imped. (ohms)
	-							0.7				-		
Ton	1	-						0.7	Solder Mask	2.2	15	_		
төр		ED-408	Prenner	1 × 3313 PC = 53.8%	37			3.4		2.2	1.5	-	_	
S1	2	111-400	riepieg	1x351510 = 55.6%	5.1			5.4	Prebred 2	0.6	0.5	-	4.5	50.0
-	-	FR-408	Core	1 x 2113 RC = 44%	4.2			3	Com	0.0	0.0		4.0	00.0
Ground	3								3	0.6	0.5			-
		FR-408	Prepreg	1 x 2113 RC = 57%	4		4	3	Prepreg					
V1	4				1010				4	0.6	0.5			
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core			U,		
S2	5	-				1			5	0.6	0.5		4	51.0
		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	6	Prepreg	8			1	-
Ground	6	FD 100							6	0.6	0.5	-		
00	7	FR-408	Core	1 x 3313 RC = 53.8%	3.1		-	4	Core	0.0	0.5	_	-	54.0
33	1	ED 409	Deserse	1 X 2242 DC + 1 X 408 - 56%	27		0.5	6	1	0.0	0.5	_	4	51.0
Ground	8	FR-400	Piepieg	1 × 33 13 RC + 1 × 100 = 50%	3.1		0.0	0	Prepreg	0.6	0.5	-		
Ground	0	FR-408	Core	1 x 3313 RC = 53.8%	37			4	0	0.0	0.0			
S4	9	111 100	0010		0.1	-			Core g	0.6	0.5		4	510
	-	FR-408	Prepred	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	6	Prepred			-	_	
Ground	10								10	0.6	0.5	-	_	
1		FR-408	Core	1 x 2113 RC = 44%	4.2	1		3	Core			-	2	
V2	11								11	0.6	0.5		1	
		FR-408	Prepreg	2 x 106 RC = 63.3%	3.7		4	3.4	Prepreg	J	-			1 2
Ground	12		(0		12	0.6	0.5			
	-	FR-408	Core	1 x 2113 RC = 44%	4.2			3	Core					
V3	13					-			13	0.6	0.5	_		
07		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	6	Prepred	0.0	0.5	-		51.0
5/	14	ED 409	Core	1 × 2242 DC - 52 9%	27			4	14	U.6	0.5	8	4	51.0
Cround	45	FR-400	Core	1 X 3313 RC = 53.6%	3.1	-		4	Core	0.6	0.5			
Ground	15	FR-408	Prenred	1 X 3313 PC + 1 X 106 = 56%	37		6.5	6	Deserve	0.0	0.5	-		
S8	16	110-100	riopiog	17,001010 - 17,100 - 0010	0.1	-	0.0		Prepred	0.6	0.5	-	4	510
1		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core			-		
Ground	17								17	0.6	0.5		}	
	-	FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7	2	6.5	6	Prepreg	4				
S9	18	-							18	0.6	0.5		4	51.0
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core					-
V6	19		-		-				19	0.6	0.5	_		
		FR-408	Prepreg	2 x 106 RC = 63.3%	4	-	4	3	Prepreg					-
Ground	20	ED 409	Care	1 - 2112 DC - 11%	4.0			0	20	0.6	0,5		1	
C10	01	FR-408	Core	1 X 2113 RC = 44%	4.2			3	Core	0.6	0.5		15	50.0
510	21	ER-408	Prenred	1 x 3313 PC = 53.8%	37		A	3.4	21	0.0	0.5	-	4.5	50.0
Bottom	22	11-400	peneg	1 X 00 10 RG = 00.070	3.1		.+	3.4	Prepred 22	22	15	-	-	
- strong		-	1					0.7	Solder Maria	4.4	1.0		-	
			1						Solder Wask			-	-	-
							-	89.6	106.0	16.4				-
								Material		Copper				
								Thickness	Total Thickness	Thickness				

Note: Place only information to left of dark line on fabrication drawing. Do not place impedance information on fabrication drawing.

Prepared by Speeding Edge, 09/03/09 Layers 1 and 22 are to be used for component mounting and traces that are not controlled impedance.

Figure 12: A stackup drawing for a 22-layer switch fabric.

half of the plane layer copper thickness.

The best way to get this right is to provide the proposed stackup to the fabricator's engineering department for review.

A Full Stackup Drawing

Figure 11 is a complete stackup drawing containing all of the information needed to ensure a PCB is constructed to meet all of the signal integrity, power delivery and manufacturing goals. There is far more information on this stackup drawing than is usually found on such a drawing, for reasons that have been explained previously. This stackup is for a generic design that has as much routing in the horizontal direction as the vertical direction. Some designs, such as backplanes, may have substantially more wiring in one direction than the other. If this is the case, the dual stripline layers will not be well utilized due to the need to avoid routing traces one over the other in adjacent signal layers. In such cases, the stackup will require single stripline layers. Figure 12 is one such example.

Tools For Creating PCB Stackups

There are a number of commercially available tools based on field solvers that permit the design of a complete stackup. Among these are:

- Hyperlynx Linesim from Mentor Graphics
- Allegro PCB Si from Cadence Design Systems

• Si9000 and Speedstack 2008 from Polar Instruments

The problem with all of these tools is the lack of a place to record the laminate type and weave for each opening in the stackup. To solve this problem, some colleagues of mine developed the Excel spreadsheet shown in Figures 11 and 12 for this purpose. The reader is encouraged to use this form if it makes recording stackup information convenient.

What About Four-Layer PCBs?

All of the discussion above has involved designing PCB stackups that have sufficient numbers of layers to meet all of the signal integrity requirements of high-speed designs. Many cost-driven designs require the use of four-layer PCBs. These PCBs usually contain two planes and two signal layers and are stacked signal, plane, plane, signal. The three main signal integrity considerations when designing a PCB stackup are impedance control, crosstalk control and creation of interplane capacitance for the PDS. In order to minimize crosstalk, the signal layers must be close to the planes. In order to create interplane capacitance the planes must be close to each other. These two considerations are in direct conflict with each other.

Figure 13 illustrates a stackup that has been designed to meet the crosstalk and impedance goals. Notice that the two signal layers are on

	GENERI	C 4 LAYE	R PCB 0	90909).		l l					
	Layer #	Material Name	Material Type	Material Constructi on	Material Unpresse d Er (at ~2 GHz)	Material Pressed Er (at ~2 GHz)	Material Unpresse d Thickness (mils)	Material Pressed Thickness (mils)	Picture	Copper Thickness (mils)	Copper Thickness (oz)	Single Ended Trace Width (mils)	Single Ended Imped. (ohms)
						1							
								0.7	Solder				
Тор	1									2.2	1.5	4.5	50.0
		FR-408	Prepreg	1 X 3313 R	3.7		4	3.4	Prepreg				
Ground	2								2	0.6	0.5		
		FR-408	Core	6 x 7628 R	4.06	1		42	Core				
V1	3	1							3	0.6	0.5		
		FR-408	Prepreg	1 X 3313 R	3.7		4	3.4	Prepreg				
Bottom	4								8	2.2	1.5	4.5	50.0
								0.7	Solder				
									55.8	5.6			
								50.2	Total Thickness	Copper Thickness			

Figure 13: A stackup drawing for a generic four-layer PC motherboard.

video interview

Fab and Design Speaking the Same Language

by Real Time with... IPC APEX EXPO



Colonial Circuits Engineering Manager Michael Tucker talks about working with designers to give them an understanding of how boards are manufactured. He also discusses buying American whenever possible.



the outside of the stackup and the two planes are on the inside. Further, the two signal layers are very close to the plane layers. This results in excellent crosstalk and impedance control. In order to meet the overall thickness goal, something close to 60 mils (1.52 mm), the plane layers are very far apart. As a result, there is no useful plane capacitance for use by the PDS.

It has been demonstrated many times that high-speed single-ended buses require plane capacitance in order to function correctly. How is it possible to make a high-speed design such as a PC with wide single-ended PCI and memory buses function properly with such a stackup? The answer is that the necessary high-quality capacitance is built into the ICs themselves. As a result, there is no need for plane capacitance on the PCB. When a four-layer PCB is used with ICs that don't have built-in capacitance, signal integrity problem nearly always are part of such a design. **PCBDESIGN**

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Sexy Software Sells: User Interface Ranks Higher than Functionality

by Abby Monaco, CID INTERCEPT TECHNOLOGY

SUMMARY: How times have changed. Years ago, PCB designers actually bragged about being able to use awkward EDA tools. But now, consumer applications such as Apple's iPhone and iPad are influencing our software expectations in the workplace. For today's PCB designers, software functionality must be presented to users in an easy-touse fashion, or that functionality might as well not exist at all.

We all know the car salesman's trick of draping a busty girl in high heels and skimpy shorts over a fancy sports car. But after you get to work in your new car, does this approach work for the next generation of EDA software? Put a slick, easy-to-install, easy-on-the-eyes application in front of a potential new user, and time to close the sale may be less than five minutes. If a user can't jump right into the driver's seat and hit the accelerator, the sale is lost, regardless of the years. Supporting a new operating system was a resource burden.

While EDA companies struggled to upgrade to support Windows, Microsoft was taking the world by storm. I spent my sophomore year of college learning how to hand-draft drawings, but by my senior year, we were all fluent in AutoCAD. When I was recruited by Intercept, you can imagine my dismay and confusion at the clunky and nearly impossible-to-use schematic application that I tested for quality assurance. What a buzzkill. I couldn't understand how anyone could get anything done with this software.

So I embarked on a crusade to bring the "pretty" to the "functional." Remember that 10 years ago, this was a fairly new concept for EDA, and my pleas were not accepted with the unanimous agreement that they are now. The EDA world had its own historic (and archaic!) stan-

software's horsepower. Forgive the mixed metaphors.

This isn't news to most of us, but it is worthy of examination in the EDA world. The concept of a user interface was really only introduced with the success of Windows 95, less than 20 years ago. There had been earlier attempts, but none were as widely adopted. However, in the EDA world, the new operating system proved to be a headache for the existing vendors, because CAD software had been supported on HP-UX or Sun-Solaris for nearly 20



Figure 1: Pantheon version 6.

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SEXY SOFTWARE SELLS continues



Figure 2: Pantheon version 7, after a complete user interface upgrade.

dards, which were light years away from what was becoming standard among other industries. Most EDA vendors thought, why should our new EDA software need to change at all?

The answer lies right in front of you. Which software application would you rather use?

If you chose version 6, please contact me for a therapy session or just retire already! If untrained users tried to get in the driver's seat with version 6, most wouldn't know where to begin. The newer version 7 has the same functionality of version 6. But with version 7, users intuitively know to start with the upper left menu and move to the right to complete your design. Why? Because this is the standard software interface today. The user interface is combined with a whole new psychology that lures the user in and keeps him there.

This new psychology decrees that software functionality must be presented to users in an easy-to-use fashion, or that functionality might as well not exist at all. Over the years, as this has become mainstream in the consumer software world, users have come to expect certain behaviors to be inherent in their software. When those behaviors are not executed as expected, frustration and distaste for the software ensue. It makes no difference if a sought-after function can actually found elsewhere in the application; when it can't be found easily, the damage is done.

When applied to EDA software, designing the perfect GUI can be tough. Some of the functionality required specifically for PCB design can be very difficult to display in an accessible manner. Let's use via fencing around an area fill as an example. With the old Pantheon 6 dialog in Figure 3, I doubt you could determine how to fence the fill on your first try. Disregarding the ancient

display, the dialog appears simple enough, but it leaves out a lot of what it's actually doing.

Using the Pantheon 7 dialog, however, you are presented with easy-to-understand terms, expanded options, and a preview showing exactly what you're getting. The guesswork is taken out of the task, and thus the same function becomes something a user can accomplish quickly, in one try. But I won't deny that it's also much more fun! Users can play with a preview rather than hitting OK, undoing what was

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Figure 3: Pantheon version 6 Fence Fill dialog.

SEXY SOFTWARE SELLS continues

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Figure 4: Pantheon version 7 Generate Via Fence dialog.

done, going back to the original hard-to-read dialog, and hitting OK again.

Indeed, the fun aspect of using software, even PCB design software, is something that cannot be ignored. Consider the Apple iPhone and iPad, or Google's Droid operating system. They're so fun to use that people are hooked on them like dogs on leashes. Their ease of use is influencing our expectations in the workplace as well; software is expected to do more of the job, namely, automating difficult or complex tasks so that they are simpler for us to accomplish. If EDA software doesn't keep up with expectations, it won't succeed in the long run.

In conclusion, I challenge you to be more vocal with your software vendor about what you expect, what you wish the software would do for you, or any areas that seem counterintuitive. The EDA industry has a longer history than Microsoft and Apple, so it sometimes struggles with the best way to present the old functionality with a new interface. A lot of the applications out there are doing a great job of catching up, but there are also plenty of snags. If we all put our analytical minds together, we can come up with some great solutions. **PCBDESIGN**



Abby Monaco, CID, is a product manager for Intercept Technology Inc. With more than 13 years of experience in EDA, Abby is actively involved in technical product planning and direction, and marketing.





Orange County Designers Council Meeting Draws a Crowd

By Andy Shaughnessy

The Orange County chapter of the IPC Designers Council held a "lunch and learn" meeting October 23 in Irvine, California.

Guest speaker Charles Pfeil, engineering director of advanced products for Mentor Graphics, discussed current and future technology BGA design issues. Pfeil is the author of the book "BGA Breakouts And Routing: Effective Design Methods For Very Large BGAs."





"We had 66 people in attendance at our recent IPC Designers Council meeting," said Scott McCurdy, president of the Orange County chapter. "Charles Pfeil did a great job talking about breakout and routing of difficult BGAs."

During the two-hour meeting, Pfeil conducted an open Q&A session addressing the benefits of using BGA packages and methods for dealing with the challenges brought on by increasing BGA density and pin count. He also focused on differential pair issues and a variety of emerging packaging styles.

The Orange County chapter is one of the largest and most active Designers Council chapters. **PCBDESIGN**

Most-Read Mil/Aero007 News Highlights



Ventec Recommended for AS9100C Accreditation

Ventec Europe announced that its parent company, Ventec Electronics Suzhou Co. Ltd., has been audited against the requirements of AS9100C and recommended for accreditation. Ventec Europe Managing Director Mark Goodwin commented, "Ventec has made great progress as a supplier to the high-reliability military and commercial aerospace sector and this accreditation underscores our commitment to be a key player in this business."

FTG Aerospace - Tianjin Earns AS9100 Certification

"FTG is committed to operational excellence across the corporation and the continuous improvement of our process controls and quality systems are an important part of these efforts," said Brad Bourne, president and CEO.

Invotec Wins BAE Systems Supplier Award

Terry Dowling, Invotec Group Ltd.'s business development director commented, "We are delighted to receive this award for the third time. There is a close working partnership with BAE based on performance and trust. Our commitment to continuous improvement and lean manufacturing principles is fundamental to our ongoing journey of providing total customer satisfaction."

Electrotek Achieves AS9100C Certification

In a continuing commitment to supplying highest quality printed circuit boards, Electrotek recently received its AS9100C certification. This adds to Electrotek's ongoing accreditations in support of its customers' needs in supplying high-reliability hardware.

NASA Identifies Counterfeiting as One of Greatest Challenges

NASA has always confronted big challenges in outer space, from putting men on the moon, to landing an SUV-sized rover on Mars, to sending a probe 5.7 billion kilometers to explore Pluto. However, back here on Earth, the storied agency now is facing what may be an even bigger challenge: the scourge of counterfeit parts, a phenomenon that threatens the success of its missions, the safety of its personnel and the security of the country.

Mentor Graphics Posts Record Q3 Revenues

Mentor Graphics Corporation reported revenue of \$268.8 million for the fiscal third quarter ended October 31, 2012.

"Revenue and earnings were records for a Q3. Mentor and the electronic design automation industry continue to benefit from the semiconductor industry's transition to the next generations of technology," said Walden C. Rhines, chairman and CEO of Mentor Graphics. "For Mentor, exceptional strength in bookings for system design, including mechanical analysis, and new applications of EDA to automotive design and embedded software development provided unique growth opportunities."

During the quarter, the company announced a major new design rule checking product in the HyperLynx high-speed analysis product line.



DESIGN FOR MANUFACTURING

How Often Do You Visit Your Fabricator?

by Amit Bahl

SIERRA CIRCUITS

SUMMARY: If you anticipate that you'll never layout boards with more than two layers, or holes, traces and spaces smaller than 10 mils, and you're sure you'll never have to deal with impedance control, you have no reason other than curiosity to investigate how your boards are constructed. But if you design complex, high-speed boards, Amit Bahl's new column is just for you.

Few designers ever venture to the shops that will or might build their boards, even when those manupractically facturers are next door. Even one hour spent watching fabrication processes firsthand could avoid stalling some future project for weeks while the design is re-spun to account for actual manufacturing tolerances.

In this inaugural column, I'll dwell on the mismatch between design rules and process limits, because the shops that specialize in building complex prototypes encounter these issues day in and day out.

If you anticipate that you'll never layout boards with more than two layers, or holes, traces and spaces smaller than 10 mils, and you're sure you'll never have to deal with impedance control, you have no reason other than curiosity to investigate how your boards are constructed. But if you take your job seriously, especially if you may one day route a circuit involving a BGA with a pin pitch tighter than 0.5 mm or one with 1,000 pins, and certainly if you must control impedance, it is imperative that you grasp the accuracy of the electrochemical, thermal, and mechanical operations at your current or prospective manufacturer, as well as the true

stability of materials, to understand how excursions from nominal values within tolerance can accumulate and kill a design. I'm tempted to mention ivory towers, but you get the picture.

> Inexperienced designers often misconstrue as ironclad the dimensions manufacturers list on their websites. For example, manufacturers - including my facility - may state that they're capable of producing traces as fine as 2 mils wide on 2-mil spacing. I don't doubt most of them can, but only under very limited circumstances, namely, only on an inner layer when plating isn't involved (and absolutely not in buildup layers with buried vias). The problem isn't the 2-mil traces: It's the spacing.

> You want 2-mil traces on 10-mil or 3-mil spacing? OK. But don't

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HOW OFTEN DO YOU VISIT YOUR FABRICATOR? continues

expect less than plus or minus 25% variation along a 2-mil space no matter the distance. This obviously rules out controlling the impedance of a differential pair of those dimensions.

You might not lose sleep over tolerances for dielectric thickness, but Z-axis variation within the boundaries of a material spec compounds the challenge manufacturers face to meet impedance requirements in HDI projects, when the dielectric height driving a customer's architecture doesn't jibe with the blind-hole size in the design to permit a 1:1 or .75:1 via aspect ratio.

There's no way to fudge the microvia aspect

ratio. So, if a design is based on a 6-mil dielectric, but uses 4-mil vias with 8-mil pads, and the via locations and trace spacing are too tight to enlarge the pads and therefore the vias, the only way the board can be built is by decreasing the dielectric height. However, if impedance must be held to 50 ohms for traces on the top or 100 ohms for differential traces, and the dielectric height needs to be decreased by half to salvage the layout, then the trace widths and spacing must be reduced by half.

Ten percent above or below nominal thickness holds true for dielectrics down to .031" cores, but with a 6-mil core, for example, the tolerance is plus or minus 1 mil. Decreasing the di-

electric thickness by half would consequently throw impedance control out the window, and narrowing the trace width and spacing by half most likely would as well. Manufacturers can adjust processes only so far to compensate for imbalanced designs. When you consider transmission line effects, there's an optimum combination of rules that must be in place to guide the layout. A certain dielectric drives a certain minimum via size, which dictates a certain pad size, which determines trace width and therefore spacing.

Finished trace thickness has a negligible bearing on impedance, but you should know

Manufacturers can adjust processes only so far to compensate for imbalanced designs. When you consider transmission line effects, there's an optimum combination of rules that must be in place to quide the layout.

how your choice of copper weight influences manufacturing, which a plant tour can clarify. The copper weight you choose governs how readily fine lines can be etched within tolerance, but there are other implications. The general but not absolute rule to follow on inner layers, except HDI layers, is to use half-ounce copper.

But if you have an inner layer with vias that will be stacked, for example, after the vias are plated they will have to be filled, planarized, and then wrap plated. Any via that must be filled must be wrap plated. If you start with halfounce copper, the trace thickness will exceed

1 mil after those operations, which may be too tall for a single thickness of dielectric in prepreg to conform and fill around features. To avoid that manufacturing issue, you should specify quarter-ounce copper weight as the starting point for such a layer. You would learn during a plant tour that finished thickness after plating is what counts the most, and that is what should limit copper weight, preprocessing.

Have I convinced you to take a field trip yet? Your prototype builder or prospective builder should be happy to arrange a tour, but what questions should you ask? If you have a design in progress, preview it so hole sizes, pad sizes, di-

electrics and the like can be discussed up front, especially if it's a controlled-impedance design or you're planning to use microvias or sequential laminations.

The processes you'll see in person will undoubtedly look different than what you had imagined and will drive home just how abstract are the images on your EDA display. When you're working with representations 500x the scale of the real thing, you can become cavalier about 1 mil.

While you're walking, ask your guide to show you jobs in progress based on technology you'll need. For example, if you have a design

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HOW OFTEN DO YOU VISIT YOUR FABRICATOR? continues

in the works (or plan to) with 5-mil traces and spaces, sequential laminations, and laser vias, ask to see something of that sort being built. If your host has to duck into the sales manager's office to find a sample, chances are the technology is not routine for the shop. There should be plenty of examples along the route.

If you don't contemplate turning to an HDI architecture, why bother looking for laser drills and laser direct imagers at the shop? But if you do, those machines should be in place and busy on site, if the company does many such jobs.

Look for processes that are self-auditing; in other words, they are not dependent upon a person flagging an out-of-range condition. There is no substitute for experience, but no operator is 100% vigilant. If you see 30 or 40 processes being automatically monitored in real time with the status displayed on screens, chances are you've found a dependable shop. If instead you see paper check sheets on clipboards, you might have second thoughts.

Perhaps you had quality issues from another supplier but know the root cause of the problem. Naturally you'd enquire about measures the prospective shop takes to prevent this. For example, if your boards had small holes with a high aspect ratio and there were plating issues, you'd be interested to know whether the electroless copper line has vibration to work loose bubbles trapped in small holes, and whether boards similar to yours make two passes for security. And you would check to make sure the plating line has pulse plating to ensure plating extends the length of the holes.

I'm not talking about the kind of detailed investigation that takes place over several days during a customer audit to validate a supplier for production runs after successful prototypes. I'm talking about getting educated about what really happens after your design files reach a fabricator, about understanding the important variables in manufacturing and the limits of processes.

You'll learn about the interdependencies among processes, how everything works together, how excursions within tolerance from process to process can stack up and defeat your design, and how to tailor design rules to avoid manufacturing issues. You'll be a better designer for it and a more valuable asset to your company. **PCBDESIGN**



Amit Bahl directs sales and marketing at Sierra Circuits, a PCB manufacturer in Sunnyvale, CA. He can be reached via <u>amit@protoexpress.com</u>.

IPC: N.A. PCB Shipments, Bookings Down in October

Rigid PCB shipments were down 1.1% in October 2012 from October 2011, and bookings de-

creased 9.2% year over year. Year to date, rigid PCB shipments grew 4.4% and bookings decreased 0.2%. Compared to the previous month, rigid PCB shipments were down 12.4% and rigid bookings fell 14.3%. The book-to-bill ratio for the North American rigid PCB industry in October 2012 slipped below parity to 0.98.

Flexible circuit shipments in October 2012 were up 15.6%, and bookings were

down 18.9% compared to October 2011. Year to date, flexible circuit shipments decreased 4.0% and bookings decreased 10.5%. Compared to the previous month, flexible circuit shipments decreased 10.3% and flex bookings were down 0.5%. The North American flexible circuit book-to-bill ratio remained low at 0.74.



FROM THE PCB LIBRARY

The Elements of PCB Library Construction, Part 2

by Tom Hausherr PCB LIBRARIES INC.

SUMMARY: The survey says? Last month, Tom Hausherr discussed many of the fundamental principles of PCB library development and asked designers to take a survey that focuses on their library component practices. This month, Tom breaks down some of the survey results. One thing is certain: American designers aren't likely to switch to the metric system anytime soon.

Part 1 of this series, in the November issue of <u>The PCB Design Magazine</u>, asked readers to take a short survey of their PCB library practices. This month, we'll take a look at some of the preliminary results. The respondents to this international survey constitute a solid crosssample of the global electronics market. Let's get started.

Measurement Units

Question 1: What footprint (land pattern) name do you use for your chip component library parts?

LIDEM	ARY

50% - Imperial (1206, 0805, 0603 & 0402) 25% - Metric (3216, 2012, 1608 & 1005) 25% - Both

The poll shows that 50% of PCB designers and their companies use the imperial unit chip component names. I believe imperial units will be around for a long time. And with 25% of respondents using metric names and 25% using both metric and imperial chip component names, I believe the electronics industry is in chaos. We will never reach the pinnacle of electronic product development automation until we adopt a single measurement system.

Look at the confusion that this dissent creates with component manufacturers, component resellers, purchasing agents, electrical engineers, PCB designers and assembly shops. Table 1 compares metric and imperial chip resistor component names. The metric names and component package body sizes match 100%, while the imperial names sometimes use rounding factors and sometimes just drop the third character.

Who controls the imperial naming convention? When do we round or drop values?

The imperial naming convention is haphazard. I am convinced that the metric system is vastly superior and simplistic compared to the imperial system. To better understand the origin of the imperial chip component names, you should read Part 1 of this series.

Question 2: What units do you use for PCB library construction?

12% - Imperial 62% - Metric 26% - Both

Metric Name	Body Size Length x Width	Imperial Name	Body Size Length x Width
0402	0.4 mm x 0.2 mm	01005	0.015" x 0.007"
0603	0.6 mm x 0.3 mm	0201	0.023" x 0.012"
1005	1.0 mm x 0.5 mm	0402	0.039" x 0.019"
1310	1.3 mm x 1.0 mm	0504	0.051" X 0.039"
1608	1.6 mm x 0.8 mm	0603	0.062" x 0.031"
2012	2.0 mm x 1.2 mm	0805	0.078" x 0.047"
3216	3.2 mm x 1.6 mm	1206	0.125" x 0.062"
3225	3.2 mm x 2.5 mm	1210	0.125" x 0.098"
4532	4.5 mm x 3.2 mm	1812	0.177" x 0.125"
5025	5.0 mm x 2.5 mm	2010	0.196" x 0.098"
6432	6.4 mm x 3.2 mm	2512	0.251" x 0.125"

Table 1: Metric and imperial chip resistor component names.

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THE ELEMENTS OF PCB LIBRARY CONSTRUCTION, PART 2 continues

A solid majority (62%) of PCB designers polled say they build their library parts in metric units. Is that because most component manufacturers only provide metric component package and recommended pattern dimensions? I've seen component manufacturers dimension the package in millimeters and the recommended pattern in inches. This seems really bizarre to me. Only 12% are using imperial units to create their library parts. Is this a sign of the future? Are PCB designers preparing to transition? The answers to Question 3 may help shed some light on the answer.

Question 3: What units do you use for PCB layout worldwide?

25% - Imperial 56% - Metric 19% - Both

So, 25% of all PCB layout is still done entirely in imperial units, while 19% toggle between measurement systems. I'm glad to see a majority, 56% of all PCB designers worldwide, using the metric unit system. Metric PCB design increases productivity and layout aesthetics. However, the numbers in America are very different than the rest of the world.

What units do American PCB designers use for layout?

72% - Imperial units 9% - Metric 19% - Both

The American electronics community is waiting for PCB fabrication shops to fully transition to the metric unit system. Assembly shops can go either way, because most of the assembly machinery is manufactured in Germany or Japan. I strongly believe that once the American fabricators go metric, the entire American design sector will follow. At that point, electronic product development automation will shift into high gear.

I believe America is the last country that has not fully transitioned to metric units yet. Yes, it's tough getting the entire team on board with transitioning to a new system. The mechanical engineers, design engineers, PCB designers, purchasing agents, and all of their manufacturers must all transition together. American fabricators will face a difficult challenge in switching to metric units, because it will require purchasing new equipment and training employees. But it will be a sweet sound to hear an American board shop require its customers to provide metric fabrication data. Right now, I do not know of a single American fabrication shop that is metric only, and American PCB designers may have to wait a long time for all of them to fully transition.

The perfect scenario: All electrical engineering, mechanical packaging, PCB design, fabrication and assembly are done in metric units. Everyone follows a standard schematic symbol, PCB solder pattern, and 3D model system, and a standard communication format between design and manufacturing—such as IPC-2581—is fully developed. No one will ever need to create another symbol/solder pattern/3D model library part; CAE, CAM, and CAD are fully integrated, while post-processing manufacturing data are automated. The U.S. electronics industry would light up with innovation, increased productivity and quality, along with reduced errors and cost. The generation of self-guided cars, robotic technology and an unimaginable standard of living would become a reality. Humans need only to create and maintain robots and robots will eventually produce most electronic products.

America's reluctance to standardize on metric units will continue to handicap its future and postpone automation.

Terms And Definitions

Question 4: What term do you use to describe a PCB library part?

7% - Land pattern 76% - Footprint 17% - CAD vendor name (decal, cell, model, etc.)

This is very confusing to me. IPC introduced the term "land pattern" in the 1987 release of the IPC-SM-782, but most PCB designers still do not use it in their everyday reference to PCB library parts. For just as many years, IPC-T-50 Terms and Definitions did not clearly define the term "footprint." Footprint is defined as "See Land Pattern." The latest version of IPC-T-50 now clarifies that a footprint is the area where the physical component leads and component body touch the PCB. Therefore, a footprint solders to a land pattern. Since the term land pattern has not taken hold in the past 25 years, I'm not sure that it will ever be adopted by PCB designers. Who invented the term footprint, the CAD vendors or the component manufacturers? If a library part is a land pattern, then the component lead solder area on the PCB must be called a "land" right? Wrong...see Question 5.

Question 5: What term do you primarily use when referring to a library part solder area?

3% - Land 94% - Pad 3% - Pin

I think it's obvious that the term "pad" is here to stay. But what does this mean to the IPC-7351C standard? Pad is never used in any IPC standard publication, but land is prevalent. Pad comes from the CAD vendors, and it has become the default standard. So the big question is, "Should IPC change the IPC-7351 Land Pattern Standard" to IPC-7351 Footprint Standard"? And should IPC change every reference of the term "land" to "pad" so that PCB designers worldwide use common terminology?

Pad Shape

Question 6: What pad (land) shape do you use most of the time for PCB library parts?

5% - Oblong 67% - Rectangular 1% - D-shape 27% - Rounded rectangular

These results are surprising to me, because every IPC standard regarding pad shapes recommends oblong. After building thousands of PCB library parts, I have noticed that each com-





ponent manufacturer's recommended solder pattern is the rectangle. But IPC has long stated that the oblong shape is easier to manufacture and it helps improve assembly. And that leads us to a new upcoming pad shape, the rounded rectangle, which I believe will eventually become the new standard as it is a compromise between oblong and rectangle. The primary reason for the slow adoption of the rounded rectangle is that many CAD vendor tools have not supported it. Actually, some still don't. Based on trends I've seen in the past decade, I believe it's safe to say that the rounded rectangle will be adopted by the design industry and may find its way into every surface mount footprint except grid array packages such as BGA, LGA and CGA, all of which have rounded or square leads and use a periphery solder pattern (no toe, heel or side solder fillet). Your responses to Question 7 provide evidence.

Question 7: Will you ever consider using a rounded rectangle pad (land) shape in the future?

48% - Yes 9% - No 43% - Already use rounded rectangle pad





THE ELEMENTS OF PCB LIBRARY CONSTRUCTION, PART 2 continues

Zero Component Orientation

Question 8: Which zero component orientation do you use to create PCB libraries?

52% - Pin 1 upper left (IPC-7351B)
29% - Pin 1 lower left (IEC 61188-7)
19% - Either, orientation is not important to me

Zero component orientation refers to the location of Pin 1 in the PCB library. With the upcoming IPC-2581 which will automate the way PCB designers communicate with fabrication and assembly, a single component orientation is preferable for optimized productivity. However, the industry is split between two standards and IPC has agreed to include both rotations in the upcoming IPC-7351C.

The original IPC rotation with Pin 1 in the upper left will be referred to as "Level A," because IPC was the first world standards organization to publish a zero component orientation standard. The IEC rotation with Pin 1 in the lower left will be referred to as "Level B." So when the PCB designer produces an assem-



Figure 3: IPC-7351 rotation.

bly drawing, they will indicate in the assembly notes which level their PCB library is based on.

I believe the IEC rotation (IPC Level B) is better because it generally creates library parts with the length in the horizontal direction. Since the standard ISO and ANSI paper sizes are long in the horizontal direction, the PCB layout board outline is typically long in the horizontal direction. When parts are placed on a PCB layout, the length of the component normally conforms to the length of the board outline and thus produces a zero orientation of "0" (no rotation). So the paper length, board outline length and component placement length are synchronized.

Silkscreen Outlines

Question 9: Do you use silkscreen outlines in your PCB library parts?

76% - Yes 9% - No 15% - Sometimes

The answers to this question indicate the importance of the silkscreen outline in the PCB library. I would imagine that the 9% who do not use silkscreen have a great communication system between engineering, design and manufacturing.



Figure 4: IEC 61188-7 rotation.

THE ELEMENTS OF PCB LIBRARY CONSTRUCTION, PART 2 continues





Figure 5: Silkscreen outside component body.

Question 10: Which outline option do you use when creating PCB library part silkscreen outlines?

36% - Outline under the component body64% - Outline outside the component body

Silkscreen outlines under components are covered up during assembly. So, the question is often asked, "What good does that do if no one can see the silkscreen after assembly? What benefit offsets the risk of possible solder problems on low-profile or miniature components when placing the silkscreen under the component body?" If the silkscreen is outside the component and visible after assembly, you can use it as alignment markings to QC the reflow process for component skew.

Question 11: Do you use silkscreen outlines on your boards?

27% - No
63% - Yes, on both prototypes and production
10% - Yes, but only for prototypes

Figure 6: Silkscreen under component body.

Here are the new silkscreen rules, coming with the new IPC-7351C in 2013:

1. No silkscreen outline under the component; these get covered up during assembly and don't provide any useful purpose; instead, it is a waste of expensive inkjet cartridges.

2. All silkscreen outlines visible after assembly process and provide a functional use as alignment marking for assembly registration accuracy.

3. All silkscreen outlines must be inside placement courtyard.

4. All silkscreen outlines are mapped to the Maximum Component Body with one exception, the silkscreen-to-pad spacing rule "overrides" the Component Body Mapping.

5. Silkscreen outlines should map the component body and not go around pads. Excess silkscreen outlines should be avoided to make room for ref des locations. Silkscreen outlines should perform a "hatch" outline along the component package body.

6. Pin 1 is identified by extending the silkscreen along Pin 1 length to indicate polarity when the package cannot be placed inverted (the only components that can be inverted are non-polarized 2-pin parts).

rom the pcb library

THE ELEMENTS OF PCB LIBRARY CONSTRUCTION, PART 2 continues

7. No silkscreen on any exposed pad. The ideal pad-to-silkscreen gap should be 0.05 mm (2 mils) + solder mask annular ring. So, if your solder mask annular ring is 0.07 mm (3 mils) $+ 0.05 (2 \text{ mils}) = 1.2 \text{ mm} (5 \text{ mils}) \text{ mini$ $mum silkscreen to pad gap.}$

Question 12: What line width do you use for your silkscreen outline?

```
18% - 0.10 mm (4 mils)
13% - 0.12 mm (5 mils)
27% - 0.15 mm (6 mils)
30% - 0.20 mm (8 mils)
9% - 0.25 mm (10 mils)
```

Obviously, it's almost impossible to standardize on a silkscreen line width, so EDA tools must accommodate each individual preference.

Question 13: Where do you get your footprint (land pattern) data for library creation?

34% - IPC-7351 calculators57% - Manufacturer recommended pattern9% - Other (please specify)

Many new component packages are nonstandard and the solder pattern cannot be calculated and therefore the component manufacturer pattern is the safest option. This is true for most connectors and non-standard parts like switches, trim pots, LEDs, transformers, convertors and relays. Any component package not covered by a JEDEC standard requires a manufacturer recommended footprint pattern.

Courtyard

Question 14: Do you use a placement courtyard in your library construction?

61% - Yes 33% - No 6% - Only on standard parts

The usage of placement courtyards has risen over the past 10 years as a part placement aid.



Figure 7: Courtyard boundaries.

The IPC-7351 standard provides the courtyard spacing rules.

5 mils (0.12 mm) - Least environment 10 mils (0.25 mm) - Nominal environment 20 mils (0.5 mm) - Most environment

3D Modeling

Question 15: Do you currently use 3D model technology?

62% - Yes 23% - No 15% - I or my company am considering it for the future

I believe 3D modeling will be even more popular in the future. The technology is advancing and it's becoming more affordable and easier to use.



Figure 8: 3D models.

Local Fiducials

Question 16: Do you uselocal fiducials on fine pitch QFP and BGA parts in your PCB library?

THE ELEMENTS OF PCB LIBRARY CONSTRUCTION, PART 2 continues



Figure 9: Fiducial placement.

41% - Yes 36% - No 23% - Sometimes

Post-Assembly Inspection Marking

Question 17: Do you use post-assembly marking in your library construction to ID Pin 1?

64% - Yes 16% - No 20% - Sometimes

Sometimes you have to remove silkscreen to identify polarity. This is common on components with bottom only terminals and microminiature components. So the absence of silk-



Figure 10: Missing polarity marker.



Figure 11: Post-assembly inspection line (or dot).

screen marking makes the best post-assembly inspection marking.

Question 18: If you use post-assembly markings, which do you prefer?

61% - Dots		
24% - Lines		
15% - Do not use j	post-assembly	markings

PCB Libraries tried dots in the past, but we found that using dots often violates the silk-screen inside courtyard rule – the upcoming IPC-7351 standard (Revision C) specifies that silkscreen should not be outside the courtyard.

I hope you found this article useful in identifying various parts of PCB library development. This is the first article of a series that will identify how your requirements in a PCB library compare to what other designers need. If you haven't already done so, I ask that you consider taking this <u>three-minute survey</u> to voice your opinion. We will keep this poll open until the end of 2012. **PCBDESIGN**



Tom Hausherr, CID+, is president of PCB Libraries Inc. He can be reached at <u>Tom.Hausherr@</u> pcblibraries.com.

Software-Defined Radio: The Driver of Universal Connectivity in the Consumer Space?

by Natasha Baker

SNAPEDA

SUMMARY: Largely restricted to the defense and telecom sectors, software defined radios (SDRs) may soon be the driving force in implementing ubiquitous and universal wireless connectivity of your consumer devices. But at typical SDR speeds, PCB designers often face an extra iteration in board protoyping, because there's only so much that can be simulated.

Unlike traditional wireless devices that perform signal modulation in hardware at the circuit level, SDRs perform the equivalent functionality in software. Because of this, the analog frontend can be implemented as a generic hardware platform, agnostic

to a particular wireless format or protocol, and defined by the application running in software (on an FPGA or DSP).

There are two main benefits to providing this added flexibility to a system. First, it provides interoperability between different wireless formats and protocols operating in different frequency bands.

Secondly, it provides flexibility in upgrading the technology since reprogramming and reconfiguring the radio is now a matter of changing the software, rather than the physical hardware or hard silicon.

The technology was originally conceived in the defense sector where it was aimed to replace conventional radio hardware. Most notable is the ongoing Joint Tactical Radio System (JTRS) project, whose goal is to replace all of the military's legacy radios with SDRs for full interoperability and to allow older radios to network with each other.

The \$1B project has now replaced singleprotocol radios with SDR in the 2 MHz to 2 GHz

66 The PCB Design Magazine • December 2012

200

spectrum, allowing aircraft, ocean vessels and ground stations to communicate.

In the telecom sector, the benefits are predominantly on the upgradeability and maintenance side. According to Steve Watts, a managing consultant at PA Consulting, who works closely with cellular network equipment suppliers, SDR has been used for configuring base stations since the late 1990s.

The technology, Watts explained, can allow operators to optimize radio performance or add new functionality over the air as standards evolve—for example, more optimised algorithms can be provided to improve performance or quality of service further away from the base station or indoors where reception might be poor. It also allows bugs to be rectified quickly, with less commercial risk.

Another benefit Watts noted is in prolonging the life of the underlying hardware and getting better economy of scale since multiple-standards can be incorporated into the same radio system. An entire network can be upgraded, for example to accommodate a new feature, without needing to alter the base station's hardware.

Consumer Applications

Now, there's talk of bringing the benefits of SDR to the consumer space, where an increasingly connected lifestyle is becoming the norm.

Wireless devices are increasingly proliferating our daily lives, whether it be garage door openers, WiFi routers, baby monitors, or of course, our mobile phones. However, all of these devices operate on separate frequency bands and support different protocols, and are, therefore, interoperable.

Per Vices, a Toronto-based company, is aiming to solve this problem with its consumer-focused SDR platform. Their first product Phi, can tune any signal from 100kHz to 4GHz allowing it to interface to a wide range of devices, making it what they call the universal wireless device.

"The biggest argument we make is 'forget your ACTV tuner, satellite radio, wireless modem and everything else that is wireless'. We place everything into one device," co-founder Yi Yao said, who has since left the company to pursue a new endeavor.

In addition to this interoperability, upgrad-

ing to a new protocol is as simple as installing a software patch.

"When I got my first laptop computer it came without WiFi, and I got a WiFi card for it—Wifi-B, and then Wifi-G came out, and then Wifi-N came out. If you had our device, it would be one device and all you would have to do was download another software patch that will upgrade it to the next generation," he added.

The company had its start in the defense sector, where they were initially catering to the military's demand for protocol translation. Their first product was an undetectable detection device, a general-purpose high-sensitivity receiver that was receive only, for any signals up to around 3 GHz, which included everything from the WiFi band to the S-band for radar.

The company's aim now is to have developers with a background in DSP building consumer applications on top of their platform, leading to what they hope will be the ultimate solution for long-awaited wireless convergence. And because the network is privately owned, it doesn't need to ping the ISP to run.

"What we're really trying to create is the Internet in the truest sense of the word. One of our grandest visions is to create a mesh network with our wireless devices—one device in each home," Yao explained.

"This will enable a wireless network of different appliances which will make up the internet of things."

Steve Watts envisions that SDR could be of particular value in the automotive industry, enabling car-to-car communication, which allows manufacturers to implement smarter safety systems. The car might use this information to keep a certain distance apart from another car. Or, a car might have increased knowledge of what's ahead based on information received from cars passing from the opposite direction.

SDR could also provide more car telemetry for theft tracking, fleet management, or for insurance companies who might track driving habits to help manage insurance premiums.

In these cases, SDR makes sense, since car manufacturers would only need to provide one piece of hardware across a line of vehicles and then get economy of scale while providing different functionality and frequencies of opera-

SOFTWARE-DEFINED RADIO continues

tion. Cars are also less cost-sensitive than other consumer products, such as mobile devices. And because functionality is implemented in software, they could tailor the functionality depending on the model purchased.

"Ford might have six or seven different cars, but would only need one hardware platform. The low-end car might have nothing beyond a normal car radio, but you go up a level and you might add DAB and real-time navigation to that," Watts said.

"At the top end you could have a completely integrated communication system—Bluetooth, real-time navigation with traffic, car-to-car comms, Internet, Outlook, and all these other things, but they're all on the same hardware platform, all the way down the vehicle family."

Furthermore, since cars have a long lifetime, a soft solution also makes sense since a wireless technology might become obsolete over the ten-year or so lifetime of the car. In this case a software update could upgrade the car to the latest network technology.

"If you had a GSM module and an operator turned off GSM in a region, it could be upgraded to 3G or LTE," he said.

Another interesting area that Watts sees as a potential application for SDR in the consumer space is personal cellular base

stations—a picocell in an office or shop, or a femtocell in a home.

Network operators roll out these base stations to improve coverage and provide enough capacity to give subscribers good data bandwidth. They might give away

small cells for people's homes similar to the way they subsidize handsets to provide better coverage in a home.

Suddenly, base stations shift from being big equipment you see on top of buildings or freeways to becoming small, industrially-designed boxes that sit on your kitchen table at low-cost and low-power.

"You go away from having a few thousand base stations to having hundreds of thousands of base stations. So suddenly, it starts to move to more of a consumer product because of the volumes," Watts explained, adding that companies may initially veer towards a hard solution to get the costs down; however, there would certainly be benefits in adding SDR.

"You could have personalized applications that sit on that base station in the home and could converge some of the various home wireless devices into the home base station," he said. "Or when they login to the base station it gives them additional services that they might not have otherwise on the public infrastructure."

Implementing a soft solution would also allow the base station to switch between 3G or 4G technology, depending on whichever network had better coverage.

Barriers in the Consumer Space

If all of this seems like a fairly trivial extension of SDR as it has been used for over a decade in the defense and telecom sectors, then why hasn't it been done before?

Yao explained that the main driving factor making it feasible in the consumer space is computer power.

"What we're talking about is not something that a desktop computer even five years ago could do comfortably," he explained.

"Take a look at CW streams in Morse Code.

People would write computer programs that would decode that

Morse code into letters. Now

this is a very narrow path signal path—you're talking about something less than 1 kHz," said Yao. "But that was still a challenge for a desktop computer, even a very good one back in the day to do that decoding in real time."

With the decreasing cost of computing power thanks to Moore's law, Yao said that they're able to work with bandwidths in the MHz range—up to 100 MHz and beyond. Their device leverages both GPU and FPGA technologies for both to stream processing, and it's the combination of the two that helps them to do what wasn't feasible for a desktop computer only a few years ago.

Steve Watts said that cost and power have restricted SDR's adoption at the consumer end in the telecom sector.

What we're talking about is not something that a desktop computer even five years ago could do comfortably.



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SOFTWARE-DEFINED RADIO continues

"Generally you add cost if you add flexibility and programmability because you have to have the ability to change it," Watts explained. "The cheapest unit cost will be achieved with a hardware solution ultimately. But the non-recurring engineering costs are much higher and you lose the flexibility. So you trade one against the other."

For a mobile phone, which is often discarded after one to two years, the benefits of implementing a full soft-solu-

tion might not justify the cost.

For example, an SDR solution for a handset might be helpful if you travel the world and need a device that can function across various networks in different regions. But not all consumers will be willing to pay the extra cost to get this functionality.

"You're not going to sell tens of millions of handsets on the basis that you can change the radio functionality. And if the unit is more expensive and uses more battery power because of that it's actually a detrimental thing," he said.

PCB Design

The process of designing PCBs for SDRs is also more complex. The speeds that devices are running at now are often faster than some of the RF signals coming out of the antenna, making digital board layout essentially an extension of RF design.

For example, in the past a signal that was around 2 GHz on a 3G connection might have been the sensitive one. But suddenly there's Serial RapidIO, PCI express, and other very high-speed interfaces that are actually running faster than the analog signals that technologists have traditionally had to worry about. At these frequencies, digital design needs to incorporate analog design techniques, which means more care in routing PCBs to avoid interference and EMC issues.

An added complication is that the FPGAs and SoCs present on SDRs have higher pin-counts and are more fine-pitched than components that would typically be present in an RF circuit, making it more challenging to get the signals around the board. At these speeds, simulation is especially important, and designs often face an extra iteration in board protoyping, because there's only so much that can be simulated. Designers need to build one, fine-tune the matching, and look at interference.

The other challenge is that the denser the devices become—the bigger the FPGA, or more complex the SoC—the more power they dissi-

pate, and the more clever designers need to be with thermal management. When designing for a consumer market, it's important to do it in a passive way—for example, liquid immersion or water-cooling techniques—since people don't like fans.

There are also more complexities when it comes to PCB manufacturing. Yao said his com-

pany works closely with the board and assembly houses to work through the technical requirements for each design.

For example, because of the presence of finepitch components, they rely often on plugged vias to do things like breakout fine-pitched BGA packages and provide heat-sinking capabilities for high power components.

But he said that the use and reliability of vias tends to be one of the most difficult requirements placed on board houses. In RF circuits, multiple vias are essential for providing a solid connection from the ground plane to a copper area on an outer layer. These vias are electrically redundant at DC. Because of this, a failed grounding may not be detected by a flying probes test, but will be detrimental at RF.

To avoid this, redundant vias are used. But the sheer number of small diameter vias used for this purpose poses a significant challenge for board houses with extended drilling cycles and demands on tooling.

Furthermore, when dealing with circuits operating in the GHz, ordinary FR-4 won't cut it. It's important to work with the board house to source appropriate high-frequency and highstability dielectrics. They also use controlled impedance and length matched traces in both RF and digital circuits. While the circuit layout is

You're not going to sell tens of millions of handsets on the basis that you can change the radio functionality.

SOFTWARE-DEFINED RADIO continues

critical to its performance, geometric stability is of utmost importance. Hence, there is a demand for geometric stability on each layer and also between layers.

They also work closely with the board house to simulate critical sections of the PCB, so as to be able to see the impact of their layout on their system. After production, critical traces are also tested for impedance matching and reflections.

There are benefits of designing SDRs, though. One benefit is that you can code certain things in software to improve the hardware performance—for example, sleep modes to reduce power or distort signals for better performance across impedances.

The Always-Connected Lifestyle

Watts did, however say that consumer demand for an "always-connected" lifestyle is driving the adoption of SDR in the consumer space.

"Apple and others have done a lot by providing applications that allow people to use their devices for many different things and suddenly they want everything to be seamlessly connected at home, on the move and at work," said Watts.

As a result, car and consumer product manufacturers are increasingly considering implementing SDR-type technology to provide connectivity.

And while today SDRs are still considered high-end systems with a foothold in defense and telecom sectors, the technology is increasingly being adapted to solve our day-to-day wireless problems, and perhaps will soon pave the way towards universal connectivity of our consumer devices. **PCBDESIGN**



Natasha Baker is developing SnapEDA, a PCB design community currently in beta at <u>beta</u>. <u>snapeda.com</u>. She writes a weekly column on the latest mobile apps for Reuters, and has written about

technology for other publications including Electronics World and Electronic Design.

video Interview

Intercept's Design Software Moving Into 3-D

by Real Time with... Designers Forum



Intercept Technology recently revamped the GUI of their Pantheon design suite. North American Sales Director Dale Hanzelka chats with Editor Andy Shaughnessy about the new interface, the challenges their customers are facing, and the drivers behind Intercept's journey into the third dimension.





Most-Read News Highlights from PCBDesign007 this Month

1 I-Connect007 Launches The PCB Design Magazine

The PCB Design Magazine will feature articles and columns by the biggest names in PCB design, including Lee Ritchey, Happy Holden, Mark Thompson, Istvan Novak, Doug Brooks, Barry Olney, and our newest columnist, Jack Olson.

2 Mentor Graphics Unveils Next-Generation PADS Flow

The scalable PADS 9.5 flow enables users to costeffectively design their products, from standard PCBs to the industry's most complex, highest performance, and densest PCBs. Enhancements in the PADS 9.5 release include the ability to switch to bottom view so the design can be viewed and modified from the bottom or top side.



SiSoft has released three Quantum Channel Designer design implementation kits for the Intel platform for communications infrastructure with the Intel Communications Chipset 89xx Series. Si-Soft has worked closely with Intel to develop these design kits which offer ready-to-run setups, allowing designers to quickly perform pre-route design space exploration.

4 IPC APEX EXPO 2013 to Hold Design-Focused Activities

For engineering staff and managers in design, sales, purchasing, and quality, the IPC Designers Forum is a full-day educational and technical exchange program focused on critical design issues. Dieter Bergman, IPC, will kick off the Forum with a discussion on roadmapping efforts in the area of design.
5 ICD Adds Floating Network Licenses for Analysis Software

In-Circuit Design Pty Ltd (ICD) has released the ICD Stackup Planner and PDN Planner with floating network licenses. "Customers can now download and launch evaluation versions which can be converted to permanent licenses using license activation," said ICD Managing Director Barry Olney. "This allows us to enable different features without the customer re-installing the software."



Agilent Technologies Releases EMPro 2012

Agilent's latest release of its 3-D EMPro software allows designers to more easily create 3-D models and analyze the electrical performance of packages, connectors, antennas, and other RF and highspeed components. It delivers a number of critical features.



Iron Atom Certifies Amazon GovCloud for PCB DFM

Iron Atom has certified Amazon Web Services' GovCloud for use with its fully automated PCB DFM Web offering. Iron Atom's DFM on-demand service uses Ucamco's Integr8tor product to perform the PCB data processing.



Mentor Graphics Corporation posted financial results for the company's fiscal third quarter ended October 31, 2012. The company reported revenue of \$268.8 million and GAAP earnings per share of \$0.27.

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ADS 2012 features new capabilities that improve productivity and efficiency for all applications the system supports and breakthrough technologies applicable to GaAs, GaN and silicon RF power-amplifier multichip module design.

Mentor Graphics Debuts New Thermal Testing Method

Mentor Graphics has released the T3Ster DynTIM tester, which measures thermal characteristics of thermal interface materials (TIM). Engineers can now perform more accurate thermal analysis when using the Mentor T3Ster DynTIM with Mentor's FIoTHERM and/or FIoEFD CFD solutions.



LIGHTNING SPEED LAMINATES

The Challenge of Routing High-Frequency Laminate PCBs

by John Coonrod ROGERS CORPORATION

SUMMARY: Yes, we're talking about the other type of routing. Designers of high-speed PCBs favor high-frequency laminates for their low loss and tight impedance control, but these materials can cause trouble for the router operator.

The routing of circuits made from highfrequency laminates can be more complicated than first assumed. This is due to the many different materials used in high-frequency laminates, and the fact that some of these materials will route differ- ent-

ly than others. Another point: These materials are s o m e t i m e s used as a hybrid construction, meaning dissimilar materials are combined to form the PCB.

Generally, there are three categories of high-frequency circuit materials: filled hydrocarbon systems, PTFE, and filled-PTFE systems. Within each of these families of products there are also glass woven reinforced and non-glass woven reinforced substrates. Additionally the filled PTFE systems often use different fillers in order to achieve certain electrical properties. All of these combinations of materials, fillers and reinforcement can have an impact on the cutedge quality when routing PCBs. The filled hydrocarbon systems are typically ceramic-filled. The many types of ceramic fillers have varying attributes. Electrical properties and thermal characteristics must be considered when choosing a filler type. The ceramic filler is used to adjust the dielectric constant and will add to its stability. Many ceramic fillers can adjust the CTE (coefficient of thermal expansion) to reduce the CTE to be closer to

> that of copper. Some ceramic fillers will be more or less abrasive to the drill and routing tools. In the case of the ceramic-filled hydrocarbon laminates, the filler will im-

pact the routing parameters and especially the tool life. Additionally, the type of routing tool used can be very important.

For instance, the recommended router for RO4350B, a high-frequency, glass-reinforced, ceramic-filled, hydrocarbonbased laminate, is a carbide

multi-fluted spiral chip breaker

or a diamond cut router bit. It is recommended to have the copper etched away in the router path. Some general routing parameters are shown in Figure 1.

These recommendations are generic and for illustration purposes. However, it is suggested that the material supplier should be

Surface speed	<500 SFM
Chip load	1.0 to 1.5 mil/rev
Tool life	>30 linear feet

THE CHALLENGE OF ROUTING HIGH-FREQUENCY LAMINATE PCBS continues

Figure 1: General routing parameters for certain high-frequency laminates.

involved in determining the proper routing conditions for a PCB using its materials.

The non-glass woven, ceramic-filled hydrocarbon materials are typically used in niche applications and have similar routing concerns. These materials are brittle and can fracture during different stages within the PCB fabrication process. However, routing is typically not a concern for fracturing. These materials are offered with a variety of dielectric constant and the filler used to adjust the dielectric constant has a different level of abrasion characteristics. Typically, the materials with the lower dielectric constant (4 or less) will be more abrasive and decrease the tool life. Furthermore the abrasive nature will cause the material to be more susceptible to poor edge quality issues such as burring. Again, the material supplier should be consulted for the optimum routing conditions for circuits made with its materials.

The PTFE-based high-frequency substrates often have different concerns than ceramic-filled hydrocarbon materials. The PTFE materials are relatively soft and can easily smear and have stringers at the routed edge. There are different techniques used to minimize this concern. A slower surface speed is typically used to reduce heating and a double-pass routing pattern is used as well. The double-pass routing is done in two different directions; the first pass may be counterclockwise, whereas the second pass would be clockwise.

The ceramic-filled PTFE systems are more forgiving in the PCB fabrication process than the non-ceramic-filled PTFE substrates. The addition of the ceramic filler adds some rigidity to the substrate as well as raising the thermal conductivity. The raise in thermal conductivity may slightly reduce the issue of overheating the substrate and causing smear during routing, however it still can be a concern. Sometimes this material is also available with woven glass reinforcement and the routing concerns are similar. However, the reinforced substrate may have slightly more issues with edge-cut quality. When routing either the reinforced or non-reinforced PTFE substrates and minimizing debris is critical, it is often recommended to have pre-routed vacuum channels in the backer boards.

Hybrid PCBs are becoming increasingly common. The combination of dissimilar materials used to create a multilayer PCB has many advantages, but there can be several fabricationrelated issues and one of these may be routing the circuits. When the dissimilar materials are significantly different in modulus, there is sometimes a concern at the interface of these materials regarding routing. Basically, the concern is that routing issues become complicated at the transition from soft to hard materials. The soft material will want to stretch and cause stringers, while the rigid material will want to cut away clean. These material transitions can be challenging depending on thickness differences and where the transitions occur in the circuit stack-up.

In general, the routing parameters should trend toward the needs of the soft materials, and as previously mentioned, the material supplier should be involved with the routing concerns to offer assistance in optimizing this process. **PCBDESIGN**



John Coonrod is a market development engineer for Rogers Corporation, Advanced Circuit Materials Division. About half of his 25 years of professional experience has been spent in

the flexible PCB industry doing circuit design, applications, processing, and materials engineering. Coonrod has also supported the high-frequency, rigid PCB materials made by Rogers for the past 10 years. Reach Coonrod at john.coonrod@rogerscorporation.com. calendar

events

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IPC Complete Calendar of Events

SMTA Calendar of Events

2013 International CES January 8-11, 2013 Las Vegas, Nevada, USA

18th Annual Pan Pacific Microelectronics Symposium

January 22-24, 2013 Maui, Hawaii, USA

43rd Annual Collaborative Electronic

Warfare Symposium January 29-31, 2013 Pt. Mugu, California



DesignCon 2013 January 28-31, 2013 Santa Clara, California

IPC APEX EXPO/Designers Forum February 18-21, 2013 San Diego, California

Medical Devices Summit February 28-March 1 Boston, Massachusetts



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The PCB List 3
Prototron Circuits Inc 13
Rogers Corp17
Sierra Circuits, Inc 21
Sunstone Circuits 33
Ventec 55

Next Month in The PCB Design Magazine

In the January issue of *The PCB Design Magazine*, we'll take a look at the state of design data transfer formats. There's a lot of talk about formats and standards, but which one is the best? Or, more accurately, which one is the best for you?

See you in January!