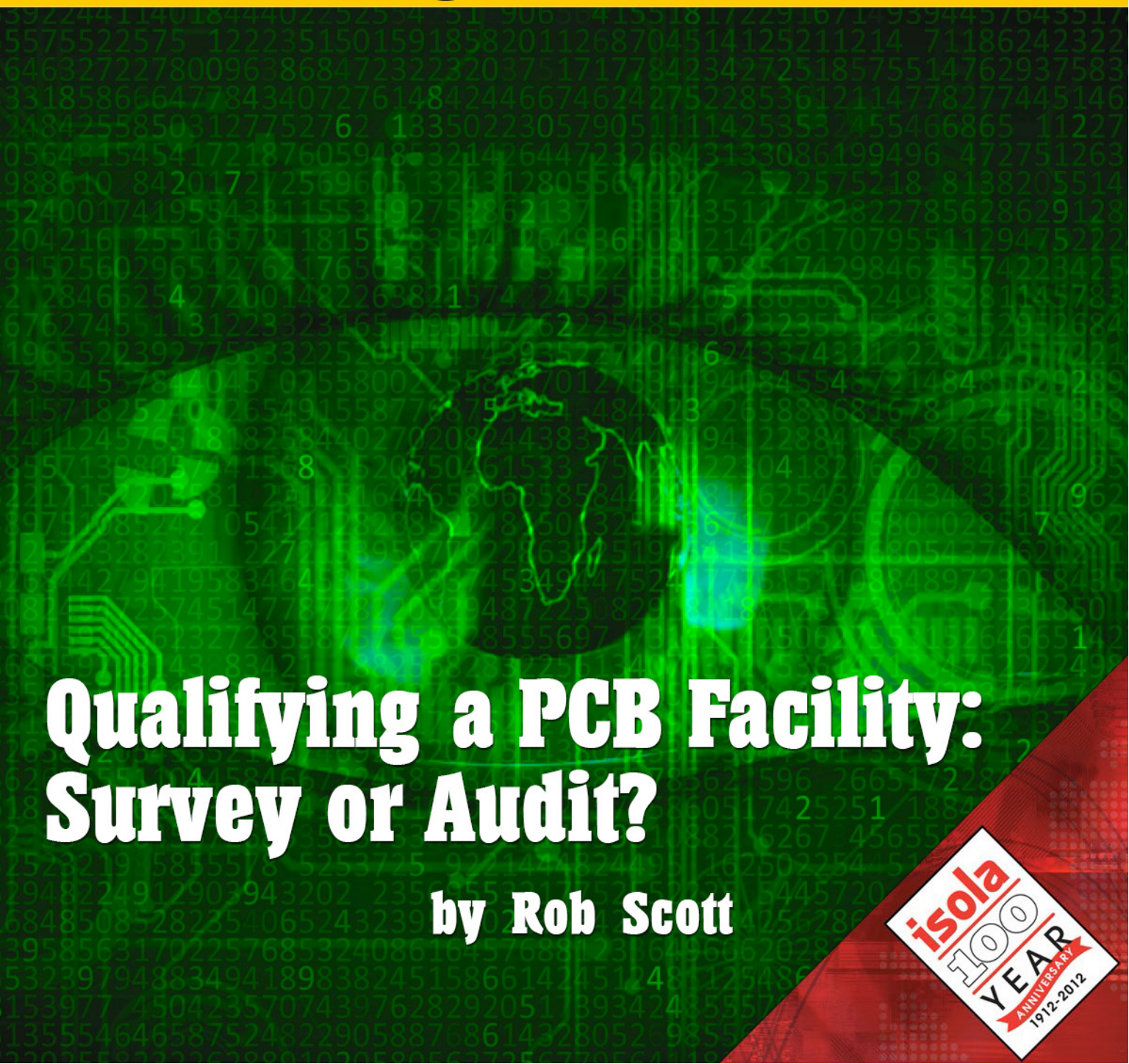
THE pcb design MAGAZINE

November 2013

AN I-CONNECT007 PUBLICATION

Qualifying Your Fabricator



Qualifying a PCB Facility: Survey or Audit?

by Rob Scott

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FEATURED EVENTS

Keynote Address — Tuesday, November 12, 2013

The Accelerating Technology Convergance in Medical Devices — Implications for the Future, Mark Kemp, President, Flextronics Medical

Panel Discussion — Wednesday, November 13, 2013

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THE pcb design MAGAZINE™
November 2013

This Issue: QUALIFYING YOUR FABRICATORS

FEATURED CONTENT

There are plenty of good fabricators out there, but how do you determine which shop is the best for your needs? Should you use a survey, conduct a site visit, or perform a full audit? This month, our expert contributors discuss the best methods for qualifying your next fabricator.

FEATURE COLUMN

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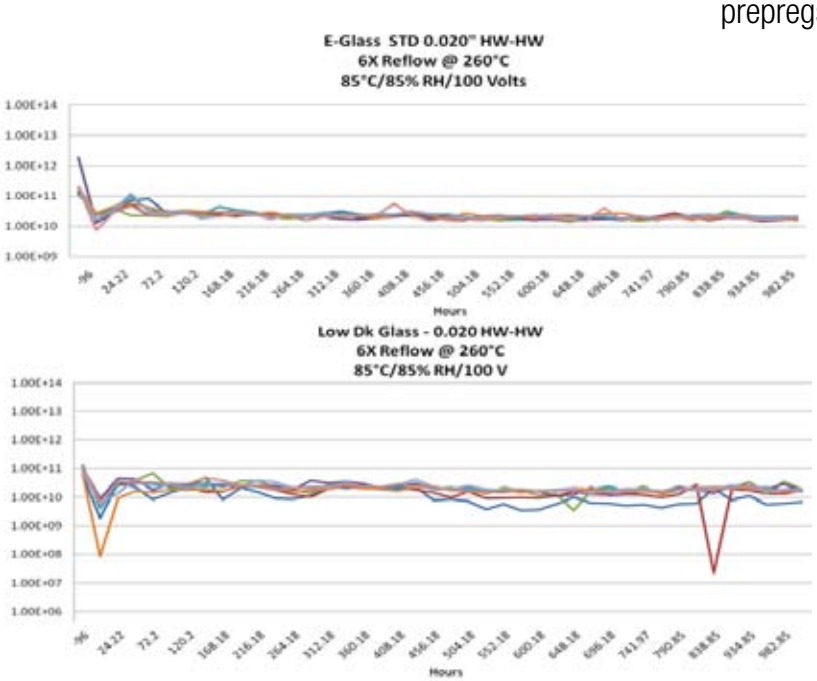

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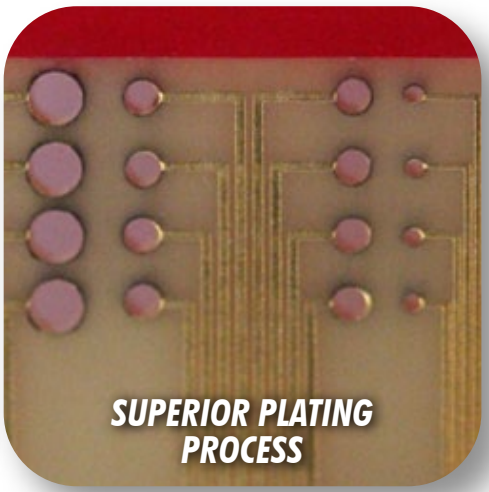

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THE SHAUGHNESSY REPORT

Happy Thanksgiving

by Andy Shaughnessy
I-CONNECT007

Another year has passed, and we're heading into the holiday season. Thanksgiving is just around the corner. Right now, I'm thankful for my new Sharper Image Shiatsu Massage Cushion, which is threatening to turn me into a blob of jelly.

I considered getting a massage chair, but this does everything a chair can do, and it fits right into my office chair. Ahhh…man, that feels good!

The rotating massage "wheels" start grinding down in your lumbar area, and they work their way up your back, though you can set it to massage just your upper back or lumbar. You can also vary the intensity of the massage from "gentle" to "on the verge of painful," which is how I like it. It may work too well; a minute ago it just about pushed me out of the chair. But it feels so good.

I'm all for better living through electronics. Is there anything that electronics can't do? (My iPhone now has its own guitar tuner, and it's a free app. There's even a new bra that sends out a Tweet every time the wearer takes it off. No

prurient intent here; it's designed to raise breast cancer awareness.)

This massage cushion is one of my rewards for living a healthier lifestyle since turning 50 this summer. You know how it is: You start taking better care of yourself when you reach the mid-century mark. You start assessing your situation and making plans for the future.

So, I'm exercising more and eating better. I've quit eating second (and third) helpings. No more eating fried foods, except when I really want something fried, which isn't that often. There's no chocolate in the house. I eat yogurt sometimes, and I ate half of an apple last week.

But on the flip side, it's also important to enjoy life. Pale ales and pizza won't kill you, unless you overdo them. It's all about finding that perfect balance. It seems to be working: Three months into my 51st year, and none of my body parts have quit working, at least that I know of. I still have all my hair and I'm still around 200 pounds.

As I sit here being vibrated out of my chair, I'm also thankful I can make a living in a fantastic industry that's full of interesting people. Your co-workers and colleagues may be good, bad, ugly, or all three, but they're real characters.

One thing that intrigues me is how little anyone "outside the bubble" knows about circuit boards, much less EDA software. You tell new neighbors what you do for a living, and they give you that look; you know the look. Then they ask, "So, you work with computers, right?"

Working in the PCB community is almost like belonging to a religion, or maybe even a cult. We have our own larger-than-life leaders. We follow customs that have been around for decades. And we tell and retell the same parables, like the wistful tale, "How Things Used to be in the Valley." That's one that everyone knows!

> ***Speaking of 2014, it looks as if next year will bring the circuit board industry more of what we've seen in 2013: single-digit growth, for the most part. But that's a lot better than no growth at all. We've all lived through worse times, in the not-too-distant past.***

As a former newspaper reporter, I like the fact that there's never a dull moment in the world of circuit boards. Design, fabrication and assembly are evolving so fast that it's tough to set any kind of a baseline for what's mainstream and what's cutting-edge. But despite being in a constant state of flux, this industry never quite throws off the old ways completely. Sometimes it seems as if we have one foot planted firmly in 2014 and one stuck in 1970.

Speaking of 2014, it looks as if next year will bring the circuit board industry more of what we've seen in 2013: single-digit growth, for the most part. But that's a lot better than no growth at all. We've all lived through worse times, in the not-too-distant past.

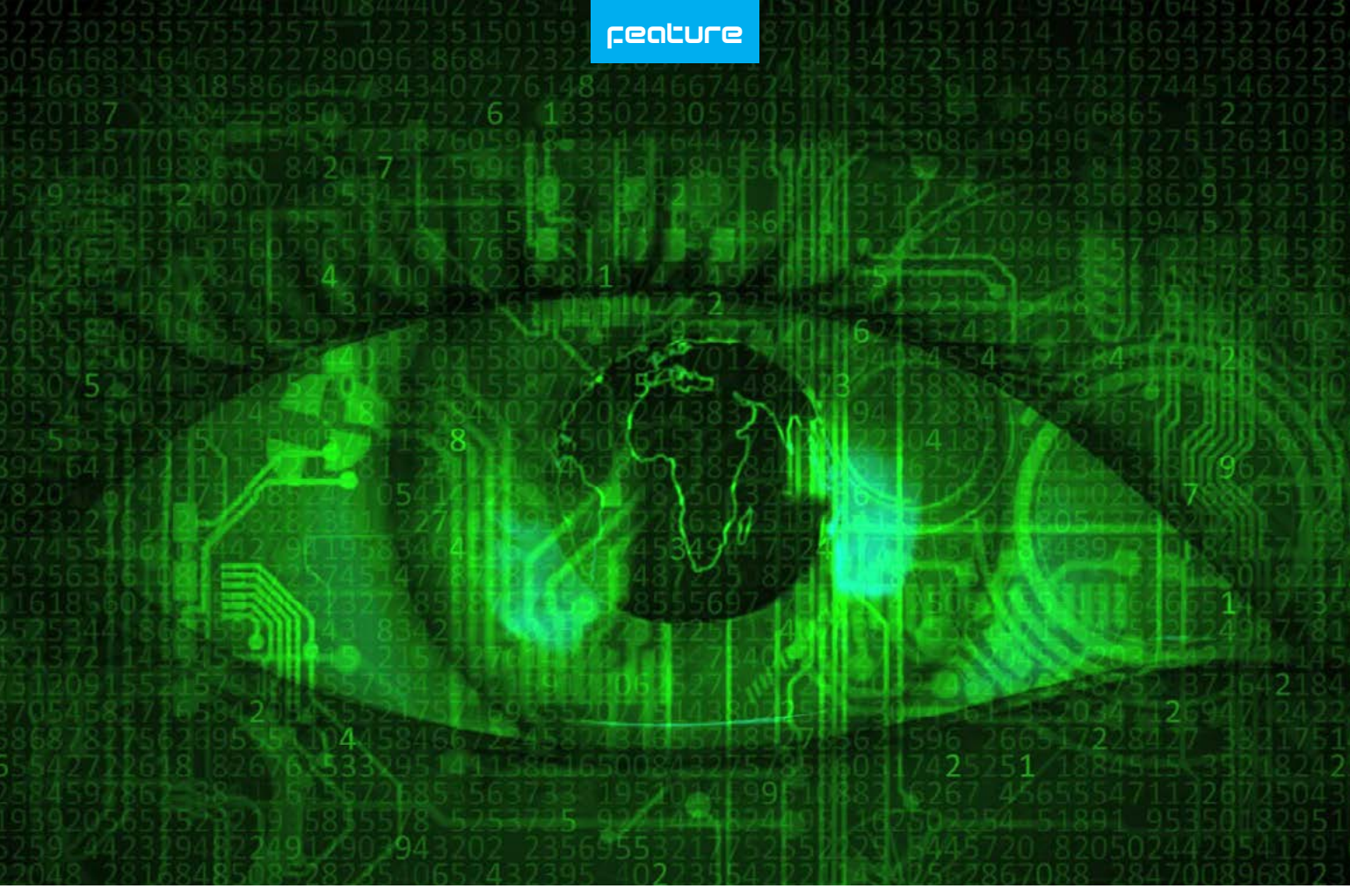
Lastly, I'm thankful that my dad is, most likely, going to be around for his 88th birthday in December. His last checkup was fine, and his doctor said there's nothing wrong with him. At this rate, we may all wind up living to be 100.

Let's take the time to celebrate the good times, which are happening right now while we're making other plans, to paraphrase John Lennon. Get a massage cushion, go to the beach, or rent a cabin for the weekend. Or just spend some quiet time with your family.

Now, excuse me while I shut this crazy thing off. I hope I can still walk.

Happy Thanksgiving! **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 13 years. He can be reached by clicking here.



Qualifying a PCB Facility: Survey or Audit?

by Rob Scott
NEXT LEVEL PCB

SUMMARY: There are surveys, and then there are audits. For the PCB designers of today, working with an audited company will minimize bad results and provide a greater level of trust. If you're an OEM, you can also market the fact that your boards are fabricated by an independently audited facility.

The History of Qualifying a Fabricator

First, let's clear up any confusion regarding surveys and audits. The definition of "survey," according to Merriam-Webster's Dictionary, is "to go around and approach (people) with a request for opinions or information." Webster's also defines "independent audit" as one "made by professional auditors who are wholly independent of the company where the audit is being made."

I learned this back in the seventies, when I was in charge of our company's customer surveys. As I recall, each survey had a different twist depending on my position at the time. As manufacturing manager, I directed it a certain way. I would dazzle the customer with equipment capabilities and processes. Later, as a sales manager, I shared our customer base. I impressed the buyer by telling him that we were building boards for some of the Silicon Valley's best companies. I showed off our most difficult boards to give the buyer the idea we could build their designs.

As president of the company in the eighties and nineties, I invited customers in and

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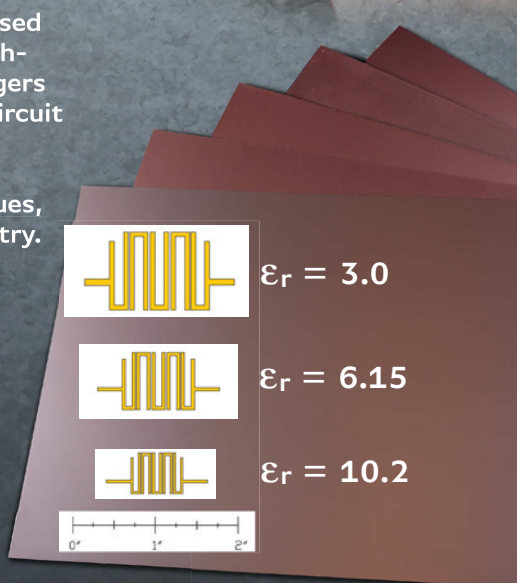

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asked for any opportunity to come and survey us. "Oh, you need a 12-layer? We can do that; here's a 36-layer board." We sold on perception.

As a fabricator, we didn't know in detail what the customer was looking for. They had their own agenda. Come to find out it was to get a feel for the facility and our staff. There were no real quality details in a survey. I could tell some of these people just wanted to get out of the office; they had a few notes on a clipboard and they asked for the latest buzz words. So we showed off our lab, handed out safety glasses, and spent time in waste treatment.

Surveys started getting more serious as complexity, delivery and quantities grew. Tier 1 companies hired PCB engineers to form qualification teams. Those customers spent hundreds of thousands of dollars for those teams in travel, salaries and expenses. All of this made sense with the volume and the potential risk of failure associated with not conducting an audit.

By this time, a fabricator had to truly understand assembly challenges and difficult designs with DFM requirements. ISO, IPC, and Mil-Spec standards were the QA standards to have. Our SPC charts, new equipment announcements and quality practices such as TQM and Six Sigma were displayed outside each department.

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Survey vs. Audit

Cut to 2013. When I speak with board house managers, they ask, "Why do I need another survey? I just spent last week with two customers." The reason is that the buyer's team wants to trust your facility, and they require measured results. But a survey is just a survey; it is not an audit.

When should you conduct an audit? As always, it depends on the project. One design manager told me, "We often fly blind when it comes to selecting PCB and other EMS suppliers. We usually select suppliers by word of mouth. If we do send an audit team, it's going to go without saying that we would never be able to get into the detail that I saw on your audit form."

Whether you're a PCB designer, OEM, CEM, or rep group looking to qualify a facility for your customer, there must be a value proposition. How about saving time and money from rejects and reworks? (God forbid it's found after assembly.) Or maybe you want to qualify a PCB facility for the first time. What if a new design is pushing the fabricator's capabilities? Maybe you're hearing, "They're OK at 5-mil lines and spaces, but this design is 3-mil lines and spaces." Or "They say they can build to those specifications, but we need it certified to IPC-610-H."

This is a whole different ballgame. Until you review what is required for IPC Class 3 certification, you'll need verification from an outside lab. Trusting the word of a salesperson who has been cold-calling you for a month trying to get an order gets old faster than a two-for-one special. Asia is notorious for this. Currently there are Asian buyers coming to the U.S. for Class 3 certification.

The complaint is that the Asian fabricator says he can build to Class 3. But that's where it gets lost in translation. Why can't the Asian manufacturer certify by supporting all of the tests and paperwork required by IPC? All these headaches must get tabulated and compared to the cost of hiring an auditor who provides your company with the proper documentation. It's a simple matter of building trust versus hoping the fabricator gets it right.

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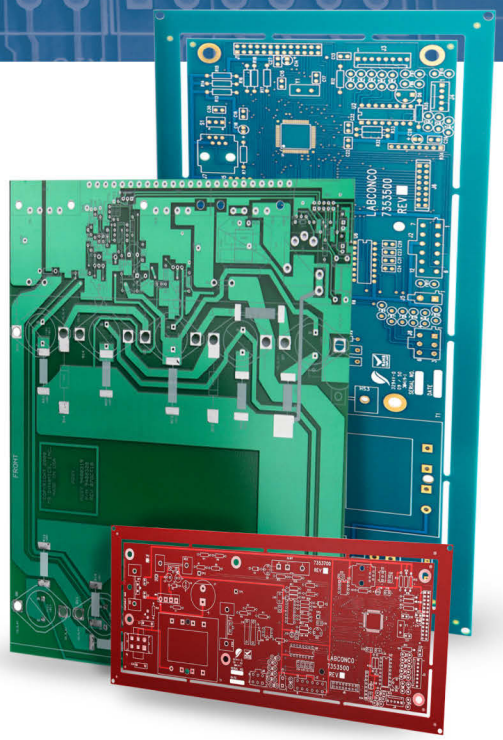

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What Goes Into an Audit?

First impressions are lasting. The audit starts when you pull up to the front gate. I audited a Mil-Spec ITAR-registered facility that specialized in mil-aero work. Their American flag out front was terribly tattered and faded. That struck me as odd.

A facility that is proud of its capabilities will request an agenda, or ask for the audit 30 days in advance. Then the audit can be reviewed,

SAMPLE METHODOLOGY FOR AUDITING A PCB MANUFACTURER

AUDIT RESULTS

The SQE auditor must complete at least 14 of the 22 processes before an audit result can be declared. It is strongly recommended that all 22 sections of the audit be completed.

The Quality Process Audit (QPA) consists of two scoring sections: major and general. The major items are considered very critical items and will have a higher required minimum score in order to pass the audit. To pass the audit, the supplier will have to meet both the minimum required score for both major and general audit items.

Items identified in the major categories require a minimum score of 90% to pass, and this score will be summarized in the spreadsheet Major Item Summary. If an overall major items score is equal to or greater than 90%, a "Pass" status is awarded.

The overall process average result determines the Audit score achieved for the PCB supplier assessed. The "Pass" score for the General Audit Items is 80% for all PCB products irrespective of complexity. If an overall process average score for the General Audit Items of equal to or greater than 80% is achieved, and no individual processes have failed, a "Pass" result is awarded.

If one or more individual processes have failed, but an overall audit score of equal to or greater than 80% was achieved, either a "Conditional Pass" or a "Fail" result shall be awarded. The determination of this audit result is at the discretion of the (NLPCB) Next Level PCB auditor, based on the severity of the issues for any of the failing sections. If the overall process average score is less than 80%, a "Fail" result is awarded.

If a "Conditional Pass" or "Fail" result is awarded, a Corrective Action Plan is due from the supplier within two weeks of the date of audit completion. The Corrective Action Plan must contain a timeline to "bridge" to a "Pass" status and must propose a target date for an NLPCB auditor to possibly do a follow-up audit, time and expense permitting. Failure to achieve a "Pass" result on the follow-up audit may impact business award decisions.

AUDIT MECHANICS and QUESTIONS

The audit breaks down the PCB manufacturing process into individual process steps, each of which is represented by an Individual worksheet. Within each worksheet is contained a series of questions specifically pertaining to the process being examined.

These questions are focused on evaluating Process Disciplines, Control Methods, Process Capability/Technology, and Attention to Detail.

The questions were devised and developed as closed questions with every attempt to avoid ambiguity. Because of the closed nature of the questions, there can only be one of two answers to any question, i.e., Yes (1) or No (0).

Thus, the criterion is either fully met or it is not. If the criterion is met, a score of 1 is obtained. If the criterion is not met, a score of 0 is obtained. If there is any doubt as to the score to award for any given criterion, a score of zero shall be awarded by default.

Any criterion that scores 1 shall be clearly demonstrated, followed, and be beyond reproach. In the event that a supplier clearly meets the intent of the audit question, but does not exactly do what the question asks, a score of 1 shall be given.

filled out, and compared to the auditor's findings at the audit date. The audit goes smoothly, saves time and money, and everyone understands any corrections or improvements. The audit is a valuable tool for buyer and manufacturer.

As an independent auditor having performed 50-plus global audits, I have found that there is one common denominator in every audit. The contact person, usually the SQE or QA manager, gets nervous. His fear is that if the manager's performance is negative, it reflects on the company. They might even get defensive over a direct question and try to avert it. The auditor is asking questions in detail. The manager wants business and realizes that not passing the audit will upset sales and management. If an SPC chart is missing entries, the manager gets nervous and makes an excuse. If I pull out a thermometer to check the temperature in a heated bath, they get worse. I'm sure no buyer on a survey has ever done that! Usually that manager gets very quiet. They also try to speed up the audit. It's my responsibility to create a relaxed and honest experience. As W. Edwards Deming said, "Just give me the data."

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Many facilities that have expanded will experience manufacturing flow issues. Knowing the flow of manufacturing is a must, but understanding how the facility deals with it can be difficult from a quality standpoint. Facilities that are well organized have confidant employees and supervisors that are very proud of their department, and it's just another day for them.

I've noticed that many board house managers who are secure about their company's capabilities will smile throughout the audit, and not break out in a cold sweat. Does this describe you?

Conclusion

Independent audits are a proactive chance for a manufacturing manager to improve his capabilities by having a second set of eyes on the operations. For the PCB designer, working with an audited company will minimize bad results and provide a greater level of trust. If you have end-customers, you can market the fact that your boards are fabricated by an independently audited facility.

One word of advice for manufacturers and design buyers: Adhere to IPC-A-600 Rev H. The scope of that document describes the preferred, acceptable, and nonconforming conditions that are either internally or externally observable on printed circuit boards. It represents the visual interpretation of minimum requirements set forth in various printed board specifications, e.g., IPC-610 series, J-STD-003, etc.

To properly apply the content of this document, the PCB should comply with the design requirements of the applicable IPC-2220 series document and the performance requirements of the applicable IPC-6010 series document. One of the first QA requirements I look for is Certified Specialists on staff. I urge each manufacturer to send staff, as time and money permits, to get certified to those standards. There are a number of contract companies that IPC will recommend to train and certify your staff. **PCBDESIGN**

Rob Scott is the owner of Next Level PCB, a provider of auditing services. He is the former owner of Phase II, a Northern California PCB manufacturer that specialized in quick-turn prototypes and high layer-count boards for more than 28 years. He was president of the California Circuits Association and a nine-year member of the IPC Board of Directors. Scott can be reached by clicking here.

Qualifying Your Fabricator: Identifying Winners (and Losers)

by Mark Thompson, CID+
PROTOTRON CIRCUITS

This month, I am once again weighing in with tips on qualifying a fabricator. In previous columns, I mentioned three things everyone should expect from their fabricators:

- Quick quote responses
- Outstanding quality
- Consistent on-time delivery

I would like to add that, based on today's board complexities, a review should be done prior to quote to make sure no manufacturing issues occur. This is critical when it comes to things like minimum pre-preg interfaces on high-copper coil boards or jobs with unique reference planes for various impedance scenarios. A potential customer would much rather be told up front that a given design is not producible than to wait three days for a quote, only to have the part go on hold after release to manufacturing because a good review was not done prior to release.

Quote Me on This

So, let's start with the quote process. Whether the part is a simple double-sided part or a complex multilayer with numerous needs, you really would like to see a quote response back in a few hours, not a few days. Additionally you want accurate quotes that have taken into consideration all aspects of the board, such as drill time based on hole quantity, additional time for AS-9102 or Class 3 6012, first article reports, and any additional time if outside services are needed.

A three-day quote should be just that, regardless of your location and any outsources you may require. It is never good when a three-day is quoted but due to outside services or time zones still results in delays. Make sure any questions you have are asked up front to avoid these delays. Also, make sure there is a contact available for expedites.

As an example, let's say your cut-off time for expedites is 12 noon PST. If an expedite has is-

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QUALIFYING YOUR FABRICATOR: IDENTIFYING WINNERS (AND LOSERS) *continues*

sues after release to CAM, many times the East Coast customer has gone home for the day.

It used to be that if your fabricator was on an AVL and they performed well for you, you were set. But in today's economy, we see more buyers being asked to source multiple fabricators to have a better pool for selection. It used to be you would send the more complex PCBs and your simpler boards to the same fabricator. This is seen less frequently these days. Project engineers turned PCB designers and buyers are looking at specific fabricators for specific board complexities. Gone are the days you would send a 4–6-layer with no special requirements to the same place you would send the high-end, high layer count HDI impedance parts.

Again, what do you want? Fast and accurate quotes? Remember, you get what you pay for. What do I mean by that? All fab shops are not the same. Some shops will help you with design aspects and manufacturing solutions, but others will not. (If it does not fit the mold, it's just not possible.) Having a good engineering support person at a fabricator is worth his/her weight in gold.

Again, what do you want? Fast and accurate quotes? Remember, you get what you pay for. What do I mean by that? All fab shops are not the same. Some shops will help you with design aspects and manufacturing solutions, but others will not. (If it does not fit the mold, it's just not possible.) Having a good engineering support person at a fabricator is worth his/her weight in gold.

And many times this means the difference between a win and a loss. As I've said before, one of the best ways to get to know your fabricator is to take a tour of their facility. This gives you a good idea of what they are capable of and how certain processes work.

The Quest for Quality

Now let's talk about product quality. This issue goes far beyond board cosmetics with today's boards. Sure, when your QA department opens that box, they want to see that the parts look good, mask is consistent with no missing mask webs or skips, the board is registered well, the surface finish is a uniform color with no oxidation or de-wetting of final surface finish, and drill registration is good.

But more and more, the PCB depends upon things that are not necessarily visible. This includes things like pattern accuracy on RF applications and unseen challenges like controlled impedances. Speaking of which, more times than not these days our customers are asking for impedance calculations and stack-ups after design but prior to the layout stage. This is something that we fabricators have been advocating for some time.

You veterans, and that's many of you, may have noticed that fabricators now ask many more questions than we used to. Years ago, we only asked you:

1. What trace sizes are being controlled?

2. Where do these traces reside? We ask this as fabricators not because we can't necessarily tell where the reference planes are for the given structures, but because you may not be controlling the same size trace on another signal layer somewhere else in the stack.

3. What is the threshold desired: 50, 90, or 100 ohms?

4. What is the tolerance associated with the impedance traces? For this one we understand you want them as perfect as they can possibly be and hopefully your fabricator is using a Polar Instruments field solver, or one just as good. You want a field solver that allows you to enter information about over-etch, under-etch, too much plating, too little plating, too much mask, etc. This is to ensure the numbers you use take the best hit through all the processes. Generally, 10% is accepted, but many fabricators ask for +/-15% for structures .1 mm or .004" and less.

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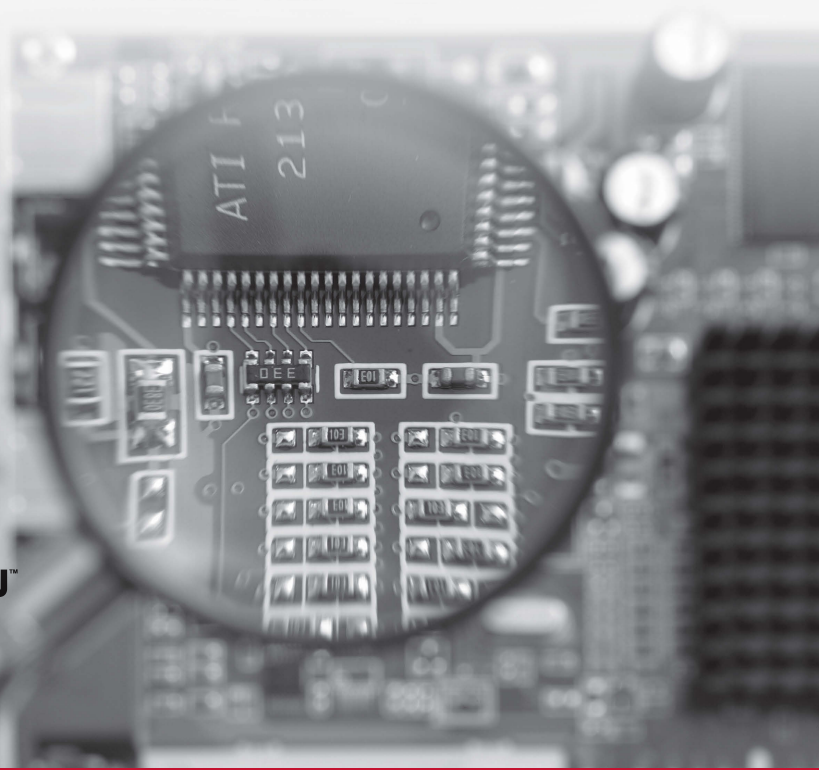

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QUALIFYING YOUR FABRICATOR: IDENTIFYING WINNERS (AND LOSERS) *continues*

Today we ask more questions before we give you calculations and stack-ups. First, will there be any co-planar structures? Or in simpler terms, will there be any poured copper closer than 3x the intended impedance trace width that would induce co-planar coupling? Many times the answer is no, but when the job comes in, sure enough, at some point the engineer has asked them to add additional copper pour for shielding, which induces co-planar coupling and must be calculated as such.

Many fabricators run the calculations for the given structure both as free space and as co-planar coupled. If the impedance hit is negligible, often a fabricator may not even bring it up. Generally on today's boards any co-planar structures will be on the outside and can be fairly easily recognized by the fabricator with RF launches at the part edge or tapered waveguides, or even just as very wide traces that are usually the only co-planar coupled structures on the outers.

Additionally, we will ask what color the mask will be. Back in the day, with traces wider than .1 mm, the mask color made little or no difference. Today, you may get a fabricator asking what color the mask will be if the traces are .004" or less, as the thickness of the mask plays a part of the impedance as it can be anywhere between one-quarter and one-half the width of the .004" trace over glass.

Many times, if you are asking your fabricator to provide trace and space and possibly ground separation distance (g-sep) values for a given impedance design, the fabricator will send you an impedance checklist with specific questions regarding the board so that when the job gets released to the fabricator for a build, there are no surprises.

"Back in the day, with traces wider than .1 mm, the mask color made little or no difference. Today, you may get a fabricator asking what color the mask will be if the traces are .004" or less, as the thickness of the mask plays a part of the impedance as it can be anywhere between one-quarter and one-half the width of the .004" trace over glass."

Recovery Time

If something should happen in the fabrication cycle that requires a remake, look for a shop that minimizes recovery time and has a process to minimize the likelihood of its reoccurrence.

On-Time Performance

Likewise, if a fabricator is consistently late on orders, you may want to seek another fabricator. A good fabricator, especially in the fast-turn prototype environment, understands the customer's time-to-market constraints and meets the expected deadlines, even sometimes shipping early if the customer allows. By the same token, I am a big advocate of communication to minimize costly iterations. This not only keeps the revisions to a minimum, but in a proto environment, good communication allows us to share any possible concerns about transitioning to large volume.

I can't tell you how many times I have had customers thank me for that last one. Offshore production volume shops may be lower in cost, but the product must still perform as expected. Prototype shops can traditionally pull off feats that production shops may balk at in large volume.

Of course, cost is always a factor. But a board buyer also knows the value of quality, service, and delivery can have a huge impact on the overall cost of the product's market cycle. **PCBDESIGN**

Mark Thompson is in engineering support at Prototron Circuits. To contact him, click here or call 425-823-7000. Feedback is appreciated.

video interview

Tips on Qualifying a Flex Fabricator

by Real Time with... SMTAI

Dave Becker, VP of sales for All Flex, discusses the current state of the flex industry, and he offers some tips on qualifying a flex manufacturer, based on his article in *The PCB Magazine*.

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Collaboration to Produce Carbon Nanotubes and Graphene

Felda Global Ventures Holdings Bhd (FGV) has collaborated with Cambridge University scientists to to produce the world's first high-grade carbon nanotubes and graphene.

In a statement, FGV chairman Tan Sri Mohd Isa Abdul Samad said the world's largest crude palm oil producer will be the pioneer in producing the nanotubes and graphene, which are by-products of crude palm oil and other hydrocarbons.

Under the MoU, both parties will develop an innovative downstream production line of high-grade nanotubes and graphene using state-of-the-art and newly developed nano-systems technology. This feat culminates years of efforts by scientists around the world to harness this promising material. High-grade carbon nanotubes and graphene has the potential to launch a new generation of electronic devices that run faster while using less energy: a new era of nanotube electronics that has long been considered a potential successor to the silicon transistor.

Apart from electrical devices, carbon nanotubes and graphene have the potential usage for next-generation communication cables, including underwater cables. By converting carbon-containing by-products, this revolutionary invention in green technology is expected to change global industries from aviation, oil and gas, electricity, and nuclear power, among others, while paving the way for a safer and more sustainable ecosystem. The proposed joint venture between FGV and Cambridge Nanosystems Ltd. will form a strategic partnership that will enhance value for both parties.

FGV will provide the raw material for the production of carbon nanotubes and graphene while Carbon Nanosystems Ltd. will provide proprietary technology to produce carbon nanotubes that is produced via a nano-systems technology.

PCB007 News Highlights

Bay Area Circuits Announces Silicon Valley Expansion

The company has relocated to a 30,000 square-foot manufacturing facility in Fremont, California. In addition to a significant increase in capacity, the additional manufacturing space will enable more in-house capabilities along with faster turnaround times.

Natel Acquires EPIC Technologies

"We are extremely pleased with the addition of EPIC because it strengthens and expands product solutions to include higher-level full system integration capabilities, as well as additional opportunities to reduce costs for our customers through the geographical distribution of our manufacturing locations," said Natel President and CEO Sudesh Arora.

Falcon PCB Group Reveals Rebranding Effort

A sustained period of investment both in plant and personnel has enabled the group to develop the high-technology rigid PCB facility, Merlin Circuit Technology Ltd. and the flex and flex-rigid facility, Merlin Flex-Ability Ltd., which have both been upgraded.

Printed Circuits Inc. Boosts PCB Manufacturing Capabilities

PCI has added a Uyemura ENIG/ENEPIG plating line to their wet process area, giving customers the ability to specify a traditional ENIG final finish on their circuit boards, or an option for the newer ENEPIG plating. ENEPIG allows PWB manufacturers single pass final finish, with high-reliability assembly yields on both wire-bondable and surface-mount components.

Candor Industries Develops New Selective Plating Process

The company, a Canadian-based high-technology PCB manufacturer, announces the development of an innovative selective plating process dubbed the "Partial Plating Process." This unique process allows designers to have a PCB with no plating on select areas of the surface, yet still have full plating within vias/through-holes located in those same areas.

IPC's PCB Industry Results for August: Stalled Growth

"Just as the North American PCB industry began showing signs of renewed growth, it was hit by some negative market developments, most notably reductions in U.S. military spending," said IPC's director of market research, Sharon Starr. "This was especially evident in sales of rigid flexible circuits," she explained.

Aismalibar's Flextherm Earns UL Certification

Eduardo Benmayor, managing director, says, "3D designs with bendable insulated metal substrates are on the cutting edge of technology. Many leading OEMs and CMs are currently utilizing the capabilities of Flextherm to meet their thermal management objectives."

American Standard Circuits Acquires First EIE Photoplotter

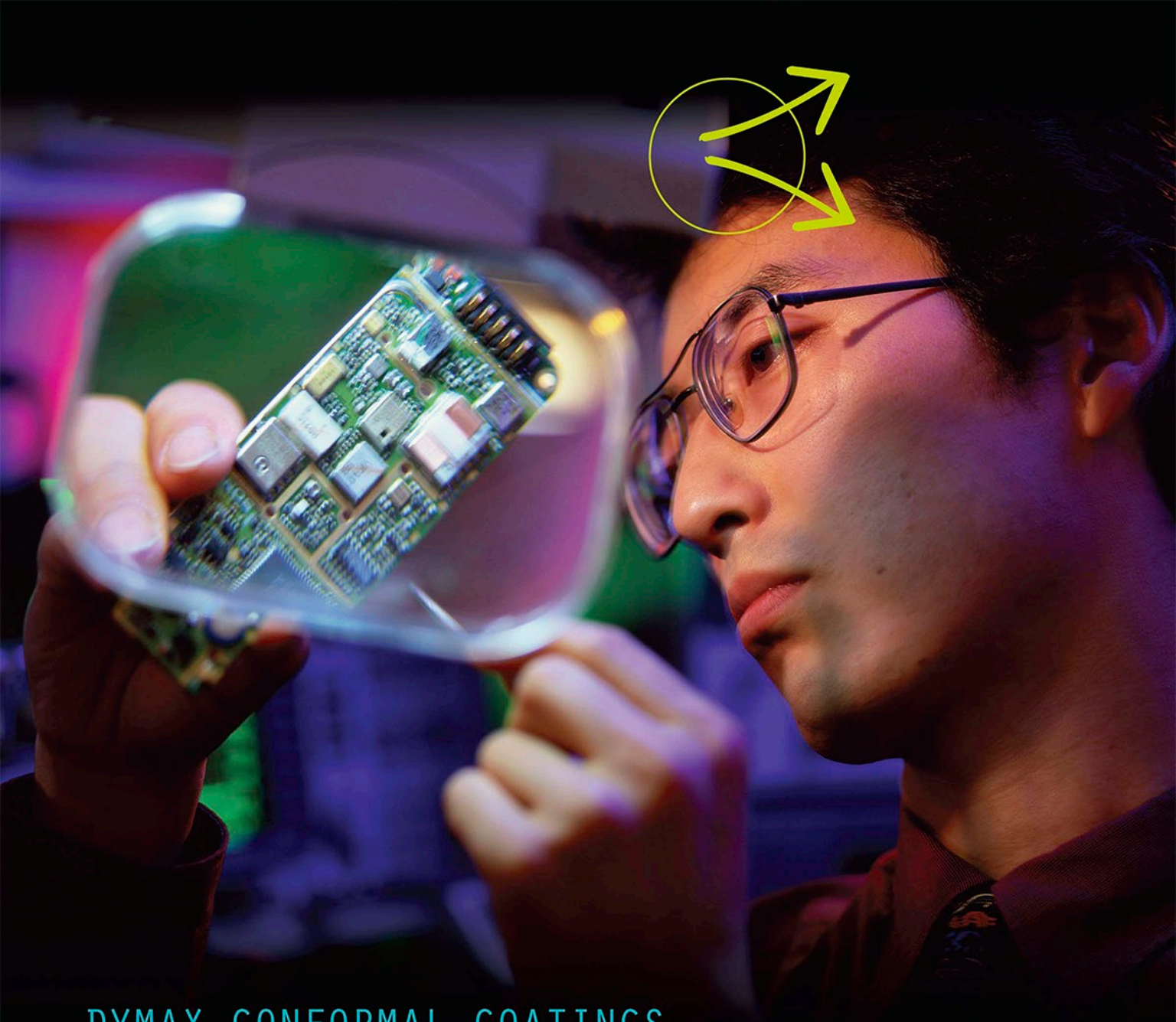
Chicago-based circuit board manufacturer, American Standard Circuits, Inc. (ASC), has announced the recent purchase a First EIE RP212+XT photo plotter. The new acquisition will allow the company to increase process capability as well as overall throughput.

IPC Report: World PCB Market Grew 1.7% in 2012

"The report's estimates are developed through a consensus process involving leading analysts worldwide and the data is trusted within the industry," says Sharon Starr, IPC director of market research. "If you need to know what kinds of PCBs are being made where, the World PCB Production Report will tell you, in detail."

Integrian Holdings Wins Bid for Endicott Interconnect

The sale of Endicott Interconnect's assets to Integrian Holdings LLC was approved by a federal bankruptcy judge on Thursday, September 26, 2013.



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FAQ: Qualifying Fabricators with Kelly

by Andy Shaughnessy
I-CONNECT007

SUMMARY: Kelly Dack, a senior PCB designer for a gaming technology company, is always on the lookout for good fabricators, occasionally conducting site visits to gauge a manufacturer's qualifications and capabilities. We asked Kelly to give us a rundown on his process for qualifying fabricators, and some of the criteria he uses.

Andy Shaughnessy: How do you identify a potential new bare board supplier? How do you narrow the field?

Kelly Dack: I stay in touch with the industry. I go to electronics trade shows where I can meet, talk, see, touch, learn and compare. When I can't travel, I read the trade publications and refer to their advertising to monitor who's out there and what they are doing. I find the online directories of PCB service suppliers very helpful.

I get a chuckle when using an online service like The PCB List to search for a supplier. It's very comparable to how my single co-workers describe searching for a partner on Match.com, and just as easy! Like a dating site, The PCB List's search attributes of board type, market, region, company type and industry can match a customer's needs with a PCB fabricator capabilities. So whether "speed dating" on-site at a trade show or utilizing the Internet, I've made quite a few matches out there using these methods and I'm happy to report that our relationships are still going strong!

AS: What are some of the criteria you have in mind when you look at a new fabricator?

KD: The capability/cost ratio is key. It is important to note that when a PCB designer goes searching for a PCB supplier partner, it is usually to fulfill a prototype requirement costing hundreds or thousands of dollars. PCB prototype designs are usually ordered in small quantities at a higher price per unit. Quick-turn requirements of hours, days or weeks are common. In a parallel universe, production fabrication suppliers are usually courted by a company's supplier management group. Selecting a production supplier involves a different set of criteria: lowest cost per unit, higher manufacturing volumes and scheduled deliveries. Third-party EMS assembly suppliers spend millions.

I have always held to the philosophy of developing and maintaining business relationships with two proto suppliers for each class of board that is being designed. The reasons are plain and relate primarily to a capability/pricing ratio. In the world of high-tech manufactur-

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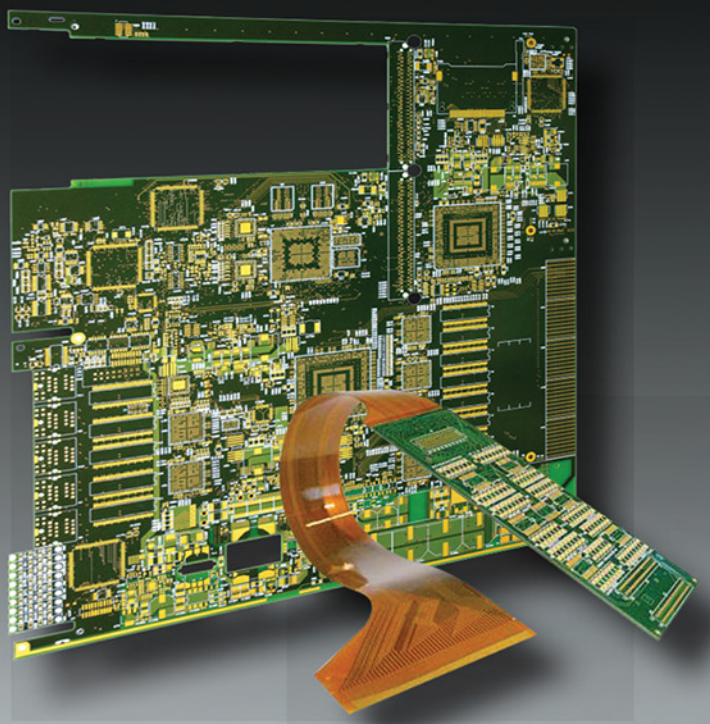

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ing, "You've gotta pay the cost to be the boss." Companies that have invested in high-tech machinery will have to charge higher pricing to cover the cost. So it just doesn't make sense to send a low-tech board to a high-tech supplier and expect low cost. Simple boards do not need to be built at a class 3 board shop; they can be directed to a shop with less capability and overhead, theoretically with a cost savings.

Maintaining two shops for every class of board encourages competitive quoting and price checking, and also ensures proto supply chain redundancy should one of the suppliers experience any down time. Take care to not engage too many suppliers at a time. I've found it always better from a business standpoint to keep one or two suppliers fat, happy and loyal, rather than to spread jobs around to too many suppliers.

AS: What is the first step in the qualifying process?

KD: The first step is assessing the ability of both the supplier and customer teams to communicate! Regardless of pricing come-ons, manufacturing capabilities and promised quality, the ability to bond business contacts—buyers with sales, designers with manufacturing engineers and CAM, quality assurance and shipping with receiving—is a huge step not to be missed. A good understanding by all regarding what to do and who to contact when problems arise (and they will) lays the foundation for success once the supplier is fully qualified.

AS: How important is location of the shop?

KD: While still important in real estate deals, "location, location, location" is less important to the PCB customer than ever before. In a global manufacturing arena, the importance of location is mostly a concern of the supplier. The PCB supplier is concerned with location due to staffing, supply chain and environmental requirements. The customer enjoys the fact that UPS, FedEx and other courier services have greatly reduced the need for a local supplier. Overnight delivery is only a fraction of the cost of an order and overnight is overnight almost anywhere in the world, regardless of the origin of shipment.

AS: Can you assess the shop's processes without visiting it?

KD: Not all of us can go jetting off to a far-away supplier to get a look at how things work. Often we go on good faith, reputation and word-of-mouth. On the one hand, the success of the end-product will assess the shop's processes. On the other hand, you'll have to engage in the business of sending the prospective PCB supplier an actual job to get feedback in this manner. And there are companies such as Next Level PCB that specialize in auditing PCB suppliers. I'm considering using this company in the future.

AS: How about price…is it a deal-breaker?

KD: In a prototype mode, prices vary by hundreds of dollars based on materials, layer count, turn time and adders for impedance tolerancing, finishes and hole sizing. The price per part can swing widely by hundreds of dollars or more, but the overall cost per order is only a small fraction of what the total value of the production costs will be. In a time-to-market environment, an engineering team needs to validate a product yesterday, and complains little when pricing varies widely with regard to turn-around time. The only way quick-turn pricing can become a deal-breaker is if the PCB designer has an alternate source to quote against and can go to a qualified lower bidder. But in a production/

volume environment, the tables are turned and per unit PCB price differences of nickels and dimes can become a deal-breaker due to large volumes and overall product price constraints.

AS: How critical is DFM and design rules checking?

KD: Very important! But it takes a depth of understanding. Early on in the qualification process, when selecting a supplier, a discussion about manufacturing constraints and capabilities will come up. It has to! After all, in order to fulfill the function of a designer, a designer has to design! A sage old manufacturing engineer once told me, "Kelly, never design anything that can't be built." I thought, well, duh.

But with all the knowledge of CAD and CAM today, PCB suppliers are still being sent data that is beyond the realm of manufacturabilty. Suppliers often have to address holes that can't be plated because the board is too thick, lines that will etch away because the copper is too thick, and stack-ups that will not even give the supplier a chance of achieving the impedance because of an overall board thickness constraint. Anyone can sketch traces and parts onto a layout database nowadays. But successful manufacturing will only occur if the designer has considered the supplier's manufacturing constraints.

AS: Can certification tip the scales?

KD: Absolutely. Certification demonstrates a willingness to take on the challenges of learning and upgrading knowledge, processes, requirements and capabilities for a given profession—to be measured and confirmed worthy of performing standardized business practices by one's peers or industry organization. There are many certifications issued by organizations such as UL, IPC, ISO, ITAR, RoHS and many more. In some cases, certification is a requirement to legally supply PCBs to certain industries.

So yes, lacking certification in critical areas of expertise can certainly affect a decision to move forward with a business relationship. But industry certification is also important for PCB designers. Training and evaluation of designer core competencies has never been more important to companies searching for PCB suppliers and PCB designers who can successfully do business with them. IPC has done an unparalleled job of educating and certifying the hundreds of designers who have become Certified Interconnect Designers.

AS: Do you order test boards from the shop?

KD: We require tested boards from our suppliers. In addition, we require certifications for adherence to continuity and impedance specifications. Almost always, a solder sample board will be included FOC with the order. This gives our assembly folks a good heads-up about what they can expect with regards to setting up their solder deposition and heat profiling.

AS: You've visited a few fab shops over the years. What do you look for?

I'm pretty bad at metaphors and comparisons, but the older I get, the more my younger years as a Boy Scout come to mind. I'd have to say that I look for the same things in a fab shop that my leaders helped me to learn as a young scout.

Boy Scouts pledge to be "Trustworthy, loyal, helpful, friendly, courteous, kind, obedient, cheerful, thrifty, brave, clean and reverent." This is handy, because there are no IPC specs on this kind of stuff!

The Boy Scouts' slogan is "Do a good turn daily." Turn this design Monday, and turn that design Tuesday.

The Boy Scouts' motto is "Be prepared." Are you ready for this design? Get prepared with the right materials, machinery, bandwidth and technology! **PCBDESIGN**

Kelly Dack, CID+, is a senior PCB designer who has worked in the aerospace, medical, telecomm, and gaming industries. He currently enjoys working for a large Northern Nevada gaming company.

Thermal Design: Still a Process Pinch Point?

by Dr. John Parry, CEng
MENTOR GRAPHICS CORPORATION

SUMMARY: ***Traditional methods of using correlations and simple design rules to perform thermal design are becoming more difficult to apply. But new CFD technology is now bringing thermal design to the generalist PCB designer and design engineers.***

In simulation-driven thermal design, productivity is king. In the past, engineers have faced a difficult choice between design productivity and tool capability, especially when attempting to explore different cooling options and the design space associated with the chosen solution. However, the development of new computational fluid dynamics (CFD) technologies is making that choice easier by offering the best of both worlds, so that rapid simulations are possible on even the most complex of geometries (Figure 1). These new technologies are necessary to meet the challenge of increasing power and geometric density in electronic products, as well as the declining availability of thermal experts to work with these more complex designs.

Thermal Design Tougher as Power, Package Density Increases

CPU clock speeds have plateaued, limiting die-level power density to the order of 100 W/cm^2. Designing electronic products with die-level power densities above 100 W/cm^2 is very challenging and expensive, so it's actually packaging technology and cost limitations that are limiting CPU clock speeds. As a result, the trend has been to use multiple cores to process tasks in parallel and handle multiple tasks concurrently to deliver higher overall performance. This has resulted in power densities continuing

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THERMAL DESIGN: STILL A PROCESS PINCH POINT? *continues*

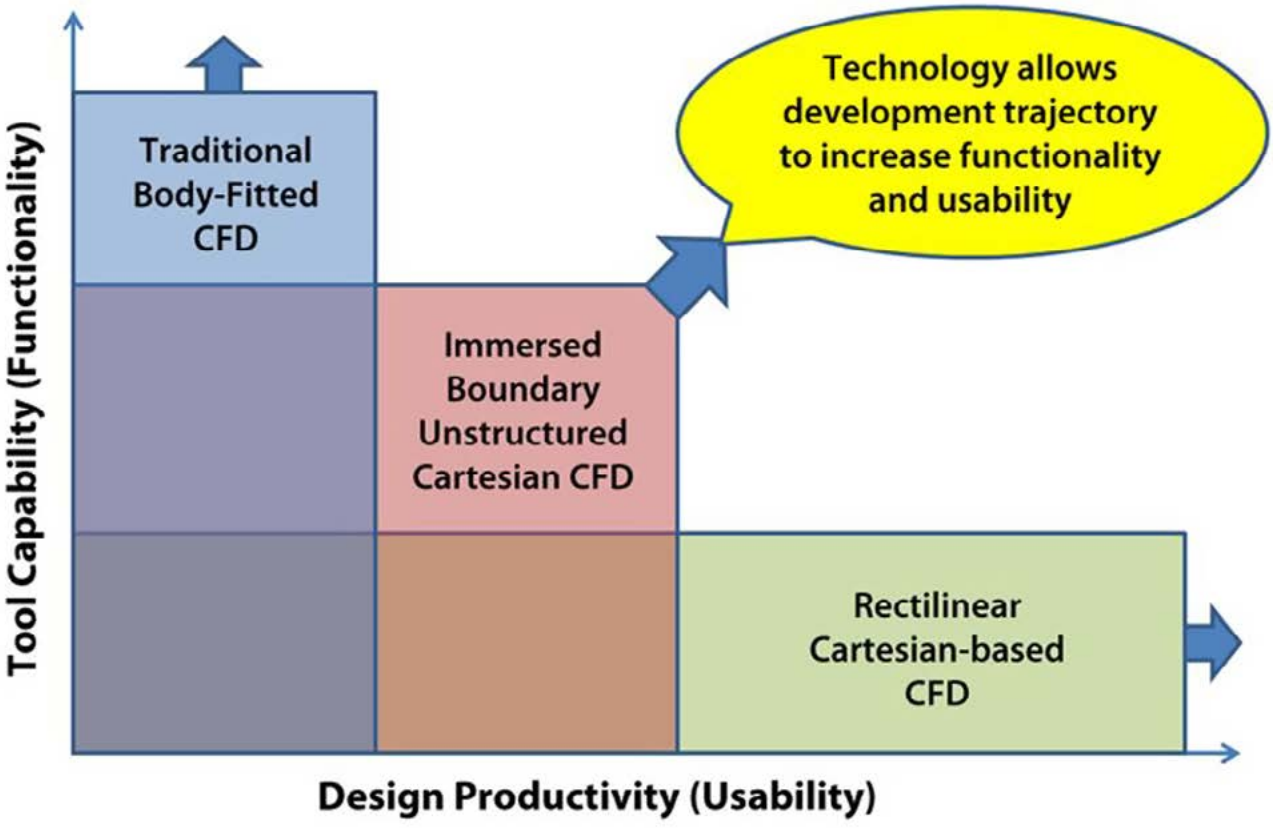

Figure 1: Development trajectories for different CFD technologies as a result of needing to address increasingly complex thermal designs.

to increase at the package, board, and system levels in many applications.

In some applications, such as mobile products, 3D IC packages are becoming more commonplace with the pressure to both shrink the height of IC packages and use stacked die. Although phone sizes have increased, which provides useful additional heat transfer area because ultimately the heat has to be either convected away to the air or conducted into the hand, that trend has more or less reached the limit of convenience in the latest touchscreen smartphones (Figure 2). More efficient materials to spread the heat provide more options, but they have an additional cost and weight penalty.

Traditional methods of using correlations and simple design rules to perform thermal design are becoming more difficult to apply. As packaging density increases, both correlations and design rules suffer the problem of being used outside their range of applicability. This is particularly the case for correlations, which are often generated in idealized conditions. Also, considerable expertise, and often some historical knowledge, is needed to know when and where to apply what correlation and/or what design rule.

Unfortunately, fewer people have experience with traditional thermal design. Many of the experts have retired or are near retirement, and too few people are following in their footsteps. This lack of knowledge and skills is exacerbated by companies distributing thermal design across the organization and moving away from having centers of thermal excellence. Thermal design is now just one task among many for generalist design engineers.

Highly Complex: Thermal Design for 3D Electronic Products

Another challenge is that correlations and design rules do not normally extend to non-

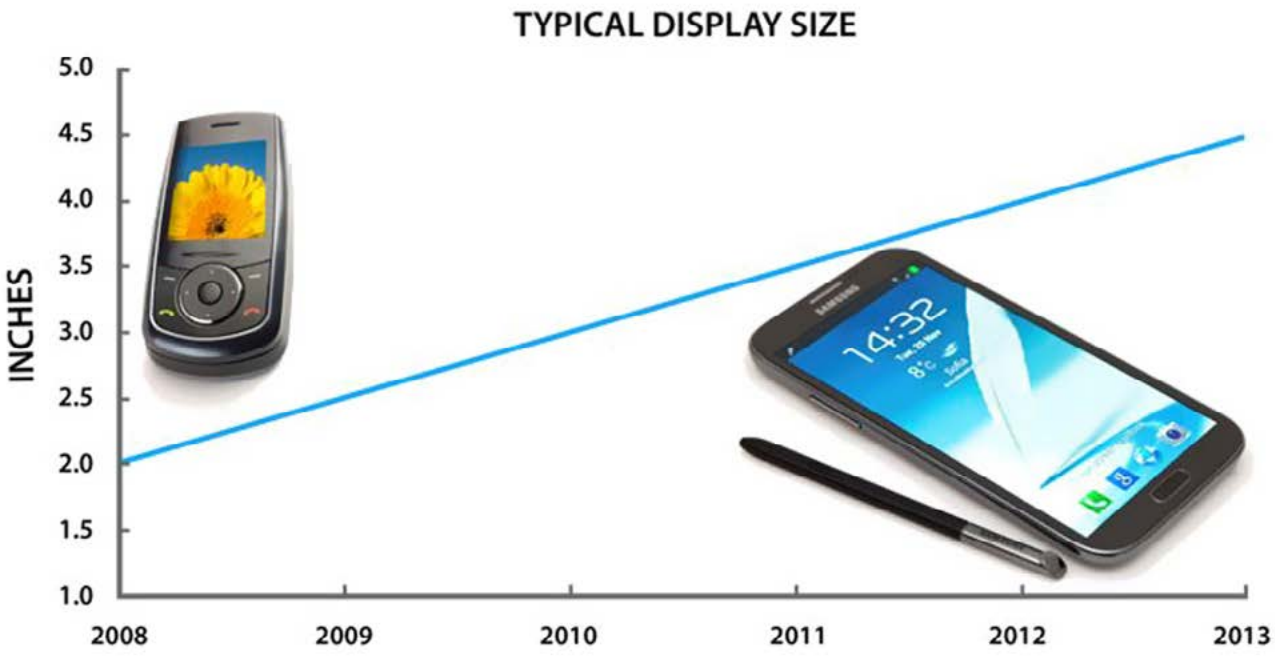

Figure 2: Mobile phone display size trend 2008-2013 (data from IHS Inc.).

steady behavior. For air-cooled electronics, getting the air flow right is critical. Local heat transfer rates can (and usually do) vary enormously, depending on whether the air is flowing fast or slowly over the surface, stagnating within a flow recirculation, or impinging. Fluid flow in an electronics enclosure is normally highly complex, with time-varying gradients and turbulent eddies influencing thermal performance.

Design for steady-state operation at maximum power can result in substantial overdesign because the ICs in the system will not maintain their maximum power for long periods of time, and the thermal mass of the system can absorb heat during power spikes, so heat does not need to be dissipated as fast as it's generated.

Problems Exist, Even With CFD

The technology of choice to address these issues is CFD, which accurately predicts air flow movement by solving the fundamental flow physics represented by the Navier-Stokes equations. These calculations allow the heat transfer rate between the solid and the air to be determined locally at every point in the system. CFD has made it possible to arrange for good air flow where hot components are located, to identify where adequate heatsinking is needed, and to select an appropriate heatsink.

Using CFD in early design is widely regarded as a best practice for optimal thermal design, minimizing product design and operating cost, as well as weight and power consumption associated with the cooling solution. The evolution of CFD-based thermal design software has made thermal design easier for both thermal experts and generalists alike.

Despite the use of CFD in early design, in many cases, physical prototyping is still used for design verification, and the goal of 100% virtual prototyping for thermal design has not yet been achieved. Some companies are still finding serious problems at this stage, risking the commercial viability of the product. Why is that?

Partly it's the uncertainty in the material property data and thicknesses of thin, but critical, features such as thermal interface materials and interfacial thermal resistances. Also, in late design, sometimes it's necessary to simplify the simulation model to keep it tractable, for example, to be able to create a mesh used for the simulation, to achieve a mesh quality that

does not adversely affect the simulation results, or because the simulation tool used doesn't support the range of complexity needed to fully capture the product geometry.

Until now, thermal designers had a choice:

- Use a tool that is particularly good for early design work and have to live with simplifications later on, or
- Use a tool that can cope with complex geometry and suffer the time and effort needed to clean up the CAD geometry and build an unstructured mesh around it, resulting in slow analysis turnaround times

Traditional Body-Fitted Tools: No Early Simulation

Where the geometry of the system is relatively rectilinear (such as for rack-based electronics), Cartesian-based CFD software has been favored because the technology is a good fit with the design (Figure 3). Such tools also tend to be the choice of thermal experts who are able to make simplifying assumptions with confidence, providing simulation results to support the rapid changes in concept design through to final product verification.

Where the geometry is curvilinear, and for non-experts, the tendency has been to choose simulation tools that use a "body-fitted" mesh, in which all the surfaces of the model are meshed and then a volume mesh is created that fills the solid and fluid regions, such that the 2D surface mesh lies on the boundary between cells in the 3D mesh. Such mesh technologies were first developed in the early 1980s, and despite enormous improvements in automation and control, the basic approach remains a manual and somewhat error-prone process, especially for highly-cluttered geometries often encountered in electronics. Poor mesh quality can negatively affect both simulation result accuracy and solution stability. In this case, more capability translates into less productivity.

Using body-fitted tools means that thermal simulation isn't performed early in the design process when the most insight is gained because it's impractical to turn around simulations fast enough. Instead, thermal simulation is relegated to late design verification when the geometry is changing more slowly, limiting the value. This method doesn't support the need to run many multiple cases concurrently as part of a design of experiment matrix. Exploration early in the process before the design "solidifies" because of other considerations such as timing, signal integrity, etc., ensures that a low-cost and reliable thermal solution can be found early enough to be designed into the product.

Data Often Unavailable for Accurate Thermal Design

Electronics thermal design is difficult also because the data needed for the simulation comes from a number of sources. Geometry comes from the main mechanical design automation (MDA) or MCAD design flow and from the electronic design automation (EDA) or

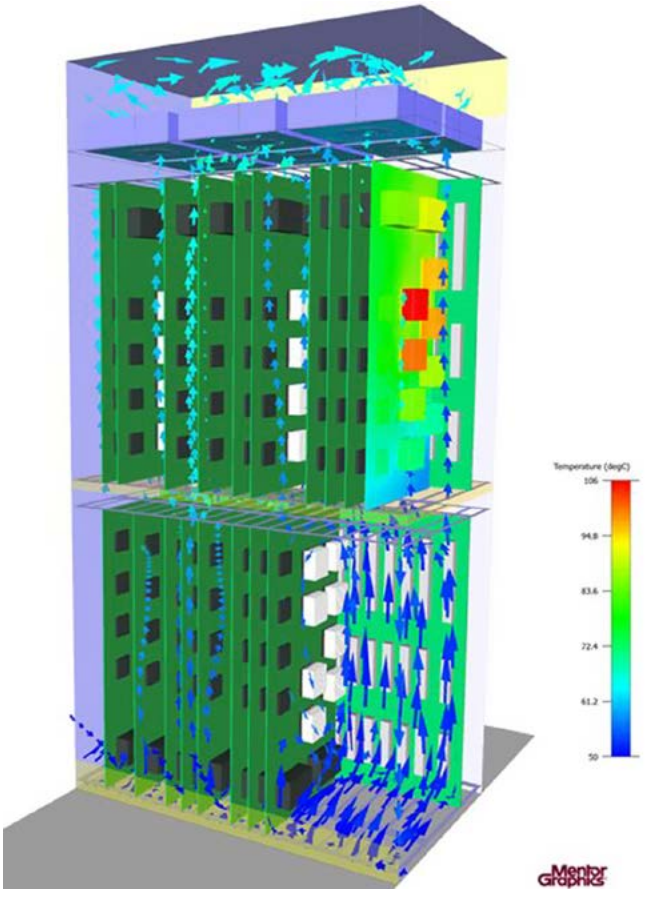

Figure 3: Detailed thermal study of a rack system using rectilinear Cartesian CFD.

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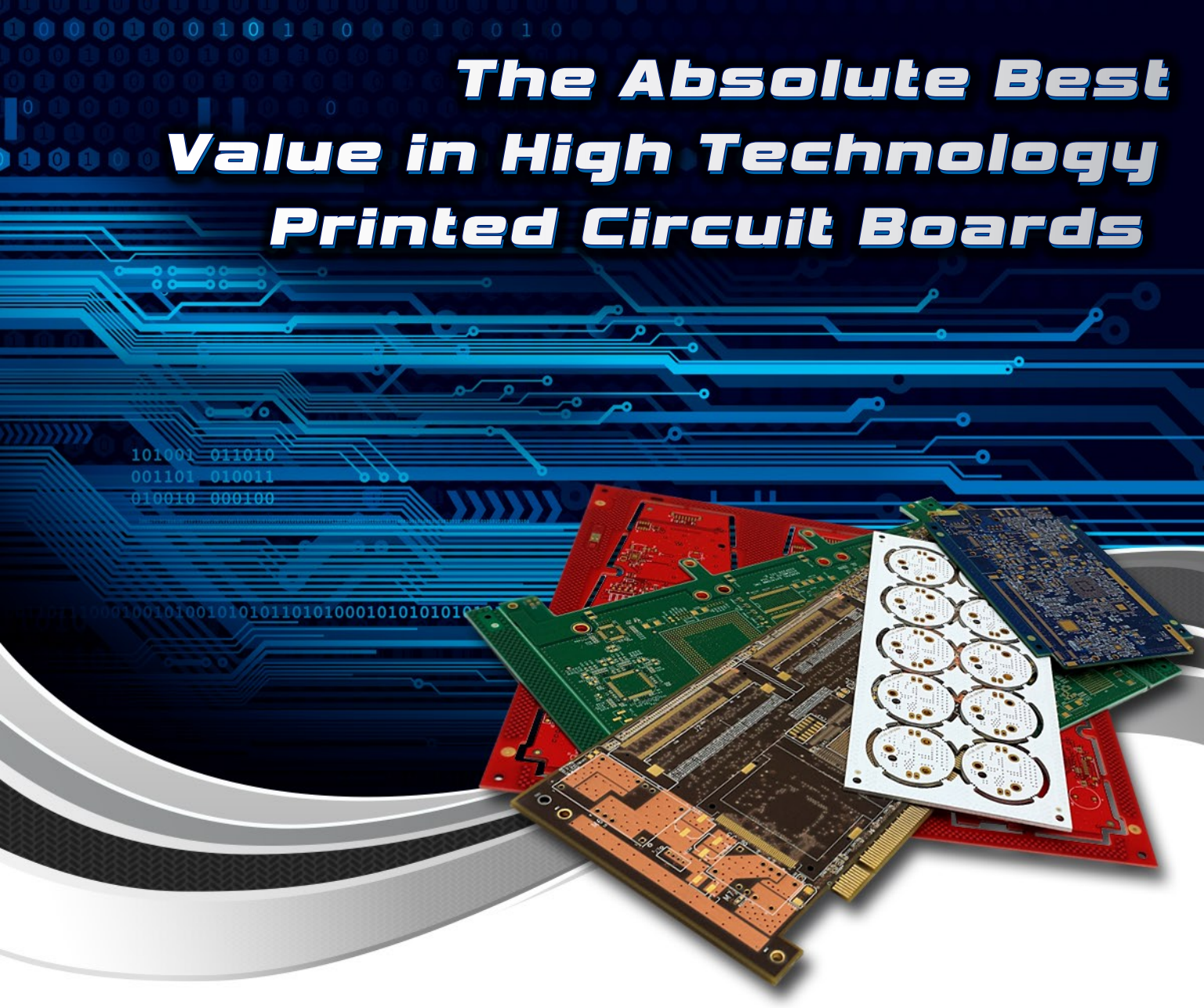

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ECAD design flow. However, this is not enough for thermal simulation.

Material thermal property data is absent from both of these sources, and estimates of the power that ICs will consume and dissipate as heat depends on the use case. In some cases, even that is insufficient because information about where these heat sources exist on the die surface, together with a detailed thermal model of the package, is needed before the thermal designer can be confident that the component vendor's specs for maximum allowable junction temperature can be met. Successfully integrating thermal design early into the product creation process requires engagement with the electronic and mechanical design teams and, in some cases, commercial-off-the-shelf (COTS) component vendors.

Immersed Boundary Treatments: Faster, More Accurate

The speed and complexity of the design of electronic products places requirements on CFD-based simulation software that are not nearly as pronounced in more traditional industries. The importance of electronics cooling is driving the use of novel CFD technologies, such as immersed boundary treatments for handling the friction and heat transfer between the fluid and solid surfaces (Figure 4).

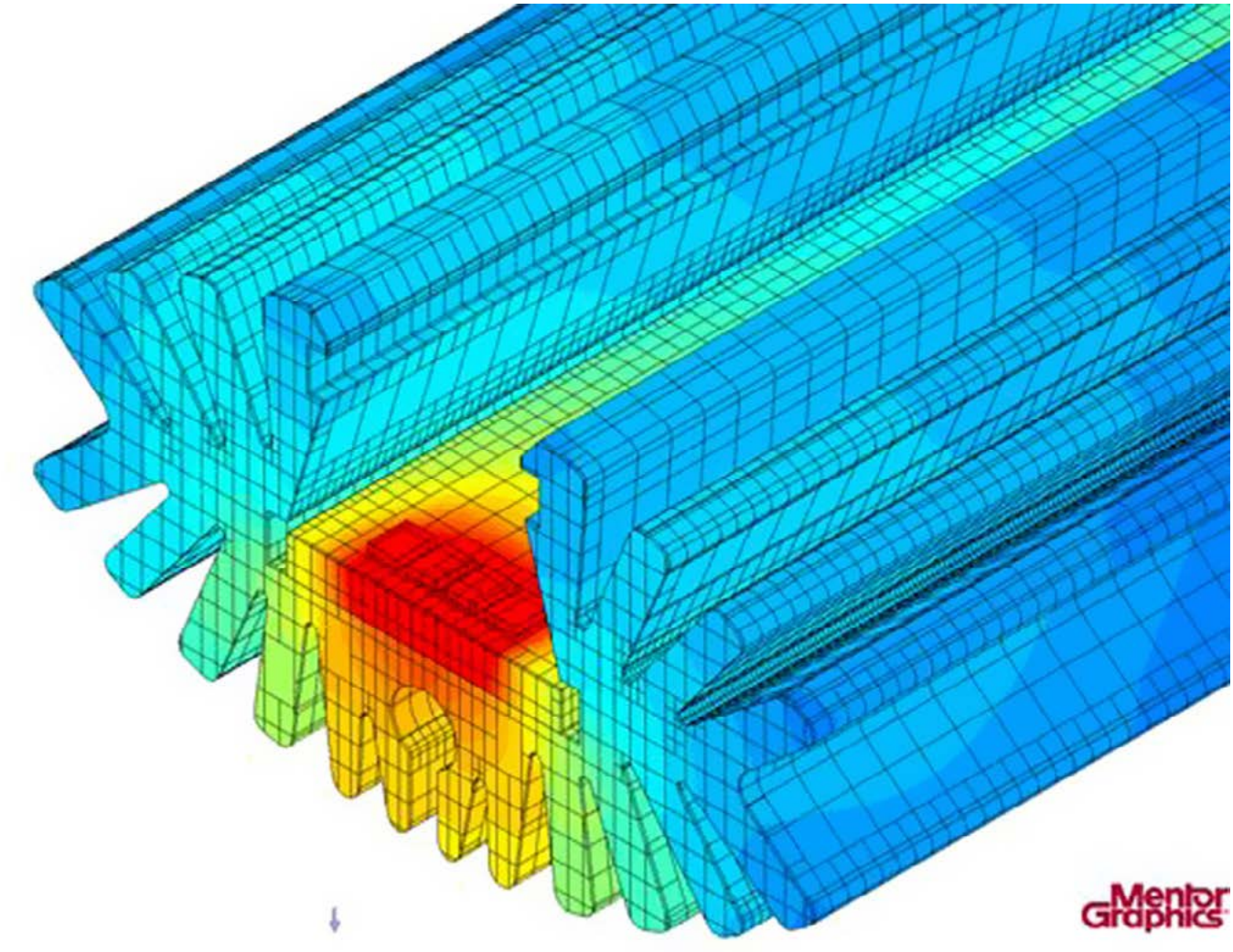

Figure 4: Thermal study of a complex heatsink assembly using immersed-boundary unstructured Cartesian CFD.

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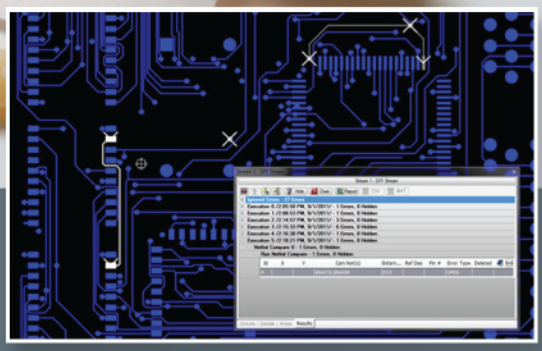
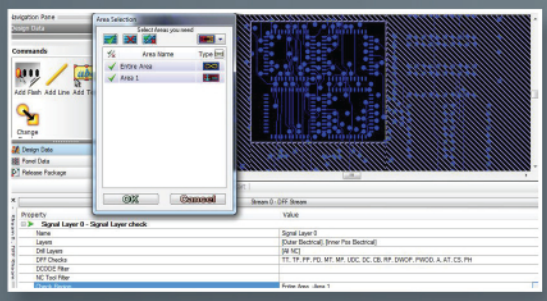


Netlist errors are quickly validated in DFMStream



Define DFM checks by area so components such as BGAs can be verified with unique rules different from rest of design

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THERMAL DESIGN: STILL A PROCESS PINCH POINT? *continues*

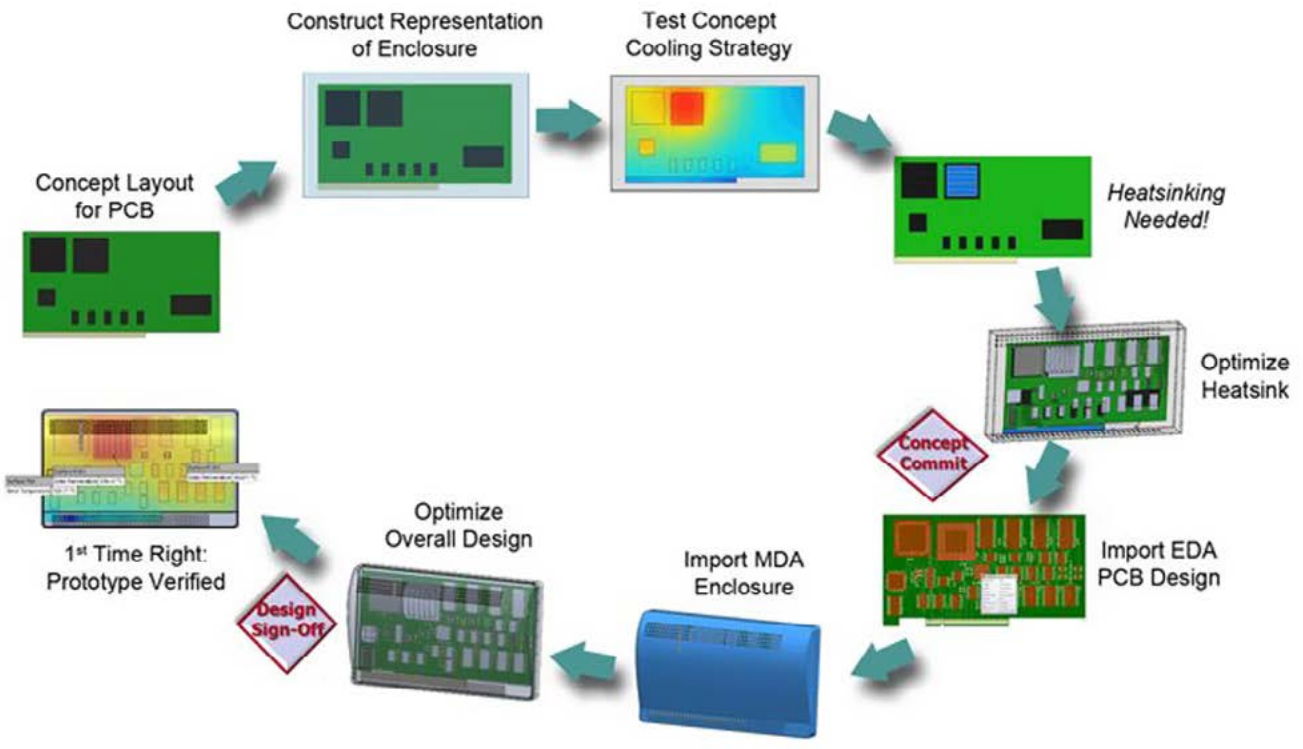

Figure 5: Concept to first prototype evolution in FloTHERM XT.

Immersed boundary treatments were first used for high-speed flows. They don't need a fine mesh near the surface to resolve flow boundary layers. They are particularly useful for complex geometries in which it's impossible to anticipate the flow structure because rerunning the simulation isn't necessary. This is usually the case when the boundary layer is resolved on the mesh if, or more likely when, the mesh is found to be insufficiently fine in some regions to adequately capture the flow behavior and provide meaningful results.

Immersed boundary treatments don't require a body-fitted mesh to capture the effect of the surface shape on the flow and heat transfer behavior, which is particularly important in applications that contain complex curvilinear shapes.

Thermal design is a highly collaborative activity, which, if done well and early, can help with geometry interference checks. One Cartesian-based CFD software tool is Mentor Graphics' FloTHERM XT 3D. This tool uses a well-validated immersed boundary treatment in conjunction with a Cartesian-based Octree mesh that is robust and doesn't require knowledge of the solution numerics, such as judging how much measures of aspect ratio, curvature, and divergence within the mesh will adversely affect result quality or time spent tweaking the mesh.

Even so, electronics systems generally contain so much detail that it's still inconvenient to capture everything on the computational mesh no matter how it's created. Systems can contain literally hundreds of components and thousands of individual nets, etc., and an individual heatsink can have hundreds of fins. One approach that's been shown to be effective is to use behavioral models that capture the integral effect of these features within each grid cell, without having to use multiple cells to resolve each feature. These "engineering models" are able to calculate the effect of the unresolved features on the flow and heat transfer within the rest of the system while also calculating temperatures, pressure drops, and flow rates associated with these sub-grid scale features.

Conclusion

Novel CFD-based simulation software development addresses the demanding thermal design requirements for today's electronic products. The importance of electronics cooling is driving the use of these CFD technologies because they enable engineers to explore different thermal designs of complex geometries earlier in the product development process. **PCBDESIGN**

Dr. John Parry, CEng, is the electronics industry manager for the Mechanical Analysis Division of Mentor Graphics. He currently represents the Mechanical Analysis Division in the JEDEC committee on thermal standards.

New Method Develops Inkjet-Based Circuits Rapidly and Cheaply

Researchers from Georgia Tech, the University of Tokyo and Microsoft Research have developed a novel method to rapidly and cheaply make electrical circuits by printing them with commodity inkjet printers and off-the-shelf materials. For about $300 in equipment costs, anyone can produce working electrical circuits in the 60 seconds it takes to print them.

These instant inkjet circuits allow the printing of arbitrary-shaped conductors onto rigid or flexible materials and could advance the prototyping skills of non-technical enthusiasts and novice hackers.

"We believe there is an opportunity to introduce a new approach to the rapid prototyping of fully custom-printed circuits," said Gregory Abowd, Regents' Professor in the School of Interactive Computing at Georgia Tech.

Recent advances in chemically bonding metal particles allowed the researchers to use silver nanoparticle ink to print the circuits and avoid thermal bonding, or sintering, a time-consuming and potentially damaging technique due to the heat. Printing the circuits on resin-coated paper, PET film and glossy photo paper worked best. Researchers also made a list of materials to avoid, such as canvas cloths and magnet sheets.

"Everything we introduced in our research is available in the market and makes it possible for people to try this at home," said Yoshihiro Kawahara, Associate Professor at the University of Tokyo and the primary investigator. "The method can be used to print circuit boards, sensors and antennas with little cost, and it opens up many new opportunities."

To show the capabilities of the new technique for capacitive touch sensing (the interaction prominent in smartphone interfaces) and the flexibility of the printed circuits, the researchers attached a capacitive ribbon with embedded inkjet-printed circuits into a drinking glass. The capacitive ribbon sensor formed to the contour of the glass and, when connected to a micro controller, was able to measure how much liquid was left in the glass.

Entanglement: The Holy Grail of High-Speed Design

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD | AUSTRALIA

While high-speed SERDES serial communications seems to currently be at the cutting edge of technology, maybe it will shortly become an antiquated low-speed solution—even speed-of-light fiber optics may become obsolete. This month, we'll look at how quantum physics is transforming our world and how it could affect PCB design.

Differential signaling evolved due to the fact that high-speed, synchronous, parallel busses were getting increasingly wider—consuming more real estate—and faster until signal integrity issues forced a fundamental change in strategy. Multi-gigabit design is now the norm with up to 10 Gbps SERDES devices commonly available in FPGAs. Beyond the theoretical 12 Gbps limit, optical interconnects become the only solution. But are they?

Using quantum entanglement, devices may be able to transfer data at >10,000 times the speed of light over large distances and also possibly across time itself. Entanglement is a property in quantum physics that seemed so unbelievable and so lacking in detail that, 66 years ago, Einstein called it "spooky action at a distance."

Einstein said, "The behaviors of materials down at the level of atoms are often strange, but entanglement borders on our concepts of sorcery." Unfortunately, the Theory of Relativity does not describe the properties of quantum particles, and there still is a huge piece of the puzzle missing. Ideally, the laws of physics should apply equally to all matter in the universe.

If two electrons spinning in opposite directions are entangled, when one changes direction, the other immediately changes, whether the electrons are side by side, across the room or at opposite ends of the universe. Other particles, such as photons, atoms and molecules, can also become entangled, but taking advantage of the property requires more than a pair or handful.

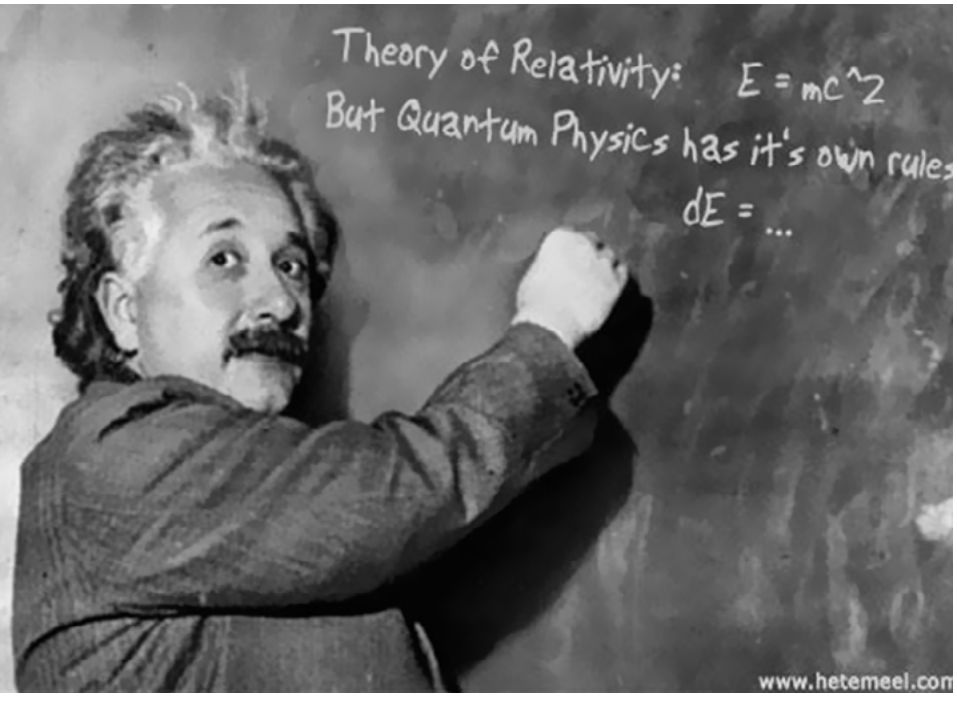

Figure 1: Albert Einstein and his Theory of Relativity.

Entanglement occurs when two particles are so intensely linked that they share the same existence. It arises naturally when two particles are created at the same point and instant in space. Entangled particles can become widely separated in space. But even so, the math implies that a measurement on one immediately influences the other, regardless of the distance between them.

Early this year, Chinese physicists have clocked the speed of

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ENTANGLEMENT: THE HOLY GRAIL OF HIGH-SPEED DESIGN *continues*

seemingly instantaneous interaction between entangled quantum particles at least four orders of magnitude faster than the speed of light or 3 trillion meters per second. We say "at least" because the physicists do not rule out that this interaction is actually instantaneous.

In a classical, binary computer, the bits—the 1s and 0s—have a definite state. They are either 1 or 0. But qubits—quantum bits—can be in both states at the same time. They are in a state called superposition. In quantum mechanics, a physical system has no definite state until it is observed. With the qubit, more information can be stored because the information is in both of its possible states, whereas in the classical binary memory system, only one state can be stored. Different operations performed on different parts of the superposition, at the same time, effectively make a massively powerful parallel processor.

One qubit encodes 0 and 1 simultaneously. Two qubits store all four permutations 00, 01, 10 and 11. Similarly, three qubits store eight states, four qubits 16 states, and so on. The power increase is exponential: n qubits have the processing capacity of 2^n classic bits. So a 512-qubit processor is extremely powerful.

Looking at entanglement at the chip level, information about a qubit could possibly be sent from an IC at point A to another IC at point B or vice-versa, as illustrated in Figure 2. No PCB traces are required as the entangled pair interact through space faster than the speed of light. The information at point A contains a 0 and 1 simultaneously. In quantum teleportation, a pair of quanta in an entangled state is sent to both a sender and a receiver. IC A and B then share the entangled pair. So the sender takes one of the particles of the entangled pair, and the receiver takes the other—this is the only thing that needs to be physically transferred. Or possibly chip-sets could be supplied in matched, entangled pairs.

The sender can run a quantum algorithm measuring his part of the entangled pair as well as the qubit he wants to transport. The receiver acquires the information, and an algorithm is run to manipulate its part of the entangled pair in the same way. In the process, B re-creates the unknown qubit that A sent over—without receiving the qubit itself.

In fact, you do not need to transmit quantum states at all to exploit their power, as quantum teleportation protocols prove; it is sufficient to possess entangled quantum states and communicate using classical bits. So, the limiting factor here is how fast the serial data can be streamed into, or out of, the entangled particle at each end. This part of the process will still require the routing of high-speed serial busses.

If harnessed, entanglement could yield super high-speed communications, hack-proof encryptions and quantum computers so fast and powerful they would make today's supercomputers look like simple adding machines by comparison. Or imagine "quantum cash" chan-

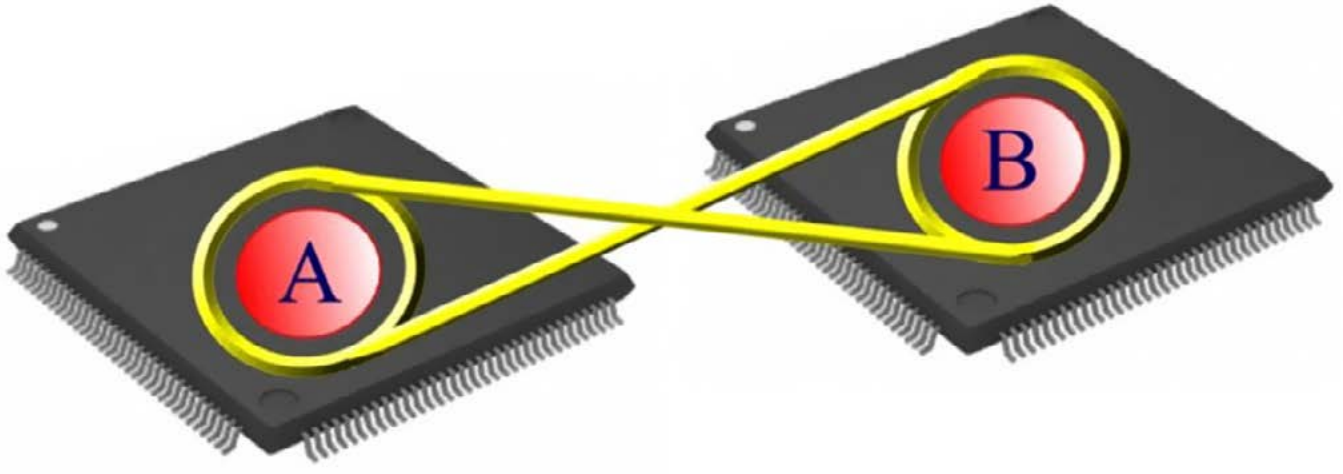

Figure 2: Data transfer via an entangled pair—no PCB traces required.

Figure 3: The first quantum network (courtesy www.extremetech.com).

neled through a financial system encrypted at the quantum level. The CIA is already using entanglement to securely encrypt communications. Entanglement may also provide a means for teleportation, as seen on Star Trek. This may all seem a bit far-fetched but let's look at practical implementations of entanglement.

In September 2012, a team of international researchers successfully teleported a quantum bit (qubit) over a record distance of 143 kilometers (89 miles), between the Canary Islands of La Palma and Tenerife. This distance is significant, as it is roughly the same distance to low Earth orbit (LEO) satellites—meaning it is now theoretically possible to build a satellite-based quantum communication network. Scientists entangled two photons in La Palma, and used a high-powered laser to fire one of the photons across the sea to a receiving station in Tenerife. Then, when the quantum state of one photon was altered, the quantum state of the second photon—despite being 89 miles away—was immediately altered, faster than the speed of light—without any measureable delay.

In the long term, a quantum network could form the backbone of an internet populated by quantum computers. In theory, each quantum processor/computer connected to the quantum network could be instantly linked to every other computer via an entangled pair of photons.

To set up another teleportation experiment, scientists from the Swiss Federal Institute of Technology (ETH), put three micron-size circuits on a chip measuring 300 mils (7.5 mm) square. Two of the circuits were the transmitters, while the other served as the receiver. The scientists cooled the chip to near absolute zero—at that temperature, the electrons in the circuits, which are the qubits, started behaving according to quantum mechanical rules (in this case, becoming entangled).

The team encoded information in the form of spin states, into the sending circuits' qubits, and measured them. At the same time,

they measured the state of the qubits in the receiver. The sending and receiving qubits' states were correlated; the information had been teleported. Since the qubit did not go through the printed circuit board or even intervening space, one could infer that this is a way to communicate faster than light.

Researcher Dr. Arkady Fedorov of the University of Queensland, Australia's ARC Centre of Excellence for Engineered Quantum Systems, says the team has reined in the behavior of information on a quantum level.

"For the first time, the stunning process of quantum teleportation has now been used in a circuit to relay information from one corner of the sample [IC] to the other...this is a process by which quantum information can be transmitted from one place to another without sending a physical carrier of information," said Fedorov. "This quantum information allows us to do teleportation with impressive speed and accuracy above what has been achievable to date."

Figure 4 illustrates the test circuit which features the isolated quantum transmitter and receiver built into the same IC.

We may not have to wait too long for this new technology, as the first quantum computer has already been shipped: D-Wave Systems is a quantum computing company based in Burnaby, British Columbia. In May 2011, D-Wave Systems announced D-Wave One, labeled "the world's first commercially available quantum computer," operating on a 128-qubit chip-set using quantum annealing to solve optimization problems. In May 2013 it was announced that collaboration between NASA, Google and the Universities Space Research Association (USRA) launched a Quantum Artificial Intelligence Lab using a 512-qubit D-Wave Two that would be used for research into machine learning, among other fields of study.

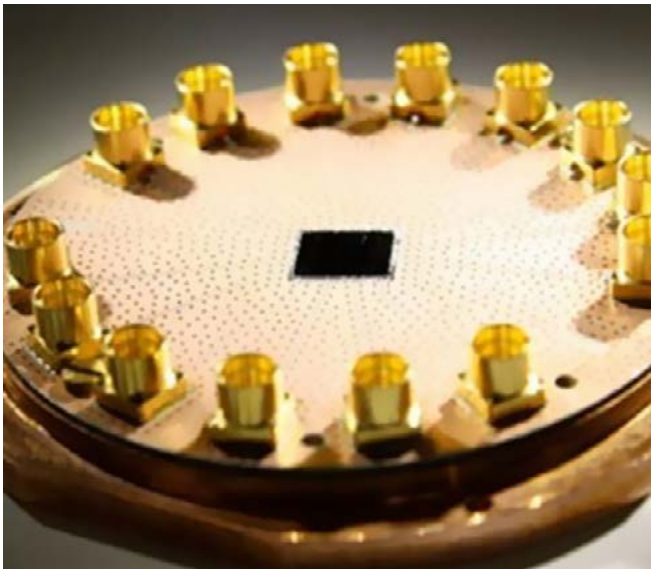

Figure 4: Test circuit for quantum teleportation (courtesy University of Queensland, Australia).

One of the major drawbacks of quantum computing is that the entangled particles must be kept at near absolute zero degrees Kelvin—the temperature of outer space vacuum—for the quantum effects to work. This may limit the mass market appeal. Also, they are highly energy intensive and obviously expensive to purchase and run. However, earlier this year, a group of Harvard scientists employed a custom-crafted industrial diamond to create quantum bits that were able to store information for nearly two seconds, and, incredibly, do it at room temperature. Two seconds may not sound like much, but when you are running at infinite speed and infinite bandwidth a lot of information could be transferred in a short time span.

Entanglement is not anywhere near the stage to "Beam me up, Scotty," but it is mind-blowing technology that shows huge potential. This technology may eliminate PCB routing altogether with the exception of the ICs and power and ground and peripheral circuitry. Maybe we will just put all the chips in a box, rattling around together, and they will just talk to each other instantaneously!

Points to Remember

- Entanglement occurs when two particles are so intensely linked that they share the same existence
- Particles, such as electrons, photons, atoms and molecules, can become entangled
- Entangled devices may be able to transfer data at >10,000 times the speed of light over large distances and also possibly across time itself
- More information can be stored with a qubit, than a classical bit, because the information

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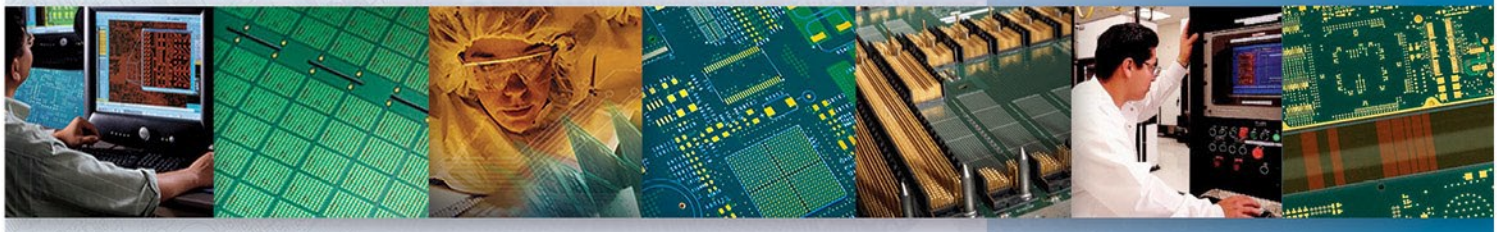

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is in both of its possible states

- The receiver end of an entangled pair can recreate an unknown qubit without receiving the qubit itself
- It is sufficient to possess entangled quantum states and communicate using classical bits
- Researchers have successfully teleported a qubit over a record distance of 143 kilometers instantaneously
- One of the major drawbacks of quantum computing is that the entangled particles must be kept at near absolute zero degrees Kelvin. However, a custom-crafted industrial diamond has been used to create qubits that were able to store information for nearly two seconds at room temperature
- The first quantum computer, a 512 qubit D-Wave Two, has already been shipped **PCBDESIGN**

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Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. ICD is a PCB design service bureau and specializing in board-level simulation. The company developed the ICD Stackup Planner and the ICD PDN Planner software. To read past columns or contact Olney, click here.

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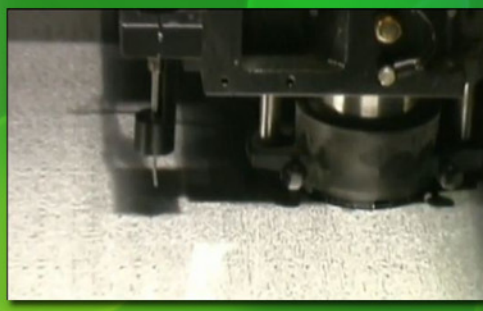

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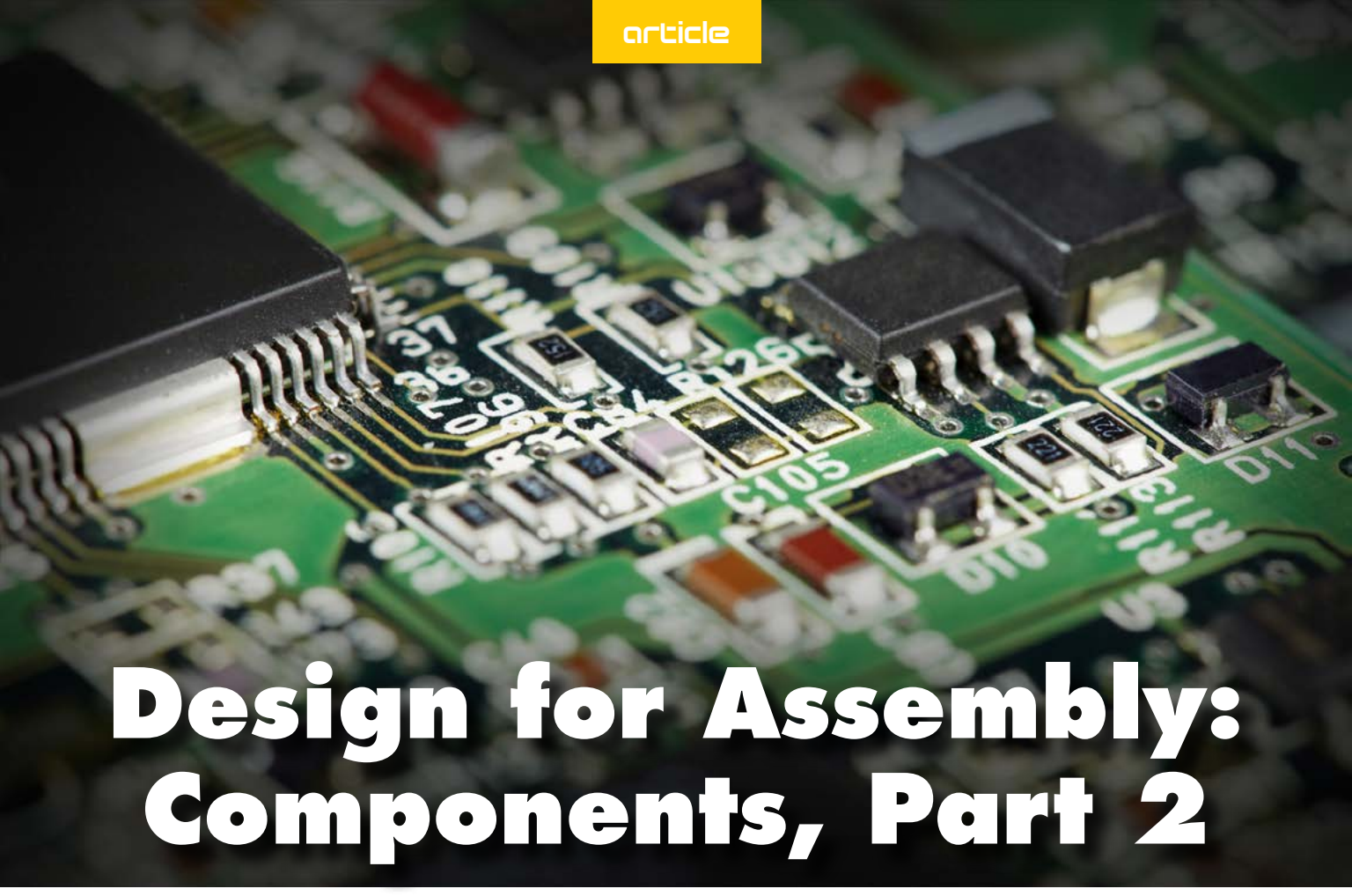

Design for Assembly: Components, Part 2

by Tom Hausherr
PCB LIBRARIES

SUMMARY: Every PCB layout must go through the component assembly process, and a PCB designer can do several things to make the assembly process easier. Click here to read Part 1 of this series.

Surface Mount Solder Joints

These seven factors are used to calculate the optimum land size per IPC-7351:

1. Component body tolerance
2. Component terminal tolerance
3. Fabrication tolerance: ± 2 mil (0.05 mm)
4. Placement tolerance: ± 1 mil (0.025 mm)
5. Land size round-off
6. Land spacing round-off
7. Solder joint goals for toe, heel and side (Figure 16)

The heel fillet in a gull-wing lead component is very important. Many reliability studies establish that 60–80% of gull-wing solder

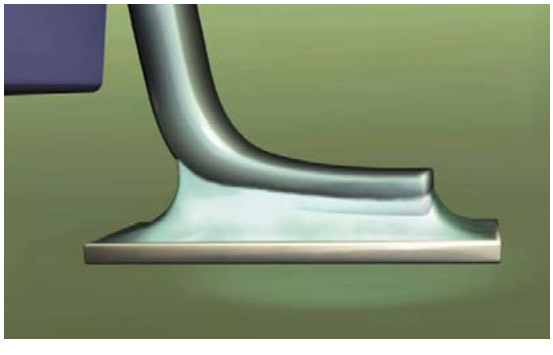

Figure 16: Image of toe, heel and side.

Gull Wing Lead Pitch > 0.625	Least Level	Nominal CLevel B	Most Level A
Toe	0.15	0.35	0.55
Heel	0.25	0.35	0.45
Side	0.01	0.03	0.05
Round-off Factor	Round-off to the Nearest 0.01 or 0.05		
Courtyard Excess	0.10	0.25	0.50

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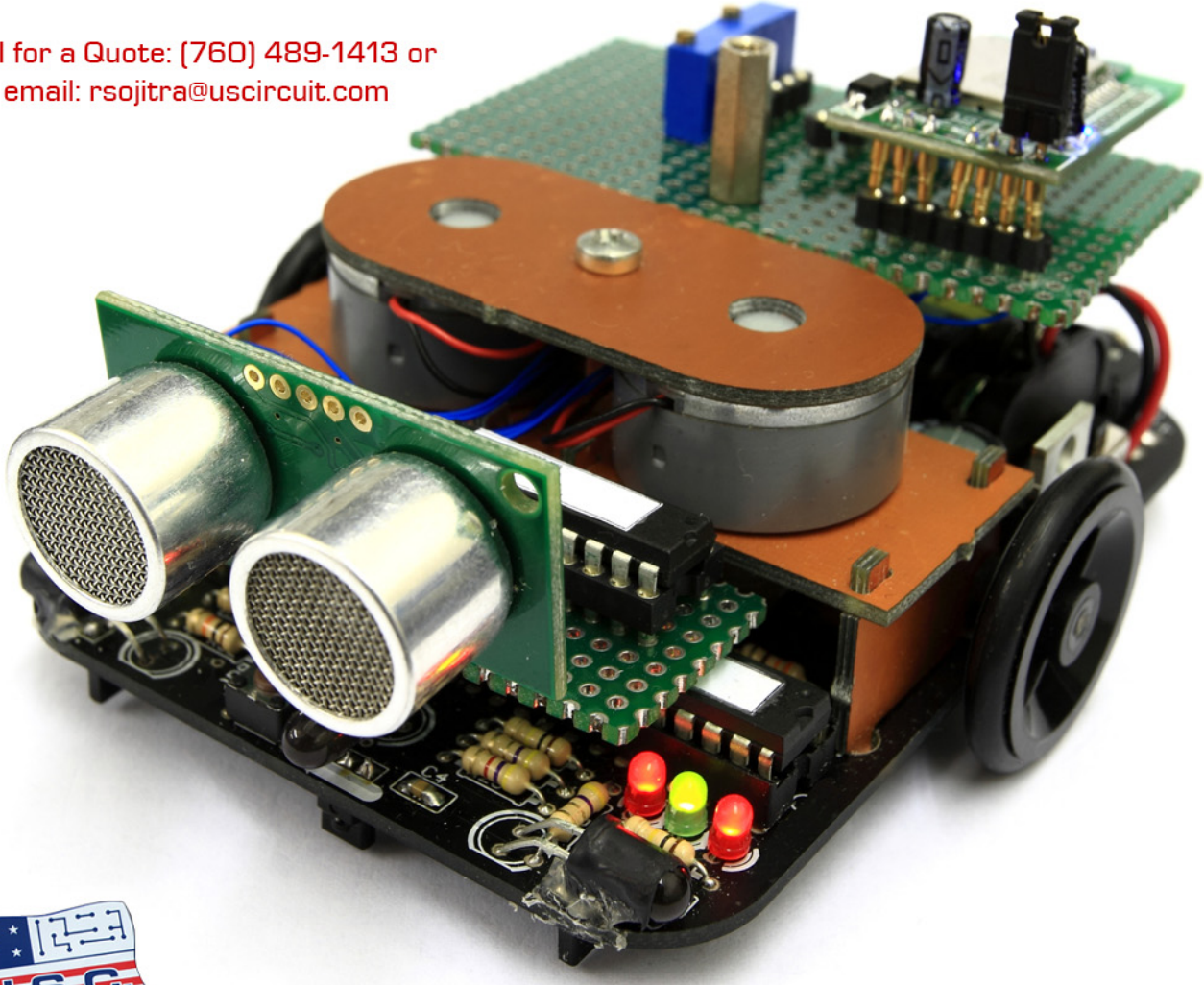

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strength is in the heel. Land position or length that precludes forming the minimum heel fillet is a failure mechanism.

Plated Through-hole (PTH) Hole and Pad Size Calculations

Before you calculate the pad size, you must first calculate the hole size per Figure 17.

Once you figure out the hole size, the annular ring can be calculated by adding a minimum annular ring value of 2 mils (0.05 mm) plus a minimum fabrication allowance of 16 mil (0.4 mm) to the hole-size. The nominal fabrication allowance is 20 mils (0.5 mm) and the maximum fabrication allowance is 24 mils (0.6 mm).

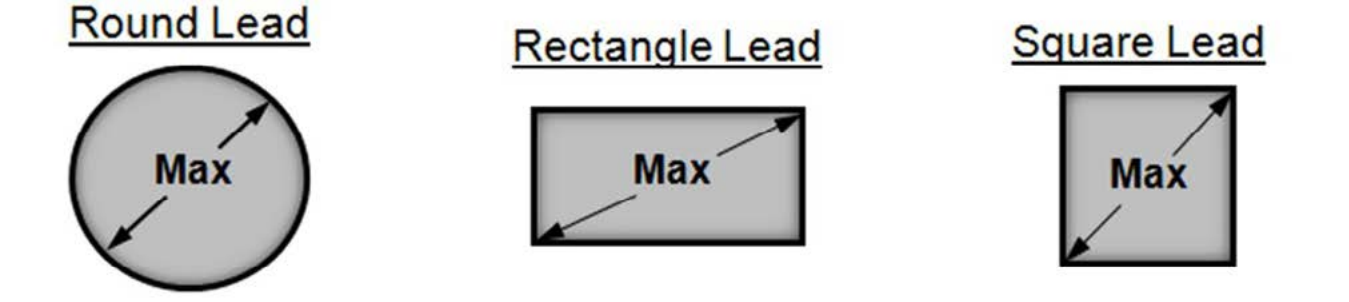
You can also use the PCB Libraries Proportional Padstack Chart to auto-generate a good known annular ring. The proportional padstack starts out using the least annular ring for small holes and nominal annular ring for average hole sizes and most annular ring for large hole sizes. To download the Proportional Padstack Chart and many other important library construction documents, click here.

Manufacturer Recommended Footprint Patterns

IPC-7351B features standard mathematical formulas for calculating standard component families. More than 50% of all component packages in the electronics industry today are non-standard packages. These non-standard packages require the component manufacturer to provide a recommended footprint pattern. Typically, the component manufacturer will create test patterns and run them through the assembly process to select the pattern with the best solder joints.

Minimum Pad to Pad Clearance

The minimum pad-to-pad clearance is defined by the assembly shop. Before you create your PCB library parts, discuss this issue with your assembly shop engineer. The IPC-7351 calculator default minimum pad-to-pad clearance is set to 6 mils (0.15 mm), but some assembly shops require 8 mils (0.2 mm) of pad-to-pad clearance to optimize their assembly process and reduce scrap and increase yield.



IPC-2222A Table 9-5 Hole Diameter to Lead Diameter Relationships		
Maximum Lead + Environment Level = Minimum Hole		
Level A	Level B	Level C
10 Mil (0.25 mm)	8 Mil (0.20 mm)	6 Mil (0.15 mm)

Figure 17: IPC specs for calculating hole sizes.

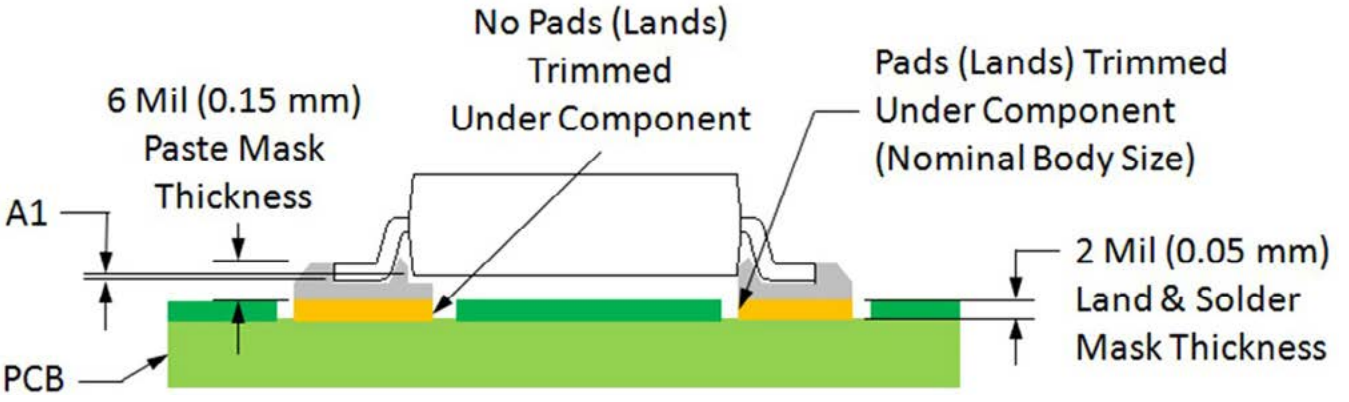


Figure 18: IPC argues that PCB designers should not trim the pads under low-profile components.

Pad Trimming Under Components

Pad trimming is used exclusively for gull wing component leads for low-profile component packages that have no space under the component (between the PCB and the component bottom). However, IPC says that regardless of the component stand-off value, a PCB designer should not trim the pads under low-profile components. (Figure 18).

Zero Component Orientation

Zero component orientation indicates the location of pin 1 and the rotation the PCB library was built to. This is important for automating the pick-and-place assembly line. When an assembly shop starts a project, they have to ensure the rotation of every part on the PCB layout to insure that every component is attached with the correct rotation. This currently is a manual time consuming process. IPC-7351C will introduce two acceptable rotations, as shown in Figure 19a. Figure 19b illustrates IPC-7351C Level B zero component orientation rotated counterclockwise by 90°.

Level A is pin 1 in the upper left corner and Level B is pin 1 in the lower left corner. If a PCB designer creates the entire PCB library with a known rotation, he can indicate this in the assembly drawing to provide the assembly shop with a known starting point. When all PCB designers organize their entire PCB library using either Level A or Level B (not both), then the

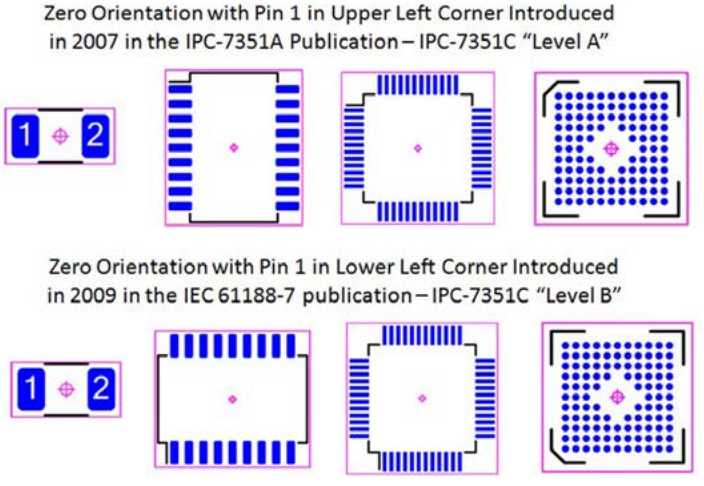


Figure 19a: Acceptable IPC zero component orientation.

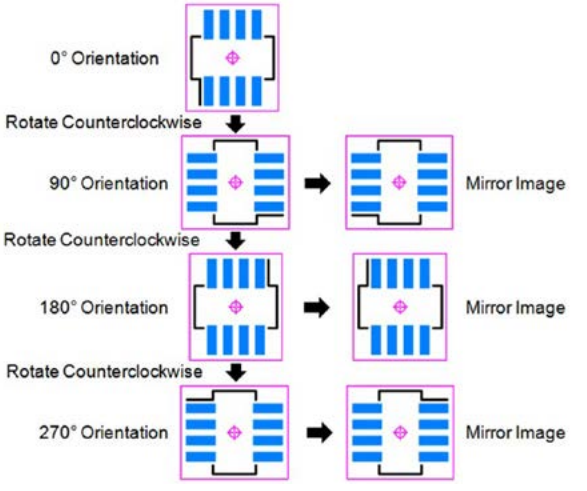


Figure 19b: IPC-7351C Level B zero component orientation.

assembly shop can start the process of automation. However, the assembly shops will continue to verify zero component orientations until they have consistency in the X/Y pick-and-place data.

X / Y Coordinate File

The PCB designer usually creates a pick-and-place file in Excel format. The spreadsheet contains the reference designator of every component in the PCB layout and its associated X and Y location from the PCB origin and the rotation of each component per the zero component orientation of the PCB library part. If the PCB designer does not provide an X/Y coordinate file, the assembly shop will take hours to calculate the center of each component to program the pick-and-place assembly line.

Thermal Pad Paste Mask Reduction

These component families have thermal tabs: QFN, PQFN, SON, PSON, SOP and QFP. The paste mask stencil must be reduced by a value between 40–65% and evenly dispersed in a checker board pattern so when the PCB goes through the reflow oven, the thermal pad paste mask spreads out evenly. Figure 20 is an example of a QFN with a thermal pad and its associated paste mask stencil reduced by 50%.

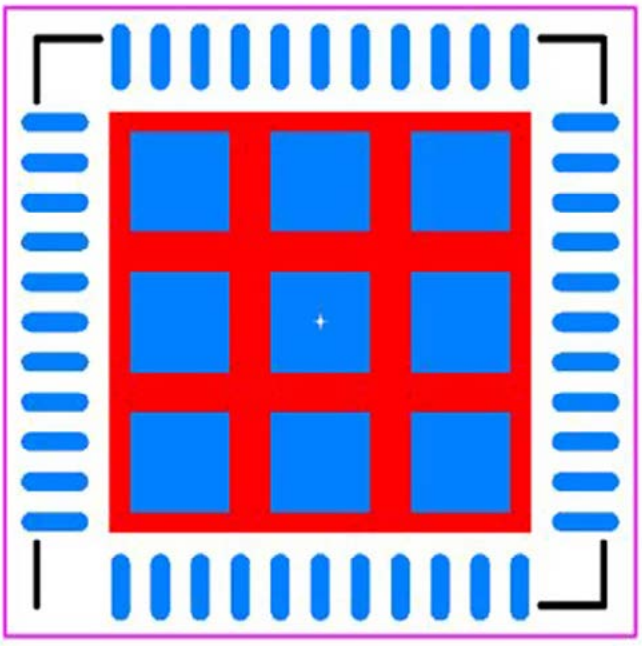


Figure 20: A QFN with a thermal pad.

Rounded Rectangle Pad Shape

Surface mount pad shapes have been at the center of controversy since the 1980s. IPC has always recommended either a full radius or corner radius pad shape while the component manufacturers recommend a rectangular pad shape. The goal is to aid the assembly process to make it more efficient. The number one issue with the industry not adopting the rounded rectangle pad shape is that many CAD tools did not support it until recently. In my opinion, the rounded rectangle pad shape should be used for every surface mount component package. It is the universal pad shape that improves fabrication and assembly and meets IPC standards. The only goal now is to get the component manufacturers to adopt it in their datasheet drawings. See Figure 21 for the optimal sizing.

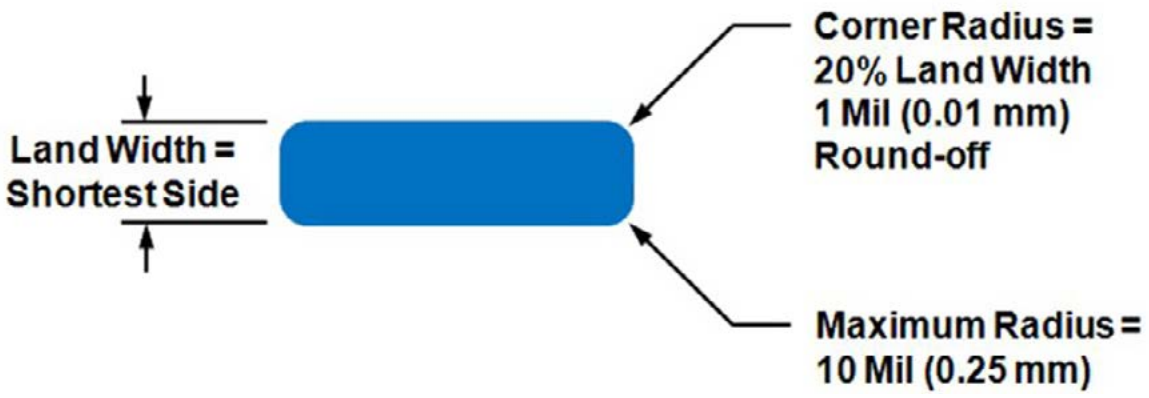


Figure 21: The optimal sizing of the rounded rectangle pad shape.

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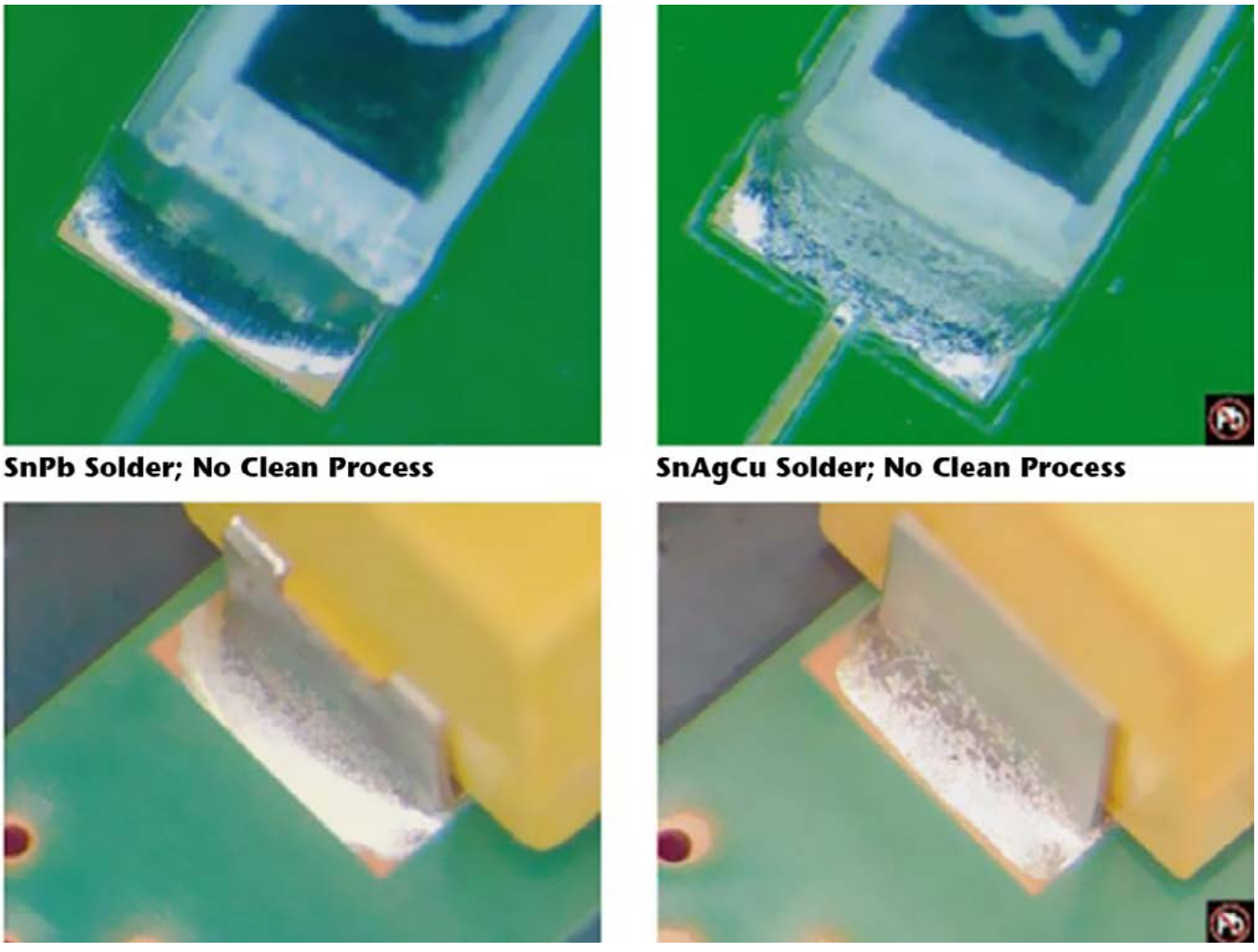

Figure 22: Assembled board with solder pulled away from corners.

If you look at an assembled PCB you will notice that most of the solder pulls away from the corners of the pad. (Figure 22). The rounded rectangle pad shape also opens up additional routing channels for dense layouts.

Via-in-pad Technology

Via-in-pad technology is just starting to take off because of new component packages like land grid array (LGA) where there is no room for a typical dog bone via fanout (Figure 23).

Also, fine pitch BGAs need to use the via-in-pad technique and sometimes not locating the via in the center of the pad is necessary to open routing channels on inner layers. Figure 24 shows an example of a routing solution for a 0.6 mm pitch BGA.

The main assembly problem with using via-in-pad technology is the fabrication process must insure that the via is plated, plugged, capped and surface finish with a flat surface. The flat surface is the most important issue. If there is a slight dimple in the pad, the paste mask will trap air that will get superheated in the reflow oven and blow a hole into the component lead and create a void. See Figure 25 for an example of a BGA void.

Non-Solder Mask Defined Pads

Either the PCB designer or the fabrication shop must swell the solder mask to prevent solder mask from encroaching on the solder pad. Depending on the solder mask fabrication process, there is a manufacturing tolerance. If you

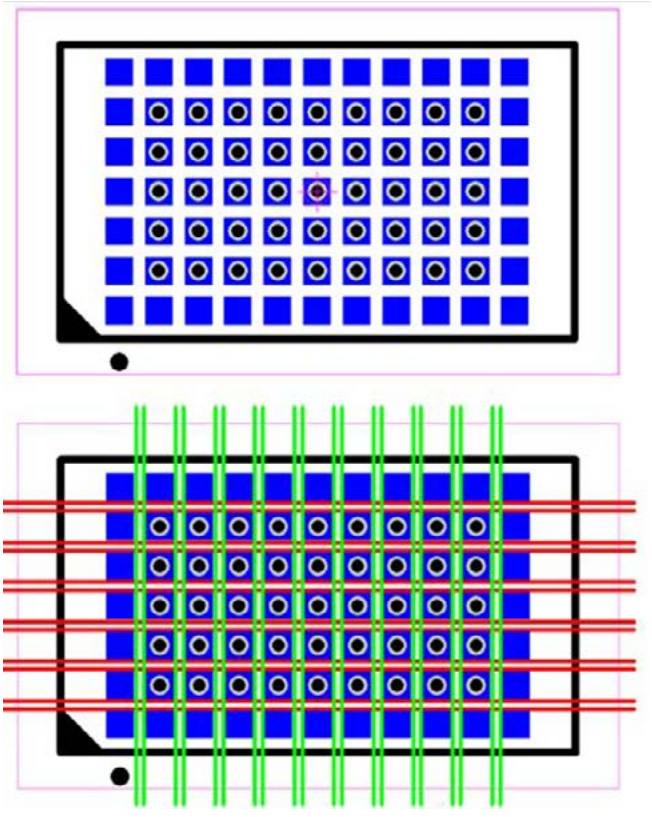

Figure 23: Via-in-pad technology is useful where there is no room for a dog bone via fanout.

are using multiple fabrication facilities, it is best not to swell the solder mask in the PCB library or in the Gerber data that you provide to fabrication. Let the fabrication shop swell the solder mask to a value that is compatible with their solder mask registration tolerances to insure that no solder mask will end up on an exposed pad. Most BGAs have collapsing balls that must collapse around the edge of the pad. If the solder mask is not swelled, the BGA ball cannot collapse around the pad edge and this will compromise the BGA solder joint connection. In Figure 26, the image on the left is a non-solder mask swell with no ball collapse around the pad. The image on the right has a solder mask swell and the BGA ball collapsed around the pad.

Note: J-STD-001E and IPC-A-610E have looser criteria for solder mask than bare board fabrication. Solder mask has a purpose during assembly—keep solder from wetting in specific areas. But during the assembly process high-temp cycles and mechanical actions may de-

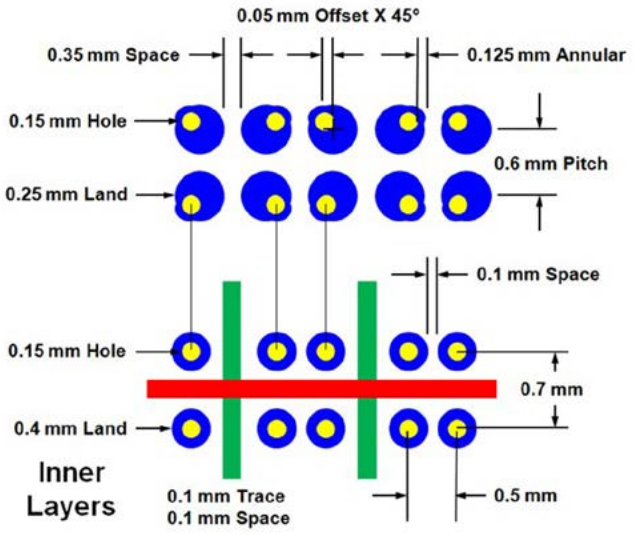

Figure 24: A typical routing solution for a 0.6 mm pitch BGA.

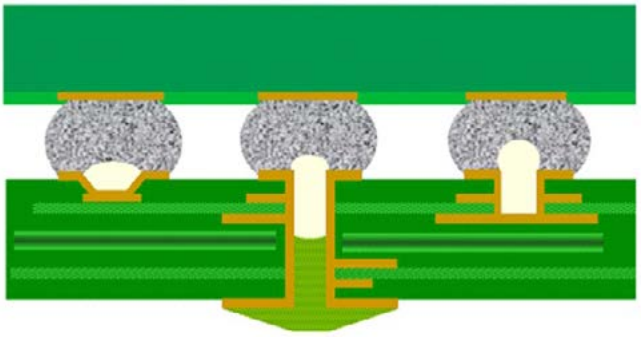

Figure 25: A BGA void.

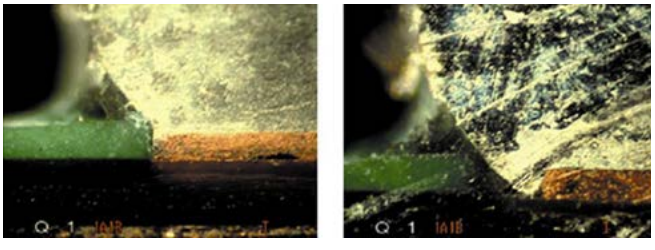

Figure 26: Non-solder mask swell (left) and solder mask swell (right).

grade the mask material. At that point it probably doesn't matter. However, it would become an issue if the solder mask darkened so much that silkscreen markings required to be discernible were not.

DESIGN FOR ASSEMBLY: COMPONENTS, PART 2 *continues*

Solder Mask-Defined Pads

I only know of two applications that employ solder mask-defined pads; one is flex circuits. When designing library parts for flexible circuits, it is best to solder mask-define the toe and the heel to assist in holding the pad down to the PCB during flexing.

The other application involves using solder mask-defined BGA pads in handheld devices. The BGA pin pitch in an average cell phone is 0.4 mm or less, and the ball and pad sizes are very small. During drop testing, it has been proven that the BGA solder joint holds up bet-

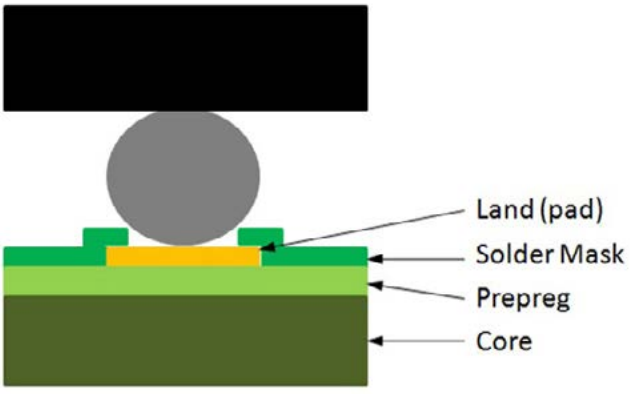

Figure 27: Solder mask-defined pads.

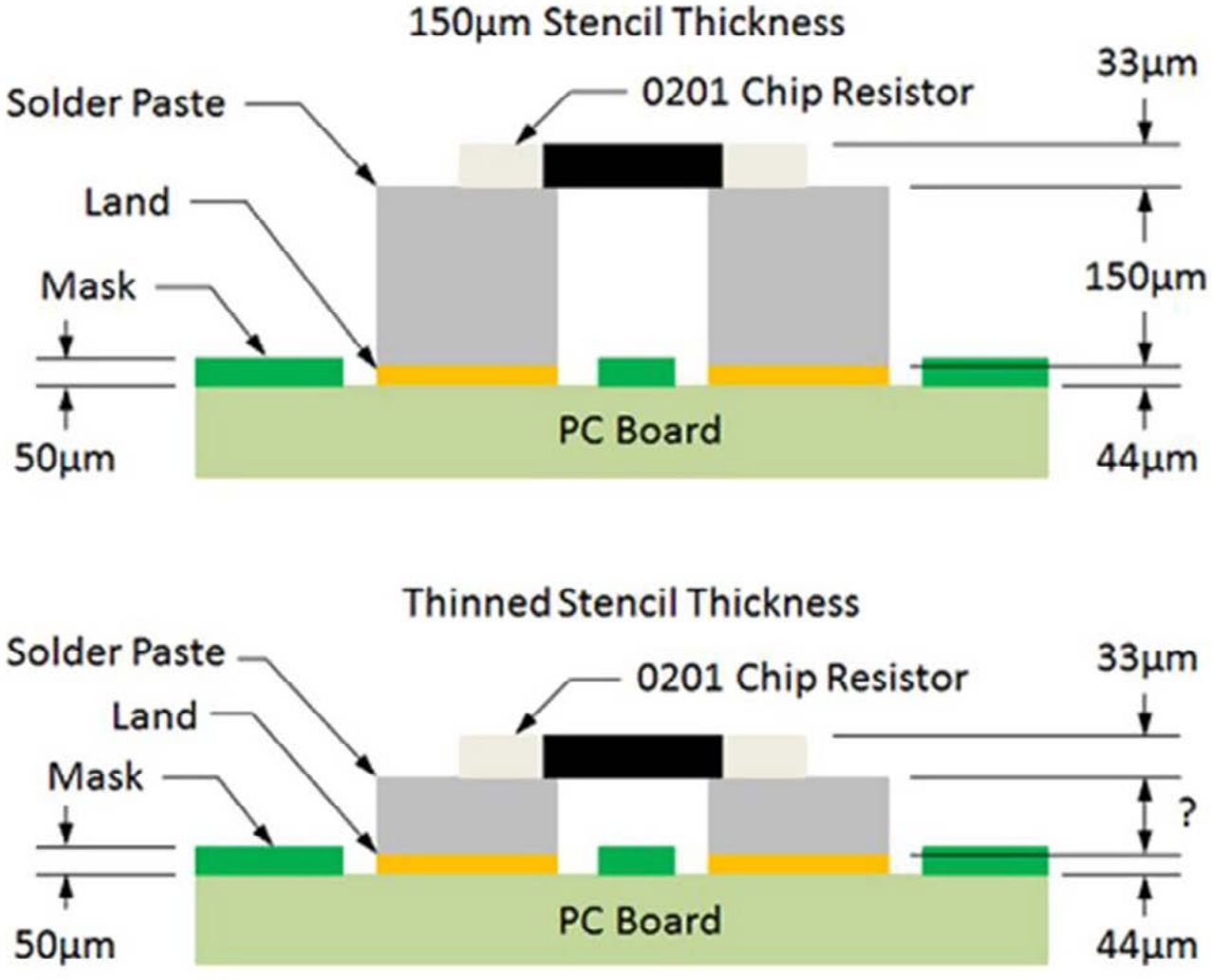

Figure 28: Graphic showing too much solder being used for 0201 chip resistor.

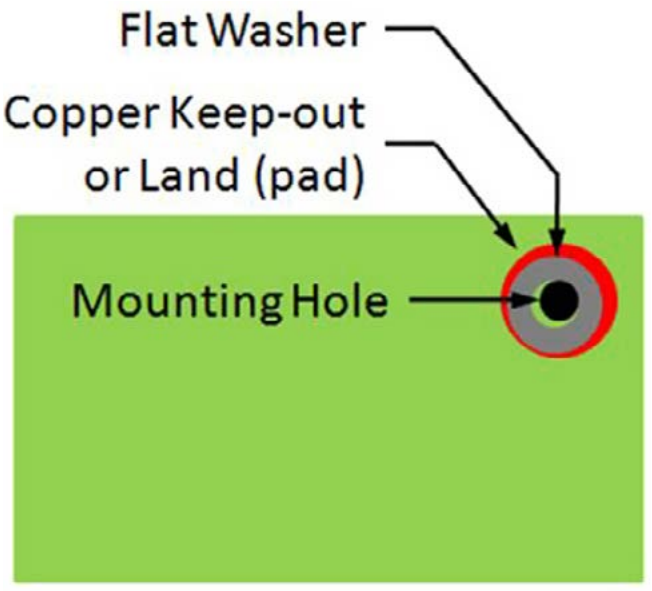

Figure 29: Keepouts can prevent short circuits.

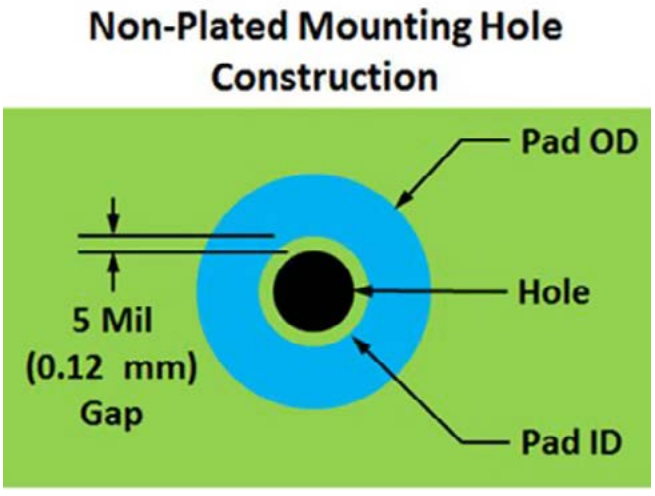

Figure 30: Example of non-plated through-hole construction.

ter than the pad to pregreg adhesion. The pad will break away from the PCB before the ball breaks away from the pad. So solder mask defined very fine pitch BGAs hold the pad to the PCB, which decreases failure if the device is dropped (Figure 27).

Paste Mask Stencil for Micro-Miniature Components

The average paste mask stencil thickness is 0.125–0.15 mm (5–6 mils) thick. The stencil manufacturer must thin out the stencil areas around all chip components less than 0402. Figure 28 is an example of a real 1:1 scale 0201 chip resistor that has a 0.033 mm thickness and placed on 0.15 mm paste mask. You can easily see that the solder volume is way too much for this miniature component. So the paste mask stencil must be thinned out to reduce the solder volume.

Mounting Hardware

Every PCB layout has mounting holes to attach the PCB to an enclosure. It is important for the PCB designer to add keep-outs to allow for the hardware manufacturing tolerance to prevent short-circuiting the hardware to a trace, via, copper pour or component pad (Figure 29).

For non-plated (unsupported) mounting holes, I highly recommend a pad; this way, the metal hardware (screw head, washer or nut) contacts a pad rather than the bare board. Figure 30 shows non-plated mounting-hole construction.

For many years I created unsupported mounting holes with no pad annular ring, but I never saw the damage that metal hardware does when it comes in contact with the bare board FR-4 material. The solder mask and woven glass get roughed up when torque is applied to tighten the screw and when too much torque is applied, the FR-4 material crushes. I also recommend that the pad be constructed using a donut pad with the inside diameter of the pad to be pulled away from the hole by 5 mil (0.12 mm) so that the drill bit goes straight through FR-4 material and does not hit any metal. **PCBDESIGN**

Tom Hausherr, CID+, CIT, is founder and CEO of PCB Libraries Inc. To contact him, click here.

Mil/Aero007 News Highlights

Blackfox Debuts IPC Course Focused on Space Assemblies

Blackfox announces the latest addition to their IPC industry-developed and approved program curriculum, IPC/WHMA-A-620 Space Hardware Addendum. As a follow up to the IPC/WHMA-A-620B course, the space addendum provides additional requirements to ensure the performance of cable and wire harness assemblies that must survive in space.

Saline Lectronics Achieves Distinction with AS9100C Audit

The company has completed its AS9100 Certification for the fifth year in a row, and this year received a Best-In-Class distinction. Saline Lectronics is now certified to AS9100 Revision C, the fourth and latest release of the AS9100 standard, which takes in the revised requirements of ISO 9001:2008 and nearly 100 additional criteria specific to the aerospace industry.

SMTA Finalizes Counterfeit Electronic Parts West Program

SMTA and CALCE are pleased to announce that the program for the Counterfeit Electronic Parts and Electronic Supply Chain Symposium West is finalized and registration is open. This symposium will provide a forum to cover all aspects of changes in the electronic parts supply chain on how an organization performs part selection and management through the entire life cycle.

Conflict Minerals Issues Reach Far into Europe

Under pressure by U.S. laws, human rights campaigns, and guidance from the Organisation for Economic Co-operation and Development, European companies are already being asked by their customers to declare the use of conflict minerals.

U.S. DLA Program Mitigates Risks of Counterfeit Electronics

A little over a year ago, an initiative by the U.S. Defense Logistics Agency launched, aiming to sharply mitigate the risks of counterfeit electronic parts entering the military supply system. The effort featured SigNature DNA, an advanced anti-counterfeit technology platform. The initiative has already begun to pay off.

Cirtronics Achieves AS9100 RevC Certification

Cirtronics Corporation, a New England-based EMS provider, is proud to announce it has achieved quality certification to AS9100 RevC. AS9100C certification is an internationally recognized quality management standard for the aviation, space, and defense industry.

Sanmina's Mexico Plants Earn Diebold Awards

Sanmina Corporation, a leading integrated manufacturing solutions company making some of the world's most complex and innovative optical, electronic, and mechanical products, has announced that its Guadalajara, Mexico operations are the recipient of Diebold, Incorporated's 2012 Gold and Silver awards for quality and performance.

Axis Electronics Hosts SC21 Best Practice Supplier Event

The event focused on the successful implementation of SC21 tools within Axis Electronics to drive business and service excellence, helping Axis customers deliver excellence to end customers.

Tin Whiskers Symposium Presented by IPC, CALCE

"IPC and CALCE share a common goal of helping to educate the industry on the latest information about tin whiskers theory and practice," says Sanjay Huprikar, IPC VP of member success. "This partnership has expanded the reach of both organizations, allowing us to develop a strong agenda with presenters who have deep knowledge of the complex technical challenges related to tin whiskers."

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Painting Pads:

The Scourge of CAD-to-CAM Communication

by Karel Tavernier
UCAMCO

SUMMARY: Often called the "backbone of the electronics industry," the Gerber format is the easiest and most reliable image data transfer format available to PCB designers and engineers. Unfortunately, this format is often used incorrectly, including one practice that PCB designers should cease immediately: painting pads and areas.

Over decades, Gerber has evolved into the bare board industry's CAD-to-CAM data transfer standard, capable of describing a PCB image to within an astoundingly accurate 0.1 nm, in a clear-cut language that is fast and easy to use. Designs described in the RS-274X Gerber format are hassle-free, reliable and accurate, and can be implemented quickly, easily and cost-effectively.

This article will help the PCB design community get the very best out of this clean but sometimes poorly used format. We will show how old, outdated habits are creating problems for their manufacturing partners as well as compromising the quality of the final products.

The CAM Process

Before going on to discuss the problems, it is worth taking a little time to explore what happens, and what does not happen, to Gerber data once it enters the PCB manufacturer's systems.

Many users of PCB CAD systems believe that the data files they send to their PCB manufacturers will drive the fabricators' production machines; they think that their Gerber image files are production tools that will be used directly on the PCB manufacturers' photoplotter, the Excellon drill files will go straight onto the manufacturers' drilling machines, and their IPC-356 electrical test netlist information will go right into electrical test machines. They don't.

Manufacturers never use the Gerber or Excellon files directly on their equipment—never. There are numerous reasons for this, but the simplest is panelisation: The designer's data describes a single PCB. However, PCBs are always manufactured on panels with borders for plating, test coupons, and so on. Furthermore, to minimize costs, the manufacturer will produce several PCBs at a time on a single, larger panel. Another reason is that manufacturing processes inevitably introduce deviations: For exam-

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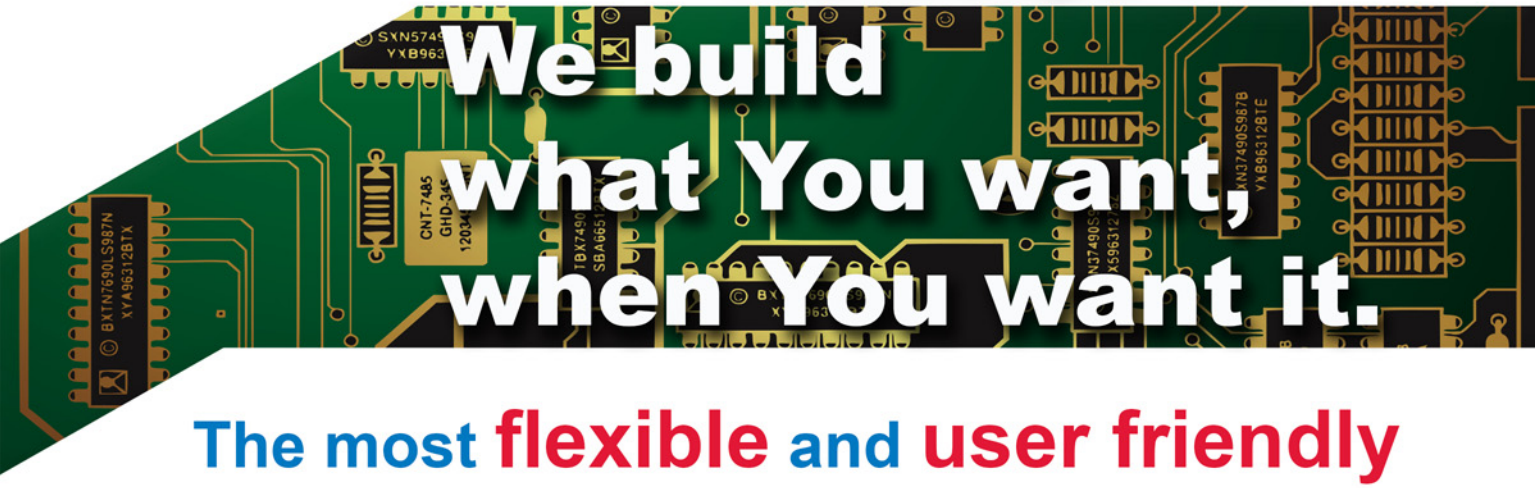

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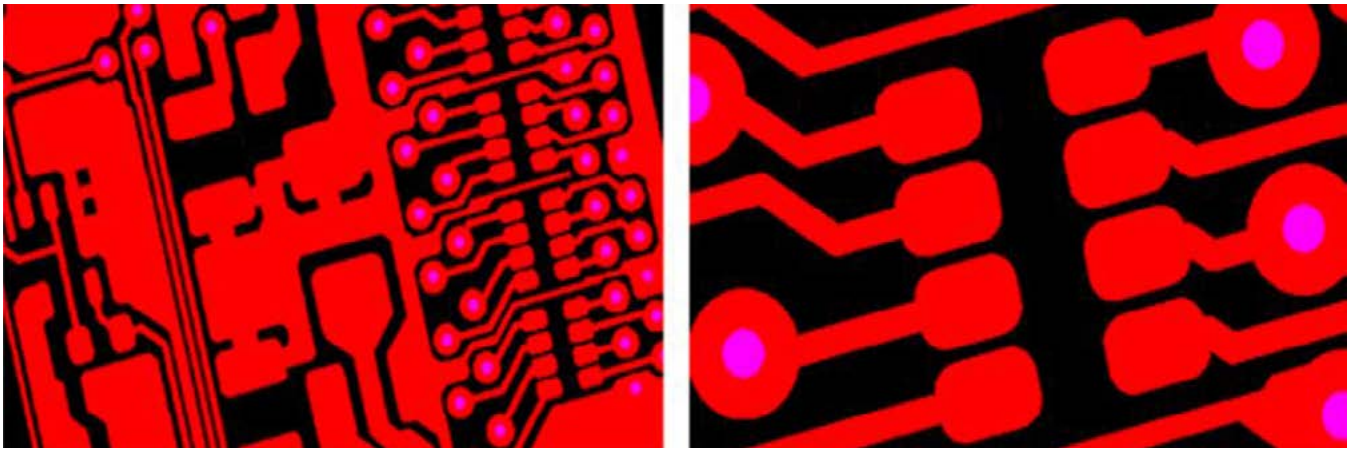

Figure 1: Painted features are visually clean...

ple, layers are distorted during lamination, and etching reduces line widths. The manufacturer must therefore modify the data to pre-compensate for these deviations.

So incoming data is always read into the manufacturer's CAM system, verified and transformed into valid production tools before it ever gets anywhere close to the PCB manufacturing line. In other words, the manufacturer loads the designer's data into his CAM system and reconstructs the PCB design and then transforms it into something the PCB facility can use. It is not possible to manufacture PCBs without this step.

For this to happen, the elements comprising the PCB must be clearly recognised and understood by the CAM system. Data files must therefore be valid, i.e., clear, unequivocal, and in a recognisable format so that they are readable in a digital system.

Too often, this is not the case, yet many of the designers and CAD vendors who could make a difference are unaware of this.

Painting

One of the most troublesome practices used by designers today is one in which pads, and sometimes other features, are "painted." This is otherwise known as "stroking," "paint-fill," "stroke-fill," and "vector-fill." This practice, born decades ago in the heyday of the Standard Gerber format, was then a necessary design step. The vector photoplotters used at that time were driven by computers that were nowhere near as sophisticated as those we use today, so the shapes they could plot were very limited indeed. Thus designers would build pads using separate elements: curves or circles for the rounded corners, lines, or strokes, for the edges, and more strokes to fill the outline.

Things have, of course, moved on since then. In today's CAD systems the pad shape is described by a geometric primitive or its outline, but instead of outputting this shape properly, too many systems are still "improving" the output by filling the outline with numerous filling strokes. The result, to the naked eye, is a clear, nicely-generated pad, and a correct image (Figure 1). But to a CAM system, it's chaos. Rather than reading a single pad, the system sees the digital reality: a hodgepodge of disconnected curves and straight lines, which it simply cannot recognise as anything particularly meaningful (Figure 2). Consider this happening not just once but maybe hundreds of times, and in different sizes, and across a densely populated PCB. It quickly becomes obvious that painted features are a CAM engineer's worst nightmare.

Of course, the image is correct, so one may think there is no big problem, just the nuisance that the files are bigger than they could be. However, the manufacturer needs more than a correct image. As we will demonstrate below, he needs to know the exact location and shape of all pads, areas and tracks.

Of course, CAM systems have tools that aid

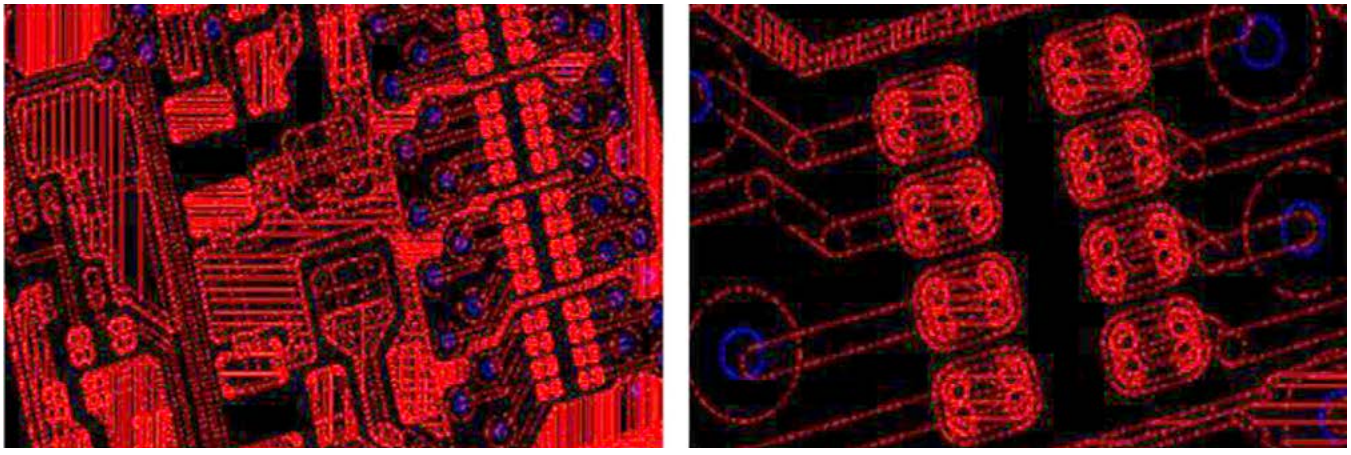

Figure 2: ...but they are also digitally chaotic.

the search for painted features and their conversion into a CAM-legible structure, but this is still incredibly labour-intensive. Everything has to be verified manually, slowing the CAM phase considerably, potentially creating delays in delivery, or worse, giving rise to PCB errors further down the line. It also adds unnecessary complexity to the Gerber file, and as each feature is made up of a large number of objects, the files are humongous and slow.

Pads

PCB manufacturers need to know exactly where every single SMD, component and via pad is on the board. This information is used for netlist creation and electrical test, to ensure that the soldermask is applied precisely where necessary, for via plugging, and to ensure that all clearances are within spec. And, of course, the assembler needs to know where pads are in order to apply paste.

Instant recognition and selection of all pads is also important where feature dimensions must be modified to comply with designers' specs, for example, and as I mentioned, to compensate for the fabricator's specific etching process parameters.

Because pad data is so important, any fabricator that receives images with painted pads must scan the whole image, guess where the pads are and typically replace all painted pads by proper flashed pads (see Figure 3) prior to working with that file. This is a lengthy process that can give rise to errors in the product, because the manufacturer ends up having to gauge the designer's intentions rather than dealing with clear data.

To obviate all of these problems, pads should be generated properly. This is easy with RS-274X Gerber, which has a number of built-in pad shapes, and a powerful and unique macro language that makes it easy to create any shape, easier in fact than with any other PCB image format. So there is really no need to use painting. Shapes are defined using the %AD and %AM parameters, and are then flashed wherever a pad should be: one flash, one pad.

Areas

Many PCB layers (e.g., power and ground layers) contain large copper areas, some of which can be extremely complex. The areas contain holes, or clearances that allow non-connecting vias to go through the planes. Theses are also known as antipads. Here too, some designers will paint these areas, carefully filling in around the antipads. The problems thus created are similar to those mentioned above, but whereas a pad is relatively small, an area can take up a significant part of a layer's surface area. The least of the CAM engineer's resulting problems is that the incoming data file is huge.

The real issue is that the inside of an area will accomodate so many draws that it becomes extremely difficult for the CAM system to differentiate between draws that should be within

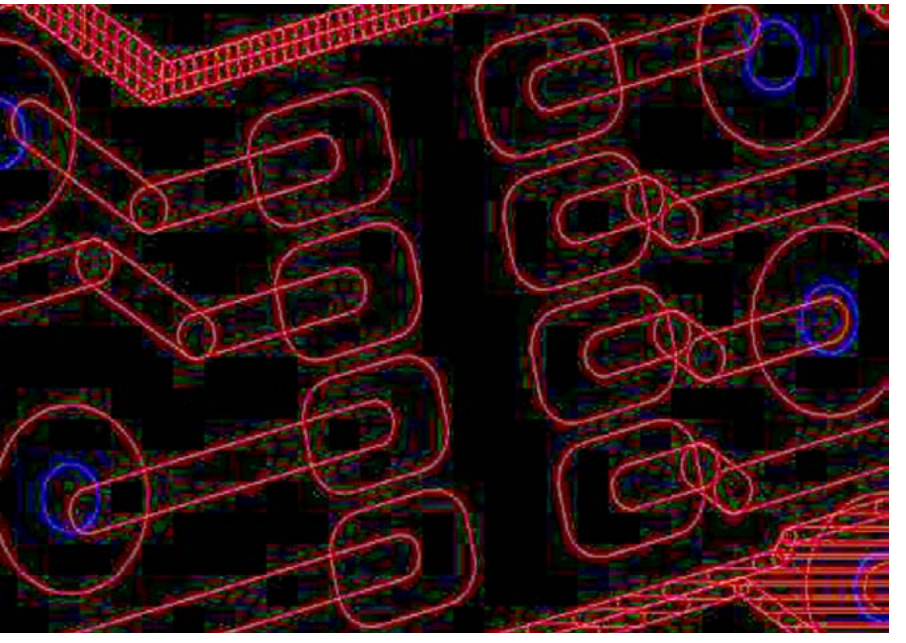

Figure 3: Painted pads are replaced manually with properly flashed structures, in this case using flashmaker.

the area, and draws that define neighbouring tracks. This creates all sorts of problems. For instance, when track width must be modified to compensate for etching parameters, it is crucially important to know which draws represent tracks and which represent painted pads or areas. The picture becomes even muddier when designers place embedded painted pads within painted areas.

Here too, in a lengthy, complicated, error-prone, manual operation, the manufacturer must replace the painted area with a properly constructed one, separating out the pads, tracks and areas from a messy jumble of draws.

This can all be avoided easily, as the CAD system will define the area by its outline, not by painting it in. The outlines can be directly stored in the Gerber file using the G36/G37 commands. This supports areas of any shape, size and complexity using concise, clear language, while antipads and their positions are defined precisely and efficiently by using the %LP parameter to make a negative layer containing all the holes. The areas are automatically filled later when the Gerber RS-274X file is created.

Tracks

Unfortunately, even tracks can be painted, the designer using multiple narrow draws to build tracks of the desired width. Here, the abovementioned problems are magnified hugely and recovering a proper job from them is a massive manual task. The only proper way to construct a track is to draw it with the correct aperture.

The Gerber Format and Painting

Some claim that painting is somehow intrinsic to the Gerber format. This is a fallacy.

But in the distant past, when RS-274-D was in use, there was some truth to this.

Using this format, the creation of non-standard shapes was so cumbersome that pad painting was a constant, and indeed painting in was the only way to create areas. So yes, D was guilty as charged for encouraging, even requiring, painting. But the D format is now obsolete, and these issues were solved more than 20 years ago with the introduction of the current Gerber format, RS-274X Extended Gerber. Why anybody in his right mind today would use D rather than X is a mystery to me.

So it is a fallacy to state that the current Gerber format requires or encourages painting. Areas can be created by contours; in fact, any pad shape can easily be created. Indeed, thanks to its aperture macros, Gerber offers designers the most powerful features available for the creation of arbitrary pad shapes.

The majority of Gerber files do not use painting, and there are plenty of files in ODB++, Barco DPF that do use painting. Which makes it very clear that painting is not a Gerber thing. Rather, it is due to a poor understanding of the CAM process, bad practices, bad setup, and sometimes poor implementation of file output software.

The Designer's Role

Of course, designers could say, and some do, that this whole issue is not their problem.

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Not so. By passing painted features to their fabrication partners, designers set up those partners to fail. The CAM engineer either resolves the painting issues pre-CAM, which is a time-consuming and error-prone process, or he passes the problems on, in which case the CAM process itself becomes time-consuming and error-prone. Caught between a rock and a hard place, the engineer's problems are made more acute when working to tight time constraints, and he may have to opt for speed rather than thoroughness.

So he's damned if he does and damned if he doesn't; he and the manufacturer get the blame for long turnarounds and missed deadlines, for quality problems in the product itself, and for potentially costly repairs and the wrath of his clients. It's an unenviable position and it's grossly unfair, but the problem is not just his to deal with. Poor data quality threatens the reputations and the businesses of everybody, from the manufacturer to the designer, the assembly company, and any OEM or EMS provider involved. And any compensation that may, unjustly, be exacted from the PCB manufacturer is poor recompense for all this damage.

The upshot is that it makes no sense whatsoever to use painting.

RS-274X does away with any need for this risky, outdated practice. I therefore urge any designers still using the obsolete RS-274-D Standard Gerber to move to the RS-274X format. I also strongly recommend that any designers using RS-274X, but who are still using painting, should make it a priority to review their working practices to eliminate it. The new, clarified RS-274X specification ensures that data is all-encompassing, clear and unambiguous. The unsatisfactory necessity of having to interpret data must become a thing of the past.

The CAD Vendor's Role

I would also like to put in a plea to CAD vendors to do their part in improving CAD-to-CAM data transfer. While it is understandable that they should retain painting as an option for compatibility with those rare systems that cannot handle proper Gerber, painting is at best a terrible waste of time, and often a quality risk. At worst, it is one of the most damaging CAD practices around. Painting should never be the default mode. The default mode should instead be flashed pads and the outlining of areas, with painting available as a legacy option.

Ucamco's Role

Ucamco does not make money out of the use of the Gerber format. On the contrary, caretaking Gerber is expensive and time-consuming. We do it because we are committed to the industry, and the industry is committed to Gerber; Gerber is used in possibly 95% of CAD-to-CAM data transfers globally. But it is also used improperly: An estimated 25% of designs created in RS-274X, for example, use painting. And then the format or the PCB fabricator are unjustly blamed. Designers seldom hear of the problems created and are often unaware that they are even using poor design practices, because fabricators feel unable to press for better data for fear of losing orders or clients.This is exacerbated by the fact that the supply chain is sometimes so long, complicated and successively outsourced that it is impossible to talk with anybody who is interested, or sufficiently versed, in design issues.

This article may have a somewhat revolutionary tone, but I hope that it at least provides food for thought. I hope the design community will take these points seriously enough to look at their design habits, to change them where necessary, and perhaps to find out where and how they can improve the lot of their PCB manufacturing partners.

Above all, I hope painting will soon become a thing of the past. It is a risky design practice that can impact every part of the electronics manfacturing chain, from the PCB manufacturer through the designer to the final customer. It is a throwback to days of old, as obsolete as paper tape or half-inch magtape. **PCBDESIGN**

Karel Tavernier is managing director of Ucamco. He has 30 years of experience with software and imaging equipment for the PCB and electronic packaging industry, including sales, service and R&D. He has been in his present role since 1995.

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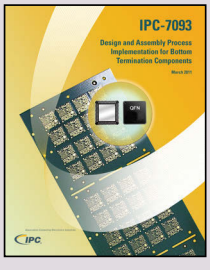
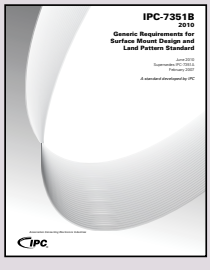
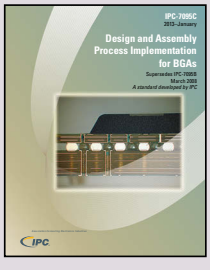


IPC-7093, *Design and Assembly Process Implementation for Bottom Termination Components*



IPC-7351B, *Generic Requirements for Surface Mount Design and Land Pattern Standard*



IPC-7095C, *Design and Assembly Process Implementation for BGAs*

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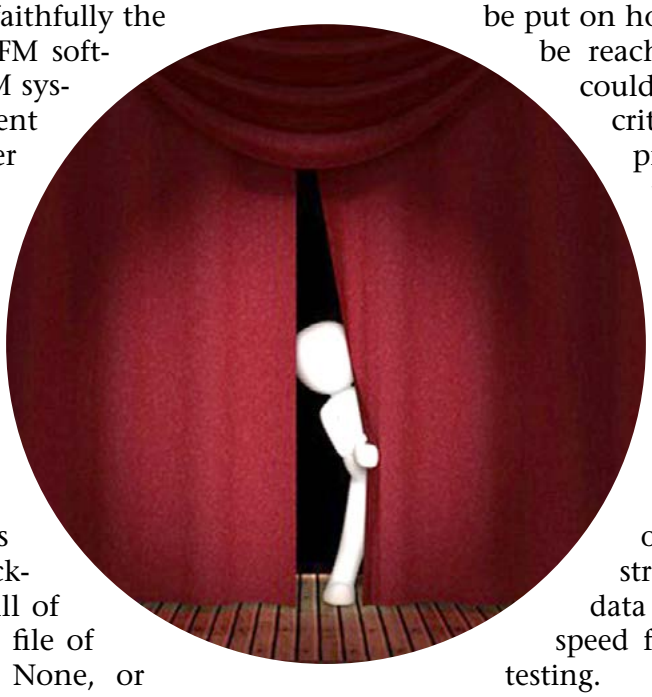
Behind the Scenes With IPC-2581

by Amit Bahl
SIERRA CIRCUITS

On October 16, 2013, IPC published IPC-2581B, the updated industry-standard format for transferring PCB design data from CAD tools directly to CAM systems for board fabrication and assembly. Representatives from the nearly 50 companies who belong to the IPC-2581 Consortium had revised the standard to support detailed stackup definition including material types, and incorporated further refinements so designers could express their build intent with even greater clarity. Whether the industry embraces this intelligent format, which can speed PCB manufacture, depends upon how faithfully the vendors of CAD tools, DFM software developers, and CAM system developers implement it. The first releases under IPC-2581B are expected in 2014.



The great majority of PCB designs are exported to fabricators as Gerber files that graphically define the layers, in conglomeration with a drill file, a netlist, a board drawing, a file of coordinates to drive assembly pick-and-place machines, a bill of materials, and a read-me file of notes and instructions. None, or few of these files share the same format, except for the Gerbers. All of that information in disparate formats must be imported to the CAM systems that control the fabrication and assembly processes. Manufacturers have to review and prepare the data before they can be downloaded, and that takes time.

Consider what happens when a board manufacturer receives Gerber files. There is no fixed guideline on the design side for naming layers, their types (plane, signal, soldermask), or polarity, with Gerbers. A fab front-end engineer has to identify the order of the layers, which usually consumes about 15 minutes per job. That may not seem long, unless you are a prototype manufacturer who receives 100 orders daily from customers with large investments riding on getting assembled boards for testing, debugging, and design revision by the product deadline.

Most Gerber files are received in the RS-274X extended format, but occasionally some arrive in the outdated RS-274D format, and those require more work. If there is any doubt about how layers are designated, the job must be put on hold until the designer can be reached. The delay certainly could jeopardize a customer's critical schedule and impact production planning at the fab.

IPC-2581B incorporates rich attributes to clearly explain exactly what manufacturers should build and aggregates all the elements of a design—every aspect from layer description through assembly—into one file, in one format, to streamline downloading the data to CAM systems. It will speed fabrication, assembly, and testing.

In my January 2013 column, I noted that my company had volunteered to fabricate a reference design on behalf of the IPC-2581 Consortium to validate the prevailing version of the standard, when CAM software would be available to load the design. No U.S. manufacturer had yet built a PCB from an IPC-2581 file.

Here is what happened. Fujitsu Network Communications and Sierra are both Consortium members, and we collaborated to evaluate the transfer and fabrication of a design output from a Cadence Allegro platform in the IPC-2581

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BEHIND THE SCENES WITH IPC-2581 *continues*

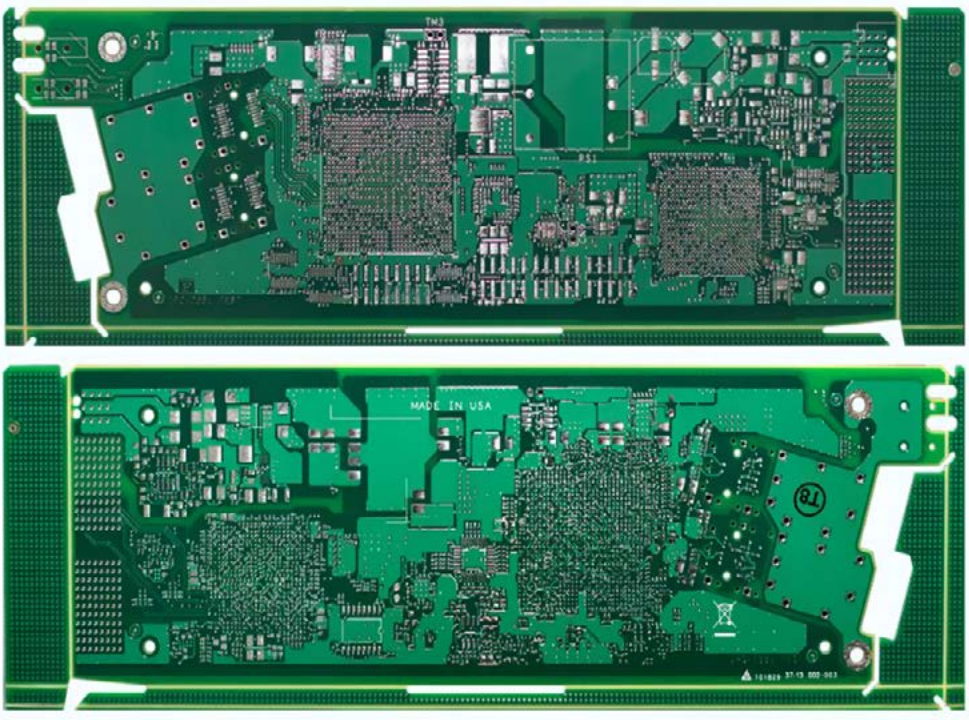

Figure 1: This network line card, built by Sierra Circuits in September 2013, is the first PCB fabricated directly from an IPC-2581 design file by a U.S. manufacturer.

(version A) format. The evaluation vehicle is a 12-layer network line card, measuring 8.5" by 3" (Figure 1). The board design was output directly from the EDA tool in both the IPC-2581 format and the ODB++ format for comparison. The design was also processed and output as an array in both formats from Wise Software VisualCAM (Wise is also a Consortium member). Each file was imported to our Valor Genesis system and compared for production.

The data were assessed to determine the source or sources of any anomalies and, in particular, whether the IPC-2581 file was valid for fabrication. Ultimately, four problems were identified, none of which were native to the files exported in the IPC format.

First, the Genesis software for inputting IPC-2581 data failed to recognize pad rotations that were properly described in the design file. Second, Genesis did not translate the step-and-repeat direction, which was correctly provided by way of the file from Wise to create the array. Third, the attribute tagging SMD pads as such in the IPC-2581 data was not recognized by Genesis. Fourth, the layer types as designated in the IPC-2581 data were not interpreted by Genesis.

Notably, none of the identified anomalies prevented the design from being fabricated directly from the IPC-2581A file. The format proved valid. Consortium member Sanmina and Sierra independently fabricated boards from the same design in the IPC format.

Aside from the glitches resulting from origins other than the design file, the test convinced me that the IPC-2581 format can save significant time in transferring design data to fabrication and improve clarity. When properly implemented, the IPC-2581 format can minimize workflow errors in fabrication.

Frontline Genesis V10.1, which will be released in the first quarter of 2014, will show layer type coincident with IPC-2581 design files. Genesis V10.1 will also correctly indicate pad rotation.

Open standards such as IPC-2581 that are free from commercial restraints are good for the entire supply chain. Sierra Circuits will compare vendors' implementations of IPC-2581B as they become available. I would very much appreciate any comments and recommendations. **PCBDESIGN**

Amit Bahl directs sales and marketing at Sierra Circuits, a PCB manufacturer in Sunnyvale, CA. He can be reached by clicking here.

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TOP TEN

News Highlights from PCBDesign007 this Month

① Zuken's E3.series 2014 Now Available

The company has announced new features for manufacturing and design productivity in the latest version of E3.series: New functionality for panel manufacturing; file preview in Windows Explorer and Outlook; support for Lattice 3D Viewer; and many new ease-of-use features.

② Intercept Celebrates 30 Years with Deep Discounts

"As the year closes, we decided to offer the most meaningful tribute to the industry we could come up with; we are discounting our software to insanely low prices for the remainder of the year," said Dale Hanzelka, director of sales in North America.

③ Agilent Launches RF and Microwave Student Certification

Agilent Technologies has announced the RF and Microwave Industry-Ready Student Certification program, developed in conjunction with the University of South Florida, a founding partner. The program, a collaboration between universities and industry, recognizes students who have demonstrated RF/MW design and measurement expertise.

④ FabStream, Electro Schematics Host SoloPCB Design Contest

The rules for this design contest are simple, the prizes are fun, and entry is easy. Use FabStream's free software, visit the Electro Schematics website, and submit your design files to enter the contest.

5 IPC-2581 Consortium Seeks New Members

Getting OEMs, design tool providers, EMS providers, and others to agree on a standard for transferring data files has proven a difficult challenge. The IPC-2581 Consortium, formed to help industry settle on a data transfer document, is beefing up its efforts by opening its membership to individuals.

6 Zuken and CONTACT Software Form Joint Venture

In a first for the electrical and fluid design market, Zuken and CONTACT Software have established a joint venture to provide best-in-class engineering process and data management specifically designed for today's distributed, concurrent design projects.

7 ICD Stackup Planner Incorporates Flex Materials

In-Circuit Design Pty Ltd (ICD), Australia, developer of the ICD Stackup and PDN Planner software, has incorporated flexible circuit and embedded component materials into its latest software release. "This enhances integration of the Stackup Planner with EDA tools that support rigid-flex design," said Managing Director Barry Olney.

8 Altium Debuts Altium Designer 14

The new Altium Designer 14 extends the company's leadership position in native 3D PCB design systems by delivering a new customer-centric platform with heavy emphasis on core PCB design technologies. Altium Designer now features support for flex and rigid-flex design, including schematic capture, 3D PCB layout, analysis and programmable design—all in a single, unified solution.

9 Downstream Releases BluePrint-PCB Version 3.6

The major component of this software release is the newly developed integration between BluePrint-PCB and Cadence OrCAD PCB Designer and Allegro PCB Layout tools. The integration automates the PCB documentation process for Cadence users and eliminates all manual file transfer between the applications. The release also includes many other new features and performance improvements.

10 Hunter Expands Portfolio; Acquires NBS Design Assets

"The purchase of the operational assets of NBS expands our portfolio of contract product design, engineering, and manufacturing services," said Hunter President Joseph F. O'Neil. "With these assets, and Hunter's ability to provide the highest quality products and services in the EMS industry, we are positioned for rapid organic growth."

events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out *The PCB Design Magazine's* event calendar.

Gartner Symposium ITxpo 2013
November 10–14, 2013
Barcelona, Spain

productronica 2013
November 12–15
Munich, Germany

SMTA/iNEMI Medical Electronics Symposium—Tabletop Exhibition
November 12, 2013
Milipitas, California, USA

Aerospace & Defense Programs
November 13–14, 2013
Phoenix, Arizona, USA

MILCOM'13
November 18–20, 2013
San Diego, California, USA

Energy Harvesting & Storage USA 2013
November 20–21, 2013
Santa Clara, California, USA

Printed Electronics USA 2013
November 20–21, 2013
Santa Clara, California, USA

Graphene LIVE!
November 20–21, 2013
Santa Clara, California, USA

OLEDs LIVE!
November 20–21, 2013
Santa Clara, California, USA

Supercapacitors USA 2013
November 20–21, 2013
Santa Clara, California, USA

HKPCA & IPC Show
December 4–6, 2013
Shenzhen, China

Austin (CTEA) Expo and Tech Forum
December 5, 2013
Austin, Texas, USA

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Next Month in *The PCB Design Magazine:*

Power Integrity Analysis

Designers and design engineers have focused on signal integrity for over a decade, but now the power distribution network is taking center stage. Next month, our experts take an in-depth look at power integrity analysis of AC and DC power, and many common PI challenges and solutions. Don't fight the power—control it!