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October 2013

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Improving Quality During Assembly with DFX

by Murad Kurwa and Jesus Tan, Page 10

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The Accelerating Technology Convergance in Medical Devices — Implications for the Future, Mark Kemp, President, Flextronics Medical

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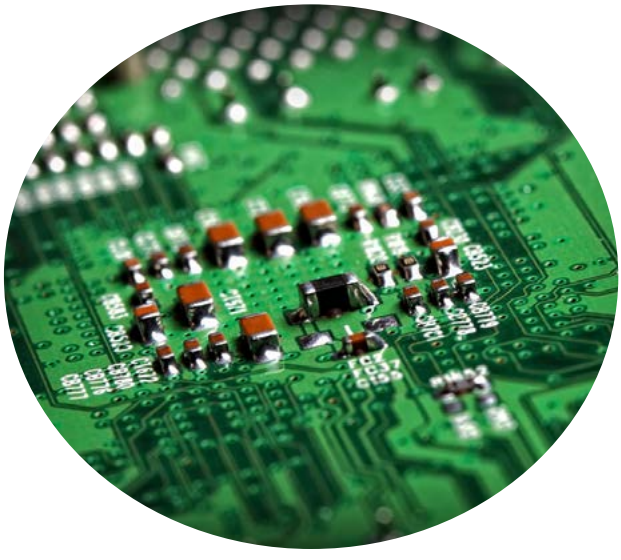
October 2013

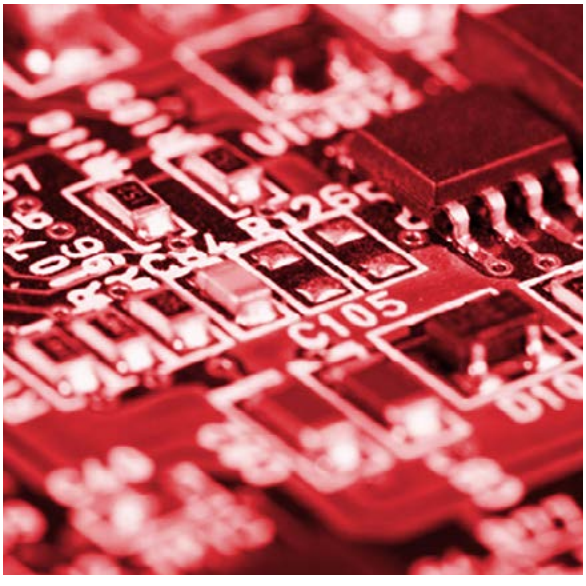
This Issue: DESIGN FOR ASSEMBLY

FEATURED CONTENT

In the rush of meeting time-to-market deadlines, it's easy for PCB designers and design engineers to overlook issues related to assembly. But processes that take place downstream can still have an effect on your job on the front end. This month, our contributors provide a rundown of some assembly trends that designers need to be aware of, and they offer valuable tips on DFA as well.



FEATURE COLUMNS



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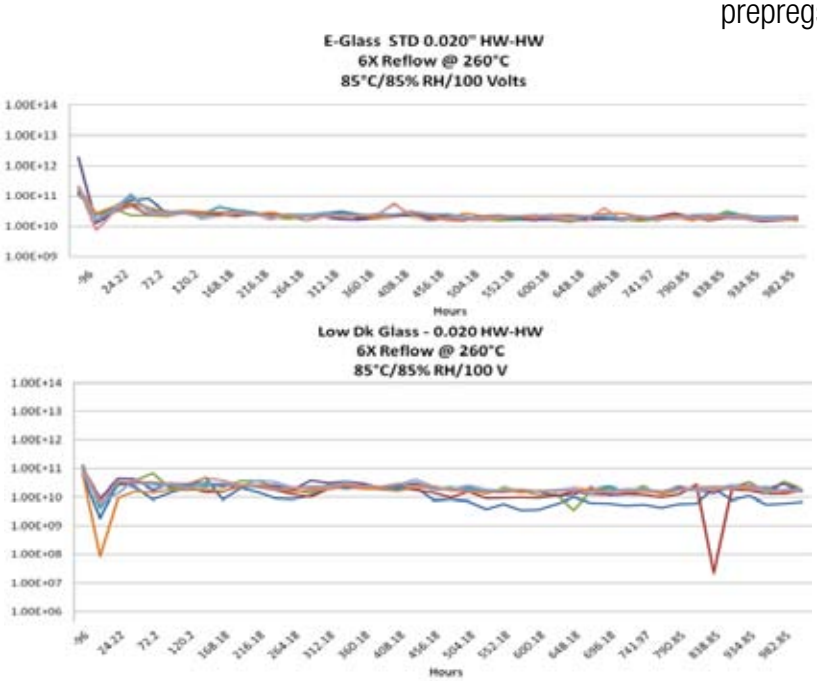

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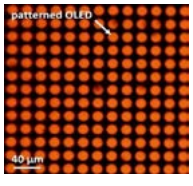

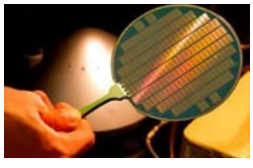

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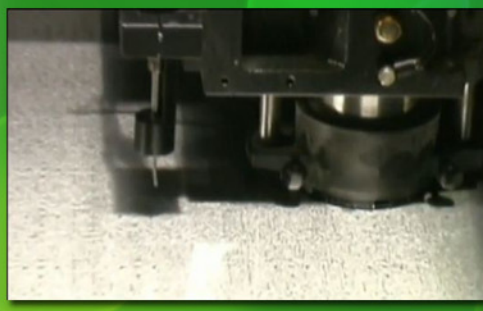

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PCB West a Good Omen for 2014

by Andy Shaughnessy
I-CONNECT007

It had been a few years since I last attended PCB West, but the show has been growing steadily over the past few years. I'm glad I went this year. It's always great to see old friends and meet new ones.

This event kicked off with the Zuken party. The company plans to spend millions expanding its presence in North America, starting with a new Silicon Valley office, and they held a poolside party at the Hyatt Regency Santa Clara. The weather cooperated, and a talented jazz band set the mood for the night.

Zuken showed off some of their customers' products: A Fiat 500 and a few Zero electric motorcycles were parked around the pool, bracketing a great sushi selection. Customers and potential customers mingled throughout the night; Zuken has been encouraging direct communication between non-customers and customers, so potential users can get information about Zuken's tools first-hand.

Speakers included Zuken COO Jinya Katsube, GM of Zuken Americas David Gullickson, and Synopsys CEO Aart de Geus, who discussed the companies' partnership. And Senior Technical Marketing Manager Humair Mandavia detailed the future of the Silicon Valley office, which he will be heading up.

The exhibition opened on Wednesday, and attendees jammed the aisles for much of the day. I didn't see any real dead times, though traffic did slow down after lunch. At 5 pm, EMA Design Automation turned on the margarita machine, Altium got the beer and wine flowing, and the place was packed again.

Now at 75 exhibitors (not quite 2000 levels, but moving that way), PCB West was buzzing. The exhibitors I spoke with all support the one-day show, anchored by a three-day technical conference. A show like this isn't too much of a budgetary bite for these small and mid-sized companies.

On the Show Floor

• Nolan Johnson of Sunstone Circuits said the company is continuing to grow. Sunstone recently introduced a new version of its PCB123 design tool.

• The DownStream Technologies booth stayed busy, with founder Rick Almeida discussing new solutions such as SoloPCB. DownStream took home a New Product Introduction award for SoloPCB.

• Prototron Circuits' Dave Ryder and Mark Thompson said the company has been slammed for months. Thompson has barely had time to work on his hobby: Flying and restoring old airplanes.

• Colonial Circuits Sales Manager Wendy Osborn said the company has been busy, and they plan to keep investing in American-made equipment.

• Gary Carter, CAD manager at Fujitsu Network Communications, showed off two more PCBs that have been manufactured by different fabricators – Sanmina-SCI and Sierra Circuits – using the IPC-2581 data format. The boards were designed on Cadence Allegro PCB design software. This marks three boards that have been successfully fabricated with the up-and-coming IPC-2581 format, and the first to be created using Frontline Genesis fabrication software.

• Semblant is seeing more companies select the Semblant Plasma Finish (SPF) and conformal coatings. The company expects to have solid growth over the next year.

• Sierra Circuits' Amit Bahl said the fabricator continues to experience steady growth, and he sees a great 2014 for the company.

• Bay Area Circuits' Peter Brissette said the company has moved into a larger facility in Fremont, California. The fabricator held an open house to celebrate the move, which Brissette believes will lead to increased turnaround times.

• Leo Lambert of EPTAC said the company has expanded its training courses. Now, EPTAC has begun offering IPC Designer Certification, in addition to its manufacturing curriculum.

All in all, PCB West was a great show, and a good omen for the electronics community and the trade show season. At I-Connect007, we're getting ready for SMTA International, October 15–16, in Fort Worth, Texas. Next, we move on to productronica, November 12–15, in Munich, Germany.

We'll be providing Real Time video coverage of both of these shows, bringing you interviews with the industry's top technologists and managers. Then, in 2014, we're off to DesignCon, IPC APEX EXPO, CPCA, and NEPCON China.

See you at the shows! **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 13 years. He can be reached by clicking here.

Improving Quality During Assembly with DFX

by Murad Kurwa and Jesus Tan
FLEXTRONICS

SUMMARY: The number of DFM issues reported on a PCBA is inversely proportional to the components' pitch values. The authors discuss the problems facing designers who use cutting-edge BGAs, and the Flextronics DFX process that detected them before mass production.

Engagements between contract manufacturers and product companies can take place at various points in the product life cycle. However, it's very common for manufacturers to engage with product companies in the later stages of the product life cycle, during product transfer to mass production. This is the stage when companies tend to face some tough challenges such as launching products on time, meeting target cost, and maintaining quality and performance goals.

Manufacturing success is enabled by a robust product design, and design for manufacturing (DFM) is the methodology or art of designing a product in such a way that it is easy to manufacture. DFM also helps facilitate the manufacturing process in order to reduce the overall manufacturing costs.

DFM involves several types of analyses that are as diverse as products in the industry, and can consist of adjacent areas such as "design for" printed circuit board fabrication, assembly, enclosure, test, reliability and cost. In addition to core manufacturing processes, there are other areas of support including design for supply chain, design for automation and design for repair. These areas are becoming more and more important as the strength of labor arbitrage is diminishing, making way for "right-shoring" products in different parts of the world.

All of these elements are grouped under the terminology "Design for X" (DFX), with the X as a variable for the combination of analysis types that can be triggered at different stages of the product life cycle. Regardless of the variables used, it is well understood in the manufacturing community that all the functions previously described have the highest potential on return of investment if aligned during the early stages of product design and development.

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IMPROVING QUALITY DURING ASSEMBLY WITH DFX *continues*

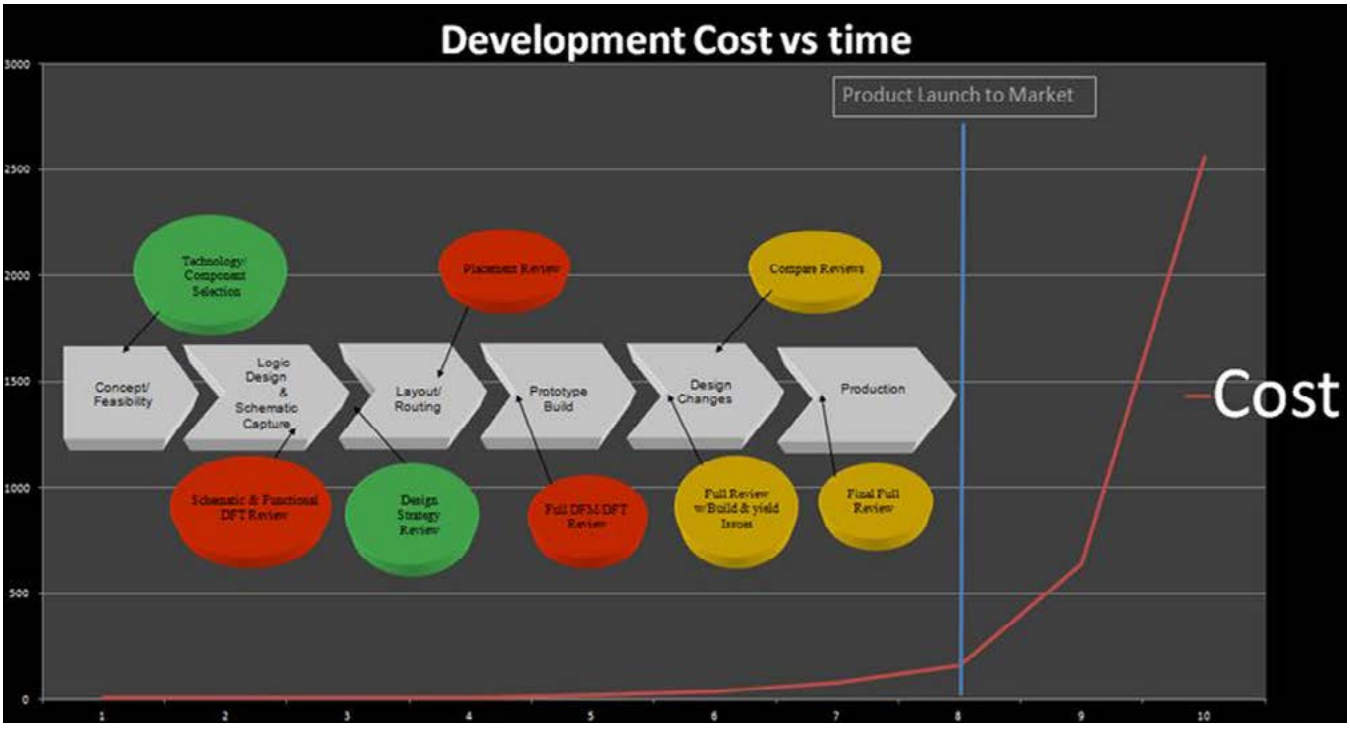

Figure 1: Development cost vs. time.

DFM has also been a crucial part of successful product development and an important methodology that is driven by concurrent engineering and time-to-market models. All the actions around this process are most effective when DFM is done at the earliest phase of the design or when the product is still being conceptualized. As the product approaches mass volume build, it becomes increasingly difficult and costly to implement modifications and design improvements to fix DFM challenges. We recommend engaging your DFX team as early as possible in the product development phases (Figure 1).

Successful DFX engagement includes collaboration and communication between the company's designers and the manufacturer. Early collaboration can help prevent potential issues on the design bench, reduce overall time-to-market risk, and eliminate additional investments to repeat prototype samples before entering the new product introduction stage.

In most cases, the tools used to perform the DFM analysis are sophisticated CAD software tools, some of which specialize in circuit board analysis, mechanical and thermal analysis, and simulation such as assembly times/cost simulation or reliability simulation. Every tool is used in different stages of the design development process, depending on whether the product requirements and functions use some of the sub-analysis or not.

Case Study

The DFM process has different development phases required for each product. To serve as an example for this discussion, we will focus on the technology component selection for circuit board assemblies and its correlation with the production yield.

The number of DFM issues reported on a printed circuit board assembly (PCBA) is inversely proportional to the pitch value of the components, so it is worthwhile to revisit what packages the designers are using.

Figure 2 depicts the packages selected for different products built by Flextronics. As of September 2013, the Flextronics Component Team has created 114,875 unique geometric packages for use in DFM analyses. A full 70% of them are discrete parts and 2,500 of them are BGA packages. BGAs are among the top five

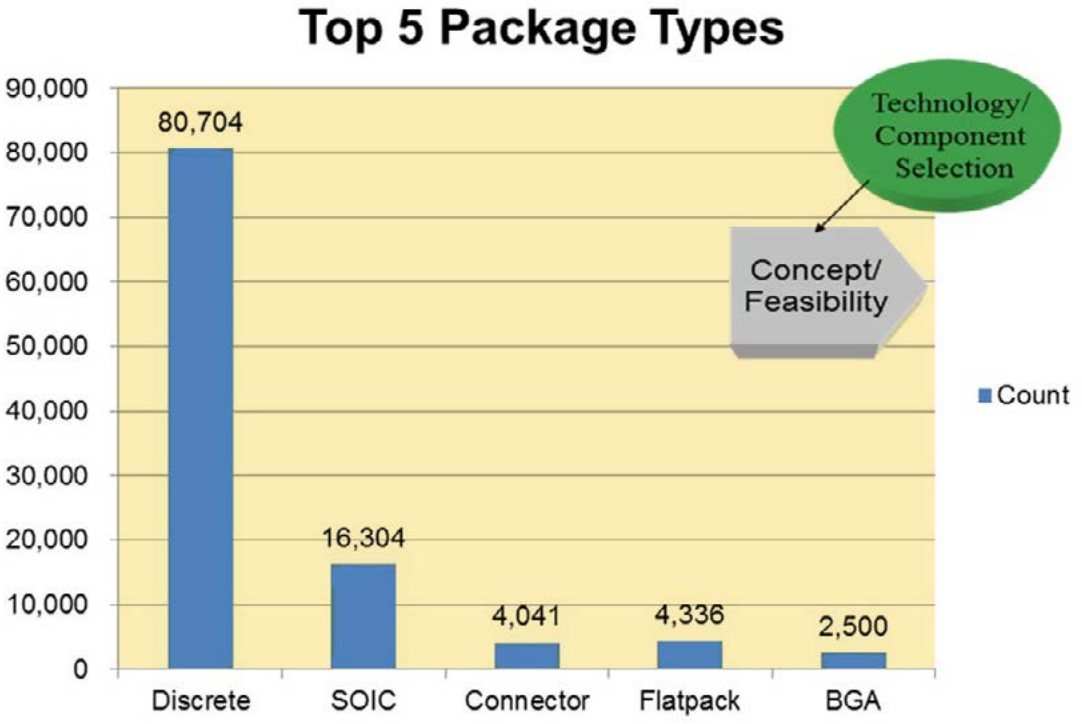

Figure 2: Top five package types used by projects at Flextronics.

package types used at Flextronics. This is due primarily to the high-velocity class of products we manufacture, combined with today's technology trends.

Almost 50% of the designs that featured BGAs utilized a 1.0 mm pitch followed by 0.8 mm pitch BGAs, both of which are prevalent in large and complex infrastructure products. On the other hand, 17% are fine pitch, 0.50 mm and 0.40 mm BGAs, which are commonly found on handheld devices (Figure 3) such as mobile phones.

Now, we'll focus on BGA usage trends on designs. 1.0 mm BGAs are commonly used in low-cost and low-power complex programmable logic devices (CPLDs). These components are selected because they save board real estate in designs of main logic boards, offer more density and a greater footprint in terms of input/output signals.

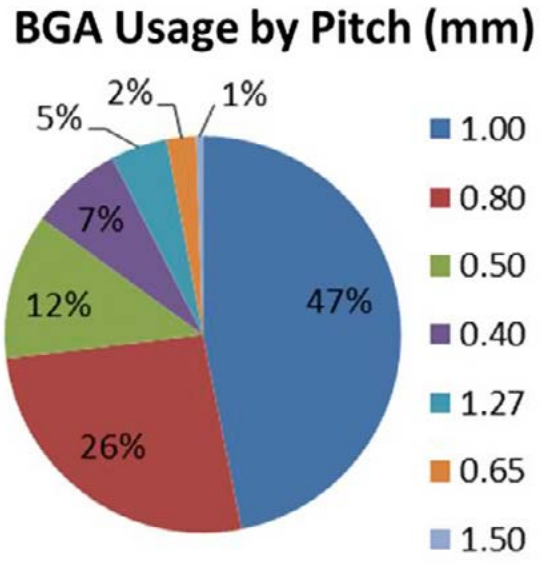

Figure 3: BGA usage by pitch, as recorded at Flextronics.

Challenges and Recommendations

BGAs with 1.0 mm pitch usually involve a high pin count and relatively larger body size. This type of BGA is prone to component warp during thermal cycling, so it is important to design the corner pads to minimize the PCB pad lift or pad cratering (Figure 4).

If this issue is detected early in the design, steps can be taken to minimize the pad lifting on corner pads, such as connecting the corner

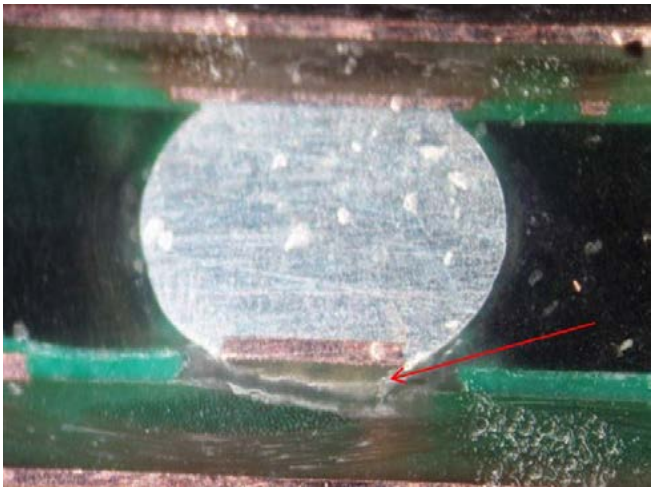

Figure 4: Sample of PCB pad lift.

pads to wider copper trace. Another method is to use a soldermask-defined pad. If the design cannot be changed, then the manufacturer needs to implement alternate or secondary processes such as adding glue on corners or underfill on affected BGA parts, which would increase the cycle time on the assembly. This process requires the addition of materials such as adhesives over the original design, and increases process steps.

The smaller the pitch of the BGA, the tougher it becomes to achieve the optimal PCB design that meets all design rules. As the pitch approaches 0.50 mm, the designer must decide whether to use microvias to meet the pad size recommended by contract manufacturers, or sacrifice the pad size and then route fine traces in between pads to save PCB cost. Figure 5 shows how difficult it is to add through-hole via in between fine pitch BGA pads.

As much as possible, steps need to be taken to avoid using a microvia to save on PCB cost. This example below is a 0.50 mm pitch BGA footprint that got away from microvia.

Another way of avoiding a microvia on a 0.50 mm BGA is to trim off a portion of the pads to make way to route copper trace in between BGA pads (Figure 7).

For BGA pitch 0.80 mm and below, if underfill and underfill rework is required, a DFX analysis would recommend soldermask-defined pads for a higher rework yield, except for 0.3 mm pitch CSP due to PCB fabrication limitations.

If DFX is performed properly and early on during the product development phase, both customer and manufacturer can benefit by making the design more manufacturable prior to mass production.

Figure 8 is based on actual data collected during product development. At the start of the DFM analysis in this case, 58 out of 63 issues were fixed by the designer, and then as the product development progressed, DFM issues

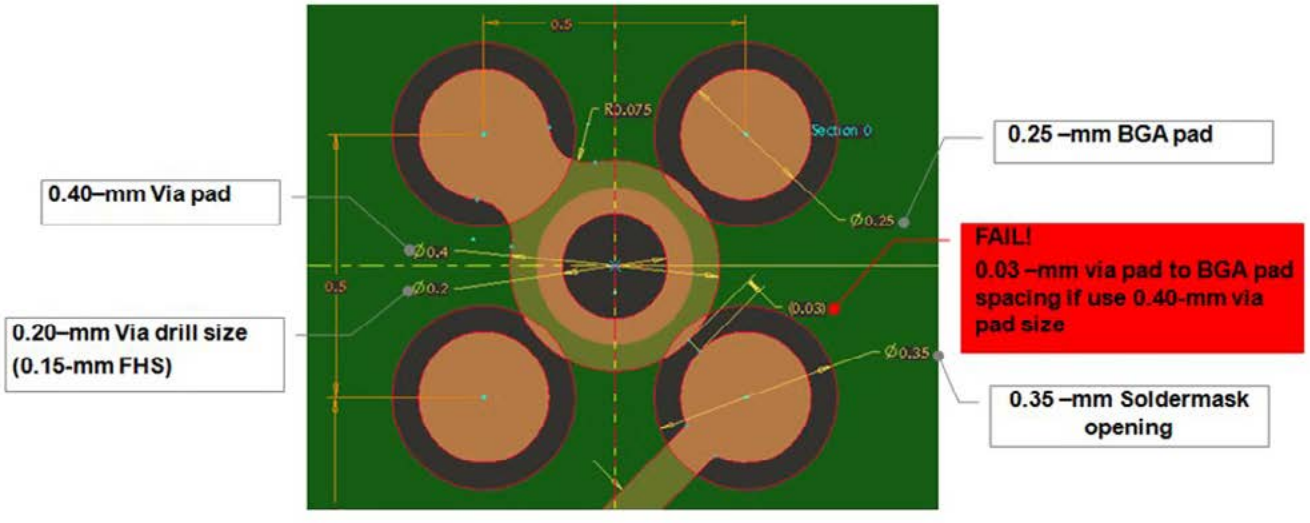

Figure 5: A 0.50 mm pitch BGA pad design with through-hole via.

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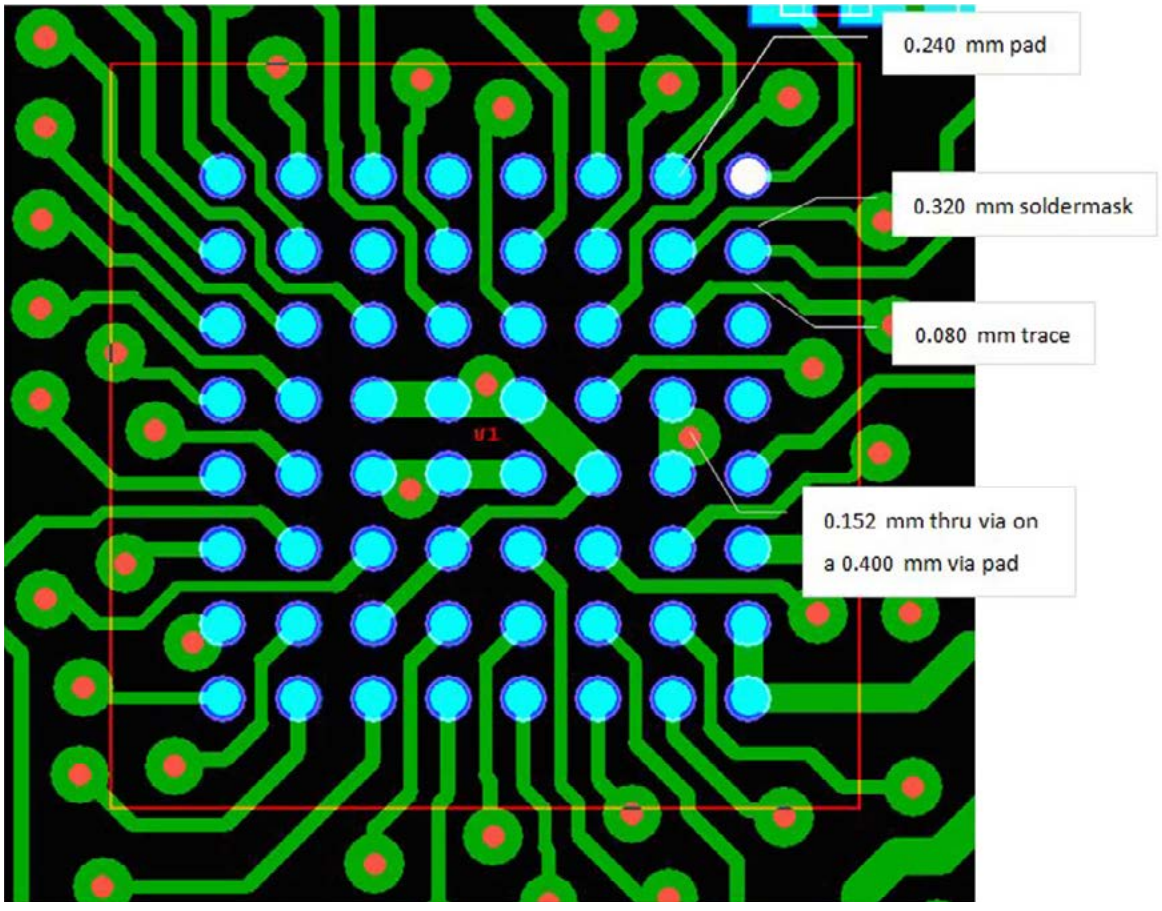

Figure 6: Sample of 0.50 mm BGA pad design.

reported were reduced, while the first-pass yield became higher. This is a simple demonstration of how DFM analysis can help in identifying the manufacturing risks and, by rectifying the design to address the DFM challenges, can result in a higher yield, which is the ultimate goal of manufacturing.

Engineering validation trials (EVT) that most often involve non-commercial and non-form factor designs are the best opportunities for starting DFX. This can lead to some iterative processes, which in turn lead to design validation trials (DVT). During this stage, more end-product and close to end-product are tested and validated to ensure performance meets specifications.

Furthermore, at this stage, production, tooling, and equipment including layout is designed, all of which is ultimately tested during product validation trails (PVT). At the PVT stage, one would expect very few DFX issues or violations, and when found, they are typically minor and can be addressed through a simple process optimization exercise, not product redesign.

Conclusions

In summary, with an increase in innovative product development, new product markets and a rise in customer demand for better products, it is imperative for OEMs and ODMs to partner with the contract manufacturer to apply DFX early in the design cycle.

More and more design check cycles are now co-managed by the designer and the manufacturer, who both share responsibilities and reduce the development cycle. DFX has also led to more use of simulation techniques such as finite element analysis (FEA) traditionally used for large form factor products or industrial product design. FEA includes both stress-strain predictions and thermal simulation, and both

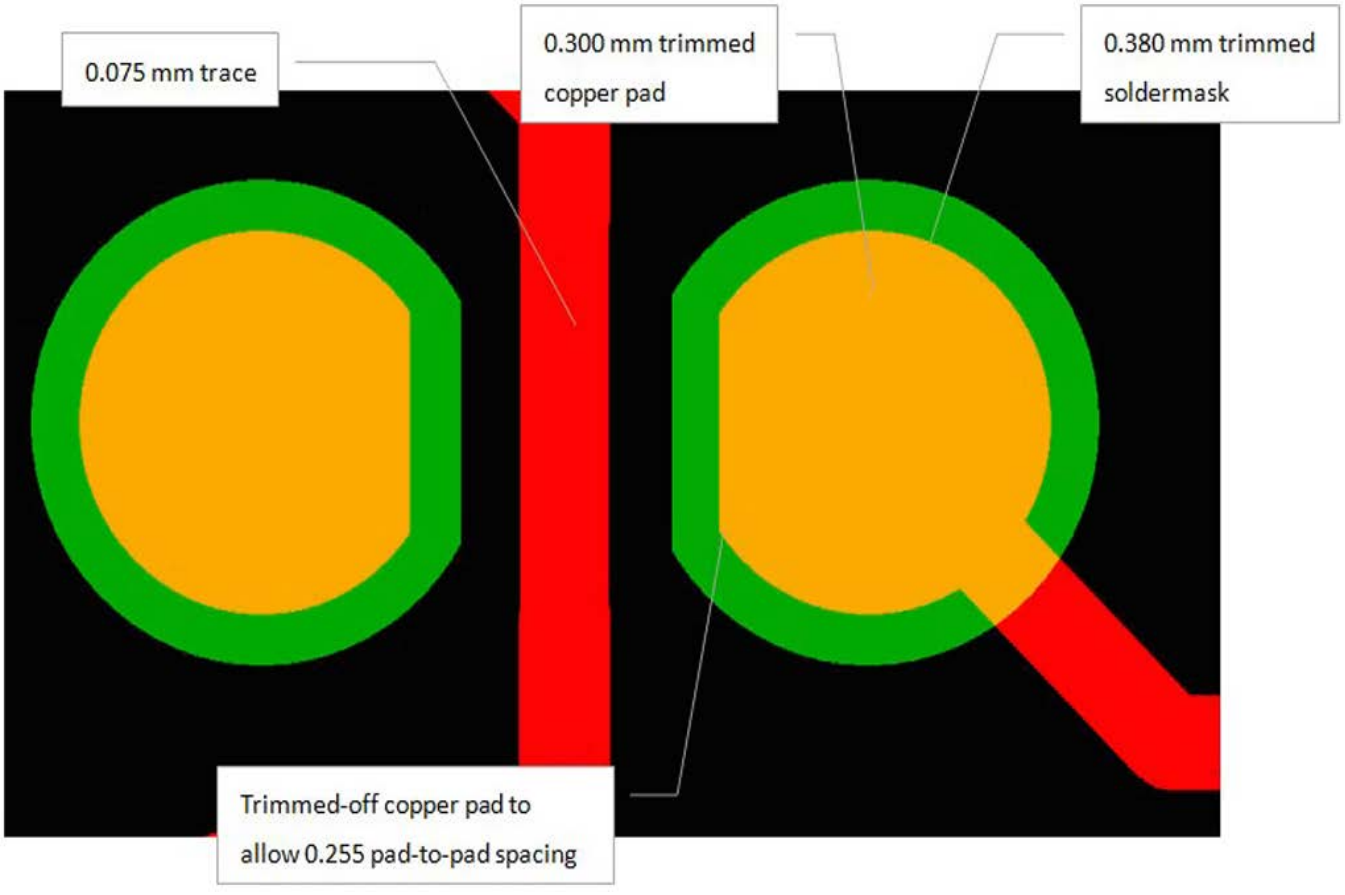

Figure 7: Alternate design for 0.50 mm BGA.

are now commonly used in Flextronics design centers as well as by the Central Advanced Engineering Group.

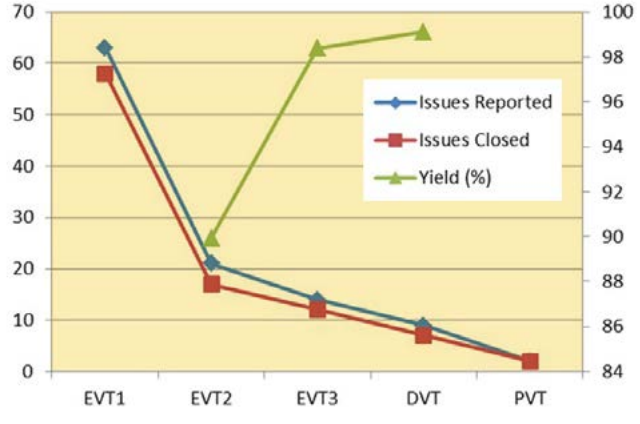

Figure 8: Correlation between DFA issues and manufacturing yield.

Contract manufacturers must work closely with customers to bring products to mass production and meet the customers' targets and goals. Early communication with the PCB designer and a robust DFX process can help reduce the number of design issues found during fabrication and assembly. **PCBDESIGN**

Murad Kurwa is vice president of Flextronics Advanced Engineering.

Jesus Tan is Asia DFX manager of the advanced engineering group at Flextronics.

video interview

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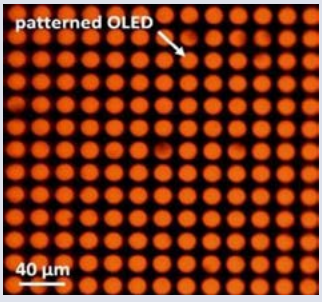
New Tech Aids Production of Organic Semiconductors

Research and development on organic semiconductors has intensified in recent years. Organic semiconductors can be used in various applications such as organic solar cells, flexible displays, organic photodetectors and various other types of sensors.

Current methods for patterning organic semiconductors include shadow masking and inkjet printing. However, these patterning methods are not suitable for high-resolution patterning on large-size substrates. Patterning based on photolithography would solve this issue. But photolithography is currently mainly adopted for patterning of silicon semiconductors. When applying it to organic semiconductors using standard photoresists, the photoresist dissolves the organic semiconductor material during processing.

Fujifilm and Imec have developed a new photoresist technology that enables submicron patterning on large substrates without damaging the organic semiconductor materials. The new photoresist technology was developed by fusing the semiconductor processing technology of Fujifilm and Imec, with Fujifilm's synthetic-organic chemistry material design technology. Since existing i-line photolithography equipment can be used, and investment for new equipment is unnecessary, the new technology contributes to a cost-effective production of high-resolution organic semiconductor devices.

For technical verification, Fujifilm and Imec developed organic photo detectors (OPD) and organic light-emitting diodes (OLED) using the new photolithography technology, and tested their performance. Organic semiconductor materials were patterned to produce OPD composed of fine light receiving elements down to 200μm×200μm size.



Generally, patterning of organic semiconductor materials degrades the property of converting light into electricity, but the OPD developed in this case were patterned without degradation. With respect to the OLED arrays that were produced using the newly-developed photolithography pattering method: 20μm pitch OLEDs emitting uniform light, were realized.

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High-Frequency Materials for Lead-Free Soldering

by John Coonrod
ROGERS CORPORATION,
ADVANCED CIRCUIT MATERIALS DIVISION

Some OEMs' qualification procedures dictate that PCBs be subjected to multiple passes through a lead-free solder reflow cycle. The qualification requirements differ from one OEM to another but some will require 5, 6 or even 10 passes through a lead-free solder reflow process. There are a few different criteria for these tests, however the basic demand is that the PCB must remain mechanically intact and show no signs of delamination. The materials that make up the PCB can have a major impact on the ability of the PCB to survive the lead-free solder evaluations, and some materials perform better than others.

The material properties related to lead-free solder survival are typically coefficient of thermal expansion (CTE), glass transition temperature (T_g), decomposition temperature (T_d) and moisture absorption.

As a general rule, the material should have a CTE of 70 ppm/°C or less and closer to the CTE of copper, about 17 ppm/°C, which is best. Other general rules suggest a T_g value higher than 170°C, T_d greater than 300°C and moisture absorption less than 0.5%.

The high-frequency circuit material industry offers many laminates and prepregs (or bonding material) to choose from. Some of the laminates and bonding materials are robust for lead-free soldering, and others are not. Additionally, there are some bonding materials which are not intended to be used at lead-free soldering temperatures.

A broad classification of bonding materials can be thought of in two categories. Some bonding materials are thermoplastic, while others are thermoset. A thermoplastic bonding material has the attribute of being able to reflow or melt when subjected to certain elevated temperatures. The thermoset materials will not melt or reflow when subjected to elevated temperatures. However, at high temperatures, the

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concern can be related to material decomposition.

Each type of thermoplastic bonding material has different characteristics, and one of these is the melt temperature. Some common thermoplastic bonding materials used in high-frequency PCB fabrication are PTFE, FEP and chloro-fluorocopolymer (Rogers' 3001 material). As for the PTFE bonding materials, some of these are pure PTFE and others are filled PTFE. Depending on the filler, some of these bonding films can have a lower or higher melt temperature than PTFE.

The 3001 bonding material is often used for laminating high-frequency PCBs when a bonding material with low dissipation factor (Df) and low dielectric constant (Dk) is needed. The Df of this material is 0.003 and the Dk is about 2.3 when tested at 10 GHz per IPC-TM-650 2.5.5.5c (the clamped stripline test). This material is also intended to be used when subsequent processes are not beyond the melt temperature of the material. During the lamination process, the 3001 bonding film is held under pressure and brought to a temperature of about 450°F (232°C). After the lamination process is complete, the PCB should not be subjected to temperatures above 350°F (176°C); however, this is not the melt temperature of the material.

As thermoplastic materials are heated, their modulus decreases; higher temperature translates into softer material. The 350°F limit for 3001 bonding film is due to the material being very soft at this temperature, and any mechanical stress could cause delamination of the PCB.

When a bonding material with low Dk and low Df is needed and the PCB will be subjected to elevated temperatures after the lamination process, FEP is often used. This material has a Dk of 2.1 and Df of 0.001 when subjected to the clamped stripline test. The melt temperature of this material is higher than the 3001 material, so the lamination temperature is higher as well. A lamination temperature of 565°F (296°C) is recommended and PCBs using this material should not be subjected to temperatures above 520°F (271°C) in follow-on processes. Lead-free soldering temperatures are typically lower than 520°F, so FEP has been used in PCB applications where lead-free soldering is necessary.

As thermoplastic materials are heated, their modulus decreases; higher temperature translates into softer material. The 350°F limit for 3001 bonding film is due to the material being very soft at this temperature, and any mechanical stress could cause delamination of the PCB.

The other thermoplastic material suitable for high-frequency PCB bonding is PTFE or filled PTFE. This requires a special fusion lamination process, and few fabricators have this capability. Thermoset bonding materials (prepregs) are generally easier to laminate, and they are more robust for elevated temperature exposures in successive processes. While this is true, some of the thermoset systems have trouble surviving lead-free soldering. This is generally due to the materials' CTE, T_g, T_d or moisture absorption properties. A relatively new bonding material that is thermoset and robust for lead-free soldering is Rogers' 2929 material. With a CTE of 50 ppm/°C, T_g of 170°C and a T_d at 400°C, this material has proven to be a good choice for high-frequency multilayer PCBs where lead-free soldering is required.

Fortunately for PCB designers, a variety of available bonding materials can withstand the elevated temperatures often associated with lead-free soldering of high-frequency PCBs. **PCBDESIGN**

John Coonrod is a market development engineer for Rogers Corporation, Advance Circuit Materials Division. To contact Coonrod, click here.

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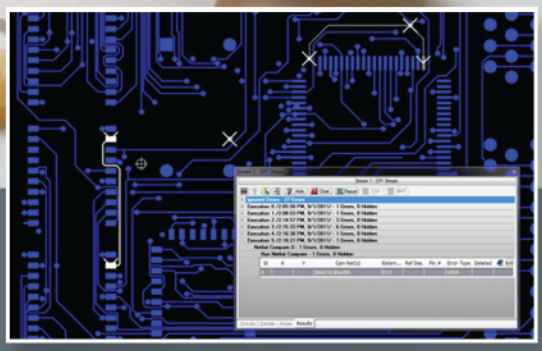

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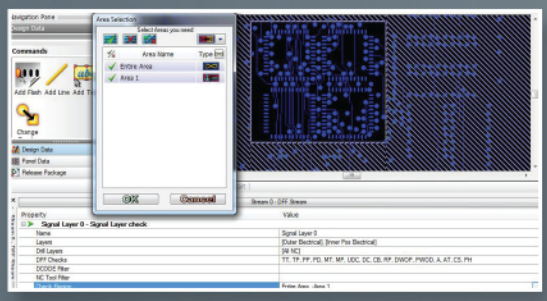

Define DFM checks by area so components such as BGAs can be verified with unique rules different from rest of design

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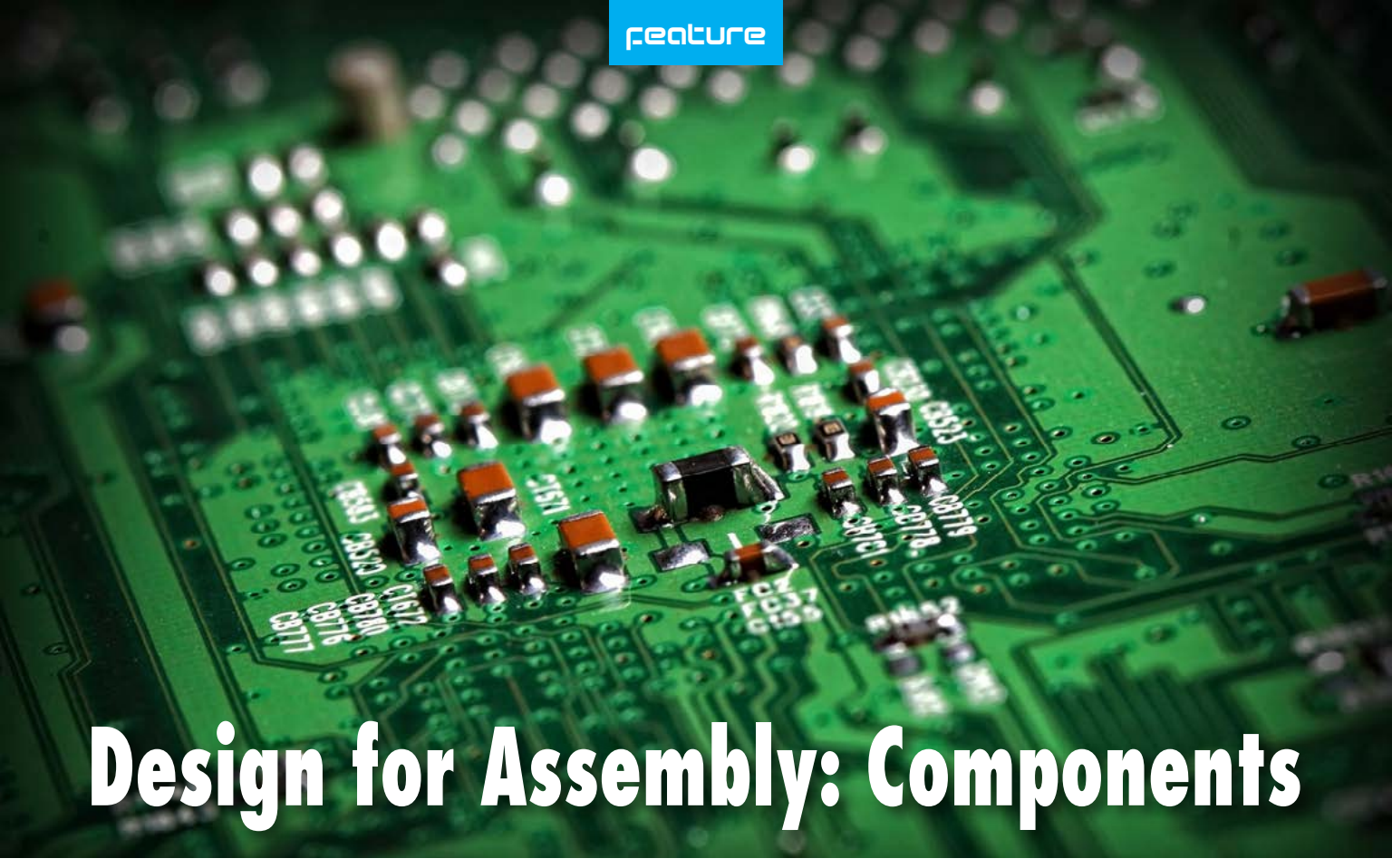

Design for Assembly: Components

by Tom Hausherr
PCB LIBRARIES

Every PCB layout must go through the component assembly process, and a PCB designer can do several things to make the assembly process easier.

IPC Classes 1, 2 & 3 for Defect Reject/Accept Criteria

A PCB designer needs to design every layout to meet one of the IPC product classes so that the manufacturer knows the category classification of the end electronic product being designed. A PCB designer can find these three product classes in most IPC standard publications:

CLASS 1: General Electronic Products

Includes products suitable for applications where the major requirement is function of the completed assembly.

CLASS 2: Dedicated Service Electronic Products

Includes products where continued performance and extended life are required, and for which uninterrupted service is desired but not critical. Typically the end-use environment would not cause failures.

CLASS 3: High-Performance/Harsh Environment Electronic Products

Includes products where continued high-performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as medical life support, military battlefield or other critical systems.

The IPC-7351B land pattern standard uses a three-tier PCB library system for various electronic device applications. These include most, nominal and least dimensional criteria. Figure 1 shows the three-tier footprint density levels.

These three tiers are not directly related to the three IPC classes, but picking the most appropriate land pattern might help the manufacturer achieve a higher yield for a specific IPC product class. It is widely assumed that designs that need to meet IPC Class 3 must use a "Most – Level A" land pattern. This is not true. Any of the IPC-7351B three-tier environments can be

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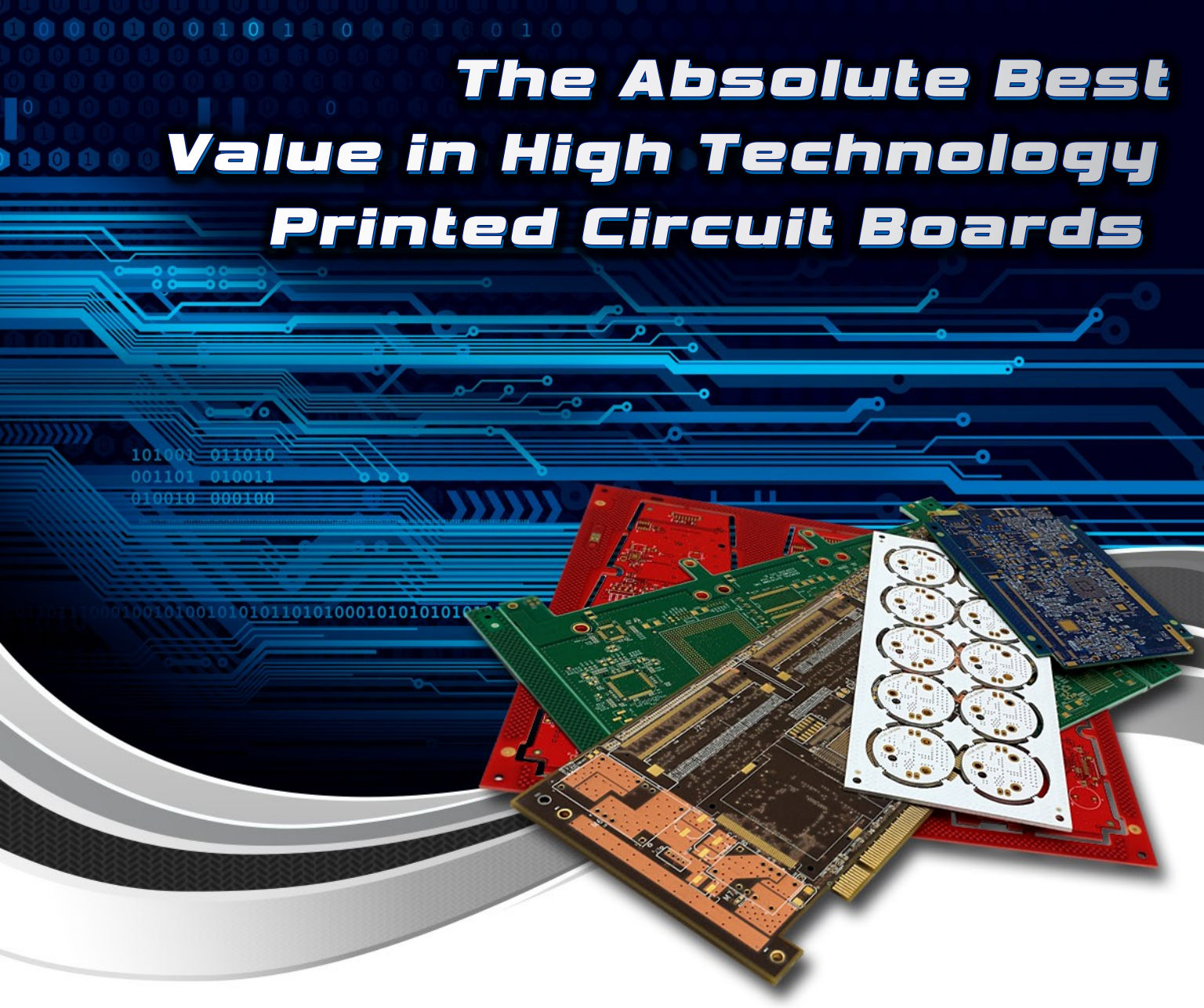

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DESIGN FOR ASSEMBLY: COMPONENTS *continues*

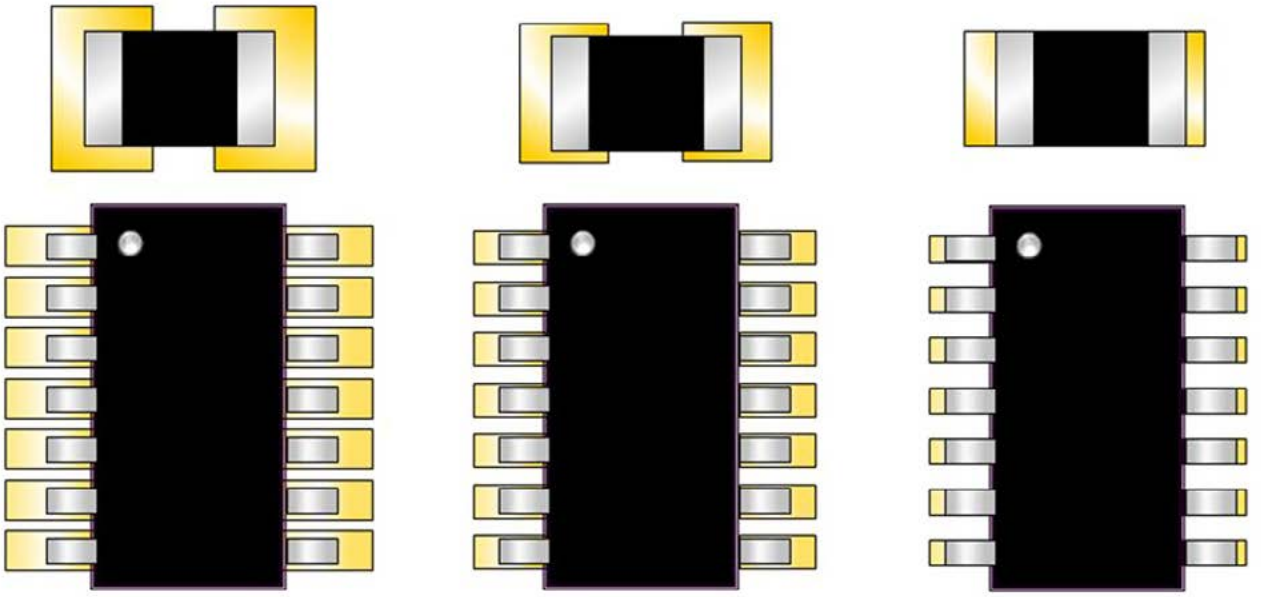

Figure 1: IPC-7351B uses this three-tier footprint density level system.

used to build a Class 3 board assembly. It's just that a Density Level A (Most Environment) land pattern will make it easier for manufacturing to achieve a higher yield. However, an IPC-7351B Nominal Environment land pattern can be used to create a Class 3 electronic product. And the Least environment might also be used to create a Class 3 product but the manufacturing price will go up as the yield goes down.

Useful Silkscreen Outlines

Silkscreen outlines add cost to PCB fabrication and in most cases they are not necessary.

However, if you use silkscreen outlines, here are my guidelines for creating PCB library parts.

1. Silkscreen outlines should never be located under the component because they are covered up during assembly and do not provide any useful function to the assembly process

2. Follow J-STD-001E Assembly Requirements Section 9.2: Silkscreen polarity marking, reference designators, revision level and serial numbers shall be visible after assembly, as shown in Figure 2

3. Silkscreen outlines should be mapped to the maximum component body outline

4. Your company's pad-to-silkscreen drafting rule should override maximum component body mapping

5. Silkscreen outlines are used for assembly placement registration accuracy and post assembly inspection

6. The silkscreen line width and pad to line gap are normally the same value

7. Silkscreen outlines should always be located inside the placement courtyard, otherwise the silkscreen outlines can get confused with other components or overlap with other silkscreen outlines

8. Only one line width should be used throughout the entire PCB library

Silkscreen-to-Pad Clearance

The yet-to-be-released IPC-7351C will introduce guidelines for three-tier silkscreen lines' widths as shown in Figure 3. Some PCB designers allow silkscreen on pads and they expect the fabrication shop to trim the silkscreen away

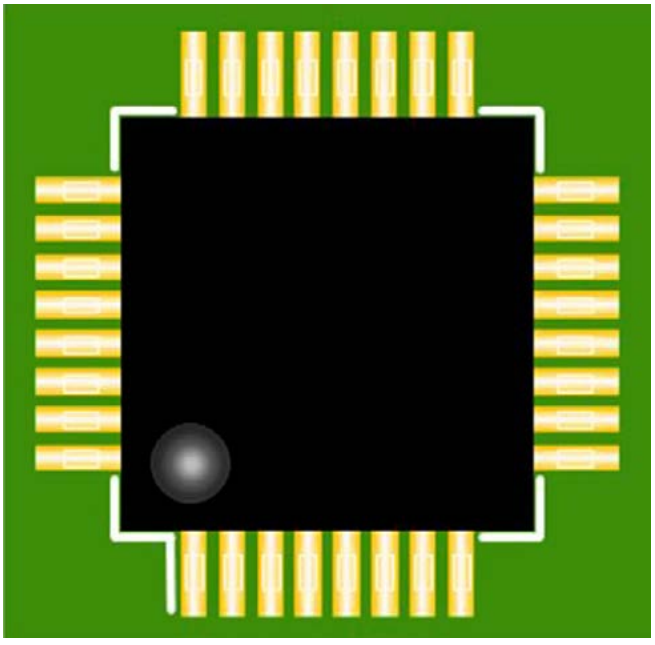

Figure 2: Silkscreen polarity marking, reference designators, revision level and serial numbers should be visible after assembly.

from the pad. But what if the fabrication shop doesn't do that? Silkscreen ink on a solder pad becomes a solderability issue. The assembly shop will be scrapping the silkscreen ink off the pads prior to applying the solder paste via stencil if fabrication shop does not. But assembly will be dealing with soldering issues from the pad contamination!

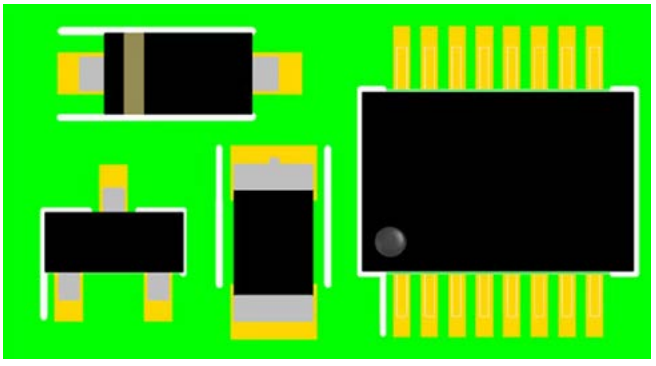

Figure 4: Recommendation for silkscreen polarity.

Polarity Markings or Not?

Components that can be inverted (like resistors) during assembly do have polarity marking. All parts that have to be inserted in a particular rotation require a silkscreen marker to indicate polarity or Pin 1. My recommendation for silkscreen polarity is to extend the silkscreen line the full length of the Pin 1 pad as shown in Figure 4.

For bottom-termination components, the placement courtyard hugs the package body or the pads. In this case, the absence of silkscreen is the best polarity marker as shown in Figure 5 for a QFN package.

Assembly Outlines and Polarity Marking

The assembly drawing component outlines should be a simple closed polygon and the po-

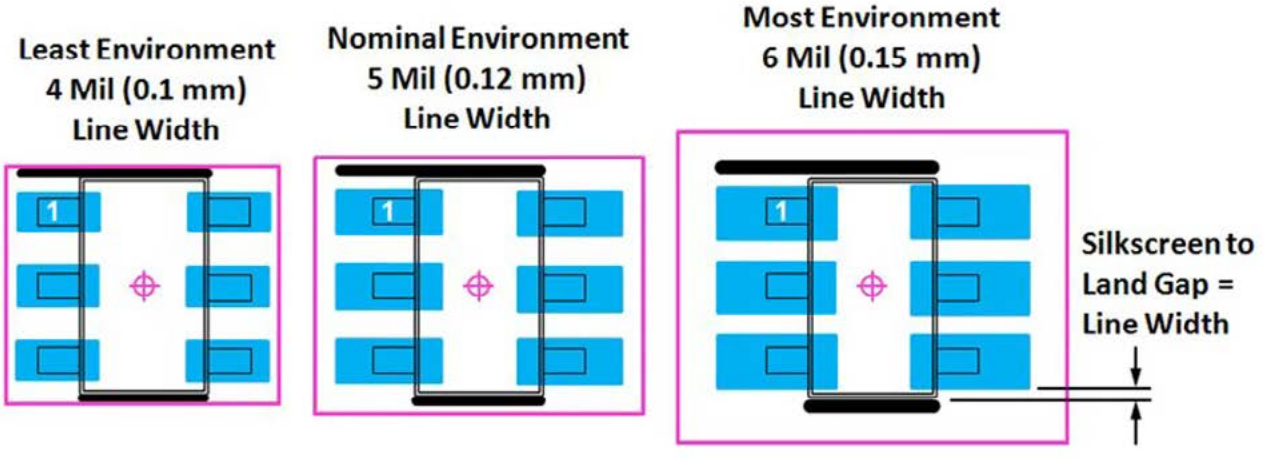

Figure 3: Three-tier silkscreen lines widths will be covered in the upcoming IPC-7351C guidelines.

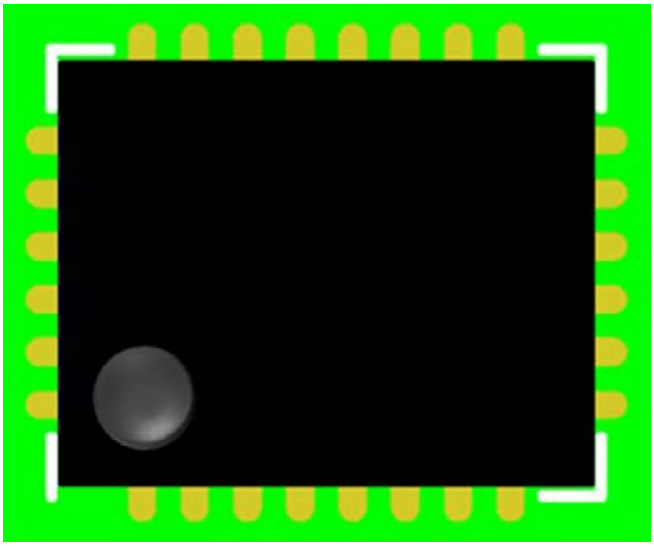

Figure 5: The best polarity marker.

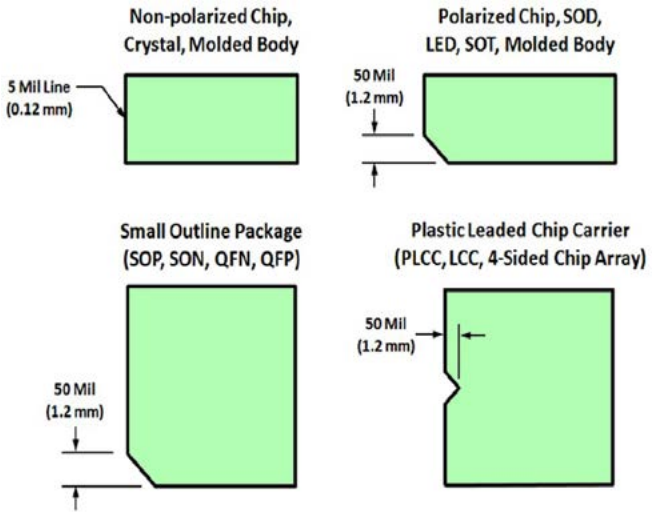

Figure 6: A good way to locate Pin 1.

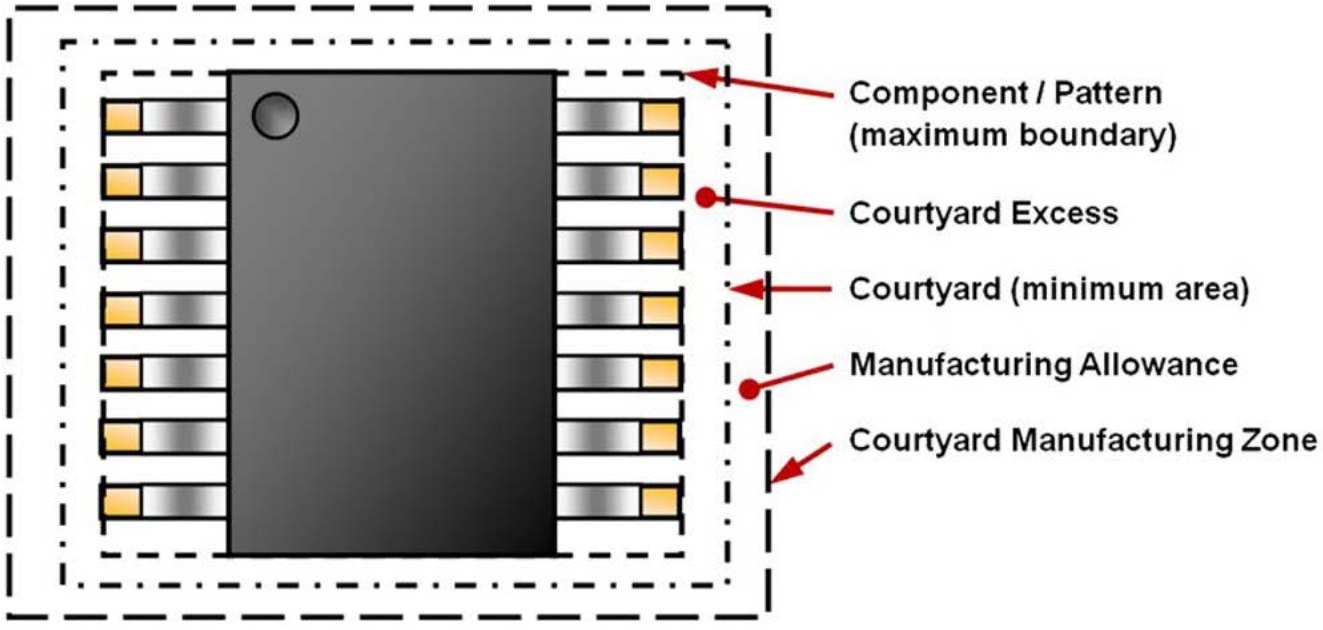

Figure 7: Courtyard excess.

larity marker should be a simple chamfer to locate Pin 1 as shown in Figure 6.

Courtyard Excess

Courtyard excess as shown in Figure 7 is used as a guideline for part placement. Every assembly shop has its own unique tolerances, and if the guidelines place the components too close together, the assembly shop has a manufacturing allowance: the necessary gap between courtyards.

If the assembly shop does not require a manufacturing allowance, the PCB designer can place the courtyards so that they touch, but

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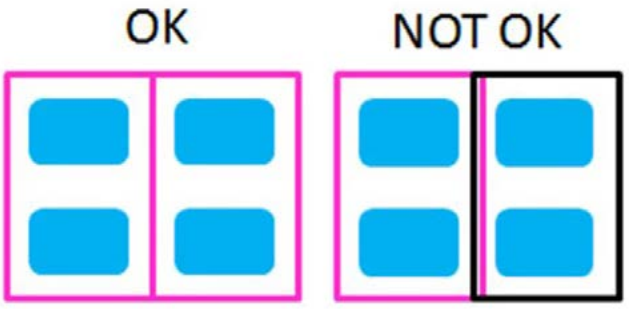

Figure 8: Courtyards should touch, but not overlap.

not overlap as shown in Figure 8. Crowding and overlapping courtyards can lead to solder bridging during assembly.

Part Placement and Alignment

In the 1980s, assembly shops preferred all polarized parts should be pointed in the same direction. With today's technology, that is no longer necessary; however, aligning parts in neat rows will add aesthetic value to the final PCB. And if you're selling boards on the open market, consumers will naturally choose the prettiest board. Also, nicely ordered parts are better for signal routing and use of space.

Footprint Origins

Components come packaged in tape and reel, tubes and trays. The pick-and-place machines pick up the component at the center of gravity. When PCB designers put the origin of the PCB library part in the center, they are aiding the assembly shop. However, some component packages have irregular shapes and the center is difficult to determine. And for PCB design layout routing, through-hole connector pins might need to fall on a grid pattern and making Pin 1 the origin optimizes signal routing. A centric origin marker helps the PCB designer identify the location of the footprint origin. However, some CAD tools auto-generate an origin marker in the software and in that case there is no need to add an additional origin marker in the PCB library part.

Assembly Rails or Frames

The assembly shop needs the board edge to clamp onto while the board travels through the pick -and-place machines and the solder reflow oven. If the PCB designer places components close to the board edge due to high density part placement, then a breakaway panel must be added to aid the assembly line. The breakaway tab could also contain the

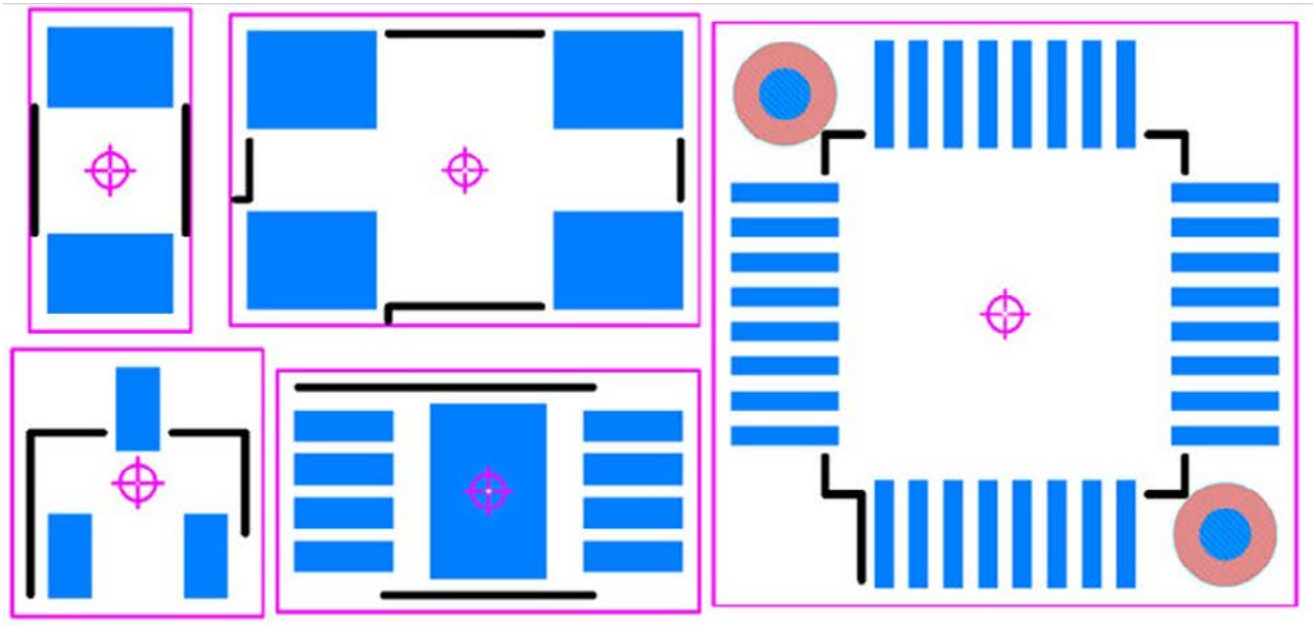

Figure 9: Centric origin markers may be auto-generated by EDA tools or added by the designer.

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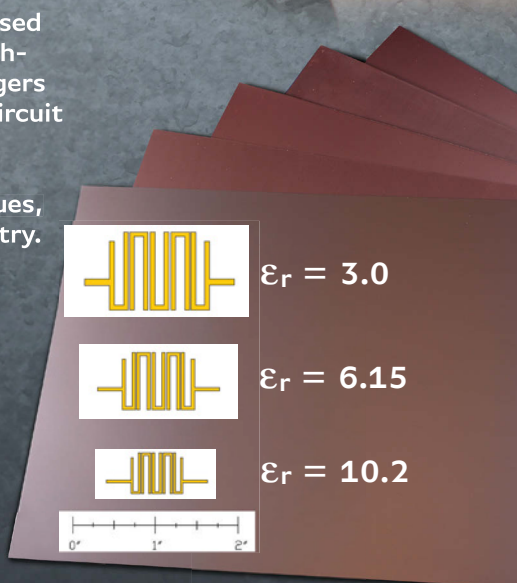

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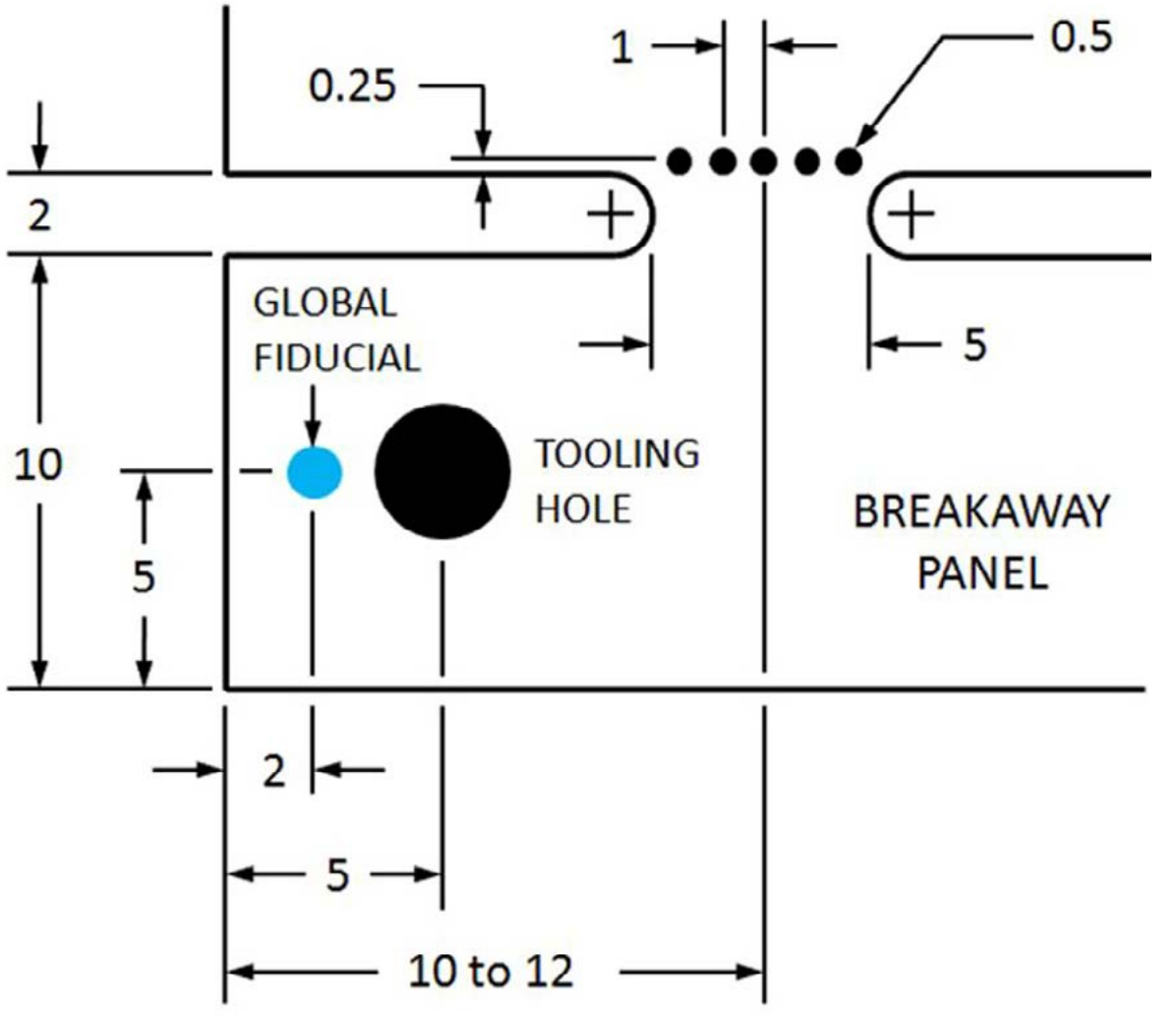

Figure 10: Breakaway tab with global fiducials and tooling holes.

global fiducials and tooling holes as shown in Figure 10.

When the board is completely assembled the breakaway tabs must be removed. There are two methods of separating the breakaway tabs. The first and most popular method is the use of routing and mouse bites as shown in Figure 11. The trace routing must be at least 1 mm away from the finished board edge and the mouse bites. And components should be located at least 2 mm away from the routed edge and mouse bite holes as shown in Figure 12.

The other process of separating the breakaway panel is V-scoring, as shown in Figure 13.

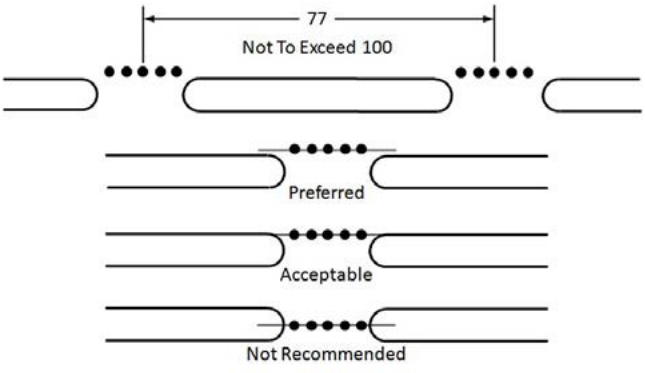

Figure 11: Not recommended: routing and mouse bites.

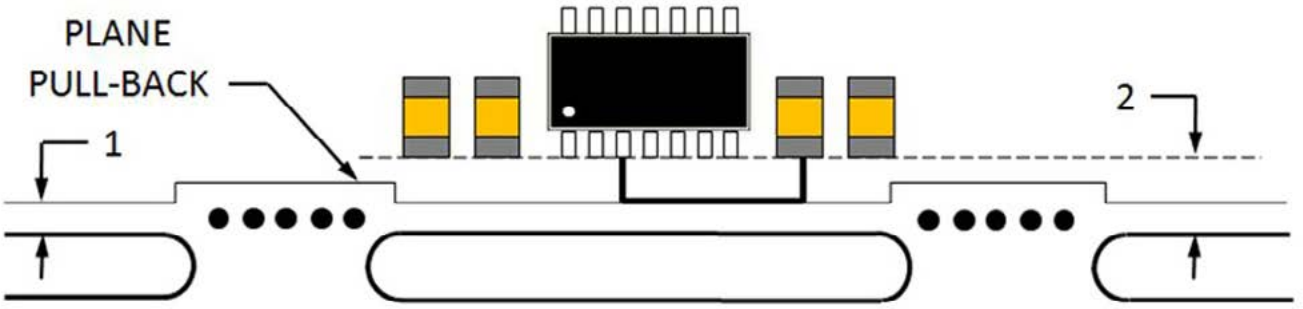

Figure 12: Components are at least 2 mm away from routed edge and mouse bite holes.

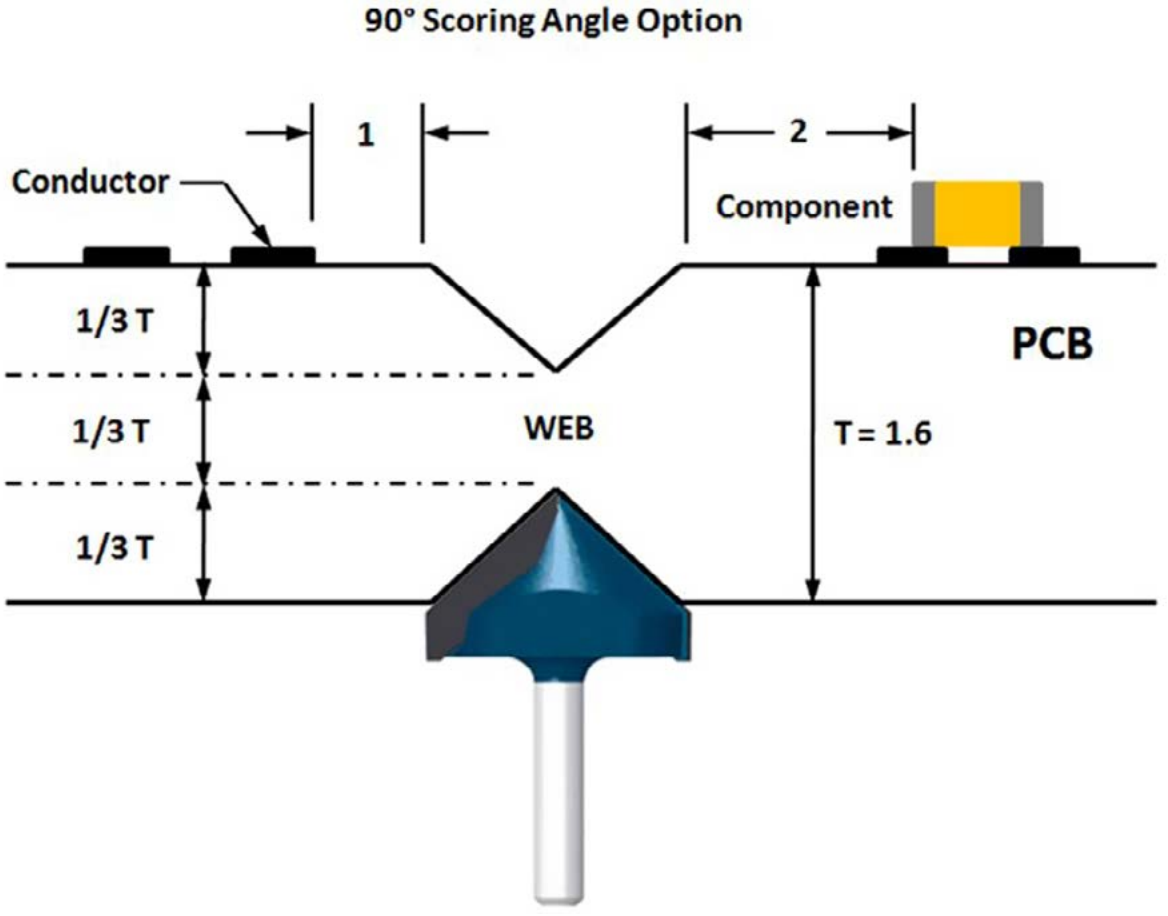

Figure 13: V-scoring is an alternative method for separating breakaway panels.

Some PCB designers like to ensure that the breakaway tabs are secure and won't breakaway during handling. In this case, the PCB designer will add a frame around the entire PCB design and use mouse bites and routing channels. Adding a frame reduces the number of boards you can get on a panel but it does add rigidity to the individual board to ensure the breakaway tabs do not prematurely break away during assembly handling.

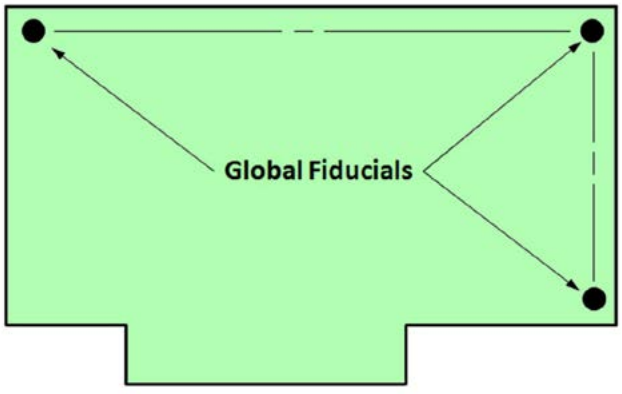

Figure 14: Global fiducials register the board for placement accuracy.

Global and Local Fiducials

Global fiducials are a must for the pick-and-place machine to optically bombsite the fiducial locations and register the board for machine placement accuracy as shown in Figure 14.

Local fiducials are used for fine-pitch QFP components when the pin pitch is less than 0.625 mm and BGA components when the pin pitch is less than 0.8 mm as shown in Figure 15. With today's modern equipment, many assembly shops do not require local fiducials; however, they might come in handy for repair/replacement. **PCBDESIGN**

Part 2 of this article will continue in the November issue of The PCB Design Magazine.

Tom Hausherr CID+, CIT, is founder and CEO of PCB Libraries Inc. To contact him or read his past columns at PCBDesign007, click here.

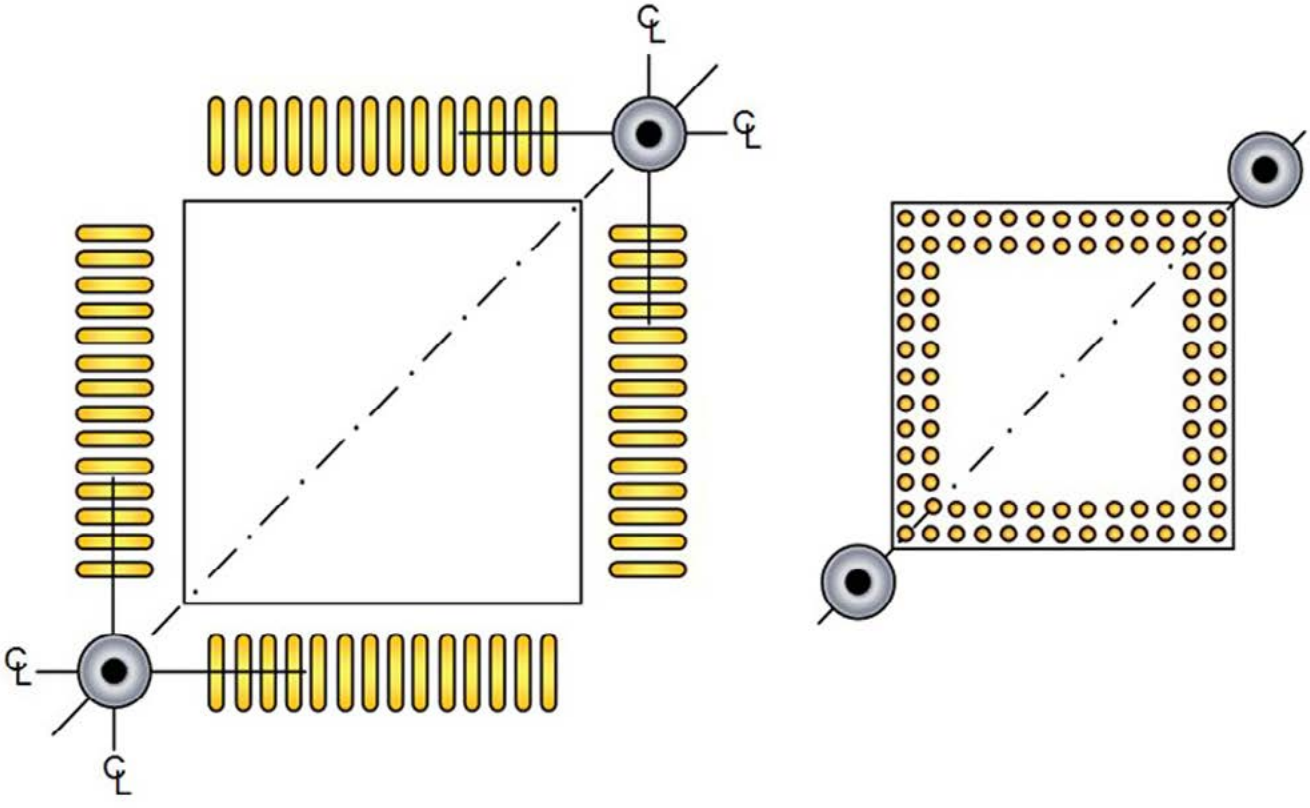

Figure 15: Local fiductials are not always required. But they may come in handy for repair work.

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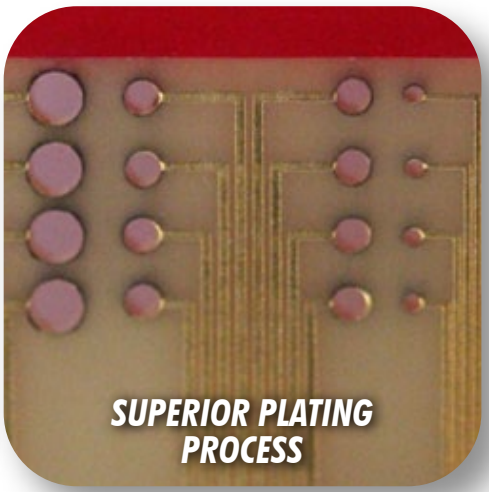

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Impedance Matching: Terminations

by Barry Olney
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The impedance of the trace is extremely important, as any mismatch along the transmission path will result in a reduction in signal quality and possibly the radiation of noise. Mismatched impedance causes signals to reflect back and forth along the lines, which causes ringing at the load (Figure 1). The ringing reduces the dynamic range of the receiver, eats into the noise budget and can cause false triggering.

Reflections occur whenever the impedance of the transmission line changes along its length. This can be caused by unmatched drivers/loads, layer transitions, different dielectric materials, stubs, vias, connectors and IC packages. By understanding the causes of these reflections and eliminating the source of the mismatch, a design can be engineered with reliable performance. For perfect transfer of energy and to eliminate reflections, the impedance of the source must equal the impedance of the trace, as well as the impedance of the load. When the signal path has an impedance discontinuity, place a terminator at the point of line discontinuity to equalize the impedance.

Everyone would agree that the signal at the load in Figure 1 is not pretty and obviously has an impedance mismatch that needs to be addressed. But when should a transmission line be terminated and how?

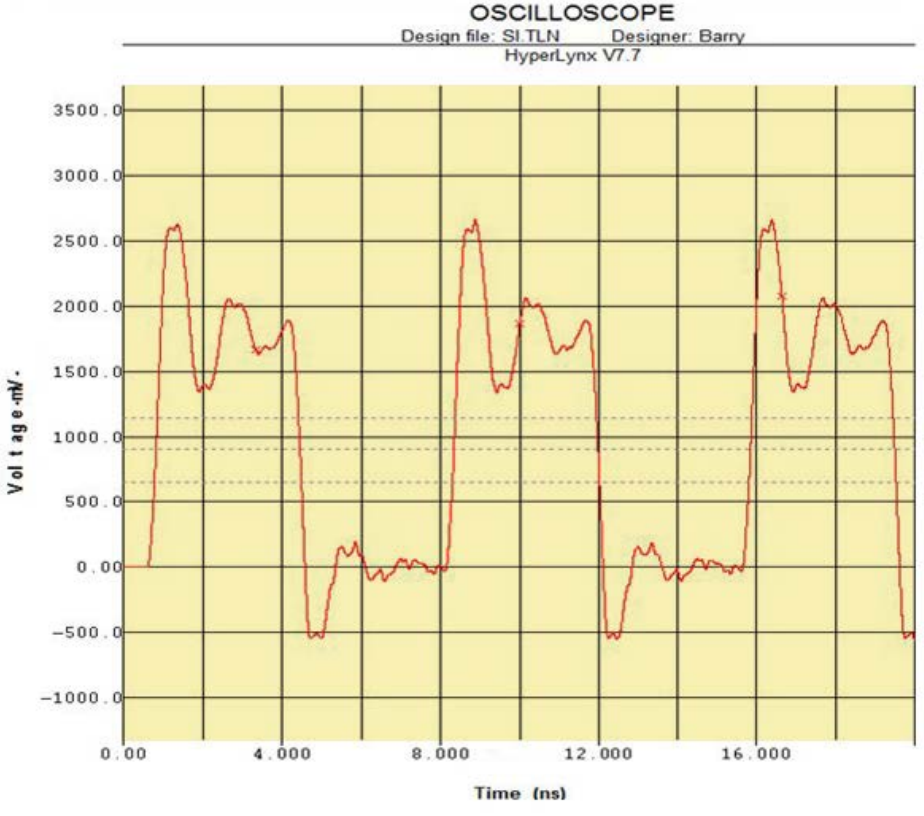

Figure 1: Unterminated 1.5 inch (38 mm) transmission line shown in HyperLynx.

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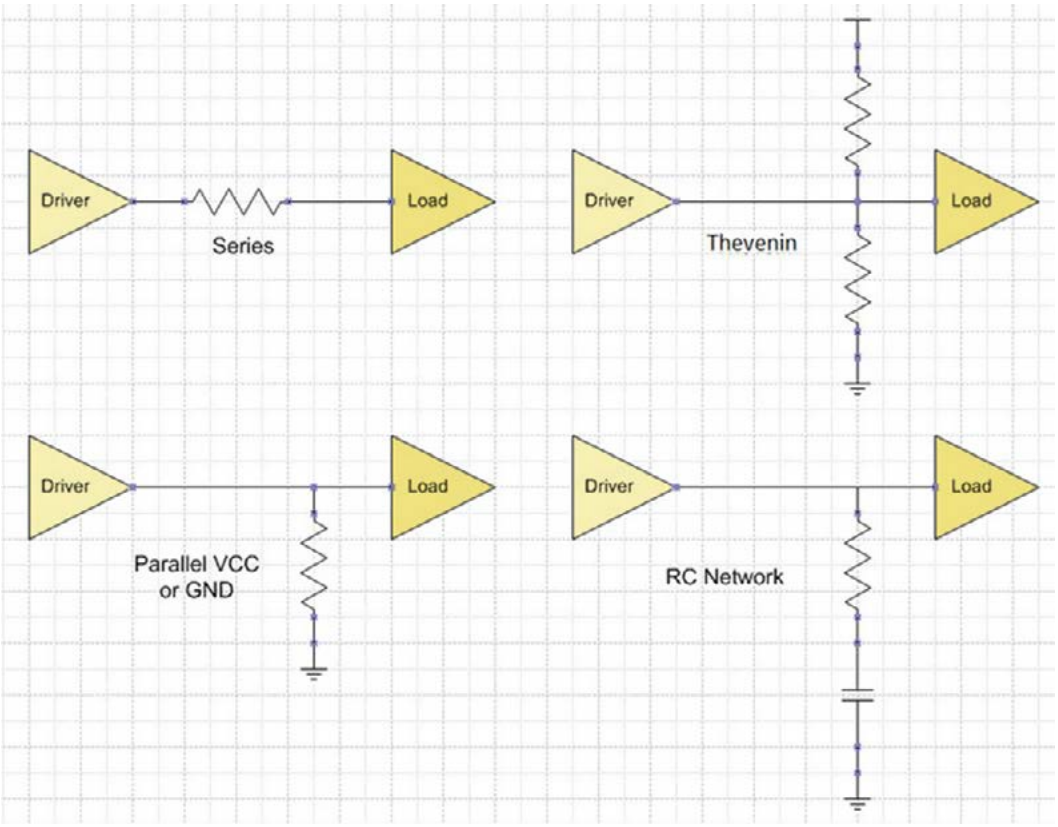


Figure 2: Termination strategies.

As signal rise times increase, consideration should be given to the propagation time and reflections of a routed trace. If the propagation time and reflection from source to load are longer than the edge transition time, an *electrically long trace* will exist. If the transmission line is short, reflections still occur but will be overwhelmed by the rising or falling edge and may not pose a problem. But even if the trace is short, termination may still be required if the load is capacitive or highly inductive to prevent ringing. Generally when the trace length exceeds one sixth of the electrical length of the rising edge rate, then termination is required.

For a driver signal with a 1 ns rise time, since the speed of a signal in FR-4 is approximately 6in/ns (150 mm/ns) then an unterminated trace can only be 6 x 1/6 = 1.0 inches (25 mm).

This brings us to the rule of thumb: All drivers whose trace length (in inches) is equal to or greater than the rise time (in nanoseconds) must have provision for termination. The easiest way to terminate is to use a resistive element. Termination can be made at the source or at the load.

Different terminating methods have advantages and disadvantages for different applications but in general:

1. Series is excellent for point to point routes, one load per net. It works well for traces that are electrically short and is used to fanout multiple loads radially from a common source—star routed—without affecting other circuits in the network. Series termination reduces ringing and ground bounce. Series is the most used termination for high speed design.
2. Parallel is preferred for busses.
3. Thevenin is commonly used for driving logic busses also.
4. RC networks provide good signal quality but are not good for high frequencies or long trace lengths.
5. Diode networks are used to limit overshoot but do not affect trace impedance or reduce reflections and the clamping diodes are generally on the IC inputs.

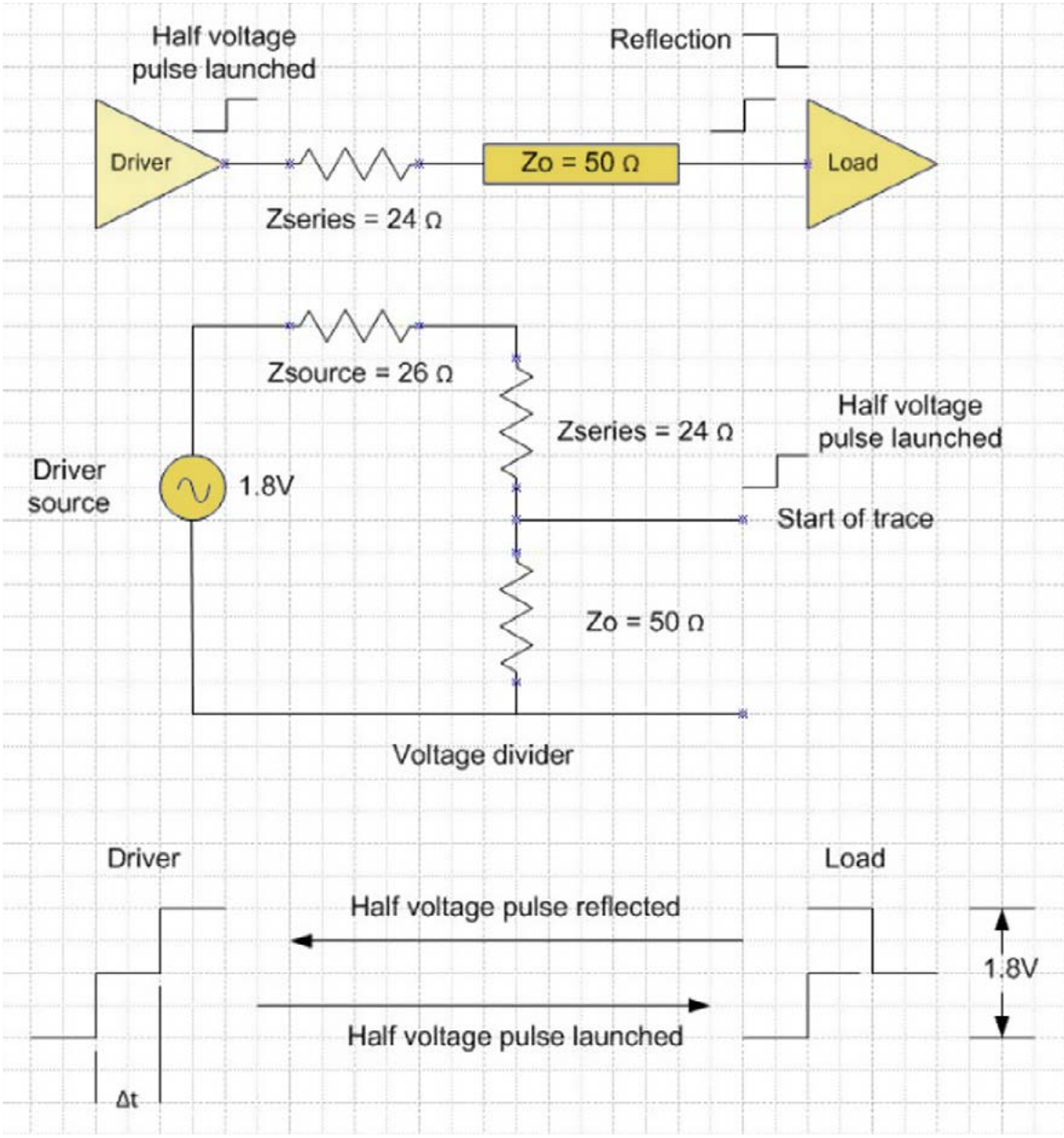


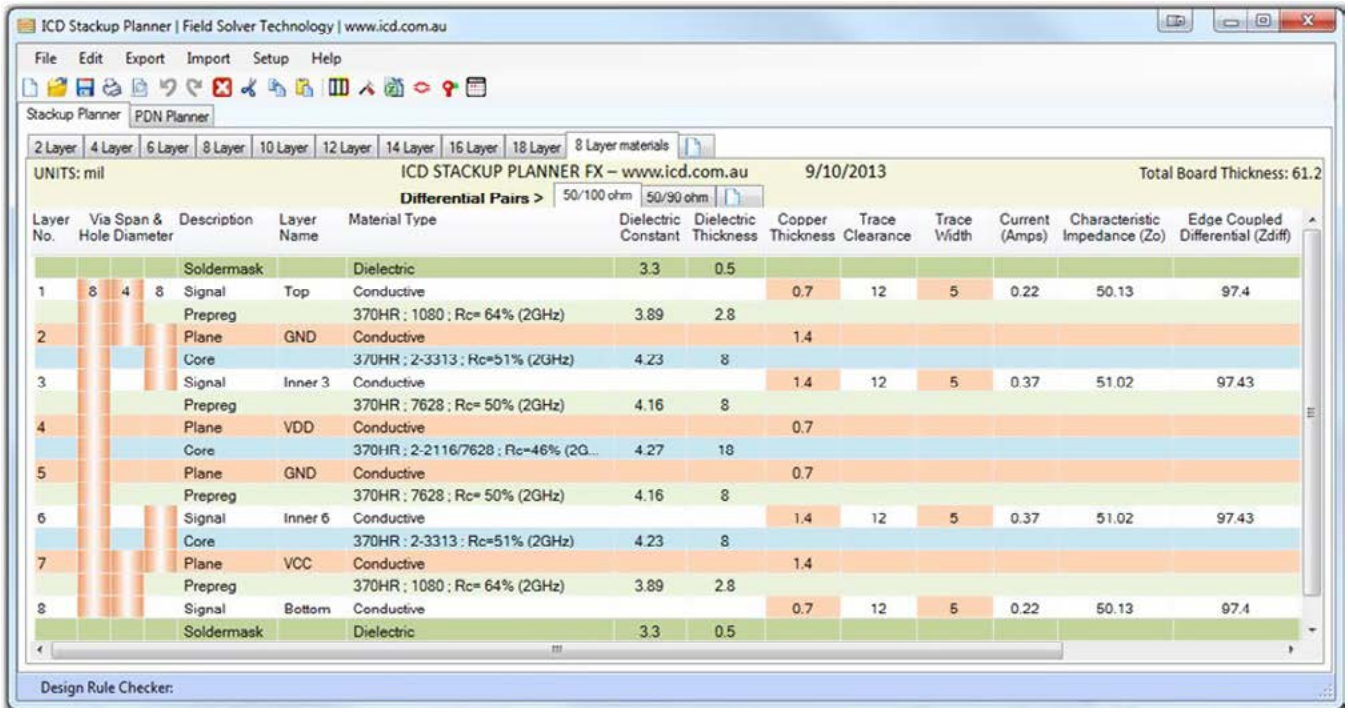
Figure 3: Impedance backmatching.

How Backmatching Works

For a point to point topology, the most common method of impedance termination is to use a series resistor close to the driver. The sum of the series resistor and the source impedance should equal the transmission line impedance.

Impedance backmatching slows down the rise and fall times and reduces the ringing (over- and undershoot) of clock drivers. A half voltage pulse is launched from the source due to the voltage divider network formed by the source impedance, series terminator and the transmission line. As this half voltage pulse reaches the load, it is instantaneously reflected back along the trace. This reflected pulse adds to the initial pulse to form a full voltage square wave—so we get the signal we want at the load.

The reflected pulse travels back to the source. When it reaches the series terminator it sees the series resistor (24 Ω) plus the source impedance



Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)
		Soldermask		Dielectric	3.3	0.5						
1	8 4 8	Signal	Top	Conductive			0.7	12	5	0.22	50.13	97.4
		Prepreg		370HR ; 1080 ; Rc= 64% (2GHz)	3.89	2.8						
2		Plane	GND	Conductive			1.4					
		Core		370HR ; 2-3313 ; Rc=51% (2GHz)	4.23	8						
3		Signal	Inner 3	Conductive			1.4	12	5	0.37	51.02	97.43
		Prepreg		370HR ; 7628 ; Rc= 50% (2GHz)	4.16	8						
4		Plane	VDD	Conductive			0.7					
		Core		370HR ; 2-2116/7628 ; Rc=46% (2G...	4.27	18						
5		Plane	GND	Conductive			0.7					
		Prepreg		370HR ; 7628 ; Rc= 50% (2GHz)	4.16	8						
6		Signal	Inner 6	Conductive			1.4	12	5	0.37	51.02	97.43
		Core		370HR ; 2-3313 ; Rc=51% (2GHz)	4.23	8						
7		Plane	VCC	Conductive			1.4					
		Prepreg		370HR ; 1080 ; Rc= 64% (2GHz)	3.89	2.8						
8		Signal	Bottom	Conductive			0.7	12	5	0.22	50.13	97.4
		Soldermask		Dielectric	3.3	0.5						

Figure 4: ICD Stackup Planner simulates the trace impedance.

(26 Ω) totaling 50 Ω. Since the transmission line is also 50 Ω, there is no discontinuity of impedance and therefore there will be no reflection. The signal will be absorbed by the terminating resistor and the source impedance preventing further ringing.

But how do you know the impedance of the driver and the transmission line? First of all, an accurate field solver, such as the ICD Stackup Planner shown in Figure 4, is required to determine the impedance of the PCB traces. Then the source impedance must be extracted from the IBIS model. Subtracting the source impedance from the trace characteristic impedance gives the required series terminator value.

Extracting the Source Impedance from the IBIS Model

IBIS stands for Input/Output Buffer Information Specification and is controlled by the IBIS Open Forum organization (www.vhdl.org/ibis). The organization also provides IBIS "Golden" Parser to validate developed models. IBIS is a device modeling technique used in simulation to provide a simple table based; non-proprietary buffer model derived from a real semi-conductor device. Note that the IBIS model does not require circuitry beyond the immediate interface. IBIS models do not reflect the product's interior logic and interactions so chip manufacturers are happy to provide them.

IBIS models can be used to characterize I/V output curves, rising/falling waveforms and pin parasitics of the device packaging. Although models impedance should really be based on the I/V curves, there is a quick way to calculate the source impedance that gives results to approximately 1 ohm.

The format of the IBIS model starts with a header, which is manually created and includes a description of the relevant IC. Following this is general information about the model, including origination date, model source, and user notes. The "notes" section contains details of the model creation, along with the basic format of the digital buffers.

The model header is followed by detailed information about the package for the products, including values for pin resistance, inductance, and capacitance. The core of the IBIS model follows with I-V and V-t tables buffer by buffer.

The pin impedance of any signal consists of the package inductance and capacitance added to the model's impedance. Shown below, the keywords "[Component]," "[Manufacturer]," and "[Package]" describe a specific package of DDR2 (model u47a.ibs available from www.micron.com).

```
| u47a.ibs * IBIS 4.0 Model
| 512Mb DDR-2 SDRAM - Die Revision „F“
| This Model is valid for Commercial Temperature Range 0C<=Ta< 85C
|
| Valid for DDR2-400/533/667/800 operation
| ***************************************************************************************************************************
| COMPONENT: MT47H128M4CF (60-Ball FBGA, x4)
| ***************************************************************************************************************************
[Component]   MT47H128M4CF
[Package Model] u47a_60ball_pkg
[Manufacturer]  Micron Technology,Inc.
[Package]       | 8mm x 10mm FBGA
|
|               typ             min             max
R_pkg           178.3m          116.4m          273.6m
L_pkg       1.88nH              1.15nH          2.94nH
C_pkg           0.32pF          0.21pF      0.50pF
|
```

The package inductance and capacitance for specific pins can be found under the "[Pin]" keyword.

```
[Pin]  signal_name   model_name    R_pin      L_pin      C_pin
C2     DQ1           DQ            202.0m   2.06nH    0.36pF
```

The second capacitance value of interest is the silicon capacitance, C_comp. The C_comp values can be found under the "[Model]" keyword

```
|
|***************************************************************************************************************************
| MODEL DQFULL_533 (Full-Drv IO Drvr with no ODT, 400/533)
|***************************************************************************************************************************
|
[Model]       DQFULL_533
Model_type    I/O
|
Vinl = 650.000mV
Vinh = 1.150V
Vmeas = 900.000mV
Vref = 900.000mV
Cref = 0.0pF
Rref = 25.000 Ohm
|
|                   typ             min             max
C_comp              2.65pF          2.50pF          2.80pF
```

The basic equation for impedance is: $$Z = \sqrt{\frac{L}{C}}$$

Expanding this equation, by adding the component capacitance and the pin capacitance—which are in parallel—the following equation defines the characteristic impedance of the IBIS model pins:

So for this DDR2, pin DQ1

$$Zsource = \sqrt{\frac{L\_pin}{C\_pin + C\_comp}} \qquad Zsource = \sqrt{\frac{2.06nH}{0.36pF + 2.65pF}}$$

$$Zsource = \sqrt{684.39} = 26.16 \text{ ohms}$$

For a 50 ohm transmission line:

$$Zseries = Zo - Zsource$$

$$Zseries = 50 - 26.16 = 23.84\ ohms$$

IMPEDANCE MATCHING: TERMINATIONS *continues*

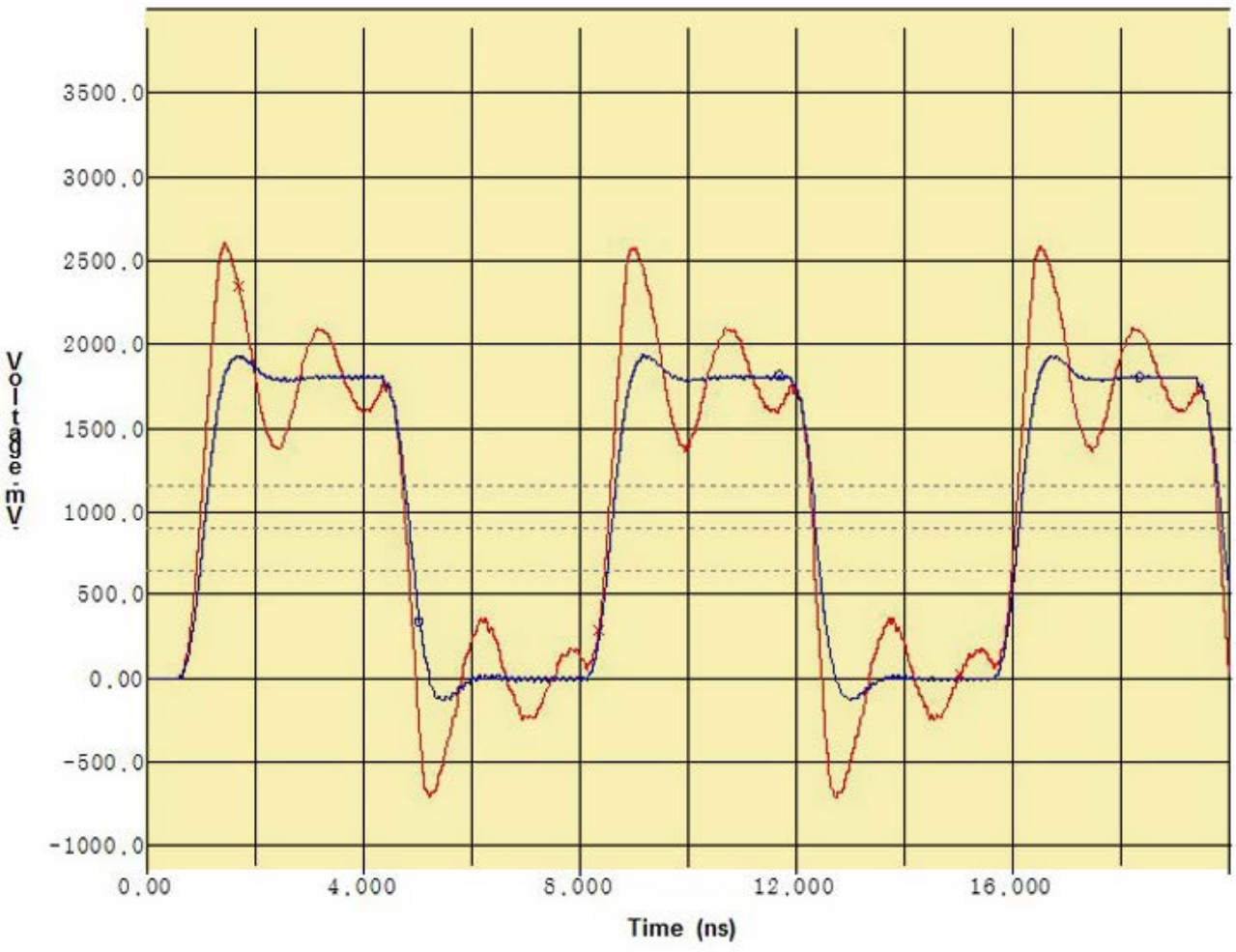


Figure 5: Ringing is reduced dramatically by adding a series terminator.

The above example is driving the data back from the DDR2 memory to the processor. The same calculation needs to be done for the processor model to extract the impedance for data travelling in the other direction, but it should be much the same. Figure 5 shows the reduction in ringing due to the series terminator.

Also note that the DQFULL_533 model was used. This is the full drive strength @ 533Mbps with no on-die termination (ODT). There are also models for ODT of 50, 75 and 150 ohms @ 533Mbps and 667/800Mbps with full and reduced drive strength.

Instead of having the necessary resistive termination located on the PCB, the ODT is located within the IC. Although the termination resistors on the motherboard reduce reflections on the signal lines and are used for individual, board mounted, memory, they are unable to prevent reflections resulting from the stub lines that connect to the components on a DRAM Module. A signal propagating from the processor to the components encounters an impedance discontinuity at the stub leading to the components on the module. The signal that propagates along the stub to the component will be reflected back onto the signal line, thereby introducing unwanted noise into the signal. ODT fixes this.

Impedance matching slows down the rise and fall times, reduces the ringing (over/under shoot) of clock drivers and enhances the signal integrity of a high-speed design.

Points to Remember

- Mismatched impedance causes signals to reflect back and forth along the lines, which causes ringing at the load
- For perfect transfer of energy and to eliminate reflections, the impedance of the source must equal the impedance of the trace, as well as the impedance of the load
- When the trace length exceeds one sixth of the electrical length of the rising edge rate, then termination is required
- All drivers, whose trace length (in inches) is equal to or greater than the rise time (in ns), must have provision for termination
- The most common method of impedance termination is to use a series resistor close to the driver
- Impedance backmatching slows down the rise and fall times and reduces the ringing (over/under shoot) of clock drivers
- The source impedance can be extracted from the IBIS model of the device
- The series terminator should equal the characteristic impedance of the transmission line less the source impedance
- DRAM modules require internal ODT to account for stubs on the DIMM **PCBDESIGN**

References

- Beyond Design, Barry Olney:

Intro to Board-Level Simulation and the PCB Design Process

Board Level Simulation and the Design Process: Plan B: Post Layout Simulation

- Practical Signal Integrity
- The IBIS Model Part 3, by Texas Instruments' Bonnie Baker
- Signal and Power integrity Simplified, by Eric Bogatin
- High-Speed Digital Design, by Howard Johnson
- The ICD Stackup and PDN Planner, available at www.icd.com.au

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. ICD is a PCB design service bureau and specializing in board-level simulation. The company developed the ICD Stackup Planner and the ICD PDN Planner software. To read past columns or contact Olney, click here.

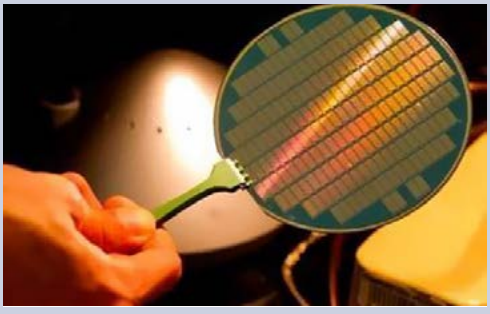
Tiny Computer with Carbon Nanotube Transistors

With support from the National Science Foundation (NSF), a team of Stanford University engineers has for the first time built a tiny computer with 178 transistors made from carbon nanotubes, a semiconductor material that may replace silicon in computer chips. This change could launch a new generation of electronic devices that are smaller, cheaper, faster and more energy-efficient.

The achievement, which culminates years of effort by scientists around the world, is detailed in the cover story of the journal Nature. The research is led by Stanford professors Subhasish Mitra and H.S. Philip Wong.

"People have been talking about a new era of carbon nanotube electronics moving beyond silicon," said Mitra, an electrical engineer and computer scientist at Stanford. "But there have been few demonstrations of complete digital systems using this exciting technology. Here is the proof."

"This paper details a most significant nano-enabled integrated system with nanotubes that can perform a general set of computer programs proposed to replace the current transistor technology," said Roco.



"They have designed what is called a 'Turing complete' computer," explained NSF Computer Information Science and Engineering program manager Sankar Basu, who managed the funding for this project.

"This is an important scientific and engineering breakthrough," Basu and Roco agree.

PCB007 News Highlights

TTM Technologies Closes China MAS Plant

The company will cease operations and lay off approximately 600 employees at its Suzhou, China facility at or near the end of September 2013. TTM intends to transfer PCB production at MAS to one or more of its other facilities in China, providing an uninterrupted supply of PCBs to customers.

IPC: N.A. PCB Sales & Orders Trending Upward

Although still not quite in positive territory, YoY sales growth has been improving steadily over the past three months, bolstered by solid growth in orders since the beginning of 2013. Most of the improvements in July's results are due to the strong performance of the rigid PCB segment.

MFLEX Reports 20% Q3 Decline in Net Sales

"We believe our third quarter results will serve as an inflection point as we anticipate a meaningful sequential improvement in revenue in the fourth quarter with continued momentum into fiscal 2014…we expect to return to profitability in the first quarter of fiscal 2014, as well as on a full year basis in fiscal 2014," said Reza Meshgin, CEO.

Global PCB Market's CAGR to Grow 7.8% in 2012-2016

The analysts forecast the global PCB market to grow at a CAGR of 7.8% over the period 2012–2016. One of the key factors contributing to this market growth is the increasing adoption of smartphones and tablet PCs.

EMS & PCB Marketplace the Highlight of productronica 2013

ZVEI is organizing a series of technical lectures as part of a Highlight Day on November 13. Experts from the EMS sector will discuss "Silver Bullet: Development, Engineering, Manufacturing and Mechatronics from a Single Source: Are (Successful) EMS Providers becoming System Integrators?"

Wurth Elektronik Expands in China; Opens New Office

The company has been in Asia for over 13 years, where it has established several local businesses, manufacturing facilities, and its own quality and design center. With this move, the company is not only expanding its business area, but minimizing customer risk because it remains a partner throughout a product's life cycle.

Sunstone Circuits Upgrades PCB123; Launches New Version

The company has launched the newest version of their PCB design tool, PCB123, which includes two major upgrades to functionality: tools to create slots and cutouts and file-specific hole sizes. With the new version 5, PCB123 users can now create plated slots as small as 0.025" and as large as 0.250".

PCB Solutions Completes Complex Build for Nokia

Nokia contacted PCB Solutions in the early spring of 2013 by requesting a quote for the manufacturing and assembly of a very difficult PCB assembly requiring, but not limited to, controlled impedance, "crossed" or "surface controlled" blind and buried vias, copper filled vias under BGA pads for multiple layers and very tight trace and space requirements.

GUH: PCB Shipments Increase as Global Demand Rises

GUH Holdings Bhd managing director Datuk Kenneth H'ng said the group was seeing orders coming in for the third quarter of 2013, compared to a sluggish first and second quarter.

Cicor Reports 11.7% Sales Increase in 1H

The group's business volume grew by 12% compared with the first, weaker half of 2012 and by 3% compared with the good second half of 2012. While this growth is evidence of the growing demand for outsourcing services and high-tech manufacturing technologies, it is also the result of investments Cicor made in 2012.

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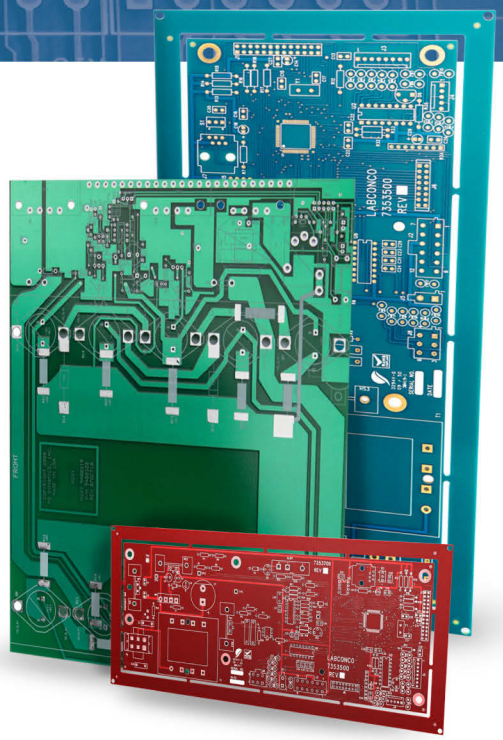

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Cable Quality Matters

by Istvan Novak
ORACLE

In my August column, we looked at the importance of properly terminating the cables that connect a measuring instrument to our device under test. We may be surprised to learn that even if we use the correct termination at the end of the cable, the measured waveform may depend on the quality of the cable we use.

To illustrate the point, we will use the same DC-DC converter evaluation board with an LTM4604 buck converter. To eliminate any possibility of ground loops, the converter is powered from a small battery pack with three AA batteries. The load is a small incandescent bulb, taking approximately 1A DC current from the output. We use a 50-ohm coaxial cable with BNC connectors at both ends. One end of the cable is connected to CH1 input of a Tektronix TDS540B oscilloscope. The input is switched to 50-ohm input impedance. The other end of the cable is connected to the BNC socket on the evaluation board, which directly monitors the output voltage. The setup is shown in Figure 1.

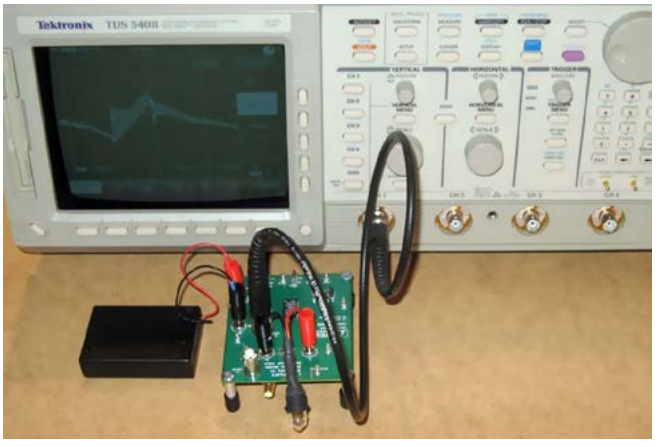

Figure 1: A DC-DC converter evaluation module is connected to an oscilloscope input with a BNC-BNC coaxial cable.

In Figure 1, you can see the output ripple waveform, which also shows the ringing when we do not terminate the cable at the oscilloscope. Figure 2 shows the ripple waveform when the cable is properly terminated.

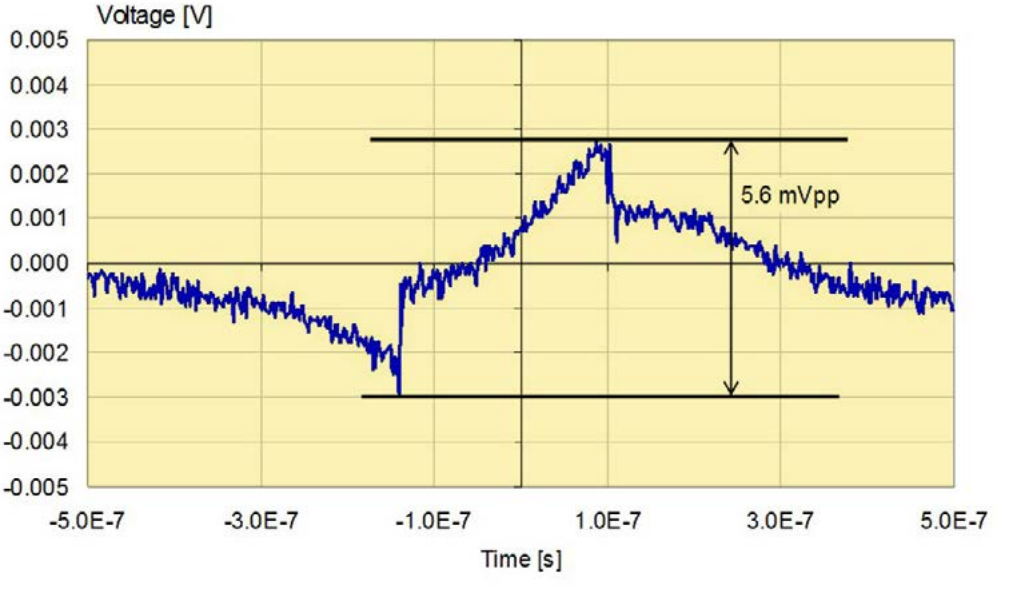

Figure 2: Switching ripple measured with the cable shown in Figure 1. The cable is terminated in 50 ohms.

The single period shown on the plot has an output ripple of 5.6 mVpp. We can also zoom on the edges to check for additional ringing. Figure 3 shows the ringing on the falling edge, at the moment when the high-side FET turns off.

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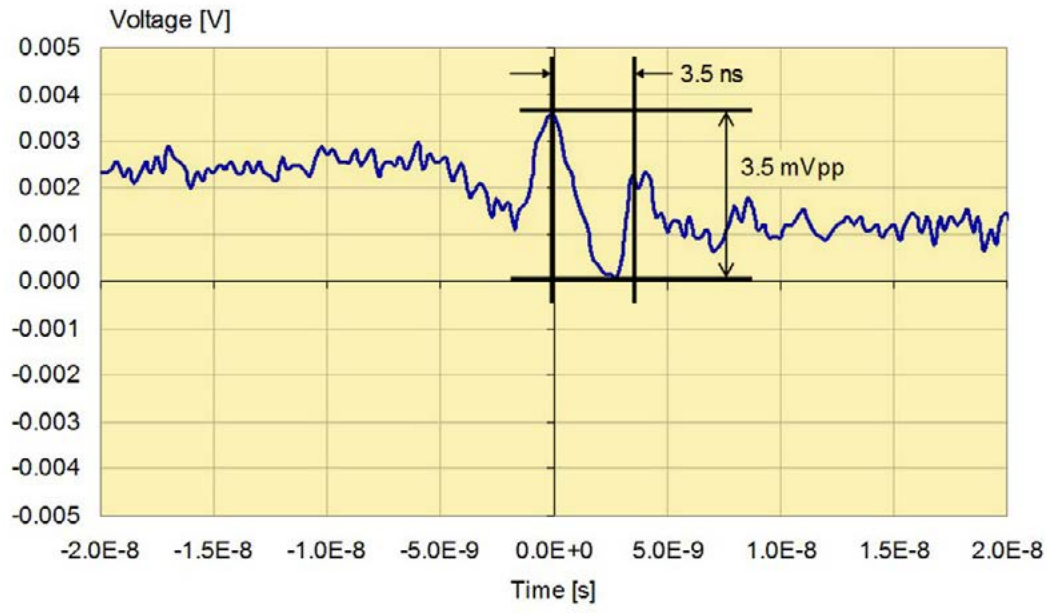


Figure 3: Waveform zoomed around the turn-off time: There is a 3.5 mVpp 3.5 ns period ringing on the falling edge.

Now we change the cable and use a smaller diameter RG178 coaxial cable. The setup is shown in Figure 4.

Note that the DUT and oscilloscope settings are left exactly the same as before. The full-period waveform is shown in Figure 5. The waveform looks very similar to what we saw in Figure 2. The measured peak-to-peak output ripple is 5.3 mV, which is 5% lower than what we measured before. Since we measure just a few millivolts and use no bandwidth limiting or averaging, this difference can be easily explained by the trace noise.

As a result, if we re-measure these plots, the peak-to-peak values will vary by a few percent. More alarming is the difference if we zoom on the turn-off edge. The waveform is shown in Figure 6. We do see a ringing similar to the one seen in Figure 3, but its peak-to-peak value is now 16% lower and the ringing signature is almost masked out by noise.

Figure 4: Setup with an RG178 50-ohm coaxial cable.

Why do we get different results with different cables? A simple test gives us the clue. We can measure the residual reading in the same exact setup, with the two different cables, when the DUT is not working. The cables are still connected at both ends, the oscilloscope end of the cable having terminated in 50 ohms by the oscilloscope input.

The residual noise reading with the two cables is shown in Figure 7, where both oscilloscope output traces were copied into the same plot. We get the blue trace with the cable used for Figures 1 through 3, and get the red trace with the cable we used for Figures 4 through 6. The difference between the two traces is the noise pickup of the cable through its shield braid from the air. Both cables have braided shield, with single-braid coverage. I bought the first cable from a well-respected cable vendor. The second cable came from an unknown manufacturer as a cheap alternative.

At first it may be surprising that we saw the correct DUT signature with the second cable, when, just from the air, it picks up a bigger signal than what we wanted to measure: The peak-to-peak signal level of the red trace is 8.5

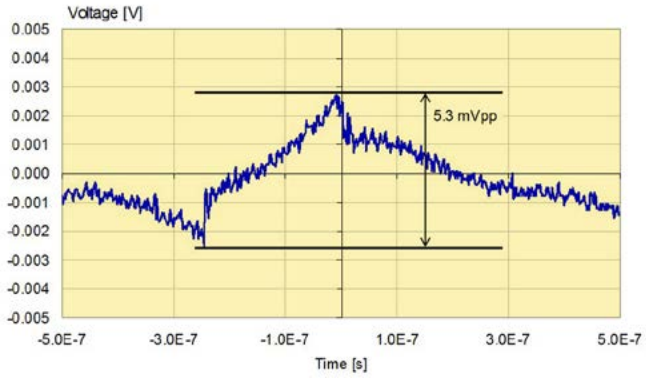


Figure 5: Switching ripple measured with the cable shown in Figure 4. The cable is terminated in 50 ohms.

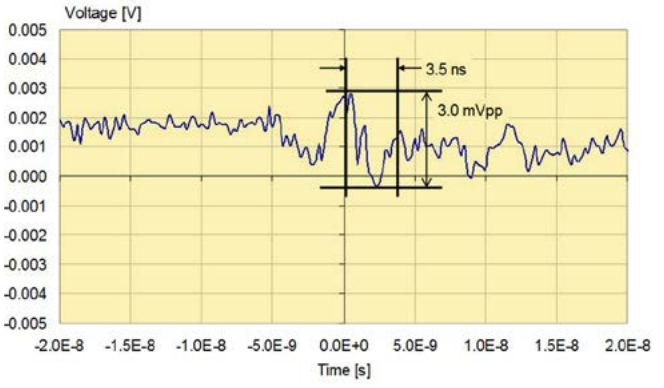


Figure 6: Waveform of Figure 5 zoomed around the turn-off time. A very noisy 3.0 mVpp 3.5 ns period ringing is seen.

mV, bigger than the output ripple of the converter. The reason why we still saw the correct signature, though distorted, in Figures 5 and 6, is that the noise is asynchronous to the measured DUT signal. The noise does not have the same repetition frequency as the DUT switching, so when we measure with a real-time oscilloscope, the degree of noise contamination depends on the timing between the noise and our DUT signal. If we are lucky, we may get little distortion, but if the noise peak lines up in time with the data set we capture from our DUT, it may completely mask out our signal.

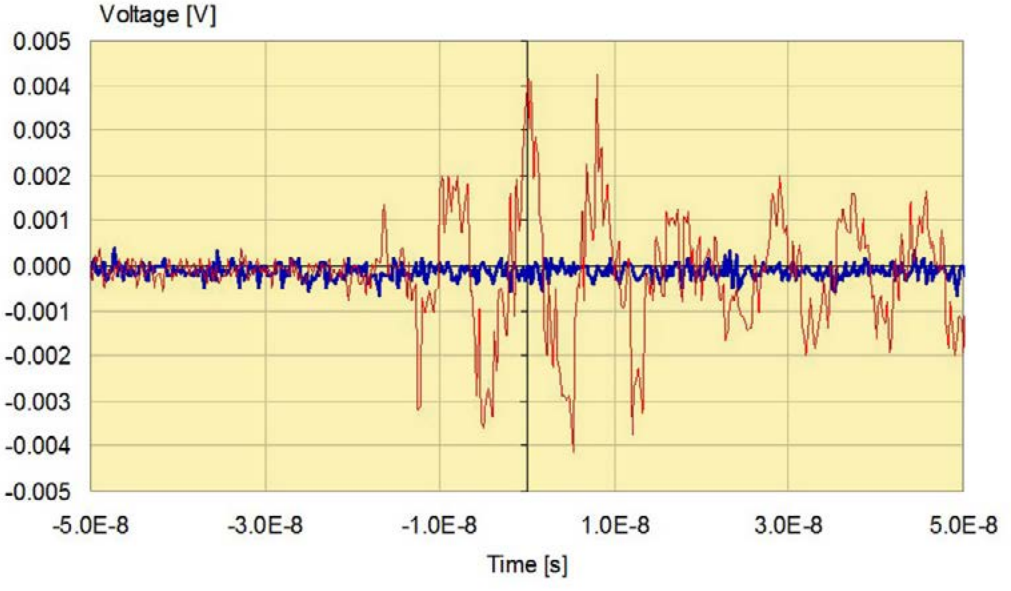


Figure 7: Voltage measured with two different cables at the DUT BNC connector, with the DUT turned off.

In a future column, we will show the construction of these cables and look at various options to check the quality of the cable shield. Until then: be aware of cheap cables, especially when you need to measure a few millivolts of PDN voltage in a noisy lab. **PCBDESIGN**

Dr. Istvan Novak is a distinguished engineer at Oracle, working on signal and power integrity designs of mid-range servers and new technology developments. With 25 patents to his name, Novak is co-author of "Frequency-Domain Characterization of Power Distribution Networks." To contact Novak, click here.

Component Placement

by Jack Olson, CID+

Mechanical Constraints

In your CAD system, you may have an infinite amount of space to put things. But in an actual product, your area is going to be limited by constraints that most board designers have very little control over. Unless you're a one-man operation designing your own products, you'll probably have to fit your circuitry into a pre-defined area. At a minimum, this will be a board outline that will represent the final board size.

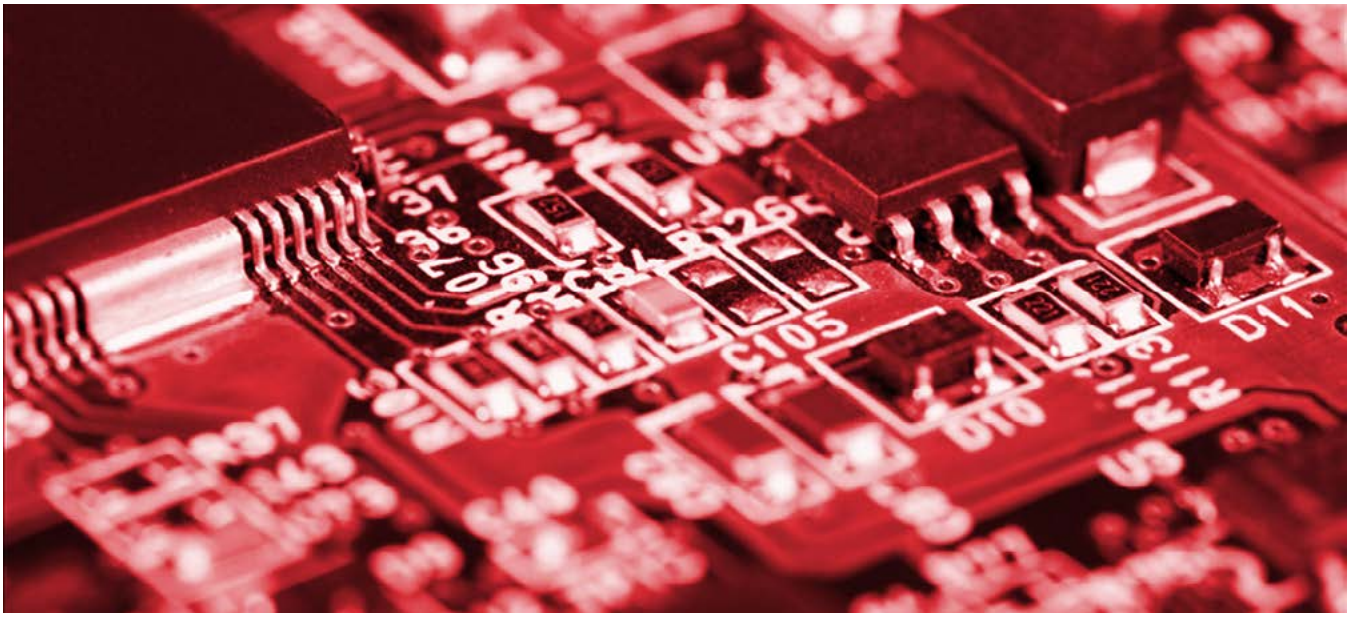
Once the board shape is defined, you will have to make provisions for how the assembled board will be mounted. The most common method is to add mounting holes that are the appropriate diameter for screws, and you should place these first. Find out how much clearance area may be needed around them for mounting bosses, assembly tools, etc., and add clearance areas or "keep-out zones" if possible. You may also need to provide clearance for card guides, card ejectors, etc. If your CAD system supports some type of data transfer to and from the mechanical design software (IDF format, for example), it's a good idea to verify the board size and mounting configuration, and then lock it down to prevent accidental changes later on.

Next, some components may have predefined locations. Connectors might have to be placed with a specific orientation to mate with other parts of the system. Switches, displays, indicators, LEDs, variable components and some types of test points may need to be placed for accessibility. All components with predefined locations should be placed first.

Manufacturing Considerations

By this time, you should be getting an idea about whether your design will be single-sided or double-sided. Will all of the components fit on one side? If so, assembly costs will be lower. Is the board large enough to be conveyorized in the assembly process? If so, you will need to keep components away from the conveyor rails, which usually hold the two longest sides of the board, using about 3 mm of the board edge. Keep components at least 4 mm away from the sides, if possible.

If this is not possible, additional rails or fixturing might be required for assembly. If



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COMPONENT PLACEMENT *continues*

the boards are small, they will probably be assembled in arrays or pallets, so you may have to consider v-scoring, router bit paths, areas for breakaway tabs, or some combination of those. If you need to add fiducial marks and unplated tooling holes (usually 0.125") you should place those before proceeding with component placement. Part of the job of a good designer is to provide for the manufacturing and test processes later.

One more consideration before we get started placing parts: If an in-circuit test (ICT) fixture will be required, you will have to add extra vias for test point accessibility to every net. Since the goal is 100% accessibility to every net from the bottom of the board (double-sided fixtures are more expensive), even short traces that can be routed on the top of the board must use a via to get to the bottom-side for a test point. Adding vias to every net means extra space between components, so keep this in mind (or just add them) while you are placing functional groups of components.

It's a good idea to meet with your fabrication and assembly partners before going too far, just to make sure your design will meet their needs. There is much more to learn about design for manufacturability (DFM), but that's beyond the scope of this article. For more information, familiarize yourself with IPC-2221 and IPC-2222

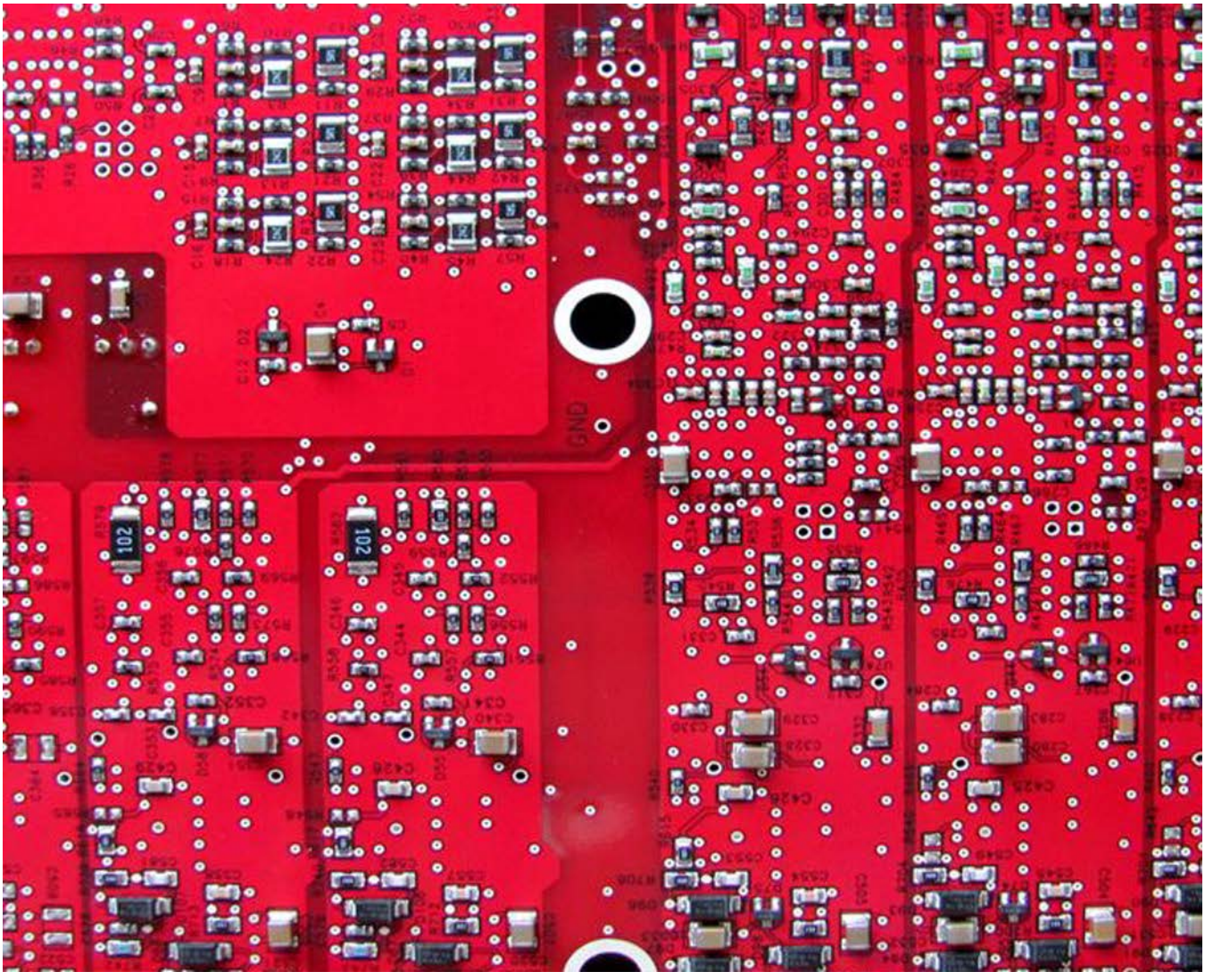


Figure 1: Example of circuit board partitioning, or "floorplanning."

(Generic Standard on Board Design), and I also recommend the IPC Certified Interconnect Designer (CID) training courses.

Placement Strategy

Now, it's time to take a step back and look at the big picture. Electronic circuitry has some kind of flow: Input and power comes from somewhere, something happens to the input internally, and some kind of result goes out.

Regardless of how the circuits are placed on the schematic pages, the floorplan of the design should be somewhat logical. We want to keep functional groups of circuitry together, we don't want groups interfering with each other, and we don't want critical signals crossing back and forth over each other. Analog circuits should be separated from digital circuits. High-frequency circuits should be isolated from low-frequency circuits. Sometimes we try to reduce the noise being transmitted into or out of our design by placing filters on connector lines. Place these components as close to the connector pins as possible.

Scan through the schematic, mentally taking note of groups of components that look like they belong together. Look for circuits that aren't anything like the rest. For example, there may be a power supply with high current requirements and very large components, but everything else is smaller. One single circuit like this with special requirements probably needs to be done first using specific rules, and then moved into location in a particular area of the board, such as near a power connector.

Pay attention to repetitive blocks of circuitry. For example, let's assume that there are eight channels of identical circuits for a particular design. In this case I would do one "perfect" channel placement, taking extra time to make the group into a rectangular arrangement, or some shape that will allow me to place the other seven channels without wasting too much board space, and then copy the remaining channels to match.

For more complicated functional groups, I generally place decoupling caps first, then higher-frequency components like crystal oscillators and associated circuitry (which might be considered more important than decoupling, but they rarely interfere with each other), then feedback components or components in the "critical path," and then all the miscellaneous passives like pull-up or pull-down resistors. As I go, I make sure to leave room for vias, quite often putting them in as I go.

Keep sorting out groups until you have all your blocks done, or enough to start organizing them on the floorplan. Even if large, active devices don't seem to have an obvious group or are connected to too many devices to manage easily, at least place all the required decoupling caps and other passives, such as pull-up and pull-down resistors. I usually try to put these underneath the large ICs so I can move and rotate them in convenient blocks.

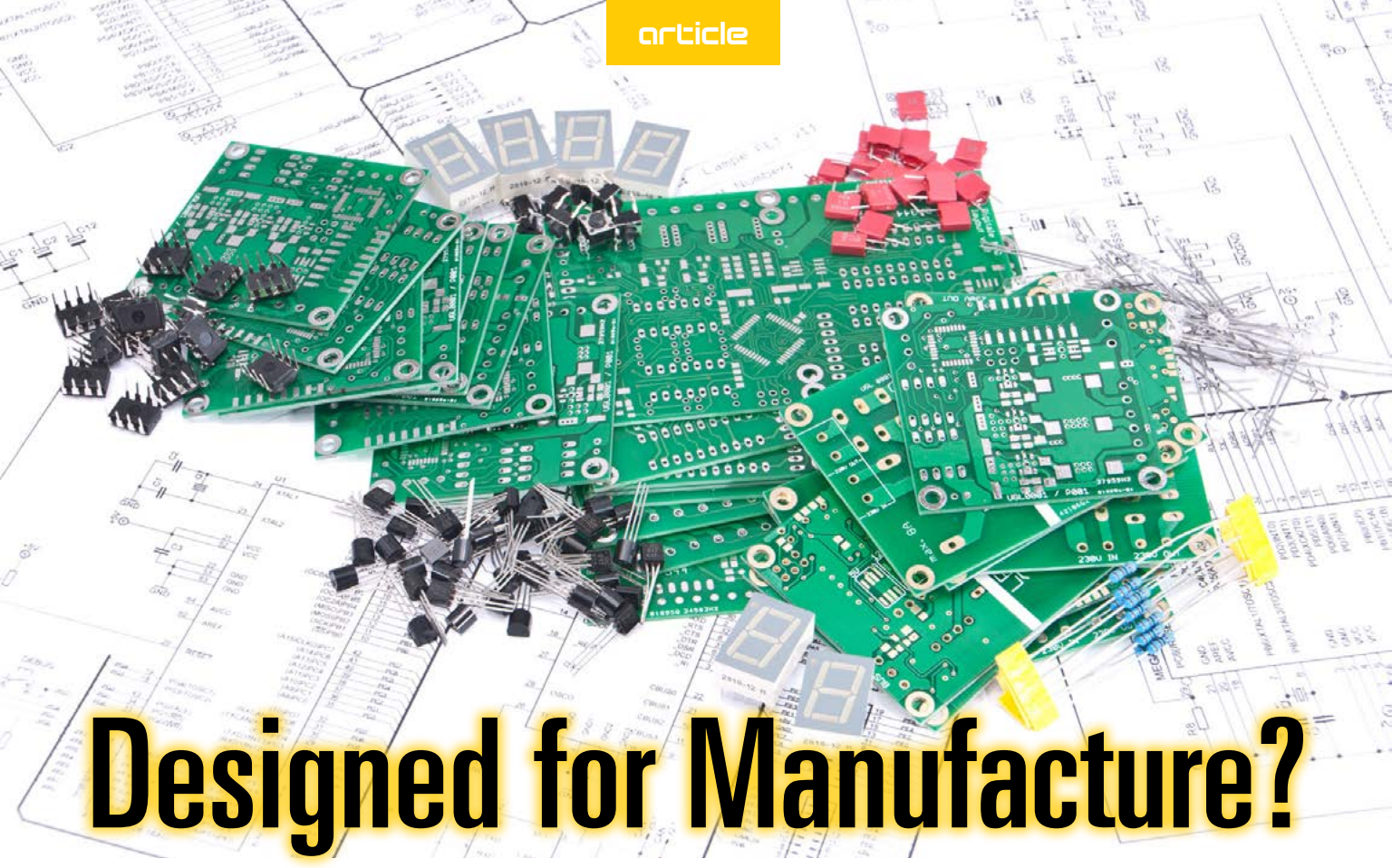
Try to get a mental picture of the best way to place the functional groups of components so the circuit flows logically. If the design is very complex and you aren't sure how it should fit together, you can start working on the functional groups individually, and then shuffle the groups around later to make them fit together.

When you have most of the groups sorted out, zoom back out to see the big picture again. You have functional blocks of circuitry placed, and now it's time to arrange them in some logical order. Even though you have made good progress on organizing components into groups, the remaining netlines may still look very complicated.

Another way to sort out the floorplan placement is by the various power requirements. For example, many modern circuit board designs have several different voltage levels used by various sections. Most of the time you will want to keep blocks using similar voltages together for the most efficient power distribution.

Once all of the components are placed, review your original rules (height restrictions, keep-out areas, etc.) to make sure nothing was overlooked. **PCBDESIGN**

Jack Olson C.I.D.+ has been designing circuit boards full-time for more than 20 years. He would like to thank the schedulers and supervisors who allow designers enough time to "do it right the first time." To contact Olson, click here.



Designed for Manufacture?

by Neil Day
EXCEPTION PCB SOLUTIONS

SUMMARY: Good DFM practices can save a lot of time and questions in CAM engineering, while ensuring your boards are easier to make. Here are a few words of advice and some techniques that can help with your next design.

The most important aspect of designing a PCB is the end goal, which in almost every case is a reliable, cost-efficient product, delivered on time for a reasonable price.

The importance of knowing how your board is made is immeasurable, so give your manufacturer a call and arrange a visit to his site. Knowing how he makes your boards will help you with every design.

The suggestions in this article are not the Holy Grail of design, and they do not address any specific design techniques. In most cases the suggestions are common sense, which when practiced regularly will become second nature and save you time.

Let us suggest concentrating on three areas that will provide the greatest return on your investment in time and education.

Early Engagement with the Manufacturer

Get involved with your manufacturer at an early stage. Ask him to create the layer build for you and provide impedance calculations for your requirements. There is little point in designing a board which cannot be manufactured or rules out the majority of manufacturers due to technology constraints.

We see multilayer boards where the designer has placed a drill stage between each layer pair, which requires multiple sequential bonding operations, tower vias and copper filling. Often there is little need for this and simple through drills will achieve exactly the same result for a fraction of the cost in a fraction of the time. We have also redesigned a board for a customer with a 0.25 mm pitch BGA which was using 0.1 mm through drills and 0.03 mm track and gap. By using a six-layer build with a layer 3-4 drilled core, foils on layers 1, 2, 5 and 6, and tower vias from 1-2, 2-3, 5-4 and 6-5, we were able to route the board with 0.1 mm track and gap. The board was more complex in terms of bonding, but the improved track and gap increased yield from 40% to 100%, which reduced the cost and improved the reliability and durability of the finished product.

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DESIGNED FOR MANUFACTURE? *continues*

Good DFM practices can save a lot of time and questions in CAM engineering and ensure the boards are easier to make, thus saving you money. If the board is easier to manufacture, yields will be higher and waste material costs lowered, which will all affect the price per circuit.

Improved Routing Techniques

Autorouting can speed up your layout process, but can create a long engineering process due to common problems that are easy to prevent or correct at the design stage. Here are a few suggestions for improving autorouted and handrouted boards.

If you need 0.075 mm track and gap to route into a BGA, create a routing area around the device with a 0.075 mm rule and leave the rest of the board with a larger track and gap to improve reliability.

This doesn't look too bad, but this is 75 µm track and gap, necked down to 50 µm into the BGA. It could easily have been routed with 100 µm tracks and gaps outside the BGA pins with a rule area around the BGA to allow 50 µm track and gap. Constraining the very fine track and gap to areas makes it much easier to etch and plate during manufacturing.

After routing, take time to review the routing. In dense areas, spread traces out evenly to prevent underetching. In very sparse areas, do not route an isolated thin trace as this will overetch; either add copper or allow the manufacturer to add copper balancing.

Note evidence of autorouting in the top right corner of Figure 2, where the tracking hugs a via pad. Tracking at the bottom of the board could have been spread out and thickened to improve manufacturability. This is all 75 µm track and gap, but it could easily have been 100 µm.

Ensure tracks enter square or rectangular pads at 90° to prevent acid traps at the pad/track intersection.

In Figure 3, the acid traps and thin gaps between thick tracks and large pads make this design difficult to etch. This will lead to poor yield, increased panel loading, and higher board price and longer lead time.

Designers should add teardrops to drilled pads, particularly where a thin track is entering a large through-hole pad. Remember to add sufficient allowance to plated through-hole pads for oversize drilling to accommodate plating and meet IPC recommendations. A 1.0 mm plated hole would typically be drilled at 1.1 mm; ideally the oversize for the pad on an outer layer would be a minimum of 0.3 mm larger than the finished hole size, for the inner layers it is 0.25 mm larger than the drilled size.

Documentation

The basic documentation required to manufacture a PCB is simply Gerber files and NC drill

Figure 1: This could easily have been routed with 100 µm tracks and gaps outside the BGA pins.

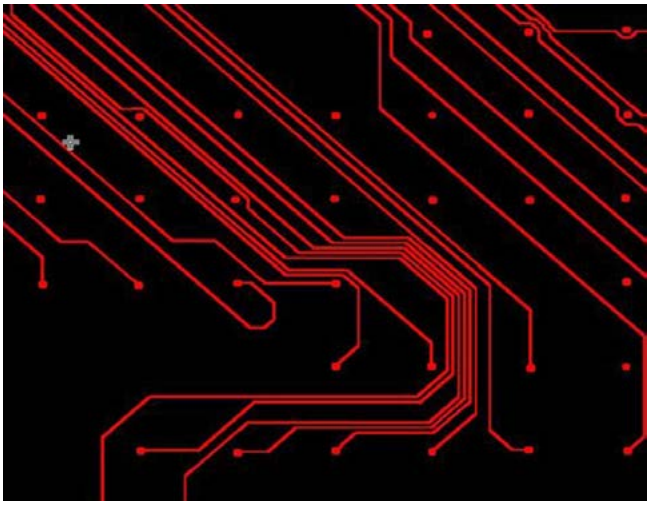

Figure 2: This section, all 75 µm track and gap, could easily have been 100 µm.

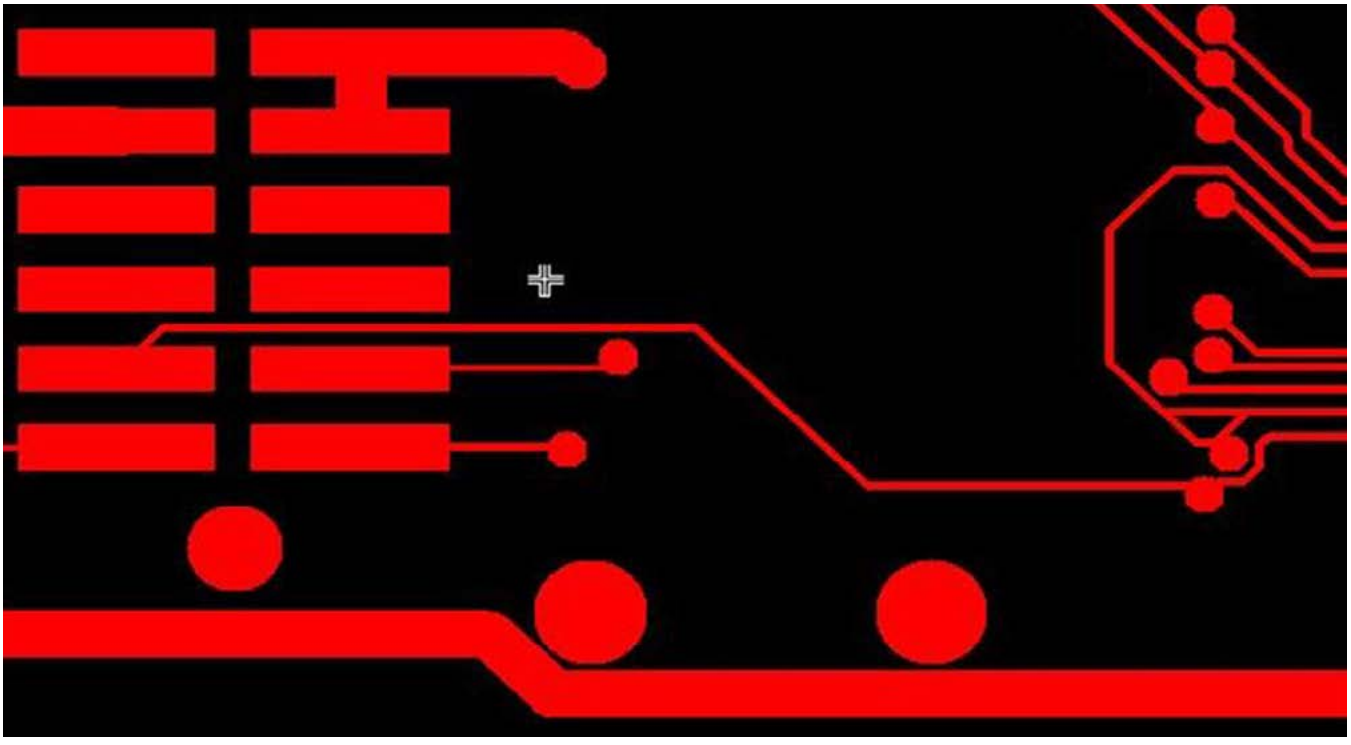

Figure 3: Note the acid traps and thin gaps between thick tracks and large pads.

files, but accurate additional information can help considerably. ODB++ data has become a standard expectation for a lot of manufacturers, and it can provide all the information required by your manufacturer in one file. However, not all design systems will produce the ODB++ data in the same way as Gerbers, and this can cause differences in the way the two formats appear on-screen, mainly with documentation files.

Ensure that drawing notes are correct. Unless a specific brand of material type is required, use the IPC spec. For instance, if an FR-4 material suitable for lead-free surface mount assembly is required, you could just specify IPC-4101/98. Most importantly, speak to your fabricator; he can provide you his most cost-effective quote and probably use material from stock.

Include a drill table with realistic tolerances and reduce the number of tools as much as practicable. We see numerous jobs with 0.7 mm, 0.8 mm, 0.9 mm, 1.0 mm, 1.05 mm, 1.1 mm, 1.2 mm, and 1.3 mm hole sizes, all of which could easily be replaced with just three drill sizes. The following table should help with rationalisation, but ask your manufacturer for recommendations on common lead sizes.

If the hole is a via that is used purely to connect layers, generally the finished hole size is less important than the annular ring. Wherever possible, specify the maximum size for a via, and give the manufacturer some free space to improve the annular ring by providing a tolerance of +0/-0.1.

The three most common reasons for your manufacturer to call you with questions can be avoided simply with good drawing notes. Provide the following information upfront and avoid these questions, which can cause delays in engineering and delivery.

1. If you're happy for the manufacturer to remove non-functional pads from inner layers, let him know on the drawing.

2. If there are controlled impedance requirements, details these in the drawing notes. A simple note such as "100R differential traces exist on layer 1 referenced to layer 2, trace width 0.1 mm, gaps 0.15 mm" will suffice.

3. Finally, if there are intentional shorts or opens in the design file and you are supplying an IPC-356 netlist to test against, detail these

DESIGNED FOR MANUFACTURE? *continues*

Component Type:	Lead Diameter	Hole Diameter
Axial:	0.38 to 0.50 mm	0.8 mm
	0.51 to 0.75 mm	1.0 mm
	0.76 to 1.05 mm	1.3 mm
	1.06 to 1.30 mm	1.6 mm
Radial:	0.40 to 0.59 mm	0.8 mm
	0.60 to 0.79 mm	1.0 mm
	0.80 to 1.00 mm	1.2 mm

Figure 4: A realistic drill table.

on the drawing with a basic note such as "Nets GND and PGND are intentionally shorted on layer 2 in the location of component reference SP1".

I believe that following these simple techniques will return significant savings in time and money. **PCBDESIGN**

Neil Day is the design and commercial manager for Exception PCB Solutions. To contact him, click here.

video interview

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Crazing and Conductive Filament Formation

by Paul Reid
PWB INC.

Crazing is a type of material damage that is seen mainly in PWBs with small hole-to-hole spacing (grid size). Crazing is the separation between the epoxy and individual glass fibers. It can propagate with thermal cycles associated with assembly and rework, and also in the end-use-environment. Conductive anodic filament (CAF) and conductive filament formation (CFF) both are the formation of conductive filaments in the dielectric material. They are the growth of conductive metal filaments or dendrites on or through a printed board under the influence of a DC voltage. They may be formed in the spaces caused by crazing. The problem with CAF and CFF is that they are conductive and may cause current leakage or a short between two circuits with opposite charges such as a ground plane and the barrel of a plated through-hole (PTH).

Crazing

Crazing in the dielectric material is a separation between the epoxy system and individual glass fibers. What happens is this: The epoxy loses its adherence to the glass fibers individually. This is not to be confused with adhesive delamination, which can present itself as a breakdown between laminated surfaces including glass fibers as a group and the epoxy system.

When viewed with a microscope in a cross-section, crazing produces a silver or white sheen running down individual glass fibers. The silver sheen is created by the air gap around the individual glass fibers reflecting light. What we see in Figure 1 is copper wicking going down the glass fibers about 0.02 mm (.0008"). Beyond

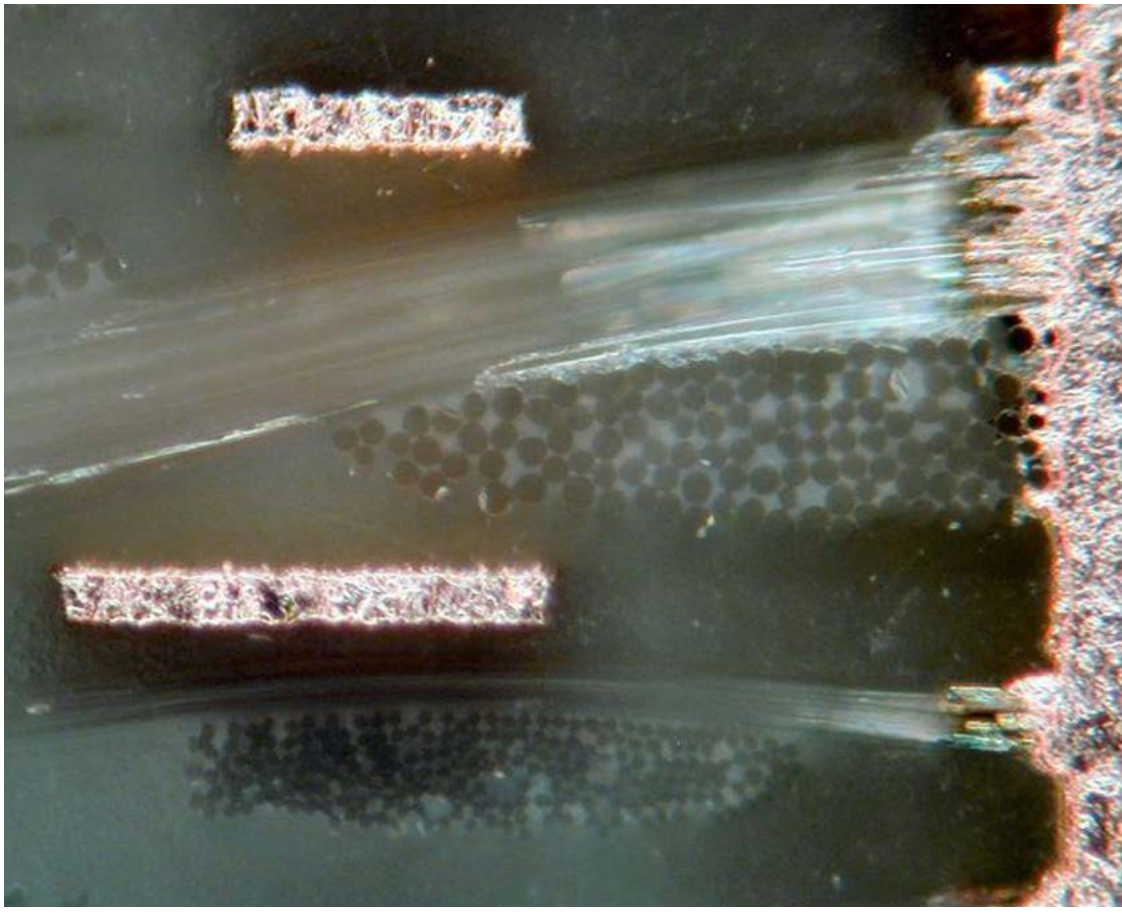

Figure 1: Dark field microsection showing crazing.

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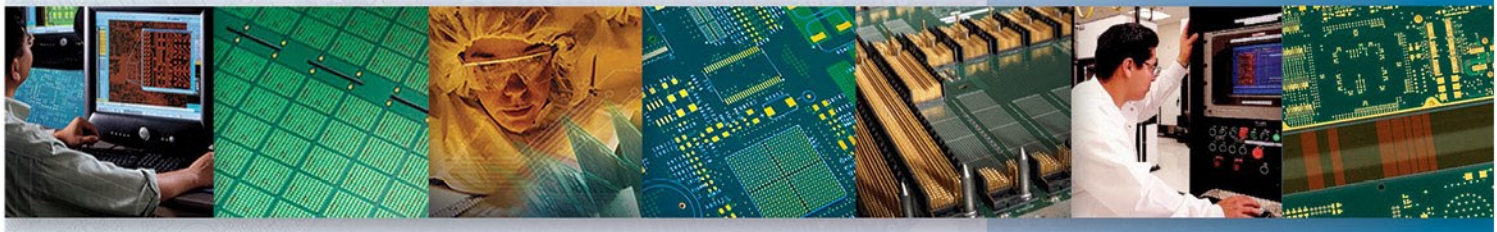

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CRAZING AND CONDUCTIVE FILAMENT FORMATION *continues*

the copper wicking, we see the individual glass fibers appear silver or white. This is the condition called crazing.

IPC-6012C-2010 paragraph 3.3.2.2 and IPC-A-600 paragraph 2.3.2 state that in class 2 and class 3, any crazing that violates the spacing between two conductors by 50% or more is rejectable. These paragraphs also state that the crazing shall not propagate due to thermal cycling that represents the thermal cycling associated with assembly and rework. The distance between the adjacent trace, in this case, is about 0.127 mm (.005") and the wicking extends approximately 0.15 mm (.006") down the glass fibers. The crazing seen in Photo 1 violates the spacing between the hole wall and adjacent trace and propagated after the coupon was exposed to preconditioning six times to 250°C (6 x 250°C). It should be noted that this defect was not visible from an observation of the surface of the coupon. It was only visible upon a cross section evaluation.

Our procedure is to measure the capacitance between ground planes, in test coupons, before preconditioning (as received) and again after preconditioning in this case 6 x 250°C. A -4% reduction in capacitance or greater is considered significant material damage. This coupon posted -6.9% capacitance change after a preconditioning simulation of 6 x 250°C. A cross-section of the dielectric confirmed material damage due to crazing.

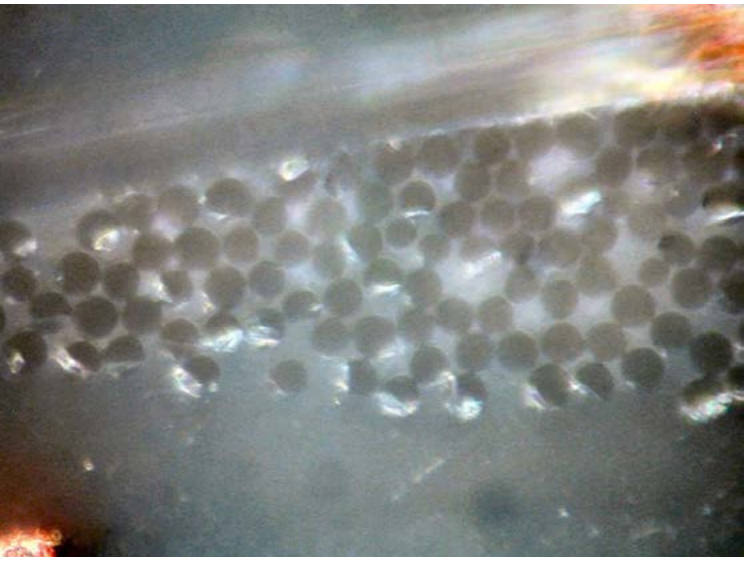


Figure 2: Crazing on the ends of glass.

The two main causes of crazing may be weak material and poor drilling. Note that the crazing seen in Figure 1 is associated with copper wicking. The copper wicking indicates that the material had cracks that were big enough to have electroless and electrolytic copper deposition during the fabrication process. Where the copper stopped is where the crazing began. What appears to have happened, based on an analysis of the section, is that the crazing was initiated by drilling, and then propagated as a result of the thermal excursions associated assembly and rework.

On a cross-section where the "end of glass" fibers are visible, crazing can present itself as half-moon separations on one side of the glass fiber, between the epoxy and the glass fibers (Figure 2).

Another condition that we have noticed is that the closer the holes are drilled to one another, the greater the tendency for crazing. What we have found is that there is a marked tendency for crazing on circuit with a grid size of 0.5 mm (.020") or less when compared to 0.8 mm (.032") or 1.0 mm (.040") grid sizes. Crazing on tighter grid sizes presents a particular challenge to PWB fabricators.

CAF and CFF

In order to have CAF and CFF formations, we must have water present in the dielectric, an electrical potential between two adjacent conductors, ionic contamination, and a path. In this case the path is caused by crazing. Without one of these conditions CAF and CFF will not occur.

There are four paths that the failure may take. The failure may be from PTH to PTH, PTH to a trace, from trace to trace or plane to plane. Whatever way the filament forms, one may find current leakage or possibly a short.

Let us consider an airplane sitting on the runway in a jungle environment with elevated temperatures and high humidity. If there is crazing in the PWB, the humid air may penetrate the space created by the crazing. The airplane takes off and climbs to a high altitude where the PWB is cooled off. As the PWB cools, more

air is brought into the space in the crazing. The water vapor may condense, leaving liquid water within the PWB. When the airplane lands in the humid air, the air may then penetrate he PWB and the process starts over. What appears to happen is that the crazing, when exposed to the thermal excursions in the end-use-environment, may act like a pump that brings water down the separation between the epoxy and the glass fibers, into the dielectric material.

Another way that water can get into the board is by means of capillary action. Capillary action is a condition by which a liquid may flow into narrow spaces with, or in opposition, to the force of gravity. The adhesive forces and surface tension of the water cause the liquid to be drawn into the space, wicking into the dielectric material. If the glass ends exhibiting crazing come in contact with liquid water, the water may be drawn up the space between the glass fiber and the epoxy. This may be observed on the exposed glass fibers that have crazing on the edge of the PWB, if crazing and water are present.

The water in the space caused by crazing may dissolve ionic contaminants found in the PWB. The contamination may be from the halogens in the dielectric, which are used as flame retardants. Typically bromine and chlorine have been added into the epoxy as flame retardants which may be dissolved by the water. Or it could be trapped plating solution, possibly trapped behind hole wall pull away, or plated closed voids in microvias. The resulting ionic solution is, by definition, conductive.

Once water is in the dielectric, it may dissolve contaminants in the PWB and produce a conductive path between two conductors that have an opposite charge. This conductive liquid may provide a medium for the growth of conductive filaments causing current leakage or an electrical short.

One of the problems with CAF or CFF is that they are hard to find, even with coupons that have been tested and failed. The problem is in the size of the conductive filament. These conductive filaments may be extremely small and are easily overlooked in the microsection. Figure 3 shows a copper filament on the end view of a glass fiber that caused a short between two conductive traces.

Under an electric potential, the CAF or CFF forms over time. A conductive filament is deposited filling the crack and bridging the gap between the anode and the cathode. Once the bridge is formed the shorting of the electric circuit causes the filament to be destroyed like a fuse that is burnt out. In the beginning of the formation the result is a short that is burnt out about as soon as it is formed.

Figure 3: Copper filament that caused a CAF failure.

CRAZING AND CONDUCTIVE FILAMENT FORMATION *continues*

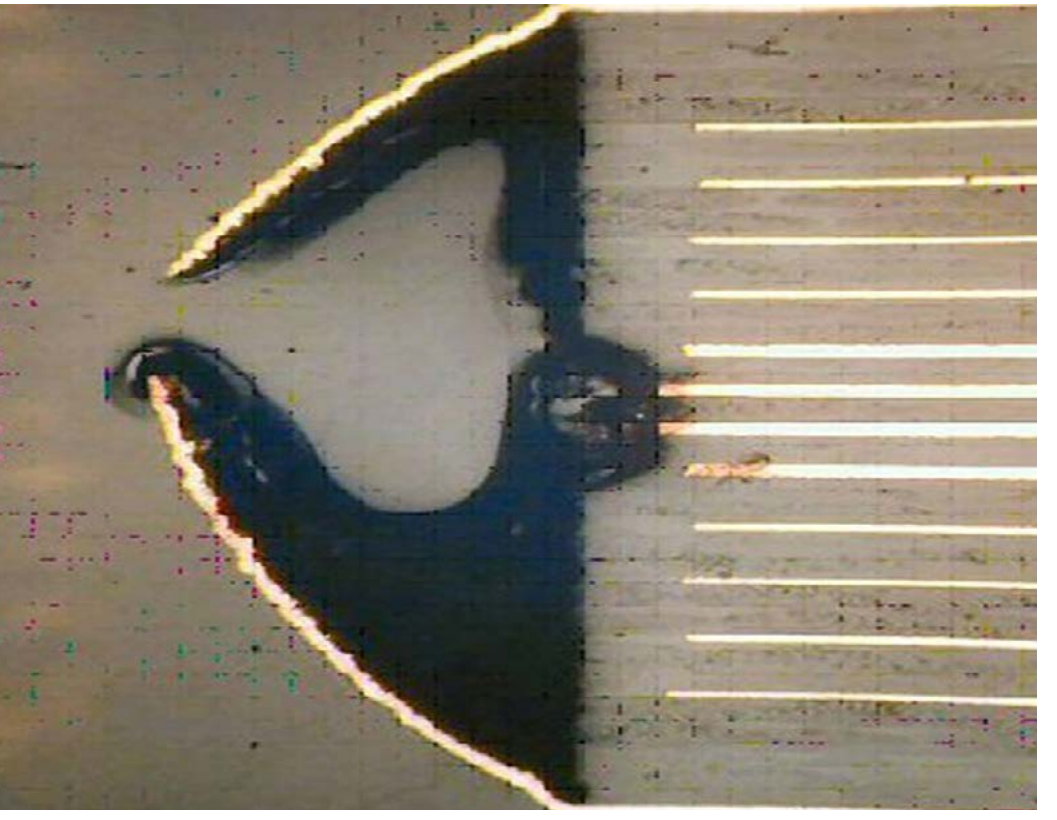


Figure 4: Short due to CAF formation.

From the stub that is left the conductive filament starts to grow again but this time with an already formed base. The second growth may be more robust than the first growth. This growth, followed by burn out, goes on until the conductive filament grows to a point that it takes longer for the short to burn out and a catastrophic failure, with material damage, may occur.

The result of CAV or CFF that creates a short that is much easier to observe in PWBs. There is a tendency to have a catastrophic failure in the end-use-environment, which develops over time. Figure 4 is an example of a short that occurred due to formation of CAF from the ground plane to the barrel of a PTH. The bias was 50 volts and this short occurred after a few months in the field.

The animation in Figure 5 shows copper filament growth over time in the end-use environment. There are no thermal cycles associated with this animation because it occurs during an isotherm at the end-use environment temperature. Note that in this animation the copper is growing down the glass bundle in which the crazing is already present. What is depicted is the copper filament that forms down the glass bundles and then jumps the epoxy rich space between the glass bundle and the adjacent trace. When the copper filament bridges the gap between the conductive filament and the trace a catastrophic failure, with the associated material damage, occurs. **PCBDESIGN**

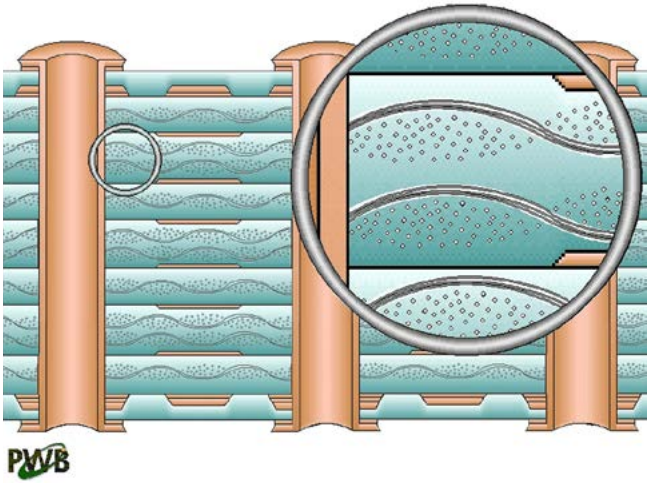
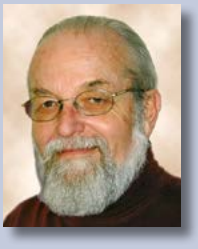


Figure 5: Click to view animation of a CAF short.



Paul Reid is program coordinator at PWB Interconnect Solutions, where his duties include reliability testing, failure analysis, material analysis, and PWB reliability consulting. To contact him, click here.

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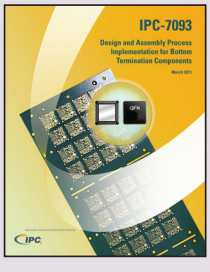

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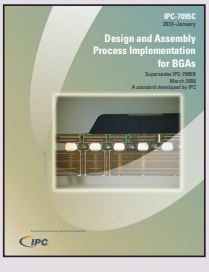

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Hallmark Circuits USA Achieves Nadcap Certification

With this accreditation, all manufacturing sites of the SOMACIS Group—in Italy, China, and now in the U.S.—are Nadcap certified, as a further proof of the dedication of the company in assuring the highest possible standard of quality and reliability for advanced PCBs utilized in demanding industries such as aerospace.

Teknoflex Earns AS9100 rev C Certification

David Knight, director of quality and process engineering, commented, "It is good to finally reach the goal we set out to achieve; this was a company-wide effort and is a mark not only of the compliance of our QMS, but to the diligence and dedication of all of our staff."

Russia to Overtake West in Defence, Growth, Electronics

Steen Lomholt-Thomsen, IHS senior vice president, EMEA, said, "Russia is an exceptional opportunity. While leaders globally are concerned and cautious about geopolitical instability and economic volatility, business sentiment is rising in Russia."

Unmanned Surface Vessels Set to Conquer the Seas

Unmanned surface vessels still lag far behind their aerial equivalents in terms of technical capabilities, technology, and deployment. However, new threats, cost-benefit calculations, operational experiences in the past decade, and new technological developments are driving rapid growth in the market.

China's Aero & Defense Industry Seeing Rapid Growth

With a rapidly growing government budget for the defense sector, the Chinese aerospace and defense industry is witnessing the growth of many multinational companies who are setting up in the country and also actively indulging in joint ventures with Chinese companies.

SOMACIS Named Meggit's Preferred Supplier Partner

Meggitt PLC, a global engineering group specializing in extreme environment components and smart sub-systems for aerospace, defence, and energy markets, has selected SOMACIS as preferred supplier on PCBs.

Maritime Satellite Markets on Cusp of Bandwidth Revolution

"With the launch of GEO-HTS maritime services just on the horizon and MEO-HTS not far behind, maritime markets are on the cusp of a bandwidth revolution, yet, more data can also come in small bytes," explains Senior Analyst and report author, Brad Grady.

Interlocking Composite Components Create Big Structures

Researchers have developed a lightweight structure whose tiny blocks can be snapped together much like the bricks of a child's construction toy. The new material could revolutionize the assembly of airplanes, spacecraft, and even larger structures, such as dikes and levees. The new approach is described in a paper co-authored by postdoc Kenneth Cheung and Neil Gershenfeld, director of MIT's Center for Bits and Atoms.

Report: South East Asia Defense Market Opportunity Analysis

"South East Asia Defense Market Opportunity Analysis" research report gives comprehensive insight on following aspects related to booming Defense market opportunity in the South East Asian region.

Non-lethal Weapons Market on the Rise

The United States is a matured market with most of the market leaders situated in this region. The United States' non-lethal weapons market is estimated to be $183.0 million in 2013 and is expected to register a CAGR of 5.05%, to reach $234.2 million by 2018.

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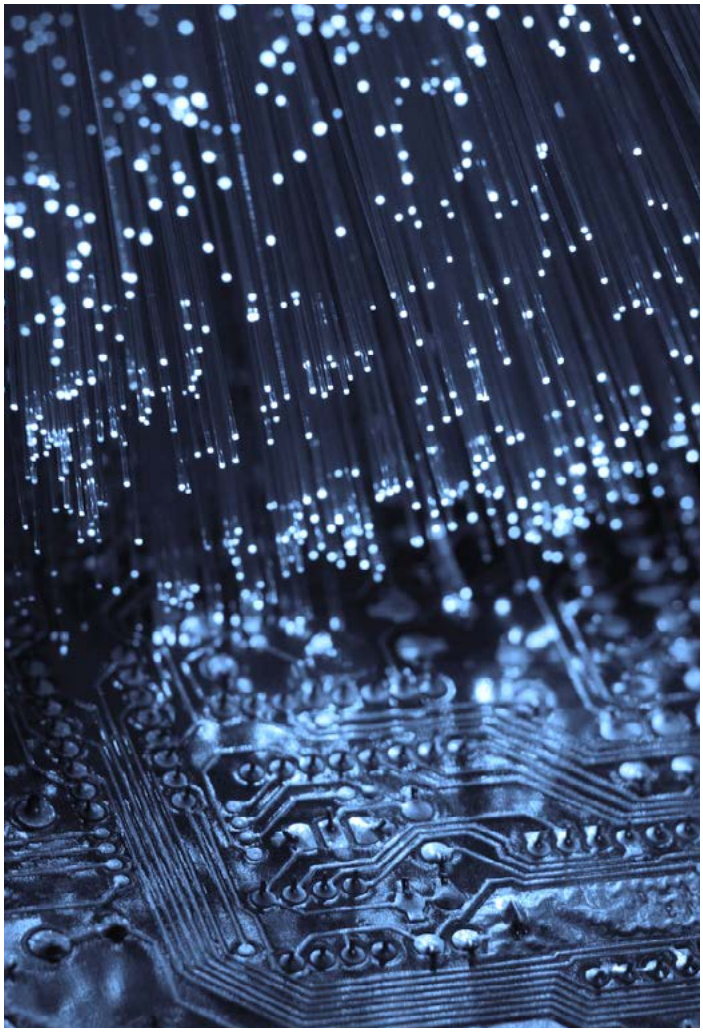
A Tale of Two Materials

by Amit Bahl
SIERRA CIRCUITS

Since the turn of the 21st century, there has been intensive research toward the development of embedded optical channels for transporting high-speed digital signals within printed circuit boards. I suspect that an alternative to copper traces might be commercially viable by 2035 or sooner, depending on the development of semiconductor devices with integrated photonics to transmit and receive signals through those channels.

The development of the optical waveguides and integrated photonics is driven largely by the capacity demands (as well as the power consumption) of high-performance routers and network switches, whose backplanes may span more than 20 inches. Signal attenuation due to dielectric and conductor losses is a major concern for designers of those backplanes, as are signal reflections caused by impedance variations resulting from shifts in the dielectric constant of laminates with frequency. Signal propagation delay, which is governed mostly by laminate dielectric constant, and trace crosstalk are also spurring the development of optical channels.



Optical channels would be immune from noise, virtually lossless, and electrically independent of surrounding material. They would be the conduit for high-speed signals, while copper traces elsewhere in the boards would comprise the remainder of circuits. However, creating those channels involves changes throughout the entire infrastructure of electronics manufacturing, including semiconductor materials and fabrication processes, IC and PCB design tools, and IC packaging technology, beyond the development of optical materials compatible with high-volume, panel-based PCB manufacturing processes. That will take time. Meanwhile, PCB materials with stable Df values on the order of 0.003 up to at least 10 GHz are necessary to meet channel loss budgets in such current high-speed digital applications as network line cards for 40 Gbit/s and faster data rates.

Various materials, some of them widely used in RF applications, have Df values low enough to satisfy the loss budgets of high-speed signal paths on 40-Gbit/s ethernet line cards, for example, within safe margin. These materials cost more than regular FR-4 laminates, so hybrid stackups are common that dedicate high-speed nets to low-loss layers and less-critical circuits to layers of FR-4 for economy.

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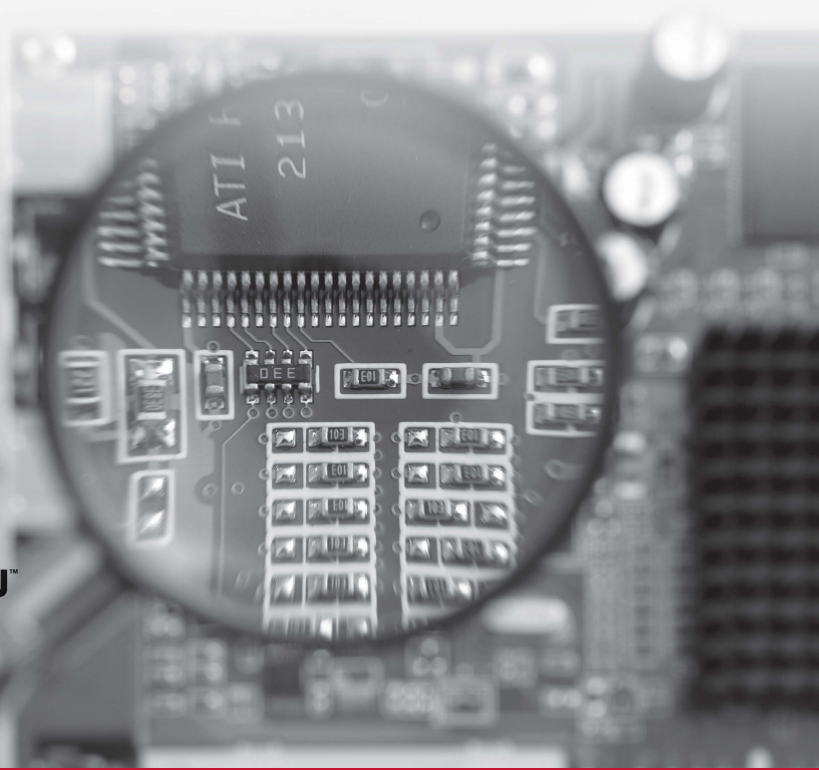

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A TALE OF TWO MATERIALS *continues*

Finding the low-loss material that will provide the best balance of performance and board cost for a given application is more complicated than simply comparing laminate data sheets and prices. Data sheets do not reveal which materials involve relatively more or unusual processing steps during PCB fabrication, which can raise manufacturing cost.

Consider Rogers 4350B and Panasonic Megtron 6, which have similar low Df and Dk values, have been used extensively in RF applications, and are increasingly being used for high-speed digital products. Both are based on hydrocarbon resins; the Rogers resin has a ceramic filler. Neither laminate is available clad with quarter-ounce copper. The thinnest foil available for the Rogers material is half an ounce, and for Megtron 6, one-third of an ounce. Both materials are available with low-profile foils to prevent signal reflections at high frequencies. The Rogers core material is essentially perfectly flat and repeatable, aiding impedance control; the Panasonic material slightly less so. The Rogers material is at least twice as expensive as Megtron 6.

> ***The most significant contrast is that Megtron 6 laminates the same as conventional FR-4 materials; no incompatible pressures, temperature, movement, or cure time are involved.***

Rogers offers three prepreg choices for bonding the 4350B laminates: a 4-mil prepreg that is available in two glass styles and one that is 3.6 mils thick with one glass style. Eight laminate thicknesses are available. Megtron 6 laminates come in 18 thicknesses, complemented by a wide range of prepreg thicknesses and glass styles, including various tightly woven, so-called flat-glass styles to avoid impedance variation caused by fiber-weave effect. Resin evenly coats the surface of those tight weaves. Three different percentages of resin content can be selected for several of the Megtron 6 prepreg glass styles.

Rogers discourages etchback of the material, advises against using a single layer of prepreg in high-layer-count, single-lamination stackups, and recommends cap construction. Manufacturers have to adjust the lamination cycle for fabricating boards when the Rogers material is involved because of the restriction on using a single layer of prepreg. The Rogers prepregs for the 4350B cores require higher pressure for proper lamination than do the Panasonic prepregs, which process no differently than conventional FR-4 materials.

What is the upshot of the differences between Rogers 4350B and Panasonic Megtron 6, beyond their raw material costs, considering that their electrical properties are alike? The most significant contrast is that Megtron 6 laminates the same as conventional FR-4 materials; no incompatible pressures, temperature, movement, or cure time are involved. Hybrid boards can be built in a single lamination with inner layers of relatively inexpensive FR-4 materials and an outer layer or layers of Megtron 6, using foil construction or cap construction. Moreover, the wider selection of Megtron 6 core and prepreg thicknesses and resin content eases stackup development and impedance control.

Many PCBs have been built using Rogers 4350B material for very high-speed digital circuits. It is a proven choice from a functional perspective, and a highly predictable material from a manufacturing perspective, with well-established fabrication protocols. Though its use is routine, it is somewhat more complicated to process than Megtron 6.

The fact that fabrication complexity and yield have an inverse relationship is worth recognizing at the outset of design. Manufacturing yield may not be a concern if you only need a few boards, but that is certainly not the case for volume production. **PCBDESIGN**

Amit Bahl directs sales and marketing at Sierra Circuits, a PCB manufacturer in Sunnyvale, CA. He can be reached by clicking here.

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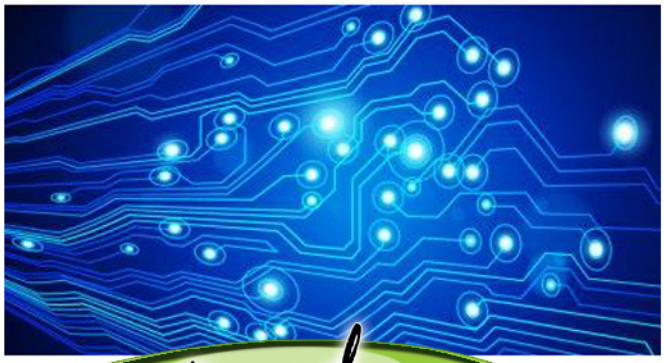

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TOP TEN

News Highlights from PCBDesign007 this Month

① Mentor Graphics Supports Bell Helicopter's Systems Upgrade

Mentor Graphics has announced that Bell Helicopter, a leading manufacturer of rotary wing aircraft, has been able to significantly streamline their wiring design processes on the Bell 525 Relentless program as part of its Business System Modernization systems upgrade.

② Zuken Unveils First PCB Layout Productivity App

The CADSTAR Touch App enables users to control Zuken's CADSTAR expert desktop PCB design software, giving simultaneous control of view and program functions, and enabling faster, more efficient design.

③ FabStream: PCB Library Expert Now Supports SoloPCB

PCB Libraries has released a new free version of the Library Expert that creates IPC-7351-compliant footprints for FabStream's SoloPCB Design Software. The Library Expert is easy to use and requires a very short learning curve so PCB designers can use it effectively in minutes.

④ Bay Area Circuits Announces Silicon Valley Expansion

Bay Area Circuits has relocated to a 30,000 square-foot manufacturing facility located in Fremont, California. The fabricator, which also provides PCB layout services, had operated in Redwood City since 1975.

5 Sunstone Circuits Upgrades PCB123 With New Version

The company has launched the newest version of its PCB design tool, PCB123, which includes two major upgrades to functionality: Tools to create slots and cutouts and file-specific hole sizes. With Version 5, PCB123 users can now create plated slots as small as 0.025" and as large as 0.250". Non-plated slots can be in the range of 0.031" to 0.257".

6 Team Design for OrCAD Gains Hierarchy & Library Support

"Many of our customers design their electronics with a team of engineers, but too much time is devoted to coordination rather than designing," said Manny Marcano, president and CEO of EMA. "This release of Team Design for OrCAD gives these teams a new level of management and control over the design process to increase team efficiency and reduce time-consuming errors."

7 JSA Designs Appoints MEng Brent Laurence

Principal Vince Di Lello has appointed Brent Laurence, MEng, to the company. Laurence has a wealth of industry experience, including hardware design, firmware development, process automation, and active noise control for consumer vehicles. He holds a Master's degree in electrical engineering from McGill University.

8 Altium Releases New Range of Component Libraries

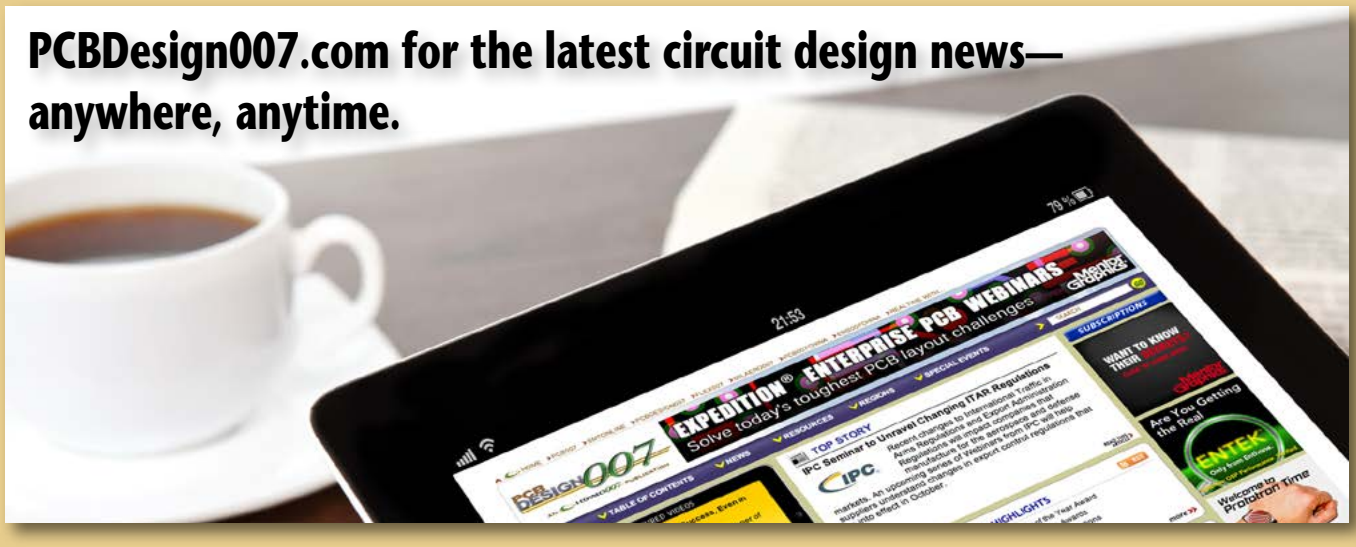
Principal Vince Di Lello has appointed Brent Laurence, MEng, to the company. Laurence has a wealth of industry experience, including hardware design, firmware development, process automation, and active noise control for consumer vehicles. He holds a Master's degree in electrical engineering from McGill University.

9 Design Automation Conference Issues Call for Contributions

The Design Automation Conference, in its 51st year as the premier conference devoted to the design and automation of electronic systems, is a not-to-miss occasion for the worldwide community of system designers, system architects, IC designers, embedded system designers, validation engineers, CAD managers, and senior managers, researchers and academics.

10 "Designing Medical Devices" Forum to be Held in Germany

The one-day seminar, "Designing Medical Devices: Advanced Solutions for Today's Designers," will educate engineers on various aspects of the medical device design process, including regulatory affairs, cleaning, device coating, final preparation, and packaging.



events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out *The PCB Design Magazine's* event calendar.

IEEE SMC 2013
October 13–16, 2013
Manchester, UK

electronicAsia
October 13–16, 2013
Hong Kong

SMTA International
October 13–17, 2013
Fort Worth, Texas, USA

SMTA Harsh Environments Symposium
October 15, 2013
Fort Worth, Texas, USA

SMC 2013
October 16–17, 2013
Santa Clara, California USA

2013 CEA Industry Forum
October 20–23, 2013
Los Angeles, California, USA

IMPACT-IAAC 2013
October 22–25, 2013
Taipei, Taiwan

TPCA Show 2013
October 23–25, 2013
Taipei, Taiwan

IEEE-SA Symposium on EDA Interoperability
October 24, 2013
Santa Clara, California, USA

Conformal Coating Reliability Seminar
October 24, 2013
Greater London, UK

MRO ASIA
October 29–31, 2013
Singapore

International Wafer-Level Packaging Conference
November 4–7, 2013
San Jose, California, USA

LA/Orange County Expo & Tech Forum
November 5, 2013
Long Beach, California, USA

productronica 2013
November 12–15
Munich, Germany

SMTA/iNEMI Medical Electronics Symposium—Tabletop Exhibition
November 12, 2013
Milipitas, California, USA

Aerospace & Defence Programs
November 13–14, 2013
Phoenix, Arizona, USA

MILCOM'13
November 18–20, 2013
San Diego California, USA

Energy Harvesting & Storage USA 2013
November 20–21, 2013
Santa Clara, California, USA

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Next Month in *The PCB Design Magazine:*

Qualifying Your Fabricator

There are plenty of good fabricators out there, but how do you find the best shop without making an on-site visit? Next month, our experts discuss the best ways to qualify a board shop.