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AUGUST 2013

**Thin Palladium
Layers: An Effective
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Strategy** p.12

**Evaluation of
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The August issue of *SMT Magazine* brings you the lowdown on high-density packaging. Our expert columnists and contributors discuss challenges associated with molded flip-chips, new packaging trends and strategies, and more.

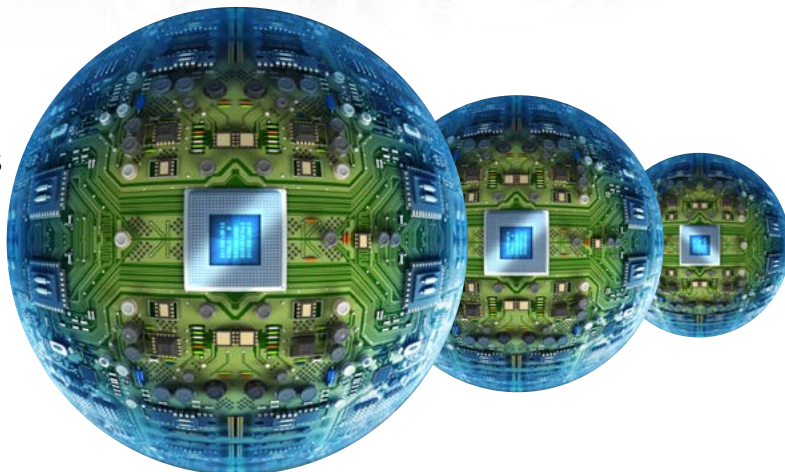
12 Thin Palladium Layers: An Effective Cost-Saving Strategy

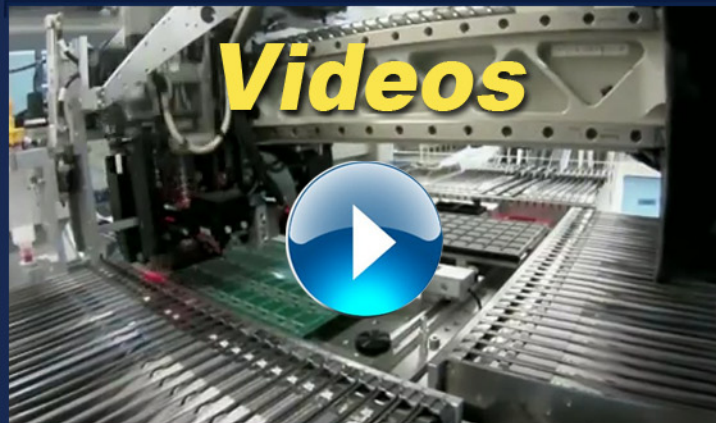
by Olaf Kurtz, Jürgen Barthelmes, Eckart Klusmann, Robert Rüther, and Stephen Kenny



24 Evaluation of Molded Flip-Chip BGA Package for 28nm FPGA Applications

by Altera Corporation, Amkor Technology USA, and Amkor Technology Korea





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THE WAY I SEE IT

ESTC, CAMEST and More

by Ray Rasmussen

I-CONNECT007

In May, IPC launched a new conference in Las Vegas. Electronic System Technologies Conference (ESTC) was the first of its kind for IPC, stepping out of its comfort zone of PCBs, design and assemblies. Here's how the association's website describes the event:

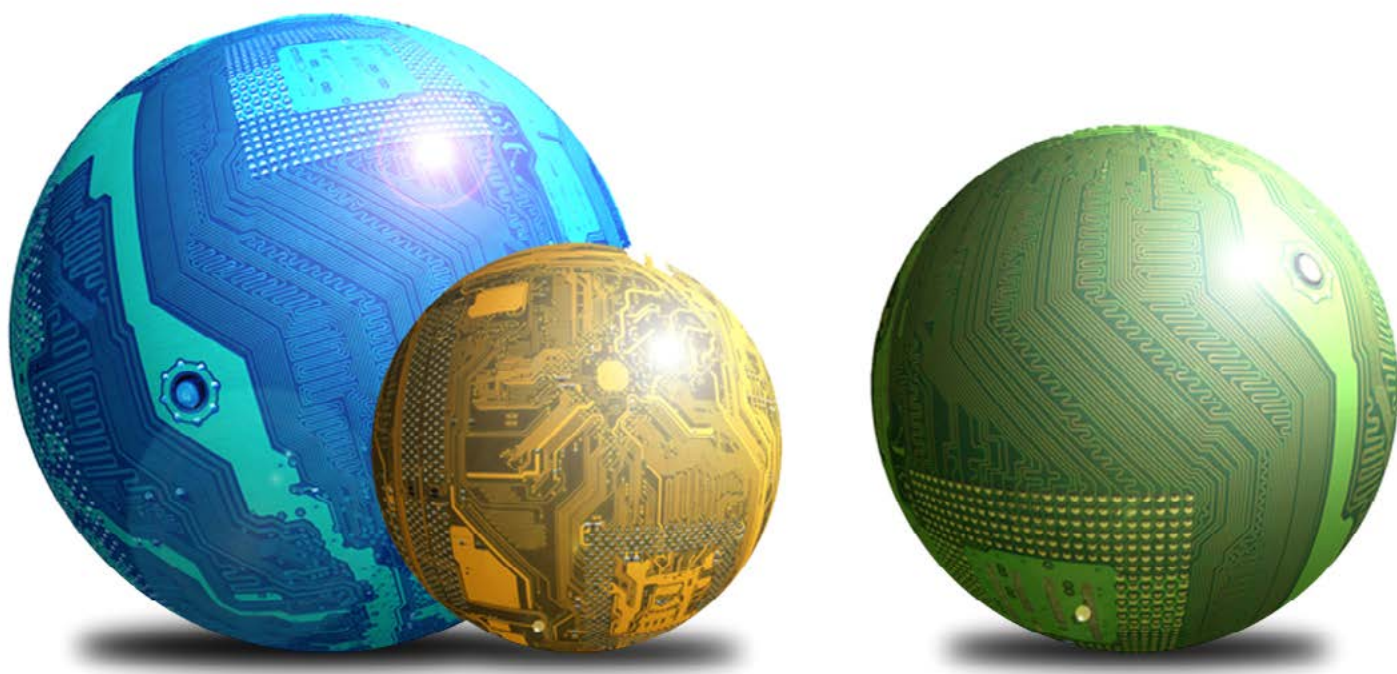
"IPC ESTC is an exciting new event for the entire electronics industry, from foundry and components to board assemblies and complete systems. It's an unprecedented opportunity to break new ground in the discussion of the technologies, products and services that will shape the future of the entire electronics industry."

The conference seems to want to be all things to all people. It's a good "perspective" event which gives all in the supply chain a look at the issues facing technologists in other sectors.

Senol Pekin of Intel led the charge for ESTC. His energy and clout brought a lot of horsepower to the event. You need to see the [program committee page](#) to get a sense of the depth of

the conference that he and his team put together. It was quite impressive. Although it was a great first-time effort, there were a few problems with the conference/show, which seemed obvious. First, the location: A few people mentioned that a high-level conference like this would have done even better in Silicon Valley. Although the Tropicana Hotel was a good venue for the event, there's nothing like a Valley location to attract a good technical crowd. I agree.

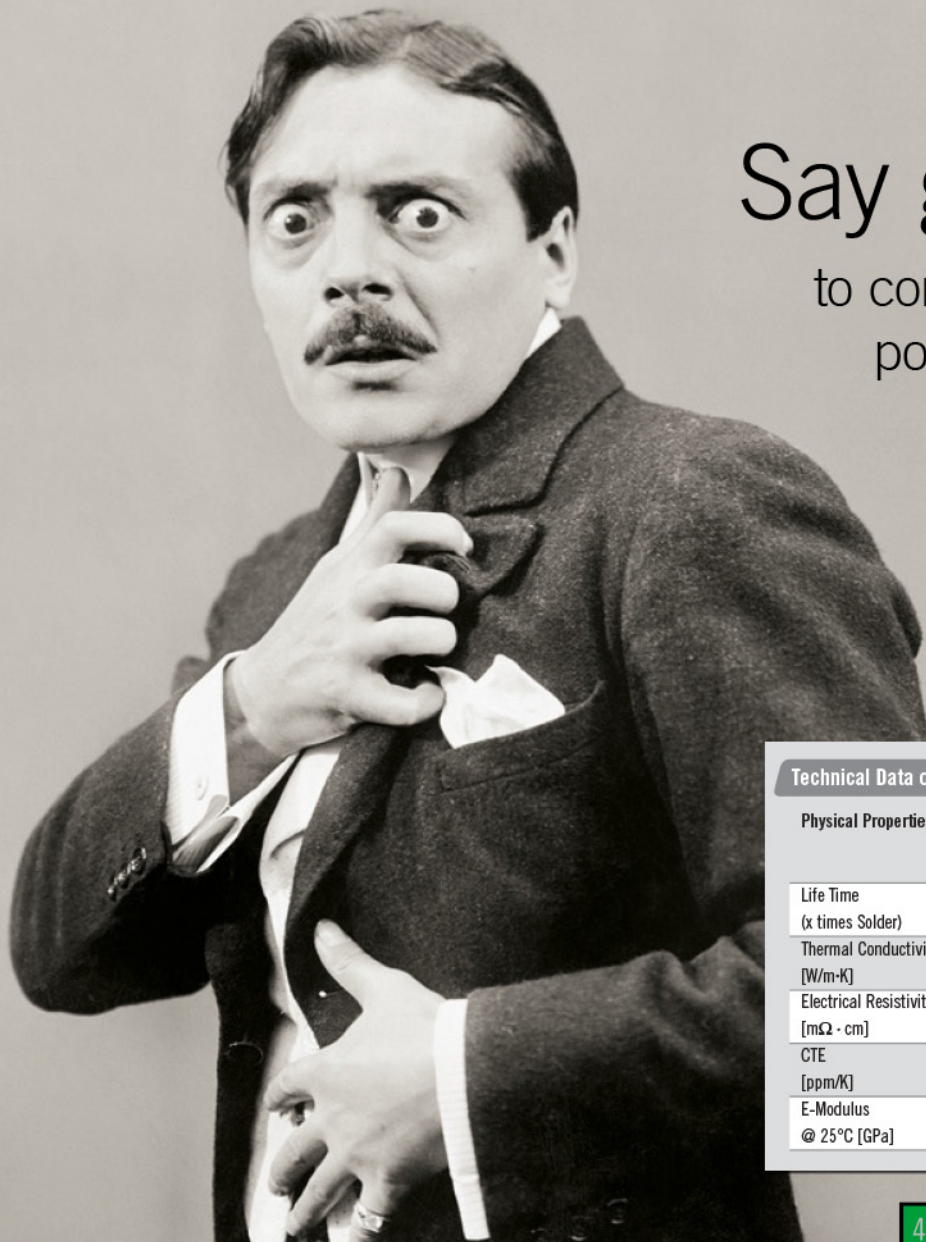
Next, I'm not sure why an exhibition was part of the event. There were only a handful of exhibitors, many of which spent most of the day talking to each other, answering e-mails, or talking on the phone, since everyone else was in the conference sessions. I guess as the conference grows and expands, and with a few adjustments to the schedule, allowing more time for attendees to visit the floor, the exhibition will make more sense. In the future, I could see some tabletop displays where, during the breaks, people would be free to walk around





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ESTC, CAMEST AND MORE *continues*

Figure 1: Senol Pekin, ESTC general chair, moderates during the Q&A portion of the event held in Las Vegas in May.

and learn about some of the latest technologies. But setting up and manning a 10' x 10' booth set expectations too high. I doubt that any of the 20 or so companies exhibiting were happy.

That said, it really was an outstanding conference.

Certainly, there were more PhDs than I've ever seen in one place, not that PhDs necessarily make good speakers or attendees, but the quality of the content and of those in attendance was excellent.

When I first heard of this conference and checked out the program topics, it seemed a bit too far off the PCB/assembly path. I figured that most of the offerings would be over our heads (or mine, at least). But after attending a few sessions, it started to make sense. In fact, this high-level conference should be attended by every CTO in the industry. If you want to know where things are headed, this was the place to be. This was an outstanding event.

CAMEST: a New Industry Council

In conjunction with the conference, I attended a meeting led by Denny Fritz. He and a group of folks that included Dieter Bergman, Gene Weiner, Dan Feinberg, Krista Crotty, Marc Carter, Phil Marcoux and Matt Holzmann, continued work on a new organization, Coalition

for Advancement of Electronic Systems Technology (CAMEST). The effort is designed to build a technology bridge between industry groups like IPC, iNEMI, and SEMI, among others. Specifically, their charter is to identify and close the technology gaps that exist between these industries and serve as "the glue among associations and consortia." Here's what they say about their reason for doing this:

"The purpose of this council is to promote a strategic partnership among organizations interested in the total solution for interconnecting, assembling, packaging, mounting and integrating system design by increasing global awareness."

Here's their mission statement:

"CAMEST is dedicated to the identification and dissemination of the critical technology application knowledge needed for the further development of the electronics industry. This organization identifies gaps in design, manufacturing, test and reliability across all aspects of electronic component assembly and subsystem manufacturing from semiconductor to final assembly, and facilitates cooperation among industry, academia, government and existing consortia to deliver solutions."

It seems to have a noble purpose. I'm still not clear on the difference between CAMEST and iNEMI, but perhaps Denny Fritz's feature in this month's issue of *The PCB Magazine* will help clarify that. Regardless, here's what iNEMI states as its mission:

"The International Electronics Manufacturing Initiative's mission is to forecast and accelerate improvements in the electronics manufacturing industry for a sustainable future."

In the iNEMI meetings I've attended and in the interviews I've conducted, I've always come away with the impression that what CAMEST is proposing is what iNEMI is doing. iNEMI identifies gaps in the technologies and puts task teams together made up of major OEMs, EMS providers and even some fabricators to come up with solutions. And with their very long list of [OEM and major supply chain partners](#), they have the clout to make things happen. I believe

CAMEST is more about gathering information about the gaps and then sharing it with iNEMI, HDPUG, IPC and others. Walking hand-in-hand, CAMEST and these groups will likely be a good partnership going forward. And although IPC is lending its support to the new industry council, they are being careful not to make CAMEST an IPC initiative, in order to keep the door open to other industry groups. Since IPC is leading the effort to get this off the ground, they should kick in the initial funding. There was lots of goodwill from the kick-off committee, but they need money to get the tools in place that will create the inertia needed to get this rolling.



Figure 2: OMG's Michael Carano at the ESTC event.

A Bit About Counterfeiting

At ESTC, I was listening to a discussion about counterfeit components. During the Q&A, I asked if it wouldn't it make more sense to go after the counterfeiters instead of spending all this money on inspection, detection and prevention? We know where most of the counterfeits come from...China. And some companies (not governments) pursue the culprits, but the response by CALCE's expert on the subject, [Dr. Diganta Das](#), surprised me. He said that people need to make a living and local governments are reluctant to clamp down on the counterfeiters since they employ a lot of people. And in China, keeping people employed is critical.

I had always seen counterfeiting as sort of an organized crime-driven effort, relegated to obscure warehouses with blacked out windows. But it seems that it's often much more above board, located in traditional factory settings. I knew that Gucci bags, Rolex watches and Calaway Golf clubs were copied out in the open, but I had never placed microprocessors in that same category. Look for a comprehensive discussion of the topic in the September issue of *SMT Magazine*. The article, "Development of a

Methodology to Determine Risk of Counterfeit Use," written by a team from iNEMI and Corealis, will run in two parts.

The organizers of this year's ESTC promise a bigger and better event next year. Whether it's located in Vegas or Silicon Valley, if they're able to put together a stellar conference again, this thing will start to take on a life of its own. I encourage technical leaders to attend this event for two reasons: to get a good look at what's going on around us and to act as representatives from our sectors to make sure the other guys know what we're doing and where we're headed. **SMT**



Ray Rasmussen is the publisher and chief editor for I-Connect007 Publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuitTree Magazine*. To read past columns, or to contact Rasmussen, [click here](#).



Thin Palladium Layers: An Effective Cost-Saving Strategy

**by Olaf Kurtz, Jürgen Barthelmes,
Eckart Klusmann, Robert Rüther,
and Stephen Kenny**

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SUMMARY: *As the price of gold continues to head skyward, palladium becomes more and more attractive for product developers who are worried about their bottom line.*

Introduction

Since 2008, financial market turbulence resulting in severe consequences for economic growth has caused an unprecedented increase in gold prices. Other precious metals such as silver or palladium have also experienced price increases, but the gold price gap has increased significantly. Today, the palladium price is approximately 35–40% of gold, with platinum just below and now losing its position as the most expensive precious metal.

Palladium provides a highly active catalyst surface for chemical reactions and the majority of its applications are found in the automotive

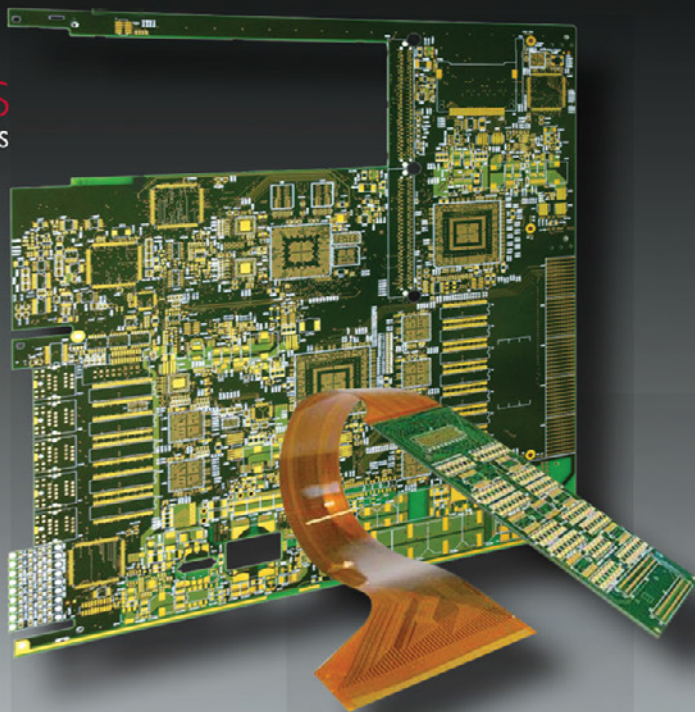
and electronics industries. Other uses include hydrogen reserve (e.g., for fuel cells) and also medical engineering. Palladium has further gained importance² in the course of conversion to more sustainable products as it provides a non-allergenic alternative to nickel as used in decorative and technical applications. Palla-



Figure 1: Price trend for palladium over the past three years¹.



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THIN PALLADIUM LAYERS: AN EFFECTIVE COST-SAVING STRATEGY *continues*

dium has also played a much more important role in the electronics industry since the July 2006 EU standard 2002/945/EC came into effect, regarding restricting the use of hazardous substances^{3,4,5}.

As a result of the high and volatile precious metal prices, further optimisation of palladium coatings for their respective applications is needed to maintain the same function at minimum thickness.

Palladium is used in the lead frame industry as part of a whisker-free coating system (e.g., Ni/Pd/Au pre-plated lead frames), replacing both tin and silver, providing ultra-thin deposition of 20–50nm.

These technical applications require excellent reliability, linearity of deposition rates and characteristics, lowest porosity and highest corrosion resistance for minimum thickness. However, as a real alternative to nickel, this system has to provide an effective diffusion barrier layer with low porosity whilst ensuring excellent corrosion and abrasion resistance properties. Palladium is already being tested and used as an alternative to nickel for allergenic applications such as jewellery and mobile phone covers.

The designation for palladium originates from the Greek goddess Pallas Athena, representing wisdom, strategy and battle. Whether the use of palladium is always wise, one cannot say; however, in times where the gold market significantly and profoundly changes, it can prove to be cost-effective and efficient due to the reduction in gold applications.

This document describes a process for the deposition of pure palladium coatings with improved porosity characteristics. Using identical porosity testing technique previously undertaken by Texas Instruments (TI) for conventional palladium coatings, the deposition characteristics were thoroughly studied using the quartz crystal microbalance. Low thickness barrier properties to 50nm were studied by means of contact resistance measurements after heat treatment at 300°C for one hour using the Ni/Pd/Au layer system.

This article demonstrates that this system also meets all technical soldering and bonding requirements for low palladium thickness.

Bonding characteristics were further tested using copper as replacement for the traditional gold wire, demonstrating an additional savings potential.

Palladium Electrolyte

The pure palladium process* used in this investigation is a neutral pH electrolyte that has been especially designed for use in reel-to-reel as well as conventional rack and barrel applications within a wide temperature range of 20–50°C. Pallacor® HT* produces bright, haze-free palladium within a thickness range of several nanometers to 10 microns that can be used as final or intermediate coatings, particularly for nickel-free applications. The chloride content has also been significantly reduced to minimize the corrosive nature of the electrolyte.

Summary of electrolyte parameters:

- Neutral pH electrolyte (pH 6.8–7.5)
- Pd content = 5–10 g/l
- Temperature = 20–50°C
- Deposit hardness = 250–270 HV25
- Purity: 99.7–99.9% w/w palladium

Deposition Characteristics

Deposition rate and coating information for the Ni/Pd/Au layer system may be obtained by means of a quartz crystal microbalance (QCM)^{6,7,8}. The QCM is a very sensitive analytical method that permits the in-situ detection of interfacial processes (e.g., weight gain by surface electrodeposition).

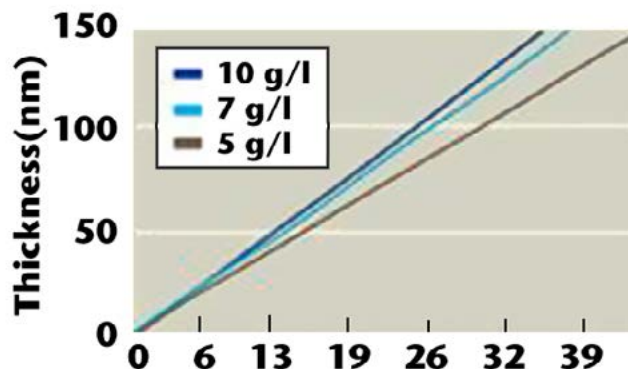


Figure 2: Deposition rate at varying g/l Pd, carried out at 1 A/dm², room temperature.

THIN PALLADIUM LAYERS: AN EFFECTIVE COST-SAVING STRATEGY *continues*

A high degree of deposition rate linearity is crucial for the replication of low thickness coatings. Figure 2 provides further deposition rate data at varying palladium concentration.

Within this study, the new palladium process provides a very high linearity of deposition rate and infers exceptional low thickness reproducibility.

Porosity Measurement

Porosity was measured for palladium thickness of 5, 10, 20 and 50nm applied to a 0.4 μ m nickel deposit. The results were compared to those from a conventional palladium electrolyte. Tests were carried out using copper alloy lead frames. The following table outlines the chosen process sequence.

The TI porosity test was used for test sample examination which involved placing onto a pre-heated (450°C) hot plate for five minutes. After cooling to room temperature (RT), the edges are sealed with paraffin wax (Figure 6).

The sealed lead frame is then immersed into a 1N (0.5M) sulphuric acid solution for five minutes, followed by the AAS determination of any dissolved copper. Hence, porosity is expressed

Process
Soak cleaning
Cathodic cleaning
Activation
Ni-plating
Pd-plating
TI-Porosity Test

Table 1: Porosity test process sequence.

in $\mu\text{g}/\text{cm}^2$ for the dissolved copper correlating directly with the deposit porosity characteristic. Figure 4 compares the results for the new palladium process to those from a conventional Pd process. A significant porosity reduction can be clearly seen for the new process at very low thickness (to 20nm).

Six repeat measurements were carried out for each layer thickness examination showing that the new process provides minimal standard deviation variance and consequently greater reproducibility of deposit thickness.



Figure 3: Sealed heat-treated lead frames prepared for TI porosity testing.

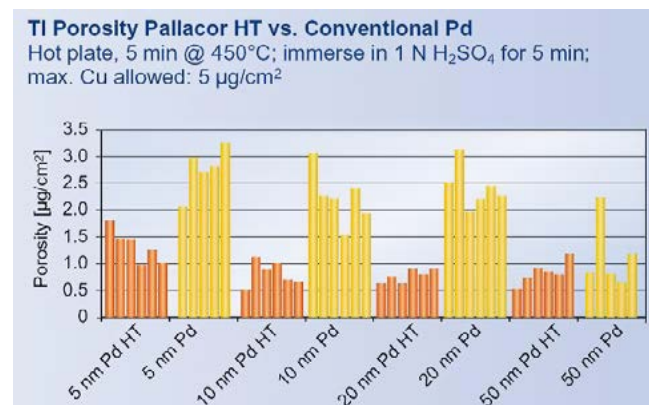


Figure 4: Reduced porosity at lowest possible thickness with the new palladium process.

THIN PALLADIUM LAYERS: AN EFFECTIVE COST-SAVING STRATEGY *continues***Solderability Testing**

Solderability testing of Ni/Pd and Ni/Pd/Au deposit combinations was undertaken using a solder balance, providing detailed wetting diagrams for the determination of wetting rate and force.

The following shows the various thickness combinations for each metal coating:

Nickel: 0.4, 0.7, 1.0µm
 Palladium: 5, 10, 20, 50nm
 Gold: 0, 5, 10, 20nm

The following solder balance parameters were applied:

Flux: Litton Kester 950E3.5
 Solder: Sn95.7-Ag3.8-Cu0.5.
 Solder temperature: 245°C
 Immersion depth [mm]: 8.5
 Immersion rate [mm/s]: 21
 Duration [s]: 5

Again, deposits from the new palladium process were compared to those from a conventional process. The following graphs show the zero crossing times (ZCT) provided from the corresponding wetting curves.

The results highlight the various deposit thickness combinations. Figure 5 shows a ZCT

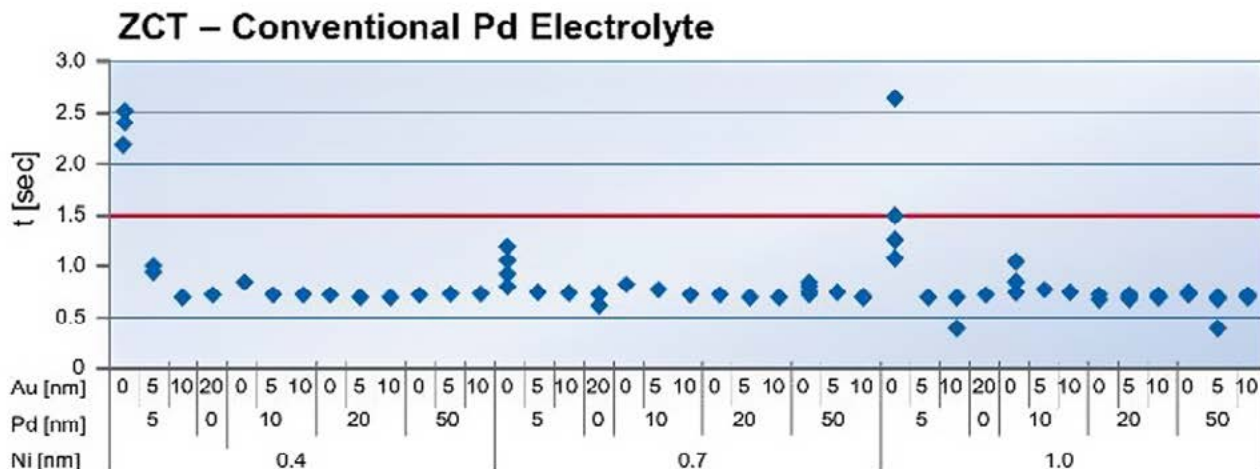


Figure 5: Solderability studies for nickel, conventional palladium and gold combinations.

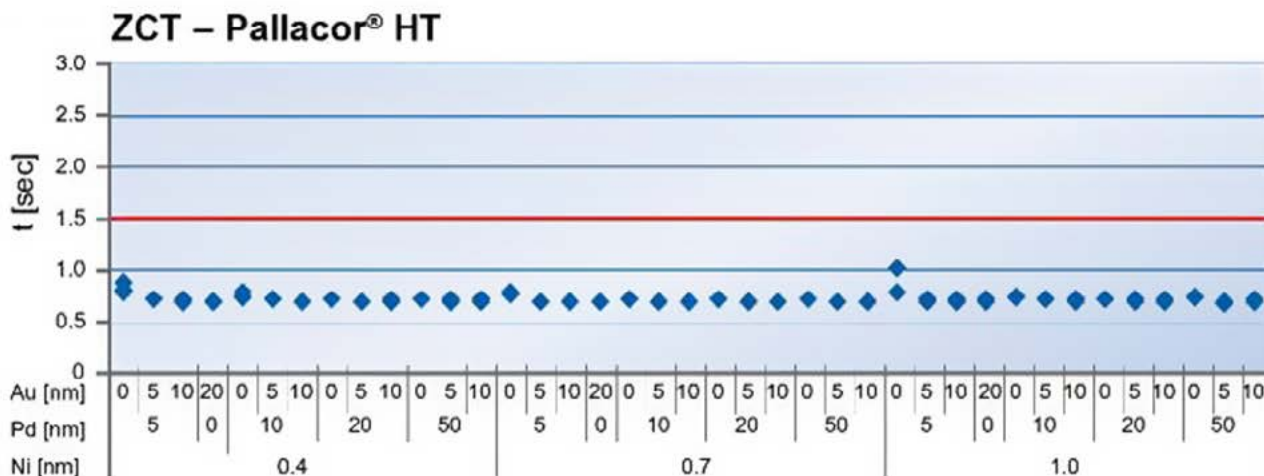


Figure 6: Improved wetting behaviour and reduced ZCT for the Pallacor® HT* deposit combinations even at lowest palladium thickness without gold.

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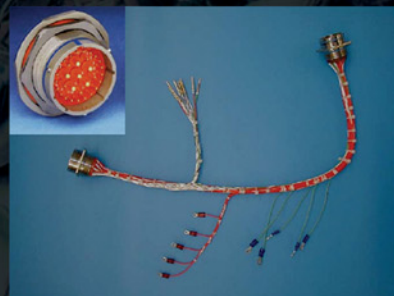
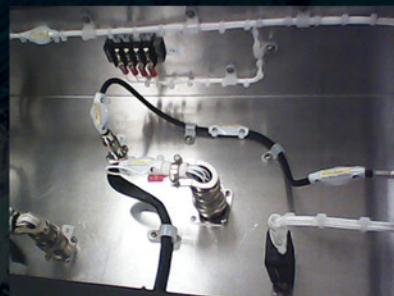
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for the conventional palladium process. A ZCT of 2.5–3s is observed when the final gold coating is omitted at the lowest palladium thickness of 5nm.

Very reliable and constant wetting times were achieved with Pallacor® HT* over the entire thickness combination range (Figure 6).

Effectiveness of Palladium as Barrier Layer, Before and After Heat Treatment

The following investigation was carried out to demonstrate the barrier effectiveness at low thickness as a result of the previous porosity reduction findings⁹.

Test specimens used in the following examinations comprised copper base material deposited with:

- 5µm Ni
- 1µm Pd
- 0.1µm of various gold alloys (AuCo, AuNi, AuFe) and pure gold.

Contact resistance of each sample was measured to study barrier effectiveness in the 'as plated' condition and after heat treatment at:

- (i) 300°C for five minutes and
- (ii) 300°C for one hour

The mean value from 30 measurements was used for each test sample.

After heat treatment at 300°C for one hour, significant increases in contact resistance were observed in the absence of a palladium barrier layer (Figure 7). This increase in contact resistance results from the diffusion of nickel onto the gold surface and its subsequent oxidation¹⁰.

When a palladium barrier layer is used, no significant increase in contact resistance was observed, even after heat treatment for the maximum duration of one hour. This applied to all gold deposit types used (Figure 8).

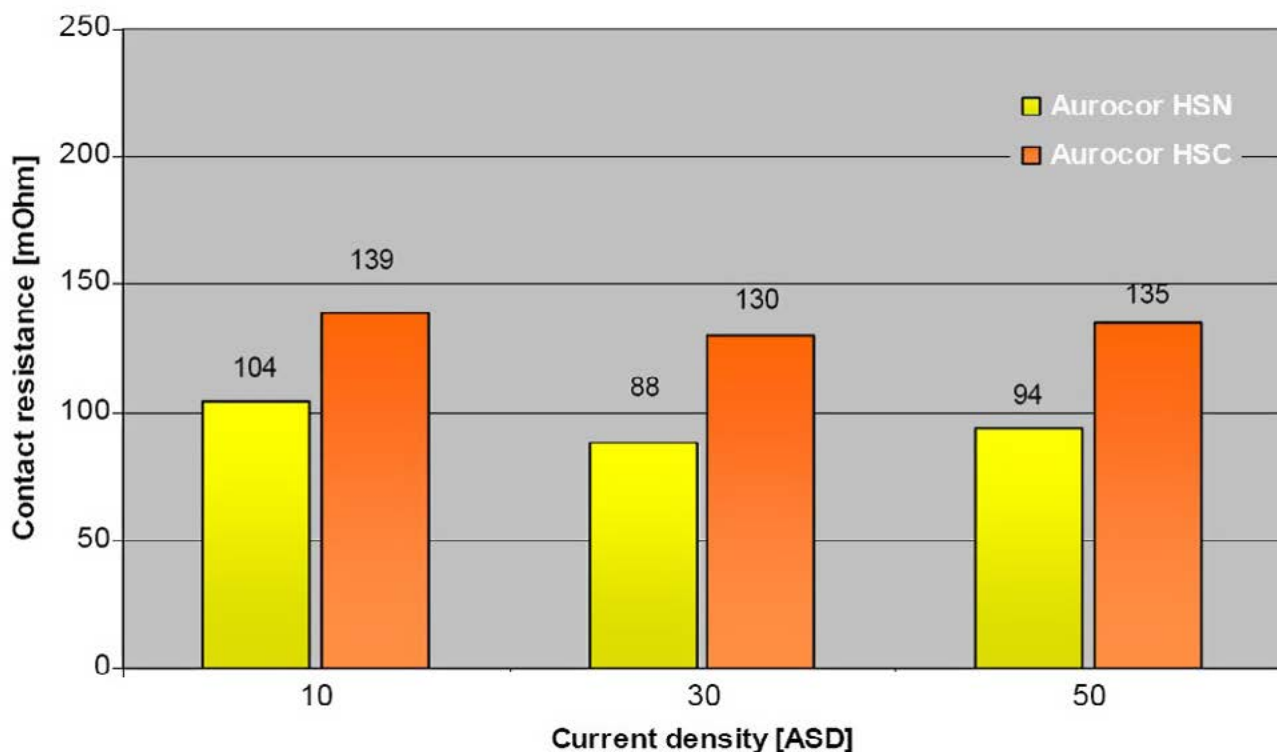


Figure 7: Contact resistance of Au/Ni & Au/Co deposit alloys in the absence of a Pd barrier layer after heat treatment at 300°C for one hour¹⁰.



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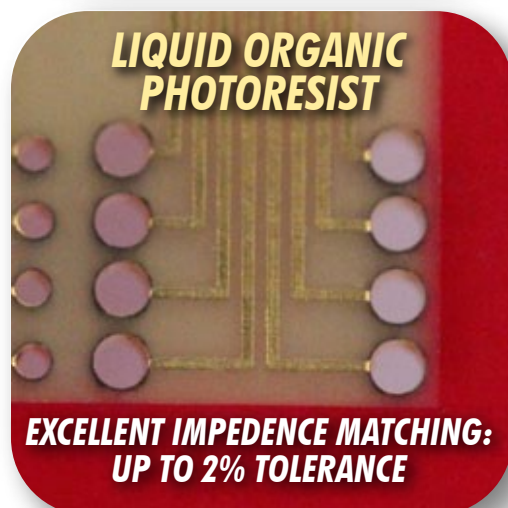


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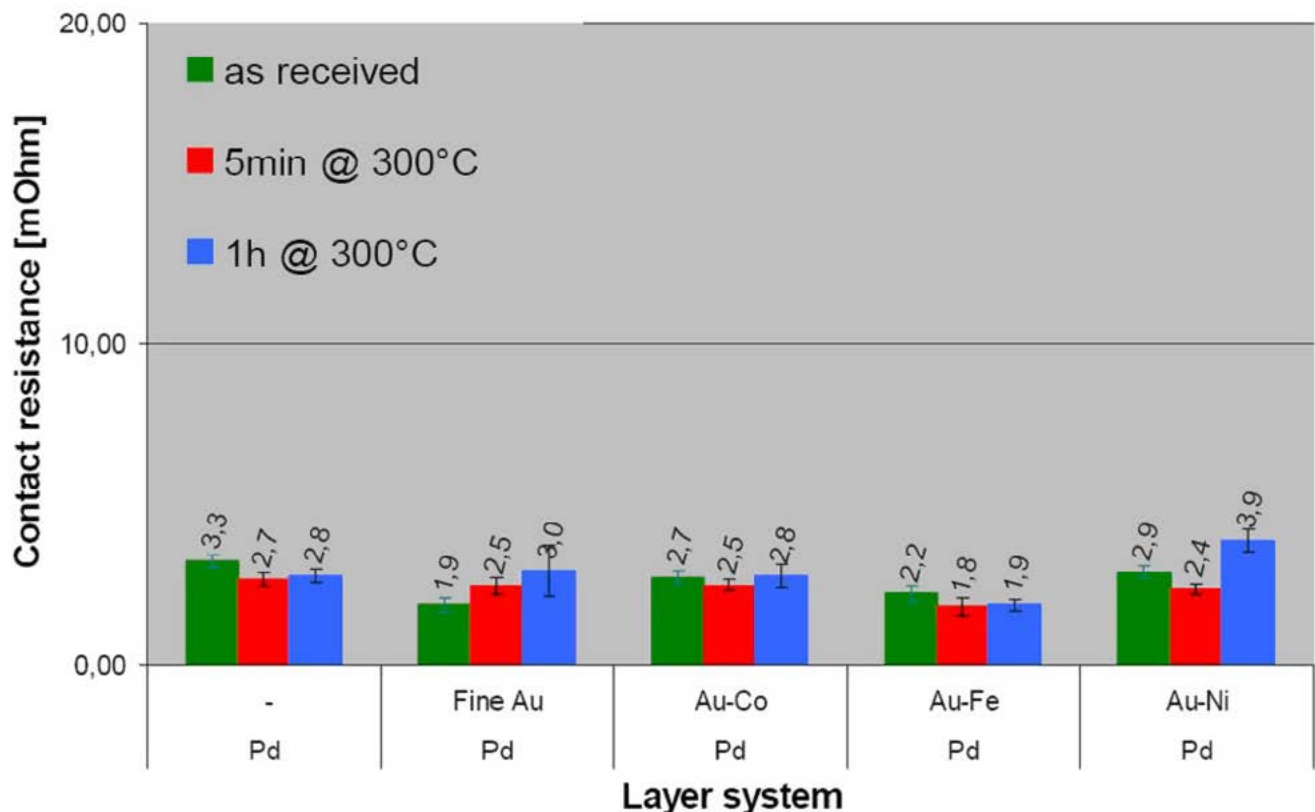


Figure 8: Contact resistance of various gold deposit types with a Pd barrier layer, before and after heat treatment.

Further examinations were carried out at reduced palladium barrier thickness of 100 and 50nm. Results further highlighted a stable barrier effect even at such low thickness.

Copper Wire Bonding Investigations

The observed exceptional barrier property of the palladium deposit was further investigated as part of a final finish comprising electrolytic nickel followed by palladium and then gold. Copper wire bonding results were compared with the industry standard for electrolytic final finish for packaging applications, plated nickel and gold. Normally a plated gold layer at 0.3µm is required to ensure reliable bonding results; this system was compared to a plated gold layer of 0.1µm and also using the new final finish with 0.1µm of palladium followed by 0.1µm of gold. Conventional gold wire, together with copper wire of thickness 0.8 mil (corresponding to about 20µm), was used for testing.

The following combination systems were investigated:

1. Ni (7µm)/ Au (0.3µm)
2. Ni (5µm)/ Au (0.1µm)
3. Ni (5µm)/ Pd (0.1µm)/ Au (0.1µm)

During testing the following bonding parameters were varied:

- CV: Tool speed (minch/ms)
- USG: Ultrasonic generator (mA)
- Force in g

For each combination, 40 wires were bonded; 20 in 'x' direction and 20 in 'y' direction. Bonding strengths were measured before and after heat treatment at 150°C for four hours. Figure 9 shows bonding strength in g for each combination system and parameter variation. The Ni/Pd/Au system provides the highest pull strength at a reduced gold layer thickness.

THIN PALLADIUM LAYERS: AN EFFECTIVE COST-SAVING STRATEGY *continues*

Ni μm	Pd	Au μm	0.45	0.45	0.35	0.45	0.45	0.55	0.45	0.45	CV
			40	30	40	40	40	40	50	40	F
			130	155	155	155	155	155	155	180	USG
7.2	-	0.3	5.9	6.2	7.2	6.1	6.5	6.2	5.5	6.4	
5.4		0.1	4.7	5.5	5.5	5.8	5.3	5.9	5.6	6.1	
5.4	0.1	0.1	6.8	8.4	8.3	7.0	7.3	7.0	7.4	6.4	

Average < 4 g pull strength	Average < 5.5 g pull strength	Average > 5.5 g pull strength
-----------------------------	-------------------------------	-------------------------------

Figure 9: Pull strength for each combination system and parameter variation before heat treatment.

Ni μm	Pd	Au μm	0.45	0.45	0.35	0.45	0.45	0.55	0.45	0.45	CV
			40	30	40	40	40	40	50	40	F
			130	155	155	155	155	155	155	180	USG
7.2	-	0.3	6.4	4.9	7.7	6.8	5.8	6.9	3.6	6.9	
5.4		0.1	4.3	5.5	6.1	5.6	5.1	6.1	4.7	6.1	
5.4	0.1	0.1	6.2	7.4	7.8	6.6	6.9	7.0	7.2	6.8	

Average < 4 g pull strength	Average < 5.5 g pull strength	Average > 5.5 g pull strength
-----------------------------	-------------------------------	-------------------------------

Figure 10: Pull strength for each combination system and parameter variation after heat treatment at 150°C for four hours.

Figure 10 summarizes the results of further bonding tests after a heat treatment simulating the aging process.

Even after artificial aging the Ni/Pd/Au system tested satisfies all bonding requirements with consistent reliability and also gave the

highest average pull strength results. In contrast the final finish with only gold gave less uniform bonding strength and on average the bonding result with thinner gold layer thickness was lower than with 0.3μm plated gold. This result shows that simply reducing the gold plated

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thickness is no answer to the demand to reduce cost as the process quality is not assured. Use of nickel, palladium and gold however offers a low-cost alternative with potential to improve the bonding quality.

Summary and Prospects

Palladium can be efficiently used for cost savings by lowering the overall gold layer thickness. However to achieve maximum benefit the palladium deposit characteristics should be defined including the minimum porosity acceptable. In this paper palladium deposition has been monitored and investigated by using QCM during the build-up of a Ni/Pd/Au sandwich system. For the used palladium electrolyte a strict linear deposition characteristic was proven at a palladium concentration of 5g/l. In addition, the deposition rates and the current efficiencies have been measured as a function of Pd concentration and bath agitation.

Deposit porosity has been examined with the TI porosity test of Ni/Pd/Au for different layer thicknesses. Palladium thicknesses of 5, 10, 20 and 50nm were deposited onto a 0.4µm nickel coating on the copper alloy lead frame specimens. The coated specimen was first heated for five minutes at 450°C. The lead frame sealed in this way was then immersed into a 1N sulphuric acid solution for five minutes. The copper concentration in the sulphuric acid solution was then determined by atom absorption spectroscopy (AAS).

In comparison to a benchmark process the investigated palladium deposit shows a significantly lower porosity. Subsequent solderability investigations were carried out using a 'wetting balance', providing detailed wetting speed and wetting force information. A coating combination nickel/palladium/gold was used for these investigations, with variation of the individual metal thickness. The good diffusion barrier effect of palladium at even very low thickness has been tested in contact resistance measurements for 1µm, 0.1µm and 0.05µm before and after heat treatment up to 300°C for one hour. The results highlight the excellent barrier property independent of the type of gold electrodeposit.

Finally the excellent barrier effect with palladium was demonstrated in Au layer reduction

in wire bonding tests. In this study both gold and copper wires were used and the Ni/Pd/Au layer system with 0.3µm and 0.1µm gold layer thickness was benchmarked against a Ni/Au system with 0.3µm thickness deposited gold. The palladium layer thickness was chosen at 0.1µm. The experiments show the pull strength before and after artificial aging for one hour at 150°C. All results show that the use of palladium ensures at least the same or better and more reliable results with a significantly lower gold layer thickness. **SMT**

* Pallacor® HT, Atotech Deutschland GmbH

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THIN PALLADIUM LAYERS: AN EFFECTIVE COST-SAVING STRATEGY *continues*

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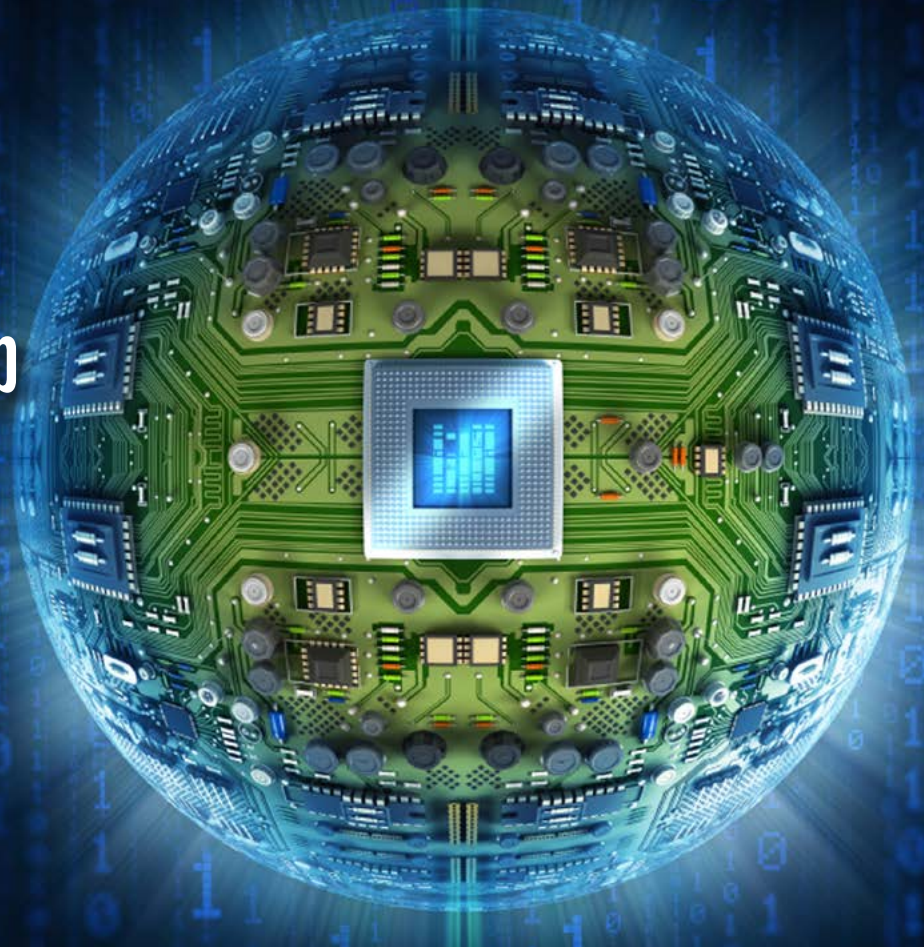
Shen Hwang, global marketing manager for CyberOptics, discusses the company's newest AOI and SPI equipment, and updates us on the firm's recent reorganization and new marketing strategy.



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Evaluation of Molded Flip-Chip BGA Package for 28nm FPGA Applications



by Altera Corporation, Amkor Technology USA, and Amkor Technology Korea*

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Abstract

As the FPGA device technology migrates to 28nm technology node and high-performance applications, selecting the right package to meet the customer usability requirements and to achieve product reliability goals becomes important. This paper describes the process used in selecting and qualifying the molded flip-chip BGA for cost effective, high-performance 28nm FPGA devices. A collaborative approach in partnership with the assembly manufacturer was employed to develop customer collateral that includes handling, reflow/rework and heatsink attach guidelines for the molded flip-chip BGA package. A detailed thermal modeling of the package was performed to characterize the thermal performance of the package. In addition, compressive loading characterization, component level and board level reliability tests were carried out to validate the long term reliability performance of

the package in customer use conditions. The results of this study demonstrate that the molded flip-chip BGA package is a cost-effective, high-reliability solution for 28nm FPGA devices.




Introduction

Altera has introduced Arria®-V FPGA product family at 28nm technology node to deliver optimized balance of performance, cost and low power for mid-range applications. In order to meet the device performance and cost goals, selection of packaging technology has become important. The package selected must meet the customer usability requirements and achieve product reliability goals. This paper describes the process used in selecting and qualifying the molded flip-chip BGA package for cost effective, high performance 28nm FPGA devices. To match the low-power, high-performance and low-cost requirements of the 28nm Arria-V FPGAs, a new package platform offered by Amkor Technology, molded flip-chip BGA (Amkor acronym: FCmBGA, Altera acronym: TCF-CBGA, Thermal Composite Flip-Chip BGA) was selected. Having an exposed die configuration, FCmBGA inherently offers a low profile form




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EVALUATION OF MOLDED FLIP-CHIP BGA PACKAGE FOR 28NM FPGA APPLICATIONS *continues*

factor. Further the exposed die allows customers flexibility with respect to thermal dissipation solutions. Finally, the replacement of capillary underfill (CUF) with molded underfill (MUF) allows coverage of the 28nm FPGA family with a single package configuration.

In subsequent sections we will describe the methodology for package selection as well as various tests run to provide application guidelines for customers using this package platform. Results for handling during shipping, SMT attach and rework results will be discussed. Heatsink attach/ rework and thermal modeling will also be reviewed. Compressive loading and well as component and board level reliability results will be summarized.

Package Selection

In order to make the decision about selecting the packaging platform for the 28nm FPGA application, a comprehensive matrix of package requirements was designed and the corresponding data was collected (Table 1).

Package profile is an important consideration, especially as more applications require thin form factors. Both FCmBGA and bare die packages offer thinner package profile form factor than a single

piece lid package, however, as the package gets thinner, bare die packages are limited on body size and die size. This is due to the coplanarity requirement. FCmBGA adds additional support to the die by coupling the MUF to the substrate. This in turn helps control package warpage/coplanarity and allows for thinner larger packages with larger die. Another gain from the molding compound around die is the package robustness compared to the bare die format. This advantage offers many benefits during component handling such as shipping, electrical test, board mounting, rework and heatsink attach. FCmBGA package is advantageous from the point of view of 28nm FPGA family coverage.

Typically, a range of die and body sizes are deployed with each new FPGA family. With FCmBGA package, one package type can cover the entire family. Another benefit of FCmBGA over single-piece lid and bare die is keep out zone (KOZ) requirements. Both single-piece lid and bare die packages use CUF. CUF requires 2–3 mm KOZ between the die and on board passives. This is to prevent partial filling of the on board passive solder joints by the CUF, which can lead to solder joint fracture during tempera-




Feature	Single Piece Lid	FCmBGA	Bare Die
			
Package Profile	GOOD	BETTER	BETTER
Room for Passives	GOOD	BEST	GOOD
Coplanarity	BEST	BETTER	GOOD
Bump Reliability	GOOD	BEST	GOOD
BGA Reliability	BEST	BEST	GOOD
Heat Sink Attach Surface	BEST	BETTER	GOOD
Thermal Performance with Heat Sink	BETTER	BEST	GOOD
Cost	GOOD	BETTER	BEST

Table 1: Package selection matrix.

EVALUATION OF MOLDED FLIP-CHIP BGA PACKAGE FOR 28NM FPGA APPLICATIONS *continues*

ture cycle condition B testing¹. FCmBGA uses MUF to encapsulate the on board passives and around the die. Thus, the KOZ for FCmBGA package is less restrictive, 0.6mm.

The FCmBGA mold cap is designed to be below the attached die height. This allows the thinnest bond line thickness, BLT, and thus the best thermal performance. Work was done with several commercially available heatsinks and TIM II materials to illustrate how heatsinks can be attached to FCmBGA. Rework of the heatsink was also performed to demonstrate the ruggedness of the molded package. Thermal performance was evaluated through FEM modeling.

Like with any new package platform, demonstrating that the package meets the customer reliability requirements is important. The industry standard component level and board level reliability tests were run to compare the FCmBGA performance to single piece lid and bare die control packages. The package performed well in direct head-to-head comparisons.

Collaboration to Develop Customer Collateral

With selection of new package type for the 28nm FPGA product family, it was essential to develop customer collateral to ensure that the package meets the customer usability requirements. The objective of customer collateral is to provide the guidance to the customers for

component handling, board level assembly and rework and develop the heatsink attach and rework process. We collaborated to develop the customer collateral by running joint evaluations on the test vehicles assembled in the FCmBGA package. Additionally, accelerated component level and board level reliability testing was run to verify the package integrity in the customer use conditions.

Selection of Test Vehicles

In order to evaluate and characterize the FCmBGA package ahead of 28nm FPGA product release, test vehicles were required to be selected for evaluations. The criterion for the test vehicle selection was that the die size and package size of the test vehicle should be closer to the largest die/package size combination for the 28nm FPGA family.

After reviewing the number of test vehicles available for testing, a 90nm FPGA device was selected for assembly process, handling guidelines, heatsink attach, mechanical characterization and component level reliability tests. A full stack 40nm daisy chain test vehicle was selected for board reliability testing. The details of the test vehicles are outlined in Table 2.

To carry out the board level characterization experiments, a development board representing typical customer assembly board was selected. The PCB was designed per IPC-9701 guidelines²

	Test Vehicle - 1	Test Vehicle - 2
Device	Full Stack 40nm Daisy Chain	90nm Altera FPGA
Die Size	22 x 19 mm ²	19.24 x 22.17 mm ²
Bump Pitch	170mm	225mm
Bump Alloy	Eutectic (Sn/Pb)	Eutectic (Sn/Pb)
Package	F1681 FCmBGA	F1508 FCmBGA
Package Size	42.5x42.5 mm ²	40x40 mm ²
Assembly	Amkor	Amkor
Rel Test	Altera	Altera

Table 2: Characterization test vehicle details.

EVALUATION OF MOLDED FLIP-CHIP BGA PACKAGE FOR 28NM FPGA APPLICATIONS *continues*

Figure 1: Assembly and characterization development board.

with 330mm x 114mm size, 2.3mm thickness, 8-layer stackup board as shown in Figure 1.

FCmBGA Handling Characterization (Tray Drop Test)

FCmBGA packages do not require a tray design different than those already available for standard FCBGA bare die (lidless) packages. In fact, the same tray can be often used for an equivalent bare die and FCmBGA package since both packages are lidless and have roughly the same height due to identical package stack ups (though coplanarity is likely lower with a FCmBGA style package). The FCmBGA mold cap is below the die so it will not interfere with a standard JEDEC style tray design. In the below work, FCmBGA packages were tested for integrity after dropping them in bundled trays. After

testing, both package and trays were inspected for damage. Three packages with three different body sizes were tested: 31, 35 and 40mm packages were tested. All packages shared the same die size.

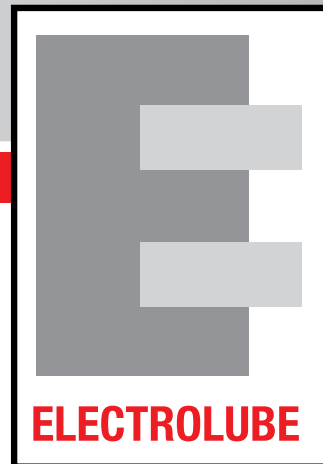
Test Procedure

Five trays were fully populated with packages and a sixth tray was added as a cover tray. All trays were banded together three times with a standard polypropylene band, bagged in an antistatic band, and then boxed. The box was then dropped from a height of 120cm. The packages and trays were inspected before and after tray drop. The results of the tray drop tests are summarized in Table 3. The visual inspection of the devices after tray drop testing showed no defects, as shown in Figures 2a and 2b.

Package Type	Body Size (mm)	Die Size (mm)	Package Damage	Tray Damage
FCmBGA	31	19 x 14	0/118	0/6
	35		0/120	0/6
	40		0/105	0/6

Table 3: Tray drop test summary and results.

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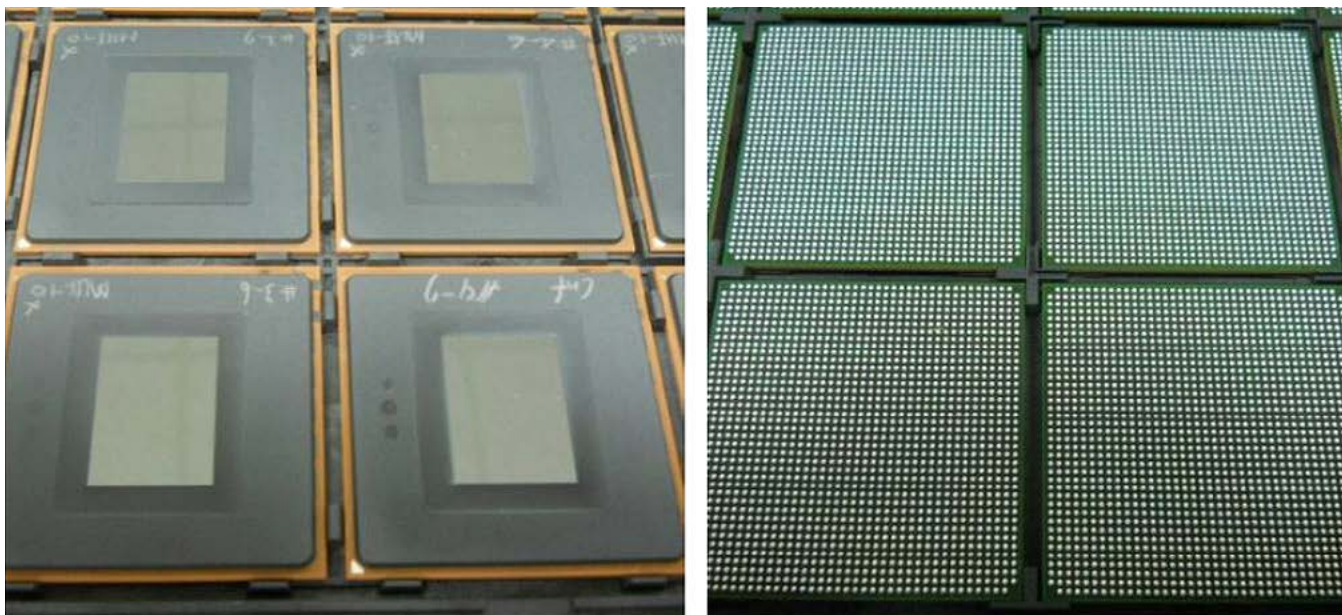
EVALUATION OF MOLDED FLIP-CHIP BGA PACKAGE FOR 28NM FPGA APPLICATIONS *continues*

Figure 2a and 2b: Top (left) and bottom side (right) of package after the tray drop test.

SMT Reflow Characterization

The SMT reflow characterization experiments conducted at a preferred SMT sub-contractor showed that the FCmBGA package follows the same SMT practices of single-piece lid and bare die packages. The same PCB designs are used. Typical surface finishes, such as organic solder preservative, OSP with eutectic or lead free solder paste may be used.

As with other flip-chip packages, a proper thermal profile is required to achieve good BGA balls collapse. Calibrated thermocouples should be used to instrument a reflow profile board and use it to develop an optimized thermal profile of the package on board.

Figure 3 shows the typical reflow profile used for assembling the FCmBGA on the PCB. The comparison of the reflow profiles for FCmBGA and the lidded flip-chip BGA (single piece lid, or SPL) package shows that the reflow profiles are quite similar and fall

within the range of reflow parameters defined in table 5-2 of JEDEC standard J-STD-020³.

After the assembly process was completed, the mounted devices were inspected to verify solder joint integrity. Visual inspection of the solder joints along the package edge and corners showed well-formed solder joints. One device

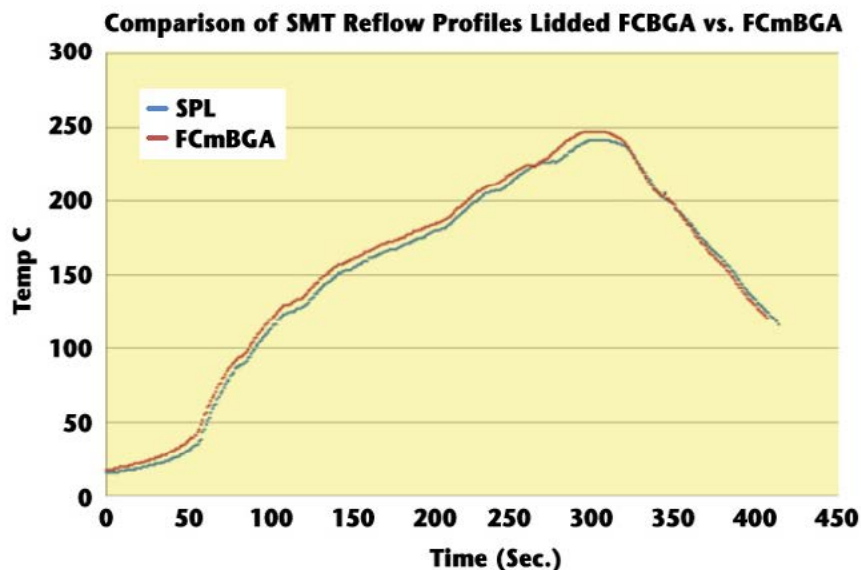


Figure 3: Reflow profiles of FCmBGA vs. lidded-FCBGA.

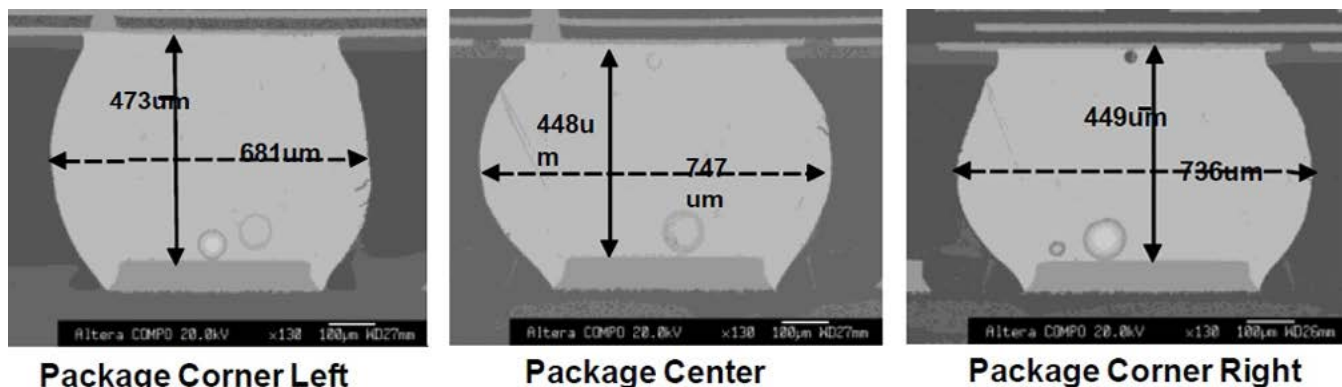
EVALUATION OF MOLDED FLIP-CHIP BGA PACKAGE FOR 28NM FPGA APPLICATIONS *continues*

Figure 4: FCmBGA solder joints after SMT reflow.

was cross-sectioned along the package edge to determine the shape and the size of the solder joints formed during SMT. Figure 4 shows that the solder joints have consistent solder joint shape across the package edge and the center.

SMT Rework Characterization

Localized SMT rework of BGA components is typically performed by customers to replace defective parts or upgrade the device to latest version. Localized attach of FCmBGA packages is possible with industry standard BGA rework machines. Like with SMT attach, a profile board with properly attached calibrated thermocouples is required to develop an optimized reflow profile.

The experiments conducted to develop the localized attach reflow profile showed that the reflow parameters were well with the parameters as defined in JEDEC standard J-STD-020. However, when compared with the lidded FCBGA,

one significant difference was found. Since the FCmBGA package has exposed die surrounded by the mold cap, the heat transfer from the top heater through the package to the solder joints is uneven. Consequently, the ball collapse along the periphery of the package is difficult if only the top heater is used. However, the uneven heat transfer from the top of the package can be compensated by increasing the heat from the bottom heater of the rework machine. With optimized top and bottom heater settings, an optimized reflow profile for localized attach of FCmBGA package was developed in this study.

The devices attached with localized reflow process were visually inspected along the package edge and corners. The visual inspection shows well-formed solder joints.

One device was cross-sectioned along the package edge to determine the shape and the size of the solder joints formed during localized reflow. Figure 5 shows that the solder joints

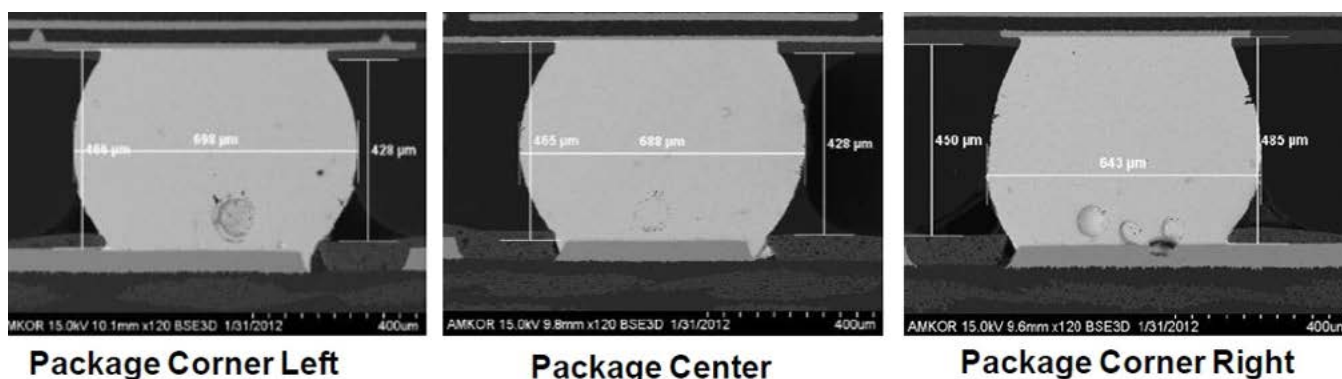


Figure 5: FCmBGA solder joints after localized attach.

EVALUATION OF MOLDED FLIP-CHIP BGA PACKAGE FOR 28NM FPGA APPLICATIONS *continues*

have consistent solder joint shape across the package edge and the package center.

Heatsink Attach and Rework

The process of attaching a heatsink to the FCmBGA package and subsequently removing the heatsink (to rework the board) is identical to that of a standard bare die or lidded FCBGA package. In this characterization work, heatsinks were attached using two different thermal interface materials (TIMs): double-sided thermal tape and thermally conductive epoxy. Six packages were evaluated for each thermal interface material. After attach and removal steps were completed, visual and SAT inspection were used to inspect for damage to the die or delamination at the passivation or EMC layers. Results show that the heatsink can be attached and re-

moved without damage to the package or die. In the FCmBGA package, the mold compound around the die offers additional surface area for increased adhesion and thermal conduction and no die chipping was observed in our evaluation.

Heatsink Removal with Double-Sided Thermal Tape

This particular adhesive tape is a popular double-sided thermally conductive adhesive tape. It is rated as reworkable by the supplier. Six heatsinks were attached and removed using the supplier's recommended method. All units were inspected with SAT imaging before and after testing. No failures or changes in package quality were detected. Figure 6 shows the process flow and the images of each process step during heatsink rework.

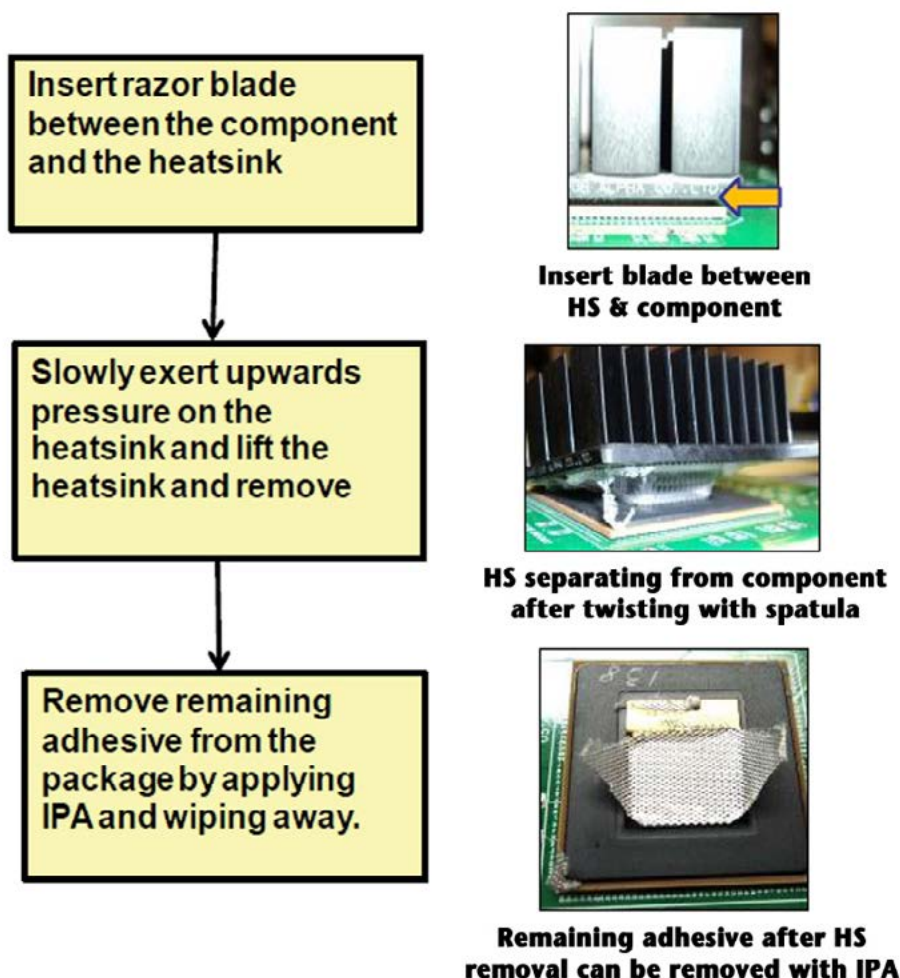
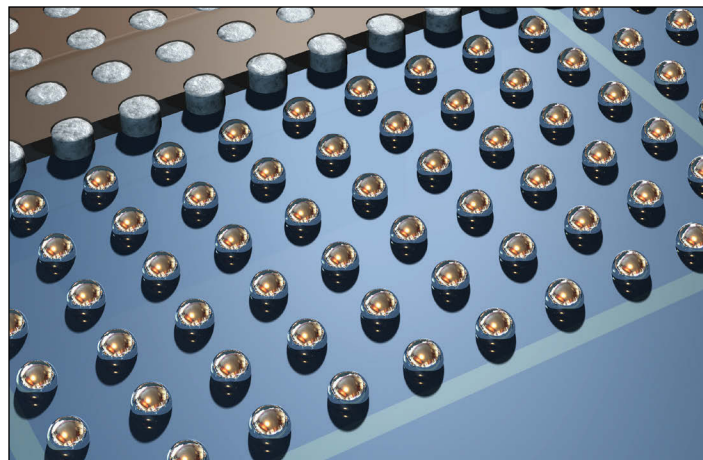
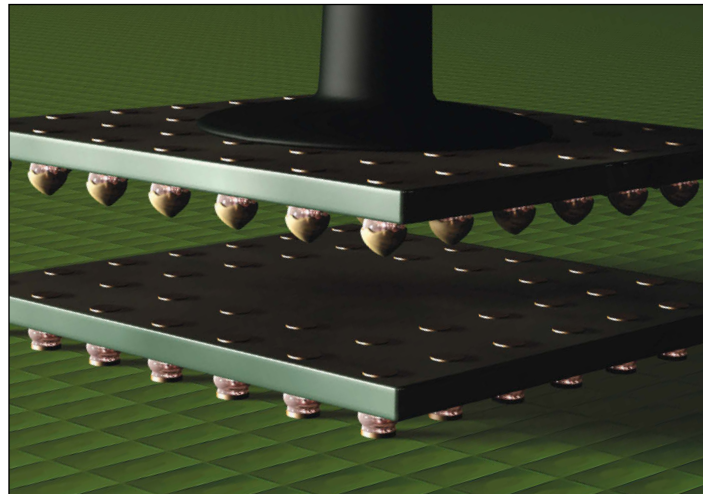


Figure 6: Thermal tape rework process flow.

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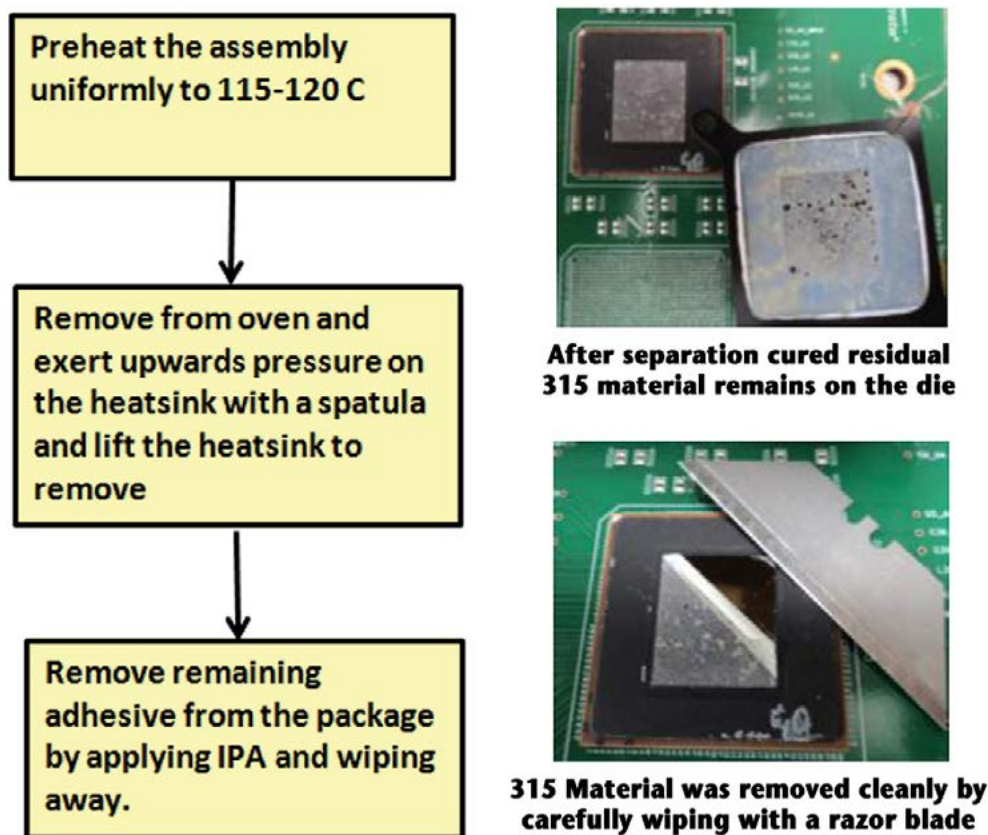
EVALUATION OF MOLDED FLIP-CHIP BGA PACKAGE FOR 28NM FPGA APPLICATIONS *continues*

Figure 7: Thermal epoxy rework process flow.

Heatsink Removal with Thermally Conductive Epoxy

This TIM is a thermally conductive epoxy material. The heatsink attach and the removal process was found to be identical to the lidded FCBGA package. Figure 7 shows the process flow and the images of each process step during heatsink rework.

Thermal Modeling

Detailed thermal modeling of various flip-chip packaging options was performed using commercially available CFD tool.

The analysis was performed to compare the thermal performance of the FC-mBGA with bare die FCBGA and single-piece-lid FCBGA (FCLBGA). The package con-

figurations are depicted in the Figure 8.

The package construction details used for the simulations are outlined in the below Table 4. The packages were mounted onto a JEDEC 1S2P board and the simulation boundary was assumed to be a JEDEC still air chamber. Also, the package top surface was interfaced with a thin sheet of aluminum (100 x 100 x 1 mm³) using a TIM-II material (0.5C-

Package Construction Details	
Body (mm)	40
Die Size (mm)	16 x 20 x 0.786
Substrate Construction	2-2-2
Cu Lid thickness for FCLBGA (mm)	0.5

Table 4: Package construction details.

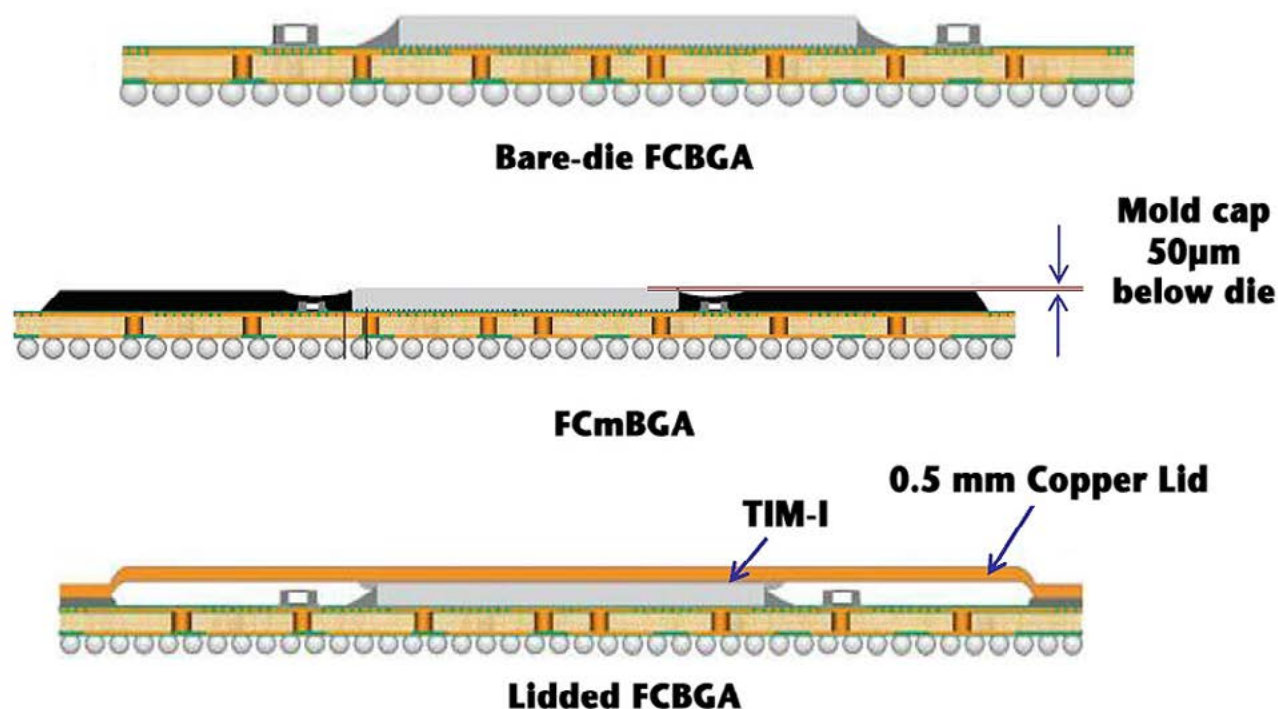
EVALUATION OF MOLDED FLIP-CHIP BGA PACKAGE FOR 28NM FPGA APPLICATIONS *continues*

Figure 8: Flip-chip package configurations considered in this work.

Package	Mold Compound (W/mK)	Power (W)	TIM-II Material (Thermal Impedance)	Theta-JA (C/W)
Bare Die FCBGA	N/A	14	0.5 C*in ² /W	5.83
FCmBGA	0.7			5.70
	1.5			5.69
	3			5.66
FCLBGA	N/A			5.24

Table 5: Thermal simulation results summary.

in²/W thermal impedance). The simulation results are shown in Table 5.

As seen from the above results, under the conditions assumed in this work, FCmBGA package thermal performance is slightly better than the bare-die package, but still not comparable to the FCLBGA package performance. The θ_{ja} of the FCmBGA package was ~9% higher

than that of FCLBGA. Also, thermally enhanced mold compounds did not have a significant impact on improving (lowering θ_{ja}) the FCmBGA package thermal performance. It is important to note that the simulation trends presented here are representative of the particular system thermal solution (TIM-II + aluminum sheet) chosen in this work. The choice of TIM-II and the ex-

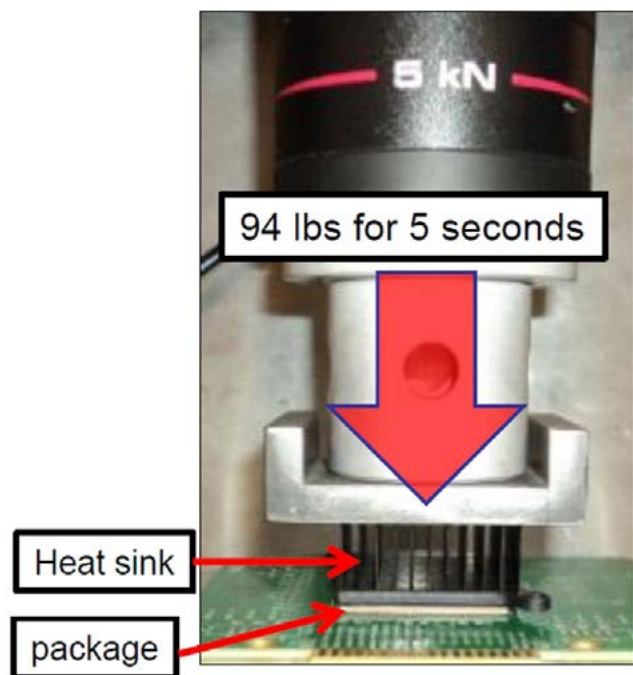
EVALUATION OF MOLDED FLIP-CHIP BGA PACKAGE FOR 28NM FPGA APPLICATIONS *continues*

Figure 9: Photo of the compression test setup.

ternal heatsink significantly impact the overall package/system thermal performance. Detailed thermal measurements comparing the thermal performance of FCmBGA with FCLBGA are presented in the paper by Galloway, et al⁴.

Compressive Loading Characterization

To verify package integrity, three FCmBGA units were surface mounted then tested in compression at 1480N (106 PSI) for a duration of 15

minutes at room temperature using an Instron mechanical tester. The test vehicles were 40mm packages with a 22 x 19mm die, surface mounted to a 2.3mm standard JEDEC style board. The acceptance criteria were the following: No damage to the die (either chip out or cracking), no damage to the mold compound (specifically cracking) and no BGA deformation leading to BGA shorting.

Compression Load Test Setup

To assure equal loading across the package, a thick steel fixture was placed between the cross-head and package topside. Double-sided thermal tape was applied between the package and steel fixture to further promote equal distribution of compressive stress, as shown in Figure 9.

No damage to the test vehicles were detected using the inspection methods listed in Table 6. Visual inspection was carried out either with a microscope or an ERSAscope for BGA inspection. The SAT inspection areas include: die surface, die active layers, the EMC adhesion to the passivation, the EMC adhesion to the package under the die, as well as the die surface.

Additionally, all BGAs of all samples were inspected X-ray imaging (Figure 10). No anomalies were detected between the BGA solder balls. No measureable differences were observed as a result of the compressive loading. For further confirmation, a unit was cross-sectioned to the bump and BGA plane (Figure 11). BGA solder balls were confirmed not to have been shorted together or significantly deformed.

Inspection Location	Inspection Method	Force	Dwell Time	Sample Size	Result
Die Surface	SAT and Visual	1500 N	15 minutes	3	Pass
Die Active Layers	SAT				
EMC to Passivation	SAT				
EMC to Package	SAT				
BGAs	X-RAY/Visual				

Table 6: Compression test summary and results.



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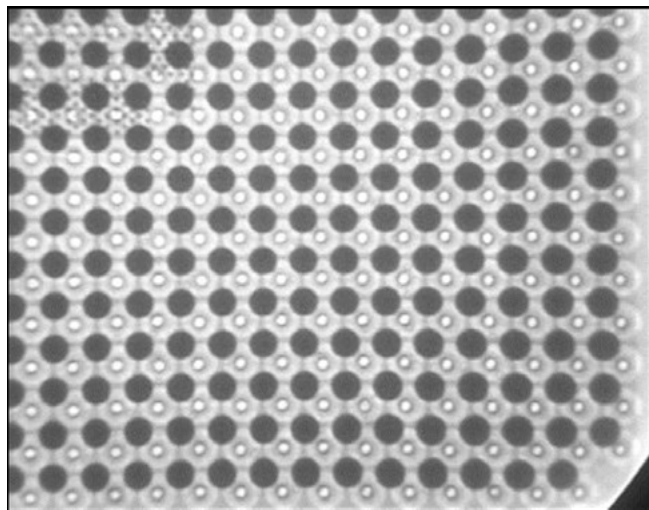
EVALUATION OF MOLDED FLIP-CHIP BGA PACKAGE FOR 28NM FPGA APPLICATIONS *continues*

Figure 10: X-ray of the BGAs after compressive loading shows no signs of shorting.

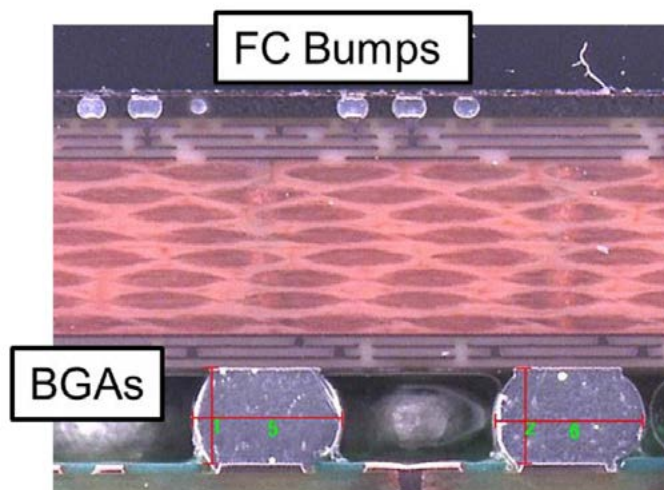


Figure 11. Cross-section of a sample confirms there is no shorting after compressive loading.

Even though the compression test results show that the package can withstand one time application of compressive force up to 1480N, it is recommended that the customers follow heatsink manufacturer's recommendations for application of compressive force for heatsink attach.

Component and Board-Level Reliability

The 28nm FCmBGA devices were subjected to component level and board level reliability test to ensure that package meets our package level and second level reliability requirements. We have defined the reliability test plan⁵ in conformance with the industry standards defined by JEDEC and IPC organizations. A 28nm FPGA device was used to perform the component-level reliability tests and a full stack daisy chain test vehicle was used for the board level reliability tests.

The FCmBGA packages were subjected to preconditioning at MSL3 level and a reflow cycle at 260°C to simulate the component assembly conditions. The devices were electrically tested at intermediate readout points to detect early failures. The parts subjected to board-level temperature cycle were continuously monitored to check resistance changes in the daisy chains during temperature cycling. Table 7 summarizes the results of the

component level and the board-level reliability tests.

The results of the component and board level reliability tests show that the 28nm FPGA in the FCmBGA package meets the industry standard reliability test requirements. To confirm that there were no latent defects in the package after the reliability tests, detailed construction analysis was performed to check the condition of the bumps, substrate and the die. The construction analysis showed no defects in the substrate, Silicon low dielectric layers and the bumps.

Conclusions

Our joint collaboration has resulted in the developing the valuable customer collateral for the FCmBGA package selected for 28nm FPGA device family. The customer usability of the FCmBGA package is shown to be equivalent to the lidded flip-chip BGA package while offering advantages of a low-profile package. The reliability tests show that the 28nm FPGA device in FCmBGA package meets the component and board level reliability requirements in compliance with IPC and JEDEC standards. The results of this collaborative study show that the FCmBGA package offers advantages of high-performance and low-cost, which are essential for the 28nm FPGA product family. **SMT**

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EVALUATION OF MOLDED FLIP-CHIP BGA PACKAGE FOR 28NM FPGA APPLICATIONS *continues*

Device	Package Size (mmxmm)	Die Size (mmxmm)	Pin count	Solder Ball	MSL	Reflow Temp C	Number of lots	Sample Size/lot	Reliability Test Results
Altera 28nm FPGA Device	35x35	18.8x14	1152	Pb-free	3	260			Temp Cycle Condition B -55/125 °C(Cycles)
									200 500 700 1000
							3	30	0/90 0/90 0/90 0/90
									Bake at 150 °C (Hrs)
									48 168 500 1000
							3	25	0/75 0/75 0/75 0/75
									Unbiased HAST 130 °C, 85% RH (Hrs)
									96
							3	30	0/90
									Lifetest 1.2xVcc, Tj = 125 °C (Hrs)
									200 500 1000
							3	24	0/72 0/72 0/72
									Temp Humidity Biased 85 °C/85% RH (Hrs)
									500 1000
							3	30	0/90 0/90
Altera 28nm FPGA Device	40x40	18.8x14	1517	Pb-free	3	260			Temp Cycle Condition B -55/125 °C(Cycles)
									200 500 700 1000
							3	30	0/90 0/90 0/90 0/90
									Unbiased HAST 130 °C, 85% RH (Hrs)
									96
							3	30	0/90
									Temp Humidity Biased 85 °C/85% RH (Hrs)
Daisy Chain TV	42.5x42.5	22x18	1681	Pb-free	N/A	260			Board Level Temp Cycle (0-100 °C)
									# of cycles completed # of Failures
							1	30	3500 0/30
							1	10	3500 0/10
Daisy Chain TV (w/HIS)									

Table 7: 28nm FPGA reliability test results.

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- J. Galloway, S. Kanuparthi and Q. Wan "Thermal Performance of FCmBGA: Exposed Molded Die Compared to Lidded Package," in proceedings of the 27th [Semiconductor Thermal Measurement and Management Symposium](#) IEEE, San Jose, March 20–24, pp. 181-186, 2011.

- Altera Reliability Report 53, Q2 2102, www.altera.com.

*Authors and Acknowledgements

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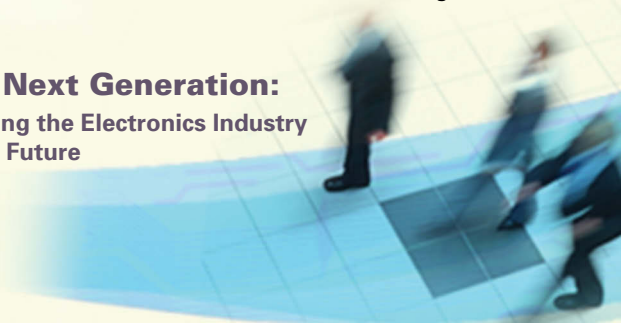
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SMTonline Supplier/New Product News Highlights



EPARO System from Manncorp Reclaims Valuable Solder

Many are unaware that 50–80% of wave solder dross is usable solder alloy. The SEPARO solder recovery system from Manncorp allows companies to quickly and easily reclaim valuable solder in-house for significant cost savings.

Indium Develops High-Performance Solder Alloy

Indium's new SACM is a high-reliability solder alloy that offers drop shock performance far superior to other SAC alloys, without compromising on thermal cycling—all at a cost below that of typical SAC solder alloys.

INVENTEC Releases Low Temperature Solder

ECOREL FREE LT 140-18 is a lead free no-clean solder paste combining the metallurgical properties and benefits of a low melting point alloy (SnAgBi) with high performance chemistry of the Ecorel range assuring that assembled electronics can reach their best reliability.

Adoption of Indium8.9HFA Accelerated

Indium Corporation's Indium8.9HFA solder paste is a versatile, halogen-free, lead-free, solder paste with leading print performance on miniaturized components. Assemblers and OEMs are adopting this new product at an accelerating pace.

Nordson YESTECH is SCS' AOI Supplier

Nordson YESTECH announced today that it has been selected by Specialized Coating Services, a contract provider of conformal coating services, encapsulating (potting), and ruggedization of PCBs, as their AOI supplier.

GOEPEL Enhances AOI of Fluorescing Conformal Coating

GOEPEL electronic offers an enhanced version of

its system for the automated optical inspection of fluorescing conformal coating. The Teachable Optical Measurement (TOM) system can be utilized for inspection of PCB coatings as well as PCB areas, which mustn't be coated. The maximum PCB size is 460 mm x 400 mm.

Dymax Launches Light-Curable Encapsulants

Dymax Dual-Cure 9101, 9102, and 9103 are resilient, chip-encapsulant materials designed with a UV/Visible light and secondary ambient moisture-cure system, making them ideal for encapsulation applications where shadowed areas are present.

Avnet to Acquire MSC Investoren GmbH

The agreement details a two-step approach whereby Avnet will acquire a majority interest in MSC Group after regulatory approval has been granted with the intent to acquire the remainder of the company within a short time frame.

GOEPEL electronic Expands GATE Program in Denmark

GOEPEL electronic, world-class vendor of JTAG/ Boundary Scan solutions compliant with IEEE Std. 1149.x announces the extended incorporation of CIM Industrial Systems A/S into the global alliance program GATE™ (GOEPEL Associated Technical Experts).

Multitest Provides Solutions for ICs and Mobile Devices

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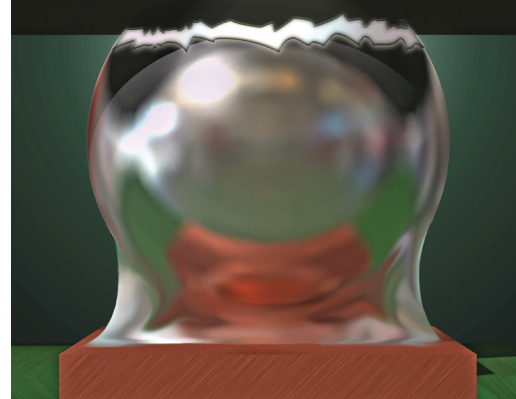
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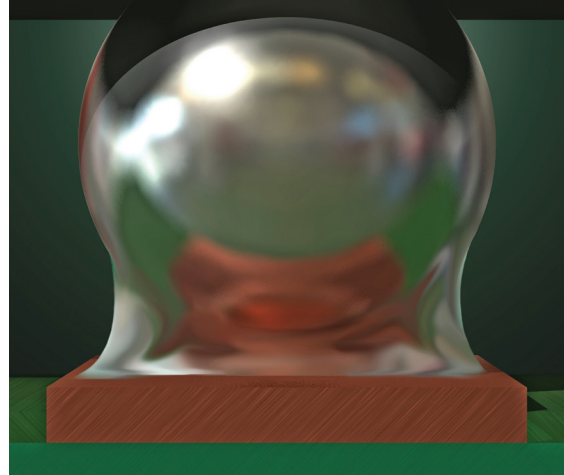
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Route 66

by Sjef van Gastel

ASSEMBLÉON NETHERLANDS B.V.



If you ever plan to motor west, travel my way, take the highway that is best. Get your kicks on route sixty-six.

I'm listening to the Rolling Stones sing those words as I drive toward Southern Europe for my summer vacation. It's a bit like the roadmap for automotive electronics, you may say, and I wouldn't argue with you.

Important Automotive Electronics Trends

The 2013 version of the iNEMI roadmap predicts an average market growth of 7.9% in value for the automotive electronics market for 2011–2017.

Hybrid and electric cars make up a major growth area which hardly existed before the turn of this century, but now account for about 8% of worldwide sales. By 2021, alternative fuel drive train systems are even expected to reach 28%! However, many things need to change

before electric cars become really popular. The most important areas needing improvement relate to increasing the driving distance, reducing charging time, increasing battery life and reducing total costs of car ownership. Additionally, there are also still far too few charging stations.

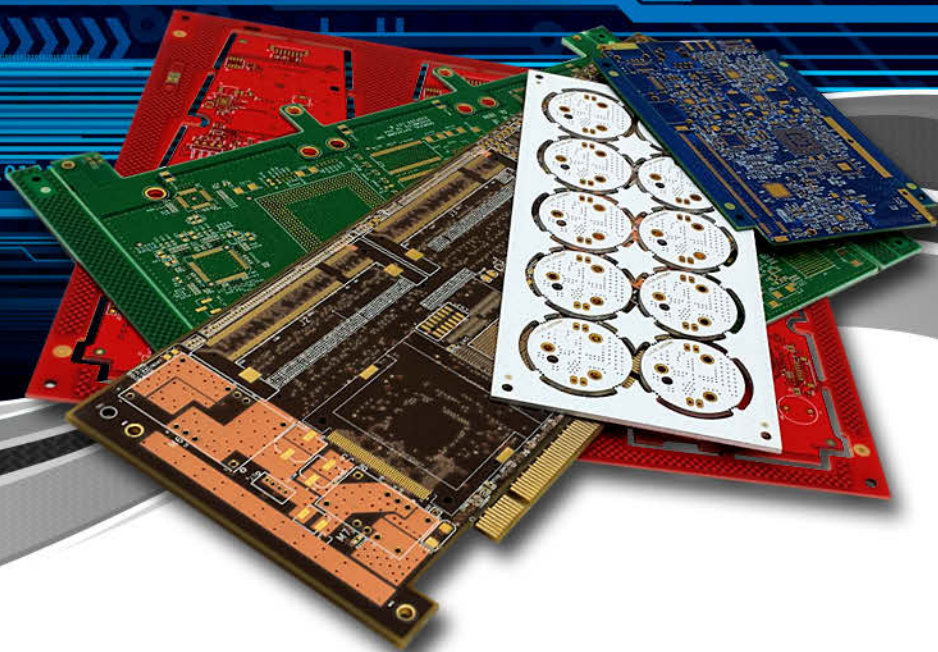
Automotive electronics will doubtless play a major role in closing these gaps. The major growth in electric cars is expected in urban areas where both space and clean air are at a premium. Half the world's population now lives in megacities, with very dense traffic and many pedestrians, so increasing car safety is also critical.

Part of the solution will come from integrating connectivity and active safety devices. That includes vehicle-to-infrastructure communication (e.g., weather condition-related drive parameter settings), vehicle-to-vehicle communication (e.g., collision avoidance and road train convoys) and ultimately, driverless cars for automatic interactive driving.



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ROUTE 66 *continues***Categories of Automotive Electronics**

The automotive electronics industry is generally divided into the following six categories:

- Powertrain electronics (systems controlling the engine or driveline)
- Entertainment electronics (in-car media)
- Safety and convenience (safety and comfort) systems
- Vehicle and body controls (steering and controlling car stability)
- In-cabin information systems (instrument clusters and telematics)
- Embedded and non-embedded sensors

Powertrain Electronics

One of the major growth areas is the drive train, where developments are largely driven by energy savings. During a car journey, acceleration is followed by braking. The car's kinetic energy is then dissipated through the car brakes, which heat up, wearing down the disks. Considerable energy savings (up to 30%) can be achieved by storing this energy in a flywheel or electric accumulator.

Key to this energy storage will be converter systems that use large capacitors. Until recently, powertrain electronic modules were sepa-

rated from the engine and drive systems. Now, though, the engine control units (ECUs) are attached to the engine, and in the near future they will be integrated into a total drive system.

The temperature and reliability requirements for ECUs will therefore increase, needing better than 10 ppm at the module level! Operating temperature requirements for under-the-hood electronic modules range from -40°C to +140°C (up from the previous +125°C). This extended temperature range can only be met by using high-temperature-resistant components, high- T_g substrates, efficient cooling (such as copper inlays in substrates, heat pipes or potting using heat conductive material), and tracks with large copper area and solid connectors.

These solid power connectors are usually connected using through-hole reflow (THR) soldering (also called pin-in-paste). The advantage of THR is that both SMD and THR components can use the same reflow solder process and that both component types can be placed by a normal SMD pick-and-place machine.

Solder paste is printed by a stencil printer, also covering the topsides of the mounting holes for the THR components. During THR component placement, the component leads smear the solder paste to both sides of the substrate. Finally, all components (both THR and SMD) are reflowed in the reflow oven. The pick-and-place machine does have special requirements, though, since the required placement forces can be up to 160 N for a 160-pin THR connector.

Entertainment

Developments in entertainment electronics include full integration of connectivity (internet in cars) as well as active safety. This will lead to interactive navigation systems that take traffic density, roadblocks and local weather conditions into account.

Safety and Convenience

A major part of safety and convenience systems will include active collision protection. Distance (park-

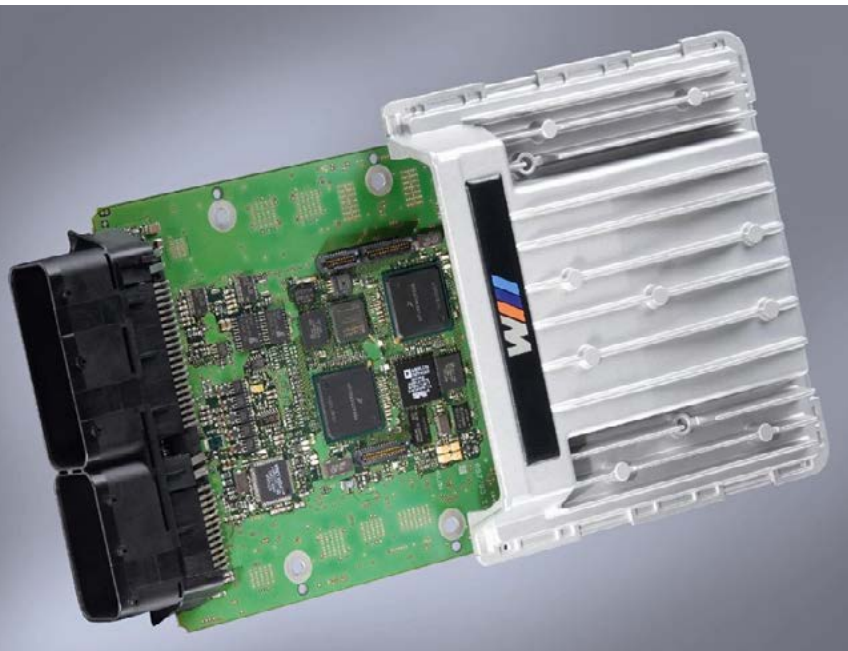


Figure 1: Engine control unit (ECU).

ing) sensors and distance observation radar are already being incorporated. These will be extended with vehicle-to-infrastructure based systems (e.g., road pricing and reduced speeds around schools), followed by vehicle-to-vehicle communication.

Vehicle and Body Controls

Most vehicle and body control developments will similarly relate to active safety and comfort improvements. One example is the active car suspension: The conventional wheel suspension system (based on helical springs and oil-filled shock absorbers) will be replaced by a mechatronic suspension system (based on actively controlled electromagnetic actuators). That will improve driving characteristics as well as passenger comfort.

Traditional wiring harnesses will be replaced by multiplexed cable systems and ultimately, power line communication systems (where both electrical power and signal transfer will use the same single cable interconnection). Hydraulic driver assistance systems for steering and braking will increasingly be replaced by electric (mechatronic) assistance. Here, the main advantage is compact design and, once again, power saving.

In-Cabin Information

Voice commands and head-up displays will become increasingly important in cabin information systems, along with LED lighting. Many cars today have energy-saving daylight illumination using LED strips. Three-dimensional MID (molded interconnection device) substrates will increasingly be used for dashboard instrument clusters. MIDs which integrate both LED luminaires (where shape and space envelope is important for car body styling) and interconnections are growing in importance. Placing and connecting electronic components on 3D surfaces will create new challenges for pick-and-place machines.

Sensors

Finally the number of sensors (both embedded and non-embedded) is growing con-

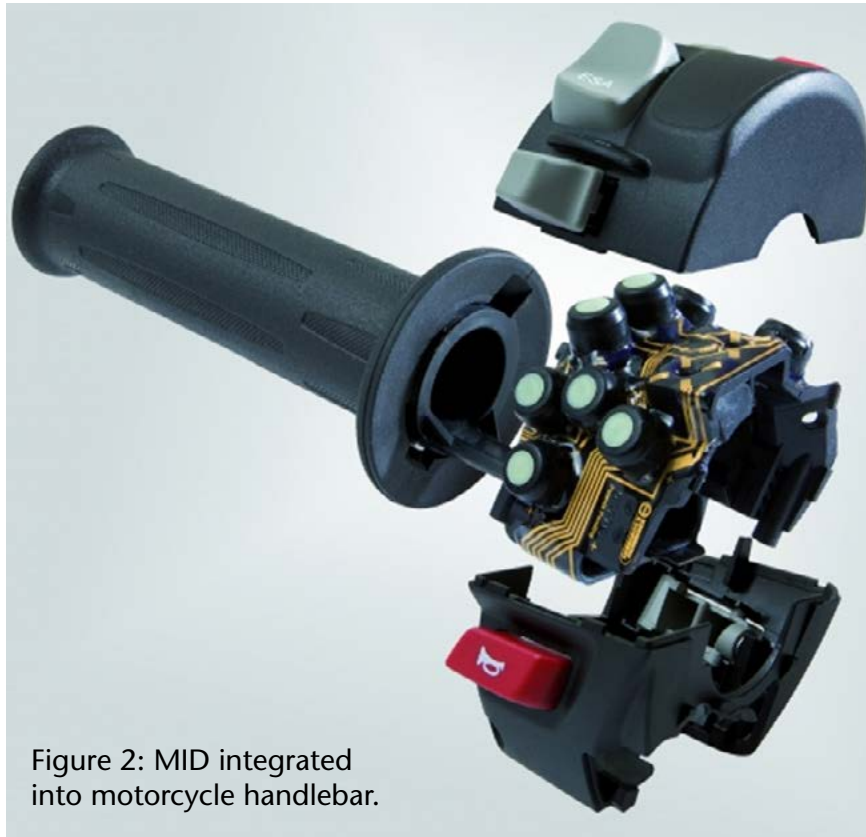


Figure 2: MID integrated into motorcycle handlebar.

siderably. These will be integrated with powertrain, body control and safety systems. Solid state (MEMS technology) sensors should meet automotive robustness and reliability requirements.

These trends will boost the electronics manufacturing industry and will contribute to a more sustainable world, but they, too, will also bring new challenges for pick-and-place machine manufacturers.

We get our kicks from solving them. **SMT**



Sjef van Gastel is manager for advanced development at Asmbleon Netherlands B.V., where he combines his experience as systems architect and machine designer to explore technical and business opportunities from emerging technologies. To read past columns, or to contact van Gastel, [click here](#).

The Ins and Outs of Step Stencils

by Rachel Short

PHOTOSTENCIL

The demand for step stencils is increasing, but why? The answer: shrinking components. In the early days of SMT assembly, step stencils were used to reduce the stencil thickness for 25 mil pitch leaded device apertures. However, as SMT requirements became more complex and, consequently, more demanding, so did the requirements for complex step stencils. Today, fine-pitch components, which necessitate a thin stencil for acceptable paste release, are sandwiched beside a variety of devices and components that require higher paste height. Getting the solder paste volume needed for larger components, while still having an area ratio that allows for good paste release on small com-

ponents, can be challenging. Step stencils offer the SMT process engineer significant flexibility in achieving the proper solder paste height and volume for the overall paste printing process.

Step stencils range from simple designs to complex multi-thickness steps. With them you can print different paste heights, with one stencil, in one print. Without them, a separate print run and stencil might be needed for each solder paste height or a manual application for additional paste deposit required. Using a step stencil is much faster, prints an actual solder brick, and allows for solder paste volume control. Dispensing and other printing methods are slower, many times more manual, yield less control on

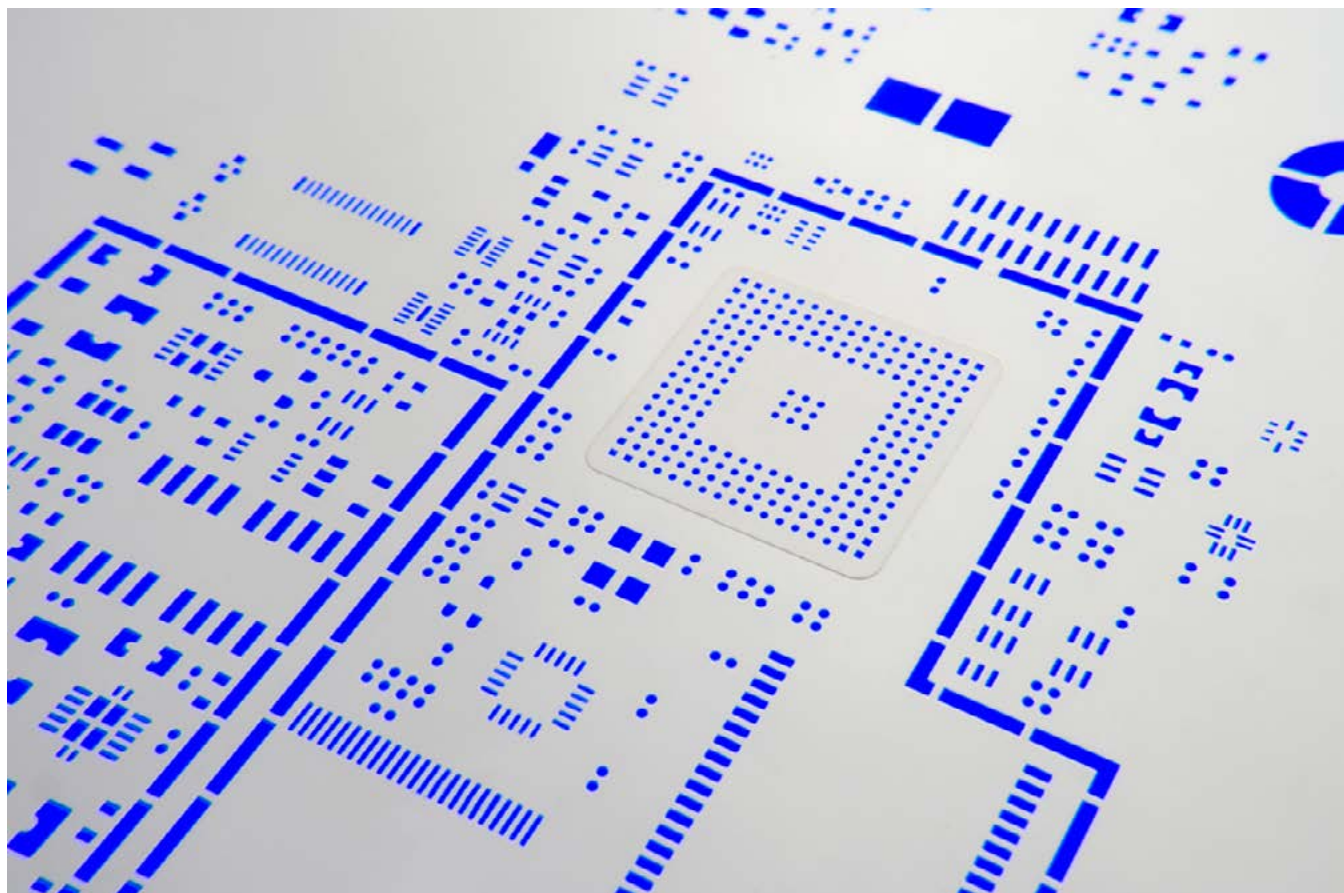


Figure 1: Complex step stencil with apertures inside of step area.

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THE INS AND OUTS OF STEP STENCILS *continues*

solder paste volume, and usually require a second step, after initial printing.

Step stencils are available in all stencil technologies: electroformed, laser cut, and chemical etched. These steps are usually etched or electroformed depending on the application and the area ratio. Although traditionally etching was used for most stencil manufacturing and aperture formation, etching is now predominantly used for step stencils. The thickness of the step areas and the overall thickness of the stencil are determined by the area ratio of the component. Step stencils have a primary base thickness and step-up or step-down areas across the board pattern depending on the thickness and volume of solder paste a particular component requires.

Component size doesn't necessarily affect the stencil design. The design depends on the paste volume requirement on the board, which is usually accompanied by area ratio struggles. The range of component sizes that can be accommodated on the same board is determined by a combination of area ratios and the necessary keep-out areas in the design. Because of the varied thicknesses around the step, there are defined keep-out areas. If the application isn't conducive to these keep-out areas, there are other options, like two-print printing and reservoir printing.

An additional consideration is the co-planarity of the component and the solder paste height delivered by the stencil. In this case, height can only be achieved by using a thicker stencil. Co-planarity problems can result in an open contact. Printing higher solder bricks (7–8 mils) on the BGA pads prevents this. SMT components, like 0.5 mm pitch QFPs, 0402 chip components, and R-Packs, won't tolerate an 8 mil thick stencil as aperture sizes are too small for good paste release. A stepped electroform

stencil gives good release when 0201 chip components and 0.5 mm pitch μ BGAs are present.

Step stencil technology offers unique solutions for various printing applications such as CBGA and through-hole paste volume/height requirements. Step-up electroform stencils address the solder volume/height while also providing excellent paste transfer for 0.5mm μ BGAs and 0201 devices. Two-print stencils, including a thick second print stencil with deep relief-step pockets, handle both glue attach printing and intrusive reflow printing. Normal

SMT stencils that are 5–6 mils thick with relief-step pockets on the contact side of the stencil can be used when there are raised areas on the PCB that would prevent a normal stencil from gasketing to the board. 3D electroform stencils are a good choice for two-print stencil operations when printing flux/paste for flip chip and paste for SMT in a mixed technology application flip chip/SMT. 3D electroform stencils with formed relief pockets are preferable for printing on boards when high protrusions exist on the board surface.

Steps can be placed on the PCB side, the squeegee side, or on both sides of the stencil. Relief-step board side

stencils eliminate the gap between the stencil apertures and the pads, allowing the stencil to cleanly gasket to the PCB. Mixed-technology applications of solder paste printing for through-hole/SMT as well as solder paste/flux printing for flip-chip/SMT require special step stencil designs. Thick metal stencils that have both relief etch pockets and reservoir step pockets are very useful for glue and paste reservoir printing. Electroform and laser-cut step-up stencils for ceramic BGAs and RF shields achieve additional solder paste height on the pads of these components. Special solutions are available for odd PCBs that have some raised areas on the board

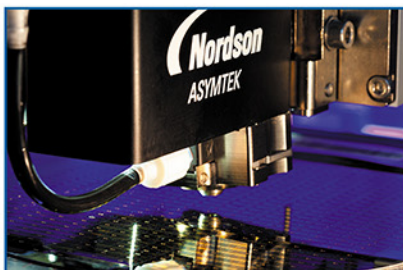
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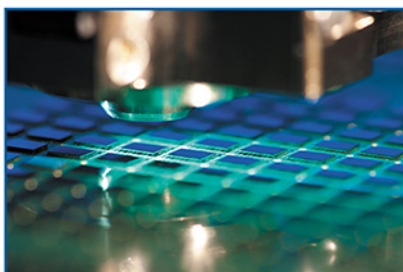
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Sealing Dispensing for MEMS Wafer Capping

Wafer capping MEMS devices presents challenges and specific requirements for dispensing sealant, volumetric accuracy, and motion systems that can be met with the correct dispensing equipment and methods.

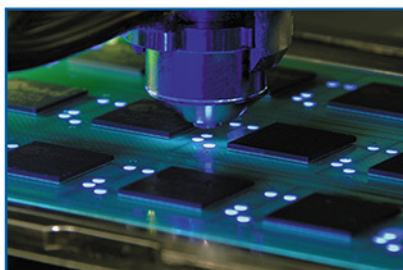
By Heakyong Park



Underfilling Using Continuous Path Motion Control

New device configurations change the amount of fluid needed for underfill and the dispensing techniques for depositing it. Using a continuous motion of the dispense head avoids backtracking and improves units per hour by 27%.

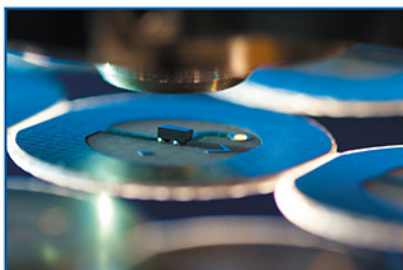
By Akira Morita



Conformal Coating Process Characterization Considerations

Selective coating coats specific areas. Using properly characterized automated equipment is a reliable way to increase yield, throughput, and reduce the cost of the conformal coating process.

By Brad Perkins



Process Improvements in Fluid Dispensing

Speed and throughput have increased exponentially over the years, yet are still factors challenging the existing dispensing systems as fast never seems to be fast enough. Increasing throughput involves more than just speeding up the actual act of dispensing.

By Dan Ashley

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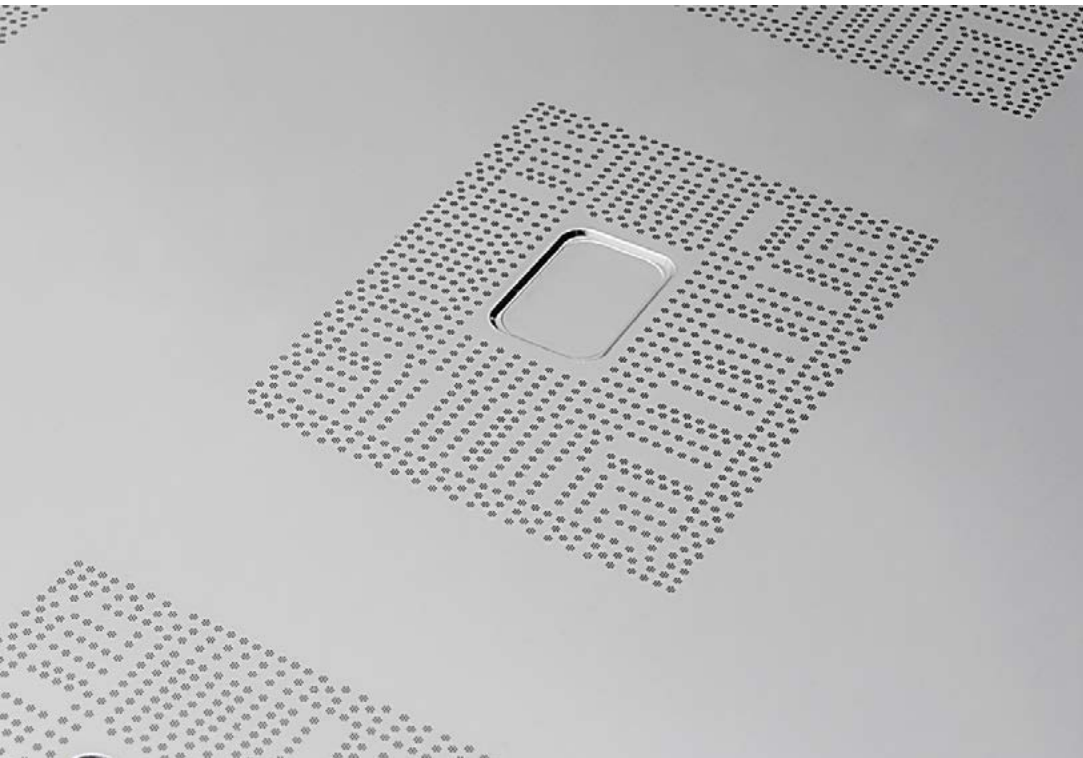
THE INS AND OUTS OF STEP STENCILS *continues*

Figure 2: Step stencil with relief pocket.

(up to .120" high). Examples and specifications can be seen here:

Step-Down Stencils

- 20 mil pitch QFN: 7 mil thick for R-Packs and C-Packs with a step-down to 5 mil for 20 mil pitch QFNs
- 16 mil pitch QFN, 0201s and/or μ BGAs: 5 mil thick stencil with a step-down to 4 mil for the 16 mil pitch QFN, 0201s, and or μ BGAs

Step-Up Stencils

- CBGA or CGBGA: 6 mil for normal components and a step-up to 8 mil for CBGAs; extra paste height is required for this component due to possible co-planarity issues
- Through-hole Connector: 6 mil for normal components and step-up to 10 mil for the through-hole connector

Relief-Step Board Side

- Bar Code Relief: When the bar code is too close to the PCB pads it can cause a gap between the stencil apertures and the pads. The relief

pocket allows the stencil to cleanly gasket to the PCB

- **Raised Via Pads:** Raised via pads can prevent the stencil from gasketing to the PCB surface. A relief-step pocket around the vias prevents this situation

- **Relief for Paste (two-print stencil):** The two-print stencil is used to print solder paste on a board which already has solder bricks on the PCB surface from a previous print cycle. An example would be a 12 mil thick glue stencil with an 8 mil deep relief-step pocket around SMT solder paste bricks

So what should you look for when choosing a step stencil? Area ratios determine the thickness of the stencil and step areas. Designs with large paste volume components with fine pitch components are usually the most likely step stencil candidates. Many BGA manufacturers recommend step stencils when using their components because the solder ball doesn't melt during reflow; therefore, the contact has to be made on the print. In any case, using a step stencil positively affects the area ratio. It achieves the necessary paste volume on a large component while still getting a successful print on a smaller component, and printing with one process increases throughput and saves time and money. **SMT**



Rachel Short is vice president of sales and marketing at PhotoStencil LLC. She may be reached via [e-mail](#), or by phone at 719-304-4224.



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News Highlights



Ducommun to Produce Assemblies for Black Hawk

The company has received a multi-year contract from Sikorsky Aircraft Corporation, a unit of United Technologies Corporation, to continue to produce electromechanical assemblies for various models of the UH-60 BLACK HAWK helicopter. Ducommun LaBarge Technologies will produce the electromechanical assemblies at its Huntsville, Arkansas, facility through 2017.

Mercury Nets \$3.6M Microwave Assemblies Contract

Mercury Systems, Inc. has received a \$3.6 million follow-on order from a leading defense prime contractor for integrated microwave assemblies for an airborne electronic warfare application.

Sparton, USSI ERAPSCO JV Lands Sonobuoys Contract

Sparton Corporation and Ultra Electronics USSI, a subsidiary of Ultra Electronics Holdings plc, announce the award of subcontracts valued at \$5.8 million to their ERAPSCO joint venture, for the manufacture of sonobuoys for the United States Navy.

Ducommun Named John Deere's Partner-level Supplier

Ducommun Incorporated has announced that its Ducommun LaBarge Technologies business group has been named a Partner-level supplier for 2012 in the John Deere Achieving Excellence Program.

OSI Systems Gets \$21M for Electronic Subassemblies

OSI Systems, Inc. has announced that OSI Electronics, a business within its Optoelectronic and Manufacturing division, has received orders for approximately \$21 million for electronic subassemblies from an advanced skin care solutions provider.

API Gets \$6M for Microwave Sub-assemblies

API Technologies Corporation has won a \$6 million follow-on order to provide microwave sub-assemblies for a major European weapons program.

Murrietta Receives Raytheon's Highest Supplier Award

Raytheon recognizes its Five Star Suppliers based on three important factors: 100% on-time delivery, 100% sustained quality, and continuous process improvements. Raytheon has over 5,000 global suppliers and Murrietta Circuits was one of only 14 to be recognized for this tremendous achievement.

Celestica Receives Achievement Award from DoD

Celestica Inc., a global leader in the delivery of end-to-end product life cycle solutions, is a recipient of the 2013 James S. Cogswell Outstanding Industrial Security Achievement Award from the Defense Security Service (DSS), an agency of the U.S. Department of Defense.

OSI Systems Nets \$11M Order from U.S. Government Agency

OSI Systems Inc. has announced that its Security division, Rapiscan Systems, has received an order for approximately \$11 million from a U.S. government agency for maintenance and related services to support Rapiscan systems that inspect cargo, vehicles, baggage, and parcels.

3CEMS Inks Maritime Agreement

"3CEMS has expanded constantly on the manufacturing areas and capacity. This new agreement is an important step for 3CEMS to meet customers' increasing demands and various product segments. We look forward to this partnership," said Leo Chien, vice chairmen of 3CEMS.

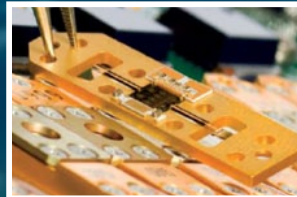
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Dropping the BOM

by Michael Ford

MENTOR GRAPHICS CORP.

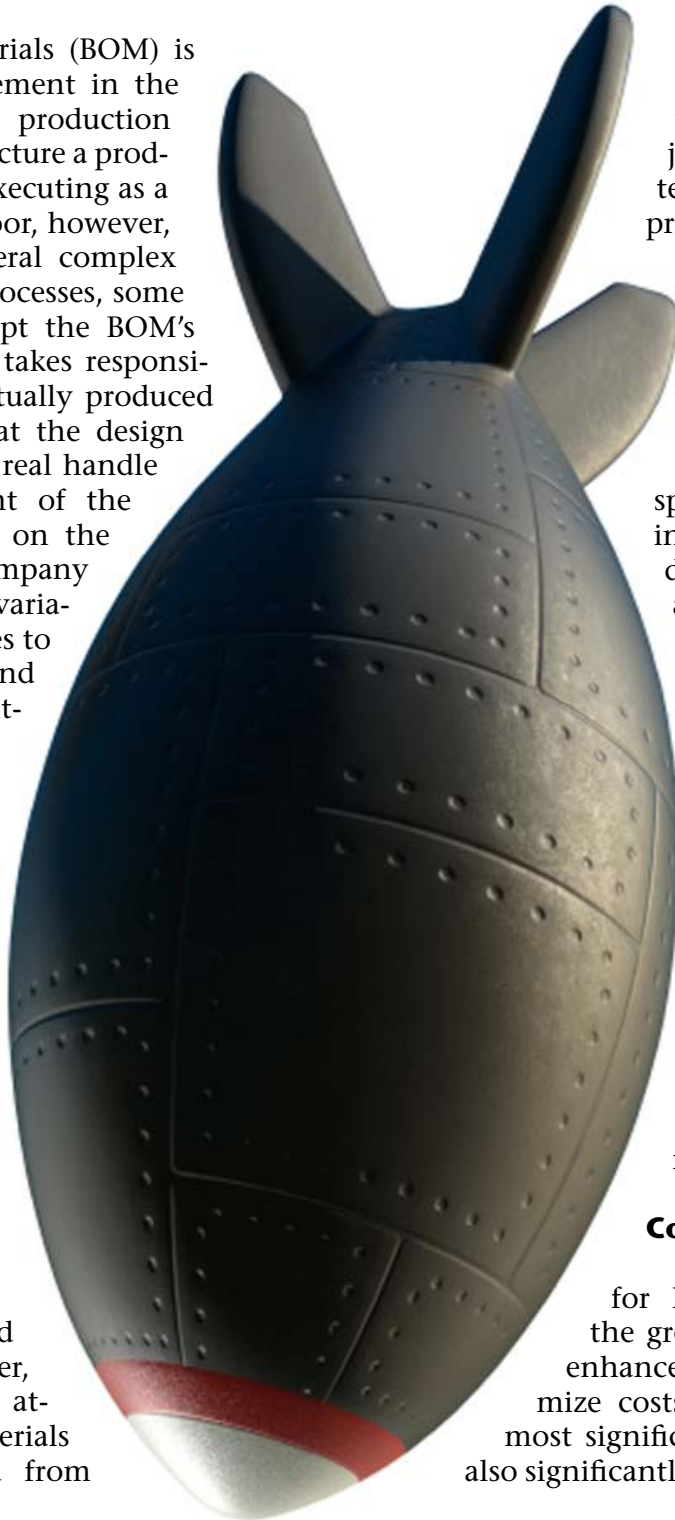
The bill of materials (BOM) is the most critical element in the definition of what production should do to manufacture a product. What ends up executing as a BOM on the shop floor, however, is the result of several complex and often manual processes, some of which will corrupt the BOM's data integrity. Who takes responsibility for what is actually produced as compared to what the design intended? Getting a real handle on the management of the BOM must be high on the agenda for any company as product mix and variation grows, lead times to market decrease, and the need for accountability increases.

The BOM starts life at the design stage. As products are conceived, often formed around combinations of key technologies and chipsets, the key materials are identified. These key materials are at the core of the design. For the electrical designer, the specifications are known in terms of functionality, and for the layout designer, in terms of physical attributes. These materials are usually sourced from

only one or two suppliers, and are not interchangeable with other devices. The majority of the remaining materials that will make up the product are so-called "common" materials: things like resistors, capacitors, diodes, etc., which have standardized specifications, are available from several different suppliers and in several different specifications of size and rating. Generally, the electrical designer decides the values and ratings of all materials, the design capturing these as well as the descriptions of the key materials. The layout engineer takes this information and has to make decisions about which actual materials to use, at least in terms of size and shape. Each individual component is uniquely named with a reference designator, a shape, a specified value and rating, and often, an assigned nominal part number.

Consider Alternatives

This is the crucial first step for BOM management, where the greatest opportunity exists to enhance product quality and minimize costs. Materials are by far the most significant cost of a product, and also significantly influence how the product



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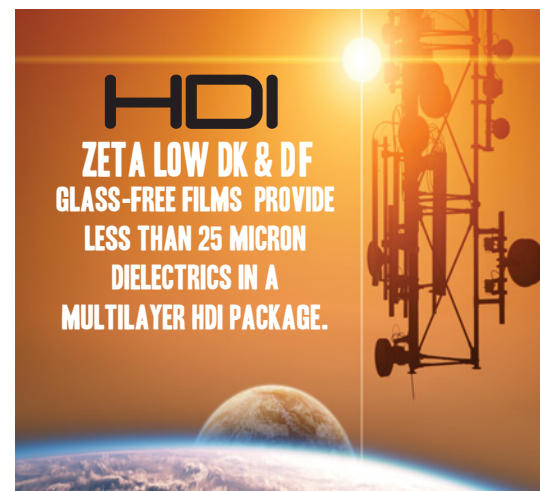
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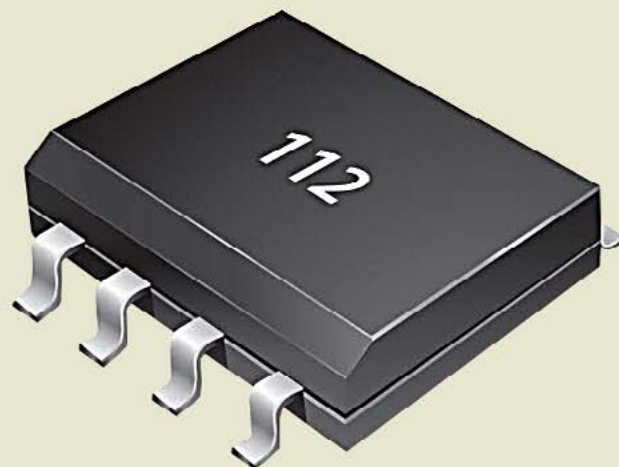
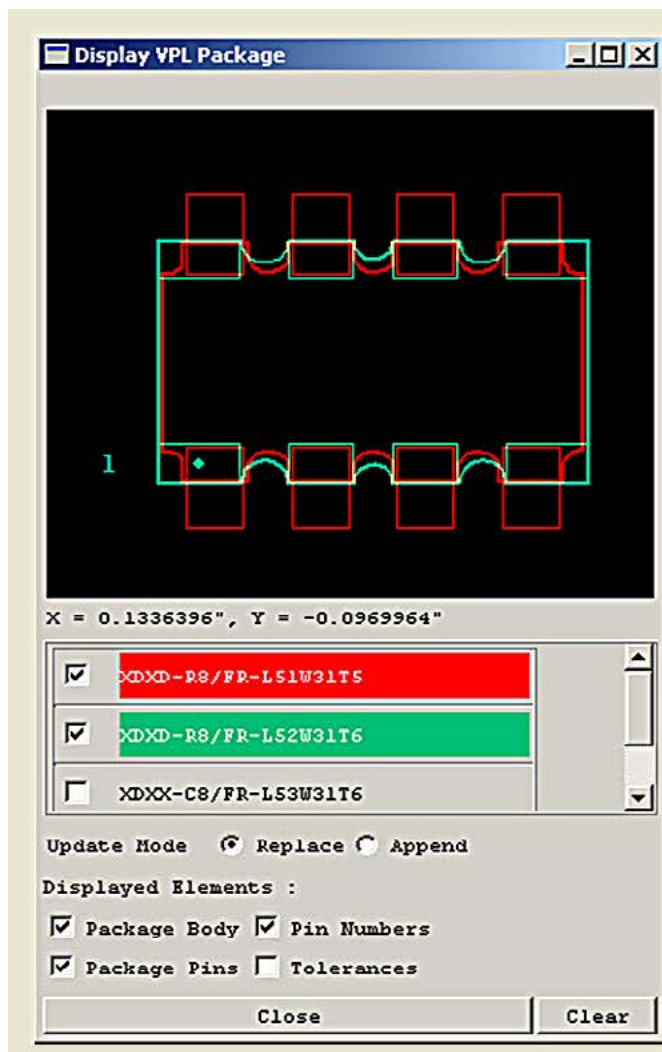
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DROPPING THE BOM *continues*

will perform, a balance that starts with the selection of materials by the layout engineer. The least effective layout engineer will simply follow the policy attributed to the product, which dictates basic technology and practices, as well as the product's mechanical, physical and size requirements, plus, the basic material specification requirements. The most effective layout engineers will also consider the wide range of material choices, looking at availability and cost of materials, durability, mechanical issues, chemical content, heat and vibration analysis, capabilities of the expected production processes, and the effect of the layout on quality and testability. The more specific the designer's information,

the better prepared the design will be for real-world production. Automated DFM tools, which analyze the PCB layout according to rules based on specific PCB fabrication and production requirements, can create a significant advantage at this point (Figure 1).

Once an initial design is completed, prototypes of the product are fabricated. These focus primarily on the performance of the product, and also reveal any issues in the layout and materials initially selected. By this time, the electrical designer may also have created several variations of the product, each with different levels of features or functionality, such that a single PCB design can serve as an engine in many dif-



Graphical analysis of package dimensions for Approved Vendors of the same part

Figure 1: More than one component from the approved vendor list (AVL) may satisfy the BOM requirements. Here a graphical analysis shows the two parts do indeed meet manufacturing requirements.



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On-Shoring in the Electronics Industry: Trends and Outlook for North America — 2013 Update

\$300 (standard), \$225 (IPC member) — coming in August

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IPC's Best-Selling Study

Study of Quality Benchmarks for the EMS Industry — 2013

This annual study, published in May 2013, reports current EMS assembly attributes from companies worldwide, including:

- First-pass and final-inspection yields by various types of tests and inspection methods
- Internal yields of key processes
- Defect rates (DPMO)
- Cost of poor quality
- Customer returns
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- Supplier performance
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The findings are segmented by company size tier, enabling EMS companies to compare their performance to other companies their size. Averages are reported for all metrics, as well as median values and 25th and 75th percentile data.

This practical reference guide is IPC's best-selling study. It is available in IPC's online store at www.ipc.org/EMS-benchmark-2013. Single-user prices are \$1,350 (standard) and \$675 (IPC member). Site and global licenses are also available.

More Information

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DROPPING THE BOM *continues*

ferent product variants in the market. The layout engineer must accommodate different materials for the same locations depending on the variant.

Once the prototypes are working to specification, the design team is under pressure to complete the design and hand it over to the product manager. Different companies may have different roles and mechanisms to manage the product lifecycle, but essentially the product manager has the responsibility to get the product to market on time and within the cost target.

Before the design is finalized, however, the BOM needs to be introduced into the MRP system. The least effective operations will simply map the BOM to regular material part numbers and associated suppliers, plus create new part numbers and sourcing for any new materials not previously used. The material information from the design is based on individual components with their unique reference designators. The nature of most MRP systems, however, is that they are part number based. The mapping operation, therefore, in MRP creates a list of part numbers—normally internal part numbers specific to the company—which then link to part numbers of vendors from which the materials will be sourced.

The specific, unique reference designators of components are retained, but often only as comments. To keep the comments short, originally to fit in the reference comment field of the MRP database, they are summarized; for example, “R201-206, 219, 221-232” would be used instead of specifically listing each designator, representing a significant opportunity for error. The more effective purchasing team, together with the product manager, will look for opportunities to reduce the variations in materials, that is, to reduce the count of part numbers used, and to select alternative, lower cost materials where possible, but that may also

have a different specification or physical form. Changes need to be done and be consistent over all product variants.

The effect of this can be a significant contribution to the profitability potential of the product, but can be exceptionally difficult to manage from within the MRP engine, where the designators have been corrupted into the shorthand form. Checking back to the design to assure that alternative materials will satisfy

the design from the design standards and policy perspective, that functional performance will not be affected, and that the layout and manufacturability will also not be affected is also very important. Iterations between MRP and design are limited by the time taken in the MRP purchasing process, versus the need for the designers to close the design and get on to the next, and for the product manager to get his product out into the market on time. Product lifecycle management tools are designed to bridge this gap to some extent, making the selection of materials and understand-

ing the consequences over all the product variants clear. These tools of course must work with the DFM tools and the design system itself in order to make the necessary fast and accurate decisions.

In higher value and safety-critical applications, all materials changes must be approved, often requiring life testing of revised prototypes, which can take many weeks to complete. At the other end of the scale, however, for example, the low-end consumer market, BOM changes often continue to be made long after the design has been closed, which may even include changes made at the point of assembly in order to further optimise materials cost and for ease of materials sourcing.

Once these steps have been completed, the product's manufacturer is selected. The least effective production operations will go ahead and order the materials based on the MRP model as

“

Different companies may have different roles and mechanisms to manage the product lifecycle, but essentially the product manager has the responsibility to get the product to market on time and within the cost target.

”

DROPPING THE BOM *continues*

it is transferred into their ERP system. The more effective operations, however, will additionally consider the production engineering requirements. Though the design is completed and cannot be changed, DFM tools designed specifically for assembly use will expose any challenges based on the performance and capability of the specific production processes in place, and the specific materials that the purchasing team has chosen. These tools, as well as those used to prepare the engineering data across the production processes, need to use the original PCB design data and the somewhat revised data.

Dropping the BOM

The BOM arrives courtesy of the local ERP system, with all of the shortened and corrupted component reference designators. This is where the BOM drops. Aligning these two pieces of information can be a difficult task, frequently exposing errors that have been made in the preceding processes. Engineering tools must be able to combine the data and immediately expose errors; this is essential if corrections are to be

made before the physical materials are ordered. Delays here potentially result in material waste and delayed production. The engineering teams will also consider the production of the product, with all its variants, in the same production environment as other products. Optimizations of production, especially in SMT, are very much related to material variations, material supply forms versus machine capability, and commonality between products to promote quicker set-up changes between work orders. This also can effect BOM changes.

Full Circle

Once these last adjustments have been made such that the actual production operation can be run as effectively as possible, there is still a question of whether the original design principles are being followed, and whether the performance, quality and life expectancy of the product will be as originally intended.

The most effective design teams are involved in determining the final material content, so that they can give their approval and in

Item	CPN	IPN	RefDes	Quantity	RefDes Count	Description	Manufacturer	MCode	MPN	EVPL
2	01K2334	C222		1	1	C820UF 4...	SANYO	SANYO	4SP820M	
3	03G9312	U48		1	1	HC11 50...	TI	TI	SN74H...	
4	03L0764	Q3,Q...		4	4	SCHOTTK...	MOTOROLA	MOTOROLA	MBRD3...	
5	04N9256	R320		1	1	R33R 1 6...	PANASONIC	PANASO...	ERJ3E...	
6	05K2414	U77		1	1	AHC1G08...	TI	TI	SN74A...	
7	08G4893	R344,...		2	2	R100R 5 ...	PANASONIC	PANASO...	ERJ3G...	
8	08G4897	R308		1	1	R160R 5 ...	PANASONIC	PANASO...	ERJ3G...	
9	08G4935	R314		1	1	R15K 5 6...	PANASONIC	PANASO...	ERJ3G...	
10	08G4967	R183,...		4	4	R430K 5 ...	PANASONIC	PANASO...	ERJ3G...	
11	09G9262	R264		1	1	R562R 1 ...	PANASONIC	PANASO...	ERJ3E...	
12	09G9296	R268,...		4	4	R1K27 1 ...	PANASONIC	PANASO...	ERJ3E...	
13	09G9310	R306		1	1	R1K78 1 ...	PANASONIC	PANASO...	ERJ3E...	
14	09G9375	R326		1	1	R8K45 1 ...	PANASONIC	PANASO...	ERJ3E...	
15	09G9378	R318		1	1	R9K09 1 ...	PANASONIC	PANASO...	ERJ3E...	
16	09G9382	R273,...		3	3	R10K 1 6...	PANASONIC	PANASO...	ERJ3E...	
17	09G9383	R300,...		4	4	R10K2 1 ...	PANASONIC	PANASO...	ERJ3E...	
18	09G9440	R304		1	1	R40K2 1 ...	PANASONIC	PANASO...	ERJ3E...	
19	09G9461	R278,...		4	4	R66K5 1 ...	PANASONIC	PANASO...	ERJ3E...	
20	09G9507	R282,...		4	4	R200K 1 ...	PANASONIC	PANASO...	ERJ3E...	
21	09G9510	R166...		4	4	R215K 1 ...	PANASONIC	PANASO...	ERJ3E...	

Figure 2: Manufacturing automation software can ensure that any modifications to the BOM are correctly identified. The complete BOM is available to all authorized users.

DROPPING THE BOM *continues*

the future, design in the needs of the production operation. The product manager communicates issues up and down the product creation stream. The challenge remains, however, to integrate the tools serving at each point in the process. The designers must know how to layout the product in the best way for production without delaying the design, and without specific manufacturing and assembly engineering knowledge. The manufacturing and assembly engineering technologists need to know that any changes they make in materials will not invalidate the design or product performance.

Once in production, material changes will continue. Local purchasing will continuously apply their purchasing policy, which usually is based on dual-sourcing to prevent supply issues. If and when supply issues arise, there can be a sudden switch to a third vendor or an alternative part. There will be variations in these materials, physically as well as electrically, which can be significant enough to cause part numbers in the BOM to change, especially when different component ratings and supply forms are involved, which production engineering and the product management should approve. There may also be design revisions for any number of reasons.

Who Owns the BOM?

The BOM is the entity that links all of these processes together, for all the product variants and all the revisions, but who is the owner of the BOM? The BOM itself has a complexity that no one person seems to be able to manage or even take responsibility for. It often ends up that there are multiple simultaneous "flavors" of BOM for a product—for example the design BOM versus the production BOM—which can easily lead to quality and supply issues. The design team should have the final say in the specification for the product; any changes made should be approved by design, so there is a strong argument that the design team has

ownership. The product manager also has a case, since his role carries the responsibility for the whole process of getting the product to market. The day-to-day BOM changes, however, are implemented on the MRP or ERP side, triggered mainly by purchasing, who have the responsibility for procurement of the materials, so perhaps they are the ones to own the BOM. But the rubber meets the road in production, so perhaps the production engineering teams are the actual ultimate BOM owners? All of these views are valid, and in different companies we will see variations with how the BOM is managed. This is made more difficult for those companies who have products produced in different sites across the world and especially those who use contract manufacturing.

The real answer to BOM management must be a systemized unification of tools starting from design, encompassing MRP and ERP, for purchasing, and process preparation for manufacturing and assembly. From the quality and compliance point of view, tracking and recording of decisions taken, plus the traceability of actual materials used, is essential. Controlling the entire BOM enables decisions to be made earlier in the overall process, with fewer mistakes and rework. It also allows data to be gathered to measure the performance of different materials.

It leaves me wondering just how evolved this process is among all the different types and tiers of electronics production operations out there. Please tell me your experiences, good and bad, your ideas for how this area is being managed, and how the trend is developing as product mix and variation increases. **SMT**



Michael Ford is senior marketing development manager with Valor division of Mentor Graphics Corporation. To read past columns, or to contact the author, [click here](#).

The BOM itself has a complexity that no one person seems to be able to manage or even take responsibility for. It often ends up that there are multiple simultaneous "flavors" of BOM for a product...

2013 MEPTEC SEMICONDUCTOR ROADMAPS SYMPOSIUM

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September 24, 2013 • Biltmore Hotel, Santa Clara, CA

In the spirit of collaboration, this event will consist entirely of panel discussions, rather than traditional presentations. This will allow for more interaction among the speakers and attendees, so that the synergies, gaps, and differences of opinion can be explored more thoroughly. A day full of panel discussions will also allow representatives of more companies, including device manufacturers and large OEMs, and industry and standards organizations, to present their views. Join us for this first-of-a-kind collaborative event!

Over the years, MEPTEC's popular Roadmaps events have been attended by high level managers, CEOs, and CTOs, looking for validation and insight into technology and business directions for their companies, for their suppliers and, in some cases even their customers. At past events they, and their competitors who were presenting their own roadmaps, were looking for strategic help and

metrics of progress.

During its long and successful existence, MEPTEC has recognized the need for one essential ingredient above all others in achieving success with any semiconductor industry roadmaps: collaboration.

First, collaboration among trade associations, standards groups, OEMs, providers of analytic and design software, sub-contract service providers, and suppliers throughout the supply chain is increasingly critical to success. Second, as distinctions among semiconductor processing, packaging and assembly technologies, and design/testing protocols are disappearing manufacturers have greater need for collaboration.

The MEPTEC Roadmap event will bring together standards groups, industry groups and consortia, industry experts, device manufacturers, and representatives of the large OEMs to update their roadmaps and development activities, which may include 2.5D/3D as well as other driving factors pertinent to their business segments. Join us for this first-of-a-kind collaborative event! ♦



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IPC TMRC Highlights Economic and Political Trends

In keeping with the forward-looking theme of the conference, Gene Marks' presentation, "Economic, Political and Other Key Trends: 10 Things Happening Today That Will Affect Your Business Tomorrow," will take a thought-provoking and entertaining look at how the economy, Washington and technology affect businesses, and what successful companies are doing today to ensure future profitability.

Component Suppliers Struggling During Market Recovery

While all leading indicators point to the return of seasonal growth in the second half of 2013, the electronic component industry, including semiconductors, is currently seeing weaker orders than expected during this phase of market recovery.

Mobile DRAM Underperforms in Q1

Laboring under the combined weight of a seasonal slump and sharply lower average selling prices, the market for mobile dynamic random access memory (DRAM) posted lackluster results in the first quarter, according to a DRAM Dynamics brief from information and analytics provider IHS.

TFT-LCD Industry's Capacity Increase Leads to Several Trends

WitsView research manager Boyce Fan says that the newly-added capacity leads to several possible directions for the TFT-LCD industry developments. Firstly, the new capacity is concentrated on the Gen 8.5 fabs, meaning the large-sized panel supply is largely lifted, and the price pressure on the large sizes is inevitable to solve the excessive capacity problem.

PC Industry Continues to Shrink; Down 10.9% in Q2

Worldwide PC shipments dropped to 76 million units in the second quarter of 2013, a 10.9% decrease from the same period last year, according to preliminary results by Gartner, Inc. This marks the fifth consecutive quarter of declining shipments, which is the longest duration of decline in the PC market's history.

Mexico's Cost Advantage to Drive Exports Growth

Within five years, higher manufacturing exports due to a widening cost advantage over China and other major economies could add \$20 billion to \$60 billion in output to Mexico's economy annually. And thanks to the North America Free Trade Agreement (NAFTA), U.S. manufacturers of components for everything from automobiles to computers assembled in Mexico also stand to benefit, according to new research by The Boston Consulting Group (BCG).

N.A. Semiconductor Equipment Book-to-bill Improves in May

North America-based manufacturers of semiconductor equipment posted \$1.32 billion in orders worldwide in May 2013 (three-month average basis) and a book-to-bill ratio of 1.08, according to the May EMDS Book-to-Bill Report published today by SEMI.

Smart Grid Tech Market: \$73B in Annual Revenue by 2020

Although the market for smart grid technologies is already established, representing more than \$33 billion in revenue in 2012, it has grown with little contribution from a number of countries with populations greater than 100 million, and with almost no activity in Africa, with its population of 1 billion.

Tablets Remain Lucrative Market; 39M Units Shipped in Q1

Tablets remain a lucrative market for the three largest world regions for consumer electronics and computer adoption: North America, Western Europe, and Asia-Pacific's Japan and South Korea. "Three regions of the world are expected to yield 97% of tablet revenues in 2013," says senior practice director Jeff Orr.

N.A. to Claim Nearly Half of \$72B Tablet Spend in 2013

More than 39 million tablets shipped worldwide during the first calendar quarter of 2013, representing the second largest volume of shipments to date; only bested by the previous quarter ending calendar year 2012, according to market intelligence firm ABI Research.

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EVOLUTIONARY SOLUTIONS

Build Quality In

by **Karla Osorno**

EE TECHNOLOGIES, INC.

Ask any customer to name the most important factors in choosing a supplier and you are likely to hear quality, cost, and delivery. These are the three areas where customer expectations are established and measured to evaluate a customer-supplier relationship. Interestingly, quality impacts costs and delivery. This is especially true when quality gaps result in increased costs and longer delivery times. Suppliers who understand this concept choose to build quality into the product rather than relying on inspection controls to ensure quality. Building quality in ensures they build products that meet internal and external expectations.

Build it in

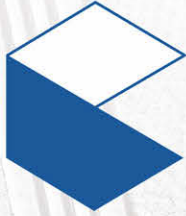
Every manufacturing process has its inputs and outputs. Manufacturers determine the desired output and then determine only the nec-

essary inputs and required steps to achieve the desired output. For each step, the process will include the quality activities and actual production activities within the production step. When done well, it will be seamless to determine which movements are quality activities and which are production activities. And some inspection activities will clearly be quality functions. By building in these quality activities, you will have more manufactured products and better results.

To visualize how critical building in quality can be, imagine a tall building—a high-rise or even a skyscraper. Each level of the building from the foundation to the rooftop must have quality built in and be inspected by the workers and inspectors as required. Failure to build quality in will result in additional costs, unnecessary delays, and potentially dire conse-



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BUILD QUALITY IN *continues*

quences. The steps to manufacturing a product also have foundational requirements, and each process builds upon the last.

Even though the number of variables in specific processes will differ, there will always be an order to the steps that makes the most sense. For example, one company may take raw materials, inspect the raw materials, build the product, and then ship the product. Another group tries to take the raw materials, build the product, ship the product, and then inspect the raw materials. In the second scenario, the inspection of raw materials would have to happen at the customer's location long after the fact. Sound like a good idea? Absolutely not. This may seem like it could never happen, but situations similar to this do happen. So check process steps by asking questions and observing, being careful to pay attention to the sequence of steps in manufacturing.

In-Process Inspection

In the sequencing, consider in-process inspection of prior steps by the assembler. Let's say you have a five-step process. When step two includes reviewing critical aspects of step one production, the opportunity to stop incorrect processing and make corrections exists. The operator at step two has authority to stop production, correct process steps, repair defects and keep time and costs from accumulating. Steps three, four, and five no longer have to deal with issues created at step one because they are prevented from reaching the later steps.

Step three reviews step two only and steps four and five review only the prior step. This is an efficient way to build quality into the process. Building it in reduces overall costs and speeds up the delivery to the end customer.

In-process inspection can also be handled by quality team members. When appropriate, quality will monitor processes by random inspection and using line stops to prevent defective products from being built.

In-process inspection can also be handled by quality team members. When appropriate, quality will monitor processes by random inspection and using line stops to prevent defective products from being built.

First article inspections are a form of product inspection. This type of inspection will confirm accuracy of product characteristics and some process accuracy. But processes are fluid and although some controls exist to keep the process stable, there is variability making in-process inspection important to the quality of the end product.

Cost of quality

For every product, there is a cost of quality. And every customer has to pay it. But they have to pay more when quality is inspected by someone other than the line operator. Costs are less when quality is built in to the product and production process.

Some of the other advantages that come from operator reviews include increased teamwork and accountability. As an operator, it is easier for me to respond to quality concerns for work I just completed moments ago than for work I did yesterday or the day before. I can own it and take personal responsibility for immediate correction. There is no need for defensiveness or negativity. I just acknowledge the issue and correct the process immediately.

Additionally, I am grateful to my team for not letting issues go on to the next step. All in all, it is a win-win situation for me, my team and the company.

Final Inspection

Final inspection activities add value and should not be eliminated. Final inspection evaluates the overall look, function and quality of a product. Test results may also be a part of final inspection review. This review along with review of product to customer documentation may also be conducted.

Random final inspection based on prior results is sufficient when in-process inspection is built in to the process. Sampling may be increased when results are unsatisfactory. All final

inspection results are documented as evidence of final inspection.

Often product certifications are provided to the customer with the end product. Any other documentation requested by the customer is also included with the shipped goods.

Metrics

Inspection results are documented at point of inspection whether in-process or final. Further analysis of the results is conducted to ascertain process root issues. These root issues can then be understood and corrected to benefit future production runs and of course the customer.

Making decisions using metrics is one of the most important activities a manufacturer can take on. When the data are collected and not used, the consequences can be tragic and costly.

Benefits

The magnitude of delivering high-quality products with the right cost and at the right

time is significant to manufacturers. By building in quality, conducting in-process inspections, making final inspections, and using metrics, manufacturers assure more consistent results and with fewer frustrations.

A focus on quality benefits manufacturers and customers in many ways, including improved communications and more successful partnerships. They also benefit by future business relationships and referrals. You have undoubtedly heard the adage "Build it and they will come." How about this instead: "Build it right and they will come." **SMT**



Karla Osorno is business development officer for EE Technologies, Inc., an EMS provider delivering complete engineering and manufacturing services with locations in Nevada and Mexico. To read past columns or to contact Osorno, [click here](#).

Video Interview

Valor MSS: The Solution for Agility

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Michael Ford, marketing development manager for Mentor Graphics, updates us on the Valor MSS suite. He explains how this manufacturing system has been growing and evolving to meet the needs of Mentor's customers.



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ECOs Reviewed: The Importance of Detailed Accuracy— Now More than Ever!

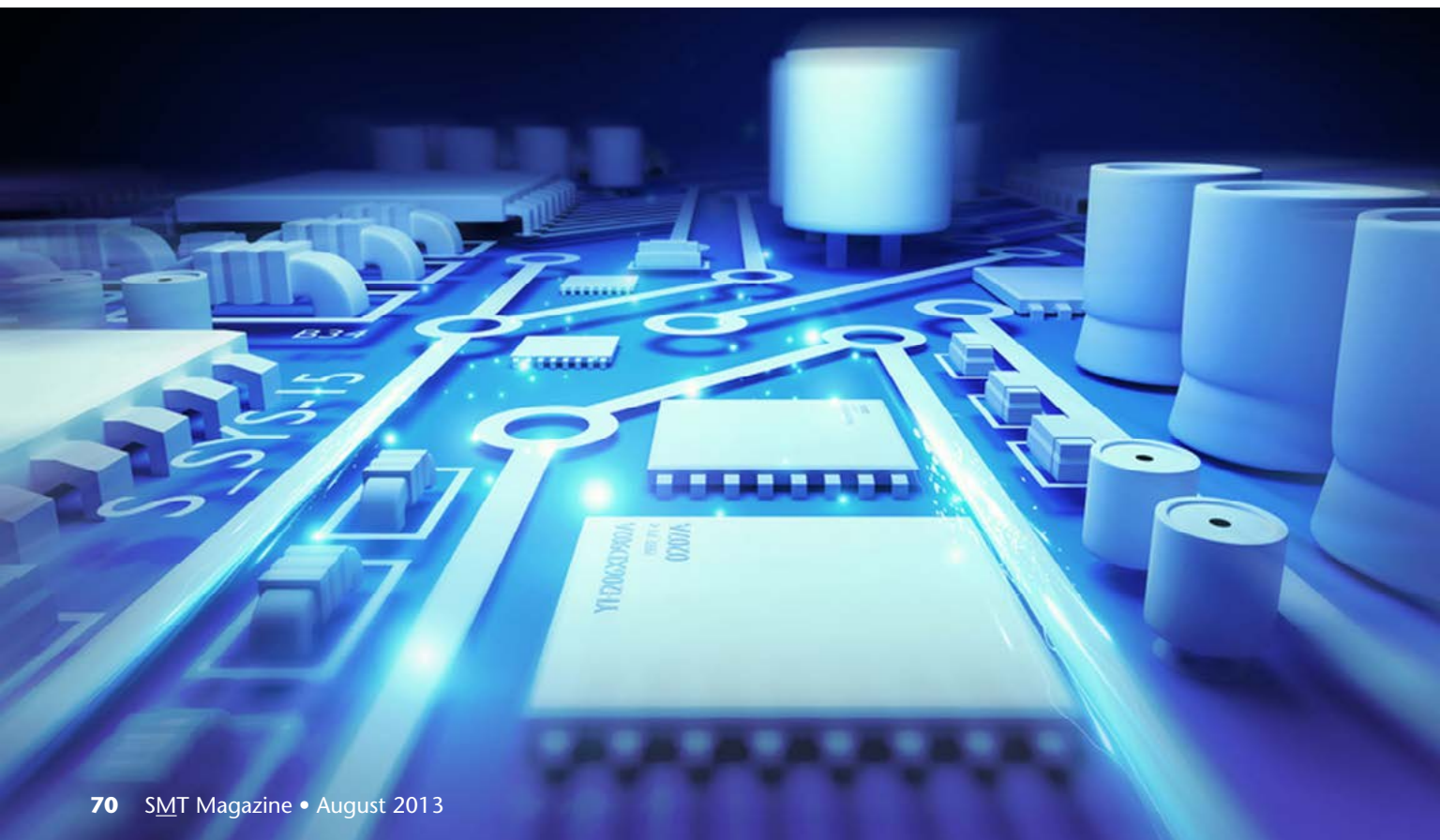
by Zulki Khan

NEXLOGIC TECHNOLOGIES, INC.

Engineering change orders (ECOs) have been part of the product development and PCB landscapes for as far back as one can remember. Particularly, when it comes to ECOs for PCBs, there are varying and endless reasons for these changes.

Certainly, PCB designers can perfectly layout a design and in theory follow written specifications to the letter and to the best of their abilities. But when you factor in the practicality of that design, virtually everything associated with it has its limitations, ranging from the material used to make the circuit board to assembly, machine tolerances, process limitations, and the list goes on.

But, before we continue, let's start at the beginning. First, the design is completed; the board is then manufactured and tested. However, once it's tested, the expected results aren't there, at least theoretically. Next, it is either re-spun and all necessary adjustments incorporated in the next revision design before it gets tested post-assembly. Or the other option is to keep the design as is and create an ECO to make the project work without re-spinning the design. ECOs are normally generated during the engineering debugging and bring-up phase of the board, when issues are found. Figure 1 shows an example of an ECO with the description of the changes along with a figure, an approval signa-





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ECOs REVIEWED: THE IMPORTANCE OF DETAILED ACCURACY *continues*

NEXLOGIC Engineering Change Order (ECO)					
<input type="checkbox"/> Product Change	<input type="checkbox"/> BOM Change	<input checked="" type="checkbox"/> Rework	<input checked="" type="checkbox"/> Deviation Req'd.	Issue Date: 10/3/2007	ECO Number 18378-1
<input type="checkbox"/> Design Change	<input type="checkbox"/> PCB change	<input type="checkbox"/> Dwg Change			
Customer:	Part Number/Description:	Revision: C1	Work Order No. 18378	Page: 1 of 1	
Reason For ECO:			Illustration:		
<p>PREP NEEDED BEFORE ASSEMBLY / REFLOW</p> <p>Before installing L2 (item 16) please place kapton tape over the two vias (shown in the drawing) before applying solder paste and before SMT reflow process.</p> <p>The purpose of the tape is to prevent any solder bridging to the holes from the installation of L2.</p>					
<p>APPROVED OCT 03 2007</p> <p>5:45 PM</p>					
<p>Approvals:</p> <p>Requester: Don Date: 10/3/2007 Approved By: [Signature] Date: 10-3-07</p>					
<p>NX0000-002 Rev. I/R Wednesday, October 03, 2007 12:11:58 PM</p>					

Figure 1: Sample engineering change order (ECO).


ture, and a date and time stamp on it.

These ECOs can then be applied to the rest of the same first lot. Let's take an example of 20 boards, in which the first five are assembled and some issues are found. ECOs can then be written and implemented on the remaining 15 boards. Or if all of them have been assembled, then these ECOs can be implemented on those complete sets of boards to make them work without having to re-spin these designs.

The ECO cannot come into play until the first set of boards has been designed, manufactured and assembled. Let's say that you are in the phase of bringing up and testing the PCB. Then, things don't work out the way you anticipate, and that's where the ECO enters. For example, since a signal can be measured with a specific current at a certain level, if it's not giving you that signal, you need to address this by possibly changing the value of a component like a capacitor, resistor, or inductor to get the results you're looking for—a small, easy fix. If this is the case, this change could be written up in an ECO with all the necessary details.

However, you might not be this lucky. Here is another, more challenging issue. Sometimes, during the debug phase, assembly floor personnel find that a certain placed component is difficult to assemble, and it is impeding the pick-and-place machine tolerances or getting in the way of another device and thus cannot be machine-placed. Or, for that matter, that component is too close to the board's edge, and as a result, it's protruding out of the defined chassis or box-build boundary.

A common mistake is deviating from mechanical constraints, mostly component height constraints and other keep-out areas. That usually occurs because the main focus is on the electronic design, the circuitry, or the hardware to determine if the circuitry is working properly. Consequently, developers may not conduct sufficient research on mechanical dimensions



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ECOs REVIEWED: THE IMPORTANCE OF DETAILED ACCURACY *continues*

or keep-out area limitations to determine if a PCB design is mechanically functional.

On the other hand, contract manufacturers (CMs) and EMS providers have well-organized teams composed of electrical, mechanical, and process engineers and technicians who work together to minimize ECOs. These teams design and assemble products more comprehensively with less need for creating ECOs; 90% of the time, the final product works correctly the first time.

But if design and mechanical engineering don't work together, the electrical and mechanical aspects of a PCB project can pose issues at manufacturing. As a result, there are considerable possibilities for ECOs, because various shortcomings or flaws surface in the initial phase. I'm not saying a perfect product results the second time around. Sometimes, it may take as many as three or four iterations. Nonetheless, ECOs are needed when you don't have the product working per your design in the first place.

However, the highly experienced and savvy PCB designer always takes a strategic approach to avoid or minimize ECOs. For example, if a component with a certain value is selected, and the value is increased or decreased, the circuitry will perform more efficiently and optimally. In this specific case, the savvy PCB designer has the opportunity to theoretically spec out a component, which is rated at five amps. If he doesn't want to run at the full rating of five amps, he can ratchet it down because from a practical point of view, a number of other factors need to be considered and incorporated, such as heat dissipation and sparking effects. So, in this case, the PCB designer optimizes his circuitry to run at three to four amps maximum and not at five amps.

Most often, novice PCB designers might overlook several of these factors in their calculations. For example, how much of an intrinsic safety factor is being considered? Also, how

much heat is dissipated when running a five-amp current on the circuitry? Could there be a thermal mismatch between different materials used in the PCB? Is there a potential mismatch between PCB materials and component packages? What kind of ground pour is required? How many ounces of copper should go on the board? And so it goes.

All of these techniques are learned with experience. But a novice PCB designer might not consider these and other factors, and once the first product is tested to the fullest extent, then ECOs are created to fix those issues in the second go around.

In summary, if you've done a thorough debugging process, you'll be able to incorporate most of the changes in an ECO. When the design changes are performed, you incorporate all the ECOs in the second revision so that you don't need to create subsequent ECO for the next debugging and bring-up phase.

The fewer ECOs, the better. This is true not only for ease of manufacturing, but also for the sake of time to market. If you have several ECOs, you'll need to perform re-work and put considerable time and effort into making the design work. Engineering will need to conduct comprehensive analysis when the revamped design is tested to assure every change is incorporated. When the prototype is manufactured the second time around, you should not have many ECOs. If you don't have any, you have done a great job. **SMT**

I'm not saying a perfect product results the second time around. Sometimes, it may take as many as three or four iterations. Nonetheless, ECOs are needed when you don't have the product working per your design in the first place.



Zulki Khan is the founder and president of NexLogic Technologies, Inc., an ISO 9001:2008-certified company, ISO 13485-certified for manufacturing medical devices and a RoHS-compliant EMS provider. To read past columns, or to contact the author, [click here](#).

2013 MEPTEC MEDICAL TECHNOLOGY CONFERENCE

*Global Momentum in the Medical Industry –
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Tuesday & Wednesday, September 17 & 18, 2013
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MANY FACTORS HAVE contributed to global momentum in the medical electronics industry, with the convergence of electronics technology and biological health sciences playing a major role. Growth in medical electronic applications (yes, there is an App for that!) will parallel Cell Phone and Tablet PC markets, with increases in computing power as well as optical resolution and touch sensor technologies. Current focus for mobile, implantable and large medical systems is on improved personal health, with preventative applications and advanced early diagnostics. Various integrated circuit (IC) technologies, now complemented by MEMS bio-sensor technologies, allowed for significant development in areas such as prosthetics, combining “artificial limbs” with “artificial intelligence”, sensing and reacting to very small electrical impulses from the brain, through direct body contact.

This conference will address the many industry challenges and opportunities including safety, reliability, miniaturization, manufacturing and



OLD MAIN on the ASU Tempe Campus, constructed before Arizona achieved statehood, will host the 8th Annual MEPTEC Medical Electronics Conference.

A combination of technical, market and health topics will be presented through presentations and panel discussions. Topics to-date include:

- Safety and reliability of medical devices
- MEMS and Mobile Health Care market overview
- Bonding techniques of new wire alloys for medical electronics
- Wafer Level Packaging and TSV for biomedical applications
- MEMS & Sensors for Medical Applications
- Security and psychological issues in medical devices
- Miniaturized electronic packaging for wearable health monitors
- Wireless communication/solid state batteries in miniature implantable medical devices
- Designing more reliable medical products
- “Fantastic Voyage” meets medical device design

materials as well as government regulations and political healthcare initiatives. The human body is a convergence of various biological phenomena and sophisticated electrical net-

works controlled by the brain, with the health sciences and medical electronics technologies converging to meet strong global demand. ♦

KEYNOTES



Sam Bierstock, M.D.

Day One Keynote

MEMS Technology and the Healthcare Industry: The Convergence of Timelines and the Perfect Storm

Sam Bierstock, M.D., BSEE Physician, Electrical Engineer, Medical Informaticist, Founder of Champions in Healthcare

Dr. Bierstock is a nationally recognized authority on healthcare and healthcare information technology. He is the Recipient of the George Washington Honor Medal, Freedoms Foundation for his work on behalf of our nation's veterans. ♦



Karthik Vasanth, Ph.D.

Day Two Keynote

Creating Solutions for Health Through Technology Innovation

Karthik Vasanth, Ph.D. General Manager, Medical and High Reliability Business Unit Texas Instruments

Karthik Vasanth received his Ph.D degree in Electrical Engineering from Princeton University in 1995. He joined the Silicon Technology Development group at Texas Instruments in 1995. In 2010 he became the General Manager of the Medical and High Reliability Business Unit at TI. ♦

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TOP TEN

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News

News Highlights from SMTonline this Month

① **ODMs 1Q NB PC Shipments Fall to Three-year Low**

Contract manufacturers of notebook computers suffered a worse-than-expected first quarter after shipments to clients like Apple Inc. and Hewlett-Packard tumbled to the lowest level in three years, according to a PC Dynamics Market Brief from information and analytics provider IHS.

② **Probe Posts Q1 Net Operating Loss; Expects Better 1H**

"We believe our end-markets have mostly stabilized and we are actively engaged in integrating Trident's business onto our platform, restructuring our expenses to drive better margins and increased organic growth," said CEO Kambiz Mahdi.

③ **Sparton Earns Medical Design Excellence Awards**

Sparton Corporation has again been recognized with honors by the medical design community. The latest award, in the category of In Vitro Diagnostics, was presented at an awards ceremony for the Medical Design Excellence Awards last week as part of the Medical Design & Manufacturing East Conference and Exposition in Philadelphia, Pennsylvania.

④ **Grum Receives SMTA's ICSR Best of Conference Award**

Harald Grumm from Christian Koenen GmbH received "Best of Conference Award" for his presentation, "The Potential of Stencil Technology—Choosing the Right Stencil Options to Maximize Yield and Earnings," at the 9th Annual International Conference on Soldering and Reliability, held May 14-17, 2013.

5 Haemonetics Selects Sanmina as Manufacturing Partner

Haemonetics Corporation has announced several important developments in the pursuit of its previously announced manufacturing transformation.

6 Jabil Completes Acquisition of Nypro

"We are pleased to finalize this transaction and look forward to integrating the Nypro business and customers with Jabil's current Healthcare & Instrumentation business," said Courtney Ryan, Jabil's Senior Vice President who will run the business from the current Nypro headquarters in Clinton, Massachusetts.

7 Flextronics Expands Relationship with Citrix

"We are happy to expand our successful relationship with Citrix and honored to have them as a partner," said Caroline Dowling, president of Integrated Network Solutions at Flextronics. "Expanding our service offering into Hungary is a great example of the value we can provide customers that leverage our strong supply chain solutions and broad global presence."

8 Plexus Marks 30th Year of Partnership with GE Healthcare

Plexus Corporation and GE Healthcare recognized a significant achievement, celebrating their strategic, 30-year partnership. Their collaboration generates economic activity across Wisconsin and other communities in which they operate.

9 Lincoln International EMS Stock Index Leads S&P

Lincoln International's EMS Stock Index outperformed the S&P 500 Index in the second quarter. Sanmina Corporation led Tier 1 companies in the Winner's Circle, posting a gain of 26% in its stock price over the period. In Tier 2, CTS Corporation led the group with a gain of 31%.

10 Flextronics Receives Excellence Awards from Ford

"Our partnership with our suppliers played a pivotal role in the progress we made on the One Ford plan in 2012," said Tony Brown, group vice president of global purchasing at Ford. "Our World Excellence Awards winners have shown a dedication to excellence. Thank you for helping Ford serve customers with the best vehicles in the world."

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EVENTS

For the IPC's Calendar of Events, click [here](#).

For the SMTA Calendar of Events, click [here](#).

For the iNEMI Calendar, click [here](#).

For a complete listing of events, check out *SMT Magazine's* full events calendar [here](#).

Microscopy & Microanalysis 2013

August 4–8, 2013
Indianapolis, Indiana, USA

Philadelphia Expo & Tech Forum

August 15, 2013
Cherry Hill, New Jersey, USA

NEPCON South China

August 27–29, 2013
Shenzhen, China

IPCA EXPO 2013

August 29–31, 2013
Gujarat, India

NEXTGEN AHEAD

September 9–11, 2013
Washington, DC, USA

International Test Conference 2013

September 10–12, 2013
Anaheim, California, USA

Capital Expo & Tech Forum

September 10, 2013
Laurel, Maryland, USA

2013 MEPTEC

September 17–18, 2013
Tempe, Arizona, USA

Failure Analysis of Electronics Short Course (CALCE)

September 17–20, 2013
College Park, Maryland, USA

Electronics Operating in Harsh Environments Workshop

September 17, 2013
Cork, Ireland

MRO EUROPE 2013

September 24–26, 2013
London, UK

ID WORLD Rio de Janeiro 2013

September 26–27, 2013
Rio de Janeiro, Brazil

SAE 2013 Counterfeit Parts Avoidance Symposium

September 27, 2013
Montreal, Quebec, Canada



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Pass the test with SMT!
Next month, we explore the latest and greatest test and inspection processes for PCB assembly. In September, our veteran contributors will focus on ICT, HALT, HASS, and much more.

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