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Featured Content

THE WAR ON PROCESS FAILURE

This month, *SMT Magazine* takes on those pesky process failures—from soldering defects and device cleanliness, to challenges of mission-critical product and the link between head-in-pillow defects and warpage.

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EDITOR'S NOTE

A Letter from the New Editor

by Stephen Las Marias
I-CONNECT007

Apart from the new strategies we are implementing in our magazines here at I-Connect007, there's another thing that will seem new to you—if you have been an avid reader of *SMT Magazine*. It's me (check out the handsome photo at the end of this article), the proud new managing editor of this publication.

I'm taking this opportunity to tell you a bit about me and provide some insights as to where things are headed for *SMT Magazine*. I have been an editor in the business-to-business (B2B) publishing industry for more than 12 years, covering the electronics industry—from microelectronics design and systems to electronic components, sub-assemblies, and supply chain—to factory automation and control systems technologies. While it will be a huge challenge to follow the steps of my predecessors here at *SMT Magazine,* I am motivated to contribute my ideas and continue to improve the quality of our magazines.

With my introduction finished, let's move on to the August issue of *SMT Magazine.*

As you may have noticed, we have changed the way we develop the content for our magazines here at I-Connect007. The electronics industry has been changing at a rapid pace—breakthroughs are being made almost on a daily basis—therefore we also have to adapt to make sure our magazine content is fresh and relevant, and address the latest challenges of the PCB design, fabrication and assembly industries. You have already seen it in our July issue, wherein our focus was on supply chain and supply chain management.

For this issue, we tackled process failure in manufacturing electronics assemblies. I am pretty sure you will find our lineup interesting and thought-provoking.

Based on our survey, the various businesses we cover can be summarized into four major issues: poor process control, poor training of

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A LETTER FROM THE NEW EDITOR *continues*

employees around quality, inability to quickly identify where and how waste is being created, and poor technical support from suppliers. David Dibble of New Agreements Inc. wrote an elaborate narrative on the results of our survey, as well as suggested some strategies that may help businesses in our industries address these issues. You can find a snapshot of David's article inside this issue, but the full article is published in this month's *The PCB Magazine*.

Verdant Electronics' Joe Fjelstad has written a piece on declaring war on process failure. In particular, he highlighted one of the most prominent causes of defects and failure in electronics, and mentioned how businesses may defeat such a prominent foe.

Another article worth noting is the collaboration between OEMs and EMS firms to combat head-on-pillow defects. Written by technical folks from Alcatel-Lucent, Ericsson, Celestica Inc., Flextronics International, Sanmina Corp., and Plexus Corp., this article addresses the root cause of head-on-pillow (HoP) defect—specifically the link between HoP defects and component warpage—and proposes the need for revised acceptance criteria when it comes to maximum warpage in BGAs.

Alpha's Jason Fullerton also talks about HoP in his article, as well as area array soldering and defect formation mechanisms.

Amy Yin Chen of Naprotek presents seven of the most common and potential options for addressing quality and manufacturability challenges of mission-critical products—in particular, military and aerospace PCBAs, which, in reality, utilize mixed technology, either due to legacy designs or concerns about the interconnection strength of SMT connectors or other critical parts that may be subject to significant shock or vibration.

> "If you are having challenges in any of your processes, please flip through the pages of this issue. I am pretty sure you will be able to get an idea about how to solve these issues, or perhaps find an expert who may be able to point you in the right direction."

An article from KYZEN and STI Electronics, meanwhile, looks at another angle when it comes to quality of assemblies: device cleanliness. It says insufficiently cleaned electronics can cause problems due to intermittent connections, corrosion, electrical shorts and arching, and therefore can negatively impact device functionality and end-user requirements.

Finally, Bob Willis discusses the different board and solder defects, and mentions some strategies to help solve these issues.

If you are having challenges in any of your processes, please flip through the pages of this issue. I am pretty sure you will be able to get an idea about how to solve these issues, or perhaps find an expert who may be able to point you in the right direction. Don't forget to check out our sister publications—*The PCB Magazine* and *The PCB Design Magazine*—to learn more about winning the war on process failure in other segments of our industry.

Meanwhile, we at *SMT Magazine* are looking to expand our roster of columnists and contributing authors. So if you have ideas—from industry trends to commentaries to technology developments—we'd like to hear from you. Feel free to drop me an e-mail if you want to contribute to our magazine or online website, SMT007.

In the mean time, I hope you enjoy reading this issue! **SMT**

Stephen Las Marias is managing editor of *SMT Magazine*. He has been a technology editor for more than 12 years covering electronics, components, and industrial automation systems.

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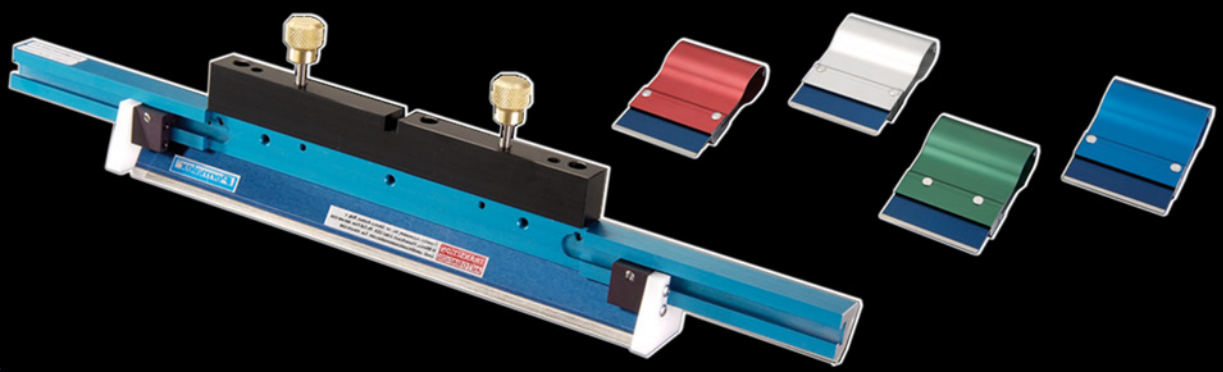

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The War on Soldering Defects under Area Array Packages: Head-in-Pillow and Non-Wet Open

by Jason Fullerton
ALPHA

"If you know the enemy and know yourself, you need not fear the result of a hundred battles. If you know yourself but not the enemy, for every victory gained you will also suffer a defeat. If you know neither the enemy nor yourself, you will succumb in every battle."

—Sun Tzu, The Art of War

What is Head-in-Pillow and Non-Wet Open?

The most difficult aspect of any soldering defect on an area array package is the inability to observe the defect easily. It is important to understand the characteristics of soldering defects in order to identify the proper action to take to mitigate the defects in a soldering process.

Head-in-pillow (HiP) defects are soldering defects on area array packages characterized by a lack of coalescence between the solder paste deposit and the package solder bump. In these defects, the solder paste deposit coalesces properly with itself and typically wets to the PCB land. Displacement of each solder deposit (paste and bump) is a common feature of HiP defects.

Non-wet open (NWO) defects are soldering defects characterized by a lack of wetting to a PCB land by a fully coalesced solder deposit on an area array package. In this defect, the solder paste and the package solder bump coalesce together fully without wetting to the PCB land. A spherical or nearly spherical shape along the PCB side of the bump is a common feature of NWO defects.

What Head-in-Pillow and Non-Wet Open are not

It is important to discuss defects that can share some symptoms with HiP and NWO, in order to contrast against defects that require different mitigation actions. One example of a de-

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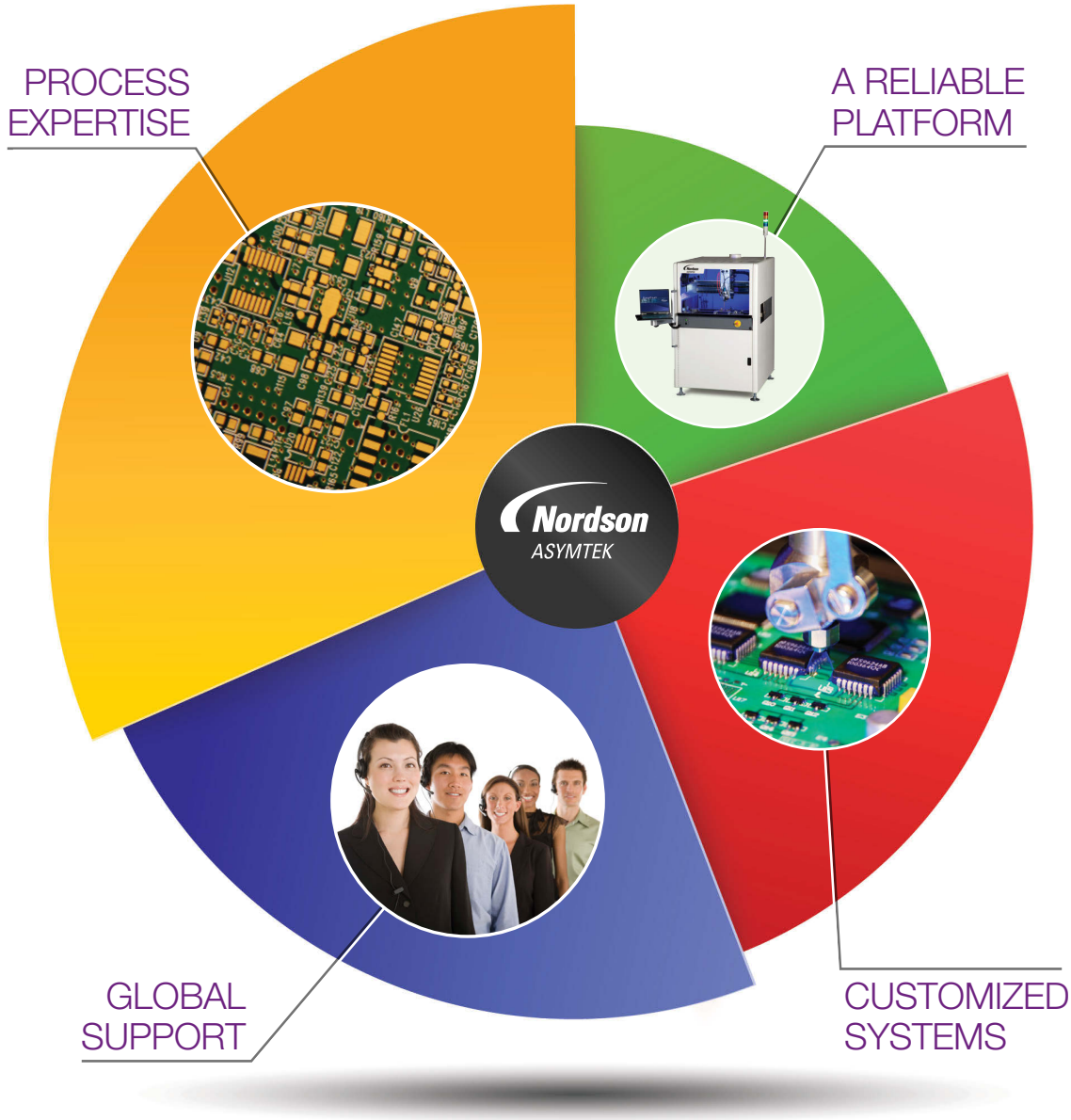

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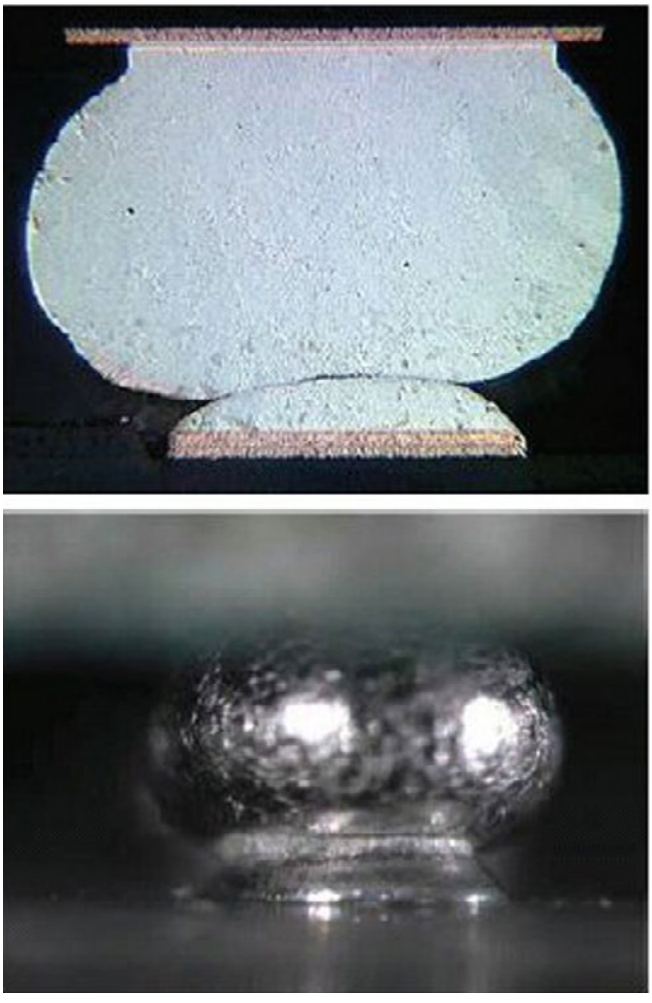

Figure 1: Head-in-pillow defect example, cross-section and endoscopic views.

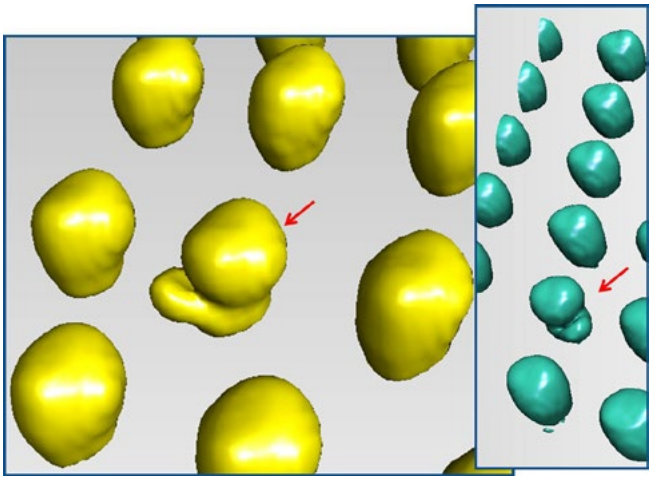

Figure 2: Head-in-pillow defect example, X-ray computer tomography view (courtesy Nordson Dage).

fect with similar symptoms to HiP and NWO is insufficient solder paste volume transfer during printing. In this case, it can appear that no wetting has occurred to the land and mimic NWO (especially if no paste has been transferred). If a small amount of paste has been printed, the resulting connection can initially appear to be consistent with HiP. Troubleshooting of HiP and NWO defects should include steps to ensure the solder paste printing process is properly controlled and performing well.

Another defect that can be confused with HiP is cold solder, which is characterized by a lack of coalescence of the solder paste deposit. HiP is a defect that occurs in the presence of a well-defined and controlled reflow process, which ensures coalescence of the solder paste deposit. Diagnosis of a defect as HiP should include an examination of the reflow profile to ensure that the process is not at risk of causing the occurrence of cold solder.

Non-wetting to a PCB land has many causes that should be familiar to most with experience troubleshooting solder defects. These defects can easily be confused with NWO since both defects share a symptom: poor wetting of a coalesced solder bump to the PCB land. The key difference is that NWO defects result in a solder bump that is spherical along the PCB side. A defect that is solely caused by poor PCB solderability will generally demonstrate the same shape as a typical area array solder connection: flatter and wider than a sphere and generally sharing the contour of the land along that interface. Testing the solderability of the PCB lands is an important step when attempting to determine if a wetting defect is a result of NWO defects.

Area Array Soldering and Defect Formation Mechanisms

During the soldering process, area array packages can appear to "drop" twice during a full reflow cycle. Each of the apparent drops by the package corresponds to an occurrence of coalescence of solder during the reflow process. The HiP and NWO defects represent the result of uncontrolled variation during one of those coalescence events.

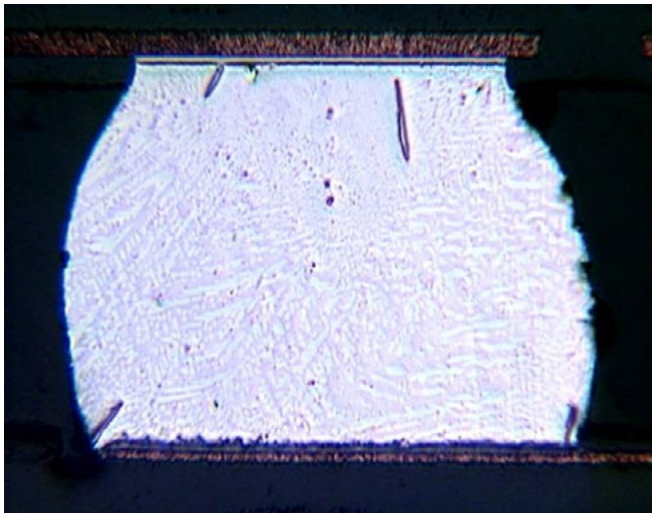

Figure 3: Typical area array solder connection cross-section.

As the PCBA reaches the liquidus temperatures of the solders, the solder paste will coalesce together into one large solder deposit. When this occurs, the package drops as the liquid solder is displaced by the mass of the package on the solder bumps. When the bumps and the paste have both reached a temperature where they are liquid, the separate solder volumes normally coalesce together and the package drops again. Upon cooling, the resulting solder connection has a characteristic shape with a flattened top and bottom (at package and PCB interfaces, respectively) and a rounded shape at the edges.

One mechanism of HiP formation is a failure of coalescence to occur between the solder paste and the solder bump. This prevents the joining of the solder volume into a single connection. Although the solder volumes share physical contact, they do not form a permanent connection and exhibit marginal electrical performance and no mechanical strength. Optimization of soldering process and materials can be effective at eliminating this type of HiP defect.

A second mechanism of HiP formation is also a primary driver of NWO defects. Both defects can be a result of warpage causing a co-planarity mismatch between the area array package and the PCB. This warpage can be described as having a "smile" or a "frown" warpage profile between the package and the PCB.

Figure 4: "Smile" and "frown" warpage profiles.

When a smile warpage occurs, the primary location for HiP and NWO defects to occur is closer to the edges of the package, where the package lifts away from the PCB. When a frown warpage occurs, the primary location for HiP and NWO defects is in the center of the package—again, where the package and the PCB have separated from each other during reflow. Mitigation of defects caused by warpage conditions is more difficult to troubleshoot and mitigate than pure coalescence failures.

HiP occurs when the two solder volumes reach liquidus when they are not in contact with each other due to the relative warpage mismatch of the assembly. Upon cooling, the dissimilar warpage of the assembly relaxes and the solder volumes come in to contact with each other for a short period before solidifying. This can allow for the molten solder bump and solder paste deposit to displace each other without coalescing together. Upon solidifying, the bumps form the namesake head (package bump) in pillow (solder paste deposit) feature as they rest against each other. This contact does not ensure a consistent

NWO defects also occur due to dissimilar warpage between the package and the PCB. This defect forms when the printed solder paste deposit has significantly more affinity for the solder bump than the PCB land prior to reflow. When the warpage mismatch separates the bump and land, the solder paste can remain in contact with the bump and reflow away from the PCB land surface. The solder paste and the package bump coalesce together, forming a larger bump at the package surface. The coalesced larger bump will form a spherical shape due to the surface tension of the molten solder. When the assembly cools, the dissimilar warpage relaxes and the bump typically comes to rest against the PCB land. The bump may form a small flat against the land or retain its spherical shape. This connection is not wetted to the

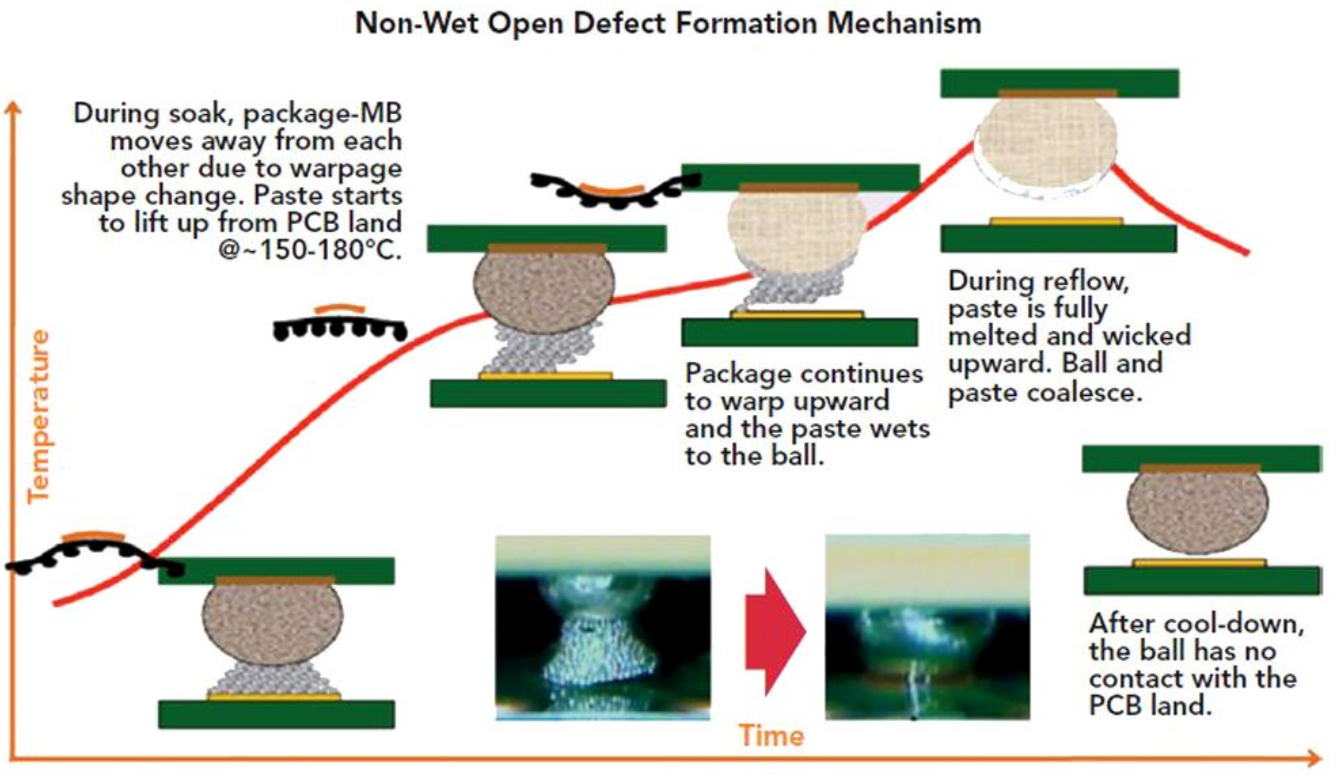

Figure 5: Non-wet open formation mechanism (courtesy Intel/SMTA)[1].

land and does not ensure a continuous, reliable electrical connection.

Strategies for Prevention of HiP: Process Factors

An improperly controlled process can be a significant contributor to HiP defects, particularly with the type that form due to an inability of the solder paste and solder bump to coalesce. The reflow profile, if defined in a way that exceeds the limits that a solder paste flux can withstand, can be a root cause of HiP. An extended preheat length or excessive soak temperature can exhaust the activator in a flux chemistry, thereby preventing the flux from performing its primary function: removing oxides from the surface of a solderable material (in this case, the solder bump). If the solder bump is oxidized, upon reaching liquidus temperatures it will not allow the molten solder deposit to coalesce across the oxide barrier.

The robustness of a solder paste to extended and hot preheat phase of a profile is specific to that formulation, but some general guidance is possible. Water-soluble pastes tend to be less robust to this condition than no-clean pastes, and water-soluble chemistries should be avoided if possible when HiP risk is a concern. Inert reflow can prevent this condition by preventing the solder bumps from oxidizing during preheat.

As the reflow profile is within the control of the assembler in most cases, it is important to experiment with the process to determine if HiP formation can be mitigated through reflow profile adjustments. It is important to understand that HiP can be low-occurrence defect, so testing should be performed on a sizeable sample of product in order to increase confidence that process performance has been improved. It is also important to understand that HiP can be caused by multiple factors, so process alterations can demonstrate improvement without complete elimination of the defect in some cases. Having a well-defined and robust reflow process is an important step to take first when troubleshooting HiP, as the other factors can be difficult to troubleshoot when process causes confound the solution by remaining an undiagnosed secondary cause of HiP.

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Strategies for Prevention of HiP and NWO: Area Array Package Factors

Some area array packages are more prone to warpage than others, due to the materials and design used by package fabricators. Component warpage can be difficult to predict and measure, and the current industry standards on warpage control are insufficient to prevent HiP defects in many cases[2]. Discuss the methods used to measure characteristic warpage on an area array package. This measurement cannot be performed during an actual reflow process, so unprocessed parts must be tested and a statistical model of a component's typical warpage can be formed. In the six case studies presented by Chan et al., it was demonstrated that the characteristic warpage measured in cases where HiP was encountered did not exceed package warpage requirements from JEDEC and JEITA. In other words, a perfectly good (per industry standard requirements) area array package can be a risk factor for HiP and NWO!

This fact is important to understand when suddenly presented with HiP and/or NWO on a new assembly or new package when used in a process that has not historically experienced these types of defects. Most external observers are quick to blame the assembly process upon discovery of a new defect. When the characteristic warpage of a component exceeds the limits necessary to cause HiP/NWO, very little can be done from a reflow process modification standpoint to mitigate the defects. The physics involved are quite complicated and it is very difficult to predict how a change in a reflow profile will affect that warpage of a component. Most commonly, any steps that can be effective in reducing warpage are far outside the requirements to ensure a robust solder reflow process.

One strategy that can be effective in mitigating HiP and NWO caused by warpage is to modify the amount of solder paste printed to the affected locations. Tibbetts and Antinori discuss a mathematical model used to calculate the optimum solder paste deposit volume to combat a case of HiP on a package that has exhibited a tendency to warp during reflow[3]. The desired volume of solder varies across the package layout in response to the amount of warpage the package experiences during reflow. Their work demonstrates that there is a relationship between solder volume, component warpage, and tendency to form HiP defects. Since the assembler can control solder paste volume but not component warpage, the strategy presented by those authors is one that takes advantage of the factors that can be controlled in an attempt to mitigate the defects.

> "The key properties of a solder paste that mitigate HiP and NWO defects are the paste's adhesion to the PCB land and package bump and the elasticity of the solder paste during reflow."

Strategies for Prevention of HiP and NWO: Solder Paste Materials

Some solder pastes are more robust to HiP and NWO formation than others. As discussed earlier as part of the process factors that can lead to HiP, water soluble formulations tend to be less robust to these defect conditions than their no-clean counterparts due to the no-clean pastes' inherently larger process window under reflow. However, within the family of no-clean solder pastes there can be a significant difference in performance with respect to HiP and NWO related to the physical properties of the pastes.

The key properties of a solder paste that mitigate HiP and NWO defects are the paste's adhesion to the PCB land and package bump and the elasticity of the solder paste during reflow. If a paste is able to stay in contact with both ends of the desired solder connection, the chances of forming a defect are greatly reduced.

A HiP defect that is caused by a separation of the paste from the bump during reflow can be prevented if that paste is tacky enough to stay in contact with the bump as warpage develops. The same goes for NWO defects caused by the paste pulling away from the PCB land; ensuring that the paste remains in contact with the land

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and bump, even in the face of warpage, is critical to preventing the formation of that defect.

HiP-resistant pastes are also designed to have the ability to remain continuous as the paste is stretched during warpage under reflow. This is analogous to the elasticity of a rubber band when stretched. Ensuring the paste deposit remains continuous is critical to ensuring that the two solder volumes are able to coalesce once reflow has been achieved.

Unlike very familiar tests performed on solder paste materials (e.g., voiding resistance, slump resistance, and tack testing), there is no standard test for HiP and NWO resistance. Direct testing of physical properties (viscosity, tack, etc.) cannot be directly correlated to HiP and NWO performance. This leads to solder manufacturers creating their own proprietary test methods to characterize and benchmark paste performance with respect to these defects. There are some pitfalls to this type of testing and it is important to discuss with your solder paste manufacturer how the test data is generated and analyzed to ensure the data provides a good reflection of actual performance.

> **“The major difficulty in developing HiP and NWO characterization tests is that these defects can occur with very low frequency, and it can be difficult to ensure formation of these defects in a repeatable fashion.”**

The major difficulty in developing HiP and NWO characterization tests is that these defects can occur with very low frequency, and it can be difficult to ensure formation of these defects in a repeatable fashion. Simply reflowing a test vehicle with a variety of area array packages is not sufficient to demonstrate robustness to HiP and NWO. Test of this nature, which are likely to result in zero HiP or NWO defects under typical conditions, fall prey to a data fallacy: If a test sample with no defects is a common outcome of a test, how can two test samples be compared against each other when they both result in zero defects? Is sample A better, worse, or the same as sample B, as both have zero defects? In addition, can either sample A or sample B be advertised as being completely resistant to the defect? In this situation, samples A and B cannot be differentiated from each other and there is no guarantee that either formula has solved the problem.

One hallmark of a good characterization test is create a test that is “designed to fail” by creating conditions that are at the very limits of performance expectations. In other words, designing a test where defects are assured to occur then changing inputs and measuring the rate at which defects occur allows for relative comparison of each sample. These types of tests are excellent at identifying when performance has been improved or deprecated when comparing multiple test samples.

Another consideration when analyzing test data is to be skeptical of claims to “eliminate HiP defects” by citing test data. Characterization tests are excellent tests when used as a tool to compare performance across similar conditions. Using a characterization test to make a claim of complete elimination of a defect is an example where a high risk of an error of the first kind (a false positive) exists. The old adage that you cannot prove a negative holds here. A claim that a solder paste eliminates HiP and NWO defects is a strong claim, but basing that claim on testing performed under controlled conditions only proves the claim until the first example from the field where HiP or NWO is discovered. A claim that a particular solder paste is more resistant to or less likely to experience HiP/NWO defects than other solder pastes is a more appropriate claim to make based on characterization testing.

A third consideration when analyzing a solder paste manufacturer’s HiP and NWO test data is sample size. All statistics are estimates to some degree, and those estimates gain precision with increased samples. Characterization testing for HiP and NWO should be performed in relatively large sample sizes in order to increase

confidence that the results will hold true when applied to a large-scale manufacturing process.

Final Thoughts

HiP and NWO defects are particularly difficult to troubleshoot and mitigate. As Sun Tzu points outs, if the reflow process is not well defined and controlled (you do not know yourself) you will succumb in every battle against HiP and NWO. Having a well-controlled reflow process but not understanding the intricacies of HiP and NWO (you know yourself but not your enemy) only ensures that you will be unable to fully defeat HiP and NWO, and should expect to suffer mix of defeat and victory. Fully understanding the mechanism behind HiP and NWO formation (knowing your enemy and yourself) means you do not need to fear the result of assembling a hundred boards. Who knew that Sun Tzu would make a good soldering engineer? **SMT**

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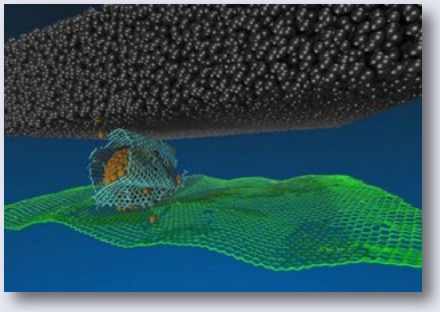
Jason Fullerton is a customer technical support engineer at Alpha, an Alent plc company.

Simulations Lead to Design of Near-frictionless Material

Argonne scientists have developed a hybrid material that exhibited superlubricity at the macroscale for the first time. ALCF researchers helped enable the groundbreaking simulations by overcoming a performance bottleneck that doubled the speed of the team's code.

While reviewing the simulation results of a promising new lubricant material, Argonne researcher Sanket Deshmukh stumbled upon a new phenomenon.

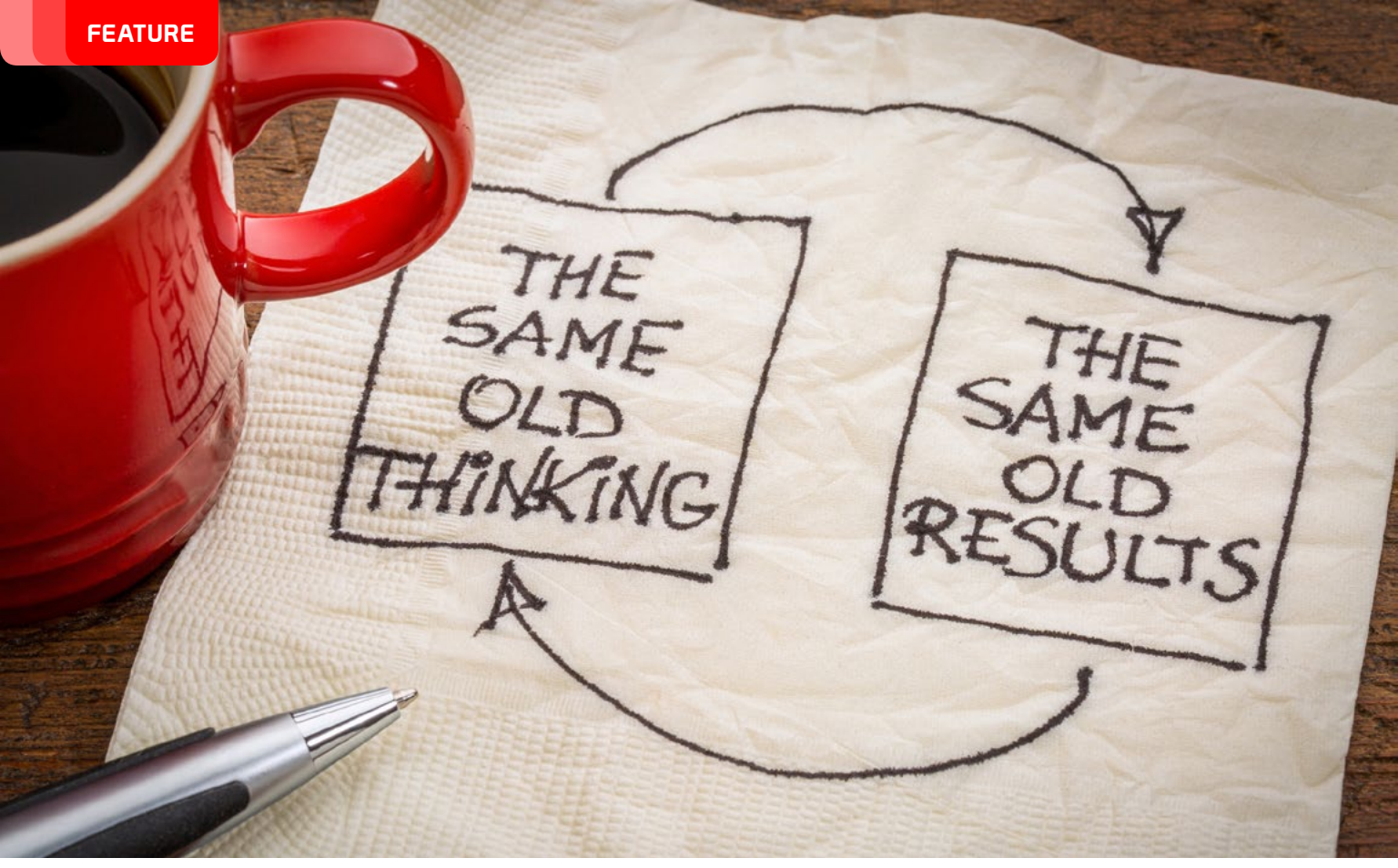
"Sanket said, 'you have got to come over here and see this. I want to show you something really cool,'" said Subramanian Sankaranarayanan, Argonne computational nanoscientist, who led the simulation work at the Argonne Leadership Computing Facility (ALCF), a DOE Office of Science User Facility.



They were amazed by what the computer simulations revealed. When the lubricant materials—graphene and diamond-like carbon (DLC)—slid against each other, the graphene began rolling up to form hollow cylindrical "scrolls" that helped to practically eliminate friction. These so-called nanoscrolls represented a completely new mechanism for superlubricity, a state in which friction essentially disappears.

"The nanoscrolls combat friction in very much the same way that ball bearings do by creating separation between surfaces," said Deshmukh, who finished his postdoctoral appointment at Argonne in January.

Superlubricity is a highly desirable property. Considering that nearly one-third of every fuel tank is spent overcoming friction in automobiles, a material that can achieve superlubricity would greatly benefit industry and consumers alike. Such materials could also help increase the lifetime of countless mechanical components that wear down due to incessant friction.



DECLARING WAR ON FAILURE IN ELECTRONICS

by Joseph Fjelstad
VERDANT ELECTRONICS

Everything fails. Think of anything in the universe and the specter of failure is inevitably there at the end. On the positive side, every failure is arguably preceded by success. That success can be marked in the form of a beginning. The stars formed from the matter created in the Big Bang, and were each and every one a success story in their own right by having accreted hydrogen gas in sufficient quantity to explode into light. Evolution is another amazing success in terms of diversity of life on this planet over time. However, both stars and evolution have failed as well—both have done so uncountable times.

The simple truth about the end of everything is captured in the opening two-word sentence of this piece: "Everything fails." Clearly, it must be a fool's errand to declare war on a foe that cannot be beaten. Or is it? Failure is a foe that needs to be taken on even though we know it will win in the end. Consider it more of a war within which many battles will be fought and any of those that are won against the foe named "failure" will advance and serve the needs of a global population.

Some elaboration on that last thought is owed the reader. Think of this for a moment: In 2014, the world welcomed its seven billionth inhabitant. In 2020, just five years from now, that number will be 8 billion. Now comes the nexus: The electronics industry is producing somewhere between $1.5 and $2 trillion worth of products per year. The vast majority of those products are targeted to serve the 3 billion people at the top of the world's economic pyramid while largely ignoring the needs of the 4 billion, soon to be 5 billion customers with similar needs. Withholding for a moment judgment as to the right-headedness of this, let me just say that it seems that a bet is being missed.

Most companies focus on the near term and the needs of those with extra cash in their pockets looking for the next new thing. Products have ever faster cycles of development along with their push to market, often with

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much fanfare. Avid consumers line up for the next tech fashion items, even before their old products have reached end of life. It has been said that economics runs on the premise that wants exceed needs. Product marketers do their best to convince the consumer that the things they want are truly needs. Does everyone who stands in line need that new device? No, they do not, but it serves the purpose of the marketers who really do not care much about failure because it is an opportunity to make and sell a replacement.

In 1932, Bernard London, author of "Ending the Depression through Planned Obsolescence," prescribed destroying outdated products and castigated those who tried to get longer life from still serviceable items. In his time, it arguably made some sense. The times were definitely more egalitarian then. A contemporary of London was Aldous Huxley, who also wrote, interestingly enough, in 1932, "Brave New World," but it was about a dystopian future, anything but egalitarian, where hypnopaedic messaging such as "Ending is better than mending" and "Less stitches means more riches" were broadcast to the populace to get them to toss out the old and buy the new. Ironically, Huxley offered up the same message as London did but having a grimmer, more disparaging viewpoint. We are arguably in that time now to some degree as we are more accepting of failure. Who has not heard a friend or colleague say, "I wish my old phone would die so I can get a new one?" This attitude does not serve well the future needs of the planet, if everyone on the planet is to be served.

Think now of the individual in a developing nation, somewhere in the world, who is making $2 per day. When that individual purchases an electronic product or any other product for that matter, their fondest wish is that the product will last indefinitely (or at least until the end of their need) because, no matter the cost, it is necessarily viewed as a lifetime purchase. Moreover, the world needs them now more than ever to have those reliable products so they can lift themselves out of grinding poverty due to a lack of education. Handhelds and wireless communications are key to allowing them to get that education and perhaps bless the planet by allowing us to tap all of the untapped genius that goes unrealized and unused—a great pity and loss. The world's poor are, ironically, much like those customers in military, aerospace, medical and automotive product markets. Failure is not an acceptable option if it can be avoided. To serve their needs a war on failure must be waged.

> "The problem with focusing on improving just reliability within the existing manufacturing paradigm is that it too often seeks ways to identify and treat symptoms while ignoring the disease."

The Battleground

Failure, in electronics, while not necessarily desired by either manufacturer or consumer, is expected. We are, in a sense, inured to failure. We expect problems. This is not to say that the industry has not attempted to improve reliability. Much is being done in an effort to improve reliability with new solder alloys, new fluxes, new materials, new equipment and process parameters, etc. The problem with focusing on improving just reliability within the existing manufacturing paradigm is that it too often seeks ways to identify and treat symptoms while ignoring the disease. In electronics, one of the most prominent causes of defects and failure is found in the soldering process and the trillions of solder joints that are created annually. Soldering is a useful technology (and will likely be used in much product in the future as it has in the past) but it comes with many challenges, which have been exacerbated by the forced conversion to lead-free solder to meet needless EU mandates. For evidence, look at any electronics industry journal or conference proceedings and one will find countless articles on solder-related challenges and defects and how to remedy them.

The complexity of the soldering process and all of the expensive test and inspection equip-

ment add cost, but no true value. They are much like medical tests used to detect disease in humans; they may alert one to the problem but they do nothing to treat it. Detection should not be confused with treatment, but too often it is. We applaud ourselves more for finding defects than for eliminating them. Clearly, soldering is an imperfect process and one that is unlikely to ever achieve perfection. Moreover, it is cause for collateral damage to both components and PCB substrates because of the high temperatures required and the deleterious effects associated with those high temperatures. Even after the product is built, solder remains the weak link. Failed solder joints are a leading cause product failure in use.

Given the situation, how might one defeat such a formidable foe? Eliminate it. Solder is useful but not necessary for electronic assembly. Most electronic products can be built without solder today by simply reversing the manufacturing process. That is, rather than soldering components to circuit boards, create component boards and build up circuits on them. The manufacturing infrastructure exists; it simply needs to be repurposed. Most legacy components can be adapted, but some are better than others. However, the purpose of this brief piece is not to provide all of the details; the subject has been written about in numerous papers with references provided at the end. Rather, the purpose is to appeal to the reader's reason by asking for their consideration of a few questions.

1. How much does it cost to procure equipment for and operate the soldering process?
2. How much does it cost to procure and use inspection equipment to support the soldering process?
3. How much does it cost to procure and use solder rework and repair equipment?
4. How much does it cost to service warranties against failure?
5. Could the monies spent in support of the solder process be better spent in making the product more robust while using many fewer manufacturing, cleaning, inspection, and test steps?

There is an adage that goes like this: "First do the right thing, then do things right." The EMS industry appears to have declared a one-sided truce with solder by continuing to use it, but solder continues to fight with the EMS industry. It is a Sisyphean effort to try to conquer such a foe; moreover, the definition of insanity left to us by Albert Einstein is, "to do the same thing over and over and expect different results." Sadly, our species is prone to forming habits. It is easiest to do what we did yesterday. Unfortunately, the future demands adaptation and change from its survivors. In the words of Bob Dylan, "If you ain't busy growing, you're busy dying." On the bright side, we have a choice.

In summary, the electronics industry is in a continuing struggle with solder, whether or not it fully recognizes it or remains in denial. Failure is the enemy and solder is, unfortunately, the root cause. There exists a potential to save many billions of dollars while making products that are, at once, more reliable and more environmentally benign by simply eliminating solder from the process. It is just a matter of will to enter into a war on failure. **SMT**

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Verdant Electronics Founder and President **Joseph (Joe) Fjelstad** is a four-decade veteran of the electronics industry and an international authority and innovator in the field of electronic interconnection and packaging technologies. Fjelstad has more than 250 U.S. and international patents issued or pending and is the author of *Flexible Circuit Technology.*

How Clean Is Clean Enough to Achieve Reliable Electronic Hardware?

by Mike Bixenman and David Lober,
KYZEN;
Mark McMeen and Jason Tynes,
STI ELECTRONICS, INC.

The golden age of the Internet, digitization and social networking is in full swing. These technologies enable the Information Age from which every company and entrepreneur can cut costs, innovate new offerings and reach billions of new customers. Embedding information and telecommunication technologies in the form of sensors will increase productivity throughout the entire economy[1].

Information technology drives processing speed, memory storage and, ultimately, new capacity. Technology is constantly improving digital product innovations that are increasingly faster, more efficient, more useful, more affordable and more powerful[2]. Speed is enabled from denser circuit designs, tighter pitch and shorter line spacing. The risk of residue present on the surface and under bottom terminations can impact chip performance at these shrinking dimensions.

Reliable hardware is more challenging to reproduce due to component size, residues trapped under bottom terminations, shorter distance between conductors, higher pinout devices in a smaller footprint, increased electrical field and environmental factors[3]. There is no one universal test method for quantifying reliability risks. The amount and nature of the data generated depends on the product being

Figure 1: Example of residue under bottom-terminated components (BTCs).

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produced, the consequences of failure and the end-use environment. A three-phase approach is commonly used to specify the manufacturing process requirements[4].

- Phase 1: Screening experiments with inexpensive test vehicles
- Phase 2: Validation experiments with more representative test vehicles
- Phase 3: Verification runs on manufactured assemblies

The purpose of this article is to develop an improved test method to measure the resistance on non-cleaned and cleaned test boards using low residue solder pastes under a series of bottom termination components. Testing the location, flux type, quantity and mobility may provide an improved risk assessment of reliability expectations.

The problem is that current chemical and electrical test methods limit the effectiveness for testing residues entrapped under component terminations. Residues under the bottom termination have the highest potential for leakage and are the least understood. Site-specific testing of the residue under the component termination has the potential to detect resistance drops. Gaining a better understanding of no-clean residues that do not outgas during reflow will help reliability engineers understand cleanliness at the interface.

Why Does Device Cleanliness Matter?

Insufficiently cleaned electronics can cause problems due to intermittent connections, corrosion, electrical shorts and arching. These effects can negatively impact device functionality and end-user requirements. A wide range of contamination sources can be found in many places, including fabrication residues on components, post-soldering flux residues, processing equipment, cleaning machine effectiveness, rework, etc., and requires a flexible evaluation approach.

Bottom Terminated Components

Typical parts soldered onto the PCB have flux residues trapped between the component body and board (Figure 2). Cleanliness at the interface is critical to reliability and the least understood[3]. Ionics in flux residue can exacerbate contamination levels under the component and/or creation of high resistance shorts across pads.

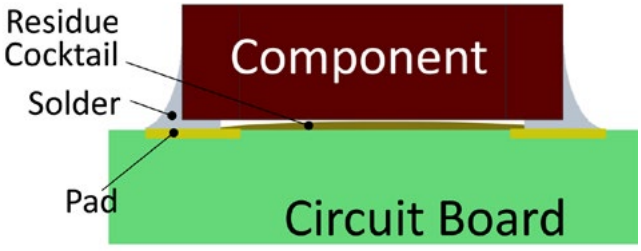

Figure 2: Residue under bottom termination.

Generally clean does not mean the product is clean where it matters most. Location of residue matters. Residue pooled under the component may still be active and ionic in nature. Pockets of contamination are influenced by flux type, placement, wash characteristics, solder paste volume, PCB cleanliness and component contamination. These factors create a "multi-variable" issue that is challenging to understand.

Experimental Design

This designed experiment seeks to quantify the influence of surface insulation resistance (SIR) on a specific set of ionic species and no-clean flux residues under bottom terminations. The intent is to explore SIR as it relates to species type, species concentration and conductor spacing. The output of this testing will be quantifiable relationships between:

1) Ionic Concentration vs. SIR
2) SIR vs. Conductor Spacing

These outputs will be used to further develop this method with the goal of improving industry guidelines for maximum ionic concentration levels for given board densities/conductor spacings. It will also be used to produce minimally acceptable SIR (cleanliness) levels.

The test board has sensors placed under the bottom termination. The sensor traces provide real-time SIR data within the residue. Locally

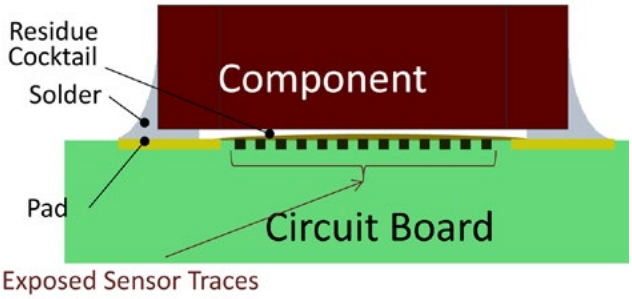

Figure 3: Sensors placed under bottom termination.

exposed traces route to the board's edge for electrical access to volume between component and board.

Background to the Problem

In electronics manufacturing, solder paste is deposited onto PCBs and used to produce solder connections between discrete devices and the PCB. The assembly is heated above the melting point of the solder and allowed to cool. This process causes the flux to volatilize and ultimately vaporize. During volatilization, the flux removes oxides and permits the solder to chemically bond with the PCB and component. Ideally, the flux then vaporizes and is removed by dissipating into the surrounding atmosphere, leaving only solder behind.

Practically, however, there is commonly a residual component of flux remaining—flux that never fully vaporized or was prevented from dissipating. This flux residue, depending on its chemical constituents, can have varied impacts on the final assembly. Many fluxes are designed to leave trace levels of inactive residues, rendering them relatively harmless. Conversely, flux is designed to attack metals, which makes leaving volatile/active fluxes on a PCB problematic.

There is a wide range of proprietary chemical makeups when it comes to fluxes. Regardless of flux type, the warrantying agent of the final product must have a clear understanding of the risks involved in producing and selling its products. Included in these risks are the detrimental effects of contamination sources. The clear warning sign of that risk manifests itself through the presence of ionic components near solder terminations. These compounds have the capability of migrating under a voltage bias, which produces a current. An even more dramatic result of the presence of ionic compounds is the creation of dendrites.

Dendrites serve as semi-permanent conductive paths between previously unconnected PCB

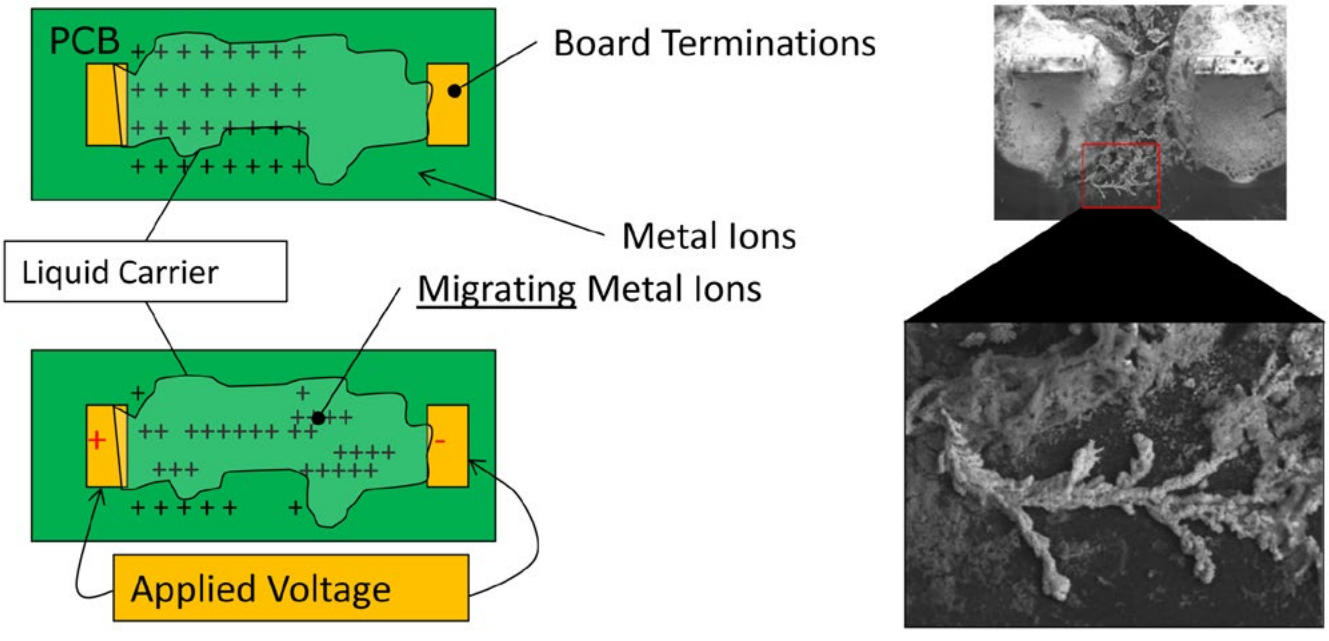

Figure 4: Active residues leading to leakage currents.

pads. They are constructed out of ionic compounds that were permitted to remain on a PCB and, under voltage bias, create a fully continuous chain of electrically conductive molecules between terminals. The result is current leakage and irregular performance in the final product.

Hypothesis 1: Some ionic constituents within solder flux residues are more detrimental than others.

Species Identification

The most commonly present ionic constituents within solder flux residues have been narrowed down to a handful of ionic compounds. Some compounds are more detrimental than others; however, the impact of each can be quantified. Below is a list of compounds, broken into groups of ionics (anion and cation) and weak organic acids.

Anions	Cations	Weak Organic Acids
Bromide	Ammonium	Acetate
Chloride	Calcium	Adipic Acid
Fluoride	Lithium	Formate
Nitrate	Magnesium	Maleic Acid
Nitrite	Potassium	MSA
Phosphate	Sodium	Succinic Acid
Sulfate		

Table1: Ionic constituents of concern on PCBs.

Hydration/Carrier System

Regardless of the compound, a fluid carrier system must be present in order to allow the ionic compound(s) to mobilize. The most viable carrier system is water. Water, without contaminants and in a normal air environment, tends toward a resistance on the order of 1–5 MΩ. The presence of sufficient moisture allows for the ionic species to mobilize in unique ways that provide repeatable resistance values that are often greater than 10 MΩ. Overhydrated compounds tend toward a resistance equivalent to water, masking the effects of the contaminant. A consistent hydration method is necessary to provide repeatable hydration levels to the ionics present on the PCB.

Hypothesis 2: Reduced spacing between test locations correlates to lower SIR values.

Conductor Spacing

It is theorized that increasing the spacing between test locations will demonstrate a corresponding increase in SIR resistance values. The coupon used to conduct this testing incorporates parallel, exposed sensor traces. These traces are .005" (.127 mm) wide and are separated by .005". Therefore, testing the adjacent sensor traces (7 to 8, 8 to 9, etc.) provides insight into the SIR over a .005" (.381 mm) gap. Skipping a

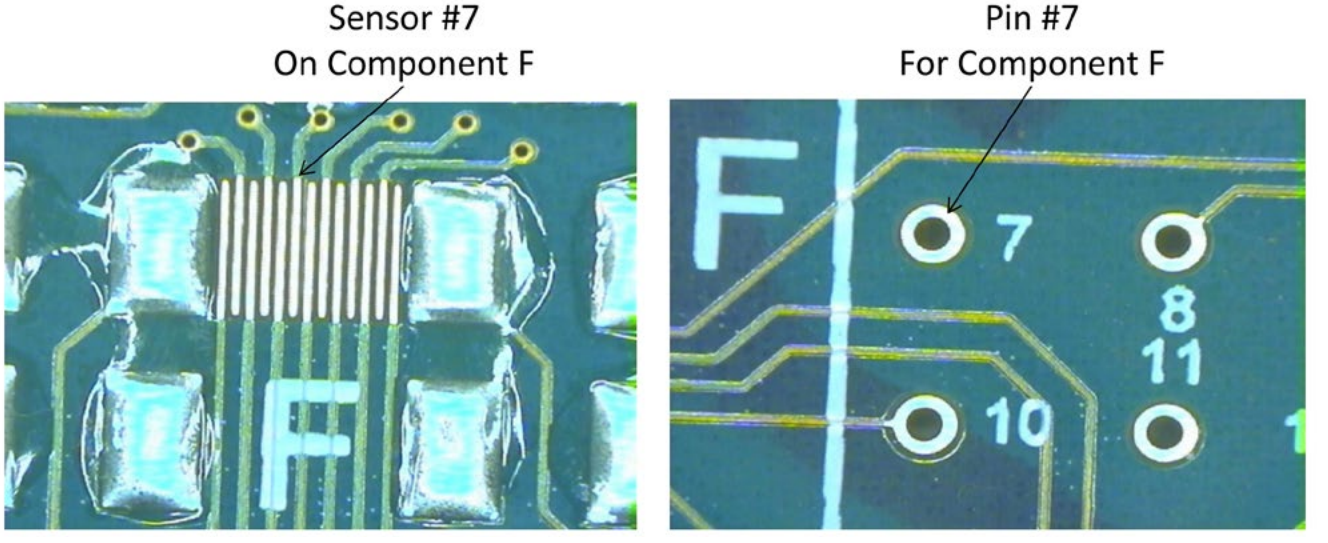

Figure 5: SIR Sensors under BTCs.

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trace (7 to 9, 8 to 10) provides insight into the SIR over a .015" gap (.005" space + .005" trace + .005" space).

With a total of 13 conductors, the effects of conductor spacing can be evaluated for .005", .015", .025" and .115" spaces. It is expected that the SIR for .005" will be substantially lower than that of .075" simply because there is a larger gap. The ability to vary conductor spacing will allow for the sensitivity of cleanliness levels to be associated with the density of the components on a board. A more densely populated board or one with fine pitch BGAs, for example, would have a more stringent SIR requirement than a board that uses only through-hole technology parts. The increase in conductor spacing could realize a decrease in SIR stringency. For this study, 5 and 15 mil spacing located at the center of the array was measured.

Noise Effects on High-Impedance Measurements

High-impedance meters measure resistance levels greater than that of polyimide or FR4 materials. For this testing, a representative voltage is applied across the test traces, and the current is measured. The equipment performs a quotient between the supplied voltage and measured current to determine the equivalent impedance. Representative voltages in a digital circuit tend to be 2.5–5.5V, and thus justifies that the supplied voltage be of an equivalent value. At 5.5V, a 1 MΩ resistor draws 5.5 µA of current—easily measured by standard equipment.

Data Findings

Flux Testing Results

Three solder pastes supplied by a common flux manufacturer were selected to have low, medium, and high activity flux compositions. These designations were provided by the flux manufacturer based from their knowledge of the flux formulation. Three boards of each flux were cleaned using an aqueous cleaning agent in an in-line washer at 15% cleaner concentration at 150°F. The cleaning agent selected was known from experience to be capable of removing all of the flux from underneath these components. The belt speed of the in-line was varied to give different levels of cleaning. The belt speeds selected were 1-ft./min which provided complete cleaning of the flux residues, 5-ft./min which provided partial flux removal, and 8-ft./min which provided virtually no cleaning. Following the aqueous cleaning process, the resistance between four sets of adjacent traces and four sets of alternating traces was measured. The measurements were carried out using ambient office environmental conditions (20–25°C and approximately 30% RH).

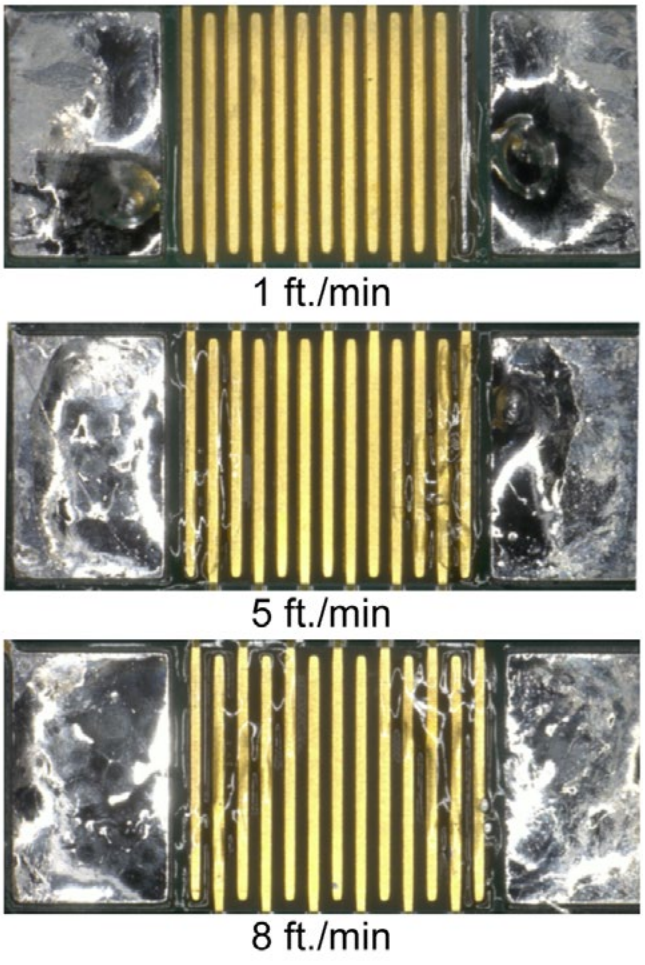

Figure 6: Residue remaining under BTC as a function of cleaning time: 1-ft./min (top); 5-ft./min (center); 8-ft./min (bottom).

Due to capacitive effects a stepped DC voltage waveform was applied. The +3.3V DC bias was applied for 15 seconds prior to a current measurement. The voltage was then switched to -3.3V for 15 seconds before another current measurement was made. This was then repeated

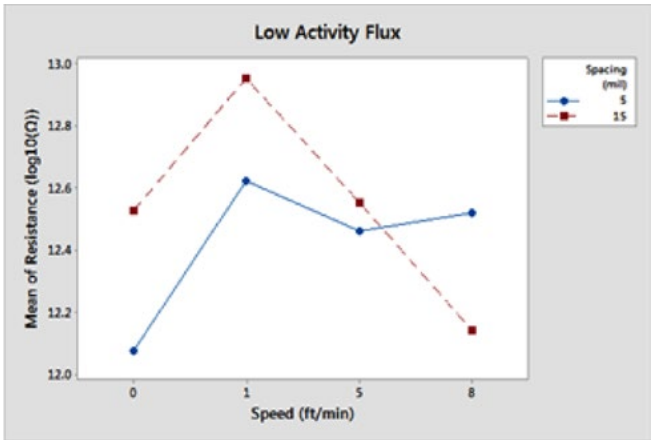

Figure 7: Low-activity boards cleaned and measured.

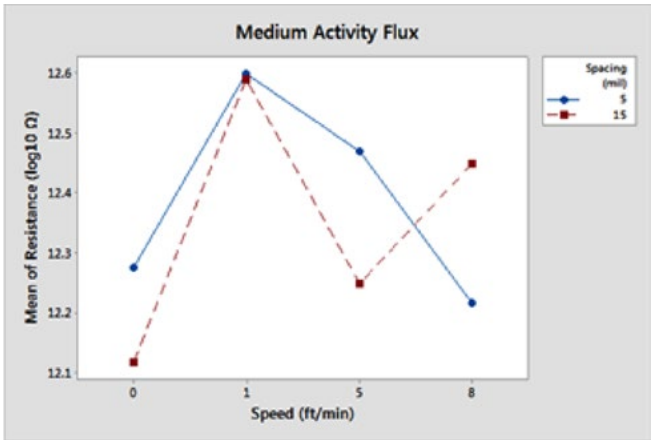

Figure 8: Medium-activity boards cleaned and measured.

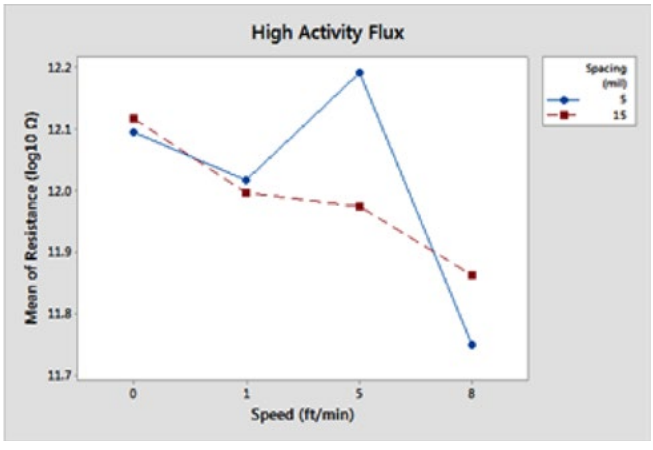

Figure 9: High-activity boards cleaned and measured.

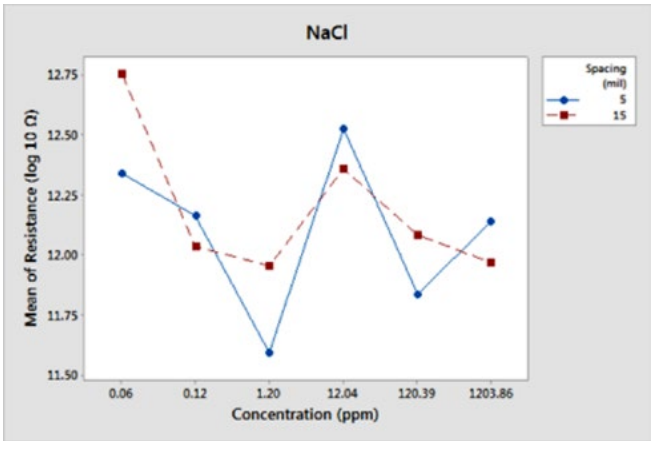

Figure 10: NaCl species data findings at PPM levels.

a second time yielding a total of four resistance measurements per sensor trace pair. The resistances for each sensor distance were average for each board. The data findings are presented in the figures below. Zero on the chart represents boards that tested the resistance of the solder paste residue before cleaning.

Species Results

For the species testing, one drop of the ionic species at the desired concentration was placed on the sensor traces. The board was then placed in a 110°C oven for 30 minutes and then allowed to cool in a desiccator for one hour. The results of the species testing are presented in Figures 10 and 11.

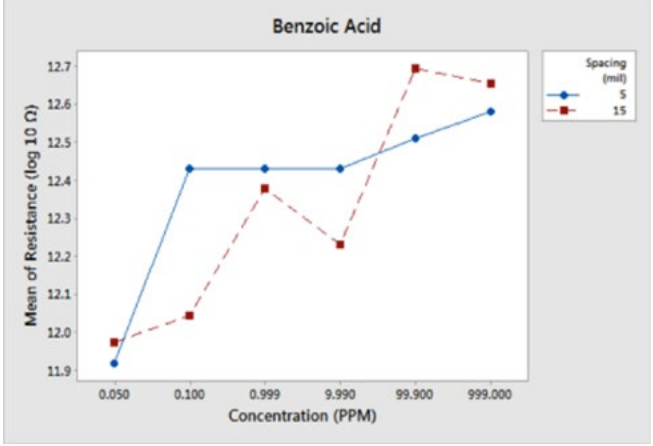

Figure 11: Benzoic acid species data findings at PPM levels.

Conclusion

There is a set of IPC specifications that drives industry compliance. The problem is that these tests do not provide the resolution needed to measure highly dense devices using BTCs. This creates a totally new environment that calls for improved test methods and specifications to quantify the issues and problems associated with residues under BTCs. The research is driving toward a better model for making accurate risk assessments.

OEMs currently count on CMs for qualifying and validating process conditions. The problem is that the CM warranty does not meet OEM warranty expectations. How does the OEM obtain the data needed to satisfy the CM warranty and consumer expectations? If these expectations can be integrated, the OEM now has the knowledge to make accurate assessments of their product toward consumer expectations. Quality and reliability engineers need to capture the right variables that allow them to meet their quality objectives. When people have horizons of 10–25 years, there is a gap in knowing whether or not you are clean enough. The problem is that the stakeholder is the OEM, not the CM who is making the decision on materials and process parameters.

To achieve this level of granularity, the testing methods in work have the potential to provide better resolution for answering these questions. Is the research method perfected today? No, but that is why you learn from the data findings, confirm your assumptions and design follow-on research to move from a hypothetical position to theory. The whole goal is confirm our theorems in an effort to improve standards.

The flux study confirmed the old saying "If you are going to do a job, do it right or not at all." While there was substantial variation in the data, this preliminary study shows that the electrical resistance underneath components can be measured using voltages that are representative of modern circuits and environmental conditions. This is not extreme.

The species testing provides needed insight into quantifying ionic levels for each ion that can lead to a drop in resistance. Follow on study is needed to gain a clearer understanding of the method for isolating specific ions. By doing so, an accurate assessment of levels can be correlated to electric field. **SMT**

"Is the research method perfected today? No, but that is why you learn from the data findings, confirm your assumptions and design follow-on research to move from a hypothetical position to theory."

***Originally presented by KYZEN at SMTA ICSR.*

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by Amy Yin Chen
NAPROTEK

Typically, mission-critical military and aerospace printed circuit board assemblies (PCBAs) are based on 100% surface mount technology (SMT) and optimized for manufacturability from day one of design. The reality is that many of these products utilize mixed technology, either due to legacy designs or concerns about the interconnection strength of SMT connectors or other critical parts which may be subject to significant shock or vibration. Use of different soldering formulations can drive challenges in meeting cleanliness standards. In many cases, these mixed technology designs often violate industry-standard design guidelines, creating manufacturability issues.

From a contract manufacturing perspective, the first option is to make design for manufacturability (DfM) recommendations for changes to the design that would correct issues that are likely to drive production defects. This is not always a viable option, especially with legacy products or products that have gone through an extensive qualification process. Consequently, the best OEM-contract manufacturing relationships in this area focus not only on eliminating issues that drive defects before they happen, but also have the flexibility to deliver superior quality even when redesign isn't possible.

To better outline issues that should be closely watched in the design process, here are seven of the most common and potential options for addressing them:

1. Mismatched Footprints: PCB design library footprints don't always match the specified component footprints, which can impact solderability on components with improperly sized pads. It can also contribute to additional defects when spacing among SMT and through-hole components is tight. Footprint accuracy should always be checked as part of the design review process.

If the design isn't changed prior to prototyping, the appropriate approach is to manually place the parts and provide feedback to the customer on the issues. When the component is an integrated circuit, it is bonded pin 1 to pin 1. The preferred option is that the PCB be re-laid out or the bill of materials modified.

2. Failure to Provide Proper Spacing/Clearance for Through-Hole Components: Mixed technology, double-sided boards

are often run on pallets through the wave solder in order to protect any bottom-side components that can't be exposed to the wave. This issue can also make it difficult to use automated insertion equipment. Use of IPC design guidelines can help the design team to avoid this issue.

The recommended clearance for fixturing is 75 mils. However, as products shrink, many PCB designers are going to 35 mils.

3. Exposed Via-in-Pad: Except in very special instances, there should be no open vias in pads, since the via can suck the solder from the component. Unless there are thermal or high-frequency design considerations this should be avoided in design or addressed during the board fabrication process.

For this case, the only option is to have the board fabricator plug the open vias.

4. Thermal Issues with Leaded Components: Use of through-hole components also drives the use of leaded components, when lead-free packaging isn't available. In a mixed technology PCBA, this means that some components can experience thermal damage during reflow due to the higher temperatures required by lead-free components. Where possible, mixing leaded and lead-free technology should be avoided. Even when a datasheet indicates that higher temperatures can be tolerated, damage may occur if the PCBA has multiple passes through reflow as a result of rework.

There are two options to minimize potential thermal issues. In some cases, a leaded reflow profile can be run in place of the lead-free reflow profile. The normal leaded assembly reflow profile is 210–225°C. Comparatively, lead-free solder has a reflow profile between 235–260°C. One option is to use an eight-zone reflow oven, of which the profile can be adjusted for a slower rise-to-peak temperature, eventually reaching 225–230°C. This achieves the melting point required by the lead-free components with leaded solder paste, without damaging the leaded components. Alternatively, leaded components can be hand soldered as a secondary operation following lead-free reflow.

5. Pads Connected to a Ground Plane: If the pads of smaller passive components, such as 0201s or 0402s are connected to a ground plane, the ground plane can act as a heat sink and create tombstoning.

6. Mismatch between Solder Paste and Stencil with Fine Pitch Components: When the designers generate paste layers, they typically base their assumptions on component requirements without necessarily knowing which type of solder paste will be used. This isn't a problem for components that are greater than 0.5 mil pitch, but can create issues with components with 0.4 mil pitch and below. For example, if a product has a 0.3 mil pitch microBGA, type III solder paste won't fit through the aperture space on the stencil. The standard formulas for aspect and area ratios don't work on microBGAs.

Typically the only option for addressing this is to change the aperture size or the solder paste type. It is recommended that a square rather than round aperture for microBGAs is used.

7. Cleanliness Challenges: Military/aerospace products often have unique cleanliness requirements. This can be an issue for mixed technology PCBAs, since cleaning chemistries that support the RMA flux used with through-hole components may not sufficiently clean residue left by no-clean flux used in SMT.

Unquestionably, industries that often have highly specialized quality requirements, combined with legacy products and/or qualification processes that limit the ability to make manufacturability-driven design changes, present contract manufacturing challenges. The best solution is to focus on manufacturability early in the design process and work with supply chain partners who are willing to develop solutions for production issues that can't be designed out of the product. SMT

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Collaboration between OEM and EMS to Combat Head-on-Pillowing Defects, Part 2: WARPAGE ACCEPTANCE PROPOSAL

by Alex Chan, Paul Brown and Richard Coyle, ALCATEL-LUCENT; **Lars Bruno, Anne-Kathrine Knoph,** ERICSSON; **Thilo Sack,** CELESTICA INC.; **David Geiger, David Mendez and Ron Kulterman,** FLEXTRONICS INTERNATIONAL; **Mulugeta Abtew, Iulia Muntele,** SANMINA CORP; **Kirk VanDreel,** PLEXUS CORP.

Abstract

There have been many publications, industry workshops, and symposia that describe process mitigation techniques for minimizing the occurrence of head-on-pillow (HoP) defects during surface mount assembly. These include inspection effectiveness as covered in Part 1 of this two-paper set. This second paper addresses the root cause of the HoP defect—specifically the link between HoP defects and component warpage. Multiple case studies contributed by the participating companies are presented to support the proposal that the current industry warpage standard needs to be revised and to demonstrate that further work is needed by the industry to understand the root cause of this defect better. Based on the data from the case studies, the authors propose revised acceptance criteria that set the maximum warpage at 0.090 mm (3.5 mil) for BGA of 0.8 mm pitch and above.

Introduction

Head-on-pillow (HoP), head-in-pillow (HiP), head-and-pillow (HnP); regardless of what you call it, it is a defect that is growing in prevalence. HoP is particularly problematic because the intimate contact between ball and paste can easily escape current x-ray inspection processes and, in many instances, adequate electrical continuity exists to pass initial electrical testing. Eventual separation of what was never a proper metallurgical bond can lead to late stage manufacturing defects and even early stage field return issues.

Significant effort has been invested in the study of HoP. As a result, the defect mechanism and its contributing factors have been substantially described in the literature[1–3]. There is wide recognition that package warpage is a primary factor in the formation of HoP. In fact,

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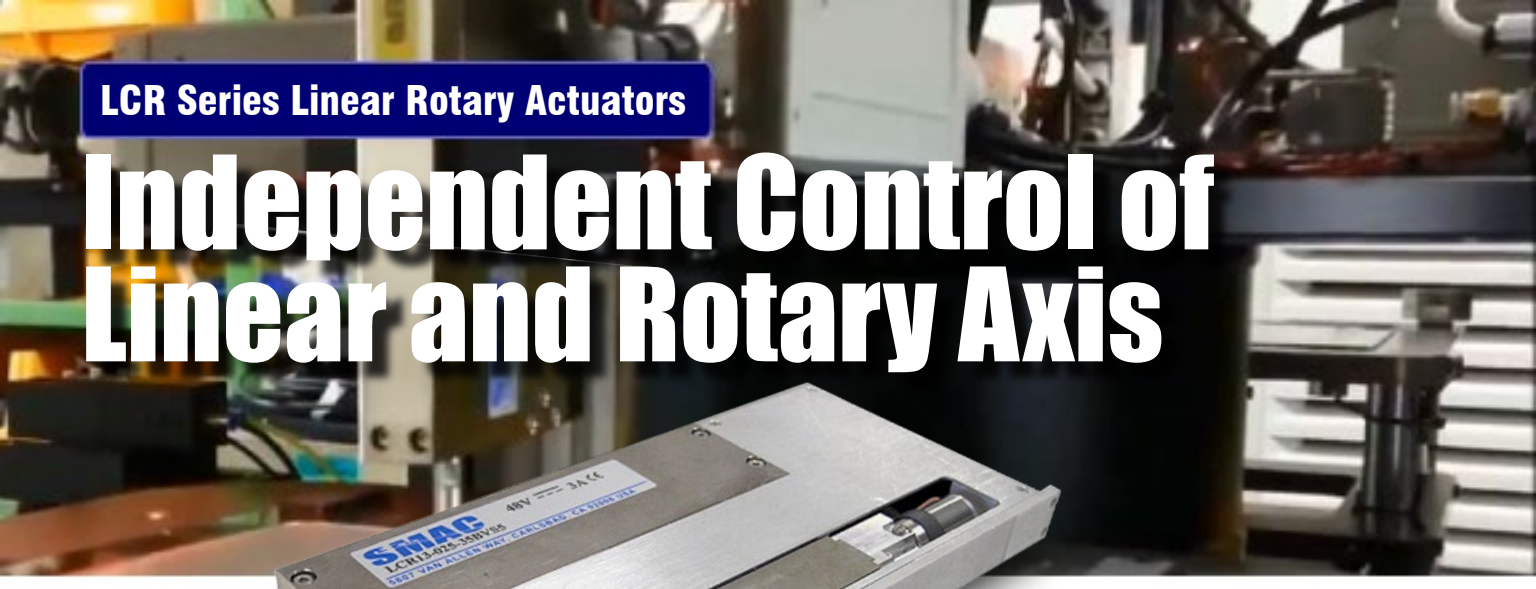

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several industry consortia efforts are currently in progress to help characterize factors influencing package warpage behavior in an attempt to define mitigation measures. These include the iNEMI Package Warpage Qualification Criteria and the HDPUG FCBGA Package Warpage projects.

As discussed in Part 1 of this paper, the authors worked on a number of mitigation practices to minimize HoP defects on product. However, it also sparked interest from the different participating OEM and EMS companies to discuss the need to address the root cause of HoP in the industry. It is the belief of the authors that there are a number of factors that lead to the formation of the HoP defect, but package warpage during reflow is viewed as the most significant contributor.

In this paper, a number of real product examples collected by different participating members will be presented. Current industry specifications governing package warpage will be reviewed and recommendations for revised process warpage criteria for BGA packages with a pitch of 0.8 mm and above will be made.

Head-on-Pillow Description

HoP is "characterized by complete melting of both the solder paste and the BGA solder ball but with insufficient coalescence to produce well-formed solder joint"[2].

Known HoP Mitigation Solutions

It is not the intent of this paper to focus on process mitigation strategies as these have been adequately described in previous papers. However it is worth listing here the four most common process modifications employed for HoP mitigation.

1. Stencil aperture modification is by far the most common method applied by the EMS to mitigate the risk of HoP. A stencil aperture with bigger openings[2] will deliver more paste to targeted areas to help increase the chance of proper soldering in the areas most affected by component warpage. The image shown in Figure 1 is just one of many stencil designs in use in the industry which illustrates progressively larger stencil openings in the 4 corners of the component land.

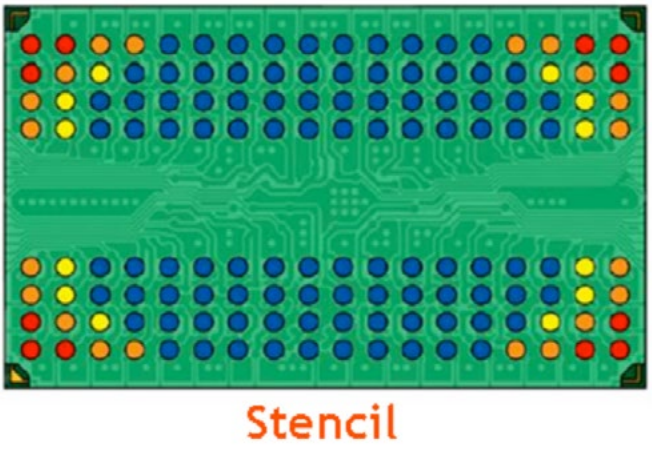

Figure 1: Mitigation through stencil aperture modification.

2. Reflow profile adjustment is another solution used by the EMS. By varying the profile type (soak or ramp), dwell time; atmosphere (air or nitrogen); different assembly houses have found varying degrees of success in decreasing the prevalence of HoP on the assembly.

3. Solder paste type has also been tested in order to understand which solder paste properties can be more effective in mitigating the HoP defect. As shown in Figure 3, multiple types of solder paste can be considered for evaluation.

4. As discussed in Part 1 of this paper, with proper engineering effort, AXI was successful at detecting more than 90% of the HoP defects on the cards used for that study. Further validation tests using products with confirmed HoP defects will lead to greater refinement of such tools thus decreasing the possibility of defects escaping to the field.

HoP Defect Hypothesis in the Process Flow

Mitigation practices will help to minimize the issue but cannot be expected to completely eliminate it. In this paper a hypothesis is put forward by the authors in order to explain the importance of addressing the package warpage as a means to eliminating the HoP defect rather than minimize it. A number of examples collected from OEMs & EMS firms are then used to support revised warpage acceptance criteria.

The hypothesis recognizes that process

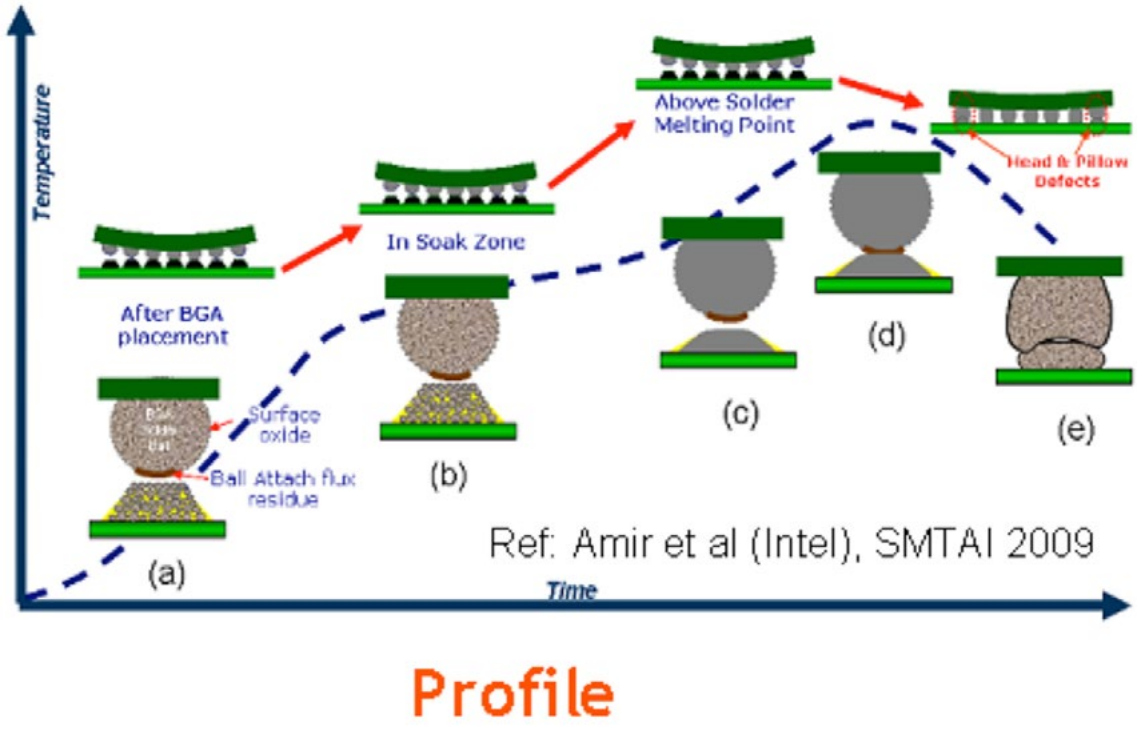

Figure 2: Mitigation through reflow profile adjustment[4].

Phase 2 Ranking	Paste D	Paste C	Paste F	Paste G	Paste I	Paste K
HIP	6	2	4	1	3	5

Solder Paste

Ref: Flextronics

Figure 3: Mitigation through paste type.

mitigation will help to eliminate 70–90% of the HoP defects. Furthermore, in process, X-ray inspection will only detect approximately 90% of the remaining HoP defects on the assembled products. Thus, there is an expectation that a percentage of HoP defects (albeit greatly reduced) will still escape inspection and end up on the final products.

From the authors' perspective, each of these compromised joints is likely to become a customer field failure. As a minimum field failures are both costly and damaging to the reputation of the OEM, at the other extreme, in life sustaining and mission critical applications these failures can be catastrophic. The new acceptance criteria seeks to address the root cause of the issue, allowing the HoP escape rate to further decrease to near zero.

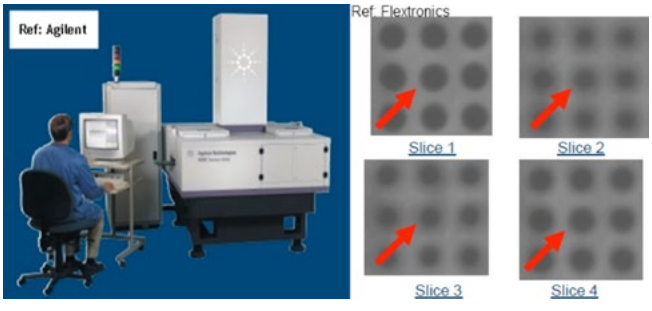

Figure 4: AXI inspection for HoP defect.

Current Specifications

Two industry standard bodies provide requirements for BGA component warpage: Japan Electronics and Information Technology Industries Association (JEITA) and Joint Electron Device Engineering Council (JEDEC). JEITA ED-7306[5] is considered to be the earliest specification the authors could locate and at one point the only standard for dynamic warpage. In 2009, JEDEC released a similar standard Publication 95, SPP-024 Issue A[6] for dynamic warpage requirements.

In both specifications, the warpage require-

WARPAGE ACCEPTANCE PROPOSAL *continues*

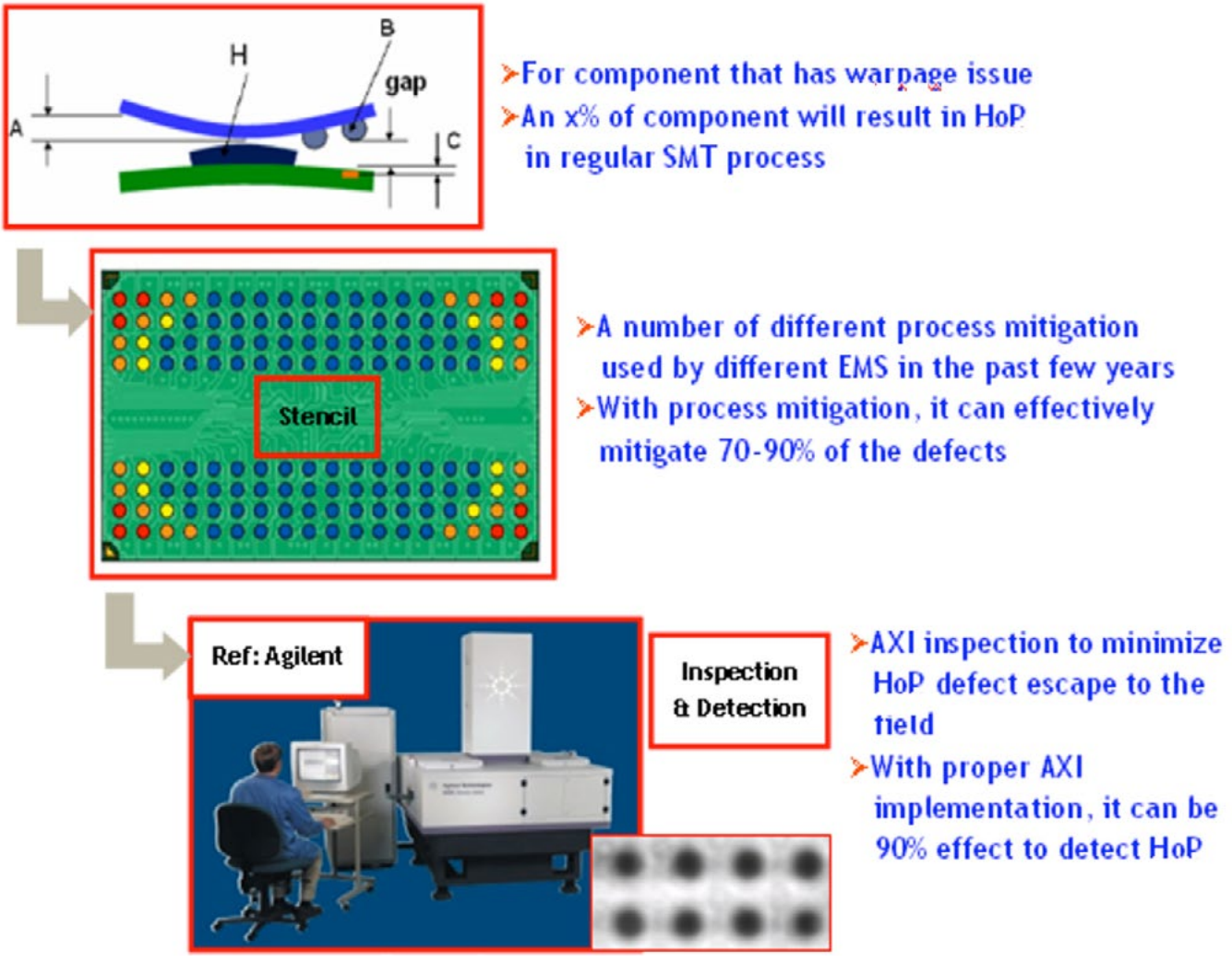

Figure 5: HoP defect escape hypothesis, illustrated.

ments were measured over the entire temperature range of a reflow profile, including room temperature. For the discussion of this paper and to the interests of the authors, the dynamic warpage zone corresponding to the reflow profile is defined as the zone between 150°C to the maximum temperature of a profile (i.e., 260°C for a small BGA and 245°C for a large BGA).

In both standards, positive warpage is described as convex whereas negative warpage is described as concave as shown in Figure 6.

Figure 7 and 8 show the current acceptable warpage by ball diameter, height and package pitch as a reference for the discussion of this paper. Again, the discussion and proposed acceptance is limited to BGA components with a pitch of 0.8 mm and above.

Figure 6: Description of the warpage shapes.

The JEITA and JEDEC specifications are structured differently and have a maximum allowable warpage based on pitch, size, etc. Using the most common 1 mm pitch BGA as a comparison, the JEITA standard allows up to 0.22 mm (8.6 mil) warpage regardless of the size of

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WARPAGE ACCEPTANCE PROPOSAL *continues*

Maximum permissible package warpages for BGA and FBGA

Unit: mm

Solder ball pitch	0.4	0.5	0.65	0.8		1.0	1.27
Condition of ball height	0.20	0.25	0.33	0.35	0.40	0.50	0.60
Maximum permissible package warpage (Absolute value)	0.10	0.11	0.14	0.17	0.17	0.22	0.25

Figure 7: Warpage table from JEITA ED-7306[5].

1 — Flatness requirements (mm) during reflow for components less than or equal to 15mm on any side, applies to temperature range from flux activation to reflow peak. Follows JEITA ED-7306.

e - Ball Pitch (mm)	b - Ball Diameter(mm)[III]												
	0.20	0.25	0.30	0.35	0.40	0.45	0.50	0.55	0.60	0.65	0.80	0.90	1.00
0.40	±0.10	±0.10	±0.10										
0.50		±0.10	±0.10	±0.10									
0.65		±0.10	±0.10	±0.10	±0.11	±0.12							
0.80		±0.10	±0.10	±0.10	±0.11	±0.12	±0.13	±0.14					
1.00					±0.11	±0.12	±0.13	±0.14	±0.17	±0.17			
1.27									±0.17	±0.17	±0.21	±0.23	±0.25
1.50									±0.17	±0.17	±0.21	±0.23	±0.25

2 — Flatness requirements (mm) during reflow for components greater than 15mm on any side, applies to temperature range from flux activation to reflow peak.

e - Ball Pitch (mm)	b - Ball Diameter (mm)[IV]										
	0.20	0.25	0.30	0.35	0.40	0.45	0.50	0.55	0.60	0.80	0.90
0.40	-0.09 +0.12	-0.10 +0.15	-0.12 +0.17								
0.50		-0.10 +0.15	-0.12 +0.17	-0.13 +0.20							
0.65		-0.10 +0.15	-0.12 +0.17	-0.13 +0.20	-0.14 +0.22	-0.14 +0.23					
0.80		-0.10 +0.15	-0.12 +0.17	-0.13 +0.20	-0.14 +0.22	-0.14 +0.23	-0.14 +0.23	-0.14 +0.23			
1.00					-0.14 +0.22	-0.14 +0.23	-0.14 +0.23	-0.14 +0.23	-0.14 +0.23		
1.27									-0.14 +0.23	-0.14 +0.23	-0.14 +0.23
1.50									-0.14 +0.23	-0.14 +0.23	-0.14 +0.23

Figure 8: Warpage table from JEDEC Publication 95, SPP-024 Issue A[6].

the BGA. On the other hand the JEDEC specification allows up to 0.23 mm (9 mil) warpage for large BGAs and 0.17 mm (6.7 mil) warpage for small BGAs.

The authors submit that these warpage specifications are too generous and will allow substantial opportunity for conditions of poor contact between ball and paste during reflow; resulting in HoP defects.

Case Studies

Six different case studies collected from participating companies will be discussed in this paper. Each of these cases is a real life product example of HoP defects found either in production or as a result of field returns. This paper will review the corresponding warpage analysis of the BGAs and compare these to the specification.

The following table displays the coplanarity values for each measurement. The coplanarity value is determined by taking the difference between the overall maximum and overall minimum of each data matrix.

Sample	Temperature (°C)	Min	Max	Coplanarity (mils)
	26 Initial	-1.3	2.4	3.6
	150 Heating	-2.1	1.9	-4
	180 Heating	-2.8	2.4	-5.1
	208 Maximum	-3.1	2.8	-5.9
	180 Cooling	-2.7	2.5	-5.2
	150 Cooling	-2.1	2	-4
	100 Cooling	-1.9	1.5	-3.4
FBGA 144 I/O	26 Final	-1.1	2.2	3.3
	26 Initial	-1.7	3	4.7
	150 Heating	-2.3	1.6	-3.9
	180 Heating	-2.4	2.1	-4.5
	208 Maximum	-2.7	2.5	-5.2
	180 Cooling	-2.3	2.1	-4.4
	150 Cooling	-2.2	1.6	-3.7
	100 Cooling	-1	1.2	-2.2
	26 Final	-1.5	2.8	4.3

Table 1: Results of the warpage measurement of two BGA from case 1.

Case 1

Package description:

- FBGA
- 144I/O
- 11 x 18.5 mm
- 0.8 x 1.0 mm pitch
- SnPb
- 0.55 mm ball diameter

Table 1 shows the results of units that were sent to a lab for analysis. According to the only standard at the time (JEITA), this parts maximum warpage of 0.15 mm (5.9 mil) is well within specification. However, a number of users reported the package as being prone to HoP defects when assembling this part with typical SMT process.

The component warpage is concave at reflow, and as a result most HoP was found in the corner joints. The graph in Figure 9 shows the actual measurements of the part at its maximum warpage. (Please note that the part was measured upside-down with the solder balls removed. Therefore to aid with visualization the graph was rotated 180 degrees to show the component warpage as it would be on the board during the SMT reflow process.)

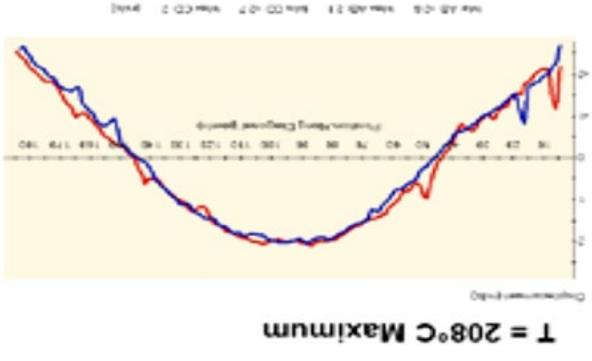

Figure 9: 2D plot of the warpage measurement of the BGA from case 1 (Shown upside-down for clarity).

Case 2

Package description:

- PBGA
- 484I/O
- 19 x 19 mm
- 0.8 mm pitch
- Pb-free

This case study came from a complex telecom product that exhibited variable production yields as reported in Coyle's paper[2]. This device was reported to have a 0.104 mm (4.1 mils) negative warpage during reflow. However the paper reported a number of confirmed HoP defects, located mainly at the corners and outer rows of the BGA (consistent with the negative warpage). According to the JEITA and JEDEC specifications, this device is completely within the acceptance limit of +/-0.17 mm or -0.14/+0.23 mm respectively. The example shows that the BGA is well within both of the specifications yet HoP defects were experienced in production.

Case 3

Package description:

- FBGA
- 154I/O
- 17 x 17 mm
- 0.8 mm pitch
- SnPb
- 0.5 mm ball diameter

Summary of Shadow Moiré results for 4 different 484 I/O PBGA components.

Device Number	Initial Warpage (µm microns)	Peak Warpage (µm microns)	Total Variation (µm microns)
1	91.44 @ (22°C)	68.58 @ (230°C)	160.02
2	104.14 @ (22°C)	83.82 @ (180°C)	187.96
3	99.06 @ (22°C)	58.42 @ (210°C)	157.48
4	96.52 @ (22°C)	104.14 @ (190°C)	200.66

4.1mil

Figure 10: Results of the warpage measurement of four BGA from case 2[2].

Case number 3 was reported by the participating company as a device that caused notable HoP issues in the factory. The device was reported to have 0.119 mm (4.7 mils) of negative warpage at reflow. Figure 11 shows the 2D and 3D plot of the warpage measurement of the BGA.

Here too we see a case where a package that is well within the JEDEC (-0.14/+0.23 mm) and JEITA (-/+0.17 mm) specifications, results in HoP defects.

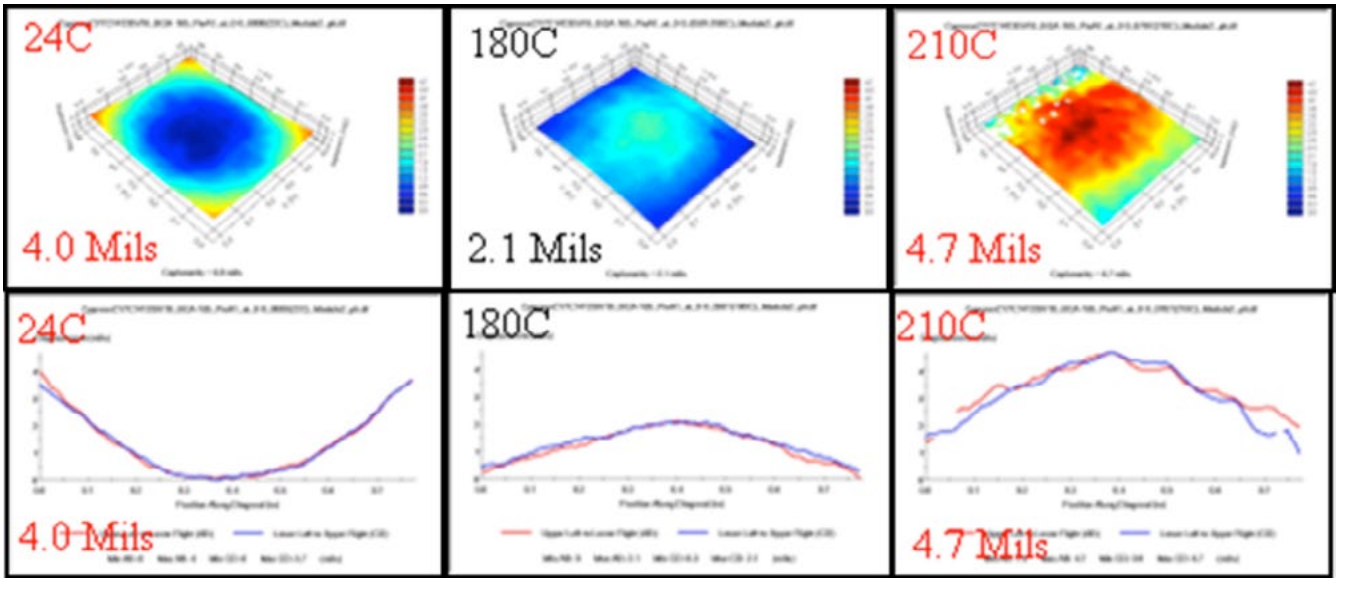

Figure 11: 2D and 3D plot of the warpage measurement of the BGA from case 3.

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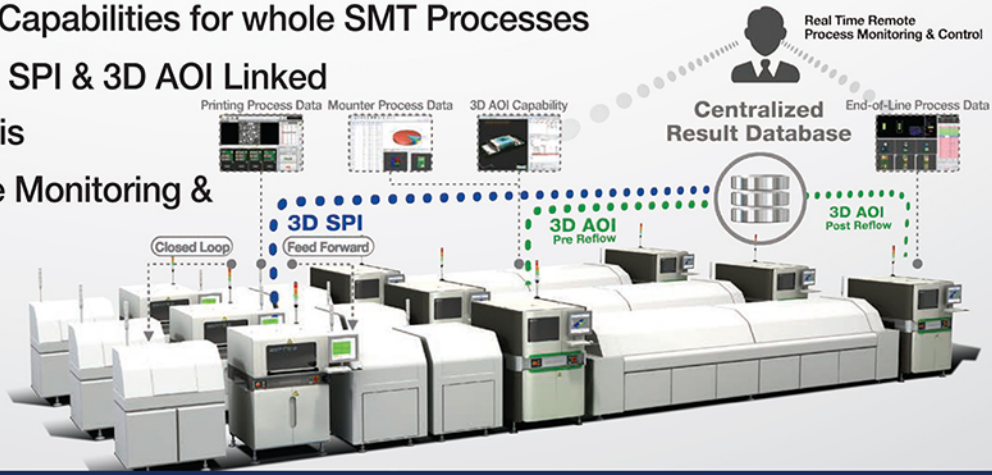

For More Information
Contact Jason Perry

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Case 4

Package description:

- PBGA
- 578I/O
- 35 x 35 mm
- 1 mm pitch
- SnPb
- 0.6 mm ball diameter

Case 4 is considered a medium size BGA. It also exhibited the highest degree of warpage of the cases presented in this paper. The device was reported to have 0.180 mm (7.1 mils) of negative warpage during reflow, resulting in substantial HoP defects during assembly. Figure 12 shows the 2D and 3D warpage measurement of the BGA. Interestingly, this part would fail the more recent JEDEC specification, (maximum -0.14 mm allowable warpage), but would pass the JEITA specification of 0.22 mm maximum allowable warpage.

Case 5

Package description

- FCBGA
- 1932I/O
- 45 x 45 mm
- 1 mm pitch
- Pb-free
- 0.63 mm ball diameter

While most of the cases presented in this paper are from production and factory HoP issues, case 5 is based on a specific test performed in collaboration with a supplier on a large BGA. This test confirmed that a BGA, with 0.110 mm (4.3 mils) of negative warpage at reflow will gener-

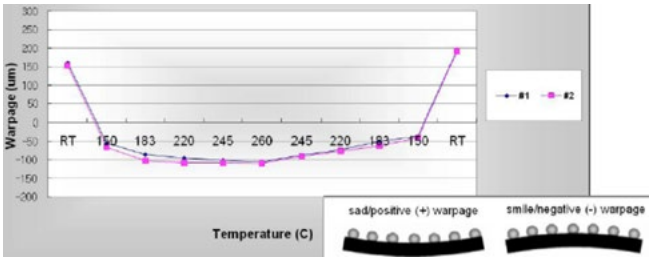

Figure 13: Warpage measurement of the BGA from case 5 before the package improvement.

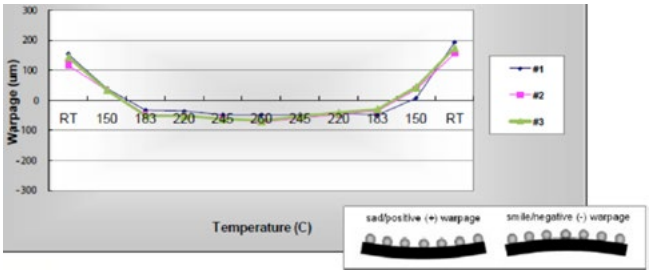

Figure 14: Warpage measurement of the BGA from case 5 after the package improvement.

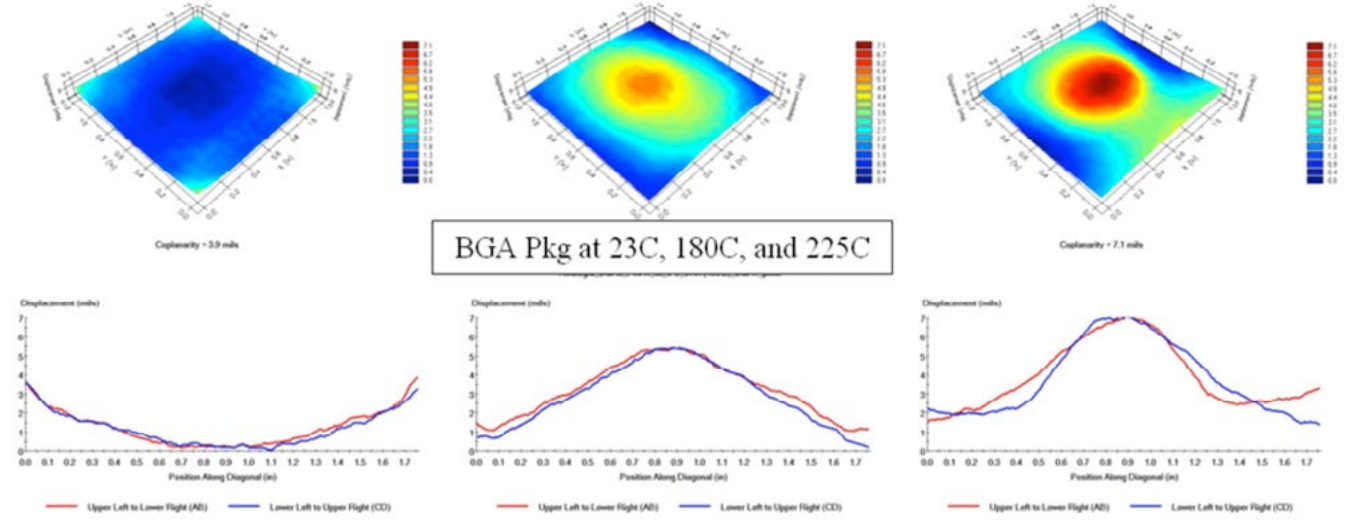

Figure 12: 2D and 3D plot of the warpage measurement of the BGA from case 4.

ate HoP defect in the assembly. Warpage measurement of the BGA across the entire temperature is shown in Figure 13. According to both the JEITA (-/+0.22 mm) and JEDEC (-0.14/+0.23 mm, note that the specification does not address a 0.63 mm ball) specifications, this amount of warpage would be completely within the acceptable range. Although the study did not correlate the percentage of improvement in yield, the supplier confirmed that improvements to that same package (bringing it within the propose acceptance criteria) would minimize and possibly eliminate the HoP defects.

Case 6

Package description:

- FBGA
- 165I/O
- 13 x 15 mm
- 1.0 mm pitch
- SnPb and Pb-free
- 0.5 mm ball diameter

Case 6 is considered a key example supporting the propose acceptance criteria. Two of the same type of BGA are used on two different products from one of the participate members. For the purposes of this paper, they will be referred to as MPN1 and MPN2. MPN1 had a different die size then MPN2. MPN1 also had the variant of MPN1A for SnPb and MPN1B for Pb-Free assembly, whereas the MPN2 used Pb-Free assembly only. Both of these BGAs caused notable incidence of HoP defects between the OEM and the EMS sites that assembled these devices. The first findings showed that MPN2 had a much higher incident of HoP defects then MPN1B (Pb-free assembly only). MPN1A and MPN1B showed HoP defects in both SnPb and Pb-Free assembly. Furthermore, MPN1 yielded HoP defects in the assembly results of five different assembly locations.

A large number of Shadow Moire analyses were performed on MPN1 and MPN2 and the data was compiled and shown in Table 2. These observation help support the propose acceptance criteria. They also confirm that the higher the degree of warpage, the more likely the part is to generate HoP defects.

For this particular part size and BGA ball diameter, the JEDEC specification allows 0.13 mm (5.1 mil) of warpage which is much tighter then JEITA specification which allows 0.22 mm (8.7 mil) warpage. Regardless, the results of this work indicate that warpage values of as little as 0.093 mm (3.7 mil) resulted in HoP defects; far below the maximum allowable warpage indicated in the current specifications.

MPN1

Temperature	25	150	180	200	220	250	220	200	180	150	25
Ave Warpage (µm)	102	-39	-54	-59	-60	-54	-43	-38	-36	-37	93
Standard Dev (µm)	12.5	12.6	11.7	11.3	8.8	9.7	9.6	9.4	10.9	11.8	10.1
With 3 StdDev (µm)		-77.0	-88.8	-93.3	-86.3	-82.8	-72.1	-66.4	-69.1	-72.7	
With 3 StdDev (mil)		-3.0	-3.5	-3.7	-3.4	-3.3	-2.8	-2.6	-2.7	-2.9	

MPN2

Temperature	25	150	180	200	220	250	220	200	180	150	25
Ave Warpage (µm)	94	-33	-62	-80	-92	-92	-71	-59	-47	-33	89
Standard Dev (µm)	13.7	12.5	9.2	5.9	7.6	9.1	8.9	8.2	8.9	8.0	9.3
With 3 StdDev (µm)		-70.8	-90.1	-98.2	-115.0	-118.7	-97.8	-83.5	-73.6	-56.6	
With 3 StdDev (mil)		-2.8	-3.5	-3.9	-4.5	-4.7	-3.8	-3.3	-2.9	-2.2	

Table 2: Warpage measurement data of MPN1 and MPN2 from case 6.

PCB Warpage Data

In an effort to make sure the PCB is not the root cause of the defect, three of the cases were able to collect corresponding PCB warpage data.

Figure 15 shows the PCB warpage data corresponding to case study 4. In the analysis of the PCB and the specific location of the BGA, it was found that the warpage was 0.04 mm (1.6 mil) at reflow. Upon review both the participating member and a subject matter expert concluded that the PCB warpage contribution was negligible and by extension not the primary source of the defect.

Warpage data of the PCB for case 5 was collected in a numerical format rather than graphical format like that of the previous example. Table 3 is an example of measurements of one of the six test sites on the same PCB. Overall, the six sites measured, the maximum warpage recorded between 150°C and peak reflow was 0.041 mm (1.6 mils). Here, too, the authors agreed that the PCB was not the root cause of the HoP defect observed in this case.

Finally, for case 6, two of the PCBs were sent for Shadow Moire analysis. Two sites on each PCB were measured and found to have maxi-

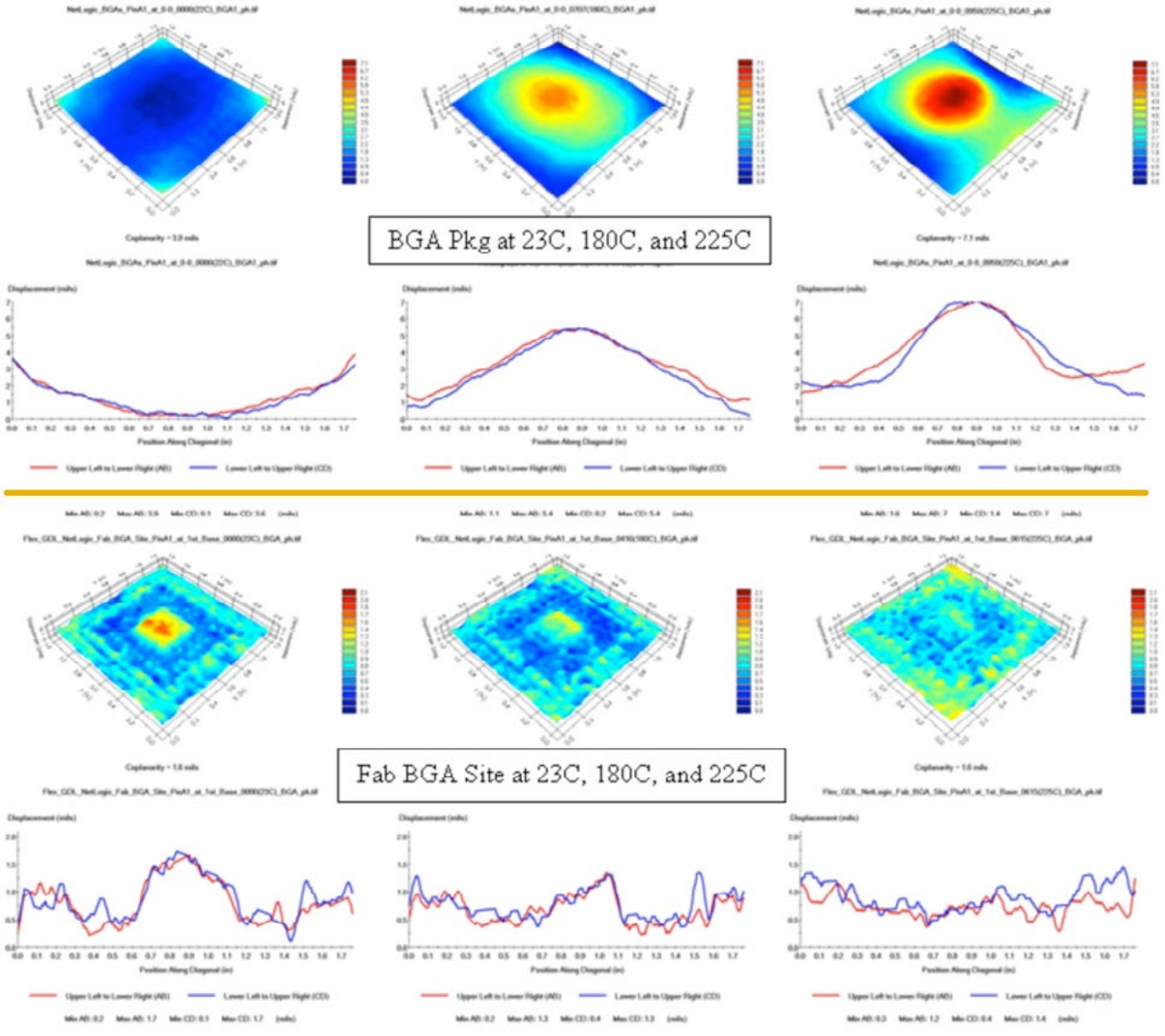

Figure 15: Warpage measurement result of the PCB site for case study 4.

mum warpage at temperature of 0.025 mm (1 mil). In comparison, the BGA had more than 0.090 mm (3.5 mil) of warpage. The authors considered the PCB to be very flat and stable during reflow and unlikely to be a main contributor of HoP defects .

Observations

The following are the key observations stemming from these case studies:

1. All of the cases meet one or both industry specifications governing maximum acceptable warpage.
2. Each of these cases studies resulted in HoP defects on the assembly.
3. The onset of HoP occurs at component warpage values in the range of 0.075–0.090 mm (3-4 mil) during reflow as suggested by these cases.
4. The higher the warpage is for the same BGA package, the higher the incidence of HoP defects.
5. For BGAs of 0.8 mm pitch and above, the case studies did not show a strong correlation between degree of warpage and BGA size.
6. The case studies that have supporting PCB data suggested that the PCB warpage is not a key contributor to the HoP defect.

Solder Paste Volume Theory

A simple theory of solder paste volume is used together with the examples provided to support the propose acceptance criteria. Most solder pastes in use contain roughly 50% flux by volume. Therefore with a 0.150 mm (6 mil) stencil, once the flux content is burned off, the theoretical height of the remaining solder is 0.075 mm (3 mil). At liquidus temperatures, the solder domes up slightly similar to stage (d) described in Figure 2. If the component has pulled away from the solder paste before liquidus, then the oxides and contaminates on the solder ball cannot be reduced by the flux. This theory suggests that if the solder paste does not remain in contact with the solder ball at liquidus, poor or no contact will result, thereby generating HoP defects.

Temperature (°C)	Coplanarity (µm)
25	21
150	32
183	40
220	28
245	30
260	-33
245	-32
220	-28
183	-26
150	-27
25	22

Table 3: Warpage measurement of PCB for case study 5.

Temp	Fab1 SiteD	Fab 1 SiteE
30C	+0.8 mils	+0.7 mils
180C	+0.9 mils	+0.8 mils
200C	+0.7 mils	+0.8 mils
225C	+0.8 mils	+0.8 mils
200C	+0.8 mils	+0.8 mils
180C	+0.9 mils	+0.8 mils
30C	+0.9 mils	+0.8 mils
	Fab2 SiteD	Fab2 SiteE
30C	+1.1 mils	+1.1 mils
180C:	+1.0 mils	+1.1 mils
200C:	+1.1 mils	+1.0 mils
225C	+1.0 mils	+0.9 mils
200C	+1.3 mils	+1.2 mils
180C	+1.0 mils	+1.0 mils
30C	+1.0 mils	+1.3 mils

Table 4: Warpage measurement result of the PCB site for case study 6.

Proposed Warpage Acceptance Criteria and Differences with Existing Industry Specifications

It is the view of the collaborating companies that the current JEDEC Publication 95, SPP-024 Issue A and JEITA ED-7306 warpage specifications are too generous to prevent the occurrence of HoP defects in SMT assembly. Consequently, the authors are proposing the following revisions to existing specifications:

1. An absolute maximum warpage of 0.09 mm (3.5 mil) during the reflow stage of soldering independent of BGA body size and I/O count. The reflow stage is defined as the entire period where the BGA component temperature exceeds 150°C. For example, this could be 150°C to 245°C back to 150°C for larger BGAs and 150°C to 260°C and back to 150°C for smaller BGAs.
2. The revised acceptance criteria would only apply to BGAs with a 0.8 mm pitch or greater.
3. The proposed acceptance criteria apply only to applications that use 0.125 mm (5 mil) or 0.150 mm (6 mil) stencil thickness.
4. Fine pitch BGAs (equal to or less than 0.65 mm pitch) with smaller solder spheres are likely to require a lower value of maximum warpage. As a future consideration, the finer pitch components must be addressed as more data warpage emerges.

Discussion and Suggestions for Follow-on Work

This collaboration between OEMs and EMSs has confirmed that a large number of users in the industry are confronted with the HoP defects in product manufacturing. It is the view of the authors that component warpage plays a significant role in the formation of the HoP defect. An acceptance criteria for BGAs with 0.8 mm pitch and above is proposed that is more rigorous with lower warpage limits than the current JEDEC and JEITA industry specifications addressing component warpage. The proposed acceptance criteria were based primarily on end user application data and experience rather than extensive DOE-like studies. Although it is the view of the authors that the proposed acceptance criteria are sound and will further minimize HoP defects, a lot of work is needed within the industry to reach an agreement between component suppliers and the users (OEM/EMS). The following is a list of suggested follow-on work:

1. Standardized test methods are needed for measuring warpage and correlating the warpage measurements to manufacturing process yields.
2. Warpage characterization should be performed on a variety of components having different levels of warpage in order to better understand the onset of HoP as it relates to component warpage. This will require a significant, coordinated effort between industry standards bodies, packaging houses, device suppliers, end users, and consortia A wide range of component sizes, pitches and degree of warpage are needed for further testing in order to better understand how the revised specification works as a function of the these parameters.
3. This paper presents case studies using 0.125–0.150 mm (5–6 mil) stencil on BGAs of 0.8 mm pitch and above. A better understanding is required for the same component type

Pitch	0.8mm	0.8mm	1.0mm
Ball Dia/(or height)	0.50mm/0.35mm(h)	0.55mm/0.40mm(h)	0.60mm/0.50mm(h)
JEITA	-0.170 to +0.170mm	-0.170 to +0.170mm	-0.220 to +0.220mm
JEDEC <=15mm	-0.130 to +0.130mm	-0.140 to +0.140mm	-0.170 to +0.170mm
JEDEC >15mm	-0.140 to +0.230mm	-0.140 to +0.230mm	-0.140 to +0.230mm
OEM/EMS Proposal	-0.090 to +0.090mm	-0.090 to +0.090mm	-0.090 to +0.090mm

Table 5: Comparison of the OEM/EMS proposed specification for 0.8 and 1.0 mm pitch BGA to the JEITA and JEDEC specification.

and pitches when the stencil thickness is reduced.

4. More study is required to understand fine pitch BGAs such as 0.65 mm pitch and below, in applications that use 3–4 mil stencil thicknesses. It is reasonable to expect an even lower warpage acceptance criteria may be required in applications with finer pitches and using thinner stencils. **SMT**

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This paper originally appeared in the SMTA Journal in July 2013. To read Part 1 of this article, click here.

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Neutrons Find "Missing" Magnetism of Plutonium

Groundbreaking work at two Department of Energy national laboratories has confirmed plutonium's magnetism, which scientists have long theorized but have never been able to experimentally observe. The advances that enabled the discovery hold great promise for materials, energy and computing applications.

After seven decades, this scientific mystery on plutonium's "missing" magnetism has been resolved. Using neutron scattering, researchers from the Department of Energy's Los Alamos and Oak Ridge (ORNL) national laboratories have made the first direct measurements of a unique characteristic of plutonium's fluctuating magnetism. In a recent paper in the journal Science Advances, Marc Janoschek, from Los Alamos, explains that plutonium is not devoid of magnetism, but in fact its magnetism is just in a constant state of flux, making it nearly impossible to detect.

Using neutron measurements made on the ARCS instrument at ORNL's Spallation Neutron Source, a DOE Office of Science User Facility, Janoschek and his team determined that the fluctuations have different numbers of electrons in plutonium's outer valence shell—an observation that also explains abnormal changes in plutonium's volume in its different phases.

"War on Failure" in the August Issue of *The PCB Magazine*

by Stephen Las Marias
I-CONNECT007

This month, our three magazines here at I-Connect007—*The PCB Magazine, The PCB Design Magazine,* and *SMT Magazine*—are all focused on the challenge around quality and process control. We surveyed companies involved in design, fabrication, and assembly, as well as OEMs and suppliers. Their major issues boiled down to four: poor process control, poor training of employees around quality, an inability to quickly identify where and how waste is being created, and poor technical support from suppliers (Table 1).

David Dibble of New Agreements Inc. has written "War on Failure," an article that aims to provide answers to these issues. He notes that while the quality programs of the past have brought us to this point in the evolution of our businesses, we clearly need more. In the war on failure, Dibble points out that we must move beyond traditional thinking and problem solving techniques to something new.

Quality Programs are not Working

After more than 30 years of familiarity with quality programs that morphed into TQM and on to Six Sigma, Lean, Lean Sigma and others, one thing can be said with some conviction: Most quality programs implemented over the past three to four decades are underperforming or outright failing in Western culture companies. Even where they have been somewhat successful, lack of sustainability is rampant.

In his article, Dibble also writes about the four primary reasons why most quality programs are underperforming: programs mentality; a lack of user-friendly tools; the absence of paradigm shifts; and leaders who don't grow.

Dibble explains that the war on failure is really a war on poor systems and non-systems-based thinking of leadership and management. Decades of data show us that more than 90% of the problems we experience in the workplace are a function of the systems in which people work, not the efforts of people. Non-systems-thinking leaders and managers tend to focus on people as the source of problems. It is also a war on leaders and managers who don't value people or don't know how to set up their people to be most successful in their jobs. Because without knowledge of systems and systems improvement, how can any leader or manager know how to set up his or her people for success, quickly and sustainably solve problems, or manage anything?

Non-systems-based leaders and managers do their best, but their best is far from optimum. It doesn't have to be that way, says Dibble. There is a whole new way of leading and managing, a whole new way of being in the workplace that wins the war on failure through quality systems and tools, systems thinking and a willingness to grow beyond more-better-different and the deadly status quo.

To read David Dibble's article, check out the August 2015 issue of *The PCB Magazine*. **SMT**

How to have better process control?		45.9%
How to train employees about quality?		39.8%
How to quickly identify where and how the waste is being produced?		36.7%
How to improve supplier technical support?		30.6%

Table 1: Based on our survey, the above are the key challenges when it comes to quality and process control.

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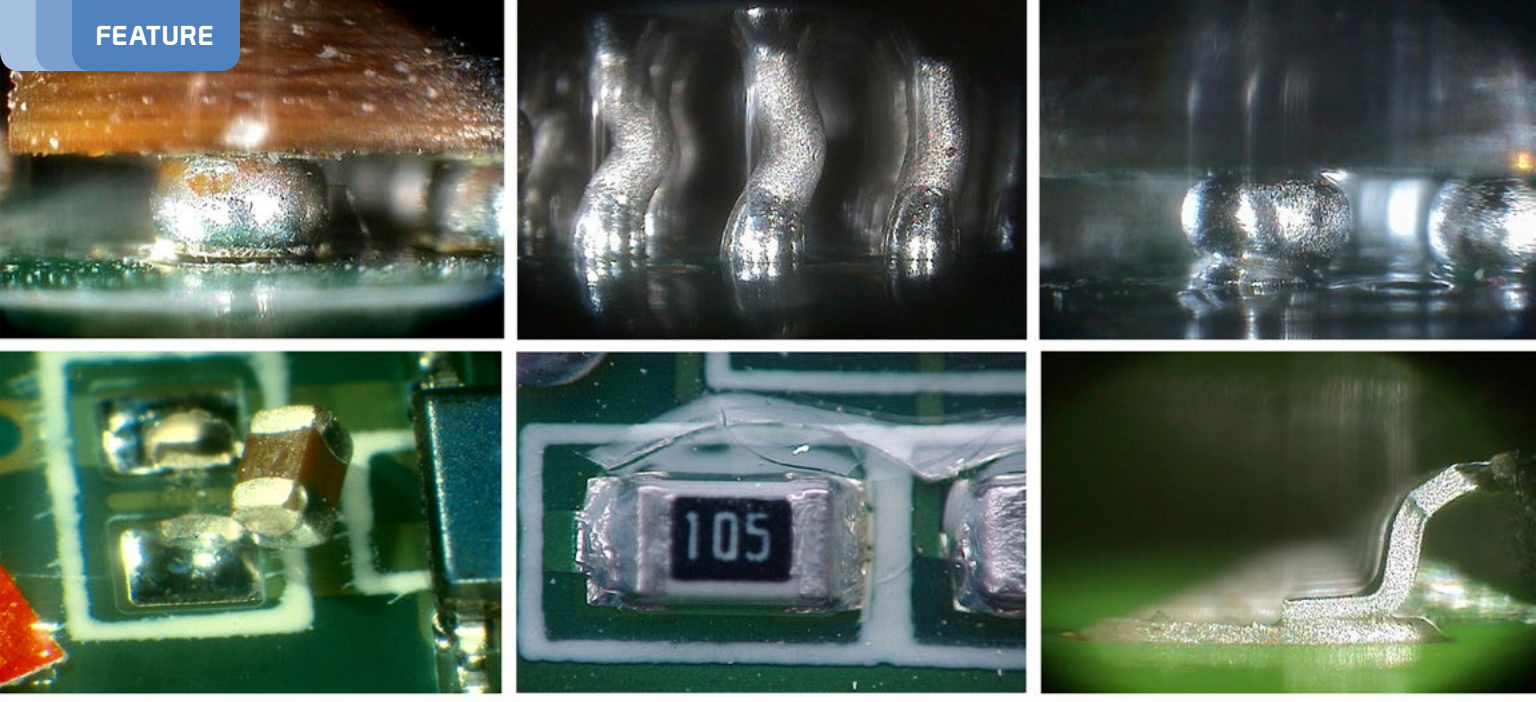

CASE STUDY: DETECTING PROCESS DEFECTS

by Bob Willis

Figure 1 (above): Typical failures of boards and solder joints.

Over the last 30 years I have seen process problems in soldering, PCB manufacture, component failures and investigating product failures worldwide. In many cases, the same process problems or failure modes just go round and round and will return if the true cause of failure is not detected. The causes can be highly complex or very simple. The examples in this article show typical failures of boards and solder joints, the solutions for which are all online if you care to search. Some people say that when we went to lead-free, all the problems changed; actually, many remained the same and looked different, but now there are new ones to solve.

The following resources provided by National Physical Laboratory (NPL) and IPC may help you solve your process problems in the coming years. In the second part of this article, I will illustrate some process problems and their root causes. First let's look at the Defect Database Live and then our "Defect of the Month Video" from IPC.

Defect Database Live

The National Physical Laboratory has created an Industry Defects Database that allows engineers to search through a range of defects covering components, printed circuit boards and assembly problems. The aim is to add more defects and via submissions from the industry each month. The defects database allows engineers to submit defects online with full details and solutions to current problems or requests for advice and possible solutions to the process issues or failures (Figure 2).

The database is unique in the industry as there is no other managed resource of its type with the added scope of having defects added via requests for defect examples from the industry.

IPC Defect of the Month

I was invited by IPC to produce a Defect of the Month video clip, to be featured on their

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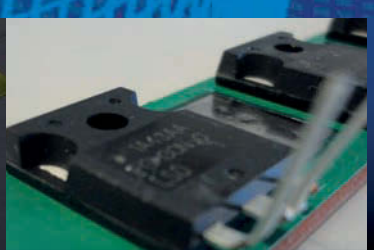

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CASE STUDY: DETECTING PROCESS DEFECTS *continues*

Figure 2: A sample screenshot from the defects database search screen (left), search result (center), and close up of the defect (right).

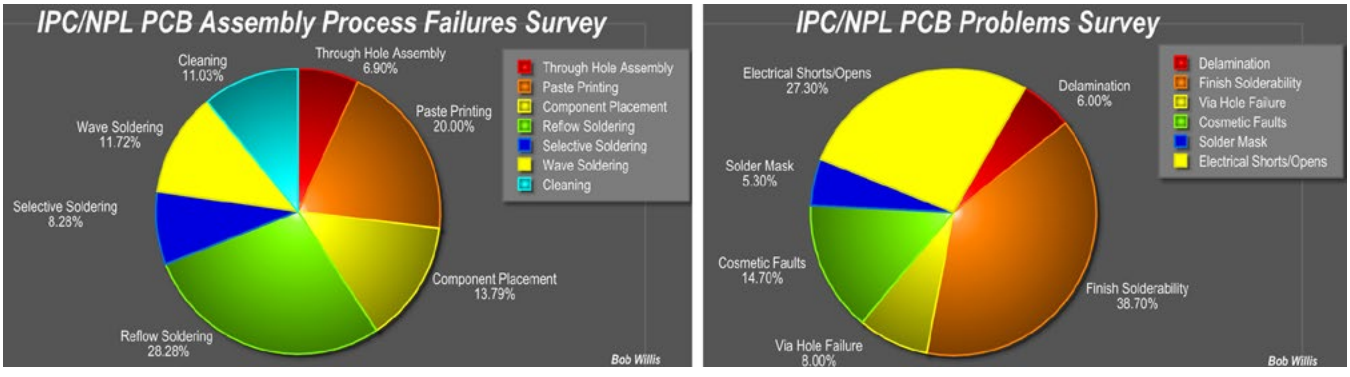

Figure 3. What engineers consider the most common problems or process issues with PCBs and assembly.

website. Each month, we focus on a different defect type and provide photographic examples or videos showing the defects happening in real time. You can visit the IPC website or my YouTube channel to see many of the 40 clips produced showing solder balling, dendrite formation, popcorning, PCB delamination and head-in-pillow failures. There are also some technical book review clips included that may be a useful reference source.

Selected Process Defects from the Industry

Now let's look at some of the most common process issues faced in the industry and some typical examples. However, it's worth looking at what actual industry experiences. The following three graphs show the results of short online surveys from engineers attending online webinars regarding the most common problems or process issues with PCBs and assembly (Figure 3).

PCB Delamination

Delamination is a blister, or air gap, formed when water vapour forms and expands during heating, not like a blister on your skin which is filled with fluid. Delamination may occur when moisture in the board expands during soldering or rework. With the higher temperatures of lead-free there is more energy placed on the materials. When and if moisture accumulates in specific areas of the board more energy is focused in those particular areas. Figure 4b shows a lack of proper adhesion of the epoxy to the surface of the inner layer which may be related to the copper surface preparation, the prepreg or the press cycle. Cutting the surface of the blister can often tell you more than a microsection and you don't need a lab. A full paper on the work we have done at NPL on PCB and moisture content is available from the Defect Database.

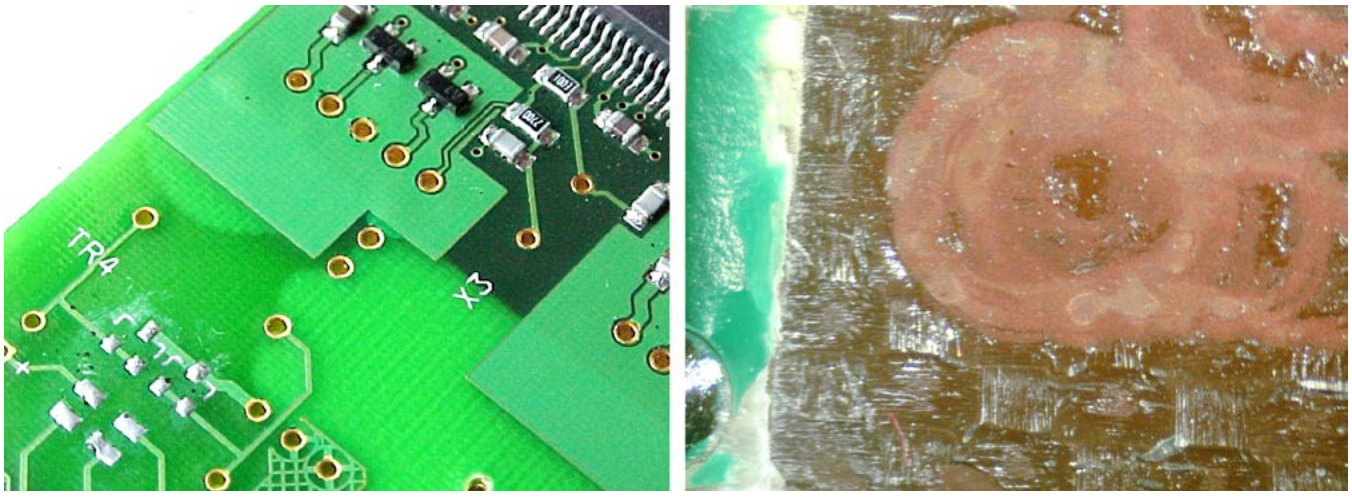

Figure 4: Example of delamination on the surface of a board (left), and one after cutting the surface of the laminate to show the copper inner layer and epoxy and glass bundles (right).

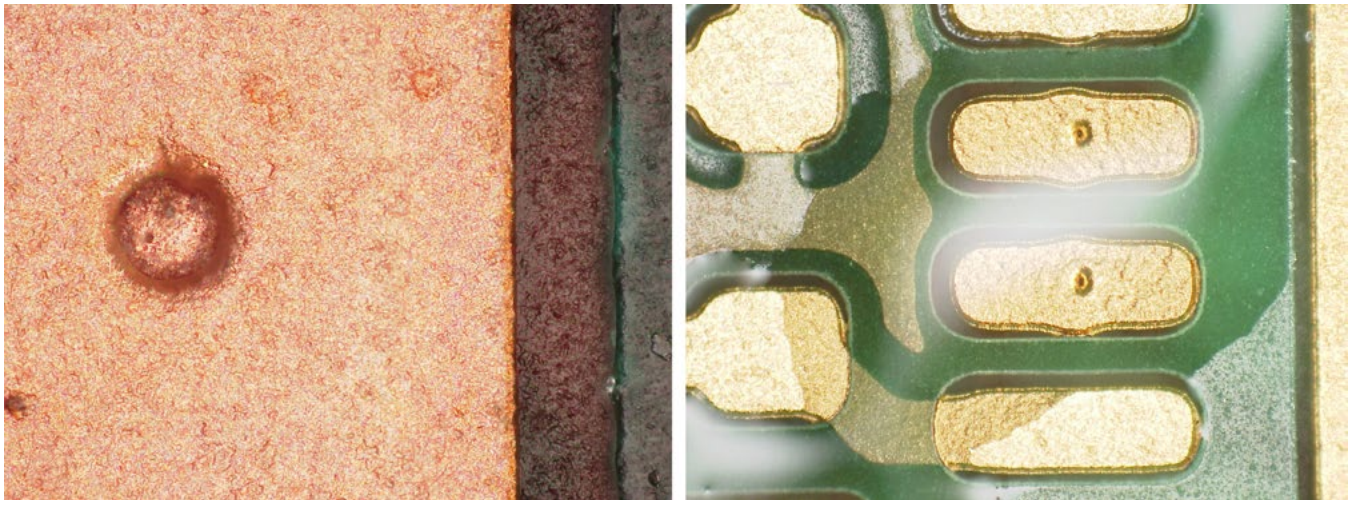

Figure 5: The sample on the left has oil in the hole, and the sample on the right is shown after testing prior to cleaning.

Outgassing from Via-in-Pad

Blind via holes can outgas just like plated through-holes. It's not always the paste volatile or air trapped in the via by the paste printing action. Testing vias prior to microsectioning allows you to assess the degree of outgassing and the copper plating thickness. The sample on the left has oil in the hole and the sample on the right is shown after testing prior to cleaning. A video of outgassing tests and methods of testing is available on the IPC video channel.

Chip Resistor Failure Sulphur

Chip resistors were failing in products in service. The silver layer between the resistive element and the termination was being corroded in automotive and medical applications. This type of defect has been investigated on a number of occasions and due to sulphur present in the environment where the products were in operation.

The same deposits can be seen on chip capacitors where the silver is exposed but due to the constructions will not lead to open circuit connections.

CASE STUDY: DETECTING PROCESS DEFECTS *continues*

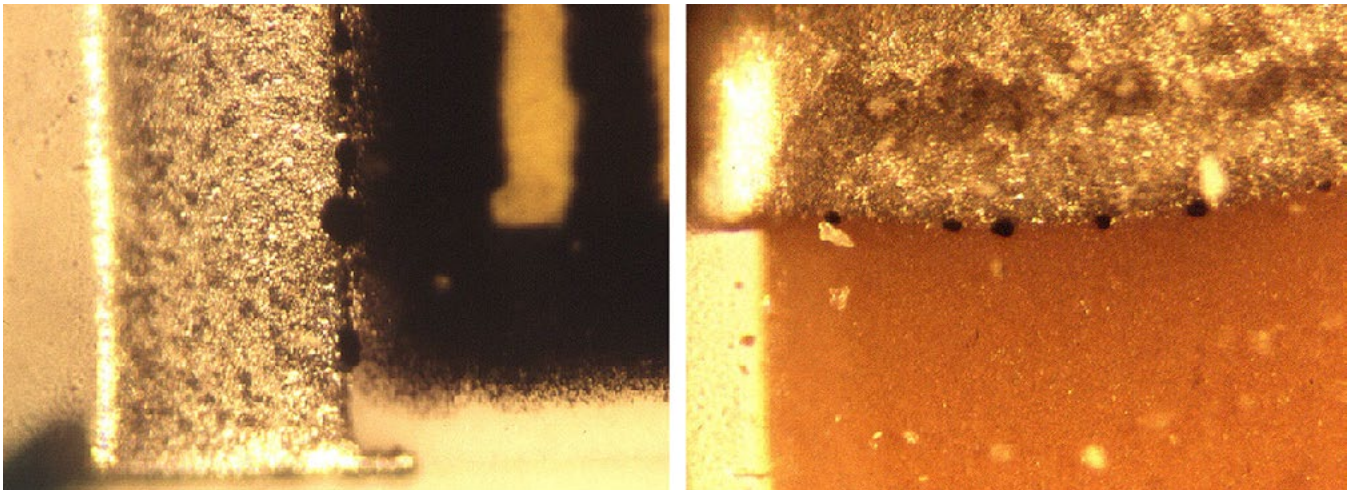

Figure 6: The silver layer between the resistive element and the termination was being corroded in automotive and medical applications.

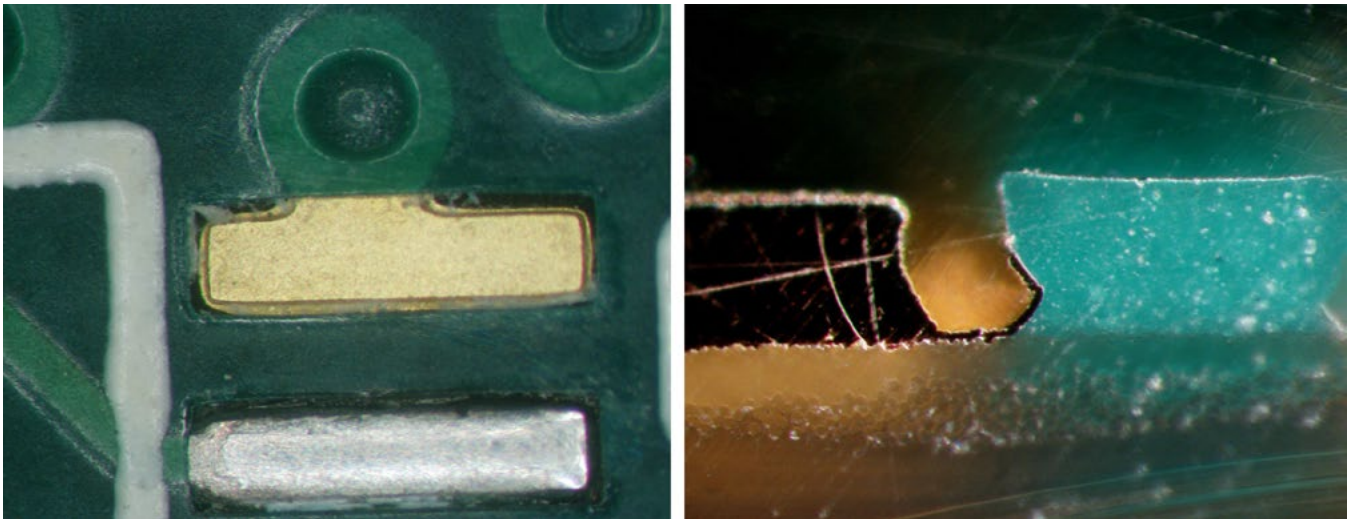

Figure 7: Example of nickel foot.

PCB Nickel Foot

Over the last few years we have seen more of this phenomenon, which indicates very poor process control in PCB manufacture. The nickel has extended onto the surface of the laminate and in one case the side wall of the solder mask. This has allowed the gold to also coat the surface (Figure 7). This could be an overactive plating process of copper needles left in the surface of the laminate after the etching process, and can impact the electrical performance and also increase the number of solder shorts.

Copper Dendrites

The three examples all show copper dendrites formed on the surface of printed circuit board assemblies. In each case they lead to intermittent failures in the field. They will occur with a tin/lead and lead-free process and need to be analysed to find the root cause of the problem. The examples show the formation of a copper dendrite/fern between two conductors. This fault may occur when flux residues remain on the board surface and are then subjected to high temperature and humidity. A circuit with a voltage applied of 5–10 volts can

CASE STUDY: DETECTING PROCESS DEFECTS *continues*

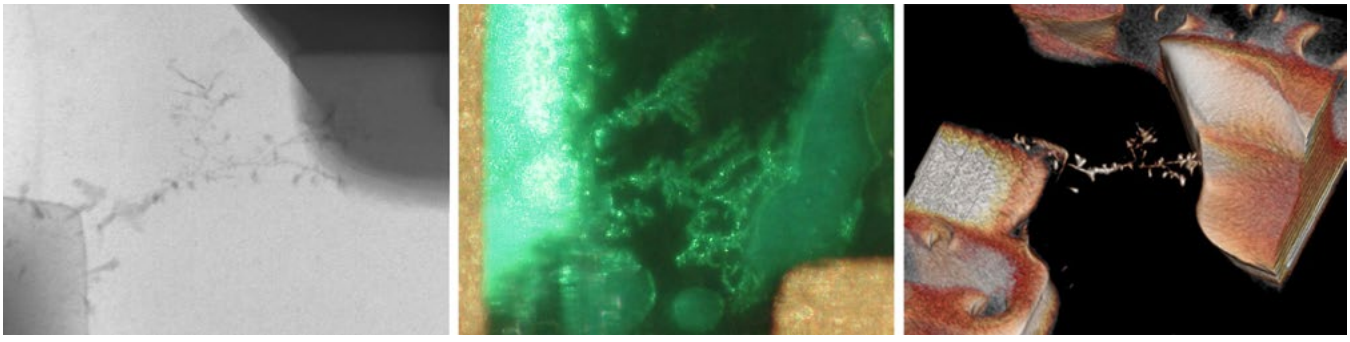

Figure 8: The images show the same defect using three different FA techniques to X-ray (left), back microsectioning (center) and CT (right).

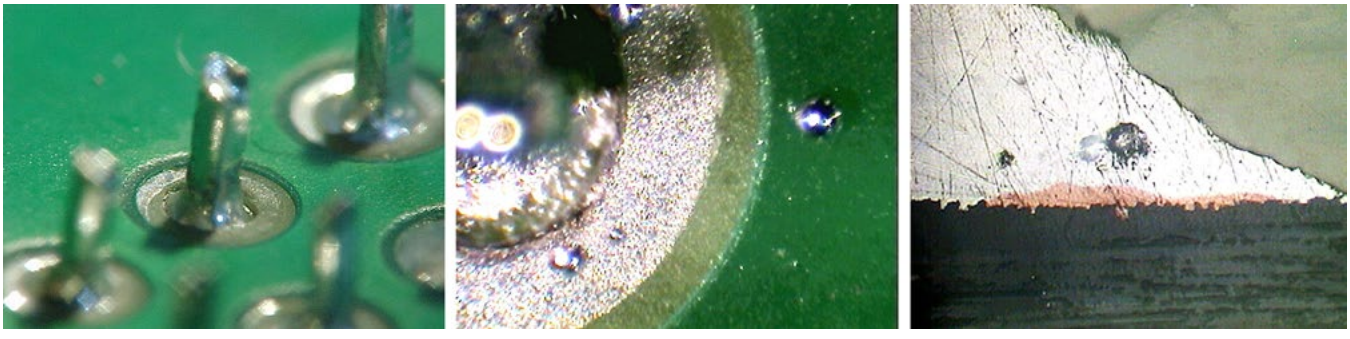

Figure 9: Examples of copper erosion.

then allow the formation of a conductive path on or through the moisture layer.

A copper dendrite often creates an intermittent fault which can be very difficult to pinpoint. Contamination testing and surface insulation resistance (SIR) assessment are two techniques often used to monitor and control the levels of harmful contamination on finished products to help avoid the possibility of corrosion. Contamination that causes this failure mode is not only from the flux; it can come from the cleanliness of the printed board prior to use. It can also be caused by the design of the board, the way it is mounted in a product, and exposure to changes in temperature and humidity. X-ray and CT were produced on a DAGE system.

Copper Pad Erosion/Dissolution

Although examples of copper erosion have been highlighted in the industry, there is little evidence of this being an issue. In the case of single-sided boards, the apparent erosion may have been due to preparation of the copper for OSP treatment. In this case copper is mildly etched, and excessive prep may have removed more copper around the pads as other areas of the tracking would be protected by the solder mask. Where mechanical cleaning is used and incorrectly controlled, the copper can be reduced around the hole leading to an apparent copper reduction. Further investigation of the problem and the examples circulated in the industry will be further reviewed and where appropriate further trials conducted.

It is interesting to note that the defects highlighted have not been shown to cause failures. At first examination we would consider them all rejectable based on our existing knowledge of tin/lead joints. That knowledge is again not necessarily based on failures but the inspection criteria for solder joints in circulation today. Perhaps we do need to re-examine

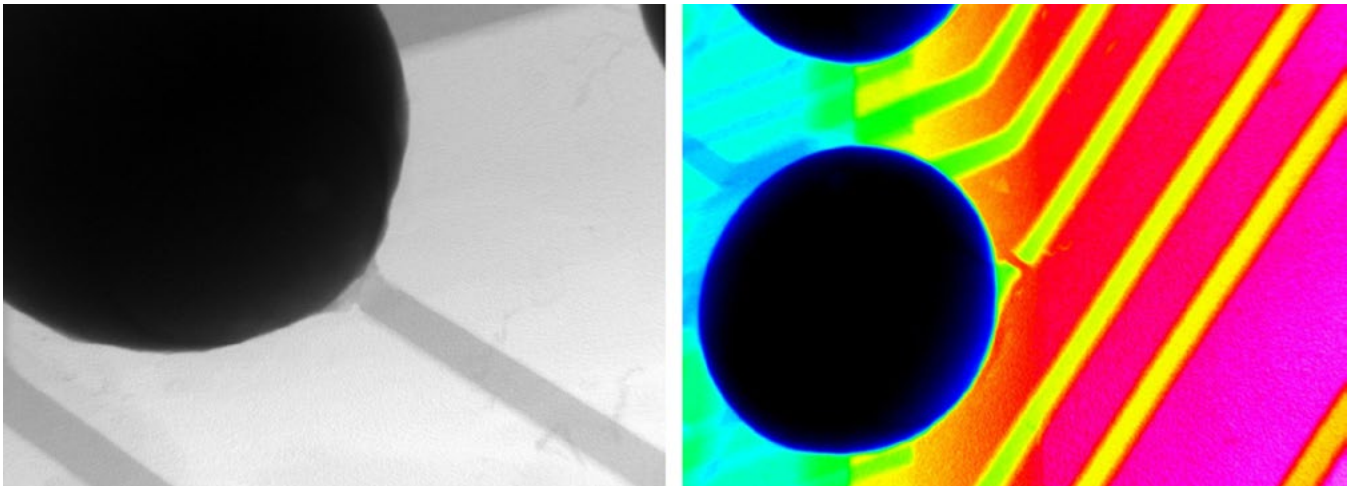

Figure 10: PBGA ball with open circuit connections.

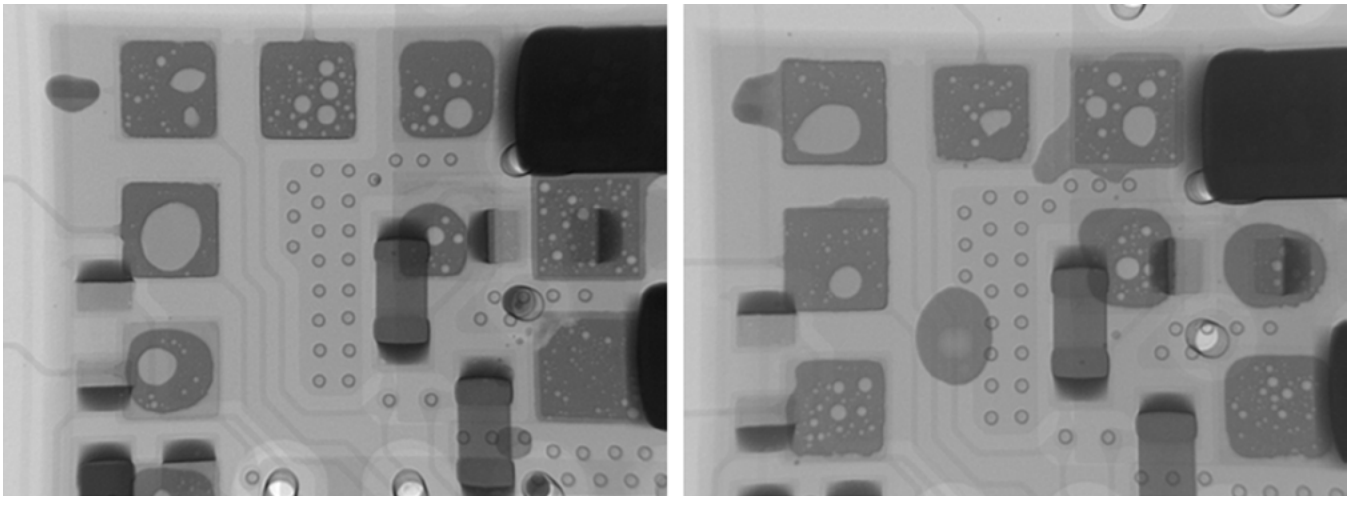

Figure 11: X-ray of components that have been placed in production prior to reflow is a good way of seeing any variation on placement force without disturbing any packages.

some of the visual criteria we use in the industry for lead-free. Recent trials have been conducted on selective soldering systems with lead-free alloys. In this case, where the boards had very thin copper plating and had been solder levelled with lead-free, the copper removal was significant. After exposing the boards to a high temperature during selective soldering for an extended time, copper pads were fully dissolved from the surface of the board. This is not typical and should not occur when a sound plated layer is present in a well-controlled lead-free assembly facility. However, it does demonstrate what can happen. A full paper on the work we have done at NPL on copper dissolution is available from the Defect Database.

Broken Circuit Tracks on BGA Design

Large PBGA ball was found with open circuit connections. X-ray examination found broken tracks leading to corner ball terminations. The PBGA was mounted on a standard 1.6 mm fibre glass FR-4 substrate. Probable cause may be expansion and contraction of the package and board during high-temperature operation; this is the likely cause for the open connections. If the pad surface had separated from the board (pad cratering), due to mechanical shock or

CASE STUDY: DETECTING PROCESS DEFECTS *continues*

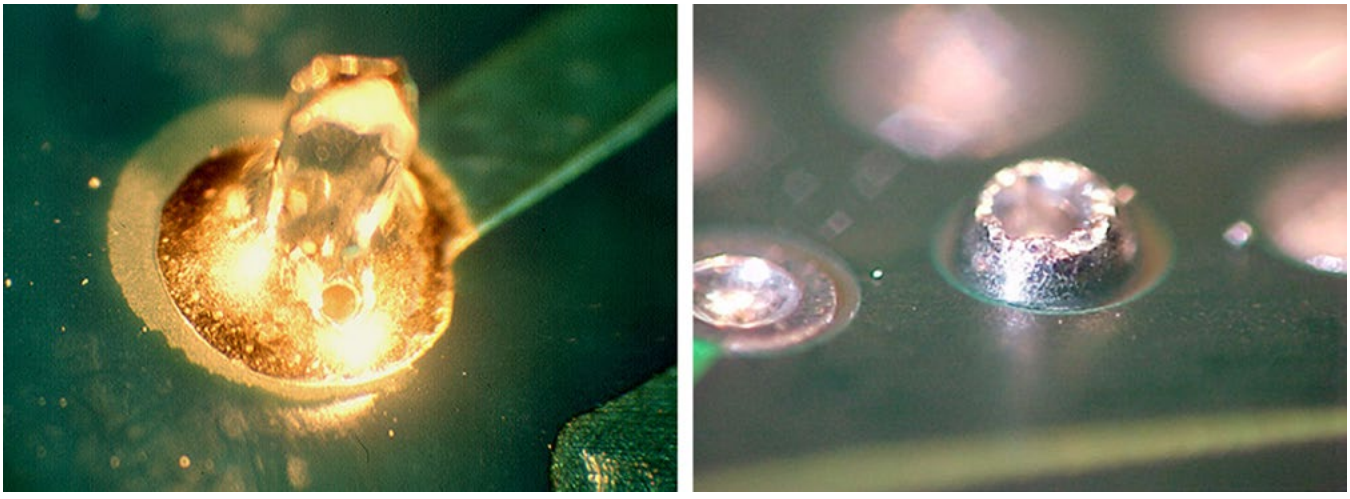

Figure 12: Outgassing from a plated through-hole board.

high Tg laminate, the failure would occur more easily. Close examination of the broken track, the quality of the original plated connection points and analysis of the operating environment would be required.

Solder Squeeze/Compression

Solder paste squeeze-out is a process issue which largely relates to the paste volume and placement force. Each of the X-ray images show paste that has been displaced then reflowed leaving what UK engineers call "solder sausages." If solder paste is displaced due to incorrect process parameters or poor control it will not flow back across the solder mask. This is due to the downward pressure of the package as other terminations start to reflow and wet to the pad surfaces. X-ray of components that have been placed in production prior to reflow is a good way of seeing any variation on placement force without disturbing any packages.

PCB Outgassing and Blowholes

New lead-free processing and materials lead to an old problem, same causes. Outgassing from a plated through-hole board is caused by moisture in the printed board expanding during soldering. The gas comes out of the hole as water vapour while the solder is in a liquid state. Voids are mostly seen on the base of the board because the solder has solidified first on the topside, hence the expanding vapour has only one way to escape. The size of the voids, blowholes or pinholes is related to the amount of escaping gas and the point at which the solder starts to solidify. Testing boards is easy with the oil outgassing test: old problem, old test and same old solution. Conducting the test shows where and how the gas escapes from holes and can show if the position is random or on selected areas of the barrel.

Baking boards can eliminate the moisture from the board ***but it does wonders to the solderability of new surface finishes,*** and it does not necessarily get to the root cause of the problem. The most common reason is the thickness of copper in the plated through-hole which may not be able to evenly cover poor drilling. This can also be impacted by the greater dissolution rates in lead-free assembly. The lead-free alloy also has an impact on what the joint looks like depending on whether it's non eutectic or not. **SMT**

Bob Willis is the owner of Bobwillisonline.com. He will be at SMTA International in Chicago offering free advice during the exhibition. To view a free webinar on process defects, causes and cures click here.

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Electronics Industry News
Market Highlights

Cloud, Big Data Driving Growth of Data Center Equipment Market

TMR analysts state that the global data center equipment market was worth US$32.15 billion in 2013 and will display a 12.9% CAGR between 2014 and 2020. Digitalization of data across various industry sectors has created unparalleled demand for data storage and data backup facilities.

Enterprise Network Equipment Market Projected to Reach $30.6B by 2020

Rising bandwidth requirements, expanding mobile workforce, growing base of mobile Internet devices, and accelerating shift towards wireless systems are expected to drive the global enterprise network equipment market to reach $30.6 billion by 2020, according to GIA.

US Medical Imaging Industry Faces Transition

Medical imaging is a notoriously data intensive field with its volume, variety and speed of data generation multiplying every day. Conventional tools are incapable of efficiently managing such large and complex datasets—posing limits on scalability, sustainability and usability.

Smartphone Sales Remain Vital to IC Market in 2015

Smartphones first accounted for more than 50% of total quarterly cell phone shipments in the first quarter of 2013. In the fourth quarter of 2015, smartphones are forecast to reach 435 million units or 80% of total cell phones shipped, according to IC Insights.

Tablet Shipments Experience Largest Decline since Inception

For branded tablets, the year 2015 is off to a rocky start. For the first time since inception, the popular consumer item experienced its largest quarter-on-quarter decline to date of 35%, and largest year-on-year decline of 16%, according to market intelligence firm ABI Research.

Manufacturing in a World of Stress

The Institute for Supply Management said the Purchasing Managers' Index (PMI), a short-term leading indicator of U.S. manufacturing growth, increased by 0.7 percentage points from May to a level of 53.5% in June.

Device Shipments to Reach 2.5 Billion Units in 2015

Worldwide combined shipments of devices—PCs, tablets, ultramobiles and mobile phones—are expected to reach 2.5 billion units in 2015, a 1.5% increase from 2014 and down from the previous quarter's forecast of 2.8% growth, according to Gartner Inc.

Wearable Medical Devices Market to be Worth $5.8B by 2019

Transparency Market Research's report says the global wearable medical devices market was worth $2 billion in 2012, and is estimated to be worth $5.8 billion by 2019. The study also indicates that the global wearable medical devices market will register a CAGR of 16.4% during the forecast period of 2013 to 2019.

China: Rise of the Robots

China overtook Japan in 2013 to become the world's largest market for industrial robots. A 53% jump in domestic sales last year means the country now accounts for a quarter of the global market; but analysts believe this is only the beginning, given the low use of robots in China's production plants.

IHS: Growth Rates of 3% "Relic of Economic History"

The long-term potential growth rate for advanced economies will decelerate to an average of 1.8%, down from average potential growth of 2.5% during 1990–2007, according to an analysis utilizing the Global Link Model from IHS Inc., the leading global source of critical information and insight.

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Reducing Risks to Employees' Health with Extraction and Filtration Technology

by Stefan Meissner
ULT AG

Capturing and Filtering of Airborne Substances is Anything but Simple

Occupational health and safety in manufacturing companies have become increasingly important in recent years. Today it should be seen as a part of the job rather than an annoyance. Manufacturing processes have gained in complexity, and resulting pollutants have become smaller and particularly more exotic. "From chipping come chips" is a popular saying. Today, the chips cannot be seen with the naked eye any longer since particle size of resulting dust and smoke has arrived in the nano range.

Pollutants of any size always affect humans, machines and the environment. In addition to social and human aspects, a high sickness absence rate of employees has adverse economic effects on a company just like malfunctioning machines due to pollutions. Maintenance expenses, rework and finally loss of reputation and falling demand are the predominant adverse effects.

These factors lead to a rising demand for extraction and filtration technology, which reliably protects equipment and employee health, and furthermore, takes account of changing process parameters.

By now, extraction and filtration technology covers a wide range of airborne substances. Nearly all processes to be found in the manufacturing industry are supported. From interconnection and separation technologies, surface processing such as drilling, sintering and milling, the utilisation of fluxes or production processes such as 3D printing or rapid prototyping by means of laser, soldering and gluing — all these processes generate harmful substances that might show extreme impact on health.

Lasers are increasingly utilised in metal and plastics processing (e.g., drilling, welding, cutting, engraving, sintering, etc.). For example, in metal processing dusts containing heavy metals are released that may accumulate in the human body. During processing of alloyed metals, contained substances such as nickel, cobalt and chromium are released. The pyrolysis of organic substances may generate dioxins or hydrogen

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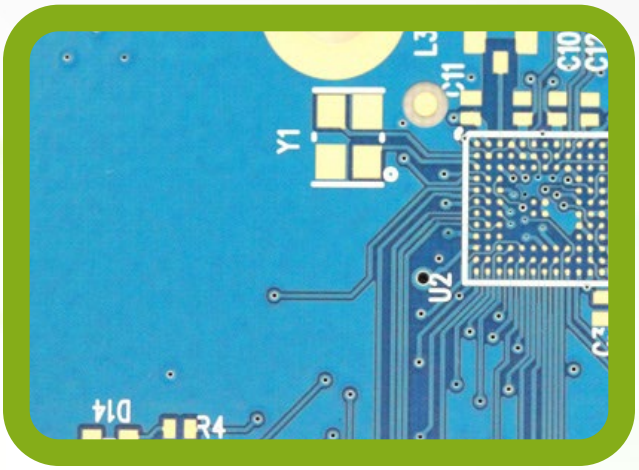

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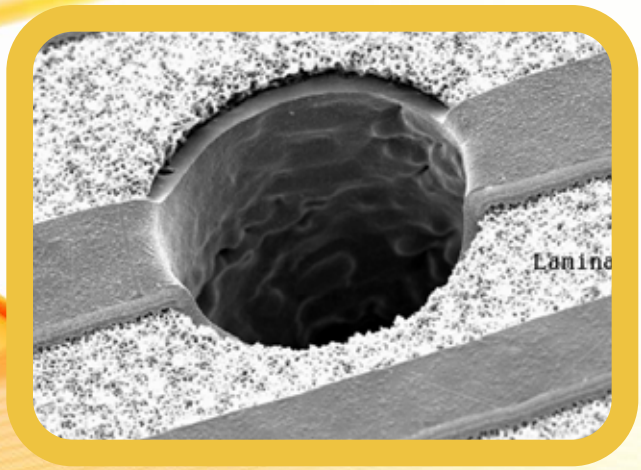

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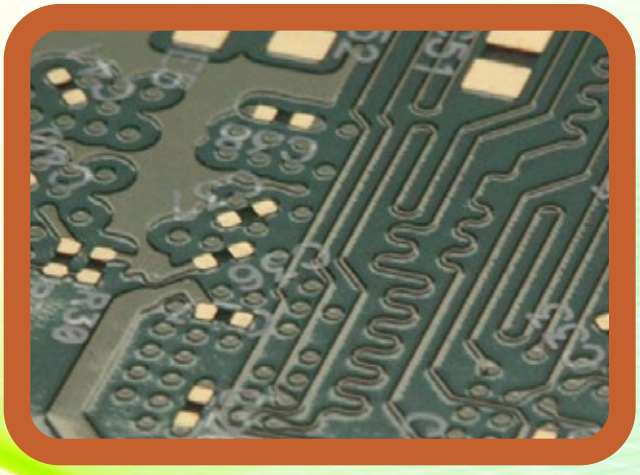

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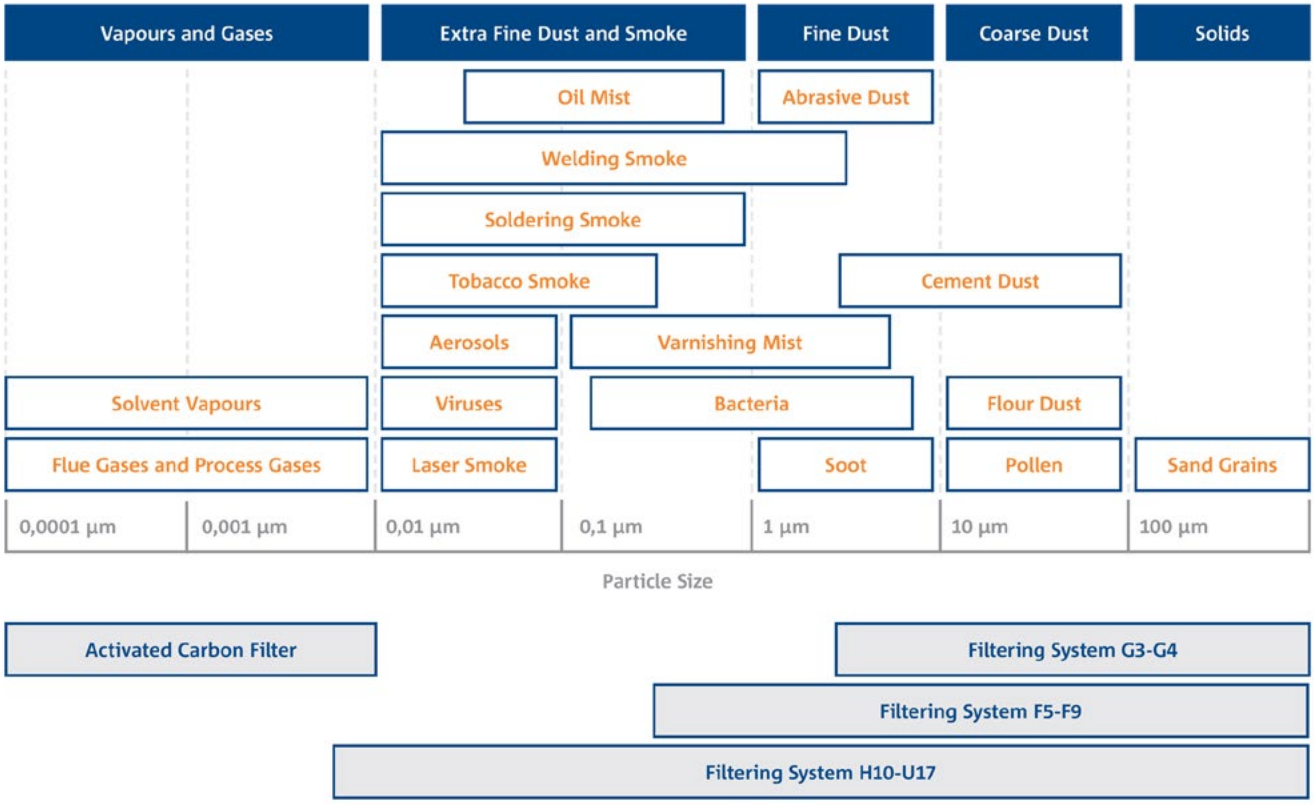

Figure 1: Overview of dust particle sizes.

chloride. Moreover, laser smoke contains fine dust that may, at worst, lead to respiratory diseases, cardiovascular problems and an increased cancer risk.

Apart from bad quality of work due to permanent smoke and odour emissions, machines may be affected or damaged due to pollution and chemical reactions of their products. In particular, in the case of finest precision mechanical works, each kind of impact by particles must be avoided.

In many countries, there are clear regulations and laws to remove hazardous substances in the breathing air. Germany, for example, has the Ordinance on Hazardous Substances, Technical Instructions for Air Quality Control and Technical Rules for Hazardous Substances. Those standards require that "produced dusts must be completely captured and safely disposed."

There is a four-level protection concept, ranging from minimising dangerous substances (level 1), via substitution of hazardous substances and (use of) extraction devices (level 2), and closed systems and access limitations (level 3), to demarcation of risk areas and respective limitation in clean air return. In addition to the regulation on contaminant capture by closed and open systems, it is specified that dusts and gases must be filtered on a high degree (>99.95%).

Users of air filtration plants do not necessarily have to know all these regulations, however, vendors of extraction and filtration systems must know them in detail. They need up-to-date expert knowledge on the full range from checking the medium to be filtered, particle size distribution and characteristics (adhesive, subliming, etc.), up to tests of hazardous substances and flammability.

Clean air return is not regulated by law but strengthens economic and ecological acceptance and self-interest. From the point of view of a healthy air balance and heat-loss avoidance, extraction and filtration technology should be utilised in the best way possible.

What do users of extraction and filtration

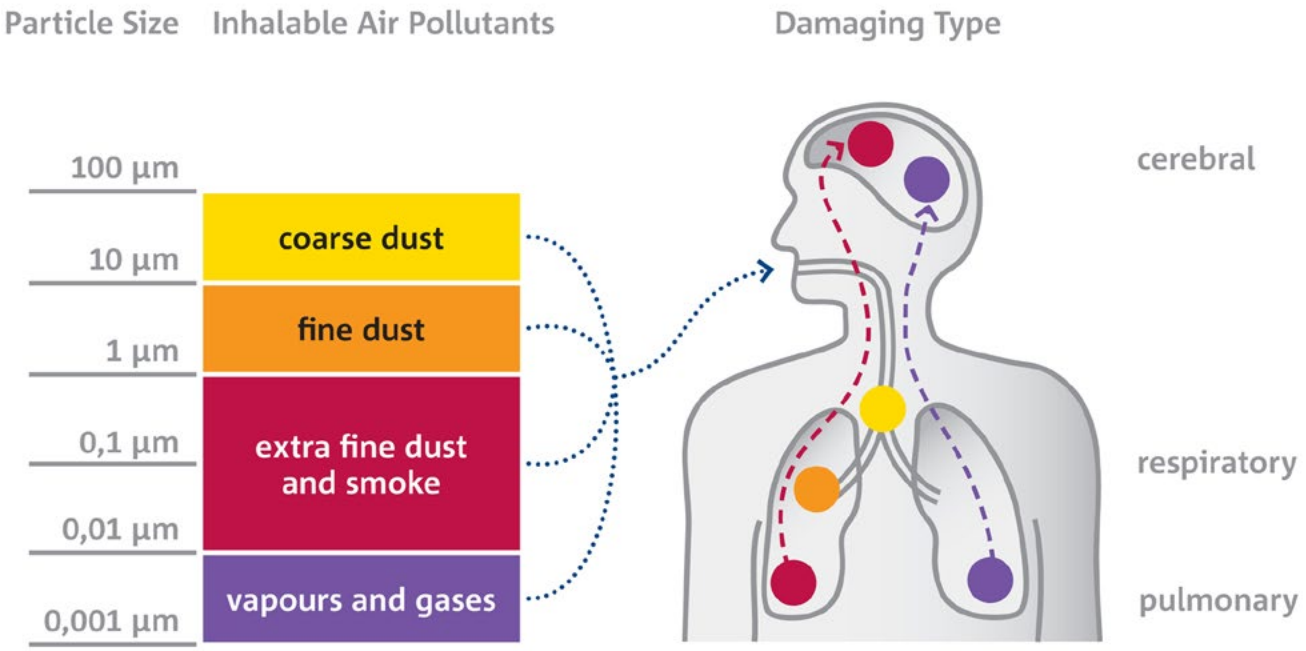

Figure 2: Impact of hazardous substances on the human organism.

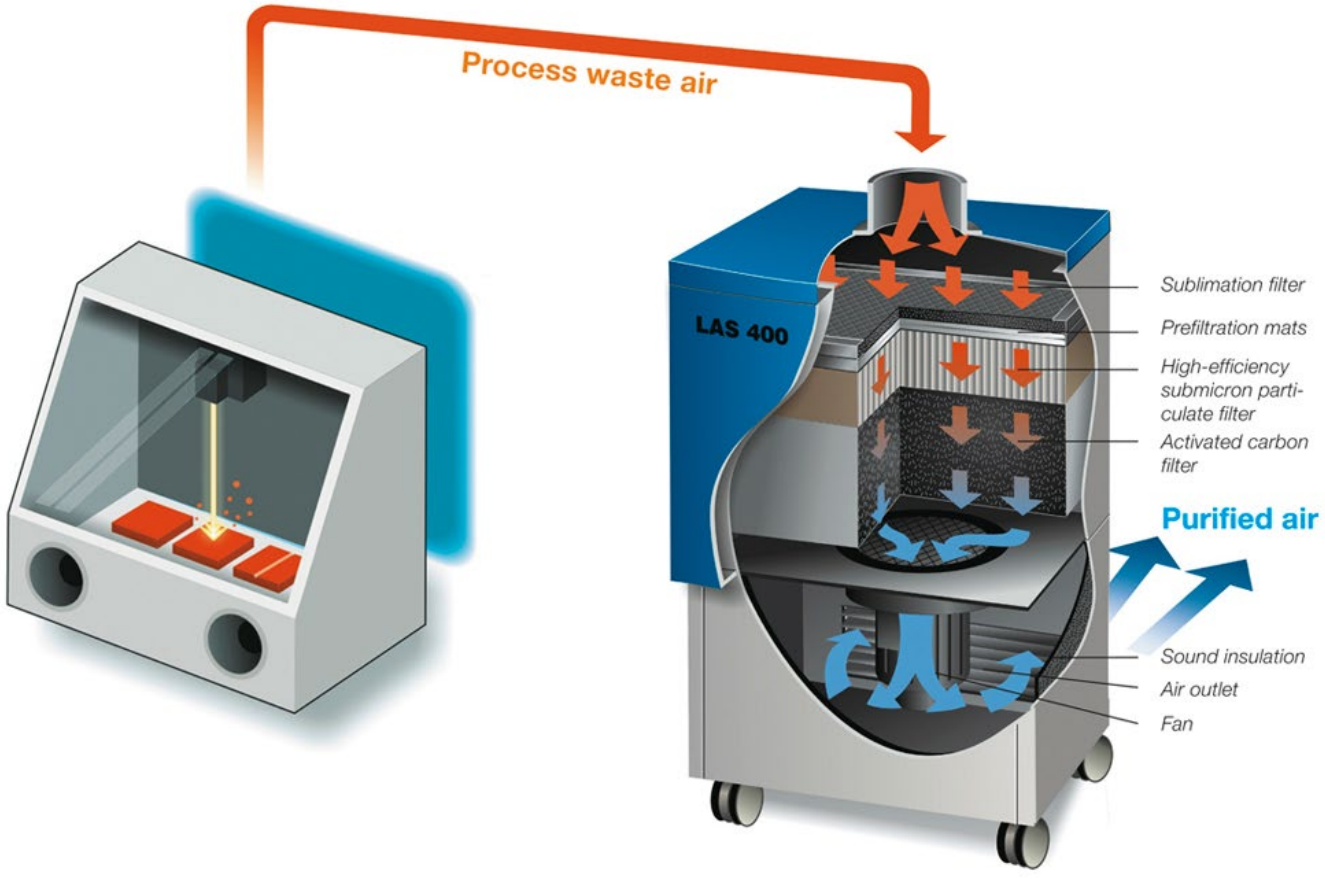

Figure 3: Example for combination filter in an extraction and filtration system for laser processes.

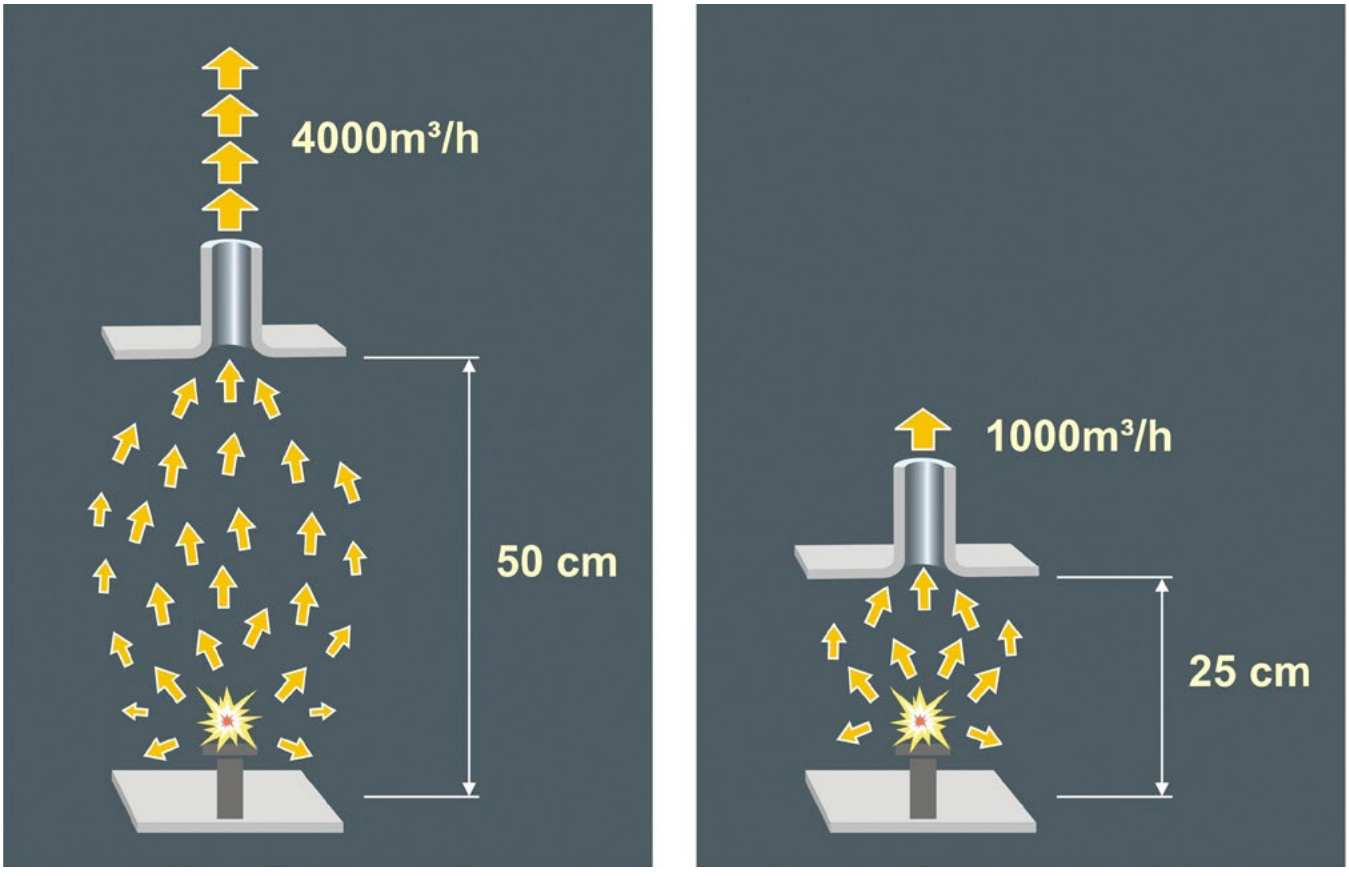

Figure 4: Influence of distance to the required air flow.

systems expect? Primarily, such systems must meet various requirements to guarantee minimal maintenance effort, health protection and high quality of work. This includes:

- Complete removal of all dusts, smokes, vapours, odours and gases.
- Incremental filtration: Utilisation of prefilters for coarse particles (sedimentation dust > 10 µm) to avoid premature saturation of fine dust filters (for particles < 10 µm) and adsorption filters.
- Adaptation to relevant contaminants: An extraction system must absorb all particles, vapours and gases. Therefore, the capacity of the filter media must be adapted to the emitted amount of particles. For example, a large amount of coarse dust requires high-capacity filters to avoid too frequent replacement. Too low saturation conditions lead to extremely high maintenance efforts for the extraction system. On the contrary, if fine dust is largely produced, coarse filters may have low capacities.
- Adaptation to work places: In large production plants, attributes such as 'space saving,' 'mobile' or 'silent' do not matter. However, such characteristics are welcome at individual and manual workstations. Filter technology must not be annoying—it should never disturb work routines, neither physically nor acoustically.

The capture of contaminants is regulated by law in various countries. These regulations determine risk categories for specific hazardous substances (e.g., in terms of fire and explosion risks or in types of health damaging effects, such as carcinogenic, mutagenic or toxic for reproduction).

Figure 5: Extraction arm for pollutant capturing at the work place.

Demand for particle capture at the point of origin makes sense, because:

- Large quantities of pollutants can be captured
- Relatively low capture efforts
- Good filtration opportunities are given
- Low energy consumption is possible

Basically, the appropriate capturing element can deliver a substantial contribution to the quality of the extraction and filtration device. The degree of capture rate forms the basis for subsequent high-grade filtration, finally providing high overall efficiency and low residue in the returned clean air.

Additionally, the place of capturing plays a key role. A general rule says that twice the distance between emission source and capturing element requires four times the exhaust performance in the extraction and filter system—a particularly noteworthy energy context in times of ever increasing energy costs.

Extraction and filtration in industrial environments goes far beyond the vacuum cleaner principle. It is not just a case of dirt removal but to eliminate hazardous substances in the air that may cause more than a dust allergy. The precondition for users is knowledge about their materials and processes. Vendors of extraction and filtration technology propose a suitable system. They have expert knowledge concerning legal regulations and chemical and physical characteristics of the media to be extracted and filtered. They finally adapt a system for air purification suitable to the operating conditions in a facility. **SMT**

Stefan Meissner is in corporate communications at ULT AG. He may be reached by clicking here.

MilAero007 Highlights

A Look at the High-Reliability Interconnect Market

In an interview with I-Connect007, Mark Cormier of Miraco Inc. discusses his company's activities and capabilities, the latest trends and drivers in the high-reliability segment, and their strategies when it comes to managing their assembly work as well as their audit processes to find EMS providers.

EIPC Summer Conference, Berlin: Day 1

Berlin, capital of Germany and a world city of culture, politics, media and science, was the venue for the 2015 EIPC Summer Conference, which attracted delegates from sixteen countries, including Russia, Hong Kong, Japan, Israel, USA and Canada, as well as the European Union, to experience a programme of 21 technical presentations over two days. Also included was a visit to the Berlin laboratories of Fraunhofer Institute, Europe's largest application-oriented research organisation.

IPC Lauds U.S. House of Rep on Passage of TSCA Modernization Act of 2015

IPC supports bipartisan efforts to reform the Toxic Substances Control Act (TSCA) of 1976, which needs to be modernized to reflect 21st century realities. A strong, cost-effective, science-based federal chemical regulatory program is important to IPC members, who use chemicals to manufacture electronics for the nation's defense, transportation, consumer and other industries.

Exception EMS Appoints Paul Rivers as Commercial & Special Projects Director

Exception EMS has appointed industry veteran Paul Rivers as Commercial and Special Projects Director. Rivers, who has a career in the PCB and PCBA industry that spans nearly 35 years, will head up the customer programs and support division.

EIPC Summer Conference: Day 2

Refreshed after an excellent conference dinner, and for most, a good night's sleep, delegates returned for the second day of the EIPC Summer Conference in Berlin, continuing the theme of improving profitability through technical leadership and innovation to meet future market requirements, with sessions on materials and processes for high performance PCBs and advanced material testing strategies to meet OEM and ODM needs.

LACROIX Electronics Earns PART 21 G

The production accreditation PART 21 G is part of the company's ambition in aeronautics' electronics that represent over 25% of the turnover of LACROIX Electronics in France.

NEO Tech Earns Raytheon Four Star Award

NEO Tech's Chatsworth facility has been awarded the prestigious Four Star Supplier Excellence Award and a Gold Award for Affordability from Raytheon IDS for supplying components on several critical programs. This places NEO Techamong the top of the 10,000 Raytheon suppliers.

IPC Europe Forum to Focus on Reliability

The IPC Europe Forum, with the theme "Innovation for Reliability," will focus on critical issues in high-reliability electronics for sectors including military-aerospace, automotive, industrial, and medical. The event will be held from October 13–15 at the Atlantic Congress Hotel in Essen, Germany.

API Technologies Names New VP of Continuous Improvement

API Technologies Corp. today announced that Domingo Isasi has been named to the newly created role of Vice President of Continuous Improvement for API Technologies, effective June 29, 2015.

Plexus Earns AS9100 for Engineering Solutions in Europe

Plexus Corp.'s Livingston Design Center in Scotland, which provides engineering solutions and award-winning customer service excellence to many of the world's leading branded product companies, has achieved AS9100 certification.

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STENCILS: Why They Still Matter

by Barry Matties
I-CONNECT007

I recently met with Eric Weissmann, president and CEO of Photo Stencil. In this interview, Weissmann shares some important points about the venerable stencil, the latest in stencil innovation, and the impact stencils, blades, and cleanliness can have on your product quality.

***Barry Matties:** Why don't you just start by telling me a little bit about Photo Stencil?*

Eric Weissmann: Sure, I'd be pleased to. Photo Stencil has been around since the early '70s making stencils, screens, and squeegee blades primarily for the SMT industry. Historically, there has been a continuum of products and demand for products for printing materials, from back in the old days with chemically etched stencils up to the modern, multidimensional 3D electroform type stencils. What we're seeing now is that there's been a bifurcation in the market for these stencils as well as simple ones that are served by laser-cut stencils. It's a piece of stainless steel that a laser cuts apertures through, which solder paste can then print through. That's on the one hand, and then there are the much more advanced applications with smaller features, products going into harsher environments, advanced packaging, and electrical interconnects on the micron scale. That is where we see our future.

For the last 18 months or so we've been making a lot of investments in our capability and our facilities to be prepared for where we see the market going.

***Matties:** What do you think of the new jet style applications?*

Weissmann: Dispensing versus printing is the broader question, and of course dispensing is a "dot at a time" kind of thing. It's a lot slower. We have the same kind of thing internally, the one-at-a-time versus a parallel process. When we make an electroform stencil, we do everything

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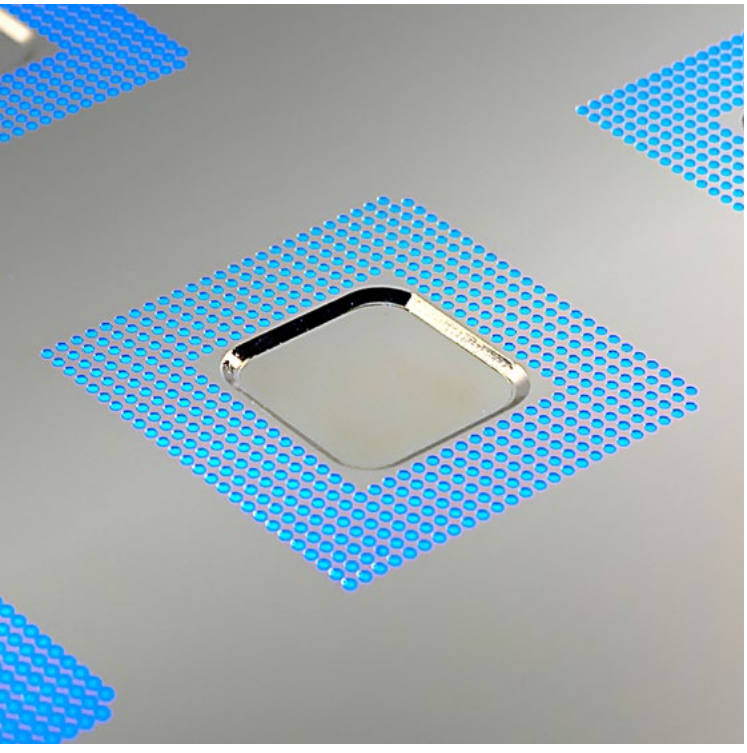
STENCILS: WHY THEY STILL MATTER *continues*



at once; a laser-cut stencil is cut one aperture at a time. If you have a wafer with a million things that need to be printed, that's going to be hours and hours instead of seconds. Speed is the fundamental difference. Other differences of course are accuracy, dimensionality, and flexibility in a stencil. Like dispensing, both technologies can print different kinds of materials. It can print flux and it can print paste.

The thing I see the most is just what everyone sees in terms of ever-smaller components and ever-tighter density. Right now we're looking at 01005 passives being quite routine, and our customers are talking about smaller passives in the relatively near future. Micro QFNs and other components are posing real challenges for people in assembly. What we're seeing are some of the companies making simpler products are using simpler stencils, but there's real value for OEMs—where the ultimate product goes into a harsh environment, like an automobile or an aircraft, or into something going into the human body like a medical device—to use a better stencil to get better paste transfer, but also a better quality mechanical electrical connection there at the joint.

Matties: *You're talking about higher quality stencils. When a customer is looking at millimeter application, what should the considerations be?*

Weissmann: The customer should be looking at the area ratio of the stencil, the ratio of the flat side of the pad that they want to print to the walls of the stencil, and how thick it has to be. The smaller that ratio is, the harder it is to transfer those things. You want to have a stencil with a smoother material, and that's a pure nickel stencil rather than a steel stencil. You also would like to have a stencil that has been electroformed, because you end up with smoother walls on the inside of the aperture, so it's easier for the material being printed to get through. One of the things that we've added this year is a laser imaging system in place of our traditional photo process, and that produces even more accurate and even smoother walls for more challenging printing applications.

Matties: *So they can go in and laser cut it?*

Weissmann: Well, a standard stencil has laser-cut apertures. Of course, the laser is melting and burning away the metal, so you end up with a jagged inside edge on the stencil. We are growing the metal, kind of like electroplating a cheap piece of jewelry, except that the plating is the product rather than the thing that that's being plated on. We grow it, and by using pure nickel or some alloys with a high amount of nickel, we can create a very smooth surface, both on the top and bottom of the stencil, but most importantly on the aperture walls.

Matties: *How long does it take to go through that process and create one?*

Weissmann: For single-level electroform stencils, we can normally ship them the next day if we receive an order released in the morning. It's a pretty fast process. If you have a very quick-turn requirement, but which is more demanding than a standard laser stencil, then we have a product called NiCut, where we have a pure nickel piece of foil, but we laser cut the apertures, and that is a little bit faster from a turn time perspective. The performance is bet-

ter than a standard laser-cut stencil, and not as strong as an electroform stencil.

***Matties:** Stencils are part of the process, but it's not what you would call the sexy part of the process, right?*

Weissmann: It's certainly not sexy, but it's important. More than half of the defects in assembly come at the printing stage—every piece of that needs to be dialed in.

***Matties:** We're focusing our upcoming magazine issue on the 'War on Failure,' and we ran a survey of assemblers. Their number one issue, of course, is software, as well as defects like head-in-pillow. When you look at all the contributing factors to this, printing obviously is one of the issues that they have to concern themselves with, along with cleaning and other variables. How do you fit into the solution of that defect?*

Weissmann: An assembler is looking at a tolerance, so they have a tolerance stack-up with variability that comes from the stencil, the material, and the printer. A cheap stencil uses up way too much of that allowable tolerance. It's a question of positional accuracy, dimensional accuracy, as well as having the ability to get the right amount of paste to transfer through that aperture. A better stencil uses a lot less of the variability in the process, and therefore can become less of a critical piece in making that happen. You need all of the pieces to work well together, but your whole process is only going to be as good as your weakest link. Too often we see that being a low quality stencil.

***Matties:** What's the price difference? What is price difference between high quality and low quality?*

Weissmann: It might be as much as 4:1 depending on the specific features, but there is a range of different products.

> "You need all of the pieces to work well together, but your whole process is only going to be as good as your weakest link. Too often we see that being a low quality stencil."

***Matties:** What's the typical price of a stencil? I'm not familiar when you say 4:1, what kind of numbers are we talking?*

Weissmann: The cheapest stencils, and we don't do much of these, might be $250 or even a little bit less. Whereas on a single-level stencil, you can go up into the thousands for a really great stencil with really demanding requirements. Most of them are a little less than $1,000 for those kinds of stencils.

***Matties:** Someone who's in automotive or high-reliability work, they're going to use the $1,000 models?*

Weissmann: It depends on their application, and we'll help them match the application with the right stencil material for what they're trying to make.

***Matties:** The cost of failure is so high in automotive or aerospace. It's life or death in some cases, and then there's, of course, product liability that comes back to some of the manufacturers. It seems to me for $700–1,000, why risk it?*

Weissmann: It seems that way to me, too. Another piece of the process that can make a difference is the blade. We find blades to be the ugly stepchild of the printing process, and customers should take more care to ensure that their blades are new and well maintained, and that they match the type of stencil that they're using.

***Matties:** How often should they change their blades?*

Weissmann: They really just have to watch and see, and then they can come up with a timeframe. But it depends on their printing pressure, their throughput and their use, and also on the type of stencil that they're using. You

STENCILS: WHY THEY STILL MATTER *continues*

want it to match, so if you're using an electroform stencil, ideally you should be using an electroform blade, and then you won't have the parts damaging one another as they scrape across.

***Matties:** Do you offer some sort of free evaluation, where you go into a shop and look at their systems and see what they're doing, and then make recommendations of how to improve?*

Weissmann: What we would normally do is take a look at the customer's board or drawing and recommend what they should be using. It's also really important that we talk to the customer and see where they're having challenges. We do often make suggestions for modifying the stencil design as well as the stencil type to come up with better results.

The thing we need to be looking at is that customers look at their whole process to improve it and find the weakest part. A stencil is an awfully easy thing to improve. You don't have to change much of the rest of your process, if any, and you can get better results by using better stencils in SMT. Study after study shows that the type of stencil makes a difference, and that the quality of the stencil makes a difference in the quality of the print that a customer ends up with.

As components get smaller and density increases, that's going to become more and more critical to avoid bridging and many of the other defects that you can see. There will always be a need to print materials in the electronics industry, whether it's solder or some of the other alternatives that are out there. You still need to get it in the right place in the right amount, and that's what we can help with.

***Matties:** There's this whole new marketplace that's just emerging where we can start printing circuits on our wallpaper or on our sofas...*

Weissmann: Or on the side of a building. We have a customer who has worked out how to make lighting on the side of a building that's only visible from one direction, and that's a materials printing process too. There are a lot of amazing material printing applications out there, and they all have to have the right amount of material in exactly the right place and exactly the right quantity.

***Matties:** As far as cleaning and maintaining, what are the issues that people should look at and concerns that they should have?*

Weissmann: The quality of a stencil can make a big difference in the cleanability of a stencil. This affects how often you have a failure, because a failure in cleaning can create a failure in printing, but it also slows the process down, like whether you have to clean every five prints or every ten prints. That makes a big difference, too. A pure nickel stencil, a stencil that has a smoother finish on the contact side surface of the stencil, will clean better and need to be cleaned less frequently. This is also one of the benefits of the nano-coating that can be applied to a stencil that helps make that possible.

It's important not to have debris introduced in your products by the indirect materials like a stencil or a blade. That's one of the reasons that in our new factory we're going to be doing all of our assembly inside cleanrooms for all of these products. Our semiconductor customers are in cleanrooms now, and as more and more of our SMT customers are moving to clean assembly,

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IWLPC Conference: October 13–14 **IWLPC Exhibits: October 13–14** **Tutorials: October 15**

EVENT SCHEDULE

Tuesday, October 13 – Wednesday, October 14

Exhibition, Panel Discussion and Technical Presentations on 3D, WLP and MEMS

Thursday, October 15

Professional Tutorials

T1: Introduction to Fan-Out Wafer-Level Packaging

T2: 3D IC Integration and 3D IC Packaging

T3: Adhesion Science & Practice with an Emphasis on Temporary Bonding of Electronics (Wafers, Displays, Devices)

T4: Wafer-Level Packaging for MEMS and Microsystems Technologies for Size and Cost Reductions

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CONFERENCE SPECIAL EVENTS

Tuesday, October 13

Keynote Breakfast Address
High Density Fan-Out: Evolution or Revolution
Rama Alapati, *GLOBALFOUNDRIES*

Panel Discussion
Fan-Out WLP Panel Processing: Will it happen and What will it be?
Moderator: Jan Vardaman, *TechSearch International*

Exhibitor Reception
Join us in the Bayshore Ballroom for the Exhibitor Reception where over 60 exhibitors will showcase the latest products and technologies offered by leading companies in the semiconductor packaging industry. This evening reception offers attendees numerous opportunities for networking and discussion with colleagues.

Wednesday, October 14

Keynote Address
2.5D/3D IC – Examining Low Cost Alternatives
Sitaram Arkalgud, Ph.D., *Invensas Corporation*

Panel Discussion
Interposers, 3D TSVs and Alternatives: What are the Options and Where do They Fit?
Moderator: Françoise von Trapp, *3DInCites*

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we're seeing that being a much more important criteria: Ensuring it's a cleanroom-ready product before you take it out of the box.

***Matties:** What sort of life expectancy should somebody expect from a stencil?*

Weissmann: In most cases, customers will change their designs more often than a stencil wears out. Sometimes you have some things that are very high runners and then they'll wear out. We have a customer that makes a set-top box, and they make about 40,000 a week and go through a couple of stencils a week to do that.

***Matties:** It's important to take good care of every part of it—good housekeeping brings good product.*

Weissmann: Right, and to be careful with it. Stencils can be thin—some of them we make now are less than 1 mil thick. It's pretty easy in handling to drop those stencils and break them.

***Matties:** How does the cleaning process work?*

Weissmann: There are two ways of cleaning stencils: One is during the use of the stencil; the underside cleaning is performed by the printer. The other is to clean the stencil afterward. We test our stencils with the different cleaners that are out there, the cleaning solutions and so forth, to make sure that they're durable. The one caution I would give is that some customers have tried to turn up the heat on their cleaning solutions, and that can adversely affect the lifetime of a stencil.

***Matties:** Another variable, right?*

Weissmann: Right.

***Matties:** It's all about the variable controls. Do you bring the Internet of Things to this part of the process, where you're measuring the wear of the blade or the surface of the stencil? Because this is where we're talking about going. This is the kind of thing that your customers would love to have, because it's going to save them from defects. Even when you're talking about cleaning, it could measure the temperature of the cleaning process and give all that feedback instantly.*

Weissmann: Or why not clean when you need to clean, instead of just randomly?

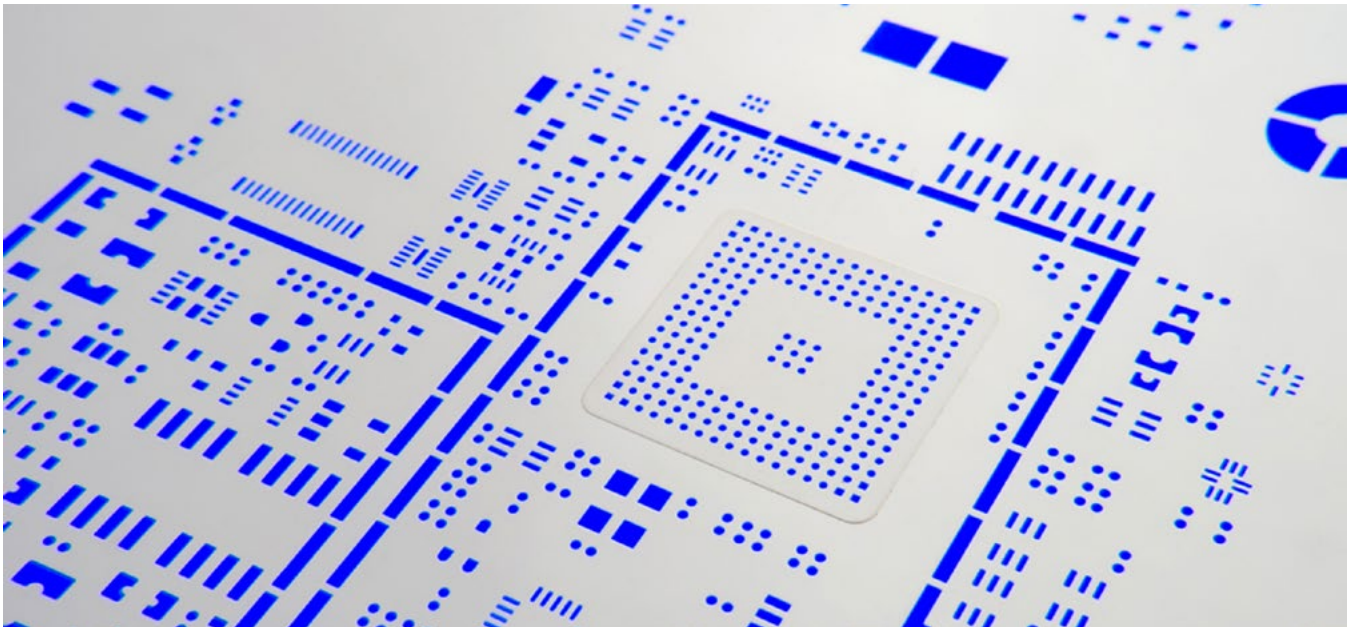
***Matties:** Exactly.*

"The one caution I would give is that some customers have tried to turn up the heat on their cleaning solutions, and that can adversely affect the lifetime of a stencil."

Weissmann: Well, maybe we'll have a discussion about that at the next trade show. There's so much opportunity in the smart factory. We say SMT printing is as much art as science. That just means we need more science.

I think one other thing I'd like to touch on is in comparing different stencil products, and it probably applies to any product, but we're most interested in helping with stencils. If we look a little bit below the hood, what does a specification mean? What does the thickness of a stencil mean? Is that the thickness at the edge of an aperture, the average thickness across, and exactly how positional accuracies are measured, and so forth?

So we would look at what it means to have each of these things, and we are planning to publish a set of open source specifications for different attributes of stencil measurement. By open source I mean that the design of the test stencil will be public, that anybody can extend it, like open source software. It can become an evolving standard faster than a standards body could evolve it; that would help customers decide what certain things mean. They'll be able to say, "Well, we want one that's measured this way." Once they determine their critical performance characteristics, they can specify that spec measured that way, as opposed to the way that a



supplier chooses to measure it to best showcase their strengths and hide their weaknesses.

***Matties:** Are you saying it's going to be an OEM that specs it? Is that something that is happening now where an OEM would go as far as spec'ing a stencil?*

Weissmann: I think that an OEM looking at alternatives would say that they need positional accuracy measured this way, as opposed to saying more broadly, "We need X positional accuracy." Because any vendor can create a measurement that works for them, and it is comparing apples to oranges. I'll give you an example: We make 3D stencils, and this is helpful if you've got something placed on an IC substrate or on a circuit board already and you don't want to diffuse it, or if you need to print down into a cavity—there are a lot of different reasons why you might need a multidimensional stencil. Well, we can make multidimensional stencils with some 90-degree pockets. We've seen on some competitors' websites that they can do 90-degree pockets, but we know they can't do them in a real environment. They might be able to do one pocket 50 microns deep on a stencil, where we do dozens of pockets and they can be 20 mils deep and it's a totally different challenge. What does it mean to be able to produce a 90-degree wall on a 3D stencil? That's a case where asking a better question can really help a customer get what they need.

***Matties:** It is just a matter of knowing to ask that question.*

Weissmann: Right, and so by publishing a set of open source standards for measuring these different things, that will help our customers compare apples to apples.

***Matties:** When will you roll that out?*

Weissmann: They'll start coming out this year. Of course, since they're open source they'll be continually updated and enhanced as we go, and it's more of a continuous improvement than a big bang drop.

If some fork of that branch gets more acceptance, then that can become the official version, and that's great. We want to exercise our leadership in this. We're certainly the most technologically advanced stencil vendor in the Americas, but we hope that others will dive in and contribute their expertise as well for the benefit of the industry.

***Matties:** Thanks so much for spending time with us today.*

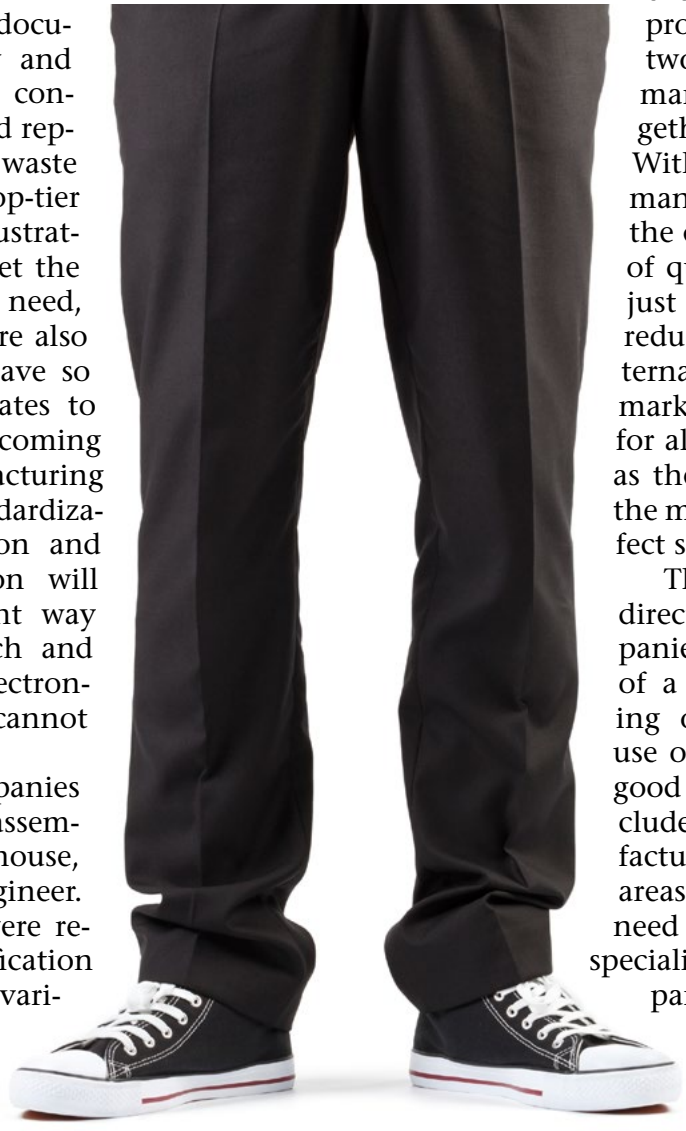
Weissmann: Thank you. **SMT**

THE ESSENTIAL PIONEER'S SURVIVAL GUIDE

Don't Allow Standards to Get the Better of You

by Michael Ford
MENTOR GRAPHICS VALOR DIVISION

A standard should be complete, unequivocal, and consistent; it should be something that everyone can use and understand, promoting quality, responsibility, conformance, and compliance, as well as openness and visibility of information. In the electronics manufacturing industry, this just doesn't seem to be the case, with so many different so-called standards for everything ranging from operational rules and documentation, to quality and traceability, which are confusing, incomplete, and represent a major cost and waste to manufacturing. Top-tier OEM companies are frustrated that they cannot get the information that they need, while manufacturers are also frustrated that they have so many different mandates to follow. Surely, in the coming Internet of Manufacturing (IoM) age, where standardization of communication and storage of information will be critical, the current way in which we approach and adopt standards in electronics manufacturing cannot prevail, can it?



When OEM companies all did their own PCB assembly manufacturing in-house, it was the age of the engineer. Industrial engineers were responsible for the specification and execution of the various production processes and flows that connected them together. Quality management engineers ensured that all products that left the factory were free of defects. The science of quality management and control as well as that of industrial engineering progressed rapidly. The comparison of market defect analysis with internal quality reports led to active quality management so that the scope and risk of defect creation during production execution is a part of the process specification. The two engineering families in many cases now work together very closely, or as one. Within a vertically integrated manufacturing operation, the control and management of quality yielded more than just one order of magnitude reduction of defects, both internally and externally in the market, an important factor for all brand name companies as the cost of poor quality in the market can significantly affect sales.

The market then changed direction, where many companies decided that instead of a "profitless" manufacturing operation overhead, the use of EMS outsourcing was a good way to go. The lure included the ability to manufacture products in lower cost areas of the world without the need for investment, where specialist manufacturing companies would have access to greater discounts on material. How though to ensure that these

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September 15–17

PCB West
Santa Clara, CA, USA

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Co-located with SMTA International

September 28

IPC EMS Management Meeting
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October 13

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DON'T ALLOW STANDARDS TO GET THE BETTER OF YOU *continues*

remote external contractors would achieve the same levels of quality as the experienced in-house teams? Documentation related to internal manufacturing practices were formalized into standards. Many of these started out as based on the internal individual company practice. Two key principles of control were formed, one that the process operation and flow would conform which the OEM needed, and the other pertaining to data collection as proof of correct operation, which doubled as a quality assurance tool, although this latter case is less used than many would believe.

This left EMS companies at the mercy of individual customers, who would insist on their standard being adopted, but each standard was different, creating many different flows and operations that were difficult and costly to implement. Engineers, many of whom were now displaced from their original roles in manufacturing, set out to create more general standards that would introduce uniformity to the industry. These were often based on areas of expertise, so, for example, standards specific to the automotive, aerospace, or medical industries were created. Different standards bodies came into existence for each of the different sectors, each holding, quite rightly in many cases, a different perspective on what requirements the standard should represent. This went some way toward easing the pressure on the communication of requirements between OEM companies and their manufacturing partners. However, many outstanding variations in standards across sectors in the industry remain, and still many proprietary standards survive simply because no general standard can provide a complete description of their requirements.

The role of a standard related to manufacturing should define how the processes are to be set up and executed with appropriate documentation, as well as to describe the capture, storage, and visibility of recorded data. This then involves the adoption and use of sophisticated information technology. Reading current standards makes it seem as though everything was being approached as a manual process, when actually, the description of many items is left quite open to interpretation. While this approach may perhaps be flexible so that no particular method of adoption is mandated, it means that the actions required to satisfy the standard are open to interpretation. Almost inevitably, companies need to create internal specialists who can understand the standards and can clearly explain how the key requirements have been achieved. Often, however, this is outsourced to specialist consultants who provide a service of accreditation, which states that operations within the manufacturing process, record keeping, and data collection are consistent with what the standard mandates. Standards often take many years to become fully understood to the degree that the majority of people using the standard agree on an interpretation.

> **Reading current standards makes it seem as though everything was being approached as a manual process, when actually, the description of many items is left quite open to interpretation.**

Industry bodies make a valiant effort to create the best standards that they can, but really, the standard of the standards from a customer perspective is still quite poor. For example, traceability is often a key component of quality standards across the whole industry. Traceability from different points of view can consist of any combination of material traceability, product tracking, and process recording. Within material traceability, for example, there are issues of what is recorded, how detailed it is, and how accurate it needs to be. Material traceability can mean the tracking of specific materials to a work-order, to a specifically identified PCB within a work-order, or even to a specific component placement on that PCB. Material traceability may include all types of materials, or perhaps only high value or safety critical parts, or only serialized parts. It may include or exclude those parts replaced at repair stations, or the case where an alternative or substitute part has been used, and many more examples where

DON'T ALLOW STANDARDS TO GET THE BETTER OF YOU *continues*

a choice in the depth and breadth of recording is needed. Accuracy is another issue of conflict. Process operational efficiency may conflict with the accuracy with which the traceability data is collected, as for example trays are re-filled without positive poka-yoke confirmation of verification. These are just some typical variations in the level and degree of material traceability.

For product tracking and process data recording, an immense number of other similar decisions have to be made. It is no wonder then that it is difficult to create a single standard that is good for all.

The current trends in manufacturing are set to challenge the standards-based operations that we have today. The Internet of Things, or Internet of Manufacturing as we apply it to PCB electronics manufacturing, introduces two fundamental requirements. The first is that data can be accurately, reliably, and completely aggregated into larger and more generalized data structures, creating so-called "big data." There needs to be some form of compatibility so that meaning and value are not compromised, which is essential where an OEM and its EMS partner are sharing information. The OEM may have several EMS partners to compare, as well as its internal operations. The EMS companies may have many customers and wish to reduce the amount of variation required for each, as well as be able to measure the business performance. Where standards mandate operational documentation and data recording, there needs to be standards in the data itself, with perhaps a simple set of choices as to the extent of depth of reporting, so that all reporting systems will recognize and process appropriately.

The second fundamental requirement for the data is that it can be used in an automated way, such as that inspired by the computerization philosophy of Industry 4.0, where data exchange from automated processes can be applied to the automation of decisions, such as the control of material supply and planning.

> "There needs to be some form of compatibility so that meaning and value are not compromised, which is essential where an OEM and its EMS partner are sharing information."

These different uses for data collected in manufacturing should not need any duplication of data collection from the same processes, it all now needs to be compatible.

There has been significant frustration from the highest levels in the top-tier companies with confusion over standards and definitions of things such as traceability. Often when needed, the required detail and dependability of the traceability data is not as expected. Equally, those in production have the sense that traceability as demanded by standards is adding unnecessary cost to the operation, which frequently for an EMS company becomes a premium service. If there were perhaps one standard of traceability, it could be built into the manufacturing operation without adding any burden, as the best-in-class traceability systems can do today. There is then no cost issue to provide appropriate levels and contents of traceability, and reliability can be assured.

The industry is reaching a point at which the confusion and costs of standards are strangling the progress of things such as the Internet of Manufacturing, which can be easy to understand and applied within a manufacturing operation and shared with the customer. The compelling event is coming from the top level of management of key companies who see the business benefits of a new kind of real standard, and they want to make it a reality. I would invite those leaders and anyone affected by these issues to contact me through this magazine, to put the real situation on the table, whether you agree with what I have written here or not, and then perhaps we will create a compelling event of our own. **SMT**

Michael Ford is senior marketing development manager with Valor Division of Mentor Graphics Corporation. To read past columns, or to contact the author, click here.

SMT QUICK TIPS

Selecting a Reflow Oven, Part 1

by Robert Voigt
DDM NOVASTAR

A reflow oven is simply any device that can liquefy solder in a controlled way to produce an electrical conductive bond between the component and its host (the board). There are several different methods to do this, not all of which can literally be called ovens. For instance, the simplest form of heating is performed by conduction, that is, by contact with a heated surface such as a hot plate. Other heating methods typically performed within a chamber (oven) but that rely on different heating methods include:

1. Convection: Boards with their assembled components are passed through heated, circulating air from a conventional electrical heat source.
2. Infrared (IR): Boards are passed inside a chamber over a direct IR heat source.
3. Vapor Phase: Vapor is generated by heating a fluid with a specific boiling point (240°C) and transfers heat to the circuit board just above the melting point of the solder.

Let's begin with a commonly asked question: What size oven do I need? The answer is also a question: How many zones can you afford?

It seems like an odd way to start a discussion about reflow ovens, but it's not entirely unreasonable. As with any complex process, there will be tradeoffs between cost and capabilities, and more zones will always give you better flexibility and more control over your profile—but at a cost. The decision has to be qualified primarily on your anticipated throughput; that is, how many boards you process in a day or a week.

There are other considerations too, such as board size, component density, and appropriate thermal technology, but we'll talk about those (and more) after identifying the work-flow volume. Following is a guideline (Table 1) for zones relating to typical volume needs.

A typical soldering operation in today's world requires three main stages for temperature profiling: preheat, soak (activate), and reflow, which perform these functions: 1) The preheat stage for a certain period of time to activation temperature; 2) the soak stage for a different period of time to activate the solder; and 3) the reflow stage where temperatures peak for yet a different time frame. After this, the board is typically cooled and removed. Depending on the material, e.g., leaded, lead-free or specialty materials such as epoxies, the heating profile for each stage will vary according to the manufacturer's specifications to achieve optimal bonding.

Board Throughput	Type/Zones	Typical Cost Range
1–5 boards/day	Single or dual hot plate; no zones	$1,000–$2,000
12–15 boards/day	Batch oven, single zone	$2,500–$6,000
100 boards/day**	Conveyorized 3-zone oven	$10,000–$15,000
Over 100 boards/day	No. of zones dependent on speed & target volume	Up to $200,000

** In a typical low- to mid-volume production world, a small conveyorized horizontal convection oven meets most basic requirements.

Table 1.

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SELECTING A REFLOW OVEN, PART 1 *continues*

Figure 1: Dual-stage hot plate.

Conduction

With a hot plate (a direct contact device), it is nearly impossible to achieve three discrete stages with any degree of accuracy, so this technique is recommended only for the hobbyist who makes a couple boards a day and isn't particular about the thermal profile. A dual-stage hot plate can do a little better, because with two digital temperature controls, the user can preset temperatures and manually move the board from one plate to another for specific times to accomplish each stage. However, no hot plate is really a technically professional method.

- Pros: Price
- Cons: Low volume; no profiling ability, thus no reasonable quality control

Convection

Single zone batch ovens can improve quality and speed by virtue of a built-in multi-stage temperature controller. This system is appropriate for the serious hobbyist, budget-conscious customer, or test lab. It works by presetting the temperatures for each stage, placing the board in the oven, closing the lid, and removing it when complete. Adding a single or multi-device shuttle helps to stage one board for loading as soon as the prior board is done and eliminating the need to open the lid. Obviously, this technique is limited by speed but also by size, since batch ovens typically handle boards only up to 8" x 8".

- Pros: Inexpensive; fair controllability for lead and lead-free profiles; small footprint (tabletop); low power consumption
- Cons: Max board size 8"x8"; limited profiling capability due to single heat zone construction; low volume

Multi-zone Ovens

Conveyorized multi-zone ovens, starting with three zones to achieve each stage of preheat, soak and reflow, are the best solution for any type of production volume. They provide complete control of each stage for temperature and timing. Moving via a constant speed conveyor, each board spends just the right amount of time in each stage based on the zone length (or alternately, the number of zones), to achieve the perfect ramp temperature rate for the material profile, board density and geometry.

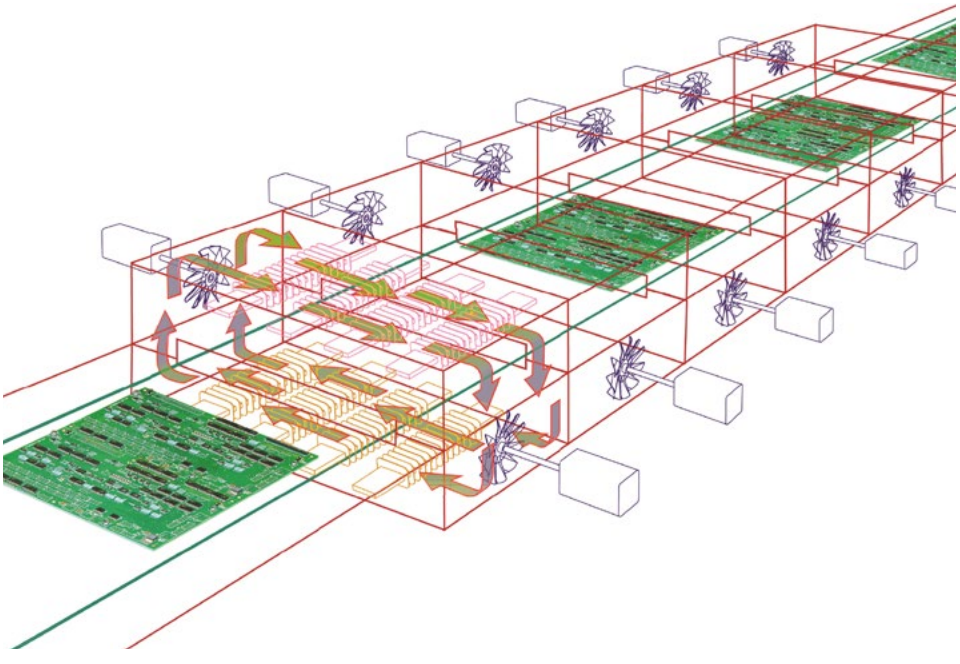


Figure 2: Multi-zone oven with convection heating.

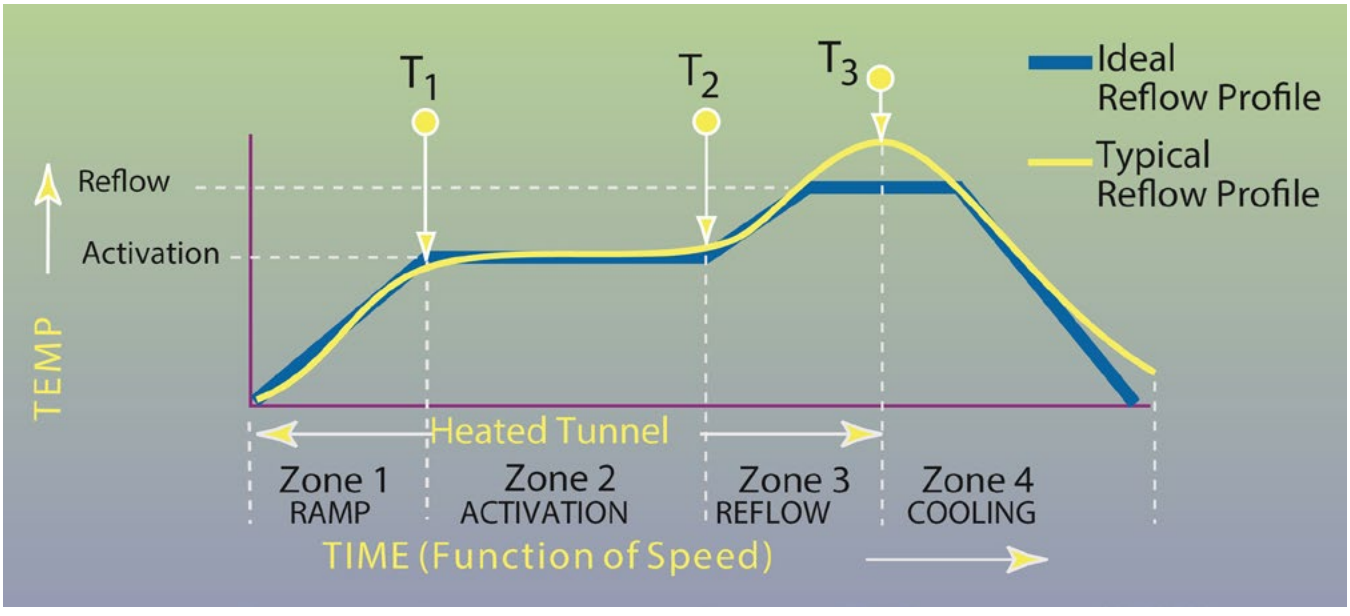


Figure 3: Discrete zone schematic in conveyorized oven.

- Pros: Economical production system f or >100 boards/day; will typically accommodate board sizes up to 12"x12"; offers precise control of ramp temperatures to handle most common leaded and lead-free soldering profiles; can be reconfigured easily to run different board profiles, an important feature for contract manufacturers
- Cons: More expensive than other methods

Now back to the original question: Why is it always a good idea to buy as many zones as you can afford? In other words, when would you need more than three zones in an oven?

The answer is a function of how much flexibility you need in your assembly operation, and that's driven by controllability, volume efficiency, and cost. More zones, along with more length will provide greater flexibility to handle more complex profiles, greater board component densities, and higher speeds (number of boards processed). As a general rule of thumb, ramp temperatures must not exceed 2° to 4°C per second for proper profiling, so more zone flexibility will provide better control.

Larger ovens can also be built with other features such as the ability to handle larger board geometries and special capabilities such as double-sided soldering. For the contract assembly operator who handles a wide variety of products, more zones provide the ability to capture more business that can't be done by competitors with smaller ovens.

Selecting a Reflow Oven Provider

When evaluating proposals from reflow oven vendors, try to find references or reviews before you buy. You can often find them on Internet search, and while not altogether scientific, you may get some clues regarding construction quality or temperature stability that could influence your decision. Some offshore products may look attractive from a pricing perspective, but may not perform to your standards; plus, aftermarket support can be problematic if you need help.

In my next column, we'll address specific heating technologies, conveyors, and software options. **SMT**

Robert Voigt is VP of global sales at DDM Novastar Inc. To reach Voigt, click here.

SMT007 Supplier/New Product Highlights

ESI's Laser Micromachining Platform Delivers Efficient Manufacturing for Consumer Electronics

Electro Scientific Industries Inc. has launched Jade, a low-cost, high-volume-production laser micromachining platform adaptable to a range of configurations for different applications including cutting, marking, drilling and engraving.

ALPHA SBX02 Lowers Assembly Costs by Eliminating Wave Soldering Process

Alpha has developed an innovative low temperature alloy, ALPHA SBX02, which can simplify PCB assembly process by enabling wave soldering to be eliminated.

Nordson EFD Introduces xQR41 MicroDot Needle Valve

Nordson EFD's valve features a 60% smaller form factor than standard valves, an exchangeable modular design for greater customization and process control, and a Quick Release (QR) clasp that allows easy removal of the fluid body to replace wetted parts in seconds.

Dymax's European Subsidiary Celebrates 20 Years of Continuous Growth

Dymax Corporation's European subsidiary, Dymax Europe GmbH, is celebrating its 20th anniversary this year. Based in Wiesbaden Germany, the company offers light-curable adhesives, coatings, and gasketing materials for applications in a variety of markets.

Nordson ASYMTEK Releases New Programmable Tilt + Rotate 5-Axis Fluid Dispenser

Nordson ASYMTEK's Programmable Tilt + Rotate 5-Axis Fluid Dispenser enables the jet to dispense using five axes of automated control instead of only three axes.

Cogiscan Hires Dave Trail as Global Key Account Manager

Cogiscan Inc. is pleased to announce a new addition to its sales team. Dave Trail joins Cogiscan in the position of global key account manager.

Alent Receives $2.3B Acquisition Bid from Platform Specialty Products

Platform Specialty Products offers to acquire all of the issued and outstanding shares of Alent, a global supplier of specialty chemicals and engineered materials used primarily in electronics, automotive and industrial applications, in a cash and stock transaction for approximately $2.1 billion. Including net debt, the total transaction value is approximately $2.3 billion.

Ellsworth Adhesives Europe Now Offers Dow Corning EI-1184

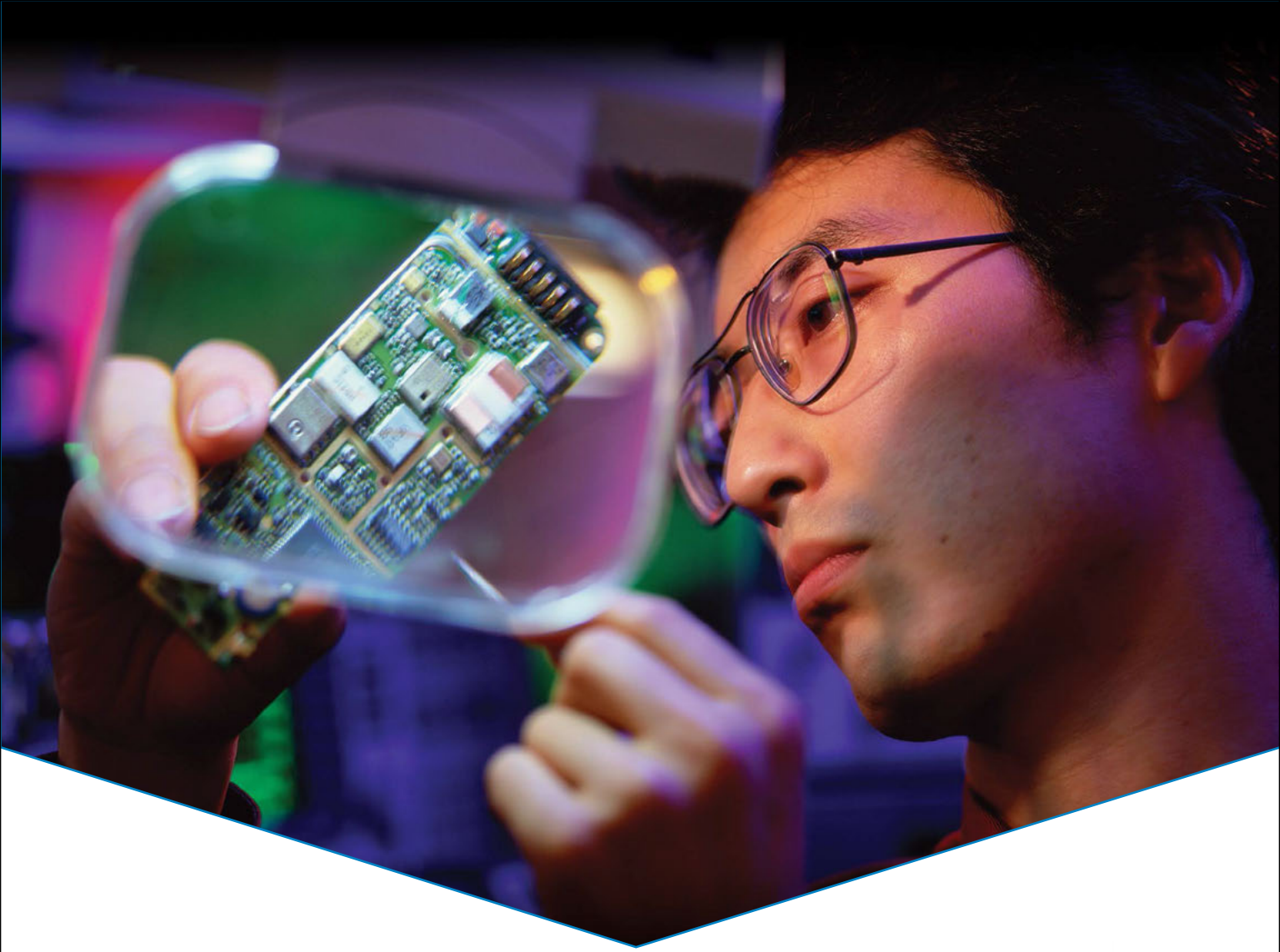
Ellsworth Adhesives Europe, distributor of adhesive materials and dispensing systems, recently enhanced its product line of encapsulants with the addition of Dow Corning EI-1184, a material specially designed for LED lighting applications.

Seika Machinery Now Carries MALCOM RDT-250C Reflow Simulator

Seika Machinery Inc. now carries the MALCOM RDT-250C Reflow Simulator, which can reproduce the temperature profile of a reflow oven while allowing operators to observe the melting state of solder paste and record the process.

Manncorp Installs SMT Assembly Line in Guadalajara

PCB assembly equipment supplier Manncorp has installed an SMT assembly line for Continental Automotive as part of a rapid prototyping laboratory at the Instituto Tecnológico Superior de Zapopan in Guadalajara.



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Dymax Conformal Coatings cure in seconds with UV light – and with ambient moisture curing available for shadowed areas, you can be confident you're getting maximum protection – even underneath components. Add vivid blue fluorescing for easy inspection of coating coverage, and you'll see more throughput, in less time, using less floor space. All with unsurpassed protection against moisture, dust, chemicals, and temperature cycling. And, they're backed by the Dymax Edge… an integrated offering of oligomers, customized adhesives and coatings, cure and dispense equipment, and application expertise that enables Dymax to deliver the best solution to the customer. Visit **dymax.com/smtcoating** to download the new *Guide to Light-Cure Conformal Coatings*.

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Supply Chain Risk Mitigation Applications for the Grey Market

by Stephan Halper
SECURE COMPONENTS

What is an Independent Distributor?

Independent distribution (ID) makes the world go round. Can't find that IC that went obsolete in 1987, an independent distributor can—it's what we are built for. Do you need 20 pieces of a part that is still in production, but not available from your authorized distributor? Call me—I'm a broker; I can find it for you. Wait a minute; are brokers the same as independent distributors? Aren't brokers the reason there are counterfeit components in the supply chain? Do you want to see my line card so you can understand my capabilities? OK, then just type this into your Google search bar: everything.

Here is a message on behalf of the independent distribution industry to anyone involved in supply chain management, whether you are from industry or part of the federal supply chain: It's 2015, and it's time that your supply chain became educated on how to effectively incorporate the benefits that independent distributors and brokers can offer your supply chain, while reducing your risk. It's time that the word "broker" be reevaluated. If your supply chain still looks down on brokers or independent distributors, your supply chain is likely missing opportunities to reduce liability and cost, and increase readiness.

Not convinced? I realize that many readers will disagree with that last statement, which is why I have agreed to write this column. My purpose is to demonstrate each month the common misconceptions that the supply chain has regarding independent distributors and brokers. Rest assured, I will surely include some the horror stories many of you are mumbling under your breath. But I would ask for you to read along, and I would challenge you to open your mind and consider the value that a quality, focused, certified broker or independent distributor can bring, in terms of reducing the risks of introducing a counterfeit component into your supply chain.

So what exactly is the difference between brokers and independent distributors anyway? An independent distributor may (but not always) carry stock. Brokers are generally not in the stocking business, they are the modeled for

SUPPLY CHAIN RISK MITIGATION APPLICATIONS FOR THE GREY MARKET *continues*

just-in-time (JIT) delivery of product. However, what makes them the same when considering the risk they pose to your supply chain is the fact that neither is authorized by the OEM or the OCM of the electronic component or higher assembly you are looking for.

Getting up to Speed

Independent distribution has been part of the supply chain for well over 50 years, and remains a self-regulating industry. Few, if any, industries are invited to support the multi-billion-dollar industries of today, with little to no regulation. The reality is that the grey market is one of the best examples our economy has of true, unregulated capitalism. The scenario of those directly supporting the supply chain with product are also, in many cases, weeding out the bad actors leaving those that comply to an unwritten rule left to service the supply chain. Sound scary? Maybe, but most times the root of fear is due to a lack of understanding, and allowing one's mind to make decisions based off emotion, and not fact. You do not have to be a graduate of the Wharton School to know what happens to a business that makes decisions based on emotions rather than facts.

> "The scenario of those directly supporting the supply chain with product are also, in many cases, weeding out the bad actors leaving those that comply to an unwritten rule left to service the supply chain."

Today, we have a prominent global trade organization—Independent Distributors of Electronics Association (IDEA), and we have an industry supply chain risk mitigation leader in Electronic Resellers Association International (ERAI). There are a handful of other industry resources, but I chose to mention IDEA and ERAI as they are considered the pioneers in bringing a sense of accountability and regulation to an industry in need of both.

Despite the work of these organizations and others in this field (sure to be called out in future articles), it is still up to the individual ID or broker to chart their own course. An ID does not need to be a member of any of the aforementioned organizations, nor are they required to be certified to any industry standards. Regulations are driven by the industries the ID or broker serves. This is an important fact for supply chain managers to understand. As with any industry, not all IDs are created equal. In general, an ID's customer base will use the services of an ID for less than 1% of their total spend. This number fluctuates depending on the industries that make up an ID's customer base, but it is a point worth mentioning, because at the end of the day, this remains a key driver in the decision-making process of an ID, with regard to investment in standards and certifications.

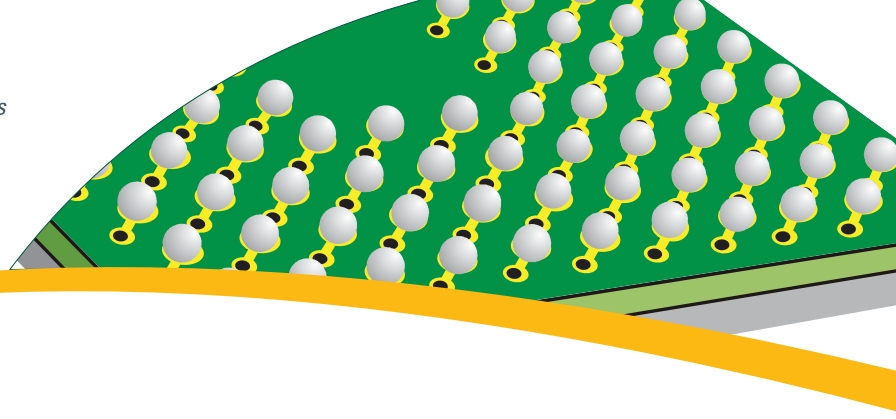
As mentioned earlier, IDs typically enter the supply chain when the authorized distribution channels are unable to support the supply chain's needs. A large population of IDs do not have agreements in place that provide a constant revenue streams for a defined period, which is yet another factor in the ID's decision with to regard the decision to allocate resources towards achieving and implementing industry based standards or government accreditations. This creates supply chain risk mitigation issues not only for the end-user, but also for other IDs, as it impacts the building and monitoring of the ID's AVL, which in turn effects QC flow-downs, etc.

Back to the Present

So where do we go from here? In my next column, I will discuss the government and industry's influence on the independent distributor, as it pertains to tiers of IDs based on the risk to the supply chain, as well as some best practices to incorporate when procuring parts from the grey market. **SMT**

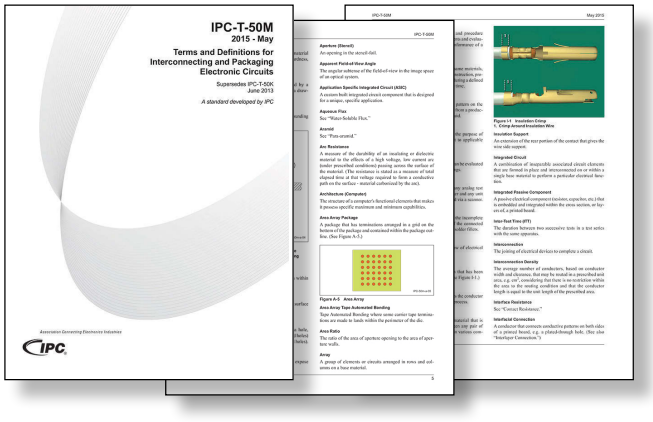
Stephan Halper is the COO and principal of Secure Components. To contact the author, click here.

Association Connecting Electronics Industries



T-50M: Defining the Language of an Industry

What's relevant for today's OEM, EMS or ODM Company?



Each year, a new slew of terms and definitions become common place in the manufacturing process. To meet these needs, T-50 Revision M, *Terms and Definitions for Interconnecting and Packaging Electronic Circuits*, delivers users the most up-to-date descriptions and illustrations of electronic interconnect industry terminology. It is a dynamic standard that adapts to the industry to provide the most thorough dictionary in the industry.

T-50M brings 150 new terms, while eliminating out-of-date terminology in order to provide a streamlined standard that focuses on the trending language of the electronics industry. This revision includes terms often cited in other standards, here is a sneak peek at some of the newly added terms for T-50 Revision M:

- **Backfill (Liquid)**
  The act of sealing the edge of a component with an adhesive or encapsulate to prevent intrusion of liquids or other contaminants.

- **Glob-Topped Encapsulation**
  A localized application of a viscous compound to a printed board assembly, other substrate or component/wire, which is then fully cured to provide mechanical support and environmental protection.

- **Microsection (Mount)**
  The polymer encapsulation of a sample for support during destructive cross-sectional view preparation. Without this support, the sample would be unacceptably deformed by grinding and polishing, such that it could not be examined. It is commonly used for the microscopic examination of printed board features.

Stay up to date with the trending terms covering the newest emerging technologies. Prepare for tomorrow's discussions by downloading T-50M today.

Recent Highlights from SMT007

1 Inspection: The Last Line of Defense

Traditionally a non-value-added step, inspection is still the best, last line of defense against defects and a bad reputation. In this interview by I-Connect007 Publisher Barry Matties, Viscom's Guido Bornemann discusses the true value of inspection and how to best use the tools to prevent defects, including head-in-pillow, from being shipped to customers.

2 Taking the Human Out of Hand Soldering: Is it a Must?

At the recent NEPCON Show in Shanghai, I-Connect007 Publisher Barry Matties stopped by the WKK booth where Japan Unix (represented by WKK in China) was displaying its new robotic soldering technology. In this interview, General Manager Hirofumi Kono explains why this new technology makes so much sense.

3 Parylene and Wearable Devices

The life of a wearable device is harder than it might seem. It could be exposed to summer in Phoenix or winter in Minneapolis. It also gets exposed to corrosive spray when it is taken to the beach or on a boat. Considering such challenges, this article talks about why Parylene is the most appropriate choice for conformal coating compounds when it comes to protecting wearable devices.

4 Reliability Study of Bottom Terminated Components

This article series discusses bottom terminated components (BTC), and the stress and strain on these components when it comes to solder joints. In Part 1, the authors look at the impact of large voids at the thermal pads of BTC components and their impact on solder joint reliability.

5 A Review of the Opportunities and Processes for Printed Electronics

As microsystems continue to move towards higher speed and microminiaturization, the demands for interconnection are opening up new opportunities for "innovative" interconnects. In the first part of this five-part article series, Happy Holden gives a brief background on printed electronics, as well as presents key technologies that are being employed for PE production.

6 Rise in Global PCB Production Drives SMT Equipment Market

Driven by the strong demand for electronic products and the ensuing increase in production of PCBs, the global market for surface mount technology equipment is projected to reach $4.5 billion by 2020, according to GIA.

7 Saline Lectronics Installs Seica's Pilot 4D V8 Flying Probe Tester

Saline Lectronics Inc. has purchased and installed a Seica Pilot 4D V8 flying probe tester, further enhancing its testing capabilities to better support each of its clients' unique testing requirements.

8 Checksum President Discusses Developments in Board Testing

Checksum President John Van Newkirk talks with I-Connect007 about his company's activities, how board testing has evolved over the past decades, and what the future of test will look like.

9 Navitas Expands Manufacturing Capabilities

Over the last couple months alone, Navitas Electronics has invested in new equipment, including a Panasonic CM Series pick-n-place machine, Glenbrook X-ray machines, ERSA automated BGA repair stations and full solder repair stations, PVA automated conformal coating machines and various other equipment.

10 Bittele Electronics Completes New PCB Assembly Line

Bittele Electronics has completed the construction of a new, fully automated PCB assembly production line featuring state-of-the-art technology, for prototype and low-volume assembly.

EVENTS

For the IPC's Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar, click here.

For a complete listing, check out *SMT Magazine's* full events calendar here.

7th Annual SMTA Vendor Show
August 21, 2015
Penang, Malaysia

NEPCON South China 2015
August 25–27, 2015
Shenzhen, China

Capital Expo & Tech Forum
September 1, 2015
Laurel, Maryland, USA

electronica India
September 9–11, 2015
New Delhi, India

productronica India
September 9–11, 2015
New Delhi, India

Medical Electronics Symposium 2015
September 16–17, 2015
Portland, Oregon, USA

SMTA International 2015
September 27–October 1, 2015
Rosemont, Illinois, USA

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OCTOBER:
Cycle Time Reduction

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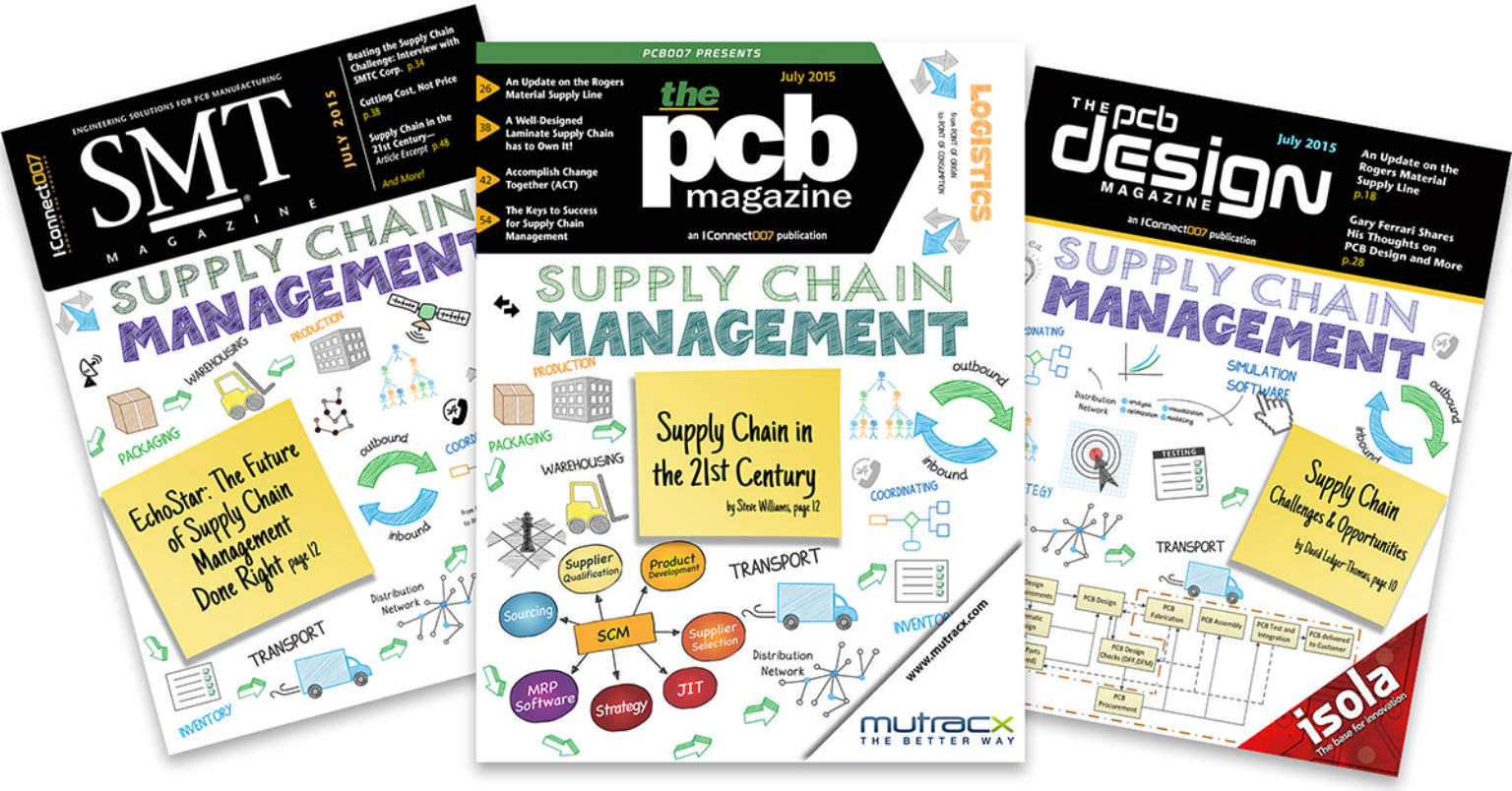

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