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National Electronics Week

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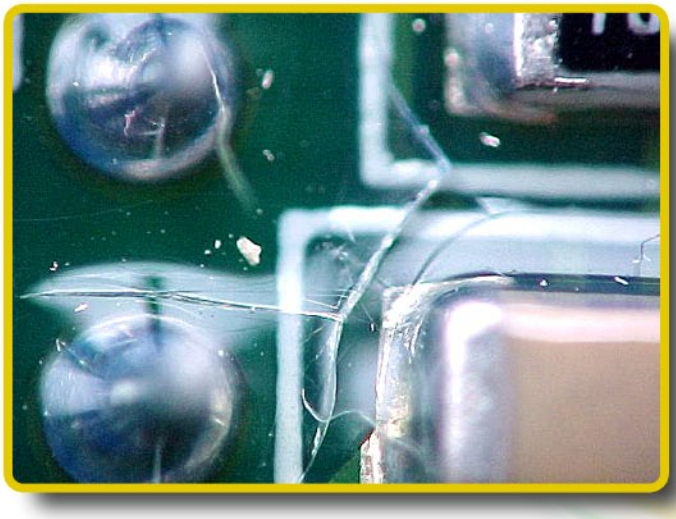
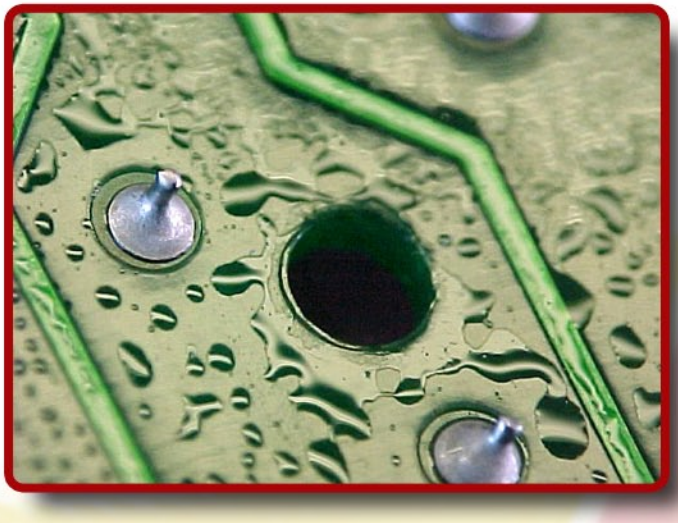
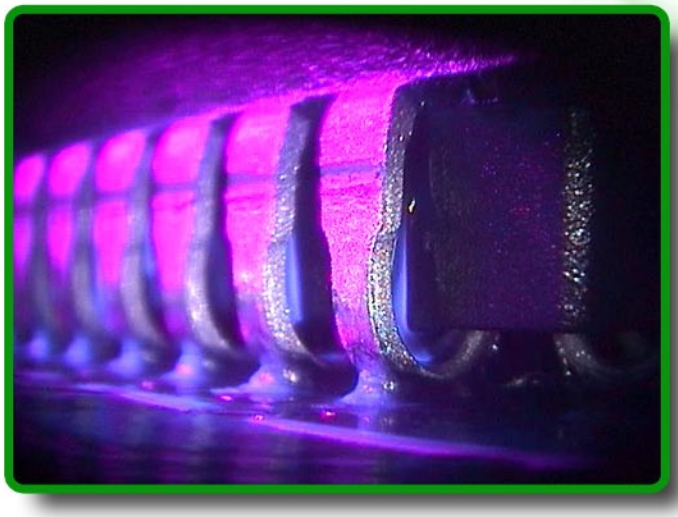
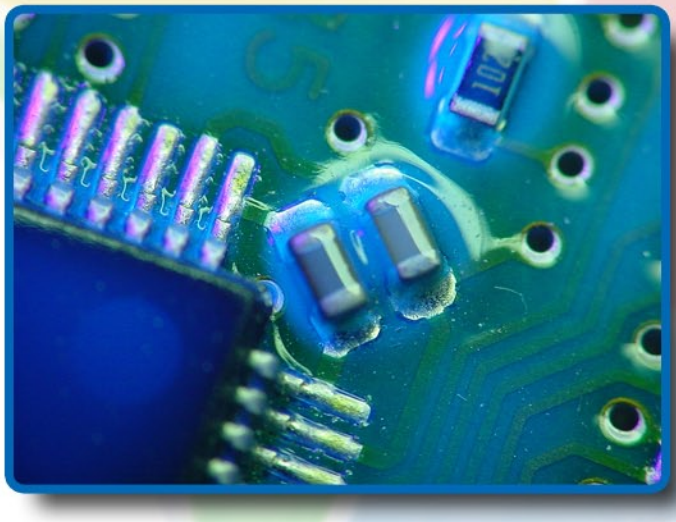
Conformal Coating and Cleaning Experience









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February 2014 Featured Content

SMT ASSEMBLY, PART 1

This month, Shea Engineering Services and Vicor team up for our cover feature, and join industry experts from Universal Instruments Corp., Nordson ASYMTEK, and DEK, for SMT Assembly, Part 1—Preparation for Soldering: Paste Printing and Component Placement.

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FEBRUARY 2014
VOLUME 29
NUMBER 2
www.smtmagazine.com

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AN I·CONNECT007 PUBLICATION

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THE WAY I SEE IT

IPC Forms a PAC

by Ray Rasmussen
PUBLISHER, I-CONNECT007

IPC just announced they're forming a political action committee. Here's their reasoning for creating a PAC:

Political action committees (PACs) have become an important tool for any group that wants to be heard when laws and regulations are written. Given the growing number of government regulations that influence the electronics supply chain, having clout in Washington, D.C. is something that can no longer be ignored. As a result, IPC's Board of Directors has decided to join the many trade associations and large companies that have established PACs.

I have reservations about IPC's new direction in D.C. There's some history.

In the early '90s, I was a huge supporter of prodding the industry to be more active in local and national government. Rules and regulations were constantly being developed without any input from our industries. The onslaught of environmental regulations coming from the EPA, the state regulators, and local municipalities left the industry frustrated and seemingly powerless. Something had to be done and the logical approach was for our national association, IPC, to take the lead. They had the industry clout to present the issues to the regulators or those in the Congress who would listen. They could tell the story and make the case for or against specific requirements. When approached, IPC's position was that they were a standards organization, and that lobbying and politics wasn't their game. That stance changed as pressure mounted and newer, more open-minded board members began to see the importance of telling our story and having a seat at the table when new requirements on our industries were being proposed. Most in Congress, we found out, had no idea who we were or what we did. They didn't know the role we played in everything electronic. They only knew of the big guys. And in their minds, anything to do with the electronics industry was "big business."

As we began to get more involved in the political and regulatory processes, we learned that we had a distinct advantage over our much larger, political action committee-holding, big electronics brethren. They all had their PACs and lobbyists, but we had something special that they didn't: a geographically diverse membership made up of small, independent businesses.

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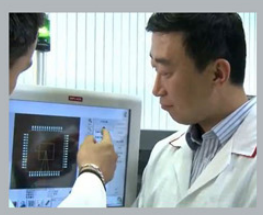

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IPC FORMS A PAC *continues*

The members of Congress loved that and almost always welcomed our letters or our phone calls as well as our visits during Capitol Hill Days. In fact, there were a few larger organizations with common interests around certain rules or up-coming legislation, which lent their support but let IPC take the lead precisely because of the makeup of our industries.

Back then, IPC hired the lobbying firm Wayne Sayer and Associates to represent the industry in Washington. Sayer's team would present our position regarding regulations and review new legislation affecting the industry. They also organized the Capitol Hill Day events, which included lobbying training, preparation for visits with our representatives as well as the specific issue we'd be presenting during the visits to the Hill. Each member had meetings with their representatives in the House and Senate. It was quite enlightening to most of us who'd never done anything like this before. I would encourage everyone in the industry to support the next Capitol Hill Day event. It's quite an experience.

Within a few years, IPC realized they needed their own people on the ground in D.C., which began a new era as we became directly involved in the policy-making. We had a seat at just about every table. Most in Congress knew who we were, what we were about and, more importantly, who we represented. In fact, by then, our industry's companies had invited quite a few of their representatives to tour their factories. Now, when we had an issue with a regulation or piece of legislation, we had the ear of Congress. In fact, one of our member companies, South Dakota-based Electronics Systems Inc. and its CEO, Leo Reynolds, forged a strong relationship with then-Senate Majority Leader Tom Daschle of South Dakota, which brought our issues to the forefront. We gained a lot of ground back then.

Since the mid-'90s, the industry has done a lot to stay active in governmental processes. It's hard to quantify the dollars associated with our inaction in the '80s and '90s, but we did miss the boat with NAFTA and lead-free legislation. Not having a seat at the table for those two issues alone has certainly cost the industry dearly. Of course, RoHS wasn't a U.S. initiative, but IPC definitely should have been at the table. We might have been able to steer the ship a bit. I wonder what would have happened if IPC, along with the other electronics associations, had leveraged their clout in Congress and had just said "no." I know what happened with NAFTA. We didn't have the systems in place to be able to address our concerns to the government back then. They asked, but received no input from us. Regarding lead-free, we were just asleep at the switch.

On the positive side, IPC's efforts in support of equipment depreciation along with minor tweaks in regulations and legislation have saved the industry quite a bit over the years. As an active industry player, IPC has certainly upped our stature and has been able to influence at least some of the things coming our way. Before the mid-'90s we had no voice. And maybe that's what IPC's founding fathers originally wanted—to stay under the radar, focusing on standards. Back then we were dumping most of our waste down the drain or, in the case of a few really bad actors, into creeks behind our factories.

For me, a PAC has a negative connotation. It's buying votes instead of leveraging the grassroots power we have as an industry. It cheapens us. Now, instead of being an industry of small businesses (which we mostly are), we push that aside in the minds of our representatives and regulators and join the likes of IBM, Dell, Cisco and Google (Motorola), the AEA and SIA. It seems to me a better course of action would be to encourage our member companies to donate to their representatives based on IPC recommendations, but keep the IPC out of PACs so that it can remain "pure," without "blemish."

Couldn't we take that PAC money and use it to strengthen our team in D.C. instead? What would bring the greatest return?

Let me know what you think. **SMT**

Ray Rasmussen is the publisher and chief editor for I-Connect007 Publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuiTree Magazine.* To read past columns, or to contact Rasmussen, click here.

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Stencil Image Courtesy of Photo Stencil.

Fine-Tuning the Stencil Manufacturing Process & Other Stencil Printing Experiments

by Chrys Shea
SHEA ENGINEERING SERVICES
and Ray Whittier
VICOR CORP.

Abstract

Previous experimentation on a highly miniaturized and densely populated SMT assembly revealed the optimum stencil alloy and flux-repellent coating for its stencil printing process. Production implementation of the materials that were identified in the study resulted in approximately 5% print yield improvement across all assemblies throughout the operation, validating the results of the initial tests.

A new set of studies was launched to focus on the materials themselves, with the purpose of optimizing their performance on the assembly line. Using a similar test vehicle as the prior experiments, DOEs characterized key aspects of the stencil manufacturing process by varying the laser cutting parameters and coating materials. As the scope of the DOE grew, it also included evaluation of new materials and a comparison of microBGA aperture designs. Eventually, additional runs were added to investigate the effects of nanocoating on wipe frequency and compare two different stencil cutting processes.

Results of the prior tests are reviewed, and the new test vehicle, experimental setup and results are presented and discussed.

Introduction

This study builds upon the results of a previous investigation that identified the best stencil

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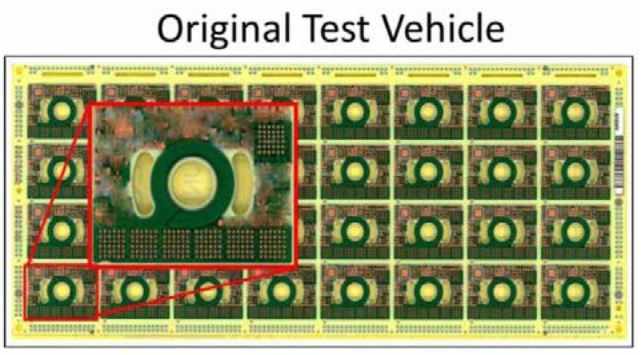

Figure 1: Test vehicle used in previous tests (non-BGA circuitry on closeup is intentionally blurred).

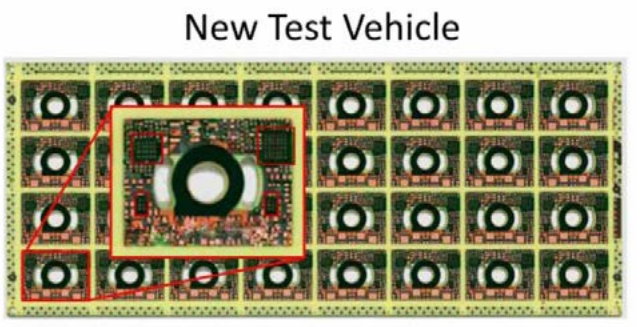

Figure 2: New test vehicle.

technology for the production of a high-density, highly miniaturized PCB assembly[1]. The test vehicle used in that study is shown in Figure 1.

The PCB design packed nearly 15,000 paste deposits in a 3x7 area; 8,500 of those were 0.5 mm microBGAs. The study used print yields, transfer efficiencies, and print volume consistency as metrics to evaluate a number of stencil technologies, including electroformed nickel stencils, electroformed nickel that had been laser cut, and two different types of laser-cut stress relieved stainless steel (SS). The study concluded that the best print quality was produced with laser-cut fine grain (FG) SS foils with two-part Self-Assembling Monolayer Phosphonate (SAMP) nanocoating applied.

With the key materials identified, a new study was launched to optimize the laser cutting parameters on the FG SS. It tested three experimental parameter sets against the process of record (POR). Prior to the outset of the tests, a new two-part SAMP nanocoating was introduced to the market, so additional tests were planned to benchmark the new generation of nanocoating against the original one.

In response to recent reports that cite square apertures as superior to circular ones on fine features[2], a leg was added to the DOE that directly compared the two.

As the time to execute the experiments approached, new experimental SS foil materials were introduced, as was a new electroforming process, so another leg was added to analyze their performance. During the execution of the tests, two additional runs were added to begin understanding the relationship between nanocoating and stencil under wipe frequency.

Upon review of the results, a final run was added to benchmark the performance of a different laser stencil cutting process.

All the tests were executed in a similar fashion, using the same ten-print test and the same metrics for analysis. Detailed information on the derivation of the area ratio, transfer efficiency and coefficient of variation metrics used in this study is provided in the original report, cites as reference #1.

Experimental Setup

Test Vehicle

The original test vehicle shown in Figure 1 was used for a multitude of comparative tests over a two-year span. It is a production PCB that offers vast amounts of comparative data. The design was recently revised; the new test vehicle used in this evaluation is shown in Figure 2.

This new design replaced some of the microBGAs with FETs, reducing the number of BGA I/Os from 8500 to 2176 per board. The number of 0201s increased on this design, from 1900 deposits per print to 3712. A 10-print test using the new TV now produces 21,760 BGA data points and 37,120 0201 data points.

Test Methods

For each stencil, 10 prints were produced sequentially on a well maintained and calibrated 2009 DEK horizon stencil printer using,

Experiment #1 Compare Cutting Parameters on FG SS	
Stencil #	**Description**
1	POR with Nano1
1a	POR w/o Nano
2	Param Set 1 with Nano1
2a	Param Set 1 w/o Nano
3	Param Set 2 with Nano1
3a	Param Set 2 w/o Nano
4	Param Set 3 with Nano1
4a	Param Set 3 w/o Nano

Table 1: Laser cutting parameter experiment.

Experiment #2 Compare Materials	
Stencil #	**Description**
5	POR FG with Nano1
5a	POR FG with Nano2
6	Exp Eform with Nano1
6a	Exp Eform with Nano2
6b	Exp Eform w/o Nano
8	Exp SS with Nano2
8a	Exp SS w/o Nano

Table 2: New stencil materials experiment.

Experiment #3 0.5mm BGA Aperture Geometry	
Stencil #	**Description**
7	Round - POR FG with Nano1
7b	Square -POR FG with Nano1

Table 3: MicroBGA aperture shape experiment.

Additional Runs 10 Prints with No Under Wipe	
Stencil #	**Description**
5a	POR FG with Nano2
7	POR FG with Nano1

Table 4: Under wipe experiment.

both front-to-back and back-to-front squeegee strokes, with an automatic dry wipe after each print. Print parameters were:

- Print speed: 7 mm/sec
- Print pressure: 8 kg (250 mm blades)
- Separation speed: 20 mm/sec
- Wipe sequence vacuum/dry/vacuum

The solder paste used in all tests was Indium 3.2 HF Type 3, water soluble, lead-free, halogen-free, lot numbers PS52867 and PS54561. Fresh paste was used on each stencil. The paste was not kneaded; two dummy prints were produced before measurements were taken. The 17 stencils were print tested in a climate controlled NPI manufacturing area over 9 different runs. During the tests the room temperature ranged from 22.0–25.3°C, and relative humidity ranged from 36.3–42.9%.

The PCB was supported with a flat, non-vacuum tooling plate and edge clamps. Deposit volume measurements were taken with a Koh Young 3020VAL using a Bare Board Teach to set the reference plane.

Test Matrices

All the experimental stencils were produced by the same supplier. Their thickness was specified at 4 mil. The laser cut stencils were all produced on the same cutter within a two-week period. The first-generation nano-coating, Nano1, (DEK NanoProTek) was applied to the specified stencils at the supplier's site; second-generation coating, Nano2, (Aculon NanoClear) was applied at the test site. The designs of the individual experiments are listed in Tables 1–4.

Results

Aperture Measurements

To calculate actual transfer efficiencies and area ratios, the stencils' apertures and thick-

nesses were measured. Their specifications are as follows:

- Circular microBGA apertures: 10.8 mil
- Square microBGA apertures: 10.8 mil
- Rectangular 0201 apertures: 11.8 x 13.8 mil
- Foil thickness: 4 mil

The apertures were measured on the PCB side with a Microvue automated vision system; 32 of each aperture size were measured per stencil. Round apertures all measured to within 0.5 mil of their specification; square or rectangular ones measured within 0.7 mil of their specification. Foil thickness were consistent at 4.0 mil on the SS due to its precision manufacturing process and averaged 3.9–4.0 mil on the electroformed stencils. The average measurements are reported in Table 5.

The measurements were used to calculate the actual aperture volumes and area ratios shown in Table 6.

Stencil #	Device	Dia. or X (mils)	Y (mils)
1	BGA	10.4	
	0201	13.1	11.3
2	BGA	10.8	
	0201	13.5	11.6
3	BGA	10.4	
	0201	13.1	11.2
4	BGA	10.5	
	0201	13.2	11.2
5	BGA	10.5	
	0201	13.2	11.2
6	BGA	10.5	
	0201	13.2	11.3
7	BGA	10.4	
	0201	13.1	11.2
8	BGA	10.5	
	0201	13.2	11.3
1A	BGA	10.4	
	0201	13.1	11.2
2A	BGA	10.8	
	0201	13.5	11.6
3A	BGA	10.4	
	0201	13.1	11.2
4A	BGA	10.4	
	0201	13.1	11.2
5A	BGA	10.5	
	0201	13.2	11.2
6A	BGA	10.4	
	0201	13.1	11.3
6B	BGA	10.4	
	0201	13.2	11.3
7A	SQBGA	10.2	10.1
	0201	13.1	11.2
8A	BGA	10.4	
	0201	13.2	11.3

Table 5: Average aperture measurements.

Stencil #	Device Type	Volume (cu mil)	Area Ratio
1	BGA	337	0.65
	0201	592	0.76
2	BGA	366	0.67
	0201	627	0.78
3	BGA	342	0.65
	0201	590	0.76
4	BGA	344	0.65
	0201	593	0.76
5	BGA	344	0.65
	0201	593	0.76
6	BGA	343	0.65
	0201	595	0.76
7	BGA	337	0.65
	0201	587	0.75
8	BGA	346	0.66
	0201	599	0.76
1A	BGA	342	0.65
	0201	589	0.76
2A	BGA	365	0.67
	0201	627	0.78
3A	BGA	341	0.65
	0201	589	0.76
4A	BGA	341	0.65
	0201	586	0.75
5A	BGA	343	0.65
	0201	593	0.76
6A	BGA	341	0.65
	0201	592	0.76
6B	BGA	340	0.65
	0201	594	0.76
7A	SQBGA	410	0.63
	0201	589	0.76
8A	BGA	340	0.65
	0201	595	0.76

Table 6: Aperture volumes and area ratios for test stencils.

Paste Volume Measurements & Print Yields

The paste volume information and print yields resulting from the 10-print tests are shown in Tables 7–9.

SPI databases were also queried for the microBGAs average positional offset in X and Y. The results are shown in Table 10.

Analysis

Experiment #1: Effect of Cutting Parameters and Nanocoating

1) Print Yields

Print yields are determined by the automatic solder paste inspection system. All 9472 depos-

Aperture	Stencil	Mean	Std dev	CV	YIELD
BGAs	1	344	31	9%	80%
	1A	273	31	11%	60%
	2	306	30	10%	80%
	2A	306	34	11%	70%
	3	273	35	13%	90%
	3A	302	43	14%	70%
	4	313	50	16%	0%
	4A	289	42	15%	60%
	5	285	41	14%	80%
	5A	278	34	12%	80%
	5A-No Wipe	288	31	11%	90%
	6	282	33	12%	60%
	6A	295	32	11%	100%
	6B	307	42	14%	70%
	7	279	44	16%	70%
	S7-No Wipe	297	35	12%	100%
	7A	358	41	11%	70%
	8	298	34	11%	100%
	8A	311	37	12%	90%

Table 7: Measured print volume results for microBGAs and print yields.

Aperture	Stencil	Mean	Std dev	CV	YIELD
0201s at 0 degrees	1	717	67	9%	80%
	1A	632	71	11%	60%
	2	618	65	11%	80%
	2A	635	77	12%	70%
	3	582	69	12%	90%
	3A	611	82	14%	70%
	4	631	93	15%	0%
	4A	597	88	15%	60%
	5	589	84	14%	80%
	5A	584	67	11%	80%
	5A-No Wipe	593	61	10%	90%
	6	579	77	13%	60%
	6A	606	68	11%	100%
	6B	604	77	13%	70%
	7	586	90	15%	70%
	S7-No Wipe	600	66	11%	100%
	7A	603	72	12%	70%
	8	609	66	11%	100%
	8A	631	72	11%	90%

Table 8: Measured print volume results for 0201s at 0 degree orientation and print yields.

Aperture	Stencil	Mean	Std dev	CV	YIELD
0201s at 90 degrees	1	694	63	9%	80%
	1A	608	67	11%	60%
	2	595	64	11%	80%
	2A	611	75	12%	70%
	3	564	66	12%	90%
	3A	591	81	14%	70%
	4	608	95	16%	0%
	4A	579	86	15%	60%
	5	567	80	14%	80%
	5A	562	63	11%	80%
	5A-No Wipe	571	59	10%	90%
	6	551	79	14%	60%
	6A	583	70	12%	100%
	6B	591	79	13%	70%
	7	569	86	15%	70%
	S7-No Wipe	582	64	11%	100%
	7A	580	70	12%	70%
	8	590	64	11%	100%
	8A	612	72	12%	90%

Table 9: Measured print volume results for 0201s at 00 degree orientation and print yields.

Postional Offsets		
Stencil	X(mils)	Y(mils)
1	0.44	-0.41
1a	0.46	0.39
2	0.09	0.67
2a	0.52	0.14
3	0.44	0.35
3a	0.52	0.60
4	0.60	0.66
4a	0.53	0.69
5	0.48	0.71
5a	0.57	0.37
6	0.69	0.95
6a	0.37	0.88
6b	0.58	0.86
7	0.40	0.63
7a	0.47	0.41
8	0.48	0.53
8a	0.55	0.40
PRODUCTION	0.41	0.00

Table 10: Average positional offset of microBGA prints.

FINE-TUNING THE STENCIL MANUFACTURING PROCESS *continues*

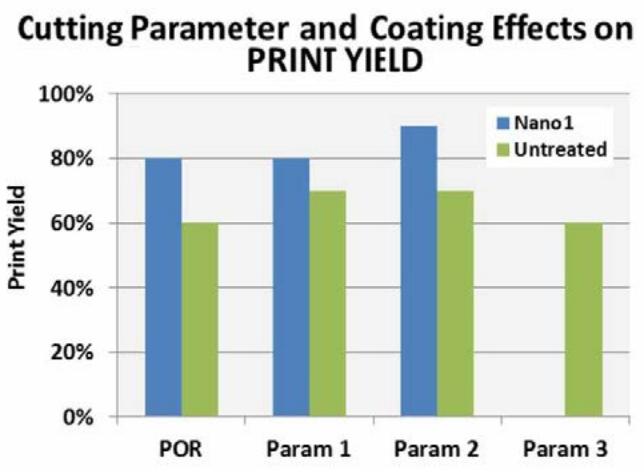

Figure 3: Effect of cutting parameters and nano-coating treatment on print yields.

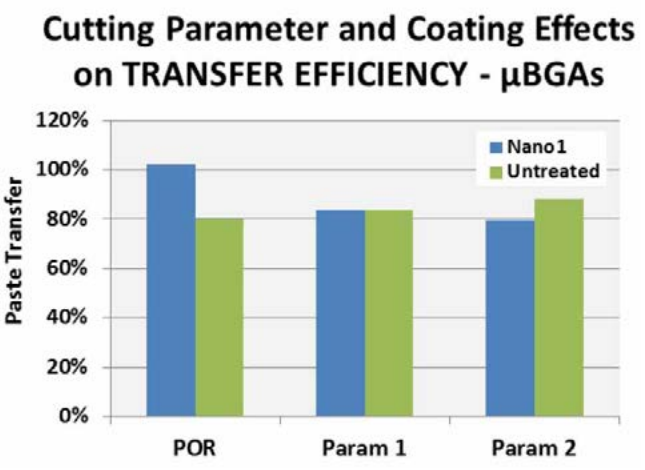

Figure 5: Effect of cutting parameters and coating on transfer efficiency. The higher the TE, the better.

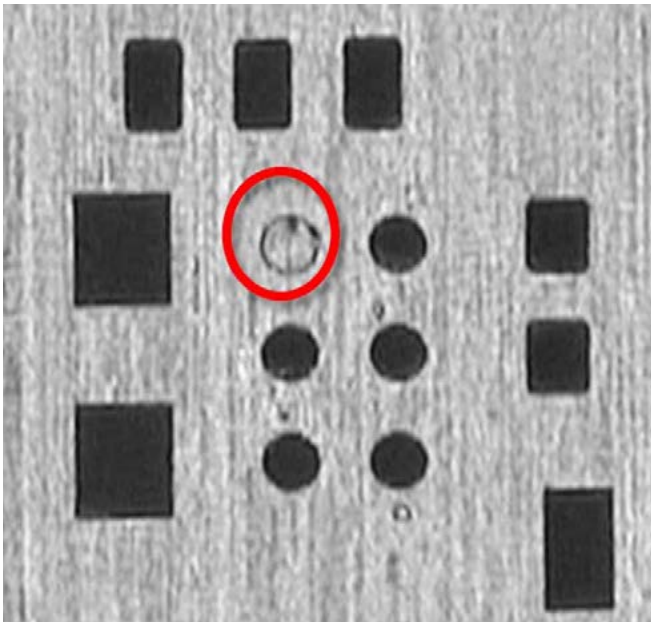

Figure 4: Miscut stencil aperture on stencil 4.

its must fall within their specified ranges for the print to be considered a pass. As little as one deposit out-of-spec will cause the print to be a fail.

The print yields are show in Figure 3. With the exception of parameter set 3, the treated stencils yielded 10–20% better than the untreated ones. Additionally, parameter set 2 produced the highest yields. The treated stencil in parameter set 3 yielded 0% due to a miscut aperture (Figure 4).

2) Transfer Efficiency

Transfer efficiencies (TE) are the ratio of the volume of the measured deposit to the volume of the stencil aperture and are expressed as a percent, or, more simply put, the percentage of solder paste that releases from the aperture. The aperture volumes used in the calculations are computed based on the average measured aperture dimension and stencil thickness, not on their specifications.

The data from parameter set 3 were not included in transfer efficiency or repeatability comparisons due to the miscut aperture.

Most of the stencils transferred about 80% for BGAs (Figure 5) and 100% for 0201s. Figure 6 shows the TE results for 0201s oriented at 0 degrees; similar results were found at 90° orientation (not shown). No significant difference in transfer efficiency was noted with the different cutting parameters, with the exception of the POR sample. The treated stencil that was cut at the POR parameters appears to have 100% TE for the BGAs and 120% for the 0201s. Years of baseline data indicate mean TEs of approximately 80% and 100% for the two device types, respectively. At the BGA's 0.65 area ratio, 100% TE is not realistic; neither is 120% for the 0201s. Therefore, special causes of the anomalous data were investigated.

Positional inaccuracy, the most likely possible cause of excess solder volumes, was in-

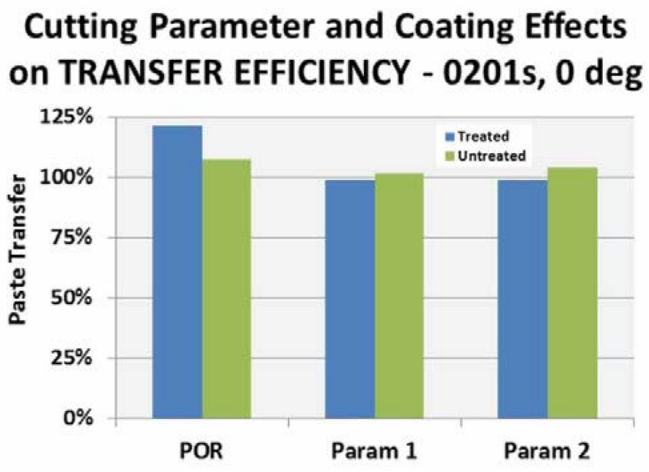

Figure 6: Effect of cutting parameters and coating on transfer efficiency of 0201s oriented at 0°.

vestigated first. The positional accuracy was found to be within 0.5 mil in both X and Y directions, so it was ruled out as a root cause. The investigation then turned to the bottom of the stencil, where numerous topographical features were observed (Figure 7). Small bits of metal fused to the bottom of the stencil appear to have separated the stencil from the PCB, preventing good gasketing. The origin of these features is unknown. Closer inspection of stencil 4 indicates that similar features may be a contributor to the miscut aperture (Figure 4).

3) Volume Repeatability

Print volume repeatability is measured by dividing the standard deviation of the print volume readings by the mean of the readings, and is also known as the coefficient of variation. It is expressed here as a percentage. The effect of the cutting parameters and coatings on volume repeatability is shown in Figure 8.

Parameter set 2, which offered highest yields in this test, also produced the highest variation, which is undesirable. Historical data indicates CVs of approximately 10%, which is the benchmark for the BGA device. Interestingly, the CV for stencil 1, the one with the metal projections on the bottom side, was the lowest of the test and slightly lower than the benchmark. The CVs for the 0201s were nearly identical to those

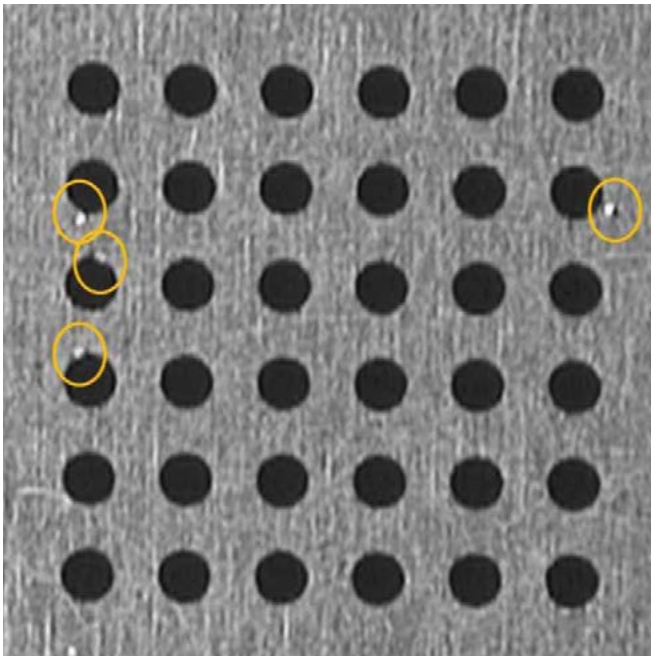

Figure 7: Topographical features found on the PCB side of stencil 1.

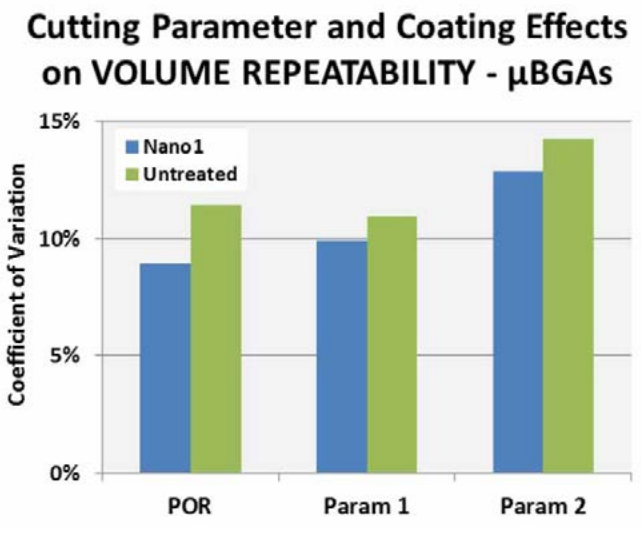

Figure 8: Effect of cutting parameters and coating on print volume variation. The lower the CV, the better.

of the BGAs and are not shown. Regardless of cutting parameters, stencils treated with nanocoating consistently provided better print volume repeatability than those without.

Experiment #2: New Stencil Materials

1) Print Yields

The FG SS with both the first- and second-generation nanocoatings produced 80% yield. The experimental SS without nanocoating produced 90% print yield, and with the new-generation nanocoating produced a 100% print yield. The experimental electroform (EF) stencil with the new nanocoating also produced 100% print yield, but the experimental EF stencils with first-generation or no nanocoating only produced 60 and 70% yields, respectively. Print yields for the different materials and coating are compared in Figure 9.

2) Transfer Efficiency

All stencils tested transferred at least 80% on the microBGAs and close to 100% on the 0201s. Figure 10 shows the microBGA results. The experimental SS and EF stencils without any nanocoating at all transferred 91 and 92% respectively, approximately 10% higher than the production process. The same materials with second-generation nanocoating released more than 86%, a less substantial yet noteworthy 5% increase from the benchmark. The other stencils performed in the expected 81–83% range.

The TE of the 0201s hovered around 100%, with the untreated experimental materials showing the highest release, and the treated materials showing the second highest. The trend shown in Figure 11 is identical to that of the microBGAs. Another repetitive trend observed in all print tests is the slightly higher TE (3–6%) for components oriented at 0° versus those oriented at 90%.

3) Variation

The lowest CV for the microBGAs was on the experimental EF stencil coated with second-generation nanocoating, at 10.8%. The next lowest was the experimental SS with the second-generation nanocoating (Figure12) at 11.4%. This trend is again observed in the 0201 CV data, but transposed, with the Nano2 experimental SS at 10.9% and the Nano2 experimental EF at 11.3% (Figure 13). The remainder of the stencils all produced higher variation.

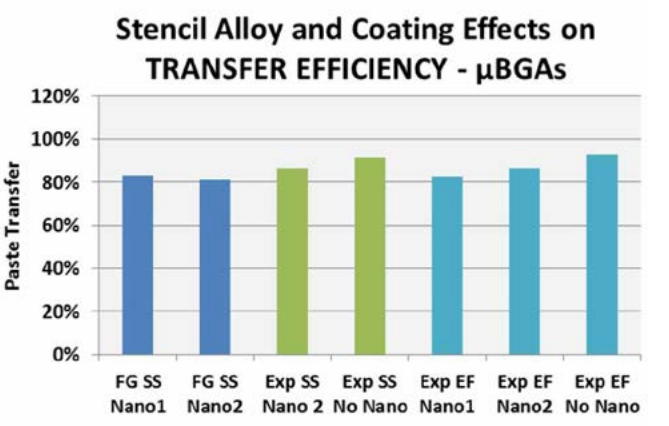

Figure 10: Effects of stencil alloy and coating on BGA transfer efficiency.

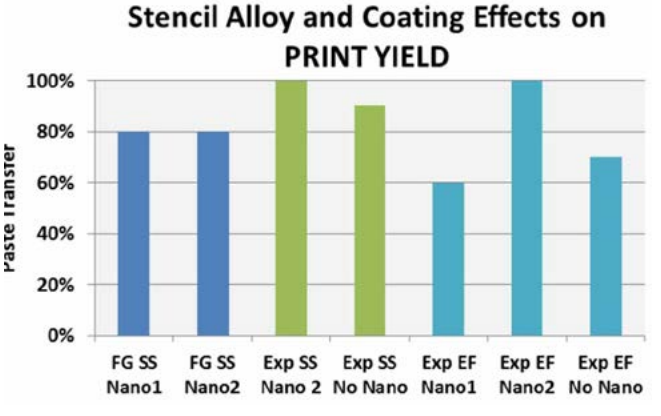

Figure 9: Effects of stencil alloy and coating on print yields.

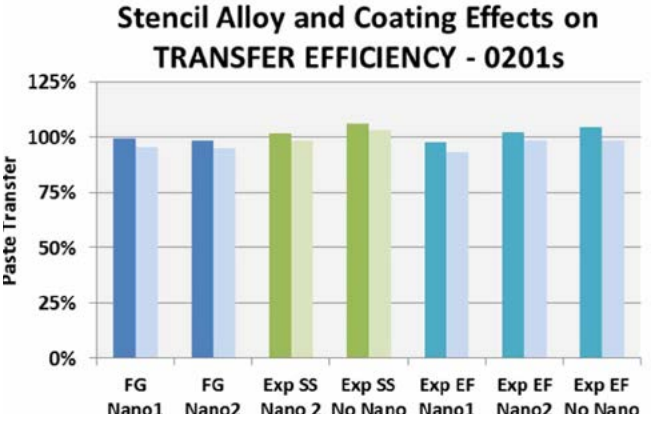

Figure 11: Effects of stencil alloy, coating and component orientation on 0201 transfer efficiency.

Experiment #3: microBGA Aperture Shape

To compare the influence of microBGA aperture shapes on print quality, two stencils were produced with identical aperture geometries for all devices except the BGAs. One stencil had specified 10.8 mil circles; the other specified 10.8 mil squares with radiused corners.

1) Print Yields

Print yields for both stencils were 70%. They are not depicted graphically.

2) Transfer Efficiency

Figure 14 shows the transfer efficiency for both aperture shapes. The square aperture has a higher percentage of paste transfer; it also has a higher volume of paste due to its geometry. The average paste volume deposited from the square aperture is approximately 358mil^3, whereas the average paste volume deposited by the round apertures was 298mil^3. The square aperture deposits an average of 22% more solder paste than the round one.

3) Variation

The square aperture design also provided better print volume consistency than the round design, as shown in Figure 15.

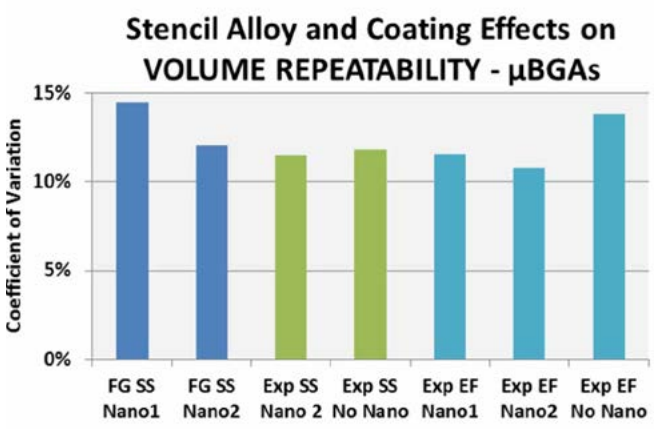

Figure 12: Effects of stencil alloy and coating on BGA volume repeatability.

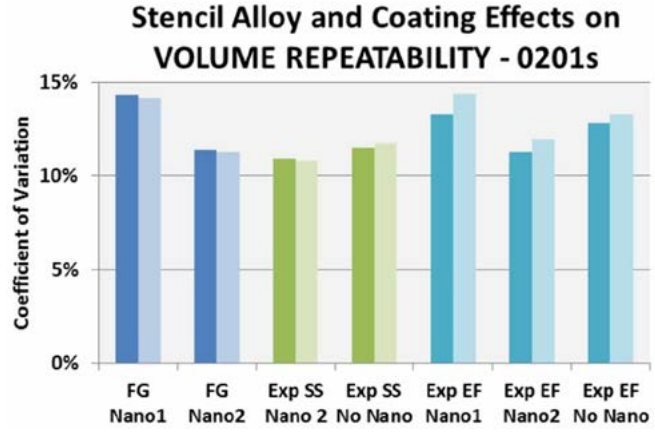

Figure 13: Effects of stencil alloy, coating and component orientation on 0201 volume repeatability.

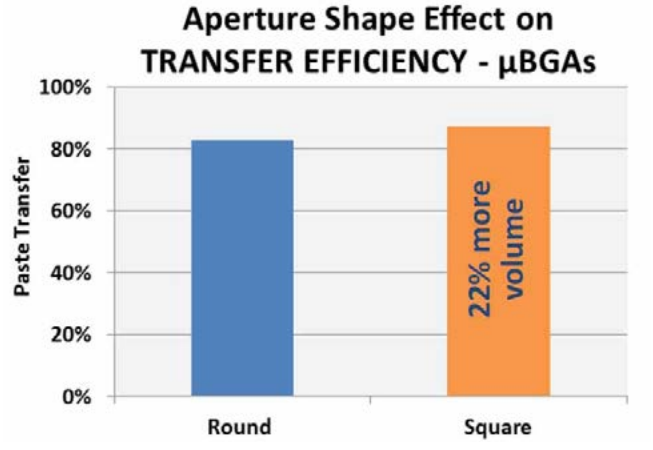

Figure 14: Effect of microBGA aperture shape on transfer efficiency.

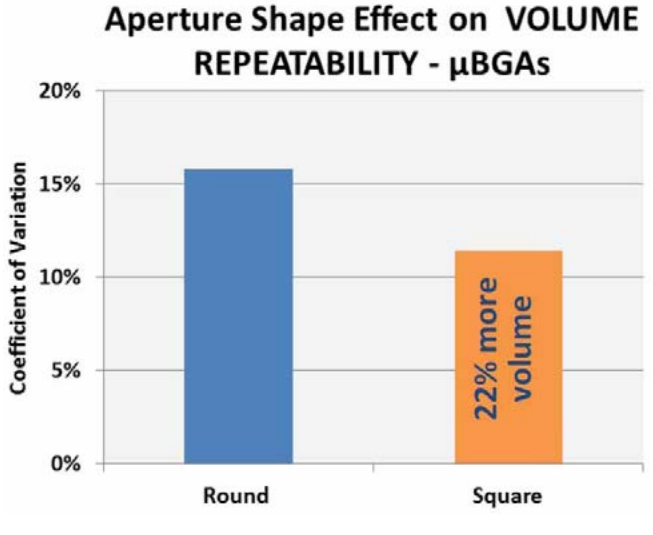

Figure 15: Effect of aperture shape on volume repeatability.

Summary of Round vs. Square Aperture Design

Round apertures are the process of record for these 0.5 mm microBGA devices. The results of this experiment indicate that the square apertures:

A) Provide 20% more solder paste volume
B) Increase transfer efficiency from 83% to 87%
C) Lower variation from 16% to 11%

The effect of the increased paste volume on reflow yields is unknown at this time. The square aperture design will be implemented on a single product and reflow yields will be closely monitored to quantify the aperture's impact on the overall SMT process.

Experiment #4: Wipe Frequency

The production print process for this product utilizes a dry/vacuum/dry wipe after every print. The 1 print per wipe interval was set by prior experimentation. To test claims of nanocoating extending wipe frequencies, additional 10-print tests with stencils 5 and 7 were performed without any wipes at all. Both stencils were the FG SS cut with the POR; stencil 5 used first-generation nanocoating; stencil 7 used second-generation nanocoating.

1) Print Yields

Print yields improved when the wiping step was eliminated from each print. Running 10 consecutive prints without wiping increased the print yields from 80–90% on stencil 5 and from 90–100% on stencil 7, as shown in Figure 16.

2) Transfer Efficiency

Stencil prints at the extended wipe interval showed slightly higher transfer efficiency, as shown in Figure 17.

3) Variation

In both cases, the processes that extended the wipe intervals showed the least variation. The trend of the second-generation nanocoating to consistently produce less variation than the first continued, as observed in other comparisons and shown in Figure 18.

Follow-Up Tests

The results of these tests and comparisons show distinct differentiation between experimental inputs and consistent trends among its outputs. They appear to serve as good relative indicators of performance. However, a considerable difference was observed in comparison to the prior round of tests and typical production results.

The test vehicle is a production product, and historically runs 98.2% print yields. It also consistently produces about 82% TE with less than 10% CV. The relatively low yield numbers,

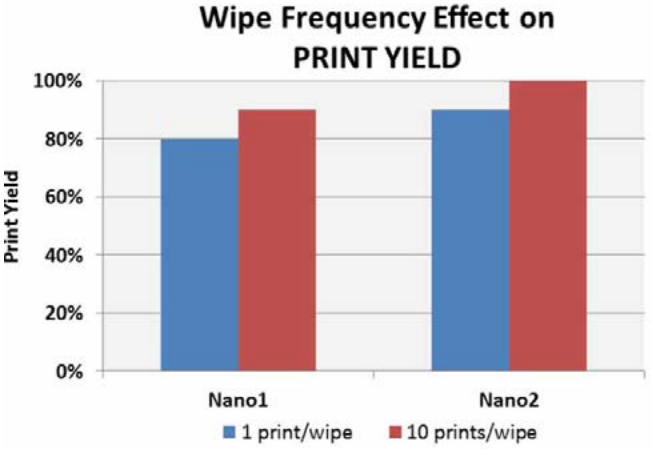

Figure 16: Effect of extending wipe frequency on print yields.

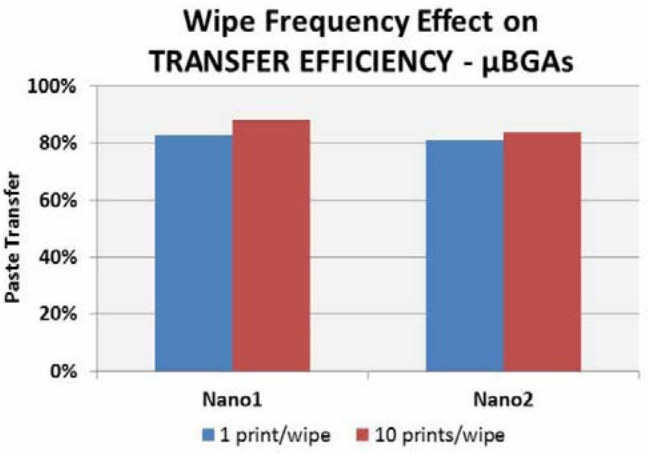

Figure 17: Effect of extending wipe frequency on transfer efficiency.

combined with the higher variation produced in this set of tests, indicated a considerable process difference somewhere in the experiment. The sources of variation were explored.

First, the test setup and equipment were investigated via a database search. The test runs always took place on after the first shift finished using the printer, over a course of two weeks. Investigation into the production print yields indicated no out-of-control situations on the assembly line during that time period; print yields for all production prints run on that line were within in their typical 98%+ range. The likelihood of the printer or print test method introducing the variation was unlikely.

Next, the performance of the stencils cut according to the POR—1, 5 and 7 were compared. Issues had already been identified with stencil 1's PCB side topography that produced atypical results, but stencils 5 and 7 did not produce results comparable with each other (stencil 7 had the highest CV of the tests). These stencils were all manufactured using the Process of Record, with one exception: The usual production stencils are manufactured at a local facility, whereas the test stencils were produced at one of the supplier's other sites.

To explore the possibility of differences in the two sites' manufacturing processes, the production stencil for this PCB was print tested using the same 10-print test as the other runs. It yielded 100% (Figure 19) and transferred 83% (Figure 20) with 9.6% variation (Figure 21), correlating with historical data.

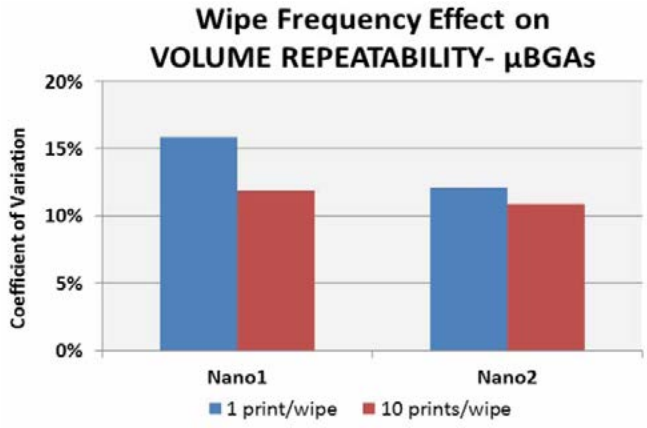

Figure 18: Effect of extending wipe frequency on volume repeatability.

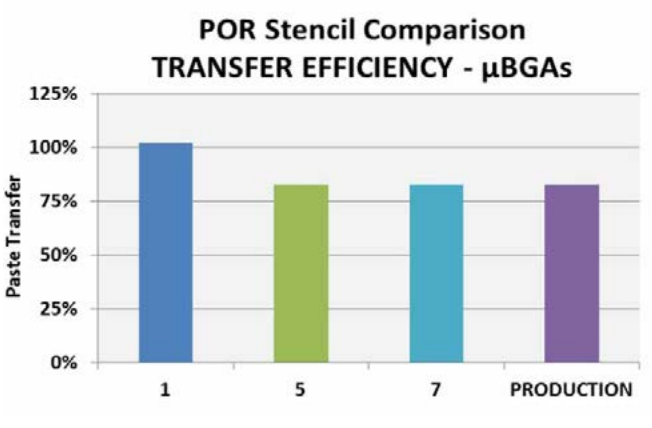

Figure 20: Transfer efficiencies for theoretically identical stencils.

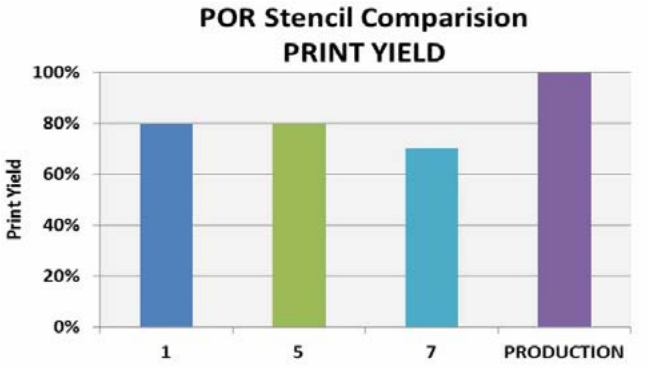

Figure 19: Print yields for theoretically identical stencils.

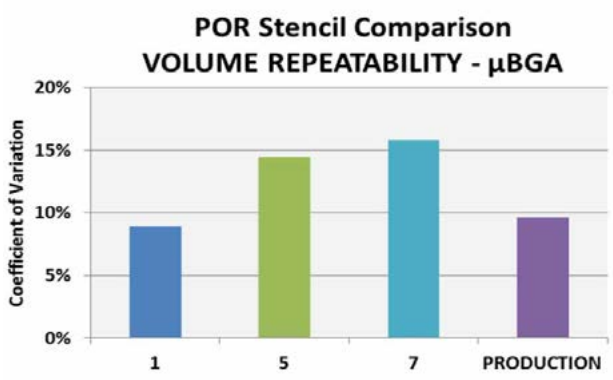

Figure 21: Volume repeatability for theoretically identical stencils.

FINE-TUNING THE STENCIL MANUFACTURING PROCESS *continues*

Investigation into the source of the variation among test stencils and their performance differences indicated considerable dissimilarity between the stencil manufacturing processes at the site making the production stencils and the site making the test stencils. The site providing the test stencils had recently undergone an equipment upgrade, which could be the root cause of the observed performance differences, including the overall lower yields and higher volume variations, and the specific issues noted on stencils 1 and 4. It is under investigation by the supplier at the time of publication.

SEM Analysis

Test coupons were cut into each stencil (except the experimental SS) during their regular manufacturing process for surface roughness analysis. All the laser cut SS stencil walls demonstrated high levels of striation. Of particular interest was the comparison of wall topography of the POR stencils. The apertures cut using the same parameters at the different facility demonstrate a much smoother wall finish when viewed at 800X magnification, as shown in Figure 22. It is likely that the lower yields and higher variation are a direct result of the rougher, more highly striated aperture walls.

Discussion and Conclusions

Despite the experimental noise presumably introduced by the different stencil manufacturing site, the trends in the data are consistent throughout the series of tests.

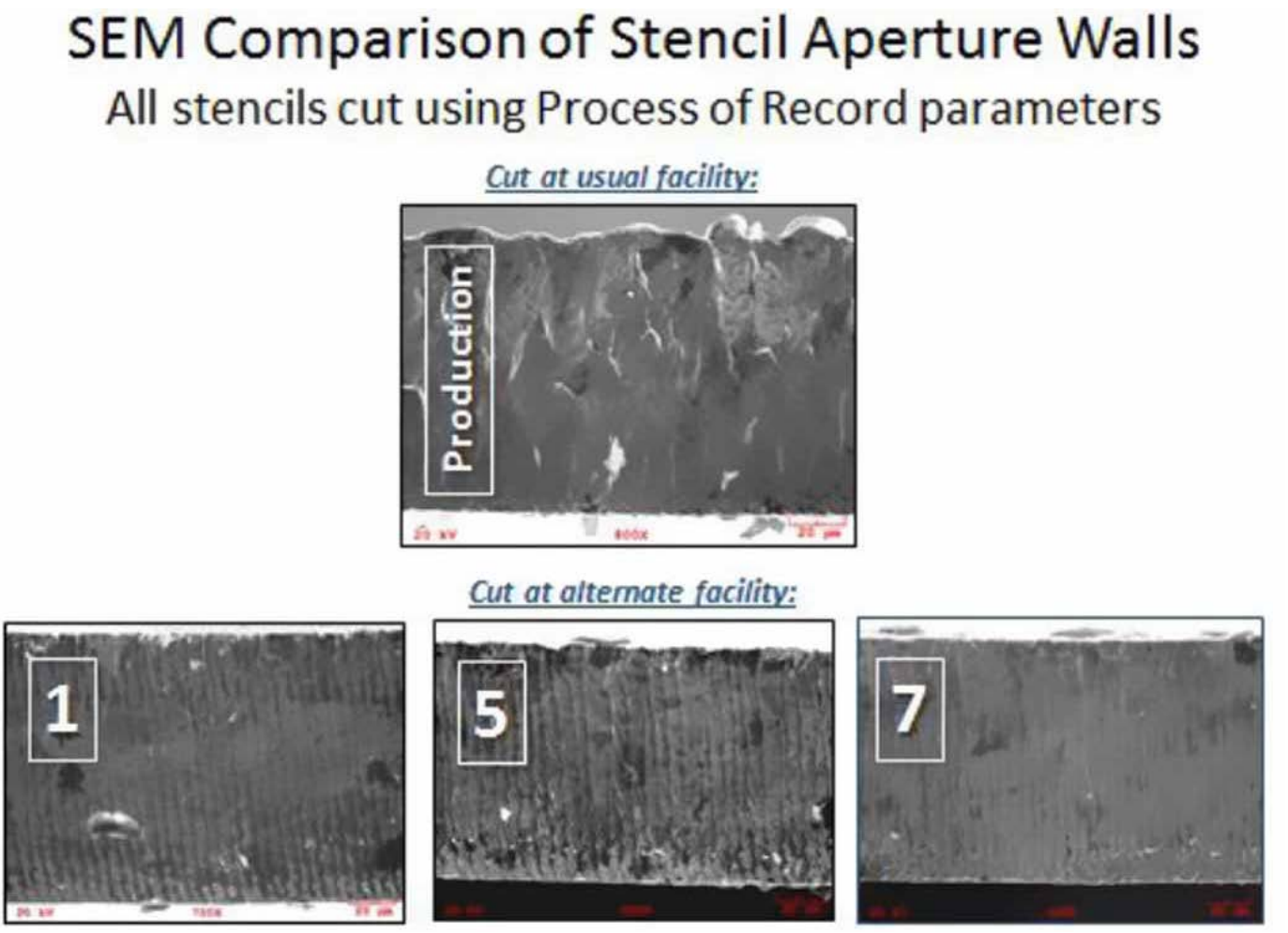

Figure 22.

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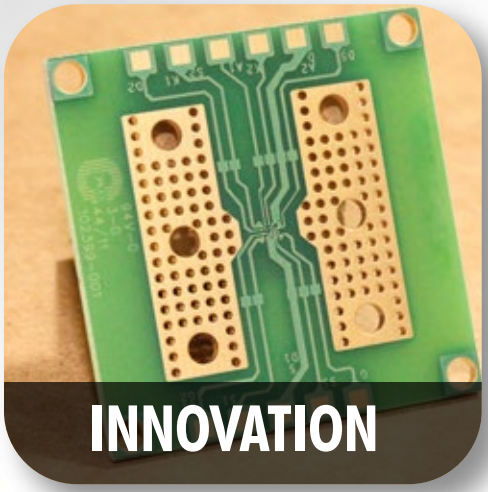

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Experiment #1: Effect of Cutting Parameters and Nanocoating

Originally, the laser cutters at the two different manufacturing sites were assumed to produce similar results. The considerable differences between their outputs were not known until the print test results were calculated and walls were examined at high magnification. The goal of Experiment #1—to refine the cutting parameters to optimize stencil print performance on the assembly line—was obviously not reached. Even comparisons within the dataset for this manufacturing facility were hampered by stencil manufacturing issues on two of the four test sets; however, one trend was abundantly clear. The stencils treated with the first-generation nanocoating consistently produced better yields and better print volume variation. The nanocoated stencils demonstrated slightly lower transfer efficiencies than untreated stencils.

Experiment #2: New Stencil Materials

The experimental materials treated with the second-generation of nanocoating produced the highest yields and best print volume repeatability. The FG and EF stencil foils were tested with both first- and second-generation nanocoatings, and in both cases, the second-generation product provided better volume repeatability.

Experiment #3: MicroBGA Aperture Shape

Square apertures provided better release, better repeatability, and higher print volumes than round apertures of the same major dimension (diameter = side of square).

Experiment #4: Wipe Frequency

Achieving 100% yields at 10 prints per wipe is a considerable achievement. Prior to executing this test, the concept of running this PCB to 10 prints without wiping was completely unrealistic. The production process wipes after every print. Previous tests on the original test vehicle were able to successfully achieve wipe frequencies of 3 prints per wipe using wet wipes with solvents that were chemically matched to the solder paste[3].

Volume repeatability also improved with the extended wipe interval. The influence of under wiping on a stencil treated with the Nano2 is now the subject of a current investigation.

General Comments

The stencil materials test compared current state-of-the art materials with developmental ones, and the results were extremely encouraging. Continued research and development of more sophisticated materials and manufacturing processes will help drive continued advancements in stencil printing technology and enable better economics in the drive for miniaturization.

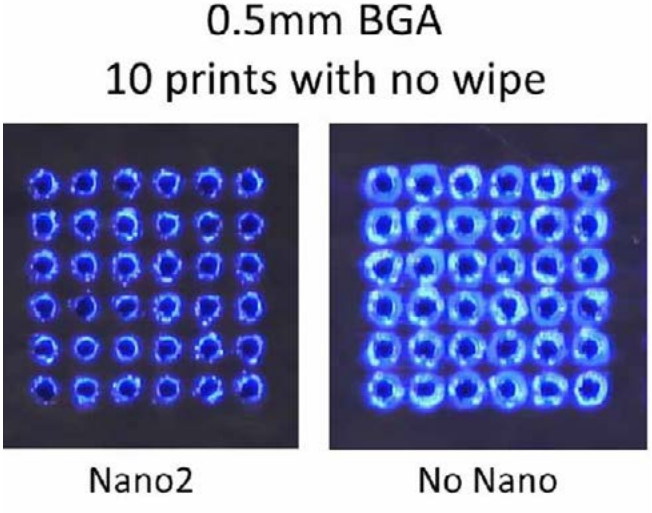

Figure 23: Effect of stencil nanocoating treatment on flux spread on underside of stencil, uBGA.

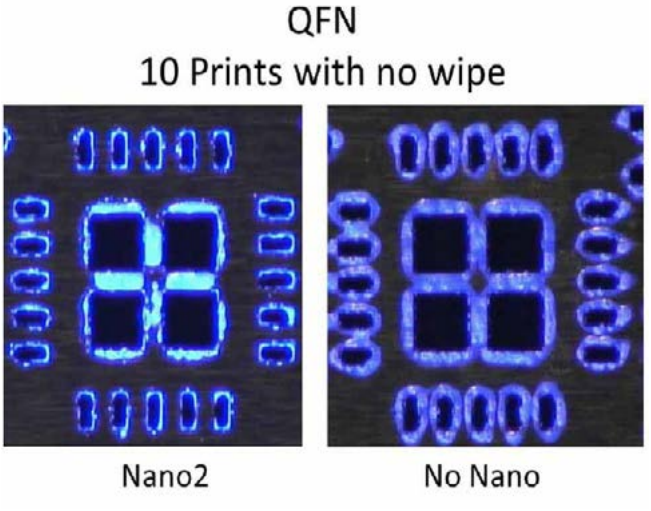

Figure 24: Effect of nanocoating treatment on flux spread on underside of stencil, QFN.

BLACKFOX EXPANDS

Press Release

Blackfox Training Institute, LLC., headquartered in Longmont, Colorado, reports that it officially expands into three additional locations with new facilities.

November 2013:

Blackfox Training Institute reports that it officially expands its training and certification services to three additional locations with new facilities. In addition to the Blackfox headquarters located in Longmont, Colorado, **Blackfox now has new facilities in Tempe, Arizona, Guadalajara, Mexico, and Penang, Malaysia.** Each of these facilities offers the same IPC Certifications and Blackfox Skill-based Certifications as offered in Colorado. Additional locations are planned in the near future.

This expansion was essential in order to create a channel for delivering the IPC Quality Standards and skill-based training and certification to areas of high demand and reduce the travel costs for customers nearby. Each of the Blackfox Training Centers have resident Master IPC Trainers as well as Master IPC Trainers that travel the world delivering all of the training programs at their customers' facilities.

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The results of the nanocoating tests were as anticipated. Lots of data has been generated over the past two years that show the nanocoating improves print yield and repeatability. The new nanocoating formulation's repeated outperformance of the original product demonstrates real improvement in this materials technology and is another example of materials advancements that continue to improve stencil printing technology.

Again in this test, the nanocoated stencils demonstrated slightly lower transfer efficiency than non-treated stencils. This trend was also observed in the original tests in 2011. It is hypothesized that the lower TE of the coated stencils may be due to crisper print definition. This hypothesis may be tested in an upcoming investigation.

The superior print performance of square vs. circular apertures on microBGAs was not surprising, based on information in current literature. What was surprising, however, was the degree of improvement the square apertures introduced. On a cautionary note, square apertures can present gasketing issues on non-solder mask defined pads, so they should be implemented carefully. The PCB used in this study has solder mask defined pads. The new aperture geometry will still be implemented carefully, and will bear less risk than if the PCBs were designed with non-solder mask defined pads.

The most surprising—and most remarkable—findings of the entire study were the wipe frequency tests on nanocoated stencils. Not only did print yields go up, so did volume repeatability! These results were completely unexpected, and are currently the subject of continued investigation.

"The most surprising—and most remarkable—findings of the entire study were the wipe frequency tests on nanocoated stencils. Not only did print yields go up, so did volume repeatability!"

Ongoing and Future Work

At the time of publication, a new test had just been executed to attempt to visualize the flux behavior on coated and uncoated stencils with and without under wiping. Using the original test vehicle, an uncoated stencil (from the regular manufacturing site) was masked and treated with Nano2 over one-half of the print area to enable side-by-side comparison and analysis. UV tracer was added to the solder paste, and the PCB side of the stencil was photographed under black light after several different print and wipe scenarios. Photographs of some of the results are shown in Figures 23 and 24. The complete results will be published at a future date.

Acknowledgements

The authors would like to thank the stencil provider for their participation in this study. They would also like to recognize their colleagues Harshal Tarar, Matthew Sawicki , and Jonathan Dragonas, who assisted in executing the tests. **SMT**

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Chrys Shea is the president of Shea Engineering Services, a consulting firm that produces technical studies and communications tools for the electronics manufacturing industry.

Ray Whittier is the principal surface mount technology process engineer at Vicor.

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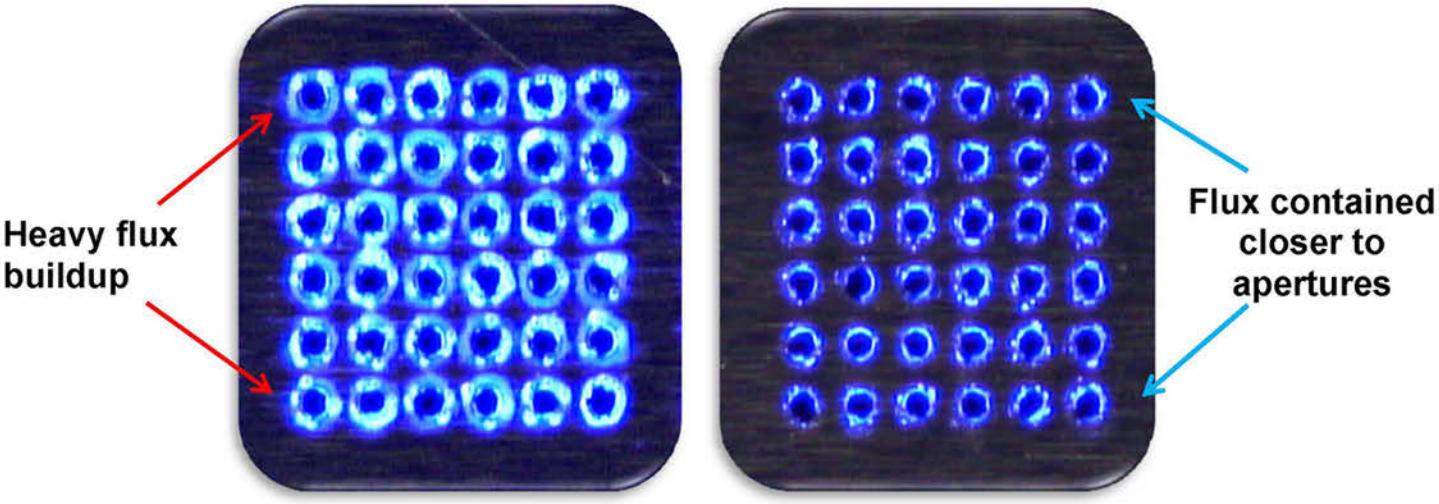

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Testing Intermetallic Fragility on ENIG upon Addition of Limitless Cu

by Martin K. Anselm, Ph.D. and Brian Roggeman
UNIVERSAL INSTRUMENTS CORP.

Abstract

As reliability requirements increase, especially for defense and aerospace applications, the need to characterize components used in electronic assembly also increases. OEM and EMS companies look to perform characterizations as early as possible in the process to be able to limit quality related issues and improve both assembly yields and ultimate device reliability. In terms of BGA devices, higher stress conditions, RoHS-compatible materials and increased package densities tend to cause premature failures in intermetallic layers. Therefore it is necessary to have a quantitative and qualitative test methodology to address these interfaces.

Typically, solder ball shear or pull testing is employed to measure the interfacial strength, sometimes requiring very high speeds to do so. While there is no current industry-accepted specification on proper test speeds, strength or energy metrics, procedures do exist which allow for relevant comparisons. These tests are always run on unassembled BGA devices, so the interaction with the PCB is completely removed. While the data is useful for the component manufacturer, the risk is that the test does not fully represent the final assembly in terms of metallurgical condition. Specifically when BGA components using a nickel-gold surface finish are soldered to PCBs with a Cu-based pad (i.e., Cu-OSP, ImmAg, ImmSn or HASL), there will be additional Cu dissolved into the solder joint. The addition of this copper can have an important effect on the intermetallic structure at the ENIG pad. Current mechanical solder ball testing procedures on unassembled BGA devices do not accurately duplicate the condition of this intermetallic structure. The test results on ENIG pads will then not necessarily correlate to actual manufacturing reliability.

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TESTING INTERMETALLIC FRAGILITY ON ENIG UPON ADDITION OF LIMITLESS CU *continues*

From this research we have determined that generating an intermetallic morphology that is similar to a standard mass reflow surface mount process is not straightforward. The method used to add Cu to the ENIG pad and lead-free solder system will affect the morphologies at the electroless Ni substrate and therefore the mechanical properties of the intermetallic. Data is presented on the intermetallic strengths and failure modes of two bond pull test methods. Specifically hot bump pull (HBP) and cold bump pull (CBP) testing are compared where Cu is added by the copper pins of the HBP tester or by Cu power in a second reflow followed by CBP testing.

Introduction

In this study we present results using a thermo-mechanical test technique which develops a similar intermetallic condition as seen during second level assembly. A careful study was conducted which examines the influence of solder alloy, reflow condition and test technique on the interfacial behavior for the most accurate replication of second-level attach without actually performing the attachment process. The above variables are used to qualitatively vary both the Cu and Ni concentrations within the solder joint, and the interaction between the formation of Ni3Sn4 and Cu6Sn5. Microstructural analysis was conducted and shows a difference in intermetallic morphology as a function of the additional copper. The testing results show that when we simulate second-level reflow onto a Cu-based board, the failure mode and ultimate interfacial strength are significantly affected. The consequence of this work suggests a more rigorous testing approach can be employed for specific condition.

Background

The soldering of ENIG components to Cu substrates generates a condition of elevated Cu concentrations with the solder joint during surface mount assembly. Typical ENIG intermetallic composition consists of primarily Cu6Sn5 due to the high concentration of Cu in the solder system. However, although composition is known, the intermetallic morphology is often not. Morphology is dependent on the concentrations of the various elements in the system, diffusion and dissolution rates of the pad metallurgy, and reflow soldering profile. These morphologies will have varying mechanical strengths and therefore may be more susceptible to failure during manufacturing and reliability testing. Typical intermetallic morphologies seen on the ENIG surface can be seen in Figure 1, where areas of thick Cu6Sn5 scalloped structures are adjacent to thin areas of intermetallic that may be Ni3Sn4 or Cu6Sn5. Typically in these mixed systems Ni and Cu atoms can substitute for one another with the matrix making the more accurate description of the intermetallic formed (Cu,Ni)6Sn5 and (Ni,Cu)3Sn4. For simplicity within this paper the former will be referred to in all future discussions.

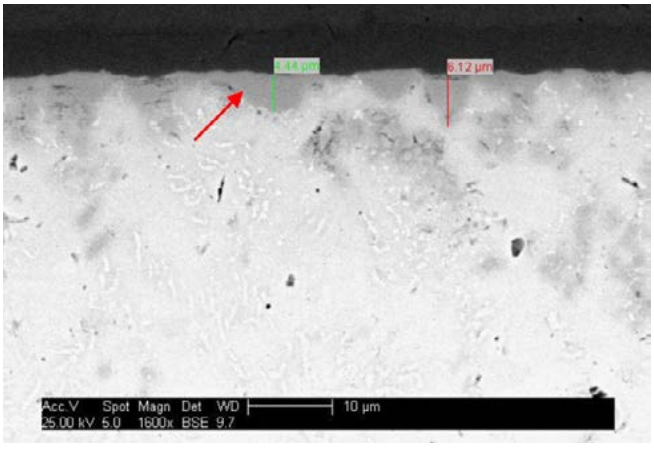

Figure 1: SEM cross-sectional micrograph of typical lead-free solder joint Cu6Sn5 formation at ENIG surface following assembly to Cu OSP board.

It has been shown in this research that the test method one selects to test the intermetallic can have profound results on the results. In addition a method must be developed to generate morphologies that better represent the structures shown in Figure 1.

Solder Alloys

All solder balls were acquired from a single supplier and are 99.9% pure. The alloys used for this research were:

1. Sn/Ag (3.5wt.%) - (SnAg)
2. Sn/Ag (3.0wt.%)/Cu(0.4wt.%) - (SAC304)
3. Sn/Pb (37wt.%) - SnPb

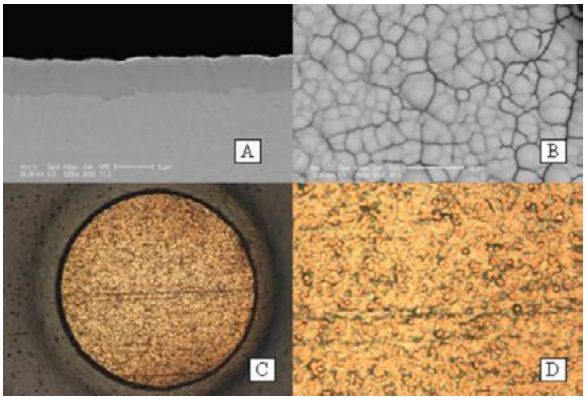

Figure 2: ENIG test board; A) SEM of cross-section, B) SEM of surface inspection ("mud flat" condition is typical for electroless Ni), C) optical image of entire pad, and D) 500x optical inspection of pad surface.

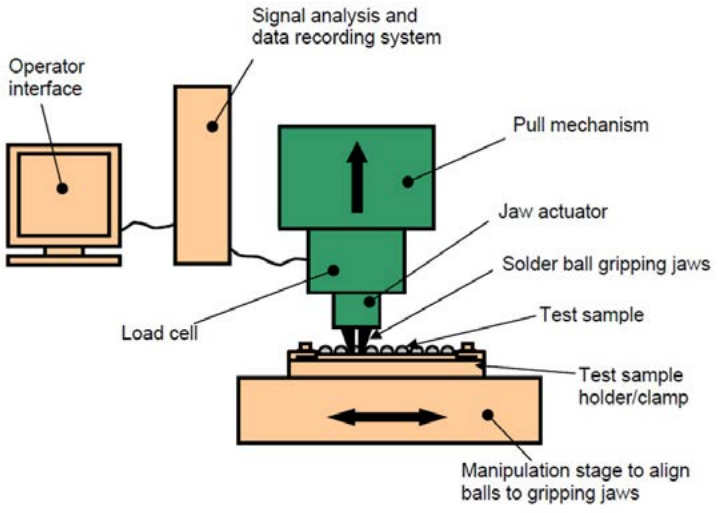

Figure 3: General solder ball pull apparatus[6].

The SAC304 alloy was selected due to the ternary Cu-Ni-Sn phase diagram. SAC304 was created combining a Sn/Ag3.0wt.%/Cu0.5wt.% (SAC305) solder ball with a calculated Sn/Ag3.5wt.% print volume knowing the solid content of the paste, density of the alloy, and calculated print transfer efficiencies for a square stencil aperture of a given thickness. A stencil was purchased with this aperture size and transfer efficiencies were measured to be ~95% with a Cyberoptics laser volume measurement tool. Exact Cu concentration is not critical in this case. However, we wanted to have repeatable results with an alloy contain less than 0.5 wt.% Cu and greater than 0.3 wt.% Cu since this is what has been described in literature to be the limits for the formation of the Ni3Sn4 and Cu6Sn5 intermetallic formation at the Ni boundary[1,2].

Substrates

An electroless Ni/immersion Au (ENIG) test board that was used in this work is a 12-layer PCB with a nominal copper to copper thickness of 2.12 mm (.083"). The board was constructed with Matsushita HF-FR-4 (Tg 148°C) laminate material and PSR-4000 BL01 solder mask. Pad openings were 22.7 mil diameter solder mask defined. Phosphorous concentration was determined to be 12.6 wt.% in the bulk Ni when evaluating cross-section by EDS. Figure 2 shows the condition of the test board as-received.

In this study we compare our controlled experiment to a commercially available Intel SnPb device (Intel 845). The pad diameter for this device was measured to be 26.2 mil solder mask defined as compared to the 22.7 mils for the test board. Although these diameters are not exactly the same the bond testing performance should be comparable. We would expect the peak load to failure to be higher for this device due to the larger pad area.

Mechanical Test

CBP testing is a technique often used in electronics to test the mechanical properties of solder joints and laminates[3,4,5,6]. JESD22-B115A is the standard used for ball pull testing and the "A" revision has been released in August 2010. Figure 3 and Figure 4 illustrate the pull testing apparatus and tweezer alignment respectively. A tweezer tool with a hollowed tip is used to grab the solder joint. Tweezers of similar diameter as the solder joint should be used in order to effectively distribute the gripping forces and minimize the deformation of the solder joint.

Solder joint deformation as well as tweezer alignment to the solder ball could affect the results of the test since the solder may not be placed under a uniform tensile stress across

the pad. Tweezer alignment is described in the JEDEC standard (Figure 4), however it is very operator dependant and may not be performed properly. Any amount of torque or excessive deformation of the solder joint may result in changes in peak load to failure or failure mode. Therefore it is critical to test many solder joints of a given sample to accurately evaluate the repeatability of the data. It has been shown in this work that similar failure modes can be generated with a narrow distribution of peak loads to failure if proper tweezers are selected and care is taken in solder joint alignment.

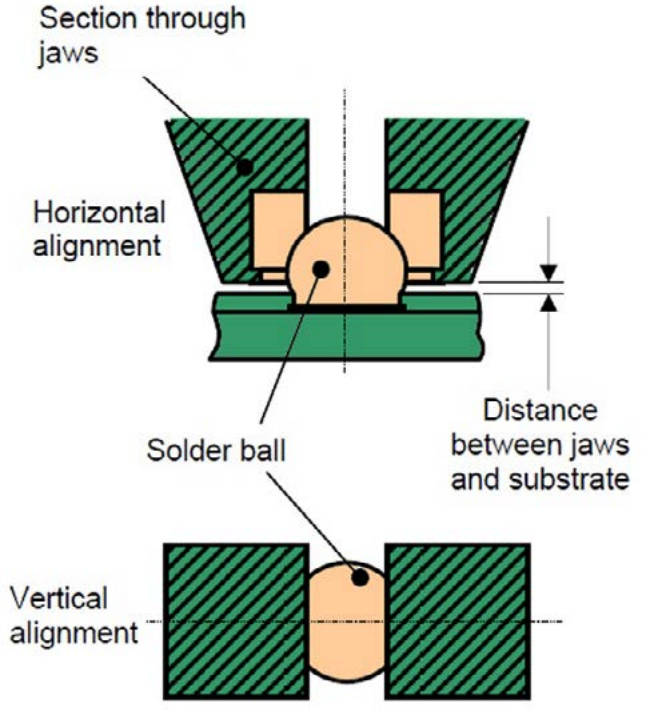

Figure 4: Tweezer alignment[6].

HBP testing is an alternate technique for mechanical testing of solder joints in electronic devices. Historically the hot pin method is used in Japanese testing standards and has been adopted by the military as acceptance criterion for laminate materials where a single unsupported land is repeatedly thermally stressed (Mil-P-5884D). Other standards also required thermal stressing of laminates and pads (IPC-6012, IPC-6013, and IPC-9708). This test method is significantly different than CBP testing in that heat is applied to the solder joint through a high-purity Cu pin or a soldering iron Figure 5. Once the pin reaches a temperature above the melting point of the solder it is brought in contact with the solder at a pre-selected depth.

It is arguable that this process cannot be compared to CBP due to its effect on the solder joint intermetallic structures. The temperature gradient of this process and the addition of Cu from the pin to the solder system must be

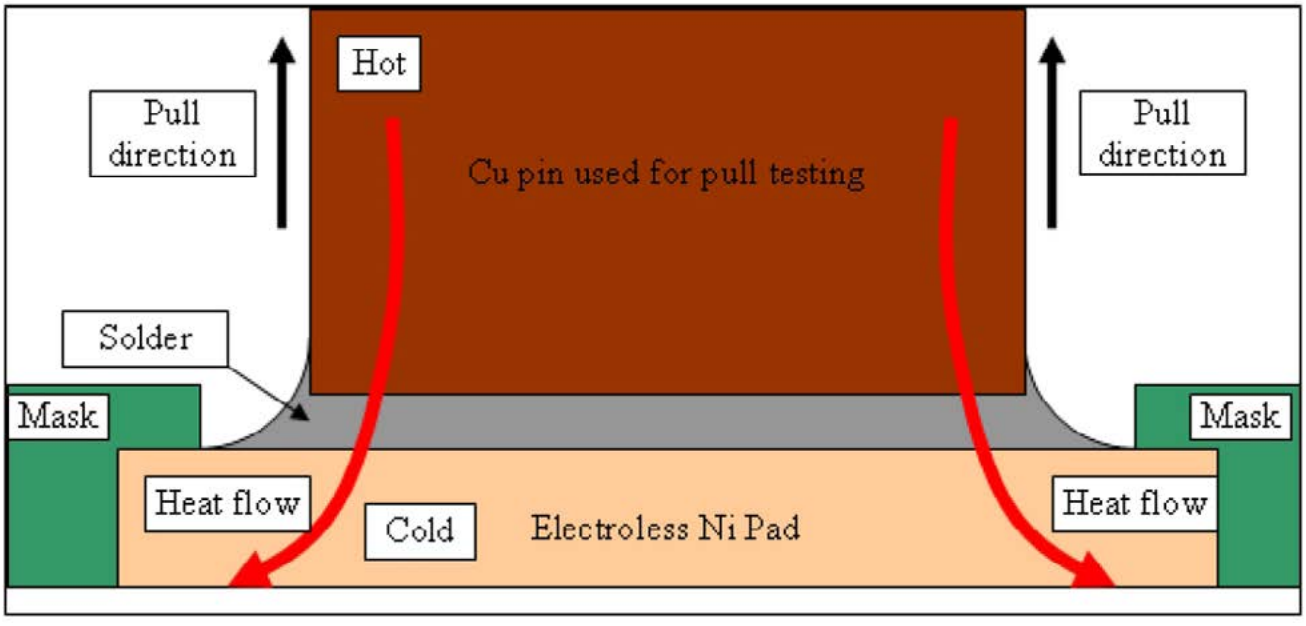

Figure 5.

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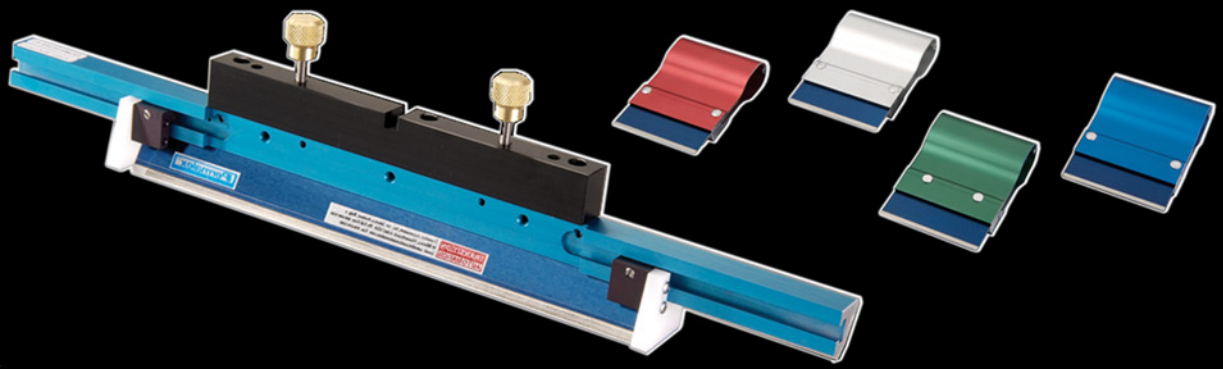

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considered when testing solder joint intermetallics in this manner. Heating from a localized pin may also affect the Cu pad adhesion to the base dielectric and cohesion of the dielectric beneath the pad in the cases of pad cratering. This test is best suited for testing intermetallics of solder mask defined pads due to the additional strength of a larger pad defined by mask.

Test Method

Intermetallic of various morphologies and compositions were created by soldering solder spheres of specific alloy to the ENIG substrate. These intermetallics were then either HBP tested or subjected to a second reflow with Cu powder and then CBP tested.

Ball Attach

All solder joints were reflowed in nitrogen environments using a Vitronics Soltec 10 zone convention reflow oven. For the first reflow process (ball attach), a short (~20 second) and long (~120 second) time above the reference temperature of 217°C was used for the lead-free solder alloys Sn/3.5Ag and SAC304. Similar times above the reference temperature 183°C were used for the SnPb 25 mil solder balls. A peak temperature was measured for the long profile to be 208°C for SnPb and 236°C for the lead-free. For the short profiles peak temperatures were limited by duration above the reference temperature however for SnPb 185°C was achieved and 226°C for the lead-free alloys.

Addition of Cu by Powder

Copper powder with a nominal diameter of 20 microns was purchased from Advanced Powder Products. This powder was mixed with Kester no-clean tacky flux (TST-6592LV) and printed on a silicon wafer using a glass slide and 0.007" feeler gauges as standoffs. Bumped test boards and the Intel 845 device were dipped into this powder/flux mixture and then reflowed in nitrogen. Images of the power dipped Intel 845 device pre- and post-reflow are shown in Figure 6.

In the second reflow the Cu powder was mixed with tacky flux and mixed with the solder joint providing a limitless source of Cu. A 60-second time above reference temperate was used since this is more representative of standard assembly processes used in electronics manufacturing. This second reflow has provided adequate time for the formation of Cu6Sn5 at the electroless Ni substrate. Peak temperatures for these profiles were 213°C for SnPb and 242°C for lead-free. Intermetallic formations following the addition of Cu were unique for the lead-free cases. Morphological differences observed optically seemed to have evidence of precipitation of Cu6Sn5 above the pad surface for the long attach profile samples (Figure 7 C & D) and

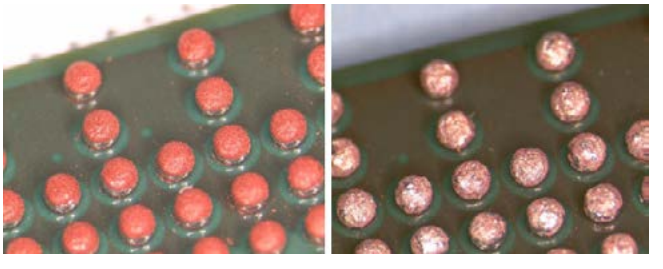

Figure 6: l-r: Device dipped in Cu power pre and post reflow respectively.

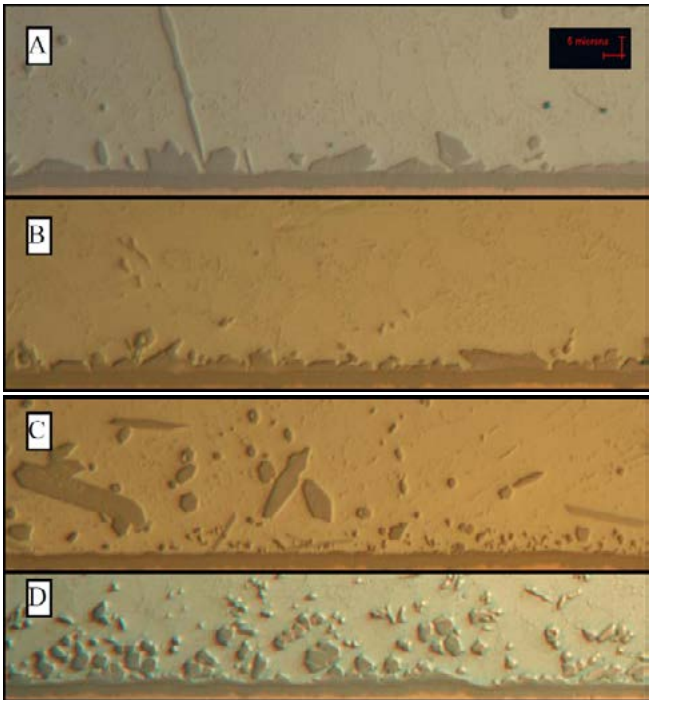

Figure 7: 500x optical inspection lead-free alloys following addition of Cu powder (A) SnAg Short (B) SAC304 Short (C) SnAg Long (D) SAC304 Long.

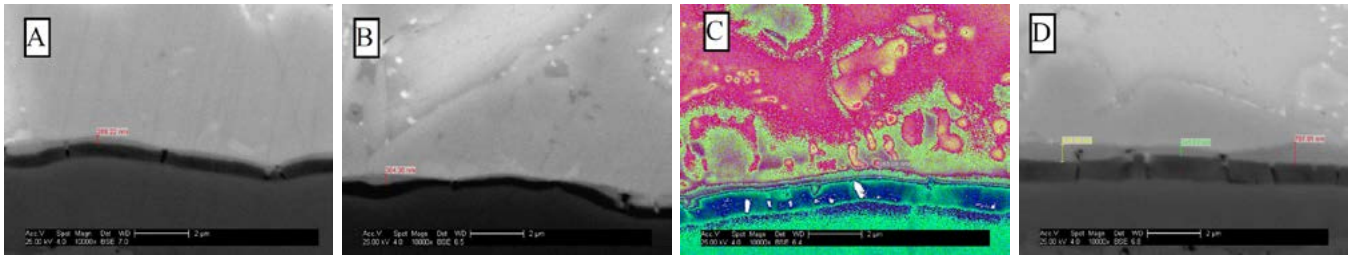

Figure 8: 10,000x SEM images of lead-free morphologies following addition of limitless Cu (A) SnAg Short (B) SAC304 Short (C) SnAg Long (D) SAC304 Long.

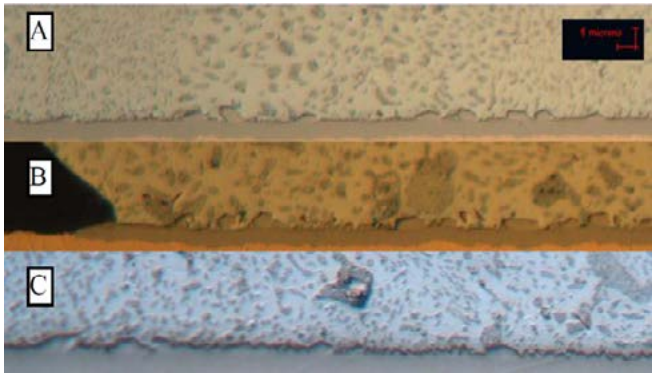

Figure 9: 500x optical images of SnPb morphologies following addition of Cu powder (A) SnPb Short (B) SnPb Long and (C) Intel 845.

Cu6Sn5 intermetallic at the electroless Ni surface for short ball attach profiles (Figure 7 A &B).

SEM inspection of the lead-free systems suggests that the SnAg Long (Figure 8C) had a unique morphology near the electroless Ni pad surface. Specifically a thinner intermetallic was observed in direct contact with the pad.

Following addition of Cu powder the intermetallic variation for the SnPb samples was far less dramatic than the lead-free samples. The long and short ball attach profile seemed to have little effect on the intermetallic morphology as determined by optical inspection (Figure 9) and SEM (Figure 10).

Cold Bump Pull (CBP) Testing

CBP was performed on a Dage 4000 bond tester (Figure 11) using a tweezer of diameter 30 mils and a CBP5kg load cell. Pull rates were determined based upon the frequency of brittle failure modes observed. A speed was selected that generated nearly 100% brittle failure at the electroless Ni substrate.

Hot Bump Pull (HBP) Testing

HBP testing was also performed on the Dage 4000 bond tester however a 30 mil diameter pin is heated and soldered to the solder joint using a HBP10kg lead cell. This load cell has an integrated heating element controlled by a temperature controller. Exact temperatures are difficult to quantify since the equipment thermocouple is attached to the heating element and not the tip of the Cu pin. A temperature was selected that induced reflow of the solder joint. The pin was brought in contact with the ENIG pad for

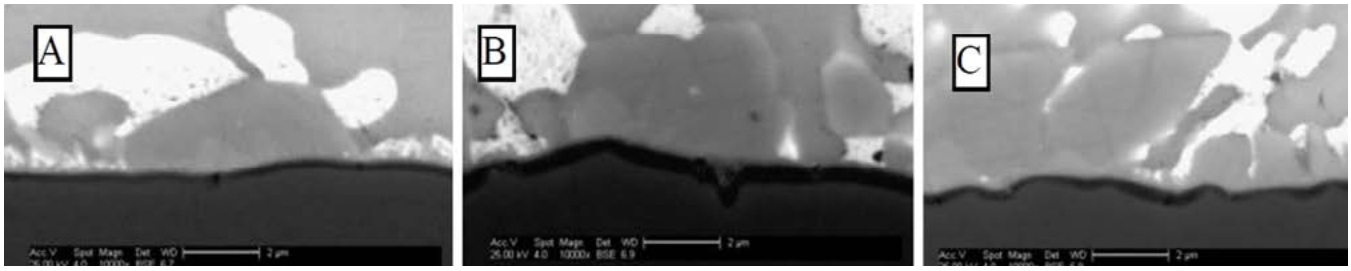

Figure 10: 10,000x SEM images of morphology IX (A) SnPb Short (B) SnPb Long and (C) Intel 845.

Figure 11: Dage 4000 slow speed bond tester.

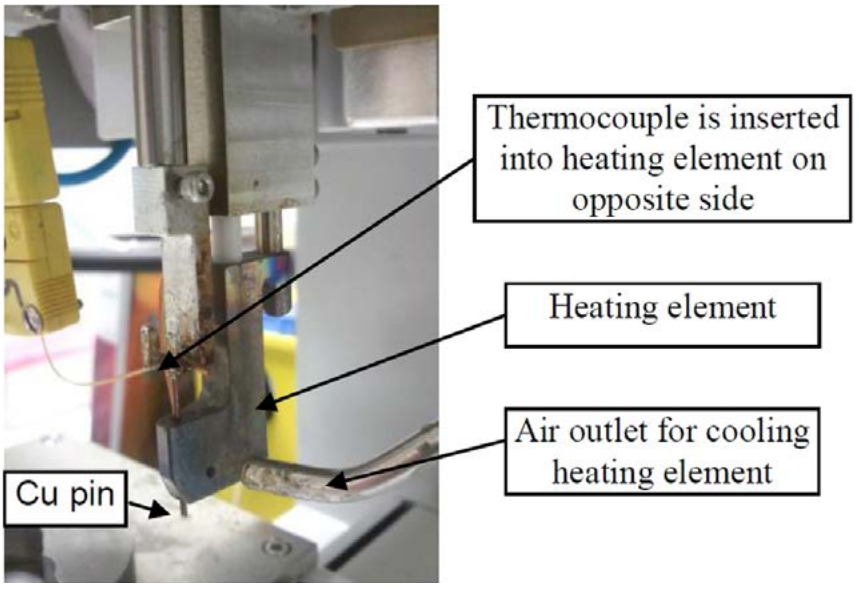

Figure 12: HBP10Kg load cell.

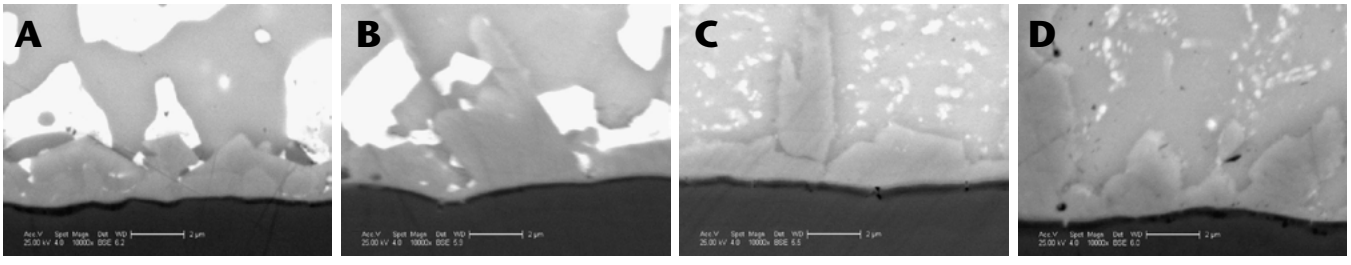

Figure 13: 10,000x SEM inspection of HBP intermetallic morphologies for Intel and Short ball attach profiles (A) Intel 845, (B) SnPb, (C) SnAg, (D) SAC304.

approximately 10 seconds during the soldering process in order to ensure complete reflow and mixing of the solder joint.

Prior to performing the pull testing on a solder joint the heating element temperature was monitored to be less than 30°C. Cooling of the pin is accomplished by a compressed air nozzle near the heating element. Pin and heating elements are identified in the image of the HBP10kg head image in Figure 12. Care was taken not to disturb the liquid solder joint during the cooling of the pin.

Several solder joints were reflowed followed by pin removal from the liquid solder in order to cross-section the solder joint and inspect the intermetallic condition. Intermetallic structures following the reflow soldering of the HBP tester Cu pin appeared very similar in SEM analysis of the solder joints. Lead-free solder joints all appeared to have similar thickness intermetallic at the electroless Ni boundary (Figure 13). A similar observation was also made of the SnPb solder samples (Figure 14).

Experimental Results

In both HBP and CBP testing the failure mode produced were brittle failures within the intermetallic at the electroless Ni substrate (Figure 15). As an aggregate the average peak load to failure of the HBP test samples was far lower than the CBP test procedure. This suggests either a dramatic decrease in the intermetallic strength or a difference in the mechanical loading between these two tests.

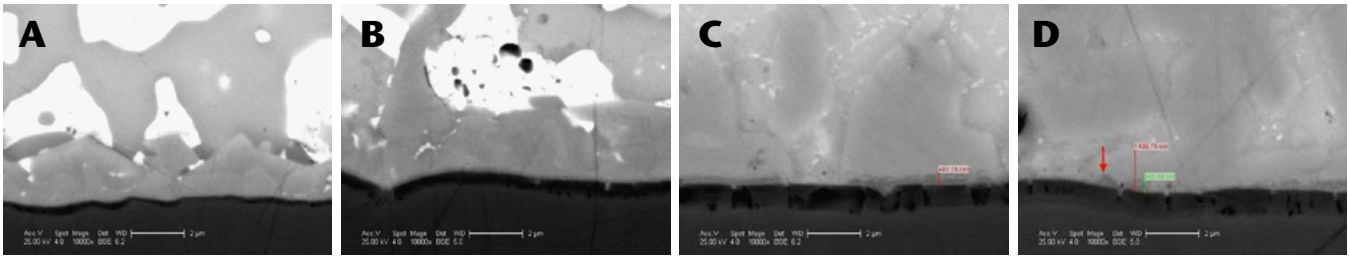

Figure 14: 10,000x SEM inspection of HBP intermetallic morphologies for Intel and Long ball attach profiles (A) Intel 845, (B) SnPb, (C) SnAg, (D) SAC304.

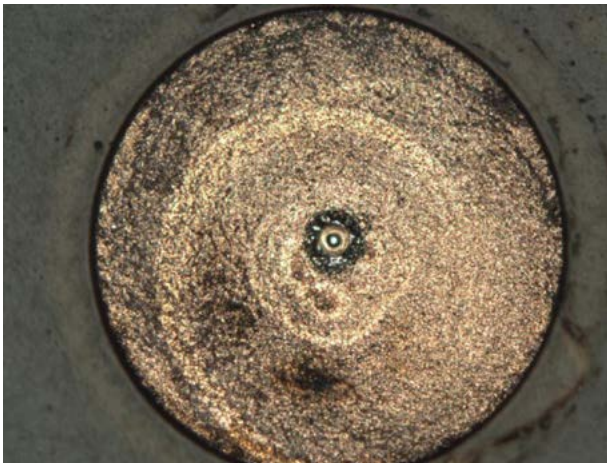

Figure 15: HBP brittle failure mode example.

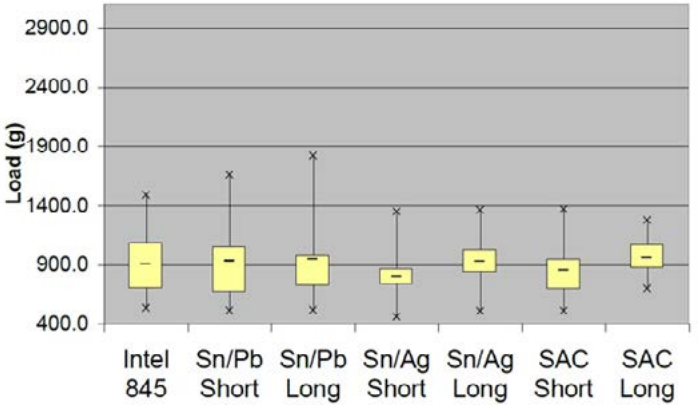

Figure 16: HBP test results between all alloy and process variations.

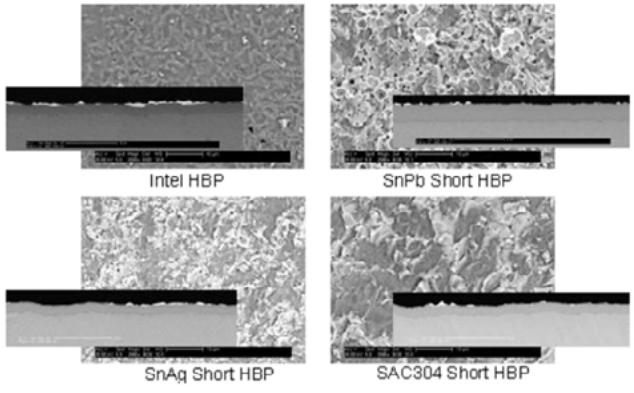

Figure 17: HBP Short profile fracture morphology comparison to Intel 845.

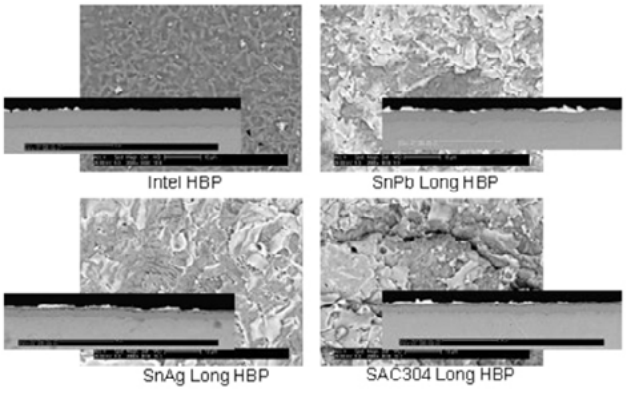

Figure 18: HBP Long profile fracture morphology comparison to Intel 845.

Peak load to failure and failure mode in HBP testing was nearly identical for all solder and ball attach variations. The HBP testing method developed for this research has mitigated the intermetallic morphology variability during ball attach and alloy selection as shown in Figure 16. Ultimately all solder joints failed in a brittle failure mode with similar fracture morphologies as shown in Figure 16 and Figure 17. Inspection of the fracture surfaces revealed that fractures

for the test board were through the (Cu,Ni)6Sn5 intermetallic at the pad surface.

Further research needs to be conducted of this test method in order to develop a process that produces variability with solder alloy and ball attach process as seen in the CBP testing.

In CBP testing peak load to failure distributions showed a marked difference between the various lead-free morphologies formed during ball attached and subsequent reflow with copper powder. All but one lead-free case produced a large standard deviation in pull testing. Only the SnAg Long ball attach sample resulted in a narrow peak load distribution similar to the SnPb cases as shown in Figure 19. This suggests that the SnAg Long sample has more consistent intermetallic properties from ball to ball. The fracture surfaces were compared and the SnAg long ball attach process seemed to have slightly more intermetallic remaining at the pad surface than the other lead-free samples as shown in Figure 20. Although brittle failures modes are not favorable in electronics packaging, having consistent result does improve an engineer's ability to predict characteristic life of the device in mechanical accelerated life testing.

The SnPb samples, by comparison, also failed in a narrow distribution of peak load to failure. This has driven the average up and arguably reduces the possibility of infant mortalities in mechanical stress conditions. Failure modes were similar for the control sample however the Intel 845 device exhibited a different fracture characteristic with more intermetallic remaining at the electroless Ni pad surface following ball removal as shown in Figure 21.

Conclusions

Intermetallic morphology affects the peak load to failure distribution in CBP testing and a possible narrow distribution can be created for SnAg using a long ball attach profile. This condition is favorable for reliability predictions and mitigation of infant mortalities for lead-free product.

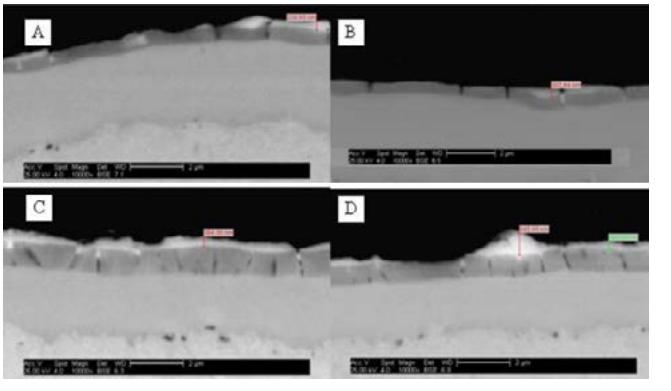

Figure 20: Cross-sectional SEM comparison of CBP fracture surfaces (A) SnAg Short (B) SAC304 Short (C) SnAg Long (D) SAC304 Long.

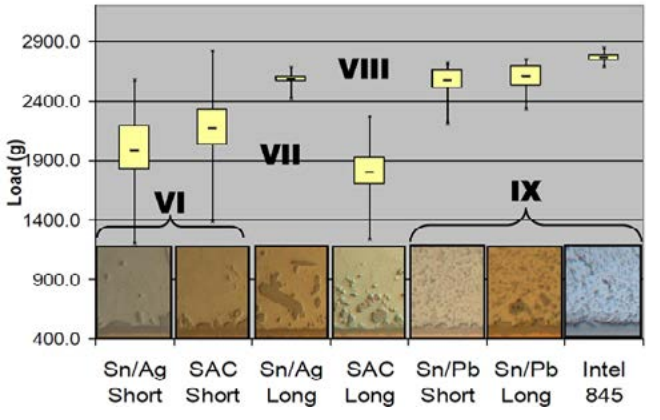

Figure 19: CBP load to failure distribution for various morphologies.

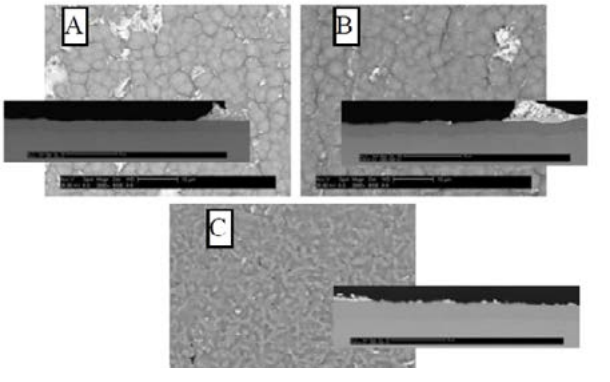

Figure 21: SEM SnPb fracture morphology comparison (A) SnPb Short (B) SnPb Long and (C) Intel 845.

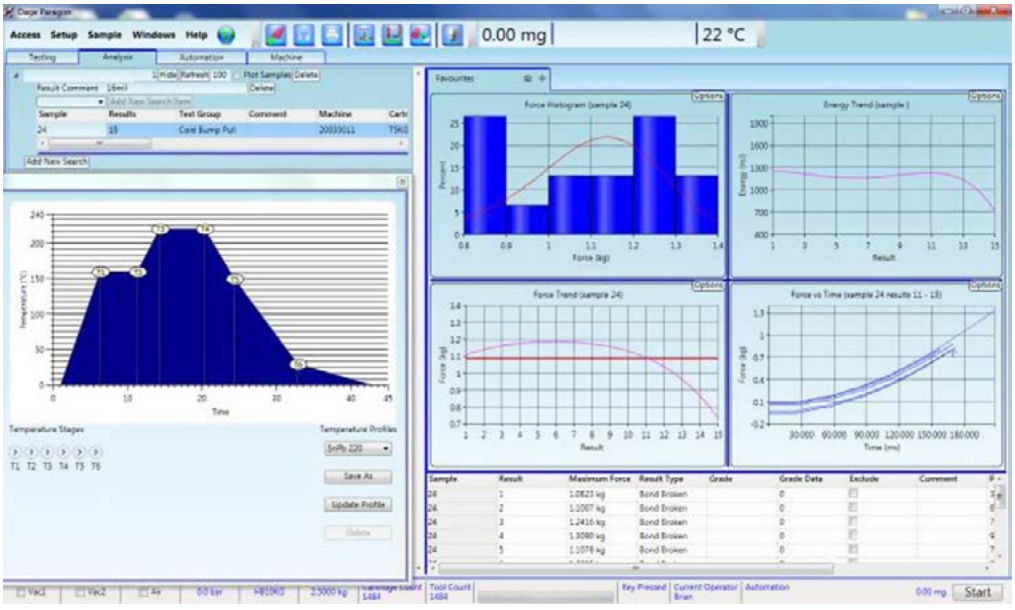

Figure 22: HBP reflow pin temperature profile used for current research into this test method.

More research must be conducted to compare the intermetallic morphologies created in these tests with those observed in standard component attach. Since individual solder joints cannot be mechanical tested in a BGA the only comparison that can be made is through intermetallic morphological comparison.

An improved HBP test method may provide pull testing results that vary based upon ball attach method and solder alloy. Current equipment offerings can mimic pin temperatures that are indicative of a mass reflow as shown in Figure 22.

Future Research

Further testing of the HBP test is required to better mimic a surface mount process. Research is being developed to test a standard ramp, soak, reflow soldering profile as well as pins of various alloys. Test methods for HBP testing may only be applicable for devices attached to circuit boards with Ni substrates since intermetallic formation rates are far slower and the system is less elementally complex.

Acknowledgements

Universal Instruments Corporation's Advanced Process Lab would like to thank Indium for supplying materials and Nordson Dage for assisting with equipment setup. **SMT**

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Martin Anselm is manager of the AREA Consortium at Universal Instruments and SMTA Training Committee chair.

Making Sense of Accuracy, Repeatability and Specification for Automated Fluid Dispensing

by Nordson ASYMTEK

SUMMARY: Understanding accuracy and repeatability is an important step to analyze fluid dispensing system performance. But these terms can be prone to misinterpretation when reviewing a product specification.

A dispensing motion system can be made to perform better or worse under different operating conditions. This article will explain accuracy and repeatability, and how they can be applied to different specifications. It will also discuss key considerations when interpreting accuracy and repeatability for decision making.

Accuracy vs. Repeatability

"Accuracy" and "repeatability" are commonly encountered terms used as performance characteristics of fluid dispensing equipment. Unfortunately, these terms are often confused or misunderstood. Accuracy (Figure 1) is a measure of how close an achieved position is to a desired target position. Repeatability (Figure 2) is a measure of a system's consistency to achieve identical results across multiple tests. The ultimate goal is to have both a highly accurate and highly repeatable system.

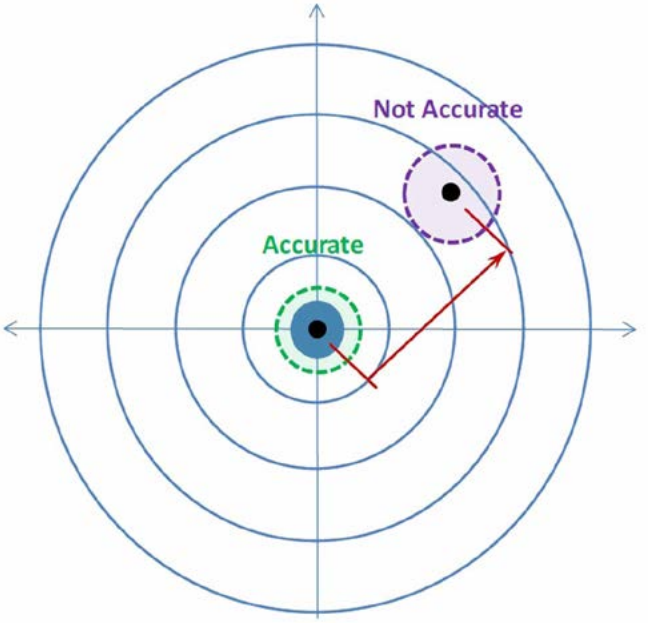
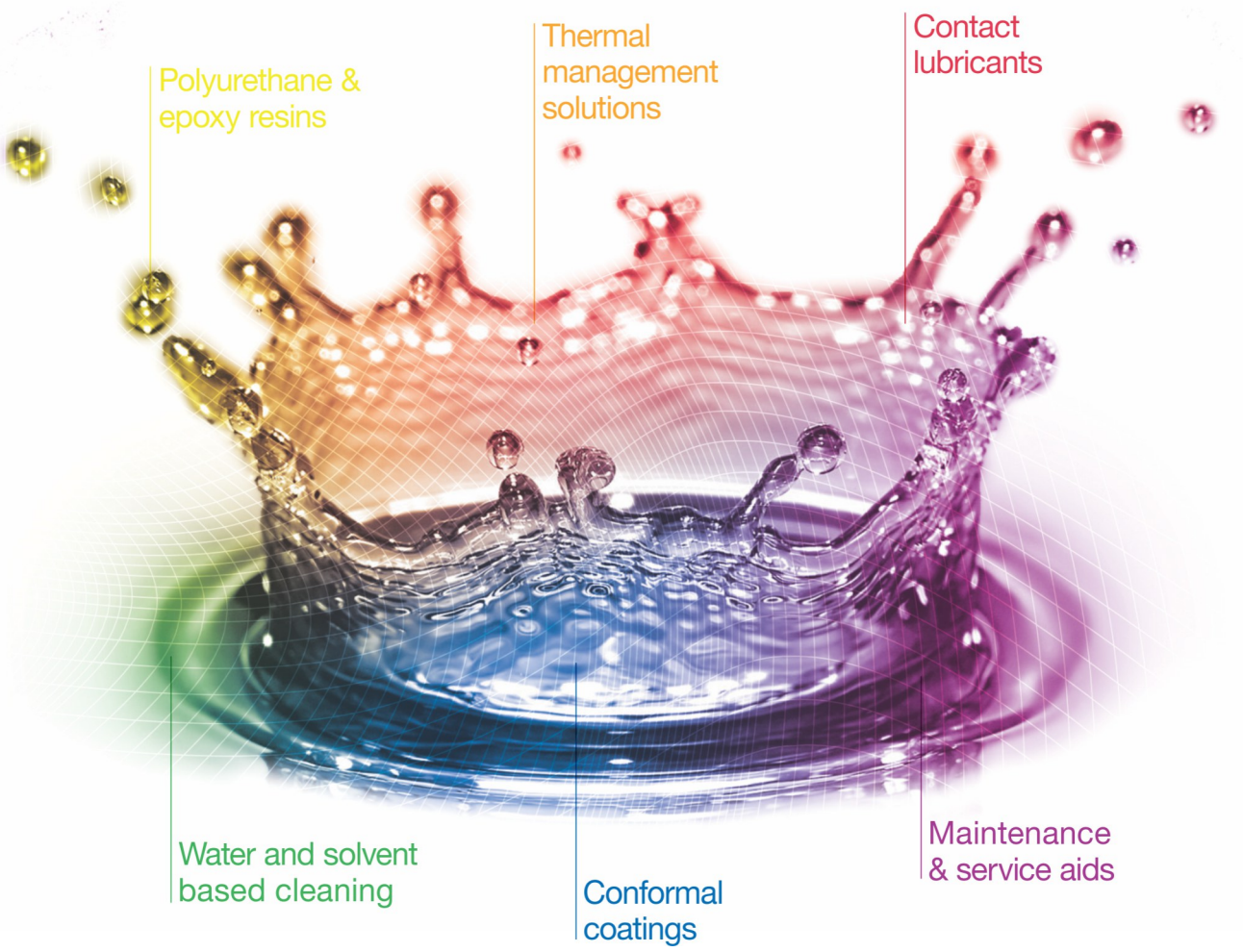


Figure 1: Accuracy.

Repeatability is often expressed as the range (variation) of measurements achieved for multi-



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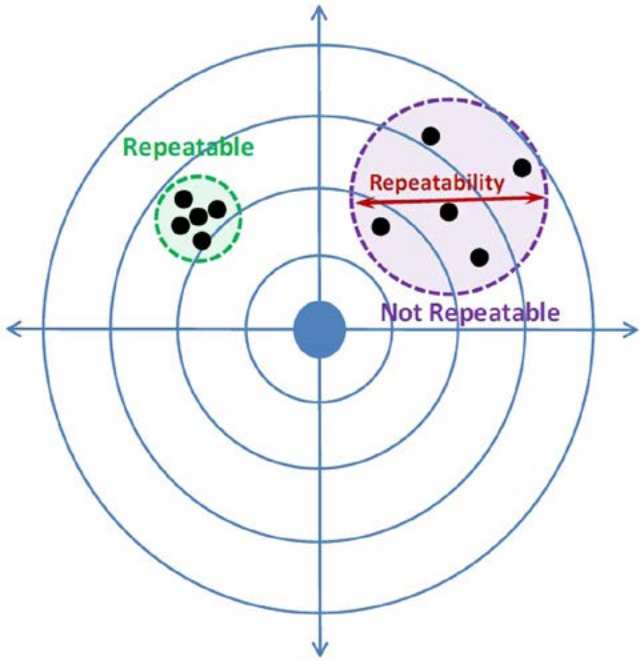

Figure 2: Repeatability.

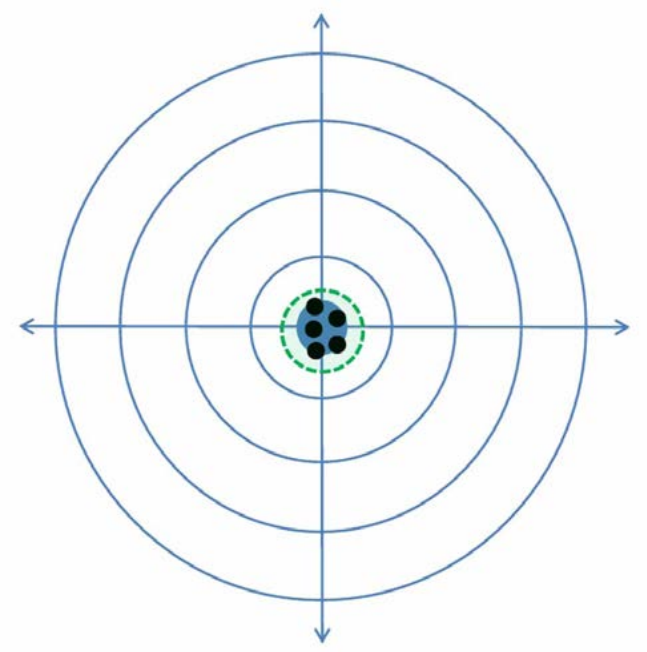

Figure 3: Accurate and repeatable process.

ple test points under consistent test conditions. Figure 2 illustrates examples of repeatable and non-repeatable processes. Thus, for the purposes of specifications, achieving smaller repeatability numbers is better because it indicates tighter groupings or a smaller range within the test data distribution. Repeatability differs from accuracy in that it is concerned with variations in achieved results relative to each other within a given sample size.

In a fluid dispensing system, accuracy is the ability of the equipment to dispense to a target position. An accurate system is one that dispenses exactly at the target location. In order to measure accuracy, though, we really measure the individual test offset error between the achieved result and the target (ideal), as shown in Figure 1. Thus, accuracy specifications are really expressions of the system inaccuracy and achieving a smaller specification means a system is more accurate. When specifying accuracy, however, it should not be based on a single test result, but many test results. As such, it is common practice to use the average (mean) error amongst a range of test data to express the accuracy of the entire test data distribution.

Accuracy and repeatability are closely related but are two independent specifications. It is possible for a system to be repeatable but not accurate and also possible for a system to be accurate but not repeatable. As previously mentioned, an ideal system is one that is both accurate and repeatable, as illustrated in Figure 3.

Accuracy and Repeatability in Specifications: Standard Deviation, Cp and Cpk

Accuracy and repeatability need to be placed in context to a specification to be meaningful. Typically, accuracy and repeatability specifications are bounded by an upper specification limit (USL) and a lower specification limit (LSL). Standard deviation, Cp and Cpk, describe how accurate and repeatable a set of test results are contained within the USL and LSL.

The standard deviation, σ (sigma), is a statistical measure of the difference between individual data points to the average value of the sample of data and indicates spread of measured data.

Standard deviation is calculated based on the following formula:

$$\sigma = \sqrt{\frac{\sum_{i=1}^{n}(x_i - \bar{x})^2}{(n-1)}}, \quad \text{Equation 1}$$

Where n = the number of samples in the data set, xi is the value of a given data point within the data set, and $\bar{x}$ is the average value of the data set.

In a normal population of data points (a symmetrically balanced bell-curve, or histogram, of test samples), 99.7% of all test data will fall within ±3σ about the mean value of the data population (see Figure 4). This indicates that for a sample size of 1000, for example, three samples will then fall outside of this ±3σ range and could be considered an outlier or reject (yield loss).

Process capability, known as Cp, indicates the spread of data relative to specification range. Cp is calculated based on the following formula:

$$Cp = \frac{USL - LSL}{6\sigma} \quad \text{Equation 2}$$

A process is said to be capable or in control when the Cp value is equal to or greater than 1.0. Using Cp, however, assumes that the center of the data set falls at the midpoint between the USL and LSL. Therefore, it is possible to have a highly repeatable process (low variation, tight distribution of data) but be completely off target (poor accuracy) as in the case of the left group of data points in Figure 2.

Cpk, by comparison, considers both the spread of data within the specification range and location of the center of the data relative to a target that is midway between the USL and LSL. Cpk is defined with the following formula:

Equation 3

$$Cpk = \text{minimum of } [\frac{USL - \bar{x}}{3\sigma}, \frac{\bar{x} - LSL}{3\sigma}]$$

Where $\bar{x}$ = mean of the sample data.

Put another way, Cp is an indicator of how repeatably a system performs, and Cpk indicates how accurate and repeatable the system performs relative to USL and LSL. The process is said to meet specified capability when the Cpk value is equal or greater than 1.0. Conceptual differences between Cp and Cpk are shown in Figure 5. It is possible to have Cp > 1 (good repeatability) but Cpk < 1 (poor accuracy) if the distribution of data is not centered at target.

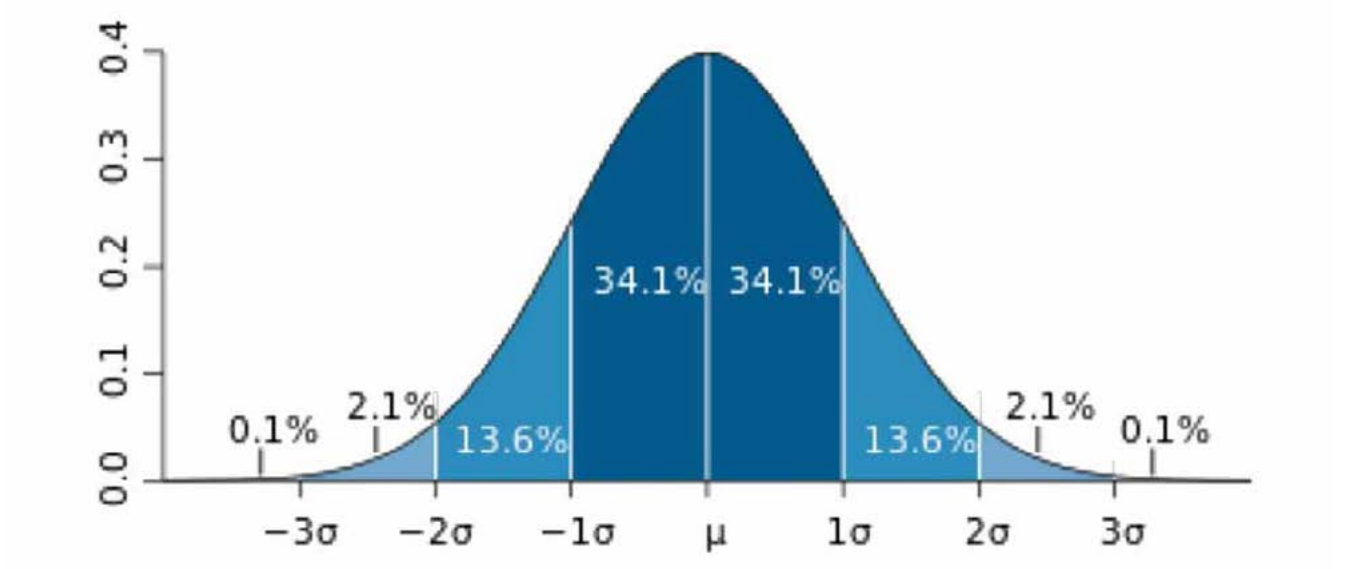

Figure 4: A normally distributed data set with percent of data at varying sigma levels.

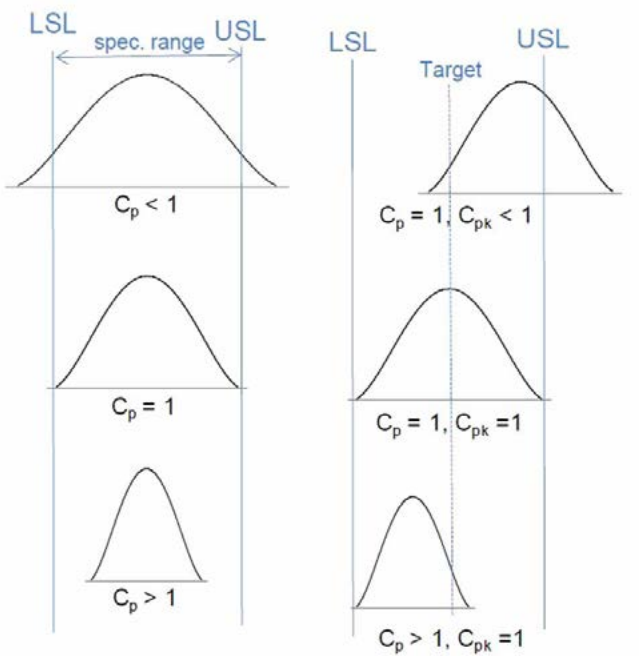

Figure 5: Difference between Cp and Cpk.

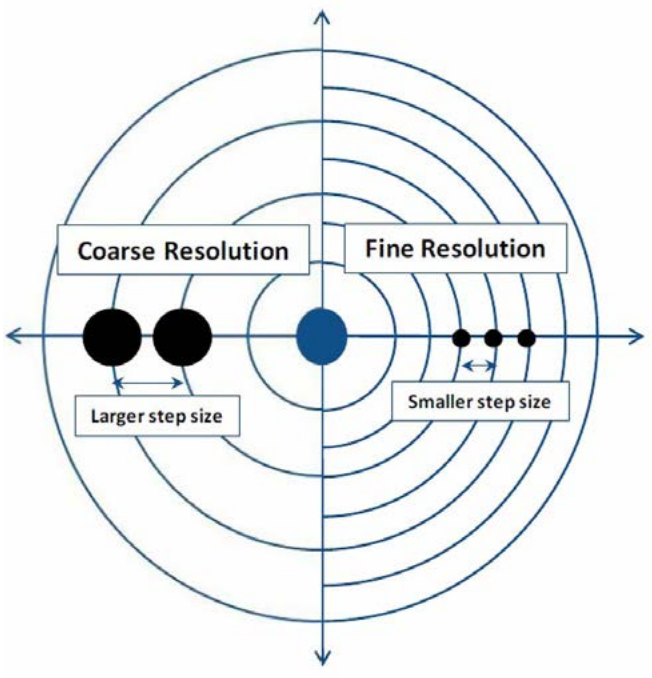

Figure 6: Resolution.

Accuracy, Repeatability and Specifications

Now we will discuss how these concepts relate to fluid dispensers and specifications for accuracy of the system. There are many factors that must be considered when generating a specification for accuracy, including the motion system, the vision system, the dispensing system and the test conditions for validating the specification.

Motion System

When considering the motion system of a fluid dispenser, there are two main factors for consideration, the resolution of detection of the system position by the system controls and the dynamic versus static condition of the motion system during a test.

Resolution, also called step size, is the smallest possible change in movement that a motion system can detect (Figure 6). The resolution is determined by capability of the motion system and feedback mechanism (encoder). It is typically specified by the resolution measured at the encoder. However, this is only a measurement of the current relative positions of the encoder scale and the encoder read head. Factors such as encoder mounting location relative to the end effector, thermal expansion, frequency of encoder reading, friction and hysteresis (backlash) are used to determine an actual position of the motion system at any given instant. The resolution of a system can indicate lower boundary of repeatability and generally better resolution can result in better accuracy. But resolution by itself does not provide accurate indication of actual performance.

Dynamic versus static condition of the motion system becomes important when examining the actual end effector (dispense valve) position at the instant of fluid dispense. A system can be considered to be in a static condition when it has fully stopped moving and any residual oscillations from a prior move have died out. In a static condition, the encoder read position should closely correlate to the end effector position as there should be little to no relative motion between the two positions. However, it will require some settling time to achieve such a condition and thus negatively affect productivity (units per hour, UPH) of the system to achieve maximum accuracy. If the system dispenses before any such oscillations have com-

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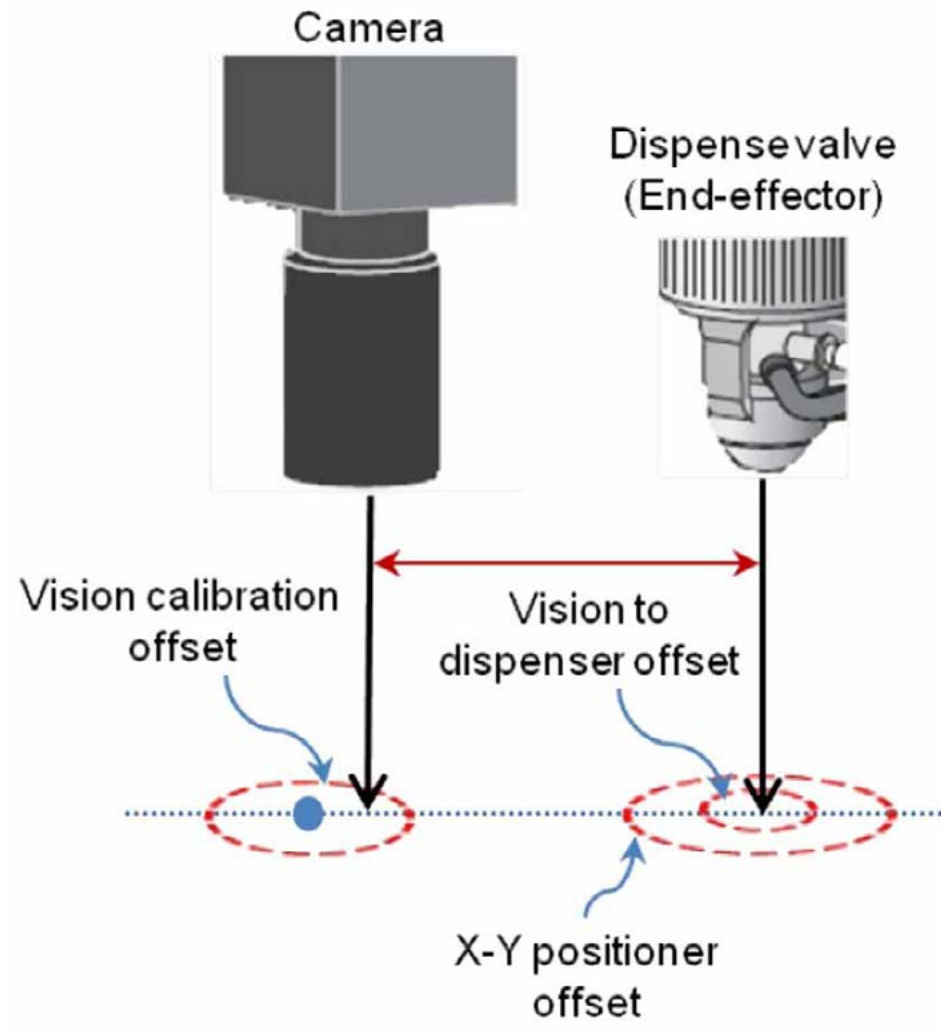

Figure 7: Camera to dispense valve offset.

pletely died out or the system is dynamically moving (dispensing on-the-fly), there is some induced error in the read position of the system at the encoder and the end effector's actual position. This error will then translate to some level of degradation of the accuracy of the actual dispensing of the equipment.

End Effector and Fluid

The end effector and fluid type can further affect the accuracy and repeatability specifications of a given dispensing system. Valve type can affect the operation of the dispenser as a whole and thus impact the dynamic versus static conditions. The mass of the valve and the fluid reservoir will affect the inertia of the system. Additionally, for valves or applications that require a much tighter dispense gap between the substrate surface and the dispensing tip, a system must move in the X-Y position then move down in Z position. This pause to allow motion in the Z-axis acts as an artificial settling time and can improve the actual dispense accuracy. Similarly, the gap between the dispense tip/orifice and the substrate can create some minor offset in the fluid position if the fluid does not eject vertically down from the dispense tip to the substrate. In such a case, having a larger dispense gap introduces a larger X-Y error.

Vision System

Most automated fluid dispensers today incorporate some means of a vision system to identify target fiducials on a substrate part to locate where to dispense. As a result, the ability of a dispenser to accurately find and locate a fiducial factors into the total system accuracy. Vision system accuracy itself has many factors affecting proper fiducial capture and finding, some of which are tied to the motion system. The frame-capture time and the correlation of a frame capture to a specific position in the dispenser's X-Y motion area creates similar issues to those previously mentioned in the motion system section. In most cases, the camera and end effector dispense point are mechanically offset from one another. In such cases, the system software must calibrate the distance between these two positions and can create an offset error if the two positions vary relative to each other or the calibration is too coarse (Figure 7).

In addition to this, the pixel-to-micron resolution of the vision system affects the system's inherent ability to adequately locate a fiducial feature similar to the motion system encoders. The vision system algorithm's ability to consistently locate the target position within the captured image then affects the target positioning for where to dispense the fluid. Substrate and fiducial imaging also depends upon having adequate lighting to create sufficient contrast in a captured image for the software to correctly identify the fiducial position. Thus, even with perfect motion system accuracy, if the vision system does not properly target the correct position, the total system accuracy can suffer.

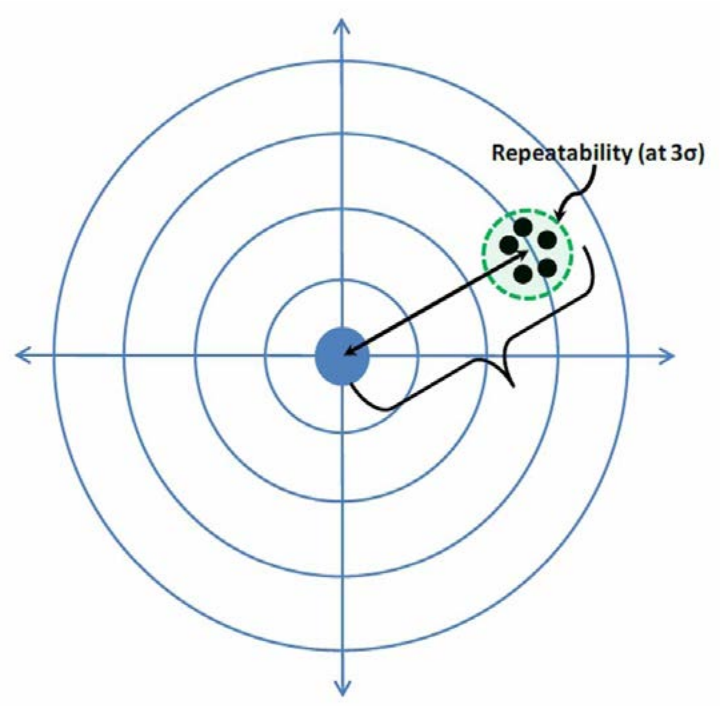

Figure 8: Total system accuracy.

Interpreting Accuracy and Repeatability Specification

In evaluating performance specifications, it is important to have clear information on how claims to dispensing system specifications are obtained. Comparing data obtained under different conditions can make specification comparison difficult and can also lead to incorrect conclusions.

Artificially high positioning accuracy and repeatability could be achieved when the equipment is operated below normal speed, for example. Therefore, the evaluator must understand actual conditions for the stated specification:

- Does the specification represent a best-case scenario or a normal operating condition?
- What is the data spread of the claimed specification?
- Is the specification achieved at the positioning sensors or at the fluid dispense location?

Rather than theoretical capability at the positioning sensors, true system positioning specification is the measured capability at the fluid dispense location. True system positioning specification considers factors beyond X-Y positioning accuracy and repeatability. It also takes into consideration the effects of calibration, vision (camera) system resolution and the offset between vision system and actual dispensing position. Figure 8 illustrates total system capability at the fluid dispense location in which the final system accuracy reflects both the accuracy (based on the sample set mean) and repeatability to achieve results around that mean position.

Conclusion

Accuracy and repeatability are important factors in determining fluid dispense capability. They are often the key attributes to evaluate whether equipment can meet target process parameters. However, claimed specification numbers are highly dependent on underlining conditions. Therefore, when comparing specifications between two systems, it is crucial to understand the complete story behind the specification. It is always recommended to check the conditions under which the claimed accuracy and repeatability are specified to determine true system specification and to be able to compare two systems equally. **SMT**

Big Ideas on...

...Miniaturisation

By Clive Ashmore, Mark Whitmore and Jeff Schake
DEK PRINTING MACHINES LTD

SUMMARY: The SMT print process is now very mature and well understood. However, as consumers continually push for new electronic products, with increased functionality and smaller form factor, the boundaries of the whole assembly process are continually being challenged.

Abstract

The next generation of miniaturised SMT devices waiting to make their mark will require the assembly community to rethink its processes and toolsets. The feature sizes that are involved in this new wave of miniaturisation are sub-200 microns. To put this into context, only a decade ago this would have been considered a Semicon domain.

Of all the process involved within the surface mount assembly process the printer is certainly the most sensitive to these changes. But it's not only about printing miniaturised features—the process engineer has to balance miniaturisation with the requirements of "standard" technology. Thus we are experiencing the age of heterogeneous assembly.

Therefore, the miniaturisation program is causing the print process to be challenged in new ways, especially the impact on the available process window available to achieve high-yield heterogeneous assembly.

This paper will investigate the impact of miniaturisation and heterogeneous assembly on the print process and strategies for assemblers to keep one generation ahead. In recent research work, actual paste deposit volumes and transfer efficiency have been monitored and compared for both square and round apertures with area ratios ranging from 0.20–1.35. This covers apertures sizes of between 100 and 550 microns in a nominal 100-micron thick stencil foil. In addition, the effect of ProActiv ultrasonically activated squeegees has been assessed as part of the same experiment. A further com-

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parison has also been made between type 4 and type 4.5 solder paste as well.

The data presented here will help provide guidelines for stencil aperture designs and strategies for ultra-fine pitch components such as 0.3CSPs.

Introduction

Miniaturisation raises a number of issues for the stencil printing process. How small can we print? What are the tightest pitches? Can we print small deposits next to large for high mix technology assemblies? How closely can we place components for high density products? How can we satisfy some of the cost pressures through the whole supply chain and improve yield in the production process?

Today we are operating close to the limits of the stencil printing process. The area ratio rule (the relationship between stencil aperture opening and aperture surface area) fundamentally dictates what can and cannot be achieved in a print process. For next-generation components and assembly processes these established rules need to be broken!

New stencil printing techniques are becoming available which address some of these challenges. Active squeegees have been shown to push area ratio limits to new boundaries, permitting printing for next-generation 0.3CSP technology. Results also indicate there are potential yield benefits for today's leading-edge components as well.

An increasingly important part of the overall equation that is often overlooked is stencil aperture shape and design. With shrinking area ratios, every cubic micron of solder paste that can be printed is becoming critical. For a given aperture area ratio a square aperture design provides the opportunity to deposit 21.5% more than its circular counterpart. When working with sub-0.5 area ratio apertures this becomes very significant.

The work reported here represents the start of a series of experiments to help further understand the significance of square vs circular aperture formats, together with the impact of other material factors, and to ultimately provide design guidelines for ultra-fine pitch printing.

Stencil Printing Rules

As illustrated in Figure 1, the area ratio calculation in its simplest form is a ratio between the aperture opening area and aperture wall surface; therefore the factors that make up an aperture, stencil thickness, aperture diameter, width and length all influence the resultant area ratio. With these two examples, we can observe the effects. A stencil of 100 microns and a circular aperture of 240 microns would result in an area ratio of 0.6; by changing the diameter to 200, the area ratio would now be calculated

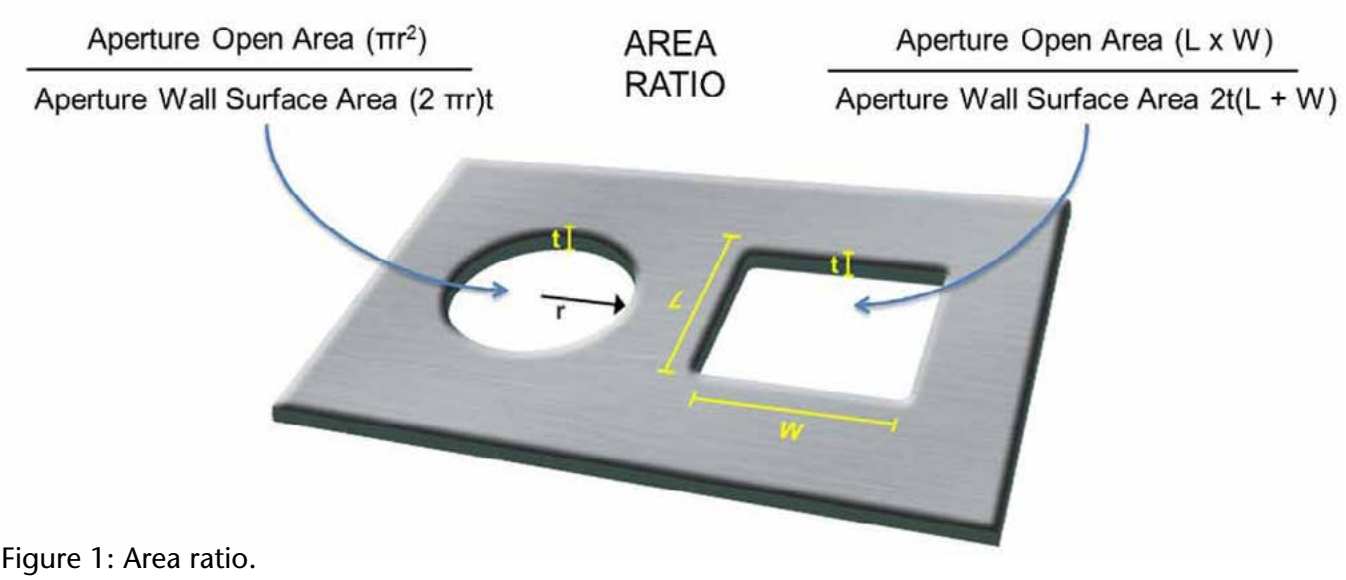

Figure 1: Area ratio.

as a value of 0.5. Needless to say the act of calculating area ratio simply allows the engineer to quickly register an apertures dimension and produce an integer. The significance of this value is explained in the next section.

Solder Paste Transfer Efficiency: Today

For many years, the design of stencil apertures has been based around the original IPC-7525 specification[1] which recommended that aperture area ratios should be greater than 0.66 for acceptable stencil printing (to achieve in excess of 70–75% transfer efficiency).

The historical transfer efficiency curve in Figure 2 is generally accepted as a point of reference for where the industry was back in the late nineties and is still used widely today as a baseline for setting up a process.

In recent years, though, a tremendous amount of research and development has taken place with solder paste materials, stencil technologies and process enhancements to improve paste transfer efficiency. Much work has been done by Ashmore, et al.[2], Mohanty, et al.,[3] and Babka[4] to name but a few, regarding the importance of squeegee angle to paste transfer efficiency. Many research dollars have been spent on looking at stencil manufacturing techniques, stencil materials and stencil finish[5,6,7,8,9]. Recently nano-coated stencils have been in vogue[10,11], and much work has been conducted by the current authors with ultrasonic squeegees[12,13,14].

Taking all these changes and improvements into account, then with a fully optimised process the paste transfer efficiency curve (Figure 2) is a truer reflection of where the SMT printing industry is today.

Whilst some of these technology advancements are recognised in the latest IPC-7525B15 specifications, it is clear that we are operating on the boundaries of existing area ratio rules for today's leading-edge components (Figure 3). Although many individual operators are able to achieve a stable, capable process with these fine-pitch components, extreme care and control over materials is required. In the future, if trying to incorporate 0. 3mm pitch CSPs into existing processes, then stencil apertures with area ratios of approximately 0.4 will be required, which are challenging and beyond today's printing rules (Figure 3). Anything that can be done to assist and optimise the printing process for sub-0.5 area ratio processes will therefore greatly benefit the electronic assembly process.

Experimental: Outline

Thirty-board print runs were conducted using a test pattern consisting of both circular and square apertures. Individual experiments were run with and without activated squeegees and with both type 4 and type 4.5 solder paste.

A DEK Horizon automatic stencil printer

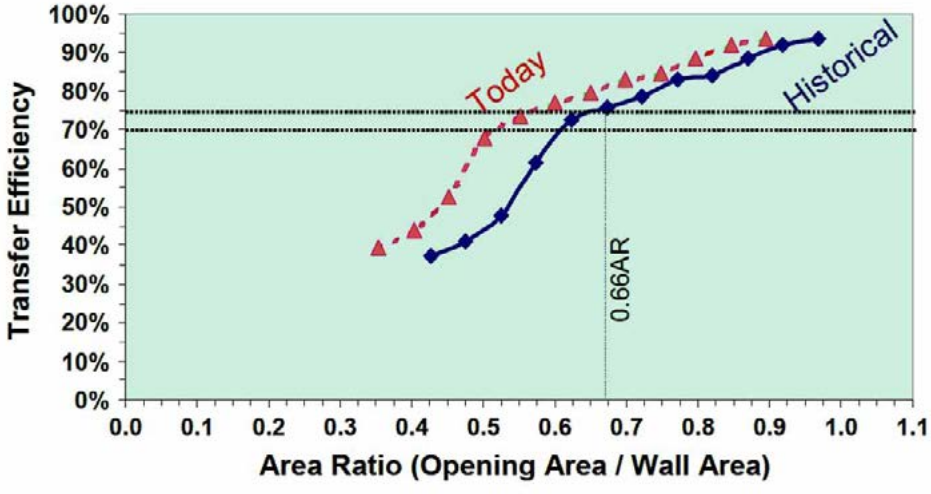

Figure 2: Typical solder paste transfer efficiency. This is a comparison between historical capabilities and today's.

BIG IDEAS ON MINIATURISATION *continues*

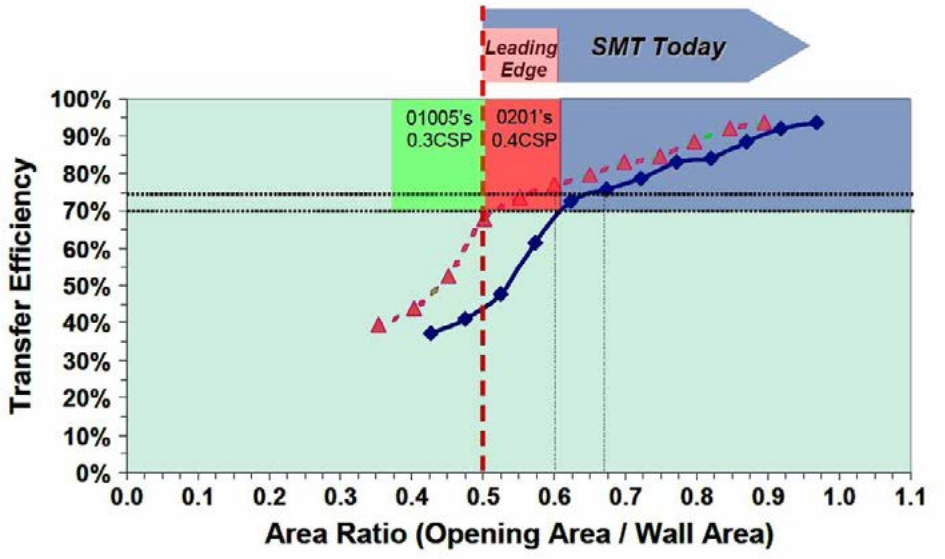

Figure 3: Area ratio requirements for current and future component technologies.

fitted with a ProActiv ultrasonic squeegee system was used to print a test pattern through an industry standard 100-micron-thick laser-cut stainless steel stencil. Printed deposits were measured for volume using a CyberOptics SE500 fitted with a micropad sensor. The test substrates used throughout the investigation were a set of numbered 1.6 mm thick, FR-4 boards. During the print cycle the test substrates were secured in place with a dedicated vacuum tooling plate.

The same squeegee assembly together with 170 mm metal blades, with 15 mm overhang, were used for all testing in both the standard and activated print mode. For a standard print process the ultrasonic capability was simply disabled. Prior to each test run the squeegees were automatically calibrated.

Industry standard lead-free type 4 and type 4.5 solder pastes from a single solder paste vendor were used for printing.

Test Substrate & Stencil Design

An example of the test substrate used is shown in Figure 4. The simple design contains a range of industry standard components. However, for the purpose of this experiment, focus was placed on the four area arrays highlighted in Figure 4. These arrays consist of 0.5 mm diameter pads on a 1 mm pitch. With the corresponding stencil design, a combination of

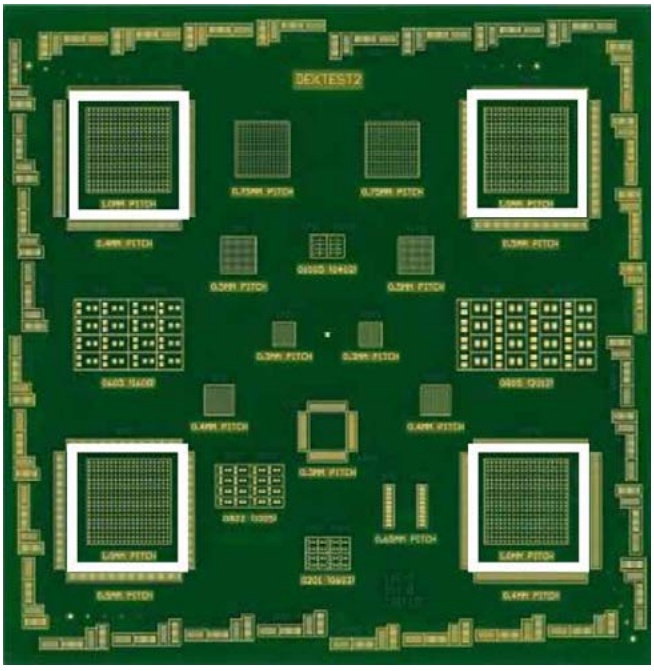

Figure 4: Test substrate with the four arrays used for the reducing array apertures highlighted.

square and circular apertures was incorporated with reducing aperture sizes, ranging between 100 microns and 550 microns (relating to area ratios of between 0.25 and 1.375). The outline of one of these arrays is shown in Figure 5. Each stencil aperture was measured using a semi-au-

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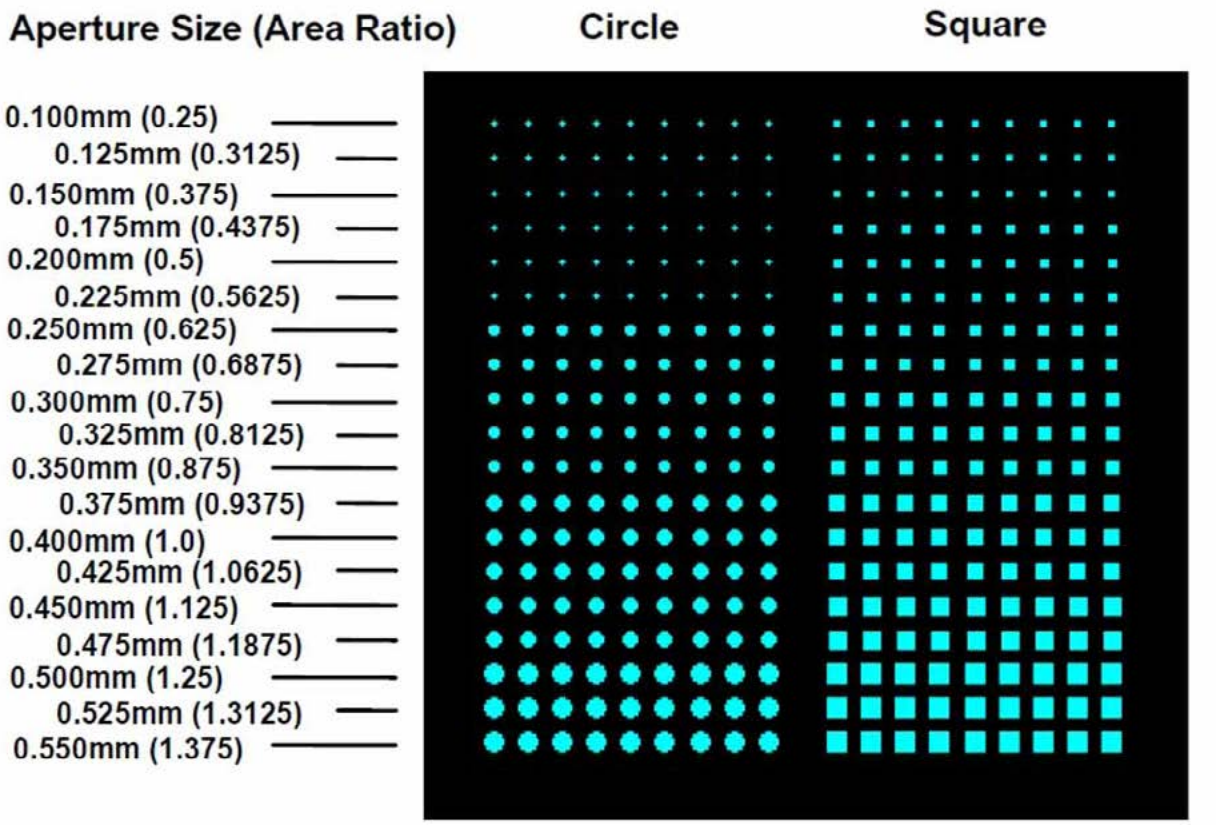

Figure 5: Reducing area array pattern used for generating solder paste transfer efficiency curves. *Note: Figures based on a stencil thickness of 100 microns.*

tomatic coordinate measuring machine (CMM) to enable "true" transfer efficiency curves to be generated (as opposed to using stencil Gerber dimensions).

Experimental Run Procedure

For each experimental condition, 30 consecutive prints were made. After the 10th and 20th prints, the stencil was manually cleaned. Print runs were conducted with and without the ultrasonic squeegee system activated and with both type 4 and type 4.5 solder pastes.

The main process parameters are listed in Table 1. Immediately following each print run the individual boards were measured using a CyberOptics SE 500 inspection tool. The 30 board print runs provided 1080 replicates for each individual aperture shape and design.

Print Speed	50mm/sec
Print Pressure	4kg
Separation Speed	3mm/sec
Separation Distance	3mm
Temperature	21-22°C
Relative Humidity	50-55%

Table 1: Print parameter summary.

Results & Discussion

The first important observation to consider arose from measuring the stencil apertures. The data in Table 2 details the actual measurements made for both the circular and square apertures and compares the actual aperture volume to that of the theoretical volume from the Gerber

dimensions used to manufacture the stencil. Both the top and bottom side of stencil apertures were measured (to take into account any taper), and the average of the two measurements were taken for volumetric calculations.

Typically all apertures were undercut by 10–15 microns. For larger aperture dimensions this is not necessarily a major issue. For example, a 550 circular aperture has a volume of 23.76 nanoliters. The corresponding cut aperture was measured at 540 microns in diameter, with a volume of 22.94 nanoliters, 3.42% less than with its intended Gerber dimensions.

For smaller aperture sizes, though, such a differential can have a significant impact on the volume of the aperture and its area ratio. This in turn can affect transfer efficiency and the final volume of paste deposited. With the nominal 250-micron apertures, the percent of difference in measured volume compared to Gerber dimensions was approximately 10%. The differential increased to 17% with apertures based on a target size of 150 microns.

This highlights the increased importance of stencil design and stencil manufacturing accuracy when considering ultra fine pitch stencils (with aperture area ratios below 0.5). It can be the difference between a successful process and a failure!

The benefits of using ProActiv ultrasonic squeegees have been reported by these authors before[13,14,15]. In this study similar trends were observed. Table 3 provides the average paste transfer efficiency for both circular and square apertures for each of the conditions tested—with/without ProActiv, and with type 4 and type 4.5 solder paste.

Each data point represents the average of 1080 measurements made over the 30 board print run.

For aperture area ratios below 0.5, the use of ProActiv affords an increase in solder paste transfer efficiency over a standard squeegee process. Effectively, the knee of the transfer efficiency curve is kicked out, resulting in the opportunity to work with aperture area ratios down to 0.4, whilst still maintaining paste transfer efficiency above 60%.

With regards to solder paste particle size, the data indicates only small differences (in trans-

Circular Aperture Data					
Gerber			Measured		
Size(um)	Area Ratio	Vol(nl)	Size(um)	Area Ratio	Vol(nl)
100	0.25	0.79	85.5	0.21	0.57
125	0.31	1.23	111.5	0.27	0.98
150	0.38	1.77	137.0	0.34	1.47
175	0.44	2.41	162.5	0.40	2.07
200	0.50	3.14	185.5	0.46	2.70
225	0.56	3.98	215.0	0.53	3.63
250	0.63	4.91	237.0	0.58	4.41
275	0.69	5.94	261.0	0.64	5.35
300	0.75	7.07	289.0	0.71	6.56
325	0.81	8.30	314.0	0.77	7.74
350	0.88	9.62	337.5	0.83	8.95
375	0.94	11.04	361.5	0.89	10.26
400	1.00	12.57	386.5	0.95	11.73
425	1.06	14.19	415.0	1.02	13.53
450	1.13	15.90	440.0	1.08	15.21
475	1.19	17.72	463.0	1.14	16.84
500	1.25	19.63	489.0	1.20	18.78
525	1.31	21.65	516.0	1.27	20.91
550	1.38	23.76	540.5	1.33	22.94
Square Aperture Data					
Gerber			Measured		
Size(um)	Area Ratio	Vol(nl)	Size(um)	Area Ratio	Vol(nl)
100	0.25	1.00	84.5	0.21	0.73
125	0.31	1.56	112.5	0.28	1.29
150	0.38	2.25	137.0	0.34	1.91
175	0.44	3.06	162.0	0.40	2.67
200	0.50	4.00	186.5	0.46	3.53
225	0.56	5.06	212.5	0.52	4.59
250	0.63	6.25	236.5	0.58	5.68
275	0.69	7.56	261.0	0.64	6.92
300	0.75	9.00	286.5	0.70	8.34
325	0.81	10.56	311.5	0.77	9.86
350	0.88	12.25	337.0	0.83	11.54
375	0.94	14.06	361.0	0.89	13.24
400	1.00	16.00	384.0	0.94	14.98
425	1.06	18.06	413.5	1.02	17.37
450	1.13	20.25	436.0	1.07	19.31
475	1.19	22.56	464.5	1.14	21.92
500	1.25	25.00	487.5	1.20	24.15
525	1.31	27.56	512.5	1.26	26.69
550	1.38	30.25	536.5	1.32	29.24

Table 2: Stencil aperture measurements and volume calculations for circular and square apertures compared to Gerber theoretical values. *Notes: Gerber stencil thickness used in calculations = 100 µm. Measured stencil thickness used in calculations = 101.6 µm. 1 nanoliter = 1,000,000 cubic microns.*

Circular Apertures: Average Transfer Efficiency					
Measured		T4	T4	T4.5	T4.5
Size(um)	Area Ratio	Std	PA	Std	PA
85.5	0.21	0.0%	0.0%	0.0%	0.0%
111.5	0.27	0.0%	3.7%	0.0%	6.2%
137.0	0.34	1.2%	41.0%	1.3%	49.9%
162.5	0.40	26.9%	63.8%	28.4%	66.3%
185.5	0.46	59.9%	68.9%	63.3%	71.0%
215.0	0.53	68.4%	72.3%	68.8%	73.4%
237.0	0.58	73.3%	75.7%	72.7%	76.5%
261.0	0.64	79.4%	81.2%	78.3%	81.4%
289.0	0.71	79.2%	80.2%	77.8%	80.6%
314.0	0.77	83.7%	84.7%	81.5%	84.4%
337.5	0.83	86.0%	86.9%	83.3%	86.4%
361.5	0.89	89.6%	90.7%	86.6%	90.2%
386.5	0.95	90.9%	92.3%	87.7%	91.6%
415.0	1.02	92.2%	93.3%	89.5%	92.2%
440.0	1.08	93.2%	94.2%	90.5%	93.3%
463.0	1.14	95.4%	96.4%	92.7%	96.2%
489.0	1.20	94.9%	96.3%	92.8%	96.4%
516.0	1.27	97.5%	99.4%	96.2%	100.6%
540.5	1.33	99.1%	100.3%	99.1%	102.6%
Square Apertures: Average Transfer Efficiency					
Measured		T4	T4	T4.5	T4.5
Size(um)	Area Ratio	Std	PA	Std	PA
84.5	0.21	0.1%	0.0%	0.0%	0.1%
112.5	0.28	0.0%	14.4%	0.1%	23.3%
137.0	0.34	7.3%	52.7%	7.5%	58.3%
162.0	0.40	47.5%	65.2%	52.3%	68.1%
186.5	0.46	63.1%	69.7%	64.1%	72.2%
212.5	0.52	71.0%	74.2%	70.5%	76.3%
236.5	0.58	74.3%	77.3%	73.6%	78.5%
261.0	0.64	79.6%	81.6%	78.2%	82.2%
286.5	0.70	81.6%	83.5%	79.8%	83.9%
311.5	0.77	86.2%	87.7%	83.4%	87.8%
337.0	0.83	88.5%	90.2%	85.4%	90.4%
361.0	0.89	91.1%	92.4%	88.7%	92.3%
384.0	0.94	92.7%	94.1%	90.5%	94.1%
413.5	1.02	93.1%	94.4%	90.6%	94.8%
436.0	1.07	96.9%	99.0%	93.7%	99.5%
464.5	1.14	99.7%	102.6%	95.5%	103.0%
487.5	1.20	104.0%	107.7%	100.4%	107.3%
512.5	1.26	108.8%	112.8%	105.7%	112.6%
536.5	1.32	110.0%	113.0%	108.2%	113.7%

Table 3: Average paste transfer efficiency for various circular and square aperture area ratios; with/without ProActiv (PA) and with type 4 (T4) and type 4.5 (T4.5) solder paste.

fer efficiency) between using type 4 and type 4.5 solder paste. With low area ratios, the net gain of using type 4.5 solder paste was an extra 2–3% in transfer efficiency. Please bear in mind though, that only one solder paste formulation was tested and other type 4/4.5 solder pastes might behave differently.

Whilst transfer efficiency data is a good reference point for the effectiveness of a process, a solder joint ultimately requires a certain amount of solder for a good connection; therefore actual volume is a more critical and useful measurement.

Table 4 provides the average volume of solder paste printed for both circular and square apertures for each of the conditions tested: with and without ProActiv, and with type 4 and type 4.5 solder paste. Again, each data point represents the average of 1080 measurements made over a 30-board print run.

The trends seen in the transfer efficiency analysis (with respect to ProActiv vs. standard squeegee printing and type 4 vs. type 4.5 solder pastes) are still prevalent in the volume data. However, the volume data serves to highlight the difference in printed volume between circular and square apertures.

A square aperture of a given size has a volume that is 21.5% greater than its circular counterpart. Generally, for apertures with area ratios between 0.44 and 1.00, this trend was observed in all print tests irrespective of ProActiv/squeegee and type 4/type 4.5 comparisons. With apertures having area ratios above ~1.00, then the volume increase in paste deposited with a square rose to 29%. This implies that the filling and release dynamics are different with apertures over a certain area ratio, although the exact mechanism was not investigated further.

With apertures having area ratios below 0.40, the differences in actual volume printed became even more significant. The bar charts in Figure 6 detail the paste volume printed (for all experimental conditions) with circular and square apertures having critical area ratios based around the knee of the paste transfer efficiency curve. At the extreme, with aperture area ratios of 0.34, virtually no solder paste was printed with a standard squeegee process, either through a circular or square aperture. By using

ProActiv with type 4 solder paste, a printed volume of 0.61 nanoliters was achieved with a circular aperture design and 1.01 nanoliters with a square aperture. By using type 4.5 solder paste the maximum volume printed was increased to 1.11 nanoliters. This data highlights how ProActiv, together with considered choice of square or circular apertures and type 4/4.5 solder paste, can push the lower limits of the printing process.

Whilst not as extreme, but nonetheless just as significant, the same trends can be seen in the data with aperture area ratios of 0.40 and 0.46. With an area ratio of 0.40 the volume of paste printed ranged from 0.57 to 1.81 nanoliters, depending on process condition. When working towards a specific volume, for example 1.8 nanoliters (which could become typical for an ultra-fine-pitch component), then the significance of aperture design and process choices becomes apparent. Careful selection will have to be exercised to ensure a process can be delivered.

The transfer efficiency and volume data discussed thus far is helpful in understanding the potential scope for future surface mount assembly. But for the full picture, it is also essential to understand the true capabilities and repeatability of a process associated to any material and process choice.

In this respect, the scatter and standard deviation of the experimental data collected was also considered. Focusing in again on aperture area ratios around the knee of the transfer efficiency curve, Figure 7 plots every single data point collected for apertures with area ratios of 0.34, 0.40 and 0.46. Simplistically, this gives the engineer a great view of what is happening in a process. The outliers represent potential board level defects and the spread of the data gives an indication of how "in control" the process is.

The charts clearly show the benefits of using ProActiv with low, challenging area ratio apertures. This is exemplified by the data for the 162 µm (0.40AR) aperture. With a standard squeegee process the scatter of data was large (and low) indicating that the process conditions were not capable. By using ProActiv the data set was significantly tightened up with acceptable

Circular Apertures: Average Volume Printed (nl)					
Measured		T4(ø)	T4(ø)	T4.5(ø)	T4.5(ø)
Size(um)	Area Ratio	Std	PA	Std	PA
85.5	0.21	0.00	0.00	0.00	0.00
111.5	0.27	0.00	0.04	0.00	0.06
137.0	0.34	0.02	0.61	0.02	0.75
162.5	0.40	0.57	1.35	0.60	1.40
185.5	0.46	1.64	1.89	1.74	1.95
215.0	0.53	2.52	2.67	2.54	2.71
237.0	0.58	3.29	3.39	3.26	3.43
261.0	0.64	4.32	4.41	4.26	4.42
289.0	0.71	5.28	5.34	5.18	5.37
314.0	0.77	6.58	6.67	6.41	6.64
337.5	0.83	7.81	7.90	7.57	7.85
361.5	0.89	9.35	9.46	9.03	9.40
386.5	0.95	10.83	11.00	10.45	10.92
415.0	1.02	12.67	12.83	12.30	12.67
440.0	1.08	14.39	14.54	13.97	14.41
463.0	1.14	16.32	16.50	15.86	16.45
489.0	1.20	18.12	18.37	17.71	18.39
516.0	1.27	20.73	21.11	20.43	21.37
540.5	1.33	23.09	23.39	23.10	23.92

Square Apertures: Average Volume Printed (nl)					
Measured		T4(□)	T4(□)	T4.5(□)	T4.5(□)
Size(um)	Area Ratio	Std	PA	Std	PA
84.5	0.21	0.00	0.00	0.00	0.00
112.5	0.28	0.00	0.19	0.00	0.30
137.0	0.34	0.14	1.01	0.14	1.11
162.0	0.40	1.27	1.74	1.40	1.81
186.5	0.46	2.23	2.46	2.27	2.55
212.5	0.52	3.26	3.41	3.24	3.50
236.5	0.58	4.22	4.39	4.18	4.46
261.0	0.64	5.51	5.65	5.41	5.69
286.5	0.70	6.80	6.97	6.65	6.99
311.5	0.77	8.50	8.65	8.22	8.66
337.0	0.83	10.21	10.40	9.85	10.43
361.0	0.89	12.07	12.23	11.74	12.22
384.0	0.94	13.89	14.10	13.55	14.09
413.5	1.02	16.18	16.41	15.73	16.47
436.0	1.07	18.71	19.13	18.09	19.22
464.5	1.14	21.85	22.50	20.94	22.59
487.5	1.20	25.10	26.02	24.24	25.92
512.5	1.26	29.02	30.11	28.21	30.06
536.5	1.32	32.18	33.06	31.65	33.24

Table 4: Average volume deposited for various circular and square aperture area ratios; with/without ProActiv (PA) and with type 4 (T4) and type 4.5 (T4.5) solder paste.
Notes: Values have been rounded to 2 decimal places. 1 nanoliter = 1,000,000 cubic microns.

BIG IDEAS ON MINIATURISATION *continues*

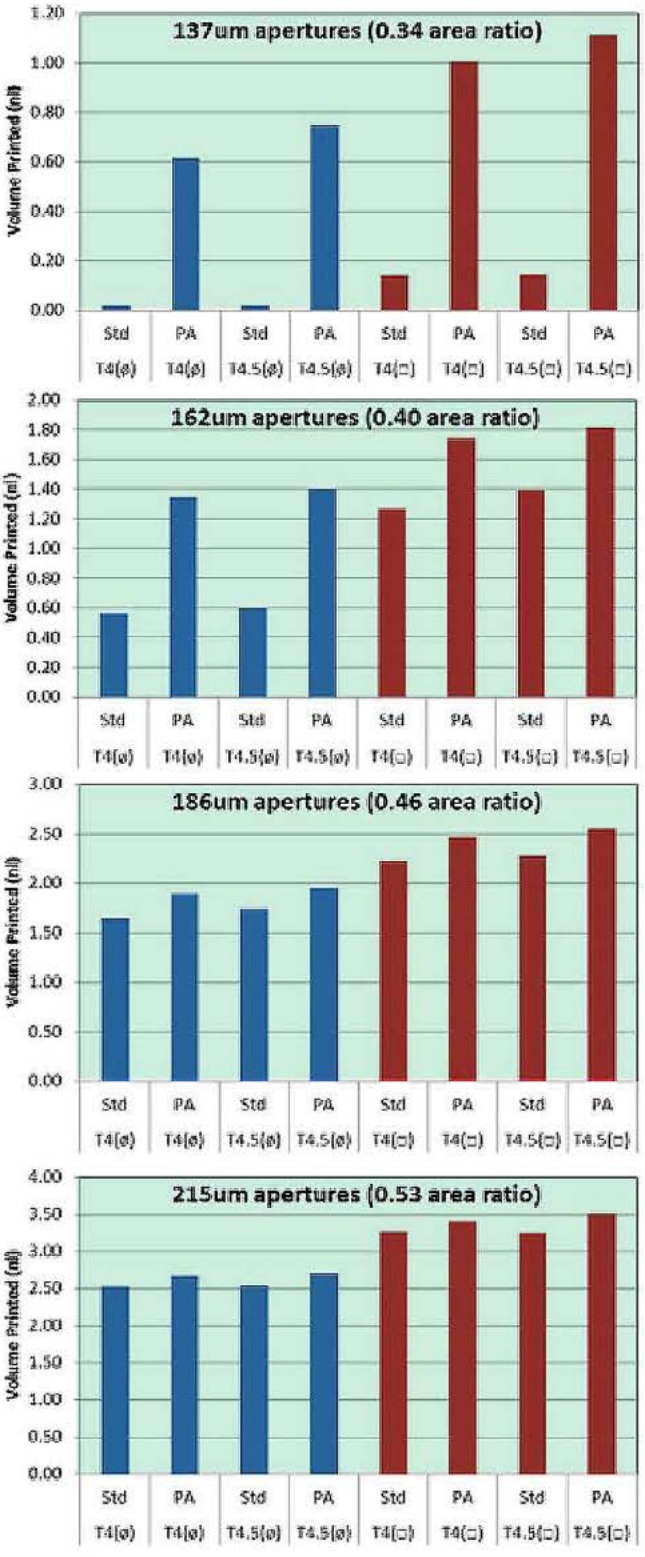

Figure 6: Solder paste volume deposited for specific area ratios. Comparing circular (ø) and square ( ) apertures; with/without ProActiv (PA) and with type 4 (T4) and type 4.5 (T4.5) solder paste.

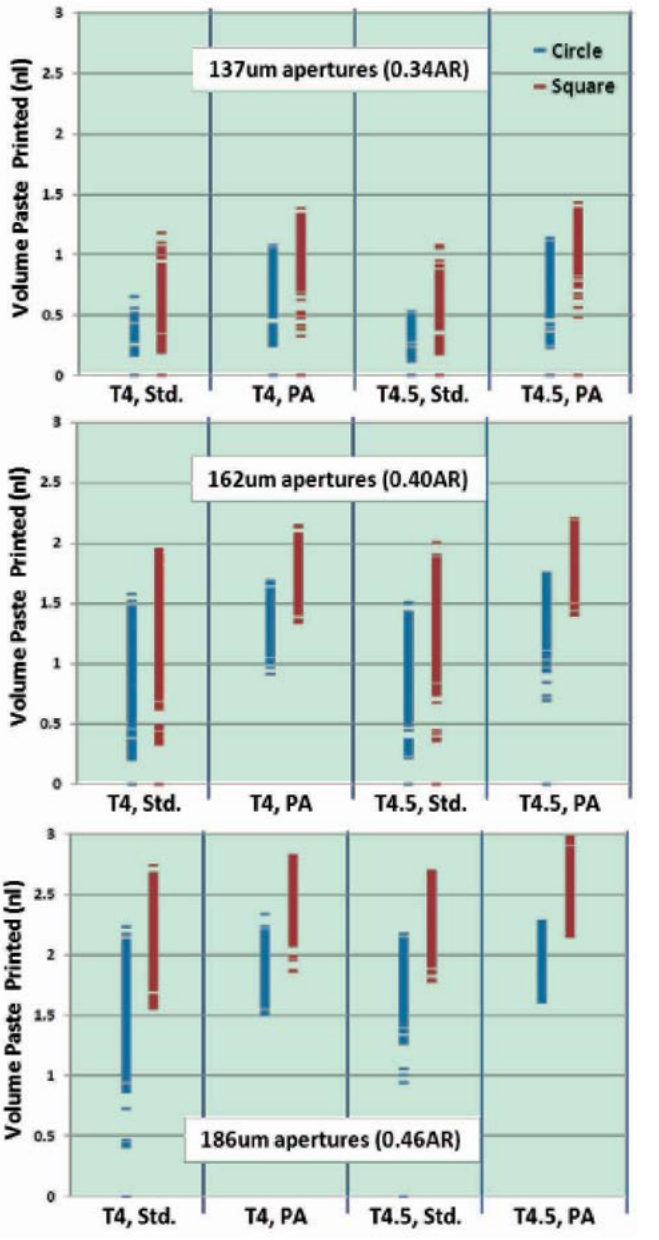

Figure 7: Solder paste volume scatter plots for apertures with area ratios of 0.34, 0.40 and 0.46. Comparing circular (blue) and square (red) apertures; with/without ProActiv (PA) and with type 4 (T4) and type 4.5 (T4.5) solder paste.

volumes being deposited. This phenomena was noted with other low area-ratio apertures.

The standard deviation charts in Figure 8 help provide a process capability view across all area ratios and process conditions tested. In these charts, standard deviation is quoted

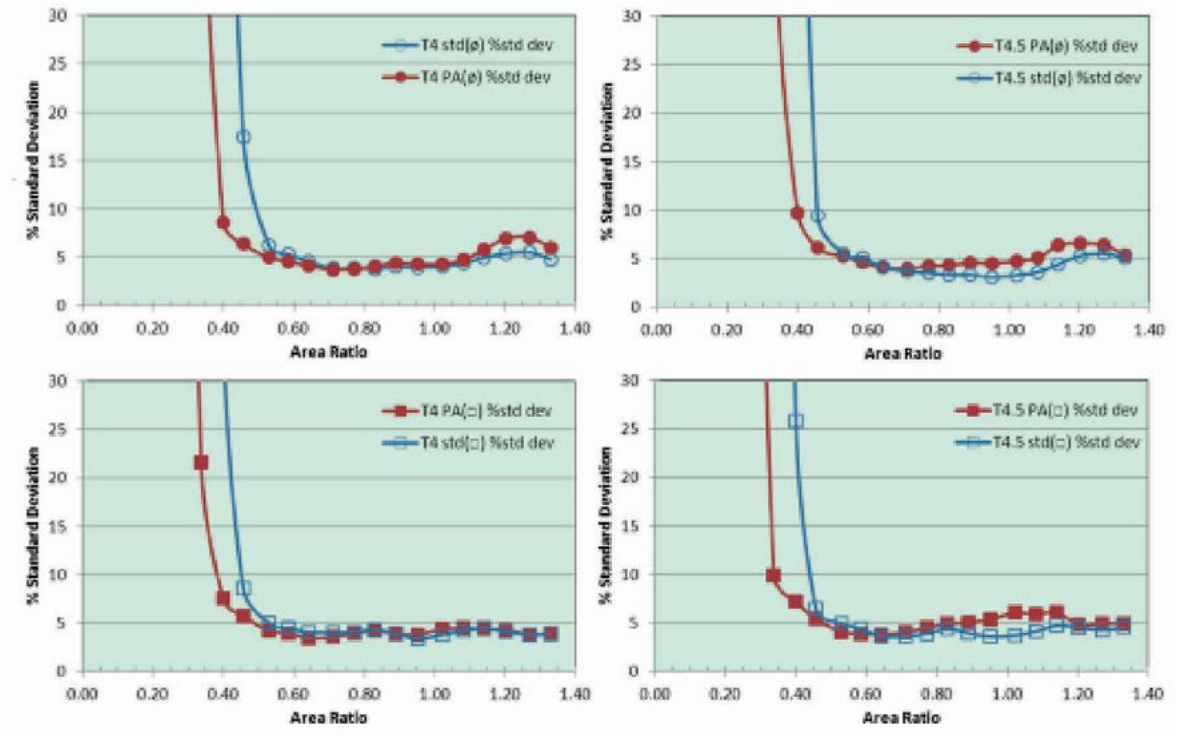

Figure 8: Standard deviation charts.

as a percent of the actual volume printed. It is generally accepted that if the percent standard deviation is maintained below 10%, then a process is in control. As can be seen from the charts, this becomes a more discerning measure with decreasing area ratio.

Generally, each experimental run held a 5% standard deviation with apertures having area ratio's down to 0.53, indicative of a stable process to that point. Below 0.53, then subtle differences were noted. Figure 9 homes in on the percent standard deviation data for aperture area ratios below 0.6. Comparing all experimental runs within the same chart, the curves fall into two distinct groups. The curves to the left were the result of using ProActiv. It can be seen that ProActiv enabled process percent of standard deviation to be kept below 10% with apertures having an area ratio down to 0.4. Under one specific condition, ProActiv with a square aperture design and type 4.5 solder paste, the process was capable down to an aperture area ratio of 0.34. In contrast the standard squeegee processes bottomed out with area ratios of approximately 0.46.

In comparing aperture shape, the data indicated that lower area ratios designs can be used with square apertures (compared to circular apertures) and still maintain a process with a percent standard deviation under 10%.

From the data presented here, it is apparent that there are many interacting circumstances to consider when designing a process, and these are assuming greater importance as we push into the realms of sub-0.5 area ratios. Ultimately, each component requires a defined amount of solder paste for good joint assembly so this will dictate requirements. However, the mechanism by which this is delivered, as shown from the experimental data here, can vary depending upon aperture design, solder paste material used and printing process utilised.

Summary

The next generation of ultra-fine-pitch components will place extreme demands on the stencil printing process. The requirement for printing solder paste through stencil apertures with area ratios below 0.5 will become common

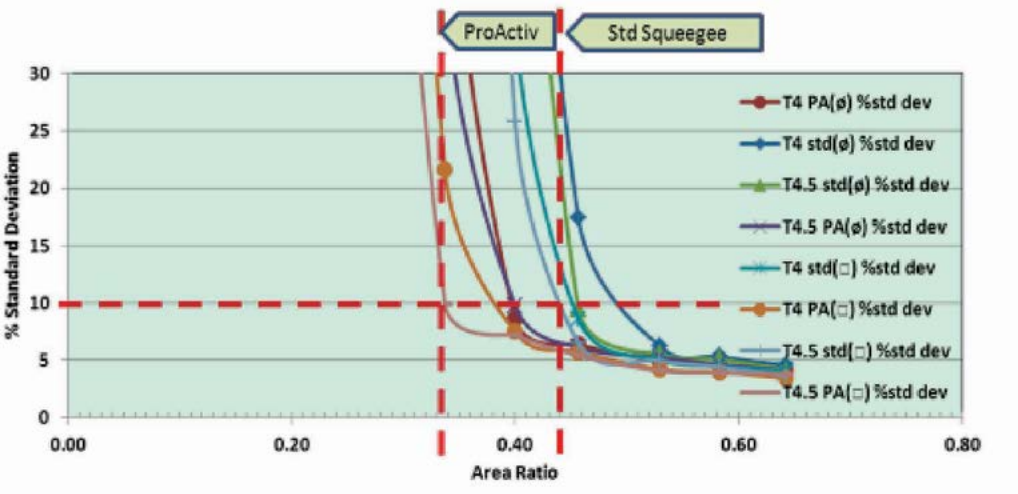

Figure 9: Percent standard deviation plots for all experimental runs.

place. The data presented here indicates that with judicial choice of stencil design and materials it will be possible for designers to work with aperture area ratios down to 0.4.

To optimise a process it is becoming increasingly important that an engineer has a good understanding of stencil aperture design specification, material properties and process options/aids available to him. The interaction between these facets is becoming more complex and critical to the successful implementation of a process. **SMT**

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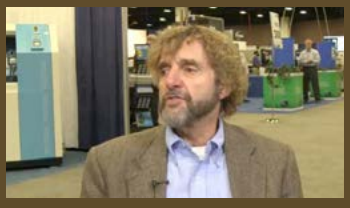
Video Interview

The 10 Deadly Sins of Electronics Manufacturing

by Real Time with... SMTAI



Jim Hall, principal of ITM Consulting, discusses his SMTAI workshop that focused on the 10 deadly sins he's found while auditing manufacturers. Lust, ignorance...it's all there!

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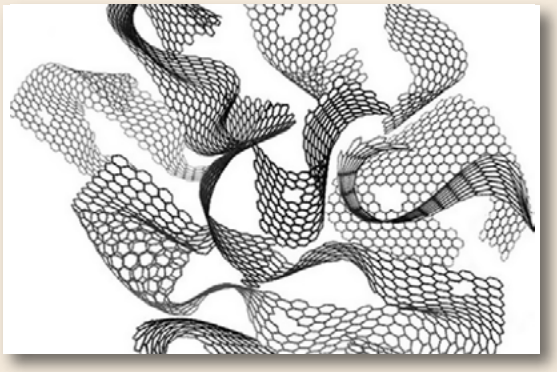
Reduction in Electromagnetic Analysis Time of Graphene-based Structures

The boundary condition can be very important in the analysis of very thin structures, including graphene. An Iranian researcher from Sharif University of Technology succeeded in significantly reducing (a few hundred times) the time required for electromagnetic analysis of graphene-based structures by presenting a novel approximate boundary conditions for magnetic field.

"In this research, we presented an approach for fast analysis of alternate arrays of graphene bands. The analysis of the arrays is very time-consuming through the methods based on Fourier's model. We present a method that can reduce the time required for the analysis of such structures a few hundred times," the researcher said.



The process increased the convergent rate of Fourier Modal Method (FMM) in the analysis of arrays consisting of graphene bands. FMM is one of the most common methods in the analysis of optical structures.

Alternate arrays of graphene have applications in the production of various optical devices, including optical sensors, light sorbents, lenses with the ability higher than diffraction limit, and terahertz supermaterials. Obviously, it is mandatory to employ a fast device to analyze such structures to design them.

Latest results of the research showed that the structure could play the role of an element of electrical circuit, and the mentioned element was characterized.

Results of the research have been published in details in Optics Letters.

SMTonline Supplier/New Product News Highlights

Indium Introduces New Lead-free Solder Paste

Tim Jensen, global product manager for PCB assembly products, says "Our customers have been asking for a high-performance solder paste that combines excellent printability with probe-testability. This solder paste delivers on all counts."

Alpha Facility Certified as Compliant Conflict-free Smelter

"As the leading global supplier of soldering materials, Alpha acknowledges the importance of the conflict minerals legislation and its impact on the global electronics supply chain," says Tom Hunsinger, director of global product management.

Enhanced DYMAX Spot Cure System Available at Intertronics

A new iteration of the DYMAX BlueWave 200 high-intensity spot curing system was announced recently by their sales partner, Intertronics. This enhanced UV spot curing lamp is versatile, user friendly, and reliable—and consequently of interest for UVA/visible light cure of adhesives, coatings, and encapsulants in the electronics, medical device, opto-electronics, and technology manufacturing industries.

EasyBraid Introduces New In-line Batch Cleaning System

National Sales Manager John Webber introduces a new in-line batch cleaning system from PBT Co. called MODULECLEAN. Built for high-capacity cleaning, the system is a flexible machine for cleaning PCBA, stencil, and other cleaning tasks in the electronics industry.

Intertronics Intros DYMAX UV Cure FIP/CIP Gasket

The company, along with sales partner DYMAX, has introduced a new UV/visible light cure form-in-place (FIP) or cure-in-place (CIP) gasket originally designed for fuel cell sealing applications. Ultra Light-Weld GA-145 is a chemical and moisture-resistant gasket which is formulated to be tack free, yet soft and flexible, with low outgassing after cure.

New ZESTRON.com: Enhanced Info & Interactive Elements

ZESTRON, the globally leading provider of high-precision cleaning products, services, and training solutions for the electronics manufacturing industry, announced that its new website is live.

Avnet, Power-One Mark 25th Anniversary

"Avnet has spearheaded the charge in our industry toward the adoption of green, alternative and smart energy technologies through our collaboration with the best of the best—and that's Power-One," said Ed Smith, president, Avnet Electronics Marketing Americas.

ACE Unveils Maintainable Drop-jet Flux Dispenser

The new automated drop-jet fluxing head is fully maintainable and available on all KISS selective soldering machines providing precise, on-demand application of flux with no overspray for true no-clean processing. It features rugged construction that handles a wide range of flux chemistries including low pH fluxes down to 2.0, as well as fluxes with solids content as high as 35%.

Koh Young: Strong 3D AOI Market, Revenue Growth

"We've doubled our revenue every year solely based on 3D SPI in the past, because we have provided customers with the true 3D values—process optimization by 3D measurement," said Dr. Kwangill Koh, CEO.

MIRTEC Concludes 2013 with 17% Growth

MIRTEC Co. LTD reports continued growth in sales revenue for its North American Sales and Service Division for 2013. "We are very pleased to announce that sales revenue for our North American Division has grown by over 17% with respect to 2012," stated Brian D'Amico, president of MIRTEC Corporation.

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THE ESSENTIAL PIONEER'S SURVIVAL GUIDE

Why Are ERP and MES so Limited in Electronics?

by Michael Ford
MENTOR GRAPHICS CORP.

Enterprise resource planning (ERP) and manufacturing execution systems (MES) are great tools that have brought manufacturing progressively forward, meeting customer and market needs, empowering global operations, and bringing success. Although the price for these tools can cause sticker shock, especially considering the IT muscle needed for their continuous operation, the critical measure of return on investment is compelling—except in the case of electronics manufacturing.

An impenetrable chaos seems to exist within electronics manufacturing that neither ERP nor MES can crack. For sure, the core functionality of these systems applies equally well for electronics, yet somehow, key stubborn issues remain. Many of these poor practices were originally introduced as countermeasures to ensure a smoother production flow. The core issues then become more elusive to solve as operational momentum builds over time. However, most issues can be traced back to the fundamental lack of control of materials on the shop-floor, specifically, the lack of material inventory, integrity and accuracy.

The effect of inventory inaccuracy is unexpected material starvation at key processes and inability to complete planned work-orders. Materials that were expected to be available, as reported by ERP, are not. Management, motivated simply by the need to ensure deliveries are met, decides to increase the overall materials stocks to prevent the starvation, increasing the warehouse and shop-floor material stock-holding. But this action serves only to delay the inevitable result of the continued accumulation of inventory error.

Then the only way to consolidate the mismatch between the ERP view of available materials and the actual physical materials is to

WHY CHOOSE US?

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WHY ARE ERP AND MES SO LIMITED IN ELECTRONICS? *continues*

perform a physical stock count. This is not a simple task because unmanaged materials on the shop-floor need to be counted as well as those in the warehouse. Several kits of materials for many work-orders for each line usually are on the shop floor, as well as partly used materials by the machines and on the machines, including live materials in use and materials not in use in a common family setup. Also, partly used materials are on trolleys reserved for production of other product families, along with partly used materials that are no longer in use, which have not been returned to the warehouse. Partly used materials are often left on the shop floor as an additional buffer-stock in case unexpected materials shortages happen. These are almost always very poorly managed, with many materials lost from the operation.

The complexity of the shop floor materials operation is the key reason why ERP tools are severely challenged to manage inventory accurately. The physical stock count often will expose a 20–40% deviation between physical inventory and that recorded as available in MRP, which is financially very significant given that generally over 80% of the cost of a manufactured electronics product is in the materials. A physical stock count is disruptive to the operation, requiring in many cases downtime of two or more days; with two counts per year, this can contribute a productivity loss of 1–2%.

These poor practices coping with material issues cannot continue in competitive operations. Changes in market-demand patterns are driving increasing product mix and the need for smaller job sizes. More flexibility is also needed as last minute customer demand changes are becoming more common. These factors combine to put increasing strain on engineering resources and materials processes.

Sooner or later, every competitive operation will need to abandon the poor practices built up around the lack of material inventory management. The solution, once poor practices are stripped away, would seem simple: to provide total material control management, over all warehouses and the entire shop floor.

How then can this be achieved, and, if this is so important, why has this taken so long to get kicked off?

Changes in market-demand patterns are driving increasing product mix and the need for smaller job sizes. More flexibility is also needed as last minute customer demand changes are becoming more common. These factors combine to put increasing strain on engineering resources and materials processes.

For a system to provide a total control of materials, fundamental issues need to be addressed. These fall into two main categories, the first of which is the accumulation of spoilage related to the materials supply and consumption:

- **Machine Spoilage:** A significant amount of variable spoilage is created by the SMT machines themselves. Several factors, including small variations in how individual components lie in their supply form, variations in size or even colour, or slight bending of leads for example, can cause the machine to fail to pick-up and place materials correctly. This happens so frequently that almost every SMT machine has the ability to automatically recover from a failed pick-up and simply try again. The spoilage is usually not physically visible or countable because of the small size of the materials and the sheer speed of the machines. Spoilage reports are usually available from the machines, though these need to be accessed in different ways and have proprietary data formats that differ across both vendors and models. There has been persistent resistance toward implementing standards for shop-floor communication. The dominance of SMT vendor's propriety solutions has created a formidable barrier to entry for ERP and MES providers.
- **Handling Spoilage:** Spoilage can occur when putting reels of materials onto feeders or when performing splicing. Whenever materials are handled, spoilage can also occur because of

ESD or physical damage. Damage may also be caused by moisture contamination. All of these should also be declared as a materials loss, but often are not, since they happen regularly and it is not practical to force operators to enter the data manually into ERP.

• **Product Spoilage:** If a PCB becomes damaged, the materials placed on it to the point of where the damage occurred will also need to be fed into ERP, one by one. This is quite a laborious process, which is almost never accurately performed.

• **End of Reel Losses:** Toward the end of reels, operators may be left with a small quantity of materials left on the reel, which they may decide to discard, but will rarely declare this to ERP.

The second category of issue is related to the MRP back-flush methodology. This has been in use probably since the days of the Model T, as the way to account materials that have been consumed to create products, and it's still the most common method used today in electronics. The methodology is to simply multiply the number of the products made by their bill of materials. Significant issues occur with this approach:

• **Alternative Materials:** The purchasing team will usually make sure that there is a choice of supplier for each material, and these choices can often change because of quality issues, supplier relationships, and of course, the relative cost of materials between suppliers. Between each alternative, however, there are small differences in the sizes of materials. SMT engineering will insist that these variations be kept within a tight tolerance, otherwise rejection of components by the SMT machines will increase dramatically. Where tolerance restrictions cannot be met, alternative internal part numbers have to be created and assigned. The declaration back to ERP about which variant of each material, or combination of variants, was used at run-time, across each of the several hundred materials used in a work-order, is rarely done consistently or accurately.

• **Time to Completion:** The ERP system creates a high-level production plan, with the whole production process being split into a series of stages. One of these stages will be the PCB assembly process. The back-flush operation works only at the completion of all products in the work-order through all of the stages. The reality is that PCB assembly processes consists of many operations, many individual steps. Each PCB may require two SMT operations, one for each surface. Then there is AOI and reflow. Pin-through-hole and manual assembly also may need to be performed before the in-circuit test (ICT) operation and even functional test operations. With many products flowing through the PCB assembly stage concurrently, work-orders are split between processes and lines and may even be divided into sub-orders by the production team. The time taken to get all the PCBs of one work-order through to the end of the operation can be long, especially if failures at ICT take time to repair. Although some ERP systems may enhance the back-flush capability to some extent, a significant delay between physical materials being consumed and the usage accounted for within ERP always occurs. During this time, ERP has no idea what count of materials may be available and so has no way to execute risk-free short term changes in the plan.

"The time taken to get all the PCBs of one work-order through to the end of the operation can be long, especially if failures at ICT take time to repair. Although some ERP systems may enhance the back-flush capability to some extent, a significant delay between physical materials being consumed and the usage accounted for within ERP always occurs."

No doubt ERP plays a fundamental role in electronics manufacturing but it cannot be

WHY ARE ERP AND MES SO LIMITED IN ELECTRONICS? *continues*

expected to achieve material inventory integrity without help. MES systems have helped this situation because materials can be tracked throughout the processes. They do not address, however, the routine process generated spoilage and still depend on manual processes to gather additional information for ERP. The "missing link" in the supply chain, the connection to the machines to gather information directly and accurately, has to be a part of the solution. To date, systems linked to machines are limited, because shop-floor tools are often on a machine-vendor proprietary platform, with significant limitations of accuracy and communication ability to be dependable in live production for total material accountability.

Once the material inventory is under control, the poor practices are redundant and can be replaced with lean-manufacturing technologies, such as warehouse-to-warehouse kanban replenishment and just-in-time (JIT) material logistics. ERP operation and performance is enhanced by this additional piece of supply-chain management, with reliable and dependable visibility of material availability as well as the progress of the current plan. Changes in plan to suit changing customer need can be executed with surgical precision. Investment in excess materials stock can be eliminated, space reduced, logistics tasks reduced, all contributing to enhanced competitive performance.

The real question here is not really why ERP or MES are so limited, but really, why are factories so limited when considering their options? Sometimes, operational momentum should be challenged, especially because it is the key factor that will contribute perhaps the most significant effect to the bottom line of the business. Time to boldly go… **SMT**

Michael Ford is senior marketing development manager with Valor division of Mentor Graphics Corporation. To read past columns, or to contact the author, click here.

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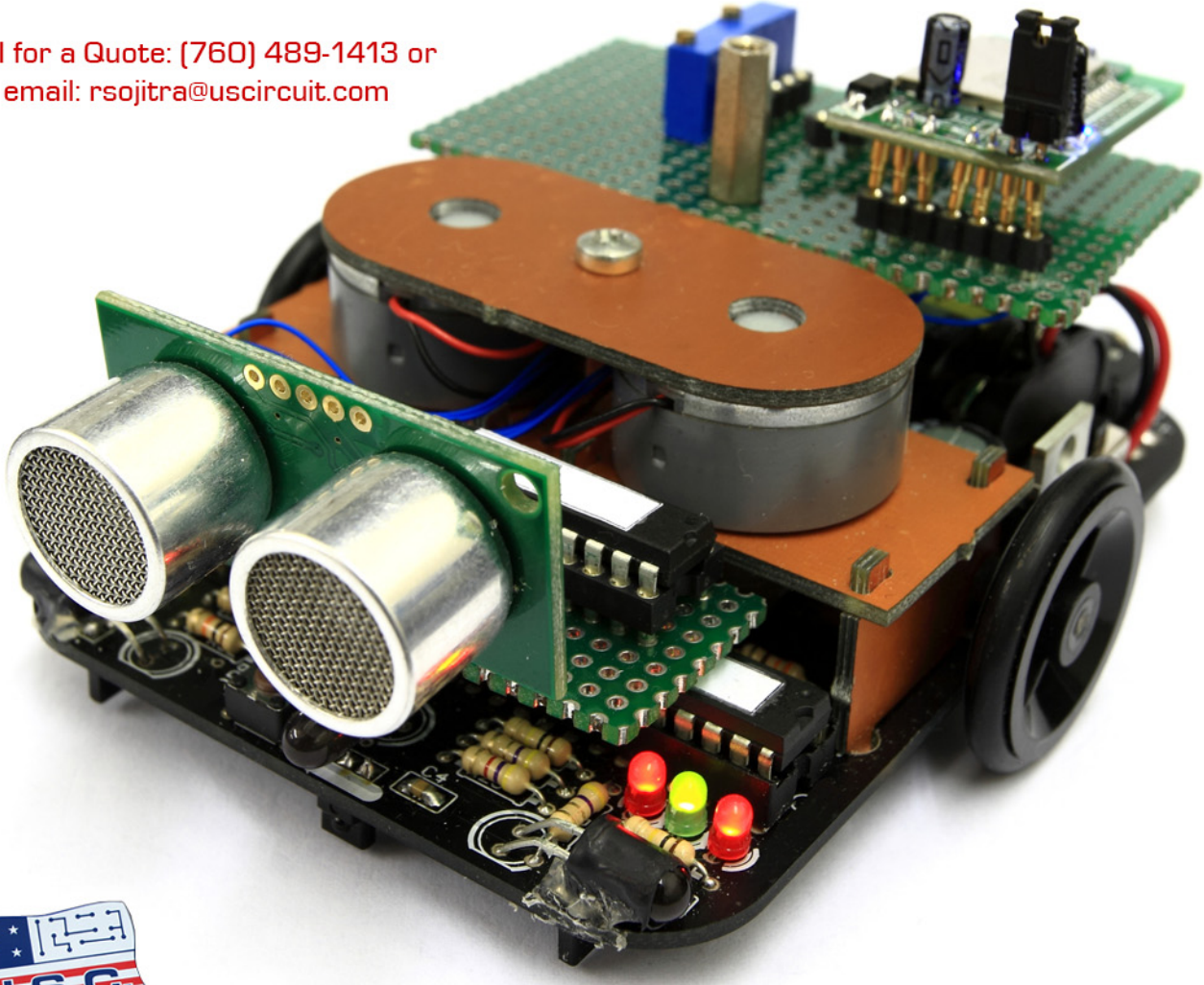

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Mil/Aero007 News Highlights

Ducommun Appoints Joel H. Benkie President

The company's board of directors has unanimously elected Joel H. Benkie, currently executive vice president and chief operating officer, to the position of president, effective January 1, 2014. As president, he will succeed Anthony J. Reardon, who will continue as chairman and CEO.

DOD Releases 2013 Unmanned Systems Integrated Roadmap

"The 2013 Unmanned Systems Integrated Roadmap articulates a vision and strategy for the continued development, production, test, training, operation, and sustainment of unmanned systems technology across DOD," said Dyke Weatherington, the director of the unmanned warfare and intelligence, surveillance and reconnaissance office at the Pentagon.

Kitron Secures Contract from Cassidian

Kitron has received the first orders from Cassidian Optronics GmbH, a worldwide leader in optronic defense and security solutions. The orders cover prototype production of power supply units for one of Cassidian Optronic's target acquisition systems.

Orbit's Power Group COTS Division Nets New Order

Orbit International Corporation, an electronics manufacturer and software solutions provider, announced that its Power Group, through its Behlman Electronics, Inc. subsidiary, has received a new order valued in excess of $695,000 for its COTS division.

Report Outlines Declines in Defense Spending

The decline of defense spending will likely force new revenue streams for the aerospace and defense industry that may include innovations in intelligence, precision strike technologies, and cyber security. "It is anticipated that global revenues for the defense sector will track to similar levels as in the past two years, particularly in the U.S. and Europe," said Tom Captain, DTTL Global Aerospace and Defense Sector leader.

Total Market for Electric UAVs to Top $1B by 2023

The total market value for electric unmanned aerial vehicles will reach over one Billion dollars by 2023 according to findings in the new IDTechEx report, "Electric Unmanned Aerial Vehicles (UAV) 2013-2023."

Global Electronic Warfare Market to Reach $12.15B in 2014

Research and Markets has announced the addition of the Electronic Warfare Market Forecast Analysis (2014–2020) report to their offerings. The global electronic warfare market is estimated to be $12.15 billion in 2014 and is expected to register a CAGR of 4.50% to reach $15.59 billion by 2020.

Perimeter Security Market to Reach $17.7 Billion by 2018

The report, "Perimeter Security Market [by System (Intrusion Detection Sensor, Video Surveillance, Communication/Alarm and Notification, Access Control System), by Deployment (Fence Mounted, Buried, Open Area)]—Worldwide Market Forecasts and Analysis (2013-2018)," defines and segments the global perimeter security market into various sub-segments with in-depth analysis.

Non-lethal Weapons Market to Grow at CAGR of 5.22%

The analysts forecast the global non-lethal weapons market to grow at a CAGR of 5.22% over the period 2014-2018. One of the key factors contributing to this market growth is the increase in global defense budget.

Global Dimensional Metrology Market in Aerospace Industry

New analysis from Frost & Sullivan, "Assessment of the Global Dimensional Metrology Market in the Aerospace Industry," finds that the market earned revenue of $482.9 million in 2012 and estimates this to reach $592.1 million in 2017.

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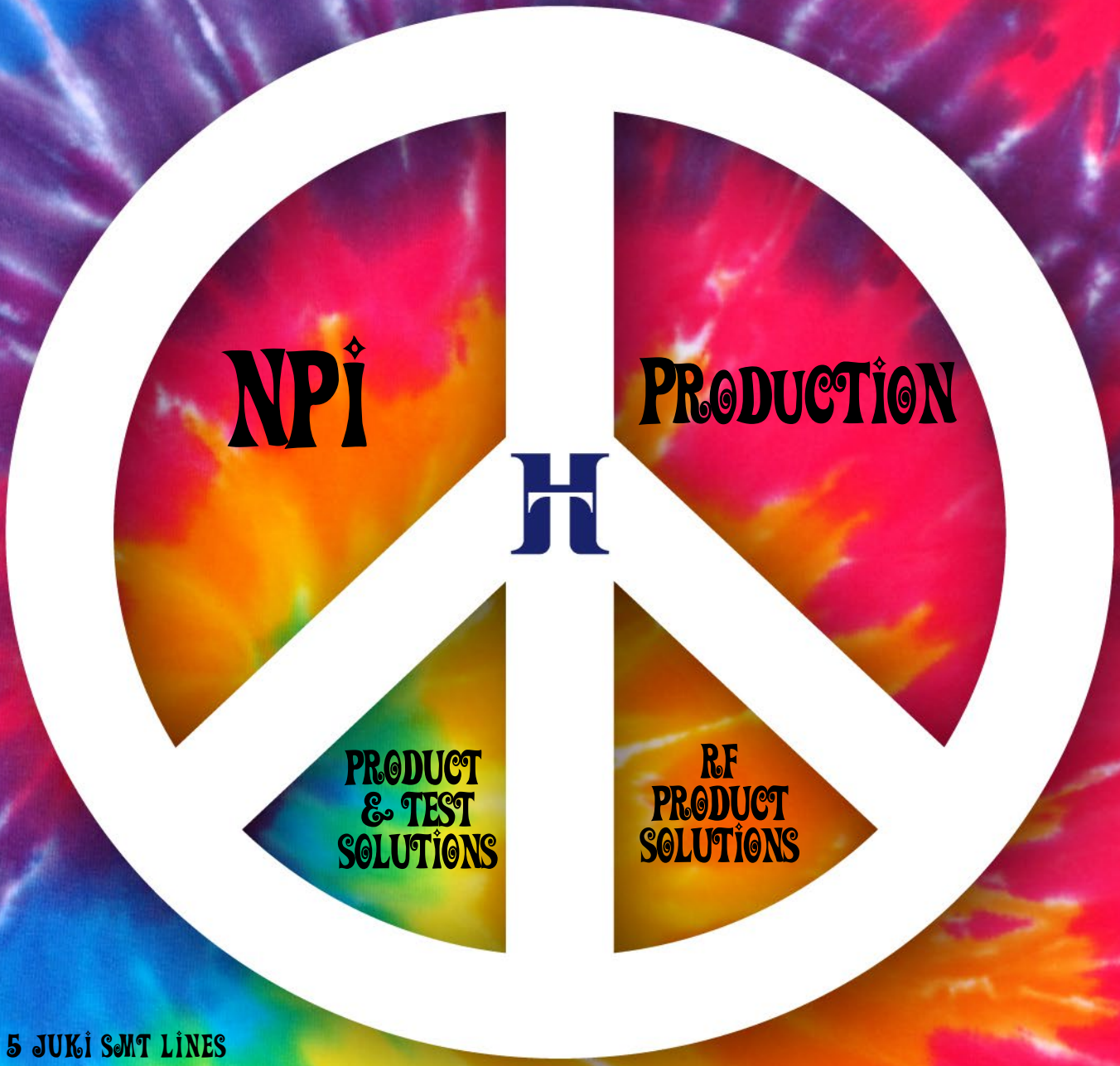

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ZULKI'S PCB NUGGETS

Uncovering Assembly Problems of High-Speed PCBs

by Zulki Khan
NEXLOGIC TECHNOLOGIES INC.

High-speed PCBs have become much more common during the past five years. However, special challenges arise due to unanticipated high-speed issues. Some relate to manufacturing or processes, while others are pure component- or fabrication-based. In particular, highly complex, highly integrated components like FPGAs need close scrutiny. Also, it's important to note that PCBs may use mixed materials like Rogers and FR-4 cores in order to incorporate those high speeds.

The mixed-material board may need prepreg special processing and temperature treatment compared to conventional FR-4 boards. In such cases, extra care must be applied to watch for certain manufacturing aspects. For example, high-speed boards might pass at certain lower spectrum speeds, but begin failing at certain other higher speeds. However, when it comes to regular investigation, those same boards might pass all the run-of-the-mill tests like flying probe, functional tests and ground-to-power short tests.

It becomes worrisome when these boards fail at certain high-speed level bands. Investigation as to the reason(s) why they fail include checking out the process and dissecting it step-by-step and scrubbing the bill of materials (BOM) all the way from A–Z to make sure there are no issues during verification testing.

The high-speed board may be perfect when it comes to BGA assembly. All the balls properly collapse; all the thermal profiles are accurately determined and performed. All soak temperatures, pre-heat, soak and cool-off periods fall within manufacturer limits and ranges. A sam-

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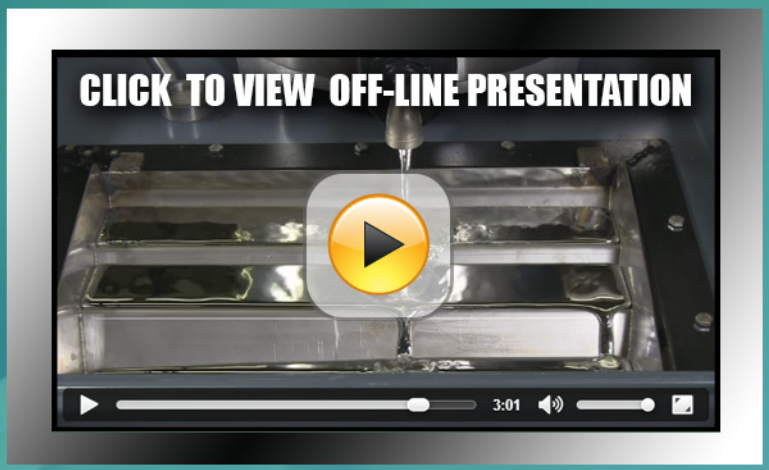

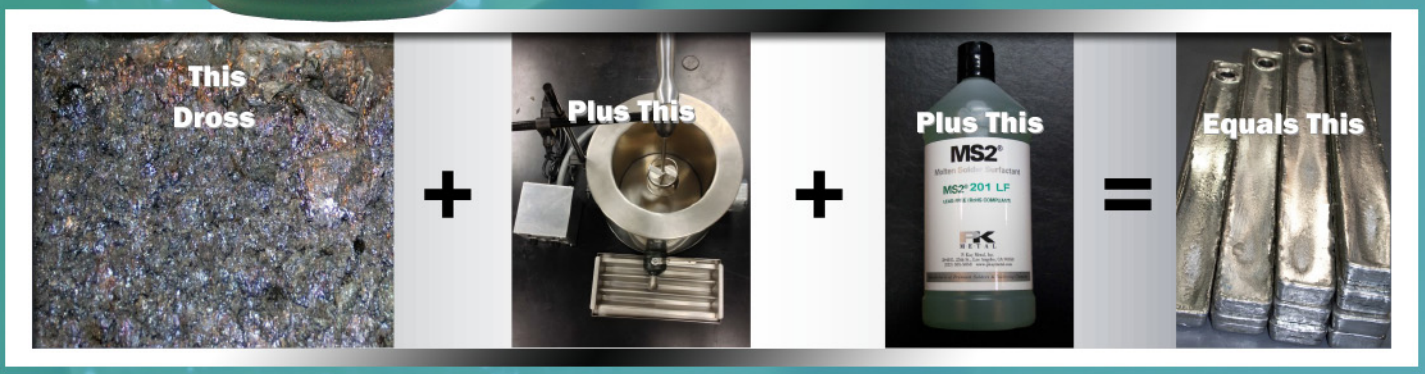

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UNCOVERING ASSEMBLY PROBLEMS OF HIGH-SPEED PCBS *continues*

ple thermal profile is shown in Figure 1. Yet, this high-speed board fails at high speed at the time of system functional level testing in the system.

In the course of the investigation, it must be determined whether or not the material used is straight FR-4, a hybrid, Rogers or polyimide and how it may be affecting the board fabrication process.

Also, when it comes to impedance, you have to look at the coupons run at the fabrication level and the tolerances the OEM provided to the fab shop. Is the fab shop looking at impedance tolerances of 15–20% or so? Or are they running extremely tight tolerances of 5%, +/-3, or something in that range?

If they are running a very tight tolerance, changing even the core of the pre-preg or the laminate is going to adversely affect the impedance calculations. Although there might be some materials that are very similar in characteristics and thermal profiles, they might tweak the stack-up just enough to throw off the calculation at a point where the final product starts failing at the higher speed levels.

Is it the components?

Certain questions dealing with ICs and other components on that questionable board also need to be asked and carefully probed. Let's look at the specifications and how they come about. Was the device or component in ques-

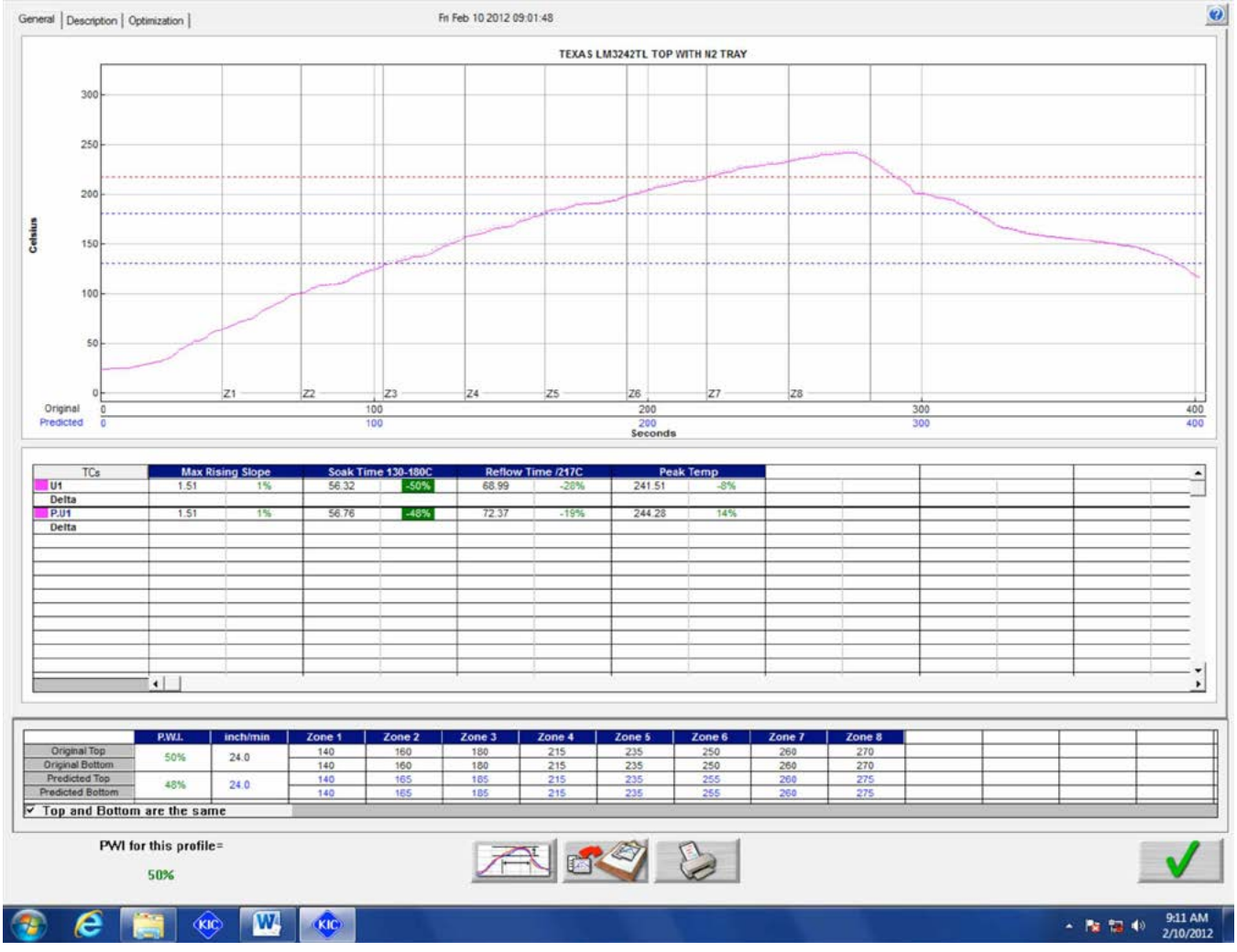

Figure 1: Thermal profile showing the actual peak temperature of U1 at 241.51°C. This profile is for a lead-free assembly and the manufacturer's suggested peak temperature range is 230–250°C.

tion specified during test procedures and verification at the foundry? Or is it one of those devices from the middle of the batch run? This latter one has the potential of being the culprit because it might be slightly marginal when it comes to the required performance at high speeds.

Today's expensive components and their possible shortcomings aren't to be taken lightly. Assembly process engineers and PCB layout engineers must be consulted so they can figure out ways to satisfactorily handle the constraints and other anomalies that chip and component makers factor into their products. Also to be considered is the OEM's speed grade specification for an FPGA design, for example, and when the FPGA was designed. Were constraints properly implemented? What are the consequences if that device is marginal or when it's not out of spec quite yet, but extremely close to the limit?

An example of where a high-speed problem may lie in an FPGA deals with its two sets of pins. One set is composed of hardwired control pins; the other set is user-defined pins. The OEM customer can use those user-defined pins without having specific knowledge of how the FPGA works. However, let's say the FPGA design engineer may have inadvertently, inefficiently, or wrongly programmed and designed some aspect of those pins. A misstep like this can create issues to prevent a PCB from attaining the higher-level speeds.

Also, as a device gets more mature, more data is available. Device binning gets more refined. The duration for which these ICs are built plays a significant role in this scenario. In the initial processes, binning is not mature or refined. When it becomes more mature, you have multiple grades. Some are tops within 5–10%, which are the best of the best.

There is also a wide range of middle-of-the-road components. These are defined at the binning stages and sold at different price points. Finally, there is a third grade, which includes devices that are barely passing, but not expensive FPGAs. The low-grade devices are normally used at highly discounted prices, mostly for consumer products.

"At the top of the list is contacting the company that designed and manufactured that particular FPGA that you think is causing issues on the board you're working on. It makes good business sense for the FPGA maker to become a close partner in this investigation not only because it is to their benefit to determine and fix the problem, but also to properly serve the OEM with a reliable product."

Back to the FPGA

It's fair to say that one or more highly advanced FPGAs are at the heart of most high-speed boards. It's like the elephant in the room. We may conclude the device could have something to do with a high-speed board passing at lower speed, but failing at some higher-level speeds. The FPGA certainly has to be included among the other usual suspects and can have some association with the issues those boards are experiencing.

At this point in the investigation, you have to take certain considerations and actions into account, which are outside the EMS realm and in particular, the responsibility of the EMS company because they're not involved in the manufacture of that FPGA. However, because you are a reputable contract manufacturer (CM) or EMS provider, you must get intimately involved because the PCB is failing on your assembly floor.

At the top of the list is contacting the company that designed and manufactured that particular FPGA that you think is causing issues on the board you're working on. It makes good business sense for the FPGA maker to become a close partner in this investigation not only because it is to their benefit to determine and fix the problem, but also to properly serve the OEM with a reliable product.

But why would an EMS provider with this kind of problem bring it to the chipmaker's attention? You don't have to be a rocket scientist

UNCOVERING ASSEMBLY PROBLEMS OF HIGH-SPEED PCBS *continues*

to figure out that a highly integrated or what used to be called VLSI (very large scale integration) chip like an FPGA could conceivably be at the root of a high-speed PCB manufacturing issue.

Think about it. Today's chip geometries are around 32 nm and continually getting smaller. Those extremely fine geometries are crucial to pack more metal-oxide semiconductor field-effect transistors (MOSFETs) onto the silicon so that millions and millions of those transistors or active devices provide the necessary electronics functions or gates to achieve high performance.

High performance means higher speeds, and that's the name of the game. That's what OEMs demand. It doesn't matter if you're an industrial, consumer, mil/aero, or computer OEM. You need high performance to meet customer requirements.

Meanwhile, at the chip level, those millions of electronic gates in an FPGA generate lots of heat. The more power generated in the newer, higher-speed FPGAs, the higher the heat that is generated inside that chip. That heat must get out or dissipate. If not, it may cause an FPGA or any other semiconductor chip to prematurely fail, or at the minimum, cause signal disruptions and lower, poorer performance.

That's one side of the story. The other deals with the fact FPGAs and other highly advanced system-on-chip (SoC) devices are today mostly outsourced for fabrication. Chipmaker-owned fabs are history, and independent chip fabricators have emerged in the last decade or so to take care of the chip making. Consequently, a gap exists wherein R&D—once prominent in the chipmaker's house—is now questionable, leaving reliability doubtful.

Also, it looks to me that when it comes to testing, verification, and validation, these companies are not putting in as much time, energy, and resources to assure ICs and FPGAs can truly be tested at high-speed levels. When high-speed devices like FPGAs are subjected to stringent testing and they are put on carefully designed boards, they can undergo assembly and pass high-speed test levels.

I highly respect FPGA and other chipmakers because today they face major design and fabrication challenges as Moore's Law continues to drive newer chip generations. However, it might be a good time in our industries—EMS and semiconductor—to bring our mutual issues to the table and find ways to closely work together to minimize or avoid issues brought on by advanced technologies.

On the other hand, avoiding these issues, even when brought to the FPGA vendor's attention, is a clear and blatant disservice to both the EMS provider and OEM. In some cases, even bringing problems to the FPGA vendor's attention may be all for naught; in some cases, they don't have the necessary validation knowledge or data necessary to determine the root cause. Technology moves so fast it is difficult or near impossible to harness that level of detail and retain it.

What is an EMS provider to do?

Primarily, a high-speed PCB is subjected to all the key test and verification steps at assembly and test. A reputable and experienced EMS provider goes even further to apply innovative methods to uncover elusive problems. However, if components like an FPGA are suspected to be the problem, the EMS provider has to be diligent and contact the component manufacturer to get to the root of a problem. Simultaneously, the EMS provider makes certain the OEM is fully aware of these component suspicions.

In the case of a questionable FPGA, it's in the best interest of the OEM to assure it is tested at their facilities at extremely high speeds at different permutations, combinations of different voltages, and different temperature settings, vibrations, cycling, and zoning to ensure that all faults relating to that FPGA are found during the OEM's testing, validation, and debugging phase. By doing so, that same FPGA doesn't have to go through the EMS cycle to locate those errors. **SMT**

Zulki Khan is the founder and president of NexLogic Technologies Inc. To read past columns, or to contact the author, click here.

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SMTonline Market News Highlights

CEA: Rise of Connected Health & Wellness Devices

The Consumer Electronics Association's new report, "The Connected Health and Wellness Market," quantifies the dramatic growth in sales of connected health and wellness devices. The report defines the market, lays out key market growth drivers and challenges, and highlights important technology trends and regulatory issues.

PC Monitor Market: Positive Growth in Q3

Total worldwide PC monitor shipments were more than 35 million units in the third quarter of 2013, an increase of 4.5% compared to the previous quarter and 1.2 million units more than forecast, according to the IDC Worldwide Quarterly PC Monitor Tracker.

CES 2014: A Preview from Dan Feinberg

"I'm heading to Las Vegas again for CES. This is my 16th year attending this exciting show and I have seen it change quite a bit over the years. This year, change seems to be accelerating. Gone are the huge Microsoft booths and many of the top-tier sub assembly suppliers," says columnist Dan Feinberg.

Smartphone AP Market Up 31% in Q3 2013

According to the report, Qualcomm, Apple, MediaTek, Samsung and Spreadtrum grabbed the top-five revenue share spots in the smartphone apps processor market in Q3 2013. Qualcomm continued its lead in the smartphone applications processor market with 53% revenue share, followed by Apple with 18%.

Memory Sector Drives Semiconductor Sales in 2013

Following a 2.5% decline in 2012, the global semiconductor market has regained its footing in 2013 with revenue set to expand by nearly 5%. Global semiconductor sales in 2013 will amount to $317.9 billion, up 4.9% from $302.9 billion in 2012, according to preliminary estimates from the Semiconductor Value Chain service at IHS.

Consumer Sentiment on Overall Economy Flat in December

Consumer confidence toward the overall economy and technology spending in December both remain steady with last month's elevated sentiment levels, according to the latest figures released by the Consumer Electronics Association.

December Manufacturing ISM Report: PMI at 57%

Bradley J. Holcomb, CPSM, CPSD, and chair of the Institute for Supply Management Manufacturing Business Survey Committee, comments, "The PMI registered 57%, the second highest reading for the year, just 0.3 percentage point below November's reading of 57.3%."

Consumer Electronics Market to Reach $1.6 Trillion by 2018

Consumer Electronics market to witness a value of US $1.6 trillion by 2018. Geographical analysis shows the highest Compounded Annual Growth Rate (CAGR) of 17.6% is foreseen from Asia-Pacific region during the analysis period 2011-2018.

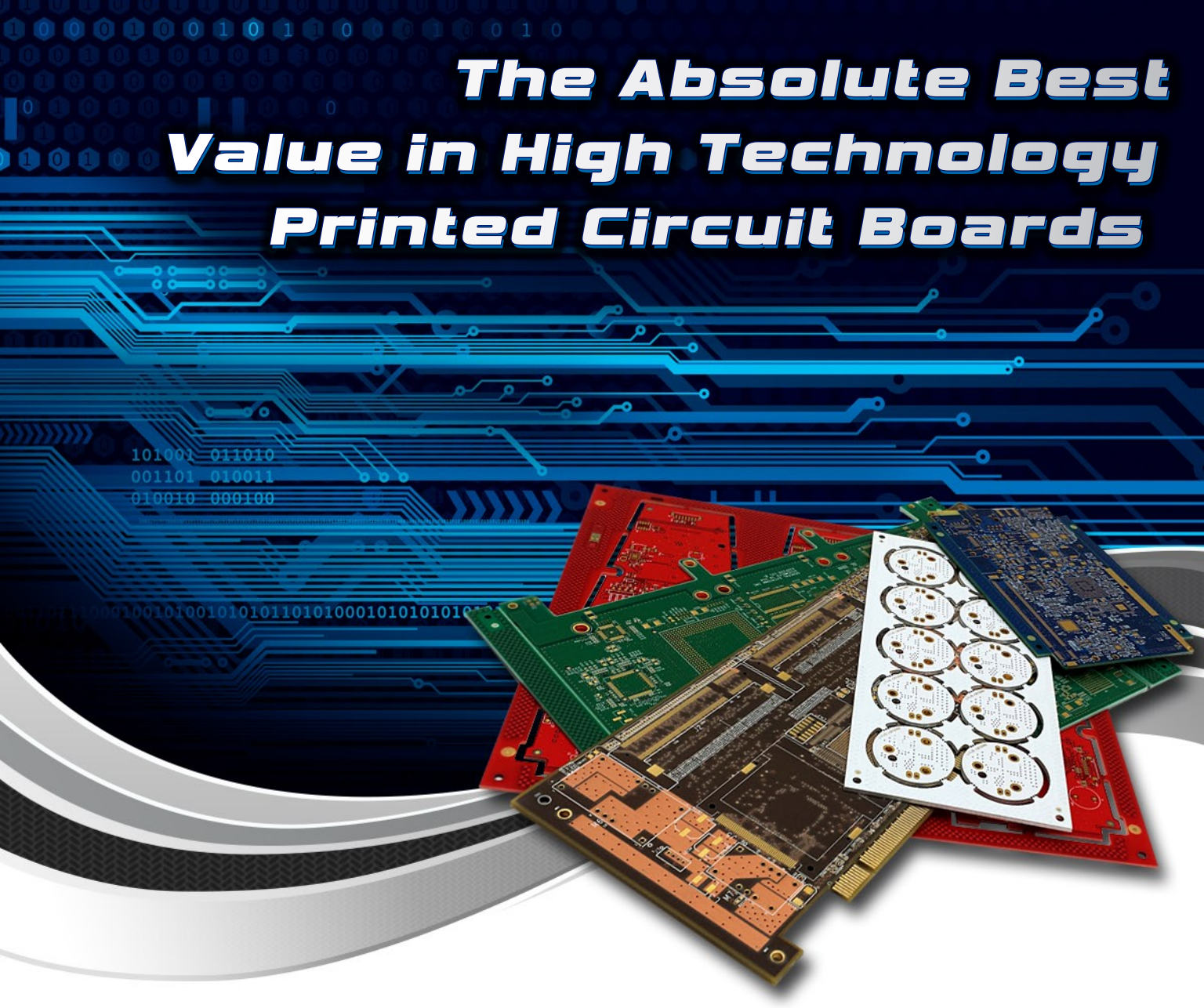
SSV Sales to Reach 55 Million Units Annually by 2022

Stop-start vehicles (SSVs), which eliminate idling by shutting off the engine when the vehicle is stationary and restarting it automatically when it is time to move, offer a portion of the fuel economy benefits of hybrid vehicles at a fraction of the cost premium.

Strategic Analysis of European EMS Industry 2012-2017

This is the eleventh edition of the European Electronic Manufacturing Services Industry report and updates both the tenth edition published in September 2011 and the first edition of the European Electronic Manufacturing Services Industry—Strategic Market Analysis, published in September 2012.

The Absolute Best Value in High Technology Printed Circuit Boards



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EVOLUTIONARY SOLUTIONS

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by Karla Osorno
EE TECHNOLOGIES

Electronics manufacturing services (EMS) depends on many people to make daily decisions. It is an intricate and complex field with many stages and steps. Because there are so many opportunities for decisions, significant quantities of errors and mistakes are possible—even probable. EMS companies are adept at implementing process controls that prevent errors. They also have corrective action systems in place to understand and resolve known issues. And one of the best known cures for error prevention and correction is a strong organizational culture.

Culture is one of five key areas of development that make all the difference when it comes to achieving state-of-the-art status. The other four are people, equipment, building and systems. This is the fourth part of a five-part series that will help you to understand the culture (definition, strength and model) and outline opportunities (action plan to becoming healthy) to create or improve your company culture.

Culture, Defined

Culture can be defined as complexes of learned behavior patterns and perceptions. Patterns include beliefs, customs, arts, way of life, way of thinking, etc. Organizational culture is the behavior patterns of people within an organization and includes values, visions, norms, working language, systems, symbols, beliefs and habits.

Davide Ravasi and Majken Schultz, in their body of work, state that organizational culture is a set of shared mental assumptions that guide interpretation and action in organizations by defining appropriate behavior for various situations. Each company will have their own culture. And in larger organizations, there may also

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The IWLPC Technical Committee would like to invite you to submit an abstract for next year's program.

Deadline for submittal is April 18th, 2014.

Suggested Topics to Submit

WAFER LEVEL PACKAGING

- Wafer Level Chip Scale Packaging (WLCSP), Flip Chip, Fan-Out and Redistribution, Wafer and Device Cleaning, Nanotechnology, Quality, Reliability, and COO

MEMS PACKAGING

- MEMS Processes and Materials, MEMS Design Tools or Methods, Nano-MEMS and Bio-MEMS, Integration, MEMS Integration and Interconnects, RF/wireless, Sensors, Mixed Technology, Optoelectronics

3-D PACKAGE INTEGRATION

- 3D WLP, Thru Silicon Vias (TSV), Silicon Interposers, Stacking Processes (W2W, D2W, D2D), IC Packaging Substrate, Embedded Die and Passives, TSV Integration: FEOL vs BEOL

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Patti Hvidhyld-Coles patti@smta.org | 952-920-7682
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WE ARE IN THIS TOGETHER! *continues*

be diverse and sometimes conflicting cultures that co-exist due to different characteristics of the management team.

Organizational culture may also have negative and positive aspects. Managing culture and minimizing conflicting culture dynamics becomes important for an organization to reap the positive benefits. Since organizational culture affects the way people interact with each other and with customers, new employees are taught collective behaviors and assumptions.

Strong culture is especially beneficial to complex service-based companies like contract manufacturers, since employees create the customer experience with their moment-by-moment decisions and actions.

Culture Strength

Strong culture is said to exist where employees respond to situations based on their alignment to organizational values. Strong cultures help companies to engage, execute and exist like well-oiled machines. In manufacturing, where low profit margins are standard, this can make the difference between survival and extinction.

Conversely, weak culture is where there is little alignment with organizational values, and control must be exercised through extensive procedures and heavy-handed management and bureaucracy.

Organizations that foster strong cultures have clear values that give employees a reason to embrace the culture. Strong culture is especially beneficial to complex service-based companies like contract manufacturers, since employees create the customer experience with their moment-by-moment decisions and actions. And these actions directly determine the decisions customers make about the company.

Organizations may derive the following benefits from developing strong and productive cultures:

- High employee motivation and loyalty
- Alignment toward achieving vision, mission, values, and goals
- Team cohesiveness among departments
- Consistency, coordination and control
- Efficiency-minded employees

Where culture is strong, people do things because they believe it is the right thing to do. Cohesiveness encourages and strengthens the group dynamic, whereby teams think consistently and any rogue activities are handled or eliminated by the team themselves rather than bureaucratic practices.

Knowing these benefits, who would say no to the desire for a strong culture? But where do you start? Start by assessing your current culture against specific culture models.

Culture Model

There are many models used to assess corporate culture. These models attempt to measure how culture affects organized performance and based on employee measurement, the organization can be deemed culturally strong or culturally weak. Employee values are measured against organizational values to predict employee intentions and predict turnover.

One example of a model for assessment that can be used to evaluate current and future culture strength is Daniel Denison's model. This model asserts that organizational culture can be described by four general elements and each is further described by three sub-elements:

1. Mission
   a. Strategic direction and intent
   b. Goals and objectives
   c. Vision
2. Adaptability
   a. Creating change
   b. Customer focus
   c. Organizational learning
3. Involvement
   a. Empowerment
   b. Team orientation
   c. Capability development
4. Consistency
   a. Core values
   b. Agreement
   c. Coordination/integration

Denison's model also allows cultures to be described broadly as externally or internally focused as well as flexible versus stable. The model has been typically used to diagnose cultural problems in organizations and determine whether an organization is healthy or not. Use this model and other descriptions to understand your company culture.

Healthy Culture

Do you want your organization to be healthy or unhealthy? This is an easy question to answer. Organizations should strive for a healthy organizational culture to maximize benefits and increase productivity, growth, and efficiency, as well as to reduce counterproductive behavior and turnover of employees. Consider this list of healthy culture characteristics:

- Appreciation for diversity
- Fairness and respect
- Employee pride and enthusiasm
- Equal opportunity for growth
- Strong communication
- Leadership, direction and purpose
- Competitive advantages in industry
- Low turnover rates
- Employee Investment learning and training

Using employee surveys, interviews, focus groups, observation, and other internal research, assess your organization in these areas. How does your company score relative to this list? If you scored well then keep doing what is working. If you scored poor then this and Denison's model becomes your priority list for action. Taking baby steps in each of these areas will strengthen your organizational culture.

The decisions will come from the top, but the real impact will come from the employees. Strong cultures possess high employee involvement, strong internal communications and an acceptance and encouragement of a healthy level of risk-taking in order to achieve innovation. Organizations with adaptive cultures achieve more success since they listen to employees and customers, take risks and initiate needed change.

Culture Change

When an organization does not possess a healthy culture or requires some kind of organizational culture change, the process can be daunting. Often, when the pain of employee turnover and failure to meet specific goals and results becomes significant, culture change becomes unavoidable.

With the assessment complete and clear identification of the desired culture complete, a change process can be designed. Culture change is impacted by a number of elements, including company history, industry, competition, size of organization, and reason for the culture change. Corporate culture is often hard to change and employees will require time to adjust to the new way of behaving. This is especially true of companies who had a long established culture. Changing corporate culture will be a long-term project.

The change will be more impacted by leadership than management. Informal leaders within the company have a large impact on the change process. Also, culture is not "managed in" but instead occurs when leaders set the tone, pace, and expectation.

> ***"Often, when the pain of employee turnover and failure to meet specific goals and results becomes significant, culture change becomes unavoidable."***

Leaders may choose to follow the following change process suggestions. First, formulate a clear strategic vision to provide the intention and direction for the culture change. This first step is critical. Since the change process can take months or years, it is too costly for morale to start and stop or to change directions frequently.

Second, show senior leader commitment. Employees will be loyal to the existing culture even if it is weak. True commitment will give them confidence in the desired culture and encouragement to make the necessary changes.

WE ARE IN THIS TOGETHER! *continues*

Third, leaders must model the kind of values and behaviors expected in the rest of the company. Modeling will provide confirmation of behavior expected and direction for whether the adjustments that are needed are significant or simply small tweaks. Key people in the organization, regardless of formal title, will be invaluable in communicating the new values. Dictating will not work. Instead, opt for being a catalyst for change and choosing other catalysts for change.

Fourth, make appropriate changes to the organization systems, policies, procedures and rules to be in alignment with new values and desired culture. Create accountability systems, compensation, benefits and reward structures, and recruitment and retention programs to better align with the new values and to send a clear message to employees that the old system and culture are in the past.

Fifth, connect culture to association. Recruit, train and when necessary, terminate in terms of fit with the new culture. Encouraging employee motivation and loyalty to the new company culture is essential and will also result in a healthier culture. Leaders will communicate verbally and behaviorally the connection between the desired behaviors and how it will impact and improve the company's success to further encourage employee buy-in in the change process. Training should be provided to all employees to understand the new processes, expectations and systems.

Finally, evaluate the change process regularly and identify areas that need further development. Identify obstacles of change and resistant employees. Also acknowledge and reward employee improvement. Add leaders or consultants to facilitate the change process and provide training. Change is inevitable and success rides on execution of a well-defined change process.

Creating a strong culture in your organization is well worth the investment. State-of-the-art products are more likely when the culture dictates behavior rather than relying solely on procedures. Employees are loyal, connected and self motivated based on cultural norms rather than a heavy hand or constant supervision. And in that environment positivity, fun, and contribution thrive and everyone wins. "We are in this together" is the mantra and state-of-the-art is the product. Culture drives success because it drives most inputs, which include state-of-the-art systems, the final topic in this five part series on state-of-the-art organizations. **SMT**

Karla Osorno is business development officer for EE Technologies, Inc., an EMS provider delivering complete engineering and manufacturing services with locations in Nevada and Mexico. To read past columns or to contact Osorno, click here.

Carbon Nanotube Sponge Shows Potential

A carbon nanotube sponge capable of soaking up water contaminants, such as fertilisers, pesticides, and pharmaceuticals, more than three times more efficiently than previous efforts, has been developed and the results of the study published in *Nanotechnology.*

The carbon nanotube (CNT) sponges, uniquely doped with sulphur, also demonstrated a high capacity to absorb oil, opening up the possibility of using the material in oil spill clean-ups.

CNTs are hollow cylindrical structures composed of a single sheet of carbon. Owing to their structure, CNTs have extraordinary thermal, chemical, and mechanical properties that have led to an array of applications from body armour to solar panels.They have been touted as excellent candidates for wastewater clean-up.

"Millimetre- or centimetre-scale CNTs, as we've synthesised in this study, float on water because of their porous structure and, once saturated with oil, can be easily removed. By simply squeezing them and releasing the oil, they can then be re-used," said lead author of the research, Luca Camilli, from the University of Roma.

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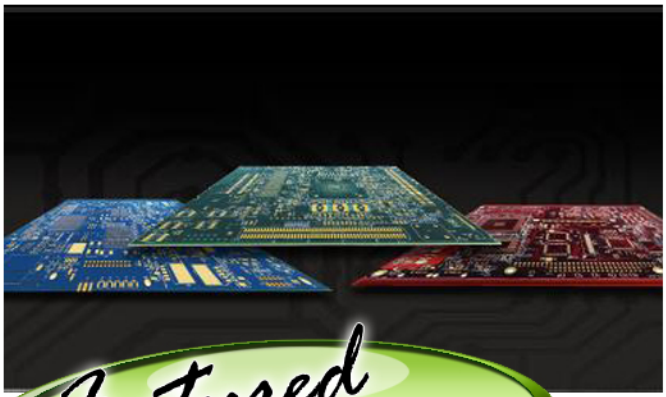

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KRAMER ON COUNTERFEITS

The Counterfeit Epidemic That Can Kill

by Todd Kramer
SECURE COMPONENTS LLC

In August 2011, a prime contractor warned the United States Navy that there were suspect, reworked parts that should never have been placed on one of their aircraft and that should be replaced immediately.

How is it possible a trusted, world-renowned manufacturer detected that it had installed a suspect or fraudulent part in its aircraft? The prime had subcontracted with another subprime contractor, who was retained to produce ice detection systems for the aircraft. In a message to the U.S. Navy marked "Priority: Critical," the company blamed the part, a Xilinx field programmable gate array, for the failure. This critical component was not bought from Xilinx direct or from one of their authorized distributors. Rather, this suspect part was traced upstream within the supply chain and had made its way through independent distributors in California, Florida, Japan, and China. If you are thinking that perhaps this is an anomaly, consider this. The U.S. Senate Armed Services Committee investigation revealed that more than 1 million counterfeit components likely exist within the U.S. military supply chain. If the supply chain of the finest military in the world can be infiltrated by 1 million counterfeit components, it's more than likely it can happen to your supply chain.

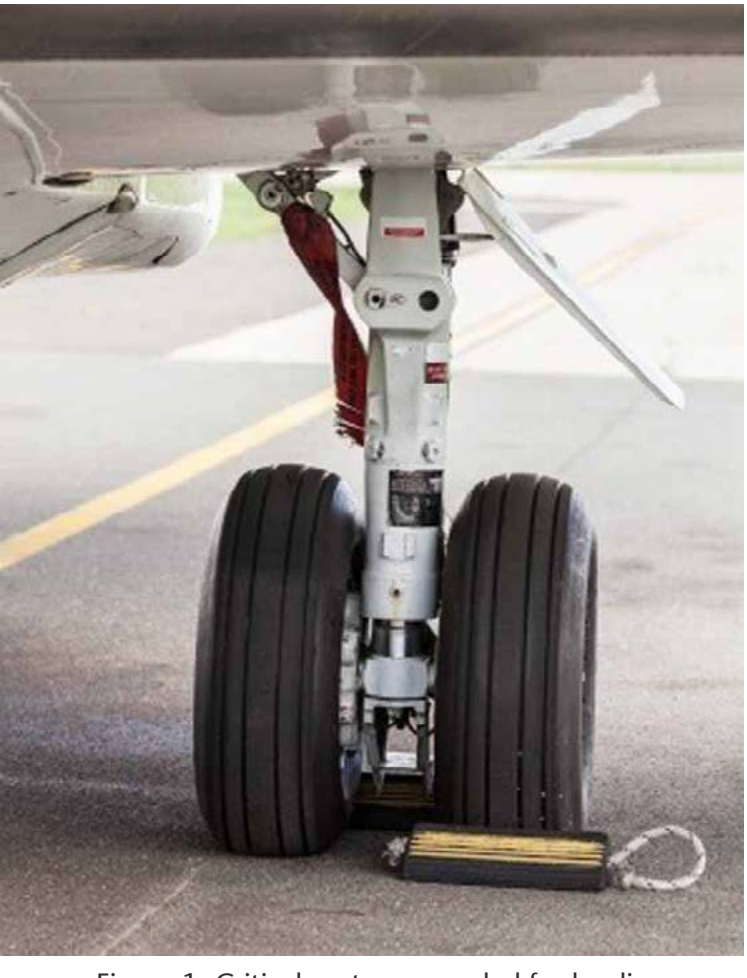

Figure 1: Critical parts are needed for landing gear.

Billions Lost to Counterfeiting

The problem is not just limited to those who supply government agencies. Recent reports show consumer and industrial businesses are losing approximately $250 billion each year because of counterfeit components. One report notes the automotive industry alone lost $3 billion in sales, while another shows the semiconductor industry takes a $75 billion annual hit.

How Does this Affect Your Organization?

Liability laws to protect the supply chain are changing within our government, which culminates with an end user. While most of the current focus by legislators is on the aerospace and defense supply market, proactive businesses are addressing the issue and not waiting on a government mandate to protect their business and their clients.

The questions that need to be asked today are numerous: Do we have a counterfeit avoid-

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May 13-15, 2014
Toronto, ON, Canada
*Paper required

SMTA International
Abstract Deadline: **February 28,**
Sept 28 – Oct 2, 2014
Rosemont, IL
*Paper required

Counterfeit Electronic Parts and Electronic Supply Chain Symposium
Abstract Deadline: **March 7th**
June 24 - 26
College Park, MD
*Presentation Only

IWLPC – Int'l Wafer-Level Packaging Conference
Abstract Deadline: **May 2nd**
November 11-13, 2014
San Jose, CA
*Paper required

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THE COUNTERFEIT EPIDEMIC THAT CAN KILL *continues*

ance plan? Is it entrenched in our quality management system? What quality and counterfeit avoidance requirements do we flow down to our suppliers? Are our suppliers capable of meeting these requirements, and if so, how do I know? How do our vendors manage their supply chain? Do they send out supplier surveys?

Programs that are considered "life critical" should specifically address these questions, and businesses should be focusing on integrating their counterfeit avoidance plans into their quality management system to secure their supply chains and protect their business from counterfeit components. This issue is no longer a matter of ethics. The laws are changing and those organizations that refuse to accept the realities of the current global supply chain are exposing their companies to unquantifiable economic loss and liability. So how did all of this happen?

E-Waste and Recycling: Part of the Problem

Many of us think of recycling and reusing as the right thing to do. We set our recycling bins next to our garbage cans, and we think that everything is going to end up in gleamingly clean, green-efficient buildings, where different products are separated and then recycled into clean and refurbished products, right? Well, not all the time. Ethical recyclers should be certified to ensure they will properly dispose of the toxic ingredients in discarded computers, printers, mobile devices, and other systems, to gain the valuable precious metals they contain with little environmental harm. Unfortunately, not everyone is ethical and not everyone is properly recycling. For example, consumers using e-recyclers who are certified to the E-Stewards Certification, can have confidence that they practice due diligence. By utilizing a certified e-recycler one can be assured they are not inadvertently providing e-waste to an organization that could potentially pollute the supply chain and contribute to the counterfeit epidemic.

Why use a certified e-waste recycler?

On November 8, 2011, the Senate Armed Services Committee held a hearing on the heels of an investigation into counterfeit electronic parts in the defense supply chain. The investigation revealed alarming facts, including that materials used to make counterfeit electronic parts often come from e-waste, shipped from industrialized countries like the United States to countries like China or India.

Figure 2: Individuals and companies must be responsible for e-waste disposal.

The e-waste is sent to these countries by the ton where it gathers into mounds for processing, to be reintroduced back into the supply chain. Each time electronic e-waste is submitted to a recycling company that is not certified to properly dispose of those components, they are potentially polluting their supply chain. It increases the likelihood that those components could be used to fuel the counterfeit epidemic.

The Gray Market: the What, Why and Who

What is the gray market? Manufacturers turn to the gray market when the original component manufacturer or their authorized distributors cannot supply the product needed or the lead time is unmanageable. Gray market companies are typically distributors or brokers that are not bound by contracts from the original manufacturer. They have the ability to search for and procure any product from any source of supply, at any time. These companies often use the internet to find the lowest priced stock—not always placing a priority on quality and authenticity. Therefore, whenever parts or

components are obtained by gray market companies, they should be subjected to a higher level of scrutiny than buying directly from an authorized source. Companies get into trouble when they purchase gray market material and use price as the determining factor on whom to purchase from.

The gray market is made up of independent distributors and brokers who use their network of contacts throughout the world to locate and procure hard-to-find product. Some companies work out of their basements and simply buy from a supplier they find online, receive the parts in, count the quantity, and send the shipment off to the next supplier in the supply chain. Other, more reputable distributors have attained certifications that ensure procedures and policies detect, avoid, and dispose of suspect, fraudulent, or counterfeit parts.

New Laws and Liability Regarding Procurement

On December 31, 2011, less than two months after the Senate Armed Services Committee held their hearing, President Obama signed the National Defense Authorization Act (NDAA) for fiscal year 2012, into law. Section 818 of this act requires all DoD contractors and subcontractors to obtain electronic parts from original equipment manufacturers (OEMs), their authorized dealers, or from "trusted suppliers" that obtain parts exclusively from OEMs or their authorized dealers.

By definition, Section 818 includes all "covered contractors" who supply parts or products that include electronic components. All DoD contractors are required, whenever possible, to obtain electronic parts that are in production or currently available in stock from the original manufacturers of the parts or their authorized dealers. However, this is not a viable reality for many suppliers and manufacturers. Parts that are in shortage or have gone obsolete are not available from these authorized suppliers. How does a company procure such a hard-to-find item?

The Slippery Slope of "Trusted Suppliers"

NDAA Section 818 references the term "trusted suppliers" in regard to what is considered an acceptable source of supply for materials that can only be procured from an other than authorized source of supply. Although the NDAA is silent in terms of defining "trusted supplier," one can infer that a trusted supplier is one that has been vetted by a third-party accredited certification body, has successfully completed a government audit, or has undergone and passed an in-person and on-site audit performed by a qualified subject matter expert/auditor. Once a company has been vetted for their procedures and processes to detect, avoid, and contain counterfeit material, then a supplier can be considered "trustworthy."

SAE International (SAE), the internationally recognized standards association familiar to the aerospace, automotive, and commercial vehicle industries, has implemented new standards that specifically address counterfeit avoidance. Standards such as AS553A and AS6081 (issued in November 2012) provide guidance for implementing counterfeit avoidance for manufacturers and independent distributors. Both of these standards have been adopted by the DoD. According to the Defense Standardization Office, "Adoption is analogous to the Good Housekeeping Seal of Approval."

This standard requires organizations involved with the purchase, acceptance, and distribution of electronic components to have a quality management system in place, to communicate and document contract provisions that establish purchasing controls, and to retain appropriate records for supply chain traceability. In addition, AS6081 requires products procured from the gray market to be verified through a series of tests, which are detailed and outlined within the standard. Further testing such as using X-ray, scanning electron microscope, or acoustic imaging is used to look inside the packaging of the product.

While AS6081 covers distribution of components, AS5553A provides similar certification for manufacturers. Originally implemented in January 2013 in response to the increasing volume of fraudulent and counterfeit parts entering the aerospace supply chain, AS5553A was expanded to mitigate such risk on a global scale with regard to various sectors. Many of the requirements of AS5553A are similar to AS6081 and likewise aim to prevent the receipt and

THE COUNTERFEIT EPIDEMIC THAT CAN KILL *continues*

installation of fraudulent or counterfeit parts through uniform requirements, practices, and methods.

Most recently, the United States National Committee who represents the U.S. interest from industry gathered at the International Electrotechnical Commission (IEC) with 14 other nations to formalize a Counterfeit Avoidance Program that is recognized by the World Trade Organization. This new third-party certification system allows supply chain entities to demonstrate compliance to these standards. For more information, please contact the Center for Counterfeit Avoidance, a not-for-profit organization, representing the international supply chain.

While it may be impossible to completely prevent the distribution of counterfeit parts into the supply chain, it is crucial to ensure that your company and those with whom you conduct business are working to protect themselves and their customers. Understanding, complying, and enforcing these federal regulations and internationally recognized requirements not only contributes to ultimately reducing the availability of counterfeit parts, it also helps mitigate the associated liability risks facing organizations. **SMT**

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- **IECQ 03-7 (Ed.1.0)** IECQ Rules of Procedure - Part 7: IECQ Counterfeit Avoidance Programme (IECQ AP-CAP) - Programme Requirements
- **SAE AS6081 (Iss. 2012-11)** Fraudulent-Counterfeit Electronic Parts: Avoidance, Detection, Mitigation, and Disposition - Distributors

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HOUSTON , TX
Web Site: http://www.dnvcert.com

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– Attached Translation - None –

IECQ-P Rev. 02

Figure 3: AS6081 Counterfeit Avoidance Certification.

To view a video interview on this topic featuring Stan Salot Jr. and Todd Kramer, click here.

Todd Kramer is CEO of Secure Components LLC, a leading independent distributor of electronic components, hardware, and mechanical parts to the Aerospace, Defense, & Commercial Industries. Kramer is an active member of organizations such as SAE G-19C, the current chairman of U.S. National Committee (USNC/IECQ) and the International Working Group 06 (Counterfeit Avoidance). His new column, Kramer on Counterfeits, will run monthly in SMT Magazine. To contact Kramer, click here.

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News Highlights from SMTonline this Month

1 Kitron Expands Business with Husqvarna Partnership

Husqvarna Group has decided to renew its contract with Kitron and has increased the contract scope by adding new products. The annual revenues under the new contract could be in the range of NOK 25 million until 2017. This would represent a doubling of current levels.

2 IEC Electronics' Executive VP Resigns

Don Doody, executive vice president, has voluntarily resigned from the company effective January 10, 2014. W. Barry Gilbert, chairman and CEO, stated, "We greatly appreciate the contribution Don has made to the company over the past nine years. During his time with IEC, we have grown from a company with a little over $28 million in revenue to a $141 million company."

3 Benchmark Expects to Exceed 4Q13 Guidance

The company, a leading integrated product design and manufacturing services provider, expects sales and earnings per share to exceed the high end of guidance for the fourth quarter of 2013. On October 24, 2013, the company provided fourth quarter guidance for sales between $685 and $715 million and diluted earnings per share between $0.34 and $0.38.

4 Global-Tech to Close EMS Business

Net sales for the second quarter of fiscal 2014 were $12.6 million, compared to $26 million for the corresponding quarter in fiscal 2013. This decrease in net sales is primarily attributable to sharp declines in sales in the company's EMS business which, as previously disclosed, continues to be adversely affected by a slowing Chinese domestic market, high turnover and rapidly decreasing margins.

5 SMT, Inc., Eruston Partner to Offer Complete Turnkey Manufacturing

"As a result of the partnership, Surface Mount Technologies and Eruston combine the best of both worlds to offer our customers complete turnkey manufacturing," commented Lewis Wagner, president of SMT. Located in Irvine, California, Eruston Corporation has been a supplier for military, aerospace, commercial, and medical equipment manufacturers since 1984.

6 Strategic Analysis of European EMS Industry 2012-2017

This is the eleventh edition of the European Electronic Manufacturing Services Industry report and updates both the tenth edition published in September 2011 and the first edition of the European Electronic Manufacturing Services Industry—Strategic Market Analysis published in September 2012.

7 IPC Forms PAC to Forward Member Goals

IPC is in the process of filing papers with the Federal Election Commission to establish the IPC PAC. This committee will support federal candidates for office that advocate for policies that support the growth of electronics manufacturing. The PAC will help raise IPC's visibility with policy makers and other key influencers in Washington.

8 Kitron Secures Medical Equipment Contract from Maquet

Kitron ASA has signed a general agreement for future business relations with Maquet Critical Care AB, part of Getinge Group. The agreement includes deliveries of mechanical and electronic-based products. Maquet is the largest subsidiary of Getinge Group of Sweden, a leading global medical technology company.

9 IEC's Q4 Earnings Hurt by SCB Impairment Charge

W. Barry Gilbert, chairman of the board and CEO, stated, "IEC took non-cash impairments of goodwill and intangible assets at SCB after analyzing and reconfiguring the operations of SCB. We also took into account market challenges for our customers during periods of government uncertainty."

10 Jabil Posts Revenue of $4.6 Billion in Fiscal 1Q14

Generally accepted accounting principles (GAAP) operating income for the first quarter was $172.7 million and GAAP diluted earnings per share were $0.57. The company indicated that $21.3 million in restructuring costs during the quarter impacted GAAP operating income.

EVENTS

For the IPC's Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar, click here.

For a complete listing, check out *SMT Magazine's* full events calendar here.

SPIE Electronic Imaging
February 2–6, 2014
San Francisco, California, USA

MD&M West Conference
February 10–13, 2014
Anaheim, California, USA

Pan Pacific Microelectronics Symposium
February 11–13, 2014
The Big Island, Hawaii, USA

Dallas Expo & Tech Forum
March 4, 2014
Plano, Texas, USA

NORDIC HDI 2014
March 5–6, 2014
Copenhagen, Denmark

Houston Expo & Tech Forum
March 6, 2014
Stafford, Texas, USA

SMTA Webtorial: Tin Whiskers—All You Should Know
March 11, 2014

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March 25–27, 2014
Las Vegas, Nevada, USA

Electronics New England
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Boston, Massachusetts, USA

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SMT® (Surface Mount Technology) is published by BR Publishing, Inc., PO Box 50, Seaside, OR 97138

February 2014, Volume 29, Number 2 • SMT© (Surface Mount Technology©) is published monthly, by BR Publishing, Inc.

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