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Novel Approach to Improve Electronics Reliability in the Next Generation of U.S. Army SUGV Under Complex Vibration Conditions p.12

Buyer Beware: Do Lifecycles Open the Door to Counterfeits? p.30

Replacing Automated Test Equipment p.34

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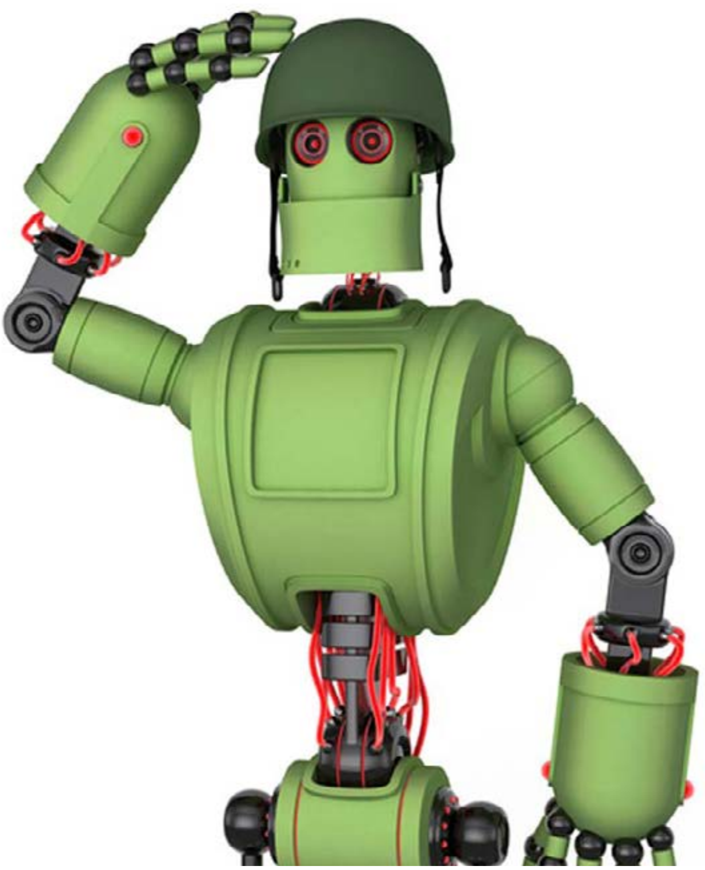
HIGH-RELIABILITY

This month, *SMT Magazine* features articles by industry experts on high-reliability issues facing a range of sectors: mil/aero, medical, counterfeit components, and more! As always, the June issue offers columns from favorites like Derek Snider, Michael Ford, Karla Osorno and Rachel Miller-Short.



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CONTENTS

3D Printed Electronics: The Future is Now

by Ray Rasmussen
I-CONNECT007

With great interest, I've been watching the emergence of 3D printing over the last few years. The idea that a product can be built from scratch using a printer, depositing layer after layer of material until a final, usable product is created, seems like something out of Star Trek. But it's not some futuristic, sci-fi fantasy. It's here, and it's now. The technology, today, lends itself to low-volume applications like mechanical parts, for instance, and the industry is expected to reach $3.7 billion in 2015 and then $6.5 billion by 2019. Although it's an up-and-coming industry and has the promise, as some believe, to herald a new industrial revolution, that revolution will likely be 10-20 years into the future, before virtually all products are made this way. At that point, when everything is produced on-demand, with molecular accuracy, products will be almost perfect and won't be made in some far off factory, but in the back room of the store, while you wait. Want a new pair of running shoes? Slip your foot into a 3D scanner and viola! In a few minutes you're out the door with your perfect fitting shoes made of the latest materials, providing long wear and durability. Oh, and at half the price!

That got me to thinking about the applications for this technology and the PCB. The idea that a machine can print the base material and circuit layers while integrating the components into the package, all at one time, seems a bit far-fetched. I can see printing circuits onto a prepared substrate. Heck, that's already being done. And yes, the newest, biggest thing is embedded components, so that's already starting to happen, kind of, but still as separate steps. We are starting to see applications where these traditionally separate components are brought closer together. That will certainly lend itself to that eventual one-stop product shop which, with the push of a button, prints out the latest techno gadget.

There are applications today where product components are being circuitized to save space and weight and, probably, cost. Optomec, an additive manufacturing solutions company, is already touting their systems designed to place

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circuits in unconventional places like a cell phone casing or on an airplane wing. Of course, if you've been around long enough, there have been companies over the years which have built "molded" circuits for 3D applications and, of course, there are today's flex circuits which provide 3D characteristics. In this case, I'm talking about printing the circuits right onto the surface of the phone's case and assembling the components as well. Now, this isn't exactly a 3D printed product, but it may very well be at some point. And, with some 3D printers priced at $1,000-$2,000, this industry is moving fast.

Keep in mind, too, that more and more companies are touting their ability to print accurately on the nanoscale, which blows away the accuracy of today's systems, even semiconductor capabilities. It really is a new ball game.

As with just about any new technology, the first real markets for anything built on these printers, today, will be one-off parts and prototypes. The time-savings easily justify the huge expense associated with the more sophisticated, more capable, 3D printing systems. One example, from a company called Shapeways, offered up a "printed" UAV wing, which was then printed with circuits using Optomec's PE printer. From a Shapeways blog:

"Common electronic materials including conductor, dielectric, resistor, and semiconductor inks can be processed by the Aerosol Jet system to print conformal sensors, antennae, shielding and other active and passive components. Printing these electronic components directly on or inside the physical device eliminates the need for separate printed circuit boards, cabling and wiring, thereby reducing weight and size while also simplifying the assembly process."

It seems to me that there's a beautiful synergy emerging when you match up printed electronics technologies with the 3D printing of mechanical or structural product components. The melding of these two technologies is the game-changer for electronics. PE without 3D is just another way to make a circuit. 3D without PE is nice, but doesn't offer much more than traditional systems do. The two technologies working in concert complete the package. The ability for product designers to integrate circuits into the traditionally static product components will dramatically accelerate both industries. The implications are huge. Think about it.

Printed electronics is certainly gaining speed and will increasingly cross into traditional PCB spaces, but there aren't many incentives for designers to move to PE for their products. Unless they just need a very low-cost circuit or a very lightweight solution, PE isn't quite ready. But if coupled with 3D printing, product designers now have a whole bunch of new reasons to look at PE. It opens up new worlds to those designers looking to reduce weight, size or cost.

Sure, it'll start out simple, but once designers see 3D PE as an enabling technology, traditional manufacturing will start to come under pressure.

From Forbes Magazine came this article, "Manufacturing the Future: 10 Trends to Come in 3D Printing," describing the future of manufacturing:

"New machines grace the factory floor. Expect to see 3D printing machines appearing in factories. Already, some niche components are produced more economically on 3D printers, but this is only on a small scale. Many manufacturers will begin experimenting with 3D printing for applications outside of prototyping. As the capabilities of 3D printers develop and manufacturers gain experience in integrating them into production lines and supply chains, expect hybrid manufacturing processes that incorporate some 3D-printed components. This will be further fueled by consumers desiring products that require 3D printers for their manufacture."

I think we'll start to see more and more individual product components being fabricated in the near future. Then, when and where possible, circuits will be added along with some passive components. This is already doable as was mentioned above. As more and more product components come together, eventually we may even see things like simple electronics completely fabricated by these machines. Maybe your iPhone 20 will be built in the back of the cell phone store while you wait, highly tailored to your preferences (perfectly fit to your hand and ear, your generation, etc.).

In the meantime, the melding of 3D printing and PE does make me think a bit more about the short-term future of the PCB. If a machine can do all the things described in some of the articles listed at the end of this article, why can't a PCB be built from the ground up? IBM and others are building components on the molecular level with 3D printing. And really, today's PCBs are fairly simple animals, when it comes to their constituents. You just need a dielectric and a conductor. Of course, there are many other things to consider that ensure reliability, etc., but I think you get my drift. **SMT**

For more on this subject, here are a few articles to keep you busy:

[Manufacturing The Future: 10 Trends To Come In 3D Printing]

[3D-Printed Consumer Electronics Just Became A Reality]

[A 3d Printed Spaceship On The Scale Of A Human Hair? Hello Nanoscribe 3D Printer]

Ray Rasmussen is the publisher and chief editor for I-Connect007 publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuiTree Magazine.* Contact Rasmussen [here].

Piezoelectric Transistors Convert Motion to Electronic Signals

Using bundles of vertical zinc oxide nanowires, researchers have fabricated arrays of piezotronic transistors capable of converting mechanical motion directly into electronic controlling signals. The arrays could help give robots a more adaptive sense of touch, provide better security in handwritten signatures, and offer new ways for humans to interact with electronic devices.

The arrays include more than 8,000 functioning piezotronic transistors, each of which can independently produce an electronic controlling signal when placed under mechanical strain. These touch-sensitive transistors, dubbed "taxels," could provide significant improvements in resolution, sensitivity, and active/adaptive operations compared to existing techniques for tactile sensing. Their sensitivity is comparable to that of a human fingertip.

The vertically-aligned taxels operate with two-terminal transistors. Instead of a third gate terminal used by conventional transistors to control the flow of current passing through them, taxels control the current with a technique called "strain-gating." Strain-gating based on the piezotronic effect uses the electrical charges generated at the Schottky contact interface by the piezoelectric effect when the nanowires are placed under strain by the application of mechanical force.

"Any mechanical motion, such as the movement of arms or the fingers of a robot, could be translated to control signals," explained Zhong Lin Wang, a Regents' professor and Hightower Chair in the School of Materials Science and Engineering at the Georgia Institute of Technology." This could make artificial skin smarter and more like the human skin. It would allow the skin to feel activity on the surface."

Novel Approach to Improve Electronics Reliability in the Next Generation of U.S. Army SUGV Under Complex Vibration Conditions

by Ed Habtour
U.S. ARMY MATERIEL SYSTEMS ANALYSIS ACTIVITY,
and Cholmin Choi, Michael Osterman Ph.D., and Abhijit Dasgupta Ph.D.
CALCE

SUMMARY: This paper presents the joint effort by the U.S. Army Materiel Systems Analysis Activity and the Center of Advanced Life Cycle Engineering to develop test methods and analytical models that better capture unforeseen design defects prior to the qualification phase, by better replication of life cycle vibration conditions.

Abstract

The functionality of next-generation U.S. Army platforms, such as the small unmanned ground vehicles (SUGV) and small unmanned aerial vehicles (SUAV), is strongly dependent on the reliability of electronically-rich devices. Thus, the performance and accuracy of these systems will be dependent on the life cycle of electronics. These electronic systems and the critical components in them experience extremely harsh environments such as shock and vibration. Therefore, it is imperative to identify the failure mechanisms of these components through experimental and virtual failure assessment. One of the key challenges in re-creating life cycle vibration conditions during design and qualification testing in the lab is the re-creation of simultaneous multi-axial excitation that the product experiences in the field. Instead, the common practice is to use sequential single-axis excitation in different axes or uncontrolled multi-axial vibration on repetitive shock shakers. Consequently, the dominant failure modes in the field are sometimes very difficult to duplicate in a laboratory test.

This paper presents the joint effort by the U.S. Army Materiel Systems Analysis Activity (AMSAA) and the Center of Advanced Life Cycle Engineering (CALCE) at the University of Maryland to develop test methods and analytical models that better capture unforeseen design defects prior to the qualification phase, by better replication of life cycle vibration conditions. One approach was to utilize a novel multi-degrees of freedom (M-DoF) electrodynamic shaker to ruggedize designs for fatigue damage due to multi-directional random vibration. The merits of vibration testing methods with six-DoF shaker and cost saving associated with such an approach will be addressed in this paper. There is a potential for M-DoF to detect critical design flaws earlier in the development


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cycle than has been traditionally possible with existing shaker technologies, and therefore produce more cost-effective, reliable and safe systems for the warfighters.

Introduction

In military applications, electronic devices play a vital role in mission success. These devices provide control, guidance, communication, and reconnaissance and are vital components in modern unmanned vehicular applications. This trend in modern warfare has increased the complexity of electronic equipment, especially in low-volume, highly sophisticated, and dense electronic systems. Figures 1 and 2 show the SUGV and SUAV [1]. These modern systems take advantage of the remarkable advances made in

Figure 1: SUGV.

Figure 2: SUAV.

low-cost commercial electronics. It is becoming progressively more beneficial to use such components in military applications for improved computational performance, on-demand availability, addressing obsolescence, and providing state-of-the-art capabilities. This current movement of using commercial-off-the-shelf (COTS) electronics and devices for military applications has led to concerns about their reliability in harsh battlefield environments. Typically, these types of systems are subjected to various complex loadings, including shock and vibration, during their life cycle. These loads may impose significant stresses on the PCB substrate, component packages, leads and solder joints [1]. These stresses can be due to a combination of bending moments in the PCB and/or inertias of components. They may lead to several failures such as delamination in the PCB, solder joint fatigue, lead fracture, or structural damage to components.

When conducting physics of failure (PoF) analysis of electronic systems, the large variety of package types is perhaps one of the main challenges to consider, since failure may occur due to one of several failure drivers. One of the most frequent failures in electronics is the package-to-board interconnect in heavy components with large center of mass (CM) and low-profile surface mount packages (SMT). The failure in heavy components with large CM can be predominantly due to inertial loads. While in light low-profile SMT packages, the dominant stress source can be due to board deflection. Both of these failure drivers may compete in heavy and large electronic components such as inductors and transformers. Depending on the architecture of these components, they can also significantly alter the local vibration response. It is common to increase the board stiffness to reduce the overall response of the PCB. However, increasing the board stiffness may increase local bending moments.

The current available vibration fatigue life prediction methods for large/heavy components force reliability engineers to use one of two extremes. One method is to construct a detailed 3D FEA. This approach may be impractical when dealing with large circuit card assemblies (CCA) containing many components, each with multiple leads and solder joints. Further, these methods can be computationally expensive and their accuracy may be compromised due to assumptions in material properties and support conditions. The other extreme is to use simple empirical equations. Probably the best-known empirical method to estimate component life under vibration is Steinberg's model [2]. However, these models are also limited to a defined set of boundary conditions and package structures. Therefore, they cannot be the only design tool to evaluate new products or emerging technologies with a high level of confidence.

This paper is concerned with a rapid analytical technique for analyzing heavy/large components that can provide an engineer high-fidelity assessment while reducing the computational time. A PoF approach was developed that may improve the reliability assessment of CCAs containing large/heavy components. This approach is a hybrid-method that combines 2D and 3D FEA where the mechanical and inertial properties of the components at the local level are taken into consideration. These properties may be used to extract an accurate natural frequency value for the CCA. Nonetheless, this approach may not eliminate the need to address the components inertial effects.

Physics of Failure Approach

Simplified Single Degree of Freedom Approach

As mentioned above, one of the best-known simplified models for analysis of PCB vibration fatigue is Steinberg's model [2]. The Steinberg model defines a critical maximum vibration induced displacement for components as [2]:

$$d = \frac{0.00022\, B}{C\, h\, r \sqrt{L}}$$

where B is the length of the PCB edge parallel to the component located at the center of the board in units of inches. L and h are the length of the component and the thickness of the PCB in inches, respectively. C is a constant coefficient which depends on the component type and r is the relative position factor of the component relative to the PCB. The Steinberg model assumes a dynamic single-amplitude displacement for the PCB. This model is valid only for single-degree-of-freedom (SDOF) systems. The out-of-plane root-mean-square (rms) displacement is calculated as follows [2]:

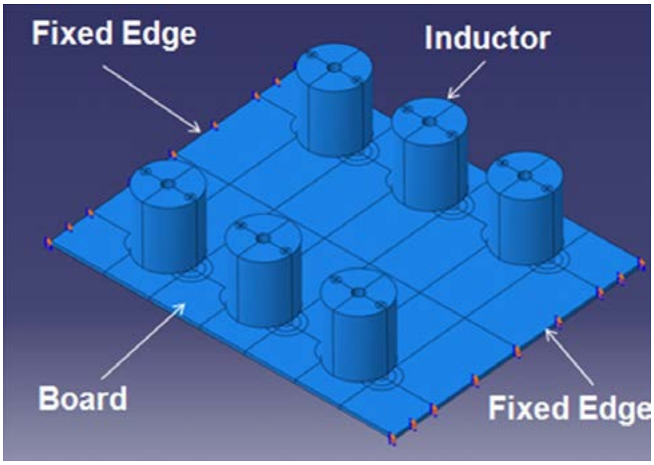
$$Z_{rms} = \frac{9.8\, G_{rms}}{f_n^2}$$

where f_n is the natural frequency and G_{rms} is the root-mean-square output acceleration. The G_{rms} can be estimated using Miles' equation:

$$G_{rms} = \sqrt{\frac{\pi\, P f_n Q}{2}} \text{ where } Q = \sqrt{f_n}$$

where P is the input Power Spectral Density and Q is the transmissibility. Steinberg states when the dynamic single-amplitude displacement at the center of the PCB is limited to the critical value d, the component is expected to achieve a fatigue life of 20 million stress reversals in a random vibration environment and 10 million stress reversals under sinusoidal vibration. One must be cautious when using this model since Steinberg's empirical approach is based on a specific experimental data set from a particular collection of specimen architectures and boundary conditions. Thus, this empirical approach may be more accurate when applied to PCBs assembled in exactly the same manner. The drawback of his model is that it cannot be used outside the range and configuration of the assembly used in the derivation of the model. It cannot be used to evaluate new products or emerging technologies with high confidence. Nonetheless, this approach may help designers obtain a rough estimate of the acceleration factors for accelerated vibration durability tests and for comparing the relative dynamic robustness of competing designs.

Electronically dense military platforms have to endure severe and complex dynamical loading conditions during the life cycle, resulting in



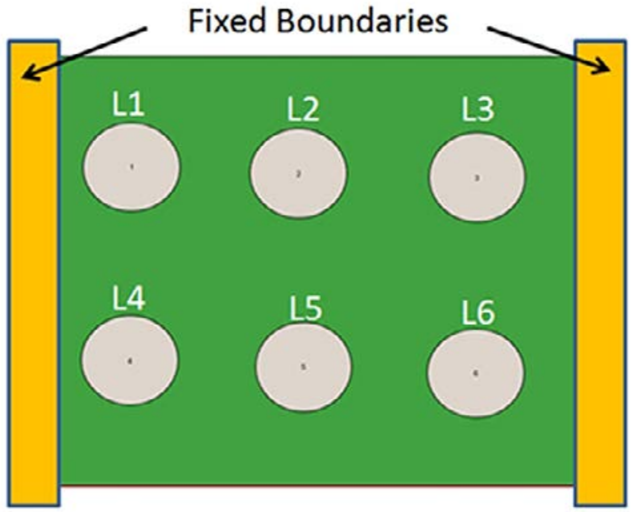


Figure 3: CAD model of PCB with large components.

high-cycle fatigue. For complex structure and dynamic loading the Steinberg's model alone may not be an adequate approach for assessing the survivability of military devices.

In this study a 127x101.6 mm^2 PCB with six large/heavy inductors was designed, as shown in Figure 3. The inductor geometry is shown in Figure 4.

The PCB was assumed to be fixed (clamped) along the short edges of the board, as illustrated in Figure 3 with the red dots. The objective is to evaluate 2D and 3D FEA approaches to assess the reliability of large electronic components. A more cost-effective approach combining 2D and 3D FEA was developed to extract the natural frequency of the PCB and more accurately determine the maximum deflection, curvature, and stress. The goal is to evaluate whether this approach can detect critical failure risks early in the development cycle. The modeling also provides effective guidance for future vibration testing using a M-DoF electrodynamic (ED) shaker. The test results will be used in the future to evaluate the accuracy of this modeling approach and to assess the effect of the local inertia of large/heavy components on the fatigue life of interconnects.

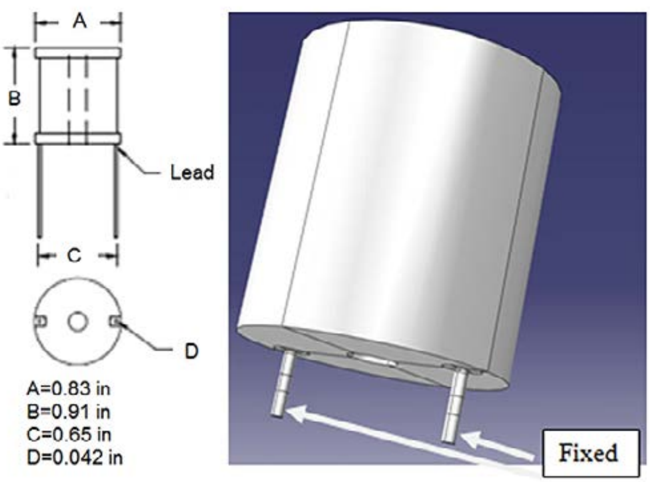


Figure 4: Large inductor used in this study.

Two-Dimensional Approach

A more detailed approach than the Steinberg model that is useful when conducting PoF analysis is a simplified 2D (plate or shell) FEA of a PCB. The mass of the components is smeared over their PCB footprints to reduce computational time and cost. This method was developed by Pitarresi and Primaver where they performed experimental and FEA modeling work to characterize the natural frequencies, mode shape, and transmissibility at the board level [3]. Later, they used the simple plate vibration models, using the property smearing approaches, as well as detailed finite element modeling.

In the case where the local inertias are significant, a traditional 3D FEA might be necessary. Transforming a 3D PCB model in Figure 3 to 2D FEA using the smeared technique is shown in Figure 5. The PCB was discretized into rectangular shell elements, as shown in Figure 5. The in-

dividual elements were defined by four nodes. Typically in traditional FEA, the shell element nodes in a continuum structure have six-DoF. For PCB PoF analysis, the number of degrees of freedom was reduced to three plate DOFs, which includes one out of plane displacement, u_z, and two rotations about the two orthogonal axes in the plane of the board. The displacement of each node is driven by the element's stiffness matrix. The element stiffness matrix is a function of the element geometry and the constitutive material properties. Because PCBs have multilayer composite construction, laminated plate theory was used to calculate the element stiffness matrix. The layers' geometric and material properties were designed symmetrically about the middle surface of the board. Therefore, the bending-extension coupling effect was not a cause for concern and the extension and the coupling matrixes were eliminated [4]. This led to a simplified plate equation with the bending stiffness only:

$$\begin{Bmatrix} M_x \\ M_y \\ M_{xy} \end{Bmatrix} = \begin{bmatrix} D_{11} & D_{12} & 0 \\ D_{12} & D_{22} & 0 \\ 0 & 0 & D_{33} \end{bmatrix} \begin{Bmatrix} \kappa_{xx} \\ \kappa_{yy} \\ 2\kappa_{xy} \end{Bmatrix}$$

where {M} and {k} are the moment resultant and board curvature vectors. The flexural (or bending) rigidity matrix, [D], is the measure of how easily the board bends. [D] can be calculated as follows:

$$D_{ij} = \frac{1}{3}\sum_{k=1}^{n} Q_{ij}^{k}(h_k^3 - h_{k-1}^3) \quad for\ i, j = 1,2,3$$

where i and j coincide with the natural axes of the material and n is the number of layers in the PCB. The distance of the outermost fiber of the k^{th} layer from the mid-surface of the plate is h_k. Q^k_{ij} is the material stiffness matrix for the material in layer k [4] for additional information on how to calculate Q_{ij}. For a uniform, symmetrical, homogeneous composite construction the board rigidity, $D_{11}=D_{22}=D$, may be approximated as:

$$D = \frac{E\,t^3}{12(1-\nu^2)}$$

where E is the elastic modulus, t is the board thickness and n is the Poisson's ratio. After obtaining the [D] matrix, the board curvature can be calculated from the simplified plate equation (4). The smeared-technique was then implemented using 2D shell elements.

The smeared technique includes the mass of the board and components by simply increasing the mass of the shell element under the footprint of each component. However, the component stiffness is not included in this simplified smearing approach. The first mode natural frequency for this board, using this smearing approach, is 108 Hz.

However, for large/heavy through-hole components, some 2D codes may approximately include the stiffening effect of the components. In this approach, the mass and stiffening effects are included by locally increasing the PCB's density and Young's modulus, respectively. Unfortunately, such an approach does not address the inertias and radius of gyration of large components with high standoff. These effects can cause additional stresses in the leads and interconnects and a traditional 3D FEA might be necessary to analyze this effect.

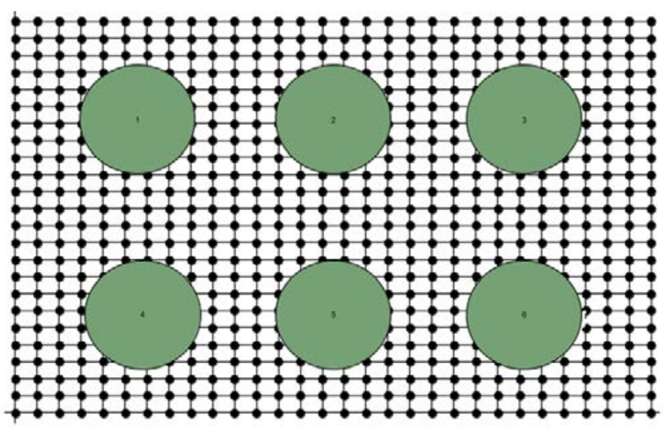


Figure 5: 2D FEA of PWB and inductors, using smearing method.

Standoff Height (mm)	Mode I (Hz)	Mode II (Hz)	Mode III (Hz)
0.5	108	1733	3266
1.0	102	1657	3161
1.5	98	1560	2682
2.0	94	1430	2200

Table 1: Inductor modal response for various stand-off heights.

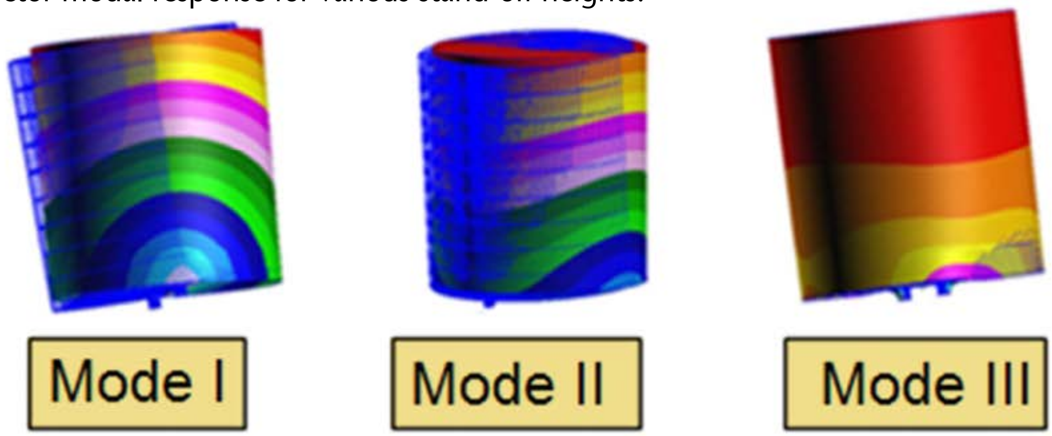


Figure 6: Inductor modal shapes when fixed at leads.

Three Dimensional Approach

In this study, modal analyses were first conducted on just the inductor with various standoff heights as shown in Table 1. In this task, the component leads were assumed to be fixed at the interface with the PWB, as shown in Figure 4. As expected the modal frequency dropped as the standoff height increased, due to the component's significant inertia. Resulting mode shapes are shown in Figure 6. This additional motion will clearly have a significant impact on the stresses induced in the interconnects, but these effects are typically neglected in the smeared properties technique.

To more accurately model the system, a 3D model of the board with attached inductors was constructed and analyzed. In this analysis, the modal frequencies of the inductors dropped significantly because of the compliance of the PWB attached to the lead foot. The first mode response of the middle inductors is depicted in Figure 7. The inductor standoff height in this analysis was 2.0 mm and the maximum response occurred in the components located at the middle of the PCB. The frequency for the first vibration mode for the middle components and the components closer to the fixed edges was approximately 71 Hz, which is approximately 20% lower than the frequency for a rigidly clamped lead foot. The PCBs first vibration mode was 159 Hz, which was about 45% higher than that predicted by the smeared 2D model, because of the additional stiffening effect of the components. The first mode shape of the PCB is shown in Figure 8.

In typical vibration fatigue analysis, the PCB is treated as a thin plate. Therefore, many researchers reasoned that the PCB's natural frequency is dependent upon the geometry and the material of the board and not necessarily on the components [5]. This might be valid for microelectronic components with low mass and low stand-off, where the drop in natural frequency due to the added mass of the com-

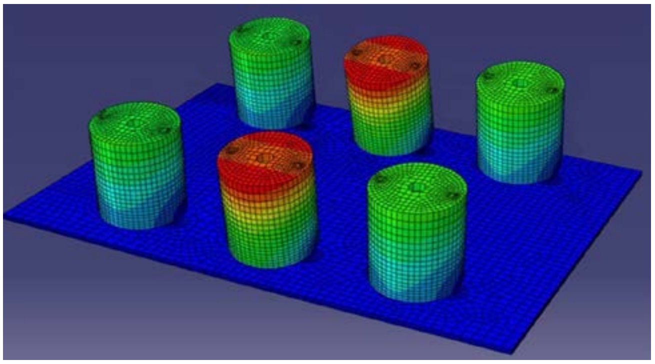


Figure 7: Middle inductor's first modal response.

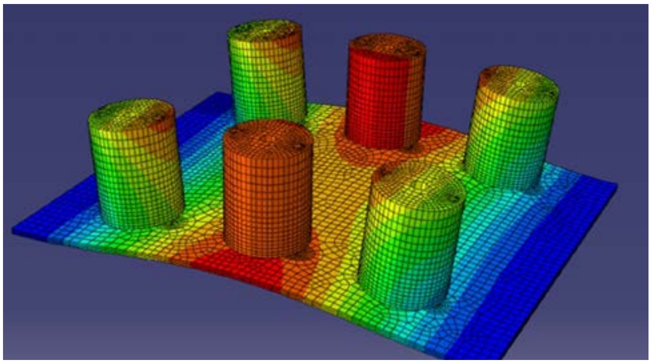


Figure 8: PCB first modal response.

ponents is compensated for by the increase in the natural frequency due to the local increase in stiffness from component mounting. However, for large/heavy components the scheme may not be applicable since the increase in the component mass and the leads stiffness might not cancel each other. The first vibration mode for the PCB described above when neglecting both the inertial and stiffness effects of the components was approximately 310 Hz. Clearly, neglecting the mass and stiffness effects of the inductor overestimated the natural frequency of the PCB. If the mass effect of the components was included only in this particular PCB, the natural frequency was108 Hz, while inclusion of the stiffening effects also, (using the 3D global FEA model) increases the frequency to 159 Hz.

Combined Two and Three-Dimensional Approach

In this study the simplicity of the global 2D FEA was combined with a more detailed local 3D FEA. The advantages of this approach are significant cost and time reduction without resorting to full 3D FEA. In this approach, the local 3D FEA model was considered first. Based on the knowledge of the effective moment-curvature relationship near the component of interest, a local effective stiffness was determined. The warpage was evaluated by simply applying a local unit load to the local model, as shown in Figure 9. This caused the PCB to experience small dynamic deflection or warpage. The local deformation was modeled with two radii of curvature. This was accomplished through the use of Kirchhoff-plate moment-curvature equations (found in several structural textbooks), where the local radii of curvature and the local applied bending moments are related as follows:

$$\begin{Bmatrix} M_{xx} \\ M_{yy} \\ M_{xy} \end{Bmatrix} = \begin{bmatrix} D_{11} & D_{12} & 0 \\ D_{12} & D_{22} & 0 \\ 0 & 0 & D_{33} \end{bmatrix} \begin{Bmatrix} \kappa_{xx} \\ \kappa_{yy} \\ 2\kappa_{xy} \end{Bmatrix}$$

$$\begin{Bmatrix} M_{x} \\ M_{y} \\ M_{xy} \end{Bmatrix} = \frac{h^3}{12} \begin{bmatrix} E_{11} & E_{12} & 0 \\ E_{12} & E_{22} & 0 \\ 0 & 0 & E_{33} \end{bmatrix} \begin{Bmatrix} \kappa_{xx} \\ \kappa_{yy} \\ 2\kappa_{xy} \end{Bmatrix}$$

where, $D_{ij}=E_{ij}h^3/12$ for i, j = 1, 2, 3. Assuming an isotropic Poisson's ratio for simplicity, the local effective stiffness due to the presence of the component can be calculated as follows:

$$D_{11} = \frac{M_x - \nu M_y}{\kappa_x(1-\nu^2)}$$

Similarly,

$$D_{22} = \frac{M_y - \nu M_x}{\kappa_y(1-\nu^2)}$$

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The curvature can be calculated from the PWB deflection of the local 3D FEA model, by the relationship below which can be obtained in any calculus book:

$$\kappa_x = \frac{\frac{d^2y}{dx^2}}{(1+\frac{d^2y}{dx^2})^{3/2}}$$

where the elastic deflected curve was expressed mathematically as y=f(x). The component was assumed to remain rigid and all the deformation was assumed to occur in the PWB and the leads. This assumption was made in the local model to make the displacement calculation more manageable.

The global 2D FEA model was constructed in the manner discussed above. However, the local flexural rigidity matrix, [D], was replaced at the footprint of each component, with the ones calculated from the local 3D FEA model. The first vibration mode was then obtained from the 2D global model, which was 160 Hz. This value was close to that obtained from the full 3D FEA model discussed above. Therefore, one may use a combined two-three-dimensional approach to reach similar results to a full 3D FEA with the advantages of less computational time and cost reduction.

Although this approach may improve the prediction of the first mode of the CCA, it does not take into account the inertial effect of the large components. Therefore, a spectral response analysis was conducted using the global 3D FEA model, for the NAVMAT P9492 Acceleration/Power Spectral Density (ASD/PSD) profile, Figure 10. The profile was clipped at 350 Hz, meaning the analysis was performed for 0-350 Hz range. This was done to study the first two modes of the assembly. A base motion excitation was used at the boundary for each in-plane direction (x and y directions) and out-of-plane (z direction) individually. The direction of the excitations and responses are shown in Figure 11.

This analysis was followed by combined excitation in all directions: x, y and z. The PSD acceleration responses are given in Figure 12. It can be seen from Figure 13 that the center component experienced the highest excitation in the in-plane y direction as well as a slightly lower excitation in the out-of-plane direction at the first mode frequency of the component, 70 Hz. Another interesting observation is the component is excited in the out-of-plane direction at the first frequency mode of the board. In terms of the PWB, the dominant mode is the first mode of the board, as expected. Nonetheless there were dynamic effects due to the excitation in the y direction that caused an acceleration peak in the PWB at the component natural frequency, 70 Hz. This peak is generated by the component's high inertia which produces a rocking motion as shown in Figure 11.

Finally, the PSD of the analyzed lead stress due to the combined dynamic loading is shown

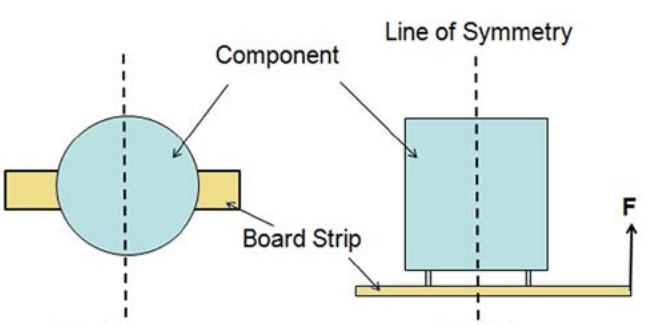

Figure 9: Local FEA model.

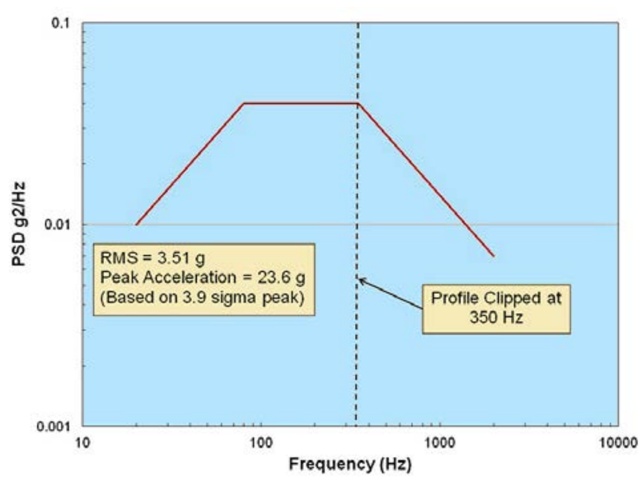

Figure 10: NAVMAT P9492 ASD/PSD.

in Figure 13. The maximum stresses were located at the leads of the center components, as illustrated in Figure 14. The stresses shown in this figure were the z-component stresses. This stress component represents the bending stresses in the leads caused by combination of inertial loads and the board deflection. Because of the board architecture and the components' inertial effect there might be alteration in the local vibration response. As mentioned above, it is a common practice to increase the board stiffness under the footprint of the component to reduce the overall response of the PCB, but this may increase local bending moments and stresses in the PWB.

Clearly, the modified smeared technique may address the overall stiffness of the CCA and produce an accurate PWB first-mode frequency; however, it doesn't tackle failure in heavy components. Therefore, the best practice is to conduct a M-DoF accelerated vibration test to assess the actual damage accumulation rates in the components, leads and PWB, followed by full 3D FEA modeling to generate acceleration factors that can be used to extrapolate the test results to various life cycle conditions and mission profiles. In practice, engineers often use one of these two approaches (i.e., modeling or testing) to qualify the product. The next section addresses the testing methodology.

Testing Approach

When considering PoF of electronics in ground vehicles, there are two types of motion that should be considered. One motion is the

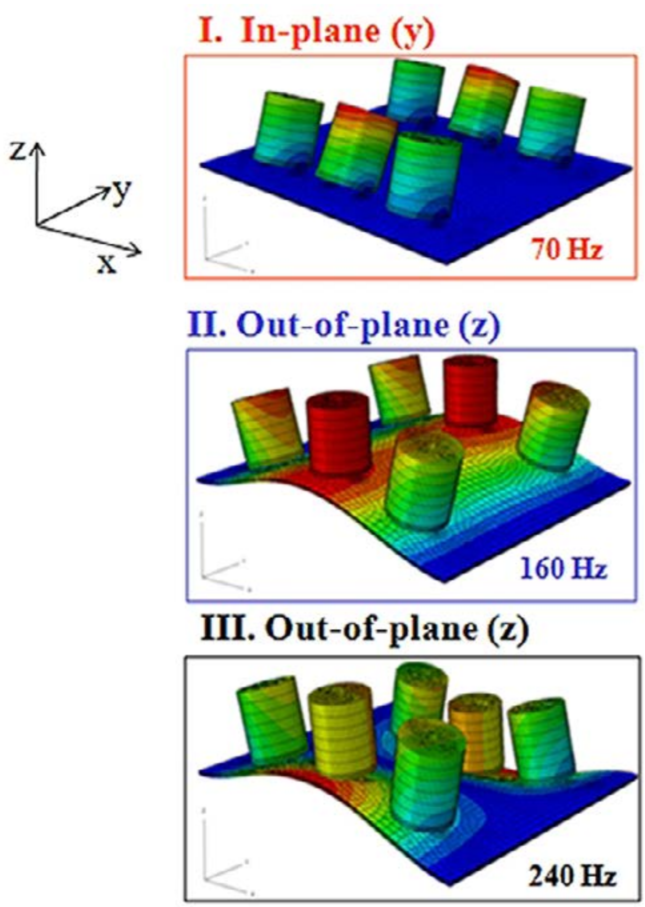

Figure 11: Response analysis.

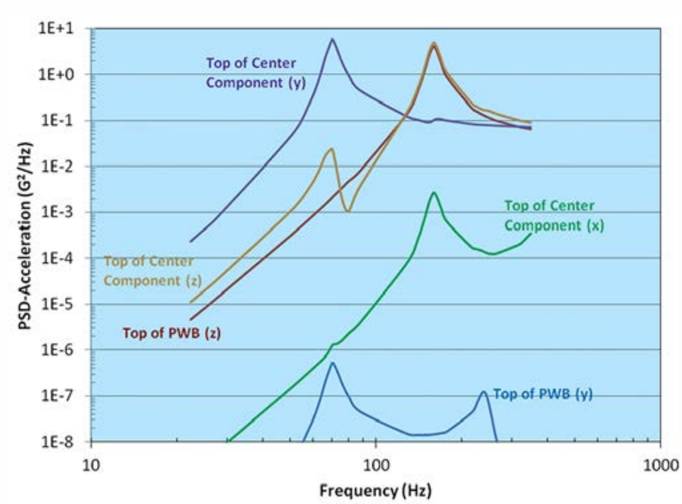

Figure 12: Spectral response analysis.

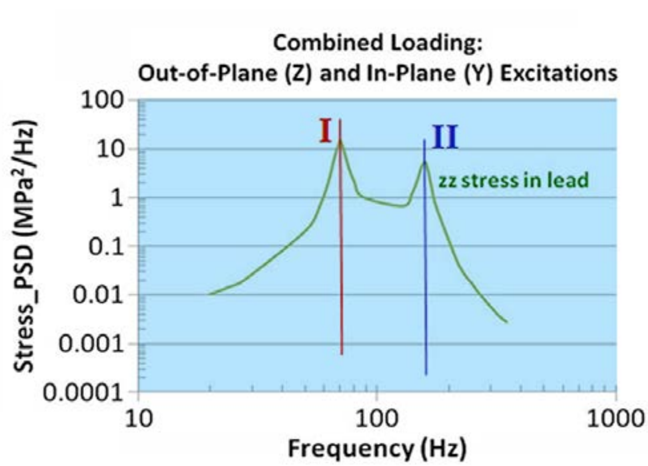

Figure 13: Stress due to combined loading.

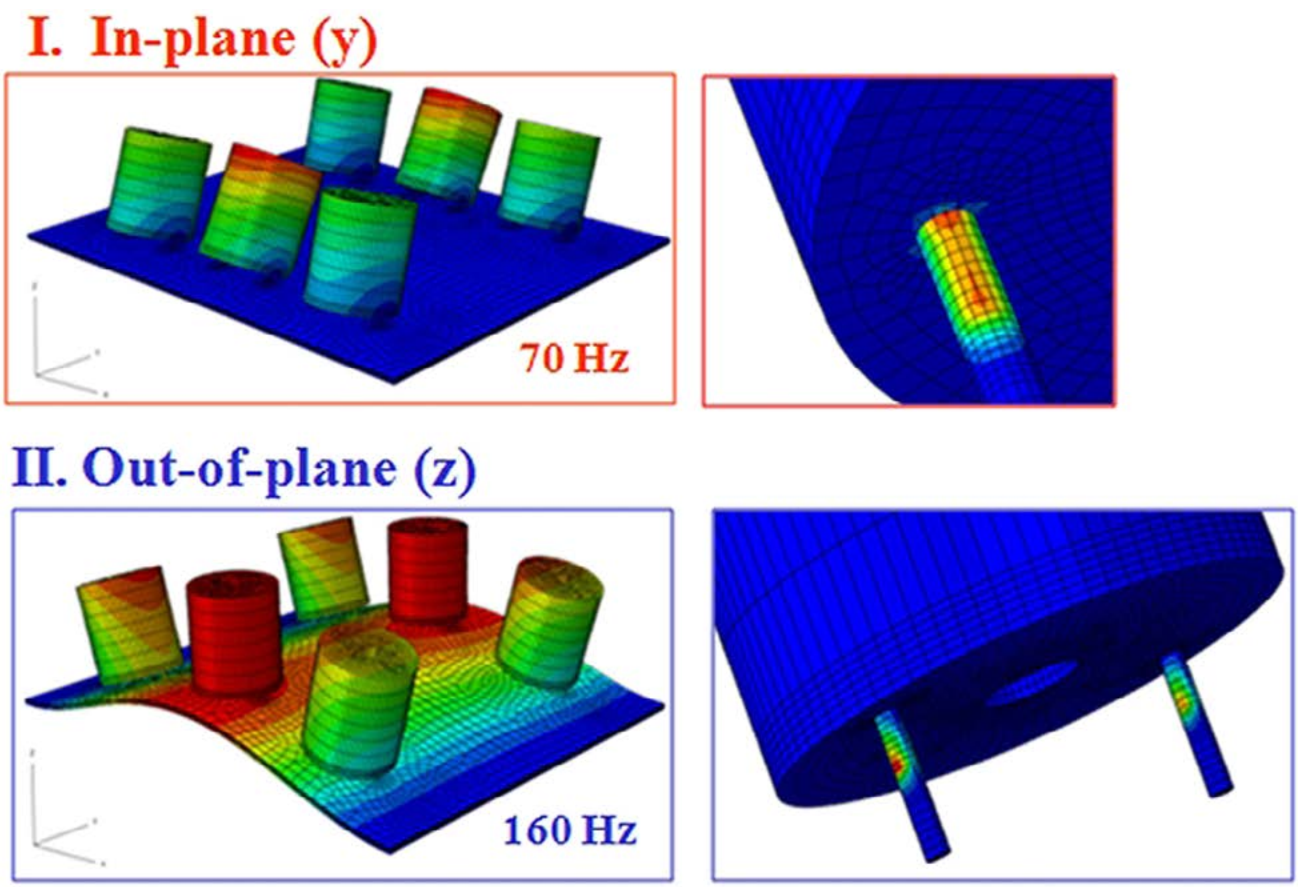

Figure 14: Maximum stresses at component leads.

induced curvature or bending in the PCB as the assembly moves in a vibratory manner (global motion). The other motion is the movement of individual components with respect to the PCB due to the compliance of the components' attachment (local motion). To accurately assess how the excitations are transmitted from the vehicle to the electronic component level, some researchers have suggested modeling the dynamic response of the vehicle subsystems. This approach, however, can be an arduous task [6]. The main reason for this lies in the fact that the vehicle chassis and body are complex systems. The reaction forces and vibration velocities depend not only on the strength of excitation within the chassis but also on the coupling of the chassis and the subsystems.

Thus, one has no choice but to count on engineering judgment in estimating the boundary conditions and system inputs. A more practical approach perhaps is using experimental frequency response function (FRF) data to represent the vehicle then combine it with the FEA models of the subassembly.

Two approaches utilized in this study for M-DoF testing are based on a repetitive shock (RS) shaker and a M-DoF ED shaker. A typical RS shaker utilizes a collection of pneumatic actuators to impart impact energy to a specially designed vibration table that transmits the resulting multiaxial vibration energy to test specimens mounted on the table. The RS shaker is often used in the industry to identify marginal designs and design weaknesses that, due to statistical variability, would eventually result in premature field failures when production quantities of the product are exposed to life cycle conditions. This method relies on the use of elevated stresses to determine the operating and destruct limits of the design.

The test is performed in a chamber which typically has a broad spectrum of vibration en-

ergy from 10 to 5,000 Hz and runs from 1 to 150 G_{rms}.

The RS testing typically does not provide quantitative information of acceleration factors for precipitated failure mechanisms, due to two major limitations [7]. First, the only input that can be controlled during vibration testing is the G_{rms} in the vertical direction (or Z direction). Thus, it is impossible to control the shape of the Power Spectral Density (PSD) profile [7]. Secondly, since the chamber employs pneumatically driven hammers, it is impossible to independently control each DoF. Furthermore, CALCE has confirmed that the coherence between the axes is nonexistent [7]. Thus, it is difficult to determine the acceleration of failure and/or the DoF that instigates the most damage to the components. Therefore, a quantitative relationship between performance in the field and performance in the test is difficult to establish.

Due to these limitations of RS shakers in M-DoF vibration testing, this team is investigating the possibility of utilizing multiaxial electrodynamic (M-DoF ED) shakers. The objective is to study the differences in failure modes and fatigue life for simultaneous multi-axis excitation versus single-axis excitation.

The M-DoF ED shaker used in this study consists of 12 electrodynamic actuators; 4 for each of the three orthogonal excitation axes. Eight are in-plane and four out of plane (underneath the shaker table), as shown in Figure 15. The twelve ED shakers are mechanically coupled to the table via self-aligning hydrodynamically lubricated bearings. The four actuators in each axis can be run in-phase or out-of-phase to produce translation in that axis or rotation about transverse axes. This architecture allows the shaker to produce a true M-DoF vibration environment. The actuators can exert up to 200lbf force per axis with max translation of ±0.25 inches and max rotation of ±5°. The excitation limit is up to 30Gs with 0-3000Hz for a 10lb payload. Unlike other testing methodologies, multiaxial ED shakers provide a more controlled

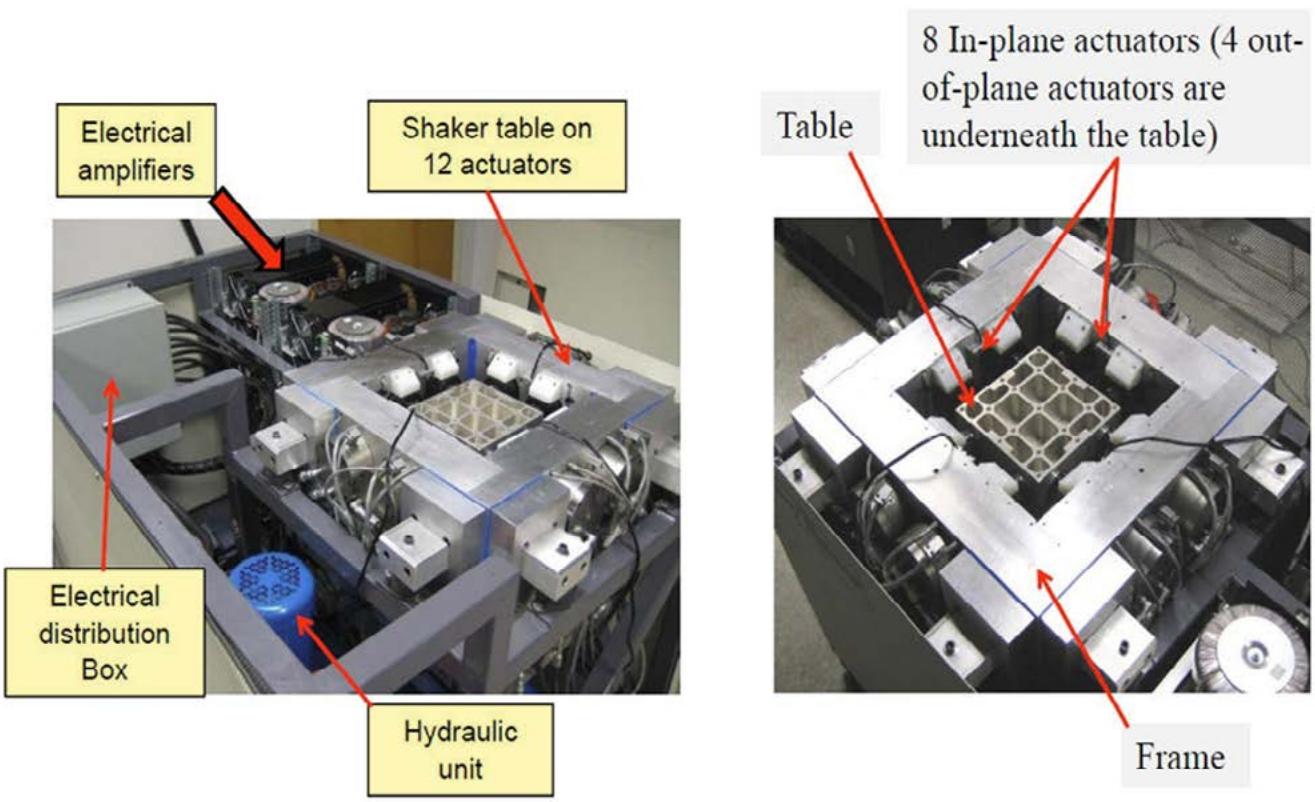

Figure 15: Multiaxial six-DoF ED shaker.

simultaneous loading along different axes of a test specimen, thus, allowing controlled exploration of cross-axis interactions that could not be easily explored with single-axis excitation or with RS shakers. The input PSDs and coherences can be controlled for all axes, as demonstrated by CALCE [7]. CALCE has also shown that the coherence between the axes is excellent. Therefore, it is possible to identify the most dominant failure mechanisms or the DoF that instigates the most damage to the components.

This approach may help in establishing a quantitative relationship between performance in the battlefield and performance in the test. It may also produce a modified smeared modeling approach that addresses inertial effects of large/heavy components without the need to resort to a fully three-dimensional detailed FEA model.

Future Work

Vibration durability tests will be conducted on the M-DoF ED shaker for various excitation orientations: 1) out-of-plane; 2) in-plane; 3) simultaneous in-plane and out-of-plane; and 4) sequential in-plane and out-of-plane excitations. Subsequently, destructive physical analysis of failed specimens will be conducted. The final step will be to develop a PoF modeling approach for vibration durability under random, multi-modal and M-DoF excitations. The natural frequencies and mode shapes will be extracted from FEA modal analysis and compared with testing results. For this step, test specimens will be fabricated (PCB with heavy through-hole inductors) to conduct a M-DoF vibration durability test on the M-DoF shaker. Additionally, FEA simulation will be carried out to characterize the dynamic response of the test CCA. Response characterization will mainly include dynamic strain history collected on the test vehicle. Corresponding FEA will be conducted and calibrated, based on the experimental results.

The characteristic flexural strain at different locations on the test board can then be either measured with strain gages or estimated from the FEA model, under different excitation levels. These strain time histories are then used to construct strain range distribution functions of the PCB, based on cycle counting.

Outcomes

As discussed above, the fatigue damage in the interconnects can be due to a combination of flexural deformations in PCBs and/or due to inertial forces caused by the mass of large/heavy components with high stand-off. When conducting electronics PoF, a hybrid two/three-dimensional FEA approach may provide natural frequency results closer to full 3D FEA while reducing cost and computational time. However, failures predominantly due to inertial loads may require full 3D FEA, testing, or both.

It is essential to understand the structural characteristics of large/heavy components in electronics devices in order to correlate the defects with the dynamic responses. As mentioned above, the main challenge in electronics packaging is the prediction of the reliability and lifetime of the critical components. Therefore, it is imperative to identify the failure mechanisms of the components through experimental analysis. However, the experimental approach has to emulate the real world operational conditions, which includes simulating M-DoF dynamic loads. This involves experimentally measuring the transient in-plane and out-of-plane displacement responses which can be accomplished with the aid of a multiaxial shaker.

This investigation will be utilized to enhance and improve existing standards for dealing with complex dynamic loading in electronics. It will also aid AMSAA in establishing a quantitative relationship between performance in the battlefield and performance in the test. It may also provide a means to validate and improve existing physics of failure models. **SMT**

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Dr. Michael Osterman is a senior research scientist and the director of the Center for Advanced Life Cycle Engineering (CALCE) Electronic Products and System Consortium at the University of Maryland. He heads the development of simulation assisted reliability assessment software for CALCE and simulation approaches for estimating time to failure of electronic hardware under test and field conditions. He is one of the principle researchers in the CALCE effort to develop simulation models for failure of lead-free solders.

Professor Abhijit Dasgupta, an expert in reliability at the University of Maryland, CALCE, has conducted over 20 years of research on the mechanics of engineered, heterogeneous, active materials, with special emphasis on the micromechanics of constitutive and damage behavior. He applies his expertise to several multifunctional material systems, including electronic packaging material systems and "smart" composite material systems.

Video Interview

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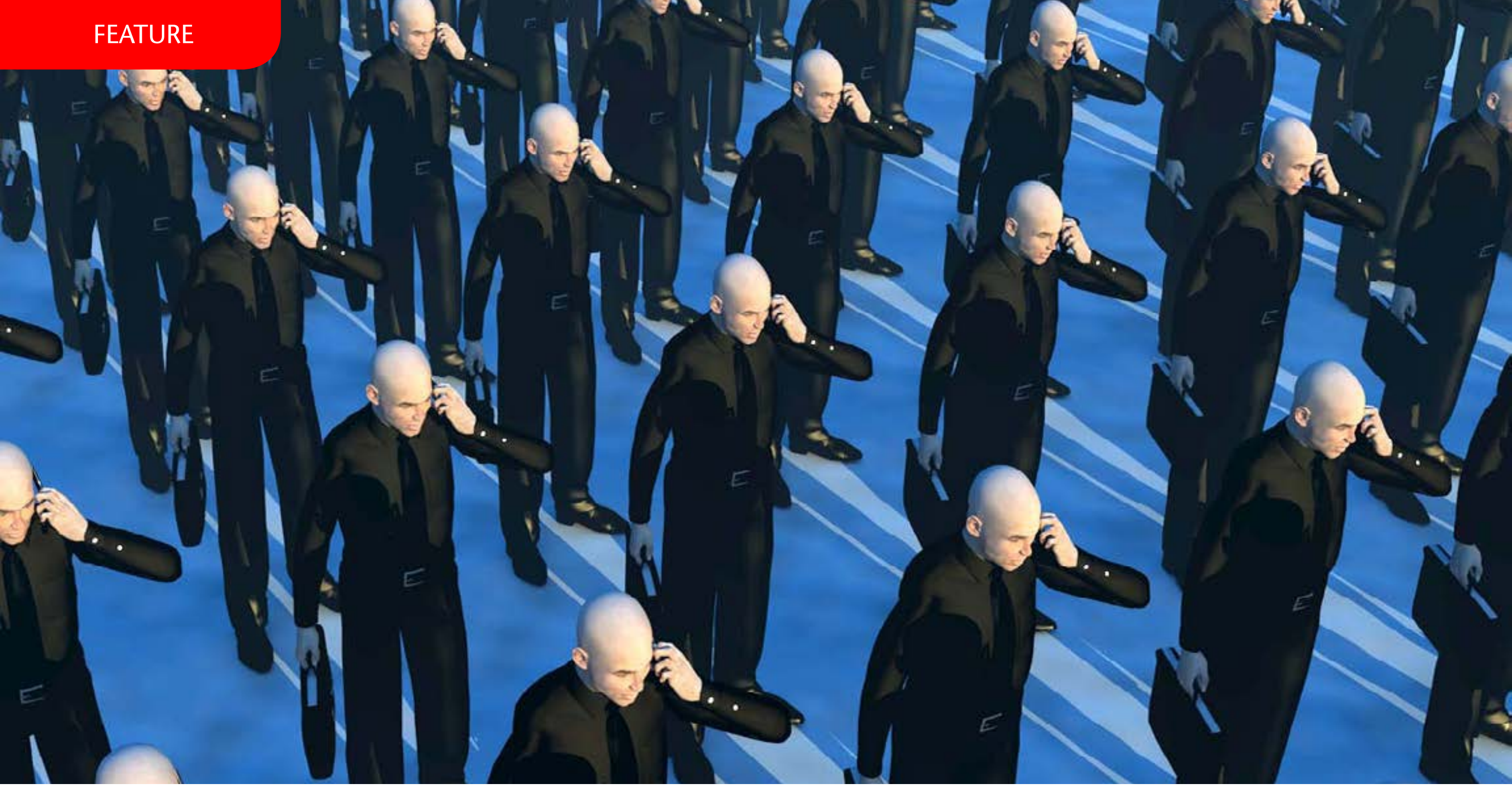

Buyer Beware:
Do Lifecycles Open the Door to Counterfeits?

by Steve Martin
COMPONENTS DIRECT

***SUMMARY:** Simply knowing what to look for and avoid has not been enough to halt the infiltration of counterfeits into supply chains, where they cause significant economic impact. Customers must constantly educate themselves about the tricks of the trade used by those who create and distribute counterfeit and unauthorized parts.*

In recent years, across many industries, there has been a growing mismatch between the lifecycle of a particular device or component and the lifecycle of the customer end-product. Reasons for discontinuing a device range from technology advancement (manufacturers may want to take advantage of advances in product or plant technology in order to preserve market leadership) to financial (to keep up with changing trends and customer demand, manufacturers are moving on to produce new, more profitable product lines) to the ability to continue to manufacture.

All of these factors result in difficulty for both customers and manufacturers who do not take the end-of-life (EOL) process lightly. However, customers and manufacturers must weigh the risks against the ever-increasing costs of keeping older lines running and the expense of supporting them. And at some point in the component lifecycle, component makers may decide to discontinue a device even if customers continue to need the device. In these situations, customers are left with the financial burden of purchasing a "lifetime" supply of obsolete or EOL components and/or searching for alternate channels of supply. This creates an opening, which in many cases is being filled by the "gray market." Purchasing products from the gray market increases the chances of purchasing a substandard product unfit for the purpose, or a counterfeit part.

According to a 2012 study by market research firm iSuppli, 57% of counterfeits reported from 2001 through 2012 were obsolete or EOL components. As Figure 1 illustrates, eliminating obsolete and end-of-life parts is not fea-

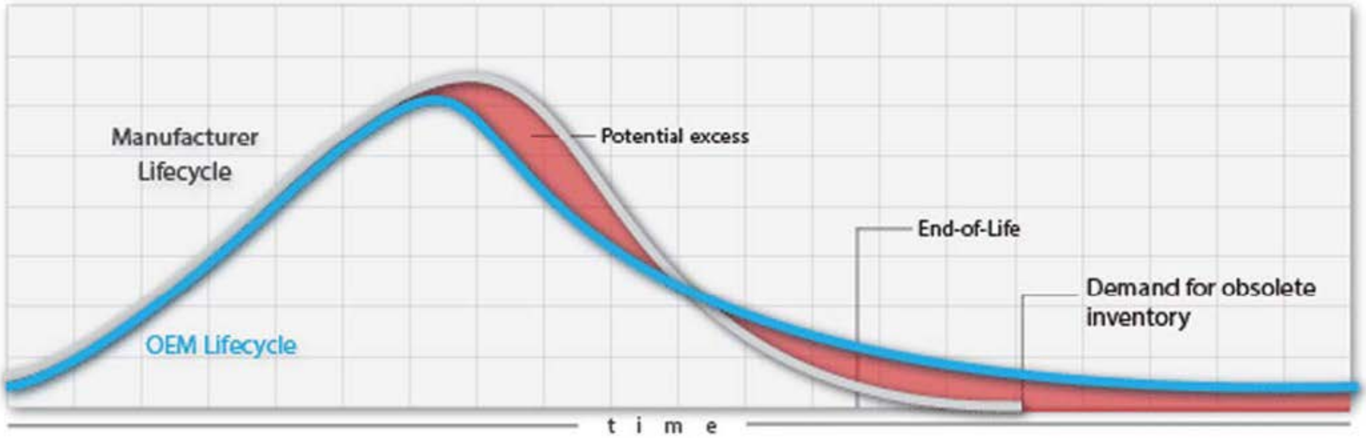

Figure 1: Chart showing typical demand for obsolete inventory after EOL.

sible, as they are vital to ongoing projects. The iSuppli research comes to the same conclusion: "…it's unrealistic or technically infeasible to economically eliminate the use of all obsolete parts." Faced with this, how does a buyer ensure that his company's supply chain remains counterfeit-free?

Key to Avoiding Fakes: Education

There are several ways in which electronics components such as integrated circuits, connectors, and power-management devices are counterfeited, but five methods have emerged as the most often used:

- **Empty shells:** These are chips which have the same external form factor and top marks as authentic parts, but are empty inside. Since they are the most easily detectable, empty shells have not proven to be as widespread in the electronics supply chain as more sophisticated counterfeit methods.
- **Pulls:** Pulls may be legitimate parts that have been recycled and repackaged as new, authentic parts, but that often become damaged in the process. Printed circuit boards are heated so that the chips can be more easily "pulled" off. The heating and handling processes often damage the components, which, if not detected, can cause massive problems when utilized in electronics production.
- **Blacktopping:** A process in which a thin black epoxy coating is applied to the top of a component so that a new part number and date code can be printed on it. Because the blacktopped part has the same dimensions as the one it is intended to copy, it usually passes visual inspection, but can sometimes be detected through X-ray inspection.

In addition to these obvious counterfeits, legitimate parts are making their way into the supply chain without going through authorized channels. Uninspected parts are legitimate components that do not go through the manufacturer's inspection and testing process, where defective parts are caught. Sample and scrap parts have been discarded because they are obsolete products, test failures, or excess inventory. "Dumpster divers" make a business of retrieving these components and reselling them. These non-conforming parts are nearly impossible to detect from authentic parts, since production and markings are the same, but they are equally dangerous if they make their way into the supply chain.

Reporting, Regulation Increasing

Simply knowing what to look for and avoid has not been enough to halt the infiltration of counterfeits into supply chains, where they cause significant economic impact (over $169 billion in annual risk, per iSuppli), and endanger lives when they fail to perform as expected. To bolster industry's anti-counterfeit efforts, industry groups and governments are becoming more proactive and aggressive. The Government Industry Data Exchange Program (GIDEP) is a cooperative government-industry group that has been instrumental in the fight against counterfeits. GIDEP has been at the forefront of encouraging increased reporting of counterfeits, something which has been hindered by industry's fear of liability.

Other groups such as the Independent Distributors of Electronics Association (IDEA) and the Electronics Resellers Association Inc. (ERAI) are helping to make reporting counterfeits easier and more transparent by instituting online forms and allowing anonymous reporting. Regulators are also doing their part. The 2012 National Defense Authorization Act encouraged the reporting of counterfeits by addressing the industry's fear of liability, although the rate of reporting has not yet increased considerably.

Despite increased awareness and education, reporting, and regulation, the first, and best, way to avoid the spread of counterfeits is to purchase components from franchised suppliers including franchised "excess & obsolete" (E&O) distributors. These authorized distributors support only authorized components with 100% guaranteed direct traceability back to the original component manufacturer. They operate with established process controls, and are certified to ISO 9001, ISO 14001 and ESD 20:20 standards for warehousing and handling procedures. Franchised E&O distributors, such as Components Direct, specialize in the fulfillment of obsolete and EOL components.

Industry organizations are stepping up to the plate, and E&O distributors can help address lifecycle mismatch and provide customers peace of mind. But in the end, OEMs must be constantly vigilant if they hope to avoid counterfeit and unauthorized components. **SMT**

Figure 2.

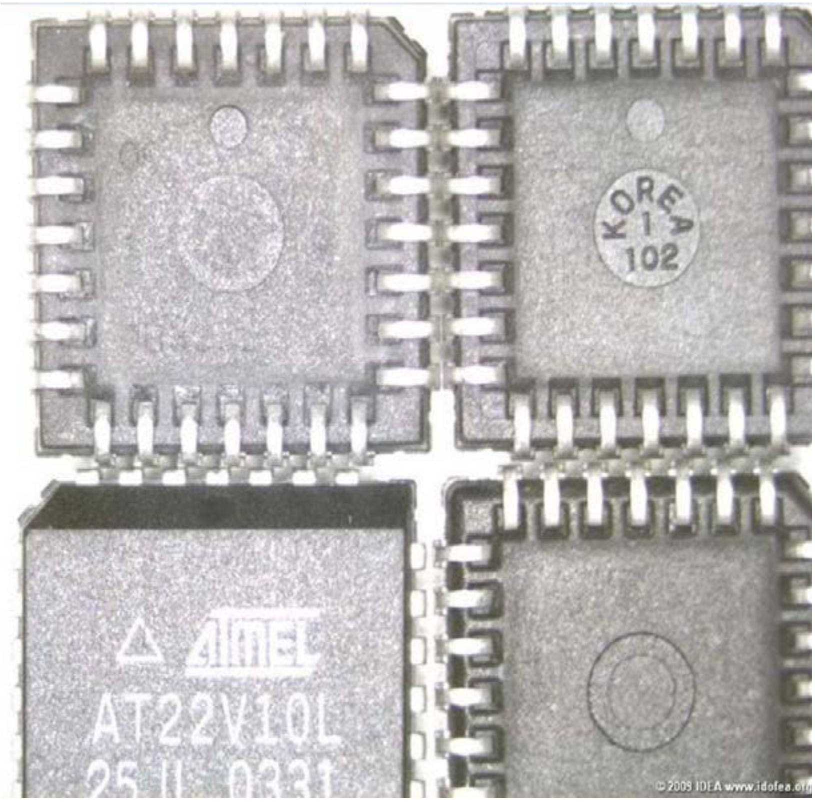

Figure 3.


Steve Martin is executive vice president of sales at Components Direct, where he has responsibility for all facets of the sales channel, incorporated with both upstream supplier and downstream customer business.

Replacing Automated Test Equipment

Courtesy of Seica

***SUMMARY:** The life span of automated test equipment typically does not exceed one or two decades. Sooner or later, no matter how well serviced and reliable the equipment, it will need to be replaced. All aspects of the process should be analyzed: Characteristics, the migration of test programs, test fixtures, and overall short- and long-term considerations.*

No matter how good, reliable, and well serviced, your automatic test equipment (ATE) often has a much shorter life span than the products it is assigned to test. This fact is particularly true in the defense and aerospace markets, where large investments are made and products and associated electronics may require service and repair for decades.

Take, for example, the F-16 fighter aircraft: Designed in the early '70s, and entered in service in 1979, the plane is a bestseller worldwide. Thanks to a midlife upgrade program that took place 20 years later, F-16s are expected to maintain operational capabilities over the next 10 to 20 years. Meanwhile, the ATE used to test electronics in the '70s is now only good for display in museums—even the subsequent generation that replaced those '70s machines is now out of production.

Indeed, the life span of ATE typically does not exceed one or two decades. Though most suppliers assure service and maintenance for a few years after their ATE has been discontinued, sooner or later users will receive a letter announcing the date after which any support will no longer be provided. That's when the good old ATE might start looking for retirement and asking for replacement after a long life of loyal service.

Before planning a replacement, users often look for alternative solutions to extend the life of equipment. The local supplier's office, for example, might be willing to provide, though with no assurance, extended service on a best effort basis. Replacement parts might be offered on the market through brokers. When multiple pieces of ATE are at the same site, some could be sacrificed and used as stock of replacement parts. But such measures will only have the effect of delaying, not stopping, the end of life of ATE. As with any electronic product, failure rates will dramatically increase over time, quickly depleting the reserve of spare parts. At the same time, repair of failing parts will become increasingly more difficult as component availability is scarce and reliability is poor. The inevitable consequences are increased downtime, increased repair costs, and, finally, unacceptable loss of efficiency on test operations.

In some cases, a thorough analysis of the state of ATE might lead to a less painful conclu-


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sion: Replacement. This is possible when only a specific ATE subsystem is the source of the problem. A mid-life upgrade, for example replacing some obsolete instrumentation and perhaps the routing cards, can be more economically viable than replacing the ATE. To minimize costs, a solution should be engineered without impact to the ATE receiver, where existing test fixtures are engaged. The solution should be analyzed with respect to its impact on changes to the existing test program sets (TPS), performance compatibility, degradation of coverage, and required debug time and costs. Finally, unless the user has multiple ATE available where the midlife upgrade will take place, the downtime of test operations during the migration should be considered.

The last, drastic solution is the replacement of the obsolete test system and the transfer of all legacy TPS. It is a major project, and all aspects of the process should be analyzed: Characteristics of ATE, the migration of test programs, test fixtures, and overall short- and long-term considerations.

ATE Characteristics

As technology evolves, and when replacing a test system designed perhaps in the early '80s, one would expect no problems in finding overall better performance without any limitations. Unfortunately, this is often not the case – he may find that the features of his old system are no longer available on a new one. Such could be, for example, the case with the programmable logic levels available on the digital channels; perhaps more accurate, but limited to the swing requirements of modern low-power devices. The new system might have modern architecture where logic levels are generated locally on each channel card, but fail to match the original system's architecture featuring selection per channel out of two centralized families of levels.

Similar problems could be encountered on the flexibility and distribution of timing for high-speed operations. These problems should be analyzed and reported for each test program to allow proper counter-measures. Similarly, analog routing of signals might be tricky to reproduce on the new system, as a variety of solutions were taken in the past for such tasks to ensure simultaneous connection of multiple source instruments. Furthermore, one would expect to have new technology and new features on replacement ATE, but, at the same time, careful to verify the ability to cope with old characteristics. For example, if the end use of the system is for

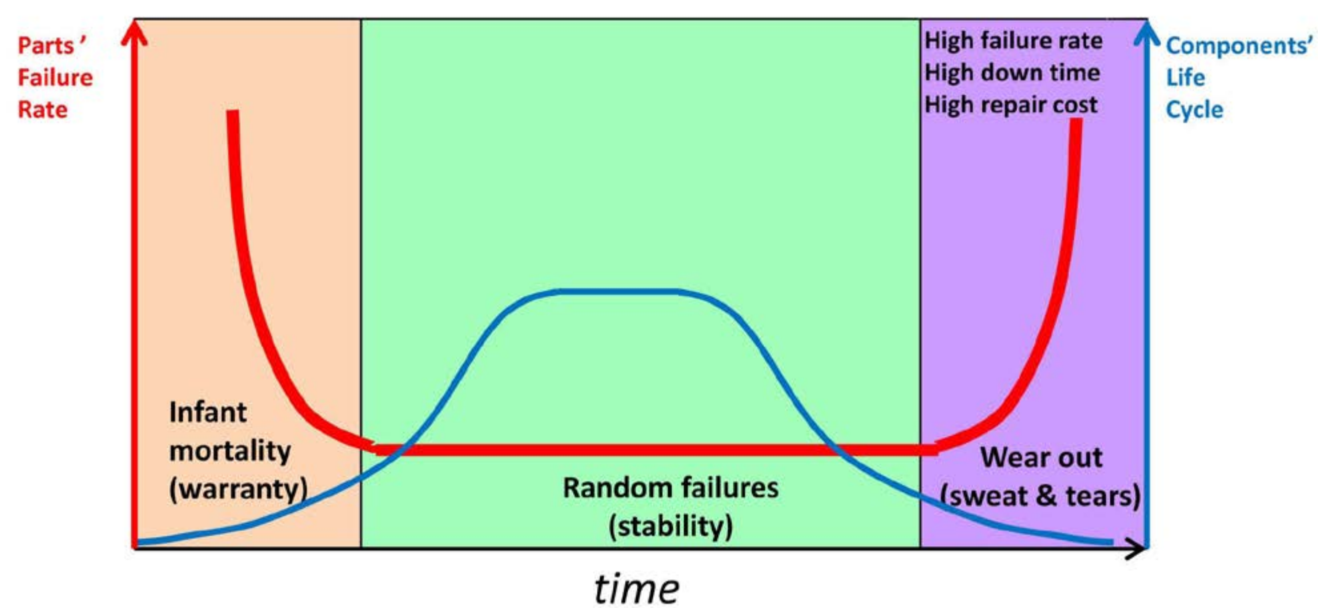

Figure 1: Failure rates will dramatically increase over time, quickly depleting the reserve of spare parts.

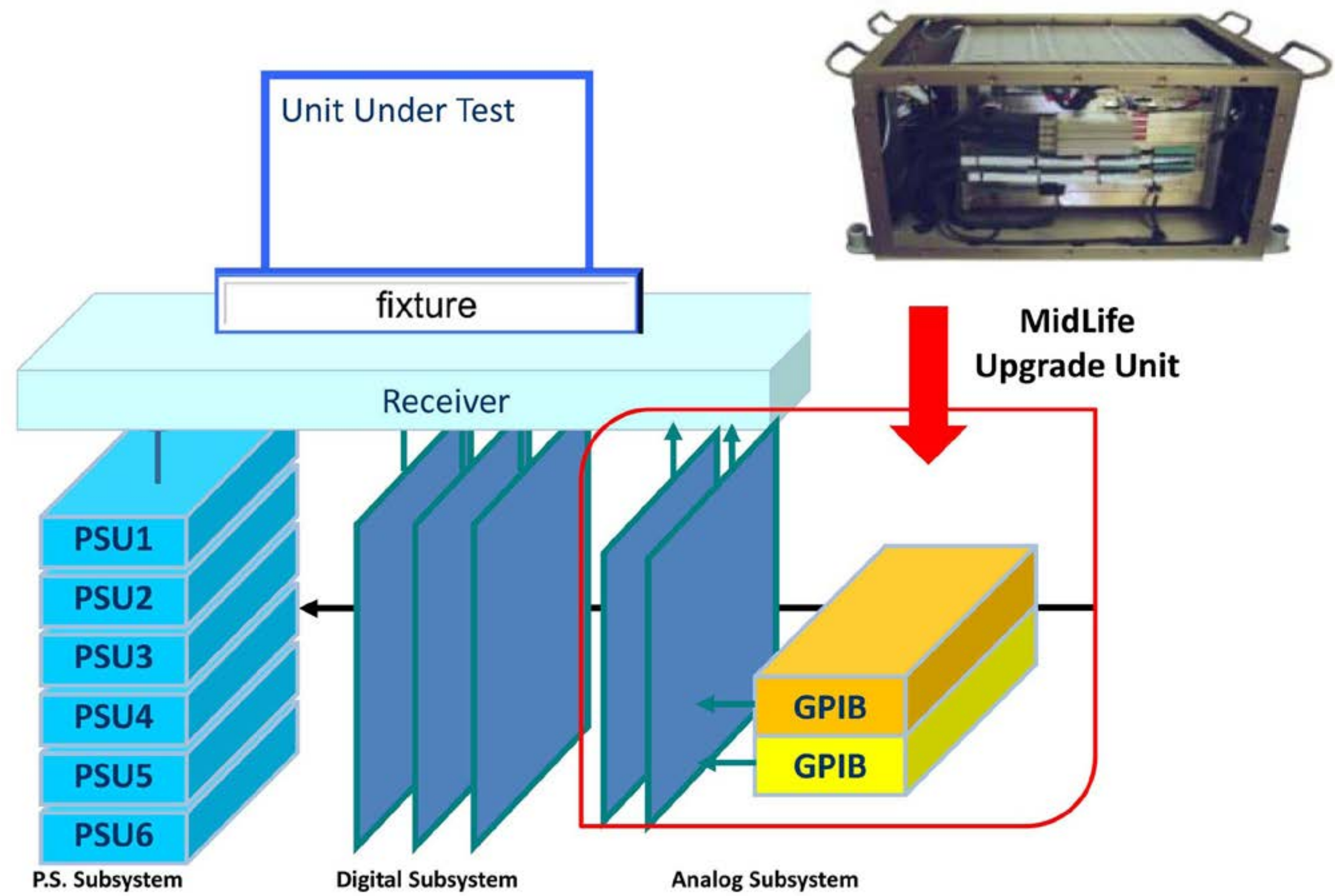

Figure 2: A mid-life upgrade—replacing some obsolete instrumentation and perhaps the routing cards—can be more economically viable than replacing the ATE.

board test and repair, more attention should be given to the ability to execute diagnostic and fault location. Old systems were driven by simulation and had diagnostic tools like fault dictionary and guided probe. Today's boards can hardly be simulated, and modern packaging prevents guided probe contact, thus the new system might miss this diagnostic capability. Old systems also featured analog-guided probe algorithms, tracing back faults across mixed-mode circuitry on the board under test. How many new systems still carry this capability?

Failing to cope with these issues will reflect either on loss of coverage and diagnostic accuracy, or on substantial cost of rework on existing test programs and fixtures; therefore, the ideal replacement system should offer performances adequately bridging on the past and at the same time offering advantages for the future.

The Migration of Test Programs

Anyone who has undertaken the process of ATE legacy replacement knows that the bulk of the cost is not around the test system, but the TPS migration. Unless the project on which the ATE is deployed concerns very few test programs that could be rewritten, in most cases it is indispensable to provide a software migration environment that ensures conversion of the old test programs to be executed on new ATE. A robust, well-designed conversion environment should be able to fully analyze the old ATE source files and flag any architectural or syntactic inconsistencies with the new ATE and provide suggestions for compliance. A user's interventions should be minimized and all conversion steps, warnings, and modifications should be duly reported.

To ease validation and debug, the converted test program should maintain a one-to-one correspondence with the source test program, carry through comments, and be self-documented. Whenever desired, the new ATE should be able to mimic the original human interface so that discomfort to test operators is minimized. Usually the development of the conversion environment follows a good dialog between the supplier and the end user to identify and satisfy specific requirements. An example could be the requirement to maintain in operation the old test simulation environment on the new system, thus including in the conversion package back-annotation from the new tester language and the old simulator.

In the end, the quality of the migration tools and the time-per-program spent on the conversion and debug process will have a major influence on the overall cost of the project.

Test Fixtures

If very few test fixtures are part of the original project, it might be convenient to rebuild them targeting the new tester receiver. But as soon as the number is over a few units, the cost of rebuilding becomes exorbitant. The cost of rebuilding 20 to 30 test fixtures could easily match the cost of the ATE and, of course, if more systems are involved, test fixtures should also be multiplied. The first proposal from ATE suppliers is usually to build a fixture adaptor to be inserted between the new ATE receiver and the existing test fixtures. This solution has a controlled one-time cost, but might not be as simple as described. The fixture adaptor might be heavy and bulky, generating logistic manipulation issues.

Most importantly, the adaptor inevitably degrades the quality of the test signals, which can impact TPS debug time or even degrade the coverage and/or the diagnostic accuracy. A better solution would be to reproduce the old receiver and to re-wire directly the ATE resources to best

Figure 3: The first proposal from ATE suppliers is usually to build a fixture adaptor to be inserted between the new ATE receiver and the existing test fixtures.

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match the original test system's electrical conditions. This might require some engineering effort, particularly if some of the components of the original receiver are no longer available on the market, but the end result will be worth the effort.

In summary, test fixtures might represent a major part of the cost of legacy replacement. Whether they are rebuilt or maintained, the solution should be evaluated with respect to its impact on the overall TPS generation, debug, and validation cost.

Final Considerations

ATE replacement is a major project and all factors should be taken into account to make the best decision. If the operation means not only changing ATE, but also the supplier, the user should be assured about his short-term and long-term support, should check for reference success installations, and be assured on the real commitment to this type of business. If the user does not have technical resources to undertake the TPS migration, it is important to verify the ability of the supplier to provide a turn-key solution, rather than addressing third-party services. If the user has multiple different ATE in view of future replacement, the ability of the solution to deal with all of them is definitively a plus.

Finally, one should focus not only on the replacement issues, but consider the benefits that the new ATE will bring for new TPS developments; such as the capabilities of the system to master improved digital performance, to cope directly with new test technologies, like for example JTAG 1149, or to embrace DSP concurrent analog test functionalities should be key to the decision.

In summary, many suppliers and solutions are available on the market. Making the right choice requires a comprehensive, detailed analysis, with much attention given to long-term operational costs. **SMT**

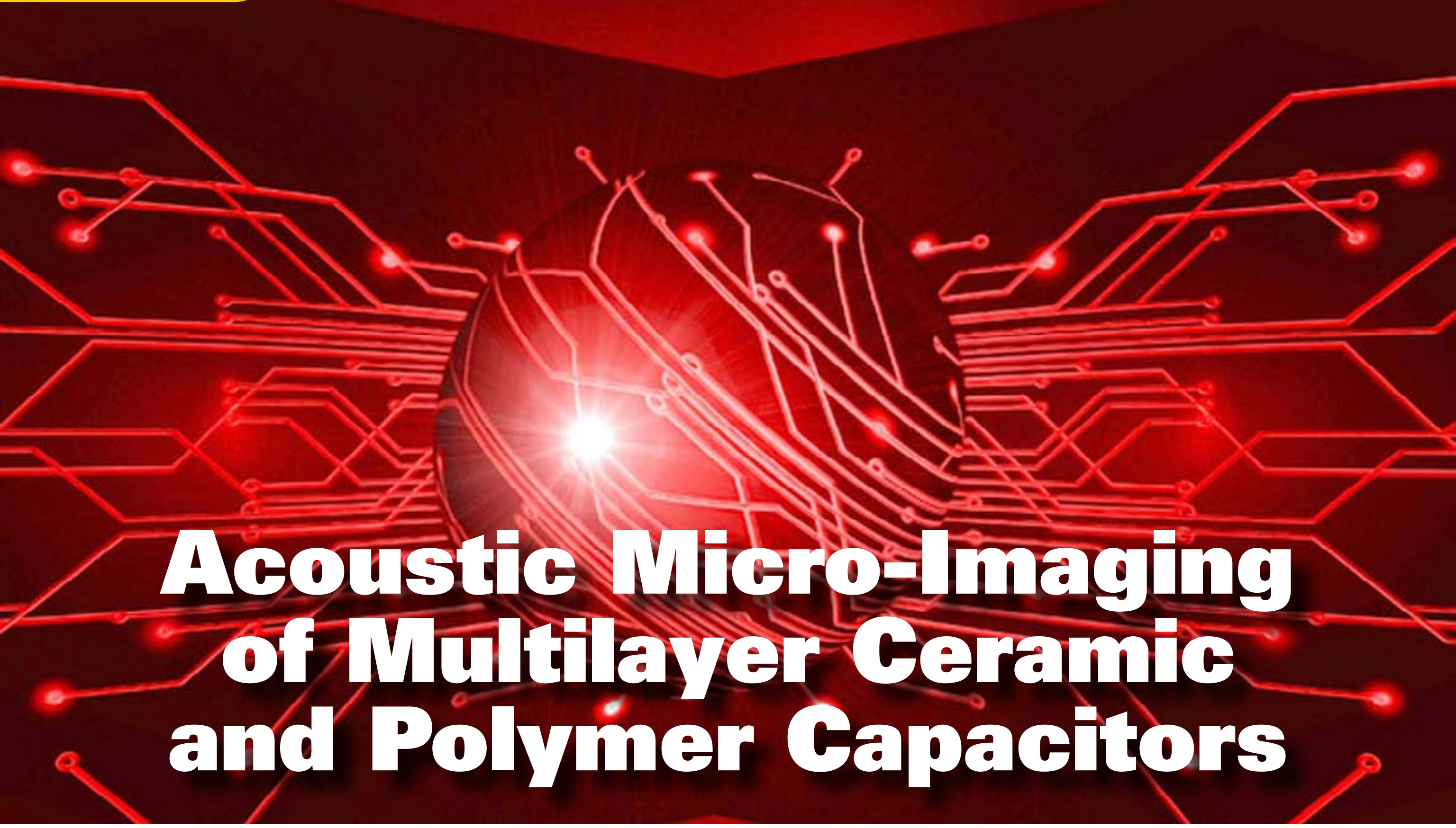
Video Interview

Solar Industry Update

by Real Time with... IPC APEX EXPO 2013

Custer Consulting's Jon Custer-Topai talks about the solar industry and prospects for the market in 2013. Although it's a difficult market, the prospects for those with the courage to invest and persevere look great!

realtimewith.com



Acoustic Micro-Imaging of Multilayer Ceramic and Polymer Capacitors

by Pedro Ramirez
SONOSCAN, INC.

***SUMMARY:** They are inexpensive and relatively simple in design, but multilayer ceramic capacitors (MLCCs) are nevertheless capable of causing unanticipated field failures whose severity may range from very minor to catastrophic.*

The root cause of multilayer ceramic capacitor (MLCC) failures is very often some type of internal structural defect such as a crack, delamination or voids. These types of defects typically create an open circuit or leakage paths between electrodes that can disrupt the capacitor's functioning and impact the performance of the system.

Because the defects are gaps in solid materials, they are easily imaged by the ultrasound pulsed into MLCCs by acoustic microscopes. SonoLab has been imaging MLCCs for three decades. Typically, the screening involves a range of small to large lots of loose capacitors, with the purpose of identifying and removing capacitors that meet the user's definition of reject before assembly begins.

Screening Acoustically for Defects

In a typical screening operation, up to several thousand MLCCs are arranged on a tray for imaging. During imaging, the transducer of a microscope such as a Sonoscan C-SAM scans over the tray, pulsing ultrasound into the MLCC and receiving the return echoes several thousand times a second. Data in the return echoes make up the acoustic image.

Even though it consists of two different layered materials (electrode and dielectric), the bulk of a capacitor acts much like a homogeneous material and sends back few significant echo signals to the transducer. But where the pulse of ultrasound strikes a crack, delamination or void, the great difference in acoustic properties between the air in the gap and the solid material just above it reflects virtually 100% of the ultrasound. This very high amplitude reflection means that gap-type defects will show up as very bright features in the acoustic image.

Individual capacitors with significant internal defects are removed from the lot. The remaining capacitors are known, at this time, to be free of internal defects that could lead to functional failures. Most MLCCs go into high-reliability military, aerospace or medical appli-

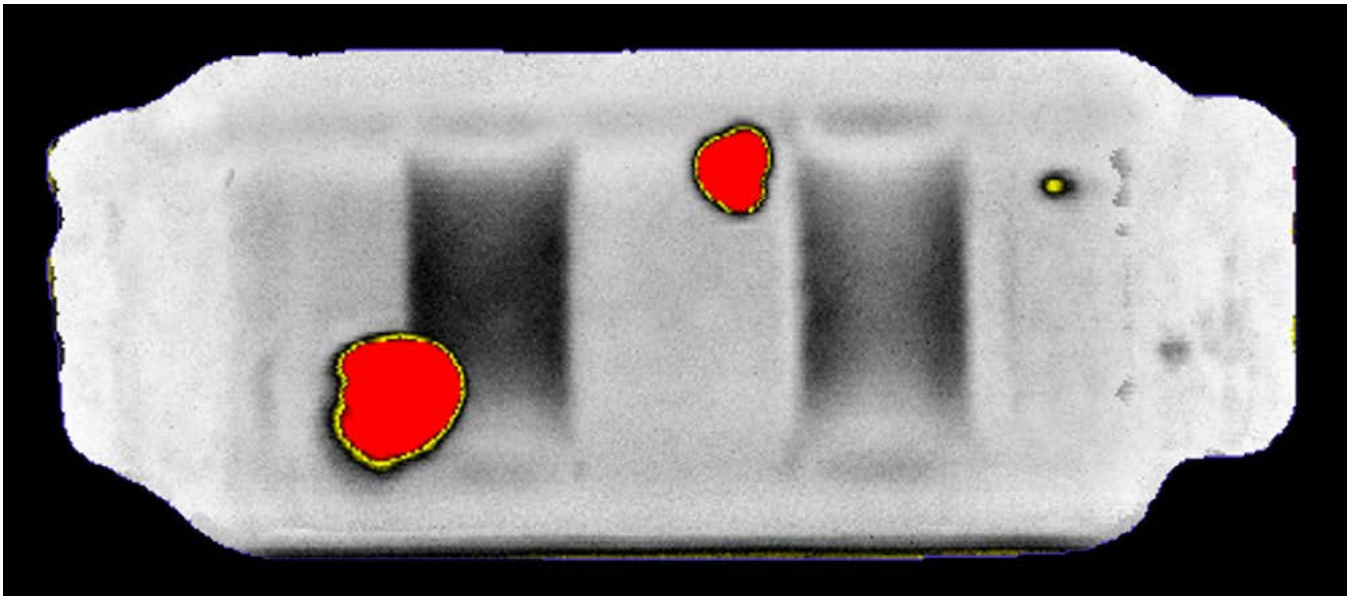


Figure 1: Bulk acoustic image of a typical ceramic chip capacitor. Electrode plates are gray; delaminations are red; void is yellow.

cations. Some are used in high-reliability commercial applications such as high-end electronics. In other cases screening is performed on a sampling basis for the purpose of lot qualification.

Figure 1 depicts a typical acoustic image of an MLCC. Echoes from the various depths in the capacitor arrive at the transducer at different times. A method called bulk scan imaging is generally used with capacitors; this method accepts for imaging all echoes from all interior depths of the capacitor. The ultrasound is said to be gated on the entire thickness of the capacitor.

In Figure 1, the two red features are delaminations, while the smaller feature at upper right is probably a void. In the color map used here, red indicates the highest echo amplitude. The top view of the electrode plates is visible—the plates are gray, indicating a material interface giving an echo of much lower amplitude. This MLCC would be rejected from any high-reliability application because the defects make it likely to fail.

Gate-by-Gate Imaging

In the past few years capacitors themselves have changed, in part by becoming smaller, but also by the use of new materials, particularly polymers, to replace the ceramic dielectric materials. The technology for viewing MLCCs acoustically has also advanced. Sonoscan has introduced an automated gate-setting system that lets the acoustic microscope operator set the locations and thicknesses of a number of individual gates.

Each individual gate represents a thin horizontal “slice” of the capacitor and produces its own acoustic image of that slice. The gates are usually set up to be adjacent to each other and all of the same thickness, but other arrangements are possible—overlapping gates, separated gates, and gates of different sizes. The maximum number of gates is 100 (or 200 with a dual-channel machine). The acoustic image of a single internal slice of an MLCC can be a useful diagnostic tool when it is necessary to understand the details and structure of internal anomalies without physically destroying the sample.

Figure 2 shows the images from three individual gates in a single MLCC. This was a high-voltage capacitor measuring 10.1 mm x 10.1 mm x 2.98 mm. The microscope operator chose to set a sequence of 50 equal gates encompassing the entire thickness of the MLCC; thus,

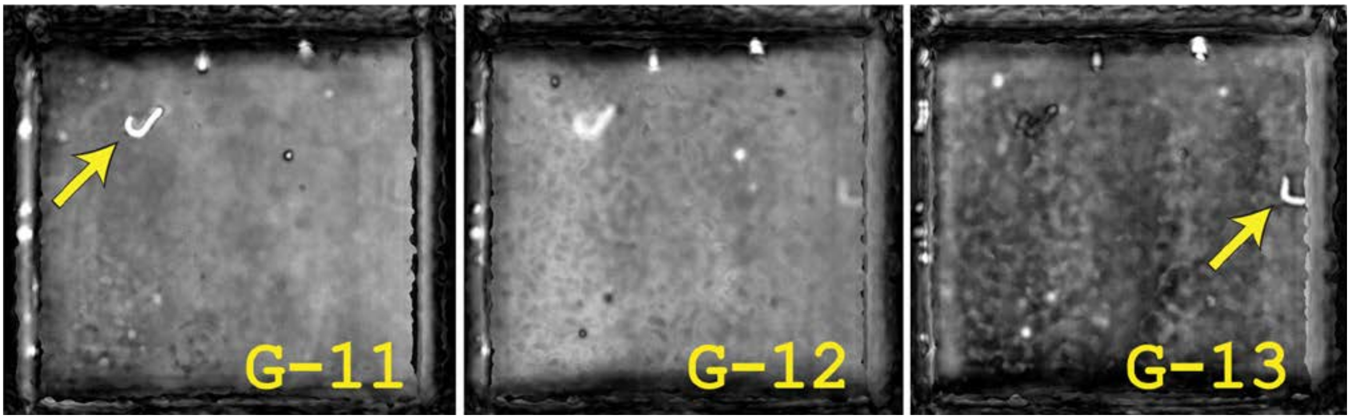


Figure 2: Acoustic images of three consecutive PolyGates in a ceramic chip capacitor. Each gate is approximately 60 microns thick. Arrows show defects that change with depth.

each gate has a thickness of approximately 60 microns. Destructive analysis after imaging showed that the MLCC had a total of 42 electrode layers, so each gate covers somewhat less than one layer.

Gate 11 shows the expected medium-gray field in defect-free areas of this slice, as well as a somewhat elongated, curved defect at upper left (arrow). From its shape, this defect is likely the void left by an airborne fiber particle that was incinerated during firing of the ceramic.

Some 60 microns deeper into the part, in Gate 12, the J-shape defect is beginning to fade, probably because only the lower portion of the void is actually within Gate 12.

But in Gate 13 a new defect appears (arrow)—a defect that appears to be another elongated void, perhaps also left by an incinerated fiber particle. This defect is faintly visible in the Gate 12 image. If we look at the location of the similar void seen in Gate 11, it is actually visible in Gate 13, but as a dark feature. The reason: This void now lies completely above the depth from which ultrasound is being reflected, and the air in the void blocks the return path of echoes from Gate 13. The void is therefore seen as an acoustic shadow.

MLCCs Keep On Shrinking

The strong demand for ways to save space and weight in cell phones and other systems has led to the design of truly tiny MLCCs. What matters is the total capacitance of a capacitor, which is in part determined by the total x-y area of the electrode plates. An MLCC that places many very thin electrode plates, separated from each other by very thin dielectrics, into a tiny x-y area gives a manufacturer a significant advantage.

Some 16,000 of the tiny capacitors measuring 0.020 in. x 0.010 in. can be placed on a single tray and imaged simultaneously, but this is a fairly rare occurrence. More often, full trays of 0.040 in. x 0.020 in. and of 0.060 in. x 0.030 in. MLCCs are scanned.

The ultrasonic frequency used for a given lot of MLCCs depends on the thickness of the capacitors, rather than on their x-y dimensions. 50 MHz is generally the starting point, and probably the most frequently used frequency. Thinner parts may be imaged using 75 MHz or 100 MHz transducers (higher frequencies give better spatial resolution). Very thin capacitors might be imaged at 230 MHz, although this is a bit unusual and gain may be limited. Thicker MLCCs—usually high-voltage types—may be imaged at 30 MHz. When a relatively thick MLCC is destined for a particularly critical application, each face of the capacitor may be imaged at 50 MHz (higher resolution), after which a single face may be imaged at 30 MHz (better penetration).

One challenge encountered when imaging very tiny MLCCs has to do with accept/reject standards rather than the capacitors themselves. The military standard is that a void in the dielectric of an MLCC is cause for rejection if the thickness of the void exceeds one-half of the dielectric thickness. The reasoning is that a void of this size or larger may turn into a leakage path between two electrodes.

But MLCCs are now shrinking down to only 0.03 in. (0.762 mm) thick, with up to 240 electrode layers, for a total of 480 layers. Each layer is thus about 0.000625 in. (0.0016 mm) thick, or 1.6 microns. A void half this size would be less than 1 micron in diameter—undetectable by the highest frequencies available because it is smaller than the spot size of the transducer. Larger and presumably more dangerous anomalies such as delaminations and multilayer voids can be imaged in these capacitors, but not the smallest anomalies permitted by current military standards.

The New Breed of Polymer Capacitors

Lots consisting of new types of capacitors that use polymers have begun to show up at Sonoscan. In these capacitors, the dielectric material is a polymer rather than a ceramic. One obvious physical advantage is better resistance to cracking. One of the most frequent causes of cracks in MLCCs is the singulation of panels by snapping the boards apart. The stresses involved may create more or less vertical or diagonal cracks, typically near the terminations. Polymer capacitors are presumably more forgiving of these stresses.

The polymer caps are not quite as easy to image as MLCCs, however. Ceramic is a good transmitter of ultrasound, while polymers tend to absorb ultrasound. A ceramic capacitor of a given size might be imaged at 50 MHz, while a polymer capacitor of the same dimensions might be imaged at 30 MHz in order to gain penetration, while giving up a little resolution.

Figure 3 is the side view diagram of a very thin (0.040 in.) organic polymer surface mount capacitor, one of several new types of capacitor to use a polymer. The pellet is a block of porous tantalum or another metal that has been immersed in an electrolyte to form an oxide lay-

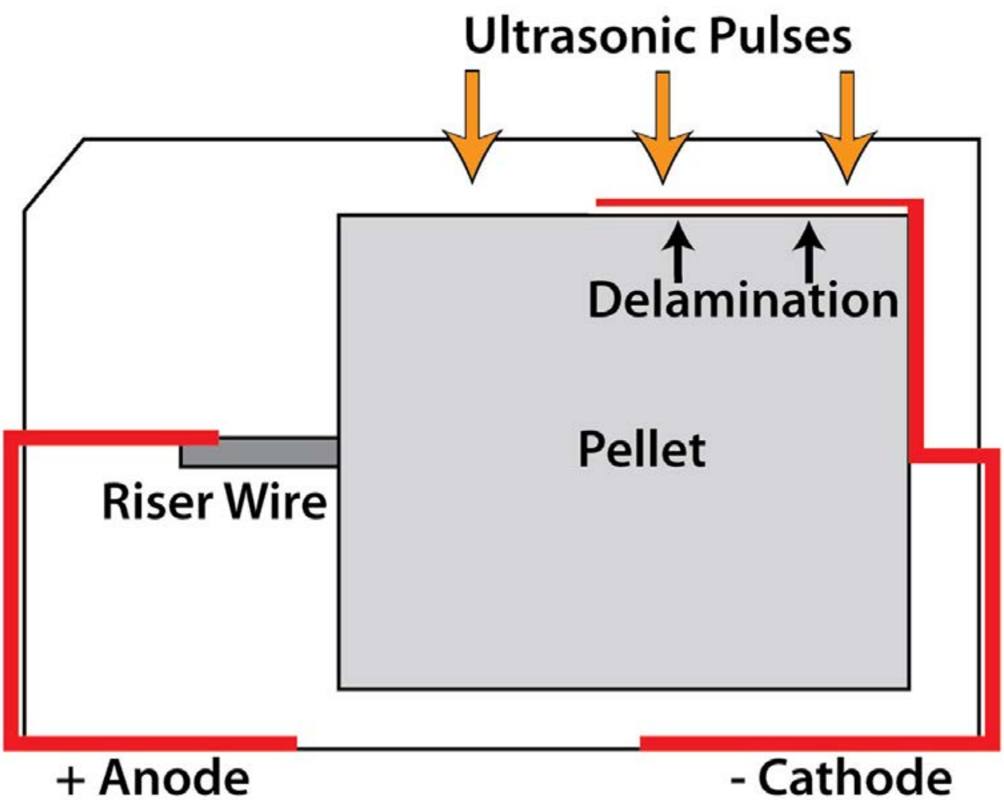


Figure 3: Side view of an organic polymer surface mount capacitor.

er on the pores. Its interconnects are the wide anode and cathode, both of which, in the top view, are as wide as the pellet. The anode is connected to the pellet by a riser wire, while the cathode is connected by a conductive polymer.

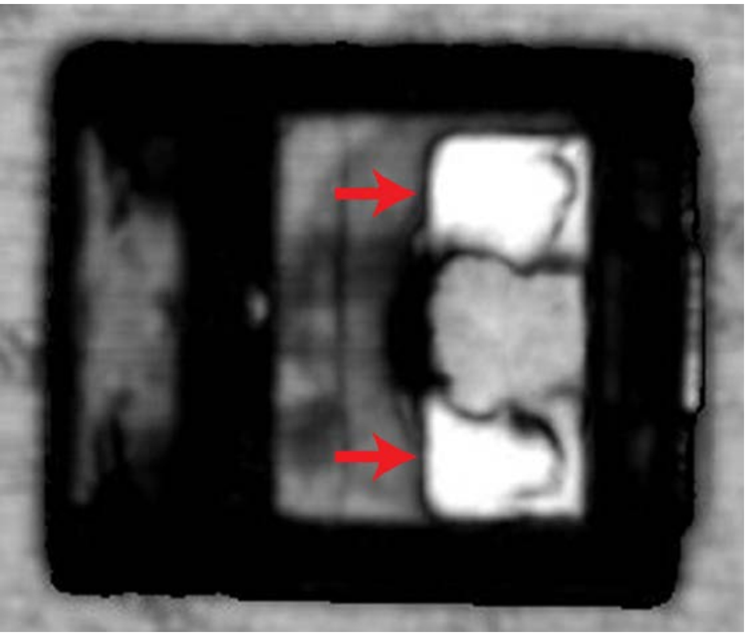


Figure 4: Acoustic image of an organic polymer surface mount capacitor. Arrows point out delaminations of the cathode from the pellet.

Because the top is thin, ultrasound can be pulsed into the top surface of the capacitor (as shown in the diagram) at a frequency of 50 MHz. The resulting acoustic image is shown in Figure 4. The two arrows point out bright white delaminated areas of the lead frame from the top of the pellet. The polarity of the echo (in this case, negative) demonstrates that the delamination is between the pellet and the lead frame, and not between the lead frame and the plastic package. The central part of the lead frame between the two delaminations is darker gray shows better bond quality. The left half of the pellet is gray, and is not covered by the lead frame.

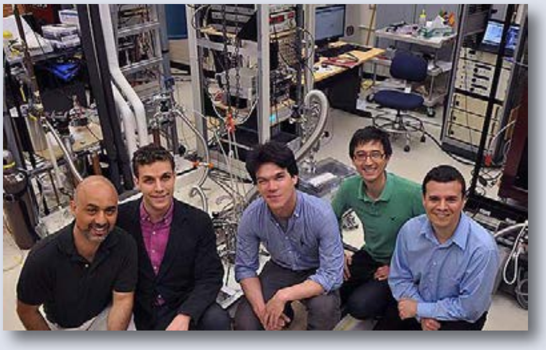
Thanks to their low cost, utility and simplicity, ceramic and polymer capacitors are growing in popularity. Acoustic micro-imaging is a proven method for detecting failures such as cracks, delaminations, and voids. **SMT**

Pedro Ramirez is an applications engineer/capacitor specialist at Sonoscan, an authority on the application of acoustic micro imaging (AMI) technology for nondestructive internal inspection and analysis. Ramirez has been with Sonoscan since 1984.

Graphene & Boron Nitride Combined to Create Semiconductor

Graphene has dazzled scientists since its discovery more than a decade ago with its unequalled electronic properties, strength, and light weight. But one long-sought goal has proved elusive: How to engineer into graphene a property called a band gap, which would be necessary to use the material to make transistors and other electronic devices.

Now, new findings by researchers at MIT are a major step toward making graphene with this coveted property. The work could also lead to revisions in theoretical predictions in graphene physics.



The new technique involves placing a sheet of graphene, a carbon-based material whose structure is just one atom thick, on top of hexagonal boron nitride, another one-atom-thick material with similar properties. The resulting material shares graphene's amazing ability to conduct electrons, while adding the band gap necessary to form transistors and other semiconductor devices.

The work is described in a paper in the journal Science co-authored by Pablo Jarillo-Herrero, the Mitsui Career Development Assistant Professor of Physics at MIT, Professor of Physics Ray Ashoori, and 10 others.

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EVOLUTIONARY SOLUTIONS

Lean In

by Karla Osorno
EE TECHNOLOGIES, INC.

"Waste" is a "four-letter" word, especially for manufacturers who attract and retain customers only when they add significant value. Waste is anything that does not add value to the product being sold to the end customer. Some examples include motion, defects, overproduction, transport, waiting, inventory, and extra processing.

But how do manufacturers identify waste and eliminate it from manufacturing processes? And how do they do this on an ongoing basis to ensure that waste does not creep back into their workplace? The answer is to adopt philosophies and systems that are proven to work. Manufacturers must Lean in to this effort relentlessly to get desired results.

Lean Manufacturing

Lean manufacturing, or "Lean," is defined as a production practice that considers the expenditure of resources for any goal other than the creation of value for the end customer to be wasteful and a target to be eliminated. Makes sense, right? Will the customer pay for the activity or process? If yes, then do it because it is value added, and if not, eliminate the activity or process because you will not be paid for it.

Lean manufacturing is a management philosophy originally from Japan. It derived mostly from the Toyota Production System (TPS). Although Lean conceptually has been around for more than six decades, it was identified as "Lean" in the 1990s. It has passed the test of time and proven to work successfully when companies work it consistently over time.

Built on the simple concept that customers will not pay for mistakes, successful Lean manufacturing starts by educating teams. Lean requires culture changes and shifts in thinking. It is necessary to shift from traditional manufacturing mindset to seeing everything from the customer's point of view.

For example, traditional thinking might look for ways to fine-tune the process steps in an effort to better utilize employee resources

or to save small increments of time. From the customer's point of view, revolutionizing the process may be more in order. This would require that teams question every activity, as well as the value to the customer. It helps to pretend you are asking the customer, "Would you pay for steps 1-5 of this specific process?" With that question in mind, manufacturers would make more significant changes than simply fine-tuning the existing process.

Remember: The goal is to eliminate waste. Waste is a reflector of imperfections of the system and must be rooted out and removed.

Implementing Lean for large and small jobs in your plant is beneficial and never time wasted. Lean may seem like efficiency planning and optimizing, yet learning the mindset and skills, then implementing the practice can be challenging. Historically, companies who choose to Lean in remain competitive and profitable.

> ***Realize there is waste in the system. If you have not already Leaned out your organization (and sometimes even if you have), then you have waste. Acknowledge this immediately. Have conversations with your team to acknowledge this reality.***

Lean In

What does it mean to Lean in? Traditional manufacturing looks at making each department in the organization efficient. True Lean says it only matters if the whole organization works together and waste is eliminated. Suboptimization is the enemy because it does not matter how each department performs if the whole system includes waste.

The following are some practical overview steps to Lean in and eliminate waste.

1. Realize there is waste in the system. If you have not already Leaned out your organization (and sometimes even if you have), then you have waste. Acknowledge this immediately. Have conversations with your team to acknowledge this reality. Manage the conversations and ensure the team knows that this exercise is for a purpose. No blame, shame, or other morale busters allowed during these conversations. The goal is to shift thinking and if there is a heavy-handed consequence when waste is discussed, the conversation will stop and Lean will be theory, and not reality, in your plant.

2. Identify types and causes of waste in your workplace. You are looking for root causes. Using Lean means you will never treat symptoms. Your efforts will only be effective when you address the root cause issue and remove the root issue permanently.

3. Find the solution to the root cause of the issue. Use Lean manufacturing tools to address the root cause. In your solution, consider the entire process. It is important here to look at the whole picture by looking at the whole system. A Lean solution is only a solution if it does not have a negative impact to the whole system. For example, addressing inefficiencies in one part of the system may create excess inventory or labor in another part of the system. Look at the solution and make sure the net effect to the entire organization is positive.

4. Implement and test the solution. Are the results as intended? If not, then make corrections or adjustments based on discoveries during the implementation process. Training and follow up also occur during this final stage. Likely, this step will take the most time. And as with each step, use the appropriate Lean tools to make sustainable changes. As you can see, earlier efforts at changing culture and learning the tools were a great investment to make.

Lean Tools

Having a Lean mindset is most important because actions will come from thoughts and beliefs. If you have not already, learn the many tools and techniques available to you so you can practically carry out your new beliefs. Here are just a few Lean tools: 5S, value stream maps, and kanban systems.

5S

5S is a technique that results in a well-organized workplace complete with visual controls and order. It brings discipline and standardization to the workplace. It's a culture and environment that suggests "a place for everything and everything in its place for when you need it." The 5S in Japanese (English) are Seiri (Sort), Seiton (Set in Order), Seiso (Shine), Seiketsu (Standardize), and Shitsuke (Sustain).

5S systems create work environments that are clean, uncluttered, safe and organized. People become empowered and engaged. When this happens processes flow well and the customer's needs are met.

Value Stream Maps

Value stream maps are a visual tool for identifying and eliminating waste. When you can see the flow you can see the waste and then work to remove the waste. The current process including all value and non-value added steps are drawn. By viewing and understanding the flow, teams can discuss the required changes. Changes will not be done by fine-tuning the current flow. Instead, changes will be done by envisioning the future state of the process and then revolutionizing the process.

Kanban

Kanban is a communication system and one of the simple tools of Lean. Kanban cards, marked spaces, and other visual indicators are used to signal requirements for the next step in the process. When materials are pulled to the next operation, there is a gap left signaling a need for replenishment. Sometimes the trigger is electronically communicated in addition to the physical vacancy.

Kanban can be used internally and also with suppliers and external parties. This is the ultimate aim of Lean manufacturing and results in lower lead times, lower costs, and space savings. The key to success is that kanban must be used in conjunction with other tools and techniques for there to be significant results.

Contract Manufacturing Specific

Lean manufacturing originated and has been practiced most frequently in large high-volume/low-mix environments. Spending the time to understand tools, map processes, identify waste and create optimal processes makes sense for projects that go on for days or weeks. However, in contract manufacturing, the environment is low-volume/high-mix and projects go on for hours or days and not generally for weeks. Thus, the costs of Leaning out the project can be more than the profits on the job.

> *"Spending the time to understand tools, map processes, identify waste and create optimal processes makes sense for projects that go on for days or weeks. However, in contract manufacturing, the environment is low-volume/high-mix and projects go on for hours or days and not generally for weeks."*

Yet, giving up on Lean thinking, cultures, and tools would be a mistake. Strong contract manufacturers Lean in and make it happen. Tools identified above and also cell systems, pull strategies, and takt time all play a vital role in implementing Lean as a contract manufacturer.

Cell systems can eliminate motion and waiting waste. Rather than sending products to another area for subsequent processes, the product stays in the cell where equipment and skilled employees complete it. The focus with cell systems is on the overall flow and not on sub-optimized individual departments. Often, workers in cells have multiple skills creating more flexibility within the cell.

Pull strategies vary from traditional manufacturing push systems. In push systems, the product is manufactured regardless of the requirements from the next operation or end customer. The disadvantage of push systems is waste in the form of over-production and excess inventory.

In a pull system, products are not manufactured until the next process requires or "pulls" the product. Ultimately, this means that the customer's current demand creates the trigger for production. This also results in a reduction of work in process (WIP). Responsiveness, flexibility and elimination of waste are the primary benefits of pull systems.

Takt time or cycle time sets the pace for manufacturing lines. It is calculated by taking the net available time for production divided by the number of units required by the customer for that same available time. For example, if you have a seven-hour work day excluding breaks, and you have demand for 100 units, then the takt time in minutes is 4.2 minutes (4 minutes, 12 seconds). This means that one unit is completed every 4 minutes and 12 seconds.

One benefit of takt time is easy identification of bottlenecks when the product is not moving on the line in time. Another is that other operational issues including station delays are easily identified. Also, since there is only a certain amount of time to perform the actual value-added work, there is strong motivation to get rid of all non-value-added tasks (such as machine set-up and transporting products).

To Lean in is to hold your foot fully on the accelerator and commit to your best work. Combine this with Lean manufacturing principles and you have the antidote to your waste problems. Companies who are in the arena and not sitting on the sidelines empower their teams to do their best work. Their best work will involve Lean manufacturing activities. For jobs large or small, the right choice is to Lean in and get the job done in a way that adds tremendous value to all. **SMT**


Karla Osorno is business development officer for EE Technologies, Inc., an EMS provider delivering complete engineering and manufacturing services with locations in Nevada and Mexico. Contact Osorno here.

Mil/Aero007 News Highlights

Sanmina's China Facility Earns AS9100 Certification

Sanmina Corporation announced that its Wuxi, China PCB facility has achieved AS9100 certification. The certification recognizes the company's ability to meet the high-quality assurance standards in products developed for the aerospace industry.

Endicott Interconnect's SiP Tech Employed by Lockheed

Endicott Interconnect Technologies, Inc. (EI) has announced that its System-In-Package technology performed successfully as a key subsystem of Lockheed Martin's Extended Area Protection and Survivability (EAPS) program during a test on March 22 at White Sands Missile Range, New Mexico.

Axis Completes AS9100 Rev C Assessment

"These auditors were new to our latest systems and it was very encouraging that no non-conformances were raised and that our home-grown systems were recognised as best in class. This gives us a great platform to improve customer service and quality," commented Chris Jukes, quality assurance director.

Q3 Sales Up 16%, Net Income Down for Sparton Corporation

"Now that third quarter softening issues are behind us, we expect a very strong fourth quarter and anticipate that our fiscal 2013 full-year adjusted earnings per share results will more than outpace our fiscal 2012 adjusted earnings per share of $0.91," said Cary Wood, president and CEO.

Productivity Improvements Drive Nortech's Q1 Sales

"Our ongoing productivity improvements, including initiatives in automation and Lean manufacturing, helped drive our profitability in the quarter as we saw our gross profit percentage increase 190 basis points versus the first quarter of 2012," said Mike Degen, CEO.

OSI System Reports 5% Revenue Drop in Fiscal 3Q13

Deepak Chopra, OSI Systems' chairman and CEO, stated, "We are pleased to announce the results of our third quarter operations. We achieved record earnings for the twelfth consecutive quarter as a result of significant operating margin expansion, led by our security division."

Probe Nets Contract from Sensing Device Manufacturer

Probe Manufacturing, Inc., a global electronics design and manufacturing services company, has secured a $250,000 purchase order from an existing customer that is a leading U.S. manufacturer and supplier of advanced sensing devices for such industries as medical, aerospace, automotive, and automation robotics.

Orbit's Sales Up in Q1, But Contract Delays Hinder Growth

"Our backlog at March 31, 2013 slightly decreased from $15.9 million at 2012 year-end, again due to contract delays. Several awards we anticipated for year-end that were pushed into the first quarter still remain open. We expect many of these opportunities will be booked in the next two quarters of 2013," said Mitchell Binder, president and CEO.

Manufacturing Vital to Nation's Military Readiness

"It has been clear for decades that our national defense needs do not begin and end at the walls of the Pentagon. The health of American manufacturing has always been vital to the health of the American economy. As this study shows, it also is vital to the health of our national defense," said USW International President Leo W. Gerard.

Kitron's Q1 Profitability Hurt by Weak Demand

The first quarter saw a negative trend in demand from several key customers. The recessionary trend in the European market is the main explanation for this development. In addition, the demand in the U.S. defence segment has been significantly lower than previously expected.


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THE SHORT SCOOP

Squeegee Blades

by Rachel Miller-Short
PHOTO STENCIL LLC

One often overlooked component of the soldering process is the squeegee blade, which is critical in solder paste application. The technology of the seemingly simple squeegee blade is as important as the stencil when it comes to the printing process. The application, type of stencil, and the printer set-up should all be determining factors in selecting the blade. Squeegee blades should:

- Provide consistent blade edge integrity over the blade life cycle
- Prevent curtaining of solder paste
- Achieve high print speeds with tacky solder pastes

Look for the life of the blade, the material it's made of, the edge surface, the surface finish, and a blade design optimized to your stencil. You can have an excellent printer, stencil, and the correct solder paste, but if you have a blade that's worn, or not optimally fabricated, it will have a significant effect on the end-of-line yield. The loss of profit involved in the downtime to diagnose and remedy the problem, plus rework, wasted solder paste, and low yield, can be considerable.

Providing consistent blade edge integrity is critical for achieving a consistent paste deposit across the entire board. A more precise and consistent blade requires less print pressure and

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SQUEEGEE BLADES *continues*

helps to substantially lengthen the working life of the squeegee blade. Maintaining the original engineered blade edge is essential in obtaining perfect solder brick deposition.

Solder paste sticks readily to most bare metal and even some after-market coated blades. This paste stick is called "curtaining." A solder-fouled print edge prevents a clean print stroke, leaving streaks or a film of solder paste behind and resulting in material waste as well as potential defects on the finished product. Excess solder stuck to the blade decreases productivity because it requires additional downtime to clean residual paste. When choosing a squeegee, always choose blades that have a dense, smooth coating that will resist solder paste adhesion. Eliminating curtaining ensures clean and consistent print results and a low maintenance, repeatable, and consistent printing process.

The specifics of the engineered blade design not only play a vital role in the quality of paste application, but are also critical to the speed of paste deposition. One OEM we encountered was experiencing difficulty printing a high tack formula solder paste at production rates. The high tack characteristics of the paste formula, combined with the long, and extremely flexible OEM metal squeegee blades, were limiting the maximum print speed to 2.5 inches per second (IPS). Switching to aftermarket nickel Teflon-coated squeegees allowed them to raise the print speed capability to 3.25 IPS, but was still short of their 6 IPS process goal. We investigated a range of squeegee blades to find one that could achieve the results they desired. Five different metal squeegee blades, each different in composition, thicknesses, and attributes, were tested for speed-printing effectiveness. Test results conclusively showed that the titanium nitride coated nickel blades alone were able to achieve a 6 IPS print speed at a 60° print angle. The closest rival could only achieve 54% of the titanium nitride coated blade print speed at 3.25 IPS.

There are numerous blade types available for paste printing; they are typically engineered for differing applications, married with stencil styles, and interface to specific manufacturers' machines. Blades that are manufactured in an electroform process are typically matched with electroformed stencils, but they can be used with multiple stencil types. These blades have the distinct advantage of allowing precise paste application at substantially decreased blade pressure. Electroformed blades are designed to provide improved print deposition and uniformity of paste volume over the entire printed image. Often called E-blades, they offer a rigid, low-friction nickel edge for cleaner prints, reduced stencil wear, and less material waste. This squeegee blade is grown by depositing ma-

Figure 1: Duraglide blade edge.

Figure 2: Competitor blade edge.

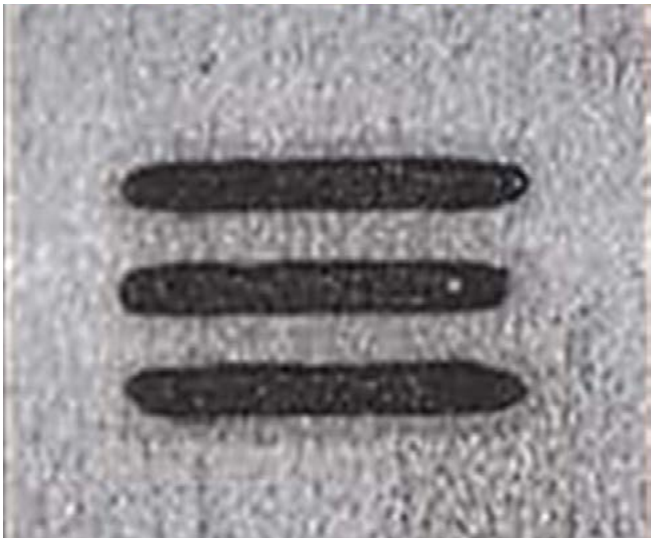

Figure 3a: Duraglider results (before).

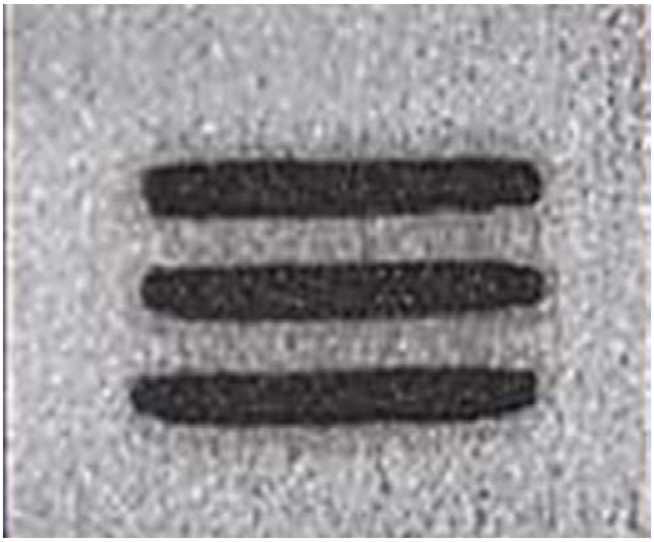

Figure 3b: Duraglider results (after).

terial on a mandrel with a mirror finish. First, the nickel deposition area is defined by a photoresist; then it is grown to a thickness of 11 mils. The squeegee blades are removed from the tank, the resist stripped, and the blades removed from the temporary mandrel. This unique fabrication process yields three extremely beneficial features:

- A very smooth blade edge void of any irregularities because the blade is built up chemically, one molecule at a time
- An extremely straight blade edge because it is formed with a photo-lithographic process
- An extremely sharp blade edge deposited at the surface of the mandrel

For high-speed production and long life, metal squeegee blades can be coated with an extremely dense, smooth, hard surface titanium nitride (TiN) finish to preserve the engineered edge throughout the life of the blade. Due to the hardness of the TiN coating, this blade type

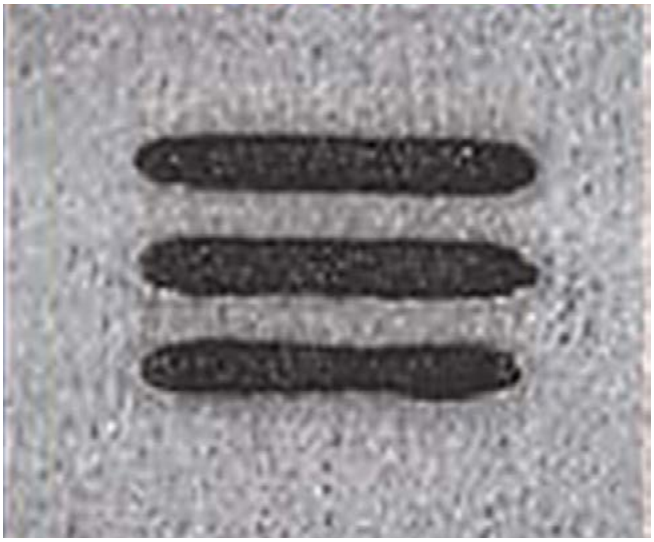

Figure 4a: Competitor results (before).

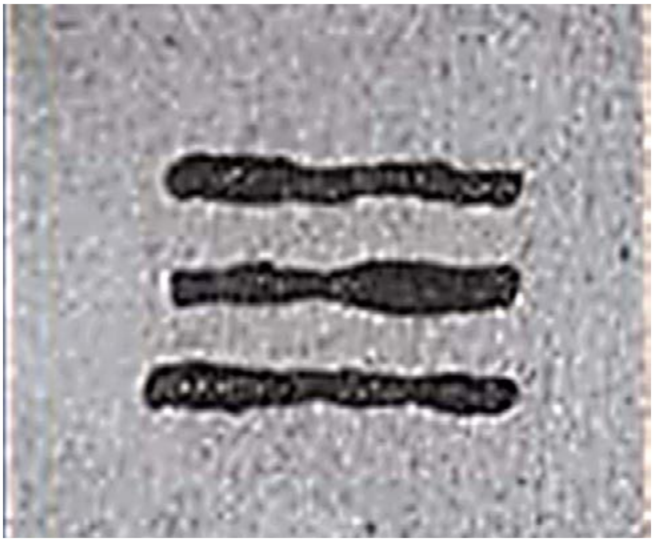

Figure 4b: Competitor results (after).

SQUEEGEE BLADES *continues*

is not well suited for use with stencils fabricated from softer nickel materials, like electroformed stencils. An independent testing agency performed accelerated blade wear tests comparing a blade coated with titanium nitride to Teflon-coated nickel blades. The titanium nitride coated blade showed no signs of wear after performing 6000 prints using twice the recommended squeegee pressure. In contrast, the uncoated nickel blades showed significant wear grooves as can be seen in Figures 1 and 2. Take a look at the solder brick deposits in Figures 3 and 4. A squeegee blade that retains its sharp original edge over its life cycle provides predictable and consistent, high-quality solder paste printing as seen in Figure 3, avoiding the level of inferior solder brick deposits shown in Figure 4.

Specialty squeegee blades are also available consisting of slit and notched blades. Slit squeegee blades are used for step stencils that have a large step-up. The slit is custom designed to match where the step-up is on the stencil. Normally, slits are placed close to the sides of the step-up allowing a portion of the blade to rise up on the step while the remainder of the blade stays in contact with the lower sections of the stencil. The slit is small, in the order of 1 mil (.001").

Notched E-blades are typically used in the case of electroform stencils that have been manufactured with raised relief pockets that form a three-dimensional step on the squeegee side of the stencil. An example is two boards that were connected with a flexible connector that rises 90 mils above the board surface. One board manufacturer's challenge was to be able to print solder paste on the SMT pads with the flexible connector obstructing a normal stencil from making contact with the board. The solution to the problem was a 3D electroform stencil. The final stencil was 5 mils thick, but had a 95 mil high-relief pocket formed in the stencil. The accompanying squeegee blade was a typical notched E-blade having the notch formed in the blade for clearance of the relief pocket. **SMT**

Rachel Miller-Short is vice president of sales and marketing at Photo Stencil LLC. Contact Miller-Short by clicking here, or reach her by phone at 719-304-4224.

Scientists Uncover Limitations of Organic Photovoltaics

Drivers who have ever noticed a residue on their windshields after going through a car wash will sympathize with nanoscientist Seth Darling's pain.

Darling and his colleagues at the U.S. Department of Energy's Argonne National Laboratory have worked for years to develop a new type of solar cell known as organic photovoltaics (OPVs). Because of their potential to reduce costs for both fabrication and materials, OPVs could be much cheaper to manufacture than conventional solar cells and have a smaller environmental impact as well.

The major drawback of OPVs, however, is they aren't as efficient as conventional solar cells. In a new study, Darling and his colleagues at Argonne's Center for Nanoscale Materials and Advanced Photon Source (APS) were able to detect for the first time a major contributing factor to this limitation: Trace residues of catalyst material left over from the development process prevent the OPVs from converting the maximum amount of sunlight to electricity.

"Scientists have recently become aware that impurities can cause problems in these nanostructured materials, but until now, we didn't have a way of actually being able to see that the impurities were even there," Darling said.

SMTonline Supplier/New Product News Highlights

Essemtec Debuts FLEXUS Pick-and-Place Platform

The FLEXUS pick-and-place machine builds on the proven concepts of the FLX and expands potential due to a new, modern H-drive that minimizes maintenance and increases the working surface. The footprint of the machine is only 25 cm larger than the FLX, but offers twice the placement space and a 30% higher feeder capacity.

Speedline's Momentum Compact Debuts in Nuremberg

The MPM Momentum® Compact high-performance printer, equipped with the new Enclosed-Flow™ Print Head and the Camalot® Prodigy™ dispense system, were exhibited for the first time in Europe, and were well received, according to Bruce Seaton, European sales manager.

Photo Stencil Unveils New Squeegee Blade Selection Guide

Photo Stencil, LLC, a leading full-service provider of high-performance stencils and tooling, introduces its new Interactive Squeegee Blade Selection Guide. Available at www.photostencil.com, the Guide provides characteristics to look for when choosing a squeegee blade, the types of blades available, and information about which blade to use for a particular application and printer make and model.

P. Kay Metal Releases New Dross System

The use of the DOFFS system in conjunction with MS2 will allow any company that generates solder dross to reclaim dross offline from the solder wave machine and, in doing so, reduce the need to purchase new solder by up to 85%.

Manncorp Debuts MC-LEDV4 for LED Assembly

Manncorp's MC-LEDV4 series of LED pick-and-place machines are specially designed to place surface-mounted LED components using four pick-and-place heads and "on-the-fly" vision for fast, accurate alignment.

Chemtronics Unveils New Water-Based Conformal Coatings

Chemtronics® has announced two new water-based conformal coatings that provide superior protection for circuit boards, low odor, and lower VOC (volatile organic compounds) emissions.

Pickering Introduces Highest Density PXI Matrix Solutions

The company is expanding its range of 2A matrices with the highest density solutions available in PXI. The new solutions increase the density of electromechanical relay matrices by up to 75% compared to the company's previous products and more than twice the density of competitor's products.

New Indium 6.4 Water-Soluble Solder Paste Minimizes Voiding

Indium 6.4 Water-Soluble Solder Paste's flux chemistry minimizes voiding under QFN and BGA assemblies. A typical water-soluble solder paste has approximately 15 to 30% voiding; however, Indium 6.4 consistently yields less than 5%.

Intertronics Introduces Polytec EC 275 Adhesive

Polytec EC 275 can be used for IC packaging, connecting circuits to copper coils (RFIDs or smart cards), and EMI/RF shielding. The paste-like adhesive can be easily applied with various dispensing techniques or screen printing and is available either as two components or premixed and frozen in syringes.

GOEPEL's New topoVIEW Allows Evaluation of X-ray Images

As an essential component of its new X-ray inspection software XI-Pilot V 3.1, the company introduces a new module for an easier evaluation of X-ray images. topoVIEW facilitates the interpretation of recorded X-ray images with respect to a better fault assessment and classification.


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• Meets IPC J-STD001, TM650 2.3.25
• Fast test times
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QUIT
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WARNING
SAFETY INSTRUCTIONS

Manufacturing Software: Make or Buy?

by Michael Ford
MENTOR GRAPHICS CORP.

From a business perspective, a significant software purchase for the production area can be a difficult decision. Software is the catalyst that makes things happen in many areas of our lives today, yet there is still a difficulty in the perception of the value of a software package for manufacturing. Top-heavy systems such as the traditional MES or ERP suffer from the perception that only a fraction of the functionality will ever be used, so why pay for all of it? Attempts by some lower level solution providers within SMT production have been less than successful, leaving a bitter taste for some.

With more software development tools available today and the availability of keen young engineers, how hard can it be to develop a solution dedicated to the specific needs and pain points of the operation? Is there really justification in the prices asked for commercial software? It is not a decision to take lightly, with profitability and competitiveness of the business at stake, as well as the reputation for quality. The make or buy question must be clearly understood before a decision is made, but what are the key elements?

Software Advantages

Software solutions can provide key advantages in many areas of production. Speeding up new product introduction, preventing incorrect material setups, providing conformance and compliance, the traceability build record for high value and safety critical products, management of materials logistics, quality management and reporting are some of the areas where software solutions can make a huge difference to the cost, quality and delivery performance. Spending millions of dollars on machines for new manufacturing lines is considered "normal," so why is there a reluctance to budget similar amounts on software, when software can make a comparable, if not a much greater, contribution to the bottom line of the operation? Software does not have the tangibility of hardware; it is just some files that can be easily copied, with only licensing to regulate the usage. The physical deliverable is the same whether it is for a single user or a multi-national operation.

The factory shop-floor is in the middle of strong, seemingly conflicting, requirements.

The supply chain, as represented by MRP systems since the 1970s, links the sales forecast, the production plan, material ordering and business systems. Run mainly by the purchasing, accounting and IT departments, these systems run "9 to 5," which significantly influences warehouse operations.

A natural barrier came into existence as materials were handed off from the warehouse to production, which ran up to 24 hours per day. This presented persistent architectural difficulties for supply chain systems to effectively break into the shop-floor. Quality systems were, for many, where software made the first impact on the shop-floor, recording defects from test, repair, and often incoming materials inspection.

Island Solutions

Engineering started to use software significantly for SMT machine programming, as the optimization required could no longer be done manually. Product-design-data-orientated systems also made a significant contribution as complexities of design and bills of materials grew, with production engineering introducing new products in an ever-decreasing cycle-time. Together, these examples and others form a series of software "islands," each consisting of software applications created or purchased for specific needs.

Most island "point solutions" created a lot of work, with significant overlap of data management and duplication of effort, resulting in a high cost of operation. Integration of these islands, based around a common data infrastructure, reduces this cost, but introduces technical and organizational challenges to satisfy different user requirements in data fields, format, level of detail, timing and work-flow. As requirements inevitably change, or as the scope of the system increases—possibly even with additional sites now wanting to use the same tool—the complexity increases almost exponentially, making the in-house solution start to look as complex as commercial packages.

Virtually every manufacturing operation today has established software islands that represent the internal know-how about the operation and flow. The scope of island solutions is narrow, created in direct response to a specific production pain point at a specific time. Internally-developed islands tend to depend on one or two key individuals from the engineering team itself, often without support from the IT team, and so have little support beyond day-to-day usage.

These islands tend to stagnate; the manufacturing and business processes around them stagnate also, as no one wants to touch the software in case it breaks. With an internal integration project comes IT, with a sustainable development team ready to assimilate the islands into a common project. For many developers in the IT team, understanding the operation, scope and focus of the islands is quite a steep learning curve.

The Make Option

Each island involves specialized knowledge of production. With few, if any, engineering systems creators remaining, it can be very difficult to provide equivalent functionality. This is the first barrier to the "make" option. The second barrier is scalability. The IT systems team, mindful of resources and time-scales, will create their system based on what they have learned, creating an effective, but usually inflexible, architecture focusing on the automation and integration of what is already there.

As business needs evolve, the system itself becomes the bottleneck and the resistance to change and innovation. The operation as a whole becomes constrained—a very serious issue when there is a need to adapt to new types of production, such as higher mix or to cover multiple sites at an enterprise level. Where these issues are understood, the "make" option is often outside the comfort zone of most IT operations.

The Buy Option

The more traditional approach by the IT team is to buy an ERP extension or a traditional MES solution. ERP has real difficulty to work effectively with an SMT shop-floor, since ERP needs accurate feedback of materials consumption and product completions. With complex products and operational flows, ERP input ultimately is manually triggered, a back-flush of materials from the final production stage—normally not accurate and often not timely—and not taking account of in-process losses. MES system providers have appeared in the market to fill this gap, providing a real-time, shop-floor management and control environment. In most industries, this synergy can work very effectively.

For PCBA production—especially SMT—this is not a trivial issue. Continuous manual input creates additional operational costs and introduces opportunities for mistakes. There can also be a high degree of customization required to support all of the assembly and test processes. Though most automated processes today have interfaces, these are complex relative to what ERP and traditional MES systems can handle.

Access to machine-process information is a critical technology barrier for any PCBA production system. It is frustrating, since software from the machine vendors is often bundled with a machine purchase. In addition to the wide variety of different data formats and access protocols, the information is very machine-centric. This creates the need for significant ingenuity to link and combine information sets together in context with the production flow and is quite a challenge with large volumes of real-time data and frequent unexpected changes happening in the machine interfaces.

Machine vendors often try to use this to their advantage, driving their own wider software solutions to effectively keep out competitors. This is mostly, however, an unrealistic option for customers; the solutions are not broad enough to provide full site functionality, and the constraint of single vendor selection is too restrictive. This basically eliminates them from serious consideration as a completely independent solution.

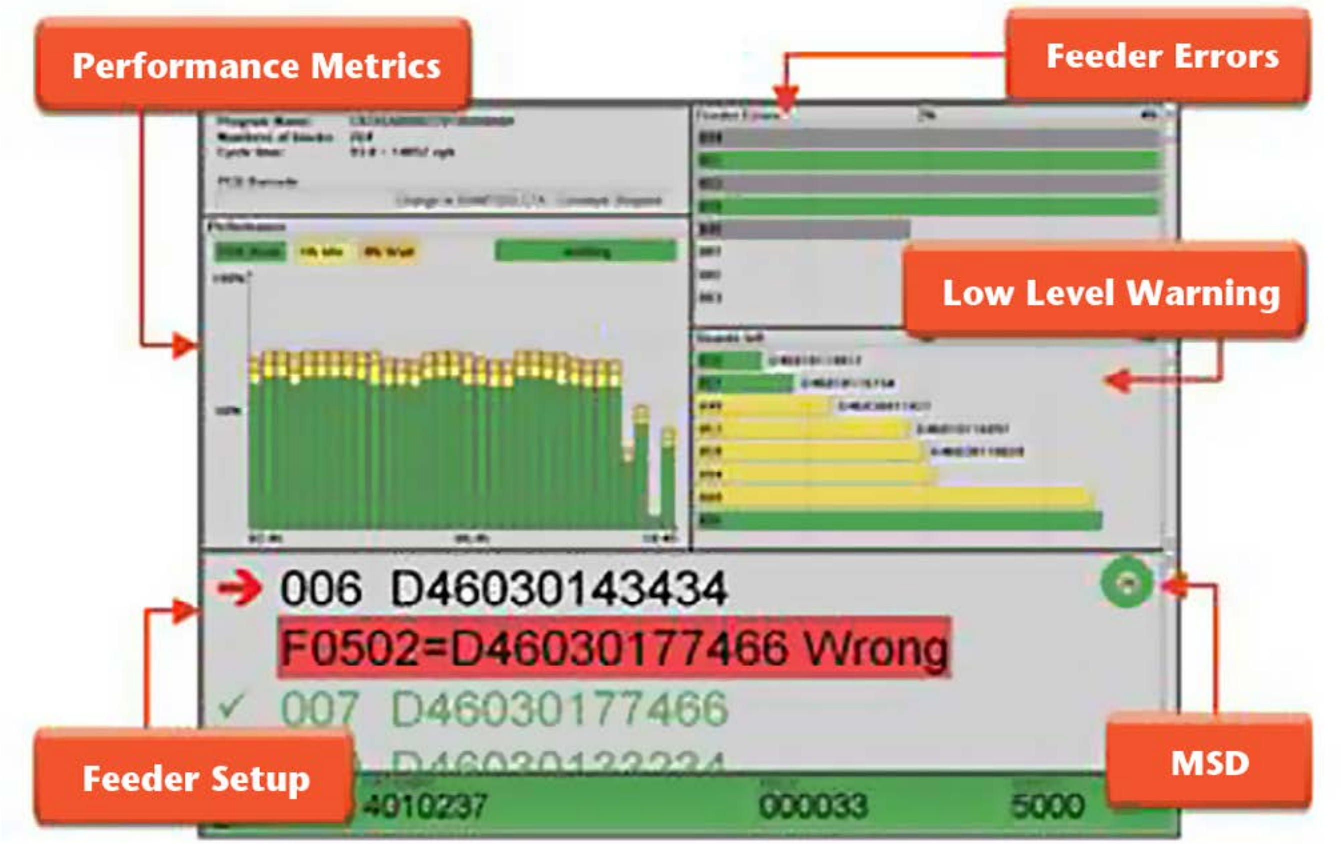

Figure 1: Third-party solutions provide a much more accurate picture into the current conditions on the manufacturing floor than do ERP systems.

Third-Party Solutions

An alternative to the ERP/MES solution is to buy a specialist third-party solution. These come from solution providers who have built their products and suites based on delivering functionality specifically to PCBA manufacturing. The strength of these systems is to provide operational and engineering value at each touch point of the system in the operation, with the subsequent information then used in the traditional MES sense. Since these systems are intrinsically linked to the operation itself, the challenge is to find a system that meets the detailed needs of the operation, both today and in the future. The systems themselves, in fact, should bring innovation to the operation itself, rather than to simply automate what is already there. The system also has to be closely linked to ERP materials and planning in order to understand and manage the operational flow, and also to design, where the base of the product engineering data will be sourced, governing the effectiveness of each of the operations.

To choose between these options, key criteria need to be established, as the priorities for each may be slightly different for each operation. The initial solution price is often high on the priority list following budgeting parameters. However, the true cost of ownership is by far the most important criteria, taking into account the initial costs, the running costs, and operational benefits. This is best viewed as a return on investment for the solution as a whole, with less than one year being challenging, but often a necessity for production.

Contrast this to ERP systems and hardware such as SMT machines that attract far higher budgets and longer term returns, often without question. Operational criteria must also be included, relating to the risks and constraints that the solution may impose on the operation, and how much innovation and flexibility would be provided. The technical architecture of the solution also needs to be considered, the ease of integration with ERP, the provision of enterprise-wide value, and with the minimum of bespoke customisation.

Cost Comparison

The biggest sticker shock for initial cost for the buy option comes most often from the ERP and traditional MES systems, which often include costs of extensive customization and consulting. Customization costs can often repeat as modifications are needed to meet changing requirements. Additional operational costs are

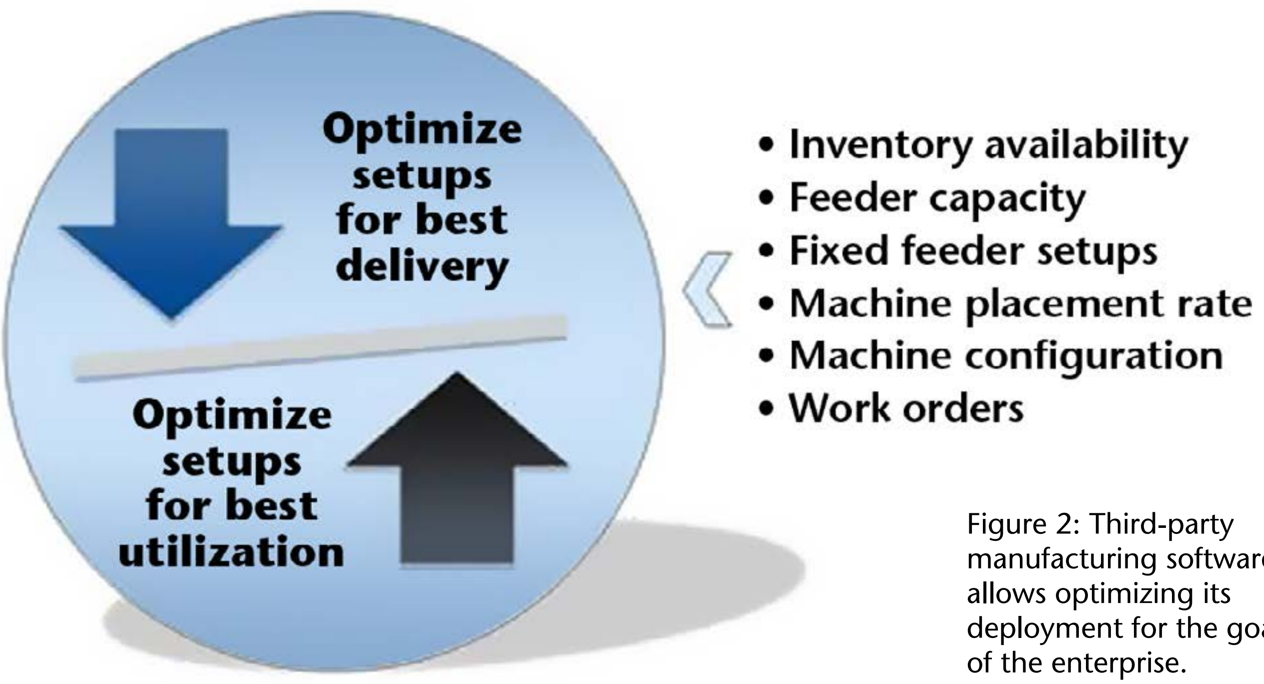

Figure 2: Third-party manufacturing software allows optimizing its deployment for the goals of the enterprise.

also high, with most inputs ultimately being manual, with little added operational value. The solutions are IT friendly and manageable and result in minimum risk compared to other types of solutions.

At the opposite extreme for initial cost is the make option. Initial costs may seem trivial, since it is mainly manpower. The values created from these home-made systems can be attractive, as specific pain points in the production process are targeted and resolved. On-going costs however can become significant as specialist developers are needed, as well as professional levels of support. Cost models often hide the true costs of the total manpower. The initial scope and requirement for the systems can easily become increasingly complex as business needs and requirements change, causing frequent reinventions of code base. The cost and effort to apply significant extensions can be more expensive than was the initial development. The quality of the system also needs to be considered, which can be poor when compared to commercial systems and can present real risks in the event that something goes wrong.

The PCBA specialist third-party solutions each offer a slightly different approach, depending on their strengths and history. The differentiator is to provide key specific operational values to each point of use on the shop-floor, including innovations to improve the operations.

Examples include the "just in time" management of material logistics between the warehouse and machines to drastically reduce excess material related costs, the optimization of work orders simultaneously with SMT material grouping between products for SMT line efficiency, and the reduction of time needed for new product introduction. Automated multi-vendor machine connections are also essential to provide timely, complete, accurate and meaningful data with which to operate, manage and control the production process. The best of these systems may also create pricing sticker shock, but the return on investment can be rapid as the system becomes an integral part of the overall execution strategy. The challenge with the selection of these systems is their depth and maturity in terms of the actual business benefits that can be expected.

The Bottom Line

It is not possible to choose one winner to satisfy every operation. However, the pattern emerging from market trends is interesting. By far, the majority of the top two tiers of OEM and CEM operations have moved towards specialist third-party solutions, having in many cases lived with islands of systems, and with some having taken the step to try to integrate them.

As predicted, however, the success of the make solutions were short-lived, and failed to live up to longer-term business needs. For the OEM, adopting specialist third-party solutions has meant a significant reduction of operating costs through the introduction of vertical innovation, shop-floor to business systems and manufacturing to design.

For the CEM, it represents increased competitive advantage in terms of speed, accuracy and quality. Other companies with less experience and more limited budgets are taking longer to consider the options, perhaps due to the sticker shock and lack of understanding of how a mature software solution can create such a significant return on investment. If the top tier companies are the ones to show the way forward, if they have found the better way with buy than make, will this scale to a different extent for other operations experiencing the same challenges and opportunities?

The answer may depend on pricing models and solution modularity, enabling independent solutions to be introduced that address specific pain points, within budgets; as the next solution for the next pain point is brought in, they combine to create the bigger picture solution. It is a way for every operation to enjoy the innovations and benefits that the top tiers have adopted. **SMT**

Michael Ford is senior marketing development manager with the Valor division of Mentor Graphics Corporation. To view Ford's previous columns, or contact the columnist, click here.

SMTonline Market News Highlights

Global Cloud Computing Market Revenues to Hit $35.6B in 2013

Visiongain's analysis indicates that the total value of the global cloud computing services market revenues reach $35.6 billion by the end of 2013, driven by increasing adoption of cloud services from the enterprise side.

LEDs: One Quarter of Global Lighting Market by 2016

The demand for all LED lighting products—including spot lights, LED luminaries, street lights, LED light bulbs, and fluorescent tubes will reach 90 million in 2016, increasing the global penetration for LED lighting applications to 26% in 2016, up from only 5% in 2012.

Global Semiconductor Sales in March Up 0.9% YoY

The Semiconductor Industry Association, representing U.S. leadership in semiconductor manufacturing and design, has announced that worldwide sales of semiconductors reached $23.48 billion for the month of March 2013, an increase of 1.1% from the previous month when sales were $23.23 billion.

U.S. Economy Benefits from Trade Relationship with China

China remained America's third-largest export market in 2012, behind only Canada and Mexico, as shown in the eighth annual U.S. State Exports to China report released by the US-China Business Council (USCBC).

Manufacturing Execs Predict Revenue Growth in 2013

Reflecting the sustained level of optimism, 78% of respondents forecast revenue growth at their own companies for the next 12 months, while only 5% expect negative results.

Intel Retains Dominant Position in Semiconductor Market

Intel, in the fourth quarter of 2012, retained its dominant position at the top of the global semiconductor industry with $11.98 billion in revenue, representing 15.4% of global chip market takings.

N.A. Semicon Equipment Book-to-Bill Ratio Up in March

North America-based manufacturers of semiconductor equipment posted $1.14 billion in orders worldwide in March 2013 (three-month average basis) and a book-to-bill ratio of 1.14, according to the March Book-to-Bill Report.

Notebook Shipment Slides 15.5% On-Quarter in Q1

In view of the quarterly result, the Q1 NB shipment attained 39 million units, dropping 15.5% from Q4 last year and declining 12.2% from the same period last year.

Tablet Sales to Reach $64 Billion in 2013

In 2013, approximately 150 million tablets (up 38% year-over-year) are forecasted to ship globally, worth an estimated $64 billion (up 28% from 2012) in potential end-user revenues, according to market intelligence firm ABI Research.

MAPI Report: China Manufacturing Growth Poised to Pickup

A Manufacturers Alliance for Productivity and Innovation (MAPI) report, China Manufacturing Outlook 2013-2014 (EO-122), notes that the fourth quarter advance was largely due to the stabilization in exports and the real estate sector, growth-supportive monetary policy, and public support for infrastructure investment.

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Embedded Assembly **Joseph Fjelstad, Verdant Electronics**
Green Electronics Materials & Processes **Tom Forsythe, Kyzen Corp.**
Prognostics & Health Management **Michael Pecht, CALCE**
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LED Packaging & Assembly
Lighting & Displays OLED Developments
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Failure is the First Step on the Road to Success—the Failure Analysis Process

by Derek Snider
INSIGHT ANALYTICAL LABS, INC.

It is an inexorable fact of life that all electronic assemblies – from the most complex, densely interconnected systems to the cheapest mass-produced consumer devices – will eventually fail. Such devices may be victims of various forms of abuse at the hands of their end users, subjected to mechanical, environmental, or electrical stresses far beyond what any design engineer would consider reasonable. Some, especially early prototypes, may be inherently flawed and susceptible to malfunction as a result of a simple mistake made during one too many late night, bleary-eyed design review sessions, conducted over energy drinks and cold takeout. Of course, it is also possible for assemblies to simply die of old age; eventually, normal wear and tear will break down even the most robust of electronic devices. In all these cases, the result is the same (at least at a very high level): a device that no longer performs its intended function.

As consumers, our natural instinct is to take these malfunctioning devices and pitch them into the trash – often with a little more force than is strictly necessary, and a trite utterance about how "they don't make them like they used to." Failure is regarded as a nuisance, an inconvenience, and nothing more. In some cases, this attitude is scarcely improved upon by OEMs or other suppliers; failing parts returning from the field are subjected to a quick bench test to verify the failure, and then relegated to the scrap heap. As manufacturers, suppliers, and designers, there is so much more that can be learned from these failures; we need only spend the time and effort to uncover the root of the problem. By diving into the minutiae of a given failure, it is often possible to discover imperfections and improprieties that can be invaluable, whether in proving that a subcontractor has not been manufacturing devices to the correct spec or revealing out-of-control processes that could spell trouble for the reliability of future lots.

The process of dissecting the remains of a failed device or assembly, slicing through the tangled web of interconnects and dielectrics to get to the kernel of truth lying at the root cause of the malfunction, is called failure analysis. By utilizing an extensive set of specialized tools and techniques, failure analysts can go from a very basic initial observation (e.g., "no output on J8 pin-4") to actionable data ("via misalignment between layer 1 and 3 on trace from U9 pin-6 to J8 pin-4"). Traversing the gap between these two points requires a meticulously detailed approach. In future columns, we will delve into the intricacies of this approach by reviewing individual case studies and techniques, to better show how failure analysis can be applied within an existing manufacturing environment to improve product reliability; in this column,

FAILURE IS THE FIRST STEP ON THE ROAD TO SUCCESS *continues*

we will provide a high level overview of what the failure analysis process looks like.

Due to the nature of failure analysis, no two projects will ever be quite the same. Failure modes, environmental conditions, device applications – all these parameters shape the circumstances of a given failure analysis project. Despite the fact that all failures are unique, there is still a generic process that can be applied to drive an investigation to its resolution. This process starts with the verification of the problem as reported – whether that report comes from a consumer, an entity further down the supply chain, or even from a test engineer directly after production, it is vital to verify that the issue can be recreated before attempting any further analysis. The verification phase of a project may be as simple as a five-minute check with a multimeter, proving that the correct voltage is not being output on a given pin or that continuity does not appear between two nodes that should be connected; in other cases, a more complicated approach may be necessary, such as when a failure is only present when a device is operated within a certain temperature range. Verifying the failure is not important only to prove that a problem exists; the verification phase also allows the failure analyst to determine the proper test conditions for later steps of the process.

Verification of the failure is the first of many steps in non-destructive testing (or NDT) of a device. As the name implies, non-destructive tests should have minimal impact on the sample under analysis; ideally, these tests should carry little to no risk of damaging the sample or potentially losing the defect. These tests will generally include a detailed visual inspection, looking for macro-scale defects like cracked solder joints or broken traces. X-ray inspection may reveal things that are buried within a circuit board or hidden underneath a component, like via misregistration or improperly wetted BGA balls. An acoustic microscope may reveal component-level failures, such as package delamination inside a component that was not properly stored before undergoing reflow. Generally speaking, non-destructive tests are not sufficient to prove the root cause of failure on their own; however, they provide key data that will shape the course of the failure analysis project.

Non-destructive testing overlaps to a certain degree with the next step in the process, wherein an analyst attempts to isolate the failure to as small of an area as possible. This phase of the project may include both destructive and non-destructive aspects as necessary to locate a defect site. Some problems may be fairly simple to isolate, given the correct tools; a low resistance short between nodes of a board may be revealed in a matter of seconds using a thermal imaging camera (Figure 1), and the aforementioned cracked solder joint found during visual inspection can usually be probed for continuity with very little trouble. Other defects may require patience, a steady hand, and a methodical plan of attack; finding a leakage site on a PCB, for example, may require an analyst to cut traces (both on the surface of the PCB and buried within) in order to limit the number of possible locations for a defect.

Once a potential defect site has been isolated, an analyst must be able to reveal the defect in all its glory. While the data gathered from isolation and non-destructive testing may be fairly strong, failure analysis follows the old clichés that "seeing is believing" and "a picture is worth a thousand words"; a failure analysis project is not truly finished until the analyst can produce images clearly showing a defect, removing any shadow of doubt that the anomaly found is at the heart of the reported problem. This step is almost always destructive; the analyst must, figuratively speaking, tear away the veil of FR-4 and copper shielding the defect from view in order to definitively show the defect. At the as-

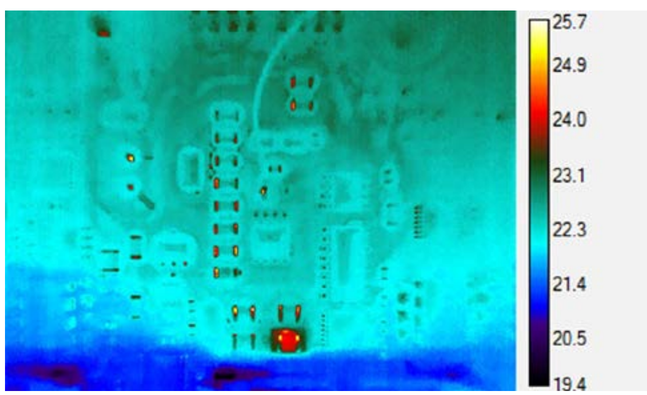

Figure 1: Thermal image showing a shorted ceramic capacitor.

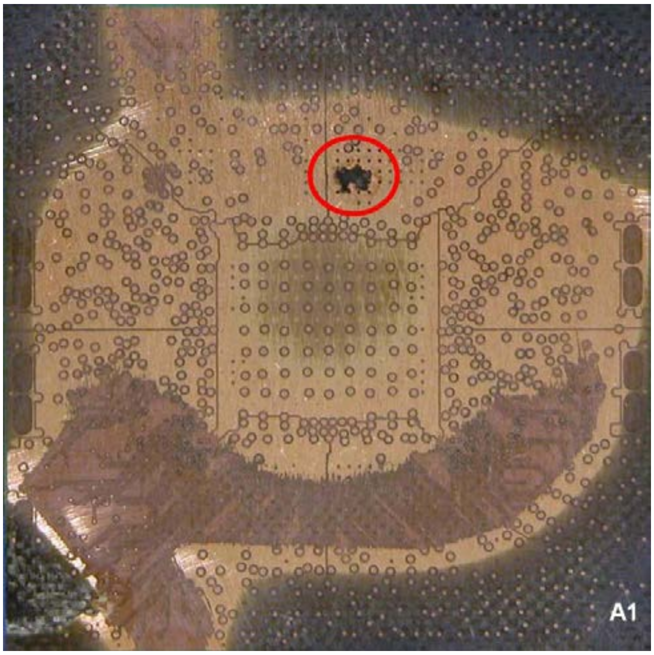

Figure 2: Photograph of a delayered BGA board showing dielectric material burnt by an electrical overstress event.

sembly level, this often includes cross-sectioning (to show cracked vias and solder joints or defects between PCB layers) or PCB delayering (to reveal damaged traces and voided or burnt dielectrics, as shown in Figure 2). Once the defect has been uncovered, an appropriate imaging solution can be chosen depending on the nature of the defect: High-resolution optical or electron microscopes are sufficient for physical damage and defects, while tools such as energy dispersive spectroscopy may be used to provide an "image" of contamination on a device that led to its early failure. With images in hand, an analyst's work is almost finished.

In the final phase of a failure analysis project, an analyst must report his findings. The tools and techniques used by a failure analyst may not be familiar to their audience, who may be specialists in PCB assembly, metallurgy, or other disciplines. In some cases, the final audience of the report may be predisposed to disbelieve the results of an analysis (for example, in the case where the evidence shows that a subcontractor's PCBs do not meet required specifications, obligating them to rerun one or more lots of product). The failure analysis report must therefore be a clear, objective distillation of all data obtained during the course of the analysis, with a strong conclusion grounded in the facts revealed during the process. Whether the results point to a pervasive problem that must be remedied in order to meet reliability targets, or are simply indicative of improper use by an end user, it is important to remember that the purpose of failure analysis is continuous improvement, not finger-pointing. Assigning blame does not offer a solution to a given problem; by understanding the nature of device failures, it is possible to implement corrective action (if necessary) to prevent recurrence of the same defect in future devices.

Conclusion

By following through the various steps of the failure analysis process – verification, NDT, isolation, revelation, and reporting – it is possible to take a device that would have been relegated to the trash can and transform it into a vital learning tool. It has been said that failure is the first step on the road to success; understanding the reason why a device has failed is a key starting point to creating a better device. Whether a defect was introduced during PCB manufacturing, solder reflow, or by an end user, all parties involved may learn from the anomaly and work to improve their own processes. While this article only provided a generic overview of the failure analysis flow, future articles will dive into further detail, exploring case studies that show the impact that failure analysis can have as well as exploring the techniques that go into a successful investigation. Until then, remember the motto of one of the most beloved groups of television scientists around – "Failure is always an option" – and keep an open mind about what that malfunctioning PCA might really be telling you! **SMT**

Derek Snider is a program manager and failure analysis engineer at Insight Analytical Labs, Inc., a company providing failure analysis services to aerospace, medical, and semiconductor manufacturing industries worldwide.

TOP TEN

News Highlights from SMTonline this Month

1 Sanmina Reports Q2 Revenue of $1.43 Billion

"Our second quarter results were in line with our expectations as we continued to manage through a soft market environment," stated Jure Sola, chairman and CEO. "We remain encouraged by new program ramps and increased forecasts from our customers that should drive improvement in the second half of the year."

2 EPIC Expands Assembly Operations; Opens New Facility

The company has relocated operations from a 56,000-square-foot facility in Lebanon, Ohio to a 74,000-square-foot facility in Mason, Ohio. The Ohio Valley Operations (OVO) facility is focused on low- to medium-volume, higher-mix electronics production. The added square footage will be used to expand the facility's higher-level assembly operations.

3 Flextronics Reports Fourth Quarter Revenue of $5.3 Million

"We generated $109 million in cash flow from operations this quarter and over $1.1 billion for the fiscal year," said Paul Read, company CFO. "Our strong cash flow generation allowed us to close the year with $70 million more cash after supporting strategic acquisitions of $184 million."

4 EMS M&A Activity Drops in Q1

There were seven completed transactions in Q1 2013. The seven transactions represent a drop in recent M&A activity compared to 11 transactions in the previous quarter.

5 Kimball EMS Reports Net Income of $3.7 Million

"We were very pleased with the performance in the EMS segment during the third quarter. Our key areas of focus in this segment are growth and further diversification of our customer base," says James C. Thyen, president and CEO.

6 Read Exits Flextronics; Collier Named New CFO

Flextronics announced that effective May 3, Paul Read, chief financial officer, has decided to leave the company to pursue new opportunities, but will remain available for any necessary transitional activities through the end of the current quarter.

7 Suntron Enters Semiconductor Equipment Industry

Suntron Corporation, a leader in integrated EMS, now offers a variety of manufacturing services, including large scale integration, for semiconductor capital equipment companies.

8 Celestica Romania Earns ISO 13485 Certification

"This is an important milestone for Celestica as we extend our medical device manufacturing and engineering services in Europe, strengthening Celestica's global supply chain network," said Kevin Walsh, vice president, Celestica HealthTech.

9 IMI Posts 8.5% Revenue Growth in Q1

"We managed to grow our business and remain profitable in the face of a persistent global economic crisis. Worldwide demand for electronic products remains challenged as the Eurozone, the U.S., Japan, and China tread uncertain economic waters. But at IMI we are experiencing improved performance, an indication of a healthy recovery," says Arthur Tan, IMI president and CEO.

10 Celestica Reports Decreased Q1 Revenue

"Celestica delivered first quarter revenue consistent with our expectations, while achieving profitability at the high end of the guidance range driven through solid execution and disciplined cost management," said Craig Muhlhauser, Celestica president and CEO.

EVENTS

For the IPC's Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar, click here.

For a complete listing of events, check out *SMT Magazine's* full events calendar here.

IMS 2013
June 2-7, 2013
Seattle, Washington, USA

SEMICON Russia 2013
June 5-6, 2013
Moscow, Russia

Innovations in Electronics Manufacturing for Medical Devices
June 12-13, 2013
Minneapolis, Minnesota, USA

Medical Devices Summit West
June 13-14, 2013
San Francisco, California, USA

Atlantic Design & Manufacturing Expo
June 18-20, 2013
Philadelphia, Pennsylvania, USA

NEPCON Thailand
June 20-23, 2013
Bangkok, Thailand

2013 CEA Market Research Summit
June 24, 2013
New York City, New York, USA

Counterfeit Electronic Parts Symposium East Tabletop Exhibition
June 25-26, 2013
College Park, Maryland, USA

2013 International Conference on Mechatronic Systems and Materials Application
June 26-27, 2013
Guangzhou, China

Upper Midwest Expo & Tech Forum
June 27, 2013
Bloomington, Minnesota, USA

Micromachine/ MEMS
July 3-5, 2013
Tokyo, Japan

Thermotec 2013
July 3-5, 2013
Tokyo, Japan

Ohio Valley Expo & Tech Forum
July 11, 2013
Cleveland, Ohio, USA

ISMSE 2013
July 27-29, 2013
Singapore

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SMT Magazine heats up in July with thermal management!

Don't miss feature articles next month from industry experts like Joe Fjelstad, Laird Technologies and more, who tackle a range of thermal management issues such as:

- Challenges during assembly
- Components and laminates
- Heat management techniques
- Thermal interface materials

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