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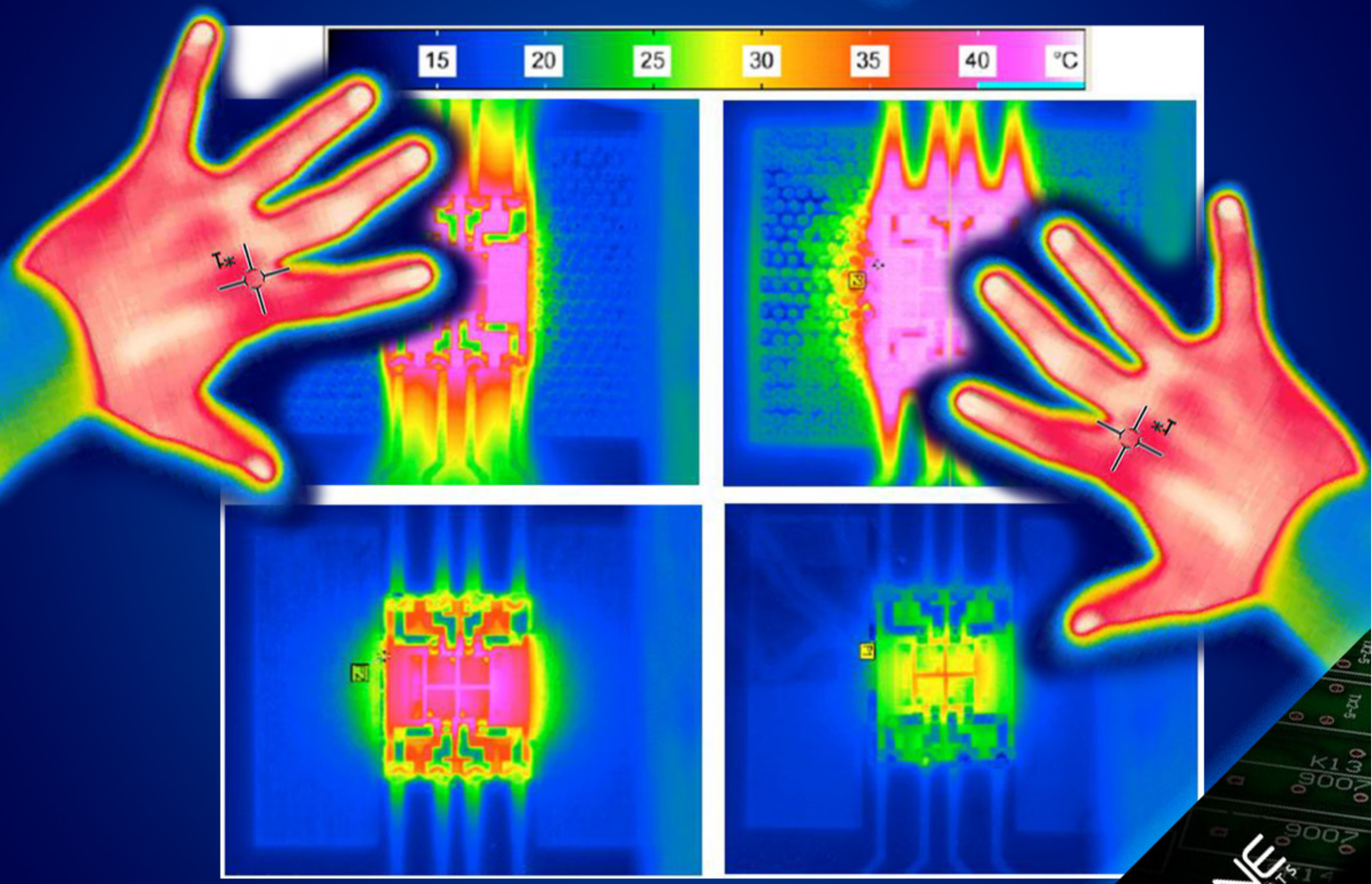
Thermal Management



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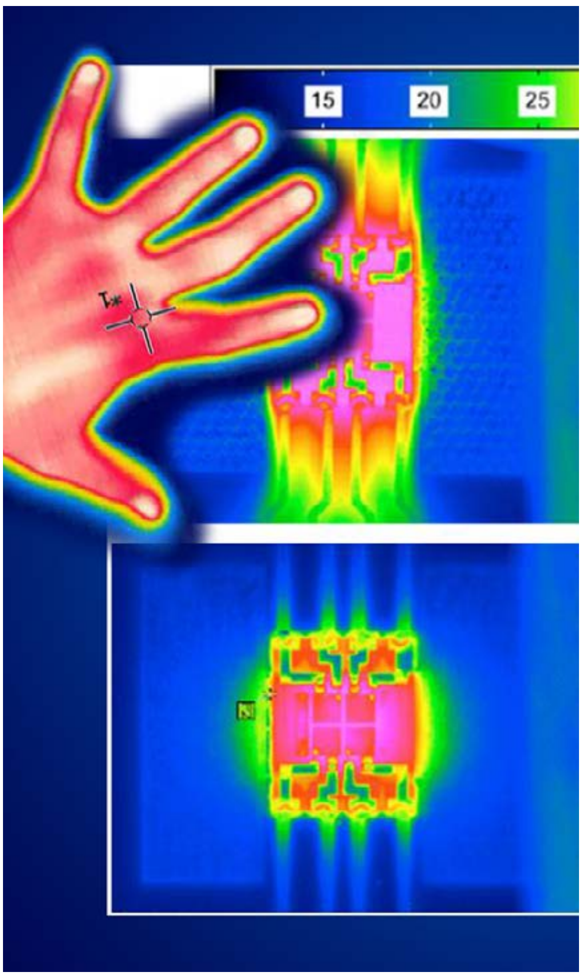
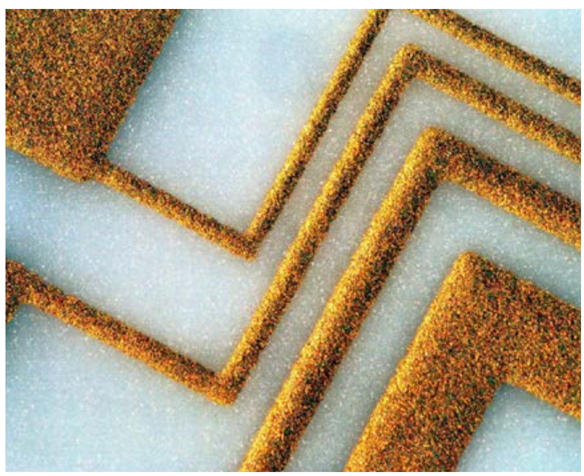
June 2014 Featured Content

THERMAL MANAGEMENT

It must be summer, because this month, *SMT Magazine* is turning up the heat on thermal management! Gregor Langer, Markus Leitgeb et al., look into advanced thermal management solutions for high-power applications. Carlos Montemayor investigates the high-temperature reliability limits for silicone adhesives, and Mark Challingsworth examines trends in thermal management for electronic circuits.





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COLUMN

THE WAY I SEE IT

We Saw This Coming

by Ray Rasmussen
PUBLISHER, I-CONNECT007

There have been quite a few predictions and studies, along with plenty of wishful thinking, about the cost of manufacturing in the U.S. The onshoring/re-shoring movement has gained a lot of attention from media like ours over the last couple of years. IPC even issued a report last year providing their take on the movement, which garnered a lot of interest from the industry.

Now, The Boston Consulting Group (BCG), a global management consultant, has released new research on the "dramatic" change of manufacturing cost competitiveness around the world. BCG's press release is entitled, "Study Reveals Striking Shifts in Global Manufacturing Costs over the Past Decade." I found the use of the word "striking" to be interesting. It almost leads me to believe they were surprised by the trends in manufacturing costs.

For those of us watching the shift over the last few years, it isn't striking at all. It's been coming for some time. As I've said in the past, all things come back into balance. The rising costs in Asia, and China in particular, have made it very clear that you can only sustain dirt-cheap manufacturing for so long. At some point, lax or non-existent labor and environmental standards, ridiculous lending policies, manipulated currencies, etc., will yield a day of reckoning. People get tired of breathing bad air and drinking polluted water. Trading partners say "enough is enough" and demand fair currency valuations. And banks struggle to survive under the weight of bad loans made during the heady days of unbridled growth.

With its success, China has opened the door to all kinds of ills associated with modern, democratic societies: regulations to improve the quality of the air and water along with some basic standards for worker safety and income. The government has had to loosen controls over the populace as well, to keep order and to sustain the illusion of a free society for most of their people. The Chinese people are getting smarter. They're starting to travel the world for business and pleasure. They want the freedoms associated with a modern, democratic society. This illusion has helped perpetuate growth by

WE SAW THIS COMING *continues*

placating their international trading partners and through the continued success of a growing middle class. Being part of the WTO has its advantages. I do believe the leadership in China wants to have a more open, democratic society, really. They're getting there. I don't want to condone their absolute, dictatorial control and lack of personal freedoms, but they have been able to pull off an economic miracle with the help of the West, which has lifted some of their people out of poverty. It ain't all bad, if you're one of those middle-class Chinese.

The release goes on to state that the UK is the low-cost producer in Western Europe, which isn't surprising. They've held a top spot for some time. They've had very friendly business policies since the Margaret Thatcher days. French government activist Olivier Cadic, the founder of PCB007, moved from Paris to the UK to take advantage of the lower costs, in part to strengthen the competitiveness of his businesses, but more likely, to send a message to the French government.

Mexico now has lower manufacturing costs than China. This news does a couple things for the U.S. First, it potentially brings manufacturing closer to home, to the same time zones and to a culture Americans are more familiar with. Second, it takes the pressure off of the border with Mexico. As more Mexicans find work in their own factories, there is less need to seek employment in "El Norte."

A Few Surprises

The cost of manufacturing in Brazil was a surprise and doesn't seem to make sense. They now call Brazil "one of the highest-cost countries." Another report from the World Economic Forum said this: "Brazil's manufacturing competitiveness is expected to strengthen over the next several years. Driven by ongoing investment in infrastructure in preparation for the 2014 World Cup and 2016 Olympic Games, relevant changes in the energy sector, and other recent policy reforms, Brazil appears to be favourably positioned for the future regarding manufacturing competitiveness." There seems to be a disconnect between these two organizations.

A pleasant surprise was that U.S. manufacturing is now on par with costs in Eastern Europe. Here's another quote from BCG: "Overall costs in the U.S., meanwhile, are 10–25% lower than those of the world's ten leading goods-exporting nations other than China." Energy: that's the ticket. We have the market; we have low-cost and very reliable sources of energy, a stable currency, great trading partners, a well-educated, hard-working labor force and a solid infrastructure to reliably produce and move goods to market.

BCG's study looks at four direct economic drivers of manufacturing competitiveness: wages, productivity growth, energy costs, and currency exchange rates. Harold L. Sirkin, a BCG senior partner and a co-author of the analysis said this:

"Many companies are making manufacturing investment decisions on the basis of a decades-old worldview that is sorely out of date. They still see North America and western Europe as high cost and Latin America, eastern Europe, and most of Asia—especially China—as low cost. In reality, there are now high- and low-cost countries in nearly every region of the world."

Based what we've seen as the economies of those low-cost producers improve, costs climb, as well. There are no more "Chinas" as far as I can see so we won't experience that phenomenon again, anytime soon. Those emerging low cost producers will take business from China, Mexico and elsewhere, in small bites here and there, serving mostly local and some international markets. I see the shift to automation removing most of the cost advantages associated with low-cost producers overseas in the not-too-distant future. With that, economies will continue to equalize as we move into the next decades.

That's the way I see it. **SMT**

Ray Rasmussen is the publisher and chief editor for I-Connect007 Publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuiTree Magazine.* To read past columns, or to contact Rasmussen, click here.

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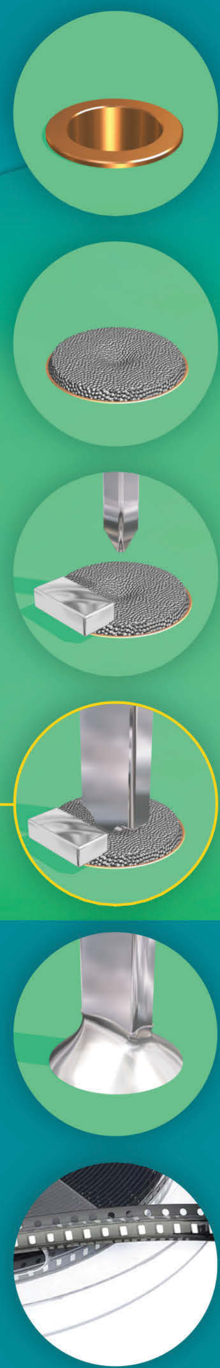

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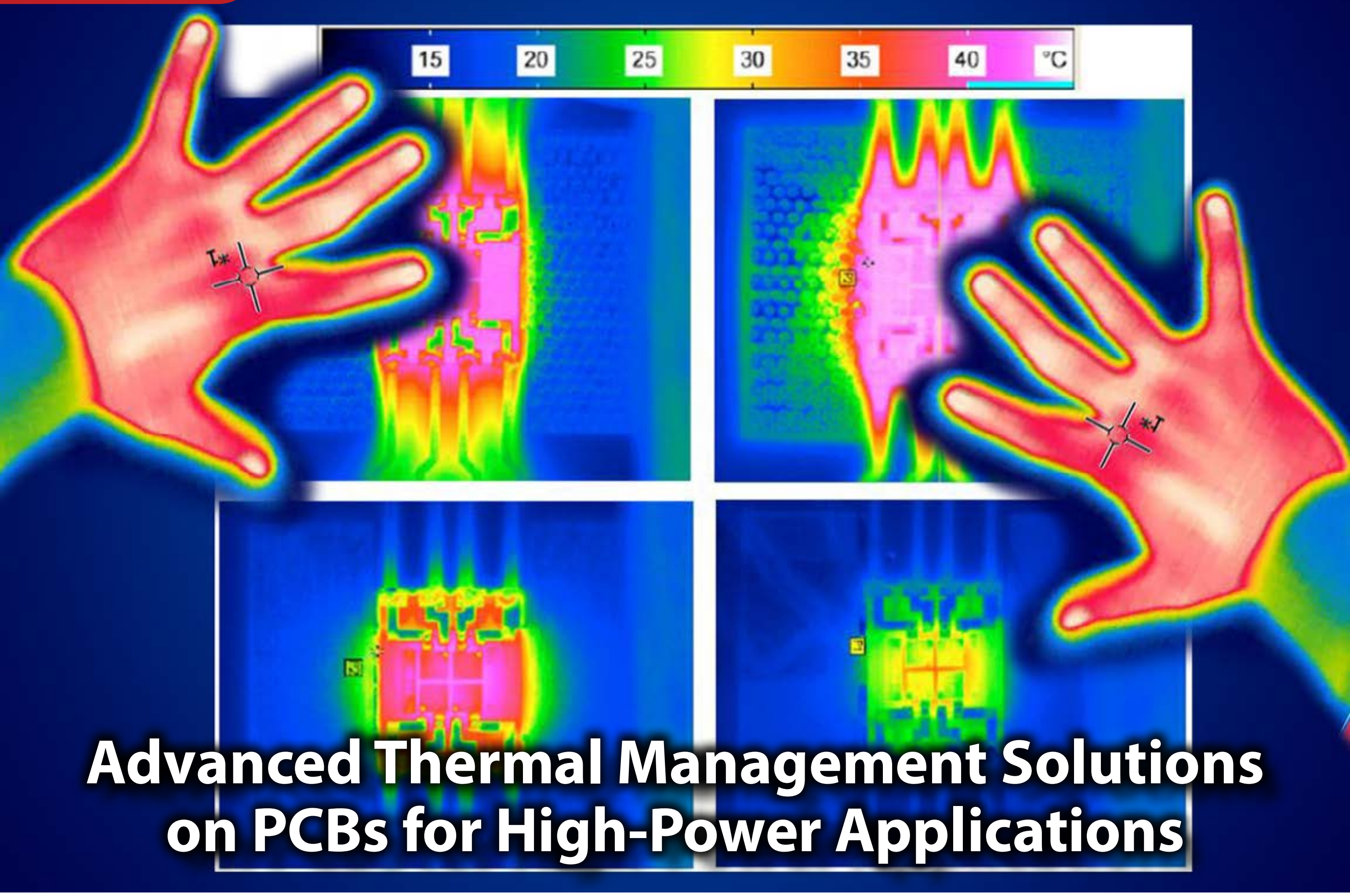

Advanced Thermal Management Solutions on PCBs for High-Power Applications

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Franz P. Wenzl, INSTITUTE FOR SURFACE TECHNOLOGIES AND PHOTONICS

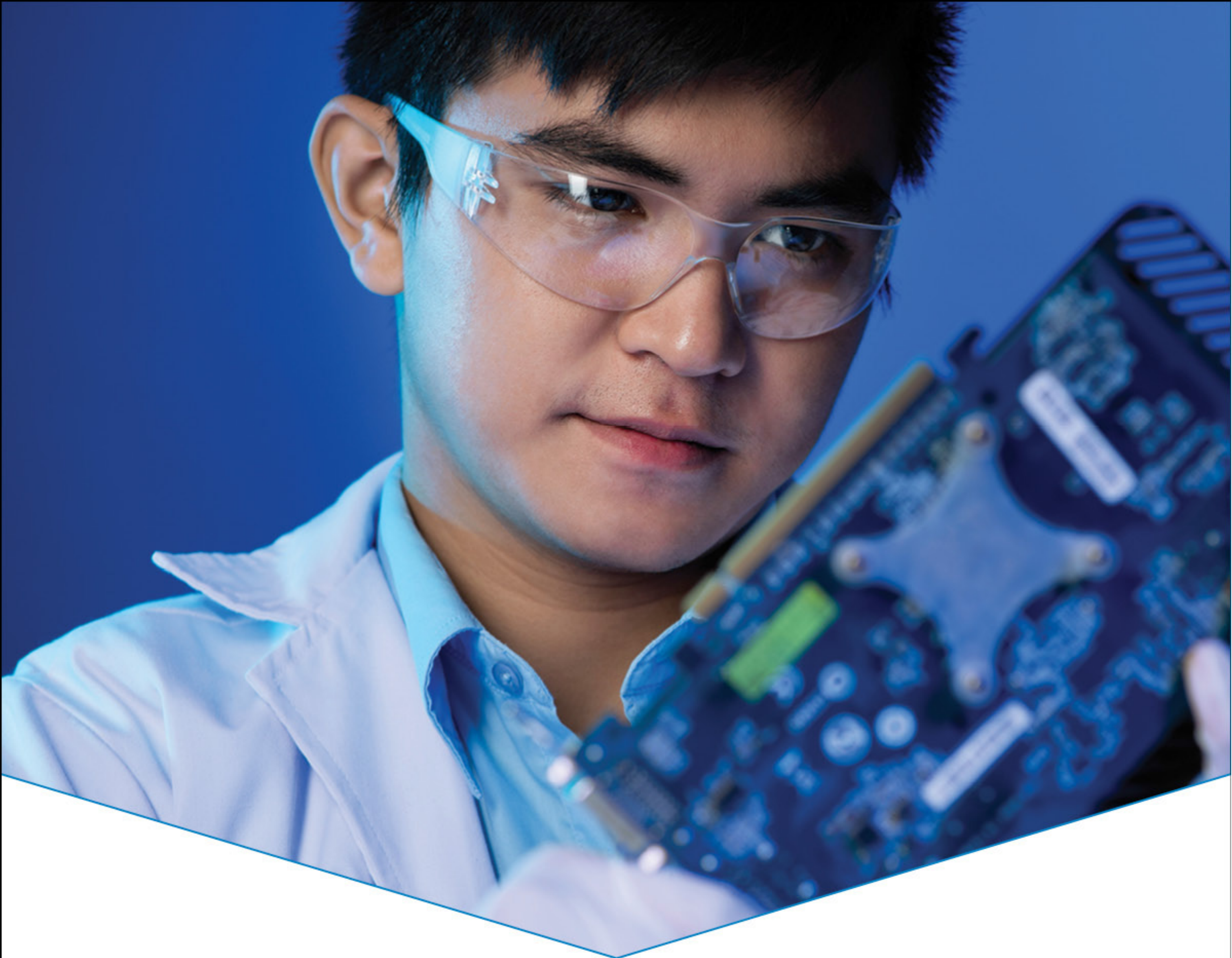
Abstract

With increasing power loss of electrical components, the thermal performance of an assembled device becomes one of the most important quality factors in electronic packaging. Due to the rapid advances in semiconductor technology, particularly in the realm of high-power components, the temperature dependence of long-term reliability is a critical parameter and has to be considered with the highest possible care during the design phase.

Two main drivers in the electronics industry are miniaturization and reliability. Whereas there is a continuous improvement concerning miniaturization of conductor tracks (lines/spaces have been reduced continuously over the past years), miniaturization of the circuit carrier itself, however, has mostly been limited to decreased layer counts and base material thicknesses. This can lead to significant component temperature and therewith to accelerated system degradation.

Enhancement of the system reliability is directly connected to an efficient thermal management on the PCB level. There are several approaches which can be used to address this issue: optimization of the board-design, use of base materials with advanced thermal performance and use of innovative buildup concepts.

The aim of this paper is to give a short overview about standard thermal solutions like thick copper, thermal vias, plugged vias or metal core-based PCBs. Furthermore, attention will be turned on the development of copper-filled



thermal vias in thin board constructions. In another approach advanced thermal management solutions will be presented on the board level, exploring different buildup concepts (e.g., cavities). Advantages of cavity solutions in the board will be shown, which not only decrease the thermal path leading from the high-power component through the board to the heat sink, but also have an impact concerning the mechanical miniaturization of the entire system (reduction of Z-axis). Such buildups serve as packaging solution and show an increase in mechanical and thermal reliability.

Moreover, thermal simulations will be conducted and presented in this paper in order to reduce production efforts and to offer optimized designs and board buildups.

Introduction

Modern power electronics is using power components such as MOSFETs, IGBTs, GTOs, high brightness LEDs and many more. Due to the enormously rapid advances in semiconductor technology, particularly in the realm of high-power applications, the trend is going to smaller components with even higher switching speeds and higher current densities. In general a strong miniaturization trend for whole modules can be seen.

With these trends and increasing power loss densities, the thermal performance of an assembly becomes one of the most important quality factors in electronic packaging. New materials and innovative approaches in PCB substrates are required to meet the required reliability levels.

Interest in power electronics has grown dramatically in the last few years, with an increasing need for electric power management and control (smart grid), renewable energy generation and control (wind power, photovoltaic, fuel cell, etc.), electric transportation, and the desire to improve operating efficiency of heavy systems (trains, industrial motors, electric vehicles, etc.).

Power electronic converters are found wherever there is a need to modify the voltage, current or frequency. These range in power from few milliwatts in mobile phones to hundreds of megawatts in HVDC (high-voltage, direct current) transmission systems (Figure 1). Usually we think of electronics in the framework of information, where speed is the primary interest. In the context of power electronics improved efficiency and lower power losses are important.

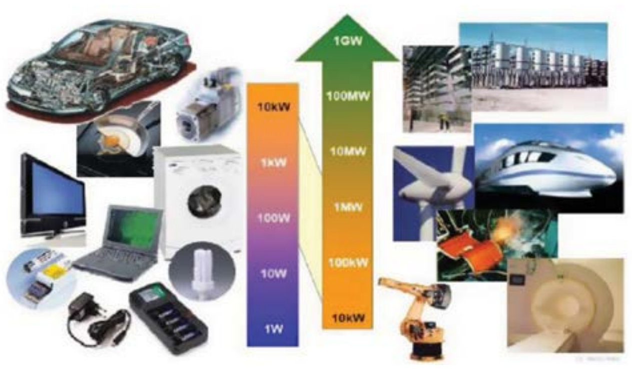


Figure 1: Range of power electronic applications. (Source: iNEMI Technology Roadmaps, Jan 2013)

Thermal Resistance

Definition of the Thermal Path and Thermal Resistance

For steady-state considerations most frequently used measures for the thermal performance of an electronic module are either the junction temperature TJ of the semiconductor device with the significant power loss or, even more common, the thermal resistance Rth. The latter has to be defined by the temperature difference J along a thermal path as e.g.

$$\vartheta = T_J - T_C \tag{1}$$

where TC denotes the temperature of the interface of the case of the module and a cooler, and the power loss (Ploss) causing the temperature difference

$$R_{th} = \frac{T_J - T_C}{P_{loss}} \tag{2}$$

Equation (2) is a useful practical approach to describe the thermal performance of a power assembly if TJ and TC are isotherms and the entire heat flow from TJ to TC equals Ploss. It should be noted that these conditions are not always fulfilled. In small silicon transistors and diodes the rather small temperature gradients within the junction can frequently be neglected. However, as can be seen by a more detailed thermal investigation of a GaAs high-power transistor, depending on the considered semiconductor device, there are tremendously high temperature differences within the junction itself [1]. Another frequently underestimated danger to misinterpret equation (2) arises if the case temperature is not enough uniform. Reaching a uniform case temperature over as large an area as possible is one major concern of thermal management on the PCB level.

A further approach to describe the thermal resistance Rth is shown in equation (3). It can be seen that the thermal resistance can be minimized by reducing the length d of the thermal path or by increasing the thermal conductivity λ of the material as well as by increasing the area of the contact pad A. As already stated in the introduction there is a trend in miniaturization of the power components, so there is no chance to increase the area. For this only the two first possibilities can be used to improve the thermal management of the system. That means the length of the thermal path through the PCB should be as short as possible, and the material between component and heat sink should have a thermal conductivity as high as possible.

$$R_{th} = \frac{l}{\lambda \cdot A} \qquad (3)$$

Motivation for Thermal Management

The main reason for deficiencies of electrical systems beside dust, vibration and humidity is by far the impact of temperature. Therefore an efficient thermal management concept on the PCB is crucial for the reliability of power electronic systems.

As an example we take high-power LED applications, which are likely to dominate in the next years residential and commercial lighting, signaling and vehicle headlights due to efficiency and extended lifetime. LEDs that range from 500 milliwatts to as much as 10 watts in a single package have become standard, and researchers expect even higher power in the future.

Thermal management is of critical importance for high-power LEDs. More than 60% of the electrical power input is converted into heat and built up at the junctions of LED chips due to non-radiative recombination of electron-hole pairs and low light extraction.

If that heat is not removed, the LEDs run at high temperature, which not only lowers their efficiency, but also makes the LED more dangerous, less reliable and shortens operating life [2,3]. Thus, thermal management of high-power LEDs is a crucial area of research and development.

In this paper results of simulations and measurements of different LED-modules will be shown and should serve as representative of thermal solutions for general high-power applications.

Standard PCB Technology for Thermal Management

Overview and Short Description

Effective heat removal can be based either on a short heat conduction path to a heat sink perpendicular through the PCB (e.g., thermal vias) or by a conductor layer acting as a lateral heat spreader (extended thermal pads) or a combination of both.

There are many different and well known build-ups for these heat removal concepts on PCBs. Thick copper approaches on PCBs guarantee a very good lateral heat spreading effect due to the excellent thermal conductivity of the copper and are very well used to reduce hot spots.

Insulated metallic substrates (IMS) are also state of the art and widely spread for thermal issues in electronic systems. An IMS consists of a metallic base material (mostly aluminum or copper) with a thickness of about 0.5 mm to 3.0 mm. On the metallic base material there is a thin dielectric layer (about 30 µm–150 µm) with a high thermal conductivity (0.5–8.0 W/

mK) in respect to standard FR-4 material (ca. 0.3 W/mK). The copper design layer is on top of the dielectric layer.

IMS show a very short heat conduction path through the thin dielectric layer, because the metallic base material serves already as first heat sink. There are several different IMS variations available depending on the requested performance.

Further build up concepts using a short heat conduction path to the heat sink are conventional through-hole plated glass fiber reinforced PCB technologies. A sufficient thermal performance in the lower power loss range up to several watts can frequently be achieved by reasonable numbers for via count, via diameter, and hole plating thickness [4]. Figure 2a shows a scheme of a PCB with open through holes serving as open thermal vias. In figure 2b an example of a footprint design is shown. It can be seen that the thermal vias are situated in the extended thermal pads beside the pad, where the component will be placed. So, to avoid the well-known problem of solder soaking, it is not possible to place open thermal vias directly underneath a component. Due to this fact, the thermal path is elongated, because the heat has to be spread first laterally on the surface before it can be guided perpendicular through the PCB to the heat sink shown in Figure 2c.

A schematic cross section as depicted in Figure 3a demonstrates a special via plating technology featuring plugged vias with a homogeneous copper layer on the front faces. In contrast to the concept with open vias, this build up allows vias directly beneath a component, which also reduces the thermal path. Figure 3b shows a microscopic view of a cross section of this type of PCB.

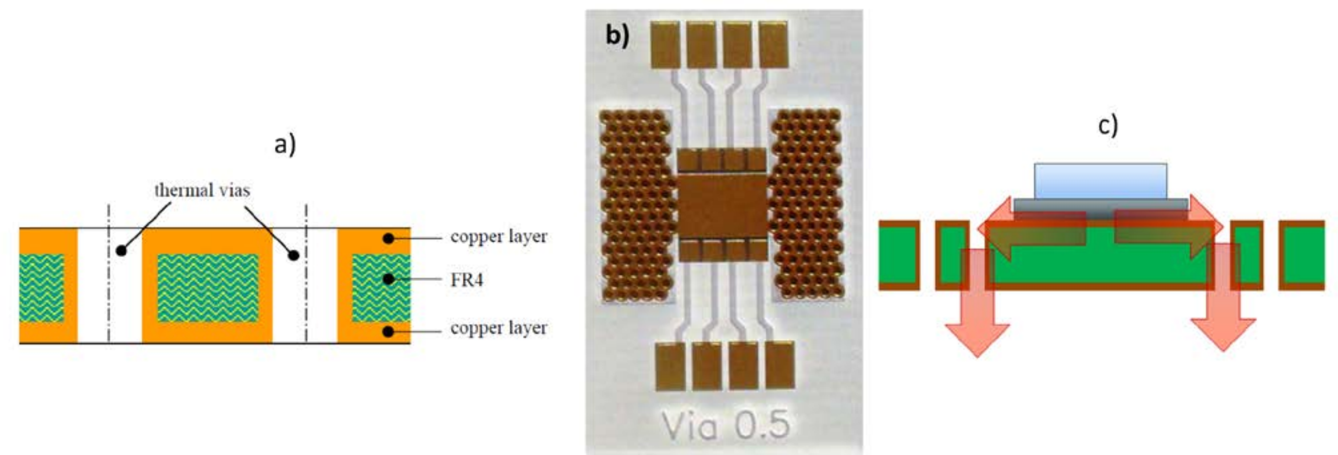


Figure 2: PCB with open thermal vias: a) scheme; b) design; c) thermal path.

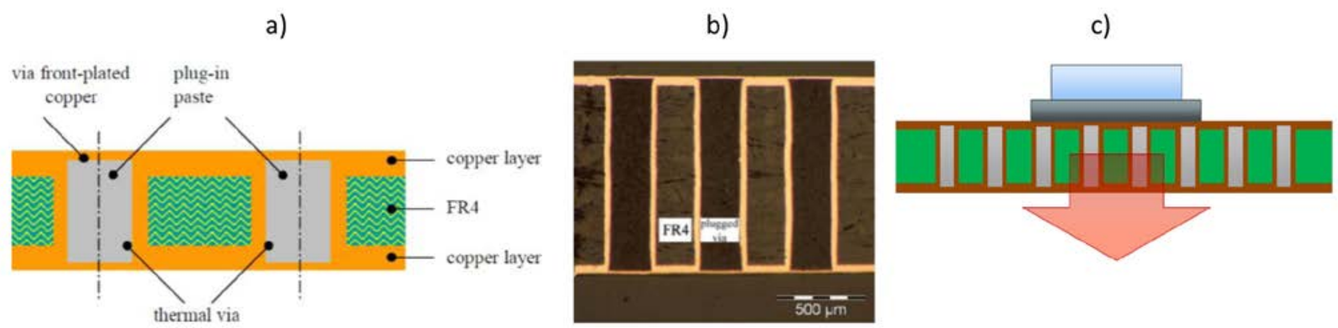


Figure 3: PCB with plugged thermal vias: a) scheme; b) cross section; c) thermal path.

Experimental Setup

Test objects were selected with following specifications:

- DK2, (FR-4, thickness = 1 mm, pads with plugged thermal vias)
- DK6, (FR-4, thickness = 0.2 mm, open thermal vias with 0.3 mm diameter, laminated onto 1.5 mm thick Al substrate with a 90 µm thick prepreg)
- IMS1, (70 µm thick copper clad, 110 µm thick dielectric, thermal conductivity = 0.5 W/(mK), Al substrate thickness = 1.5 mm)
- IMS3, (70 µm thick copper clad, 125 µm thick dielectric, thermal conductivity = 4 W/(mK), Al substrate thickness = .5 mm)

All PCB samples were prepared with a size of 30 mm x 40 mm. The layout allowed testing of two power LEDs at the same time (Figure 4a) whereby the comparatively large via arrays should help to maximize heat spreading.

Most important qualities of an experimental setup are to simulate boundary conditions as close as possible to the following extreme conditions:

a) The PCB itself acts as a heat sink by conducting the heat flux in the plane direction and dissipating (e.g., by natural convection and radiation)

b) The PCB acts as mean to interconnect the power component with a cooler and to help spreading the heat flux uniformly over the entire attachment surface of the cooler

In this section, we compare the thermal performance of FR-4-based PCBs with thermal via arrays (two different modifications: with open vias and with plugged vias) and IMS in an experimental setup according to condition b). For this purpose a water-cooled copper block was used as a heat sink with constant temperature. The samples were attached to the copper block using an equally distributed thin layer of thermal grace with a thermal conductivity of 0.6 W/(mK). The samples were pressed against the copper block with pointed plastic screws in order to keep the thermal resistance of this interface as stable as possible without heat removal from the top side (Figure 4b).

Temperature distributions of the top side of the samples during operation with the nominal forward current (If = 700 mA) were recorded using a high-end thermography system. An emissivity correction was made by a calibration measurement with a miniaturized thermocouple at the LED pad.

From evaluation of transient thermal response on power-on-steps with the nominal power value we see that the final temperature distribution on the entire sample surface is obtained within only a few seconds in all cases.

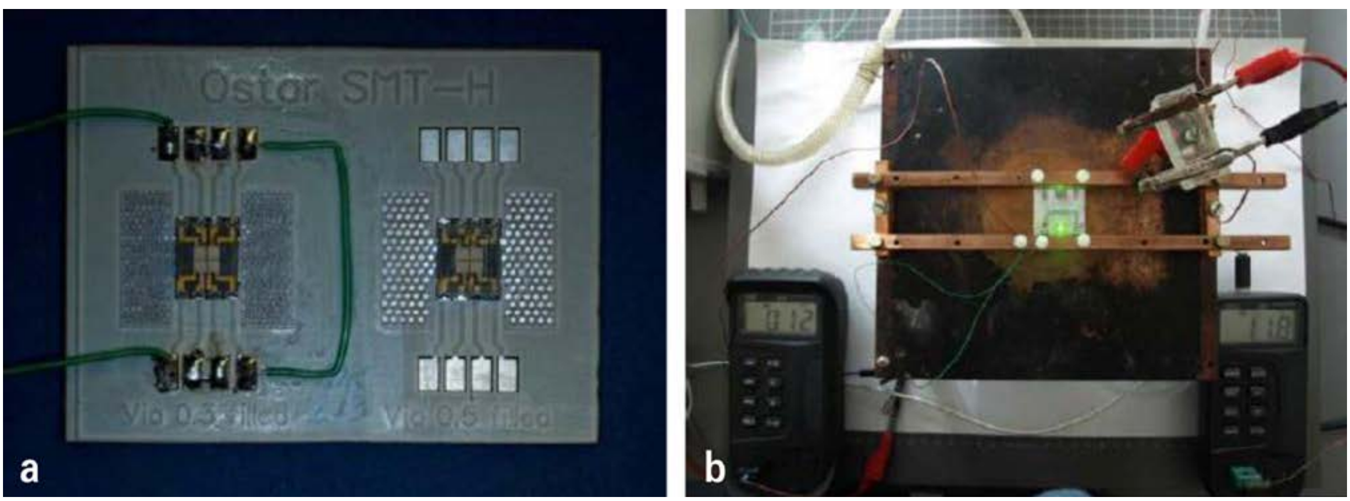


Figure 4: LED module mounted on water-cooled heat sink: a) top view of test sample; b) sample under test.

The temperature distributions obtained by IR thermography in the steady state are compared for all four sample types in Figure 4. During experiments with the nominal forward current a voltage drop of 4Uf = 13.5 V was measured (four single LED elements in one module, connected in series). Assuming an average photonic efficiency of h = 20% we considered a continuous power loss of 7.56 W per sample. Since establishing of the junction temperature was related to high uncertainties we defined the pad-to-cooler thermal resistance Rth,p-c as the relevant parameter characterizing the thermal performance of the PCBs in the following way:

$$R_{th,p-c} = \frac{T_{pad} - T_{cooler}}{4U_f \cdot I_f \cdot (1-\eta)} \quad (4)$$

where Tpad is the temperature of the copper pad in the vicinity of the LED submount body and Tcooler is the temperature of the copper block. Using the respective temperature values from the IR thermography images and the values mentioned above equation (4) the results as listed in Table 1 were obtained.

Thermal Measurements and Results

From the IR thermography picture of the DK6 sample a well-developed heat spreading effect can be recognized (Figure 5). The temperature gradients in the vicinity of the LED chip are the lowest ones compared to the other three types, thus the heat flux is conducted into the cooler through an enlarged area of the dielectric. This high heat spreading effect is due to the excellent thermal coupling of the two copper layers by the microvia arrays. However, because of the thick dielectric—a 90 µm thick prepreg with moderate thermal conductivity of only 0.3 W/(mK), the temperature distribution and therewith Rth,p-c reaches the highest values.

From view point of the copper layout the DK2 and DK6 samples are very similar (not that the thin copper layer at the "plugged" via front faces does not contribute much to the heat dissipation). Though the thickness of the

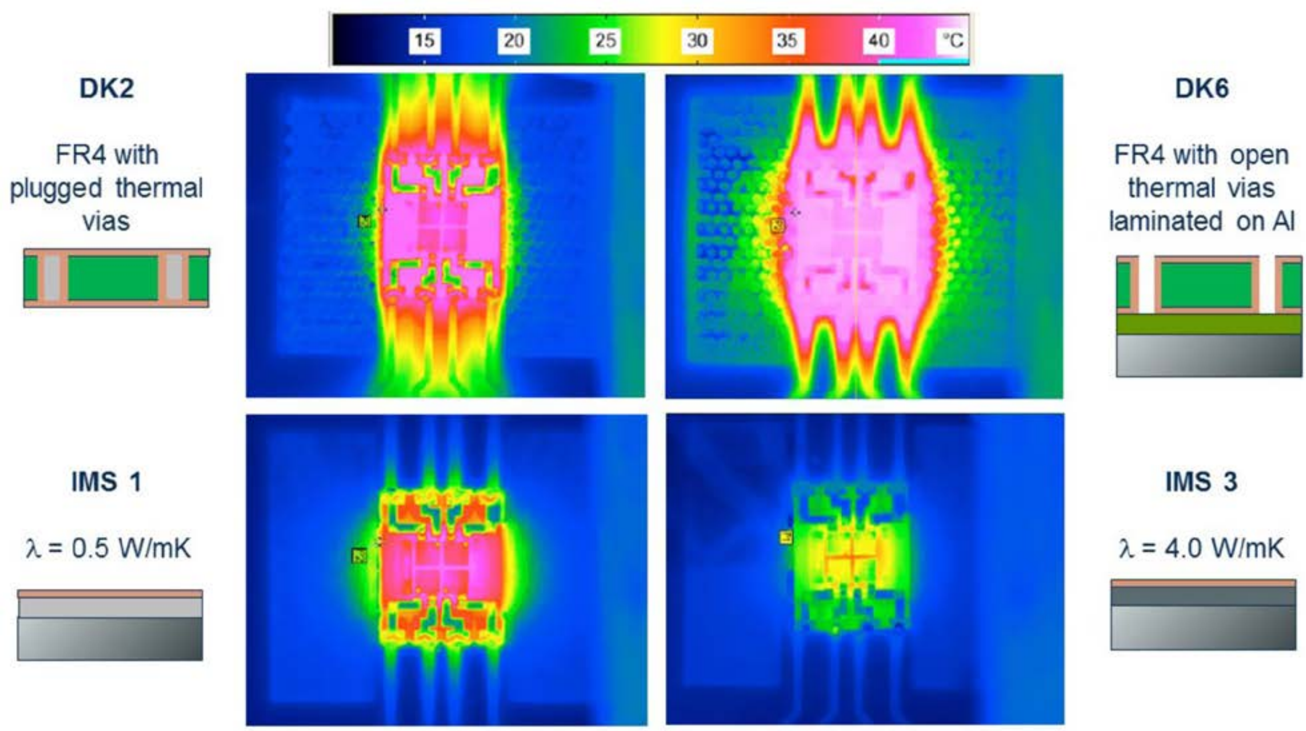


Figure 5: Comparison of results obtained from IR thermography measurements.

Sample type	$T_{pad,IR\text{-}cam}$	T_{pad}	T_{cooler}	I_F	P_{el}	$R_{th,p\text{-}c}$
	°C	°C	°C	mA	W	K/W
DK2	36.0	41.6	13	700	9.45	3.8
DK6	42.9	49.6	13	700	9.45	4.8
IMS1	28.2	32.6	13	700	9.45	2.6
IMS3	26.6	30.8	13	700	9.45	2.3

Table 1: IR-thermography measurement results and evaluated thermal resistance values.

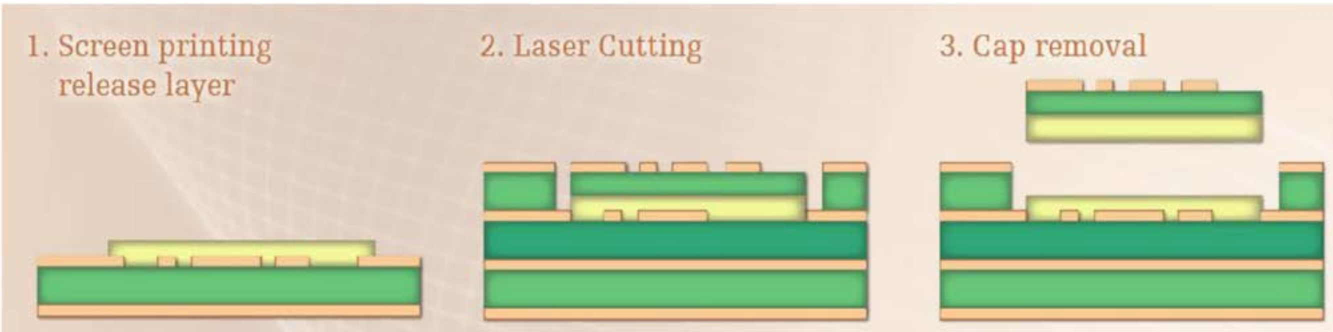


Figure 6: Schematic process flow of cavity formation.

FR-4 in the DK2 is five times higher than that in the DK6 the heat is conducted into the cooler at a remarkably lower temperature because the thermal vias are in intimate contact with the cooler. This also leads to a steeply declining temperature in lateral direction outside of the LED chip.

Significantly lower as on the first two PCB types are the temperature distributions on the two IMS type samples. In spite of a heat flux density of more than 50 W/cm^2 the maximum temperature of the LEDs are lower than 40°C in case of the IMS1 sample and even lower than 33°C in case of the IMS3 sample. This can be explained by the higher thermal conductivity of the dielectric (in IMS1: 0.5 W/(mK), in IMS3: 4 W/(mK)).

Advanced Thermal Management Solutions: Cavity Boards

Introduction

Another possibility to reduce the thermal resistance of the PCB is the use of cavities. Local depth reduction (through various methods and technologies) has long been applied to achieve a number of design and/or application linked results.

In this section the advantages of PCBs with special cavities regarding to advanced thermal management performance are presented.

Cavity Formation

The production method of PCBs with cavities presented in this paper is based on patented technology [5], which enables the removal of multiple layers at varying depths. The specific depth is achieved by the application of a paste on the release layer with subsequent relamination of the entire board. A laser cutting process then trims and cuts at the predetermined shape to separate the relaminated layers from the release layer. The final steps are "cap removal" and paste stripping (Figure 6). What remains is the solder footprint pattern. Diverse surface finishes and also application of solder mask can be employed in the cavities.

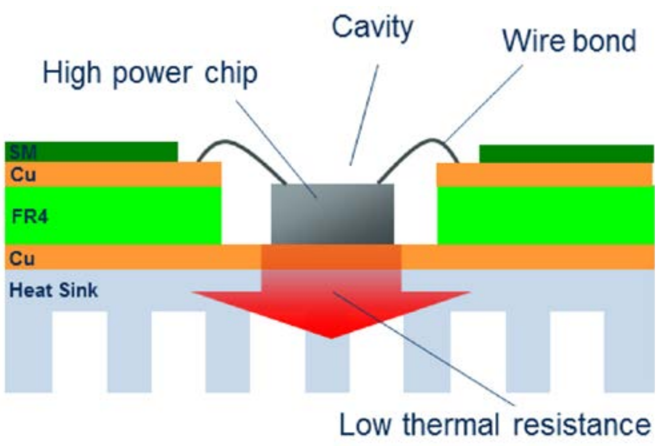


Figure 7: Chip in cavity build-up with optimized thermal path.

In order to achieve an optimal thermal performance the cavity formation process of Figure 6 is modified, so that all dielectric layers are removed and only the bottom copper foil is remaining. The high-power chip is directly attached into the cavity onto the bottom copper layer of the cavity. In this configuration a very short thermal path with the lowest possible thermal resistance (equation 3) between the component and the heat sink is formed. It consists of only the adhesive or solder layer of the component-PCB connection, the bottom copper-layer of the PCB, and the thermal interface material between PCB and heat sink (Figure 7).

Surface finishes like ENIPIG is applied on all layers, and the electrical interconnection is done with wire bonding onto pads on the top or medium layer (Figures 7 and 8). For light applications, the cavity walls can be coated with highly reflective material as well (Figure 9).

Beside the excellent thermal behavior, this cavity board also shows additional advantages: It serves as package, which is protecting the component and in combination with an additional cavity (cavity in cavity, Fig. 9) it is also protecting the wire bonds. All together the concept results in a miniaturization in z-direction and finally in a reliable chip-package solution that supports long-term stability of LED-based luminaires.

Thermal Simulation

It is difficult to compare the overall thermal performance of different packaging concepts purely on the base of single point temperature measurements. A deeper understanding of particular advantages and bottlenecks of particular setup features is gained by thorough thermal simulations. Next, we compare three different packaging concepts using the same LED chip and the same operation conditions (Forward current IF = 300 mA). These blue-light emitting LEDs were assumed to produce a power loss of Ploss = 660 mW, while the color conversion to white light is related to additional losses due to Stokes shift and absorption in the glob top in a total amount of 160 mW. Though this number might appear small it should be noted that these optical losses are set free in a silicone matrix with low thermal conductivity. This kind of loss causes by far the highest temperature values inside the LED set-up.

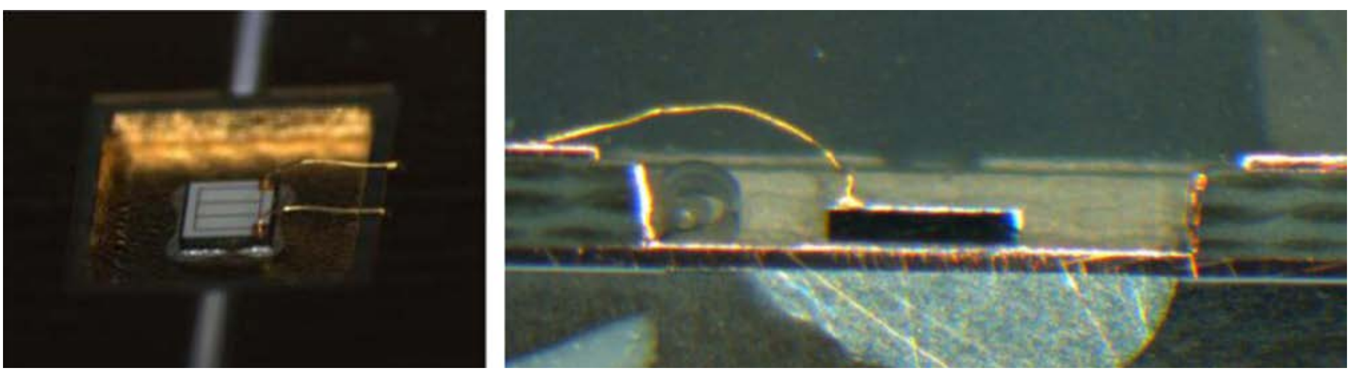


Figure 8: Chip in cavity bonded to the upper layer.

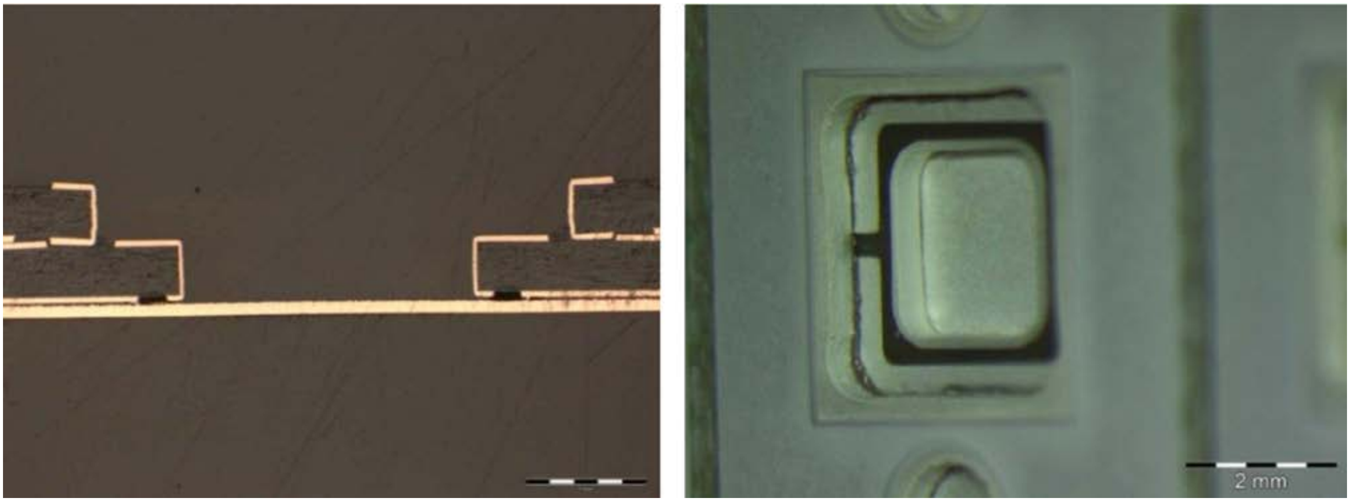
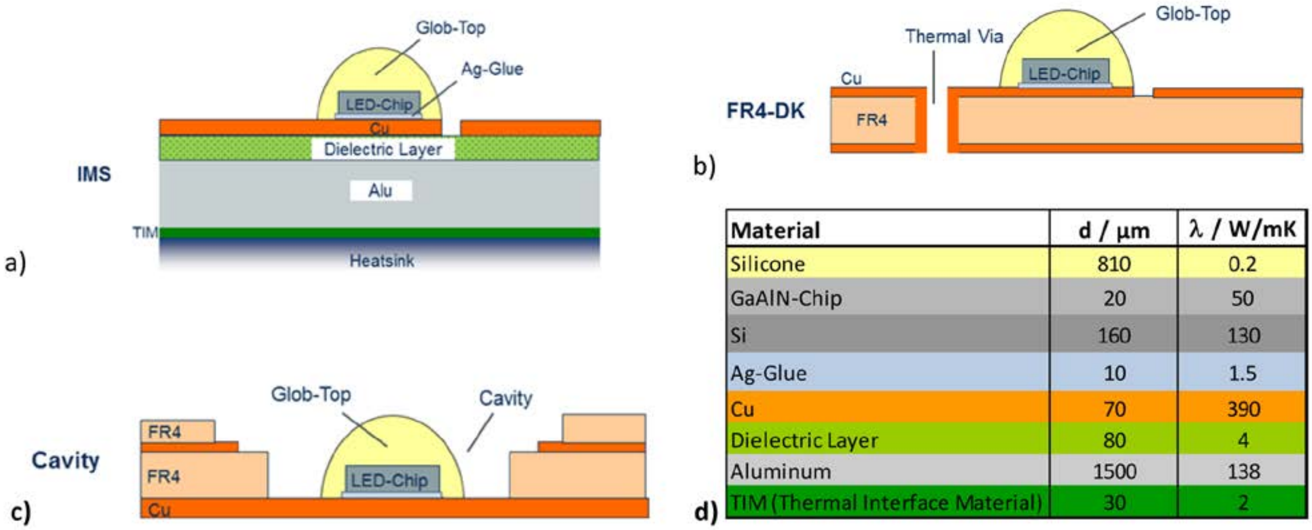


Figure 9: Cavity in cavity board with high reflective cavity walls.



d)

Material	d / µm	λ / W/mK
Silicone	810	0.2
GaAlN-Chip	20	50
Si	160	130
Ag-Glue	10	1.5
Cu	70	390
Dielectric Layer	80	4
Aluminum	1500	138
TIM (Thermal Interface Material)	30	2

Figure 10: Build-up of: a) IMS; b) FR-4 DK; and c) cavity board (LED-in-cavity); d) material parameters used for thermal simulation.

We considered the spatial distribution of these losses (an exponential approximation of the decrease of the loss intensity with increasing distance to the LED surface) with an "onion shell" model [6]. The test assembly is assumed to be mounted on a heat sink with a constant temperature of 25°C. Thus, at the assembly's bottom face, Neumann boundary conditions were considered: TC = 25°C. Further boundary conditions on the remaining surfaces were considered as natural convection and radiation assuming an emissivity of one. Three-dimensional steady-state thermal simulations with the finite element method using a multiphysics software package with materials data were made for all set-ups of the considered packaging concepts as shown in Figure 10.

Figure 11 depicts the thermal model of an FR-4-DK set-up as shown in Figure 10(b). In order to reduce the necessary node number without loss of accuracy, the hollow thermal vias were replaced by cylinders filled with

a substitute material of which the thermal conductivity in the perpendicular direction is equivalent to the hollow cylinder shaped copper vias with a wall thickness of 25 µm (Figure 11b). In this way a virtual thermal conductivity λsub of the via can be calculated on the base of the thermal conductivity λCu of copper, the cross sections of the copper walls *A*Cu and of air (DK6) or epoxy (DK2) in real vias[7]:

$$\lambda_{sub} = 4\frac{\lambda_{Cu} A_{Cu}}{d^2 \pi} \tag{5}$$

where d is the drilling diameter and the thermal conductivity of air or epoxy is neglected in comparison to λCu.

Results

The thermal simulation revealed that under normal operation conditions all three investigated packaging concepts allow to keep the LED-chip surface temperature at moderate levels between 27.5°C (LED-in-Cavity concept) and 45.5°C (FR4-DK concept) and that very high temperature gradients (more than 200°C/mm) exist in the silicone glob top immediately above the chip surface. In all cases the temperature maximum is found at glob top surface (ca. 85°C at the IMS, ca. 95°C at the FR4-DK, ca. 70°C at the LED-in-Cavity samples). Figure 12 depicts the temperature distribution of a LED-in-Cavity sample. For reasons of comparability, in all cases the shape of the color converter was assumed as spherical glob tops. It should be noted that in a real case of the LED-in-Cavity the color converter does not tower above the PCB top surface. Therefore, the height of the color converter and therewith the maximum temperature is even lower than considered in our simulation. The quite remarkable temperature differences inside LED chip and color converter of the three concepts can be understood by considering the temperature course along the perpendicular symmetry axis.

In spite of a heat flux density of more than 80 W per square centimeter the LED-in-cavity set-up keeps the LED chip at a temperature level below 28°C due to the 70 µm thick copper base layer and the shortest possible heat conduction path. The most significant temperature drops can be found in the thermal interface layer (TIM) between the heat sink and the copper base layer and in the adhesive layer under the LED chip (Figure 13).

The IMS module shows a LED-chip temperature between 32°C and 34°C. The most significant temperature drop is caused by the dielectric between the copper layer and the aluminum plate. The excellent thermal conductivity of the aluminum plate and the 35 µm thick copper layer can be recognized by the almost negligible temperature change inside the layer.

The highest temperature differences between heat sink and LED chip are found in the FR-4-DK samples. Due to the fact that the ther-

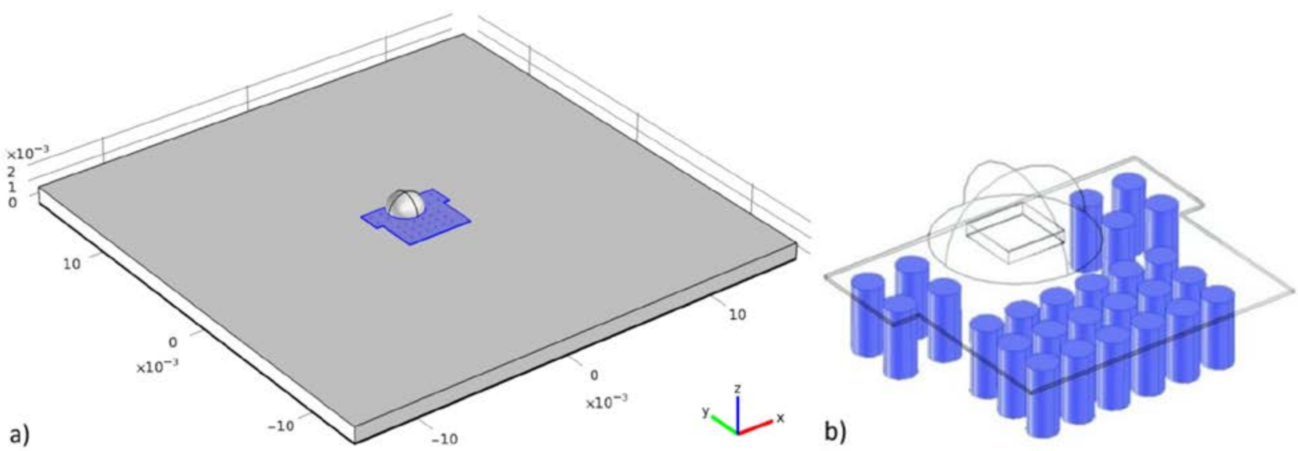


Figure 11: Thermal model of the FR-4-DK test sample: a) entire model; b) detailed view thermal via array.

mal vias are placed only in a pad range apart of the LED chip instead of beneath, the path for a major part of the heat flux is comparatively long. This leads to LED chip temperature between 32°C and 41°C depending on the choice of geometry variation (via count, drilling diameter, Cu thickness etc.). In this context the feature of the plugged via technology should be highlighted: Although the thermal conductivity of a plugged via is practically the same as the open one with same hole geometry, with plugged vias the perpendicular temperature drop across the PCB can be reduced significantly because they can be placed directly beneath the LED chip without the risk of solder soaking. The respective temperature functions along the perpendicular symmetry axis are compared with each other in Figure 14.

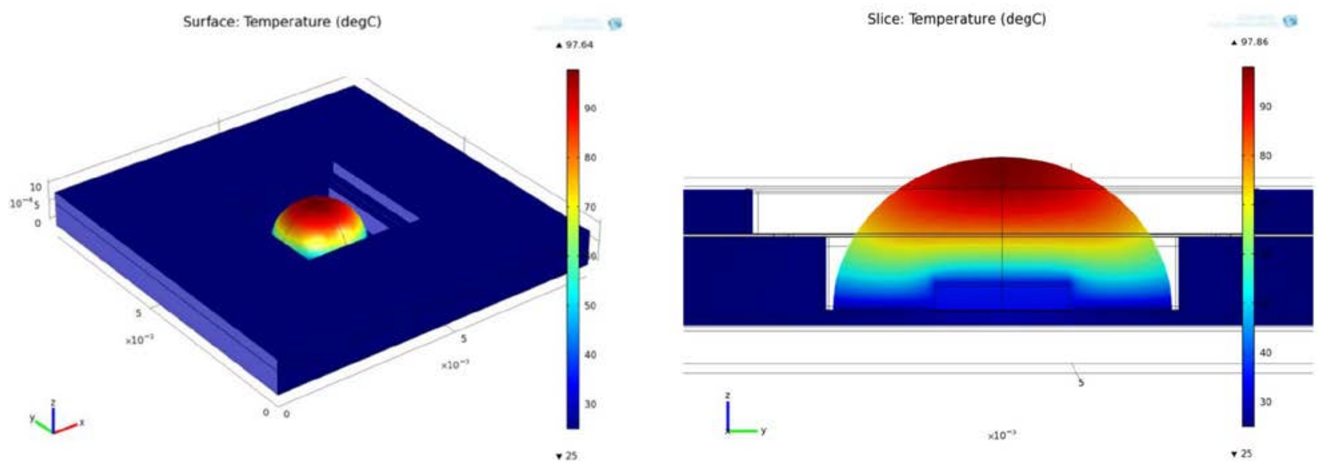


Figure 12: Results of thermal simulations; detailed views of temperature distribution in vicinity of the LED.

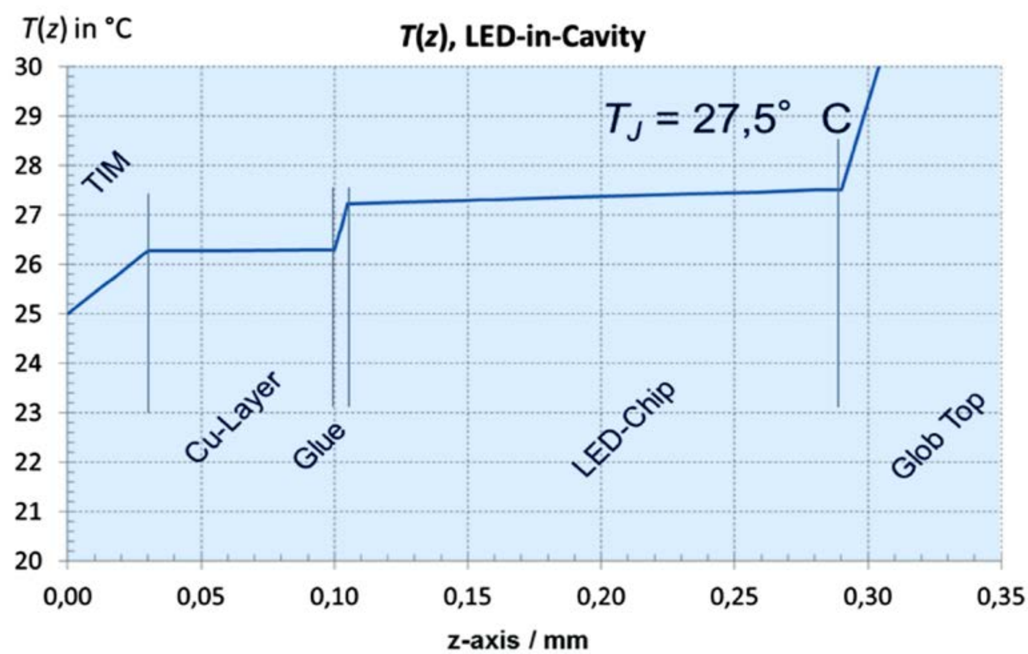


Figure 13: Results: Temperature profile along the symmetry axis in out-of-plane direction (Z-axis) of a LED-in-cavity set-up.

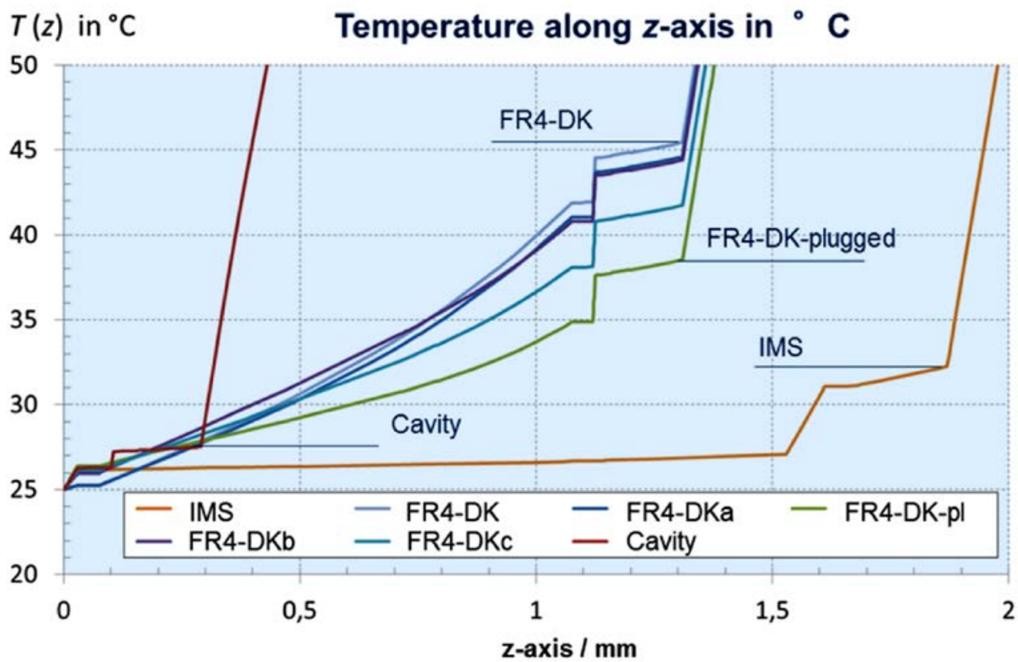
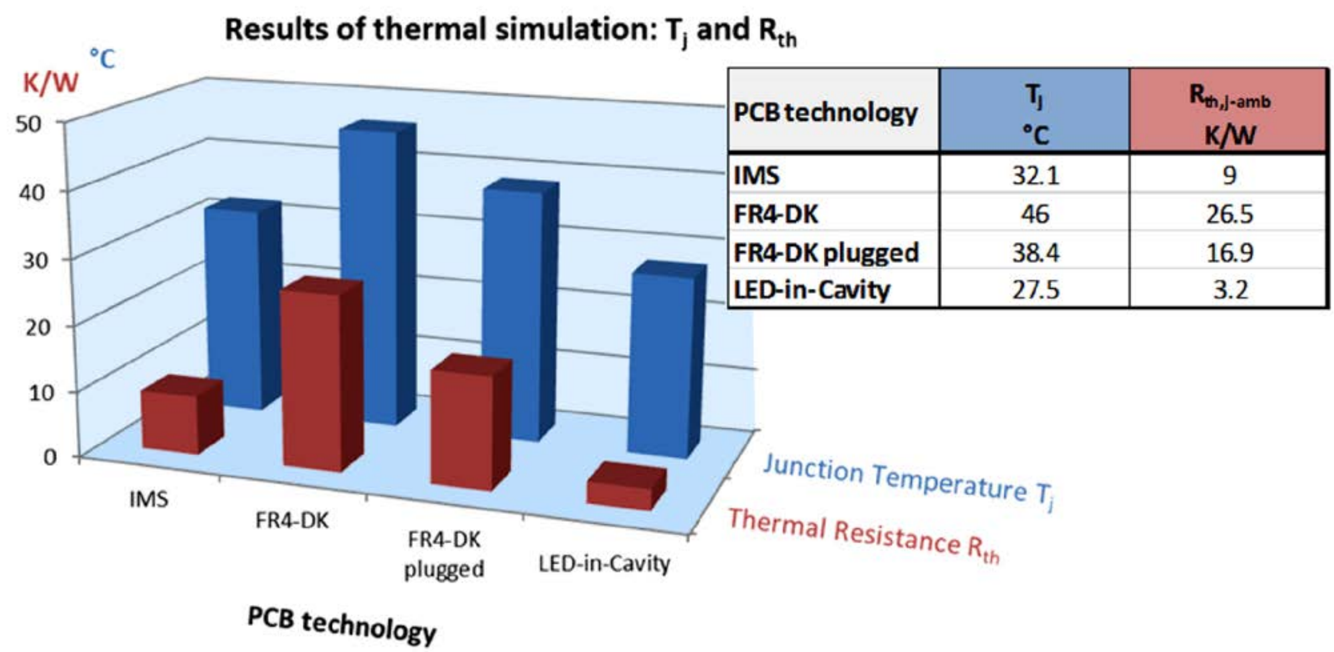


Figure 14: Comparison of the results of the different PCB technologies.



PCB technology	T_j °C	$R_{th,j\text{-}amb}$ K/W
IMS	32.1	9
FR4-DK	46	26.5
FR4-DK plugged	38.4	16.9
LED-in-Cavity	27.5	3.2

Figure 15: Comparison of the results of the different PCB technologies.

Using the average temperature of the light emitting LED chip surface as the junction temperature and the heat sink temperature as the ambient temperature, we defined the junction-to-ambient thermal resistance and compared this measure as the most representative one for all investigated set-ups (Figure 15). By far, the lowest thermal resistance can

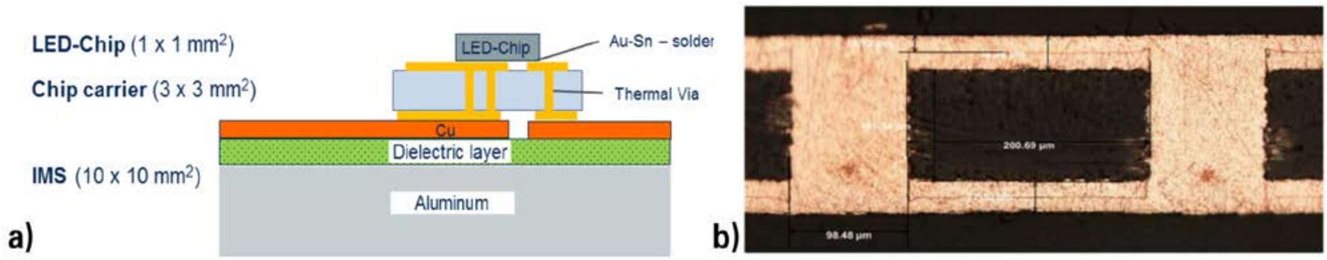


Figure 16: a) Chip carrier module build-up; b) cross section of chip carrier.

$$A_{hollow} = \frac{d^2 - (d-2a)^2}{4}\pi, \qquad A_{filled} = \frac{d^2}{4}\pi, \qquad \beta = \frac{A_{filled}}{A_{hollow}} = \frac{1}{4}\cdot\frac{d^2}{ad-a^2} \tag{6}$$

be seen at the LED-in-cavity set-ups, followed by the IMS variants. However, it must not be withheld that an insulation layer between heat sink and semiconductor is frequently unavoidable. An insulating layer between the copper layer and the heat sink is also possible for the LED-in-cavity solution but would also increase the thermal resistance. Conventional FR-4 PCBs with thermal optimized via technology have higher thermal resistances but proved to be attractive and cost effective variants at least for the mid-power range.

Advanced Thermal Management Solutions: Cu-filled Thermal Vias

Thermal vias are employed since a long time to improve the heat transfer between the two sides of the PCB and to couple heat spreading copper areas. Because of the fact that thermal vias are normally hollow cylinders, solder can be soaked by the vias as mentioned above and, therefore, components are frequently not directly placed on top of the via array. Exceptions are large high-power components where enough solder can be applied without the risk of critical voids forming underneath the component. This problem can be fully avoided if vias are fully filled with copper using a reverse plating process [8]. This can also help to increase the heat transfer area dramatically as can be shown by the following simple consideration. Let us compare the cross section of a hollow via (Ahollow) with the one of a filled via (Afilled) an average copper cross section ratio b can be calculated above in equation 6.

Herein d denotes the via diameter and a the via copper plating thickness.

For example, for a via with d = 200 µm and a = 30 µm b = 1,96 which clearly shows that by using filled vias the thermal resistance between top and bottom side can be cut in half.

Module Build-up and Thermal Simulations

For an investigation of the effectiveness of the filled-via approach a setup according to Figure 16(a) is considered. A LED-chip of 300 µm thickness and 1 x 1 mm² lateral dimensions is soldered by Au80Sn-solder onto a bismaleimide triazine (BT) submount (3 x 3 mm²) that is copper coated (35 µm) on both sides forming the thermally relevant structure of the LED submount. Filled vias (d = 200 µm, n = 20) connect top and bottom side of the submount (Figure 16b). This submount is soldered with Sn96Ag solder onto an IMS carrier (10 x 10 mm²) acting as heat spreader and heat sink interface. The solder layers were not modeled (omitted) because the temperature drop caused by the heat flow would be less than 50 mK. The aluminum part of the IMS was replaced by a constant temperature boundary condition. Table 2 lists the thermal properties of the materials inside the model.

The simulation results show that it is highly beneficial to use filled vias to reduce the resistance of the thermal path. The component can

Component	Material	Thermal conductivity λ in W/mK
LED	Sapphire	36
traces and vias of PCB	Copper	390
Dielectric of PCB	BT	0.12
Solder	Sn96Ag	not modelled (ΔT < 50 mK)
Dielectric on heat sink	Transtherm T2022	0.6
Dielectric of IMS	Filled epoxy	1.0 (thickness = 100 µm)

Table 2: Material properties of components used for finite element model.

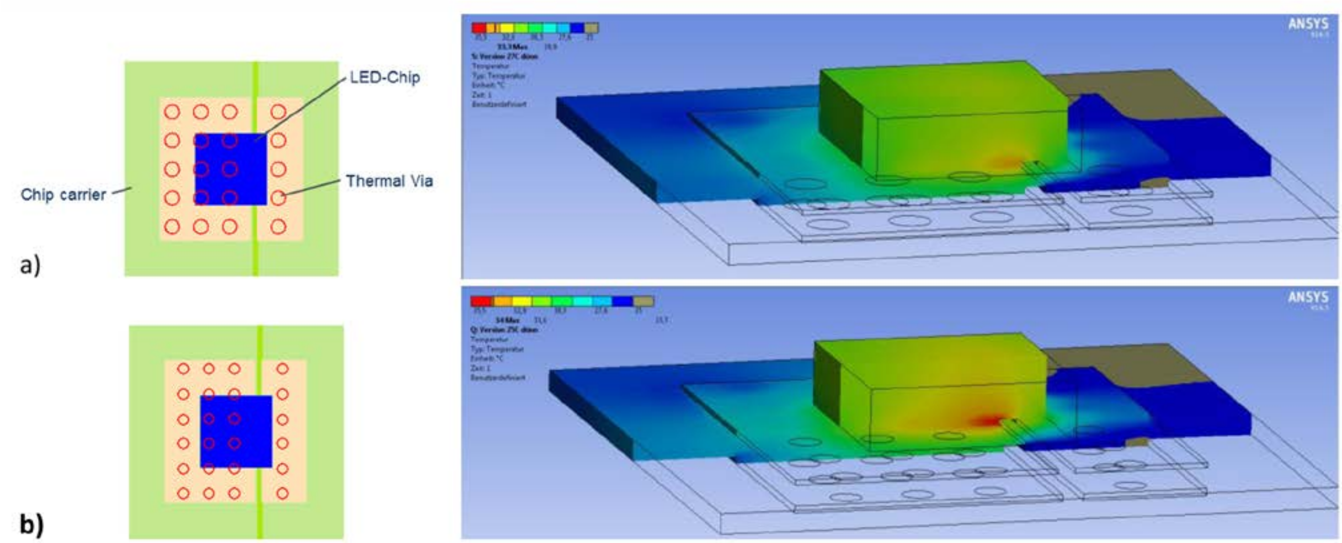


Figure 17: Chip carrier design and first results of thermal simulation: a) 20 vias, d = 200 µm; b) 24 vias, d = 150 µm.

Variant	via diameter in µm	number of vias		effective via cross section in mm²		max. temperature in K	thermal resistance in K/W
		all	under chip	all	under chip		
a	0.2	20	5.9	0.5	0.19	33.3	10.9
b	0.15	24	5	0.42	0.09	34	11.6

Table 3: Maximum temperature and thermal resistance with different thermal via setups.

be placed directly on top of the vias without any problems with insufficient solder (e.g., because of solder sucked up by the copper clad via hole). However, experience gained from manufacturing makes it clear, that via-filling is not always perfect and dimples on the surface can occur. Such an air void inside the solder layer beneath the chip is shown in Figure

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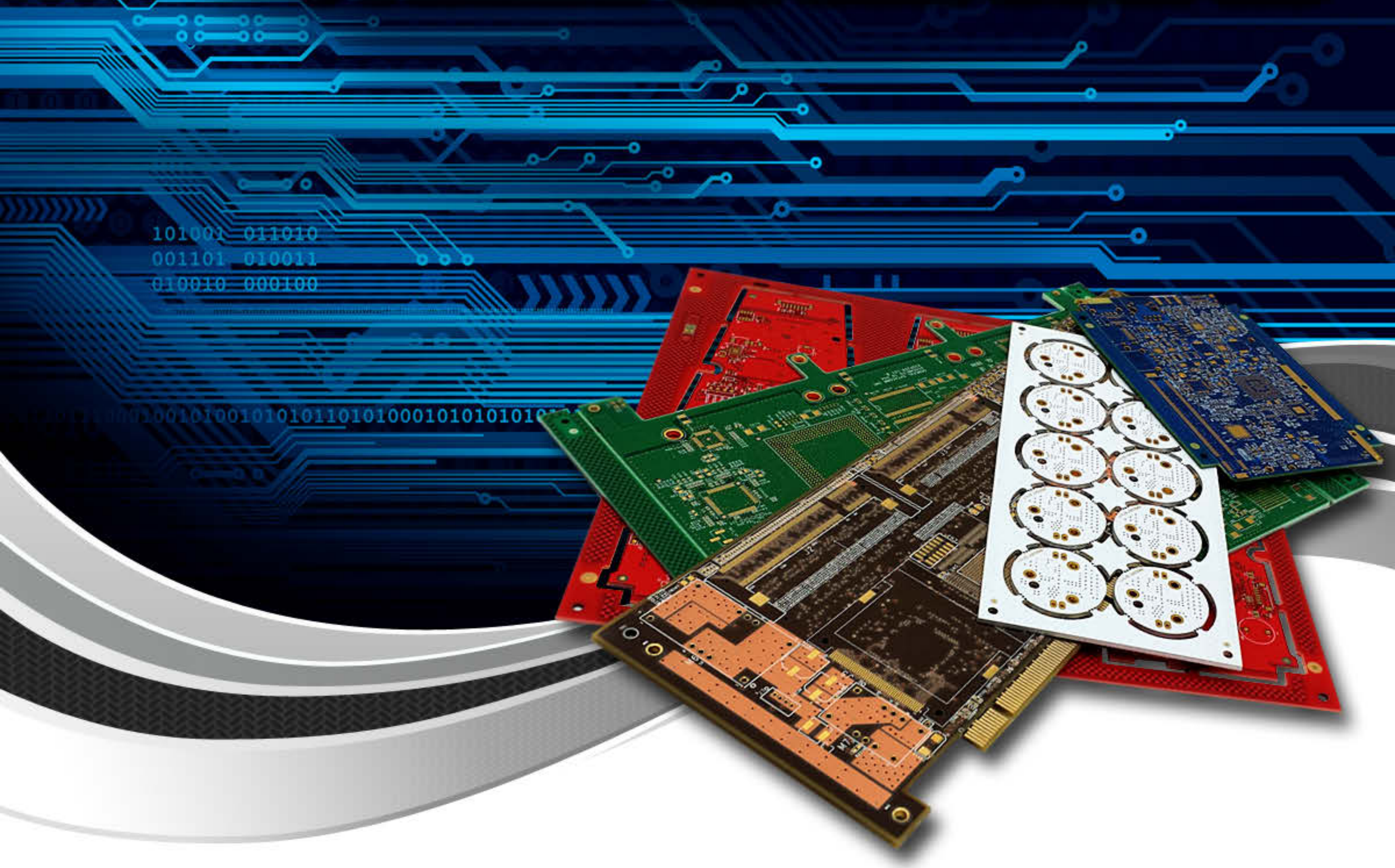

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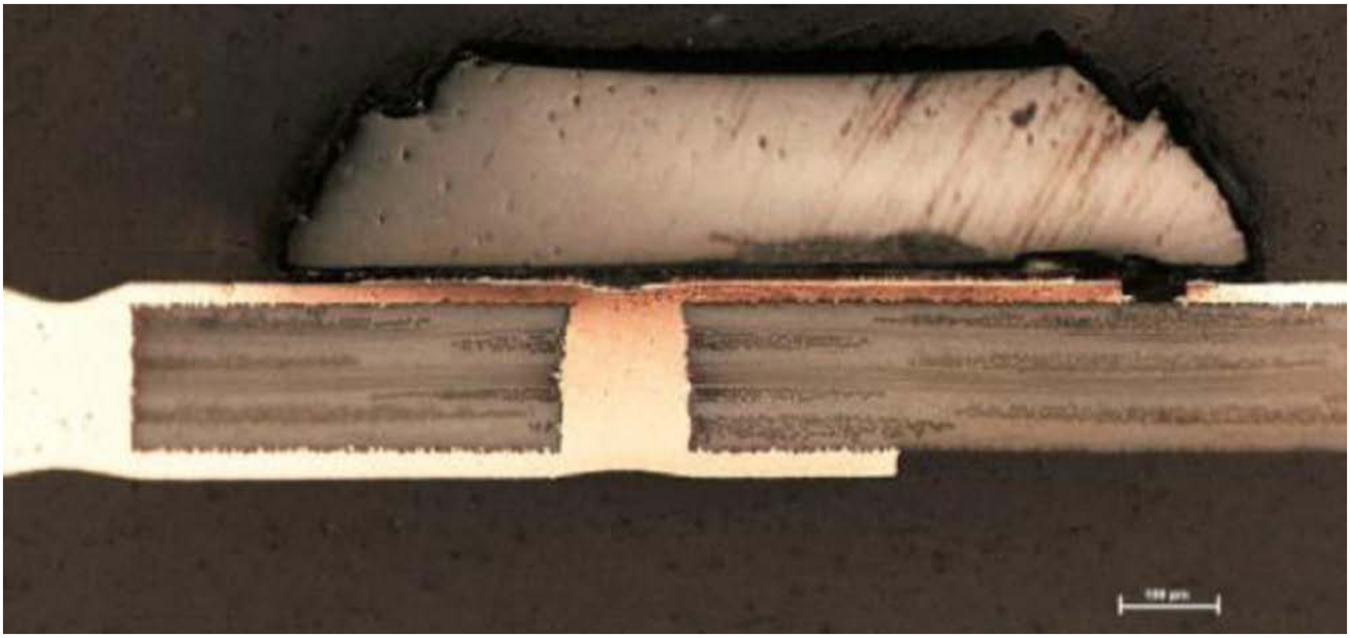

Figure 18: Chip carrier with dimple inside via.

18. The meaning of the solder defect due to the dimple formation in the galvanic process mechanical reliability will be investigated in further studies. However, thermal simulation proved that they are insignificant for the thermal resistance. Also optimization of via geometry and placement will be conducted, as well as the influence of copper thickness of the top layer that contributes the most to initial heat spreading of the chip's power loss.

Summary

Several different concepts for thermal management solutions on printed circuit boards for high-power applications were shown in this paper. Benefits of state-of-the-art concepts, like insulated metal substrates and open or plugged thermal vias, were illustrated by comparing the thermal performance of high-power LED modules built-up with different concepts. In particular, the plugged thermal vias and the insulated metal substrates, which allow technologists to realize short heat conduction paths, turned out to be interesting thermal management solutions.

Beside these well-established variants, some new concepts have also been presented. Cavity boards (boards with local depth reduction) show thermal advantages due to a reduced thermal path along the Z-axis through the board.

Thermal simulations of cavity boards attached with high-power light emitting devices show excellent cooling performance. In comparison with the simulation results of state of the art concepts, the cavity board approach shows by far the lowest thermal resistance of the board system and guarantees therefore also the lowest junction temperature for the attached high-power component. The realization of test vehicles of these concepts is planned, to verify the simulation data by thermal measurements on these test boards.

Furthermore, also the thermal advantages of copper-filled thermal vias in chip carrier boards have been presented. First results of thermal simulations have been shown and discussed. Further simulations and measurements on test vehicles are going on, and the results of these thermal investigations are also planned to be published in the near future.

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Exploring High-Temperature Reliability Limits for Silicone Adhesives

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Abstract

The thermal stability of silicone polymers, fluids and resins has been well documented and studied extensively. The high-temperature performance of silicone adhesives and sealants used for electronics applications has only moderately been investigated. This report documents the effects of very high-temperature exposures to electronics-grade silicone adhesives and sealants for such properties as tensile strength, elongation, tensile modulus, weight loss, shrinkage, durometer, and lap shear adhesion. The goal of the work is to determine application "life expectancies" of the products as well as an extrapolated estimate of the Underwriter's Laboratories' "continuous use" temperature rating— the highest temperature at which a product is expected to lose no more than 50% of its original value for whatever key property degrades the fastest.

Four different formulations of silicone adhesives and sealants were evaluated for high-temperature stability. For these products, elongation was found to be the fastest degrading property among those tested. The data was found to fit a power curve of exposure temperature vs. time to reach a 50% loss of initial tensile strength and elongation to an R-squared value of 0.99 and to a linear fit in an Arrhenius plot to the same very strong fit. These plots could be used to closely estimate the effects of heat aging on the material over a wide range of temperatures.

Introduction

Silicone is the generic name used by many to identify a family of products based on the polydimethyl siloxane (PDMS) molecule with unique characteristics. For electronics applications silicones can be used as adhesives, encapsulants, gels, protective coatings, thermal

management materials, even device packaging materials and wafer-level coatings.

Silicones have a combination of properties which contribute to provide a proven long-term reliability and performance in electronics applications. These features include: unmatched thermal stability, flexibility, moisture resistance, adhesion to many common substrates used in electronics, low ionic impurity and compatibility with common processing techniques. Among all these characteristics that are shared by the majority of silicones, one property is recognized as one of the most useful in electronics applications and that is their consistent performance over a very wide temperature range.

The lower and upper operating temperature limits for silicones are not very well defined. Some approaches have placed these limits in the range from -40 to 150°C. Others, less conservative, have placed the limits between -50 and 200°C. Both approaches are correct; however, the applicability of each will depend much on the product used. Operating temperatures for silicones have a great dependency on the formulation, filler type and content, additives, functionality of silicone polymer, etc. Silicone products can be formulated in different ways to provide higher thermal stability or lower temperature flexibility. There are silicone products that can be exposed for long periods of time to temperatures as high as 250°C or as low as -80°C. These would be considered, within the product line, as special materials. For general purpose adhesives/sealants, within the scope of this paper, the operating temperature limits will be defined as -45 to 200°C.

In electronics, the upper temperature limits are most frequently determined by the end use application. For some applications, such as automotive electronics, electronic parts may be exposed up to 175°C for extended periods of time or even higher temperatures for short durations. Likewise, the time duration used to determine thermal stability is extremely dependant on the specific requirements of each application.

The performance of silicone adhesive/sealants, such as the ones under the scope of this paper, when exposed to temperatures around 200°C has been very well documented and evaluated. However, there is very little relevant data detailing the performance of these products when working above the operating limits (200°C) for long-term exposures or even short-term periods. This missing data acquires great relevance for today's electronics applications, where electronic modules may be exposed to extreme high temperatures for short or long periods of time, identifying as extreme high temperatures any temperature above the limit exposed here, which is 200°C. It is the goal of this paper to review the performance of four different formulations of silicone adhesives/sealants when exposed to temperatures above 200°C as a way to provide valuable guidance in the proper selection of these kinds of products for an electronics application.

High-Temperature Requirements

Nowadays a large number of industries require materials to be exposed to high temperatures, usually for rather short time durations but sometimes for extended periods that could go from a couple of months to several years. In electronics, the upper temperature limits are most frequently determined by the end use application. For some applications, such as automotive electronics, electronic parts may be exposed up to 175°C for extended periods of time or even higher temperatures for short durations. Likewise, the time duration used to determine thermal stability is extremely dependant on the specific requirements of each application. Solder reflow ovens may only sub-

Application	Max Temp	Duration
Solder reflow ovens	225-260°C	10-90 seconds
Automotive on-engine modules (extended warranty)	175°C 150°C 150°C	5 min. 1000 hrs 3000 hrs
Industrial power devices	250°C 200°C 175°C	hours months years

Table 1: Typical application temperatures and durations.

ject the materials to a few seconds or minutes of high temperature, and materials are not expected to significantly change in performance even though the exposure temperatures may be very high.

Many applications may have transient temperature "spikes" that considerably exceed their standard operating temperatures. These spikes could have durations ranging from a few seconds to a few minutes or even an hour or more. While it may be assumed that a few seconds at relatively high temperature may have insignificant consequences on material properties, it is unrealistic not to recognize that even a few minutes at very high temperatures may change certain material characteristics. For example, for thermoplastics such changes may be readily apparent if the material begins to melt and lose dimensional stability. For thermoset products however, degradation may not be as easy to observe.

Silicone adhesives and sealants are widely used to bond, seal and sometimes protect electronic components or modules for high-temperature applications. The stability of silicone adhesives and sealants to high temperature in the order of 200°C is well accepted, and typically is higher than most other polymeric materials used in electronics. However, there is very little relevant data detailing long-term high-temperature exposure (>200°C) or even short-term to the temperatures experienced in today's electronic applications (Table 1).

Test Methodology

Determining the thermal stability of a material is not always a straightforward task. There are many important properties of a given material, and many or most will change with heat induced degradation. All important properties should be evaluated with a test methodology that ideally enables short, mid and long-term durability estimates to be made.

Thermogravimetric analysis (TGA) has been extensively used to determine the thermal stability/degradation of different materials. The basic principle involved in TGA is simply to weigh a sample of the material under study in a controlled atmosphere while the temperature of the sample is varied in a known manner. Thermal degradation is related then to the weight loss of the sample. This method has proven poor efficacy in determining the thermal degradation of silicone products as silicones when exposed to high temperatures undergo several transformations by a variety of processes, including oxidation, siloxane rearrangement and hydrolysis. Siloxane rearrangement occurs without the formation of volatiles where extensive depolymerization may take place before fragments small enough to evaporate without further decomposition can be produced. This rearrangement will lead to the loss of physical properties, not precisely linked to weight loss.

At the same time, the degradation of silicones at high temperature by oxidation slowly transforms the material into more quartz-

Silicone Adhesive	1	2	3
Description	1-part het cure (self- leveling)	1-part heat cure (thixotropic)	1-part moisture cure (thixotropic)
Hardness, Shore A	65	65	40
Tensile Strength, psi	870	750	1150
Modulus, psi	600	660	200
Elongation, %	200	120	500
Lap Shear, psi	700	600	500

Table 2: Typical properties for the products used for this study.

like properties. Thus the electrical insulation properties of the product remain almost unchanged or even improve with such exposures. Under these bases, it is easy to understand that the thermal stability of silicones adhesives and sealants under the scope of this paper needs to be linked to the degradation of physical properties, such as: tensile strength, elongation, etc.

UL Standard 746B10 offers a methodology that can be used to estimate a 10-year life expectancy or half-life of polymeric materials. It proposes the useful life of a material to be defined as the time required to lose no more than 50% of any application-important property. The highest temperature at which 10 years of continuous exposure will retain 50% of the most sensitive important property is referred to as the relative temperature index, or RTI. This standardized method works quite well to study high-temperature exposures for silicon adhesives and sealants as there are quantifiable properties such as tensile strength or hardness that can be easily measure to verify the performance of the material.

The UL RTI type of standard gives a means of quantitative comparison between materials for long-term exposures, and the data can also readily provide short-term exposure expectations as well. However, it is important to remark that sensitive applications may require additional validation with specific performance and exposure time parameters. UL RTI values are 10-year exposure estimates. To obtain data for this length of aging is, of course, not practical. Instead data is typically collected at a minimum of four high temperatures. The time to lose 50% of original properties is then plotted vs. temperature to obtain predictive graphs. Ten-year life estimates are then extrapolated from these plots. For this study, five exposure temperatures were used: 200, 225, 250, 275 and 300°C.

The performance and life expectancy of the silicone adhesives studied here when exposed to temperature higher than 200°C will then be expressed in a more useful way following the guidelines mentioned above.

Proposed Products and Tests

The group of products used for this study is formed by a one-part moisture cure silicone sealant and two heat cure adhesives (self-leveling and thixotropic). These products will be evaluated for thermal stability by measuring properties such as tensile strength, elongation, modulus of elasticity, durometer and lap shear adhesion (to unprimed aluminum) after exposure to the five different temperatures indicated above for up to 1,000 hours or less, depending on the time to lose no more than 50% of original value for the property measured.

The typical properties for the products included in this study are shown in Table 2.

Cured sheets of 2 mm nominal thickness were prepared and standard tensile dog bone samples were die cut from listed products. These samples were laid onto trays and placed in convection ovens for set time durations and then removed, cooled to room temperature and tested. Lap shear adhesion was evaluated onto bare aluminum.

Property	Value
Durometer, Shore A	64
Tensile Strength, PSI	874
Elongation, %	216
Tensile Modulus, PSI	622
Lap Shear Adhesion, PSI	674

Table 3: Initial properties for Adhesive 1 (one-part, self-leveling heat cure).

Results and Discussion

Samples prepared as described in the previous section of this report were aged in convection ovens at five temperatures. Since one of the purposes of the study was to find a much faster means to predict 10 years of heat aging, very high temperatures were used to obtain fast degradation rates.

At the very high temperatures the degradation of the silicone adhesive occurred very quickly. This led to a problem in how to account for the time the samples required to reach the oven set temperature. It was found that in nearly all cases the small dog-bone samples required approximately six minutes to reach 95% of the oven set point temperature. These six minutes were discounted for the purposes of this study. Therefore a time recording of 0.1 hours would in actuality refer to six minutes of residence time at the specified temperature plus an additional six minutes to reach the oven temperature. While this method has its drawbacks especially at the highest exposure temperature, it was a practical and expedient method that appeared to fall within the experimental error of the data.

For reporting purposes, the following experimental data presented in detail through next sections of this report will describe the performance of the adhesive 1 (one-part, self-leveling, heat cure adhesive) when exposed to high temperature as representative of the other two adhesives/sealants tested.

Thermal degradation is often not catastrophic but instead a process of steady property loss. Determining a suitable endpoint can therefore be somewhat subjective. One line of reasoning would say that when any property exceeds specification limits it has degraded past the part design and qualification standards for which it was chosen.

However, many material specification limits are based on a standard set of properties that are more specific to identifying the main characteristics of the material vs. actual application-use requirements.

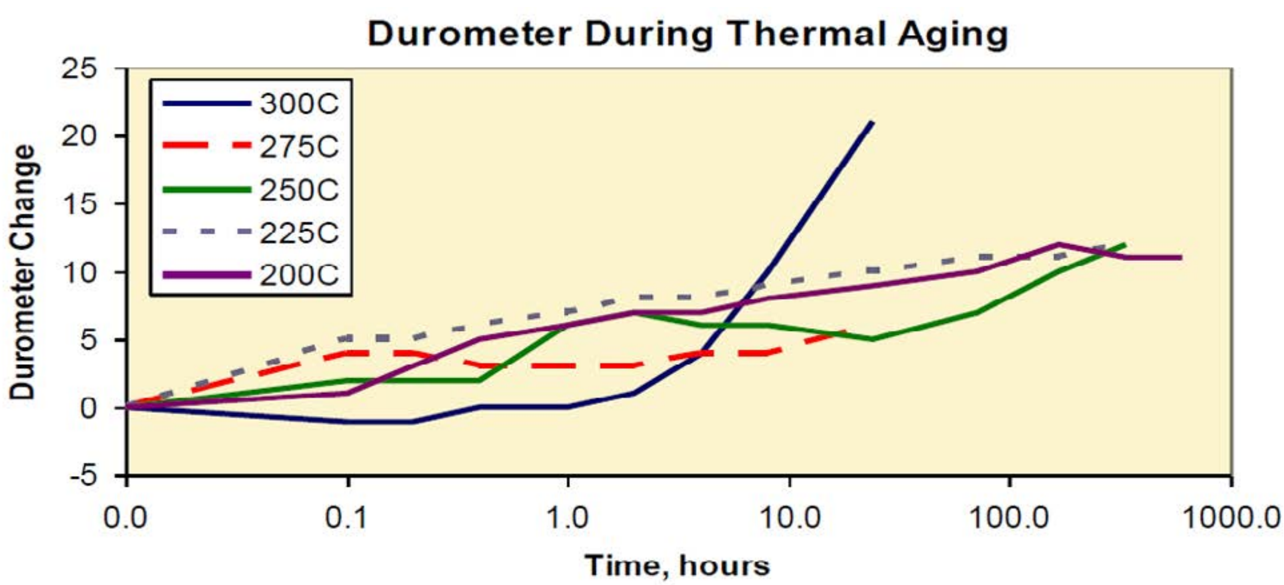


Figure 1: Change in elongation during thermal aging.

For a highly elastomeric material like silicone, an interesting point is elongation. Note that the typical elongation of the adhesive 3 (Table 1) is 500%. It is unlikely that for actual applications the adhesive is stressed close to its property capability, stretching the adhesive up to 500% its original size. Using the UL RTI type of test criteria where the end-of-life set point of any property is the loss of half of its original value, one would conclude that when the elongation of this material had dropped to 250% it is degraded to an end-of-life set point. However, a material

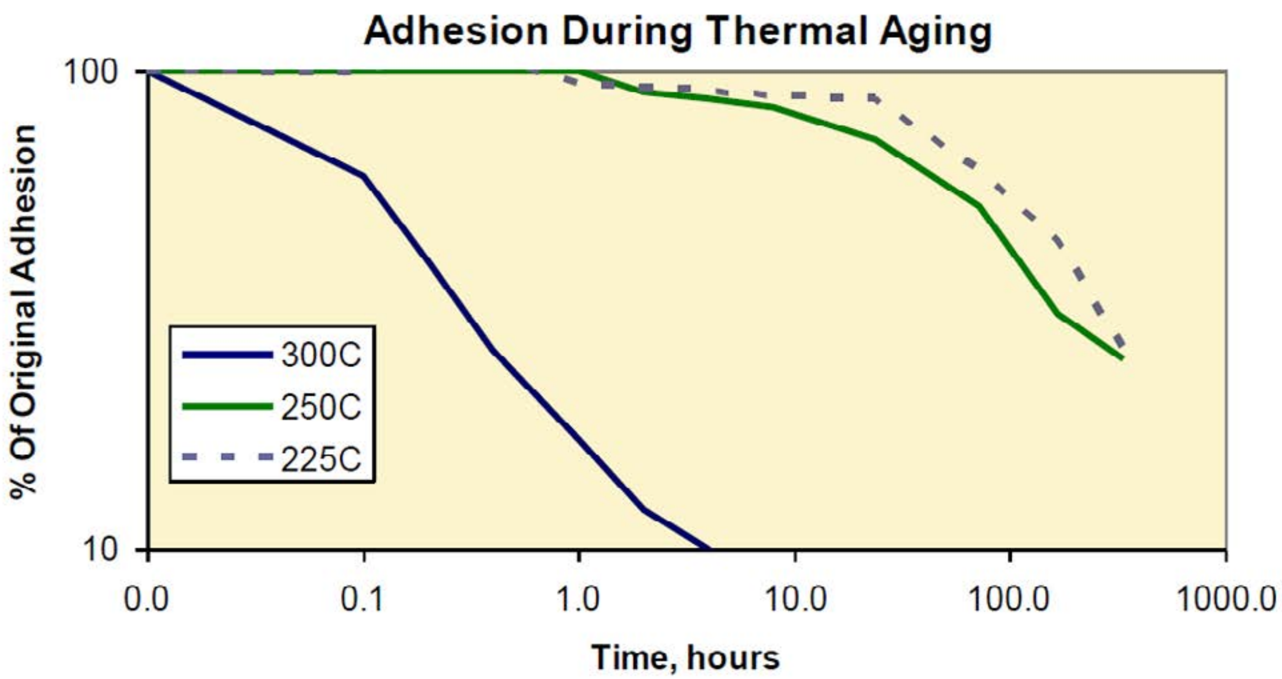


Figure 2: Change in tensile strength during thermal aging.

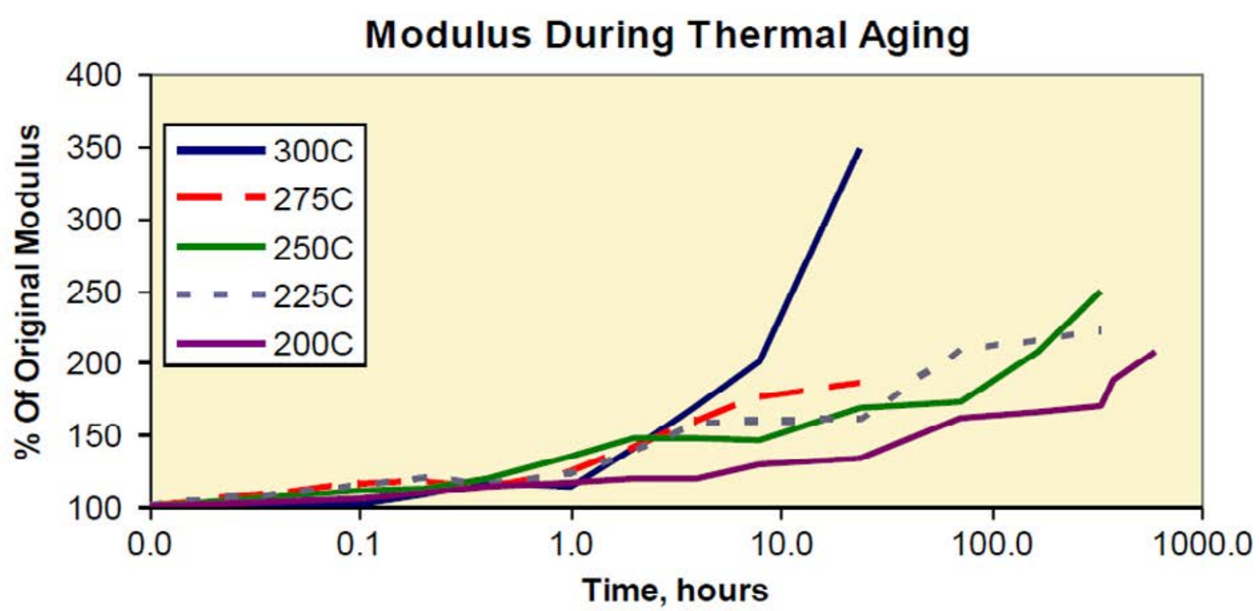


Figure 3: Change in durometer during thermal aging.

Time, hr	% Change Durometer, points	Tensile	Elongation	Modulus	Adhesion
0	0	0	0	0	0
0.1	-1	76	52	101	60
0.2	-1	70	42	109	40
0.4	-3	60	34	117	26
1	0	53	29	114	17
2	1	46	22	140	12
4	4	42	19	160	6
8	10	50	16	201	8
24	21	62	12	348	4

Table 4: Thermal aging for Adhesive 1 @ 300°C.

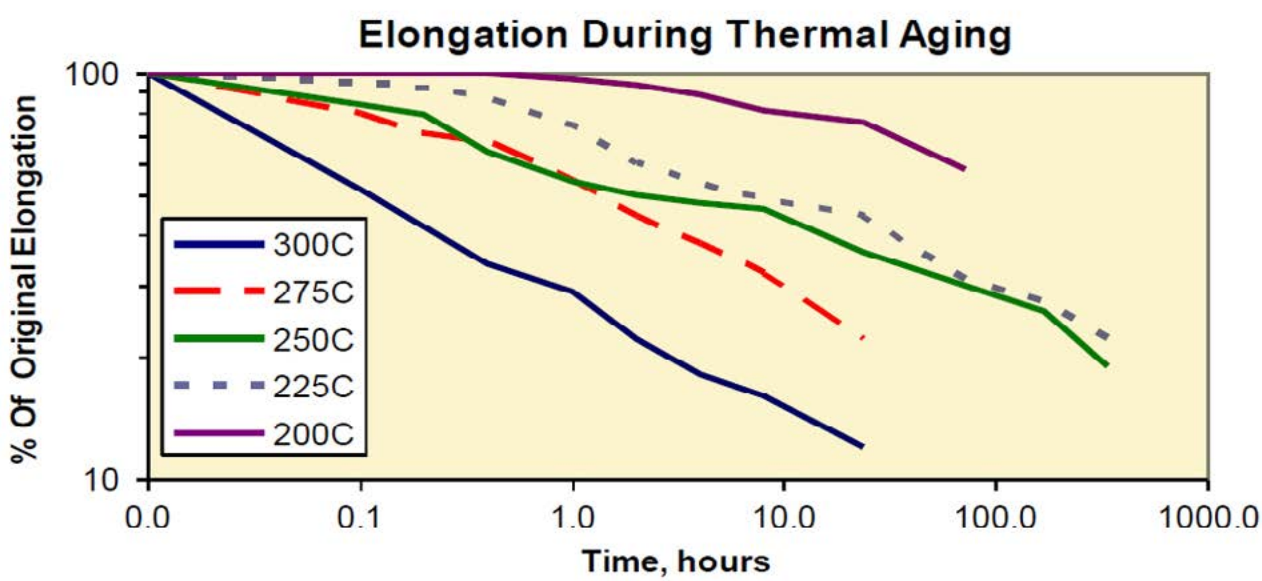


Figure 4: Elastic modulus during thermal aging.

retaining 250% elongation is still highly elastomeric and this property is likely still more than adequate for a great number of applications.

Another line of reasoning would say that an end-of-life set point should be determined as when a material reaches some certain minimum value for a given important property. In the material example, the criteria might be retention of an absolute value of 50–100% elongation. Of course, these criteria would be very application specific and would require a great deal of testing for any given application, considering operating conditions and geometric dimensions of the sealed part.

Table 4 show the percent change in each property measured for sample 1 when exposed to 300°C at different times. Elongation and adhesion were found to be the most rapidly changing property during thermal aging. This is something typically observed in silicone products. High-temperature degradation promotes polymer rearrangement and oxidation (as discussed earlier) that creates additional chemical bonds between polymers, forming a stiffer structure. As the new bonds are formed, it is common for silicones to become physically stronger exhibiting a higher tensile strength (Figure 2), higher durometer (Figure 3), and higher modulus (Figure 4). However, tensile strength will eventually begin to decrease as the material continues aging at high temperature, becoming somewhat brittle. As the new polymeric structure loses some of its flexibility, which is clearly shown in Figure 1, elongation is dramatically reduced by thermal aging.

For adhesive 1, the original elongation for the product reduces to 50% after an effective exposure of approximately six minutes at 300°C, marking this point the life expectancy limit at this temperature following the guidelines of UL Standard 746B10 previously mentioned. Similar behavior is observed when the adhesive is exposed to the other temperatures (Figure 1). A summary of results for the other properties (durometer, tensile strength, lap shear adhesion and modulus) are presented in the following figures.

The test procedures used in this study allows to obtain data in a period of weeks to a couple of months at very high exposure temperatures that could be used to confidently predict longer term property degradation at much lower temperatures. The 10-year life expectancy to lose no more than 50% of its initial elongation was predicted to be 149°C for adhesive 1 (one-part, self-leveling heat cure adhesive).

For this study working with silicone adhesives, elongation was probably the best property to track since it was found to degrade the fastest and had by far the most consistent results. Tensile strength also generally lowered over exposure time, but there was more scatter in the data and it is entirely possible that at early points in a given high-temperature aging process the tensile strength may increase and durometers may decrease for a short period before going in the directions most normally observed in thermal oxidative degradation mechanisms. At the beginning of the work, there was concern that lap shear adhesion may be the property to degrade the fastest. The data showed that while

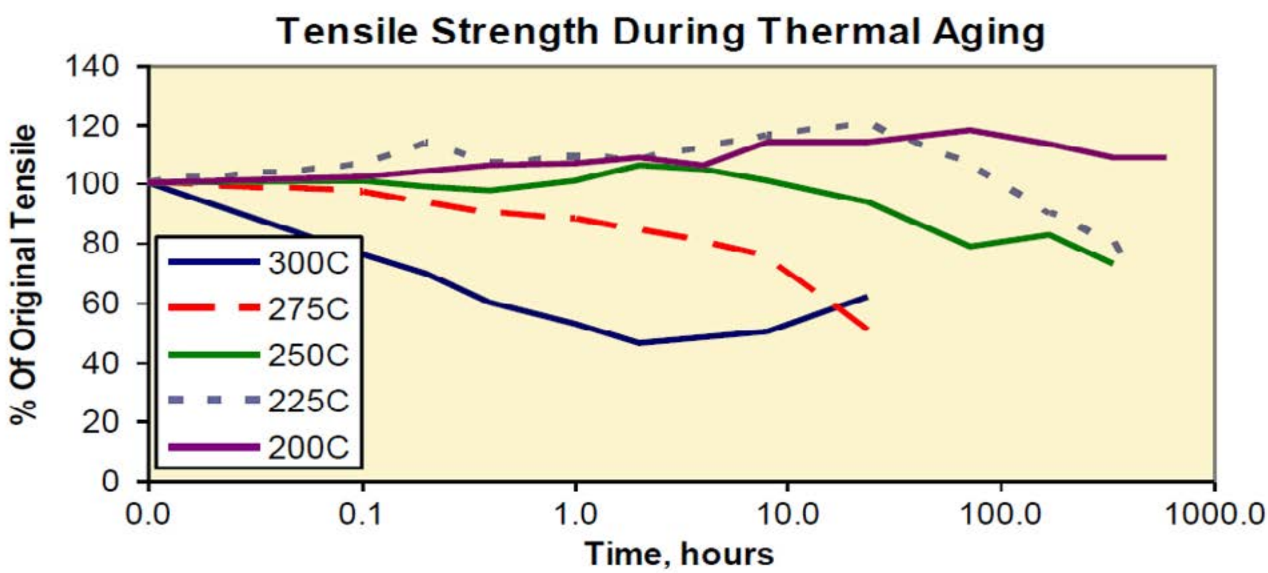


Figure 5: Lap shear adhesion during thermal aging.

Silicone Adhesive	1	2	3
Description	1-part heat cure (self-leveling)	1-part heat cure (Thixotropic)	1-part moisture cure
10 yrs	149C	136C	158C
1000 hrs	188C	178C	254C
1 hr	265C	266C	321C
1 minute	325C	335C	340C

Table 5: Time to lose 50% of original elongation for silicon adhesives.

adhesion did indeed deteriorate with high-temperature exposure, it did not change as fast as elongation.

Since elongation was the fastest degrading property, this was used to generate a predictive plot of time to lose 50% of the original value.

Using the same procedure and method as indicated for the adhesive 1 (one-part, self-leveling, heat cure adhesive), the estimated highest temperature exposure for the other two adhesives/sealants evaluated here is shown below (Table 5).

Conclusions

When silicone adhesives/sealants are exposed to temperatures above 200°C, and in some cases above 150°C (depending on the silicone formulation), some chemical degradation starts impacting some of the physical properties of these products. This chemical degradation is promoted by a variety of processes, including oxidation, siloxane rearrangement and hydrolysis. The property that shows the highest and fastest degree of degradation is the elongation. Elongation was used then to predict the temperature limits exposure for the adhesives/sealants evaluated under the scope of this paper, following the guidelines offered by the UL Standard 746B10.

In this way, the limits indicated here were determined by the time required for the adhesive/sealant to lose no more than 50% of its original elongation when exposed to different temperatures. It is important to remark that for some silicone adhesives/sealants with initial elongation values in the range of 400 or 500%, losing 50% of its original value leave them with an elongation in the range of 200 or 250%. A material retaining 250% elongation is still highly elastomeric and this property may still be more than adequate for a great number of applications. Therefore, the data reported in this paper should be used only as a guideline to establish general temperature exposure limits. Any specific application will require extensive testing and evaluations to determine the durability and maximum temperature exposure for the silicone, taking into consideration operating conditions and environmental factors. **SMT**

Carlos Montemayor is an applications engineer with Dow Corning.

Figure 1: Fine-line gold conductor on a ceramic substrate provides excellent thermal properties.

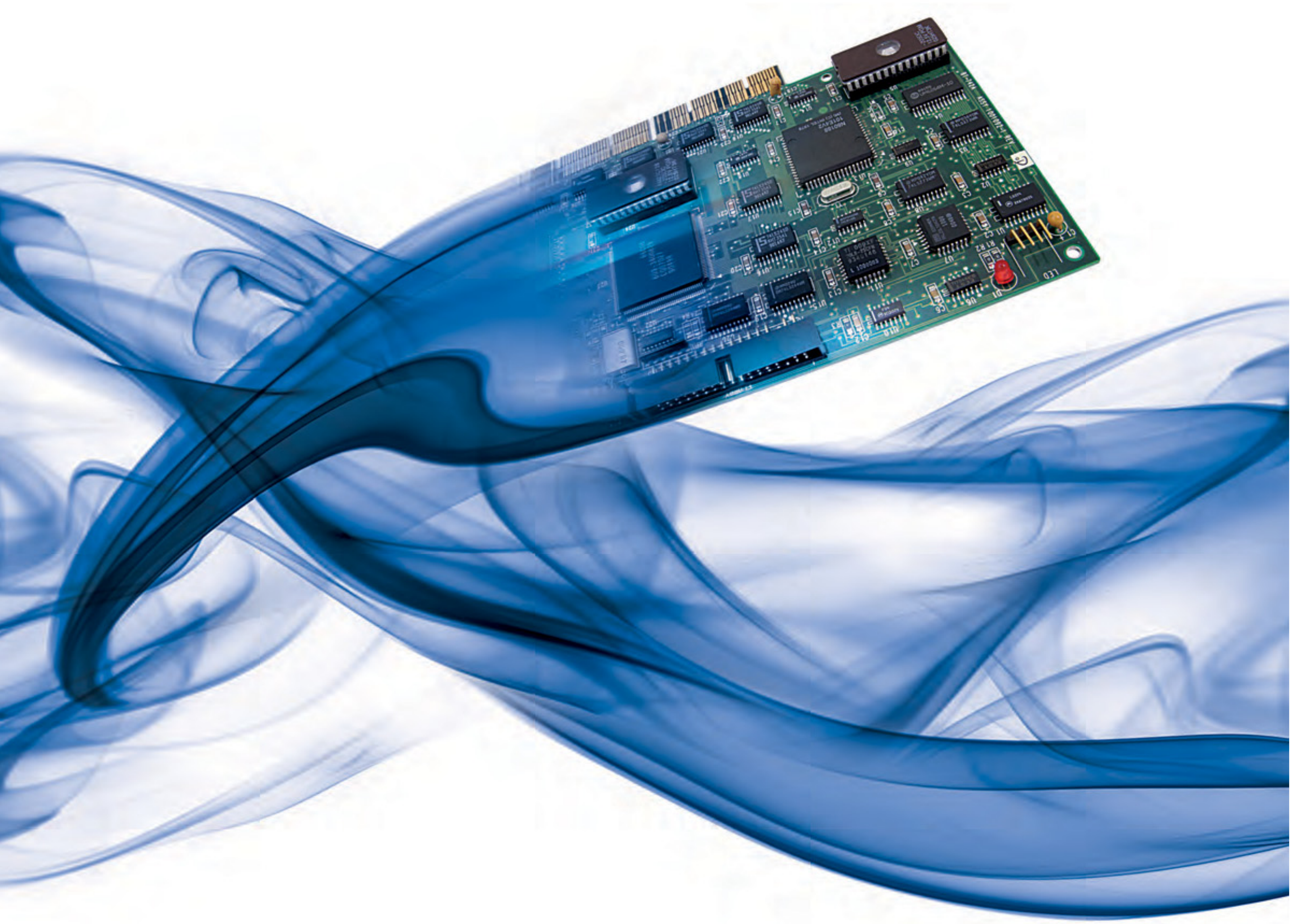
Trends in Thermal Management Materials for Electronic Circuits

by Mark Challingsworth
HERAEUS PRECIOUS METALS

All electronic devices generate heat, and this heat must be dissipated to guarantee reliability and prevent untimely failures. However, the various materials used in electronic devices, such as polymers, ceramics and metals, all have different thermal expansion coefficients, and these differences can cause thermal management problems.

One of the biggest challenges facing the electronics industry is matching different material sets used to ensure the highest thermal conductivity, while keeping the thermal expansion of the various materials similar enough to prevent reliability issues. Keeping heat out of the electronic device, or removing the heat and cooling the device, is necessary for proper operation. Heat removal helps to eliminate mismatched thermal performance which can cause operational failure.

Thermal management is an important component of electronic circuitry for a myriad of products, from power electronics used in electric and hybrid cars, to solar and wind energy equipment, to oil and gas downhole drilling applications, and high-powered LED devices. As an example, renewable electrical energy from solar and wind sources must be converted from direct current (DC) to alternating current (AC).



To accomplish this, the solar and wind energy passes through a power conversion module. The circuitry must be able to handle the heat generated in the conversion process, and that is where thermal management techniques come into play.

Power devices contain a metallized substrate that carries the high current through the circuit with minimal losses. The substrate is not only an important component for the overall thermal performance of the electronic device, but must also provide minimal thermal resistance. This thermal substrate is also necessary for high mechanical and electrical reliability, and must be compatible with standard circuit manufacturing technologies to help with cost competitiveness.

Handling the Heat

Another challenge affecting thermal management applications is the push by electronic manufacturers for materials that can handle extremely high temperatures. In the past, most materials, such as those for the automobile industry, were made to handle temperatures from -55°C to 150°C. Now, the OEMs are interested in designing cars with the electronics closer to the engine for better monitoring capabilities. This means, though, that the electronic circuits will be subject to hotter environments near the motor. It is necessary then

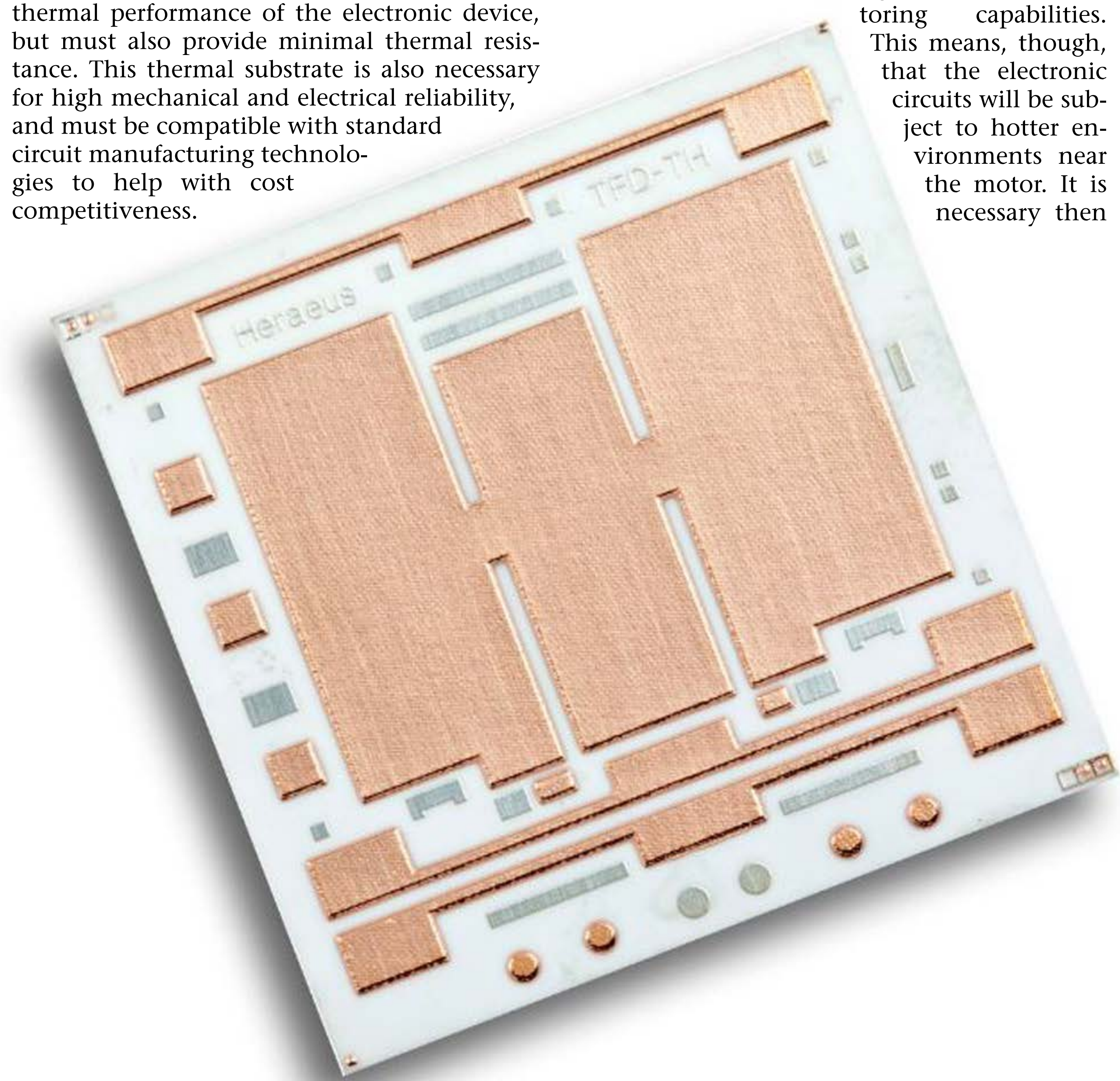


Figure 2: Power substrate made from thick-printed copper paste.

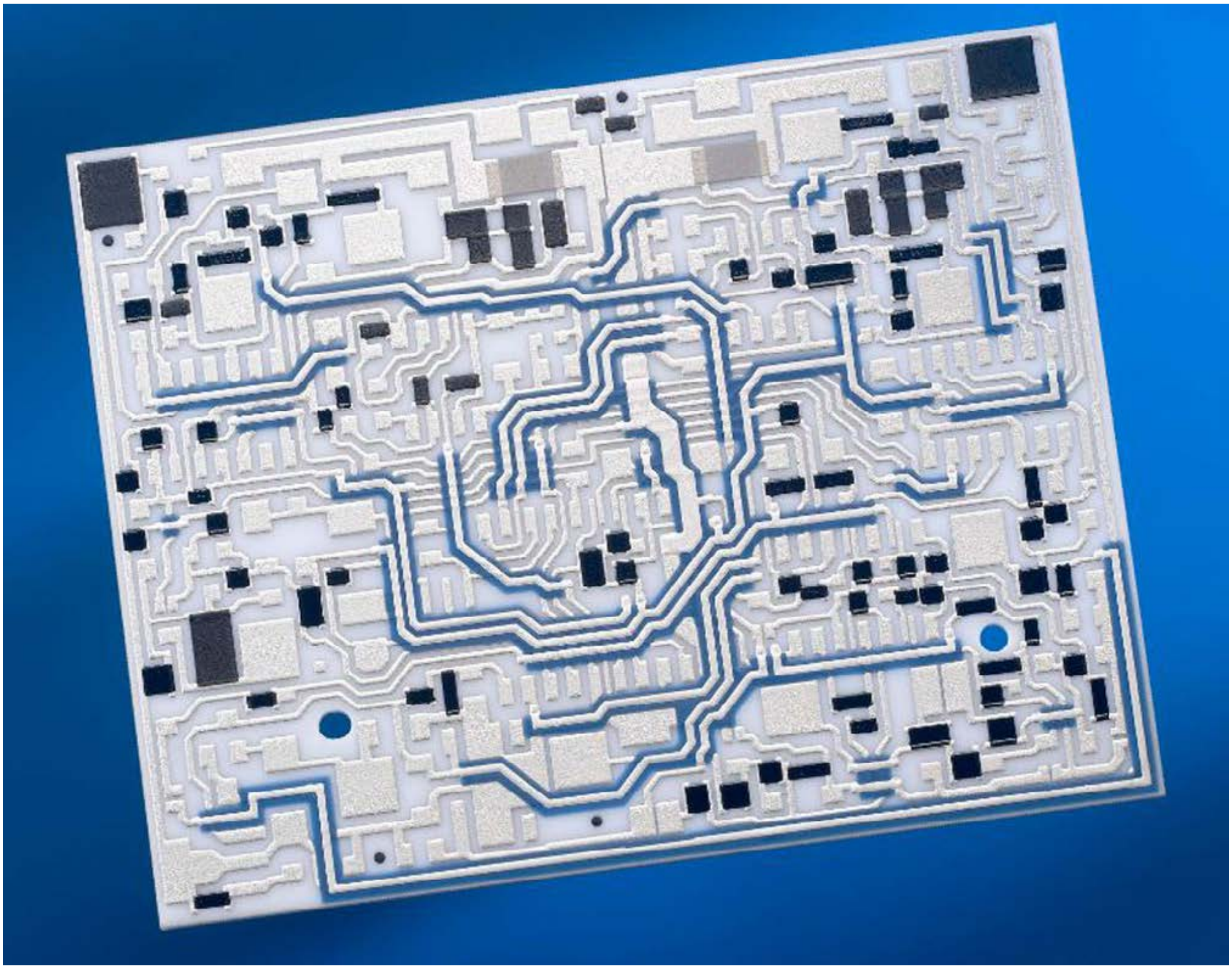


Figure 3: Silver/palladium silver and copper conductive paste materials are designed for hybrid circuits.

to find electronic components and parts, and the materials used in them, which can withstand these extreme temperatures that are increasing to 175°C and up to as high as 300°C.

The oil and gas drilling industry is also looking for materials that can withstand high-temperature applications. The trend in the drilling industry is to find material sets that can operate at temperatures of approximately 175°C and higher for extended time periods. In downhole drilling applications, electronic sensing devices are inserted in pipes that have been drilled into the earth. The temperatures in these pipes are extremely high, and the electronic sensing circuitry must be able to operate properly to send back the signals needed for the drilling operations.

Heat-Dissipating Solutions

Many power electronic circuits are built on a technology known as direct-bond copper (DBC), a sheet of alumina or aluminum nitride with a piece of copper film bonded to it through a thermal chemical process. Although DBC circuits are ideal for high-current applications, they do have some limitations. These limitations include substrate cracking and metallization peeling due to thermal mismatch between the substrate and copper layers resulting in thermal cycling reliability failures. This can affect the long-term reliability of the electronic device, especially in high-temperature applications. Design engineers are seeking solutions that can match the thermal expansion of cop-

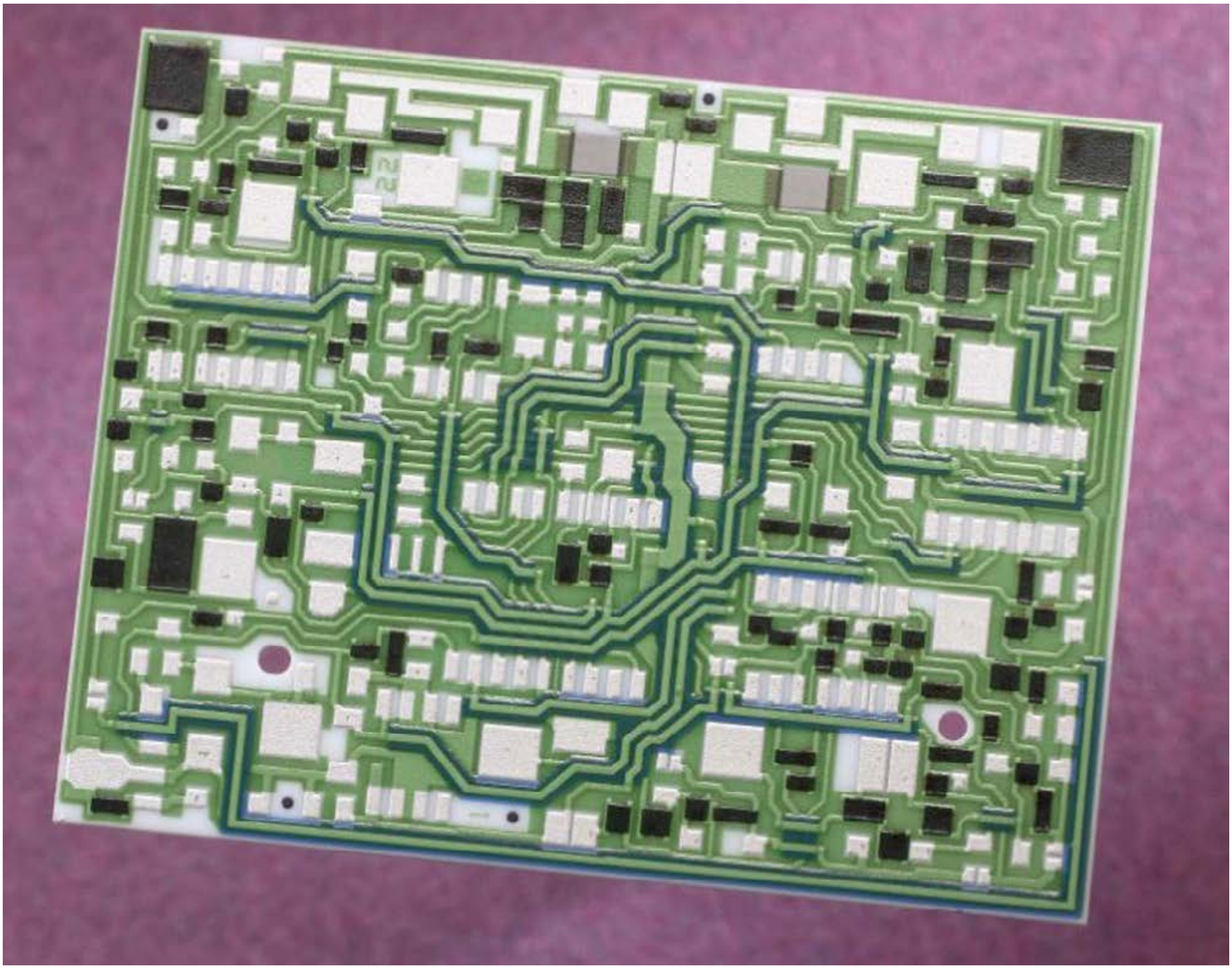


Figure 4: Thick-film hybrid circuits are made by screen printing thick-film paste onto a ceramic substrate; the paste is fired to produce an electrical circuit.

per and ceramic materials, and offer high reliability.

Among the products available for better thermal management of electronic circuitry are copper, silver and silver/palladium conductor pastes. For example, Heraeus' lead-free copper conductor system features a thick-film paste combination of metal, glass and ceramic to better match the ceramic substrate. The system is designed for applications involving high thermal and electrical properties, and allows the substrate to survive high-temperature-range thermal cycling requirements.

For decades, thick-film technology has been used to build robust electronic circuits on ceramic substrates for applications requiring high reliability such as in the automotive, military and aerospace markets. Some of these proven applications include engine control modules, and pressure and fuel level sensors for the automotive industry.

Alumina, used extensively in building electronic circuitry, can be problematic, especially when trying to keep circuits cool. Alumina does not have high-thermal conductivity; it is eight times less thermally conductive than aluminum nitride. Heraeus has developed several silver/palladium, silver and copper conductors which are screen printed onto the aluminum nitride to form the circuits.

The copper and silver thick-film conductors offer up to 300 µm fired conductor thickness, with excellent thermal, electrical, wire bonding, and soldering properties. They are compatible with standard 96-percent alumina and aluminum nitride substrates. By using the additive screen-printing deposition process, a single substrate can contain both thin-printed, dense circuitry for signal processing and thick-printed areas for power-device monitoring. The materials also allow through-hole connections for thermal and electrical connections on both sides of a substrate.

The improved bonding mechanisms of these thick-film pastes to the substrate, as opposed to thin film or direct bond copper, offer the advantage of increased thermal cycling and thermal shock performance.

Managing LEDs

As government mandates dictate the necessity for reducing lighting energy use, LED light bulbs are quickly becoming a viable, cost-efficient alternative to standard incandescent bulbs. Energy-efficient LED lighting products offer low-energy consumption and long service life in a compact size. LED light bulbs are finding acceptance not only in home use, but for high-power, high-brightness applications such as traffic lights, streetlamps and automotive headlights.

Thermal management is also a crucial component of LED lighting design. LEDs convert only 20–30% of their electric power into visible light. The excess energy is dissipated into the substrate as heat, allowing the bulb to run cooler for brighter light output and longer life expectancy. Although many LED configurations are built onto metal-core circuit boards (MCPBSs), better thermal management substrates are available.

Aluminum is a substrate that offers good thermal conductivity and is becoming more popular for LED design. However, aluminum requires an insulation layer on the substrate to isolate the circuit from ground. New products such as Celcion®, a thick-film materials system produced by Heraeus, are designed to insulate aluminum substrates.

As the trend to smaller and smaller electronic devices intensifies, thermal management of circuitry will become all the more essential. Smaller devices, with more circuits packed into tinier areas, translate to more heat generated and more heat that must be dissipated as the circuits get closer to each other. The challenge for the thermal management industry will be to continue developing materials and systems that allow electronic products to operate reliably in extreme high-temperature applications. **SMT**

Tips for Designing Thermal/Power Circuits

Designing thermal/power circuits can be challenging, especially when dealing with thermal management issues. Following these design tips can make the design process a bit easier:

- Closely matching the thermal expansion coefficients of the various materials used in a circuit is critical for long-term reliability
- Minimizing or eliminating thermal interfaces is key to minimizing thermal resistance
- Using the highest thermal conductivity materials possible also helps to minimize thermal resistance
- It is essential to use materials that can withstand high temperatures without degradation
- Thick-film materials can provide the solutions for these critical design issues

Mark Challingsworth is the technology director for Heraeus' Circuits and Components Business Unit within the Electronic Materials Division.

WHY CHOOSE US?

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Mil/Aero007 News Highlights

Saab to Acquire ThyssenKrupp, Inks MoU

ThyssenKrupp Industrial Solutions AG, a subsidiary of ThyssenKrupp AG, and Saab AB have signed a non-binding Memorandum of Understanding concerning the sale of the Swedish shipyard ThyssenKrupp Marine Systems AB (formerly named Kockums) with operations in Malmö, Karlskrona and Muskö, to Saab AB.

Celestica Earns Supplier Award from Rockwell Collins

The company was presented with the 2014 Assemblies Supplier of the Year Award from Rockwell Collins during the recent Annual Supplier Conference held in Cedar Rapids, Iowa. The award is an acknowledgement of significant contributions made during the year by suppliers and is based upon quality, delivery, total cost of ownership, lead time, and customer service.

Sypris' Electronics Group: 16% Revenue Increase in Q1

The company reported revenue of $84.2 million for the first quarter compared to $78.4 million for the first quarter of 2013. Revenue for the Electronics Group expanded 16% to $8.4 million in the first quarter, an increase of $1.1 million from $7.3 million in the comparable prior year quarter, primarily due to higher electronic manufacturing and engineering services revenue.

Ducommun Posts 2.2% Sales Increase in Q1

"The first quarter of 2014 showed the diversity of Ducommun's product portfolio and strength of our operating leverage," said Anthony J. Reardon, chairman and CEO. "Top line growth was driven by gains across our commercial aerospace business, including a further pickup in revenue with Airbus and on Boeing's 787 platform.

Digicom Electronics Earns ITAR Registration

"Our attention to quality and detail and our ability to handle low-volume, high-end products has enabled us to prototype and manufacture many military, aerospace, and government-related projects," explained GM Mo Ohady. "Receiving ITAR certification expands the base of projects we can accept and gives more flexibility to our customers."

OnCore Implements E2open's Supplier Collaboration Solution

OnCore Manufacturing, LLC, a global supplier of EMS, has implemented E2open's supplier collaboration solution. E2open enables OnCore to offer more effective customer service—given the real world of unpredictable demand.

Cal Quality to Support Boeing's CSEL Program

The company announced a multi-year, multi-million dollar contract signing with The Boeing Co. to support the Combat Survivor Evader Locater (CSEL), a major government program that is the U.S. Department of Defense Program of Record for Joint Search and Rescue. Cal Quality is providing manufacturing, assembly, and testing services to Boeing.

API Nets $1.6M Filter Solutions Order

"Our customers in the electronic warfare arena demand products that address a broad set of technical requirements with unparalleled performance and reliability," said Bel Lazar, president and CEO, API Technologies. "As a supplier to both emerging and existing EW platforms, our products are helping save the lives of warfighters from our armed forces and allies around the world every day."

Probe Order Backlog Rises to $3M; To Meet Target

Kam Mahdi, CEO, commented, "Our order backlog puts us in excellent position to meet our revenue target of 20% year-over-year growth by the end of 2014. We strongly believe that manufacturing for small to medium sized businesses is coming back to the U.S. We have witnessed businesses of this size become adversely affected by the subsequent increase in costs, unmanageable processes, and intellectual property protection concern of manufacturing abroad."

Nortech: Modest Growth in Q1; Continues Improvements

"We're pleased to see our pretax profits rise 13% on a slight sales increase," said Rich Wasielewski, president and CEO. "While the mixed economic recovery is impacting each of our customers differently, we continue focusing on improving our operating performance by managing the areas under our control and actively working on building a qualified sales pipeline."

The Trouble with BGA Solder Joints

by Thomas Wenzel and Andreas Türk
GOEPEL ELECTRONIC

The increasing density of modern assemblies imposes new requirements on the packaging technology, especially BGA housings. However, the terminals of those components escape physical probing and visual inspection. This gives rise to the question: How can technologists ensure the quality of solder joints with extremely reduced access?

All That Glitters is not Gold

The ever-progressing employment of surface mount technology (SMT) was further accelerated by the introduction of BGA housings in the mid-1980s. This package's terminals are solder balls on its bottom side. Compared to wired ICs, BGA technology provides many advantages, such as:

- smaller packages
- increased packaging density
- increased pin density
- improved signal transmission characteristics
- improved thermal linkage with the board.

The latest packages of this type, e.g., VFBGA (very fine BGA), permit several thousand pins and a pitch of less than 0.5 mm. BGAs are assembled in a soldering process with many influencing parameters. This process normally leads to a partly matte-finished solder joint, which has to meet various mechanical and electrical criteria:

- strong bonding between ball and board
- high mechanical long-term stability
- high structural integrity of the ball
- high conductivity
- high electrical signal integrity, and
- high insulation strength between neighbouring pins.

Even at this early point of discussion, the interaction between physical conditions and the resulting electrical properties is quite obvious.

Figure 1 shows a simplified illustration of the structural relationships. A static, oriented signal with simple ohmic resistors is assumed. The chip's internal conditions (wire bonding, etc.) are considered OK and thus not shown here.

During reflow, the solder of the balls and the solder paste will melt, and through a chemical reaction an intermetallic zone will be formed between molten solder and board surface. Another intermetallic zone exists between ball and chip. It is built up during manufacture of the BGA chip and must be checked by the BGA manufacturer. From an electrical point of view, the line resistance of the ball and the intermetallic zones is essential. Normally, the resistance between signal source and sink should remain stable in the milliohm range.

But all theory is grey, and in practice systematic and random errors occur and lead to heavily altered parameter values. Even shiny solder joints can't guarantee solder joint integrity.

Soldering defects arise from quality defects of the elements to be soldered, but also from deviating soldering profiles. The error patterns may differ widely. They range from visible deformations of the joint in the sense of insufficient or excess solder, where the electrical contact may be given, to visually perfect solder joints with random or even no contact.

With regard to evaluation of a BGA solder joint, the standard IPC-A-610E[1] plays an important role. It sets up acceptability requirements for electronic assemblies and identifies criteria for BGA components. In a production environment system solutions are necessary, which are capable of verifying compliance of the solder joints with that standard. This helps to avoid structurally unstable solder joints, which may break under mechanical load and lose electrical conductivity. It should be noted, however, that many defects, which are related to the form of the solder joint, will show electrical effects only under extreme conditions.

In contrast, failures in the intermetallic zone are particularly devilish and hard to recognise. "Head-in-pillow" and "black pad" are widely known phenomena of that kind. With the first effect, the solder doesn't fuse with the solder paste, so a sort of barrier layer will be build up. The visual appearance of the solder joint, however, normally doesn't reveal that. This effect is mainly caused by contamination of the ball surface.

On the other hand, black pad is more related to board issues. Here, the ball reacts with the solder paste, but below it, a layer is built up with reduced or entirely missing conductivity. This phenomenon is mainly caused by quality defects of the surface of the board's pads. Table 1 gives an overview of the fault categories discussed so far.

As Table 1 shows, there are a number of fault scenarios, and all of them must be controlled to ensure the required production quality. What's more, in practice the typical problems vary between different manufacturers, and sometimes

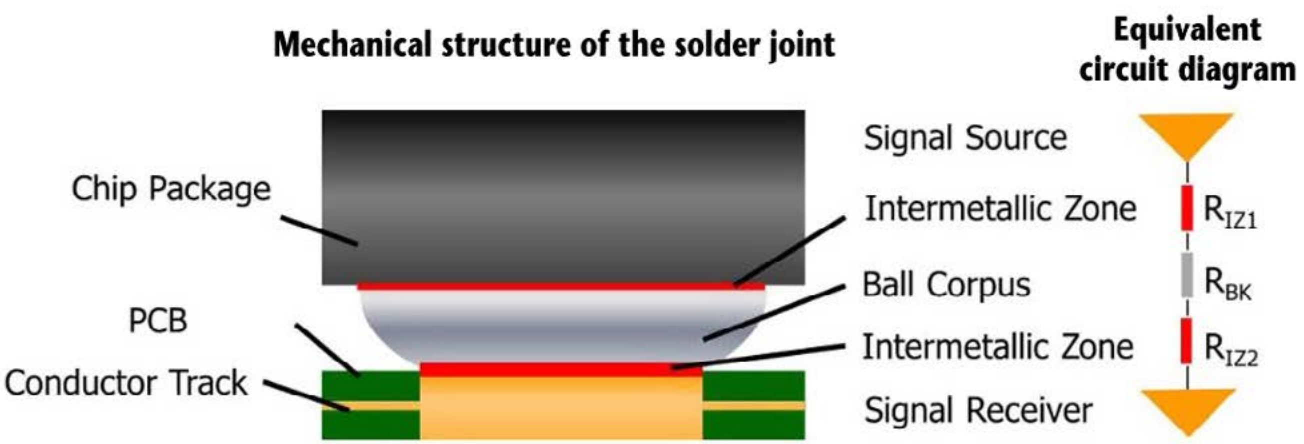


Figure 1: Static reference model illustrating corresponding mechanical and electrical design.

even between different products in the same production site. Possible faults in intermetallic zones with sporadic contact failure are an essential threat and may lead to catastrophic consequences for critical applications in, for example, automotive electronics. Depending on the respective situation, appropriate test equipment technologies should be used. But which technologies meet these requirements best and is there an ultimate strategy for quality assurance per se?

A Look Behind the Scenes

Test and inspection systems have two key strategic objectives. On the one hand, all production process faults shall be found, and on the other hand, each system acts as a process sensor in the required control loop of quality assurance. In practice, there are a number of different technologies available to meet this challenge; however, only a few are suitable for BGA solder joints. This is all the more true if an IPC-A-610-compliant production must be demonstrated.

Modern 3D inspection systems are capable of quantitatively measuring solder joints, whereas electrical test systems can only provide pass/fail information about the contact status. Table 2 lists the capabilities of various test/inspection methods with respect to essential test criteria and technical features. Methods include AOI (automated optical inspection), MXI (manual X-ray inspection), AXI (automated X-ray inspection), AXOI (automated X-ray/AOI inspection), boundary scan (IEEE1149.x), ICT (in-circuit test) and FPT (flying probe test).

It quickly becomes evident that no universal solution is available. Each technology aims at certain defect classes. MXI systems offer high-resolution in the lower micron range and thus are capable of detecting all mechanical defects. However, they are pure off-line machines and

Fault category	Mechanical/visual appearance	Electrical appearance	Potential cause of failure
faulty balls	- incorrect ball shape - incorrect area/size - voids - incorrect position - wrong ball pitch - poor coplanarity between chip and board	- R_{BK} hardly changed - $R_{BK}=\infty$ (open joint) - short circuit between balls	- BGA chip (ball) - solder paste quality - solder paste application - assembly offset - soldering profile - pad design
bonding weakness between ball and solder paste “head in pillow”	- correct ball shape - contamination layer between ball and solder paste - no mechanical strength	- $R_{IZ}=\infty$ (open joint) temporary contact due to mechanical loading	- BGA chip (ball) - solder paste quality - soldering profile
bonding weakness between solder joint and board “black pad”	- correct ball shape - contamination layer between ball and solder paste - cracks in the intermetallic zone - dark pad discolourations - low mechanical strength (tear off)	- $R_{IZ}=\infty$ (open joint) - temporary contact due to mechanical loading - R_{IZ} is in normal range, however connection tears off on loading (open joint)	- board quality - soldering profile

Table 1: Overview of typical fault categories of BGA solder joints.

Feature	AOI	MXI	AXI	AXOI	BScan	ICT	FPT
Qualification of the BGA chip (IPC-A-610E)	-	√*	√ [3D]	√ [3D]	-	-	-
Bonding weakness in intermetallic zones	-	√*	(√)	(√)	-	-	-
Co-planarity of the IC	√	-	(√)	√	-	-	-
Rotated IC	√	-	-	√	-	-	-
Conductivity of the solder joint	-	-	-	-	√	√	√
Defective el. driver/sensor	-	-	-	-	√	√	√
Access to traces via micro-miniature test points	-	-	-	-	√	-	√
No physical access to the trace	-	-	-	-	√	-	-
Adapterless operating principle	√	√	√	√	√	-	√
Full in-line speed	√*	-	√*	√*	√	√	-

√* system dependant (√) restricted by technology

Table 2: Performance of various technologies regarding identification of BGA faults.

can't be used for automated operation. Quite the opposite is valid for AXI systems. They are in-line-capable in principle and 3D machines can qualify according to IPC-A-610. Unfortunately, they have a lower resolution, so they have problems with detection of poor bonding in intermetallic zones. AXOI devices combine AXI and AOI into one system. So they are capable of putting down BGA solder joint defects to incorrectly placed chips.

In the field of electrical tests, physical contactability of traces plays an essential role for the applicability of those technologies. High-density BGA assemblies with completely embedded traces push long-term reliable test methods like ICT and FPT into an increasingly marginal role. The boundary scan test method is known as a groundbreaking alternative: it is standardised according to IEEE1149.x [2] and operates adapterless.

Based on the already discussed production test requirements for complex BGA assemblies, two technologies crystallise: X-ray systems (AXI and AXOI) and boundary scan systems for the electrical counterpart. Both methods will be discussed in more detail in the following. A complementary situation is assumed, because an electrical test yields no information on the mechanical status of the solder joint and an automated inspection of the solder joint doesn't guarantee an electrically perfect signal transmission.

Maxing Out the Potential of X-Ray

Even if in principle X-ray technology is capable of seeing the balls by taking a look through the BGA, this is a required technical prerequisite. The effective customer benefit is primarily defined through the technological

Figure 2: OptiCon X-Line 3D with integrated AOI option (AXOI).

device concept. In modern SMT production environments, X-ray systems are deployed in-line or as a standalone solution to perform fully automated X-ray inspection. Also the use of high-resolution manual or semi-automated X-ray devices (MXI) for sample analysis is widespread.

In sum, AXI systems for use with BGA assemblies in SMT production lines must meet some basic criteria:

- Full inspection according to IPC-A-610E
- Low fault slip
- Low false alarm rate
- Throughput matching the beat rate of the production line (in-line operation)
- Automated fault detection
- Simple programme generation
- Intuitive user interface
- Support of statistical process control (SPC)

Regarding BGA components, IPC-A-610E deals with criteria like solder ball offset, solder ball distance, solder ball form and voids in the solder joint. It is also associated with IPC-7095B[3], which specially deals with design and process development of BGAs. To check assemblies according to the requirements of IPC-A-610, tomosynthesis-based 3D AXI systems such as GOEPEL's OptiCon X-Line 3D[4] are particularly effective.

Figure 3 shows a solder ball and its vision evaluation. The images illustrate a cut through the centre level of the BGA balls. The evaluation yields results like ball area, roundness of the ball, position of the ball and its grey level. Here, the X-ray technology demonstrates its strength, delivering real measurement values. X-ray images show changes in the material itself, as well as changes in material density and thickness.

Voids are just an additional criterion of BGA ball integrity. They arise, amongst other things, during the reflow process, when the flux of the

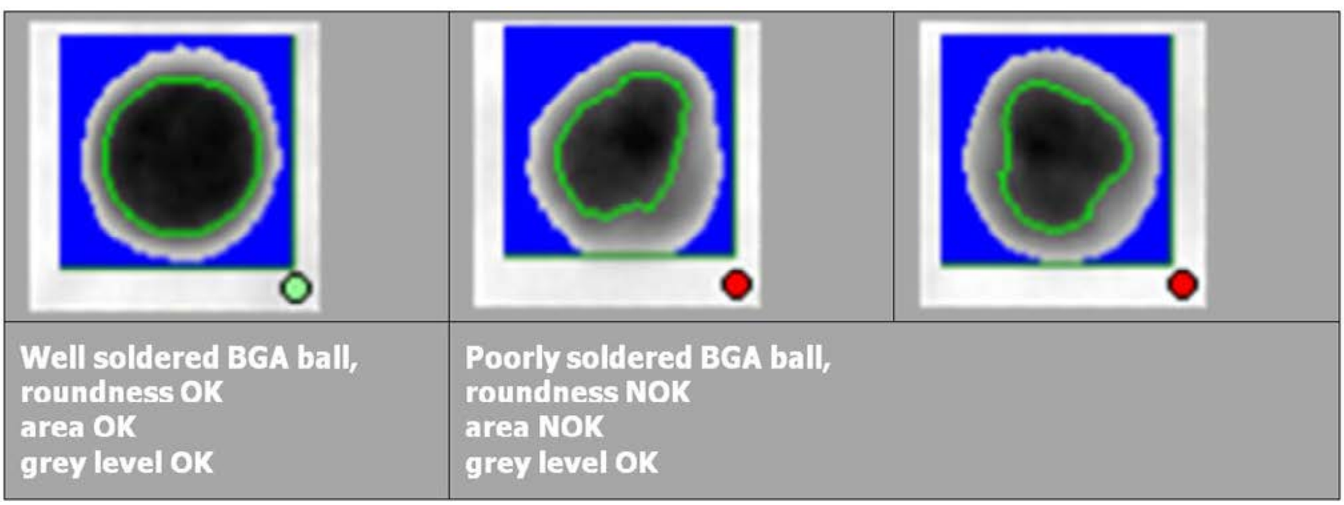


Figure 3: Measurement of good and poor solder joints.

solder paste is heated up and transferred into a gaseous state and gets entrapped by the solder of the ball. Voids may also originate from the board design, e.g., if any pads feature micro-vias. Size and number of voids depend mainly on the selected solder paste, the flux percentage and the chosen temperature curve of the reflow oven. The following example shows that also the amount of printed paste influences void generation.

Typically, during void checking, the void area (not the void volume) is determined. Mainly, the ratio between void area and ball area is calculated and given as a percentage. Assuming that voids take a spherical shape, the void volume can be calculated from the void area. In practice, however, this is rather atypical. The AXI system determines the void area in the centre level of the BGA balls. The image down left illustrates automatic void determination. IPC-A-610E sets the limit value for voiding at 25% of the total solder joint area.

As seen in Figure 5, not only can solder balls be evaluated with regard to shape, presence and voids. Even short circuits between solder balls can be detected.

Figure 5 also shows a tilted BGA. All balls have electrical contact and received a “pass” from the boundary scan test. The optical evaluation, however, unveils the tilting in the 3D X-

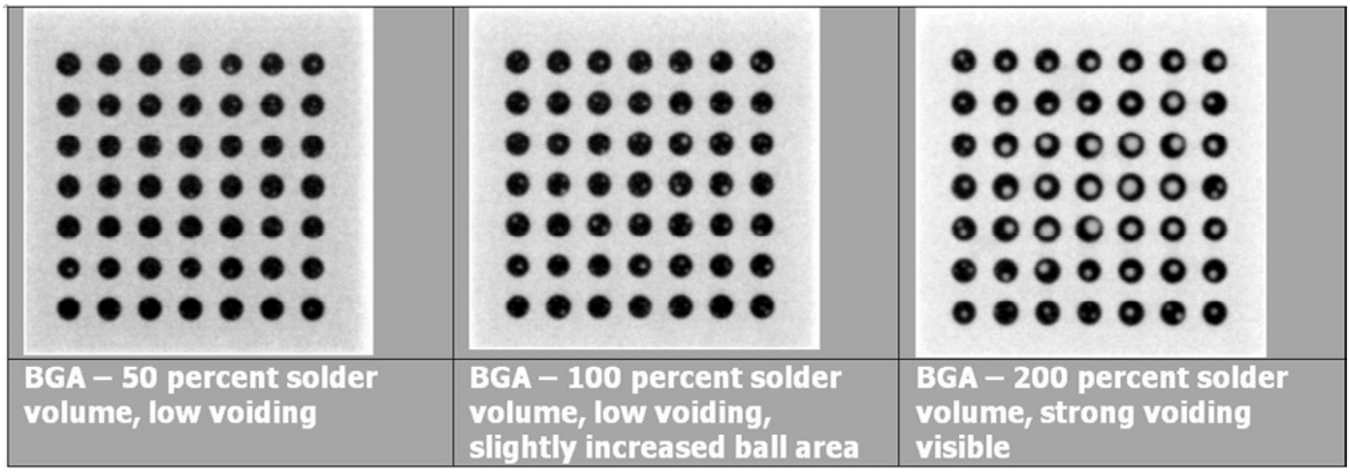


Figure 4: Illustration of voids.

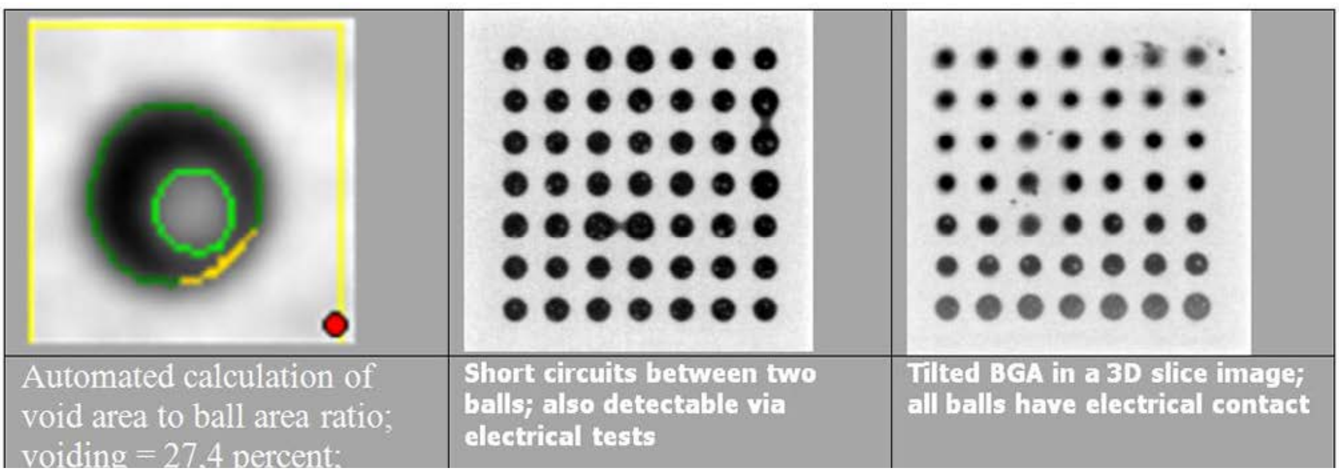
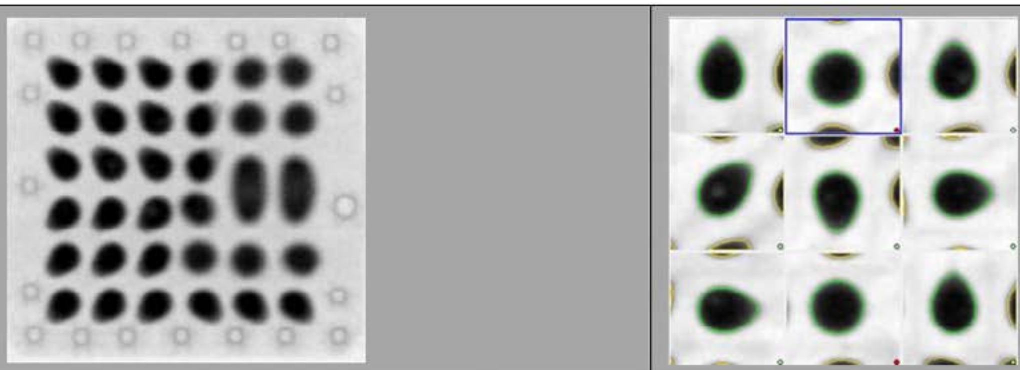


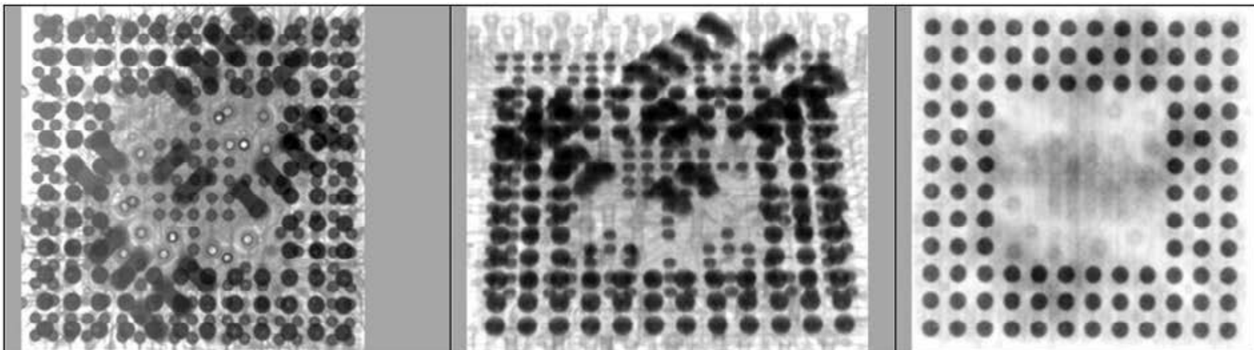
Figure 5: Illustration of voids, short circuits and non-co-planar BGA device.



X-ray image of a BGA with tear drop pad design; round solder shapes indicate a ball "resting" on a pad

Section from automated evaluation of BGA balls from figure 6. Balls from top and bottom position of the middle row are faulty and "rest" on the pad

Figure 6: "Resting" balls (head in pillow) visible due to tear drop pad design.



Vertical view (2D) using GOEPEL's semi-automatic X-ray system ScopeLine MX; superimposition of three assembly layers recognisable

Angled view (2.5D) using GOEPEL's semi-automatic X-ray system ScopeLine MX; superimposition of three assembly layers recognisable, first bottom row of balls evaluable

3D slice image of the middle layer using GOEPEL's OptiCon X-Line 3D. All rows of balls evaluable

Figure 7: Different radiographic views using 2D, 2.5D and 3D technologies.

ray image (slice plane = ball centre of the bottom row). This BGA will probably fail, if it will be mechanically or thermally loaded. Such tilting may be caused by wandering components that settled under the BGA.

The fault scenario of the head-in-pillow effects has already been discussed. One approach to evaluate this fault scenario in a safe and reproducible way would be to use the tear drop pad design. Here, terminal pads of the BGA are not round, but rather tear drop shaped. Figure 6 illustrates that in an X-ray image.

When a ball melts and fuses with the underlying solder paste, the typical tear drop shape will be visible. If the ball doesn't fuse with the solder paste, it will keep its circular shape and can be identified by parameters like roundness, axis ratio or ball area.

The tear drop design often cannot be used with smaller pitches. The tear shape decreases

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Figure 8: ScopeLine MX-1000 for semi-automated BGA analyses (MXI).

the distance between two pads and the minimal insulation clearances may be violated. Then the classical round pad layout must be chosen, which has to be considered when parameterising the X-ray test.

A sole evaluation of the solder joint according to its ball form is often insufficient for distinguishing between good and bad. In the case of single-sided assemblies, the transition between pad and solder ball can be evaluated using a high resolution 2.5D X-ray system. A visible necking-down would indicate a "resting" ball: the head in pillow situation. If, however, the assembly is populated on both sides or has even more than two soldering planes, this approach is somewhat problematic. The 2.5D X-ray image then shows strong superimpositions of the BGA with components from the other side. Figure 7 shows a board section with three soldering planes (TOP = capacitors, BOTTOM 1 = BGA_1, BOTTOM 2 = BGA_2).

Here, only a 3D X-ray system will provide a remedy.

GOEPEL's ScopeLine MX [5] is a semi-automated X-ray system for offline analysis.

Better Functionality without Nails

As an addition to X-ray inspection of complex BGA assemblies, boundary scan is the method of first choice. As opposed to classic in-circuit test physical nails are "moved" into the chips and become virtual nails (Figure 9).

This design-integrated test electronics is serially controlled via a test bus. The virtual nails are in fact boundary scan cells, arranged as a shift register (boundary scan register). The synchronous handling of the cells makes the electrical test of BGA solder joints a simple task. However, in the case of directed connections

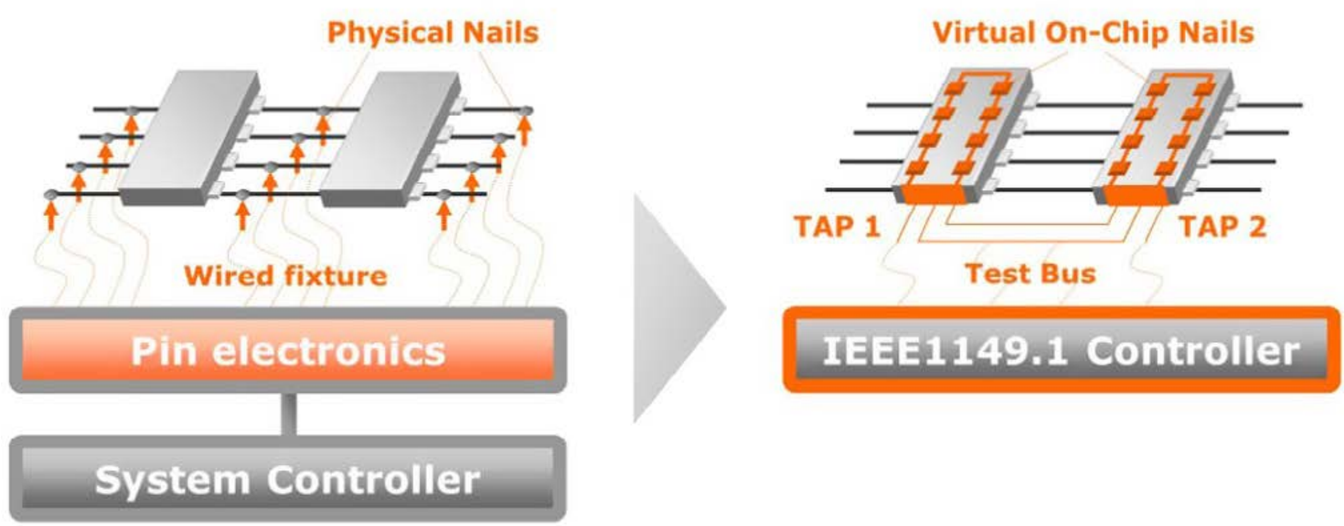

Figure 9: Transition to design-integrated test electronics.

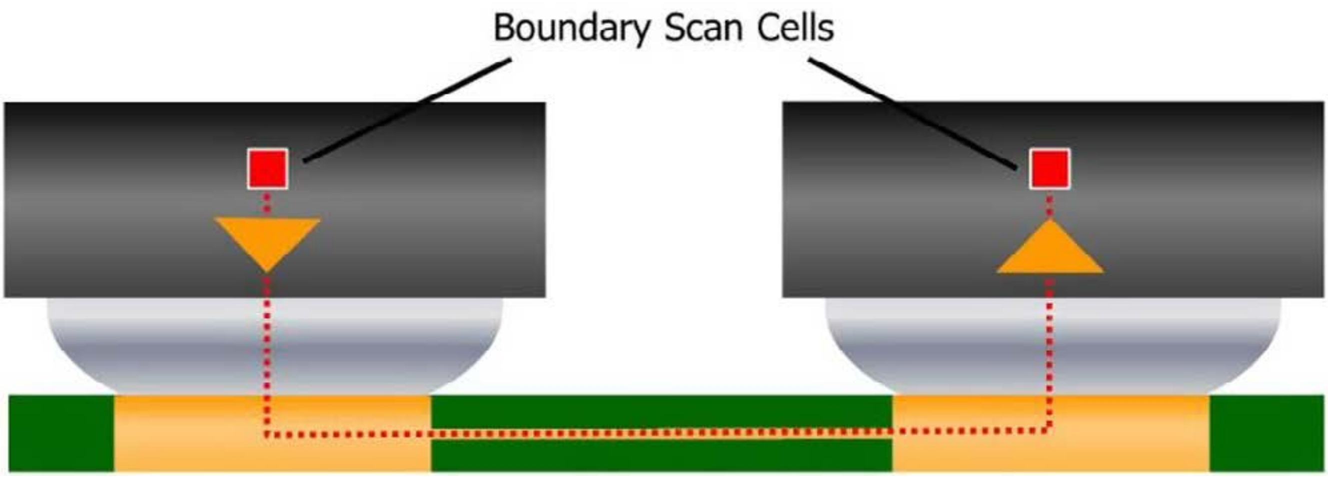

Figure 10: Connection test of two BGA pins per boundary scan.

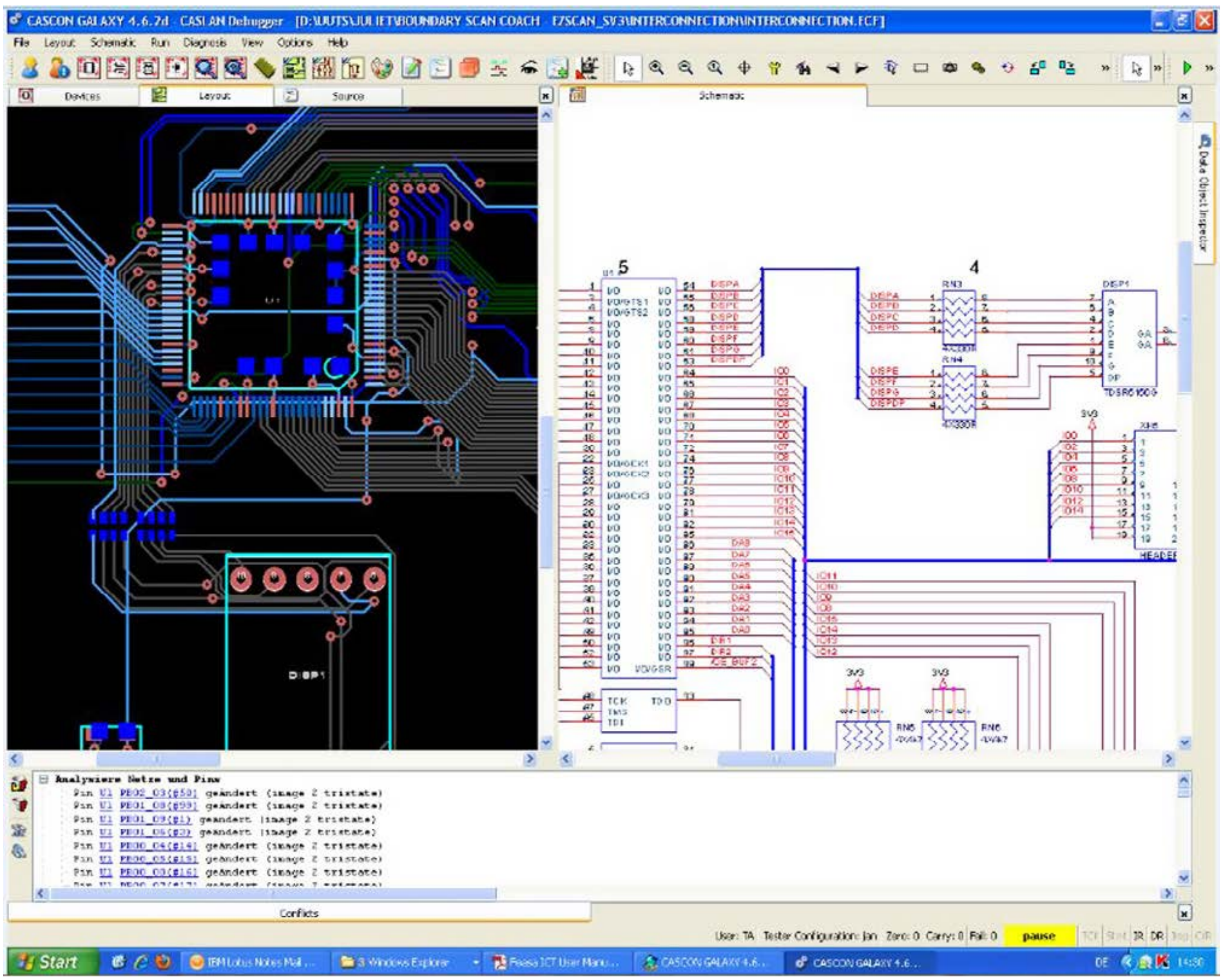

Figure 11: Representation of layout and schematics while running interactive pin toggling.

(Figure 10), the failure location can't be exactly nailed down. For that, an MXI-like method would be required.

Multipoint connections such as bus structures provide pin-level fault diagnostics. What's special about boundary scan is its high testing speed and its flexibility when it comes to prototype tests. Boundary scan is a structural procedure and, as such, independent from the chip's integrated functional logic. Finally, that means that each pin can be tested independently. So, this procedure can be ideally combined with stress testing, e.g., where thermal cycling in a climatic chamber tries to force bad solder joints to fail. But boundary scan also has its strengths in lab use. For rapid prototype verification designers often need to evaluate certain signals. For that purpose, graphical tools yield best results.

It not only features cross referencing between layout and schematics. Boundary scan cells can be activated by simply clicking on the respective pin. The resulting logic signal states are displayed using customer specific colour schemes.

Powerful in a Process Team

The very existence of the discussed technologies and system solutions isn't sufficient for a production with highest quality standards. The use of X-ray systems and Boundary Scan systems in the production of BGA assemblies requires a thorough analysis of the entire production situation. Accurate knowledge of the expected faults and their statistical distribution is of paramount importance. There are more than 100 parameters, which influence the definition of an optimised inspection and test strategy. So it is impossible, to name here the "ultimate" strategy. But one thing is certain: The combination of AXOI and boundary scan for BGA assemblies is capable of delivering a fault cover-

Figure 12: Components of the GOEPEL PicoTAP Designer Studio package.

age close to 100%. And the higher the percentage of BGAs, the higher the importance of these technologies. In today's situation, they seem to be the only solution for HDI assemblies. Figure 13 illustrates a possible production line for that situation.

The basic idea is, to install a sensor after each production process and to feedback statistical fault information to all process steps. Due to its high inspection speed, the AXOI system can qualify the assembly according to IPC-A-610E and measure, for example, the inner solder meniscus of TQFP components. The still missing mechanical fault coverage will be ensured by the integrated AOI system. The MXI machine is used for high precision analyses.

Summary and Conclusions

BGA components are an important part of complex board assemblies. They permit ever higher densities and improvements of electrical parameters. The steadily decreasing node access enforces appropriate countermeasures to be taken in the form of alternate inspection and test methods. In practice, particularly 3D AXOI machines (combined AXI/AOI systems) plus electrical Boundary Scan test methods have the greatest potential to solve those access issues. Both methods complement each other perfectly and permit a fault coverage for BGA solder joints of almost 100%. Furthermore, boundary scan has a fundamental future proofness, as it is based on progressive IEEE standardisation activities[9] [10].

Remember, the optimal use of the discussed system solutions requires a thorough analysis of the entire process. **SMT**

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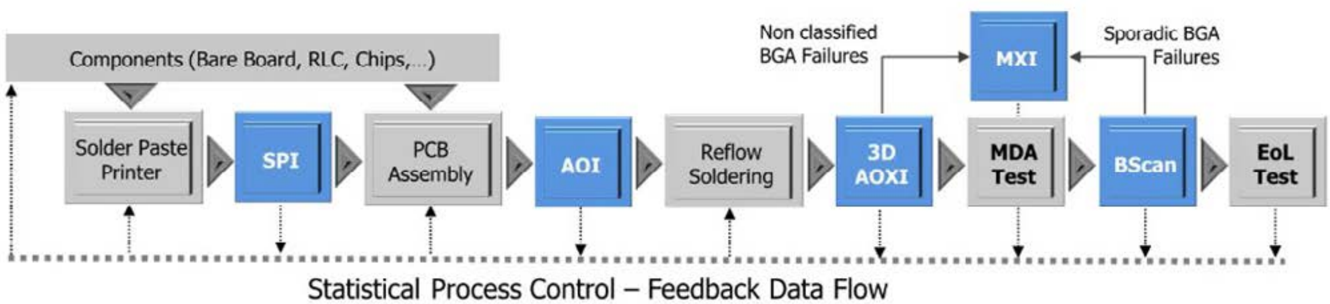


Figure 13: Example of the use of AXOI, MXI and boundary scan in a BGA assembly line.

SMTonline Supplier/New Product News Highlights

AIM Solder Develops NC520 No Clean Solder Pastes

NC520 is a no clean, halogen-free solder paste designed for the most demanding high-density electronic assemblies. It offers excellent wetting, improved printing, and reduced voiding. The solder's wetting ability results in bright, smooth, and shiny solder joints. Consistent transfer efficiencies reduce head-in-pillow defects even when component/substrate co-planarity is not optimal.

MYDATA Debuts New MY600 Jet Printer

"We're delighted to introduce this high-performance platform to customers struggling to mount difficult components using classic dispenser technology or screen printers," says Robert Gothner, senior VP and GM. "The MY600 is up to 10 times faster than a dispenser and, like its predecessor, shoots paste with high precision on the fly—something no one else can achieve."

Techspray Expands Cleaner Product Line

Techspray introduced two new defluxers into their Techspray Renew Eco-dFluxer inline and batch cleaner product line: Eco-dFluxer SMT200 and Eco-dFluxer SMT300. These new products offer increased cleaning performance, better metals compatibility, and reduced environmental impact.

Nordson ASYMTEK President to Join IPC SMEMA Council

Peter Bierhuis, president of Nordson ASYMTEK, has been invited to join the IPC Surface Mount Equipment Manufacturers Association Council (SMEMA). "I have been actively involved in the electronics industry for many years and have seen the valuable role that IPC and SMEMA play. I am looking forward to making whatever contribution I can to the group and the industry," said Beirhuis.

ACE to Acquire GPD Global's Lead Tinning Business

"This is a major step forward for our rapidly growing lead tinning business," said Alan Cable, president of ACE Production Technologies. "The acquisition will allow us to serve the GPD Global customer base providing them with world-class lead tinning support to improve their solderability, mitigate tin whiskers, and eliminate gold embrittlement."

Techspray Intros Fine-L-Kote AR Conformal Coating

Techspray expands their conformal coating offering with Fine-L-Kote High Viscosity AR. This new product is now a part of the company's Fine-L-Kote line, which includes a wide assortment acrylic, silicone, and urethane coatings.

Indium10.1 Offers Lowest Voiding Levels

Indium Corporation's Indium10.1 Solder Paste is a lead-free, halogen-containing solder paste with the lowest levels of voiding for QFNs, BGAs, and pads with large ground planes. The oxidation-inhibiting properties of Indium10.1 promote industry-leading head-in-pillow and graping resistance, with complete coalescence, even after long reflow profiles.

Dymax Releases New Selector Guide

From conformal coatings and encapsulants to edge-bond materials and display lamination, Dymax Corporation provides innovative, solvent-free, UV light-curing technology solutions for smart connected device assembly. The company offers many cost-reducing solutions that turn problems like shadowed areas, cure confirmation, and production throughput into non-issues.

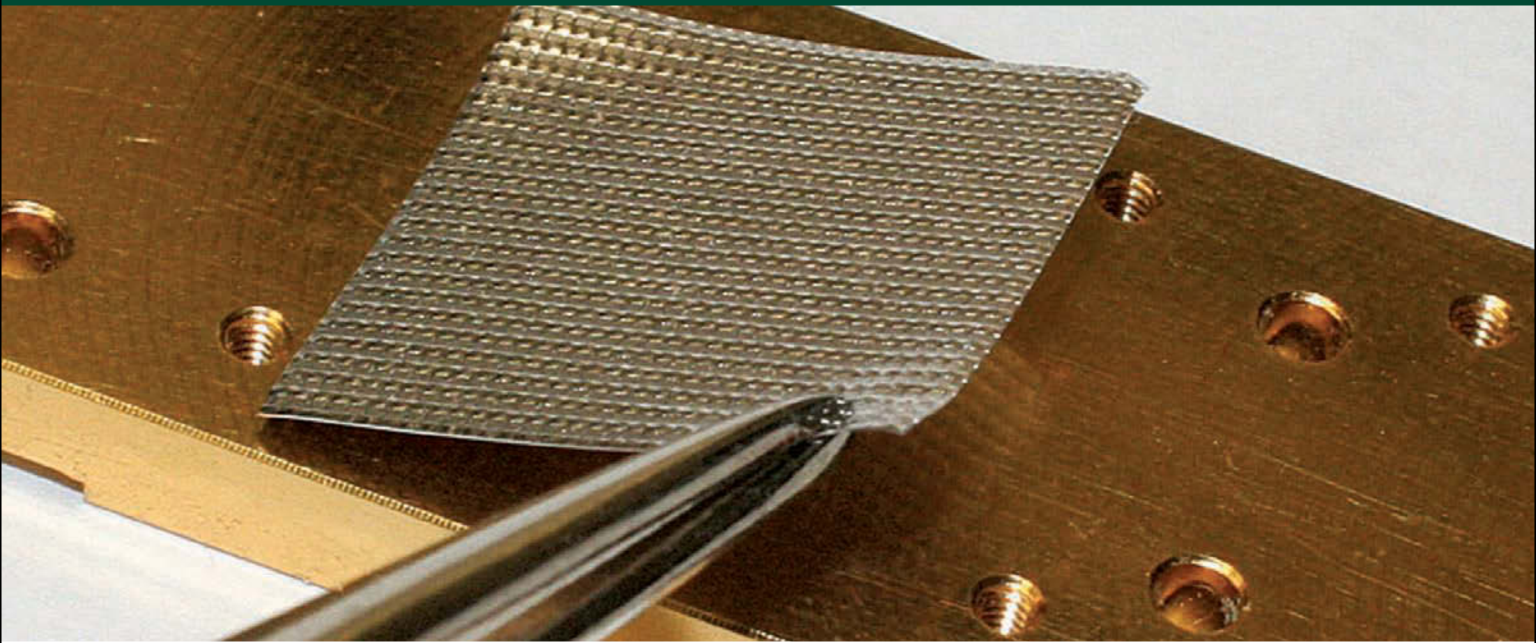
Agilent Technologies Achieves New Certification

Agilent Technologies Inc. has announced that the Agilent HDMI 2.0 test solution has been certified by the HDMI Forum as an official compliance test tool. The solution has the widest coverage for HDMI Physical layer compliance test. Certification was achieved with the collaborative framework of Panasonic; the solution will be used at the Panasonic Authorized Test Center, in Osaka, Japan.

Manncorp Enhances Dip Soldering; Debuts New Models

New models of Manncorp's popular Auto-Dip series include features that take dip soldering technology to new levels of performance and reliability. While dip soldering of through-hole components has long been an easy and affordable way to automate manual soldering processes when the costs of wave soldering cannot be justified, these latest enhancements increase quality and repeatability to a degree that make auto-dip systems ideal for virtually any short-run, batch application.

High Performance TIMs



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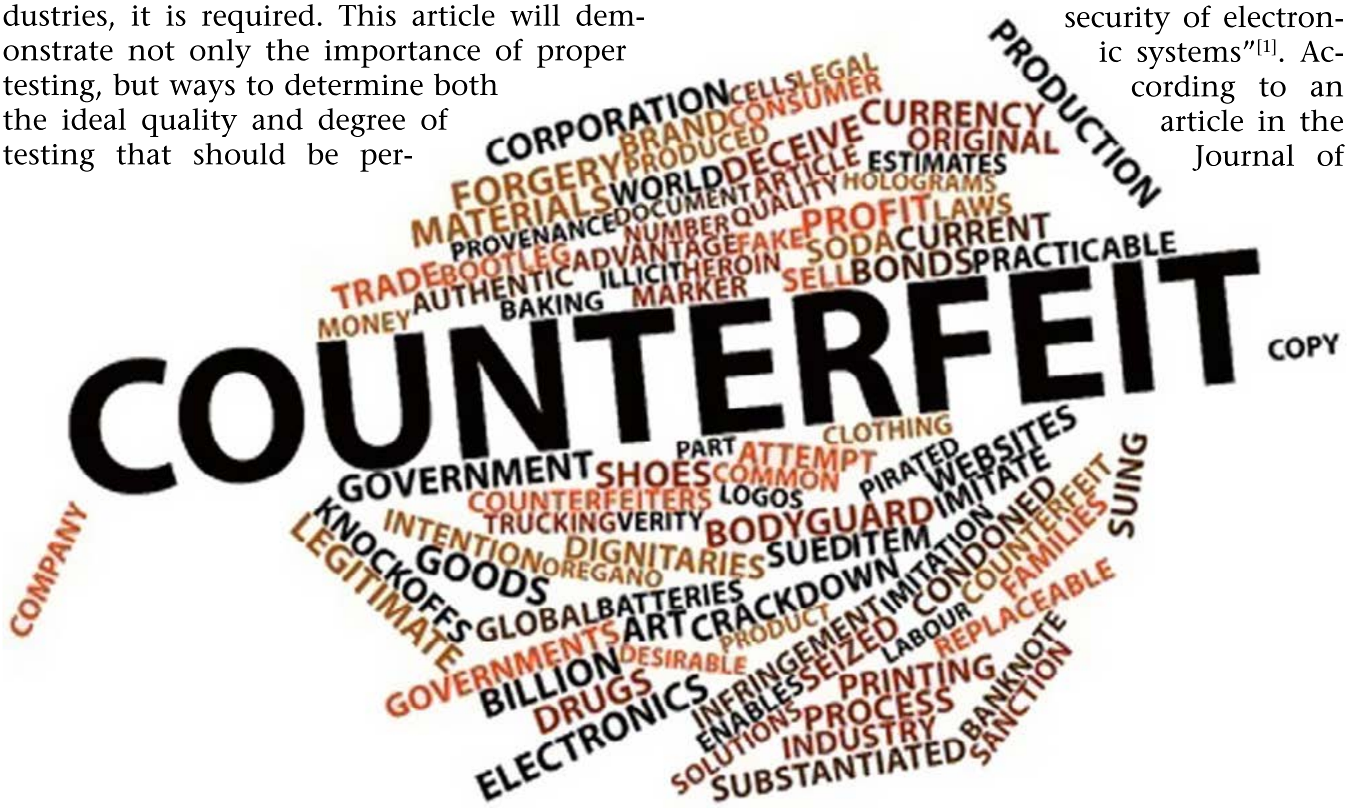
Determining Testing Requirements for Components from Unauthorized Sources

by Todd Kramer
SECURE COMPONENTS LLC

It is common knowledge in the electronics industry that counterfeit parts can cause serious, potentially fatal system failures. It is also known that the prevalence of counterfeits has increased to massive levels in the last decade. While there are numerous methods of alleviating this problem, most all of them are centered around some form of testing, which is meant to verify that the part is both legitimate and in the condition that the buyer believes it to be.

An additional reason to ensure that parts are adequately tested is liability. While no level of testing can guarantee that a part is absolutely authentic, fully functional, and is not a used or cloned part, showing supplier due diligence is vital when product that is not procured from an authorized source is used. In some environments, such as the aerospace and defense industries, it is required. This article will demonstrate not only the importance of proper testing, but ways to determine both the ideal quality and degree of testing that should be performed—and how to identify when you are receiving this quality.

Counterfeiting is a serious problem with massive negative effects—economic and otherwise. According to the International Chamber of Commerce, "The cost of counterfeiting and piracy for G20 nations is as much as $775 billion (USD) every year," as of 2008[1]. In the same report that brought this fact to light, the cost of counterfeiting to G20 nations was expected to grow to $1.7 trillion annually by 2015[1]. In addition to the ICC's report, a report issued by the Senate Armed Services Committee in 2012 indicated that there were over one million counterfeit components in the United States military supply chain. These were indicated by the report to be a major concern due to their "significant impact on reliability and security of electronic systems"[1]. According to an article in the Journal of



DETERMINING TESTING REQUIREMENTS *continues*

Electronic Testing entitled "Counterfeit Integrated Circuits: Detection, Avoidance, and the Challenges Ahead," there are seven main types of supply chain vulnerabilities to counterfeit electronics. These categories are:

- Recycled: used parts re-packaged and sold as new
- Remarked: parts on which the original markings are removed and replaced with a different part's information
- Overproduced: parts fabricated and sold outside of contract by untrusted facilities
- Out-of-Spec/Defective: parts that are known to be defective, but are sold as new
- Cloned: parts produced and sold by unauthorized organizations through either reverse engineering or illicitly acquired intellectual property
- Forged documentation: provision of illegitimate documentation for parts
- Tampered: a device which has been modified with the purpose of making it defective. This is usually done for malicious reasons such as sabotage, rather than for profit

As there is such a diversity of counterfeiting methods, it is easy to understand the fact that there are major challenges to the detection of counterfeits. This is where the importance of knowing that you are performing the right kind of testing, and to the proper degree, becomes evident.

There are two main types of testing: physical inspection and electrical inspection. Physical inspections include categories such as interior testing, exterior testing, and material analysis. Blacktop testing, marking permanency, and physical dimension evaluation are some examples of specific physical tests. Electrical inspection, on the other hand, is a term which encompasses parametric and functional testing, as well as burn-in and structural tests. It is common for parts to require both forms of testing—this should be taken into account when choosing a testing facility.

When seeking to keep counterfeits out of the supply chain, buyers and firms must ask two important questions:

- How do I know that I'm performing adequate testing?
- How do I find a good testing facility?

In order to determine the answers to these questions, it is helpful to use an industry benchmark. If the company seeking testing is certified to the SAE International AS5553-A standard, they should seek testing to the levels outlined in SAE AS6018, in accordance with AS5553-A. In fact, it is advisable for all firms to perform testing to the levels outlined in AS6081, as this standard is the most recent and most stringent anti-counterfeiting standard currently in existence, and has been approved by the United States Department of Defense. Another standard that clearly establishes uniform industry wide testing standards is MIL-STD-883. Additionally, SAE 6171 (Test Methods Standard: Counterfeit

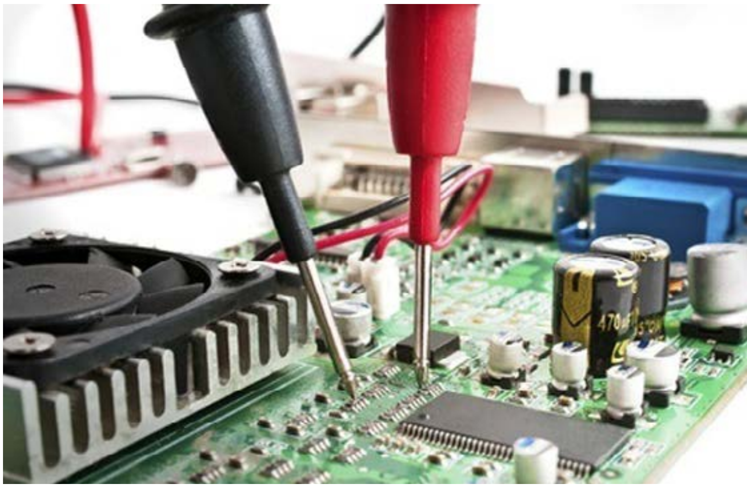
Electronic Parts), which was developed by the G-19A Test Laboratory Standards Development Committee provides excellent insight into the degree of testing which should be performed on electronic components. When determining appropriate levels of testing, all of these standards should be referenced and the processes within implemented whenever possible.

When searching for a test facility, it is important to keep in mind that there are many test facilities that offer a wide variety of testing levels. Some facilities are very high-tech and very expensive. Others are less expensive and less qualified, and therefore do not offer the same level of assurance. Ultimately, the main concern is determining what meets the appropriate level of quality for both your business's and your customers' requirements and quality flow downs.

A good testing facility will have the ability and expertise to perform testing to these standards. Key knowledge and abilities that testing facilities should have is also outlined in Annex 1 of ANAB Accreditation Rule 36, which includes items such as "knowledge of component design processes" and "knowledge of agency reporting requirements for fraudulent and/or counterfeit parts"[2]. Along with these capabilities, there is another major consideration that must be taken into account when choosing a test facility: transparency. When considering a test facility, these are some things that should be taken into account:

- How did you find them?
- Is their website completely stock photos? Does it truly represent the firm?
- Is the picture of the business really their office?
- Are the owners or management clearly identified?

These are all indicators of the level of transparency that a testing firm exhibits. This is an important consideration because firms that are unwilling to provide information about themselves are less likely to be forthcoming with information about the extent of testing and procedures used to determine the legitimacy of parts than transparent, up-front facilities.



In order to gauge a test house's level of transparency, ability, and general legitimacy, firms who wish to have testing performed on their parts should ask for certain things prior to entrusting parts to the test facility. Key questions to be asked include:

- Who is ultimately testing the parts?
- What are their qualifications?
- What are the consequences of a potential part failure?

In order to determine answers to these questions, certain requests should be made of the test house, such as:

- Sample comprehensive test report
- List of the lab's capabilities
- List of the lab's certifications
- Proof of successful third-party audits from government or other recognized organizations

Additionally, the consequences of a part failure on the component's end application should be thoroughly considered. A circuit card that will be used in a microwave oven, for example, will require less stringent testing than one which is destined for the control systems of a military aircraft. When determining which testing procedures should be utilized for a batch of parts, this should be taken into account. In addition to these considerations, the cost of testing oftentimes plays a part in choosing which test facility you will use.

DETERMINING TESTING REQUIREMENTS *continues*

From a broader perspective, everything related to the choice of testing facility is based on the risk assessment performed by your firm's engineering department and your customer. This risk assessment should also include the level of confidence in your source of supply and the proof that your supplier can provide of its supply chain traceability for the life of the component.

Ultimately, the potentially deadly consequences of part failure, combined with the growing counterfeit epidemic, necessitate sufficient and effective testing from qualified test facilities. The degree of testing is generally determined by the type of part and the end application, but is also influenced by international standards such as AS6081. In addition to these considerations, firms must also keep in mind the level of transparency and legitimacy that their test house provides, as these could be the difference between an accurate and useful test result, and a result which causes faulty components to be installed in an end application—possibly with catastrophic effects.

Clearly, in my business, I understand the need for testing and the costs associated with it that did not exist just a few years ago. One of the biggest challenges we face is educating clients on the value of additional testing costs. In order to best address this, I felt it was appropriate to gain some insight from Jesse Silverman, Esq., who serves as Secure Components' in-house counsel on counterfeit mitigation-related issues. I asked Silverman what his advice would be to a client looking to ensure they had performed adequate due diligence in their buying activity related to the testing of electronic components procured from "other than authorized" sources of supply.

Silverman had this to say: "If I were counseling a client on how to best avoid liability associated with incorporating a counterfeit part I would simply pose the question: If you are hauled into court to defend your procurement and testing methodologies are you confident that you could demonstrate best practices?" The penalties spelled out in Section 818 of FY2012 National Defense Authorization Act are quite severe:

- For an individual, not more than $2 million or imprisonment of not more than 10 years, or both, for a first offense and not more than $5 million or imprisonment not more than 20 years, or both for a second or subsequent offense.
- If a person other than an individual the fine shall be not more than $5 million for a first offense and not more than $15 million for a second or subsequent offense.

Silverman went on to express this: "With these penalties as the backdrop, I would again ask: Are you confident that if called upon in a court of law that you can demonstrate that you exercised best procurement and testing practices? In order to answer this question in the affirmative you need to demonstrate that you procured parts from the original manufacturer, an authorized dealer or a trusted supplier. Absent a clear definition of "trusted supplier," you should perform due diligence on your supplier base and determine which ones you would have complete confidence in should you be dragged into court and asked to explain how, and from whom, you procured parts. Similarly, your selection and vetting of a test house should be just as robust and vigorous."

I believe Silverman's advice on this matter should be well considered by those in the industry who are currently not ensuring that their Counterfeit Avoidance Plan includes a comprehensive testing protocol and partner. I am reminded of the advice we often give to our prospective clients who resist the idea that testing electronic components is essential in today's market, and claim it is too expensive and to do so would remove their ability to be competitive: Price is what you pay today, while cost is what you will live with every day after.

Do not allow your organization to become a victim of the counterfeiters. Understand the need and the value that your firm can gain from investing in a policy that demands a testing protocol. Create a sales plan that is a tool used by your team to establish a client base who demands a quality product. This investment will protect you and your customer from exposure to criminals who are profiting from those organizations that simply refuse to understand the realities of the current global electronic component marketplace. The benefits of a comprehensive test report last forever and demonstrate your commitment to quality. **SMT**

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Todd Kramer is CEO of Secure Components LLC, an AS6081 & AS9120 certified independent distributor of electronic and mechanical components to the aerospace, defense, and high-reliability industries. To contact Kramer or to read past columns, click here.

Video Interview

IPC APEX EXPO Show Wrap-up

by Real Time with... IPC APEX EXPO 2014

How was the show? Moderator Pete Starkey and guests discuss the 2014 IPC APEX EXPO, held at Mandalay Bay in Las Vegas. Guests include Michael Weinhold of the EIPC, Dan Feinberg of P. Kay Metal, and Joe Fjelstad of Verdant Electronics.

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SMTonline Market News Highlights

Employment Gains Buoyed by Professional & Business Services

In April, the unemployment rate fell from 6.7% to 6.3%, and the number of unemployed persons, at 9.8 million, decreased by 733,000. Both measures had shown little movement over the prior four months. Over the year, the unemployment rate and the number of unemployed persons declined by 1.2% and 1.9 million, respectively.

Wearable Electronics to be a $70B Business in 2024

Wearable electronics is a fragmented industry when it comes to manufacturers. Even mature sub-sectors have no clear leaders in what will be a $70 billion-plus business in 2024 with 12,000 developers and manufacturers, as recently calculated by analysts IDTechEx.

Global Smartphone Shipments Reach 267M Units in 1Q14

"The Q1 momentum came mostly from the emerging market sectors and China," noted Avril Wu, assistant vice president of TrendForce. "The Chinese smartphone manufacturers' increased 4G smartphone production is key to the smartphone industry higher than anticipated Q1 growth."

Eco-friendly Electronics Drives PE Market Growth

Analysts forecast the global printed electronics market to grow at a CAGR of 20.6% over the period 2013–2018. One of the key factors contributing to this market growth is the increased need for eco-friendly electronics products. The market has also witnessed the miniaturization of electronics devices. However, a lack of technology standards could pose a challenge to growth.

What's Driving the Global Diagnostic Imaging Market?

Some factors, such as increasing investments and funds by government bodies worldwide, investments by public-private partnerships, increasing number of diagnostic procedures and diagnostic centers, rising number of cancer patients, and technological advancements, are driving the global diagnostic imaging market.

Wireless M2M Devices to See CAGR of 21.4%

According to a new research report from the analyst firm Berg Insight, the number of devices with cellular or satellite connectivity deployed in oil and gas applications worldwide was 423,000 at the end of 2013. Growing at a compound annual growth rate (CAGR) of 21.4%, this number is expected to reach 1.12 million by 2018.

China Plays Vital Role in U.S. Economy; Exports Hit $120B

"Exports to China play an essential role in the U.S. economy and job growth," said USCBC President John Frisbie. "With China's large population, rapidly growing middle class, and a long list of economic development goals, American companies of all sizes are sending a variety goods and products to an ever-growing consumer and business marketplace in China."

Small Business Owners Optimistic About Growth in 2014

In a survey of small and mid-sized business, the Pepperdine Private Capital Markets Project 2014 Economic Forecast shows that business owners are optimistic about growth opportunities, both nationally and personally, for the remainder of 2014.

PE Market to Reach $40.2 Billion by 2020

The printed electronics market is estimated to grow at a CAGR of 33.8% from 2014–2020. and it is estimated to reach $40.2 billion by 2020, according to a report published by MarketsandMarkets. Rising energy costs, coupled with climate change are driving the increase of renewable energy sources such as solar photovoltaic technologies. Thin-film photovoltaic cells are found in one of the major applications of printed electronics.

Global Semiconductor Industry Hits Record Sales in Q1

The Semiconductor Industry Association (SIA) announced that worldwide sales of semiconductors reached $78.47 billion during the first quarter of 2014, marking the industry's highest-ever first quarter sales. Global sales reached $26.16 billion for the month of March 2014, an increase of 11.4% from March 2013 when sales were $23.48 billion.

THE SHORT SCOOP

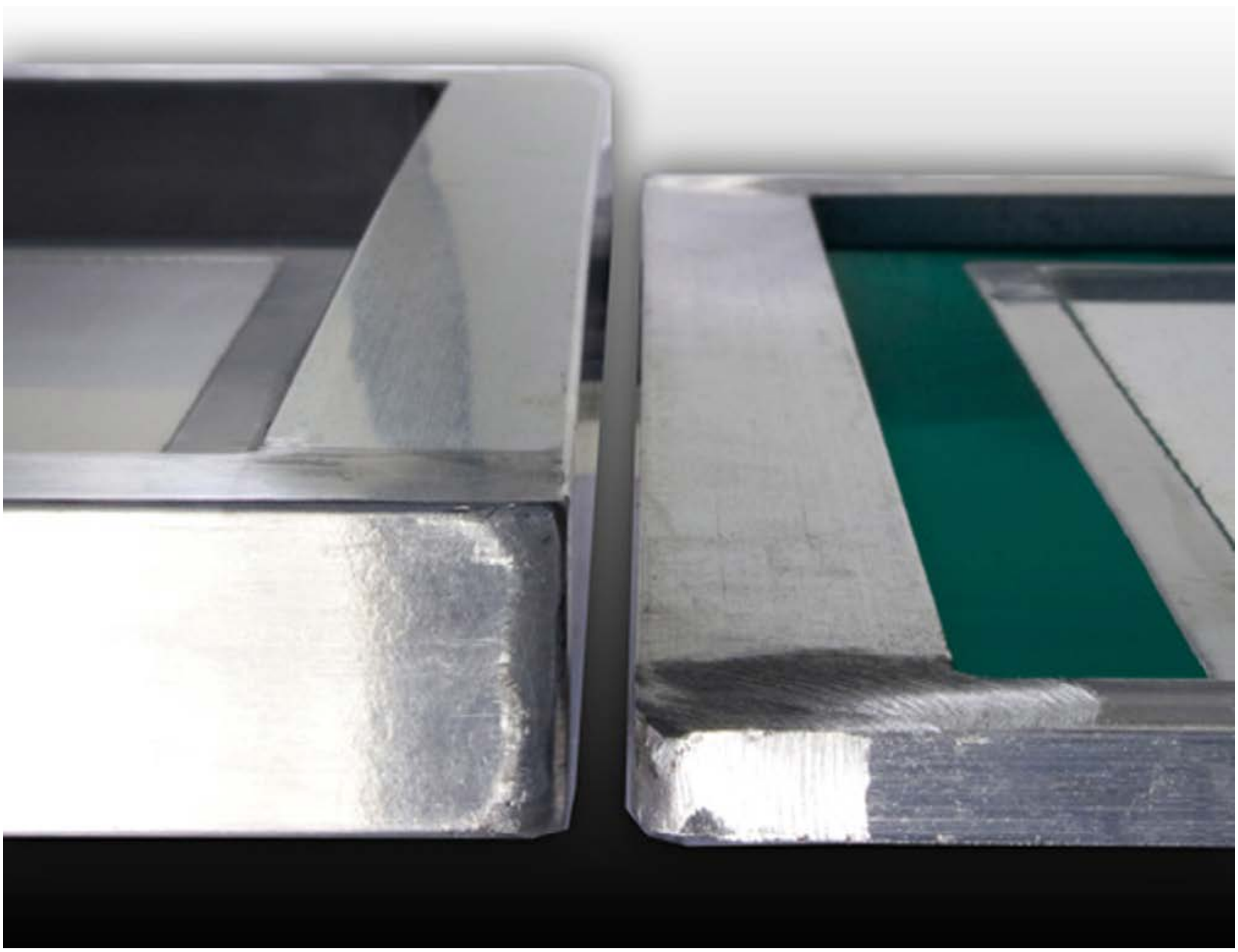
Selecting a Stencil Frame

by Rachel Miller-Short

If you have been following our Short Scoop series, you will recall that we have focused on different types of stencils and their applications and what to look for when selecting a stencil. We talked about the importance of the blade in the printing process, various stencil fabrication techniques, and specialty coatings that drive paste release, particularly for fine pitch components. Another part of stencil selection that is often overlooked, but that is also quite necessary, is the selection of the frame. This month's Short Scoop talks about the stencil frame and some of the options to consider when specifying the frame required for your printing process and needs.

What is a Frame?

For a stencil, the frame primarily provides a rigid support structure that allows the stencil to be used with your printing equipment. Without the frame, the stencil is no more than a thin foil with limited use due to the flexure of the stencil when left unsupported. The frame enables the foil to be stretched taut so that the stencil

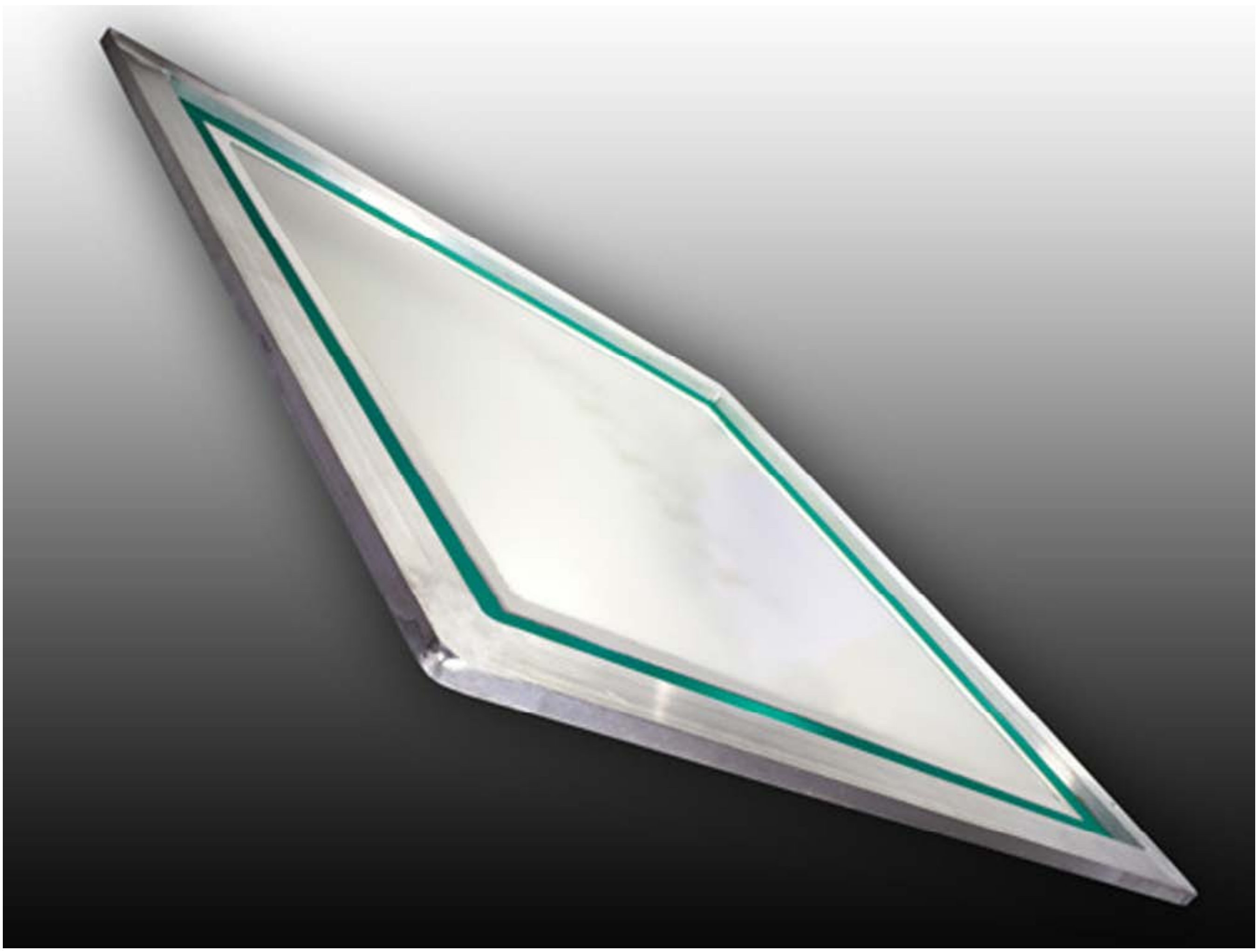


can gasket to the board, and thus solder paste will release properly from the stencil onto the circuit board.

Frames can range from large to small and thick to thin and be cast aluminum, welded aluminum, space-saving, or frameless systems, including VectorGuard™ and QTS. They can range from 8" x10" die cast (DC) frames to 29" x 29" tubular frames with many options in between. It is usually the printer type and printing equipment that determines the overall frame dimensions/size to be used. Besides choosing the frame type that fits your printer, there are additional options. Frames can usually be purchased either from the printer manufacturer or from the stencil manufacturer.

The overall size of a stencil frame is dictated largely by the size of the outside diameter of the stencil itself. Frame specifications should take into account the stencil's inside dimension, outside dimension, corner hole locations (if applicable), hole thread size, frame thickness, flat and parallel dimensions, and the maximum print area. If you have a lot of option variability with the printer you are using, make sure to pick a frame size large enough to accommodate the foil size (stencil size), the glue border to mount the foil, and allow an additional 2" square spacing around the outside of the image which is necessary to print successfully. It is perfectly acceptable to have more than a 2" square around the image area before the glue border starts, but successful printing usually cannot happen if the spacing is less. Sometimes, extra-large board sizes can cause a need for an oversized frame to be used. We can accommodate any size up to 70" x 102".

While there are multiple sizes of frames available, most frames fall into a few standard



sizes. Eighty percent of the frames that we fabricate fall into either the 29″ x 29″ (736 mm x 736 mm) or 23″ x 23″ (584.2 mm x 584.2 mm) size. The predominance of these standard sizes drives many stencil manufacturers to keep little or limited stock in other frame sizes. However, having additional sizes available offers options for those who can't use one of those two sizes. Purchasing from a company that can offer a selection of frames helps out considerably with lead time and cost when a non-standard format is required.

Space Saver Frames

While both standard and non-standard-sized frames that are purchased are usually tubular, there are also space saver frame options available. Space saver frames were designed to reduce the storage volume required for the stencil, yet they still provide the same functionality as a full size frame. The benefit of space saver options is that usually they are a simple plug-and-play option that helps save storage space as the number of retained stencils grows for many end-users. Space saver options include frames that are thinner than standard tubular frames as well as frameless systems that require adaptor frames for use in printers. These space saver frames are available to replace the normal 29″ x 29″ x 1.5″ thick frames used in most printing systems today with a frame that is .5″ (12.7 mm) thick. While some printing systems will accept these thinner frames with no modification, for those systems that must use a 1.5″ thick frame, a master frame with 2 locating pins that correspond to alignment holes in the space saver frame can be procured. This single master frame adapter is used with any space saver frame of the same size and allows for thickness compensation when specific printers will not handle the thinner frame. The benefit is that you will be able to store three times as many frames in the same area as you now store one conventional frame. The system is also available for 23″ x 23″ outside diameter frames. Once again, the space saver frame is .5%″, but the smaller format frame replaces the standard 1″ thick frame most common for this size. The 23″ system also can use a master frame to compensate the thickness. This cumulative space savings can be substantial, particularly if you are running a high mix of parts on your machine. It either allows a larger quantity of frames to be stored directly in the workspace or minimizes the space required so that processing areas can be compressed on the manufacturing floor.

Frameless Stencils

Another space savings option is the frameless stencil. Frameless stencils assist even more with space saving and, in many cases, they also help save money on the overall cost of procuring stencils. The additional savings for this type of frame system comes from a coupling of the lower cost for stencil manufacturing as well as cost savings for the shipping due to the reduced weight and volume of the stencil. The term "frameless" relates to the product as shipped, since a frame is still employed when the stencil is used to print an image. However, the stencil doesn't have to be delivered with the frame attached to it. Instead of the frame being integrated with the stencil foil by the fabricator, the stencil is attached to the frame and tensioned by the user. While the frameless system has tangible benefits, it will typically require some capital equipment investment.

One type of space saving stencil is the VectorGuard frameless stencil tensioning system. It delivers an end product capable of meeting all the diverse manufacturing requirements of a standard framed stencil. Relative to space savings and storage efficiency, this frameless stencil's protective cassettes reduce storage space by up to 75% when compared to conventional stencils, so the storage density in your facility is even greater than can be accomplished with other space saver frames.

The VectorGuard accepts a wide range of stencil foils and is available in the two predominate frame dimensions as well as several other popular sizes. Stencil foils between .003″ and .010″ are all acceptable for use. Mounting the stencil in the frame and tensioning it can be accomplished with minimal training and takes very little time to complete. With VectorGuard frames, the stencil is not shipped as a foil. Instead, the fabricator adheres molded plastic alignment corners and interlocking aluminum edge protection features to the stencil. This cassette provides protective edge safety features and attachment points for the frame to grab the stencil cassette when mounting and tensioning.

Another type of space-saving system is the QTS Wizard Stencil Stretch Frame System. The system has two frames and a stencil. The user can change stencils and tension them quickly using adaptable components and compressed air. The system is an innovative approach to stencil mounting, tensioning, and storage, designed to save time, costs, shipping, and waste. Both VectorGuard and QTS are reusable and recyclable frame technologies that prioritize operator safety so that hazards typically associated with an operator's handling of thin sharp foils is minimized.

Summary

Although selecting a frame is important, and there are several options that should be considered, if you have a reputable stencil manufacturer, the chances of choosing the wrong frame is slim. A quick review of the stencil size, coupled with the frame request and other details, are usually standard procedures for new stencil customers and on most orders. However, using the wrong frame can either directly affect the print and gasketing of the stencil or it will deem the stencil un-usable as it won't mount or fit into the printer.

Yes, the printing process truly is complex. The frame is an important consideration and one you should think about when you initially select your stencil. With a little forethought and some help from your printer or stencil manufacturer, you can look forward to a successful printing process. **SMT**

Rachel Short is vice president of sales and marketing at Photo Stencil LLC. She may be reached via E-mail, or by phone at 719-304-4224. To read past columns, click here.

THE ESSENTIAL PIONEER'S SURVIVAL GUIDE

Is It OK To Be Human?

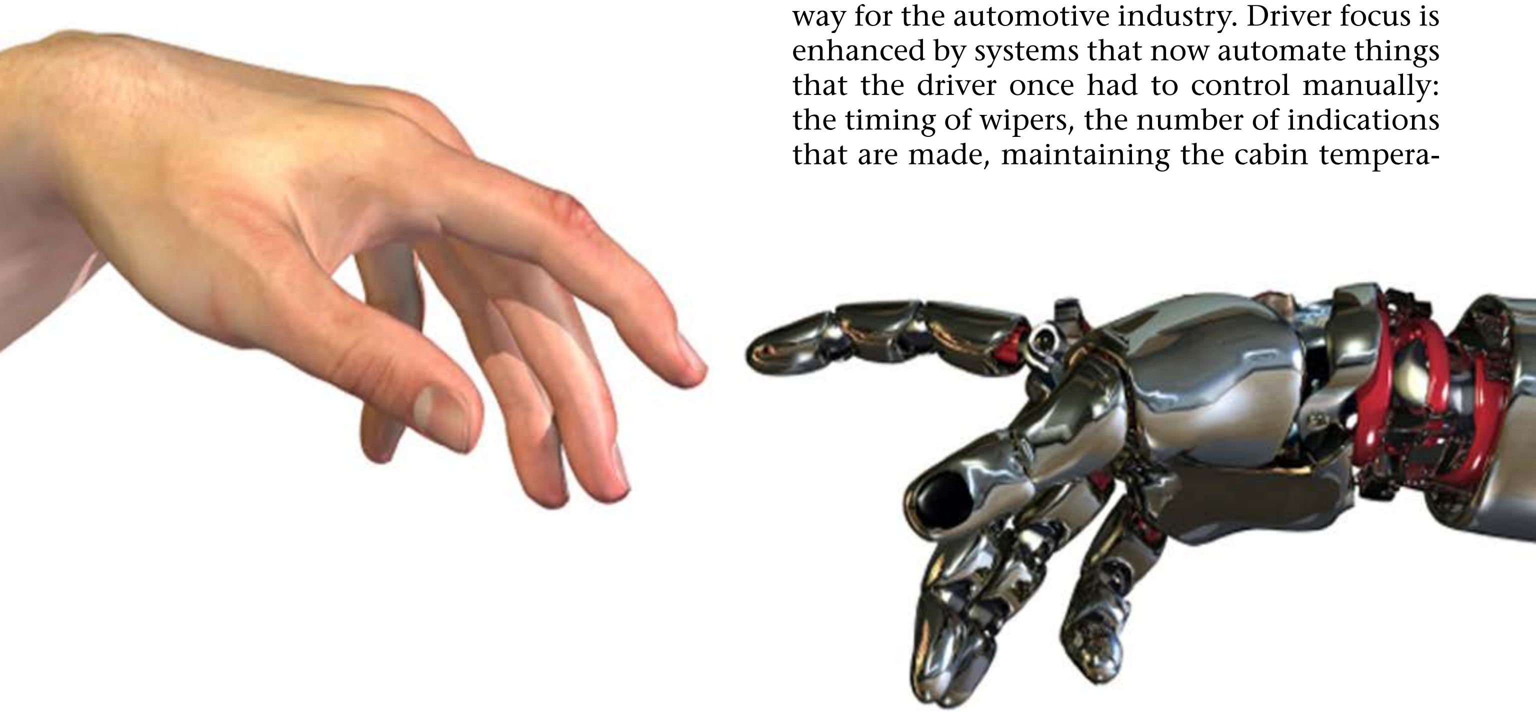
by Michael Ford
MENTOR GRAPHICS VALOR DIVISION

Automotive manufacturing once led the industry to build products of the highest quality at consumer-level competitive pricing. With the quantity and complexity of electronics increasing almost exponentially in automotive manufacturing, market quality issues, including recalls, continue apace, while the demand grows for a more modern manufacturing delivery profile that reflects the changing needs of the customer. After being stagnant for many years and adopting production principles based on process qualification and repeatability, can automotive find a new way forward, with quality assurance and cost competitiveness, but also with flexibility, which is most critical now? Is it the risk of human error that has prevented the industry from moving forward toward highly reactive processes, such as those mandated by Industry 4.0?

The Opportunity for Automotive

The automobile continues to enjoy a special position in the consumer market. For many people, a car is a necessity and represents a major part of their personal expenditure. This can easily be justified because a significant part of many people's lives are spent in the car, and this is the time when they are on view to the widest audience in society. The car has become a social vehicle, driven by fashion and personal desires, as well as by performance and costs. Car makers have provided buyers with many choices of models with a huge amount of variants and options. Buyers can effectively have the automaker build something that matches their precise wants and needs, and yet is affordable. For many high-end models, it can be rare to find any two cars with the exact same specification. For the factories, this means that every car made is, to a significant extent, built to order.

Technology has developed in a favourable way for the automotive industry. Driver focus is enhanced by systems that now automate things that the driver once had to control manually: the timing of wipers, the number of indications that are made, maintaining the cabin tempera-



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IPC & EIPC Design for Reliability and Design for Manufacturing — Best Practices

July 10
Conflict Minerals: Staying Current in a Changing Landscape
Santa Clara, CA, USA

August 20
Southeast Asia High Reliability Conference
Penang, Malaysia

September 28–October 2
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co-located with SMTA International
Rosemont, IL, USA

October 14–15
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Raleigh, NC, USA

November 18–20
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sponsored by IPC and SMTA
Schaumburg, IL, USA

November 19
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Bangkok, Thailand

December 3–5
International Printed Circuit and APEX South China Fair (HKPCA and IPC Show)
Shenzhen, China

More Information
www.ipc.org/events

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IS IT OK TO BE HUMAN? *continues*

Figure 1: Unseen logic now also manages almost every aspect of the engine operation and stability of the vehicle, controlling power delivery, suspension, and brakes.

ture, turning lights on and off, etc. Unseen logic now also manages almost every aspect of the engine operation and stability of the vehicle, controlling power delivery, suspension, and brakes. Light bulbs are monitored electronically to ensure that they will work when needed. Sophisticated navigation and communication systems are available on most cars, with a huge range of choice of entertainment systems. More recently, cameras and other sensors continuously scan around the car, providing features such as lane deviation alert, automated braking to avoid collision, and even features to allow cars to park themselves.

A great deal of effort is also going into energy conservation, such as recycling energy from the braking systems, turning engines off when stationary, etc. Cars that operate purely on electricity are also gaining momentum in the market, bringing in a whole new generation of electronics such as sophisticated safety features to protect the batteries, which contain huge amounts of stored energy, from harm. The whole environment into which these technologies are expected to work is extreme, with very high and low temperatures, humidity, vibration, and shock. Considerations must be made to ensure that should any faults occur, they can be self-diagnosed and bypassed to avoid extreme consequences.

In contrast to the recent downs and ups of the global economy generally, automotive electronicsis continuously expanding. The expansion has stimulated the move into automotive for many new and existing companies who have not previously worked in the automotive segment. They face a significant learning curve to understand the requirements and implement the necessary standards of operation required.

Legacy Automotive Practices

The reality for the manufacture of almost all complex products is that in many cases, the end manufacturers themselves are not the original source of the faults. Issues often lie with the providers of the many sub-assemblies, which can include dozens of individual microcomputer controllers of critical safety systems, which today are heading towards making up almost 40% of the value of a car. The automotive industry defined the original requirements for traceability, and they were extended to the suppliers of critical sub-assemblies. In their day, these led the way for much of the rest of the electronics manufacturing industry.

The solutions that were adopted, going back to the 1980s, still in common use today, were founded upon solid industrial engineering practices of the time. It was based on two key principles: qualification and traceability.

Qualification consists first of all on fully documented and planned procedures, materials, and operational practice. All possibility of variation is removed, eliminating all possible sources of variation and human error. Once the operations were fixed, the qualified manufacturing line would create sample products which then were rigorously life-tested, often taking several weeks, until there was a negligible risk of failure. Until this process was completed, no products could actually be made. The line could not ever be used for any other purpose and was effectively tied in and dedicated to producing the specific product to which it was assigned. There was no flexibility; the performance of the line had to meet the peak demand requirements, and at other times would run at a reduced productivity. Long-term commitment, determined by contractual agreement, would limit the variation in demand so as to allow a reasonable chance of profitability; but in doing so, it simply pushed the burden of dealing with fluctuation on to the car maker themselves. In many cases, the burden could not be shared, such as with Toyota in Japan, who would only accept sub-assemblies as needed.

> *"Qualification consists first of all on fully documented and planned procedures, materials, and operational practice. All possibility of variation is removed, eliminating all possible sources of variation and human error."*

The second principle that automotive adopted was traceability. The information technology available at the time was mainly paper based, written by humans. Although primitive, it was fully flexible and had little perceived cost. In reality, however, the small but frequent overhead for data recording, collating, and cross-referencing became a major burden. Paper does not suffer from issues related to digital data storage, but it does require significant space and very careful management. The storage of paper for traceability has yielded amazing stories over the years, including one case where a large manufacturing site, with a circumference of almost a kilometre, had two floors; the ground floor was SMT and assembly production, and the lower ground floor was simply an archive area for the paper traceability records. Fire risks meant that the air had to be replaced with nitrogen, except when people had to go "into the vaults" to find the paper trail of events where an issue had been discovered. It could take months to piece together all of the paper records to find the extent and scope of an issue that may be serious enough to trigger a recall event.

To industrial engineers working outside the automotive segment, these practices were far in advance of other areas, and seemed unacceptably restrictive. Consumer and other high-volume areas did not see the need for such qualification and traceability tasks, and they were deemed to be cost-prohibitive. At the highest end of the market, where budgets were more generous, volumes were very small, and so line qualification and dedication did not make sense. The emphasis was placed instead on preparation and testing. Only automotive electronics manufacturing companies found themselves in a safety-critical, high-quality, high-volume market combined with cut-throat cost-competitiveness.

Since the 1980s, information technology has moved on. Some attempts were made by automotive manufacturing to embrace new opportunities, but because of the immature nature of computing technology and harsh environment of manufacturing, the idea of having computers working live on the shop-floor, although appealing compared to the legacy practices, did not become widely accepted. Unreliable networks, computer crashes caused by memory leaks, home-grown software maintenance, data corruption, and sudden data losses all contributed to those who remained steadfastly attached to the older tried and tested working practices.

Automotive pretty much gave up on new technologies, a situation which persists to the present day, especially as vendors of surface mount machines failed to agree on standards for shop-floor data transfer, choosing instead to use it as a competitive tool. In general for the industry, this lack of useful shop-floor data has presented a huge barrier for major players such as ERP or MES to be able to provide specific shop-floor process-related support. Outside automotive, much of the rest of the industry was on a parallel path, with only a few key companies willing to be the early adopters of integrated information technology on to the manufacturing floor. So-called "point solutions," often provided by machine makers or developed internally within companies, came and went and continue to do so in the majority of the market.

"With opportunity fuelled by the growth in the market, automotive electronics are in the best position to once again take the lead to define the best practices for modern electronics manufacturing. However, to do this will require a significant change of the core operational practice."

With manufacturing so limited in terms of flexibility but with the customer having a freedom of choice in specifying the car variations that they want, a very sophisticated method evolved to predict and optimize the demand and supply of key electronic systems, such that suppliers can be kept productive and competitive prices maintained, while retaining the quality ethic. For many years, the automotive electronics business has had the reputation of being very high risk, both in terms of quality issues and also financially.

In only the last few years, however, as the trend for scope and complexity of electronics has continued to increase rapidly, car makers and suppliers have been put into a very difficult position. A necessary relaxation of the specific automotive manufacturing qualification has been inevitable, even though it is likely that such allowance opens up the scope of opportunity for defects to creep in and for human errors to occur.

Is it OK to be Human?

Millions of dollars lost in safety-related settlements would dictate that no allowances for error can be made. This specialized area of the electronics market can be responsible for significant loss of human life. Automotive electronics manufacturing has found itself in a position, in common to some extent with the rest of the industry, where something significant has to change. The legacy practices of process qualification need to be replaced with something that can provide the same degree of quality and reliability, which is at least as competitive, and has the flexibility to cope with the market needs. With opportunity fuelled by the growth in the market, automotive electronics are in the best position to once again take the lead to define the best practices for modern electronics manufacturing. However, to do this will require a significant change of the core operational practice.

It is 2014, After All

The information technology of today is a world away from the homegrown and commercial point solutions of the past. Hardware, software and operating systems have developed to become reliable for professional applications, even critical ones such as live manufacturing. Looking at how integrated solutions today work, spanning the entire process from design through to the final product shipment, it can seem that there is a very big step to take, especially for those who have stuck with only the kaizen style continuous incremental improvement philosophies for a significant time. The compelling event to drive the change has come in two parts. Firstly, the understanding that the current operational process will not be able to meet future business needs, and secondly that alternative solutions are now available, can practically be adopted, and the benefits obtained are very significant.

Back to Basics: Eliminate the Variation

The legacy automotive practices were formed on sound principles. Uncontrolled variation, as nicely defined by Six Sigma has always been the enemy of volume manufacturing. The new solution for manufacturing is one where variations have been removed while retaining or even promoting flexibility.

This starts with design, where the "perfect" design will have been qualified against the practical operational requirements of manufacturing, so as to ensure that manufacturing processes will run within their optimum capability, providing the best possible performance and yield. Manufacturing-driven design for manufacturing (DFM) systems can eliminate issues that would otherwise force manufacturing process compromise. A fully qualified product model can be delivered to manufacturing as a single complete object, for example, using the ODB++ file.

Today, the setup of manufacturing can be done within a single process preparation tool, taking the fully qualified product model and creating all the necessary engineering data for all of the different processes, all the way from initial surface mount to the final test, including all documentation for manual assembly, inspection, and repair. With software simulation of the machines operation and central library management, virtually all potential human error is avoided. Process setups, machine programs, and documentation can be specifically assigned to steps within work-orders to ensure that processes can only execute the intended operation, eliminating variation from data management.

The supply of materials can also be controlled, using the qualified process preparation setup data, ensuring that only the correct specific materials are used. The verification process provides confirmation and management for live material conditions such as moisture contamination. This ensures that no variation in the product will come from the use of any non-qualified materials.

The source of flexibility comes from the planning tool, which can work effectively only where changes can be made without significant cost or risk. Having confidence that any product can be prepared for any capable line configuration within its optimum operational parameters, without the need for line down-time, where only the correct version of the programs will be used, and only the correct selection of materials can be made, makes this possible.

The manufacturing operation can now change as often as required without the creation of variation that would trigger potential quality issues. Integrated intelligent software systems can today provide this level of control and assurance, while recording every event as process and material traceability, creating automatically an electronic build record for each individual product.

Of course, it is not only automotive that can benefit from this operational paradigm. In most sectors of electronics, flexibility while retaining performance and quality is an essential element for business success. The time has come for everyone to embrace what technology can really bring to manufacturing. **SMT**

Michael Ford is senior marketing development manager with Valor division of Mentor Graphics Corporation. To read past columns, or to contact the author, click here.

News Highlights from SMTonline this Month

1 "PERM Council Pb-free Research Priorities" Released by IPC

IPC's PERM Council has released a white paper identifying priority research areas regarding the impact and risks associated with the implementation of lead-free materials in electronics. The research areas include tin whisker failure modes and risk mitigation, complex systems logistics, and lead-free interconnections.

2 IPC APEX EXPO Panel Discussions: Don't Miss Them!

Exploring timely issues and cutting edge technology, these panels offer lively debate and unique perspectives on topics ranging from data file transfer formats to breakthroughs in flex circuitry—and so much more. In a small group setting, industry experts weigh in with their thoughts on business and technical issues that you won't see anywhere else.

3 SMTA Publishes Electronic Assembly Handbook

Chapter topics include soldering and materials, printed wiring boards, components, paste-print stencil, component placement, assembly line design and optimization, solder reflow, wave soldering, dispensing, and inspection and test. Each chapter outlines the fundamental attributes of critical assembly processes with full-color images and diagrams to illustrate real-world applications.

4 IPC APEX EXPO 2014 Concludes Successfully

In addition to experiencing a 14% increase in registrations to the technical programs and near-record participation levels in Standards Development Committee meetings, IPC APEX EXPO hosted a sold out exhibition: Four hundred forty-three exhibitors encompassing 137,700 net square feet—the largest exhibition in five years.

5 Varitron Expands Presence; Acquires Altronics

"Varitron and Altronics provide similar services, but also have complementary offerings intended for different markets," notes Michel Farley, president of Varitron Group. "By pooling our expertise, we will be able to serve more customers and to provide added value in terms of volume with the aim of consolidating the U.S. market and developing new niches."

6 Flextronics Aids Design & Manufacture of Jeep Cherokee

Flextronics announced that its Automotive Group has provided design and manufacturing services for the all-new 2014 Jeep Cherokee. Services provided include manufacturing and assembly of the daytime running lamps, remote start antenna, portions of the power lift-gate and sunroof modules and more.

7 Kitron Sees Q1 Revenue Increase; Takes Action to Improve

"While the increase in revenue was a positive aspect of this quarter, margins are suffering from price pressure and are clearly not satisfactory. Kitron is therefore taking action to improve profitability, as exemplified by the reorganisation of the sourcing operations and the downsizing of the Arendal operations," says Dag Songedal, interim CEO.

8 Benchmark Beats Estimates in Q1; Revenue Up 18%

"Benchmark again delivered strong performance, which allowed us to exceed our earnings expectations in the first quarter," noted Gayla J. Delly, president and CEO. "Our focus on growth opportunities in the non-traditional market sectors, coupled with operational excellence and enhanced customer solutions, resulted in improved year-over-year revenue and operating margins."

9 Kimball's EMS Unit Drives Q3 Sales; Spin-off Continues

"Our EMS segment continued to perform very well during the third quarter. We are confident in the strategic focus within both of our segments and that the investments we are making are balanced and appropriate for future growth and profitability in all of the markets we serve," says James C. Thyen, president and CEO.

10 Flextronics' Net Sales Up $2.5 Billion

"Fiscal 2014 marked a year of continuous improvement and execution," said Mike McNamara, CEO. "We consistently grew revenue, adjusted operating profit dollars, and adjusted EPS sequentially every quarter from our March trough a year ago through our December quarter."

EVENTS

For the IPC's Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar, click here.

For a complete listing, check out *SMT Magazine's* full events calendar here.

MEDTEC Europe 2014
June 3–5, 2014
Messe Stuttgart, Germany

RAPID Conference & Exposition
June 9–12, 2014
Detroit, Michigan, USA

IPC SE Asia Workshop on Soldering of Electronics Assemblies
June 9, 2014
Penang, Malaysia

MedTech MD&M East
June 9–12, 2014
New York, New York, USA

IEEE ICC 2014
June 10–14, 2014
Sydney, Australia

CES Unveiled Warsaw
June 17, 2014
Warsaw, Poland

Upper Midwest Expo & Tech Forum
June 18, 2014
Bloomington, Minnesota, USA

CE Week
June 23–27, 2014
New York, New York, USA

Symposium on Counterfeit Electronic Parts and Electronic Supply Chain
June 24–26, 2014
College Park, Maryland, USA

Ohio Expo & Tech Forum
July 17, 2014
Cleveland, Ohio, USA

SusTech 2014
July 24–26, 2014
Portland, Oregon, USA

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Tin Whiskers

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Assembly of Printed Electronics

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Automation