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Specialist Boundary-Scan
with ICT **p.18**

In-line Solder Penetration
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TEST & INSPECTION

High-Density Interconnect and Embedded Board Test

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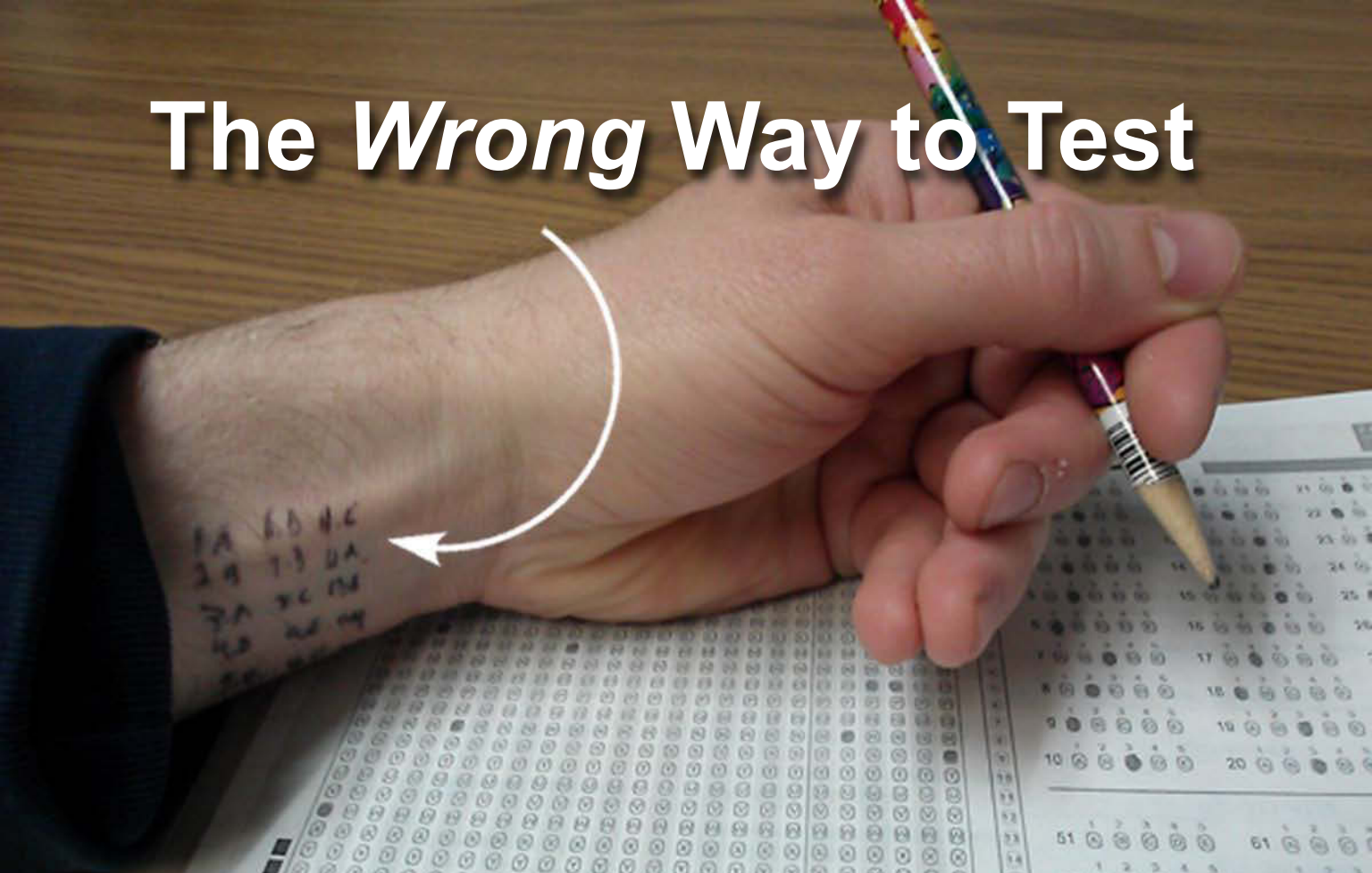


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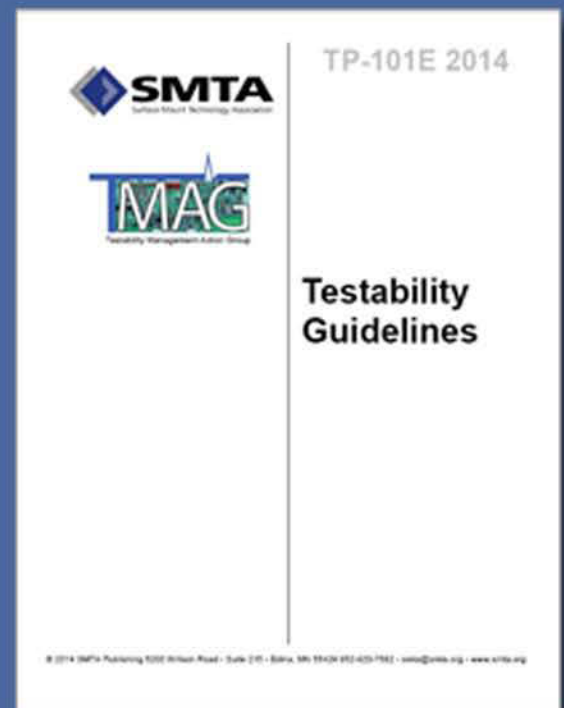
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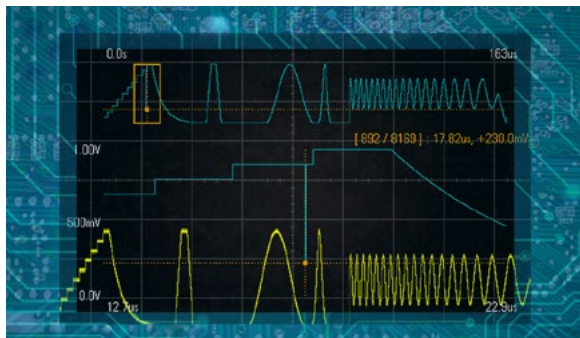
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TEST & INSPECTION

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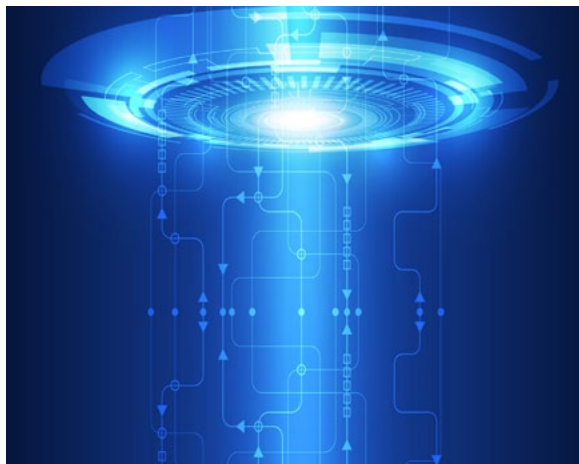
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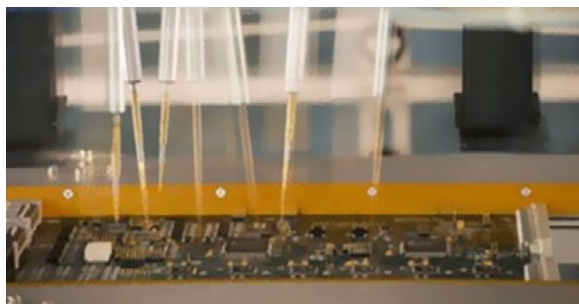
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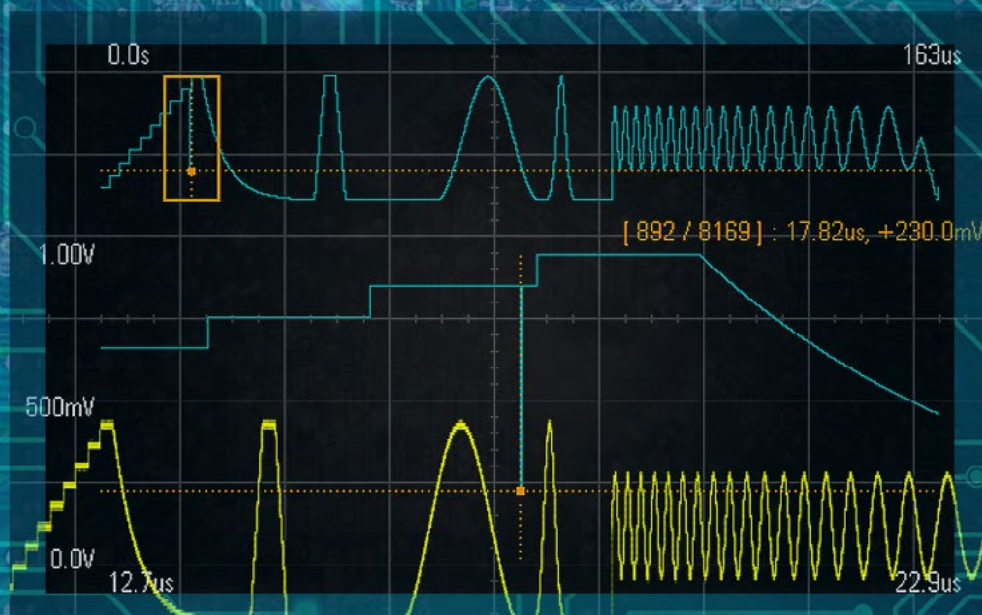
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High-Density Interconnect and Embedded Board Test

by **Mark Lau**

KEYSIGHT TECHNOLOGIES INC.

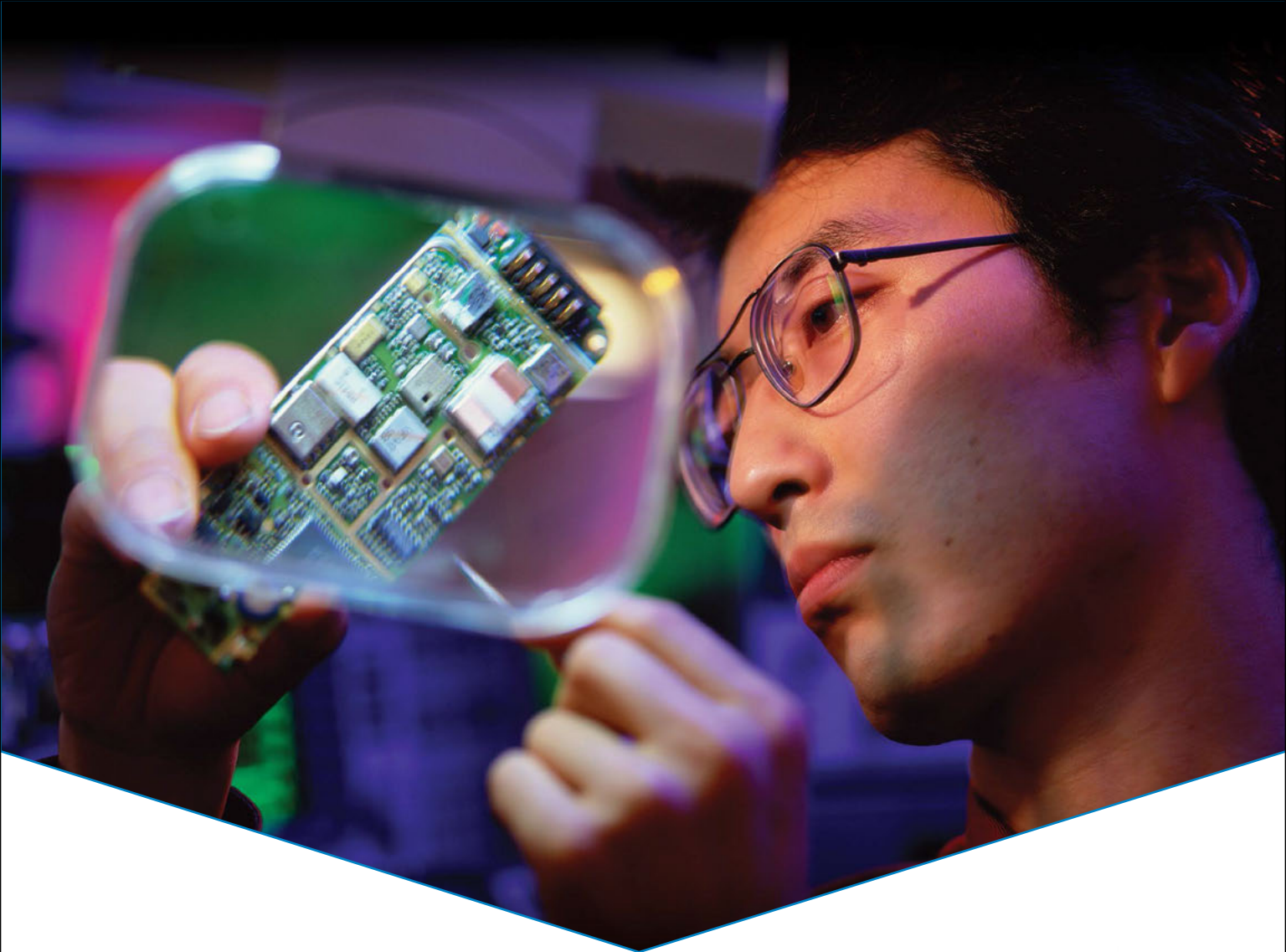
The printed circuit board assembly landscape is changing rapidly, driven primarily by handheld consumer devices. The highest-volume PCBA is the cell phone, which is understandable given that virtually everyone equips themselves with at least one such device to stay connected these days. More and more consumers want data connectivity, not just voice, and that has pushed telecommunication companies to switch from voice to data networks. In the process, server farms and data centers have sprung up around the world to support the data volume generated by the ever growing list of cell phone applications.

Cell phones and portable devices have now become the driver for electronics innovation and technology development. As an example, the need to stay connected every second of the day to instantly receive the latest news or up-

dates has prompted industry to pursue a way to bump up the cell phone's speed and turn down its power for longer battery life. Likewise, consumers' insatiable demand for feature-packed, thin, lightweight, and energy-efficient devices is spurring the need for HDI technology. It's an innovation that is now rippling through the electronics ecosystem—from semiconductor integrated circuits (ICs) to PCBs and SMT equipment.

An Industry Perspective

The semiconductor industry rose to the "more than Moore" challenge, downsizing 28 nm silicon nodes to 22 nm and now 14 nm to increase the speed and lower the energy consumption (watts) of devices. The primary beneficiary of this silicon node technology is the central processor unit, which also exists in the micro controller unit and when integrated with other electronic functions becomes system-on-chip (SoC). Innovations like through-silicon via (TSV) have enabled the creation of 3D integrat-



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HIGH-DENSITY INTERCONNECT AND EMBEDDED BOARD TEST *continues*

ed circuits (3D ICs) by connecting layers of different silicon dies stacked vertically, which can then be integrated into the smallest and densest SoC package. The stacked silicon die can be of the same technology, like DDR memories, or a SoC made up of different technologies or applications.

Figure 1 shows the upward trend of IC package pin counts. The declining average area per pin shown in the figure represents the increasing pin density of IC packages.

The silicon integration trend will reduce the size of the PCBA as more ICs get integrated into one dense IC package. The input-output (I/O) pin count for this dense IC package will be slightly less than the total I/O of all the combined ICs. IC packaging suppliers have increased the rows of solder balls on an array package like BGA to accommodate the demand for more I/O pins. Incrementing a row of solder balls in an array package can yield up to 25% additional I/O pins. Besides increasing the rows of solder balls, newer array packages have reduced the pitch between the solder balls from 0.5 to

0.4 mm. Packaging array trends show a growth of IC packages with 0.5 mm pitch and smaller, while the demand for IC packages greater than 0.5 mm pitch has stagnated. This is a sure sign that PCBA designers are switching to fine pitch array packages to downsize the PCB.

Why HDI Technology?

A 0.5 mm pitch array package has just enough space to accommodate a 3 mil (0.075 mm) PCB trace in between the solder balls and keep out areas. A 0.4 mm pitch array package, on the other hand—after accounting for the keep-out clearance—has insufficient space to layout a PCB trace between the solder balls (Figure 2), which forces the PCB layout tools to bury the trace in the PCB inner layers rather than placing it on the surface. As a result, the number of PCB layers may increase. This is problematic as the added layers are in direct conflict with consumer demand for ‘thin’ products.

One solution to this dilemma is to utilize innovations in PCB materials and via technology for connecting the different layers within an HDI

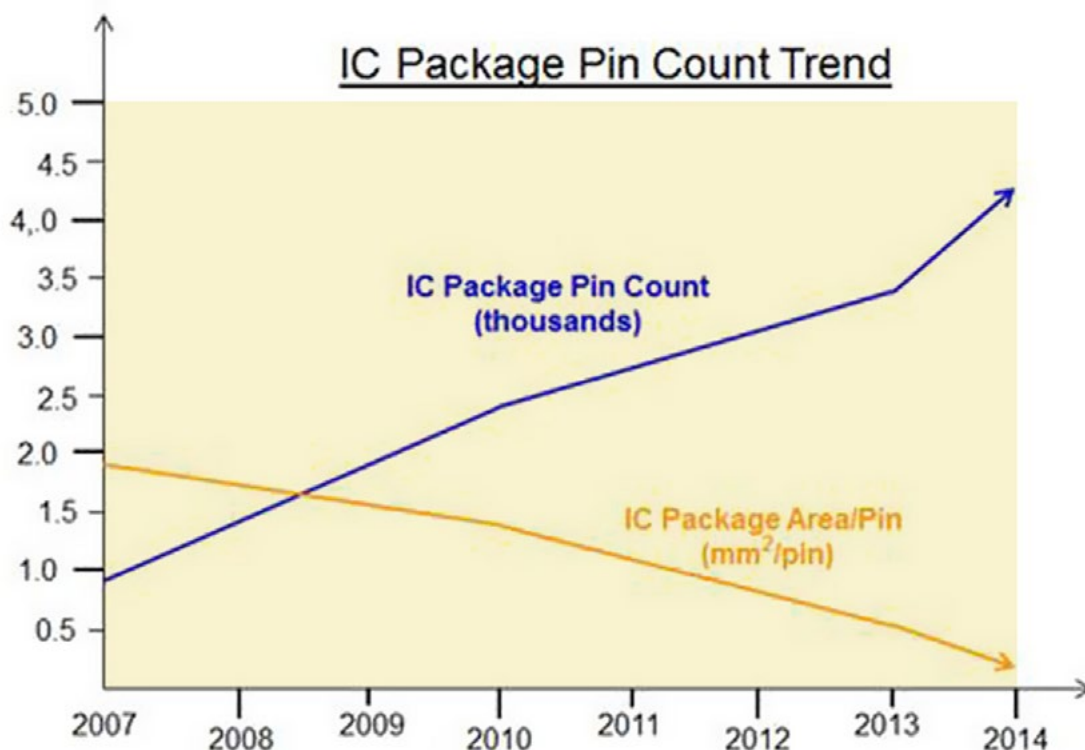


Figure 1: Current trends in IC package pin count.

HIGH-DENSITY INTERCONNECT AND EMBEDDED BOARD TEST *continues*

PCB. Today, the size of a PCB via has shrunk to microvia and stacked microvia. Also, the counter bore via has been introduced to minimize capacitance and regain signal fidelity for speeds greater than 5 Gb/s. A combination of some or all of these vias is used to deliver a HDI PCB.

Warning: Challenges Ahead

Placing the fine pitch array packages on the HDI PCB and achieving 100% solder attachment with single-digit defect parts per million is a science. It requires the use of the correct solder paste composition, accurate SMT placement and a magic recipe heat profile for the multi-stage reflow oven. Multiple vision systems are now commonly used inside SMT placement equipment to accurately align components to PCB pads. Standalone AOI equipment is also part of today's SMT line to review solder pre-reflow paste and/or post-reflow joints. Sometimes a manual or automatic X-ray vision inspection system is used to review post-reflow solder joints underneath IC array packages that are not visible to AOI.

HDI designs incorporating 3D ICs increase the number of non-visible solder joints on the PCBA to the detriment of AOI effectiveness and consequently, its utilization. AXI utilization is also reduced due to its ineffectiveness to separate solder joints across three planes: inside the 3D IC package, the 3D IC package attachment to the PCB, and the bottom side PCBA solder joints. Because of this, the onus of ensuring PCBA manufacturing quality shifts to electrical tests like in-circuit test and functional test.

Unfortunately, the adoption of a 0.4 mm pitch array package reduces the accessibility for electrical tests as surface traces are shifted into the HDI PCB inner layers. ICT test coverage therefore diminishes, pushing FT to compensate. However, using FT to make up for the missing test coverage typically means longer test development and test times, which in turn increases cost. The challenges associated with HDI PCBA post-reflow test are summarized in Figure 3.

HDI PCBA designs are prevalent today with one fine (or very fine) pitch array package for

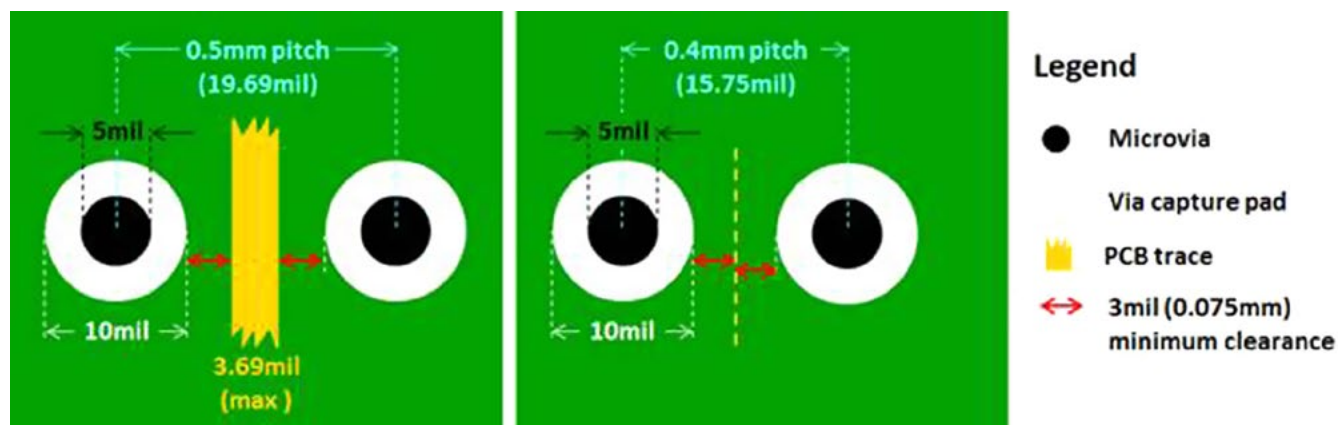


Figure 2: A 0.4 mm pitch array package cannot accommodate a PCB trace in between the solder balls.

Post-Reflow AOI	AXI	ICT	FT
Inability to inspect 3D ICs and increasing percentage of hidden joints.	Call accuracy to separate joints inside 3D ICs and the attachment joint to pcb.	Reducing test access as more traces migrate to inner pcb layers.	Trade-off test time and tester capacity to recover test coverage lost by AOI, AXI and ICT.

Figure 3: Shown here are the post-reflow test challenges for HDI PCBA.

HIGH-DENSITY INTERCONNECT AND EMBEDDED BOARD TEST *continues*

the CPU or SoC acting as the “brain” with supporting ICs and components. Examples of such designs can be found in mobile phones, tablets, television setup boxes, automobiles, notebooks,

and servers. Figure 4 illustrates the CPU- or SoC-dependent designs of these PCBA types. These designs (except for the server) are constrained by PCB real estate, making electrical test access

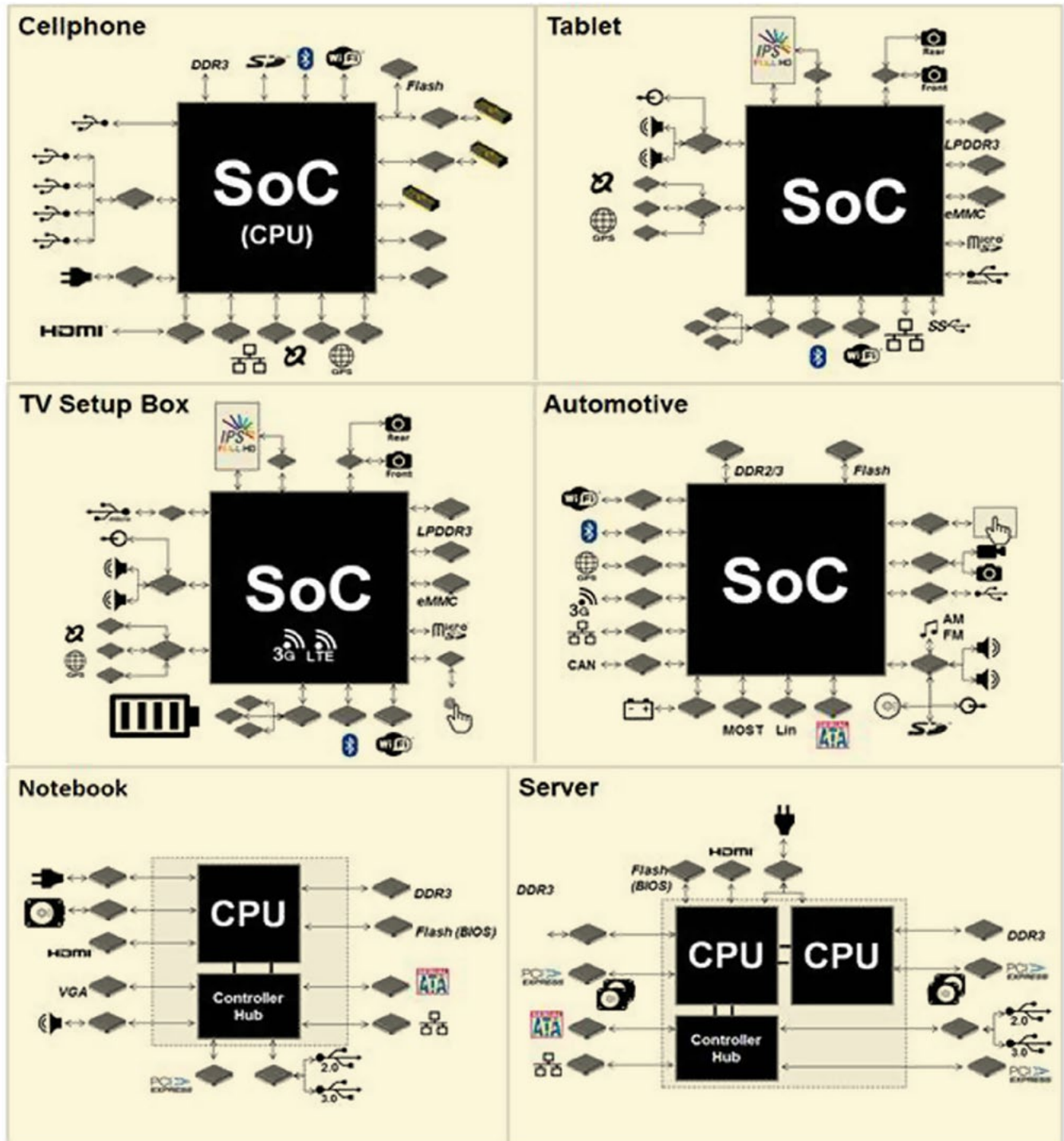


Figure 4: The CPU or SoC is central in the design of a cell phone, tablet, TV setup box, automobile, notebook, or server.

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HIGH-DENSITY INTERCONNECT AND EMBEDDED BOARD TEST *continues*

a premium. The current test strategy for these HDI PCBA types utilizes AOI, AXI and ICT to pre-screen manufacturing defects like shorts, opens, and wrong/bad component, so that FT can use precious test time to verify the functionality of the PCBA. Reduced test coverage of manufacturing defects makes it more challenging to diagnose the correct defect. FT does not pinpoint the defect. What it does do is present the symptoms so that the debug technician can manually diagnose the failure mechanism and find the defect.

Testing HDI PCBA Designs

There is a need to innovate the manufacturing test strategy for HDI PCBA designs. Vision inspection technologies will be severely challenged and defect call accuracy will decrease, with fine pitch array packages increasing the proportion of non-visible solder joints with less solder volume. A complementary limited access electrical test technology is needed to fill the test coverage void of AOI, AXI and ICT. IEEE 1687 is one possible solution, but it will be a few years before an IEEE 1687-compliant IC is commercially available. It took almost 10 years for IEEE 1149.1 to gain critical mass. IC designers

had to start incorporating boundary scan cells in the silicon and allocating 4 I/O (TRST is optional) in the IC package before PCBA designers could even design-in the use of boundary scan ICs and begin chaining them from the TDO of an IC to the TDI of the next IC. Hopefully the pace of silicon implementation and adoption will be faster for IEEE 1687.

The concept of IEEE 1687 is to use the IEEE 1149.1 pins (i.e., TMS, TDI, TDO, TCK and optional TRST) to put the IC into a test mode to control and exercise on-chip functionality and if possible, using the IC's outputs, to interact with surrounding devices. Both IEEE 1149.1 and IEEE 1687 are standards designed to guide IC designers to create in-chip access, independent of the core logic, for the sole purpose of IC verification when it is attached on a PCBA.

Embedded Board Test (EBT) uses the IEEE defined in-chip access to verify that the IC is attached to the PCBA and in good working condition. It then extends the tests to surrounding components and potentially drives through to test ICs further away. Silicon nails and cover-extend are examples of extending tests through an IEEE 1149.1-compliant device to DDRs and connectors, respectively.

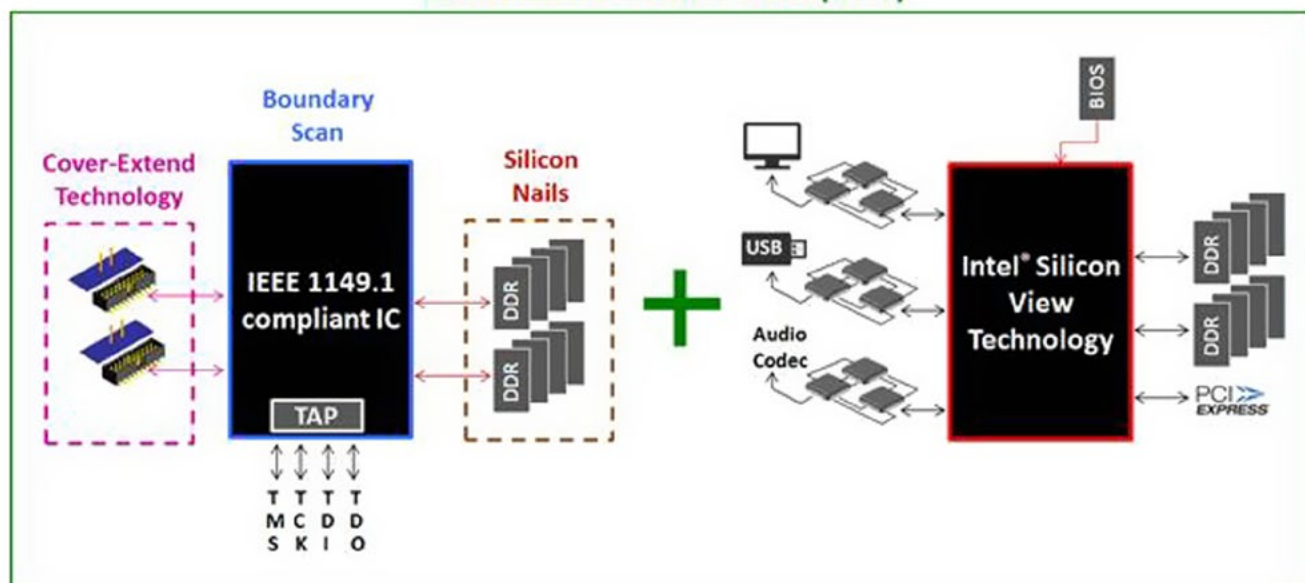
Embedded Board Test (EBT)

Figure 5: The concept of embedded board test uses the IEEE 1149.1 boundary scan and silicon view technology.

HIGH-DENSITY INTERCONNECT AND EMBEDDED BOARD TEST *continues*

IEEE 1687 is in its infancy with no compliant device available. Intel® Silicon View Technology (SVT), though not IEEE 1687 compliant, embodies the embedded board test concept. SVT works in tandem with the BIOS as the PCBA boots to discover internal devices and initialize communications, and interacts with surrounding ICs. It can be used to extend tests to the edge of the PCBA, gaining test coverage for connectors to display and USB ports. Intel SVT is available today for the code-named microarchitectures Haswell, Broadwell and the upcoming Skylake. HDI designs for tablets and notebooks with limited test access will benefit from the additional test coverage gained by Intel SVT. Figure 5 illustrates the combined test coverage of the EBT concept.

The EBT testing concept suits HDI PCBA designs in which one or more CPU or SoC functions as the 'brain.' The test coverage for such HDI PCBA designs will be high since the CPU or SoC can exercise almost all internal functions and extend it through to the PCBA edge.

Successful adoption of EBT requires it to be crafted early in PCBA design to develop the test software as the PCBA design evolves and matures. Ideally, EBT should be deployed starting from the first PCBA prototype build and continuing on to mass production; evolving the EBT test program to increment the test coverage progressively and maturing it prior to manufacturing release. The initial investment to adopt any new technology is high, but the cost amortizes across subsequent PCBA designs and models; increasing the electrical test coverage to sustain and potentially improve FT yields to return the investment.

Test coverage lost due to buried traces can be recovered using EBT, which makes it a comple-

mentary test to ICT. Pairing ICT and EBT is ideal as ICT can perform unpowered tests to locate and pinpoint short and open defects, as well as wrong components. This ensures the PCBA can safely power up for EBT to continue testing through the CPU or SoC to the PCBA edge. Figure 6 illustrates the impact of EBT to the post-reflow test of the HDI PCBA.

A key ingredient in the success of EBT, similar to ICT and FT, is the test fixture and fixture automation. Design for Test (DFT) is critical for electrical test to design-in and layout test pads to realize the complementary test coverage of ICT, EBT and FT. Repeatability and reliability of the test fixture to accurately make the probes contact the test pads will reduce false fails so the tester can deliver its full value. Automating the insertion and sequencing of connectors to the PCBA edge for loopback connectivity test will eliminate human mistakes and achieve consistent test cycle times. The demand for mechanical precision and probe targeting accuracy increases as test pad and connector sizes shrink. The electrical testing of the HDI PCBA requires the tester, test fixture and fixture automation to work as a single solution to maximize its potential. It also requires one owner to architect, plan and implement the test solution; not three individual test vendors just contributing their parts.

HDI PCBA for a server has sufficient PCB real estate to accommodate test access to more than 80 percent of total nets. The test strategy will continue to use ICT at the first stage of electrical test with empty CPU socket(s) and empty DIMM slots. EBT offers an alternative to exercising the PCBA with the inserted CPU(s) and DIMMs in a bench-top station setup after ICT. The CPU(s) and DDRs are usually soldered down for microservers so the test strategy of a

Post-Reflow AOI	AXI	ICT + EBT	FT
Inability to inspect 3D ICs and increasing percentage of hidden joints.	Call accuracy to separate joints inside 3D ICs and the attachment joint to pcb.	DFT using a complementary ICT and EBT to recover test coverage.	ICT+EBT pre-screen structural and basic functional defects. FCT to focus on performance test.

Figure 6: EBT complements ICT and positively impacts the post-reflow test for HDI PCBA.

HIGH-DENSITY INTERCONNECT AND EMBEDDED BOARD TEST *continues*

combinational ICT and EBT provides excellent test coverage.

Conclusion

With new electronic functions constantly being integrated into a SoC encapsulated in a less than 0.5 mm pitch array package, the future looks bright for EBT. The SoC will become a main stream component in all consumer portable devices extending into IoT devices. These fast and power efficient products will push higher density interconnects, burying almost all nets except for power and ground nets and

creating the need for EBT. While EBT is currently in the early adopter stage, growing adoption and implementation of IEEE 1687 is sure to enable EBT to cross the chasm to the early majority stage in a few years. **SMT**



Mark Lau is a product manager with Keysight Technologies Inc., formerly Agilent Technologies' electronic measurement business.

SMART Group's 2015 European Conference

Reservations for delegate places and bookings for table top exhibition space are already being received for the SMART Group European Conference & Exhibition, to be held September 22–23 at the National Physical Laboratory (NPL), one of the UK's leading science and research facilities, in London.

The conference will be held over two days with a table top exhibition, allowing delegates to see and meet many of the leading suppliers of materials, equipment and testing services in the industry. The exhibition will open each day prior to the start of the conference, during the coffee breaks and lunch. A special reception for delegates, speakers and exhibitors will be held on the first evening of the conference.

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Test Match-Partnering Specialist Boundary-Scan with ICT

by **Robert Thompson**
XJTAG

Introduction:

Boosting ICT to Improve Testability

Popular ICT platforms from well-known vendors can perform a wide variety of analogue, digital, powered, and unpowered tests to verify the integrity of electronic assemblies. In addition to basic opens and shorts testing, analogue test capabilities include resistor, capacitor, potentiometer, diode and transistor tests. They can also verify power rails, and can generate digital test vectors as well as analogue waveforms to check for circuit functionality.

The test coverage that can be achieved using a bed of nails fixture alone is becoming increasingly limited. The biggest problem here is that any component pins not extending through to the probed side of the assembly are not acces-

sible to the fixture nails unless the individual nets connected to it are exposed via unmasked vias, attached thru-hole connectors, or test points. The process of adding test access for ICT increases the cost of design, layout, and manufacturing: extra vias, extra test points, and extra routing necessities all increase the overall complexity of the assembly. Physical test access is not free.

Boundary-scan, used in conjunction with fixture-based tests, can extend test coverage on boards where test access is limited, and is critical to providing powered-shorts, opens and core-logic testing. IEEE 1149.1 compliant boundary-scan devices have the capability of driving and measuring pin states without physical access to the pin using a tester probe. ICT vendors integrate boundary-scan capabilities developed in-house to provide basic scan functionality that is native to the test platform, but this is not without its drawbacks.



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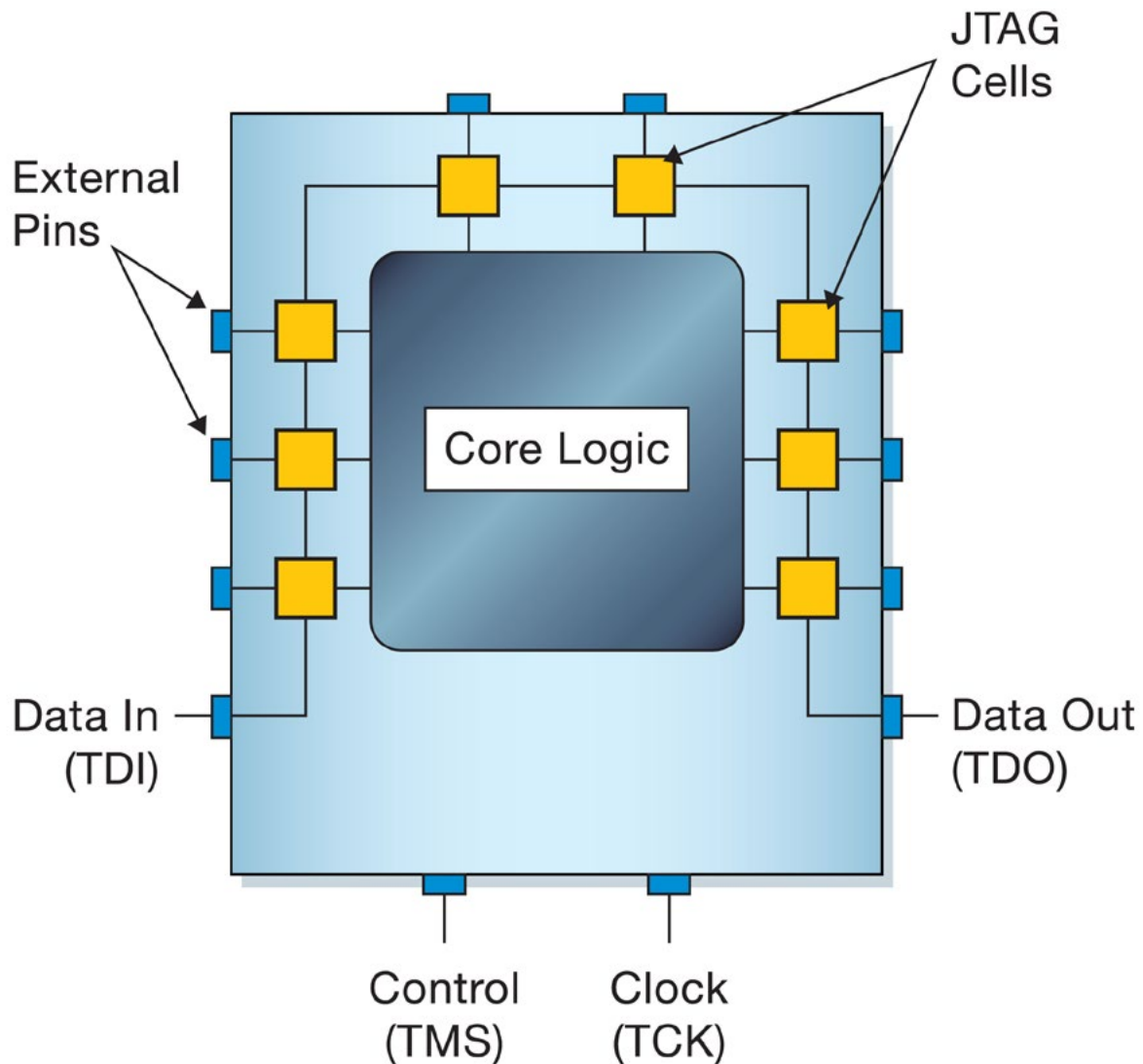


Figure 1: Simplified diagram of a boundary-scan component.

Flying probe testers can offer an alternative to ICT that eliminates some disadvantages such as the cost and lead times associated with bed-of-nails test fixtures and the PCBA modifications they require. On the other hand, devices like BGAs with inaccessible pins restrict the coverage possible using ordinary flying probe testing. Augmenting flying probe with boundary-scan can help overcome this problem and delivers additional valuable benefits.

Test Without Touching

The native boundary-scan test capability of a system such as the Keysight 3070 ICT station

is able to generate tests for boundary-scan devices connected to the boundary-scan chain.

Testing non boundary-scan devices on nets connected to the boundary-scan chain is possible, using Keysight's optional Silicon Nails tool.

As the name suggests, Silicon Nails uses the scan capable IC in a boundary-scan chain to probe the pins of the connected non boundary-scan device. However, some amount of manual interaction may be required, particularly if any pin on the non boundary-scan device is not connected to a boundary-scan cell. The VCL (vector construction language) libraries assume that all pins on the target device are accessible. If this is

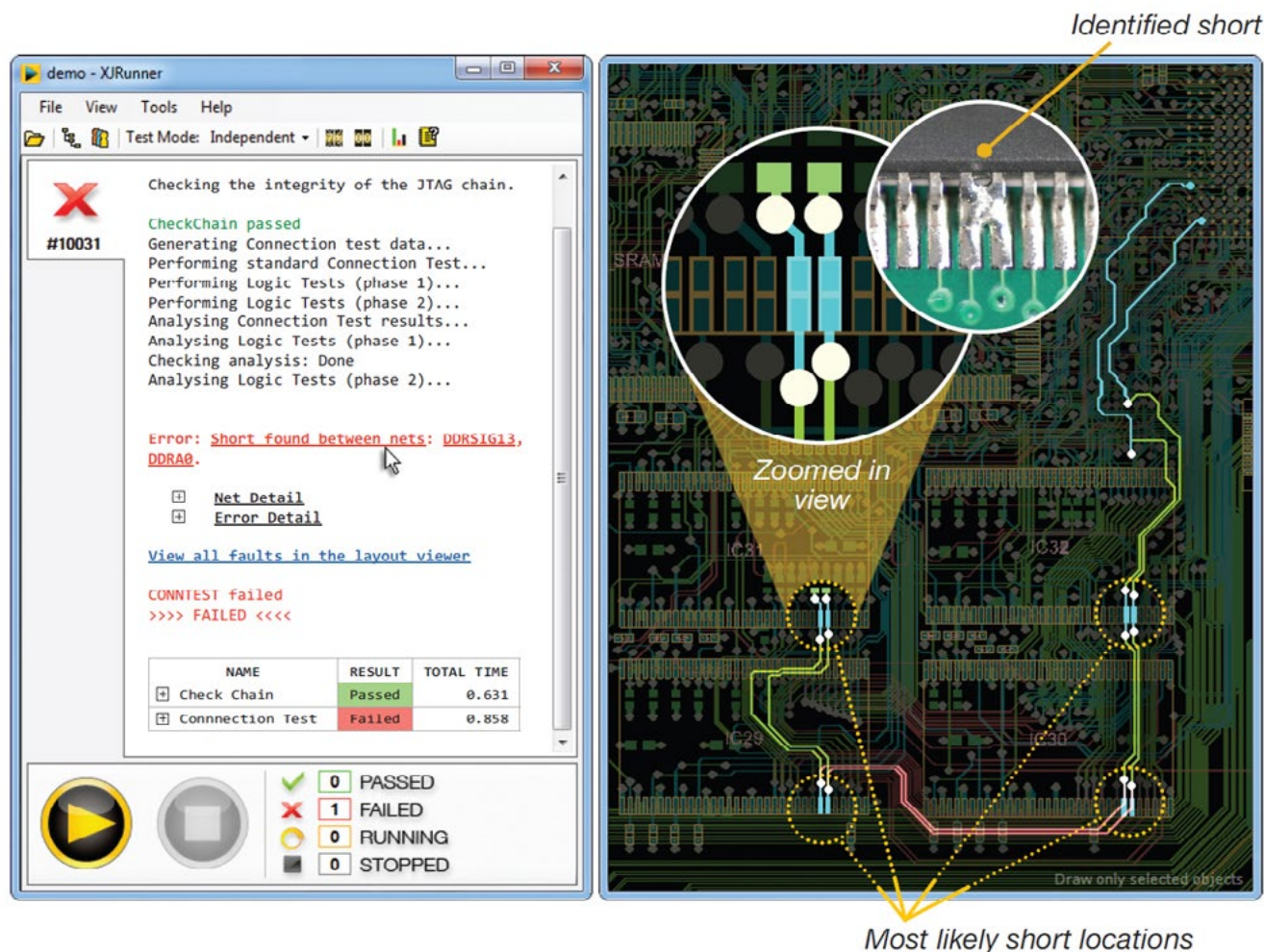
TEST MATCH—PARTNERING SPECIALIST BOUNDARY-SCAN WITH ICT *continues*

Figure 2: Advanced connection tests can identify and pinpoint the possible physical locations of faults.

not the case, Silicon Nails will not generate the test properly. The user must then modify the library to change the properties of non-accessible pins so that the Silicon Nails test can be generated. Similar modifications have to be made for every test that the system is unable to generate automatically.

In contrast, writing test scripts can be straightforward with specialist external boundary-scan tools, especially when using a high-level device-centric language. The system automatically generates test vectors at runtime that meet the stated requirements. Moreover, users can benefit from the increased capabilities of specialist equipment, such as advanced connection tests that are able to identify faults that more basic tests cannot detect, and can pinpoint the causes of any faults extremely ac-

curately. Tests such as shorts, opens, pull-ups, pull-downs and interconnection testing can be performed automatically.

By combining specialist boundary-scan capabilities with ICT, users can take advantage of state-of-the-art boundary-scan functionality, such as automatic generation of tests for non boundary-scan devices. Test scripts are easy to write, particularly when using a high-level device-centric language that allows the test description to be abstracted from the detail of generating test vectors.

Making changes to the executing boundary-scan tests is as simple as changing the underlying scripting language rather than wading through millions of lines of test vectors: Pinout and board netlist changes can be easily integrated into the test platform without making

TEST MATCH—PARTNERING SPECIALIST BOUNDARY-SCAN WITH ICT *continues*

changes to the board file and regenerating (and hence needing to re-debug) test vectors.

Libraries developed in a higher level device centric language are also more reusable and can be migrated project to project without modification. DDR3, PHY, SPI, I²C, and much more become easily testable and the libraries are not specific to the devices.

In addition, specialist boundary-scan tools tend to have better signal integrity and can push bits into the scan chain at a much faster rate than most ICT hardware, allowing more devices to be tested more quickly.

Integrating Specialist Boundary-Scan

Integrating a specialist boundary-scan system such as XJTAG with the ICT equipment provides a convenient means of performing boundary-scan test without changing to a different test-execution environment or removing the unit under test from the ICT fixture. Combining ICT and external boundary-scan in one efficient process step can help improve efficiency, minimise demand for additional items of test equipment on the production line, and protect sensitive hardware from physical damage, loss or misplacement.

The Keysight 3070 utility card and similar Teradyne multi-function application board simplifies integrating the user's choice of external electronics. Users can plug-in custom modules to perform specific test functions.

Specialty boundary-scan controllers take advantage of this extensibility. They are approved by the respective ICT vendors, and plug directly into the expansion board to provide access to specialist boundary-scan test and programming tools. Multiple instances of the controller can be installed into each board, which can boost throughput significantly without custom fixturing.

Specialty controllers can connect to a maximum of four boundary-scan chains on the unit under test, and multiple controllers can be fit-

ted to each utility card or multi-function application board. This gives users the flexibility to test boards with more than one boundary-scan chain, or to test multiple panelled boards simultaneously. The controller also allows in-system programming of devices at close to their theoretical maximum programming speeds. Multiple controllers can program multiple boards simultaneously, so all boards in a panelised assembly can be programmed in the same time needed to program a single board. Paired with the throughput multiplier effect that comes from combining ICT, boundary-scan and programming in a single step, this can become a tremendous time saver.

Test Re-Use Boosts Productivity

Integrating specialist boundary-scan in this way can not only simplify test generation, but also helps when it comes to diagnosing and repairing boards. The increased test coverage of previously inaccessible nets and devices saves the need to interpret failure messages that can be ambiguous, thereby reducing the time to identify the cause of a defect.

The same boundary-scan tests can be used in bench-top repair as are used in production ICT since they are not dependent on access granted to the circuits by a fixture which increases throughput of the ICT station and test fixture by minimising the time devoted to rework.

Production equipment can be used for production more often.

Test engineers can utilise the same boundary-scan tests used by the board designers when creating tests to be run on the production test platform, which minimises duplicated effort.

Moreover, boundary-scan tests can be debugged on the bench rather than on the tester, minimising the time test engineers must spend using the production test equipment to troubleshoot tests. The boundary-scan application can be completely validated before being integrat-

“Multiple controllers can program multiple boards simultaneously, so all boards in a panelised assembly can be programmed in the same time needed to program a single board.”

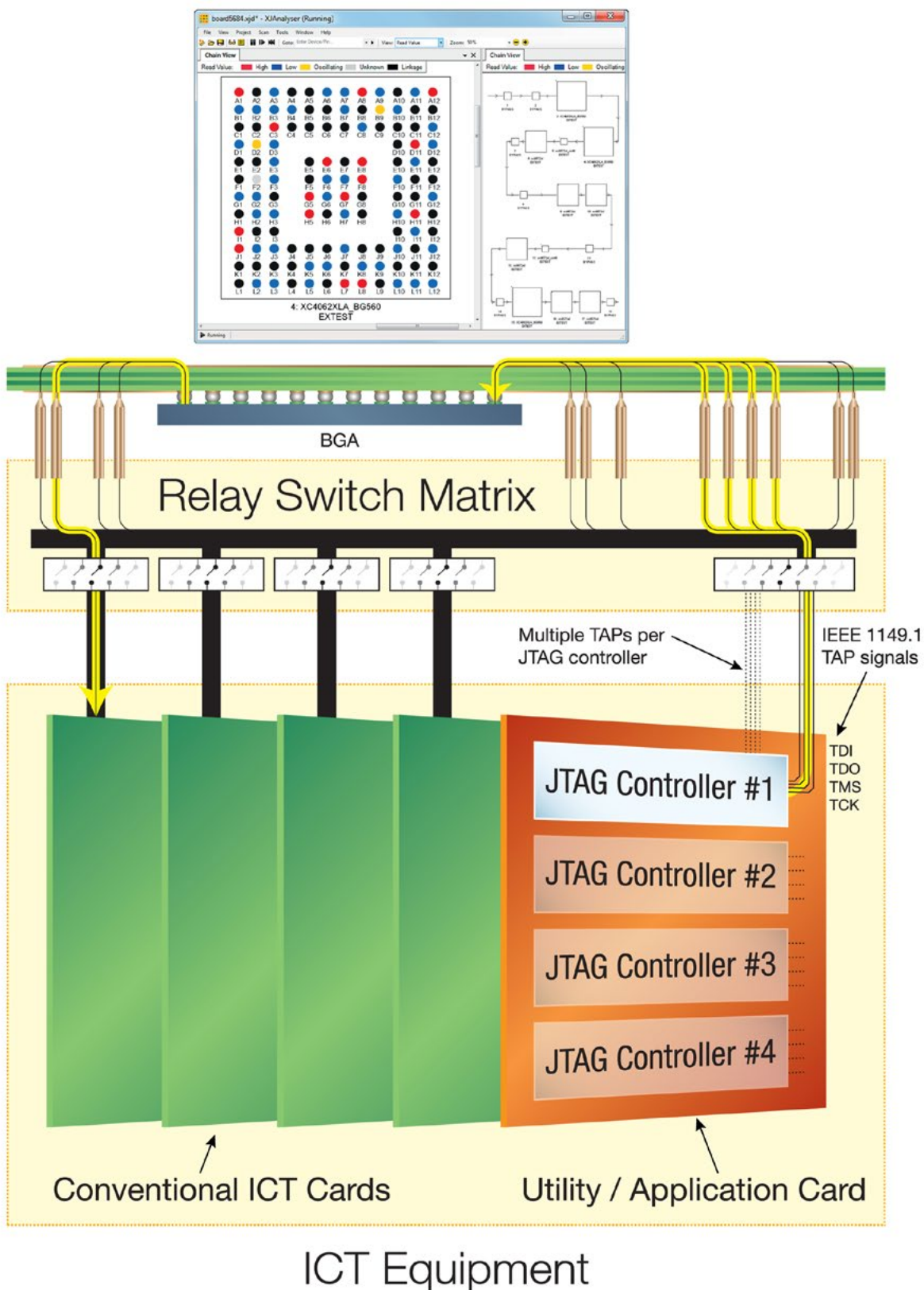
TEST MATCH—PARTNERING SPECIALIST BOUNDARY-SCAN WITH ICT *continues*

Figure 3: Specialist boundary-scan can work alongside ICT to increase fault coverage and simplify test creation and fault analysis.

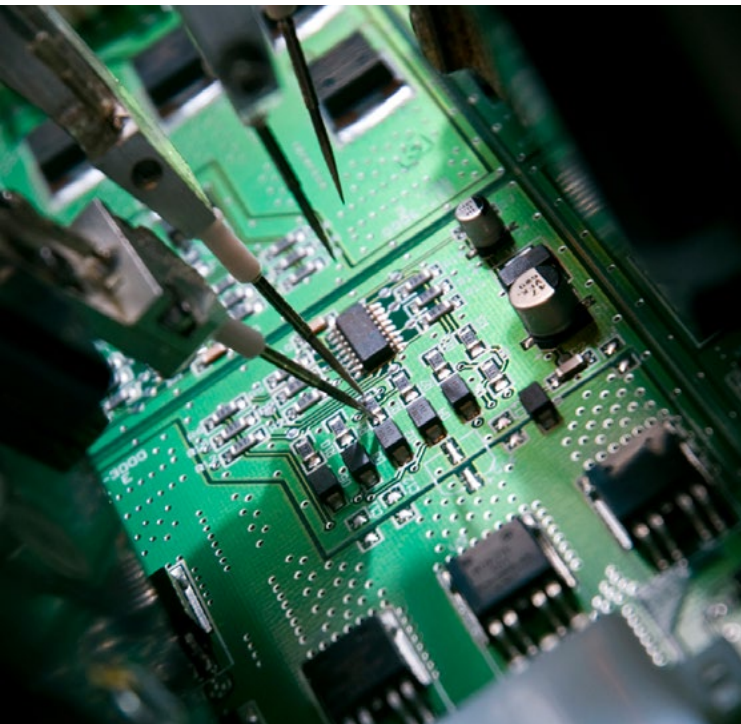
TEST MATCH—PARTNERING SPECIALIST BOUNDARY-SCAN WITH ICT *continues*

Figure 4: Typical flying probe tester.

.....

ed into the ICT, which can save fighting code that needs to be debugged and potential fixture problems all at the same time.

Flying Probe + Boundary-Scan

Flying probe machines work around the constraints of physical access needed for ICT test fixtures. With the help of automated programming and debugging, which helps to minimise development time, a new application can be turned round in an afternoon instead of weeks needed to deliver an ICT fixture.

However, components with inaccessible pins can still compromise test coverage. By integrating boundary-scan capability in the flying probe tester, it becomes possible to apply powered-test vectors directly to pins of a boundary-scan device. Testing can also be extended to non boundary-scan capable devices on the board. Monitoring the response then allows the status of the device and its connections to be assessed. Moreover, the benefits associated with library re-use are as applicable to flying probe as they are to ICT, and help flying probe to retain its quick-turn advantage.

Boundary-scan also allows processes not normally possible using conventional flying probe methods—such as oscillator testing, programmable part verification and complex logic disabling—without adding excessive complexity and so defeating the purpose of a flying probe tester.

With boundary-scan added to the mix, testing is no longer limited to four, six, or eight probes. Tests can drive and receive as many signals as the board design allows, which opens up test coverage and diagnostic usability previously impossible to attain.

Increased test coverage means better defect detection at test and fewer defects and product returns after the customer hits the “on” switch for the first time.

Depending on the type of board, this combination of flying probe and boundary-scan test may exceed the test coverage achievable using ICT with a bed-of-nails fixture!

Engineers can add the benefits of boundary-scan to flying probe without also adding the difficulty of a fixture-based test program. Diagnostics are improved, and operators do not need to be taught how to interpret ambiguous test failures since boundary-scan is a digital test technology and points directly to the problem.

It is even possible to run the same boundary-scan test on the flying probe and on an ICT platform like the 3070. A project can start with flying probe boundary-scan and then transition smoothly to ICT when higher volume testing is required, since the boundary-scan tests are re-usable.

Conclusion

Specialist boundary-scan is an ideal companion to ICT and flying probe testing. Users can benefit from better fault coverage, better test re-use, faster test development and fuller diagnostics. Popular ICT platforms have the necessary expansion capability built in, and specialty boundary-scan can be integrated successfully with flying probe equipment. **SMT**

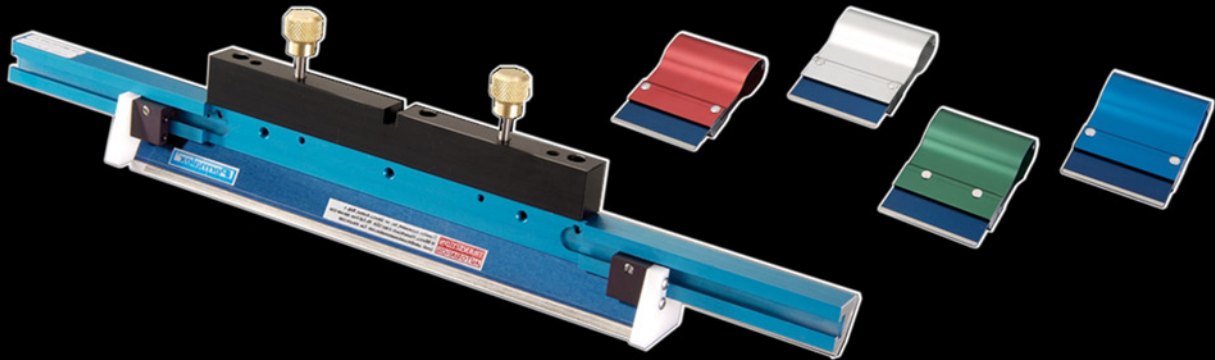
Robert Thompson is a field application engineer for XJTAG.

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In-line Solder Penetration Testing with 3D X-ray Inspection

by **Andreas Türk**
GÖPEL ELECTRONIC

Through-hole technology (THT) is probably the oldest assembly technology in the field of PCB manufacturing. However, even in this modern age of surface-mounted technology (SMT), it still has its place. Even today, wired components are often assembled using wave soldering—in keeping with the tradition of times past. This has the disadvantage of requiring additional manufacturing equipment. It is therefore advisable to use reflow soldering for connectors and other wired components. To this end, through-hole components were devised for automatic assembly and for high thermal loads in the furnace, which led to the birth of the term, through-hole reflow (THR). With this technology, it is now possible to process components in through-hole technology within the SMT process. But how can these solder joints be reliably tested? What technology is needed in order to be able to assess the solder penetration, for example?

Acceptance Criteria for THT/THR Solder Joints

Figure 1 is a schematic representation of a THT solder joint in cross-section. The solder wave flows from the solder source side to the solder target side (component side), due to capillary action. In so doing, it wets the connecting surface of the solder side, surrounds the pin and forms a solder meniscus on account of the protrusion of the pin on the solder side.

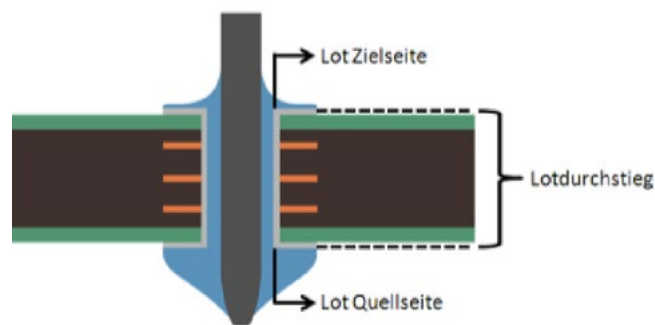


Figure 1: Schematic representation of a THT solder joint in cross-section. Ideal soldering with 100% solder penetration.

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IN-LINE SOLDER PENETRATION TESTING WITH 3D X-RAY INSPECTION *continues*








IPC criterion		Category 1	Category 2	Category 3
Solder side	circumferential wetting of pin	270° 	270° 	330° 
Solder side	wetted connecting surface	75%	75%	75%
Component side	circumferential wetting of pin	immaterial	180° 	270° 
Component side	wetted connecting surface	0%	0%	0%
Solder penetration		immaterial	 75%	 75%

Table 1: Overview of selected acceptance criteria for THT solder joints according to IPC-A610E.

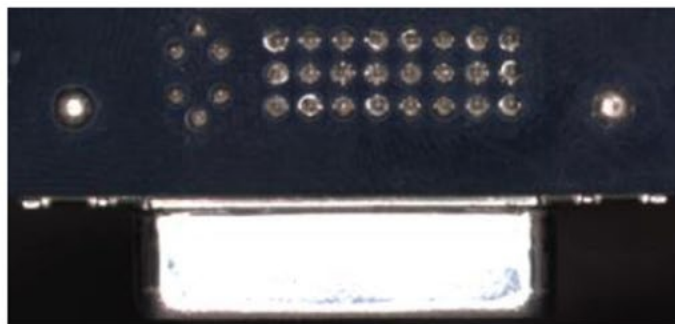
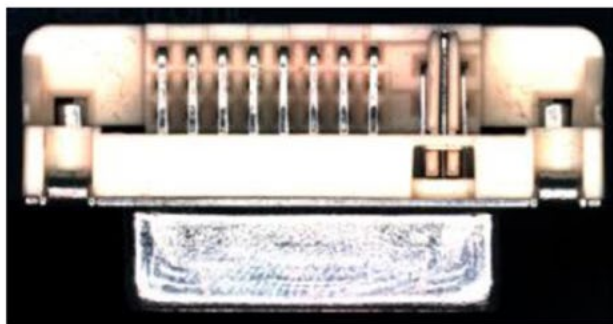


Figure 2: Connectors shot from above and below using AOI.

The acceptance criteria are defined in IPC-A610 in order to distinguish between good and bad solder joints after successful soldering. Table 1 gives an overview of the criteria in excerpts:

It is now necessary to select testing technology which meets the specified acceptance criteria. Based on the example of a multi-row connector (Figure 2), the following table provides an overview of the test coverage of AOI and 3D AXI systems.

AOI systems are highly suited to assessment of the peripheral wetting of the pin and the sleeve and to evaluation of the wetted connecting surface on the solder side of a THT solder joint. The disadvantage of a traditional 2D AOI or an innovative 3D AOI system here, however,

is that it is often only possible to assess the solder side because the pins on the component side are usually concealed by the component body itself. An assessment of the solder joints on the component side is therefore not possible with an AOI system. The solder penetration also remains hidden from traditional AOI technology.

A modern 3D X-ray system can provide a remedy. The 3D X-ray inspection not only makes the solder joints on the component side (i.e., below the component housing) visible, but is also able to calculate the solder penetration and the solder volume.

In addition to 3D X-ray technology, 2.5D X-ray imaging (oblique radiation) is also used to test the solder penetration. However, assessment

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IN-LINE SOLDER PENETRATION TESTING WITH 3D X-RAY INSPECTION *continues*

IPC criterion		2D/3D AOI	3D AXI
Solder side	circumferential wetting of pin and sleeve	Yes	Yes, somewhat restricted
Solder side	wetted connecting surface	Yes	Yes, somewhat restricted
Component side	circumferential wetting of pin and sleeve	Yes	Yes, somewhat restricted
Component side	wetted connecting surface	No	Yes, somewhat restricted
Solder penetration		No	Yes
Calculation of volume		No	Yes
Presence of pin		Yes	Yes
Short circuit		Yes	Yes

Table 2: Overview of test coverage using 2D/3D AOI and 3D AXI.

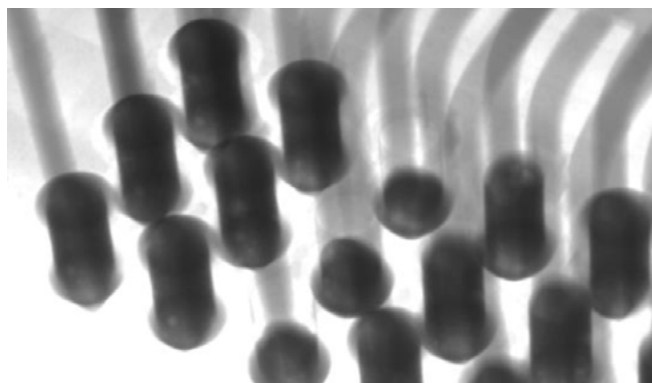


Figure 3: Connectors in 2.5D oblique radiation with easily visible defects in the solder penetration.

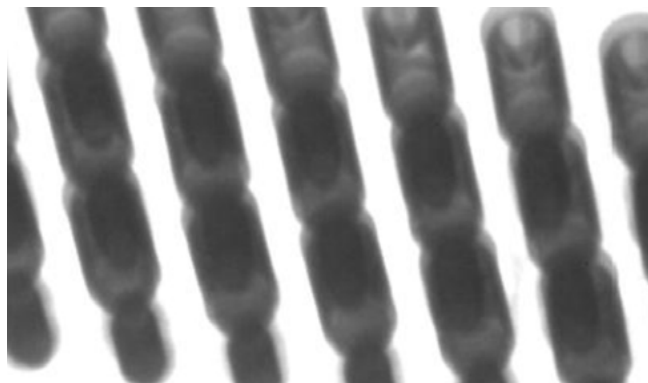


Figure 4: Connectors with many successive rows of pins one behind the other in 2.5D oblique radiation; the solder joints are difficult to separate.

of the solder penetration by means of 2.5D X-ray imaging is often very difficult, especially in the case of multi-row connectors. The pins of the individual rows are often concealed by one another. In addition, multi-row connectors are harder for the classification staff to interpret in a 2.5D image than in a three dimensional sectional image in which the solder joint is always displayed from above as a slice.

The Salami Tactic

To calculate the solder penetration, the THT solder joint is digitally divided into slices. In a method comparable to slicing salami, slices with

the thickness “d” are generated and the area of each slice that is covered with solder is calculated. Figure 5 shows the digital section schematically.

To calculate the solder penetration, a minimum allowable slice area is then defined in mm² in the THT test function. A check is then carried out slice-by-slice to determine whether this minimum area is achieved. If the area is under the minimum, this is the stop criterion for determining the solder penetration. The penetration height “h” (mm) is then calculated by the machine and, in the event of any faults, this measurement is displayed beside the X-ray fault image on the repair station/classification

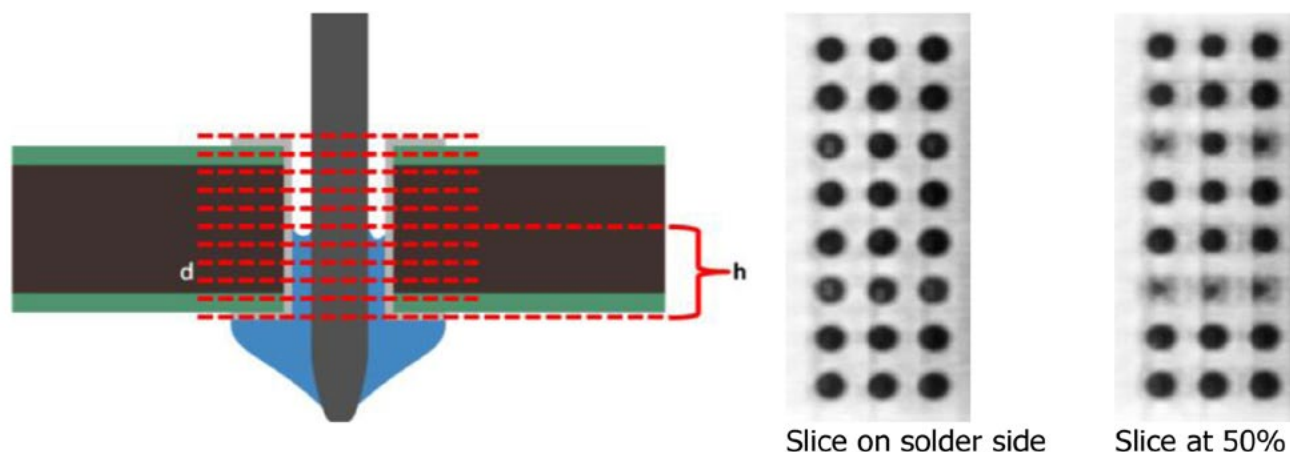
IN-LINE SOLDER PENETRATION TESTING WITH 3D X-RAY INSPECTION *continues*

Figure 5: Left: schematic representation of the N-sectional planes. Centre: Slice on the solder side. Right: Slice at 50%.

station. In addition to determining the solder penetration, the system is also capable of calculating the solder volume (mm^3). In order to do this, N-slices with the thickness “d” are generated between the solder and component side as before for determining the penetration, and the individual volume is calculated for each slice. Finally, the sum of the volumes of all the slices gives the total volume.

In the case of a THR solder joint, the solder source side and solder target side are reversed. The acceptance criteria remain the same, however. Inspection of THR solder joints is therefore easily possible. However, due to the degassing of the flux of the solder paste during the soldering process, in the case of THR solder joints there is often a relatively high proportion of air pockets within the solder joint. This is where the use of a 3D X-ray system is predestined to be able to detect breaks in the solder penetration.

In order to set the parameters for the THT test function, only the corresponding connectors need be selected; the X-ray images (slices) are then displayed precisely above the AOI image. The parameters for the test function are then set using a few slide controls in order to enter the geometry of the THT solder joint and the necessary grey-scale value thresholds. This demonstrates another advantage of 3D X-ray technology: the solder joints are always shown in normalised plan view. This means that a single component library can be used. In addition,

an integrated debugging statistics tool helps programmers to compare measured values from N-module inspections with each other and to optimise measurement thresholds.

All the X-ray images required for the 3D reconstruction (oblique radiation images) are captured in motion (scanned) and computed in real time (reconstructed). This scanning image capture is 3–4 times faster than in systems with planar stop-and-go image capture technology. As a result, large assemblies with numerous connectors can also be inspected within the clock cycle.

Summary

To test the solder joints of THT/THR connectors, an in-depth look is necessary in order to ensure that it is not just “the tip of the iceberg” that is considered. A pure AOI system is not sufficient for fault finding if IPC guidelines are to be met. 3D X-ray technology enables conclusions to be drawn about the solder penetration and the solder volume, among other things, including a precise assessment of these criteria, while at the same time, meeting the high demands of the production line cycle. **SMT**



Andreas Türk is division manager for Automatic X-ray Inspection Systems at Göpel Electronic.

Acoustic Surface Flatness of Components and Boards

by Tom Adams
SONOSCAN INC.

Plastic packaged ICs, including BGAs, whether single or stacked, may experience warping as a result of processing. Thermal stresses in a warped BGA package that has been mounted on a board can break solder ball connections. Often it is the corners of the package that curl upwards and cause the solder balls at the corners to lose contact.

Package-on-package assemblies (PoPs) are also subject to warping. The risk is greater if—as is usually the case—the bottom chip is a processing device and the top is a memory device, or even a stack of two memory chips wire-bonded to each other.

Acoustic micro-imaging tools are used to image internal features, including anomalies and defects, in many types of components, but in plastic IC packages the surface topography may

be scanned simultaneously to produce surface flatness data and images. BGA packages are often the subject of this imaging, although other package types are often imaged as well.

Sonoscan has developed and patented a method that uses acoustic micro-imaging tools to measure and map the flatness of the top surface of a BGA package and other package types where warping may occur. The method is called acoustic surface flatness (ASF) and it is useful during the development of a BGA or PoP as a way to determine non-destructively whether internal stresses are warping the surface. It is also used during production to remove BGA packages whose warping exceeds applicable standards, and after electrical failures in testing or in the field to isolate possible causes of a failure.

The technology uses an ultrasonic transducer that raster-scans the surface of the sample whose internal features are being imaged. While it is scanning, the transducer launches a pulse of ultrasound into the BGA package at each of mil-



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ACOUSTIC SURFACE FLATNESS OF COMPONENTS AND BOARDS *continues*

lions of x-y coordinate locations, and receives the echoes from any material interfaces that the pulse encounters at those locations. The transducer carries out this function at several thousand x-y locations per second while it is scanning. The first material interface encountered by the pulse is the couplant-to-package-surface interface. This is the only interface where defects (other than flatness variations) do not occur. Internal defects occur at deeper interfaces, such as the mold compound-to-die interface, the mold compound-to-substrate interface, and the die-to-substrate interface.

The thinness of the BGA package and the acoustic velocity of the materials in the BGA package (mold compound around 3300 m/s, silicon around 8300 m/s) mean that a pulse launched by the acoustic micro imaging tool's transducer arrives back as an echo in a few microseconds. And the lateral speed of the moving transducer is high: >1 m/s. This is why the transducer can collect echoes from several thousand x-y coordinates per second while scanning. At each coordinate it can collect echoes from various depths within the BGA package, because those echoes will arrive at the transducer at different times.

As Figure 1 shows, Echo 1, the echo from the couplant-to-mold compound interface at the top of the BGA package, is the first echo to arrive back at the transducer. The elapsed time since the launch of the pulse is used to measure the distance from the transducer to the package surface at every x-y location. If the package surface is truly flat, the elapsed time and the distance will be the same for each of the millions of x-y coordinates over the entire package surface. When the surface is mapped by assigning a pixel color to various distance ranges, the truly flat surface will have the same color across its entire area. In practice, of course, such perfect flatness is rare or non-existent. The colors used in the color map make distance variations across the package surface more visible.

Echo 2 and Echo 3 (and deeper echoes) are from material interfaces below the surface of the BGA package. Their elapsed times are used to verify the depth of an interface. The amplitude of the echo is measured and is critical in differentiating between good interface bonding and non-bonds, delaminations, voids or other gap defects. In a PoP, if underfill is not used, much of the space between the two packages is filled with air, which an ultrasonic pulse does

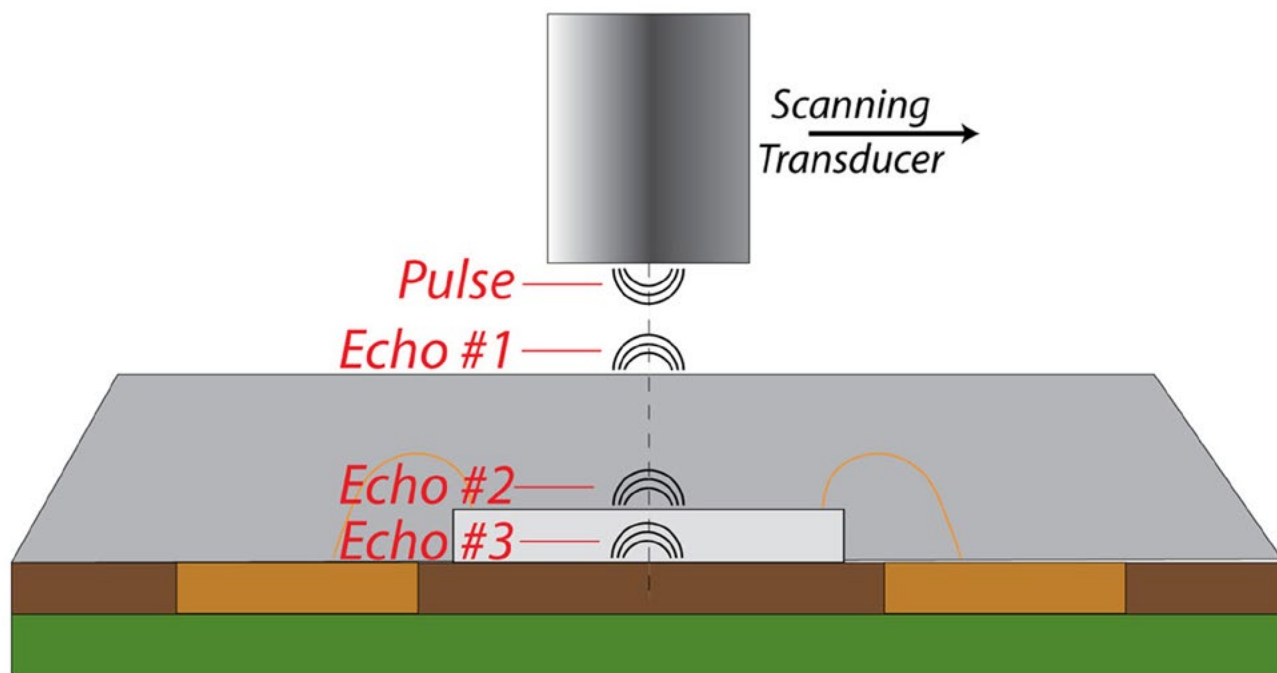


Figure 1: Echo 1 is from the BGA package surface; the other echoes from internal interfaces.

ACOUSTIC SURFACE FLATNESS OF COMPONENTS AND BOARDS *continues*

not penetrate. Where the two packages in a PoP are bonded, acoustic imaging of the bonding may be possible.

The ASF data from the top surface of the BGA is collected during the same transducer scan as data from deeper interfaces, and thus creates a separate surface flatness image without requiring additional scan time. The amplitude of the ASF echo is seldom of interest because the two materials involved—couplant and mold compound—do not vary.

Figure 2 is the ASF image showing in color the surface topography of a plastic BGA package that is the top member of a PoP assembly. The surface resembles a very shallow bowl: the deepest part is at the center (dark red in the color map at left). From the deepest part the surface moves upward to the dark blue regions at

the corners of the package. The degree of warping is not consistent. For example, the large yellow region in the lower left quadrant indicates slightly less upward curl. The difference in elevation between the lowest and highest points is 0.4 mm (400 microns). The degree of warping is thus of concern because it is four times the allowable departure from planarity permitted by the JEDEC design guide for PoPs.

The data can also be viewed in other ways. Figure 3 is the exaggerated profile of a single scan horizontally from left to right across the center of the BGA package in Figure 2. The somewhat irregular extent of warping can be seen clearly in this profile. Top-to-bottom profiles can also be produced.

The surface of a warped BGA package can also be represented as a three-dimensional

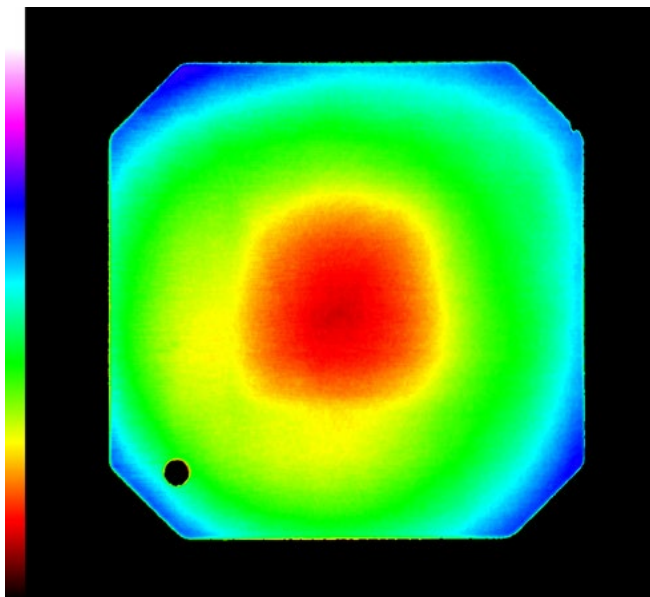


Figure 2: The surface of this BGA is lowest (red) at center and highest (blue) at the corners.

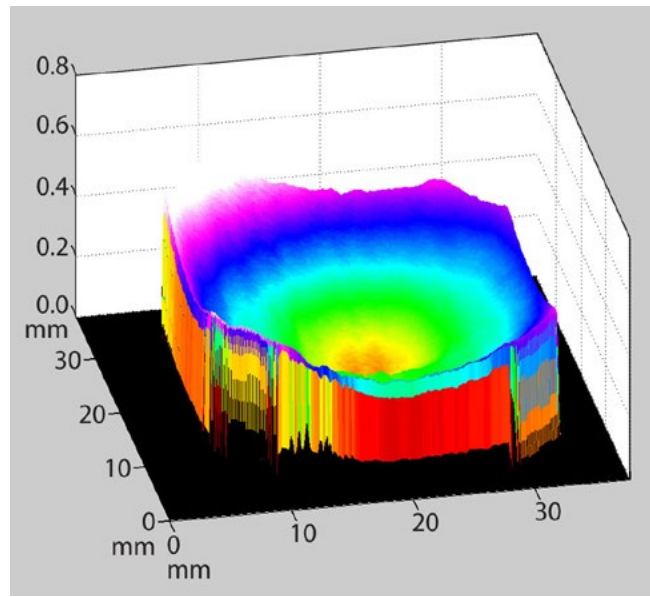


Figure 4: 3D acoustic image of a similarly warped BGA.



Figure 3: Vertically exaggerated profile of a left-to-right section through the center of the same BGA.

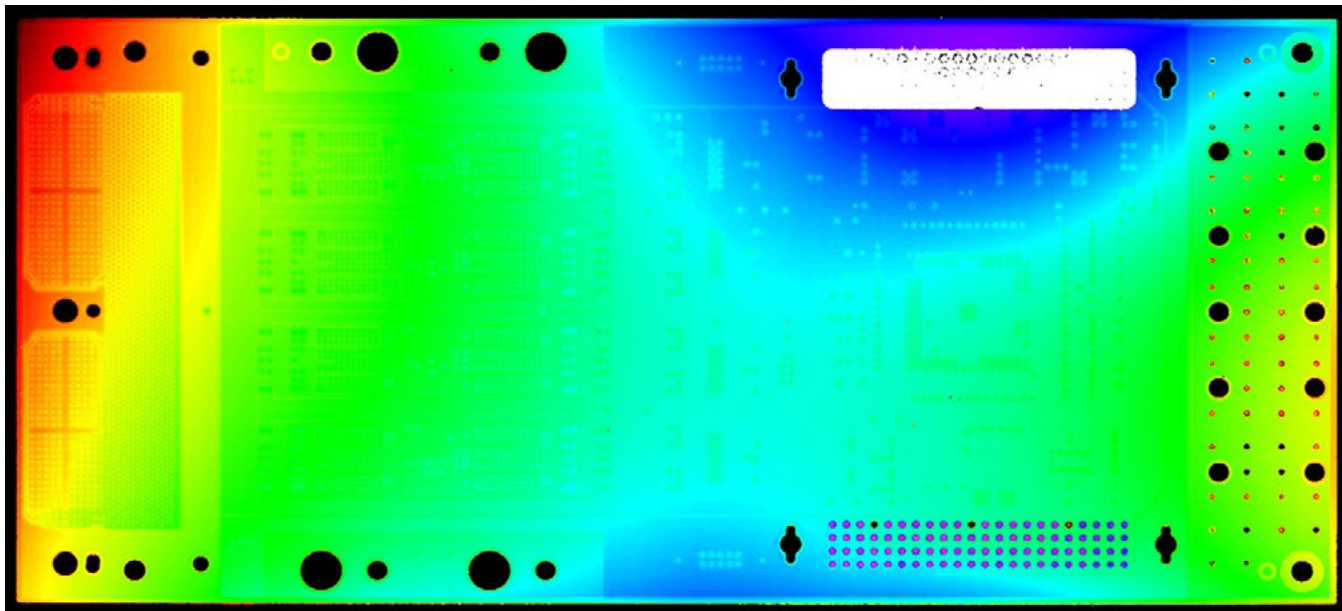
ACOUSTIC SURFACE FLATNESS OF COMPONENTS AND BOARDS *continues*

Figure 5: Acoustic image of a PCB whose surface is asymmetrically deformed, and which has a smaller board (white) attached.

acoustic image, as shown in Figure 4. This is a different BGA package from the one shown in Figures 2 and 3, although the color map used was similar. The highest elevation at upper left extends into the white portion of the color bar. The total vertical extent of the warpage extends from 0 to slightly more than 0.4 mm.

ASF may also reveal phenomena in the PCB itself. Ultrasound does not penetrate deeply into the complex structure of a PCB, but ASF can image the surface changes caused by phenomena within the board.

Figure 5 is the ASF image of the back side of a populated board. This board is not warped in the generally symmetrical fashion seen in BGAs, but has more irregular contours. The red regions at left have the lowest elevations, while the highest elevations are dark blue and, just above the white area, a small blue region that has the maximum elevations. The white area is actually a much smaller board attached to the larger board on the back side. The elevation of the top surface of this smaller board is so much higher than the elevations of contours on the larger board that it is white. But this smaller board has several holes drilled through it. Along the top edge of the smaller board, the outlines of the holes (i.e., vertical walls that reflect little

ultrasound) are visible. The blue distortion of the larger board in this region was likely caused by the attachment of this smaller board.

ASF can also image the populated side of the board, although the top surfaces of the components will be out of focus. In the areas not covered by components, ASF can map the topography of the top surface of a board having surface deformations, and it may be possible to estimate the risk of solder joint cracking or cracking within a component.

A printed circuit board may also have surface deformation caused by anomalies within the board. Generally this occurs when an anomaly in the board is very thick, or very close to the surface. ASF can map the local elevation change caused by these conditions, but if the anomaly is deep within the circuit board and very thin, the elevation changes on the board surface may be too slight to be mapped. **SMT**



Tom Adams is a consultant for Sonoscan.

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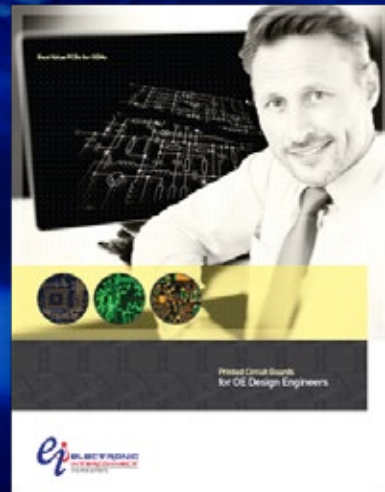
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Electronics Industry News

Market Highlights



Commercial Avionics Systems Market Driven by Modernization

According to a new market research report “Commercial Avionics Systems Market by Sub-segment, by Platform (fixed wing and rotary wing), and by Geography—Forecast 2014–2020,” published by MarketsandMarkets, the commercial avionics systems market was estimated at \$15,748.26 million in 2014, at a high CAGR of 7.06% from 2014–2020, to reach \$23,715.24 million by 2020.

Smart Home Automation System Market to Reach \$34B in 2020

Global revenues from smart home automation systems will grow at a 21% CAGR between 2015 and 2020, according to ABI Research, with North America accounting for the lion’s share of the market, followed by Europe and Asia-Pacific.

PC Shipments in EMEA Decline amid Currency Fluctuations

PC shipments in Europe, the Middle East, and Africa (EMEA) reached 20.2 million units in the first quarter of 2015—a 7.7% decrease year on year, according to International Data Corporation (IDC). After a strong 2014, the market returned to a decline as expected, with business renewals decelerating after last year’s uplift prompted by the end of Windows XP support.

Tablet Market Experiences Contraction amid Competition

Worldwide tablet shipments recorded a year-over-year decline for the second consecutive quarter in the first quarter of 2015 (1Q15). Overall shipments for tablets and 2-in-1 devices fell to 47.1 million in 1Q15, a -5.9% decline from the same quarter a year ago, according to preliminary data from the International Data Corporation (IDC) Worldwide Quarterly Tablet Tracker.

Automotive Powertrain IC Market Up 8.3% in 2014

IHS Technology forecasts that revenues related to powertrain semiconductors will increase with a compound annual growth rate (CAGR) of nearly

6% in the next five years, from \$7.2 billion in 2014 to \$9.5 billion in 2019.

IoT Adoption in India will Advance at a Slow Pace Through 2020

Indian enterprises are at the early stages of understanding the impact of the Internet of Things (IoT) on their business, according to Gartner, Inc. While the concept of IoT is not completely foreign to Indian enterprises, adoption will advance slowly through 2020.

In-Building Wireless Market to Reach \$9B by 2020

ABI Research’s latest In-Building Wireless market data forecasts that North America will drive the overall market while Europe and Asia-Pacific will pick up the pace during 2016. The market for in-building wireless equipment and deployments will more than double the current market by 2020.

TrendForce: More Worries than Hope in Q2 Panel Market

The prices for TV panels of mainstream sizes will hold steady in April as Chinese brand vendors are stocking up for Chinese Labor Day sales, according to WitsView.

Wearable Technology Market Forecast 2015–2020

The global wearable technology market has thus far not quite delivered upon previous expectations of revenues, consumer adoption and even technological advances. However, 2015 might be the breakthrough year in which wearables begin to achieve that mass market acceptance that has long been expected.

Wi-Fi Equipment Market to Recover

The worldwide consumer wi-fi equipment market increased 5% in 2014, surpassing 166.1 million unit shipments. “Shipments of devices which support the 802.11ac standard grew significantly in 2014, representing more than 11% of total access point shipments,” says Jake Saunders, VP and practice director, ABI Research.

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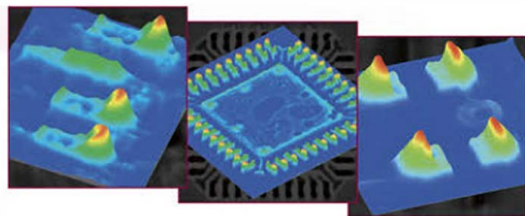
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/ The Future in Focus

Inspection:

The Last Line of Defense

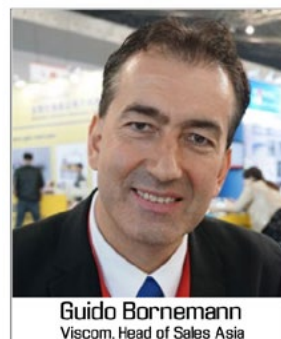
Traditionally a non-value-added step, inspection is still the best, last line of defense against defects and a bad reputation. In this interview conducted by Publisher Barry Matties, Viscom's Guido Bornemann discusses the true value of inspection and how to best use the tools to prevent defects, including head-in-pillow, from being shipped to customers.

Barry Matties: *Guido, tell me about Viscom's role in inspection.*

Guido Bornemann: We are one of the top three AOI/AXI makers in the world. We are a market leader in Europe with our stronghold mainly in the automotive industry. So in Europe we are growing, and now we are getting more active in China by addressing the contract manufacturers, EMS companies, and local Chinese automotive companies.

Matties: *The automotive industry certainly is growing in China—probably one of the largest areas of growth. I've been coming to China for nearly 15 years and there used to be more bikes than cars, and now you hardly see a bike. It's all about cars.*

Bornemann: We see that a lot of our main customers, especially those from Germany, are setting up factories here, like BMW, Audi, etc. They are all here. With this occurring, of course, their suppliers are coming here as well.



Guido Bornemann
Viscom, Head of Sales Asia

Matties: *We're seeing the same in America. Companies like Cadillac and Lincoln are introducing cars for the high-end Chinese market. But getting back to inspection, 3D is obviously a big area.*

Bornemann: It started with 3D SPI/3D AXI and now everybody's talking about 3D AOI. People are still figuring out, "What do I need? Do I need a full 3D? Do I need partial? Can I combine the best of worlds, 2D and 3D?" Then definitely there are certain defects where you really need 3D, but also situations where maybe 2D is absolutely fine.

Matties: *Doesn't it just depend on where they are in their process or their product development?*

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INSPECTION: THE LAST LINE OF DEFENSE *continues*

Bornemann: Yes, it basically depends on the design. If you have small chip components in the shadows of big ones, 3D is limited because you have shadowing. It's good to be able to switch back to 2D. Glass 2D is offering a higher resolution, working on the real images, and speed, of course.

Matties: *So when you first acquire the data for testing, how do you do that?*

Bornemann: We are working based on any kind of data where we need placement data, rotation and so on. So it could be Gerber data, it could be cut data, whatever they have. We are algorithm-based, so we import this into our software and then we assign our algorithms to their components and run the inspection. It's completely algorithm-based.

Matties: *Do you offer X-ray solutions also?*

Bornemann: We offer X-ray for both.

Matties: *So you can cover them from start to finish in the process of an inspection. I know head-in-pillow is a large issue, and with your X-ray technology you can at least prevent potentially defective products from being shipped.*

Bornemann: Head-in-pillow is one of the big issues and here we are working with very high-resolution systems. We are just launching our flat-panel, inline X-ray system, and with this we are able to cover the head-in-pillow issue.

Matties: *By the time the product gets to your process, it's already built; it's done. You're just preventing your customers from sending out a potentially bad board. You don't actually have them improve their process, do you?*

Bornemann: When you do the inspection at the end of the line it's basically too late, but

since we have inspection solutions for every test, whether it be an SPI, pre-reflow, post-reflow, AOI, or X-ray, we are communicating all along the line. We have installed a true yield, which is our feature to communicate between the machines, even with some pick-and-place machines and with some printers, in order to give customers information about the process, where the defects might happen, and how to countermeasure it.

Usually it happens either on the printing or in the oven. So if they are using an SPI, 3D SPI glass, and then the 3D AXI, we can help them determine when that occurs.

Matties: *Catching it at that early stage would save them a lot of capacity, time, and resource overall. How many customers have adopted that strategy?*

Bornemann: It's mainly the automotive customers who are really spending a lot on inspection for nearly every test.

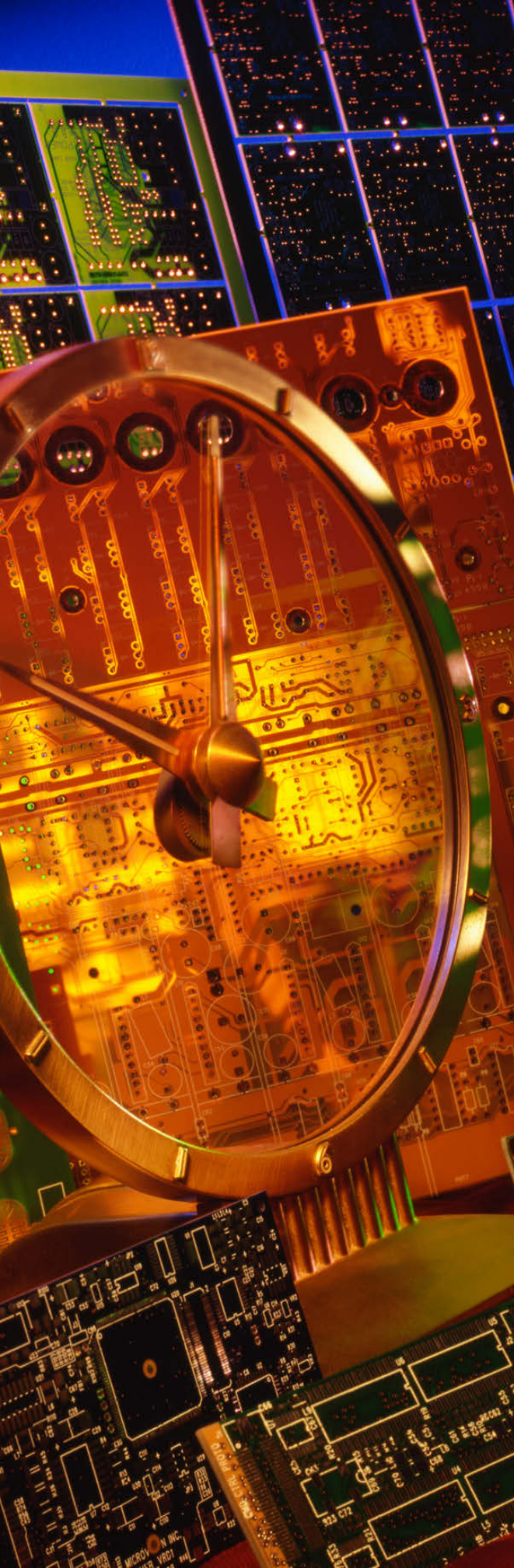
That's really a life-or-death situation. If an airbag is broken or the

anti-lock braking system is not working, it could be life or death. Automotive companies must make sure that every single defect is found. To find 80% of the defects is not really difficult, but it's also not enough. It might be okay for low-end products, but automotive must really find every single defect. Even if their process is fully optimized, they still need the inspection.

Matties: *That's really interesting because when you look at inspection as a stand-alone process, it doesn't add value at all. It only adds cost, but the cost of failure is so catastrophic that you have to do it.*

Bornemann: That basically was the case with AOI 10 years ago. With no value-add, people thought they didn't need it. In the end, they were forced by their customers to test and that's how AOI became a standard in today's lines.

“
If an airbag is broken or the anti-lock braking system is not working, it could be life or death. Automotive companies must make sure that every single defect is found. To find 80% of the defects is not really difficult, but it's also not enough.”



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INSPECTION: THE LAST LINE OF DEFENSE *continues*

Matties: *What sort of value-add can you bring to a customer that is forced to buy this?*

Bornemann: The process orientation is important. It helps to cut their cost.

Matties: *They get that from any inspection device though, right? Or is there some key data or information that you're doing that is unique?*

Bornemann: Basically, it is the communication all along the line. So it's not only between Viscom machines, but also between the printer and the pick-and-place machines.

Matties: *Are other inspection companies doing the same thing, and if so, how are you doing it better?*

Bornemann: Some companies only supply SPIs or maybe only supply the X-ray and AOI. I would say besides us, there is only one other supplier who is really supplying the whole range. We're bringing 30 years of experience to this.

Matties: *We talked about market segments. Is China still the fastest growing for you?*

Bornemann: Indeed, it is. Last year China and Asia contributed about 70–75%. We see Vietnam starting a little bit slowly. Thailand is picking up. We had some hopes for India, but it didn't develop like we expected. Now it is picking up a little bit. Korea is a little bit difficult for us, since our main competition is coming from there.

Matties: *What about North America? Is there any activity there for you?*

Bornemann: Yes, we have our offices in Atlanta and Mexico, and they had a really good year last year also.

Matties: *Automotive was really good last year. Is that now the core market for Viscom and where your key focus is?*

Bornemann: It is our standard market, but we had a rather big dive during the automotive crash, and back then we decided we needed to find customers outside of the automotive industry, so that's what we did. We set up new centers and increased our workforce in China. We set up global key accounting, which is really focusing on these customers, and that means more development. You need to be fast. You need to be flexible, and that's why we have set up a team specifically for this group of customers.

Matties: *When you talk about setting up teams, are you actually embedding into their organization and working out of their facilities and their test areas? Is that how you're doing it?*

Bornemann: We do both. It can be at customer facilities, but we have also just opened a new demo center in Shanghai where we have the whole range of available machines. We can invite customers there and can easily ship them

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INSPECTION: THE LAST LINE OF DEFENSE *continues*

very quickly to customers' facilities. It's more efficient for them and it's more efficient for us. Once they are satisfied or they feel that we are able to meet the requirements, we can also go on-site.

Matties: *What sort of demands do customers make?*

Bornemann: It is a very wide range. Typically, the first is non-escapee; absolute no escapee must go through for the high-speed factories. Of course, cycle time is a very important issue. They want to know how big the throughput is. More and more false-cause rate has been important; every false cause is wasting time and is a potential risk, because the operator might classify it wrongly. So a low false-cause rate has been one of the really big demands recently.

Matties: *Is that a big demand because the technology has shifted in the marketplace?*

Bornemann: Yes. You get more accurate results now, and what is also happening is that usually the escapees that slip through to customers are so-called human slips. It means the machine was right, but due to too many false causes the operator just pressed false cause. So every false cause is a risk for a human slip also.

Matties: *Switching gears a bit, where are you producing your machines?*

Bornemann: Our machines are made in Germany. All of the production and engineering is done in Germany. We do the camera modules ourselves, and the machines are hand-built. Singapore is our Asia headquarters, sales, administration, service and application support. Then we have a big China operation in Shanghai, Suzhou, Kunshan, Changchun, and Sanjiang, with resident engineers, application and service.

Matties: *Do you find the currency issue to be favorable?*

Bornemann: Most of our customers are still pay-

ing in Euros, so in that case it doesn't really affect us. But for those customers buying in U.S. dollars we are able to offer better prices. That's definitely favorable to us.

Matties: *What sort of service contracts do you require your customers to buy with your equipment?*

Bornemann: We are flexible in that regard. We offer carefree contracts, in which everything is included. We offer hour-by-hour, case-by-case issues where customers can buy a hundred hours at discounted rates. We offer maintenance contracts if they want us to do a maintenance calibration contract. Usually every contract is somewhat customized to what they need and what capabilities they have.

Matties: *What type of warranty do you offer with your equipment?*

Bornemann: We usually offer a 12-month warranty.

Matties: *Your machines, of course, are tied to the Internet, and you have access to the data linked together, as you're saying. How do you use that data? Do you ever look at it in an aggregate to see what the trends of quality are by region?*

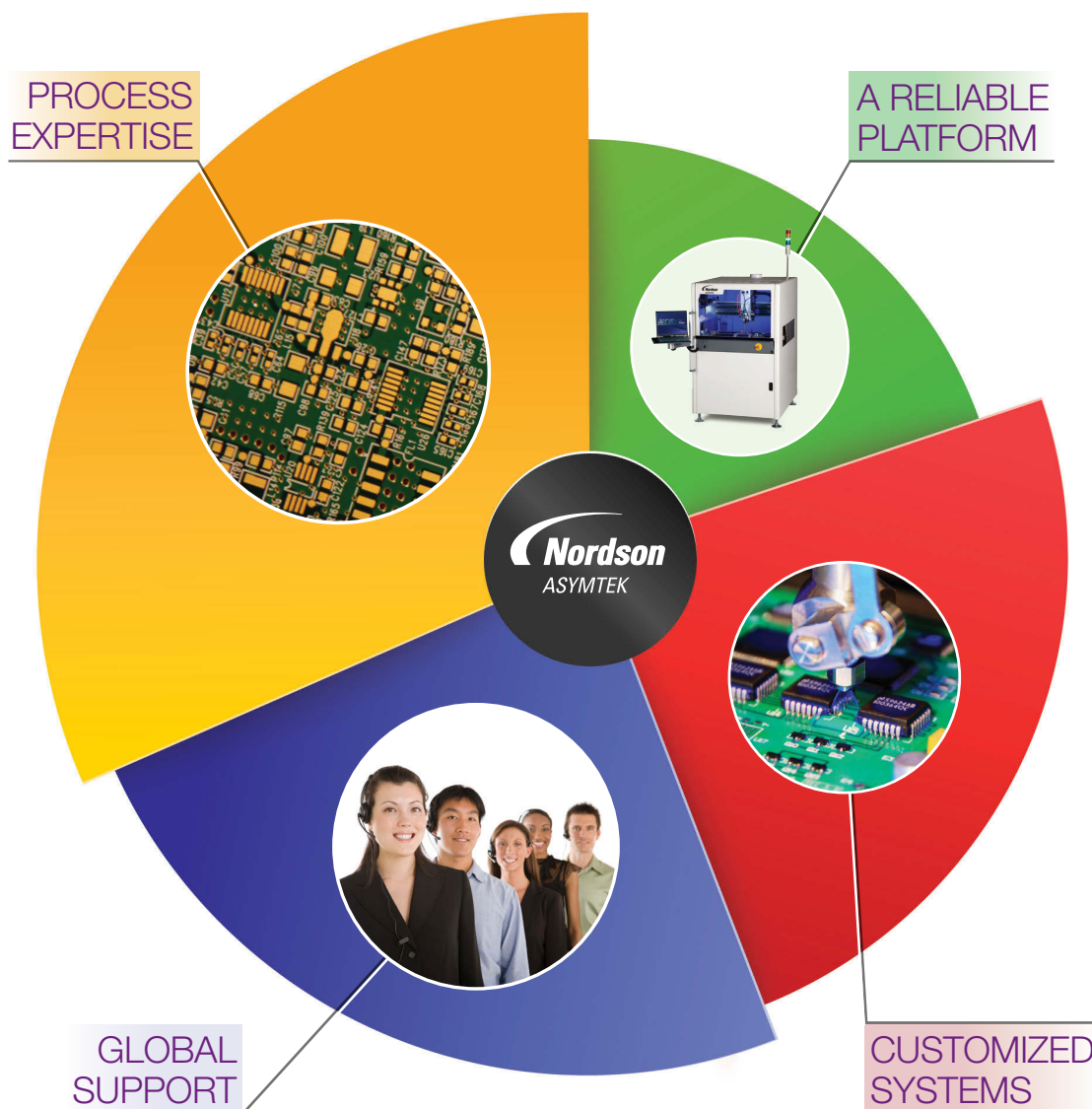
Bornemann: We are evaluating their performance by region, which is also a matter of service quality.

Matties: *Theoretically, with enough units placed in different regions, you could actually see who is building the highest quality products, by region. Have you ever looked at that data that way?*

Bornemann: No, we usually do it service-wise. So we are checking what typical downtime issues for each region are. We evaluate this by customer specifics to see where we need to do something, and mainly we are just using this to check our service property.

Matties: *That is interesting. And are you in medical as well? I would think their demands for quality are equal to automotive.*

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INSPECTION: THE LAST LINE OF DEFENSE *continues*

Bornemann: We are doing a couple of medical applications, but still we feel that automotive is definitely, considering China, the key driver of our business.

Matties: *Do you have any concerns about the auto collapse like we saw previously?*

Bornemann: Looking at the forecast for China, I don't see that. If we look at 20 million cars in China, that still leaves so many people without a car who have the money to buy cars now. And that is supposed to grow by up to five million cars per year. I'm not positive about how realistic it is, but these are the numbers we keep hearing, so I don't see anything happening in the next five years.

Matties: *What about their highways? Isn't the problem going to be how the highways are going to be able to support those numbers?*

Bornemann: That is the problem: the infrastruc-

ture. It's also interesting to see how the growing train business will influence car sales. They are building fast speed trains all over the country. Metro subways and public train systems are springing up even in cities I've never heard of, but still, I would say it's a rather stable growth.

Matties: *The interesting thing might be that if there's a crush of people buying cars, there will be so much traffic that they go back to using bicycles.*

Bornemann: Exactly. It might be e-bikes.

Matties: *Well, it's been a pleasure talking to you.*

Bornemann: Thank you very much for your time. **SMT**

Guido Bornemann is the head of sales for Viscom.

VIDEO INTERVIEW**Solving Inspection Problems with True 3D in AOI, AXI and SPI Systems**

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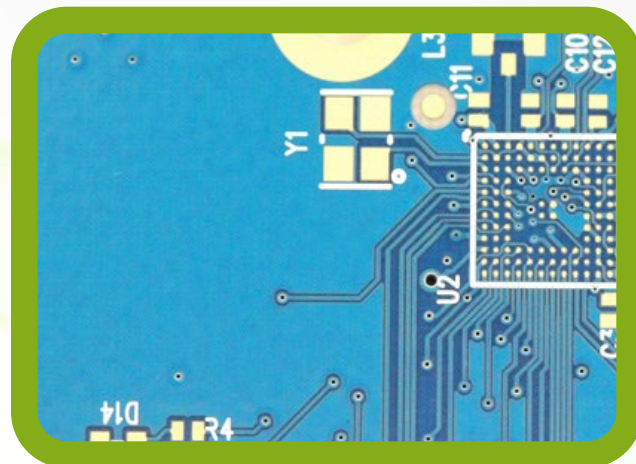
SAKI America's family of true, 3D inspection systems covers the whole spectrum of SPI, AOI and AXI tasks. Quintin Armstrong explains how the unique resolution capability of their AXI achieves 100% detection of head-in-pillow defects.



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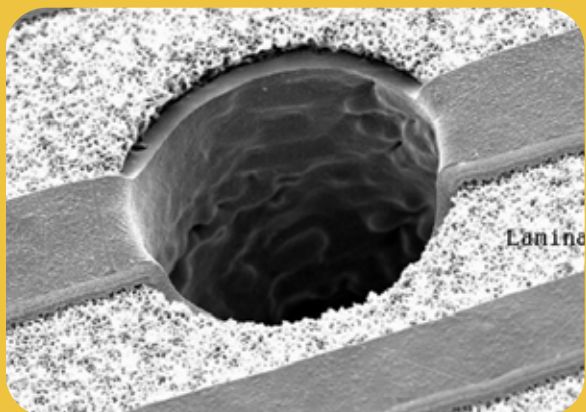
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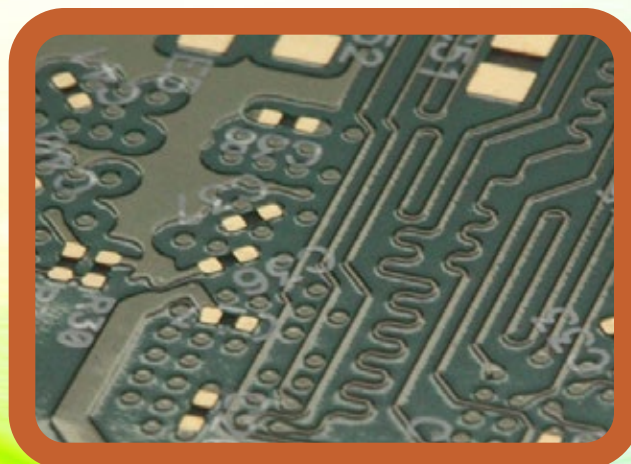


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SMT007 Supplier/New Product News Highlights



MIRTEC, YXLON Collaborate to Empower Industry 4.0

MIRTEC, the global leader in 3D AOI Technology and YXLON International, the leading industrial X-ray and computed tomography (CT) specialist, announce a new strategic cooperation which will empower yield improvement in the electronic manufacturing industry.

KYZEN Receives 50th Industry Award

KYZEN announces that it has been awarded a 2015 EM Asia Innovation Award in the category of Cleaning Materials for its AQUANOX A4708 pH Neutral Electronic Assembly Cleaning Chemistry. The award was presented to the company during an April 22, 2015 ceremony at the Shanghai World Expo Exhibition & Convention Center during NEPCON China.

Multitron Unveils New Square Light Guides

Multitron, the exclusive UK & ROI agent for the substantial German component manufacturer MENTOR, has announced the availability of a new range of Square Light Guides/Light Pipes.

LaserMicronics Assumes LDS Production for Festo BionicANTs

Festo AG & Co. KG from Esslingen has already presented a few engineered structures based on models from nature in the past. At this year's Hannover Fair, the company has chosen to demonstrate collaborative ants (BionicANTs) working together on tasks they could not accomplish alone.

Metcal Gets Best Presentation Award at SMTA China

Metcal is pleased to announce that SMTA China awarded its Applications Manager Paul Wood "The Best Presentation of Vendor Conference One," for the presentation titled "Why Non-Contact Array Solder Clean Up is Required."

Rocket EMS Ramps Up Inspection with Two V510 G2 Series AOIs

Rocket EMS Inc., a Silicon Valley-based full service EMS supplier, announced that it has purchased two V510 G2 Series AOI systems from ViTrox Technologies. The V510 G2 Series offers powerful technology and high throughput productivity for SMT line production.

Nordson MARCH Offers Free Technical Consulting Services

Nordson MARCH, a global leader in plasma processing technology, is offering free technical consulting on how plasma treatment systems reduce premature device failures in the field and ways your company can improve its manufacturing process through plasma cleaning.

Jeff Wettstein Joins Valtronic to Expand Midwest Reach

Valtronic, manufacturer of miniaturized electronic products for trusted medical device partners, announces that Jeff Wettstein has joined the Valtronic Technologies (USA), Inc. team as its newest sales engineer, directly reporting to Jay Wimer, president and CEO.

Engineered Material Systems Debuts CA-180 Low-Temp Cure Conductive Adhesive

Engineered Material Systems, a leading global supplier of electronic materials for circuit assembly applications, introduces its newest conductive adhesive—CA-180. The low-temperature cure conductive adhesive has been designed for die attach and general circuit assembly applications.

ZESTRON's VIGON EFM the AK-225 Alternative for Manual PCB Defluxing

ZESTRON, the global leading provider of high precision cleaning products, services and training solutions in the electronics manufacturing industry, has released the AK-225 alternative for manual PCB defluxing—VIGON EFM.



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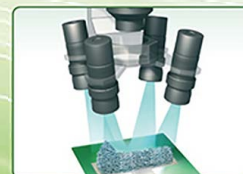
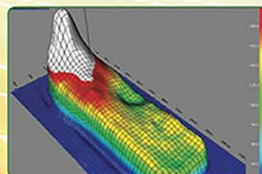
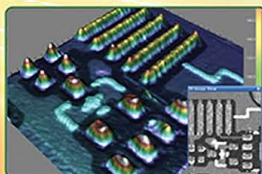
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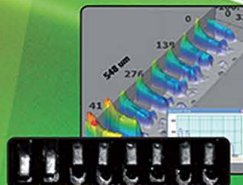
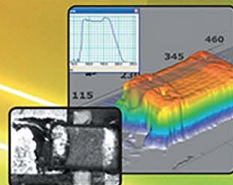
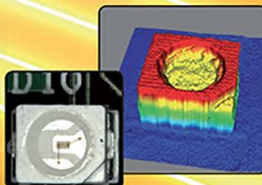
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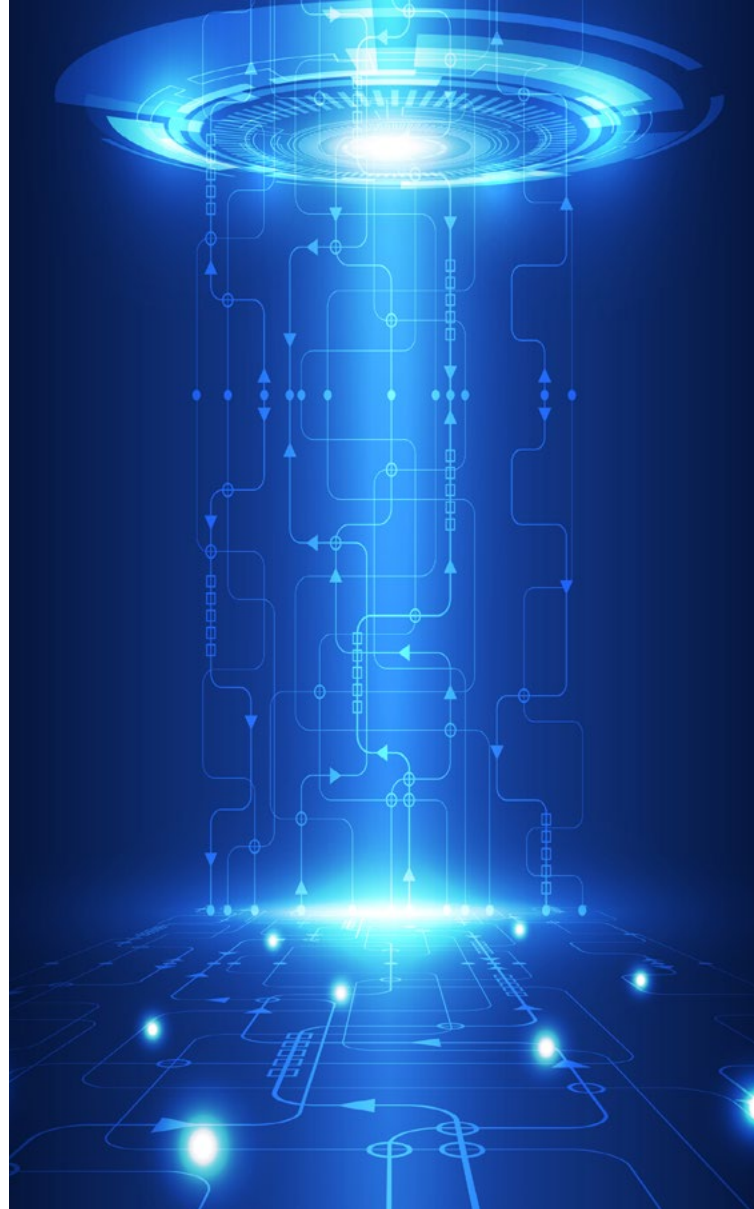
EVENT REVIEW: 6th Electronic Materials and Processes for Space Workshop (EMPS-6)

by **Barrie Dunn**
EMPS

EMPS-6 workshop was held on April 15–16 at the German Space Operations Centre (DLR), near Munich, Germany. The EMPS workshops are a University of Portsmouth School of Engineering initiative that started in 2010 with EMPS-1 and are held at least once per year, typically at one of the six ESA-approved skills training schools. The workshops are non-profit and held to develop and promote the materials and manufacturing processes utilised for spacecraft applications.

The modern lecture hall was filled by more than 70 enthusiastic engineers, academics and students from 17 countries, and 18 presentations were delivered during this two-day event. Organisers included the ESA skills training school managers Leo Schoeberle, IFE, and Karl Ring, ZVE; Dr. Jussi Hokka, ESA-Estec; Martin Wickham, NPL; Dr. Barrie Dunn and Dr. Misha Filip, UoP.

The opening address was given by Professor Dr. Felix Huber, director, Space Operations and Astronaut Training at the DLR site. Professor Huber described the work at DLR which covered space missions and the development of naviga-



tion systems such as the European GPS satellite system Galileo. The civilian Galileo programme is expected to include 30 satellites orbiting the earth at an altitude of 24,000 kms. This work has begun, and already Galileo spacecraft are transmitting signals to the DLR Command Center. An exciting development at DLR involves the successful construction of “robonauts” to support humans in space. Although seemingly science fiction, these robots have been developed and are being considered to be sent into space in order to take on tasks considered far too dangerous for humans.

During the workshop, delegates were given a short insight into the DLR Communications and Navigation facility which resembled a mini Houston, with screens showing the location of orbiting European spacecraft as well as a dedicated operations room having direct contact



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EVENT REVIEW: (EMPS-6) *continues*

with astronauts on board the International Space Station as it passes over Europe.

Dr. Giles Humpston of Cambridge Nanotherm Ltd, UK, kicked off the workshop session related to circuit technologies. Nanotherm was founded in 2010 and produces nanoceramic coatings on various aluminium alloys. These coatings are dense and have a high breakdown voltage ideal for electronic applications. The nanoceramic layer can be made to vary in colour from ivory-white to black (dependent on the composition of the aluminium alloy: the darker coatings are made on copper-containing aluminium alloys such as AA2024, and the white coatings are produced on purer grades of alloy). Inorganic PCBs can be manufactured from the ceramic-coated aluminium by adhering copper foil to the top surface of the nanoceramic. Such PCBs have a thermal conductivity of 115 W per mK. Assembly of components to these PCBs (with pre-drilled holes) is similar to the component assembly of conventional epoxy or polyimide-glass fibre PCBs. This fully inorganic substrate can operate to 350°C, and there is no outgassing-under-vacuum; with such a high thermal conductivity it is expected that this novel material will find many applications during the design of spacecraft electronics, combustion monitoring systems and craft heading to the inner planets, Mercury and Venus.

The following presentation was made by Ilknur Baylakoglu of the Saturn Engineering and Training Consultancy, Ankara, Turkey. She stressed the need for reliable PCBs for space missions. The manufacture of these conventional PCBs can involve about 180 individual process steps. Modern spacecraft PCBs are becoming smaller with increasing component density; new components are introduced early, possibly without sufficient reliability testing, and this combination is a potential driver for failure. The European space industries ECSS standards covering PCBs, such as the design rules, choice of materials and the qualification of manufacturing lines were described. Detailed examples were given of PCB failure modes, particularly those involving plated through vias (PTVs). Baylakoglu characterized the base laminates in terms of glass transition temperature, mechani-

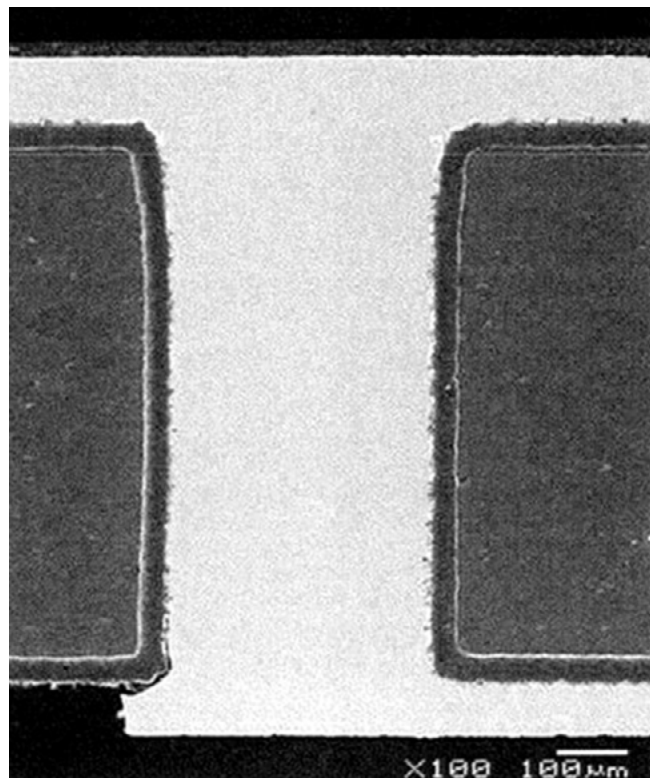


Figure 1: Pre-drilled aluminium panel, processed by the Nanotherm method to convert substrate to nanoceramic.

cal properties and other moduli. This well-focused presentation concluded with a series of photomicrographs showing the need for contamination-free production lines in order to obviate the growth of conductive anodic filaments and other electrical short circuit occurrences.

Dave Davitt from COMDEV, Canada, a global company manufacturing space hardware for communications, space science and remote sensing satellites, gave an interesting talk that focused on the use of passive electronics for low-risk satellite payloads. He described coaxial and stripline circuits for microwave devices and explained the difficulties faced for the electrical signal transition from these circuits to adjacent hardware. The RF VIA approach developed by COMDEV was outlined, together with the need for matched impedance. The circuit laminating difficulties often encountered were explained. Also, a series of manufacturing defects were highlighted by means of metallographic sec-



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EVENT REVIEW: (EMPS-6) *continues*

tions and recommended alternative processing methods were provided. An inhomogeneous stripline interface transition was detailed as a novel approach for designs incorporating a transition from alternate impedance circuits to standard 50 ohm impedance interfaces. This transition included a good degree of stress relief in the axial direction and this novel ISIT interface technology has been qualified for space use.

The following two presentations were made by Dr. Jan Vanfleteren from the IMEC Centre for Microsystems Technology, Gent University, Belgium. He reported on the manufacturing processes developed at IMEC for embedding ultra-thin chip packages into the thickness of both rigid and flexible printed circuit boards. Here, bare commercial semiconductor dies are thinned down to thicknesses of between 20 and 30 microns without losing their functionality. These chips are then embedded in spin-on polyimide material and, using thin-film technology and lithography, the fine pitch chip contact pads are fanned out to a more coarse pitch which is compatible for alignment and contacting with conventional PCBs. These IMAC packages have a thickness below 100 microns and they are mechanically flexible. The full description of the processes was described and physical samples were demonstrated to be completely bendable as they were passed around for assessment by the workshop participants.

Dr. Vanfleteren's second presentation was equally fascinating; it covered elastic and rigid 2.5D free-form circuits. The copper conductors on these flexible circuits were designed rather like springs so that they could elongate between 60% and 100% without failure. These substrates are made from elastic polymers (e.g., silicone rubbers or polyurethanes). Again, remarkable samples of (wearable) "blue light therapy" devices were passed around the audience. These stretchable electrical connections are thought

to have many interesting features for space applications. Due to their flexibility, such circuits could be incorporated as interconnections between highly bendable parts such as on solar arrays and even astronauts' spacesuits.

The next session concerned Processes and Re-processing and was started by Dr. Klas Brinkfeldt of Swera/IVF, Sweden, entitled, "Nanosilver Die Attach and other Emerging Technologies for Power Electronics." Dr. Brinkfeldt explained his sintered silver

particle material and demonstrated its use in a manufacturing process for low-volume, high-performance applications—particularly for the attachment of dies in power electronic units. Present common failure mechanisms in power electronic assemblies were illustrated using scanning electron fractographs (wire bond failures, delamination of substrate materials, and the cracking and fatigue of solder alloys, as well as burn-out failure mechanisms). The

use of sintered silver nanoparticles in an organic matrix was seen for a die attach application to be of similar, or better, reliability than conventional solder-attach processing. Thermal cycling of these die-attach configurations between -40°C and +125°C gave excellent results and, for power cycles between +45°C and +175°C, for the same silver sintered die attachments, up to 160 million power cycles can be envisaged from Coffin-Manson modeling. By using the same environmental testing cycles, present-day solder interconnections would fail at about 40,000 cycles. For real-life applications it was acknowledged that some precautions must be taken in order to avoid silver migration and resulting short circuiting; suitable coatings do exist and would need to be applied to these devices. Also, Dr. Brinkfeldt considered that the silver sintering process steps could be optimized, and should include a physical pressure cycle that would further enhance the adhesion between mating surfaces. The thermal management of compact, small scale power electronic

“
The copper conductors
on these flexible
circuits were designed
rather like springs
so that they could
elongate between
60% and 100%
without failure.”



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EVENT REVIEW: (EMPS-6) *continues*

systems can be improved and this will lead to extending their lifetimes: achievable by cooling component devices on both sides and by the selection of SiC-based substrates with high thermal conductivity. This presentation concluded with examples of SiC-based inverters for electric vehicles and the use of additive manufacturing heat sinks, all developed at Swera/IVF.

The re-processing of leadless semiconductor packages and column grid array (CGA) packages are part of the core business capabilities of Micross Components Ltd (Crewe, UK). Mark Walmsley discussed how lead-free terminations on a very wide range of component packages can be reprocessed at their Crewe facility into tin-lead technologies. The use of Sn-Pb terminations and Sn-Pb solder interconnections are known to have a higher reliability for military avionics, space, nuclear power and other critical applications—industries producing such hardware are exempt from the EU RoHS directives related to lead-free electronics. A new material/process for Micross involves the practice of using non-collapsible stand-offs incorporated within the solder interconnections of area grid array packages. These have been shown by environmental testing to be extremely reliable for both ceramic and plastic packages mounted onto a variety of PCB laminates. Where column grid arrays are concerned, Micross have transferred a “column last attached solder process” from IBM in the U.S. to their facility in Crewe. The so-called CLASP columns consist of 10/90 Sn/Pb columns with eutectic Sn/Pb end fillets; they have been approved by U.S. users and will be “qualified” using UK processed packages.

Don Tyler of Corfin Industries, Salem, New Hampshire, U.S., continued the theme of re-processing by describing his company’s facility for converting Pb-free ball grid arrays into tin-lead by “robotic hot solder dipping.” The use of lead-free terminations with tin-lead solder alloys results in weakened solder joints. This

so-called “mixed technology” is unreliable and Corfin Industries have been de-balling Pb-free BGAs using robotic systems for many years. The Pb-free spheres are removed over a solder wave in combination with forced hot air. The devices are then de-fluxed, cleaned and dried before re-balling in a programmable convection oven. Area grid array packages have been re-balled up to three times without appreciable loss of nickel or copper from their pads by dissolution into the liquid solder. Quality controls include scanning acoustic microscopy, cleanliness testing and solderability testing to IPC standards. Examples of all the processing steps were described and illustrated by means of a video film and photomicrographs of metallographic cross-sections.

Fernando Perez Garcia (CRISA, Airbus Defence and Space), Tres Cantos, Spain, delivered a challenging, if not controversial, talk concerning the complexity of gaining ESA qualification for surface mount technologies to be used for spacecraft. He discussed whisker mitigation methods and the possible use of Level 2C solder assembly philosophy per GEIA-STD-0005-2, where lead-free tin finishes are permitted under certain well defined circumstances.

Antti Rautiainen of Aalto University, Finland, has spent some time during his doctoral candidacy at ESA studying solid-liquid inter-diffusion bonding for MEMS sensor integration. This technique is based on the formation of intermetallic compounds between high and low melting point alloys. So-called SLID bonding offers high re-melting temperature interconnections with low processing temperatures and small footprints. Rautiainen compared other conventional metal bonding processes with SLID both in terms of manufacturing routes and resultant microstructures—mainly for Cu-Sn and Au-Sn final bond structures. He discussed reliability in terms of strength and environmental testing. The samples produced showed some

“
**Area grid array
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re-balled up to three
times without appreciable
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dissolution into the
liquid solder.**”

June 9

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June 9–10

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- SMT Problem Solving

June 10

ITI & IPC Conference on Emerging & Critical Environmental Product Requirements

Des Plaines, IL, USA

June 12

ITI & IPC Conference on Emerging & Critical Environmental Product Requirements

Milpitas, CA, USA (San Jose area)

September 27–October 1

IPC Fall Standards Development Committee Meetings

Rosemont, IL, USA

Co-located with SMTA International

September 28

IPC EMS Management Meeting

Rosemont, IL, USA

October 13

IPC Conference on Government Regulation

Essen, Germany

Discussion with international experts on regulatory issues

October 13–15

IPC Europe Forum: Innovation for Reliability

Essen, Germany

Practical applications for meeting reliability challenges like tin whiskers, with special focus on military-aerospace and automotive sectors

October 26–27

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November 2–6

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November 4

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December 2–4

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EVENT REVIEW: (EMPS-6) *continues*

voiding at the progressing Cu₃Sn intermetallic interfaces. Further work will be conducted at Aalto University to understand the reliability of hermetically sealed MEMS devices, together with the measurement of accurate leak rates.

The final session on the second day related to the failure modes or potential failure modes related to spacecraft electronics.

Ronald Schonholz from Isola-Group in Germany reviewed the well-known failure mechanism caused by the growth of conductive anodic filaments (CAF) within multi-layer boards. This is particularly a problem for spacecraft electronics due to their progressive miniaturization. Spacecraft PCBs can be subjected to moisture during ground testing, and also when assembled boards are thermal cycled from cold to hot environments they can be exposed to condensed water. The electrochemistry related to CAF for various laminates was discussed, in particular the weave of laminate glass fibre fabrics was deemed to be very important. New fabrics used by Isola have a more even distribution of glass filaments and are better wetted by resin during manufacture. These are so-called “spread fibres” with Silan finishes (providing a better Si-O-Si-coupling agent to polymer) result in a far better chemically bonded interfaces between glass and resin. Examples of CAF failures were demonstrated by metallographic images for the old fibre systems.

Following the CAF review, Poul Juul of the Hytek Institute, Aalborg, Denmark, demonstrated electro-chemical migration (ECM) between tracks on PCBs. Examples of ECM caused by flux residues were shown. Many examples of laminate failures were illustrated; their causes were said to be often related to insufficient bonding between resin and glass fibre, hollow fibres, poor drilling and void formation. Juul emphasised the urgent need to retain highly skilled persons in the European PCB manufacturing industry (process and chemical engineers, laboratory technicians and operators).

Inventec, part of the French Dehon Group, was represented by J.H. Serzisko. This company produces hydrofluoroethers which are clear, colourless and low odour liquids, partially halogenated carbon bonds, with low boiling points. This liquid material is used in specialised cleaning tanks for aerospace mechanisms, electronic assemblies, spacecraft mechanisms and fire protection systems.

This cleaning liquid meets all the legal requirements such as REACH and the cleaning equipment requires no local extraction.

Continuing with the theme of cleaning for spacecraft electronics, Graham Naisbitt, director of GEN3 Systems, Farnborough, UK, reviewed the topic of flux residues and the need to clean such contaminants prior to conformal coating. All fluxes leave residues which might compromise electronic assembly performance. It is essential to know

the electrochemistry of such fluxes and it is strongly recommended that the surface insulation resistance (SIR) of any residues that may be present after cleaning are fully understood. SIR and ROSE testing are the recommended methods for determining whether circuit reliability will be compromised by contaminants including the so-called “no-clean” flux residues. Other techniques such as ion chromatography may be effective at measuring the presence of ionic salts but the method is not suitable for assessing whether reliability will be compromised. SIR testing evaluates whether electrochemical failures may occur in the presence of humidity, ionic contamination and bias. Various ionic contamination test methods are available (ROSE and SEC). These determine the amount of salt (equivalent) remaining on both bare and component-assembled printed circuit boards. The tests involve a 75/25% mix of IPA with de-ionised water. The conductivity of the mix solution is known, and once a contaminated test PCB assembly is agitated in the solution a second reading computes the dissolved ionic

SIR and ROSE testing are the recommended methods for determining whether circuit reliability will be compromised by contaminants including the so-called “no-clean” flux residues.

contamination as micrograms/per sq cm NaCl equivalent. A new test method, process ionic contamination test (PICT) was discussed in detail, including the equipment and the criteria for specimens to pass or fail. The PICT test is described as an inexpensive fast and easy test to control an assembly process accurately.

Cathy Barnes, quality manager at Spur Electron Ltd, Havant, UK, then described the challenges and advantages of an independent laboratory as provider of expertise to the space and defense industries. The services of Spur include engineering and component procurement; they have an advanced manufacturing capability and an extensive laboratory. One of the greatest challenges of an independent laboratory is how information gained from failure investigations can be used to the benefit of the space industry

(due to non-disclosure agreements). However, analyses and verification programmes conducted for ESA have revealed many problem areas related to component and solder joint failures that can be shared with the entire space community. Problems related to the design and assembly of electronic circuits have been relayed to ESA and Eurospace in order to enhance relevant standards in the ECSS series. Barnes ended her talk by showing numerous unusual failures, some of which were caused by tin whisker growths.

The results of a tin whisker growth study using a standard accelerated environmental test following JESD22-A121A was described by Dimas J. Morilla of Alter Technology, Seville, Spain. This is a JEDEC test designed to assess the susceptibility of commercial tin plated com-

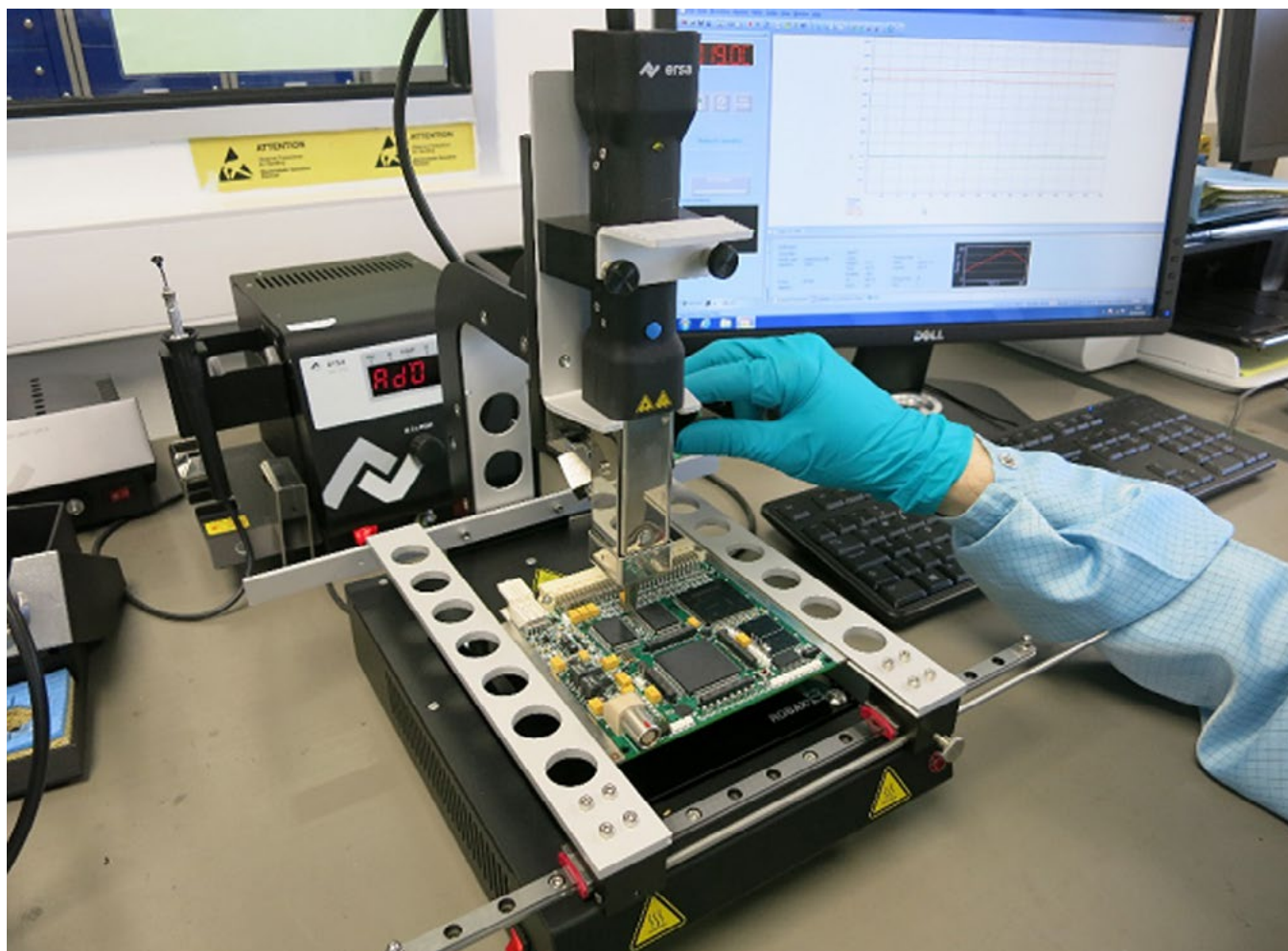


Figure 2: Installation of components on a spacecraft PCB by hot air reflow^[1].

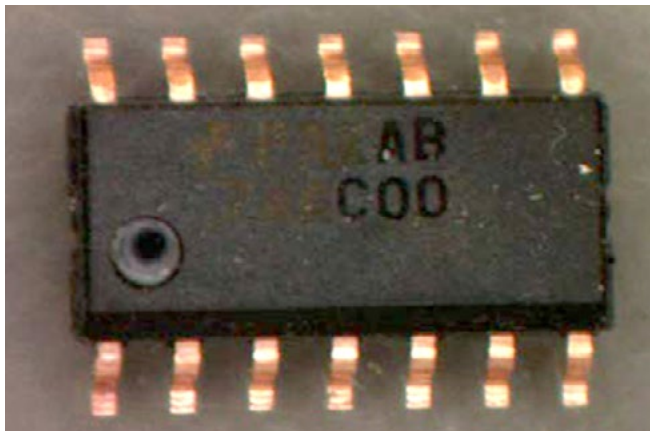
EVENT REVIEW: (EMPS-6) *continues*

Figure 3: Pure tin stripping up to package body without removing package identification, for space and military circuits using a standard chemical process; leads are then pre-tinned with eutectic solder^[1].

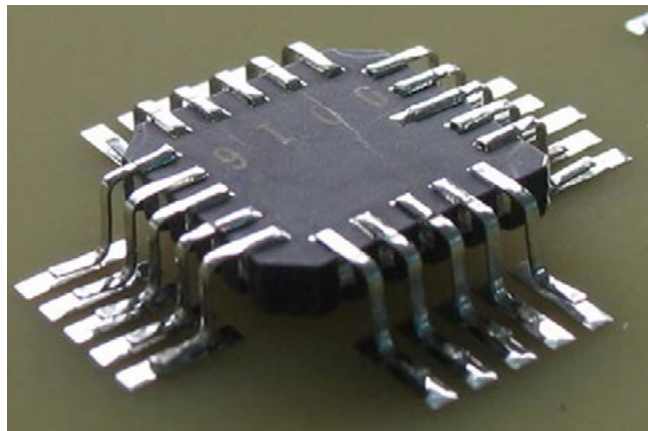


Figure 4: Modification of interconnection design to ensure absence of thermal fatigue under severe thermal cycling environments^[1].

ponents for whisker growth. The numerous past failures caused by tin whiskers were related to satellites, heart pacemakers and the shutdown of nuclear power stations. The Alter Technology test samples included surface mount devices having two tin-plated terminations (chips). These results will be published during 2015. However there is some controversy concerning the JEDEC standard (only whiskers greater than 40 microns are considered potentially harmful and whiskers shorter than 40 microns are acceptable).

As this is a short-term accelerated test it is not suitable for space electronics. Out of three lots of testing, the first lot showed three parts having one whisker each, with lengths of 99, 57 and 112 microns, respectively. The second lot showed two parts with whiskers up to 122 microns and the third lot showed 41 whiskers of up to 192 microns in length. Reliability testing was considered essential whenever tin finishes are envisaged. For long-life electronics the JEDEC standard is probably not suitable. The best strategy, considered by Alter Technology, is to avoid using pure tin-plating on any component parts. Morilla also discussed mitigation strategies that included conformal coating, the use of a nickel barrier layer and component baking treatments. It should be noted that the test components did include a nickel barrier layer

between substrate and tin-plating but this was found to be an ineffective mitigation method. Reference was also made to the *Guidelines for a Lead-free Control Plan*, published by ESA.

The final paper also concerned tin whisker growths and was given by Martin Wickham of the National Physical Laboratory, Teddington, UK. Wickham compiled the results of many whisker growth studies performed at NPL, and particularly the study of various families of conformal coatings applied to tin-plated plates, and their ability to prevent short circuits. All coatings are better than no coatings; whisker growth is greatest at edges where coatings may be thin—it was noted that whiskers can grow at any time to cause electrically intermittent contacts. Other studies were made using “real assemblies” that included integrated circuits having tin-plated Olin 194 lead frames where the leads were heat treated for 15 minutes at various temperatures up to 150°C; some were reflowed at 230°C. It was noticed that increasing the temperature of heat treatment (and also reflow) delayed the time for the first whisker to appear. These tests are continuing, but it is reported that the uncoated control samples have “shorted extensively,” and all samples will be revisited/inspected biannually. Wickham enquired whether additional companies might support these studies, particularly when con-

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EVENT REVIEW: (EMPS-6) *continues*

Figure 5: Delegates from the EMPS-6 workshop who attended the tour and dinner at the Kloster Andechs, near Munich.

sidering the effect of vibration and forced air cooling on whiskers emanating from tin-plated component leads.

The workshop dinner was held at Kloster Andechs, a large property consisting of a beautiful hill-top chapel and an adjoining brewery, owned and run by an order of Benedictine monks. They provided our large group with a specially brewed beer and a simple, but excellent supper. Seating during this warm sunny evening was in a beer garden with a spectacular view over the surrounding Bavarian countryside. **SMT**

For those interested to present their work, or attend, the next Workshop (EMPS-7) will be hosted by Bill Strachan and Dr. Misha Filip at

the University of Portsmouth, UK, on 13–14 April, 2016. Details will be announced on the [website](#).

For more information on past EMPS workshops, [click here](#).

1. Adapted from Cathy Barnes' paper on Spur Electron's capability as an independent SME.



Barrie Dunn is an EMPS co-founder and Professor at the University of Portsmouth (previously with the European Space Agency).

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EU Votes to Make Mandatory Certification Regarding Conflict Minerals

The International Trade Committee of the European Parliament (INTA) voted on amendments to the EU's conflict minerals regulation that were proposed by its members. The INTA voted to make mandatory the proposed voluntary system of certification for EU smelters and refiners.

Kitron Posts Revenue Growth in Q1

Kitron ASA today reported the fourth consecutive quarter of improved profits, due to a combination of growing revenue and cost initiatives. Kitron's revenue amounted to NOK 471 million, an increase from 436 million in the first quarter of 2014.

Sonobuoy Tech Systems Wins \$9.4M in Foreign Sales Contracts

Sparton Corporation and Ultra Electronics USSI, a subsidiary of Ultra Electronics Holdings plc (ULE), announce the award of subcontracts valued at \$9.4 million from their ERAPSCO/SonobuoyTech Systems joint venture.

Benchmark Electronics' Angleton, Texas Facility Earns AS9100

Benchmark Electronics Inc., a leading integrated contract manufacturing provider, today announced that its Angleton, Texas manufacturing facility recently achieved the aerospace AS9100C quality certification.

PartnerTech, Kongsberg Devotek Initiate Cooperation

PartnerTech and Kongsberg Devotek, a leading Norwegian technology company in product development, have entered an agreement to cooperate around a joint offering to product-owner customers, with complete service from the concept stage to the finished product.

Celestica Receives Supplier Excellence Award from Diebold

Celestica Inc., a global leader in the delivery of end-to-end product lifecycle solutions, today an-

nounced that it has received the 2014 Platinum Award for Supplier Excellence from Diebold Incorporated. This is the second consecutive year Celestica has been recognized with this prestigious award.

Sypris Electronics Posts Revenue of \$8.9M in Q1

Revenue for Sypris Electronics was \$8.9 million in the first quarter of 2015 compared to \$8.4 million in the prior year period, reflecting the ramp-up of a new electronic manufacturing services program, partially offset by declines in engineering services due to the completion of a program during the period.

Season Group's Multiple Sites Earn AS9100 Certification

Season Group has recently obtained AS9100 certification for its Toronto, Canada and Havant, UK facilities, adding to the approval already in place for its facility in Penang, Malaysia. Having invested in developing facilities with TS16949 and ISO13485 capabilities over recent years, Season Group saw an increasing demand for its global services from a number of major aerospace and defence companies.

NATEL and OnCore Rebrand as NEO Tech

NATEL Engineering Company, Inc. and OnCore Manufacturing, LLC announced today that the merged company will be named: NEO Technology Solutions (NEO Tech). The name NEO Tech captures and combines the company's legacy members, NATEL Engineering, EPIC Technologies, and OnCore Manufacturing, while creating a name on which to build a brand.

Kitron Secures Order from Kongsberg

Kitron has, through its subsidiary Kitron AS in Arendal, received an order from Kongsberg Defence & Aerospace AS for military communications equipment. The equipment to be supplied is linked to contracts for deliveries to Hungary.

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In-Circuit Pin Testing: An Excellent Potential Source of Value Creation

by **Mitch Holtzer**

ALPHA

In-circuit pin testing (ICT) is a common method of inspecting electronic assemblies to measure the effectiveness of the assembly process and to predict electrical functionality. Test probes are put in contact with dedicated test points along the surface of an assembly, checking for electrical functions such as resistance, capacitance inductance and signal timing. Some circuit assemblers use functional testing for quality assurance as a substitute for ICT. In this example, the entire assembly either works or it doesn't.

Unlike printing paste, placing components and reflowing solder, ICT is considered a non-value added process. In fact, ICT increases the cycle time of the assembly process. If the ICT is a fail, but the circuit being tested is actually good (known as a false negative), even more time is wasted trying to determine whether or not a good assembly will function properly.

The two basic types of ICT are commonly referred to as clamshell and flying probe (Figures 1 and 2).

The clamshell ICT simultaneously tests dozens of points on a single board. One laboratory type of clamshell ICT device uses three types of pins and four different forces. Crown, spear, and blade pins are shown in Figure 4. A test vehicle

is placed in the clamshell fixture. The clamshell is closed, and electrical resistivity is measured at each of the test pins.

Although clamshell devices are commonly used, they are somewhat impractical for testing solder paste and flux's ability to be probed. Typically, there can be a 15-minute cycle time per test. Pin residue build up generally occurs after hundreds of tests. Cleaning flux build-up from pins is time-consuming, but necessary to minimize false negative readings.

Clamshell fixtures are quite expensive. A customized fixture must be fabricated for each unique assembly. This cost is only justified for the testing of high-value or high-volume assemblies.

Flying probe testing is also commonly used for lower value or lower volume assemblies. Flying probes test sequences are determined by easily changeable programming inputs. Clamshell fixtures are not required. Therefore, this type of test method is more suited for high mix circuit assembly applications.

In a common laboratory flying probe procedure, one pin type and one force are used, but the test runs for a total of 4,000 strikes. Flux build-up on the pins is an important part of the



Figure 1: Clamshell ICT device.

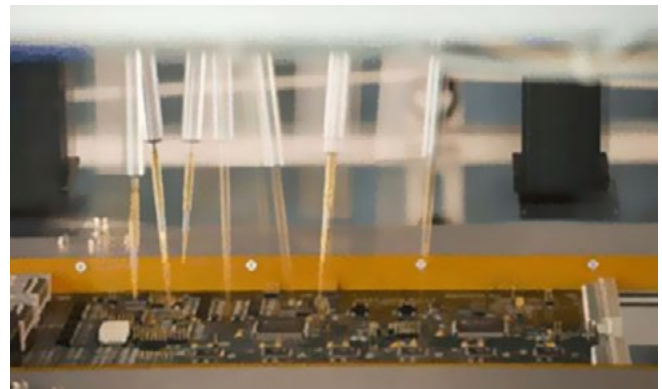
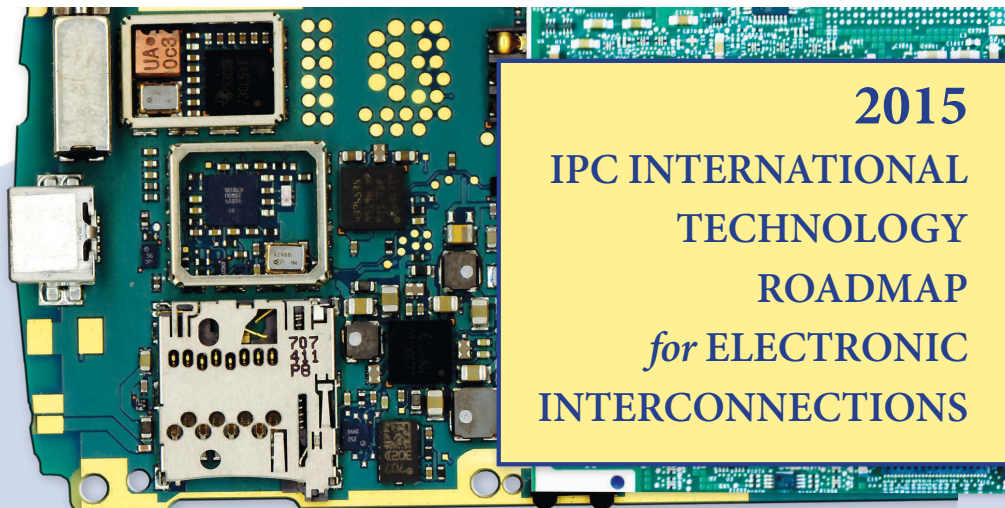


Figure 2: Flying probe ICT device.



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IN-CIRCUIT PIN TESTING: *continues*

Pin Shape	Force (oz)
Crown	2
	4
	6
	8
Blade	2
	4
	6
	8
Spear	2
	4
	6
	8

Figure 3: Combinations of force and pin shape used in clamshell test device.

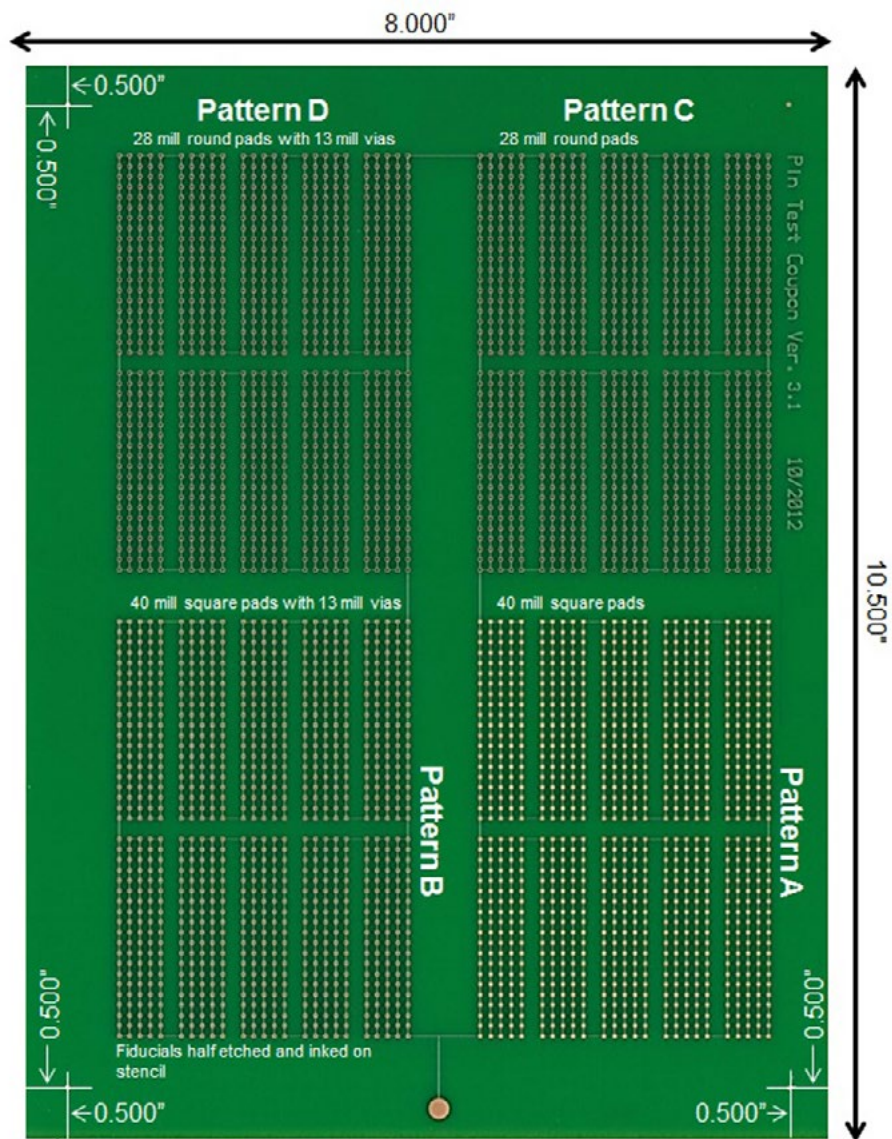


Figure 5: A value-in-use model, based on the first-pass yield of paste A versus paste S. Simple modeling was confirmed that the savings in first-pass yield was \$128 for every kilogram of paste used.

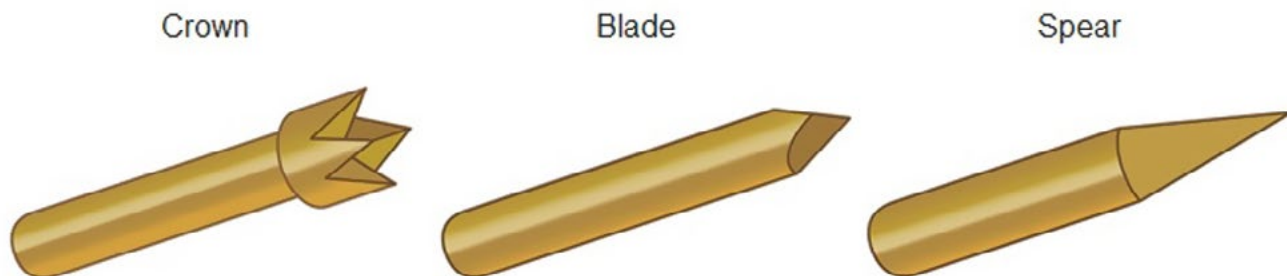


Figure 4: Three common pin shapes.

IN-CIRCUIT PIN TESTING: *continues*

test. In addition, one common laboratory test vehicle contains four different types of pads. In this example, pad A is a 40 mil (1 mm) square pad without vias, pad B is a 40 mil (1 mm) square pad with 13 mil (0.33 mm) vias, pad C is a 28 mil (0.7 mm) round pad without vias, and pad D is a 28 mil (0.77 mm) round pad with 13 mil (0.33 mm) vias. (Figure 5). There are 1,000 opportunities for each pad type.

Pads with vias tend to collect more flux residue and generally have lower yield for a given paste or wave soldering/selective soldering flux. Often these pads are the source of discrimination between high performing paste and flux, because the first pass yield is somewhere between 0 and 100%. Tests that show 0% or 100% yield are never good tests for discriminating between the efficacy of material sets.

Having said that, value is created when the first pass yield of the ICT approaches 100%. This means that the pin probe is able to penetrate flux residue and make positive contact with the test point in the circuit. Value is lost when the probe

does not make a low resistance reading with a fully functioning test point, but the test shows an open or high-resistance circuit. This is a false negative. Even though the assembly is perfectly functional, re-testing and extra handling are required, increasing the assembly cycle time.

Based on actual test data, a value-in-use model has been created to estimate the value of increased first pass ICT yields. A leading competitive paste has been tested using both the clamshell and flying probe method discussed above.

In-circuit paste testing accuracy is a significant competitive advantage. If the paste or flux residue is not conducive to clamshell or flying probe test accuracy, you may quickly fall behind in an increasingly competitive marketplace. **SMT**



Mitch Holtzer is global director of customer technical service (CTS) for Alpha. To reach Holtzer, [click here](#).

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Recent Highlights from SMT007

1 **Zentech: Expanding EMS Solutions and Supporting Innovation**

Zentech CEO and President Matt Turpin sat down with I-Connect007 Publisher Barry Matties recently for a wide-ranging discussion on the state of both domestic and global manufacturing, and Zentech's recent acquisition that will significantly expand the company's capabilities. They also addressed supply chain issues, automation, regulations, and the importance of STEM education in the U.S.

3 **NEPCON China Showcases Latest Manufacturing Tech in Asia**

Considered Asia's most influential SMT and electronics manufacturing event, NEPCON China 2015 attracted over 450 leading brands from 22 countries, and showcased the latest electronics manufacturing technologies and products across an exhibition area of 25,000 sqm. I-Connect007 is on hand again this year with exclusive interviews and photos from the show floor.

2 **Solder Paste Stencil Design for Optimal QFN Yield and Reliability**

During the past 15 years, the implementation of the QFN/BTC package has garnered a great amount of attention due to the assembly and inspection process challenges associated with the package. The difference in solder application parameters between the center pad and the perimeter pads complicates stencil design, and must be given special attention to balance the dissimilar requirements.

4 **Zentech Manufacturing Acquires Colonial Assembly and Design**

The acquisition provides tremendous synergy with Zentech's established customer set in the DoD and military C4ISR (command, control, computers, communications, intelligence, surveillance, reconnaissance) sectors while also providing enhanced engineering, product design, circuit design, machining, over-molded cable assembly and wire harnessing capabilities to the Zentech portfolio.

5 Jabil Opens Innovation Center

Strategically located in the Silicon Valley, the 100,000-square-foot Blue Sky Center features Jabil's intelligent digital supply chain toolset called Jabil inControl, factory-of-the-future technologies, state-of-the-art IoT and rapid prototyping labs, as well as access to advanced capabilities for increasing customer collaboration and product innovation.

6 Solder Jet Printing: Is It the Right Time?

Publisher Barry Matties gets an update from Nico Coenen, sales director for Mycronic, on their solder jet printing system. Mycronic has been developing and pioneering this technology for 10 years and they believe now is the time for it to gain real traction. One thing is certain; solder jet printing certainly has advanced and could make a big difference in process and quality.

7 Electronics Industry Leaders Urge Full Funding of NNMI

Top executives from leading electronics companies across the United States are calling on Congress to provide robust funding for the new National Network for Manufacturing Innovation (NNMI), as they gather in Washington, D.C. for IMPACT 2015: IPC on Capitol Hill.

8 SJIT, Solder Joint Integrity Test, To Find Latent Defects in Printed Wiring Board Assembly

Capacitance method and IEEE 1149.1 or boundary scan method are often used to find opens between component leads and pads on a printed wiring board. These methods, however, can find complete opens or complete shorts only. There is a method to find such latent defects by using 4-wire small resistance measurement technique.

9 IPC Posts Committee Reports from IPC APEX EXPO 2015

These standards committee reports from IPC APEX EXPO 2015 have been compiled to help keep you up to date on IPC standards committee activities. This is the first in a series of reports.

10 Celestica's Q1 Results Meet Guidance

"Celestica delivered revenue and adjusted earnings per share in line with our guidance," said Craig Muhlhauser, Celestica's president and CEO. "Despite a challenging demand environment, we also delivered year-over-year improvement in free cash flow, driven by our continued strong operational performance throughout our global network."

SMT007.com for the latest SMT news and information—anywhere, anytime.



EVENTS



For the IPC's Calendar of Events, click [here](#).

For the SMTA Calendar of Events, click [here](#).

For the INEMI Calendar, click [here](#).

For a complete listing, check out *SMT Magazine's* full events calendar [here](#).

IPCA 2015

June 3–5, 2015
Tokyo, Japan

Huntsville Expo & Tech Forum

June 4, 2015
Huntsville, Alabama, USA

NCEDAR 2015

June 4–5, 2015
Bangalore, India

IPC Technical Education Courses

June 9–10, 2015
Chicago, Illinois, USA

SEMICON Russia

June 17–18, 2015
Moscow, Russia

Philadelphia Expo & Tech Forum

June 18, 2015
King of Prussia, Pennsylvania, USA

Symposium on Counterfeit Parts and Materials—Tabletop Exhibition

June 23–24, 2015
Hyattsville, Maryland, USA

Upper Midwest Expo & Tech Forum

Jun 25, 2015
Minnetonka, Minnesota, USA

SEMICON West

July 14–16, 2015
San Francisco, California, USA

Ohio Expo & Tech Forum

July 16, 2015
Cleveland, Ohio, USA



PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

SALES MANAGER: **BARB HOCKADAY**
(916) 608-0660; barb@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

EDITORIAL:
MANAGING EDITOR: **LISA LUCKE**
(209) 304-4011; lisa@iconnect007.com,

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

EDITORIAL ADVISORY BOARD:

BILL COLEMAN, PH.D., Photo Stencil

HAPPY HOLDEN, IPC and SMTA

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MAGAZINE PRODUCTION CREW:

PRODUCTION MANAGER: **SHELLY STEIN** shelly@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **SHELLY STEIN, MIKE RADOGNA**

INNOVATIVE TECHNOLOGY: **BRYSON MATTIES**

COVER: **SHELLY STEIN**

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Coming Soon to ***SMT Magazine:***

JULY:

**Supply Chain
Management**

AUGUST:

**The War on
Process Failure**