ENGINEERING SOLUTIONS FOR PCB MANUFACTURING



Mechanical Reliability: A New Method to Forecast Drop Shock Performance p.30

Signal Integrity in Test Fixtures p.50

MAY 2014

PCBA Test: Enabling the Right Management Practice p.58

The Changing Economics of In-Circuit Test p.64

SUNSTORE CON

The Future of Test p.78

Test & Inspection of Electronic Assemblies





THE best way to find a PCB fabricator, anywhere.



Quick Search



Advanced Search



A few words from our clients.



"...Not only did we gain the potential of a valued new customer, we also had the eyes of a skilled PCB expert reviewing our operations and systems providing some positive and constructive feedback."

Steve Robinson President, APCT, Inc.

View full testimonial

" ...with Rob's years of experience performing audits and his vast knowledge, I believe Wizlogix and my end customers are benefiting. Moving forward, we will continue to explore more opportunities and collaborations with Next Level PCB services in the future."

Shawn Ng

Director/Co-Founder, Wizlogix Pte Ltd

View full testimonial

We offer a full range of auditing services for both buyers and sellers, backed by 35 years of industry experience. We'd love to talk with you about getting to the next level.

Say hello to us



(360) 531-3495 www.nextlevelpcb.com

SM[°]L

May 2014 Featured Content

TEST & INSPECTION OF ELECTRONIC ASSEMBLIES

This month, our expert contributors shine a spotlight on the test and inspection of PCB assemblies. How can you ensure signal integrity in your test fixtures? What is the state of the ICT landscape? How can you utilize X-ray inspection to detect head-in-pillow defects? What's the best way to predict drop shock performance? How can executives best manage PCBA test, now and into the future? Read on!

16 Head-in-Pillow X-ray Inspection

by Alejandro Castellanos, Dr. Zhen (Jane) Feng, David Geiger, and Murad Kurwa



30 Mechanical Reliability: A New Method to Forecast Drop Shock Performance

by Ronald Frosch, Guenther Mayr, and Manfred Riedler



50 Signal Integrity in Test Fixtures *by Rob Humphrey*



58 PCBA Test: Enabling the Right Management Practice



64 The Changing Economics of In-Circuit Test

by Alan Albee



78 The Future of Test by Richard Ayes



The SMT Source^{**} Latest News About Manncorp May 2014 SMT Assembly Equipment Flexible Pick & Place for High-Mix S

MC400



0

Manncorp

5000 CPH MC-385V1V \$49,995 More Info



4-HEAD 10,500 CPH Maximum speed, PCB size and feeder capacity MC-388 \$99,995 More Info



8.000 CPH

Dual-head version of MC-385V1V MC-385V2V \$59,995 More Info



LED PLACEMENT 4-heads, 15K CPH, PCBs up to 1.8m long MC-LEDV4 \$59,995 More Info



STARTUP

MC-400 \$39,995

More Info

PRODUCTION Full vision placement of 0201s, BGAs, 15 mil QFPs

EXTRA CAPACITY 23.6" x 13.8" placement area; up to 160 feeders MC-392 \$69,995 More Info

BENCHTOP Full vision placement of 0402s, BGAs, 25 mil QFPs FVX \$29,995 More Info

© 2014 by Manncorp

Monnee FF 💟 🚜 👥 ୶ East Coast (Huntingdon Valley, PA) 800.PIK.MANN (745.6266) • West Coast (San Diego, CA) 888.PIK.MANN (745.6266)

Mexico: 52 1 656 217 8215

MAY 2014 VOLUME 29 NUMBER 5 www.smtmagazine.com



ENGINEERING SOLUTIONS FOR PCB MANUFACTURING

CONTENTS



COLUMNS 8 Googlebotics by Ray Rasmussen



12 Tin Whiskers, Part 5: Impact of Testing Conditions by Dr. Jennie S. Hwang



46 A Strategy for Design-Through-Manufacturing

by Dan Hoz



86 Independent Distributor: Supply Chain's Best Friend or Worst Enemy by Todd Kramer



94 LED the Sunshine In by Sjef van Gastel



NEWS HIGHLIGHTS 76 Market

- 84 Mil/Aero
- 92 Supplier/New Product
- 98 SMTonline

VIDEO INTERVIEWS 11 Do You Know it All? Training is Essential!



49 Dealing With Counterfeit Components



57 Scienscope Introduces X-Ray Inspection Equipment



SHORTS

- 15 Flexible Carbon Nanotube Circuits Made More Reliable
- 44 Samsung Develops Method to Commercialize Graphene

EXTRAS 100 Events Calendar



101 Advertiser Index & Masthead

CLICK FOR VIDEO PRESENTATION

illilli



(>)

FREE PARTS

LET US FABRICATE AND ASSEMBLE YOUR BOARDS, AND WE WILL PAY UP TO \$500 FOR THE PARTS.

FIRST TIME CUSTOMERS ONLY UP TO 10 PIECES



THE WAY I SEE IT

Googlebotics

by Ray Rasmussen PUBLISHER, I-CONNECT007

January's big news was that Google was getting into robotics in a big way with some very strategic acquisitions. In February we heard that Foxconn and Google were partnering to build the "factory of the future."

In an interview with <u>The Observer</u>, Ray Kurzweil, Google's director of engineering, believes that by 2029 computer systems (automation and robotics included) will be as smart as people and much more capable. Kurzweil, famous as a futurist and focused on the exponential changes in technologies, predicted the Internet, among other technology breakthroughs. He also predicts that that by 2030, solar energy will be able to meet all the energy needs of the planet. That's just 15 years away!



If you're interested in gaining a better understanding of the difference between robotics and automation, <u>check out this link</u>.

As I've mentioned before, robotics are going to have a profound effect on people, both positively and negatively. In fact, I believe the automated and robotic factory along with the evermore automated business will dramatically change our society—it has to. IPC APEX keynote speaker and X-Prize Founder Dr. Peter Diamandis talked about this very issue during his presentation. What's both exciting and scary at the same time is that, as he pointed out, technological change is accelerating and our society is transforming into what he called "technological socialism" as machines replace workers. Societies will need





Living proof that flying dragons are real! Dragon Circuits is proud to be at the forefront in unmanned aviation.

Interested in unmanned aerial or ground vehicles? Dragon Circuits is developing the newest technology to enhance vehicle run-time, performance and durability to put your company at the top of the industry. Proprietary electronics, built in the USA with ITAR, AS9100 and MIL-SPEC standards. Contact us for more information on a range of services from design, manufacturing, and even flight school!

LEARN MORE »

www.dragoncircuits.com | 972.790.7610

TS

GOOGLEBOTICS continues



Figure 1: iRobot Ava 500 brings together iRobot's autonomous navigation with Cisco telepresence to deliver a new level of collaboration for office environments and other facilities.

to come up with ways to keep people busy. I think we'll figure it out over time, but there will be a rough patch as companies transition to the factories of the future and replace hundreds of millions of jobs over the next decade. In other words, it's here, now. We've arrived!

To understand where I'm coming from you have to let your imagination run a bit. You can start this exercise by thinking about where automation and robotic systems won't work. That's a bit easier than trying to come up with all the ways they will. The experts say that if you're into landscaping maintenance, that'll probably remain a manual task, mostly, for some time. Some form of robotics or automated system will likely transform most everything else.

The argument has been made for years, which the data supports, that as industries move toward more automation it will lead to improvements in productivity, which leads to greater growth and the development of new industries. This will offset the loss in employment and actually drive new jobs. As those industries grow, they will need more advanced automated systems for their next-generation factories. And on it goes. Of course, if we lived in an infinite world, that cycle would continue forever. But, what happens when the robots build all the robots (and they will) and there aren't jobs for people?

Think I'm crazy? When Google bought <u>DeepMind</u>, which develops "learning algorithms," as part of the agreement, Google had to set up an ethics board to ensure that once all this technology is in the hands of a company like Google, things won't get out of control. Think of this: Google already employs many of the world's experts on artificial intelligence. They have the horsepower to drive this. It's going to happen.

When you read articles written by futurists and experts in the field, you get a good sense of where this is headed. You don't have to work too hard to see that just about everything we do can be automated. Here are a few of the systems which have become commonplace in our society today, but not that long ago seemed a futuristic idea. ATMs come to mind first. They have dramatically reduced the need for tellers to cash checks, make deposits, withdraw funds, and even transfer money from one account to another. It's a great convenience for most of us. And these machines are everywhere. They're displacing hundreds of thousands of people worldwide. Now, we're beginning to see automated check-out stands at our grocery and hardware stores. Frustrating for some to use at first, they quickly have become a nice convenience, especially if you have a quick, simple purchase. Hospitals are under tremendous pressure to reduce costs and are beginning to invest in automated systems to monitor patients' vital signs, and deliver nourishment (IV) and medications, etc. Certainly patient care will improve (you would think) as a result. What about automated toll collection and parking lot payment systems?

How can a company like Foxconn successfully bring manufacturing to the U.S. and Europe? It has to automate. One highly trained U.S. employee in an automated factory will

GOOGLEBOTICS continues

take the place of dozens of Chinese factory workers. Overall costs may be about the same but will come with far fewer headaches. No need for huge dormitories or cafeterias. No 30% annual employee turnover. No suicides, no underage employee problems. No collective bargaining, no wage increases (actually, the cost of automation will continue to decrease). Their customers (Apple) get the non-governmental organizations (NGOs) off their back. In fact, Foxconn is planning to use robots in their mega-factories in China, as well. I'm sure Terry Gou has done the math. An automated factory, wherever he decides to build it, makes good financial sense and will make his life and company stakeholders' lives a lot easier. Partnering with Google to accelerate this effort was probably an easy decision for him.

The growth of robotic systems is accelerating. The capabilities will continue to increase as prices drop. The combination of more capable systems at a much lower cost per function will provide the fuel needed to drive this industry at greater and greater speeds. Google's investment into robotics isn't altruistic; it's pure capitalism. And what the dozen or so smaller robotics companies could do on their own has now been coalesced and focused into building the robots of the future. In 10 years, this could be Google's biggest business. The potential is certainly there. At least, that's the way I see it.

Check out this link to learn more: <u>A Peek</u> <u>Into Google's Plan With Robots</u>. **SMT**



Ray Rasmussen is the publisher and chief editor for I-Connect007 Publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuiTree Magazine*. To read past columns, or to

contact Rasmussen, <u>click here</u>.

Video Interview Do You Know it All? Training is Essential!

by Real Time with... IPC APEX EXPO 2014



Editor Kelly Dack and Blackfox Training Institute President Al Dill discuss Blackfox's recent expansion. The training company now boasts four IPC certification centers worldwide, and looks forward to more growth, especially in the area of defense.



SMT PROSPECTS & PERSPECTIVES

Tin Whiskers, Part 5: Impact of Testing Conditions

by Dr. Jennie S. Hwang H-TECHNOLOGIES GROUP

In this installment of the tin whisker series, we'll take a look at the impact of testing conditions, and follow-up with this statement from Part 4: "...all-encompassing tests to confirm or deny the culprits for tin whiskers are prohibitively costly and time-consuming..."

The JEDEC Solid State Technology Association (formerly known as the Joint Electron Device Engineering Council) has published several documents that address and/or are related to the testing of tin whiskers, which are good guidelines with which to start.

- JEDEC Standard No. 201: Environmental Acceptance requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes
- JEDEC Standard No. 22A12: Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes
- JEDEC Standard No. 22-A104D: Temperature Cycling

Primarily, three sets of testing conditions are included in the JEDEC documents: ambient temperature storage, elevated temperature storage and temperature cycling, with the following parameters:

Room Temperature Humidity Storage

 $30 \pm 2^{\circ}$ C and $60 \pm 3\%$ RH (1000 hrs interval inspection /3000–4000 hrs total duration)

Temperature Humidity Unbiased

 $60 \pm 5^{\circ}$ C and 87 + 3/-2% RH (1000 hrs interval inspection /3000–4000 hrs total duration)

Temperature Cycling

Lower end temperature: -55 to -40 (+0/-10)°C Higher end temperature: +85 (+10/-0)°C (500 cycles inspection /1000–1500 cycles duration/air to air/5–10 min soak/3 cycles per hour)





We think different.

Call us...we speak your PCB language instantly. At any time, in any country.



pcbs from just around the corner.



TIN WHISKERS, PART 5: IMPACT OF TESTING CONDITIONS continues

Indeed, testing such intricate phenomena of tin whisker formation and growth is not straightforward, not to mention its laborious and costly nature. Nonetheless, a well thought-out test plan including the properly selected parameters is the prerequisite in order to draw a viable conclusion, positive or negative, from the test results. As selecting testing parameters that are in sync with the intrinsic properties of the system is a critical step, it is plausible to choose the test parameters based on the anticipated underlying process and/or a postulated theory so that the tests can capture the action.

In contrast to testing the mechanical behavior of solder joints (e.g., thermal fatigue, mechanical shock) the test parameters should set to monitor the nucleation and growth pattern of tin whiskers or lack thereof. More importantly, the tests for the intended purpose are to gauge the relative susceptibility to whiskering. Testing the absence of whiskers is as meaningful as the presence of whiskers. The end-game is to secure a tin-whisker-resistant system (not necessarily tin-whisker-proof) or to discern between the tin-whisker-resistant and tin-whisker-prone systems. To this end, one has to define what is deemed to be tin-whisker-resistant in a practical sense.

Tests should monitor:

- First appearance of whisker, if feasible
- Max length of whisker at high T
- Max length of whisker at low T
- Density of whiskers
- Overall pattern and appearance

Desirably:

- Rate of formation over a temperature range
- Activation energy

Ideally:

• Accelerated test vs. real-life phenomena

Among the various sources of causes and factors as presented in the literature and in my last column, *Tin Whiskers, Part 4: Causes and Contributing Factors*, they can be refined into primary factors (e.g., tin and alloy composition, coating thickness, coating chemistry, crystal

structure, surface morphology) and aggravating factors (mechanical force, intermetallics at the interface, CTE mismatch, substrate base metal). The use of this refinement that affects the way the tests are run improves the odds in achieving the sound conclusions.

Real-life stresses either introduced at or subsequent to the tin plating or during its service life may lead a different tin whisker behavior as in accelerated tests (e.g., temperature cycling, elevated temperature storage). Alloy-making process to achieve homogeneity needs to be taken into consideration. For an "impurity" system, how the process that adds elements into tin could also affect the whisker propensity.

Tin whiskers occur for certain reasons. Thermodynamics shows that nature spontaneously directs to a state of lower energy in the absence of external energy input, and the stress/strain has a tendency to be released by making changes. The fact that tin whiskers spontaneously grow out of the surface of the coating with time should be associated with the change in energy state (stress/strain) in the coating to the direction that lowers its energy state. Additionally, in order to grow whiskers, there must be a supply of the material (tin atoms) through a passable path at a rate that is fast enough in a finite time frame. There is also fundamental distinction between the crystal growth within the lattice and the growth out of surface (protruding from the surface, like whiskers).

Relatively speaking, the energy to drive grain growth is very low and so it tends to occur at much slower rates and is easily changed by the presence of second phase particles or solute atoms in the structure. The external temperature (test temperature) drives the kinetics of defect dynamics in the tin layer by affecting stress relaxation and atomic mobility-related mechanisms. For instance, a high temperature (relative to tin's recrystallization temperature) is expected to impede the continued growth along the protruding direction, resulting in short whiskers. It is also worth noting that tin's recrystallization temperature changes with the level of its purity. In other words, when adding elements into tin, tin's behavior in relation

TIN WHISKERS, PART 5: IMPACT OF TESTING CONDITIONS continues

to the external temperature (test temperatures) will change.

However, recrystallization is only a part of the tin whisker process, and far from the whole story.

Accelerated tests (e.g., temperature cycling, elevated temperature storage, etc.) that induce and/or aggravate the internal strains offer a fertile bed for tin whisker growth. With a given tin coating, the real-life excursion right after the coating process all contributes to its energy state.

For all these reasons—both theoretical and practical, the inclusion of a reference material is in order when testing a new system. A reference material is also the simplest way to fill the gap. Based on the scientific principles as well as the decades' field service performance, a tin-lead reference material containing lead in the range of 3–37% is indispensable. And this defines tin-whisker-resistance.

Testing tin whisker propensity, due to its underlying mechanisms, is a more challenging endeavor than testing solder joint reliability. Not to over-test nor under-test is the gist of the effort.

Upcoming Appearances

Dr. Hwang will present an extensive seminar series *Preventing Manufacturing Defects and Product Failures and PoP and BTC Updates* at NEPCON Malaysia 2014, June 10–12. SMT



Dr. Hwang, a pioneer and longstanding contributor to SMT manufacturing since its inception as well as to lead-free development and implementation, has helped improve production yield and solved challenging

reliability issues. Among her many awards and honors, she is inducted to the WIT International Hall of Fame, elected to the National Academy of Engineering, and named an R&D-Stars-to-Watch. Having held senior executive positions with Lockheed Martin Corp., Sherwin Williams Co., SCM Corp, IEM Corp., she is currently CEO of H-Technologies Group, providing business, technology and manufacturing solutions. She has served on U.S. Commerce Department's Export Council, various national panels/committees, and the board of Fortune 500 NYSE companies and civic and university boards. She is the author of 400+ publications and several textbooks, and an international speaker and author on trade, business, education, and social issues. Her formal education includes four academic degrees (Ph.D., M.S., M.A., B.S.) as well as Harvard Business School Executive Program and Columbia University Corporate Governance Program. To read past columns, or to contact the author, click here. For further info, go to: www.jenniehwang.com.

a team at Stanford has developed a process to create flexible chips that can tolerate power

fluctuations in much the same way as silicon

"This is the first time anyone has designed

Flexible Carbon Nanotube Circuits Made More Reliable

Engineers would love to create flexible electronic devices, such as e-readers that could be folded to fit into a pocket. One approach involves designing circuits based on electronic

fibers known as carbon nanotubes (CNTs) instead of rigid silicon chips.

But reliability is essential. Now

uld flexible CNT circuits that have both high immunity to electrical noise and low power consumpnic tion, " said Zhenan Bao, a professor of chemical engineering at Stanford. The



circuitry.

cal engineering at Stanford. The Bao Lab reported its <u>findings</u> in the Proceedings of the National Academy of Sciences.



by Alejandro Castellanos, Dr. Zhen (Jane) Feng, David Geiger, and Murad Kurwa FLEXTRONICS INTERNATIONAL INC.

Abstract

Manufacturing technology faces challenges with new packages/processes when confronting the need for high yields. Identifying product defects associated with the manufacturing process is a critical part of electronics manufacturing. In this project, we focus on how to use AXI to identify BGA head-in-pillow (HIP), which is challenging for AXI testing. Our goal is to help us understand the capabilities of current AXI machines.

For the study, we used two boards exhibiting HIP defects with four types of AXI machines located at four Flextronics sites, or at a vendor laboratory. The AXI machines used have different X-ray technologies: laminography and tomosynthesis. We collected three sets of data with AXI 1 machine (laminography), and AXI 4 machines (tomosynthesis); one set of data with AXI2 (tomosynthesis); and four sets data for AXI3 (tomosynthesis). We studied AXI measurement data with the different AXI algorithm threshold settings. The data indicated clearly that the Algorithm Threshold settings are very critical for detecting HIP, including open. The defective HIP pins are validated by using 2DX and CT scan.

The test data consist of defects escaped %, false call ppm and also gage R&R. The AXI images for HIP pins, false call pins and defects escaped pins are presented in the paper. The 2DX and CT images are provided for identifying HIP type (shape and size).

Introduction

More BGA and area array devices are appearing on PCBAs as product and functional complexity increases. Furthermore, to achieve good signal integrity, more I/Os are packed in smaller areas within the available real estate. It is very important to use AXI and other Non-



destructive techniques to identify BGA joint qualities and prevent escape. We did a study for BGA crack several years ago with AXI, time domain reflectometry (TDR), 2DX, and crosssection/SEM comparison; however, we didn't

have good detected results from AXI ^[1]. During the study, we realized that 2D X-ray with tilting angle detector has the capabilities to identify BGA crack at 5 microns or higher. Recently more AXI machines using both laminography and tomosynthesis technologies have better capabilities to detect BGA defects; therefore we would like to develop the optimization algorithm and threshold settings to identify HIP on BGA for high volume products.

Based on 2DX images, we have identified two boards containing HIP: #495 with 45 HIPs, and #266 with 2 HIPs. With the HIP

defective boards, we have tested them at four sites, with four different AXI machines. AXI1 is a laminography machine; AXI2, AXI3, and AXI4 are tomosynthesis machines from different vendors. We worked together with site engineers and vendors' support engineers for this project. We focused on HIP defects escaped %, false call PPM and gage repeatability & reproducibility (gage R&R) with that BGA.

The old axiom "A picture is worth a thousand words" proves accurate. Indeed, a highquality microstructure of a solder joint provides "sights' and "insights" into the state of solder joint integrity and its anticipated behavior. Similar benefits can be achieved using highquality 2D and 3D offline X-ray inspection images and data. Through this study, we try to understand more about AXI machines capabilities, especially for improving AXI programming optimization used for our best practices. Although machine's testing conditions were not exactly the same, but close, the philosophy for achieving optimization is similar. Look at the measurement data first, finding the difference between good solder joint and defective solder joint; and then balance the defects escaped %

and false call numbers to find the right threshold settings. For the high volume products, monitoring AXI programs is an ongoing process based on further fine-tuning with feedback from ICT, functional test and 2D/3D offline X-ray inspection.

Experiments and Analysis

Two boards with HIP defects were from production SMT line of a different site. The BGA has 1,017 balls with ball diameter of 21 mils for outer balls and 19 mils for inner balls of the pad. The HIP defective pin (ball) is identified at 2DX machine with tilting angle detector. Tilting (oblique) angle is 55–68 degrees; and rotation of the X-ray detector 0–360 degrees around the examined joint. This is not trivial, but it is very

easily accomplished using the 2DX equipment. The oblique and rotation angles of the X-ray detector are key factors for identifying BGA defects, such as HIP, open, and small crack₁. There are a total of 47 HIP pins on the two boards based on 2DX images (resolution 0.1μ m). Some 2DX HIP images are shown in Figures 1, where pins with arrow are HIP, except for pin number G32 which is crack (9µm).

For this project, the "defects escaped %" and "false call PPM" are calculated with these equations:

Defects escaped % = # of HIP escaped / total # of HIPs, where total # of HIPs is 47 (Equation 1)

False call PPM = (total # of false call / total pins # tested) X10, where total tested pins number is 2034 for two boards (Equation 2)

The gage R&R results are calculated with SPC tool Minitab with nine sets of variable data by three operators from each machine. Data of BGA diameter for pad and middle slice, and some main AXI algorithm (open outlier, neigh-

The old axiom "A picture is worth a thousand words" proves accurate. Indeed, a highquality microstructure of a solder joint provides "sights" and "insights" into the state of solder joint integrity and its anticipated behavior.





HIP: Z24, AA24



HIP: L13, N11



HIP: V17, W17, Z16, Z18, Z19

Crack: G32

HIP: N30

Figure 1: Samples of 2DX images of defective pins (board #495).

bor outlier, and solder area pad) are collected during the studies.

A. AXI 1 (Laminography)

AXI 1 type is the largest number of AXI machines in our worldwide manufacturing sites. From our experience, AXI 1 plays a good role of detecting various solder joint defective types (solder bridge, insufficient, excess ...) based on experience during the last 15 years; it does not detect 100% of BGA HIP defects effectively. Engineers from different sites share their knowledge, such as an experience with latest software, and new algorithm's features in order to achieve the best performance by maximizing the machine's capabilities.

First, we tested two boards with AXI 1 type at site 1, and then used the same program to test the same boards at sites 2 and 3 with a little bit of fine-tuning (editing of threshold settings). The main thresholds which we focused on are: open outlier for pad slice and open outlier for middle ball slice. As we know, each AXI machine flags a pin as a defect if the measurement falls outside of the algorithm threshold limit. So it is important to know the difference between a good and bad solder joint with various measurements data for each algorithm. It is easy to have optimization threshold setting if the measurement difference has a big gap; otherwise it is challenging to make AXI program detecting defects with low false call rate.

The main thresholds of adjustment are: open outlier for pad slice and open outlier for middle ball slice. The threshold setting is < -3 for "open outlier lower sensitivity for pad slice", and > 3 for "open outlier sensitivity for middle ball slice." These should be good threshold numbers for many products (BGA packages). Table 1 lists the pins, which are called defect from site 2 based on their threshold settings: open outlier sensitivity for slice 1 (midball) is 3; open outlier lower sensitivity for slice 2 (pad) is -3. The program detected 17 HIP pins from 45 defects (board # 495); and it had seven pins

BGA U4D1 Pin #	Pin Type	OpenOutlier (MidBall)
T24	HIP	3.11
Z18	HIP	3.17
N30	HIP	3.27
N11	HIP	3.3
P13	HIP	3.3
AH13	HIP	3.31
W14	HIP	3.36
U8	HIP	3.39
T12	HIP	3.48
AK18	HIP	3.73
AG16	HIP	3.93
AH19	HIP	4.34
AL11	HIP	4.62
AA27	HIP	4.71
AJ10	HIP	4.73

BGA U4D1 Pin #	Pin Type	OpenOutlier (Pad)
AD28	False call	-4.06
Z12	False call	-3.77
Z23	False call	-3.37
AB15	HIP	-3.29
AD15	HIP	-3.24
A23	False call	-3.14
L13	HIP	-3.13
AC15	False call	-3.09
G28	False call	-3.05
M15	False call	-3.05

Table 1: AXI 1 open outlier measurement data for pad and middle ball slices (board #495).



AB15 (escaped)



L13 (detected)



AD28 (false call)



M15(false call)

Figure 2: AXI 1 images of detected HIP; escaped HIP, and false call pins.

as false calls, and escaped 28 HIP defects. The detected HIP pins (in green), escaped HIP (in red color), and false call pins (orange color) are listed in Figure 2. There are no significant differences between the good and HIP pins based on the AXI 1 images. This may be the effect of AXI1 HIP detection capabilities.

Figure 3 shows "open outlier" measurement data for middle ball and pad slices of board #495. The measurement data tells us that AXI1 has the capabilities to detect some HIP pins. However, there is no clear measurement data gap between the good and HIP pins with the current version AXI software as it is reflected on AXI 1 images. Therefore, we understand why some HIP pins escaped, and also has difficulty to have zero false call. Table 2 lists the number of detected HIP, false call, and HIP escaped with different threshold settings at site 2. With the default threshold settings from AXI 1, the program didn't detect any HIP with zero false call. If we tighten the threshold from < -3 to < -2.5 for pad slice, and from >3 to >2 for middle ball, the detected HIP increased from 18 to 29, however the false call increased from 7 to 17 with the same program. As a recommendation, we suggest the settings



Figure 3: AXI 1 "open outlier" measurement data for middle ball and pad slices (board #495).

Board #	Open Outlier Threshold Settings	Detected	False Call	Escaped
266	Pad < -3 as defect; Mid Ball > 3 as defect	1	5	1
495	Pad < -3 as defect; Mid Ball > 3 as defect	18	7	27
495	Pad < -2.5 as defect; Mid Ball > 2 as defect	29	17	16
266	Pad < -6 as defect; Mid Ball > 6 as defect	0	0	2
495	Pad < -6 as defect; Mid Ball > 6 as defect	0	0	45

Table 2: AXI 1 detected HIP and false call vary with threshold settings (board #495).

Site	# of Total Escaped Defects Defects Escaped %		# of Total False Call	False Call PPM	
1	46	97.87%	0	0	
2	28	59.57%	12	5900	
3	24	51.06%	13	6391	

Table 3: Testing summary with of AXI 1.

for open outlier < -3 for pad slice, and > 3 for middle ball slice which are the main algorithms that can detect HIP. The rest of the parameters for open outlier can be used with default numbers if the test results are fine.

Table 3 listed AXI 1 testing results summary by using equations 1 and 2 from site 1; site 2; and site 3. The site 1 used default threshold setting; site 2 and site 3 use the same threshold settings which are listed in the first two lows of Table 2 for testing two boards. The data tells us that AXI 1 has the capabilities to detect HIP with the right algorithm thresholds settings.

B. AXI 2 (Tomosynthesis)

There are a few AXI 2 machines at Flextronics. For the AXI 2 machine, the threshold settings for neighbor outlier is < -3.5 for pad, and > 4.5 for middle ball. Table 4 listed AXI 2 test results summary from site 1. Two detected HIP pins (in green), and two escaped HIP (in red), are listed in Figure 4. Similarly, there is not a huge difference on pin images between good and HIP pins. In comparisons to AXI1 versus AXI2, the AXI 2 (tomosynthesis) seems to have better HIP detection than AXI 1 (laminography).

Site	# of Total Escaped Defects	Defects Escaped %	# of Total False Call	False Call PPM
1	16	34.04%	3	1475

Table 4. Testing summary with AXI 2.











AB15(escaped)

Figure 4: AXI 2	images of	detected HIP;	escaped I	HIP pins	(board	#495).
-----------------	-----------	---------------	-----------	----------	--------	--------

Site	Algorithm (Neighbor Outlier)	Threshold
1	Minimum and Maximum for Pad	< - 3.2 ; > 4.5
2	Neighbor Outlier - Pad (multi-pass)	> 2.2
3	Neighbor Outlier - Pad	> 2.2 (#495); >3.3(#266)
4	Neighbor Outlier - Pad	> 2.2 (#495); >3.3(#266)

Table 5: Algorithm thresholds with AXI 3.

C. AXI 3 (Tomosynthesis)

AXI 3 machine uses Tomosynthesis technology which is similar to AXI 2 machine. The AXI 3 has faster testing speed than AXI 1, and AXI 2. We used the same HIP boards tested at four sites, and worked with the vendor to have algorithm and threshold settings studies. The algorithm threshold settings are different when we tested the boards at different site with the latest software at that time. The main algorithm thresholds for detecting HIP with AXI 3 are listed in Table 5. Because board #495 and #266 were built at different manufacturing facilities with little difference in solder shape and volume, different algorithm thresholds were set to detect HIP effectively at site 3 and site 4. Figure 5 shows detecting HIP pins, escaped pins, and false call pins for board #495, and all pins for board #266 which is from site 2. The AXI 3 flagged pin as HIP when its pad "neighbor outlier" > 2.2 with multi-pass algorithm. AXI3 detected 38 HIPs (escaped 7) with six false calls for board #495, and detected two HIP (no escapes) with six false calls for board #266. Table 6 listed the test summary from each site with AXI 3 which has better performance than AXI 1 for both HIP detection percentage and false call PPM.

The AXI 3 images for detected HIP, escaped HIP and false calls are shown in Figure 6. There is no very clear difference between good and HIP pins similar to AXI 1, and AXI 2. It is not

We deliver Advanced PCB Solutions!



Landless Via Technology

We're the only manufacturer in the world to have perfected a liquid photo-imageable resist (PiP) in electrolytic form, used for all our production.

CLICK TO LEARN MORE

Our unique processes enable us to create and deliver Advanced PCB Solutions that meet the needs of the demanding market at competitive prices!



Fine line PCB, 2 mil line /space

We have developed a unique set of processes based on electro-depositable liquid photoresist.

CLICK TO LEARN MORE



Impedance Tolerance <5%!

With our panel plating process combined with continuous foil lamination, our impedance tolerances are second to none!

CLICK TO LEARN MORE



CANDOR INDUSTRIES, INC. ADVANCED PCB SOLUTIONS

www.candorind.com | sales@candorind.com | (416) 736-6306



Figure 5: AXI 3 "open outlier" measurement data for pad slices from site 2 (Board #495 & #266).

Site	# of Total Escaped Defects	Defects Escaped %	# of Total False Call	False Call PPM
1	13	27.66%	9	4425
2	7	14.89%	12	5900
3	5	10.64%	7	3441
4	8	17.02%	12	5900

Table 6: Test summary with AXI 3.



L13 (detected)



R15 (detected)



G32 (escaped)



T20 (false call)

Figure 6: AXI 3 images of detected HIP; escaped HIP, and false call pin (board #495).

easy for operators to indentify real defective HIP defects based on these images from the repair station. Therefore we should be very carefully to set threshold correctly to detect HIP. We prefer to detect some HIP without the high rate of false calls on one BGA especially for large-volume production based on current AXI capabilities.

D. AXI 4 (Tomosynthesis)

AXI 4 uses tomosynthesis technology also. Its resolution can be adjusted per different package or solder joints. We had test data from three sites with little fine-tuning for the program. The AXI 4 main algorithm thresholds for detecting HIP are listed in Table 7. Similarly, different algorithm thresholds for two boards are adjusted

Site	Algorithm	Threshold	Note
2	Solder Area Pad	< 83% ; >130%	< 0.129 or < 0.144 mm ²
3	Solder Area Pad	< 70% ; >130%	< 0.125mm ²
4	Solder Area Pad	< 70% ; >130%	< 0.130mm ² ; < 0.142 mm ²

Table 7: Algorithm thresholds with AXI 4.



Board #495 with partial pins

Board #266 with all pins

Figure 7: AXI 4 "solder area" measurement data for pad slice from site 3 (boards #495 & #266).

to detect HIP effectively.

Figure 7 shows AXI 4 measurement solder area at pad level for detected pins, escaped HIP pins, and false call pins for board #495; and all pins for #266. At site 3, with the settings listed in Table 7, AXI 4 detected two HIP pins (no escaped) for board #266 without any false call; and detected 43 HIPs (escaped 2 HIP) with one false call for board #495. The two escaped and one false call images are listed on Figure 8. As other AXI machine, there is still no very clear difference between good and detective HIP pins as shown in Figure 8.

Table 8 listed the test summary from each site with AXI 4 which has better performance than AXI 1 for both detection percentage and false call.

Comparison and Improvement

All four AXI machines have capability to detect BGA HIP defect with different success levels. The AXI performance is based on program algorithms, its thresholds' setting, and machine testing conditions. We also collected data for gage R&R from these AXI machines from the different sites. The gage R&R for BGA ball diameters are less than 30% for all AXI machines. The gage R&R for middle ball diameters are less than 10% for some AXI machines. However the gage R&R for open outlier, solder area, neighbor outlier are not what we expected because most of them are at the boundary level: around 30%. This is why AXI testing results are not repeatable. For example, please refer to the AXI 1 test summary shown in Table 9. There are nine test cycle results with board #266 and #499 at AXI 1 machine in our manufacturing (Table 9). It is easy to see the difference of AXI 1 test results with the same algorithm thresholds settings (pad < -3 as defect; mid ball > 2 as defect).

Current AXI technology still has plenty of room for improvement in detecting HIP due to its hardware and software limitations. So, what can we do in order to optimize the AXI HIP detection capabilities? At Flextronics, we share our best practices from site to site; as with this project, we suggest setting these algorithm thresholds settings (pad < -3 as defect; middle



R15 (detected)

G32 (escaped)

L13 (escaped)

AD31 (false call)

Figure 8: AXI 4 Images of detected HIP; escaped HIP, and false call pin (board #495).

Site	# of Total Escaped Defects	Defects Escaped %	# of Total False Call	False Call PPM
2	2	4.26%	4	1967
3	2	4.26%	1	492
4	1	2.13%	4	1967

Table 8: Test summary with AXI 4.

# of		Board #266 h	d #266 has 2 HIP pins			Board #495 has		
Testing	AXI 1 Results	Detected HIP	Escaped HIP	False calls	AXI 1 Results	Detected HIP	Escaped HIP	False calls
1	7	1	1	6	28	18	27	10
2	7	1	1	6	32	18	27	14
3	10	1	1	9	29	17	28	12
4	9	2	0	7	29	18	27	11
5	8	1	1	7	31	17	28	14
6	12	1	1	11	30	18	27	12
7	11	2	0	9	31	18	27	13
8	8	1	1	7	30	18	27	12
9	8	1	1	7	28	18	27	10

Table 9: Testing summary with AXI 1.

ball > 3 as defect) as a start, then look at the measurement data to adjust according to the process. We also share our experience with AXI vendors, and provide feedback to them as well as working together with them for better and improved AXI performance.

Table 10 uses two subtypes for this BGA due to two different types of pad on the board: pad diameter is 19 mils for inner balls, and 21 mils for outer balls on BGA. For AXI 1, we have reduced HIP escaped number from 27 to 15 with the same false calls; for AXI 4, we have reduced false call number from four to

one with the same defects escaped. This best practice shows good results with the two different AXI machines.

In order to verify our AXI / 2DX results, we performed 3D CT board-level x-ray inspection (limited angle computer tomography). This is a novel technique permitting areas of a very large board to be examined using 3D CT without cutting the board. Figures 9–12 show the CT images and results. Figure 9 demonstrates clearly that pin G32 has a 9-micron crack. This potentially critical defect was identified with offline 2D X-Ray (2DX image, Figure 1) and confirmed



IPC Training and Certification Courses

EARN CREDENTIALS ON FIVE KEY IPC STANDARDS

Programs focused on understanding and applying criteria, reinforcing discrimination skills and supporting visual acceptance criteria in key IPC standards include:

- IPC-A-610, Acceptability of Electronic Assemblies
- IPC-A-600, Acceptability of Printed Boards
- IPC/WHMA-A-620, Requirements and Acceptance for Cable and Wire Harness Assemblies

IPC Programs covering IPC standards knowledge plus development of hands-on skills include:

- J-STD-001, Requirements for Soldered Electrical and Electronic Assemblies
- IPC-7711/IPC-7721, Rework of Electronic Assemblies/Repair and Modification of Printed Boards and Electronic Assemblies

Click for Course Schedule

For more information contact us at 888.837.9959 or sharonm@blackfox.com

www.blackfox.com

Site	AXI	Type of Algorithm Threshold	# of Total Escaped Defects	Defect escaped %	# of Total False Call	False Call PPM
2	AXI 1	1	27	60.0%	7	6883
2	AXI 1	2	15	33.3%	7	6883
4	AXI 4	1	1	2.2%	4	3933
4	AXI 4	2	1	2.2%	1	983

Table 10: AXI 1 and AXI 4 test summary with 1 and 2 types of algorithm threshold settings.



Figure 9: CT image for BGA crack with 9 µm.



Figure 10: CT images for HIP N30.

using large board CT. However none of the AXI machines detect it as defect.

There are varying types of HIP defects with different size and shape as shown in Figures 10 and 11. All current AXI machines have capabilities to detect HIP N30 shown on Figure 10, however not all machines detected HIP pins Z15, AA 15, and AB15 (Figure 11). The laminography AXI 1 machine detects HIP type defects as pin AB15; however, it is challenging for AXI 1 to detect HIP type as Z15. Tomosynthesis AXI machines do not easily detect HIP type as AB15.



Figure 11: CT images for HIP (AB15, Z15 and AA15), AC15 is good.

Summary

• Current AXI has capabilities to detect some HIP with right Algorithm threshold settings. The tomosynthesis technology looks better than laminography technology for detecting HIP as the tomosynthesis technology are utilizing digital technology as compared to the analog laminography technology.

• The algorithm threshold settings are very critical for detecting HIP. The false call number has to be reasonable for the production line. The AXI program optimization is based on its measurement data analysis.

• There are no clear image differences between good solder joint and HIP with current AXI machine, especially for HIP type defect AA15 shown as in Figure 11. Therefore we have to have good balance between HIP defect escaped and false call.

• We are looking forward to see AXI machine with more accurate and repeatable measurement data, and better image separation between good solder joint and HIP pins.

• 2DX and large board CT are very important techniques used to verify the AXI results and fine-tune the algorithms.

References

1. Zhen (Jane) Feng, Juan Carlos Gonzalez, Evstatin Krastev, Sea Tang, and Murad Kurwa, "Non-Destructive Techniques for Identifying Crack Defect in BGA Joints: TDR, 2DX, and Cross-section/SEM Comparison", SMTA Proceedings, August 2008.

2. Jennie S. Hwang, "Can Microstructure Indicate a Good Solder Joint? Part III," SMT Magazine, October 2012.

3. Flextronics ATG, "CT versus AXI with HIP," project is ongoing, October 2012.

Acknowledgements

The sites of Guadalajara, Mexico; Austin & Milpitas, U.S.; Malu & Zhuhai, China; Timisoara, Romania Engineering and production teams of Flextronics Inc.; AXI 3, AXI 4 and 2DX vendors support teams; and Peter Chipman, and Dr. Evstatin Krastev for their timely support. SMT

Alejandro Castellanos works in test area management at Flextronics Guadalajara. He has been working with the Advanced Engineering Group in order to improve AXI detection and share best practices.

Dr. Zhen (Jane) Feng is a process engineering manager of the Flextronics Advanced Engineering Group. She works in Worldwide Assembly and Test Technology Division.

David Geiger is director of the Advanced Engineering Group at Flextronics.

Murad Kurwa is vice president of the Advanced Engineering Group at Flextronics.

Mechanical Reliability

A New Method to Forecast Drop Shock Performance

by Ronald Frosch, Guenther Mayr, and Manfred Riedler AT&S SHANGHAI, CHINA

Abstract

In light of the recent technological trends within PCB manufacturing industry, there is an increasing degree of interest in understanding the influence factors of mechanical stress on the durability of mobile devices.

In the past, many papers focused on PCB reliability and the influence factors during drop shock test. In most cases, the potential influence factors in regards to underfill have not been fully investigated. Additionally, there is no clear direction on the influence of the interaction between solder mask inks and underfill systems.

The intent of this article is to identify an accurate method to predict drop test behavior by understanding the surface tension of both

the solder mask ink and the underfill material. This could become a significant advantage for improving the reliability of the entire electronic construct. In this paper a method has been examined that can be used to subsequently analyze the reliability of the latest mobile device related materials and design.

The prescribed test has been constructed using a cross comparison of pad design, surface finish, solder mask and underfill, measured by drop testing. Based on the resulting data, a method was evaluated to predict and optimize drop test reliability by understanding the surface tension of solder mask and underfill (adhesion).

We are now able to identify specific advantages and limitations for different material combinations, without the need of expensive and time intensive drop tests.

In an effort to achieve a broader understanding of the entire process and product scope, the

SACM[™] Solder Paste

Low cost

High reliability

- Superior drop testing
- Excellent thermal cycling

Drop-in replacement for SAC305

- Same reflow profiling
- Visually identical
- Excellent print performance

For detailed technical and reliability information, visit www.indium.com/SACM

PROBLEM



FAILED SOLDER JOINT





http://indium.us/D1139

From One Engineer **To Another**[®]

www.indium.com/SACM askus@indium.com

ASIA • CHINA • EUROPE • USA



participants in these trials were an HDI PCB manufacturer (AT&S) and its material suppliers.

Introduction

Continual miniaturization and RoHS requirements have significantly aggravated the

endeavor to achieve customer expectations in terms of reliable electronic devices. Drop shock performance has especially become an important factor in the past several years, due to the increasing number of portable electronics, such as mobile devices, MP3 players and tablet computers.

Many investigations have shown that the interaction of solder paste and surface finish, material selection and the rigidity of the whole electronic construct all have an impact on the final drop shock performance. Even an optimum combination of the before mentioned factors might not be enough to ensure a satisfying quality of drop shock resistance. without factoring in critical design features component selection. and It is common to lower such risks with an under filling step between surface mount components and the printed circuit

board. The efficiency of such an additional step strongly depends on the adhesion between solder mask and underfill material.

The investigations for this article include a full factorial drop test DOE (design of experiments) and a new method to predict drop shock performance based on the knowledge of the surface energy of solder mask and underfill material.

Test Equipment & Method

The drop test was performed based on an AT&S internal standard (mobile devices), which was evaluated and developed in conjunction with mobile device customers to meet their spe-

Many investigations have was calibrated daily before shown that the interaction of solder paste and surface finish, material selection and the rigidity of the whole electronic construct all have an impact on the final drop shock performance. Even an optimum combination of the before mentioned factors might not be enough to ensure a satisfying quality of drop shock resistance, without factoring in critical design features and component selection.

cific requirements. A correlation between JEDEC JESD22-B111i and our mobile device standard might be difficult in terms of absolute number of drops, but it can be compared to determine basic trends (failure mode and time to failure results are similar). For the intent of this article, the material was the major focus,

not the overall design.

The PWB level drop tester starting any actual DOE measurements. The test vehicles were assembled with 12 dummy components and flat ribbon cables ^[1] soldered to the PTH terminals. To minimize the risk of solder joint failure of the signal cables during drop shock stress, the joints have been additionally fixed with a common available 3M tape. Furthermore the cables were fixed to the test equipment in such a way that the stress during test was reduced to a minimum (Table 1).

Test Vehicles

The PCB build-up for the 30.7 mil thick DOE samples was an 8-layer multilayer with a common available halogen-free 150TG FR-4 material. The soldering was performed with a 4 mil thick electro-polished stainless steel stencil,

glued into polyester mesh and tensioned in an aluminum frame. The outer stencil dimensions were 736 x 736 x 40 mm. A commonly available SAC type 3 solder was used for assembly. The underfilling material was based on a singlecomponent epoxy system with fast curing, low CTE and Pb-free compatible behavior. In the table below, the three steps of sample production (multilayer, assembled multilayer & assembled multilayer after underfilling) is shown.

The DOE layout was full factorial with four factors, each with two sub groups (see Table 3). Besides the main focus on solder mask type and underfill, the influence of pad design and sur-



Table 1: Basic test setting of mobile devices standard & JEDEC JESD22-B111.

face finish (phosphorus content of nickel phosphorous layer: MP = 6-9wt% P; HP = 9-12wt% P) was observed. For each DOE group nine cards were dropped and the response was statistically analyzed by Weibull method. The failure mode was optically determined by cross sectioning and optical microscopy.

The drop events were continually monitored (online) until an event detector recorded electrical failures of any of the four middle components or until 5000 drops were exceeded. The four middle components were chosen because electrical defects happen first at the center positions of the board due to the highest tension/ compression in this area (Figures 1 and 2).

Test results

The influence of drop shock performance caused by the phosphorus content in the nickel layer was in both cases, with and without un-

Basic Design						
Structure		1-1-1-2-1-1-1				
Nominal board th	ickness		30.7mil +/-3mil			
Cu thicknes	S		1/3 oz			
Glass fiber	s		1080 & 106			
Dielectrical ma	terial	F	FR4, halogen free 150TG			
Glass Transition Temp	erature (Tg)		150°C			
Surface fini	sh	ENIG	ENIG (Ni – $3\mu m \& Au - 0.05\mu m$)			
Pad size			Ø 20mil (via in pad)			
Solder past	e		SAC type 3			
Flux syster	n		low sputter application			
Reflow prof	ile		lead free			
max. reflow temp	erature		247°C +/- 1°C			
(from left to right: s	* CU * CU	3 8 2 2 3 8 3 1 2 3 8 3 1 2 3 8 4 1 2 3 8 5 1 2 3 8 5 1 2 3 8 5 1 2 3 8 6 1 2 3 8 7 2 3 8 3 8 8 3 8 3 8 3 8 1 2 3 8 3 8	012 0106 012 1080 022044 1080 012 1080 012 012 012 0106 012 012	ss number)		
Image: Description of the second se						

Table 2: Test vehicle build-up.

derfill, slightly better for HP in compare to MP samples. But as it can be seen in the interval chart of Figure 3, the statistical significance was not convincing. Summarized can be concluded that HP-ENIG surfaces have at least no negative impact to the drop shock resistance.

Well known from previous studies is the positive effect of Cu defined (CuD) pads in

comparison to solder mask defined (SMD) pads. Due the fact that the influence of solder mask/underfill interaction surpasses the influence of the pad design (Figure 5), the difference between CuD and SMD pads is statistically not so obvious in the case of underfill, but is the major impact for samples without underfill (Figure 4).

Design	Surface Finish	Pad Design	Solder Mask	Underfill	No. of cards
01	ENIG - MP	SM defined	Type A	without	9
02	ENIG - MP	SM defined	Type A	with	9
03	ENIG - MP	SM defined	Туре В	without	9
04	ENIG - MP	SM defined	Type B	with	9
05	ENIG - MP	Cu defined	Type A	without	9
06	ENIG - MP	Cu defined	Type A	with	9
07	ENIG - MP	Cu defined	Type B	without	9
08	ENIG - MP	Cu defined	Type B	with	9
09	ENIG - HP	SM defined	Type A	without	9
10	ENIG - HP	SM defined	Type A	with	9
11	ENIG - HP	SM defined	Type B	without	9
12	ENIG - HP	SM defined	Type B	with	9
13	ENIG - HP	Cu defined	Type A	without	9
14	ENIG - HP	Cu defined	Type A	with	9
15	ENIG - HP	Cu defined	Type B	without	9
16	ENIG - HP	Cu defined	Type B	with	9

Table 3: Full factorial drop test DOE.



Figure 1: Red = area of tension; green = strain less area; blue = area of compression.

As mentioned earlier, the major impact for this DOE was the use of underfill and the interaction with solder mask. Two types of solder mask inks have been compared; both are commonly available and released for mass production. As seen in Figure 5, the difference between the inks for samples without underfill is negligible. However, in drop testing performed on underfilled parts, there was a notable difference in the drop test results between the solder mask inks.

Considering that the performance of solder mask type A & B without underfill was similar,



Figure 2: Schematical view of drop test boards—the four critical components are marked in red.



Figure 3: DOE output for ENIG surface finish. High phosphorous (9% - 12%) vs middle phosphorous (6% - 9%).

we concluded that the interaction of underfill and solder mask is the main impact to the overall drop performance.

As shown in this analysis, the main influence factor for this DOE was the underfill (with or without), which caused performance changes up to 100 times. Surprising was the prevalent failure mode which was independent of underfill, solder mask or surface finish. Differences in the pad design seemed to create the only impact, resulting in either "solder crack close to PCB" in the case of solder mask defined pads, or "via/prepreg crack" in the case of copper defined pads (Figure 6).

The different DOE parameters have been compared by two-parameter Weibull analysis. For below comparison of the different DOE factors, an improvement factor was calculated by

DOE factor	Factor (based on weibull analysis)
Underfill (w/ vs. w/o)	106
Solder Mask (type B vs. type A, both w/ underfill)	14
Pad Design (CuD vs. SMD)	7
Surface Finish (HP vs. MP)	1,5

Table 4: Impact of DOE factors.

using the same slope parameter (β) for all Weibull curves (Table 4). It should be mentioned that due to the complexity of the interaction of all parameters, these test results are only valid for


Figure 4: DOE output for copper defined (CuD) and solder mask defined (SMD) pads.

this specific DOE, but the order of magnitude of the impact of the given parameter should allow for reasonable estimates to be made.

Summarized can be said that the interactions of solder mask and underfill, or their adhesion properties, have a major impact to the final drop shock reliability performance.

Contact Angle, Surface Energy & Adhesion

A common method to predict the interaction between two materials are contact angle measurements which enable the determination of surface energy. Knowing the surface energy of two materials allows the calculation of WoA (work of adhesion) and IFT (interfacial tension), which are indicators for adhesion quality. It must be mentioned that WoA and IFT are important indicators for strong and lasting adhesion. In simplified terms, WoA represents the initial adhesion strength, while IFT represents the force which works against it (long term). Therefore, the higher the work of adhesion and the lower the interfacial tension, the better the adhesion. Depending on the application, it has to be decided which of both behaviors have to be rated higher.

The measurements were carried out with a fully automatic Kruss DSA100 drop shape measurement analysis system following ASTM D7334^[8] and ASTM D7490^[9] (Table 5). The calculation of surface energy followed Fowkes Theory^[10] (Figure 8).

Several types of solder mask (A–K) and two types of underfill systems (UF A & UF B) have been compared (Figure 9). The solder mask types are commonly available and there was



Figure 5: DOE output for solder mask type A & B.



Figure 6: Drop test failure mode.



Figure 7: Schematic overview of adhesion determination.



Figure 8: Fowkes theory.

no special focus on color, supplier or process. Solder mask A and B, as well as underfill B, are the same used in the drop test DOE; all other solder mask inks have not been cross compared by drop shock test.

Figure 9 shows that the total surface energy (equal to the sum of the polar [blue] and the dispersive part [red]), displays notable differences between the solder mask inks, and likewise for the underfill. It can be assumed that two ma-

Contact Angle Parameter			
Standard	ASTM D7334 & ASTM 7490		
Equipment Type	Kruess, DSA100		
Droplet Volume	1,5µ1 +/- 0,1µ1		
Measurement Time	< 5sec after drop applying		
Liquids	Water & Diiodmethane		
Sample Condition	1 x lead free reflow		
Solder Mask	11 solder mask types 2 types of underfill		

Table 5: Parameter setting.

terials with similar polarity will also have lower interfacial-tension. The reverse should be true for the total surface energy: The higher the total surface energy, the higher the work of adhesion.

Figure 10 was created using the Kruss adhesion tool, which enables the calculation of WoA as well as IFT based on the knowledge of the polar and dispersive part of two materials. The interaction between underfill A and the different types of solder mask inks is shown in blue, likewise the interaction of underfill B in red. The bar reflects WoA (left axis) and the point the interfacial tension (right axis).

Comparing the interaction of solder mask A & B with underfill B (red) it can be assumed that the adhesion of solder mask B will be significant better due to higher WoA and lower IFT, which coincides with drop test results. Comparing the same solder mask inks and their interaction



Figure 9: Surface energy comparison of different solder mask and underfill inks.

TRANSITION AUTOMATION

Technology for Improving SMT Print Quality and Production Yeild





WWW.TRANSITIONAUTOMATION.COM



Figure 10: Work-of-adhesion and interfacial tension of solder mask and underfill.

with underfill A (blue), a clear statement of a preferable solder mask would get difficult due to reverse behavior of WoA and IFT. Furthermore, it can be assumed that solder mask C and the interaction with underfill B causes remarkable adhesion, supported by excellent drop shock re-

Conclusion

liability.

The first part of this paper was a drop test DOE focusing on four factors and their influence to the drop shock reliability of assembled PCBs. The second part has focused on the main influence factor, the interaction between solder mask and underfilling system, including a method to predict the efficiency of such additional production step without the need of time and cost intensive drop tests. It was proven that the drop shock performance of two different solder mask inks without an underfilling step are quite comparable, independent of pad type or surface finishing. The use of underfill provided a reliability improvement for both solder mask types, but the efficiency strongly depended on the specific solder mask. Consequently, underfill/solder mask interaction (adhesion) has a major impact to the final drop shock reliability.

The different ink and underfill types were measured by contact angle. Based on these results, surface energy, work of adhesion and the interfacial tension of each sample was calculated. The calculated adhesion fits quite well with the drop test results—the better the adhesion, the better the shock resistance.

Finally, it should be mentioned that contact angle measurements strongly depend on factors like contamination, pre-treatment or environment, therefore, comparison tests should only

WHY CHOOSE US?

All OEM customers want quality, delivery and cost that meets their expectations and helps them to reach their strategic goals. And many have specific needs that can only be met in a partner with domestic and international manufacturing locations. EE Technologies offers this advantage with headquarters and a manufacturing plant in Reno, Nevada and a manufacturing plant in Empalme, Sonora, Mexico. Prototype, quick turn, and small quantity jobs can be run domestically. While production and large quantity jobs can be run internationally to take advantage of reduced labor costs. The option to transition products through each stage of development with the same EMS provider is a major benefit to OEM customers. Costs are lower and manufacturing engineering lessons learned stay with the project throughout. Serving with global locations is a competitive advantage for EE Technologies.

Here are just a few of our competitive advantages:

- Capacity
- Rapid prototyping
- Metrics-based decision making
- Culture of continuous improvement

Locations-domestic and international

- Certifications
- Technical services
- Competitive pricing
- Flexible and responsive

Learn more...visit us online at: eetechinc.com or call: 775-284-1177

EE Technologies, Inc. 9455 Double R Blvd. Reno, NV 89521

Empalme, Sonora Mexico



echnologies,"*





Click here to request more information.

ISO/TS 16949:2009



Electronic Evolution Technolgies Registered to ISO/TS 16949:2009 Certificate Registration Numbers: US: 10000767 Mexico: 10003616

be carried out by knowing exact experimental setup. **SMT**

References

- 1. Signal cables for event detection.
- 2. Maximum de-acceleration.
- 3. Peak at 10% of maximum acceleration.

4. Shape of acceleration curve.

5. Mechanical part which caches sledge to prevent double bounces.

6. Surface on which the sledge drops.

7. Board-Level Drop Test Method of Components for Handheld Electronic Products, JEDEC Standard 2003.

8. Standard Practice for Surface Wettability of Coatings, Substrates and Pigments by Advancing Contact Angle Measurements, ASTM International.

9. Standard Test Method for Measurement of the Surface Tension of Solid Coatings, Sub-

strates and Pigments using Contact Angle Measurements, ASTM International.

10. For more information on the Fowkes method, visit the <u>Kruss website</u>.

Ronald Frosch is a quality management specialist with AT&S (China) Co.,Ltd. He is project manager for next-generation technologies.

Guenther Mayr is a technology and quality manager at AT&S. He has specialized in HDI PCBs for the last 10 years.

Manfred Riedler is global lab manager for AT&S. He has been with AT&S since 2001, eventually heading the research lab at AT&S Hinterberg in Leoben, Austria.

Samsung Develops Method to Commercialize Graphene

Samsung Electronics announced a breakthrough synthesis method to speed the commercialization of graphene, a unique material ideally suited for electronic devices. Samsung Advanced Institute of Technology (SAIT), in partnership with Sungkyunkwan University, became the first in the world to develop this new method.

"This is one of the most significant breakthroughs in graphene research in history," said the laboratory leaders at SAIT's Lab. "We expect this discovery to accelerate the commercialization of graphene, which could unlock the next era of

consumer electronic technology." Graphene has one hundred times greater electron mobility than silicon, the most widely used material in semiconductors today. It is more durable than steel and has high heat conductibility as well as flexibility, which makes it the perfect material for use in flexible displays, wearables and other next generation electronic devices.

Through its partnership with Sungkyungkwan University's School of Advanced Materials Science and Engineering, SAIT uncovered a new method of growing large area, single crystal wafer scale graphene. Engineers around the world have invested heavily in research for the commercialization of graphene, but have faced many obstacles due to the challenges associated with it. In the past, researchers have found that multi-crystal synthesis--the process of synthesizing small graphene particles to produce large-area graphene--deteriorated the electric and mechanical properties of the material, limiting its application range and making it difficult to commercialise.

The new method developed by SAIT and Sungkyunkwan University synthesizes large-area graphene into a single crystal on a semiconductor, maintaining its electric and mechanical properties. The new method repeatedly synthesizes single crystal graphene on the current semiconductor wafer scale.









ventecUSA

IPĊ

Mentor

Graphics[®] Gardien

Sponsored by:

2014

VIEWPOINT

A Strategy for Design-Through-Manufacturing

by Dan Hoz

MENTOR GRAPHICS VALOR DIVISION

Technology Convergence Critical for PCB Manufacturing

The PCB industry is showing some signs of life, which indicates that the pendulum is swinging in a more positive direction economically, but we're not quite ready to uncork the Champagne. A June 2013 report by Research & Markets forecast that the global PCB fabrication industry alone will reach about \$94 billion in 2017, with a compounded annual growth rate (CAGR) of 8.1% during this period. If we include assembly and test, the prediction exceeds \$1 trillion. This is encouraging news for those of us in the PCB design, fabrication and assembly markets, driven by consumer demand for highend products loaded with high-performance features and functionality.

Much of the growth will be in the Asia/Pacific market, with China leading as a primary manufacturing country, particularly with the increasing appreciation of Chinese currency and increasing costs of raw materials, such as copper. As a result, today's designers will be challenged to develop sophisticated new products that can be manufactured cost-effectively and efficiently.

Another trend reported by iSuppli (IHS iSupply Outsourced Manufacturing, November 2012) focusing on electronics OEMs indicates their plans to reduce the number of contract manufacturers they work with over the next year. This decision to reduce vendors is based on the need to trim their outsourced manufacturing suppliers to reduce costs, which include EMS provider and original design manufacturers (ODM). Currently, OEMs average about eight external contractors. Critical changes that OEM decision-makers must undertake with their vendors include lead-time reduction and price negotiation, according to the iSuppli study, which covered OEMs in all facets of the electronics industry: computing, communications, automo-



Engineering And Providing Balanced Interconnect Solutions



Flexible Printed Circuits • Rigid Flex • Wire Harnesses • Complete Assemblies

Our products and services are specifically designed to empower our customers to produce a product with superior performance and quality, as well as lower design, assembly, and system installation costs.

Partnering With Your Engineering Team To Deliver The Best Solution

...connecting technology

Miraco, Inc. • 102 Maple Street, Manchester, NH 03103 • miracoinc.com 603-665-9449 • Fax: 603-665-9459

PROTECTING YOUR SUPPLY CHAIN FROM COUNTERFEITS AND LIABILITY continues

tive/transportation, consumer electronics, and industrial. With China remaining a lower-cost labor force, other concerns include labor law compliance and product quality. Again, electronics companies who design and manufacture products will need to determine best practices to survive during these turbulent times since the PCB industry appears to be on an upward path.

As the general manager for the PCB manufacturing and assembly software division of a leading electronic design automation company, I need to know what I can do to positively affect our customers. Our customers tell me that they are challenged with increasing costs of raw materials, regulatory requirements, quality standards, resource management including labor, warehousing, and competitive threats that impact their bottom line. Since I am involved in the technology sector, the software products we develop need to address all of these issues and it starts with the importance of PCB design through the manufacturing and assembly process.

To remain competitive, customers who succeed in today's market realize the importance of adopt-

ing new methodologies that streamline their processes, automating manual tasks while providing high visibility of their resources, from materials management, inventory, and workflow to IT support and reporting. This is no easy task, and few software vendors can provide this level of detail, particularly with remote sites and the technical barriers between the worlds of PCB design and manufacturing.

It's imperative to consider adopting new technologies that can bridge the gap between PCB design and manufacturing. I believe that one of these bridge solutions is the ODB++ intelligent data format, which our company established. Viasystems Group Inc., PCB manu-

facturer with 14,000 employees worldwide, uses ODB++. Kent Balius, Viasystems' vice president of global front-end engineering said that standard Gerber files require one to two hours just to import, analyze and prepare data for production CAM tooling, whereas ODB++ provides intelligent data which can help drive automation and reductions in operator interactions.

> Another consideration for today's manufacturing executive is to look at a seamless methodolo-

gy where PCB design is tightly integrated with the manufacturing side of things. Since Valor was acquired by Mentor Graphics three year ago, our engineering teams have worked together to provide an intuitive approach that enables design and manufacturing teams to optimize their engineering processes bi-directionally between PCB designers, partners, systems manufacturers and the product supply chain.

The product development process needs to be a continuum supported with software that allows a feedback loop to previous steps for continuous improvement and quality. This is a key "best practice" that

has been identified by leading electronics companies to achieve best-

in-class status, according to Aberdeen Research.

Moving DFM rules into the design process and using software tools to verify that those rules are followed means that manufacturability issues can be corrected before any physical boards are made. This eliminates costly re-spins, saving a significant amount of time and cost, creating what we call the "Lean NPI Process." Transferring the resulting design data to the board fabricator sets in motion a seamless connection between both disciplines. Once this product-level NPI stage is completed, the automated setup and optimization of the production line, the process-level NPI, can be performed in a mere fraction of the time otherwise

the design process and using software tools to verify that those rules are followed means that manufacturability issues can be corrected before any physical boards are made. This eliminates costly re-spins, saving a significant amount of time and cost, creating what we call the "Lean NPI Process."

Moving DFM rules into

PROTECTING YOUR SUPPLY CHAIN FROM COUNTERFEITS AND LIABILITY continues

needed. Using a robust PCB manufacturing and assembly software suite, process setup and optimization can be performed and verified without impact to line time.

Work-order management links qualified setups for execution for all processes, and then provides real-time monitoring and visibility of equipment performance, actively driving material logistics such as Lean "Just In Time" material management, and finally, captures and analyzes test results, providing expert assistance derived from the intelligence from the ODB++ data, for the correction of any failures. Overall, this process provides the ability to deliver products created "right the first time," on time and cost-effectively.

However, the process does not end when the product leaves the shop floor. No, this is a continuum—information captured from each stage of the design-through-manufacturing flow can now be fed back into the previous steps. This improves the ability of the design analysis to model real-world fabrication and assembly capabilities and constraints, thereby further reducing any unnecessary costs, producing more competitive products and processes.

Therefore, my advice to business leaders today is to invest in new and emerging technologies that can provide a comprehensive PCB design-through-manufacturing workflow, while delivering visibility at each stage for continuous improvement. This approach can help electronics companies meet their aggressive business goals and result in a positive impact on the bottom line. **SMT**



Dan Hoz is the general manager of Mentor Graphics Valor Division. He previously served as CEO and principal accounting officer of Valor Computerized Systems Ltd.,

which was acquired by Mentor Graphics Corporation in 2010.

Video Interview Dealing With Counterfeit Components

by Real Time with... IPC APEX EXPO 2014



Michael Ford of Mentor Graphics discusses his IPC APEX EXPO poster presentation on counterfeit electronics. He points out the steps that OEMs and CEMs need to take to keep counterfeits out of their supply lines, and what companies can do to limit the damage when they do detect fake parts.



Signal Integrity in Test Fixtures

by Rob Humphrey XJTAG

FEATURE

Stable and reliable test procedures are important to avoid unnecessary, and sometimes costly, delays in production. When these require some form of test fixture connecting a device under test (DUT) to the automatic test equipment (ATE), poor signal integrity between the two can often make tests unreliable. Identifying and resolving such problems can be time consuming, but by following some simple guide-lines when designing both the DUT and fixture, test stability can be significantly improved.

JTAG Test Access Port (TAP) signals, used to implement boundary scan testing, will be used as an example, although other test and programming protocols can also benefit by following these guidelines.

Minimising the Loop Area

When signals are connected within a test fixture it is quite common for the wires carrying those signals to be given far more consideration than the return ground connection. A ground is likely to be included somewhere, but could it be improved?

With low-frequency and DC signals, the routing of ground wires relative to the signal wires can be different without any obvious side effects. However, as the frequency of the signals increases, the routing of the ground wires becomes more and more significant, up to the point where getting matched impedances is important. For TAP signals, such levels of precision are often not necessary; however minimising the loop area is a good rule of thumb.

The key to identifying the loop area is to determine:

1. The route that a signal's current will take from its source to destination. This is often easy to establish, because it is the same route as the signal's wires and tracks.

2. The route that a signal's associated return (ground) current will take from the destination back to the source. This can be slightly harder to establish, but can be approximated by assuming it stays as close to the signal as possible.

We are Commited to Delivering Outstanding Quality and Service, On-Time-our CUSTOMERS AGREE!

Prototron Team,

Technology Kitchen develops microcontroller solutions for customers in many industries. Prototypes are a key piece to our phased development process.

We have appreciated the timely responses to our requests for quotes for various quantity, delivery and board finish scenarios. The Prototron team always hits the delivery date with quality boards! We have also appreciated your willingness to drop ship to various Technology Kitchen partners.

Everyone we interact with at Prototron makes Technology Kitchen feel like we are your only customer!

Thanks,

Ken Ward, Technology Kitchen





FASTEST America's Board Shop

It is important to realise that this doesn't just cover the cables between circuit boards, but also the route of the current around each board.

To minimise the loop area, the physical area bounded by the signal and its return current should be minimised. Ideally the signal and its return will be routed directly next to one another, which can be easily achieved in a ribbon cable (Figure 1a) or a traditional twisted pair (Figure 1b). Both of these arrangements have small loop areas, and so will help improve signal quality.

As soon as the return path for the ground current takes a different route to the signal current then a much larger loop area is formed causing three problems:

1. The signal becomes much more susceptible to electromagnetic interference (EMI)—the cable becomes an aerial picking up electrical noise.

2. The signal is radiated away from the cable, creating additional electrical noise that may interfere with other signals.

3. There is a change in characteristic impedance as the signal propagates down the cable. This degrades the quality of the signal.

Figure 1c shows an obvious case where there is a larger loop area, and demonstrates how easily this can occur if care is not taken to keep the signal and return wires close together.

How to Minimise the Loop Area for Test Fixtures

Test fixtures are often created using many individual wires, one for each active signal. Although this makes it easier to wire up the fixture, it can also lead to an electrically noisy environment and consequently signal integrity problems which are particularly evident when using JTAG.

Figure 2 shows some common mistakes seen in test fixture design: The ground connection to the JTAG controller is connected to the DUT a long way away from the TAP signal connections; and the ground and TAP signal cables do not run close to each other. This can be easily,



Figure 1: The arrangement of signal and return cables using (a) ribbon cables, (b) twisted pairs, and (c) individual wires, can have a significant impact on a signal's loop area.





See videos and more about the new **Quantum**

Make the Right Move!

With the NEW Quantum[™] Fluid Dispensing System

Maximize your investment with the right automated fluid dispensing system. The new Quantum[™] is a high-performance, large-format fluid dispenser that delivers speed, flexibility, and productivity for SMT, PCBA and other microelectronics assembly applications. Reduce dispense time by 50% or apply two different materials with dualvalve configurations. Realize higher productivity with a larger dispense area and yield enhancement with patented closed-loop process control.

Recommended Applications:

- Surface mount adhesives
- Underfill
- Corner and edge bonding
- Dam and fill
- MEMS assembly

Backed by Nordson ASYMTEK's award-winning service and support network.



See Nordson ASYMTEK at SMT Nuremberg in the smarTec stand 7-219 www.nordsonasymtek.com/Quantum





Figure 2: A bad test fixture design, due to large loop areas for all TAP signal connections.



Figure 3: A good test fixture design, keeping the loop area small for all TAP signal connections.

and significantly, improved by making the following changes, as shown in Figure 3:

1. Add at least one ground test pin as close as possible to the TAP signal test pins in the test fixture. This isn't for the main ground connection used to power the board, but instead is to provide a good ground connection between the JTAG Controller and the board to improve the signal quality.

2. Use twisted or parallel pairs, each containing one signal and a ground, for each TAP signal. This is most important for the clock signal (TCK) but also any other signals that are



Figure 4: Wiring multiple signals when there are not enough ground connections on the DUT or JTAG controller.

continuously switching (i.e., TMS, TDI and TDO). When the JTAG Controller has fixed (hard) ground pins as well as configurable (soft) ground pins, a minimum of at least one hard ground connection should be used.

There does not need to be a separate ground test pin for each signal/ground pair, and instead the ground cores in multiple pairs can be connected to the same test pin. If this is not directly possible then small adapter boards can be used to share one ground connection across multiple pairs. No matter how this is achieved, it is important to keep the ground and signal wires close to each other, as shown in Figure 4.

When using connectors directly on the DUT instead of test pins, a similar philosophy can still be used. For example, separating signals in a ribbon cable so they are interleaved with ground connections is sensible whenever possible, and the importance of doing this increases as the length of cables increase. If the DUT connectors are not designed to allow this organisation then it can be achieved by creating a custom cable. This might appear to be making things more complicated than they need to be; however, as previously stated, getting this right early on can significantly reduce

the cost of fault finding later on during test development.

Minimising the Loop Area for PCB Design

To help ensure a PCB can be thoroughly and reliably tested, its testability should be considered during the design phase and not just considered as an afterthought. Design for Testability (DFT) guidelines can cover a wide range of areas, many of which focus on improving how much of a PCB can be tested. However, if the signals used to implement this testing are not considered, it is possible to design a board that can be thoroughly tested but where the tests themselves are unreliable.

Improvements to a PCB design can be split into two categories: improving signal connections to the board, and improving the signal routing within the board. The first of these should allow a test fixture to be created that can easily minimise the loop area:

• When using test pins, include one ground test point close to each TAP signal test point. If board space is limited, try to include at least one ground test point for each pair of TAP signals.

• When using headers that will be connected via ribbon cable, include ground pins

so that there is one ground core between each TAP signal in the ribbon cable. If the number of available pins is limited, as a minimum try to include ground cores on both sides of clock signals, such as TCK.

Even with a well designed test fixture and good test signal connections to the DUT, it is still possible to make JTAG tests unreliable if a PCB is not designed correctly. Leaving the routing of the TAP signals until last might initially appear to be sensible: They're only for testing the board, so why not route all functional signals first? The problem is that this can result in poorly routed signals that can make the testing unreliable, and in the worst case can even require a new board design, resulting in significant extra expense and delay.

It is worth keeping in mind that TAP signals can clock at frequencies exceeding 20 MHz. This means they should be treated just like any other signals at similar frequencies:

• Correct signal termination should be applied to the signals, as specified in JTAG DFT guidelines. These follow standard good design practices, such as placing parallel termination resistors as near to the receiver end of a track as possible.

• Avoid stubs in tracks, and use buffers to improve signal fan-out.

• Route TAP signals over a continuous ground or power plane. If there are breaks in this then the loop area is increased, making the board more susceptible to unreliability during test.

Figure 5a demonstrates how the routing of a TAP signal trace (red) across a break in a ground plane can affect the return current path (black dash). This results in a larger loop area than initially expected, deteriorating the signal integrity. Although the signal track is longer in Figure 5b, the total loop area is still reduced and so this would be the preferred solution if the ground plane could not be changed.

Summary

Minimising the loop area will always be a rule of thumb, and as such is not always applicable. However, by being more aware of the route a signal's return current will take, this can provide a solid foundation when designing PCBs, determining the pin-outs for connectors, and designing and building test fixtures. By considering this as part of the design process, costly and time-consuming delays later in the development cycle can be avoided. Where available, DFT guidelines should also be consulted, because these will contain additional information to further improve the testability of DUTs and the reliability of these tests.



Figure 5: Return current through a ground plane (black, dashed) will follow the signal trace on a different layer (red) where possible. Routing over breaks in the ground plane (a) can significantly increase the loop area, and so should be avoided (b).

What is boundary scan?

JTAG boundary scan is an electrical test method designed to overcome problems in test access generally associated with complex, high density boards. Components such as FPGAs, CPLDs and CPUs contain boundary scan technology, which allows engineers to stimulate and test the circuitry digitally with a JTAG Controller and attached software, in order to pinpoint precise locations and causes of faults.

Boundary scan reduces the requirement for test points on the circuit board, so the physical access problems associated with ICT and some functional tests are no longer an issue. The test system and boundary scan cells are connected only by means of a four or five-wire test bus, which must be considered during board design to ensure testability. Many leading vendors of JTAG boundary scan systems supply DFT guidelines to encourage design engineers to do so.

How does it work?

All the signals between a boundary scan compliant device's core logic and its pins are intercepted by a serial scan path known as the boundary scan register (BSR). In normal operation these boundary scan cells have no effect; however, in test mode the cells can be used to set and/or read values from the device pins. A set of four or five JTAG Test Access Port (TAP) signals are used by boundary scan enabled devices to allow the boundary scan data to be transferred to and from the device, allowing controlling software to analyse the circuit's performance. **SMT**



Rob Humphrey is a principal hardware engineer at XJTAG. He is responsible for the hardware and FPGA development of all XJTAG's products and also provides consultancy services and the

final level of technical support for customers.

Video Interview

Scienscope Introduces X-Ray Inspection Equipment

by Real Time with... IPC APEX EXPO 2014



Scienscope General Manager Dan Kelsey discusses the growth of his company over the past 20 years, and his drive to create high-end X-ray inspection equipment, especially for BGAs.



PCBA Test: Enabling the Right Management Practice

by NK Chari AGILENT TECHNOLOGIES

The electronics manufacturing industry, though a very mature industry with robust surface mount technology, is constantly evolving as the industry faces new challenges—both technology-driven and people- or process-related. These changes impact how test is done by each manufacturer. This article reviews the challenges and recommends key strategies for both OEMs and contract electronics manufacturers (CMs).

One of the big changes taking place is outsourcing of PCBA test strategy and test development by many OEMs to CMs, and using final functional test as the key quality gatekeeper. Many OEMs are also considering eliminating PC-BA-level functional test to reduce their costs. This outsourcing process has resulted in OEMs quickly losing their test development resources and capabilities. OEMs now expect CMs to take responsibility of all PCBA test challenges and quality.

From a technology point of view, the drive to smaller products is fuelling the trend towards more integration with package-on-package (PoP), system-on-a-chip (SoCs), complex highspeed connectors, and on-board high-speed memory devices being deployed on modern PCBA designs. All of these increase the complexity of tests and often test points may not be available due to the compact PCBA footprint.

Simultaneously, increasing labor costs are driving more automation trends with the deployment of both robots and inline methods. A recent review of these new process changes at a key OEM with their CMs revealed a number of challenges and expectations:

Availability and knowledge of advanced PCBA test

Many CMs have relied on OEMs to direct the test strategy and may not have all the necessary skill sets and expertise to understand test requirements. Some CMs and OEMs may further outsource to third-party programming houses that may or may not have all the needed technological know-how as well. Some of these test technologies include advanced boundary scan, Cover-Extend, embedded test and advanced vectorless test.

Ability to collaborate with R&D on test strategies

OEMs expect that an expert from the CM will review and suggest test strategies based on their PCBA design.

VALOR NPI GIVES YOU THE "GREEN LIGHT" TO SUCCESS

WE'LL KEEP YOU MOVING | With Mentor Graphics® Valor[™] Lean NPI Flow, New Product Introduction (NPI) engineering teams can discover a new level of integration between PCB design, manufacturing, and assembly operations. Mentor Graphics provides a unique, lean NPI flow solution, using industry standard ODB++ files to link between product models and manufacturing process definition, ready to use by shop-floor tools for programming and documentation. To maximize your overall NPI operation and to learn more click here.



©2014 Mentor Graphics Corporation. All Rights Reserved. Mentor Graphics is a registered trademark of Mentor Graphics Corporation.

PCBA TEST: ENABLING THE RIGHT MANAGEMENT PRACTICE continues

Ability to review production and test data

OEMs also expect their CMs to work collaboratively with them to improve design for testability (DFT) prior to high-volume manufacturing.

Lack of manufacturing test expertise at OEMs

OEMs may not have planned an appropriate DFT or test methods early enough, causing their CMs to face challenges of lower yield during the high volume manufacturing phase.

Lack of sensitivity to CMs' automation needs

OEMs may not understand the cost and design challenges faced by the CMs in deploying automation.

Implications of These Challenges

There is a critical need for contract manufacturers to rise up to these various challenges, because they can impact their own costs considerably. In previous business models, CMs could negotiate with their OEMs to identify the test strategy and charge them appropriately for each test process. In the new model, today's OEMs often declare that CMs manage these costs and drive quality-oriented goals at functional test. In such scenarios, if the test strategy has not been well defined, it would lead to additional cost burdens. For example, if in-circuit test access has not been catered for at the design phase, the dependency would be on functional test, which would not give the level of diagnostics needed to improve the process or repair the boards. On the other hand, OEMs may also face more challenges, especially with time-tovolume and time-to-market, as they cannot get quality boards to flow through, thereby increasing costs at final assembly. Any undetected defects can also flow to consumers, which can have negative impact to revenue and loyalty.

The overall cost to produce a printed circuit assembly comes from the cost of components, cost of manufacturing, and cost of test. It is critical for OEMs and CMs to achieve profitability and quality through design for testability. Enabling the right test technologies to ensure accurate diagnosis can not only identify product failure, but also process failures. While there is a



Figure 1: A variety of defects and variables that are tough to control.

PCBA TEST: ENABLING THE RIGHT MANAGEMENT PRACTICE continues

vision of zero defects being created in the industry, even best-in-class manufacturing sites typically have 100~500 DPMO (defects per million opportunities) for lower complexity boards and ~2000 DPMO for higher complexity boards.

There are three main contributors for product yield: design, materials, and manufacturing processes. As shown in Figure 1, there are many defects being created and these variables are difficult to control in manufacturing.

A review of test and inspection strategies Most SMT processes employ various imaging and test methods to produce defect-free PCBAs—these include pre- and post-reflow automated optical inspection (AOI), 2D or 3D automated X-ray inspection (AXI), in-circuit test (ICT, MDA, flying probers) and finally, functional test. Some of these test processes could be inline or offline sample tests. Most test and production managers would balance their test strategies, quality and output.

Table 1 gives a quick review of these test technologies. While inspection technologies like AOI and AXI are now mature and have improved the process yield, defects do still flow through to the test stages. These are further complicated by the challenge of powering the board in manufacturing test, which captures a range on defects which may not be visible otherwise.

With this broad spectrum of test strategies available, some of the critical questions often in the mind of test managers are:

How should my test engineer define the test strategy?

The definition should be based on a mix of ROI calculations, coverage of test, diagnostics effectiveness, and critically, DFT implementation. As the goal of test is to find defects, diagnostics effectiveness plays a crucial role in deciding what makes an optimal test strategy. Diagnostics effectiveness is all about how fast and accurately the root cause of the failure can be determined. The higher the diagnostic effectiveness, the lower are the rework costs and process change costs. Of course these need to be balanced with the cost of each test stage. However, it is important in the test management process to ensure the test strategy allows for the best diagnostics effectiveness.



Figure 2: Graphic line representation showing the process from paste printing through shipping.

PCBA TEST: ENABLING THE RIGHT MANAGEMENT PRACTICE continues

Technology	Benefits	Challenges	Notes
AOI	Quick and easy for operator and diagnostics Low cost Faster and possibly more consistent than an operator, especially for today's PCBA where components are very small in size (e.g., 0102 capacitors)	Only visible joints; false call rates are high	
AXI	Able to inspect solder joints beyond visual contact, such as ball grid arrays (BGAs) and plated through holes (PTHs)	Cycle time unable to keep up with production line rate Heavy shading may cause false calls in some component types, or when both sides of a board are loaded with components	Very useful for HDI and 3D devices and quality Used as a sample inspection method Need expert programming and operator skills
MDA	Low cost fixture Low system cost	Limited power up or digital test capability Limited capabilities in customizing test sequence Lower test stability and accuracy Requires constant fine tuning in test transportability	Good enough test for simple boards that have high yield functional test
Flying Prober	Does not require any fixtures Limited test access situations can be mitigated by probing on component leads, where possible	Very limited power up and digital test coverage Limited IC testing capabilities (max 4 pins at a time)	Not suitable for volume production
In-Circuit Test	Standard test platform across product types, easy to learn, implement & maintain Fast diagnostics Has integrated limited access test like boundary scan and programming capabilities	Requires test points for good test coverage Test fixture costs Does not test at-speed	Highest diagnostic value Requires good test engineering skills
Functional Test	Confirms finished good is working per the specifications from a user point of view Validates the manufacturing process prior to final assembly Able to catch faults from a system level rather than component level	Low diagnostics Challenging failure analysis Test system customized for DUT Rework costly Usually longer test times, causing bottlenecks Test specification usually not optimized for production	Functional tests range from quality verification tests (quick tests) to single loop tests & multi-loop reliability tests

Table 1: A myriad of different types of test are available today.

Does DFT enable good diagnostics?

Design teams need to have a comprehensive understanding of the available test methods, fault spectrums and plan for manufacturing tests with diagnostics effectiveness in mind. Many R&D engineers confuse coverage and overall test with diagnostics, and they do not plan for the right level of access. Critical design challenges of smaller size components and complexity will drive a continued war on PCB real estate and design engineers need to collaborate with engineering to identify ways to maximize diagnostics coverage.

Can the faults be found earlier?

As shown in Table 1, test methods from MDA, flying probers and ICT, followed by functional test have been prevalent in the industry. The key challenge is to decide what test methods to use. From a ROI perspective, finding faults during earlier manufacturing steps can reduce costs by as much as 10X. It is critical to understand projected bone piles and potential scrap based on each test method implemented. Currently, in terms of test coverage with diagnostic effectiveness, ICTs lead the effort, followed by MDA and flying probers.

To build a successful test management practice, design engineers and test engineers need to understand the following:

- The fault spectrum in manufacturing
- Each opportunity for defect creation
- How to define the test coverage
- The impact of catching the defect earlier

New Challenges with SOCs & HDIs

There is increased usage of HDI and 3D SOCs, which are prevalent on modern PCB assemblies like tablets and smartphones. The use of SSDs causes a lack of access on board real estate, so there may not be enough access to define a good test strategy. This has led to the increased use of functional test as the key gate-keeper for screening manufacturing defects—however, testing at such a downstream stage of the manufacturing process is also normally the most expensive stage.

Advocating the principle of earlier detection of such defects as a lower cost method, some ICT

test suppliers have risen to the challenge by modularizing test strategies and integrating embedded test in manufacturing. Test solutions are now available for integrating a variety of test methods, from basic ICT to complex embedded test in manufacturing, with the objective of diagnosing defects before they reach functional test.

Successful Test Management Practices

• The test engineering community needs to collaborate with design teams to ensure 100% (nets and components) coverage. While this is difficult to achieve in some cases, it is critical to engage with R & D teams on these discussions early in the process

• If access is an issue, review the design and try to answer this question: What is the cost impact of not accessing a particular net?

• Review implementation of limited access test technologies like advanced boundary scan, Cover-Extend, embedded test and bead probes to regain coverage of the nets which are otherwise not accessed

• Test engineers should simulate PCA test coverage upfront in the design process and enable the use of all technologies to ensure test coverage before functional test. There are a number of software tools available to simulate test strategies

• Review DFT processes and recommendations. There are a fair amount of tools available in the industry, including testability guidelines by TMAG/SMTA **SMT**

References

1. Duane Lowenstien, <u>Simplifying Econom-</u> ics of Test and Repair in Factory and Depot

2. Bob Neal, <u>Design For Testability</u>

3. Rosa D. Reinosa and Carl Michel, <u>Manufacturing Test Strategy Cost Model</u> 4. Stig Oresjo, <u>A New Test Strategy for Complex</u> <u>Printed Circuit Board Assemblies</u>



NK Chari is director of marketing for the Measurement Systems Division of Agilent Technologies. He leads the MSD marketing team covering in-circuit test and board/automotive functional test solutions.

The Changing Economics of In-Circuit Test

by Alan Albee

684

TERADYNE

A new brand of ICT production test systems removes the traditional barriers associated with automating electrical test. Zero footprint and multisite design concepts are changing the economics of ICT in dramatic ways for manufacturers of high-volume printed circuit board assemblies.

The Role of Test & Inspection

Test and inspection equipment used on the production floor of high-volume PCB manufacturers generally includes automated optical and X-ray inspection (AOI & AXI) imaging systems and one or more electrical test systems commonly referred to as manufacturing defect analyzers (MDA), in-circuit test (ICT) or functional test (FCT) systems. Each of these technologies is adept at detecting certain defects, and the Venn diagram shown in Figure 1 indicates that combining these techniques at various points in the manufacturing process provides the best level of confidence that the products being built are free of defects.

To support trends toward automated assembly of PCBs, the makers of test and inspection equipment have developed versions of their systems that are specifically designed to be integrated into various in-line production environments. The success of these in-line automated versions has been met with mixed success.

Imaging inspection equipment has experienced a much higher adoption rate into the automated line and it is common to find dedicated imaging systems that are integrated directly into the assembly line to perform specific tasks such as paste inspection, checking of component placement and proper soldering of device pins.

Electrical test systems like ICT have been adopted into the automated line at a much slower rate than imaging systems and it is still common for electrical test systems to remain isolated from the main automated production line—islands of test operating independently of the automated assembly line.^[1]

We Deliver...A 5-Star Performance

At U.S. Circuit, we are UL Certified to build **hybrid construction** with Rogers/FR408 family & Rogers/370HR as well as Isola I-Speed materials.

Call for a Quote: (760) 489-1413 or email: rsojitra@uscircuit.com



Manufacturer of Printed Circuit Boards U. S. Circuit, Incorporated 2071 Wineridge Place Escondido, CA 92029

Ph: (760) 489-1413 Fax: (760) 489-2965

www.uscircuit.com

Superior Quality Superior Service







ITAR Registered

MIL-PRF-55110G



Figure 1: Overlapping and complementary fault detection properties of test & inspection equipment.

In-circuit Test Automation Challenges

The slow adoption of ICT systems into the main automated assembly line is due to the fact that they have unique characteristics that make them much more challenging to automate than imaging systems.

Equipment Size

ICT systems typically contain a large variety of test modules that are utilized to electrically test the product under test. These modules include test controllers, system & user power supplies, AC & DC voltage source/measurement units, waveform generators, digitizers, timer/ counters, and high-speed digital driver and sensor pins. These instruments gain access to the product being tested through a complex switching matrix and test receiver that typically requires thousands of relays and test probes.

The physical dimensions of ICT systems are driven primarily by the required amount of test

instruments and the maximum tester pin capacity, which have typically made them much larger than imaging systems. Many ICT systems are designed with a support infrastructure that can support thousands of test pins allowing them to be used for a wide variety of product applications. This makes the equipment size quite large, even for manufacturers of small products that only require low pincount tester configurations. Automating these large general purpose electrical test systems have traditionally required large adaptation efforts, complex setup, bulky handling equipment, additional support bays and a large amount of factory floorspace.

Figure 2 shows an example of an ICT solution where the test instrumentation is integrated directly into the automation equipment. This implementation requires additional support bays to hold all the instrumentation which increases floor space and the length of the manufacturing line. Most manufacturers prefer their



Figure 2: Example automated ICT solution with extra support bays.

automation equipment to fit within a standard 19" wide instrumentation rack and that is difficult to accomplish with automated electrical test solutions that must support large numbers of pins and instruments.

Equipment Speeds

Assembly equipment speeds have continued to improve since the advent of automated PCB manufacturing. A nearly threefold improvement in assembly speeds have placed pressure on downstream test and inspection equipment to improve their operational speeds so as to keep up with the "beat rate" and avoid becoming the bottleneck on the production floor.

Unlike imaging test systems, the throughput limitations of ICT systems are bound by the physics of performing electrical tests. To perform electrical tests, relays must be opened and closed, test instruments must be turned on and off, residual voltages must be discharged, component setup and hold times must be obeyed, and components that are not being tested must be guarded or disabled so that they do not interfere with the components under test. Most of the test time associated with performing electrical tests is related to performing the above activities and the tester instruments and computer are often sitting idle waiting for them to complete. This means that the throughput of ICT systems cannot be dramatically improved by adding enhanced instrumentation or a higher performance CPU.

Because of this, ICT systems can become a bottleneck on the production line forcing manufacturers to perform ICT using multiple offline test systems or requiring them to add multiple ICT systems in-line, which increases overall manufacturing floorspace requirements.

Electrical Measurement Integrity

ICT systems must make electrical test contact with the product being tested so that it is able to electrically stimulate and measure test points on the circuit board. The product that is being tested usually sits on a bed-of-nails fixture that is custom designed to make electrical connections between targeted nets on the PCB and the tester receiver interface. When the test fixture is placed on the ICT system and the PCB is placed in the test fixture, the tester is able to perform electrical tests on all nets that have test access.

The fact that ICT systems require a test fixture and must physically contact the printed circuit board under test places a greater constraint on them compared to imaging or other test techniques that do not need to physically touch the circuit board. ICT system designers take great care to keep the signal paths between the tester instruments and the tester receiver as short as possible so as to maintain the integrity and reliability of the electrical test measurements. To obtain best performance, ICT systems minimize the impedance and inductance in the signal path and try to keep the distance between the instruments and the tester receiver as short as possible.

When adding ICT systems to an automated production environment, the manufacturer must accommodate interfacing both the custom test fixture as well as the test instruments inside of the automation handling equipment.

Because of limited factory floorspace, some automation solutions may end up placing the ICT system instrument bay behind the handler rather than under it; this results in extra-long cables (two feet or more) between the test instruments and the test fixture which can nega-

tively impact the capacity of the ICT system to perform accurate and reliable tests.

When an integration approach that significantly increases the measurement path is used, the ICT system is still capable of detecting many electrical defects, but it will most likely no longer be able to meet the full accuracy and instrument performance specifications that are outlined in its technical product documents.

Ease of Maintenance & Repair

Automated manufacturing lines are only productive when the equipment on the line is up and

running properly. Any equipment on the line that malfunctions can halt manufacturing, resulting in costly delays and lost production time. Therefore, it is important to be able to quickly service and repair the equipment on the line when something does go wrong. The goal is to keep maintenance times as short as possible so that the manufacturer achieves high equipment utilization.

ICT systems have unique service and maintenance challenges compared to other equipment in the automated production line. The probes used to make electrical test contact in the tester receiver interface and the test fixture are subject to wear after repeated use and the relays that make up the switching subsystem may need to be replaced after their rated lifespan is exceeded. The electrical specifications of the tester instruments must also be calibrated to external standards at regular intervals to identify when there is any loss of precision that could affect test measurements.

The maintenance and repair of automated ICT systems has historically been difficult and

The probes used to make electrical test contact in the tester receiver interface and the test fixture are subject to wear after repeated use and the relays that make up the switching subsystem may need to be replaced after their rated lifespan is exceeded.

time consuming. because the test fixture and sometimes even the conveyor automation hardware, needs to be removed from the test equipment so the service technician can run the diagnostic programs and get access to the tester electronics. Replacing a faulty instrument

or relay on some automated ICT systems requires technicians to pull

out the instrument from under the handler and rotate the pin cage to perform a simple board exchange. After replacing the board, technicians must put the whole system back together and make sure it is aligned and operating properly.

 The additional complexities associated with servicing automated ICT systems contributes to longer down times, lower equipment utilization rates and the need for manufacturers to keep highly trained technicians on staff to troubleshoot and fix equipment

failures.

Solving ICT Automation Challenges

Many of the challenges previously described are directly related to the fact that most ICT systems are not designed with automation in mind; and most automation equipment is not designed with ICT in mind.

Historically, combining automation and ICT was performed as an afterthought, an arrangement that typically resulted in trying to adapt manual test systems by adding conveyors and special tooling or by imposing a tax on automation equipment to support the space and routing demands of electrical test equipment.

Designing an ICT System with Automation in Mind

A project team of engineers and designers were commissioned to create a new brand of ICT system designed from the ground up with automation in mind, having the features and characteristics necessary to resolve the previously outlined challenges.

The high level goals that served as the driving requirements behind the project consisted of four major elements:

1. A zero footprint concept that allows installation of the electrical test components into standard size automation equipment—without adding extra length to the assembly line.

2. A multisite concept that allows expansion of the electrical test throughput capacity of the ICT system without the need to add new test systems.

3. A selectable receiver concept that allows the test system to be configured with a variety of high integrity test fixture connection schemes.

4. A "clean connect" concept that simplifies maintenance and repair activities of the electrical components of the test system.

The engineering team designing the new brand of ICT system incorporated a number of key changes that contributed toward achieving these design concepts.

Shrinking Equipment Size

One of the biggest obstacles to fitting an ICT system into the standard 19" space typically reserved for automated test and inspection equipment is the infrastructure built-into the tester to support testing of complex PCB assemblies with more than 3000 nets. An electrical test system capable of testing large net count boards requires a large switching subsystem that takes up a lot of space.

Historically, ICT system manufacturers have developed test systems with a one-size-fits-all approach, capable of testing the highest complexity PCB assemblies. This resulted in electrical test systems with large receiver interfaces, large instrument backplanes, numerous user power supplies and all of the related infrastructure that is required to support high complexity test applications.

During market discovery activities, it was determined that the majority of manufacturers building high-volume products on automated assembly lines do not generally require high pincount capacity test systems. It was learned that most high-volume automated manufacturers are building products that have less than 2000 nets and often less than 1000 nets. It was also learned that these applications seldom required more than three user power supplies.

Based on those discoveries it was decided to optimize the design of the new brand of automated electrical tester around pincounts of 640, 1280 and 2560, and to reduce the maximum number of user power supplies from 14 to 5. These optimization decisions allowed the designers to reduce the size of the tester backplane by 66% and 83% compared to traditional test systems, and it significantly reduced the mechanical and electrical infrastructure associated with supporting large pincount test systems. By tuning the tester electrically and mechanically to the typical size of the products they are building, high-volume manufacturers building smaller pincount products are not burdened with the overhead of accomodating test features that they never intend to use.

Increasing the Density of the Pin Fields

In a typical in-line production environment, the dimension of width matters much more to the manufacturer and the automation equipment supplier than the dimensions of depth or height. It is the width of the assembly and test equipment more than anything else that determines the total length of the assembly line and the amount of floorspace that is required. Manufacturers often have extra space directly above or behind the automated assembly line that is not being utilized.

With this knowledge in mind, the high-density pin boards utilized in the new brand of automated ICT system optimizes the number of pins available in the depth dimension so that less space is required in the width dimension. With this approach the designers were able to support approximately 400 test pins per linear inch of width and 2560 test pins in less than 6.5 linear inches, which effectively doubled the density of previous systems and ensured that fully configured test systems would fit easily within 19" automation equipment enclosures.

Implementing Flexible Fixture Options

Discussions with automated PCBA manufacturers revealed no consensus with regard to

the type of receiver interface that the electrical system should support.

Some manufacturers preferred the standard pogo-pin/bed-of-nails vacuum type fixtures, some manufacturers wanted the bed-of-nails interface with a pneumatic-type fixture. Some manufacturers wanted a press-down unit with a low-cost cassette type fixture, some wanted a simple Pylon type wire post interface that allowed them to wire wrap to a custom fixture interface that was compatible with an existing fixture.

Based on these diverse requests, the engineering team designed the new brand of ICT system with a selectable receiver interface. The system can be configured with a vacuum based pogo-pin interface, non-vacuum pogo pin interface, wire-wrap type interface, or no interface at all so that it can customized by the end user to meet their specific requirements.

The decision to support selectable receiver types had implications for the self-test and accuracy verification routines that are provided to ensure the test system is operating correctly and that the instruments are within specifications. These routines require self-test and verification fixtures designed to connect precision components on the fixtures to the tester instruments. Rather than design numerous self-test/accuracy fixtures for different receiver types, the design team decided to create a self-test module that plugs directly into the tester backplane which can be used by manufacturers and service engineers regardless of the selected receiver type.

Simplifying Installation and Maintenance

The goal for the new brand of ICT system was to fit into anyone's automation equipment. The first step toward achieving that goal was to make the test system smaller. The second step was to understand the constraints of the most common automation equipment in the marketplace.

For this step the design team reviewed different automation equipment designs and did a tour of Integrator/Handler equipment manufacturers to ensure that the new ICT system would not violate any of their design constraints.

The design team took care to ensure that mounting features incorporated on each of the electrical test modules would enable fast and reliable attachment to the automation equipment.

The connections between each of the electrical test modules were also designed to provide quick and secure attachment by incorporating snap connectors, eliminating lengthy umbilical cords between modules and reducing the amount of required manual assembly steps. All of the major modules were designed for easy serviceability, accessible from the front of the system without having to perform complex disassembly and assembly procedures.

Figure 3 shows a picture of the resulting electrical test subsystem ready for integration into automated handling equipment. It is designed specifically with automation in mind and has the same capabilities of the much larger system



Figure 3: Compact ICT subsystem designed for automation.



Figure 4: ICT Subsystem designed for easy integration.

on which it is based, but it is six times smaller.

Its small footprint, high-density pin fields and snap together modules result in a very compact electrical test subsystem that is easy to integrate into a wide variety of automation equipment, either inline or offline as part of manual work cells (Figure 4). It is designed to be easy to service and has short connection paths that provide excellent signal integrity.

Achieving Faster Equipment Speeds

Multisite testing is a concept pioneered by manufacturers of semiconductor chip test equipment. Multisite test systems allowed chip manufacturers to test multiple devices in parallel by providing duplicate instruments in their test systems that support testing of more than one device at a time.

While examining the characteristics of PCBs being built by high-volume automated assembly lines, it was noted that a large majority of these products are built as part of panelized assemblies—the same identical board replicated on a panel multiple times. Panelized assemblies are employed by manufacturers to optimize the



Figure 5: Example of semiconductor multisite interface board.

performance of the assembly equipment and improve line utilization.

The problem is that the performance of most ICT systems does not improve when testing panelized boards because the ICT system has limited instruments and can only support testing one board at a time. For example, the test time required to test a 4-board panel on

most ICT systems is 4x the amount of time it takes to test a single board.

To gain the benefits of improved test throughput for panelized type board designs, the engineering team extended the semiconductor concept of multisite testing to the design of the new brand ICT system. The multisite design exploits the parallelism found in panelized boards.

Up to four ICT test modules, each with test instruments that are capable of simultaneously testing a single board, can be added to the system. Economies are achieved by sharing site resources where it is possible (power supplies, receiver, display, bar code, etc.).

Due to the overall system size reductions achieved, it was possible to add multiple test sites to the new ICT system without exceeding the available space inside the automation equipment. This made it possible to expand test throughput capacity without expanding manufacturing floor space requirements.

Figure 6 is similar to Figure 3, except that it shows the ICT subsystem in a dual-site configuration. The dual-site configuration is capable of testing two identical PCBs at the same time, effectively doubling the test throughput of a single site tester. A third or fourth site could be added to achieve 3x or 4x the test throughput of a single site tester. Unlike some ICT systems that do not support parallel testing of all ICT test, this innovative multisite ICT design supports parallel testing of all ICT test techniques, which allows manufacturers to truly get the performance of 2, 3, or 4 test systems in a single test system that is approximately half the size of one traditional ICT system.

For simplicity, the use model for developing test programs for the multisite tester is the same as it is for developing programs for single site systems. In both cases, the user develops and debugs a single test program. Once the program is debugged and running, the software replicates the program to simultaneously test other boards using the other test sites. Each test module has dedicated hardware and PC controllers and can execute tests independently of the other moduless—however synchronization signals are built into the design so that develo-



Figure 6: Multisite configuration of compact electrical test subsystem with two test modules.

pers can synchronize the modules to suit the test application.

Changing ICT Test Economics

High-volume PCB manufacturers can make use of these new brand of ICT systems which are optimized for automation and parallel test efficiency to dramatically lower the total ownership costs of the ICT systems in their production test facilities. Savings can be achieved in three important areas: acquistion costs, fixture costs, and operator costs.

Lower Capital Equipment Costs

Because multisite test systems have parallel test capabilities it is possible for them to test up to 4x faster than traditional ICT systems. A single multisite system could replace 4 traditional ICT systems while taking up less than half the floorspace of one traditional ICT system.

The capital equipment cost for a multisite tester is more expensive than a traditional ICT system, but buying one dual-site ICT system is approximately 30% less expensive than buying two traditional ICT systems—and the cost savings become even greater with tri and quad multisite configured ICT systems.
THE CHANGING ECONOMICS OF IN-CIRCUIT TEST continues



Figure 7: Screenshot showing two boards being tested in parallel.

Because of the high throughput capacity of the multisite systems it becomes possible to replace multiple offline standard ICT systems on the production floor with a single inline multisite ICT system, thus reducing equipment costs, overall factory floorspace requirements and handling time.

Reduced Fixture Costs

Standard ICT systems used in high-volume production lines can often not keep up with the beat rate of the assembly equipment. In order to keep up with the volume of PCBs being produced these manufacturers must usually dedicate two or more standard ICT systems to each high-volume assembly line. Each ICT system requires its own test fixture, which can become a significant recurring cost to the manufacturer over time.

Since one multisite ICT system can have

the test capacity of four standard ICT systems, high-volume manufacturers can deploy a single test system on the production line that only requires a single test fixture—thereby eliminating the purchase costs of duplicate fixtures and lowering the manufacturer's recurring fixture acquisition costs by half or more.

Reduced Operator Costs

The new brand of ICT system removes many of the barriers that were previously in place for automating in-circuit test. With these barriers removed, manufacturers can benefit from moving from an offline ICT operation to an operator-free inline ICT operation.

Making this move can significantly reduce labor costs for the manufacturer while simultaneously reducing handling time and improving test reliability.

THE CHANGING ECONOMICS OF IN-CIRCUIT TEST continues

Even if the manufacturer decides to continue using offline ICT test systems, the offline multisite tester configuration still lowers labor costs because a single multisite tester, with one test operator, can do the work of four standard testers requiring four test operators.

An Example Cost Comparison

To highlight the economic benefits that can be achieved by high-volume manufacturers with the new brand of ICT system, Table 1 shows the three-year ICT ownership costs for an inline dual-site ICT system compared with the costs of two standard offline ICT systems.

These numbers were derived in consultation with a manufacturer who was estimating the costs of setting up a high-volume assembly line on their production floor. The manufacturer calculated that a single standard ICT system would not be capable of keeping up with the beat rate of the production line and that at least two standard ICT systems would be required to test the expected product volumes.

The manufacturer also estimated that the assembly line was likely to be retooled 11 times for different product designs over the course of three years and that the average ICT fixture cost for each new product design would be \$15K.

The cost comparison exercise showed the manufacturer that the inline multisite test approach would save them \$651K over three

years, compared to the two standard offline ICT system approach.

The savings realized by the manufacturer in lower fixture and operator costs alone outweighed the initial capital equipment costs. The economic model showed that even if it were possible to acquire two offline standard ICT systems for free, the three-year ownership costs of the inline multisite solution would still be \$275K less expensive!

Acknowledgements

The author would like to thank John Arena and Bobby Griffis of Teradyne for their contributions to many of the ideas and concepts presented in this article. **SMT**

References

1. A. Albee, B. Griffis, "New Directions in Electrical Test Scalabality and Automation," SMTA International Conference Proceedings, October 2013.



Alan Albee is a product manager working in Teradyne's Production Test Group. He has authored numerous technical articles on topics related to board test, and he has been awarded two patents.

Costs	ONE Inline -Dual Site ICT System	Two Offline Standard ICT Systems
System	1 System	2 Systems
	\$250K	\$376K
Fixture	11 Fixtures	22 Fixtures
	\$165K	\$330K
Operator	0 Operators	2 Operators/2 Shifts
		\$30K/yr Salary
	\$0	\$360K
Total Cost	\$415K	\$1066K

Table 1: Three-year ownership cost comparison, inline multisite ICT system vs. offline standard ICT system.

The Absolute Best Value in High Technology Printed Circuit Boards

MIN 1

Since 1979, Eagle Electronics Inc. has provided our customers with the highest quality Printed Circuit Boards at fair and competitive prices. From our modern 50,000 sq. ft. facility, we continue to meet and exceed our customer's ever increasing expectations and requirements.

101003

001101 01001

101010101010101010101000101010101010



MANUFACTURERS OF QUALITY PRINTED CIRCUIT BOARDS

- Prototype to Production
- Time Critical Production
- · Commitment to Customer Service
- Best Quality Performance
- Best On-Time Delivery Performance
- Fair and Competitive Pricing/Costs
- Rapid Response to Quote Requests
- Flexibility Scheduling
- Stock/Consigned Inventory Programs

click here to learn more

www.eagle-elec.com

S<u>M</u>Tonline Market News Highlights



Conference Board Labor Market Improving

The economy generated a gain of 192,000 jobs in March. Undoubtedly, there was some catch up in hiring following the inclement weather this winter. Still, the underlying trend is encouraging, with more good news expected this spring and summer. This confirms the signals from The Conference Board's Consumer Confidence Index and Leading Economic Index for the U.S.

Energy Efficiency Retrofits to Top \$127B by 2023

Efforts to reduce energy consumption and greenhouse gas emissions have led to increasing deployments of energy efficiency retrofits for commercial and public buildings. According to a new report from Navigant Research, the worldwide market for energy efficiency retrofits in commercial and public buildings will grow from \$68.2 billion in 2014 to \$127.5 billion by 2023.

Global TV Market Continues to Drop

The global television market shrank last year for the second year in a row after total shipments declined by 6% from already soft 2012 levels, accompanied this time by a rare deceleration in the liquid-crystal display (LCD) TV space in China, Asia-Pacific, and Eastern Europe, according to a new report from IHS Technology.

<u>3D Printing Market to Reach</u> <u>\$16.2B in 2018</u>

Canalys predicts that the 3D printing market, including 3D printer sales, materials, and associated services, will rise to \$3.8 billion in 2014, with the market continuing to experience rapid growth, reaching \$16.2 billion by 2018.

BBVA Compass: U.S. Economy Not at Risk of Deflation

As experts debate what the Federal Reserve should do about inflation, BBVA Compass economists say in their latest research that the policymaking board shouldn't divert from its timeline on tapering because the U.S. economy is not at risk of tipping into deflation.

Global Smartphone Market to See CAGR of 15.3%

Analysts forecast the global smartphone market will grow at a CAGR of 15.3% during the period 2013–2018. One of the key factors contributing to this market growth is the declining ASP of smartphones. The global smartphone market has also been witnessing increasing demand for largescreen smartphones.

Industrial Electronics Chip Market Rebounds

Powered by the freshly-fueled gears of reviving economies, the global market for semiconductors used in industrial electronics applications overcame a serious fall in 2012 and roared back to life last year, boding well for an even more energetic 2014.

Report: Test & Measurement in the Global EMS Market

This study analyzes growth opportunities and trends in test and measurement for EMS providers, as increasing complexity of assembly and miniaturization of components bolster demand for testing services. OEMs are increasing reliance on EMS partners for product quality assurance.

MEMS Combo Sensors Revenue Continues to Climb

Combo sensors are headed for another major growth spurt this year in the global microelectromechanical systems (MEMS) sensor market as revenue climbs an expansive 37% after two years of already phenomenal increases, according to new analysis from IHS Technology.

Dell, HP See Growth in Worldwide PC Monitor Market

"Dell and HP both saw increases in unit shipments for the worldwide PC monitor market for the second time in a down year," said Jennifer Song, research analyst, Worldwide Trackers at IDC. "At a regional level, EMEA experienced the largest positive growth during the fourth quarter, with Italy and Spain posting the biggest gains."

INTRODUCING THE AKILA ALL-IN-ONE DOFFS UNIT For Use with MS2®



Why sell your dross to a recycler for a fraction of its true value? Ask us about the new compact Akila off-line solder recovery unit that, along with our MS2[®] Molten Solder Surfactant, takes the guesswork out of the solder recovery process.

- Easily convert dross into usable solder bars
- Fully enclosed machine
- Fume-free operation
- "Plug & Play" set up
- Small footprint



Contact sales @pkaymetal.com for more information. (323) 585-5058





The Future of Test

by Richard Ayes I-CONNECT007

In an interview with *I-Connect007*, editor Richard Ayes, and Steve Brown, vice president of quality and engineering for SMTC Corp., discuss the issues surrounding testing and inspection of electronics assemblies—from technologies and challenges, to cost—from the perspective of an EMS company. Brown also sounds off on the future of the EMS industry. Here is an excerpt of that interview:

When it comes to SMT assembly inspection and testing, what are the biggest challenges being faced by a company like SMTC?

The primary SMT inspection and test challenges can be grouped into three major categories: design, process and cost. Design ultimately dictates the access and coverage that can be achieved, whereas the technology drives the type of test that can be applied. Process can dictate the number of opportunities for error where increased manual operations can drive increased inspection and test to maintain quality, whereas a more automated solution provides a lower defect per million opportunity output.

Cost is always a challenge. Some customers perceive test as a cost rather than a value driver. A cost-effective test/inspection strategy is fluid during the product lifecycle and can change significantly given volumes, product price challenges and value associated with test/inspection. At SMTC, we look at the entire test chain from PCBA all the way through to the product level functional test when developing a test strategy. SMT assembly inspection and testing is an important part of any test plan as it iden-

Privately Held Global Printed Circuit Board Fabrication

LOCAL SUPPORT

and a WORLD of Circuit Board Manufacturing Options

USA

GERMANY

JORDAN

TAIWAN

CHINA

Manufacturing at ANY Volume, both On and Offshore Quick Turn, Prototypes, DFM, Global Management Specialties like Rogers, Aluminum, Hybrid Materials Logistics including Consignment, VMI, JIT & More 24-7 Local Engineering, Service, and Support

Download Digital Brochure

Download Our Capabilities

sales@htglobalcircuits.com

(727) 327-6236

www.htglobalcircuits.com

GLOBAL CIRCUITS

THE FUTURE OF TEST continues



tifies defects upstream in the process where the feedback loops are real time and repair costs are the lowest. We use a comprehensive approach that considers all test sectors, from automated optical inspection (AOI) to functional test, and put together a plan that is product-specific and removes the redundancy of testing the same characteristic multiple times. In this way, we maximize the effectiveness of the test suite while minimizing the cost of quality across the supply chain.

That is why in our experience, early supplier involvement during the product design phase in a design for test (DFT) engagement is so important. In working together as early as possible, we can ensure that the design offers the right opportunities for test coverage and that we apply that coverage in the real world to maximize first pass yields in our assembly processes, verify sub-component operation, and deliver the lowest possible field failure rates for the customer.

Are the technologies you are using now capable of addressing most of the inspection and testing challenges you refer to?

Yes, in most cases, as technology has continued to advance in all areas, and in a number of cases, it provides overlapping test coverage across equipment sets with complementary technologies. This provides options for reduced levels of inspection/test and more flexible/customized test strategies.

AOI systems now have higher resolution cameras to cover smaller components, are better at detecting poor solder joints, and can now cover co-planarity issues by using angular views. X-ray technology has standardized on oblique angles for detection of non-wetting opens/ head-in-pillow defects and with the addition of digital tomosynthesis, we have a greater ability to inspect 3D packages like package-on-package (PoP) with better resolution/field of view than ever before.

Flying probe equipment can handle finer pitches with higher accuracy, have added top and bottom probes for better throughput, and have added features like power on tests. Manufacturing defect analyzers (MDA) have added higher probe counts and additional test features, while ICT has seen advances in mechanical fixturing so that we add probes down to .018" apart, to access denser products with finer pitch components.

Advances in functional test software and hardware have allowed us to capture more parametric information than ever, especially in application areas such as RF and optical.

Is there need for an even better test/inspection solution? If so, what should it be like, considering the increasing complexity in electronics assembly and the continuing miniaturization trend of components?

At SMTC, we are continuously evaluating new platforms and test techniques to ensure we are one step ahead of the next challenge. This is driven from technology roadmap sessions we hold with our customers on an annual basis. From our perspective, we would like to see more cost-effective detection techniques at the primary attach operation to make it more of a closed-loop operation with immediate feedback. Integrated and cost-effective AOI solutions at chip placement are a prime example. As technology continues to trend to smaller packages and stacked packages, where access is limited, test methods such as JTAG become almost mandatory. More robust boundary scan libraries that include the testing of core logic in

THE FUTURE OF TEST continues

addition to existing structural tests would be a real gain.

How did the move towards lead-free solder impact the test/inspection process? Did it entail a complete process change and present new defects that need rectification?

The move to lead-free did present several challenges to the test sectors within SMTC. As you know, the transition to lead-free introduced many new materials to the assembly process, from chemistry to raw laminates that required elevated thermal cycles and tended to cause increased PCB warpage, leave harder residues, and chang component termination/surface finishes. This transition introduced a set of defects around cracked joints or internal trace separation on higher layer boards, test pad contact issues due to harder residues. Changes to our DFM and Test (DFX) rules required increased probe maintenance and required us to revisit component pad to test point clearances; in some cases, it drove increased keep out or cleaning that did not require this process before.

Through the application of design of experiments (DOE), root cause corrective action (RCCA), and the introduction of second and third generation materials, these areas were able to be addressed. As a result, our design guidelines have been updated to reflect SMTC's recommendations for lead-free chemistries and are in volume production today at very high quality levels.

Would you say that in-circuit testing has come to its limits in terms of board accessibility and utilization flexibility, and that boundary scan is the logical successor or makes the most sense for achieving the highest possible test coverage?

In-circuit test [ICT] is still the benchmark tool for component-level electrical testing, and in most cases, still provides a high level of coverage and access primarily though advances in fixturing and tighter tolerances. We see boundary scan/JTAG as complimentary test technologies in combination with ICT to provide the required levels of coverage. While boundary scan is important, it misses discrete component testing and analog parts where the majority of the defects still occur today. On their own, they provide a piece of the puzzle; we believe the best solution is the continued use of JTAG within ICT.

On lower-density products, we commonly look to lower-cost test solutions where ICT may not be appropriate or has an undesirable return on investment due to lower product volumes and higher mix products. In these cases, test solutions including AOI, flying probe (fixture-less ICT) or MDA can deliver a comprehensive and cost-effective solution to our customers.

What about testing cost? Does it still have a significant impact in your process?

Test cost is commonly viewed as being limited to the cost to perform the test on the manufacturing floor, but this is only part of the total test costs, and minimizing these costs may in fact increase the overall costs of the product over the entire supply chain. Since the purpose of test is to provide a level of quality both during manufacturing and out in the field, the objective should be to minimize the total cost of quality (COQ). Minimizing the overall COQ for our customer is best practice for defining the process and test strategy.

A typical product COQ will include the costs of the test itself, costs associated with process fallout/repair and re-inspection, product scrap costs, costs associated with test fallout/repair and re-test and field failures. Our experience has shown that field failures are at least four times more expensive to repair whereas early detection of defects upstream is a fraction of that cost.

To minimize the overall cost of quality, defect detection should be driven up the supply chain, ideally to the point of use. An effective test plan utilizes the effective access to develop and address coverage gaps to allow early detection of problems in, say, sub component quality, and provide an efficient and effective closed loop to prevent escapes. This greatly decreases the risk to the customer and limits opportunities for large field issues requiring recalls and associated costs.

THE FUTURE OF TEST continues

An effective test plan provides the shortest path to defect detection and correction. Significant impacts to process are caused when test/ inspection are used as final verification only and drive higher level troubleshoot and repair loops that could otherwise have been avoided/ minimized.

Where do you think the test/inspection equipment segment is headed? What new technologies are coming online?

One of the trends we are seeing is in the introduction of targeted test solutions for certain segments. AOI machines dedicated to UV for testing conformal coating applications are a good example. Stand-alone plug-ins for ICT that address memory and flash applications would be another.

We also see the next generation of combination units, AOI and X-ray for example, appearing on the market as the industry continues to improve cost and reduce cycle times. Finally, we are seeing more holistic coverage tools which help deliver better test optimization solutions. All of these areas are of interest to SMTC.

How do you see the EMS industry performing this year? What opportunities and challenges are you expecting?

Overall, the EMS industry continues to grow, and we see many opportunities with first-time outsourcers in many new market segments. We are seeing more opportunities to provide a broader range of services to our customer base. Product design, DFX and functional test development are areas of note in addition to our more traditional work around ICT development, alternate sourcing, and other value proposals we make to our customers. We are also seeing a lot of interest in having products manufactured in Mexico.

What strategies has SMTC put in place to address EMS industry challenges?

We have added a strong design and functional test presence through our partnership with Idneo, a world-class development team



based in San Jose, California, and Europe. We also continue to scale our operations in Chihuahua, Mexico, with plans to add more capability in metal fabrication, PCBA, and industry certifications. We will be adding TS16949 to support automotive customer for example.

Finally, please enlighten us on some of your plans for this year.

As always, it begins with holding effective technology roadmapping sessions with our customers and we will continue to do that this year. On the assembly side, we are implementing more PoP capability across our operations network, moving to halogen-free chemistries, placing ever larger BGAs, ever-smaller chips (01005s), and enhancing our configure-to-order offering.

In test, we will be enhancing our test analysis and coverage optimization tools to identify and address redundancy to provide more costeffective test solutions. Finally we will also be making a significant upgrade to our factory operations software package, which will allow customers better access to production and test information and enhance our product traceability capabilities. **SMT**



Steve Brown is vice president, quality and engineering for SMTC. He is responsible for overseeing SMTC's global quality management system and technology roadmap develop-

ment and implementation.

SMTA / TMAG Release Latest Testability Guidelines Revision E

The Surface Mount Technology Association (SMTA) and the Testability Management Action Group (TMAG) announce the recent release of the SMTA/TMAG Testability Guidelines TP-101E.

The SMTA/TMAG Testability Guidelines were constructed by several groups of test and testability professionals working in various Task Forces, each contributing separate chapters. The Guidelines were intended to assist the reader in dealing with testability considerations necessary for the design, development, and test of a product.

The latest revision supersedes the 2008 SMTA Testability Guidelines TP-101D. The chapters most affected by these revisions include Chapter 2 on Probing and Fixturing Guidelines and Chapter 4, Vectorless Test and Fixturing Guidelines that now includes the IEEE-1149.8.1 criteria. Several revisions were also made to Chapter 6, X-Ray Inspection Guidelines. While other chapters remained pretty much unchanged, known errors and critical changes were made as needed throughout the document. Several other chapters had some new guidelines added and when warranted some guidelines eliminated.



Companies contributing to this revision include A.T.E. Solutions, Inc., Agilent Technologies, Huawei Technologies, Jabil Circuit, Inc., Nordson DAGE, and more. The guidelines are available in electronic format through the SMTA BookStore. Corporate and global site licenses are also available.



For more information about the guidelines, contact SMTA Director of Communications Ryan Flaherty. (952-920-7682 or ryan@smta.org)



The SMTA membership is an international network of professionals who build skills, share practical experience and develop solutions in electronic assembly technologies, including microsystems, emerging technologies, and related business operations.



The Testability Management Action Group (TMAG) is a grass roots organization made up of test professionals who believe that success for Testability in general, and Design for Testability (DFT) in particular, requires the involvement and the support of management at all levels.

Mil/Aero007 News Highlights



Peter Sarmanian Corporate Award Goes to Raytheon

IPC is recognizing Raytheon's ongoing support by awarding the company with its Peter Sarmanian Corporate Recognition Award, which recognizes an IPC member corporation that has made contributions to the printed board industry and supported IPC through participation in technical and/ or management programs.

IPC Voices Stand on RoHS2

Substance Revisions

IPC highlighted its disagreement with the UBA identification and ranking of TBBPA as a second highest priority substance for potential restriction under the RoHS Directive. According to an EU Risk Assessment, TBBPA has been found to be safe for human health and the environment and should not be considered for further assessment under the Directive.

FTG to Supply Heads-up Display to LIEOE's C919 Aircraft

Under the terms of the LOI, FTG will design, develop, manufacture, and supply the HUD CPA. The design, development and initial manufacturing will be completed at FTG Aerospace—Toronto. Volume manufacturing will be performed at the company's facility in Tianjin, China.

BEST Launches New "Shop Vac" for PCBs

The new PCBVac a shop vac can clean up both unwanted liquids and solids from a PCB. This adjustable vacuum cleaning system allows you to connect to clean, filtered shop air and then have a hand held tool in your hand to get around and underneath components.

Sparton, USSI Win \$13.3M in Foreign Sales Contracts

Sparton Corporation and USSI, a subsidiary of Ultra Electronics Holdings plc (ULE), announce the award of subcontracts valued at \$13.3 million from their ERAPSCO/Sonobuoy TechSystems joint venture.

Declining Defense Orders Lower PartnerTech's 2013 Sales

Net sales for the year totalled SEK 2,237 million, compared with the previous year's SEK 2,242 million. Increased sales toward the end of the year, to both new and existing customers, could not offset the weaker start to the year and declining defense orders, as well as the realignment process in Norway.

Ducommun Expands Supplier Gold Status from Sikorsky

Ducommun Incorporated has earned Supplier Gold status from Sikorsky Aircraft Corporation, a subsidiary of United Technologies Corporation, at its Berryville and Huntsville, Arkansas facilities. Ducommun's Joplin, Missouri plant has maintained UTC Supplier Gold status since 2010. The facilities manufacture complex custom interconnect and electronic assemblies for Sikorsky's BLACK HAWK helicopters.

MTI Electronics Achieves Recertifications

MTI Electronics Inc, an Electronic Manufacturing Services provider, announced that it has been re-certified to the new ISO 9001:2008, ISO 13485:2003 and AS9100C for the manufacture of PCBAs.

Kitron to Supply Electronics Modules to Kongsberg Gruppen

Kitron has received a new order worth approximately NOK 30 million from Kongsberg Gruppen to supply electronics modules for integration in Kongsberg's weapon guidance system Remote Weapon Station (RWS). In addition, Kitron has received a prognosis for orders of a further NOK 20 million.

Ducommun Nets Osprey Contracts from Bell Helicopter

Ducommun Incorporated has received contracts valued at \$5.6 million from Bell Helicopter, a subsidiary of Textron, Inc., to provide electronic assemblies and wiring harnesses for the V-22 Osprey tiltrotor military aircraft through January 2015.

here at Hunter Technology, **we make it happen!**

For over forty-five years now, we have been "making it happen" for our customers. By having an unsurpassed committment to quality.By providing the EMS services that you need. And mostly by being there for you, every step of the way. Here's what our customers are saying:



We couldn't make anything happen without our great staff. Here are few words from the people that make it happen:



Call us today to find out what we can make happen for you!



+1 (408) 957-1300 www.hunter-technology.com **KRAMER ON COMPONENTS**

Independent Distributor: Supply Chain's Best Friend or Worst Enemy

by Todd Kramer

SECURE COMPONENTS LLC

I started earning my living brokering electronic components in 2001. I quickly learned that the term "broker" came with some very negative preconceptions, such as the idea that brokers were unscrupulous liars, cheaters, etc. While much has changed about the component industry, much remains the same.

As independent electronics distributors come under increased scrutiny, I am often asked about the changes that I have seen since my



early days in the industry. Generally speaking, the loudest voice against independent distributors comes—as it always has—from the powerful presence of authorized distributors. This segment of the industry views independent distributors as both a threat to their bottom line and an easy target for the scapegoating of the component industry's ills. However, due to the fact that high-quality independent distributors are critical to supply chain-wide counterfeit

mitigation, I think it is pertinent to discuss the things that companies should consider before working with brokers or independent distributors. This advice is especially beneficial when it comes from the perspective of someone with first-hand industry knowledge and experience. Additionally, I wish to add some insight as to what I believe are legitimate criticisms of independent distributors and what are misconceptions that do not represent the whole story.

In order to discuss the industry of independent component distribution, some terms must first be defined. A broker is simply defined as "an agent who negotiates contracts of purchase and sale." This term generally applies to independent distributors who sell parts outside a set arrangement with an original equipment manufacturer (OEM) or an original component manufacturer (OCM). Authorized distributors, on the other hand, have a direct arrangement with a manufacturer, often in the form of a franchise agreement. This distinction is important when it comes to counterfeit mitigation.



IPC 2014 Events

Mark your calendars now for IPC events in 2014! While many of the programs are being finalized, you can sign up today to receive updates on select event news and special promotions as they become available.

SIGN UP FOR EVENT UPDATES

May 6 | Andover, MA May 8 | Santa Clara, CA May 13 | Chandler, AZ May 15 | Schaumburg, IL **Critical and Emerging Product Environmental Requirements Seminar**

September 28–October 2 IPC Fall Standards Development Committee Meetings

co-located with SMTA International Rosemont, IL, USA

May 7–9 **ECWC 2014** Nuremberg, Germany

May 19–22 IPC APEX India[™] Bangalore, India

May 28 | Singapore August 20 | Penang, Malaysia Southeast Asia High Reliability Conferences

June 10–11 IMPACT 2014: IPC on Capitol Hill Washington, D.C., USA October 14–15 IPC Europe High Reliability Forum Düsseldorf, Germany

October 28–30 IPC TechSummit[™] Raleigh, NC

November 18–20 High-Reliability Cleaning and Conformal Coating Conference sponsored by IPC and SMTA Schaumburg, IL, USA

December 3–5 International Printed Circuit and APEX South China Fair

(HKPCA and IPC Show) Shenzhen, China

Questions? Contact IPC registration staff at +1 847-597-2861 or registration@ipc.org.

INDEPENDENT DISTRIBUTOR continues

Regardless of contemporary rhetoric, counterfeit electronics are an epidemic because not enough emphasis is placed on the core of the problem: purchases that are made from other than authorized suppliers. While parts should be purchased from original manufacturers or authorized distribution whenever possible, situations do arise in which this is not possible. In cases that require the purchase of components that are obsolete or on allocation, authorized distribution networks are unable to effectively supply needed parts. While some would advocate a delay in purchasing until parts can be produced by an original manufacturer, the lead times involved make this an impractical option at best. For military applications, excessively long lead times can have serious operational consequences. As the saying goes, "War doesn't wait."

Independent component distributors add value to the electronic components market in numerous ways that authorized distributors cannot. For example, independent distributors possess the ability to move both commercial and government excess throughout the component markets. This allows parts to be found for situations that require parts made under contract, such as sole-source military requirements. Authorized distributors, however, are limited to



Figure 1: Many times, parts are obsolete or on allocation.

supplying products that are still produced by the original manufacturer.

Additionally, independent distributors help to prevent line-down situations by providing needed parts where they cannot be obtained through authorized distributors or OEMs. This occurs frequently when parts are out of production (obsolete) or on allocation.

Like it or not, companies literally buy thousands of obsolete components and materials which are unavailable through authorized distributors. Ultimately, qualified and certified independent distributors provide valuable support to protect your supply chain in the event you are unable to buy parts from authorized distributors.

While independent distributors add value in many ways, many within the component industry view them in a negative light. In some ways, this is quite reasonable—unscrupulous and deceitful firms do exist and have caused purchasers of electronic components many headaches over the years. Outfits that operate with ethics as a secondary consideration will often make statements such as, "I am getting parts from an OEM in Europe," or "The parts are late because they are stuck in customs," or "We never buy parts in China."

While these statements, if true, are totally legitimate explanations of an independent distributor's purchasing process, they can also be used to misrepresent a firm's sourcing practices. The first two statements are sometimes used by unethical firms to make a customer believe that they have the parts requested by the customer in stock, while in fact, they are using these excuses to try and buy time to find the parts. Although there is nothing wrong with an independent distributor needing time to source and ship parts after making it clear to the customer that this is their intent, misleading the customer by claiming that the parts are held in stock when they are not is completely unethical. Regarding the final statement, there are indeed some distributors that do not source parts from companies based in China or other countries known for counterfeiting parts. However, a distributor that says this but does buy from China is blatantly lying to their customers, which is obviously highly unethical.

INDEPENDENT DISTRIBUTOR continues

To avoid doing business with these unscrupulous brokers, here are just a few questions to consider asking:

- How were the parts found?
- Is the company's website using completely stock photos? Does it truly represent the firm?
- Is the picture of the business really their office?
- Are the owners or management clearly identified?
- Are they listing a line card with hundreds of manufactures? If so, are they truly authorized for all those suppliers? If not, why list them?



Figure 2: Many companies misrepresent themselves on websites.

INDEPENDENT DISTRIBUTOR continues

The company's website, as mentioned on this list, is a great tool for aiding in the identification of illegitimate firms. Generally, distributors that prove to be unscrupulous are not very forthright about their business on their website. An unwillingness to accurately identify their office's location, the firm's management team, and which (if any) manufacturers that they are an authorized distributor for are all causes for major concern. While a detailed and accurate website is no guarantee that a firm is legitimate, a shady Internet presence should be looked upon as such, as it usually indicates that the distributor in question does not offer the counterfeit protection and transparency that is needed by today's electronics industry.

When part numbers are searched for on these questionable websites, they are invariably shown as being in stock. After doing business with these companies, however, it becomes clear that they are not masters of supplying electronics, but are rather masters at search engine optimization.

When sent a request for quote, these companies have not looked for the parts at the time that they submit a quote, and in fact do not begin searching until they have received a purchase request. When they can't find the parts, these companies will offer excuse after excuse, until finally abandoning the deal entirely, wasting the buyer's time and ultimately leaving the end customer, often military personnel, without needed components.

An additional factor that should be taken into consideration is the firm's background. For example, are they certified? If so, are the certifications from accredited organizations that utilize third-party audits? Does the firm use terms like "compliant" instead of "certified"? If so, this is an indication that the distributor in question is trying to reap the benefits of association with an accredited certification program without undertaking the work necessary to become certified. An additional consideration is the firm's standing with industry and regulatory bodies: Are they in good standing with organizations such as the ERAI, the Better Business Bureau, and Dun & Bradstreet?

Another idea to consider is whether the company has made a conscious effort to improve their credibility within the industry. For example, have they been able to effectively complete the ARP 6178 Risk Assessment Tool? Also, are they willing and able to answer questions regarding their counterfeit avoidance plan?

Finally, the firm's efforts to ensure that their clients receive quality parts should be investigated. To what degree do they test their product? What is their warranty policy? Will they provide a test report and put in writing the exact quantity that have been tested? Is the test facility itself certified? If the parts fail, will they cover the cost of testing? Do they do the tests themselves? Who trains them in testing protocol? These things should be key considerations when deciding to do business with a distributor.

Ultimately, these are the things that you should look for in an independent supplier:

- Certification—efforts to gain industry credibility
- Transparency—in person and on the internet
- Testing—willingness and ability

Although some independent distributors do not operate in a legitimate fashion, there are many that do. These firms that operate ethically and provide their clients with quality components and service are essential to the modern electronics industry. To separate one category from the other, it is important to know your supplier rather than buy your parts based on random Google searches. Ultimately, trust begins with transparency and testing. **SMT**



Todd Kramer is CEO of Secure Components LLC, an AS6081 & AS9120 certified independent distributor of electronic and mechanical components to the aerospace, defense, and high-

reliability industries. To contact Kramer or to read past columns, <u>click here</u>.



Counterfeit Electronic Parts and Electronic Supply Chain Symposium

JUNE 24 - 26, 2014

Marriott Hotel and Conference Center | College Park, MD

Technical Sessions & Expo – June 24-25

SMTA and CALCE University of Maryland are pleased to announce the 2014 Symposium on Counterfeit Electronic Parts and Electronic Supply Chain. Don't miss this opportunity to learn from and share your insights with experts from government, industry and academia who are addressing the counterfeit problem. This symposium is the best forum in the country for presenting and learning about the latest technology and policy developments in the area of electronics supply chain and counterfeit electronics prevention.

Technical Presentations Given By:

Defense Logistics Agency (DLA), US Navy, CEPREI (China), Rochester Electronics, SMT Corporation, University of Maryland, University of Connecticut, Applied DNA Sciences and many more.

Workshops — June 26

- Inspection Based Counterfeit Detection Methods Bhanu Sood, *CALCE/University of Maryland*, Sultan Lilani, Integra Technologies and Anne Poncheri, *APQ Consulting*
- Part Obsolescence and Supply Chain Management (Including Process Change Notices and Taggants) Peter Sandborn, Ph.D., and Diganta Das, Ph.D., *CALCE/University of Maryland*



Technical Committee

Diganta Das, Ph.D., *CALCE/University of Maryland*, Conference Chair, Diganta@umd.edu Sally Arno, *Plexus Corporation* Bill Cardoso, *Creative Electron* Dennis Fritz, *SAIC, Inc* Erik Jordan, *Nisene Technology* Sultan Ali Lilani, *Integra Technologies* Kevin Sink, *TTI, Inc.* Bhanu Sood, *CALCE/University of Maryland*

Advisory Committee

Daniel DiMase, *Honeywell* Henry Livingstone, *BAE Systems* Mark Snider, *ERAI*



www.smta.org

calce

www.calce.umd.edu

Going beyond anecdotes and examples of counterfeit parts, this symposium focuses on the solutions available and under development by all sectors of the industry.



www.smta.org/counterfeit

Organized by



Dymax's Needle Valve Offers High Dispensing Precision

Dymax Corporation's Model 485 pneumatic, normally closed needle valve is designed to deliver precise dots or very fine beads of low- to high-viscosity fluids.

ECD Celebrates 50 Years of Innovation & Excellence

ECD is celebrating its 50th year of providing innovative products for the electronics manufacturing industry. Best known for its former aqueous cleaning systems and for revolutionizing electronics thermal processes with the development of the M.O.L.E. suite of thermal profiling tools, ECD's rich history includes broad experience in electronics and other industries including baking, industrial, and solar.

Alpha Intros Wave Solder & Rework Lead-free Alloy

New ALPHA SnCX Plus 07 is a lead-free, silver-free alloy developed by Alpha, consisting of tin, copper, and several unique additives designed to enhance alloy performance. It is engineered to be a cost-effective alternative to other lead-free, silver-bearing alloys in terms of overall performance and reliability on standard complexity single and dual-sided electronic assemblies.

UEC Integrated into Arotech's Battery & Power Systems

Robert S. Ehrlich, chairman and CEO, said, "UEC is a highly-complementary business to our Battery and Power Systems Division. The combination opens up many new market opportunities for us. UEC brings us significant electronic engineering and manufacturing skills which combines well with our expertise in military and commercial grade battery technology and management systems."

LPKF Opens Korean Office

LPKF is one of the world's leading providers of laser systems for the production of electronic components. Approximately 70% of the company's sales are generated in Asia. South Korea joins China and Taiwan as one of the Garbsen, Germany-based laser specialist's key markets.

Super Dry Expands: Signs Agreement with CM Group

Moisture specialist and manufacturer of ultra low humidity drying and storage solutions, Super Dry, has announced the appointment of The CM Group to represent their newly-expanded product line in The Pacific Northwest.

Essemtec's Paraquda Nets Award

The company has been awarded a 2014 NPI Award in the category of Component Placement—Multifunction for its multi-functional SMT Center. The award was presented during a ceremony that took place at the Mandalay Bay Convention Center during IPC APEX EXPO.

Mek Launches Direct Operations in the Americas

AOI and SPI designer and manufacturer Marantz Electronics Ltd. (Mek) has announced the opening of direct sales, marketing, and applications engineering operations in the Americas. Headquartered in Nevada, Mek Americas LLC will be directed by industry veteran John Rider.

Super Dry Intros Low-temp Desiccant Storage Cabinets

Moisture specialist Super Dry has launched a new series of desiccant storage solutions. Complementing the company's extensive range of ultra-low humidity desiccant storage cabinets, the XSDC Cooling series features both <1% RH and below ambient temperature control.

Electrolube Signs Distribution Agreement for Spain and Portugal

Electrolube is pleased to announce a new distribution agreement with AB Electronic Devices to represent their conformal coatings range in Spain and Portugal. The new agreement will enable AB Electronic, Electrolube's distributor for the Iberian market, to offer the company's entire product portfolio to the Spanish and Portuguese markets.





Information Technology Industry Council



Critical and Emerging Product Environmental Requirements Seminars

May 6	Philips Healthcare Boston, MA
May 8	Agilent Technologies Santa Clara, CA
May 13	Intel Corporation Phoenix, AZ
May 15	Motorola Solutions Chicago, IL

Don't settle for second-hand information. Trust IPC and ITI to help you ...

- ... Tackle compliance challenges and comprehend the latest environmental product requirements
- ... Stay informed of domestic and global challenges confronting electronics manufacturers
- ... Engage with peers, customers and suppliers in discussions on substance restrictions, eco-labeling, market and consumer pressures and more.

Speakers include key officials with a direct role in the development and implementation of European Union (EU) regulations, as well as experts on sustainability and product environmental trends, and key product-related environmental regulations in the United States and Asia, including California's Safer Products Regulation.

Silver Sponsor

Bronze Sponsor



www.ipc.org/iti-ipc-seminar

SMT TRENDS & TECHNOLOGIES

LED the Sunshine In

by Sjef van Gastel

ASSEMBLÉON NETHERLANDS B.V., VELDHOVEN

After a relatively slow start, LED lamps are now becoming affordable, and domestic LED lighting is about to take off. It is expected that by 2020, more than 65–70% of all lighting will use LED lamps or LED modules. The manufacturing process for LED lamps is based on SMT, and this month's column explains some of manufacturing's special requirements.

To save energy and limit carbon emissions related to lighting energy, the EU has legislated to ban incandescent lamps. Starting in 2009 with 100-watt lamps, all incandescent lamps were phased out of the market by the end of 2012. Customers have three options to replace them: improved efficiency (halogen) incandescent lamps, energy-saving fluorescent lamps, or LEDs (the benefits of LEDs make them clear favorites for most domestic lighting).

In the early days, drop-in replacement LED lamps did not come up to customer expectations. Luminous flux and light color (too cold) were disappointing, and prices were high (up to US\$52 for a 60-watt equivalent). The promised long (50,000 hrs) lifetimes were usually not met. In the past few years, LED technology has made a giant leap forwards, though. Affordable lamps now offer warm white light color, light flux comparable to conventional lamps and good quality (constant lighting properties over time, and long life). LED lamps also offer much better lighting efficiency and controllability (both luminance and color). Finally, the small form factor of LEDs gives the lamp designer new possibilities for elegant design.

The world market for packaged LEDs is expected to grow until 2016, and stabilize between 2017 and 2020 at a revenue level of about \$16 billion (Figure 1). There are two main reasons for this stabilization: market saturation since most incandescent lamps will have been replaced by LED lamps/modules (with a lifetime 10–50 times longer!) and upcoming OLED lighting solutions (offering large area homogenous lighting).



LED THE SUNSHINE IN continues



Figure 1: Packaged LED market by application (source: Yole Développement, September 2013).

Anatomy of a LED lamp

Now let's look at the anatomy of a LED lamp (Figure 2). Most LEDs are driven by a DC constant-current supply (LED driver). Energy efficiency of LEDs is very high (typically 6–8 watts for a LED lamp versus 60 watts for an incandescent lamp with comparable luminosity). However, since the dimensions of a LED package are typically much smaller, local heat dissipation (below the LED package) per unit area will be higher. Special measures are needed to cool the LED board and hence safeguard long LED lamp lifetimes: substrate material selection (insulated metal substrate or FR-4 with thermal vias) and a heat diffuser (connected to both LED board and driver board).

IMS consists of a core of aluminum sheet material covered by circuit layers. In most cases, the circuit material is white to ensure good light reflection. Since IMS material is a factor 8–10x more expensive than FR-4, low-cost consumer appliances more frequently use FR-4. Since



Figure 2: Anatomy of a LED drop-in replacement lamp.

LED THE SUNSHINE IN continues

thermal conductivity of FR-4 is worse than IMS (typical values for FR-4 are 0.3 watts/mK and for IMS are 1–3 watt/mK), special precautions are needed for FR-4 substrates to be used in this tough thermal environment.

These precautions relate to the use of thermal vias in the board. Here, vias are drilled below the footprint of the thermal pad of the LED packages to be mounted. These vias are then filled with copper or thermally conductive paste enabling heat transfer from the LED packages to the heat diffuser that is connected to the bottom of the LED substrate.

Placing LED Packages

Since most LED lamps consist of an array of multiple LEDs, limitations relating to optical and electrical properties of these LEDs apply. For example: Significant differences in flux

or color will be clearly visible to the customer. As a result, such products are rejected and the LED industry has introduced LED product classes. During production, LEDs will vary in color, flux and forward voltage, and this is also true for products from the same batch. The differences are significant and so LED properties are measured and delivered to the market in subclasses or groups called bins. This process of segregating LEDs is called binning.

So a particular bin may contain LEDs, which emit light within a range of wavelengths, a range of flux values and also a range of forward voltages that can be applied safely to the LEDs. If the LEDs aren't properly matched, they will produce a kind of rainbow of different shades of white light on the wall. This problem doesn't exist with an incandescent lamp since it produces a wide range of frequencies. To minimize this potential problem, vendors provide binning charts.

White LEDs are binned for correlated color temperature

(CCT) or by x, y coordinates of the LED in the CIE 1931 chromaticity diagram (Figure 3). The x, y coordinates define the color point of any light source in the CIE diagram. New binning structures for white LEDs consider both CCT and x, y coordinates of the LED whilst binning. This is because even white LEDs with approximately the same CCT can have different color appearances. Each lighting manufacturer has its own recipe (build plan) for LED array manufacturing, indicating binning restrictions for neighboring LED components.

These restrictions translate at the pick-andplace machine to so-called binning software. In the binning software, the remaining parts stock at the pick-and-place machine is compared to the manufacturing batch size. If the remaining parts stock is insufficient, the pick-and-place machine should instantly switch over to a new



Figure 3: CIE 1931 chromaticity diagram; points a–g refer to LED images a (top right) to g (bottom left).

LED THE SUNSHINE IN continues



Figure 4: Anatomy of Philips Rebel HB-LED.

placement program to continue the current production batch. In this new placement program, the LED parts to be mounted will be selected according to part availability at the pick-andplace machine and build plan restrictions.

Finally, special precautions should be taken to prevent LED lens domes from sticking to placement nozzles. Most high brightness LEDs (HB-LEDs) consist of a LED die (emitting blue light) covered by a phosphor layer (producing the desired light color) and a lens on top (Figure 4). This lens focuses the emitted light into a light beam. Most lenses are made of (soft) silicone material which is pretty sticky. Special LED handling nozzles at the pick-and-place machine prevent lens sticking and lens scratching. Usually, special plastic nozzle inlays are used for this.

The End of Incandescent Lights

With the final phase of the incandescent lamps ban now in effect, consumers are looking at alternatives to these energy-gobbling lights. LED lamps, an expensive novelty not too long ago, have come onto the scene in a big way over the last year. While the energy savings of these lamps are a real plus, the real future of lighting lies in smart WiFi-connected lights that allow you to control your home lighting from a smartphone or tablet.

The technology is still in its infancy, but app makers are already developing cool new uses for these lamps. For instance, you can set your lights to come on as you approach your home, and turn off when you leave. Or maybe you want to ditch your alarm clock and program your light to turn on slowly, simulating a sunrise in the morning. In other words, LED the sunshine in. **SMT**



Sjef van Gastel is manager for advanced development at Assembléon Netherlands B.V., where he combines his experience as systems architect and machine designer to explore technical and business

opportunities from emerging technologies. To read past columns, or to contact van Gastel, <u>click here</u>.



News Highlights from S<u>M</u>Tonline this Month

Q1 North American EMS Market Snapshot

More than 370 industry professionals answered the call to I-Connect007's first-ever quarterly market survey. This one-minute survey is designed to provide a snapshot of the current state of the EMS and PCB industries. Based on the results so far, we believe, with your help, we've been able to capture a fairly accurate picture of the current state of the market.

2 Creation Names Mathur New President & CEO

"After an extensive search, our Board of Directors has selected a leader with proven success in our complex industry. I am confident the years to come will be filled with new opportunities under Bhawnesh's leadership," said Geoff Reed, chairman of the Board and one of the company's founders.



In recognition of their significant contributions of time, talent, and ongoing leadership in IPC and the electronics industry, six long-time IPC volunteers were presented with IPC President's Awards at IPC APEX EXPO at Mandalay Bay Convention Center in Las Vegas, Nevada.



The EMS and ODM market was valued at approximately \$363.8 billion in 2013, representing a slight decrease of 0.3% over 2012, mainly due to a significant decline in laptop shipments.

WSI Industries' Sales Growth Continues in 2Q14

Benjamin Rashleger, president and CEO, commented, "Our top line sales growth continued in our fiscal 2014 second quarter as we experienced our second consecutive quarter with sales in excess of \$10 million."



Sparton Acquires Aubrey Group; Expands Medical Portfolio

"We are pleased to announce the acquisition of Aubrey Group, which will add an innovative product development offering to our portfolio, allowing us to provide enhanced services throughout the product lifecycle," stated Cary B. Wood, president and CEO of Sparton.

Michalkiewicz to Chair Top IPC Leadership Committee

Renee Michalkiewicz, MIT, general manager, Trace Laboratories, Baltimore, has been elected chair of the IPC Technical Activities Executive Committee (TAEC) for a two-year term. Michalkiewicz succeeds Douglas Pauls of Rockwell Collins, who held the role for IPC's top standards development oversight committee for the past two years.

8 SMTA Publishes Electronic Assembly Handbook

Chapter topics include soldering and materials, printed wiring boards, components, paste-print stencil, component placement, assembly line design and optimization, solder reflow, wave soldering, dispensing, and inspection and test. Each chapter outlines the fundamental attributes of critical assembly processes providing full-color images and diagrams to illustrate real-world applications.



One of the big challenges for many board designers today is to eliminate or reduce the damage caused by shock and vibration. Whether they're producing cell phones or aerospace boards, engineers want to use the best design and manufacturing processes for attaching ball grid array packages to printed boards.

10 Kimball EMS Earns Award from Future Electronics

On March 19, Kimball Electronics Group was recognized by Future Electronics with the "Global Customer of the Year 2013" Award. The award was presented to Don Charron, president of Kimball Electronics Group, during the Future Electronics world-wide sales conference held in Montreal.



CALENDAR



For the IPC's Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar, click here.

For a complete listing, check out *SMT Magazine's* full events calendar here.

Nordic SI Week 2014 May 5–9, 2014 Stockholm, Sweden

<u>SMT Hybrid Packaging 2014</u> May 6–8, 2014 Nuremberg, Germany

Atlanta 18th Annual Expo May 7, 2014 Duluth, Georgia, USA

International Conference on Soldering and Reliability

May 13–15, 2014 Toronto, Ontario, Canada



Internet of Things May 14–15, 2014 Milwaukee, Wisconsin, USA

Toronto SMTA Expo & Tech Forum May 15, 2014 Toronto, Ontario, Canada

2014 Technology & Standards

Spring Forum May 19–22, 2014 Seattle, Washington, USA

12th Annual MEPTEC MEMS

Technology Symposium May 22, 2014 San Jose, California, USA

IPC Southeast Asia High-Reliability

Conference May 28, 2014 Singapore

RAPID Conference & Exposition

June 9–13, 2014 Detroit, Michigan, USA

IPC SE Asia Workshop on Soldering of Electronics Assemblies

June 9, 2014 Penang, Malaysia

IEEE ICC 2014

June 10–14, 2014 Sydney, Australia

CES Unveiled Warsaw

June 17, 2014 Warsaw, Poland

Upper Midwest Expo & Tech Forum June 18, 2014

Bloomington, Minnesota, USA

<u>CE Week</u> June 23–27, 2014 New York City, New York, USA

Symposium on Counterfeit Electronic Parts and Electronic Supply Chain June 24–26, 2014 College Park, Maryland, USA PUBLISHER: **BARRY MATTIES** barry@iconnect007.com

PUBLISHER: RAY RASMUSSEN (916) 294-7147; ray@iconnect007.com

SALES MANAGER: **BARB HOCKADAY** (916) 608-0660; barb@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE** (916) 266-9160; tobey@iconnect007.com

<u>EDITORIAL:</u> GROUP EDITORIAL DIRECTOR: **RAY RASMUSSEN** (916) 294-7147; ray@iconnect007.com

MANAGING EDITORS: **LISA LUCKE** (209) 304-4011; lisa@iconnect007.com, and **ANDY SHAUGHNESSY** (770) 315-9901; andy@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY** +44 (0) 1455 293333; pete@iconnect007.com EDITORIAL ADVISORY BOARD: BILL COLEMAN, PH.D., Photo Stencil HAPPY HOLDEN, Gentex Corporation CRAIG HUNTER, Vishay DR. JENNIE S. HWANG, H-Technology Group MICHAEL KONRAD, Aqueous Technologies GRAHAM NAISBITT, Gen3 Systems & SMART Group RAY PRASAD, Ray Prasad Consultancy Group STEVE PUDLES, IPC S. MANIAN RAMKUMAR, PH.D., Rochester Institute of Technology ROBERT ROWLAND, RadiSys Corporation DONGKAI SHANGGUAN, PH.D., National Center for Advanced Packaging, China VERN SOLBERG, Independent Technical Consultant GARY TANEL, Electronics Alliance MICHAEL McCUTCHEN, ZESTRON America

MAGAZINE PRODUCTION CREW: PRODUCTION MANAGER: SHELLY STEIN shelly@iconnect007.com MAGAZINE LAYOUT: RON MEOGROSSI AD DESIGN: SHELLY STEIN, MIKE RADOGNA INNOVATIVE TECHNOLOGY: BRYSON MATTIES COVER ART: SHELLY STEIN



SMT® (Surface Mount Technology) is published by BR Publishing, Inc., PO Box 50, Seaside, OR 97138 ©2014 BR Publishing, Inc. does not assume and hereby disclaims any liability to any person for loss or damage caused by errors or omissions in the material contained within this publication, regardless of

whether such errors or omissions are caused accidentally, from negligence or any other cause.

May 2014, Volume 29, Number 5 • SMT© (Surface Mount Technology©) is published monthly, by BR Publishing, Inc.

ADVERTISER INDEX

Blackfox 27
Candor Industries 23
CML-Eurasia 13
Dragon Circuits 9
Eagle Electronics 75
EasyBraid17
EE Technologies 43
H&T Global 79
Hunter Technology 85
I-Connect007 45
Imagineering7
Indium 31
IPC 87, 93

Manncorp 5
Mentor Graphics 59
Miraco Inc 47
NextLevel PCB 3
Nordson Asymtek 53
P Kay Metal 77
Prototron Circuits 51
SMTA 83, 91
Sunstone 1
The PCB List 2
Transition Automation 41
US Circuit 65

Coming Soon to S<u>M</u>T Magazine:

JUNE: Thermal Management

JULY: Tin Whiskers

AUGUST: Assembly of Printed Electronics