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Brittle Failure in Pb-free BGA Solder Joints

by Julie Silk–pg. 14

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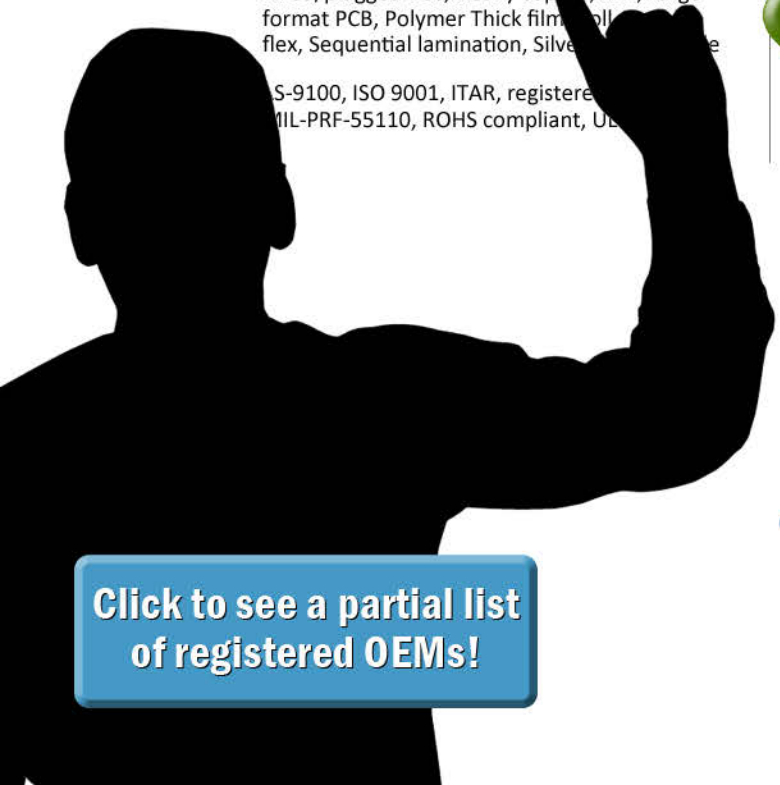

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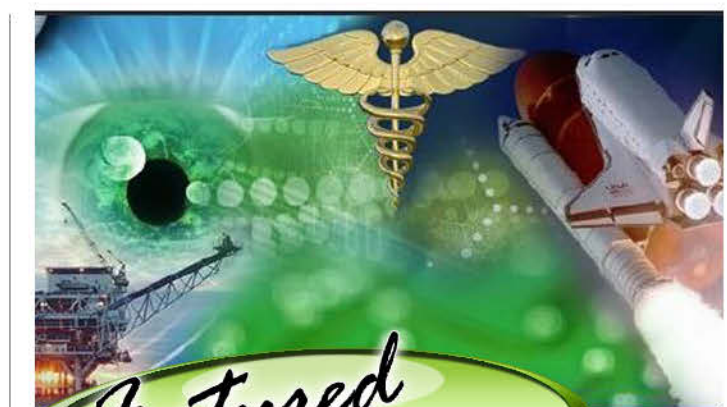

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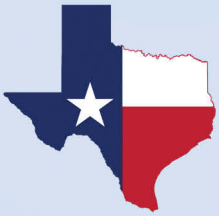

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September 2013 Featured Content

TEST & INSPECTION

Pass the test with SMT! In this issue, we explore the latest and greatest test and inspection processes related to PCB assembly. Our contributors from Agilent, Teradyne, ASSET Intertech and Cincinnati Sub Zero focus on ICT, HALT, HASS, and much more.

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THE WAY I SEE IT

China Stumbles

by Ray Rasmussen
PUBLISHER, I-CONNECT007

The need to see China fail verges on jingoism. Americans distrust the Chinese model, find that its business practices verge on the immoral and illegal, that its reporting and accounting standards are subpar at best and that its system is one of crony capitalism run by crony communists. On Wall Street, the presumption usually seems to be that any Chinese company is a ponzi scheme masquerading as a viable business. In various conversations and debates, I have rarely heard China's economic model mentioned without disdain. Take, as just one example, Gordon Chang in Forbes: "Beijing's technocrats can postpone a reckoning, but they have not repealed the laws of economics. There will be a crash."

The above statement is from a blog by Zachary Karabell, president of River Twice Research and River Twice Capital, a regular commentator on CNBC, and a contributing editor for Newsweek/Daily Beast.

As mentioned in the blog, it's hard to know what's really going on in China. Nobody believes the government's official data, but even the official reports out of China confirm a significant slowdown in economic growth. The official line is now growth of 7.5%, which is a significant change from the 10% average rate of growth the country has experienced over the last two decades. With growth and exports way down, a housing bubble looming, international pressure on currency exchange rates, rising wages and costs, along with environmental pressures, the country is in a deep mess. Of course the official spin makes it sound like things are under control. But that may not be the worst of it. A July 29 article on CNBC.com muses that there is actually no growth, or negative growth, and that the 7.5% Chinese government official number is nonsense.

Robert Barbera, co-director of Johns Hopkins Center for Financial Economics, had the

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CHINA STUMBLES *continues*

following to say about China's economy, as he makes his case that things are much worse than they appear:

"If you take the top 10 trading partners with China and you add up their exports to China, you've got data that the Chinese government doesn't get to put their hands on," he said. "If you look at that data, what you've actually got is about minus 4%, year-over-year."

It would seem that China's in a tough spot.

Quite honestly, a big part of me is happy to see economic difficulties in the PRC. It's payback. And, now that I looked up the word, it's jingoistic as well. China's been riding high for way too long, building their economy on the backs of many small businesses here in the states, Europe, Japan and elsewhere. Tens of thousands of businesses have had to close their doors after Chinese competitors crushed them with artificially low-priced products. The Chinese government's artificial economic environment was so enticing that investment flooded into the country as companies were compelled to move their factories to far-off China just to survive. I think I know why the Chinese did it, but it wasn't fair. Thousands of small business people lost everything. Of course, our government officials allowed all this to happen so they're at fault, too. Enough said. Back to the meltdown.

China's been riding high for way too long, building their economy on the backs of many small businesses here in the states, Europe, Japan and elsewhere. Tens of thousands of businesses have had to close their doors after Chinese competitors crushed them with artificially low-priced products.

Too Big to Fail

I've always liked this aphorism: If you owe the bank $20,000 (or any relatively small amount), you have a problem. If you owe the bank $20 million, they have a problem. The sad part is that in this case, regarding China's difficulties, we, the West, have a problem.

China's rapid ascension to become the second largest economy has put us all in jeopardy. The Chinese economy is integrated economically into just about every other country on the planet. It's an integral partner in the global economic system, which makes them a "too big to fail" partner. We (the West) have created a monster. We allowed China to play in our sandbox while making up its own rules along the way; shame on us for not demanding better controls and transparency. Having said that, we have trouble running our own economies, demanding our own transparency and enforcing our own rules so we really can't have much to say about China and the way the Chinese run things. At this point, our job is to help them even more to ensure they don't collapse and drag the rest of us down with them. Keep this in mind: The West sells a lot of equipment and systems into the PRC. A collapse or significant slowdown in the Chinese economy will have a dramatic effect on our industries. The good news is that we sell to the entire world, so problems in China won't kill our industries, but a China meltdown (which many claim is already underway) will ripple around the planet, weakening the fragile, global recovery.

I feel for China. Not the government, but the people. We all may want the Chinese government to take a few lumps for their dastardly deeds over the last decade or two, but they do have some ground to make up after their more than 50 years of communism. When we have problems in the West, people struggle financially, and we might see a few demonstrations and such, but with China, if they let things get out of hand, hundreds of millions of lives will be at stake. Their issues are potentially catastrophic. A structural collapse in China will cost millions of lives and set things back in that part of the world 10–20 years, which will affect all of us.

Here's another statement from Zachary Karabell's blog:

"The consequences of a Chinese collapse, however, would be severe for the United States and for the world. There could be no major

Chinese contraction without a concomitant contraction in the United States."

You should read the blog entry The U.S. can't afford a Chinese economic collapse. Basically, he says that we may not like the idea of helping China out of this mess, but we have to. It's now in our best interest.

It's been my experience over the years that everything eventually comes back into balance. China will find its rightful place in the world economy; it will come into balance. It would seem as if that process is fully underway.

If you want to read more about the difficulties facing China, I've added a few links to some interesting articles. Enjoy!

China's Economy stumbles in May, growth seen sliding in Q2

More Signs China's Economy Is in Trouble

Will China's economy crash?

China's environment: an economic death sentence

Will China's Slowdown Hurt the U.S. Economy? **SMT**

Ray Rasmussen is the publisher and chief editor for I-Connect007 Publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuiTree Magazine.* To read past columns, or to contact Rasmussen, click here.

EYESHOTS: The Future of Robotic Technology

Replicating human behaviour in robots has long been a central objective of scientists working in the field of information and communication technologies (ICT).

However, a major obstacle towards accomplishing this has been controlling the interaction between movement and vision.

Tackling this issue was the main aim of an EU-funded project by the Universita Degli Studi de Genova in Italy, "Heterogeneous 3D perception Across Visual Fragments (EYESHOTS)." By simulating human learning mechanisms, the project successfully built a prototype robot capable of achieving awareness of its surroundings and using its memory to reach smoothly for objects.

The implications of this breakthrough range from potential improvements in robotic mechanics to achieve better diagnoses and rehabilitation techniques for degenerative disorders such as Parkinson's disease.

The project first examined human and animal biology. A multi-disciplinary team involving experts in robotics, neuroscience, engineering, and psychology built computer models based on neural coordination in monkeys.

The key was recognising that human eyes move so quickly that the images produced are in fact blurred, and the brain pieces together these blurred fragments to present a more coherent image of our surroundings.

Using this neural information, the project built a unique computer model that combined visual images with movements of both eyes and arms, similar to what occurs in the human cerebral cortex.

The project, completed in 2011, was built on the premise that being fully aware of the visual space around you can only be achieved through actively exploring it—by looking around, reaching out and grabbing things.

Through the application of neuroscience, the EYESHOTS project successfully identified a means of giving robots a sense of sight similar to human vision. This represents an important milestone in creating a humanoid robot that can interact with its environment and perform tasks without supervision.

SMT PERSPECTIVES & PROSPECTS

Tin Whiskers: Phenomena and Observations

by Dr. Jennie S. Hwang
CEO, H-TECHNOLOGIES GROUP

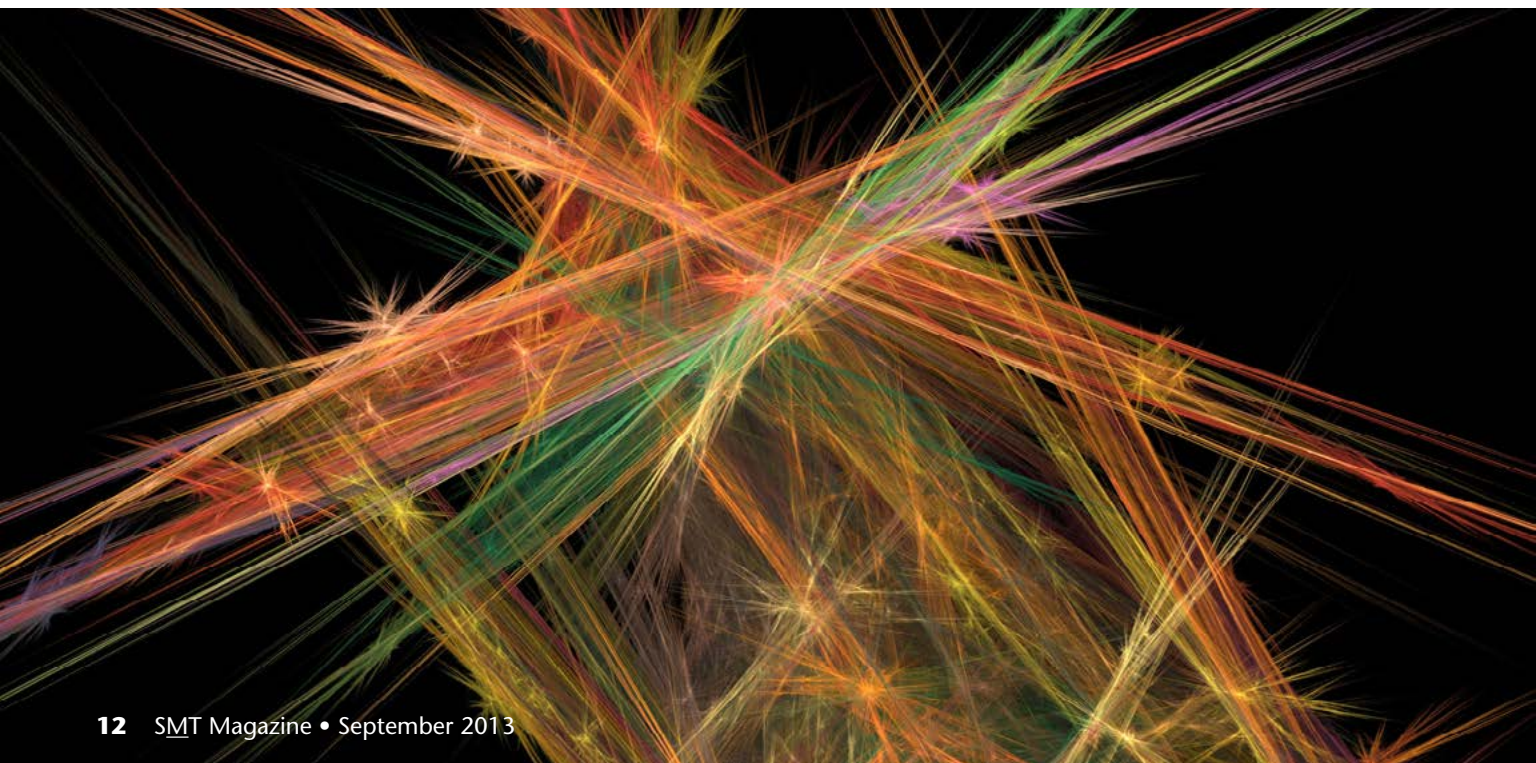
The first in this series on tin whiskers, Tin Whiskers – Clarity First (*SMT Magazine,* May 2013), has set the stage for subsequent topics in this series, including this month's focus, along with these upcoming titles: Tin Whiskers—Potential Impact and Concerns; Tin Whiskers—Contributing Factors; Tin Whiskers—Plausible Theory; Tin Whiskers—Impact of Testing Conditions; and lastly, Tin Whiskers—Preventive and Mitigating Measures.

The metal whisker phenomenon was discovered in the late 1940s. Telephone companies reported that telephone line failures caused by electric short were traced to those fibrous hairy whiskers. These whiskers were found to have grown from the tin plating on capacitor plates, which perhaps was one of the first formal reports on tin whiskers.

Tin whisker reflects its coined name. It has long been recognized to be associated with electroplated tin coating and most likely occurs with pure tin. Its appearance resembles whiskers. However, whiskers can also form in a wide range of shapes and sizes, such as fibrous filament-like spiral, nodule, column and mound. Tin whiskers are often single crystals and electrically conductive. They are normally brittle in nature but can be rendered ductile when very long and thin.

The whiskers, having a crystalline structure, "sometimes" grow up to a few mm long, but usually less than 50 µm with a few microns in diameter. They "sometimes" grow from surfaces where tin (especially electroplated tin) is used as a final finish. In this context, "sometimes" is a tricky word, but bears substantive significance, meaning it does not always follow a consistent pattern phenomenally and is seemingly elusive.

Whiskers may grow, but they may also be self-annihilating as the electric current can fuse the whisker if the current is sufficient. The annihilation ability varies with the whisker's size in length and diameter (e.g., typically more than 50 mil-



liamps is often required). This self-annihilating occurrence further contributes to the observed inconsistent or mythical nature of the events.

What are the driving forces that initiate the formation of whiskers? Can these driving forces be controlled practically and economically? These are million-dollar questions and deserve a careful treatment.

Before we delve into these critical questions, let's look at various findings. One experiment indicated that whiskers can be eliminated by controlling the plating process in an equivalent way to controlling stresses in materials. The very sharp decrease in internal stress of tin electrodeposits was observed after plating as quickly as within minutes. It is interesting to note that this fast stress release occurs regardless of whether initial stress in the deposit is compressive or tensile. In either compressive or tensile case, the value of stress drops to a very low number, but it remains as the same type as the initial stress form (i.e., high initial tensile stress reduces to much lower stress value, but remains tensile, and high compressive stress remains compressive).

It has been observed that the inclusion of organic elements in the tin structure promote tin growth. Organic inclusion or the level of inclusion is in turn affected by the plating chemistry. And the bright tin has exhibited to be most susceptible to whisker formation. Bright tin plating chemistry is prone to creating an environment that creates greater organic inclusion and higher stress level in tin crystal structure.

When comparing between Cu substrate and Ni substrate, Ni substrate tends to retard whisker formation. This phenomenon related to inter-diffusion rate and intermetallic formation correlates well with the relative diffusion rates between Cu and Sn vs. Ni and Sn. Cu has a higher diffusion rate into tin than the tin into Cu. As a result, tin lattice is distorted and the tin lattice spacing is altered, which generates stresses to the tin plating layer.

Another observation showed that the external forces exerted to tin plating, such as bending, stretching, torque, scratches, and nicks could provide additional driving forces at the local regions that exacerbate whisker growth in that stressed region.

Still another experiment exhibited that whisker formation involved a "shelf" time. However, the shelf time varies without a straightforward correlation with temperature, humidity and other environmental conditions. Data showed that a moderately warm temperature served as the "green house" that nurtured whiskering, yet the temperature above 150°C inhibited whisker formation.

Furthermore, highly disparate whisker growth rates have been reported, ranging from 0.03 to 9 mm/year. And whiskers can grow even in a vacuum environment.

So what are the driving forces and root causes?

At first glance, observations and data obtained over the decades are versatile and disparate. But as an aggregate, two points are clear: The driving forces are stress-related, and the internal stress (compressive or tensile) plays an important role to both whisker formation and growth. Various tests were performed under temperature cycling and electric field. The lack of harmonious testing results regarding the effects of temperature cycling and electric field on whisker growth suggests the intricate nature of the internal stresses engaged in the process.

Despite the fact that the test results are at variation with the observations, the internal stress is deemed primarily responsible for the metal whisker formation and growth. As such, the factors that can contribute to internal stress at the tin plating and the conditions that impart additional residual stress to the plating layer during and after plating deposition are the right places to be deliberated. **SMT**

Dr. Jennie Hwang is CEO of H-Technology Group and a pioneer and long-standing contributor to SMT manufacturing since its inception. She is the author of 350+ publications and several textbooks, and an international speaker and author on trade, business, education, and social issues. To read past columns or contact Dr. Hwang, click here, or phone (216) 577-3284.

Brittle Failure in Pb-free BGA Solder Joints

by Julie Silk
AGILENT TECHNOLOGIES

SUMMARY: The increasing complexity of electronic assemblies, coupled with the transition to higher-temperature Pb-free soldering, has given rise to another case of brittle interfacial failures induced by double reflow. This article describes and characterizes electrically intermittent, brittle interfacial solder joint failures in a Pb-free BGA subjected to two reflow cycles.

Abstract

Assembly defects can effectively shorten reliability lifetimes in addition to lowering manufacturing yields or creating premature service failures. This article describes and characterizes an unusual open circuit failure mechanism in Pb-free ball grid array (BGA) solder joints. The failure occurred during Pb-free solder assembly of a 31 mm, 1.27 mm pitch, perimeter array, SAC305 (Sn3.0Ag0.5Cu) BGA. Due to design constraints, it was necessary to assemble some BGA components during the first reflow cycle. Following the second reflow operation, some solder joint opens were detected on the BGA component which had been subjected to the atypical second reflow exposure. Metallographic cross-sectional analysis indicated that the open solder joints initially were well-formed but the failure resulted from a brittle interfacial fracture at the package side of the solder joints. The failure mechanism and possible root cause is discussed in terms of the combined impact of stress induced by component and board warpage and the lower inherent strength of the solder joint near the melting and solidification temperatures.

Introduction

The electronics industry continues to identify and uncover potential performance and reliability risks associated with the transition to Pb-free design and manufacturing. This is a particular concern for complex product designs requiring high reliability and extended service life. The continued integration of printed cir-

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cuit board assemblies (PCBA) using more complex packages, smaller solder joints, diminishing pitch and complex components mounted on both sides of the PCBA has resulted in increasing yield and reliability challenges. Among those issues is the emergence of solder defects that appear to be related to higher assembly temperatures due to the use of Pb-free solders. These assembly defects can effectively shorten reliability lifetimes in addition to lowering manufacturing yields or creating premature service failures.

In the mid-1990s, there were published reports of brittle interface failures of surface mount solder joints that had been subjected to a second soldering operation. The first reported case occurred subsequent to a wave soldering operation[1] but there was another case reported subsequent to a second surface mount reflow operation[2]. Because brittle interfacial solder joint failures were observed during a second reflow soldering operation they were called "double reflow" failures. There have been no additional published cases of double reflow failures since those early occurrences. However, the increasing complexity of electronic assemblies coupled with the transition to higher temperature Pb-free soldering has given rise to another case of brittle interfacial failures induced by double reflow.

This article describes and characterizes electrically intermittent, brittle interfacial solder joint failures in a Pb-free BGA subjected to two reflow cycles. The failed BGA is a 1.27 mm pitch, perimeter array with a body size of 31 mm and SAC305 (Sn3.0Ag0.5Cu) solder balls. Due to the presence of several surface mounted daughter card modules on the non-BGA side of the board, the BGA-side of the printed circuit assembly was soldered first. In effect, this constraint put the BGA components atypically on the bottom-side during the second reflow. The solder joint failures were characterized with metallographic cross-sectional analysis using optical microscopy and scanning electron microscopy. The failure mechanism and possible root cause are discussed in terms of the combined impact of stress induced by component and board warpage and the lower inherent strength of the solder joint near the melting and solidification temperatures. The primary objective of this work is to document this new case of double reflow failure to enable a heightened awareness of the failure mode. These assembly defects are difficult to detect and shorten reliability lifetimes in addition to lowering manufacturing yields and creating premature service failures. This also emphasizes the importance of reviewing and checking the assembly qual-

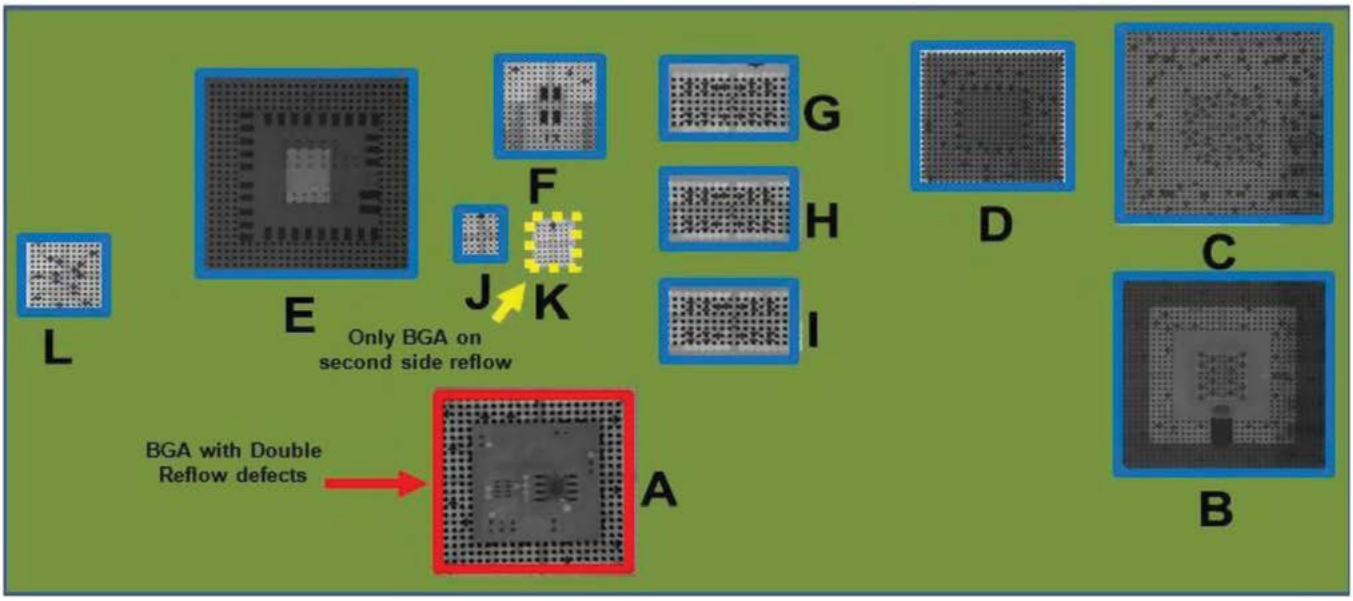

Figure 1: PCBA BGA component descriptions, locations and reflow process.

ity and reliability of assemblies before shipping product.

Assembly and Manufacturing Details

Figure 1 shows the layout of the printed circuit board assembly (PCBA) that contained the soldering defects. Table 1 provides detailed component descriptions for all the area array devices assembled onto the PCBA. All the BGA components with the exception of Component K were subjected to two reflow cycles. Due to the properties of the PCB, soldering was done using two vapor phase reflow cycles, instead of the more typical hot air convection reflow cycles. Following the second reflow, the assembly exhibited parametric failures at test. The parametric failures were traced to the plastic ball grid array component (PBGA) labeled Component A and designated by the red box in Figure 1. Component A, which is a perimeter array BGA, 31 mm^2, 304 I/O solder balls of 1.27 mm pitch and 0.76 mm diameter, exhibited intermittent solder joint electrical opens. There were no indications of solder joint electrical opens on any of the other components on the PCBA.

A preliminary failure analysis of Component A at the factory suggested poor adhesion of the ball to the substrate, with possible inner row solder ball separation at the component side. The root cause was suggested as solder ball "de-wetting," rather than solder joint fracture. Additional failed PCBAs were analyzed using transmission X-ray, dye and pry testing, and metallographic cross sectioning. Warpage measurements of the component and PCBA were done using thermal shadow Moiré[3]. Additional metallographic analyses were conducted to determine the failure mode.

Failure Analysis: Background and Methodology

Solder joint quality inspections inherently are difficult to perform on BGA components and the detection and characterization of intermittent defects using nondestructive test (NDT) methods is even more problematical. Correlat-

Component Designator	Body Size (mm)	Package type	Ball Count (I/O)	Pitch (mm)	Ball Count (I/O)	Pitch (mm)	Ball Diameter (mm)
A	31 x 31	Perimeter PBGA	304	1.27	304	1.27	0.76
B	31 x 31	Full array BGA	964	1.27	964	1.27	0.76
C	27 x 27	Full array FCBGA	676	1.0	676	1.0	0.60
D	25 x 25	Full array TEBGA	576	1.0	576	1.0	0.65
E	31 x 31	Perimeter TBGA	352	1.27	352	1.27	0.75
F	15 x 17	Full array PBGA	256	1.0	256	1.0	0.50
G, H, I	12 x 9	Full array PBGA	119	1.27	119	1.27	0.75
J, K	8 x 11	Full array PBGA	64	0.8	64	0.8	0.62
L	13 x 13	Full array PBGA	144	1.0	144	1.0	0.60

Table 1: Detailed BGA component descriptions for PCBA shown in Figure 1.

ing electrical parametric test data to failed interconnection locations likewise can be difficult with complicated product designs. These factors make physical failure analysis challenging, particularly when the analysis is restricted to small sample sizes or unique product samples. The protocol used in this analysis was to perform all the typical NDT inspections regardless of the expected outcomes prior to initiating destructive analysis.

There are a number of distinct BGA solder assembly defects that can appear symptomatically as intermittent electrical failures. Intermittent failure modes occur at either the package or board side of solder joints and they include different types of brittle interfacial fractures, variations of head-on-pillow (HoP), non-wet opens, inadequate solderability (poor joint formation), microvoid-assisted fractures, and de-wetting. All of these failure modes are caused by some type of physical or metallurgical anomaly in the soldering process or soldered structure that interacts with a sufficient applied stress to cause defect initiation and ultimately failure of the interconnection.

The preliminary electrical test data at the contract manufacturer site indicted Component A as the single failed device on the PCBA. The test data indicated the possibility of multiple failure locations along the inner rows of the BGA. However, definitive identification of failed sites could not be made solely on the basis of the electrical test data.

Defect Detection

Because the suspect failure locations were not in the outer rows, defect detection by visual and low magnification optical inspections was unsuccessful. Transmission X-ray inspection also was unable to detect or image failed solder joints. This is expected since conventional transmission X-ray cannot resolve fine cracking or thin planar defects that are nothing more than air gaps in the soldered structure. Consequently, destructive analyses were initiated starting with the "dye and pry" (DnP) method. The primary objective of the DnP was to determine if the solder joint had failed at the package or PCB side of the joint. Dye intrusion occurred at multiple solder joint sites and dye penetration was observed at the component side of all failed solder balls. A typical image of a DnP surface is shown in Figure 2. It was also noted that incomplete dye penetration was observed at some locations. This is indicative of either incomplete initial solder joint formation or subsequent cracking through only a fraction of the intended attachment area.

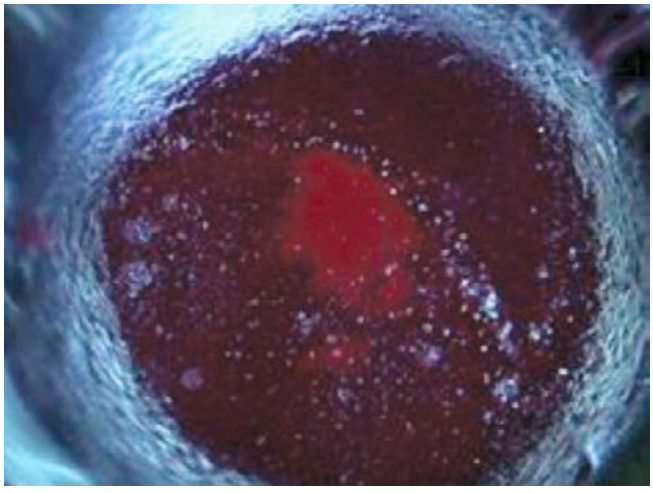

Figure 2: Optical photomacrograph of a failed solder ball surface after dye and pry (DnP) testing. This surface has fractured between the solder ball and BGA package pad (at the component side). The red color on the surface is from the dye intrusion that occurs prior to the mechanical prying.

Figure 3 shows the a composite map of failure locations taken from three different Component A samples overlaid on a low magnification transmission X-ray micrograph of the package ball pattern. The pattern of indicted sites is asymmetric within the package array and is concentrated in proximity to the inner row of perimeter ball array. This inner row failure signature is atypical for many of the intermittent failure modes discussed in the previous section. Those types of failures tend to manifest in the outer rows at the corner and near-corner locations that are known to be the highest stress-strain locations in BGA packages. However, exceptions to this trend can be found in PBGA packages that exhibit certain specific warpage signatures. It is common for warpage stresses to be high at the corner sites, but they also can be high in the die shadow region due to the

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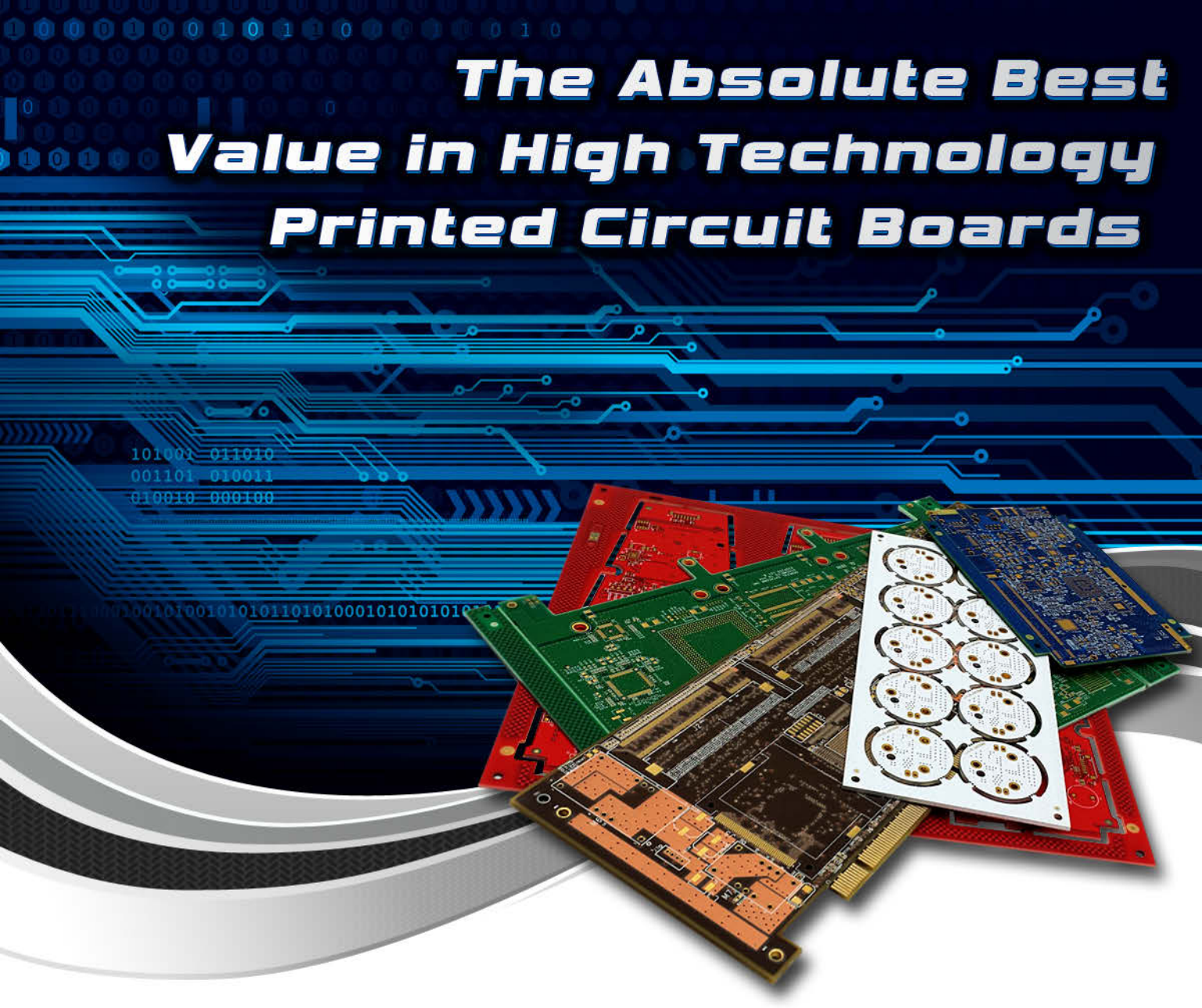

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high CTE mismatch between the package laminate and the silicon die. Asymmetric failure patterns (Figure 3) are not common but when they occur they are believed to result from mechanically or thermally unbalanced structures in either the PCB or the package that affect CTE and thermal transfer.

This map is a composite of failures for Component A taken from three different PCBAs.

Additional optical and SEM micrographs of failed solder joints at the component side are shown in Figures 4 and 5. These failures initially were diagnosed as ball de-wet or ball drop, pointing to the assembly process as the root cause.

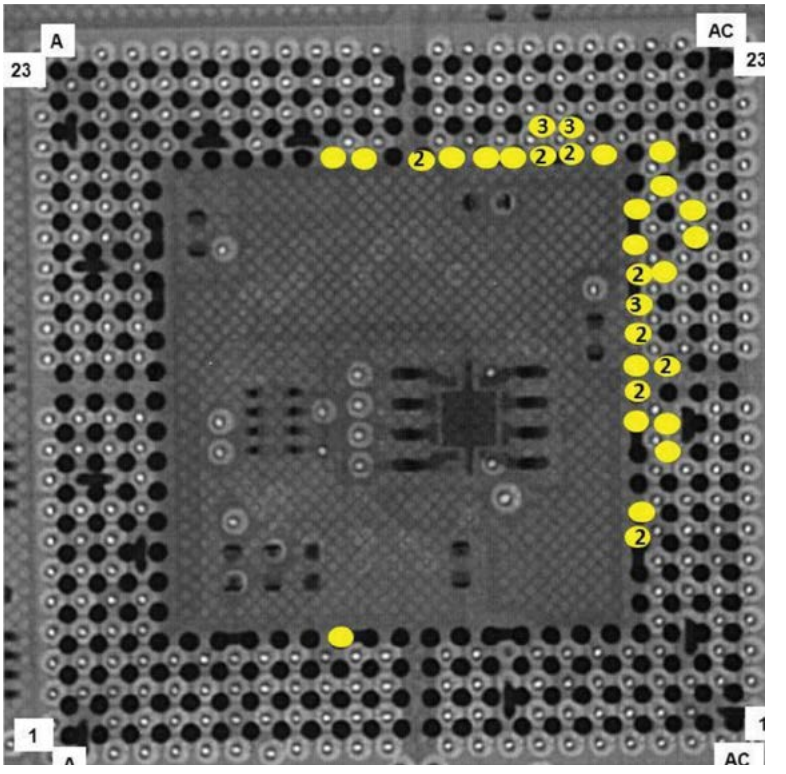

Figure 3: Failure location map from dye and pry test data overlaid on a transmission X-ray image of BGA Component A.

Destructive Cross-Sectional Analysis

Destructive cross-sectional metallographic analysis was performed to provide more detailed and conclusive failure mode data. The analysis was conducted on Component A from a PCBA sample that contained suspected solder joint

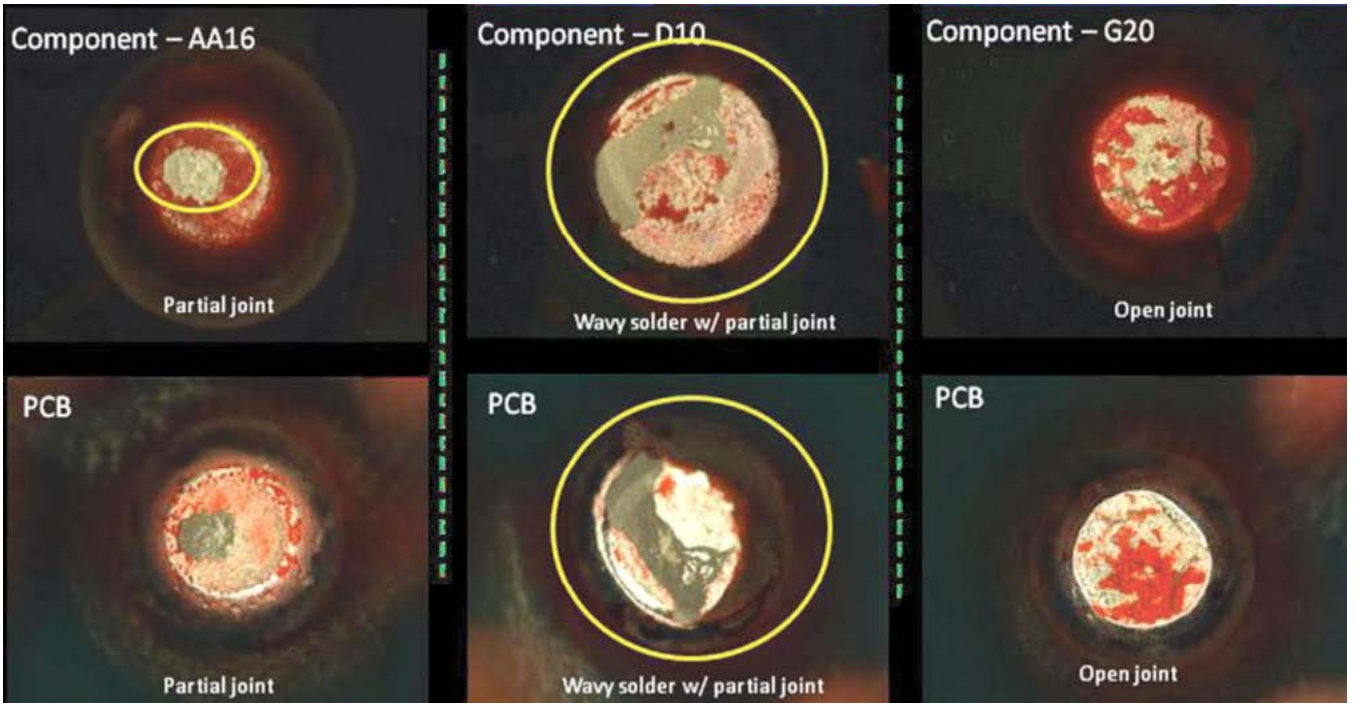

Figure 4: Optical photomacrographs of various fracture surfaces after DnP testing.

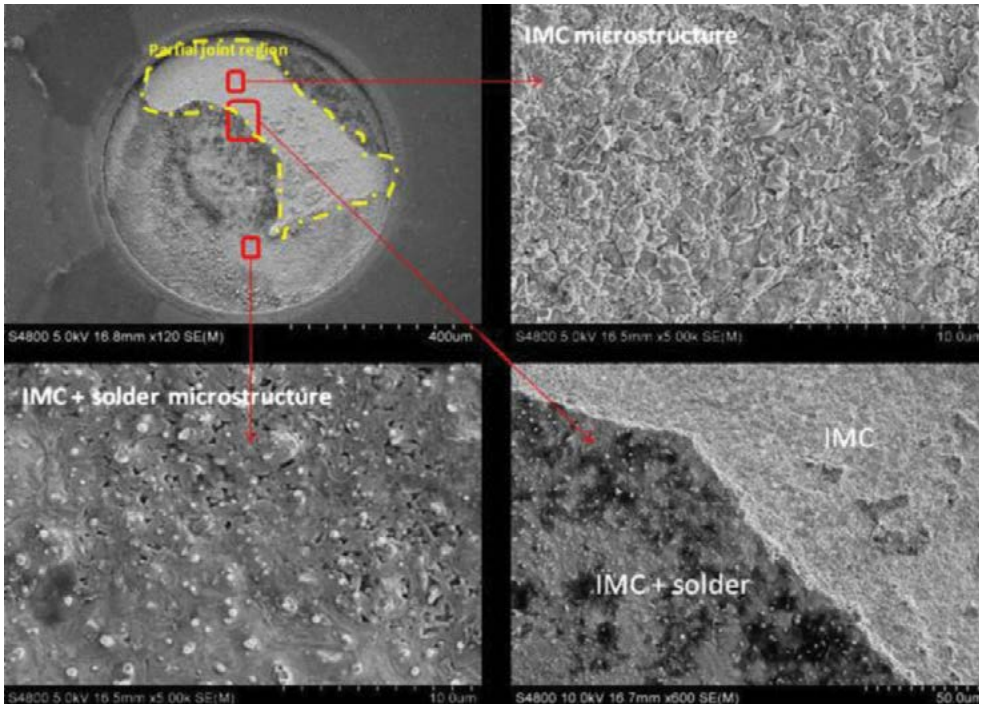

Figure 5: SEM micrographs of various fracture surfaces after DnP testing.

opens. The component was cross sectioned with row-by-row analysis and optical photomicrographs were obtained for multiple solder balls in each row. The photomicrographs in Figure 6 show cross sections of multiple solder balls across row 20 in Component A. Row 20 is one of the inner rows of the "picture frame" of the BGA package pin diagram. The solder joint at pin location T20 does not appear to be formed properly and this is confirmed in the higher magnification image in Figure 7.

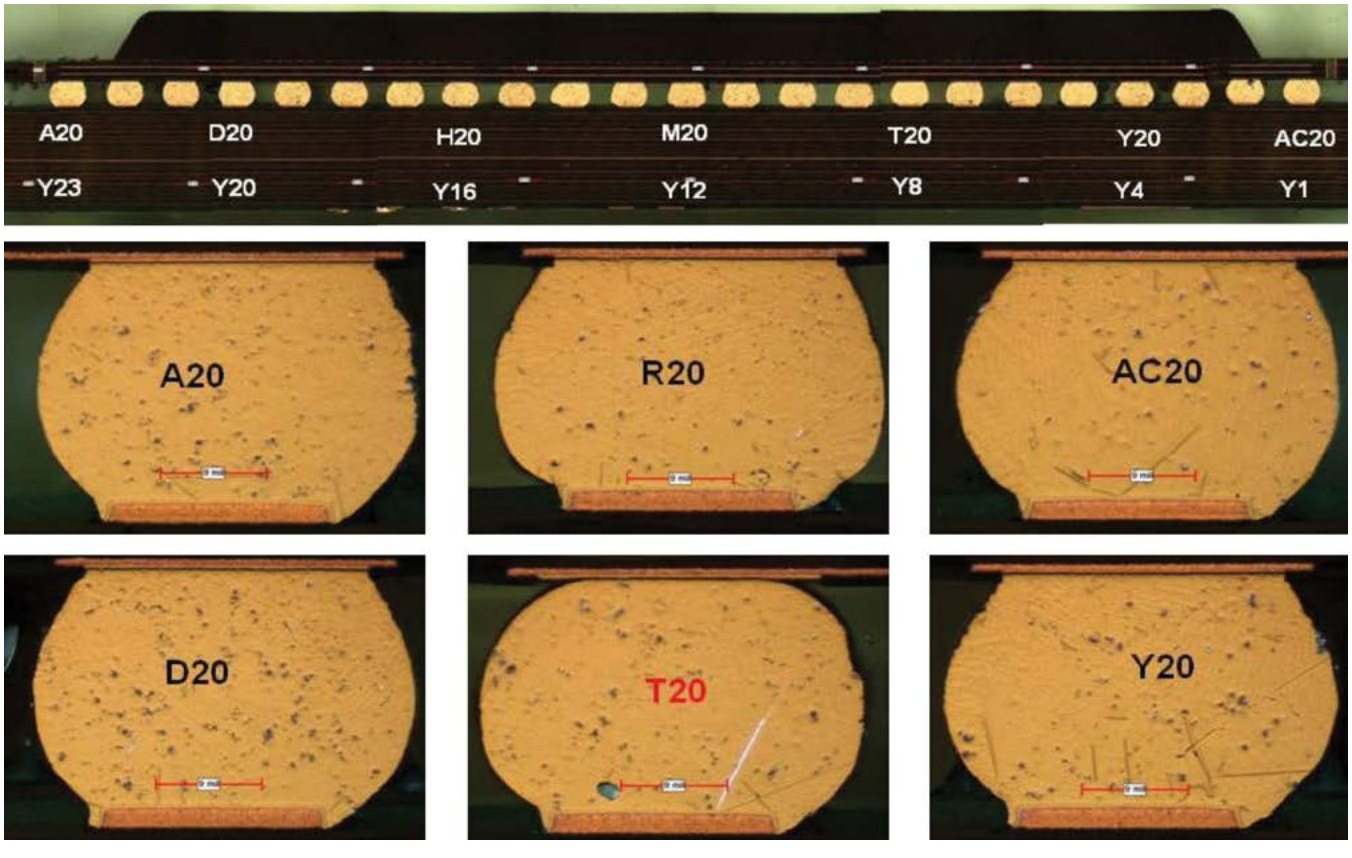

Figure 6: Multiple metallographic cross sections of solder balls in row 20 of Component A.

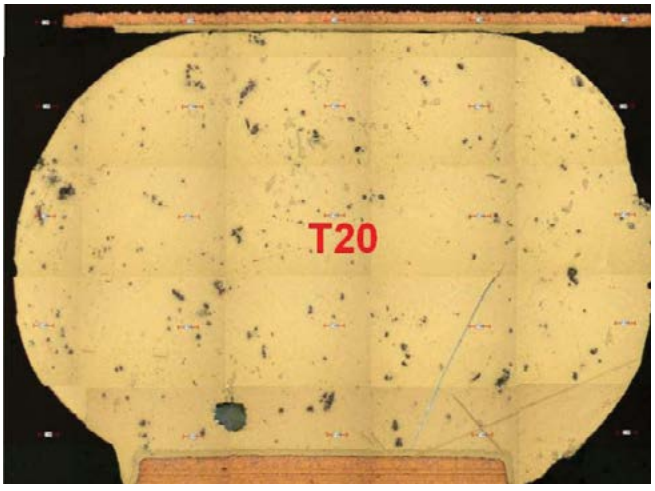

Figure 7: A higher magnification photomicrograph (initial magnification 500X) showing a defect that appears to be de-wetting at package location T20 in Component A. The ball seems to be detached from the package pad.

The initial indication from the high magnification photomicrograph in Figure 7 is that the T20 ball was never soldered to the BGA pad. At this low magnification, the solder ball appears to be de-wetted from the pad. However, an even higher magnification photomicrograph presented in Figure 8 shows that the T20 solder joint actually separated from the BGA pad at the interface between the Ni-Sn intermetallic compound (IMC) and the bulk solder. The presence of an IMC layer and a relatively small amount of solder on the PBGA pad confirm the solder ball had been previously attached to the pad. The spherical curved surface of the bulk solder at the perimeter of the solder ball also indicates melting. By all indications, the soldering reaction was successful initially and the solder joint was formed properly. In contrast, the top of the solder ball is flat and parallel to the component pad indicating that a brittle solder

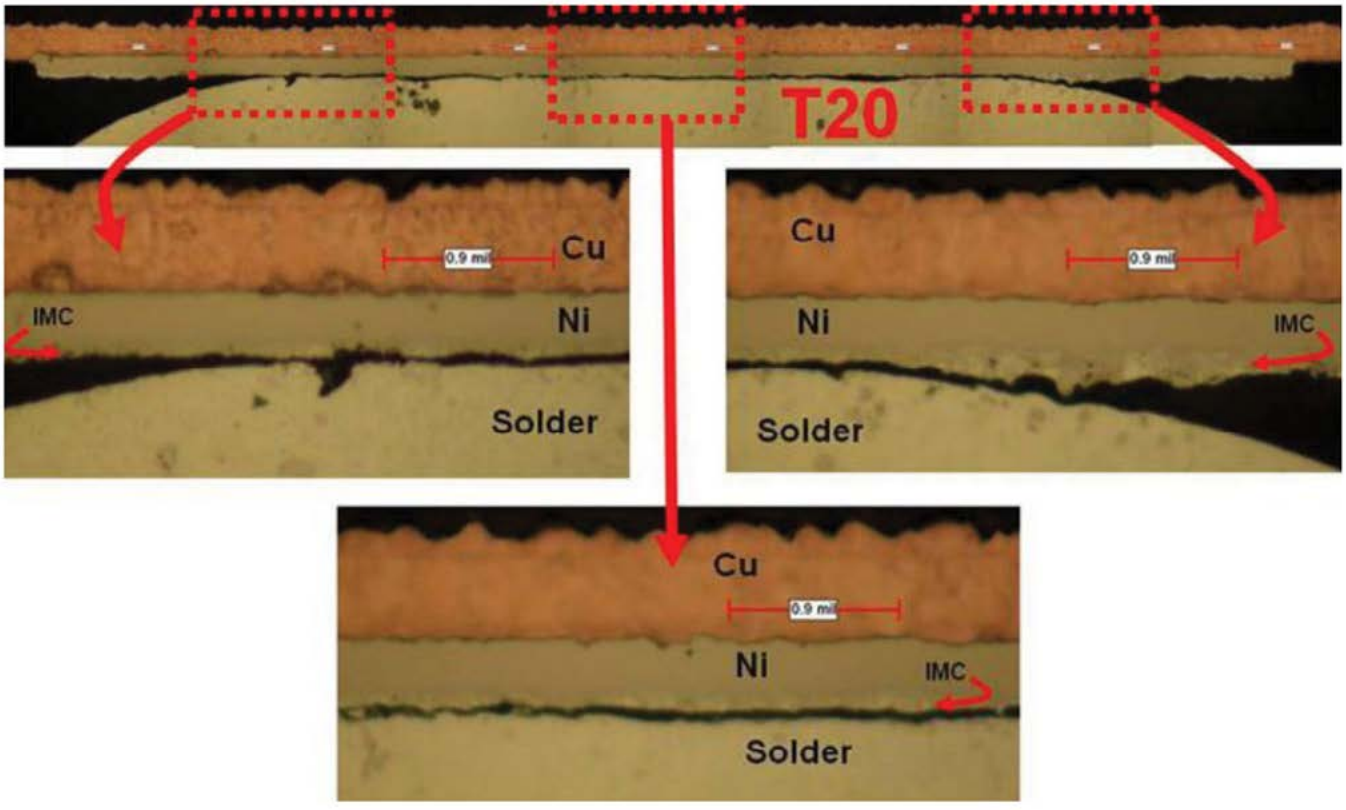

Figure 8: Higher magnification photomicrographs (initial magnification 1000X) adjacent to the T20 BGA pad area showing evidence of a prior successful soldering reaction on the BGA pad with subsequent fracture at the interface between the IMC layer and the bulk solder.

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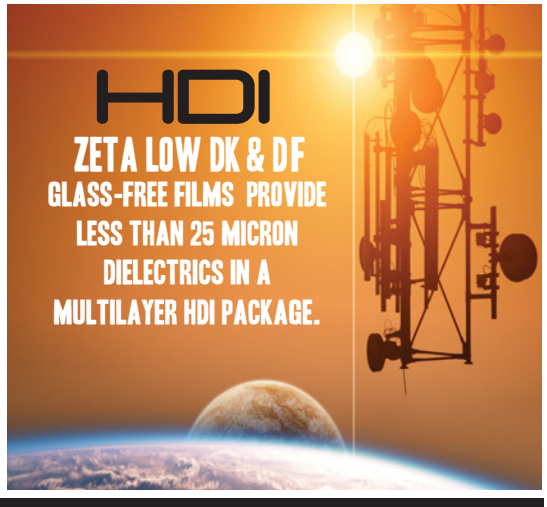

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joint fracture occurred. This failure signature is consistent with that reported in the double reflow references[1, 2] and it is suggested that a similar failure mechanism can account for the T20 solder joint failure. As the solder joint temperature increased and approached the melting temperature during the second reflow, mechanical stress in the PCBA structure was sufficient to induce a brittle fracture at the IMC interface just prior to reaching the melting temperature. The source of the stress could be a combination of CTE mismatch in the package as well as PCB and component warpage. The subsequent melting of the solder ball moments later in the reflow process accounts for curved surface of the solder ball and de-wetted appearance at lower magnification.

To draw a distinction between the de-wet and brittle fracture modes, the solder joint separation surfaces (interfaces) must be analyzed carefully. In addition to the total separation shown in the T20 solder joint, the three adjacent balls P20, R20 and U20 shown in Figure 9 exhibit similar but partial separation of the solder ball from the Ni-Sn IMC. At first glance, the separations marked by the dashed yellow lines in Figure 9 look like the solder joint de-wetting failures. However the separated areas marked by the dashed red lines in Figure 9, show clear indications of cracking or fracturing rather than de-wetting.

It is assumed that once Component A was attached to the PCBA during the first reflow process there was a good physical and metallurgical connection of solder balls to the PCB and package bond pads. During the subsequent second side reflow operation, the solder joints previously formed on Component A are sub-

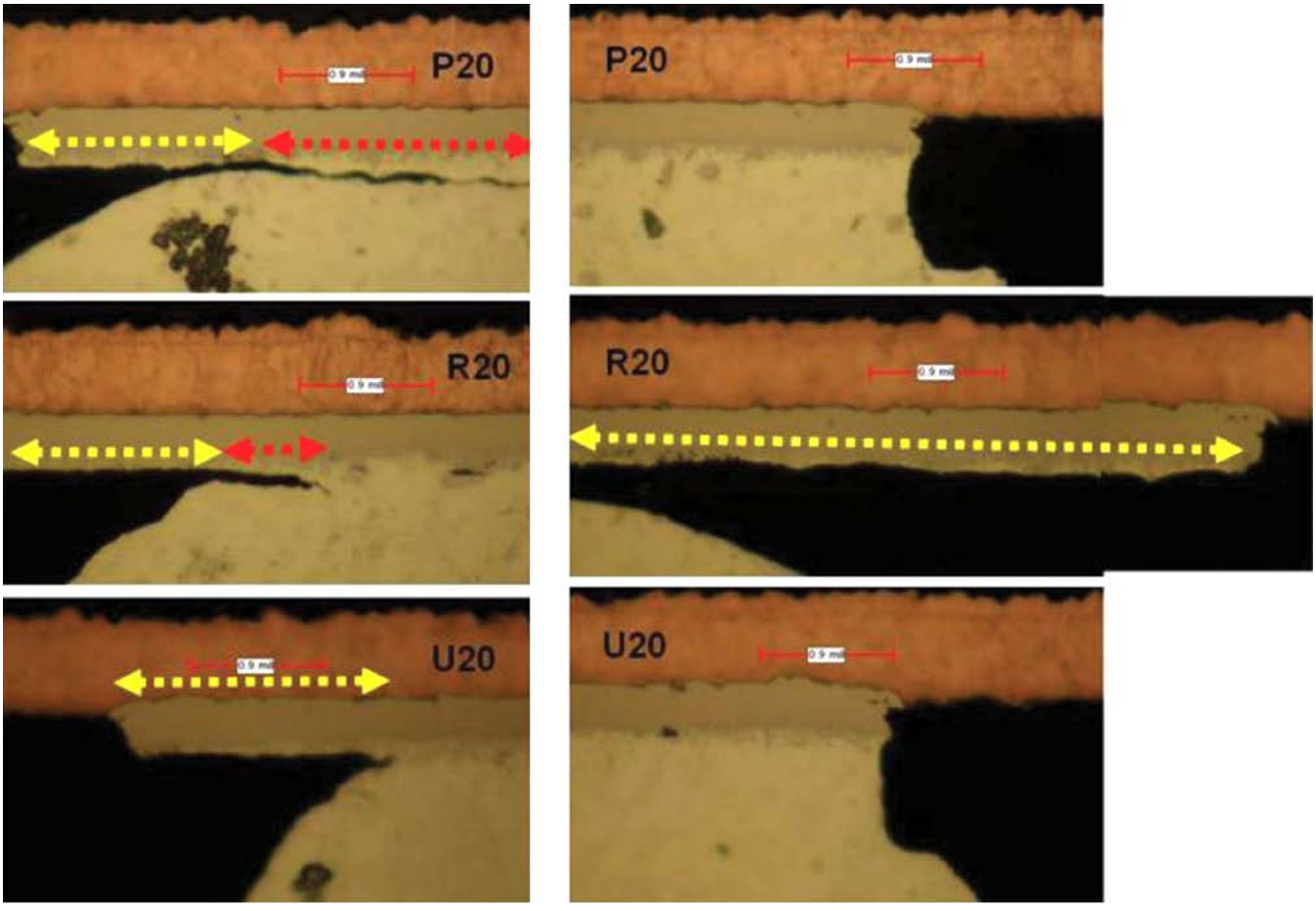

Figure 9: Magnified cross section, 1000X, of PCBA, Component A, solder balls P-20, R-20, and U-20.

jected to an increasing thermal stress signature. It is reasonable to expect the mechanical strength of those solder joint interconnections to decrease as the temperature increases. Concurrently, stress and strain are induced in the solder joints due to the mismatch in coefficient of thermal expansion (CTE) between the composite structures of Component A and the PCB laminate. The stress in the joints could be exacerbated by any warpage in either the component or the PCB. If these stresses exceed the tensile strength of the solder joint, fracture will occur along the weakest interface. At higher temperatures near-reflow, the weakest link typically is the IMC/solder interface as indicated in Figure 8. Based on those cross sections, it is reasonable to conclude that fracture results from the increasing stress on the component solder joints during the second reflow process due to a combination of CTE mismatch and the component and PCB warpage.

There are two possible scenarios to consider. In the first scenario, the solder joint could be fracturing during the reflow ramp up. This could be happening at any point before the solder begins to melt. Stress of course cannot be transferred to the IMC interface once the solder has melted. Although vapor phase reflow is rapid and provides more uniform heating than forced convection IR reflow, temperature gradients will exist across components. Solder joints in the outer rows of the perimeter array are expected to reach the solder melting point a finite time before the inner rows. The differential melting may generate additional local stresses that could add to the any global stresses generated by differences in component and PCB CTE and warpage. Once the balls on the perimeter of the package melt, all the stress in the package is transferred to inner unmelted balls, which could result in fracture at those sites.

In the second scenario, the solder joint could be fracturing during the reflow ramp down. It is important to recognize that stress cannot be transferred to the IMC interface as the solder ball remains molten. Therefore, the solder joint fractures would have to occur at some time after the onset of solder solidification. Unfortunately, the actual solidification temperature is difficult to estimate given the degree of undercooling in Sn-based Pb-free solders[4, 5]. As in the first scenario, temperature gradients will exist across the component. However during cooling the joints in the outer rows of the perimeter array are expected to solidify before those in the inner rows. This differential solidification could also generate local stresses that could add to the stresses generated by differences in component and PCB CTE and warpage.

The differential melting may generate additional local stresses that could add to the any global stresses generated by differences in component and PCB CTE and warpage. Once the balls on the perimeter of the package melt, all the stress in the package is transferred to inner unmelted balls, which could result in fracture at those sites.

The first scenario, fracture during the reflow ramp up prior to solder melting, seems more plausible because it is easier to envision stress being transferred to and concentrated at the inner, unmelted joints. Clearly, the stress distribution and the relationship between peak stress, temperature, and solder solidification must be complex so fracture during cooling may be possible.

Subtle differences in local solidification and stress could account for the observed inner row failures and the variations in the extent of the cracking from site to site along the inner row. The asymmetric failure pattern could be caused by thermo-mechanical imbalances in the package and PCB. The fact that fractures occur only at the package side of the joints is most likely related to the fact that a solder joint formed on a non-solder mask defined Cu pad (as on the PCB) is more resistant to tensile and shear loading than a solder joint formed on a solder mask defined Ni plated pad (as on the package).

It is inexplicable that only a single BGA component on the entire PCBA is affected by the double reflow failure mechanism. It can be

Full Field Signed Warpage (mils)

	Temperature °C													
Sample	25	90	110	130	150	170	220	245	220	170	150	130	110	90
BGA "A"	-1	-1.6	-1.9	-2.0	-1.9	-2.0	-2.0	-0.8	-0.8	-1.4	-1.5	-1.6	-1.8	-1.7
PCBA	2.6	2.5	2.4	2.3	2.3	2.3	2.2	2.7	2.9	3.0	3.0	3.2	3.1	3.2
Max. Δ	2.7	4.1	4.3	4.3	4.2	4.3	4.2	3.5	3.7	4.4	4.5	4.8	4.9	4.9

Suspected temperature and warpage range for double reflow defects

Table 2: Thermal shadow Moiré measurements showing maximum warpage across the overmolded region of BGA Component A and the bottom side of the PCBA opposite Component A.

speculated that this particular BGA component has sufficient dynamic warpage or a uniquely vulnerable warpage signature with temperature that precipitates the failures. Cross-sectional analysis of several other BGA components showed no evidence of brittle fracture. It is possible that brittle fracture occurs to a lesser extent in some of the other BGA components but it was never found to manifest as a failure nor detected in the failure analysis done on these parts.

Shadow Moiré Dynamic Warpage Measurements

Dynamic warpage was measured on an unattached (stand-alone) Component A and on an entire assembled PCBA. A thermal shadow Moiré system was used to characterize warpage over a temperature range intended to simulate a solder reflow profile. Shadow Moiré uses geometric interference between a reference grating and its shadow on a sample to measure relative vertical displacement at each pixel position in the resultant interference pattern image. The thermal chamber is designed to enable measurements to be made during both heating and cooling cycles.

Dynamic warpage measurements were made on Component A and on the bottom side of the PCBA. Table 2 presents the warpage data as a function of temperature from room tempera-

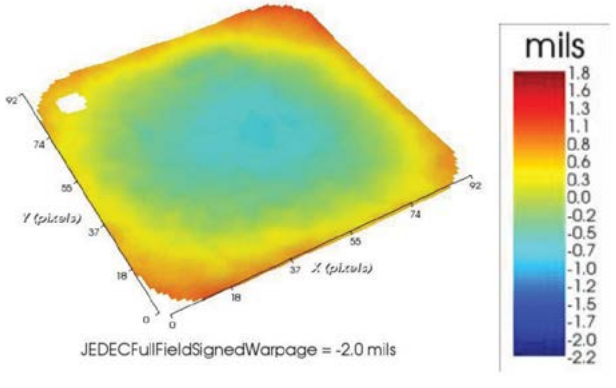

Figure 10: A warpage displacement map across the overmolded area of Component A measured during temperature ramp up at 220°C.

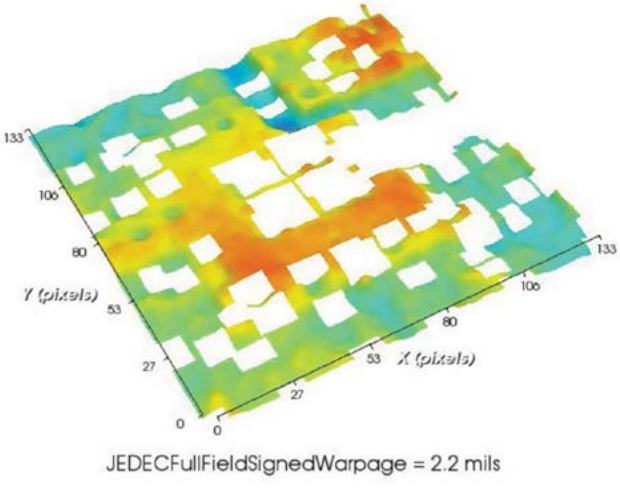

Figure 11: A warpage displacement map for the PCB footprint matching Component A. The measurements were made during temperature ramp up at 220°C.

ture to reflow at 245°C and back down to 90°C. These data show a maximum displacement (Δ) of >4 mils as the package ramps up to the solder melting point (220°C) and as the package begins to ramp down to solder solidification. Examples of three-dimensional warpage maps are shown in Figures 10 and 11. Figure 10 shows the warpage map for the overmolded region of the package. This is the region of the package that contained the failures (Figure 3). This measurement was made during temperature ramp up at 220°C. The maximum displacement over this surface is approximately -2.0 mils with out-of-plane bending in opposite corners (red regions). Figure 11 shows a comparable warpage map for the PCBA in the region of the Component A footprint. The maximum displacement of the PCB is +2.2 mils over this surface. Therefore, the maximum net displacement (warpage) of Component A relative to the PCB is 4.2 mils.

The thermal shadow Moiré data in Table 2 indicate a net displacement or warpage of Component A relative to the PCB of approximately 4 mils during heating in advance of melting or during cooling before solidification takes place (shaded Max. Δ cells in Table 2). It must be acknowledged that there are uncertainties in interpreting these displacement measurements. First, these measurements may not reflect the component and PCBA behavior accurately as it would occur during an actual factory reflow cycle. More importantly, the amount of warpage needed to induce solder joint fracture is unknown. A similar amount of warpage can create other serious BGA defects such as head-on-pillow (HoP), but HoP is a completely different failure mode[6, 7].

In most applications, 4 mils of warpage would be considered acceptable because defects like HoP and dropped ball would not occur. On the other hand, solder assembly defects due to warpage can appear with deviations in warpage as small as a few mils[8]. In the case of BGA double reflow, the magnitude of the warpage and induced thermal stress may not be the primary consideration. The more important factor may be the strength of the solder interconnection at higher temperatures close to the melting and solidification points of the solder. Consequently, it is conceivable that a small stress applied to the solder joint at high temperature when the joint has its lowest strength could cause a brittle interfacial fracture.

“The root cause analysis and subsequent successful corrective action indicate that in order to prevent double reflow defects, BGA components should not be subjected to multiple reflow passes. These double reflow defects could be another manifestation of warpage-related assembly defects that are increasing across the industry.”

Corrective Action

The obvious path for elimination of the failures in this design was to subject the BGA-side of the PCBA to only a single reflow pass. This corrective action was implemented successfully. The soldering of the heavy daughter card modules on the non-BGA side of the board was achieved by modifying other aspects of the assembly process.

The root cause analysis and subsequent successful corrective action indicate that in order to prevent double reflow defects, BGA components should not be subjected to multiple reflow passes. These double reflow defects could be another manifestation of warpage-related assembly defects that are increasing across the industry. A risk assessment is recommended whenever double reflow assembly of BGA components is proposed. The assessment should include evaluation of dynamic warpage data for the BGA components used in the design.

In the current analysis, using vapor phase reflow may actually have mitigated the effects of warpage. If the more conventional IR convection reflow had been used, it may have exacerbated the component and PCB warpage and increased the severity of the double reflow defects.

Conclusions

A comprehensive failure analysis was performed on a complex electronic printed circuit board assembly (PCBA) that exhibited intermittent open circuit electrical failures following Pb-free solder assembly. The following observations and conclusions are drawn from the results of the failure analysis.

• The root cause of the intermittent open circuit failures was brittle solder joint fractures at the interface between the Ni-Sn (nickel-tin) intermetallic compound (IMC) and the bulk solder at the package side of the solder joint. The solder joint fractures could not be detected until destructive cross-sectional analysis was performed.

• The fractures developed in a Pb-free perimeter plastic ball grid array (PBGA) following exposure to a second reflow cycle. The failure signature is characteristic of the so-called double reflow failure mechanism that has been reported very sparingly in the literature over the years. This may be the first reported example of this failure mechanism in a Pb-free solder assembly.

• The most likely scenario for describing the failure sequence is that the solder joints fracture just prior to solder melting during the 2nd reflow. In this scenario, the solder joint strength is at a minimum prior to melting and brittle solder joint fractures are induced by a complex combination of CTE and warpage stress on the solder joint during its exposure to the second reflow cycle. Thermal gradients across the BGA package during heating may contribute to the stress.

• The brittle fractures were eliminated by process changes that allowed the BGA-populated side of the PCBA to be exposed to only a single reflow cycle.

Acknowledgements

The authors would like to thank Neil Hubble of Akrometrix for the thermal shadow Moiré measurements and helpful technical discussions. **SMT**

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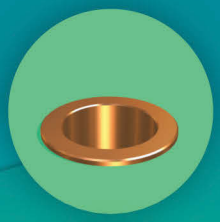

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The Evolution of ICT: What's Driving Today's Innovations?

by Alan J. Albee
TERADYNE INC.

SUMMARY: ***ICT systems have evolved greatly since their introduction three decades ago. In fact, the newest ICT systems might be termed "electrical test controllers" because some now support in-circuit, boundary scan, PLD programming, cluster and functional testing techniques.***

Abstract

Many manufacturers employ one or more in-circuit test (ICT) systems in their PCB manufacturing facilities to help them detect manufacturing process and component defects. These bed-of-nails electrical test systems are highly valued for providing the qualities of simple program generation, high fault coverage, fast test throughput, low false fail rates, and exceptional diagnostic accuracy as compared to other available test and inspection techniques.

Advancements in PCB technologies, along with changing test philosophies and manufacturing business models in recent years have created new and diverse requirements for manufacturers of in-circuit test systems. Particular challenges that ICT manufacturers have had to address include the erosion of test point access in certain product sectors, the progression of ultra-low voltage components, the variable test requirements of different product applications, the varying test philosophies of different market segments and different manufacturing regions, and the demanding throughput requirements of high-volume production facilities.

This article highlights how in-circuit test systems have evolved in recent years to include innovations and advancements to address these challenges and trends. Topics covered include boundary scan and functional test integration strategies, advancements in vectorless test techniques, incorporation of limited access electrical test techniques, test strategy analysis tools, high-accuracy pin drivers and sensors, concurrent test throughput improvement options, scalable test performance capability architecture, and program development accelerators.

This paper describes how these new ICT advancements contribute to lowering overall manufacturing test costs by improving the fault coverage, reliability, and throughput of in-circuit production tests.

Introduction

When in-circuit test systems were first introduced in the late 1970s, the world was a different place. PCB assemblies used through-hole technologies, spacing between pins was typi-

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cally 100 mils, components were only placed on a single side, the largest components rarely had more than 14 pins, the prevalent voltages used to power the boards were 5, 12, and 15 volts, manufacturing occurred in the highly industrialized regions where the products were consumed, and manufacturing test consisted primarily of the execution of complex and time consuming functional tests.

The introduction of in-circuit test systems revolutionized the PCB manufacturing process by changing the test paradigm from testing the functionality of the board to testing the functionality of the parts along with the integrity of the assembly process. In-circuit test systems accomplished this by using a bed-of-nails test fixture to make electrical contact to every net on the PCB allowing each component to be individually stimulated and measured. With such electrical test access and innovative guarding and voltage forcing techniques—which allowed each component to be tested individually without the influence of its surrounding parts—ICT systems could quickly detect shorted and open pins, missing components, incorrect analog component values and tolerances, and faulty digital component logic. The theory behind in-circuit testing is that manufacturers can be confident that the board will operate correctly if they verify that all the components are operating correctly and have been properly assembled.

The real breakthrough with in-circuit testing was the benefits it provided compared to traditional functional tests. Test generation was greatly simplified because test developers no longer had to understand the functionality of the board, and they could automatically generate programs in days, not weeks. The quality of the test coverage also improved with ICT, because direct access to every net eliminated the functional test complexity of trying to propagate faults from internal nets to externally observable test points. Finally, in-circuit test systems provided faster test throughput and exceptional diagnostic accuracy that were not possible with functional tests. All these benefits resulted in fast adoption of ICT systems, and they quickly eclipsed complex functional test systems and became the test system of choice for most high-volume manufacturers.

In-circuit test systems have had to evolve throughout the years to keep up with the demands of ever-changing PCB technologies, the advance of global manufacturing capabilities, and the diversity of testing philosophies for different product and market segments.

"The real breakthrough with in-circuit testing was the benefits it provided compared to traditional functional tests. Test generation was greatly simplified because test developers no longer had to understand the functionality of the board, and they could automatically generate programs in days, not weeks."

Addressing Erosion of Test Point Access

The cornerstone of traditional in-circuit testing has been the ability to gain electrical test access to all of the nets on the PCB using electrical test probes. In-circuit test providers use comprehensive CAD analysis and probe placement solutions to analyze circuit board designs and generate wiring instructions that fixture fabricators use to assemble bed-of-nails in-circuit test fixtures.

It is becoming increasingly more challenging to find probe placement solutions that provide full electrical test access to all the nets on the PCB. This is because shrinking packaging technologies, greater IC integration and functionality, higher pin counts, faster I/O speeds and reduced product footprints have led to ultra-miniaturization. To support this trend, manufacturers are designing increasingly complex HDI boards that make use of blind and buried vias, smaller tracks with tighter spacing and with less copper available on the board surface for electrical test access. This trend is more pronounced for high-volume consumer products which place a premium on small size, fast performance, and low power consumption.

One way that designers and fixture fabricators have addressed these challenges is through the use of more advanced probe technologies. Traditional ICT probe technology which consists of a small probe contacting a larger test pad target on the unit under test (UUT) is restricted to a target diameter of .024 inches with center spacing of .0395 inches between probes. New highly accurate probe fixturing technologies developed by the fixture fabricators are available that make it possible to design ICT fixtures that can reliably contact test points as small as .012 inches with pitch of .020 inches[1].

To provide access to even smaller test points, manufacturers can use micro-access test technologies. Instead of using a small point test probe in the fixture to contact a large test pad on the board, micro-access test technologies use a large head test probe in the fixture to contact a small test point on the board. Micro-access test technique concepts have been around since the 1990s, and Table 1 describes the general concepts behind five different implementations. Micro-access technologies allow manufactures to get electrical test access to test points that are as small as the signal traces themselves; however, their use is only viable on signal traces that can be accessed from the top or bottom layer of the UUT and the micro-access test points must be spaced appropriately to avoid conflict with the large head probes that are used in the test fixture.

Despite the advances in ICT fixturing technology, manufacturers sometimes find it challenging to get complete physical test access to the boards they are testing. The effectiveness of ICT diminishes as physical test access is lost, so some ICT test systems have evolved to augment physical test access with virtual test access techniques. Table 2 shows the reduced access tools that are available on some ICT test platforms.

The tools highlighted in Table 2 extend the capabilities of the ICT system allowing manufacturers to still maintain high fault coverage even on boards that do not have full physical

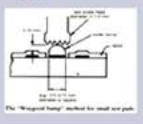
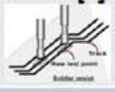
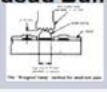
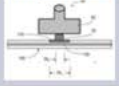
Micro-Access Technique	Date	General Concept	Benefits	Considerations
Waygood Bump [2] 	1990	Place small solder bumps on test pads and contact them with large head probes	Improves probing accuracy by targeting small solder bumps with large test probes rather than large test pads with small test probes	Size of test pad may hinder performance and probe placement for high speed/high density PCB designs
Vaucher [3] 	1996	Open small apertures in solder mask above signal traces and contact them with deformable tipped probes	Allows direct access to signal traces with special probes that do not require solder bumps	Contact reliability depends on deformable probe performance
Prasad Bump [4] 	1997	Same as Waygood Bump, except proposes that solder bumps be placed on significantly smaller test pads	Better suited than Waygood Bump for high speed signals and high density interconnect designs	Smaller test pads and solder bumps may reduce mechanical performance
Bead Probe [5] 	2003 + 2007	Place small solder bumps directly on signal traces through open apertures in solder mask and contact them with large head probes	Also good for high speed signals and high density interconnect designs	Licensed technique limits which test equipment Mfgs can use / Less robust mechanical performance
Test Access Component [6] 	2007	Place small conductive Surface Mount Components directly on top of signal traces and contact them with large head probes	Very robust mechanical performance compared to other Micro-Access techniques	Need to place extra SMT component which can add costs

Table 1: Micro-access comparison matrix.

Technique	Description	Benefit
Boundary Scan / Embedded Test	Many boards today have components with built-in testability features like boundary scan that can be activated during in-circuit testing to run board self tests or provide virtual access to signals on the board when the ICT system does not have physical test access.	Detects faults on nets that do not have physical test access. Uses ICT resources and board testability features in concert for maximum test effectiveness. Consolidates tests on single manufacturing test solution.
Combined BSCAN + Framescan [7]	Combines BSCAN and capacitive opens test techniques. BSCAN devices provide digital stimulus, probe sensor plate in fixture detects stimulus signal.	Identifies open pins on connectors, sockets and IC devices that do not have physical test access.
Indirect Testing	Indirect stimulus of inaccessible pins through low value resistors or buffers on the board.	Allows ICT system to indirectly test nets that do not have direct physical test access using physical nails on the other side of low value resistors and buffers.
Cluster Testing	Groups of two or more components are tested as a single entity to verify proper operation	Allows testing of functions like RC Networks and filter circuits without access to all pins in the cluster.
Functional Test [8]	Application specific circuit board functional tests are executed using add-on functional test instrumentation.	Some ICT systems have ability to plug in industry standard PXI instrumentation which allows ICT to be integrated with functional test in a single test stage.
Adaptive Test Generation	Intelligent test generators and device models are designed to automatically adapt to circuit constraints and missing test access.	Faster test generation and program debug; less time modifying tests to account for different wiring configurations.
Distributed Test [9]	Intelligent analysis tool that can analyze test access, objectively report fault coverage, model alternative test strategies, and recommend optimal test strategies based on manufacturer preferences.	Simplifies the task of understanding ICT fault coverage and the alternative inspection methods that could be used to detect defects other than ICT.

Table 2: Limited access tools augment ICT.

test access. It must be noted, however, that the tradeoff for using these tools is often an increase in programming complexity, less accurate diagnostics at the repair station and longer test execution times. Given these tradeoffs, it is in the best interest of designers and manufacturers whenever it is possible to provide physical test access to every pin they can.

Addressing Ultra Low Voltage Technologies

As Moore's Law predicted, the number of transistors in integrated circuit packages has approximately doubled every two years over the last two decades. The greater the number of transistors in a package the more power it requires. The amount of power a transistor requires is calculated using the formula

$$Power = Frequency \times Capacitance \times Voltage^2.$$

Designers have discovered that the most effective way to reduce the power requirements for their products and satisfy the reduced power consumption and environmental concerns of their customers is to lower the voltages at which they operate. As a result, many boards now contain devices that operate with a combination of low voltage logic levels of 1.8V and below. The challenge for many in-circuit test systems is that their pin electronics were originally designed when 5V was the predominant

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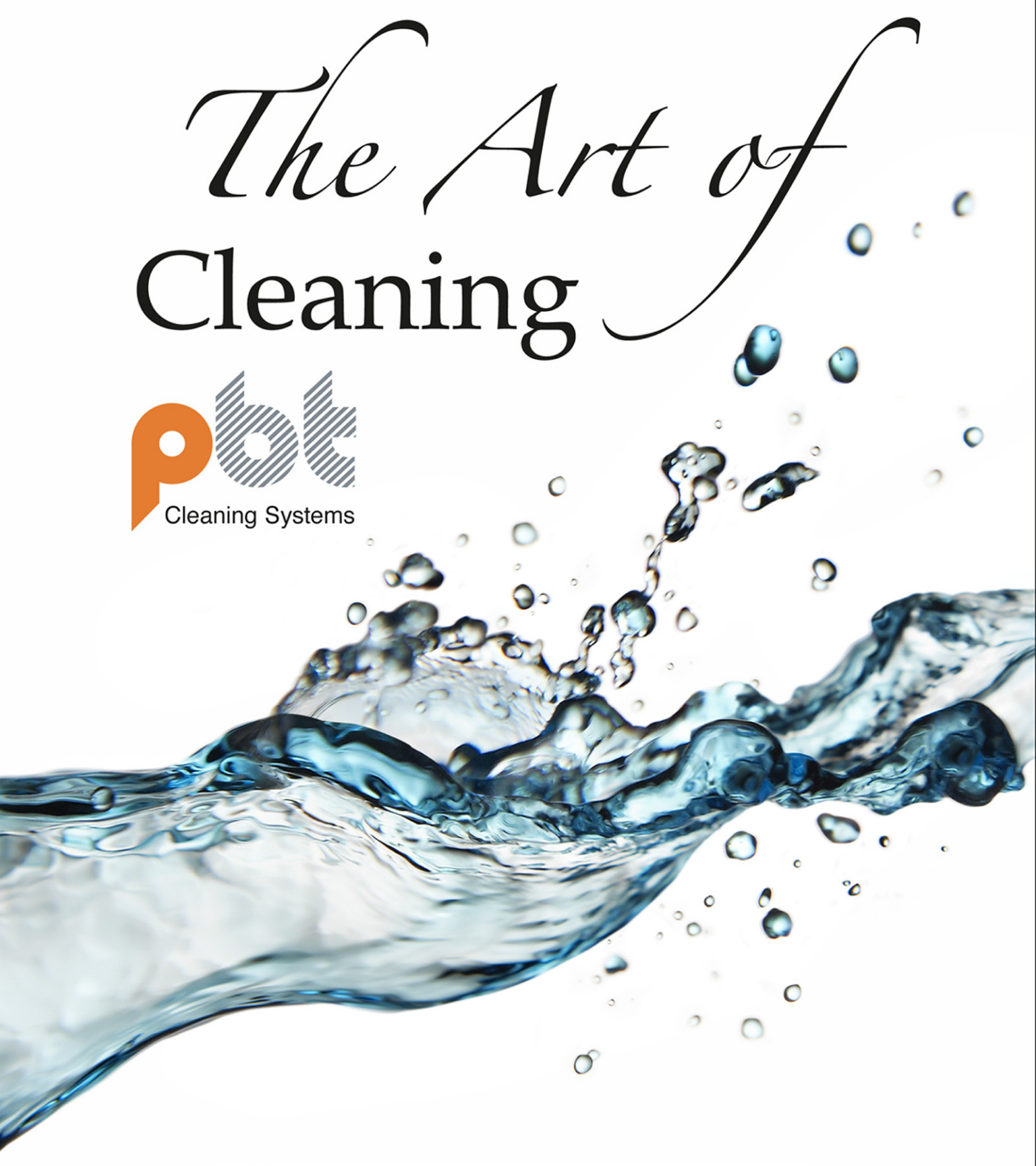

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logic technology and many of them do not have the required accuracy to test these ultra-low voltage components accurately, reliably, and safely.

Some in-circuit test systems have evolved to address this low voltage testing challenge by updating their digital pin electronics with dramatically improved drive and sense accuracy (as low as 15mV). Other capabilities added to ensure safe and reliable testing include real-time backdrive current measurement and control features (to prevent devices from being harmed by electrical over-stress conditions); automatic driver verification (to guarantee that drivers reach their programmed logic levels); dual-level sensor thresholds (to ensure device output drivers are within published specifications); and programmable per-pin logic levels (to support devices that require multiple independent logic levels)[10].

In-circuit test systems equipped with these advanced digital test capabilities can confidently perform powered-up digital testing of the latest low voltage technologies. However, if manufacturers are using in-circuit test equipment that do not have these advanced digital test capabilities they may not be able to reliably or safely test low voltage components, or they be forced to resort to unpowered vectorless test strategies of their low voltage digital parts which are slower, more expensive, and less comprehensive[11].

Addressing Diverse Test Requirements

In addition to evolving to meet the technology requirements previously described, manufacturers of ICT systems have had to evolve to meet the shifting testing philosophies and business economic drivers of their customers. ICT vendors have struggled to satisfy the demands of manufacturers who specify different requirements for their ICT systems and who have different expectations as to what they need the system to do.

The factors that drive these expectations include:

- PCB complexity—simple or complex board; low or high pin count; full or limited test access?
- Product cost—low margin consumer product; high cost server, communication, or military/aerospace board?
- Reliability and regulatory obligations—what safety standards are required for automotive, medical, and industrial equipment?
- Manufacturing strategy—outsourced vs. internal manufacturing, multi-site manufacturing, frequent manufacturing location changes.
- Product volume and mix—high mix/low volume, dedicated high-volume production lines, automated vs. operator-driven operation.
- Manufacturing skill levels—experienced vs. inexperienced developers and operators, trained vs. untrained personnel.

All these factors combine to place conflicting demands on ICT systems. Low-margin manufacturers demand low-cost ICT. Manufacturers of high-reliability, highly complex products demand high fault coverage and high pin-count capacity. Untrained operators demand simple operation; highly skilled test engineers demand powerful programming capabilities. High-volume manufacturers demand ever higher test throughputs, while manufacturers using outsourcing business models demand equipment compatibility. To further complicate matters for ICT vendors, different market segments and geographic regions implement different test philosophies.

"Untrained operators demand simple operation; highly skilled test engineers demand powerful programming capabilities. High-volume manufacturers demand ever higher test throughputs, while manufacturers using outsourcing business models demand equipment compatibility."

Historically, ICT vendors have addressed these conflicting demands with different classes of ICT systems. Manufacturing defect analyzers offered low price and simple test operation, but provided limited

test capabilities and low fault coverage. High-performance in-circuit testers offered extended test capabilities and high fault coverage, but were expensive and complex to program. In the middle were a variety of standard in-circuit test systems that offered more performance than an MDA class system at a lower price than high-performance class ICT systems.

Given the different classes of test systems, many manufacturers now have production floors with multiple incompatible classes of ICT systems, often from different ICT vendors. There can be a hidden cost to this multi-system test strategy because it increases system training and service costs, increases program maintenance costs, and reduces flexibility in test equipment utilization.

If a manufacturer decides to only use an MDA class tester, then they may not be able to adequately test complex PCB assemblies due to its limited capabilities. On the other hand, if a manufacturer decides on a high-performance ICT platform solution, it can be overkill for simple PCB assemblies where the high-performance ICT features are not always needed and the program development requires higher skilled operators.

Some ICT vendors have evolved their testers into highly scalable systems that satisfy diverse test requirements in a single compatible platform. These systems can support multiple pin board types, independent hardware options and software plug-ins that can be used to expand the capabilities of the tester. Figure 1 shows how this approach can be used by manufacturers who can buy only the test capability they need and grow or reduce test capabilities without changing the tester. The benefits include lower training and programming costs because operators only have to learn one test system and develop one test program, higher equipment utilization rates because a single test system can be used for multiple test applications and higher equipment value because the tester can be configured as an MDA+ system all the way to a high-performance digital ICT system. To facilitate test program compatibility and equipment utilization, the test executive on these ICT systems will adapt to run only those tests in the program that can be supported with the given hardware and software configuration of the target tester. No more need to create custom test programs designed for the configuration of each tester on your production floor!

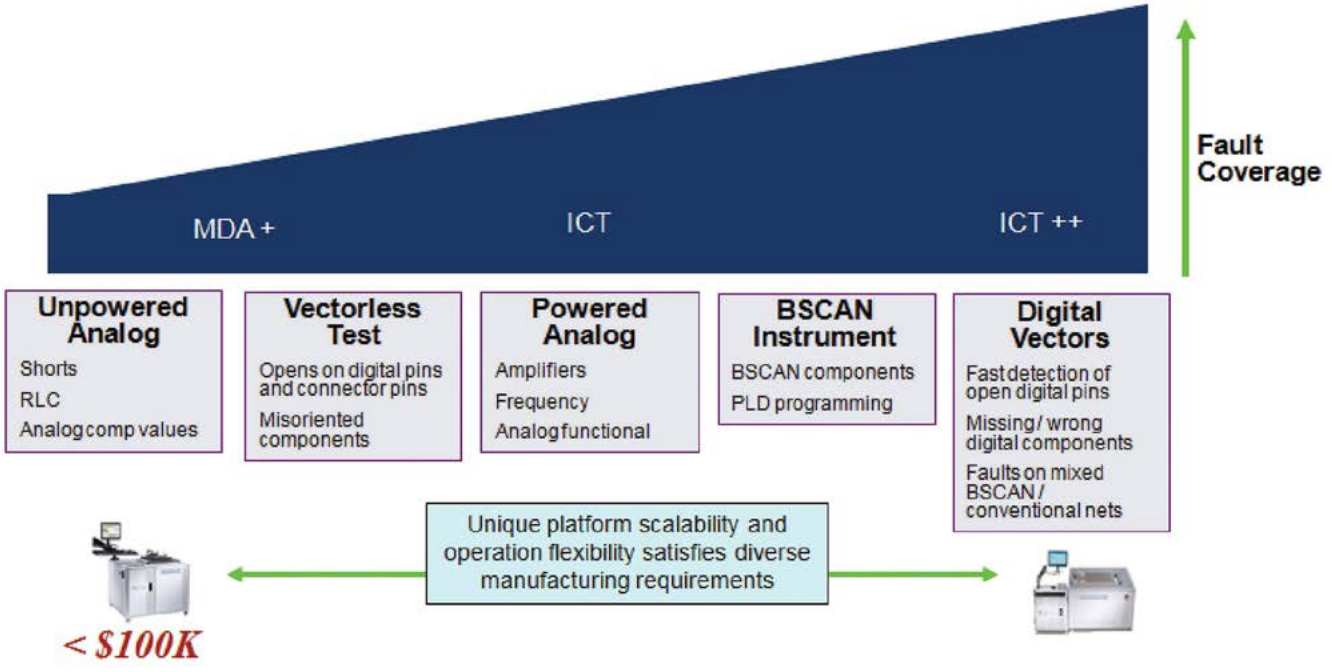

Figure 1: Scalable ICT platform satisfies diverse manufacturing requirements.

High-Volume Manufacturing Requirements

High-speed assembly equipment continues to improve resulting in ever faster beat rates on the production line. The beat rate for today's high-volume production lines is often less than 30 seconds. In-circuit testers can become the bottleneck in the production line when their test times exceed the beat rate of the assembly equipment and place a limit on the number of boards that can manufactured per hour.

When this happens manufacturers can choose to add additional test equipment to increase their test capacity or they can reduce test times by eliminating tests until the test time is below the target beat rate. Neither of these options is considered ideal as adding additional test equipment is expensive, requires extra test fixtures, and is not always possible because production facilities often have limited floor space. Eliminating tests requires extra program maintenance and reduces the amount of defects that can be detected by the ICT system.

A better approach is to increase the execution speed of the tester until it no longer is the bottleneck on the production line. Some ICT systems have evolved to support concurrent testing of more than one component at a time. This is accomplished by duplicating instrumentation in the test system so that the test executive can test multiple components in parallel (typically on boards manufactured as part of a panel). How concurrent test is implemented differs for different ICT vendors and the amount of concurrency depends on many factors, but ICT systems with concurrent test features can generally test 1.5–2 times faster than a standard ICT tester.

In addition to increasing the test execution speed, high-volume manufacturers also try to reduce or eliminate the board handling times. This can be done on non-automated lines by using dual-well fixtures so there is no delay between testing boards, however the highest volume can be achieved by eliminating the test operator and placing the ICT system in an automated line. Some ICT vendors sell their ICT subsystems as standard 19" rack mount components so that they can be easily integrated into the automated handler solution that is preferred by the manufacturer.

Finally, some manufacturers provide test throughput analysis and optimization software that can modify test parameters to ensure that the test program is optimized for the fastest test throughput. This software reduces test times by an average of 15% and identifies test inefficiencies in the program that could be corrected to further reduce test times.

"Some ICT systems have evolved to support concurrent testing of more than one component at a time. This is accomplished by duplicating instrumentation in the test system so that the test executive can test multiple components in parallel (typically on boards manufactured as part of a panel)."

Conclusion

ICT systems have evolved to address the technology and business challenges of modern PCB manufacturing, with capabilities advancing greatly since ICT's introduction. Reduced access test techniques, integration of boundary scan and embedded testability tools, advanced pin electronics capable of testing low voltage technologies, concurrent test capabilities, functional test capabilities, and scalable test system configurations have all combined to extend the life of ICT systems and make them one of the tools that is still most valued by high-volume PCBA manufacturers.

Considering how the in-circuit tester has evolved and all of the electrical test capabilities that do not require actual physical test access, it may be time for the industry to stop categorizing these test systems as in-circuit testers. It may be more appropriate to start categorizing these versatile test systems as "electrical test controllers" because the most capable ones can support in-circuit, boundary scan, PLD programming, cluster and functional testing techniques all in a single consolidated test platform. **SMT**

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This paper was originally presented at IPC APEX EXPO 2013.

Alan J. Albee is product manager at Teradyne.

Creating a 3D Image Through a Single Lens

Researchers at the Harvard School of Engineering and Applied Sciences (SEAS) have developed a way for photographers and microscopists to create a 3D image through a single lens, without moving the camera.

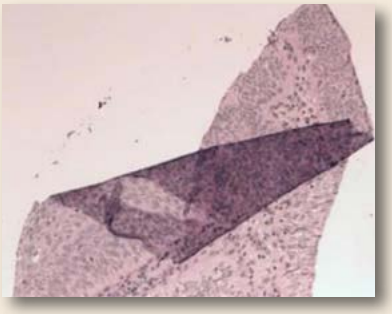
Published in the journal Optics Letters, this improbable-sounding technology relies only on computation and mathematics—no unusual hardware or fancy lenses. The effect is the equivalent of seeing a stereo image with one eye closed.

Principal investigator Kenneth B. Crozier, John L. Loeb Associate Professor of the Natural Sciences, explains.

"If you close one eye, depth perception becomes difficult. Your eye can focus on one thing or another, but unless you also move your head from side to side, it's difficult to gain much sense of objects' relative distances," Crozier says. "If your viewpoint is fixed in one position, as a microscope would be, it's a challenging problem."

Crozier and graduate student Antony Orth essentially compute how the image would look if it were taken from a different angle by relying on the clues encoded within the rays of light entering the camera.

"Arriving at each pixel, the light's coming at a certain angle, and contains important information. Cameras with all kinds of new hardware, microlens arrays and absorbing masks can record the direction of the light, and that allows you to do some very interesting things, such as take a picture and focus it later, or change the perspective view. We asked, can we get that functionality with a regular camera, without extra hardware?"



SMTAI Conference and Exhibition in Ft. Worth, October 13–16

The SMTAI Conference and Exhibition in Ft. Worth, Texas beginning Sunday, October 13 promises the latest information for attendees who would like to reduce defects and control processes. This international technical conference will offer tutorials, tech sessions, spotlight sessions, technical committee meetings, and more.

The event kicks off on Sunday with tutorial sessions in the morning and afternoon, and is followed on Monday with more tutorial sessions, AIMS/Harsh Environment Symposium, and Evolving Technologies summit.

On Tuesday, Keynote Speaker Bob D. DuLaney, Lockheed Martin, USAF Major General (Ret), officially opens the event, which is followed by technical sessions, free spotlight sessions, free lunch, poster session and certification seminars all day Tuesday and Wednesday.

The Electronics Exhibition, featuring more than 150 exhibiting companies, will be open Tuesday and Wednesday, October 15 and 16, from 9 a.m. to 5 p.m. For a complete listing of exhibitors, click here.

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Board Design Moves Beyond Reach of In-Circuit Testers

by Adam Ley
ASSET INTERTECH

SUMMARY: ***Although intrusive test technologies on the manufacturing floor such as ICT have been effective in the past, recent advancements in basic electronic technologies are disrupting legacy test methods. Now, non-intrusive board testing is replacing the intrusive types, such as in-circuit testing.***

In just the last five years, the advancements in microprocessors, communications chips, memory and other base technologies have been phenomenal. Circuit board design and assembly techniques have changed accordingly to accommodate the many breakthroughs in base technologies. Consequently, these new design and assembly techniques are wreaking havoc on the test coverage previously provided by intrusive test technologies like ICT.

Fortunately, non-intrusive board test (NBT) has emerged as a more cost-effective test methodology for the manufacturing floor. Certainly, ICT and other intrusive test technologies, such as manufacturing defect analyzers (MDA) and flying probe testers (FPT), will continue to have their place, but they soon could be relegated to special case testing or for testing rudimentary circuit board designs. NBT offers better test coverage and a lower cost structure.

Specifically, today's sophisticated board design techniques do not provide physical access for probes, which is a requirement of ICT. What's more, system and board designers don't want to provide ICT access. At best, designing in tests pads to give probe access to a circuit board could slow system performance to unacceptably low levels; at worst, the system's ability to function as specified could be placed in jeopardy.

From a business perspective, ICT systems are expensive to procure, maintain and operate. Complex bed-of-nail test fixtures are time-consuming to produce and costly. Many new product introductions have been delayed because engineers had no other choice but to wait weeks at a time for ICT test fixtures to be produced

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for each re-spin of a board design. The alternative is NBT, a suite of technologies that provide comparable or better test coverage at less cost and are software-driven, not hardware-intense.

Shrinking ICT Test Coverage

ICT test coverage is shrinking for a variety of technical reasons.

Circuit Density

Increasing chip and board densities have limited the physical space available for test probes. For example, the geometry of chips in ball grid array (BGA) packaging has shrunk considerably, dropping from .4 mm ball pitch (center-to-center spacing) to .3 mm. This seemingly small shift has a significant effect on probe access. With a .4 mm ball pitch, there is enough room for a via—those vertical interconnects that span multiple layers on boards—to be routed through the circuit board and connected to the chip by way of a high-density interconnect (HDI). But fine pitch .3 mm BGAs do not allow enough room on the board for a via except directly into a ball or pad on the device (Figure 1). To accommodate smaller device geometries and greater circuit densities, new circuit board manufacturing methods like microvias for HDI and others have been adopted. These board design and assembly methods have made physical access for ICT even

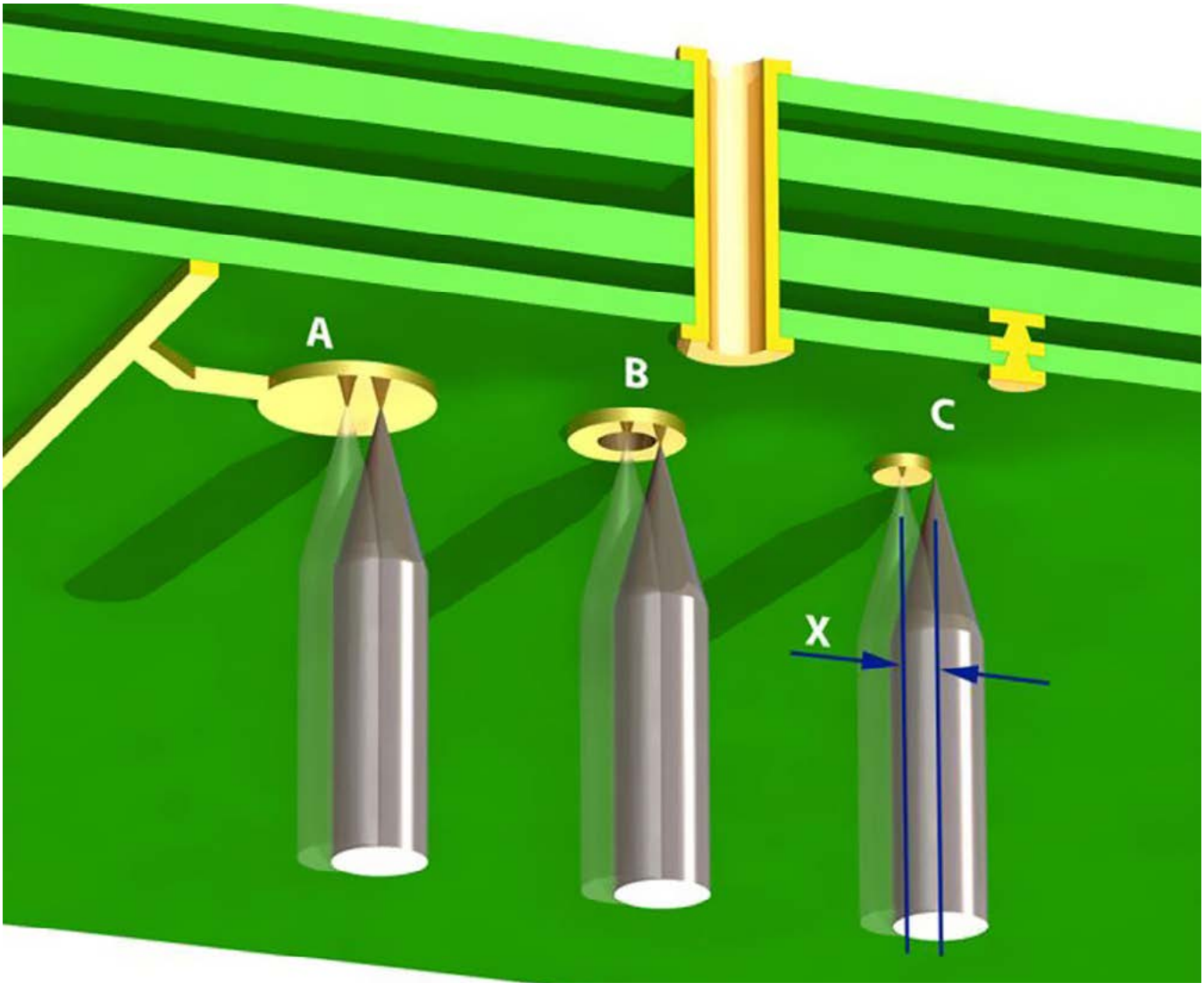


Figure 1: Circuit density and its effects on probe placement.

more difficult to come by since the surface features, if any, are much too small to access by test probes.

Probe-Induced Strain

When an ICT bed-of-nails fixture places a probe on a circuit board, strain is exerted on the board. This strain, or "flexure," can create defects in solder joints (Figure 2). In fact, this ICT-induced strain can be much greater than any force placed on a board when it's installed and in operation in the field. It is ironic that ICT, which is attempting to find defects, can actually produce the defects it is trying to detect.

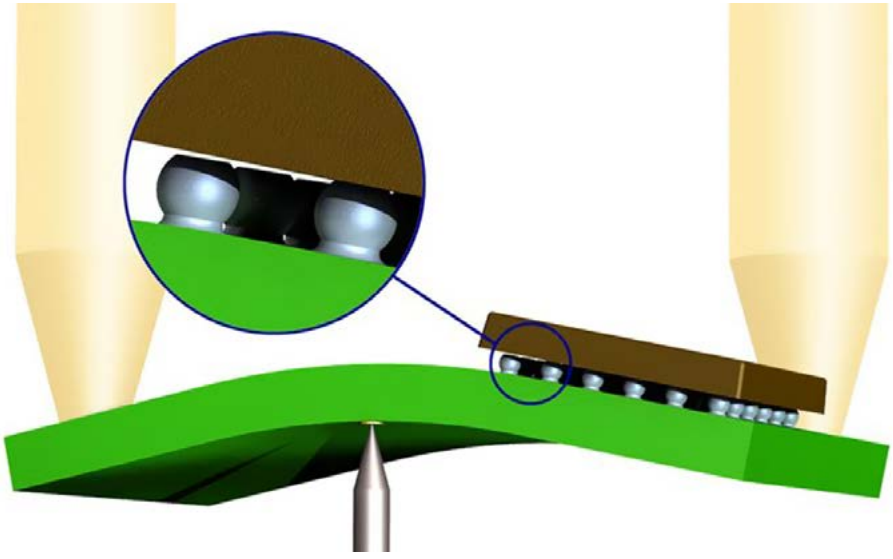


Figure 2: Flexure, the strain resulting from the force of ICT probes, can actually cause the structural failures they are trying to detect.

Circuit Speed

The speed at which signals travel across traces on circuit boards is constantly increasing to keep up with the increasing performance of chips and to support the huge data throughput rates that are typical of today's networked systems (Table 1).

As the speed of a bus approaches 5 gigatransfers per second (GT/s), the traces on a board become very sensitive to capacitive coupling, electromagnetic interference (EMI) and electromagnetic compliance (EMC) concerns. In fact, placing any sort of test pad on one of these high-speed buses could disrupt bus signaling to the point where system performance is jeopardized. Bringing an internal route to a surface layer to connect to a test pad would create an un-terminated stub on the route, inducing signal reflections and ringing, and possibly reducing bus speeds. For these and other reasons, many reference designs provided and recommended by the suppliers of high-speed chips such as Intel and others strictly prohibit the placement of test pads on high-speed buses. Fewer test pads mean less test coverage for ICT.

In addition, many board designs limit or totally restrict routes on the surface layer (Figure 3). Sometimes a circuit board's surface will func-

Double Data Rate memory (DDR)	
DDR1	400 MT/s
DDR2	1.066 GT/s
DDR3	2.133 GT/s
DDR4	4.266 GT/s
Peripheral Component Interface Express (PCIe)	
PCIe 1	2.5 GT/s
PCIe 2	5 GT/s
PCIe 3	8 GT/s
PCIe 4 (2014/2015)	16 GT/s
Universal Serial Bus (USB)	
USB 1.1 - Low-Speed	1.5 MT/s
USB 1.1 - Full-Speed	12 MT/s
USB 2 (Hi-Speed)	480 MT/s
USB 3 (SuperSpeed)	5 GT/s
Serial Advanced Technology Attachment (SATA)	
SATA 1	1.5 GT/s
SATA 2	3 GT/s
SATA 3	6 GT/s
Direct Media Interface (DMI)	
DMI 1 (2004)	2.5 GT/s
DMI 2 (2011)	5 GT/s

Table 1: Escalating speeds on several popular high-speed buses.

tion as a power or ground plane to better cope with EMI issues. For example, the top and bottom layers of a board may be coated with metal to better control EMI. EMI concerns have also limited the adoption of the bead probe method of ICT. In order to deploy bead probe on an ICT system, the routes must be exposed on the surface layer. Unfortunately, surface routes will radiate significant EMI, which has become increasingly unacceptable.

In addition, vias are frequently back-drilled as a way of proper termination to ensure signal integrity. A via routed from a chip on one surface to a test pad on the opposite side of a board would be an un-terminated stub, which would cause signal reflections and ringing on the trace. Back-drilling eliminates the stub and also the possibility that a test pad for ICT testing could be placed on the via.

Blind and buried vias are often designed into circuit boards to limit the number of board layers. Both types eliminate the possibility of test pads on the via. A blind via is routed from one surface layer to an internal layer. A buried via interconnects nodes on internal layers and never comes to a surface layer (Figure 4). This internal routing may reduce the number of layers, but it also eliminates external physical access to the nodes. Blind and buried vias can severely reduce the test coverage provided by ICT testers.

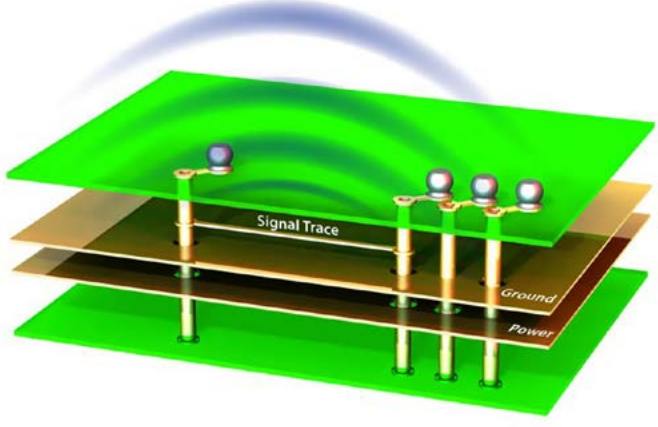


Figure 3: Electromagnetic interference (EMI). Many circuit board designs today place the traces on internal layers to reduce EMI emanating from surface layer traces and test pads.

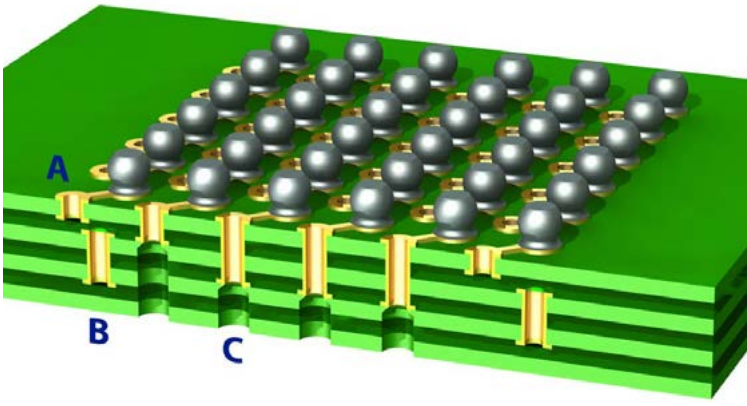


Figure 4: Via stubs. The image illustrates a blind via (A), a buried via (B) and a via that has been back-drilled (C) to reduce EMI issues.

Non-Intrusive Board Test (NBT)

As a software-based methodology, NBT is not subject to the limitations of probe-based test technologies like ICT. A simple connector on a printed circuit board typically links the board to an NBT test station, which is usually a PC or laptop. Frequently, NBT test technologies connect to the board through a JTAG port (IEEE 1149.1 Boundary-Scan Standard's Test Access Port). In addition, NBT will utilize embedded instrumentation intellectual property (IP) in chips and on circuit boards. Several complementary debug, validation and test technologies can comprise an NBT test strategy. The typical test technologies that can be included in an NBT test strategy are high-speed I/O validation using instruments embedded in chips, boundary-scan test (BST) for structural testing, processor-controlled test (PCT) for structural and functional testing, FPGA-controlled test (FCT) for a variety of test functionality and others.

NBT applies test vectors that are internal to the board and offers extensive diagnostics to pinpoint faults. Because it is a software-driven test strategy, an NBT test station can run several complementary test technologies and, in this way, obtain improved coverage for all three of the critical types of testing: structural, functional and performance. Moreover, implementing NBT's multiple test technologies on one test platform simplifies NBT's deployment on the manufacturing floor.

The test technologies that can be configured in an NBT test system are capable of testing a larger fault spectrum than ICT. For example, ICT only tests boards at the speed of the ICT tester, not the speed of the board or the chips on the board. In contrast, NBT's signal integrity tools for high-speed buses are at-speed tools that can validate operational performance. Some NBT systems feature a bit error rate testing (BERT) tool that can uncover which lanes on a high-speed serial interface are malfunctioning. NBT margining tools can plot eye diagrams to determine the signal integrity on the bus. Another at-speed NBT tool, PCT, accesses the board through the processor's debug port to perform debug, device initialization, at-speed functional test with structural diagnostics and other test functionalities. FCT temporarily inserts test instruments into an on-board FPGA and applies test vectors at-speed. The nature of any particular FCT test suite will depend on the instruments inserted into the FPGA and this will be determined by the objectives of the test strategy for the particular circuit board.

Oil and Water?

Some ICT suppliers have tried to incorporate NBT techniques into their testers, but this is like trying to mix oil and water. It doesn't work very well. For example, an ICT system is not an effective platform for boundary-scan test (BST). Running BST on an ICT tester shackles BST with the limitations of ICT. Standalone NBT systems with BST avoid this problem. Consider that most ICT testers have a maximum test clock (TCK) of 1 or 2 MHz, which is far too slow for testing high-speed memories like DDR2/3. In addition, most installed ICT testers do not currently support the boundary-scan standard for high-speed AC-coupled nets, IEEE 1149.6. This rules out testing high-speed buses like PCI Express, XAUI and SATA on an ICT tester. In addition, BST on ICT will require isolation of the main probes in the test fixture to reduce noise from the probes and to make the test repeatable and deterministic. Often, this results in dual-stage ICT fixtures, which drive up the cost of test significantly as well as the complexity of test operations.

Test re-use over a system's entire life cycle is another benefit of BST found in NBT test stations. The non-intrusive debug, validation and test technologies incorporated in NBT systems can be deployed throughout a product's life cycle, beginning in design for prototype board bring-up, followed by volume manufacturing, and eventually migrated to repair and troubleshooting operations. Software-driven tests developed early during the design stage can be reused until product obsolescence, reducing the total cost-of-test significantly. Costly ICT testers only make economic sense in high-volume/low-mix manufacturing environments, but their eroding test coverage is making ICT less cost-effective in all applications.

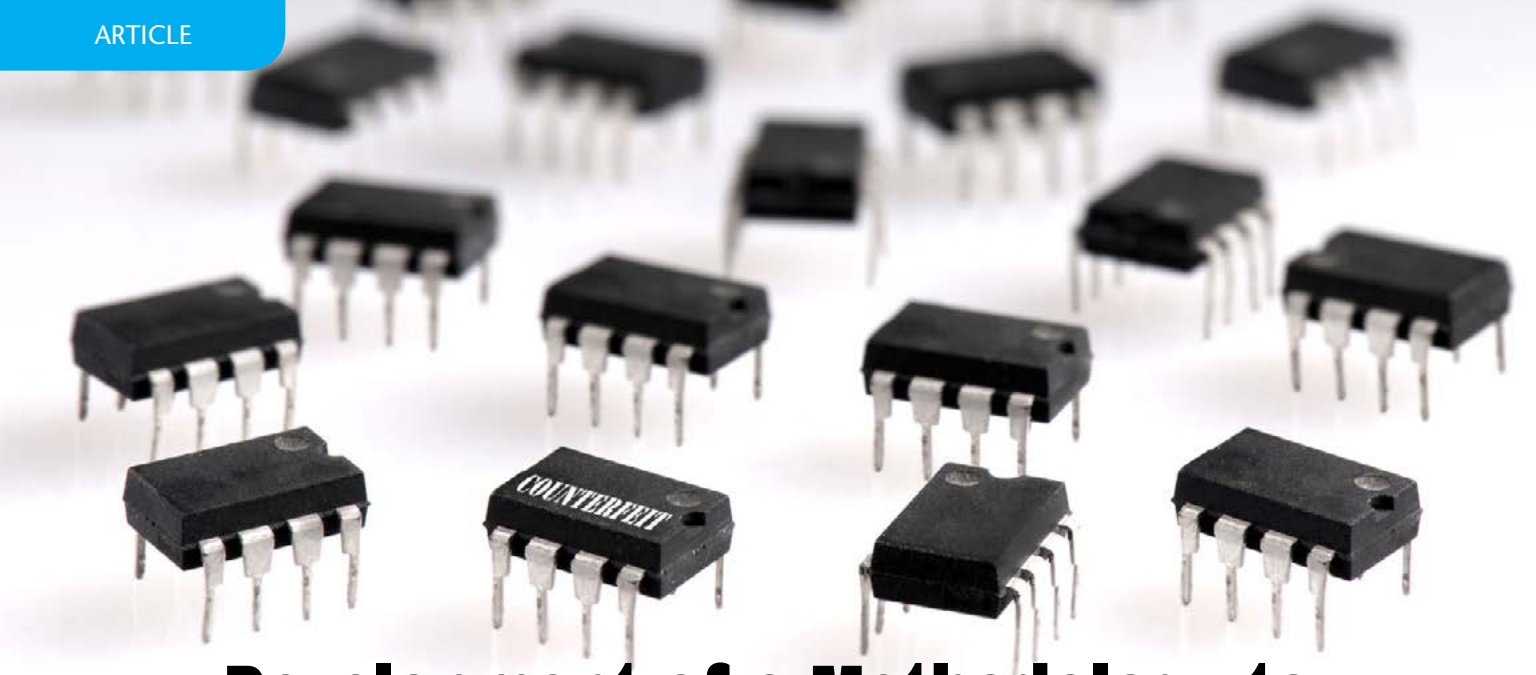
Conclusions

Although intrusive test technologies such as ICT have been effective in the past on the manufacturing floor, recent advancements in basic electronic technologies are disrupting legacy test methods. Fortunately for electronics manufacturers, non-intrusive software-based test technologies have emerged over the last 10 years. By capitalizing on the strength of software—its low procurement and operational costs relative to hardware-intense test systems like ICT, as well as its flexibility, adaptability and agility—NBT technologies offer an array of significant solutions today and will continue to do so as electronic technology advances in future. **SMT**

References

A number of white papers and eBooks explaining non-intrusive test technologies can be found here.

Adam Ley is chief technologist for non-intrusive board test and JTAG for ASSET InterTech. For the decade prior to ASSET, he held several positions with Texas Instruments, including application support for TI's boundary-scan logic products and for test and characterization of new logic families.



Development of a Methodology to Determine Risk of Counterfeit Use, Part 1

by iNEMI Counterfeit Components Project Team:
Harrison Miles, CORELIS,INC.
Mark Schaffer, INEMI

ABSTRACT

Counterfeit components have become a multi-million dollar, yet undesirable, part of the electronics industry. The profitability of the counterfeit industry rests in large part on its ability to recognize supply constraints and quickly respond, effectively taking advantage of a complex and vulnerable supply chain. Factors such as product obsolescence, long life cycles, economic downturn and recovery, local disruptions in manufacturing due to natural disasters, and lack of proper IP legislation all represent opportunities for the counterfeit component industry to flourish. Electronic counterfeits affect every segment of the market, including consumer goods, networking and communications, medical, automotive, and aerospace and defense. In manufacturing, the use of undetected counterfeits can lead to increased scrap rates, early field failures, and increased rework rates; while this presents a major problem impacting profitability, the use of counterfeit components in high reliability applications can have far more serious consequences with severe or lethal outcomes.

The independent distributor level has typically been seen as the weak link in the supply chain where counterfeits are most likely to be introduced. With the emergence of new legislation and through the efforts of different industry entities, new standards and guidelines are now available for suppliers to establish and maintain product traceability and to establish receiving inspection and detection protocols. There is no substitute for a healthy supply chain, and distributors play an essential role in the dynamics of the system. At the same time, there is an increased awareness of the need for proper management of electronic waste. Regardless of the nature of the counterfeits, whether cloned, skimmed, or re-branded, counterfeits are dangerous and too expensive to be ignored.

The work presented here by the iNEMI Counterfeit Components Project takes a comprehensive view of the problem by surveying the possible points of entry in the supply chain and assessing the impact of counterfeit components on the industry at various points of use. We then propose a risk assessment calculator that can be used to quantify the risks of procuring counterfeit parts. This calculator is aimed at all segments of the supply chain and will be of interest to component manufacturers, product designers, distributors, loss estimators, industry groups and end users.

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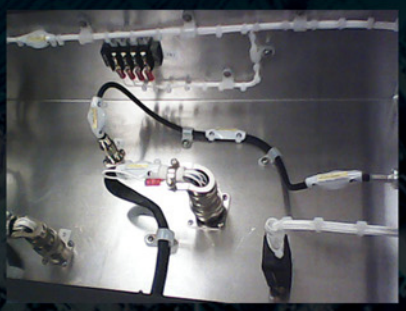

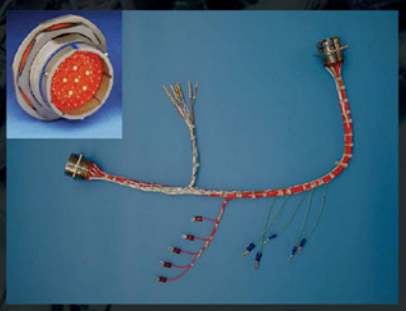

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DEVELOPMENT OF A METHODOLOGY TO DETERMINE RISK OF COUNTERFEIT USE, PART 1 *continues*

Introduction

The existence of counterfeit electronic components, materials and assemblies (hereafter referred to simply as counterfeit components) is not a new phenomenon[1,2]. However, global trade of counterfeit components has recently increased markedly. There are four distinct categories of electronic products in which counterfeit components are most frequently found:

- Manufacturing shortfall and product shortages
- High value products
- Obsolete, discontinued, and legacy devices
- Field installable options or upgrades

The Semiconductor Industries Association Anti-Counterfeiting Task Force[3] has defined counterfeiting as:

- Substitution or the use of unauthorized copies of a device or product
- The use of inferior materials or a modification of performance without notice
- The sale of a substandard component or product in place of an original OCM device or OEM product

The following definition was adopted from "Defense Industrial Base Assessment: Counterfeit Electronics"; US Dept of Commerce—Office of Technology Evaluation; January 2010[4].

A counterfeit is an electronic part that is not genuine because it:

- Is an unauthorized copy
- Does not conform to original manufacturer's design, model, and/or performance standards
- Is not produced by the original manufacturer or is produced by unauthorized contractors
- Is an off-specification, defective, or used product sold as "new" or working
- Has incorrect or false markings and/or documentation

Counterfeit Device Categories

Counterfeit components can be produced, sourced, and distributed in many different ways. The identity of these non-standard parts is usually very well concealed in the present supply chain. Types of counterfeit components can be divided into the following categories.

Cloning

The complete manufacture of a reverse engineered device to have the same form, fit, and function as the original. Devices are produced on low end equipment and will not meet the original reliability requirements. Devices are branded and sold as original component manufacturer (OCM) parts.

Product "skimming," subcontractors, or second source supplier

Manufacturers may over-produce or claim a lower production yield. These extra devices can then be introduced into the market through the broker chains.

Disposal of scrap and rejects

Devices rejected during manufacturing are sent to recyclers to salvage precious metals. Recyclers may certify destruction without scrapping devices and subsequently sell it back into the supply chain.

Devices used as qualification samples

OCMs and OEMs used large quantities of devices to qualify/certify form, fit and function of devices. Accelerated life testing is used to evaluate the functionality and reliability at end of life. Pilfered devices stored for future evaluations can be sold into the supply chain as virgin product. When scrapped, many units may still function making this material a prime target for diversion frauds.

Reclamation and reuse of components

Large quantities of electronic equipment containing working devices are scrapped. Valuable components can be recovered for reuse; however, uncontrolled removal can damage and/or compromise the original electrical performance, reliability and operational life. These compromised parts can then be sold into the supply chain.

Re-branding

Some products have high-performance requirements and must undergo more extensive testing during manufacture (for example, devices that must operate at extreme temperature ranges, such as automotive, aerospace and military applications, or high speed versions of memory modules and processors). Devices with lower specifications that were never tested to the more stringent specifications are acquired at a lower cost, re-marked, and resold at the higher price.

False claims of conformity to industry certifications (e.g., RoHS)

Paperwork is provided stating devices are compliant and old (non-compliant) devices are substituted.

Devices containing embedded malicious malware

Programmable devices are reprogrammed to cause latent damage to products. This problem is most critical in the aerospace, defense, and medical sectors in which counterfeits could render systems inoperative, compromising the safety and security of users. The Office and Large Business Systems sector, in particular, the FSI (financial services institutions) and pharmaceuticals own a lot of embedded servers supporting mission critical activities that could pose serious economic and health risks. The latter may have greater implications and impact on a global crisis via malware.

Situation Analysis

iNEMI segregates the electronics industry into the following product sectors:

- Aerospace and defense
- Automotive
- Medical
- High-end systems (including data communication, networking, voice communication and large business systems)
- Office systems
- Consumer and portable

All of these product sectors are at risk to introduction of counterfeit components; however, each has its own set of requirements for commonly used components. It is not clear that there is a "one size fits all" solution to the

Industry	Sectors	Product Service Time
Aerospace & Defense	Avionics (Civil)	10–20 years
	Avionics (Military)	10–30 years
Automotive	Cars and Trucks	10–15 years (warranty)
Medical	External Equipment	5–10 years
	Internal Equipment	7 years
High-End Systems	Infrastructure Equipment	10–30 years
	Data Center Equipment	7–10 years
	High End Servers	7–10 years
	Industrial Controls	7–15 years
Office Systems	Desktop Computers	24–60 months
Consumer & Portable	Appliances	7–15 years
	Cell Phones	18–36 months
	Laptop Computers	24–36 months

Table 1: Industry Sector Product Service Time.

counterfeit components problem due to the variations in requirements among sectors.

Aerospace and defense

These products require flawless performance on demand, in a multitude of rugged environments, and must sustain this performance over long periods of continuous service. Due to the long service life, systems rely on legacy devices to maintain and expand existing systems. Defense and aerospace systems require extensive testing to meet performance requirements and designs are modified (ruggedized) to meet the thermal, vibration, humidity, salt, fog, and other environmental and reliability requirements associated with DoD platforms. Both need to have a proven supply chain to ensure devices meet security requirements.

Automotive electronics

These applications involve temperature extremes that require improved process controls on the devices. Controllers communicate with sensors and drive relays, injectors, motors, lamps and solenoids. The engine controller is currently the most complex product for harsh-environment automotive electronics. There is also the need for large traces required by high current and power circuitry. Long life, high reliability devices are needed as product warranties extend to as long as 10 years.

Medical products

These include large infrastructure equipment, small stationary equipment, and implantable devices. High reliability is required for life-critical applications such as electronic implants, medical imaging systems, and resuscitation systems. Many of the large systems use legacy devices and need a reliable supply of replacement parts.

High-end systems

These include three major categories: high-performance computing, data centers and communications. The networking and computing hardware has been gaining more common components as the communications becomes an integral part of enterprise computing and as technology advancements enable tighter integration of the communication and computing technologies in commercial business systems. The products represented include mainframe and high-performance computers, the data centers and server farms that house the computers, and communications equipment such as switches and routers and enterprise service provider equipment.

Office systems

These include desktop PCs and other general office equipment (printers, copiers). This sector is cost-sensitive and requires the latest cost effective technologies. The main vulnerabilities relative to counterfeit components are cloning, product "skimming," reclamation, and rebranding.

Consumer and portable

These products are increasing in complexity; however the main drivers are the reduction in cost and increase in functionality while looking at ways of continuously shrinking the system footprint. The sector has the shortest product life, and the main vulnerabilities are similar to the office and large business systems, i.e., cloning, product "skimming", reclamation, and rebranding.

Possible Strategies

Dealing with the different counterfeit device categories will require the use of a variety of strategies. There are different strategies for each category that are most likely to be successful:

Cloning

Legacy and high value components are suspected to be the most dominant. Device serialization may prove to have a beneficial impact on this category of counterfeits.

Product "skimming," subcontractors, or second source suppliers

Place better controls on the documentation with violators identified and prevented from conducting further business.

Disposal of scrap and rejects

Establish better controls on scrap processing

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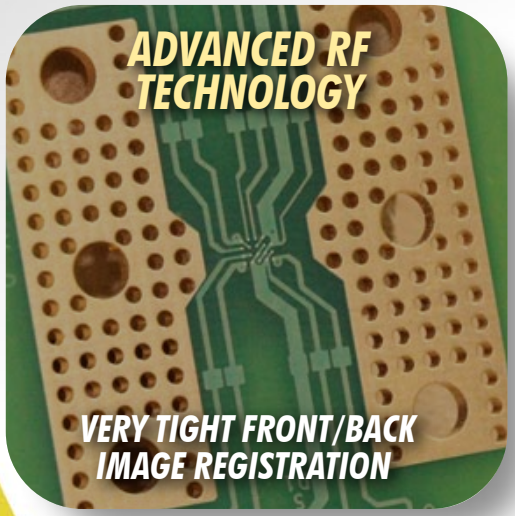

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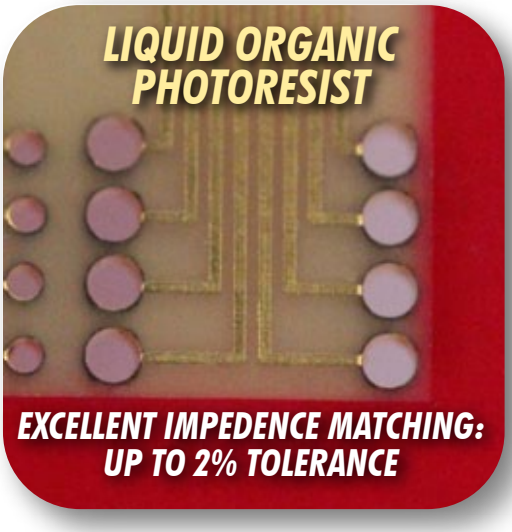

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and handling. Systems designed to more effectively monitor and audit the waste stream may be needed.

Devices used as qualification samples

This form of counterfeit may not be prevalent enough to warrant developing solutions; however, this needs to be verified by an investigation into the extent of this source of counterfeit components.

Reclamation and reuse of components

Some OCMs and OEMs have legitimate operations to reclaim and reuse components using strict procedures to ensure that quality and reliability have not been compromised. Verification procedures for legitimate devices need to be established.

Rebranding

Inspection, inspection, inspection (mechanical, electrical, etc.) as well as lot testing.

False claims of conformity to industry certifications (e.g., RoHS)

Incoming inspection should be required, since counterfeiters are providing false documentation. Traceability and serialization may help to reduce this category of counterfeit devices.

Devices containing embedded malicious malware

This problem is most critical in the aerospace and defense and medical sectors in which counterfeits could render systems inoperative, compromising the safety and security of users. The use of all possible approaches to counterfeit reduction is warranted for this sector.

Initial Work

The first phase of iNEMI's Counterfeit Components Project is broken into several high-level tasks. The first three tasks (on which this paper is based) were:

Task 1: Identify and summarize any related research or development within the industry and academic communities.

Task 2: Review and tabulate successes that have worked in the past (best known methods/best known practices).

Task 3: Develop a methodology to evaluate or assess the risk of counterfeit use.

In addition to the tasks specifically identified in the project statement of work, the team also:

- Focused on those attributes that are of most value to the supply chain and participating project members, and that are applicable to multiple spaces across the supply chain.
- Identified and developed methodologies with associated metrics to assess the overall extent of the counterfeit problem in the electronics industry. The outputs will enable iNEMI members to assess the risk of counterfeit use in their respective industries, the risk of untrusted sources of supply in that industry and understand the total cost of ownership associated with those risks.

Note: The methodologies and strategies apply to all phases of the manufacturing cycle and supply chain. Not only do counterfeit components have a serious impact on the OCM, but impact all downstream users from the legitimate component brokers to the OEMs that integrate these components to the end user. Metrics to assess the overall extent of the problem and anti-counterfeiting will be identified for all phases.

The team began by identifying the key sectors of the electronics supply chain (Figure 1).

- Wafer manufacturers
- Chip manufacturers
- Board manufacturers
- System manufacturers
- After-market sales and refurb support
- Disposal/Recycle

The electronics supply chain was then broken into a series of manufacturing "cluster maps" to help visualize how materials, parts, assemblies, and waste move, and identify the key players in each manufacturing sector (Figure 2).

Figure 2 highlights two principle flows between the major electronic manufacturing

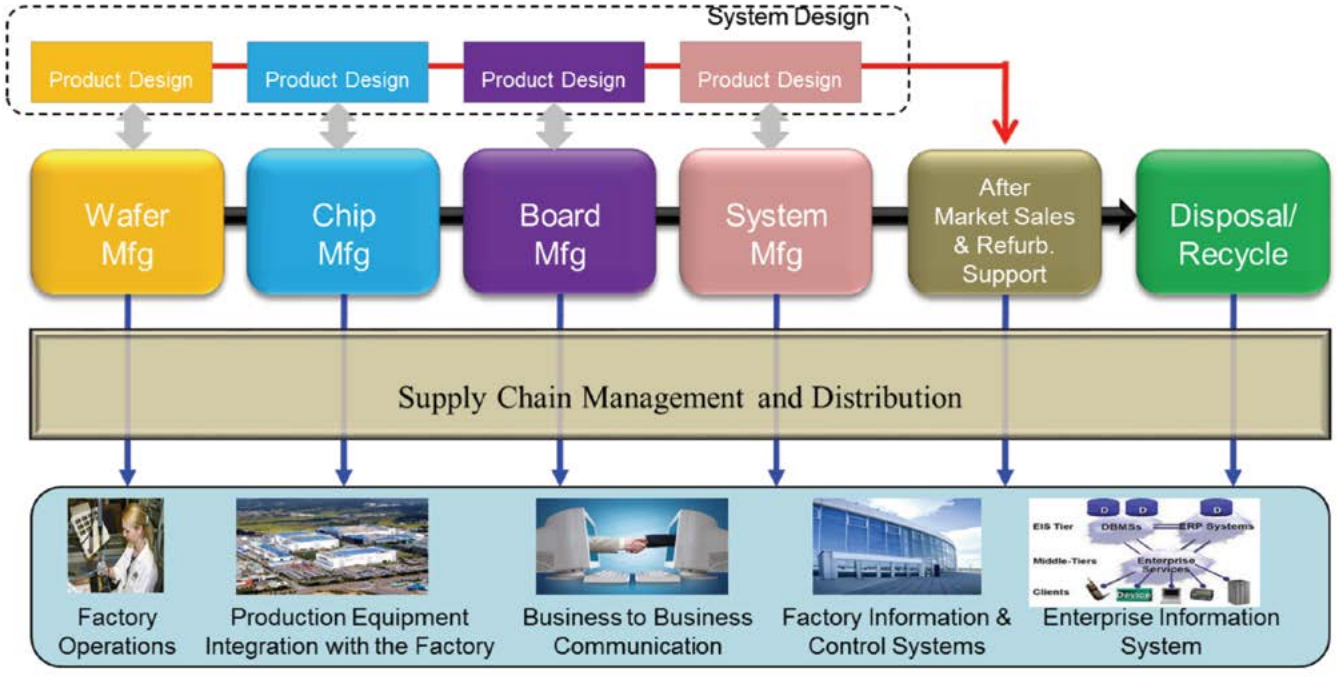

Figure 1: Electronic manufacturing workflow diagram[5].

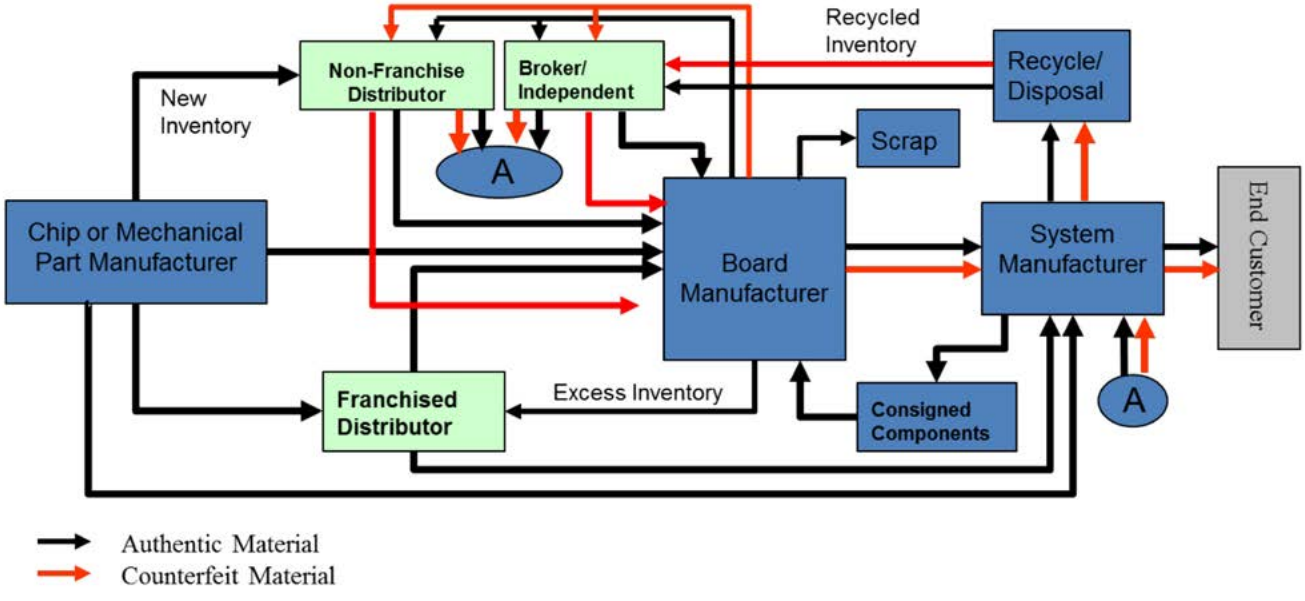

Figure 2: Board manufacturer cluster.

workflow blocks: the "authentic" and "counterfeit" material flow paths. The authentic material flow pathways indicate peer-to-peer connections where the board manufacturer has established strong agreements and has policies in place to prevent corruption of their supply stream. These measures generally provide a high confidence in the supply chain and feature traceability of the pedigree of electronic components.

The counterfeit material flow pathways highlight potential opportunities for breaching into the supply chain and corrupting traceability and pedigree of the electronic components. The risk of infiltration using one of these pathways increases when product shortages occur. Risks can also increase as new participants enter the networks to service growing demand. For example, as green manufacturing increases demand for recycling, new players rushing to capture market share may overlook security protocols. Also consider how criminals are well versed at pretending to be new participants.

With the completion of the cluster maps for the electronics supply chain, the team was able to begin work on the task of developing a methodology for assessing the risk of counterfeit use.

Developing a Risk Assessment Calculator

1. Premise of the Spreadsheet/ Assumptions

Examining the cluster maps for the different segments of the electronics supply chain, the team decided that the risk of counterfeit use was based on four key elements:

- The profile of the product in question
- The inputs or characteristics of the supplier and supply line
- The processes used on the product to deter counterfeit use
- The outputs or channel characteristics

The team's goal was to provide a quantitative methodology on risk assessment built on these four key elements that any company could use to rate their product.

2. Structure of the Spreadsheet/ Rating Scale

2.1) Product profile

The profile of the product in terms of demand for that product and where it is on the life cycle are key determinants in the risk of counterfeit use. The higher the demand for a product, the more attractive it becomes for counterfeiting. If a product is in high demand and also the original supply is near end of life, then the product profile risk of counterfeit is highest.

2.2) Inputs

The profile of the supplier and the history of that supplier in terms of counterfeit incidents, the clarity of the supply line, and the anti-counterfeit controls used by the supplier are key factors in determining the risk of counterfeit use. For example the inputs risk is highest where the supplier is a broker with no controls who has previously supplied confirmed counterfeit product and cannot confirm the origin of the product in question. Conversely, the inputs risk is lowest when the product is coming directly from the OCM, there are strong counterfeit mitigation procedures in place, and there is no known history of counterfeit supply.

2.3) Process

The processes required to produce the product, the ease of counterfeit detection of that product and the counterfeit controls used in the original product are also key factors in determining the risk of counterfeit use. Where a product requires a large capital investment is easy to authenticate and uses a high level of counterfeit controls, the process risk of counterfeit use is low. On the other hand, where there is little or no investment required to make the product, validation is difficult, and there are no special counterfeit controls in place, the process risk of counterfeit use is highest.

2.4) Outputs

The key factors in the case of the outputs risk are the sales channel used, the handling of excess inventory, prototypes, reworks and scrap and the customer profile. The outputs risk is at its highest when the sales channel is unknown; when there is no control or traceability on excess inventory, prototypes, reworks or scrap; and where the end customer is unknown. In contrast, where the end customer is well known, the sales channel is well defined and the excess/prototypes/reworks and scrap are well controlled, the outputs risk is lowest.

3) Examples of Calculation

Rating each of the four key risk elements above, the methodology gives an overall score for the product in question. FLASH is a well-known target for counterfeiters, making it

DEVELOPMENT OF A METHODOLOGY TO DETERMINE RISK OF COUNTERFEIT USE, PART 1 *continues*

Risk of Counterfeit Use v3.1

Methodology to Evaluate or Assess the Risk of Counterfeit Use

CF = Counterfeit

Profile		Input					Process				Output							
Select or Enter Product Type	Demand / EOL	Supplier	Supply Line	Mitigation & Controls	Supplier History	Input Score	Ease of Counterfeit	Ease of Detection	Counterfeit Controls	Process Score	Sales Channel	Excess Inventory & Prototype	Customer	Rework	Ease of Fraudulent Reuse	Disposal	Output Score	Total Rating
ASIC	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2
FPGA	3	3	3	3	1	27	3	3	3	27	3	3	3	3	1	3	243	579
CPU	5	5	5	5	3	375	3	3	5	45	3	1	3	3	1	3	81	1,874
Thermal System Controller	1	5	3	1	1	15	3	3	3	27	5	5	5	5	1	5	3,125	1,913
Tantalum Capacitor	3	5	3	3	5	225	3	5	5	75	5	5	5	5	1	5	3,125	6,356
DRAM	3	1	5	3	3	45	3	3	3	27	3	3	3	3	1	3	243	620
FLASH	5	5	5	5	5	625	5	3	5	75	5	5	5	5	2	5	15,625	49,594
Hard Drive	3	1	1	1	1	1	5	3	2	30	4	4	5	3	1	1	240	524
	0	0	0	0	0		0	0	0		0	0	0	0	1	0		

Please select the rating from the table below that best corresponds to the description for that rating.

Rating = 1	Product has Low demand and is not EOL	OCM	Direct from OCM	Supplier has Strong Mitigation & Controls	No known Counterfeit Incidents	Very difficult to counterfeit; requires factory access or capital investment >$1M	Easy to detect, e.g. by check of packaging, documents, labels, history	Uses Unique Overt and Covert Controls & Identifiers that are easy to validate	Direct- OCMs/ Manufacturers /Suppliers	Minimal Excess inventory. Very limited prototyping/tight OCM security and traceable records that are digitally signed/encrypted and/or independently audited.	Direct to OEM	In-house only under tight controls in certain designated areas, tight security and traceable records (signed / encrypted and/or independently audited)	Exponential factor from 0 to 2; 0 being impossible to reuse to 2 being very easy or trivial to reuse. This exponent modifies the Disposal rating chosen.	In house only, on site physical destruction, traceable records (signed / encrypted and/or independently audited)	1
Rating = 2	No 2 rating	No 2 rating	No 2 rating	No 2 rating	No 2 rating	Requires major equipment / facilities such as wire bonders and laser markers, >$100k capital	Possible by optical inspection	Unique Overt or Covert Controls / Identifiers that are easy to validate	Known channel: Franchised/ Authorized Distributors	Excess and prototype inventory under tight controls and security	Trusted Sales Rep and Franchised Distributor to OEMs	In-house + vendor, under tight controls and security		In house + vendor physical destruction, traceable records, third party certification*	2
Rating = 3	Product has Low demand and is EOL or high demand and not EOL	Authorized Distributor	Multiple known suppliers	Some evidence of mitigation / controls	Counterfeit supply suspected	Requires moderate equipment and capital ($10k-100k)	Possible by routinely applied 2D X-ray inspection, decapsulation	Overt and Covert Controls / Identifiers but validation not easy	Limited - OEMs/ CMs and some use of Brokers	Significant inventory but under tight controls and security	Trusted Sales Rep and Unfranchised distributor to CMs	Primarily offsite vendor based, with controls and security.		Offsite vendor, with controls and records for physical destruction	3
Rating = 4	No 4 rating	No 4 rating	No 4 rating	No 4 rating	No 4 rating	Needs simple equipment such as sand blasters and ink printers (<$10k capital)	Requires advanced analytical tactics, i.e. XRD, CSAM, 3D X-ray	Some overt controls / identifiers but validation not easy	Very Limited - Primarily Reputable Independent Distributors /Brokers	Some controls in place. No traceable records. No security	Independent Distributors, dependent on end user oversight.	Offsite some controls in place. No traceable records. No security		Offsite vendor, some controls and records. No proof of physical destruction	4
Rating = 5	Product has High demand & is EOL	Broker or Ind. Distributor	Supply line not defined / clear	No evidence of mitigation / controls	Counterfeit supply confirmed	Easy - little / no investment required (<$1000)	Difficult to detect; nearly indistinguishable from authentic	No special controls in place	No control / Unknown- Unknown Independent Distributors/Brokers /Unknown Sources	Excess and prototype inventory not controlled	Customer not defined, open market.	Offsite Vendor, no controls and no traceability		Vendor or no vendor. No controls, no records	5

Figure 3: Methodology to evaluate risk of counterfeit use.

a good test of the methods developed here. Based on the values used by the team for each of the factors, the overall rating is very high indicating that our methodology gives the risk of counterfeit use as very high. In contrast the rating for a typical ASIC device is very low, i.e., the risk of counterfeit use is low. These results serve to validate this method or risk assessment.

At this stage, the methodology is useful for comparative purposes only. The team would like to encourage iNEMI members to test the methodology and provide feedback to the team. The wide range of data collected would enable the team to provide guidelines in the form of levels of risk of counterfeit use. For example, an overall rating of 1 ~ 500 means the risk of counterfeit use is very low and no additional actions are recommended. A rating of 5000 ~ 10,000 means the risk is very high and immediate action needs to be taken in the high-risk areas.

When materials are purchased through the distribution channel, there are ways to minimize exposure to suspect, fraudulent, or counterfeit parts passing undetected through the distributor to you. SAE International Standard AS5553A[6] identifies a series of controls and certifications to ensure detection and prevention of counterfeit components. You can select a dis-

tributor that has been audited by a third-party certification body and is compliant with:

a) AS6081 (Counterfeit Electronics Parts; Avoidance Protocol, Distributors)[7]
b) AS6301 (AS6081 Verification Criteria)
c) ISO/IEC 17025 certified for counterfeit testing

For distributors to be compliant with these standards, all materials must be inspected, tested, and certified as non-counterfeit materials before they can resell the parts. This level of testing will add additional cost to the materials, but the risk will be significantly mitigated. The level of testing and controls required from the distributor selected can be balanced in terms of the cost vs. risk avoidance benefit for your business needs.

For suppliers outside the authorized distribution channel, there are qualitative means to better assure end customers that your organization is providing genuine materials. Chief among these is to always know your source of supply which can be achieved by tracking and recording problems to provide a historical record of past transactions. This is particularly important for high-volume suppliers.

In addition, understanding parts and associated package types is a must. This affords the purchaser the ability to recognize the most blatant attempts at counterfeiting. This may lead to a limiting of drop shipping parts from their original source to an end customer with no handling by the intermediary party. There is an associated cost impact to inspect parts; however, it may be a necessary cost of doing business, in particular when there are unknown providers in the chain. **SMT**

Click here to read Part 2 of this article in the I-Connect007 Daily Newsletter.

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Key Surface Properties of Complex Oxide Films

Better batteries, catalysts, electronic information storage and processing devices are among the benefits of a discovery made by Oak Ridge National Laboratory scientists.

The findings, published in Nanoscale, showed that key surface properties of complex oxide films are unaffected by reduced levels of oxygen during fabrication—with implications for the design of functional complex oxides used in a variety of consumer products, said Zheng Gai, a member of DOE's Center for Nanoscale Materials Sciences at ORNL.

"With these materials being a promising alternative to silicon or graphene in electronic devices, the ever-decreasing size of such components makes their surface properties increasingly important to understand and control," Gai said.

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Ensuring Supply Chain Reliability and Integrity

by Richard Ayes
I-CONNECT007

It's become standard procedure for companies to claim a worldwide reach. But with operations in Canada, Silicon Valley, China, Hong Kong and Mexico, EMS provider SMTC Corp. is truly a global enterprise. In an interview with SMT Editor Richard Ayes, Corporate Value Engineering Manager Brian Morrison and Vice President of Account Management Frank Gerber discuss SMTC's strategies to ensure that the devices that enter their supply chain meet the high-reliability standards in electronics assemblies. They also highlight how the company adapts to the changes amid the ever-evolving requirements in the different sectors that they serve, as well as the different security issues that a major EMS provider like SMTC must address.

SMT: IPC-A-610 and IPC-J-STD-001 are widely believed to ensure high reliability of electronic assemblies. Certain EMS providers comment that they drive up costs and make products less reliable. What is your opinion?

Brian Morrison: We believe that IPC-A-610 and IPC-J-STD-001 provide the necessary guidelines to achieve highly reliable electronic assemblies based on the underlying theory that all products are designed to achieve target conditions. Not all designs are created equal and there are always exceptions, but these exceptions can almost always be associated with an underlying DFX issue or critical design criteria that create a non-ideal condition. These situations commonly drive up rework to attempt to achieve target conditions and as a result lower reliability. Any high-reliability product starts with a

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design taking into consideration both performance and manufacturability. More and more companies now are seeing the value in engaging with their EMS partner in reviewing and providing feedback to ensure DFX is a key part in achieving IPC standards and high reliability.

SMT: What precautions ensure the integrity and authenticity of bought-in components? Do your customers specify what sources you must use, or leave that responsibility with you?

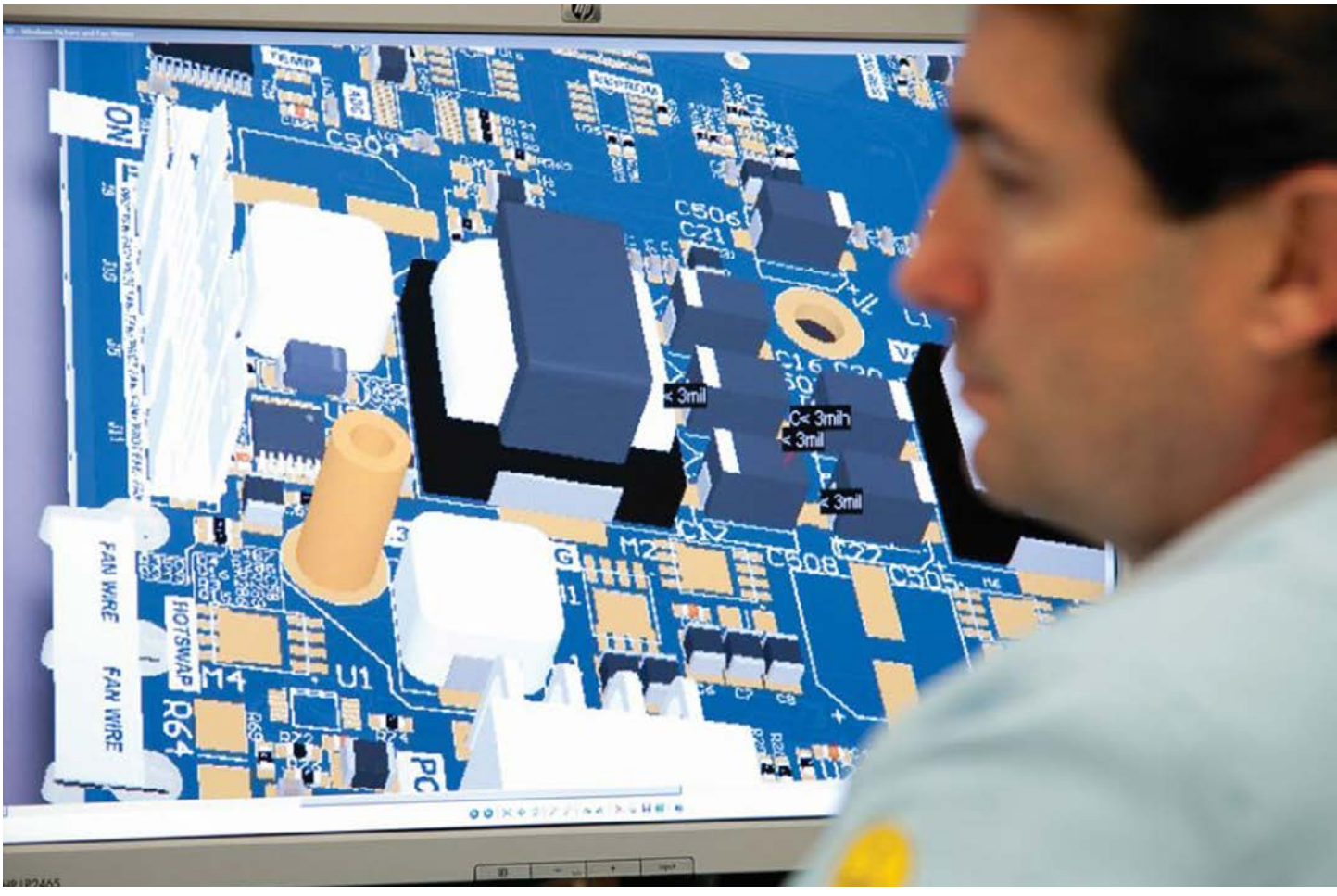
Morrison: SMTC only purchases from the customer approved manufacturing list (AML) through either direct or distribution and require all of our suppliers to follow SMTC global procurement policies. In cases of material shortages, SMTC will purchase only from our approved brokers. In order to be considered an SMTC approved broker, the broker must sign up for 100% liability against counterfeit material and a minimum liability of $3 million, covering all aspects of material cost (both direct and indirect). SMTC's sourcing of components is a global activity managed through our global procurement, ensuring all sites are executing to the same copy-exact policies and procedures so that integrity is maintained.

To complement our procurement policies, SMTC receives product change notices (PCN) for all approved AML including counterfeit/failure notices to alert and action potential material issues. Upon receipt of incoming material, all manufacturing sites employ a robust receiving inspection that incorporates material traceability and ties liability to the supplier, enabling material to be contained and purged effectively and quickly. Through this stringent sourcing practice, to date, SMTC has never received counterfeit material.

SMT: Certification can cover a wide range of issues including incoming components and materials, operator training, manufacturing processes, compliance with legislation, conformity with product specification, and many others. How does an organisation as geographically diverse as SMTC deal with certification? Is it handled locally or globally?

Morrison: SMTC recognizes that training is a critical part of our overall strategic business plan to meet and exceed the expectations of our customers, by producing products with outstanding quality and reliability. At SMTC, we embrace the importance of international standards certification including ISO and IPC and ensure all sites are certified to these standards. SMTC utilizes a Global Copy Exact Philosophy to operate our facilities in a standardized way, utilizing a best practice approach that provides flexibility to manufacture products locally or globally and enables seamless global product transitions. All sites follow similar approved processes, equipment, materials and documented procedures per ISO 9001 and ISO 13485 international quality standards or regulatory requirements where applicable. Any changes to procedures are processed and approved globally through a corporate ISO team and distributed to sites for certification.

Being a global company, it is the responsibility of each site to translate the documents, software, formats and other activity to the language used at each site in order to facilitate understanding and certification. New processes, equipment and materials can be evaluated at individual sites, and if the new method is deemed "best practice," then it is incorporated at each site over time, allowing time for implementation and certification.



SMT: It is clear that SMTC goes to great lengths to understand the dynamics of key market areas. Your website lists industrial, computing, communication, consumer, medical and renewable energy. How do you adapt to the changes that influence your customers' businesses?

Frank Gerber: SMTC has an account management organization that gets deeply involved with our customers. The account manager is a senior level individual that builds relationships across the key functional areas within the customer and gains an in depth knowledge of the customers' business. They facilitate relationships and exchanges at the executive level of both companies. Our key strengths are in our ability to not only meet the needs of our customers by being an exceptional manufacturing partner, but by vertically integrating our services to help better understand our customer's business model and adapt to their changing needs. Program management plays a key role on managing expectations of the customer and ensuring that our strategic plan. On a quarterly, basis we engage with our customers on a business review to ensure both sides are meeting expectations and there is a clear plan to address changes to that plan.

SMT: What are the main security issues that a major EMS provider like SMTC must address?

Gerber: An EMS provider must address a number of different security issues for our customers. Probably, the biggest security concern of an OEM customer is financial. The customer wants to know that the EMS provider is financially sound and has a strong balance sheet so they are assured that the EMS can make the investments required, buy the inventory and pay the suppliers to fulfill the demand. Our customers also have a significant concern regarding the control of our customer intellectual property as

we live in a competitive market and they trust the security of their designs and products to SMTC. SMTC follows stringent SOX (Sarbanes-Oxley Act) compliancy protocol with limited and controlled access to the outside, and does not allow direct network access to any internal systems to ensure the security of information is maintained.

Sharing of information with suppliers is something that cannot be avoided, and we have maintained a supplier management program that starts with a Non-disclosure Agreement outlining SMTC policies on sharing of confidential information. Suppliers are closely monitored and approved through global procurement to ensure only suppliers that have been selected can be used.

In certain applications, very high security is required for payment systems, which require key injection. In those circumstances, SMTC works closely with our customers and security representatives to ensure we comply with all regulatory requirements and will provide dedicated locked control rooms and select authorized personal access only to ensure the highest level of security.

SMT: What specific value-added service on a specific end-application or market sets SMTC and Idneo Technologies apart from its competition?

Morrison: Our partnership with Idneo provides our customers a unique, integrated and seamless new product introduction experience from concept to full production not commonly available from a tier-2 EMS. Through our Technical Services Group and Transition Management, a customer can engage with SMTC on a design concept and achieve earlier design engagement from both design and manufacturing to ensure the design not only meets the requirements of the customer, but is designed to meet both Idneo and SMTC DFX requirements, for a seamless introduction into production.

SMT: Any final comments?

Brian Morrison: Commonly, EMS engagements can be disconnected and can involve multiple parties including third-party design partners, customer design teams and other manufacturing entities. In general, design and manufacturing parties will have their own set of goals, and development is typically isolated from one another. Design rules and requirements can vary significantly and commonly cause conflict, which can drive up costs or require expensive re-design costs. To combat this issue, best practices typically involve early design involvement with all parties to truly ensure all requirements are taken into consideration—where 80% of the product cost is defined. In reality, this can be difficult and can add lead time to launch products, which increases in complexity with the number of parties involved. Engaging with one integrated supplier that can take a product through all stages of the design with an integrated DFX review process provides the platform for innovators to advance ahead of their competition and significantly decreases time to market. **SMT**

ABOUT THE INTERVIEWEES

As Corporate Value Engineering Manager, Brian Morrison B.A.Sc., P.Eng, is responsible for working collaboratively with customers to reduce cost and improve performance in order to protect and enhance overall product value through the NCI/NPI process. Morrison leads the Technical Services Group that provides a broad range of design services, capabilities and partnerships covering all aspect of design from layout, DFX, development through to production release and continuous improvement.

As Vice President, Account Management of SMTC, Frank Gerber is responsible for establishing, maintaining and growing relationships with our customer base on a global basis. Prior to joining SMTC, Gerber held various technical, business management and customer relationship management positions with IBM, Celestica, C&D Technologies and Murata.

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Improving Reliability Through HALT and HASS Testing

by Mark R. Chrusciel
CINCINNATI SUB ZERO

SUMMARY: HALT and HASS technology use a combination of accelerated stresses to expose product flaws early in the design and manufacturing stages (often at board level), improving product reliability and customer confidence. This article will discuss why companies are succeeding with HALT and HASS.

HALT and HASS are used to uncover many of the weak links inherent to the design and fabrication process of a new product, as well as during the production phase to find manufacturing defects that could cause product failures in the field. The types of HALT and HASS chambers available in the market, along with the equipment capabilities, will be reviewed. We will also explore how they used for detection of flaws in design, making the product more rugged and reliable. These capabilities are essential to precipitation and detection of product defects.

Highly accelerated life test (HALT) is a method aimed at discovering and then improving weak links in the product during the design phase. Highly accelerated stress screen (HASS) is a means for finding and fixing process flaws during production. Both techniques employ stresses far beyond the normal operating condition. The process uses discovery testing in which problems are found by testing to failure using accelerated stress conditions. HALT is a discovery test as opposed to a compliance test. The goal is to find problems, remove them, and improve the product making it more robust.

The acronym HALT was coined by Dr. Gregg Hobbs in 1988 after he used the term "design ruggedization" for 18 years. In these tests, every stimulus of potential value is used to identify weak links in the design and fabrication processes during a product's design phase. These stimuli may include vibration, thermal cycling, burn-in, voltage, humidity, and whatever else will expose relevant weaknesses (including stresses that will not occur in the real world if they generate real-world failure modes). The

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stresses are not meant to simulate the field environments, but to find the weak links in the design and processes using only a few units and in a very short period of time. The stresses are stepped up to well beyond the expected field environment in order to obtain time compression in identifying design weaknesses. HALT has, on many occasions, provided substantial MTBF gains, from 5 to 1,000 times. Even when used without production screening, HALT has reduced time to market substantially and also reduced the total development costs.

HASS uses accelerated stresses (beyond product specifications and as determined appropriate by earlier HALT testing) to detect product defects in manufacturing production screens. The accelerated stresses of the HASS program shorten the time to failure of defective units and therefore shorten the corrective action time and the number of units built with similar flaws. Many issues caused by process changes after HALT screening were previously seen only as early life failures in the field. With an appropriate HASS implementation, these defects can now be detected and corrected prior to shipment.

HASS is generally not recommended unless a comprehensive HALT has been performed, since without HALT, fundamental design limitations and flaws will restrict stress levels that can be applied in the HASS process. HASS can generate significant savings in screening costs as less equipment (shakers, chambers, monitoring systems, power and liquid nitrogen) is necessary due to time compression in the screening process. As with HALT, HASS is discovery testing as compared to compliance testing.

The HALT Process

In HALT, every stimulus of potential value (temperature, all-axis vibration, humidity, UV, radiation, etc.) can be used under accelerated test conditions during the development phase of a product to find the weak links in the design and fabrication processes. Accelerated stresses in combination (e.g., high-temperature ramp rates and all-axis vibration levels together) are necessary to compress or minimize the time to failure. Again this method is aimed at discovering and then improving weak links in a product

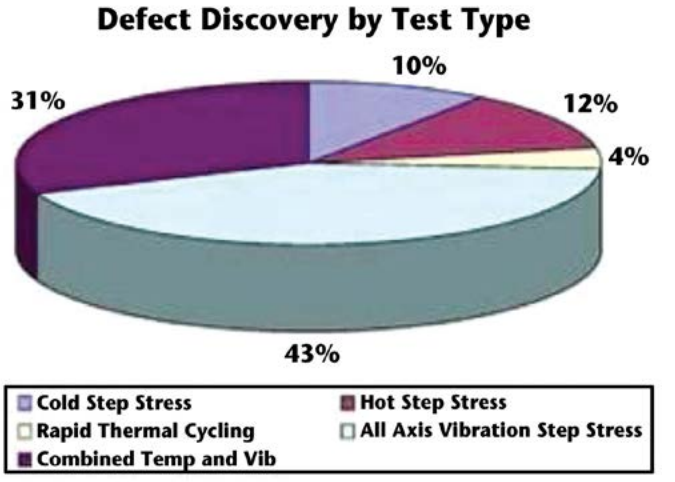

Figure 1: Defect by test type. (Courtesy of Chuck Laurenson, Parker Hannifin.)

during the design phase. This is a discovery test whose goal is to identify problems.

Figure 1 shows where design flaws were discovered during the HALT process and why all-axis vibration is important.

Therefore, 74% of the flaws would have been missed without simultaneous, all-axis vibration. By stressing the product beyond its design specification, operational and destruct limits can be determined, and decisions can be made regarding how to increase these margins. Each weak link provides an opportunity to improve the design or the processes, which will lead to reduced design time, increased reliability, and decreased costs. Used properly, HALT compresses this design cycle while providing a significantly more reliable and mature product at introduction. Studies have shown that a six-month advantage in product introduction can result in a lifetime profit increase of up to 50% for the market mover[1].

Basic Steps in the HALT/HASS Process

The term precipitation means the changing of a defect which is latent or undetectable into one that is patent or detectable. A poor solder joint is such an example. When latent, it is probably not detectable electrically unless it is extremely poor. The process of precipitation will transpose the flaw to one that is detectable, that is, cracked. The stresses used for the trans-

formation may be vibration, combined with thermal cycling and perhaps electrical overstress. Precipitation is usually accomplished in HALT or in a precipitation screen.

Detection means to determine that a fault exists. After precipitation by any means, the defect may become patent, that is, detectable. Just because it is patent does not mean that it will actually be detected, as it must first be put into a detectable state. Assuming that we actually put the fault into a detectable state and that the built-in test or external test setup can detect the fault, we can then proceed to the most difficult step: failure analysis.

Failure analysis allows us to determine why the failure occurred. In the case of the solder joint, we need to determine why the joint failed. If conducting HALT, the failed joint could be due to a design flaw, that is, an extreme stress at the joint due to vibration or possibly due to a poor match of thermal expansion coefficients. With HASS, the design is assumed to be satisfactory (which may not be true if changes have occurred) and, in that case, the solder joint was probably defective. The manner in which it was defective and why it was defective must be determined in sufficient detail to perform the next step: corrective action.

Corrective action means to change the design or processes as appropriate so that the failure will not occur again. This step is absolutely essential for success. In fact, corrective action is the main purpose of performing HALT or HASS. One of the major mistakes in the industry is that manufacturers "do HALT" and discover weaknesses and then dismiss them as due to overstress conditions. It is true that the failures occurred sooner than they would in the field due to the overstress conditions, but they would have eventually occurred in the field at lower stress levels.

Corrective action must be verified to determine that the product is really fixed and that the flaw that caused the problem is no longer present. The fix could be ineffective or there could be other problems causing the anomaly that are not yet fixed. Additionally, another fault could be induced by operations on the product, and this necessitates a repeat of the conditions that prompted the fault to be evident. One method of testing a fix during the HALT stage is to perform HALT again and determine if the product is at least as robust as it was before. It should be somewhat better. If in the HASS stage, performing HASS again on the product is in order. If the flaw is correctly fixed, then the same failure should not occur again.

The last step of the six is to put the lesson learned into a database for later use. Companies that practice correct HALT and utilize a well-kept database soon become very adept at designing and building very robust products with the commensurate high reliability[1].

Figures 2 and 3 compare HALT and HASS chambers.

Figure 2: HALT/HASS chamber.

Figure 3: HALT testing.

There are many factors that need to be considered when evaluating a HALT chamber purchase. One of the most obvious criteria is to select a chamber big enough to handle the size of your DUT. Other factors to consider are the high and low vibration limits of the chamber and the characterization of the table (how well the vibration is distributed). A safety door interlock system should be in place to prevent the door from being open when liquid nitrogen is flowing into the chamber. It would also be useful to have multiple cable ports for connections to your DUT, and front and rear doors on the larger units. You will also want to check out the nitrogen and compressed air usage along with their sound levels.

Liquid nitrogen is the predominant cooling media used in HALT testing, so you need to consider how many tests you will be running per day, per month, to determine the amount of liquid nitrogen required (you do not want to run out during a test). You may then contact a gas supplier and decide on the most cost-effective solution. If you currently have a source of liquid nitrogen in your facility, you will need to plan the chamber's location. Running the vacuum-jacketed connection lines from the source to the chamber is very expensive (approximately $200/running foot). It is also a good idea to put an oxygen sensor in your lab, to let you know if too much nitrogen escapes into the lab.

An ideal situation is to run your DUT on a chamber before you make a purchase decision. Many chamber manufacturers will have a chamber available for your use, and I would suggest that you take them up on their offer. This will also give you an opportunity to determine what fixtures are necessary. The manufacturers can also guide you through the first steps in setting up your HALT test.

Using fixturing that does not transmit the stress to the product under test can be a problem because sufficient levels of stress never reach the product. Three examples are:

1. Using a vibration fixture that will not transmit the frequencies associated with critical modes of vibration of the product under test or isolates the mid and high ranges.
2. Using a thermal fixture that does not transmit the conditioned air to the product such that the product can be rapidly changed in temperature over a broad range.
3. Using electrical overstress and having some circuitry such as the lightning arrestor circuitry bleed off the high voltage before it gets to the internal circuits.

If the stress does not reach the product, then nothing has been accomplished[2].

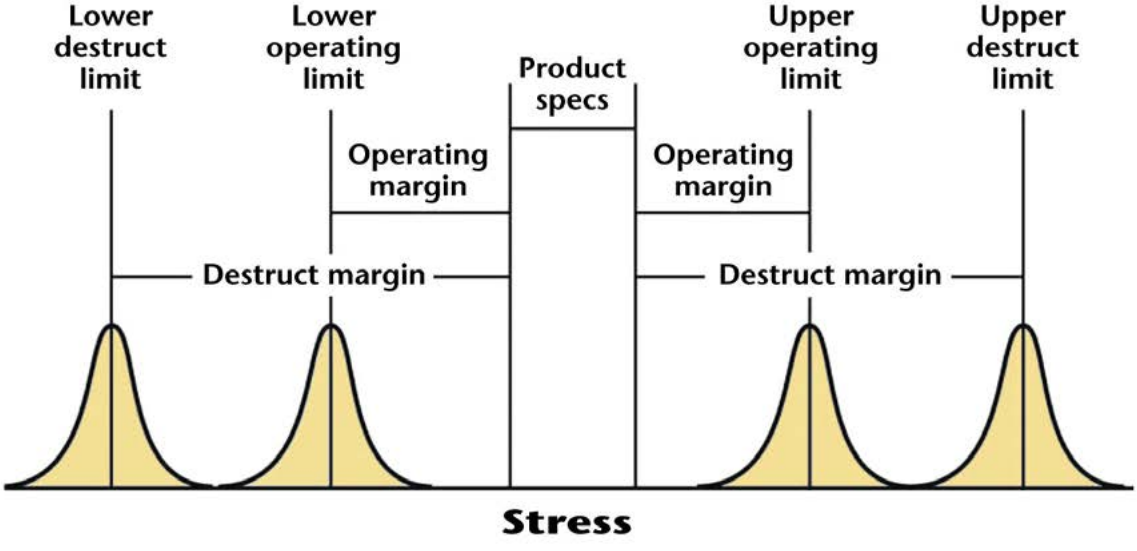

Figure 4: Operating and destruct limits.

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The Basic Steps of HALT

Determination of operational and destruct limits for temperature and vibration is an important part of HALT. Some companies (such as aerospace firms) do not test to destruction due to the high costs of test units. Some engineers incorrectly think that HALT consists only of determining operational and destruct limits. However, operation margins are important indicators of product robustness, and therefore reliability. Figure 4 shows the operating and destruct levels relative to the product specification.

Usually the starting point for HALT testing is to begin with each stress applied separately, first in a step-like fashion and then in combination. IPC-9592A Requirements for Power Conversion Devices for the Computer and Telecommunication Industries makes the same recommendation. A typical progression of HALT would be:

- Cold thermal step stress (see IPC-9592A)
- Hot thermal step stress
- Rapid thermal shock stress
- Vibration step stress
- Combined thermal and vibration stress

You may also uncover some intermittent failures that the traditional HALT method may not uncover. Experience has shown that modulated six-axis vibration combined with slow temperature changes exposes many flaws that could not be found otherwise. Modern HALT and HASS equipment will easily do the modulation, and it increases detection efficiency by a factor of ten or more in many cases. It has been repeatedly demonstrated that patent defects could not be found until the modulated excitation was done. Many times, 100% of the patent defects cannot be found without it. This is especially true for cracked plated through-hole solder joints and cracked surface mount solder joints. Very low vibration levels are important, if not essential[2].

Since HALT and HASS may identify failure modes using "unrepresentative" stress conditions, it is easy for engineers to ignore important product improvement opportunities. Corrective action should also be verified, which may require a re-HALT to verify that a problem has indeed been solved (and that new problems were not introduced)[3].

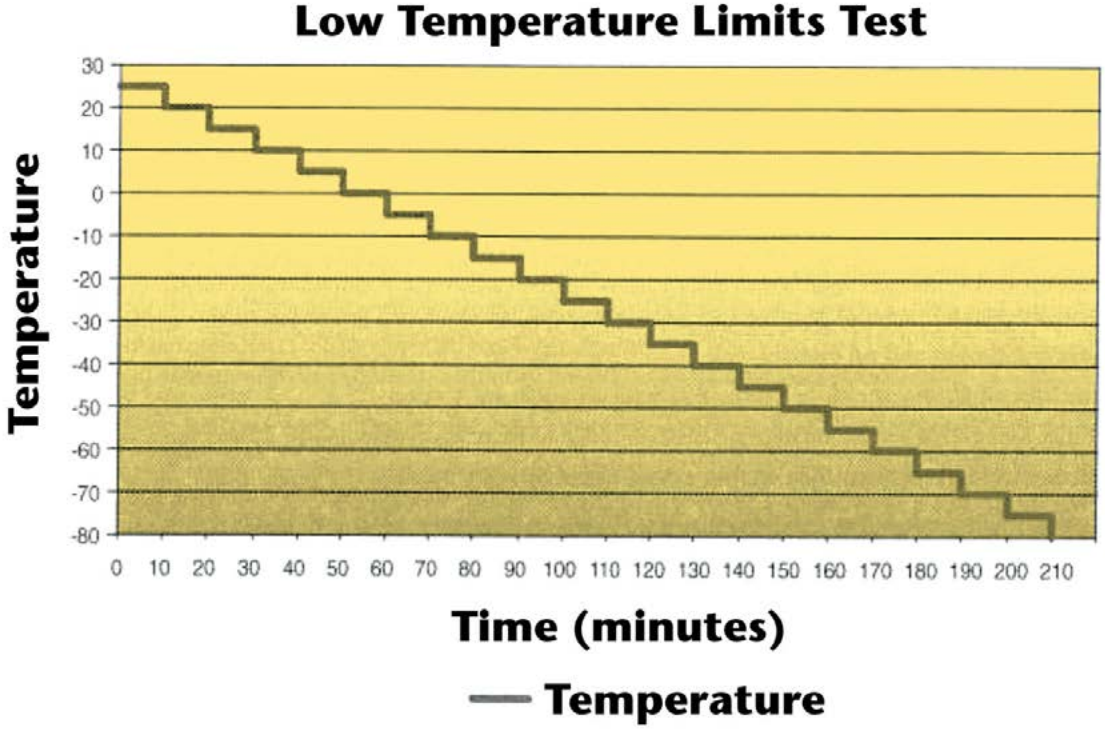

Figure 5: Low-temp test graph.

Conclusion

Every weakness identified in HALT offers an opportunity for improvement. Larger margins translate into high reliability and that can result in improved profit margins. Today, HALT is required on an ever-increasing number of commercial and military programs. Many leading companies use HALT and HASS techniques successfully; however, most of the leaders are being quiet about it because of the phenomenal improvements in reliability and vast cost savings attained. The basic philosophy is, "Find the weak spots however we can and then make them more robust."

Correct application of these techniques is essential to success, and there are many incorrect sources of information on the techniques today. Used consistently, completely and correctly, HALT and HASS always work to the benefit of the manufacturer and end user. A typical ROI for the techniques was 1,000:1 some 20 years ago and, with the improved techniques and much better equipment available today, we can do much better. This is why the real leaders do not publish[1]. **SMT**

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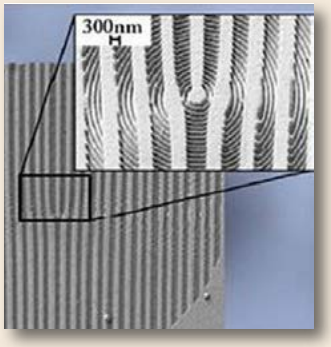
Mark R. Chrusciel is director of global sales for Cincinnati Sub Zero. He has served on the board of the Accelerated Stress Test and Reliability Workshop for the last five years, and he is a senior member of the IEST.

"Groovy" Hologram Creates Strange State of Light

Applied physicists at the Harvard School of Engineering and Applied Sciences (SEAS) have demonstrated that they can change the intensity (brightness), phase (two waves interfering with one another to either strengthen or cancel each other), and polarization (direction of light vibrations) of light rays using a hologram-like design decorated with nanoscale structures.

As a proof of principle, the researchers have used it to create an unusual state of light called a radially polarized beam, which—because it can be focused very tightly—is important for applications like high-resolution lithography and for trapping and manipulating tiny particles like viruses.



This is the first time a single, simple device has been designed to control these three major properties of light at once.

"Our lab uses nanotechnology to play with light," says Patrice Genevet, a research associate at Harvard SEAS and co-lead author of a paper published this month in Nano Letters. "In this research, we've used holography in a novel way, incorporating cutting-edge nanotechnology in the form of subwavelength structures at a scale of just tens of nanometers." One nanometer equals one billionth of a meter.

Genevet works in the laboratory of Federico Capasso, Robert L. Wallace, Professor of Applied Physics, and Vinton Hayes, Senior Research Fellow in Electrical Engineering at Harvard SEAS. Capasso's research group in recent years has focused on nanophotonics—the manipulation of light at the nanometer scale—with the goal of creating new light beams and special effects that arise from the interaction of light with nanostructured materials.

Mil/Aero007 News Highlights

Medical, Aerospace Certifications for API Technologies

API has received two new quality certifications for its EMS business, including the ISO 13485:2003 medical certification and AS9100 Rev C aerospace certification. The former marks the company's first medical-certified facility certification.

Positive Q4 Results Position OSI Systems for Growth

Deepak Chopra, OSI Systems President and CEO, stated, "During the fourth quarter, our security division achieved record operating profits as the higher margin turnkey screening solution business was a key factor in increasing our operating margins from 7% in fiscal 2012 to 16% in fiscal 2013."

Ducommun LaBarge Segment Posts Flat Sales in Q2

The company's DLT segment reported net sales for 2Q13 $107.5 million, compared to $107.8 million in the 2Q12. The defense electronics and commercial aerospace revenue increased 16.5%, offset by a 25.8% decline in the segment's non-A&D revenue.

Sypris' Electronics Group Revenue Up 6% to $7.7M in Q2

Revenue for the Electronics Group was $7.7 million in 2Q13, compared to $7.3 million for 1Q13 and $16.1 million in 2Q12, reflecting factors including budgetary and funding uncertainties within the U.S. DoD.

AVX Awarded 5-Star Supplier Award by Raytheon

AVX Corporation, a leading manufacturer of advanced passive components and interconnect solutions, was honored with the 5-Star Supplier Excellence Award from Raytheon's Integrated Defense Systems (IDS) business unit.

EPTAC to Help with IDEA Counterfeit Programs

EPTAC Corporation has partnered with the Independent Distributors of Electronics Association (IDEA) to deliver several counterfeit component mitigation and inspection programs providing clients with educational options and pathways to IDEA certification.

Murrietta Receives Raytheon's Highest Supplier Award

Raytheon recognizes its Five Star Suppliers based on three important factors: 100% on-time delivery, 100% sustained quality, and continuous process improvements. Murrietta Circuits was one of only 14 to be recognized for this tremendous achievement.

IECQ Program to Address Counterfeit Component Crisis

In response to the growing demand and need of the electronics supply chain, IECQ launched a programme designed to address the international counterfeit crisis faced by the aerospace, defense, medical, and high-performance (ADHP) sectors.

New Material May Transfer Heat More Effectively

A team of theoretical physicists at the U.S. Naval Research Laboratory and Boston College has identified cubic boron arsenide as a material with an extraordinarily high thermal conductivity and the potential to transfer heat more effectively from electronic devices than diamond.

DARPA Unveils ATLAS Robot

On Monday, July 8, 2013, the seven teams that progressed from DARPA's Virtual Robotics Challenge (VRC) arrived at the headquarters of Boston Dynamics in Waltham, Massachusetts to meet and learn about their new teammate, the ATLAS robot.

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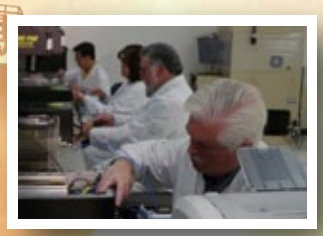
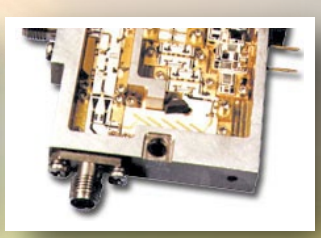
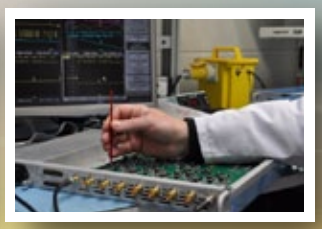


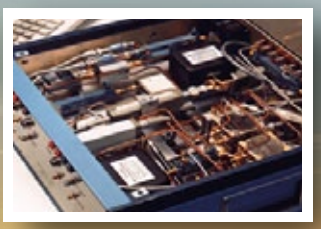
AS-9100C ELECTRONIC MANUFACTURING SERVICES



COMPLEX RF ASSEMBLIES



FUNCTIONAL RF TESTING TO 77 GHz



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A Study in PCB Failure Analysis: the Intermittent Connection

by Derek Snider
INSIGHT ANALYTICAL LABS INC.

Over the course of a failure analyst's career, he will be exposed to an extensive and varied array of devices. No matter the technology—whether they be nanoscopic silicon sensors with moving parts so small as to defy belief or massive circuit assemblies comprised of thousands of discrete components and integrated circuits—no device is completely immune to failure. Variations in process control, insufficiently robust designs, and extended abuse by an end user can all spell early doom for a device.

In our introductory article, Failure is the First Step on the Road to Success—the Failure Analysis Process (June 2013, *SMT Magazine*) we took a high-level overview of the failure analysis process, discussing the steps an analyst takes to turn a failing, rejected product into actionable knowledge for process improvement. In this column, we will see how these steps are applied to a specific failure. Naturally, examining a relatively trivial case would not provide the necessary depth of learning, so instead we choose to give an example of a failure many analysts dread: an intermittent failure on a printed circuit assembly.

In this study, a single printed circuit assembly was received as an RMA from an end-user (Figure 1). The end-user was able to identify the

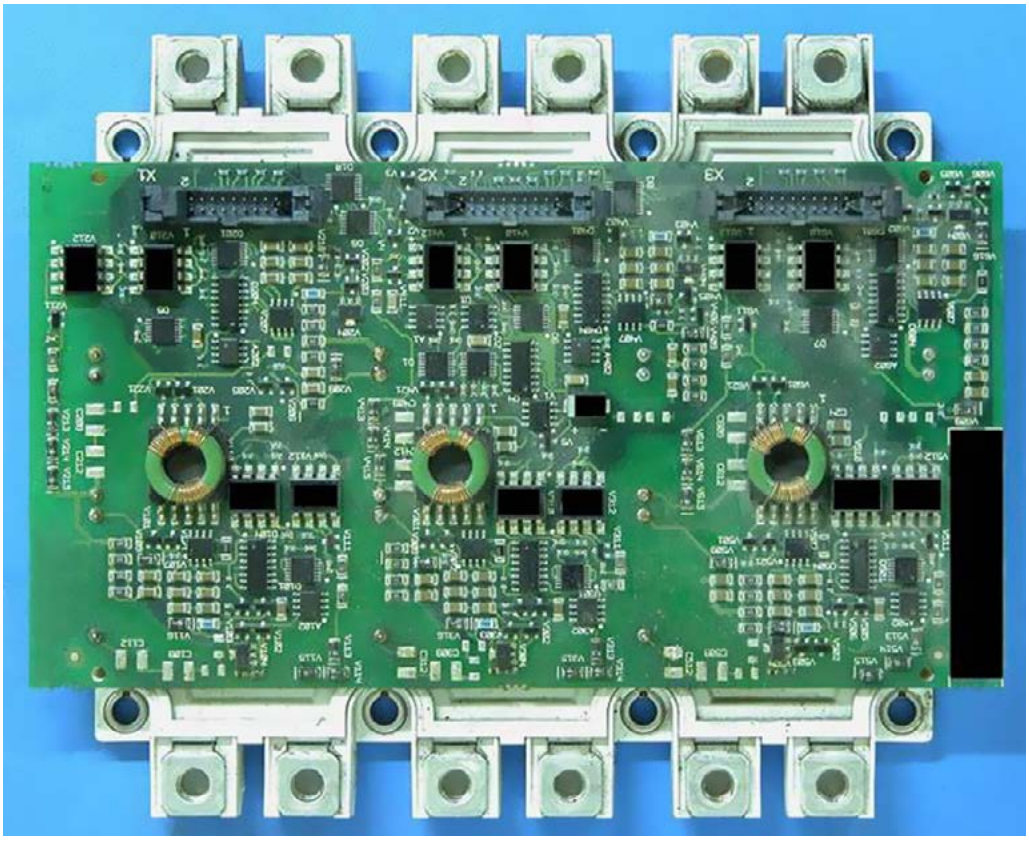

Figure 1: Photograph of the failed PCA.

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A STUDY IN PCB FAILURE ANALYSIS: THE INTERMITTENT CONNECTION *continues*

failing assembly only by swapping parts; lacking any sort of test equipment, the customer was unable to provide any detail that could help to narrow the scope of the analysis beyond the most basic of failure descriptions ("this part doesn't work anymore"). The first step in the failure analysis process is to verify the failure; after initial photodocumentation, the assembly was put into functional testing using an application test bench. Initial results were disheartening, to say the least; the assembly functioned as designed, with supply current and output levels within specifications. In the absence of any reproducible failure mode, an analyst must rack their brain, grasping at any explanation for why the product has miraculously returned to normal function. Could the product have been improperly used by the customer? For example, were all connectors fully seated? Were power supply voltages stable and held at the correct levels? Had this board been processed with a top secret, self-healing material pulled straight from the annals of science fiction that had repaired whatever defect was responsible for the initial failure (hopefully not, lest our intrepid analyst find himself out of a job)?

Fortunately, in this case, our analyst was rescued from the throes of despair and his search for a new career writing schlocky novellas about autonomous, regenerating electronic assemblies by a sudden change in the functional test results: An output that was previously within specifications suddenly dropped out, with only a fraction of the expected current being supplied to its load. Though our analyst rejoiced at being returned firmly to the realm of reality, these results indicated that the most likely root cause of failure would be hard to pin down—an intermittent connection.

The initial functional test led to several key observations that helped to characterize the failure. Initially, the assembly worked as intended, but after some period of time under power, the device would fail. Furthermore, the failure was not a "hard fail" (i.e., a short circuit or open circuit); power was still being supplied to the output pin, but insufficient drive current was available. After repeating the functional test and seeing the same failure characteristics, it was hypothesized that some thermal effect (thermal expansion, for example) was causing the device to fail. When first powered up, the board was at room temperature; however, after being under bias for a length of time, the power dissipated by the board caused enough self-heating to create a failure. Environmental testing was performed, and the temperature of the board was modulated; a strong correlation was noted between higher board temperature and reduced load current provided by the failing output. With the failure verified and characterized, the next step was to isolate the problem; in this case, isolation was done completely non-destructively, by tracing the circuit from the failing output back until an unexpected high resistance (48,000 ohms) between two points on the same node was noted (Figure 2).

With the failure verified and isolated to a relatively small area, non-destructive testing procedures were performed. For PCB failures, X-ray analysis and optical inspection are chief among the non-destructive approaches available; other techniques, like acoustic microscopy, are more appropriate for component-level failures. At this point in the process, an analyst would inspect for cracked solder joints or broken PCB traces, misaligned via drills, or any other anomalous features that might help to explain the failure mechanism; in this particular case, no issues were noted during non-destructive testing (Figure 3). While a negative result like this may seem like no value added to the analysis, in this case the data can be used to rule

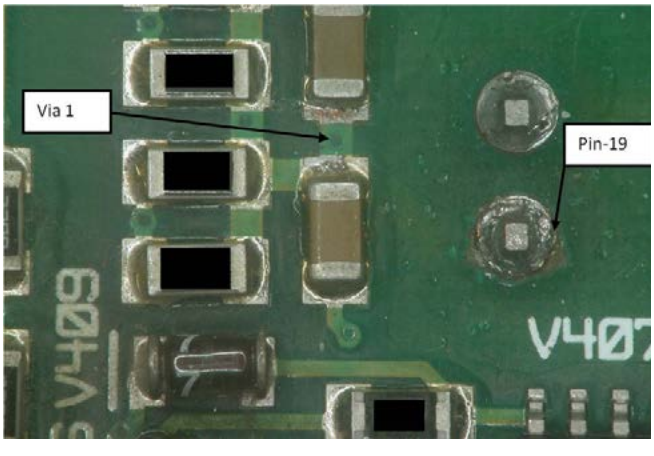

Figure 2: Photograph of the area of interest. High resistance was measured between Pin 19 and the capacitors connected to Via 1.

out certain types of defects (e.g., a crack in the copper trace between the two points as a result of warping of the PCB is unlikely).

The next step in the failure analysis process, revealing the defect, would almost certainly involve destruction of the board; as a result, a strong hypothesis was necessary before embarking upon any further analysis. In order to determine the best course of action, our analyst reviewed the facts as they stood:

1. The failure can be thermally modulated—as board temperature increases, the failure becomes more pronounced.
2. In the failing condition, high resistance is measured between two points on the same node. This high resistance results in reduced output current.
3. No signs of solder quality issues—cracking or non-wetting—were noted in the area of the failure.
4. X-Ray inspection did not reveal any signs of damage to the copper trace between the two suspect points.

Given this list of facts, our analyst determined that the most likely cause of failure was an intermittent contact between the two points in question that became worse under thermal expansion (as the board materials heated and expanded, less material remained in contact to conduct electricity). The most likely location for this type of failure would be at the connection between the copper trace and the barrel of a via or plated through-hole; given this hypothesis, the analyst elected to cross-section through the PTH for the suspect pin (Figure 4).

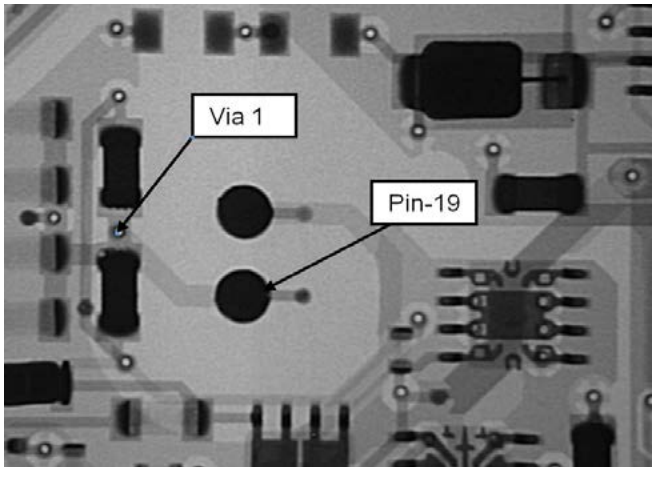

Figure 3: X-ray of the failed PCB area of interest. No anomalies observed.

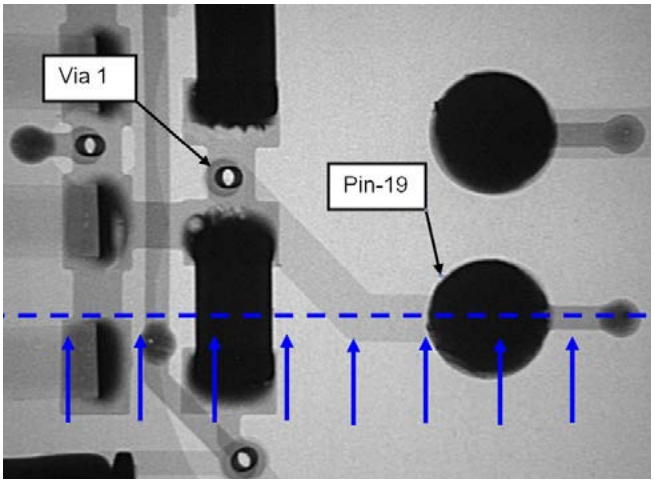

Figure 4: Higher magnification X-ray image of the PCB area of interest. The blue dashed line and arrows represents the direction and location of cross-sectional analysis for Pin 19.

The area of interest was cut away from the bulk of the PCB and encapsulated in epoxy. A cross-section was performed by grinding into the suspect pin with progressively finer grits of polishing abrasive, finishing with a sub-micron polishing compound to bring the sample surface to a finish suitable for high magnification imaging. The PTH was imaged with a high power optical microscope; as hypothesized, an incomplete connection between the copper trace and the PTH barrel was noted (Figures 5 and 6). The analyst had the proverbial smoking gun; now, the only remaining step was to tie the physical defect to its most likely cause.

Though the physical defect had been revealed, the analyst's job was not over; the goal of any failure analysis project is to find the root cause of failure and determine the most likely origin of any existing defect. Of the many possible explanations for this type of failure, two were considered as the most likely candidates:

- Mechanical stresses (vibration, thermal cycling, board flexure) may have broken a trace that was originally well connected

A STUDY IN PCB FAILURE ANALYSIS: THE INTERMITTENT CONNECTION *continues*

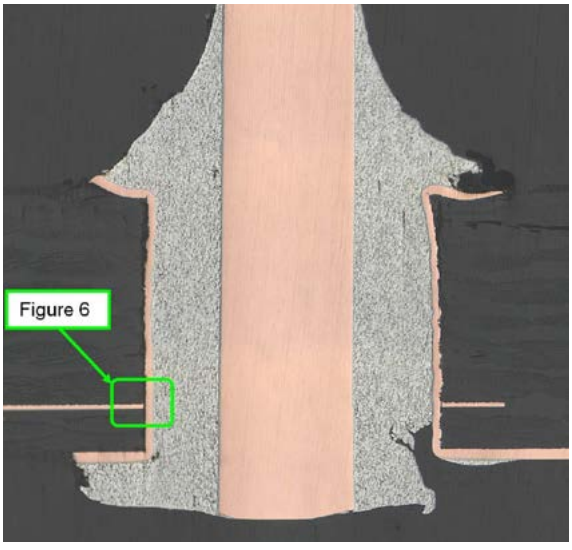

Figure 5: Photograph of the cross-sectioned Pin 19.

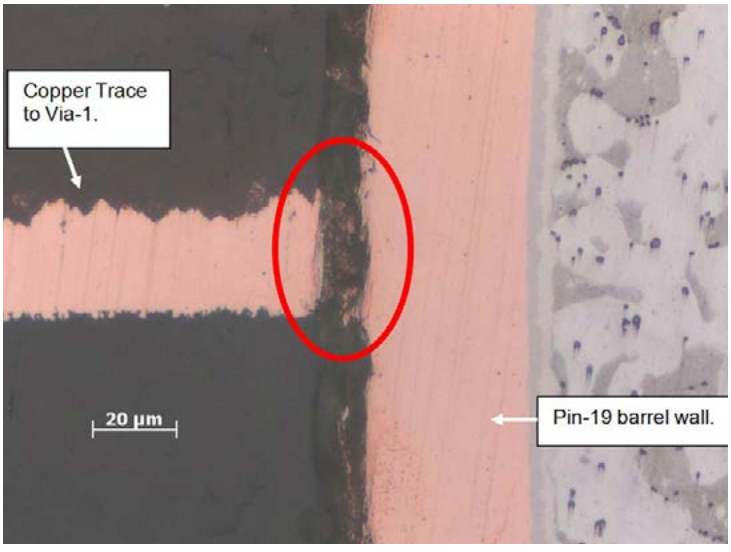

Figure 6: High magnification image of the cross-sectioned Pin 19. The red circle indicates the location of the separated via ring.

• Insufficient etchback or smear removal (follow-up after drilling holes in the board) was performed during the PCB manufacturing process, preventing a good bond between the buried traces and the barrel

If mechanical stresses were the root cause of this failure, an analyst would expect to see much more damage to the PCB's copper traces (some degree of tearing or other stress-related cracking); other than the separation from the barrel wall, no such damage was noted. Improper cleaning and etchback during manufacturing, on the other hand, could very well result in an incomplete bond between a buried trace and the via barrel. The defect was therefore classified as most likely occurring during manufacturing. Corrective action was implemented by adding additional inspection and destructive physical analysis on incoming PCBs per IPC-A-600 as part of production screening; as a result, other failures similar to this were found before reaching the end user, and the PCB manufacturer was able to identify and correct an inadequacy in their process.

Conclusion

In this case study, we examined how the failure analysis process enables a defective part to produce actionable data that suppliers and manufacturers can use to improve their product. Despite starting with little more than a nebulous problem description ("this doesn't work"), the analyst was able to methodically work towards a more comprehensive explanation of the failure; in doing so, an expensive chunk of scrap was transformed into a valuable source of knowledge, identifying a process weakness and helping to prevent further defective product from reaching end users. Future columns will continue to provide other approaches to failure analysis of printed circuit assemblies, components, and other electronic devices; in the mean time, keep an open mind, and remember that failure is nothing more than an opportunity to improve! **SMT**

Derek Snider is a program manager and failure analysis engineer at Insight Analytical Labs, Inc., a company providing failure analysis services to aerospace, medical, and semiconductor manufacturing industries worldwide. To contact Snider, click here.

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SMTonline Supplier/New Product News Highlights

Molex to Acquire FCT Electronics Group

According to Tim Ruff, Molex senior VP of business development and corporate strategy, this is a strategic acquisition that will help expand the company's presence in the medical electronics, industrial, telecom, and aerospace markets.

Europlacer: Flexible Problem Solving for Microtech

Europlacer, a manufacturer of market-leading flexible SMT placement machines, announces that Microtechrecently purchased an iineo system.

Arrow Electronics Reports Q2 Revenue of $89.9 Million

Arrow Electronics, Inc. has reported second-quarter 2013 net income of $89.9 million, or $.86 per share on a diluted basis, compared with net income of $114.4 million, or $1.02 per share on a diluted basis in the second quarter of 2012.

Indium8.9HFA Solder Paste Welcomed by Industry

Indium Corporation's Indium8.9HFA solder paste is a versatile, halogen-free, lead-free, solder paste with leading print performance on miniaturized components. Assemblers and OEMs are adopting this new product at an accelerating pace.

Dymax Debuts GA-140-SC Cure-In-Place Gasket

Dymax has introduced GA-140-SC, a UV/Visible light-curable, form-in-place and cure-in-place gasket. Formulated with patented See-Cure technology, GA-140-SC is bright blue in an uncured state, enabling confirmation of placement prior to cure.

Multitest Provides Solutions for ICs and Mobile Devices

The MT2168 pick-and-place handler offers a variety of smart features that meet the special requirements of ICs for mobile devices. The MT2168 fully supports advanced packaging.

Manncorp Installs Systems at Calsonic Kansei Mexicana

Calsonic Kansei Mexicana S.A. de C.V., a subsidiary of Japan's Calsonic Kansei Corporation, recently purchased two ULTIMA STR2 selective solder systems and an ULTIMA SSP selective fluxer from Manncorp.

Nordson ASYMTEK Launches Spectrum S-820-C

Nordson ASYMTEK, a Nordson company, a leader in dispensing and jetting technologies, has released its Spectrum S-820-C stainless steel dispensing system that is third-party certified for Class 100 cleanroom use.

GOEPEL's Inspection System Features New Camera

GOEPEL electronic offers an internally-developed camera and illumination system for optical inspection of selective solder joints to be integrated into external test cells. The integration package contains a specifically designed four-megapixel BUZZARD camera with GigE interface, multispectral illumination, a PC, and respective software.

Nordson ASYMTEK Improves Dispensing Speed

Nordson ASYMTEK, a Nordson company, has developed continuous path motion control software for jetting underfill for flip chips. The software optimizes dispense head motion, saving time and increasing units per hour (UPH).

NEW Technology Collection: Understanding Dispensing, Jetting, and Coating

Nordson ASYMTEK

Learn about key technologies for fluid dispensing, jetting, and conformal coating in these white papers you can download now.

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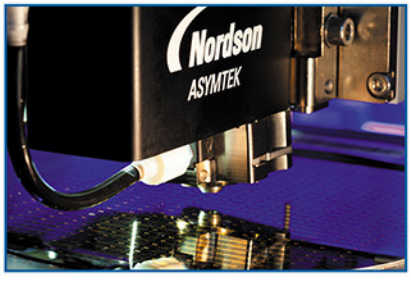
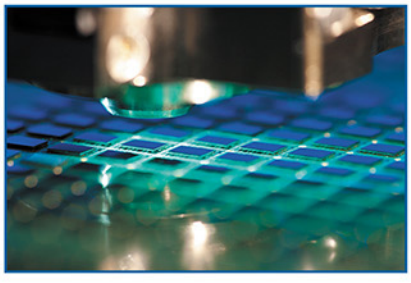


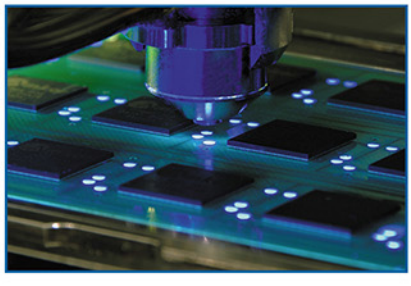
Sealing Dispensing for MEMS Wafer Capping

Wafer capping MEMS devices presents challenges and specific requirements for dispensing sealant, volumetric accuracy, and motion systems that can be met with the correct dispensing equipment and methods.
By Heakyoung Park



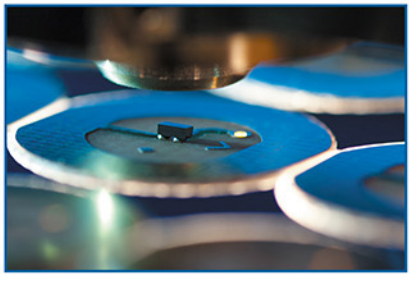
Underfilling Using Continuous Path Motion Control

New device configurations change the amount of fluid needed for underfill and the dispensing techniques for depositing it. Using a continuous motion of the dispense head avoids backtracking and improves units per hour by 27%.
By Akira Morita



Conformal Coating Process Characterization Considerations

Selective coating coats specific areas. Using properly characterized automated equipment is a reliable way to increase yield, throughput, and reduce the cost of the conformal coating process.
By Brad Perkins



Process Improvements in Fluid Dispensing

Speed and throughput have increased exponentially over the years, yet are still factors challenging the existing dispensing systems as fast never seems to be fast enough. Increasing throughput involves more than just speeding up the actual act of dispensing.
By Dan Ashley

See Nordson ASYMTEK at SMTAI booth #509

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Doing More Than One Thing at a Time

by Eric Klaver
ASSEMBLÉON

With women being renowned for multitasking abilities, perhaps they should be designing production lines—it could make our processes more efficient.

Look at maintenance. Although hardware can last for years, it will pick up dirt during production—with just how much varying from shift to shift. You can plan fixed maintenance slots per day, week or other fixed period but production goes down during those slots. If rush jobs are going through you might be tempted to skip maintenance actions, but that will have consequences. KPIs will drift outside control limits, and you may be forced to stop production altogether for repairs.

At the heart of the problem are the traditionally fixed roles of operators, technicians and supervisors, which can lead to a lack of cooperation. Cleaning and inspection is often not the operator's responsibility, with equipment faults and failures requiring calling in the technician. There is no real feedback loop, with fixed maintenance schedules rigidly telling people what to do and when. And audits generally only look for compliance that maintenance has taken place—not its effectiveness.

Maintenance is thus viewed as a cost or penalty to production, rather than a benefit to productive output and predictability. It is seen as less important than just keeping the line running.

Maintenance: No Need to Interrupt Production

While some major maintenance items require the line to be stopped, many small maintenance steps do not. These include cleaning, lubricating and attending to standard checklist actions. Best of all, performing these actions while production is still going will actually keep your machines in better condition than waiting for scheduled maintenance (well, as long as rush jobs don't delay your scheduled maintenance).

We do, however, need new tools to help. The rapid acceptance of smartphones and tablets mean they are ideal for smart production environments (Figure 1). Such methods are already being used for verification and reel replenishment/warning notifications, which you can react on and immediately make corrections. But what about in between those times?

Figure 1: Rapid consumer use of smart devices makes them ideal tools for use in production.

EE Technologies continues to review and expand capacity to serve existing and new customers. With 10 surface mount lines in Empalme, Sonora, Mexico and 4 in Reno, Nevada, EE Technologies has the capacity to provide flexibility and responsiveness. Long-term planning, flexible staffing, and cross training contribute to having the right capacity at the right time. EE Technologies currently runs multiple shifts in two locations with several lines running 24 hours a day 7 days a week. Having the right space, the right equipment and the right team in place is key to serving relentlessly and achieving our mission. Capacity is a strong competitive advantage for EE Technologies.

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DOING MORE THAN ONE THING AT A TIME *continues*

Smartphones and tablets can combine with intelligent maintenance procedures. They help track all the required actions, and remind you if you forget or don't have time for any of them. As long as these actions are performed in time, they can be done at any moment—effectively customizing the standard manufacturer's schedule to your actual production situation.

How can you fit all these actions in, though, when your system is up and running? In reality, there are plenty of small stops: during a production pause somewhere in the line, or during stencil cleaning, parts supply, changeovers, setups or many other temporary stops. These are the exact timeslots where people could perform quick, necessary maintenance actions.

Taguchi and Loss

It's all about working as close as possible to the minimum of the Taguchi loss function (which shows loss vertically and variation horizontally). Taguchi showed that costs don't suddenly step up as variation goes outside specification limits (Figure 2). When a process runs at its optimum, the losses are at a minimum. As you move away from optimum, the losses rise exponentially.

Pete Jessup of Ford Motor Company gave an example that explains this perfectly: What is the best temperature for an office? This will be different for everyone, of course, but there will be some minimum value that will be best for all the occupants. If the temperature varies say 3°C or F around this minimum, there will be little loss—people will hardly notice. Another 3° one way or the other and some people will feel a bit uncomfortable. Another 3° and more people will start to lose concentration. Another 3° and people will start shivering or sweating and will want to get away from the office so they can be comfortable again. When you hit specification limits—the legal minimum or maximum—people need to put down tools and leave the office. Each 3° increase or decrease from the optimum has greater effect than the previous 3°.

Similarly, the loss from your processes doesn't suddenly step up when the variation hits specification limits. Outside specification limits you get massive losses, it's true: loss of production, loss of expensive components and boards and—most important of all—loss of you and your customer's reputation. Just meeting specifications is not good enough, though. If placement variation is at one extreme and (for example) stencil variation is at the other extreme then you can still get rejects. The larger the variation in process, the more rejects your process will produce, even if each individual process is within specification limits.

The most important decision is of course when to buy new equipment, since that sets the overall position of the curve—and your overall losses

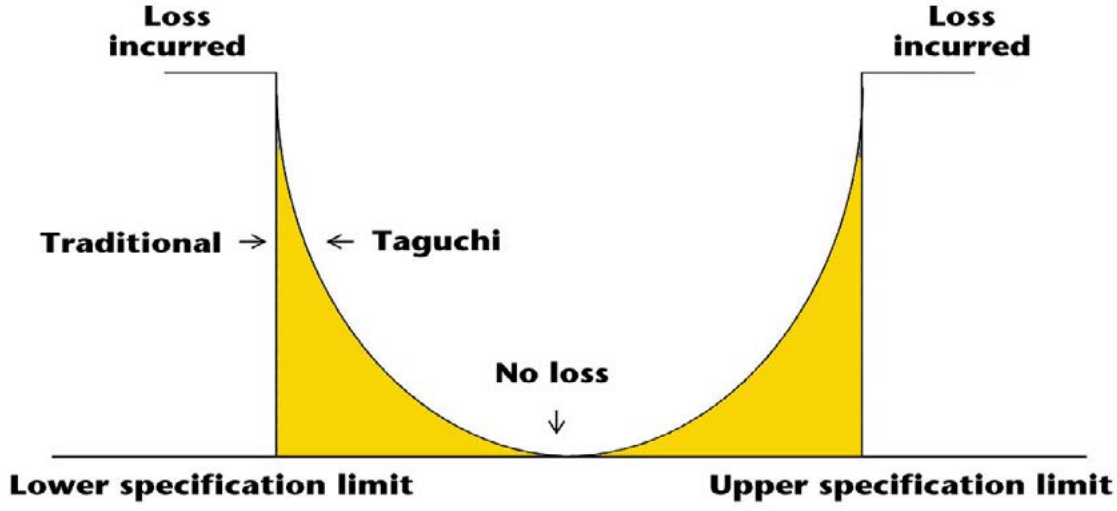

Figure 2: As a process varies either side of optimum, the losses rise exponentially.

over the years that you'll be using the equipment. Once you've installed your production line you need to keep losses at a minimum. Maintaining equipment during spare moments does exactly this. It keeps your line performing at its best, and keeps your losses to an absolute minimum.

Closed Loop Maintenance

Closed-loop maintenance draws the equipment manufacturer into the loop along with the operator, technician and supervisor—all share responsibility for equipment care. That means helping to train and support the operating and maintenance team, monitoring results with the production team, and defining corrective actions.

Assembléon's recent closed-loop maintenance package is tablet-based for immediate feedback and action, and is an extension of total productive maintenance (TPM). Operators, technicians and supervisors work together to co-ordinate shift maintenance tasks for fewer breakdowns. People pay attention to the machine more often and so are more likely to spot other potential defects. That in turn makes your line more predictable—so you can meet the commitments you've made to your customers.

Closed-loop maintenance does require discipline and drive from your operators, but it encourages greater ownership and teamwork to reduce variation and waste—always a good thing for your overall equipment efficiency.

Smarter maintenance complements smarter software and smarter hardware. And for surface mount assembly, multitasking is at the heart of it. It effectively gives you an extra shift a week. **SMT**

Eric Klaver has been with Assembléon since 1998. He is currently the chairman of IEC work group TC40WG36, which specializes in component packaging. To contact Klaver, click here.

SMTonline Market News Highlights

Global Smart Grid Technology to Grow $220B by 2020

With the smart grid core and enabled technology market expected to grow to $220 billion by 2020, the smart grid is seen by many utilities around the globe as the ticket to addressing the escalating demand for reliable power, renewable energy integration, and greater energy efficiency.

Global Mobile Phone Market Up 6% in Q2

The worldwide mobile phone market grew 6.0% year-over-year in the second quarter of 2013 (2Q13). According to the IDC Worldwide Quarterly Mobile Phone Tracker, vendors shipped a total of 432.1 million mobile phones in 2Q13 compared to 407.7 million units in the 2Q12.

Global Semiconductor Industry to Reach $394 Billion In 2017

The Asia Pacific (APAC) region represents approximately 75% of the global market. Some of the major players include Intel Corporation, Samsung Electronics, Taiwan Semiconductor, Texas Instruments, and Toshiba Corporation. A combination of factors influences market dynamics tremendously.

Market & Technology Drivers to Bring 3D-IC to Production

With semiconductor technology moving toward systematic integration of stacked heterogeneous chips and 3D-IC becoming a mainstream trend, the latest developments will be featured at 3D-IC & Substrate Pavilion and Advanced Packaging Technology Symposium at SEMICON Taiwan 2013 and the SiP Global Summit 2013.

3D Scanning Market to Reach $4.08B by 2018

The global 3D scanning market is forecast to grow from an estimated $2.06 billion in 2013 to $4.08 billion by 2018, at an estimated CAGR of 14.6% from 2013 to 2018. Recent industry trends show the technology is continually improving—right along with demand.

Tablets Shipments Soar in Q2; Up 43% YoY

Over 34 million tablets shipped in Q2 2013, a 43% year-on-year increase. Tablets now account for 31% of worldwide PC shipments, but Apple's performance faltered. Its tablet shipments declined 14% on Q2 2012 and its market share dropped to 43%.

Key Raw Material Demand to Double as LED Market Booms

Global demand for precursor, a material used in manufacturing of light-emitting diodes (LEDs), is set to more than double from 2012 to 2016, as the market for LED lighting booms, according to a new report entitled "Precursor for LED MOCVD—Market and Industry Analysis," from Displaybank.

Global Semiconductor Revenue to Rise 6.9% in 2013

The SAF also forecasts that semiconductor revenues will grow 2.9% year-over-year in 2014 to $329 billion and log a compound annual growth rate (CAGR) of 4.2% from 2012-2017, reaching $366 billion in 2017.

U.S. to Witness Uptick in Economy in 2014

The U.S. economy is in for another year of sluggish growth in 2013, but a rebound in the housing market is expected to lead to stronger gains next year, according to The Conference Board of Canada's U.S. Outlook, Summer 2013.

Small Cells Market to Grow, Rise 125% in 2014

In ABI Research's latest forecast, overall enterprise and consumer Femtocell shipments will reach 5.7 million units in 2014 compared to 3.8 million units in 2013. While 3G indoor small cells will continue to represent the vast majority of shipments, LTE indoor small cells are expected to ramp up significantly.

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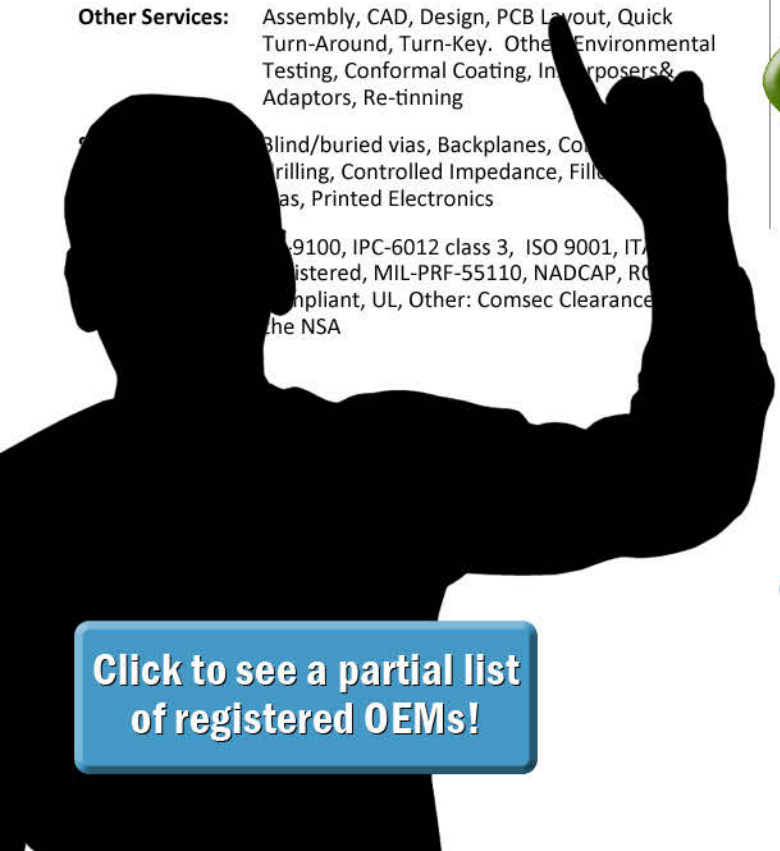

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A SHORT SCOOP

Step Stencils, Part 2: Applications and Solutions

by Rachel Short
PHOTOSTENCIL LLC

In my last Short Scoop, (The Ins and Outs of Step Stencils, Part 1) you heard a little about step stencils—what they are, why demand is increasing, different types, and what to look for. In this column, we explore step stencil applications and solutions.

Step stencil applications fall into eight categories:

1. Step-up stencils for ceramic BGAs
2. Step-up stencils for intrusive reflow of through-hole components
3. Step stencils with a relief pocket on the contact side (board side) for:
   a. Raised vias
   b. Bar codes
   c. Board hold-down clips
   d. Additive traces
4. Step stencils for two-print applications using mixed technology
   a. SMT/through-hole
   b. SMT/RF shield
   c. Flip chip/SMT
5. Thick stencils with reservoir pockets for printing glue on a variety of components with different stand-off heights
6. Two-print stencils with relief pockets for printing component attachment glue after SMT solder paste has been printed
7. 3-D electroform stencils with a formed relief pocket for a high profile flex connector

The following is a breakdown of these eight categories.

Ceramic BGAs

Ceramic BGAs (CBGA) present a problem to the SMT assembly process. Slight variations in ball co-planarity can result in an open contact to the balls. Printing higher solder bricks on the CBGA pads can prevent this. Normally, a brick height of 7-8 mils is desirable, but .5 mm pitch QFPs, 0402 chip components, and R-packs will not tolerate an 8 mil thick stencil. Aperture sizes are too small to achieve good paste release with such a thick stencil. Therefore, a step-up stencil is required.

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STEP STENCILS, PART 2: APPLICATIONS AND SOLUTIONS *continues*

Intrusive Reflow of Through-Hole Components

There has been a trend to reflow through-hole components with SMT components rather than wave soldering them. For this application category, solder paste is printed in and around the through-hole and pad. Three ways to achieve sufficient solder paste for this application are:

1. Overprint the hole/annular ring with an oversized stencil aperture.
2. Step-up and overprint the hole/annular ring with an oversized stencil aperture.
3. Two-print stencil where the second print stencil is very thick and provides more solder paste for the through-hole.

Relief Etch Pocket on the Contact Side

Relief pockets on the PCB side of the stencil provide relief clearance for raised areas on the PCB, allowing good gasketing of the PCB to the stencil. Some common relief-etch applications are:

1. Raised via pads on the PCB: These features prevent the stencil from gasketing to the PCB. For good stencil/board contact, a relief pocket is etched on the contact side of the stencil wherever there is a raised via. Typically, the relief pocket depth is one-half the stencil thickness, usually enough to clear the obstruction.

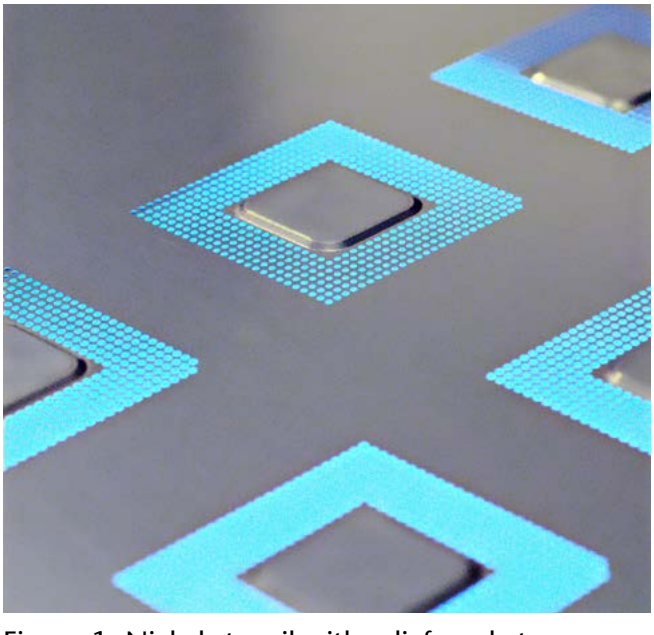


Figure 1: Nickel stencil with relief pocket.

2. Bar code on the PCB: A stencil with a relief pocket etched in the area of the bar code allows the stencil to sit flat on the PCB during printing and allows proper stencil gasketing in areas with adjacent print features.

3. Board hold-down clips: Some stencil printers have edge clips to hold the PCB down during printing. If component pads are close to the edge of the board, the stencil may not be able to gasket to the board on the edge and a relief pocket will be needed.

4. PCB with additive traces: Traces added to the PCB surface correct design problems by altering the lead wiring, but the trace adds height. A relief pocket around the additive trace will solve the problem.

Two-print Applications for Mixed Technology

1. SMT/through-hole mixed technologies: When overprint (oversized apertures for the through-hole) with a normal step-up stencil doesn't provide enough solder paste volume for proper intrusive reflow, a thicker stencil must be used. The problem is SMT components won't tolerate a 15–20 mil thick stencil and a step down from 20 mils to 5 mils won't work well. For this situation, the two-print stencil operation is a viable solution. The only alternative to providing more solder paste is to make the stencil thicker. In the two-print operation the SMT solder paste is printed with a normal 5 or 6 mil thick stencil. The second 15–20 mil thick stencil provides increased depth SMT paste relief pockets etched on the contact side to clear first print solder features.

2. SMT/RF Shield: Small hand-held communication devices usually have RF shields positioned very close to small SMT components. Additional paste height is required for the RF shield, requiring a thicker stencil than the thickness required for the SMT components. The spacing between the RF shield and the components prevents the use of a normal step stencil. The two-print option provides a solution when the distance between RF shield and SMT com-

ponents is as small as 15 mils (.38 mm) with paste height up to 8 mils (.2 mm) for the RF shield.

3. Flip chip/SMT mixed technologies: Sometimes it's desirable to print flux or solder paste for a flip chip component and solder paste for SMT devices. Both are then placed and run through the reflow cycle. Normally, the stencil thickness for the flip chip printing is much too thin for SMT printing. Once again, two-print stencils are an ideal solution. A thin (1–2 mil) electroform stencil prints either flux or solder paste on the flip chip pad sites. A second 5 mil thick SMT stencil is then used for solder paste. Relief pockets are formed on the contact side anywhere flip chip flux or paste was previously printed.

Printing Glue for Components with Different Stand-off Heights

There are advantages to printing glue rather than dispensing it. Set-up and process times are shortened since glue bricks are deposited in parallel rather than one dot at a time. Glue does not print the same way as solder paste and it is acceptable as well as useful to leave some of the glue remaining inside the stencil aperture. Large apertures will release all the glue while small apertures will release only a portion of the glue, which is useful for different component stand-off heights. An example is an application with a chip component with a 4 mil stand-off, a 15 mil stand-off SOIC, and an SOIC with a 30 mil stand-off on the same board. To achieve height differentials, aperture sizes can be adjusted to provide glue height variation, or for applications requiring thicker glue deposition a print/controlled flood feature or a glue reservoir stencil may be employed and can achieve glue deposition up to 50 mils.

Two-Print Glue and Solder Paste Application

In this application the applied glue is thicker than the solder. Solder is first applied using standard application techniques. A two-step stencil with formed reliefs is then used to apply the thicker glue. This application is attractive for glue attaching large chip devices for second pass reflow.

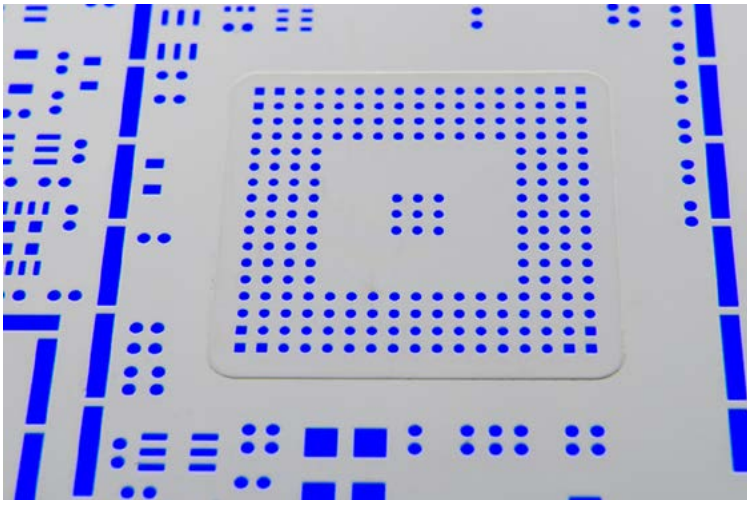


Figure 2: Electroformed step stencil, 5 mil base, 7 mil step areas, with apertures.

3D Stencils with Flex Circuit Relief

Imagine two PCBs that are connected with a flexible connector that rises 90 mils above the board surface and that is obstructing a normal stencil from making contact with the board. How do you print solder paste on the SMT pads with the connector in the way? The solution is a 3D electroform stencil that is 5 mils thick, but has a 95 mil high relief pocket formed into the stencil. In order to apply the paste, a custom E-blade was formed with a notch for clearance of the relief pocket.

Step stencils provide unique solutions to a wide range of complex printing applications. By tailoring the stencil to specific applications, a wide range of processing parameters for thickness and aperture size can be achieved. Step stencils can easily accommodate varied solder heights, mixed technologies, and even, in conjunction with two-print stencils, application of dissimilar materials onto the same board. **SMT**

Rachel Short is vice president of sales and marketing at PhotoStencil LLC. She may be reached via e-mail, or by phone at 719-304-4224.

EVOLUTIONARY SOLUTIONS

Deciding by the Numbers

by Karla Osorno
EE TECHNOLOGIES, INC.

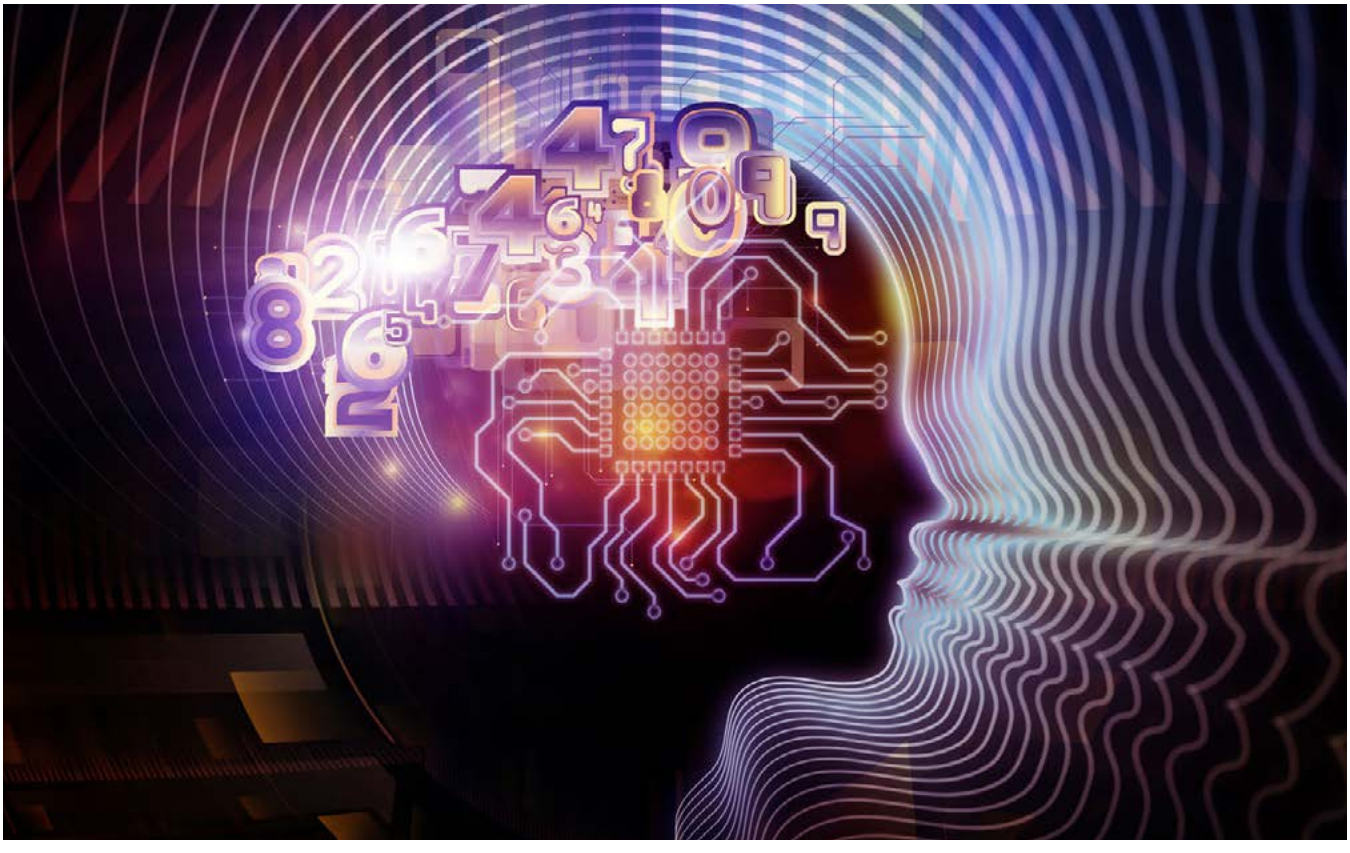
In a contract manufacturing environment, thousands of decisions are made daily. Decisions that have consequences on the end product are made by workers, middle managers and senior managers. These decisions are made on the line, in support areas, and in conference rooms. They are made months in advance and in minutes, as the product moves throughout the production area. Organizations that succeed in the short and long term create a culture where data is always used for decision making.

Value of Data Based Decisions

Making decisions using data and metrics is one of the most important activities a manufacturer can take on. Collecting the data is critical to understanding the operational performance. Each company will want to choose which specific data is value added and then establish methods of collection. Training employees on the methods of collection and the reasons for collection is also important. And of course, using the data collected will speak volumes to the employees and increase their motivation to continue collection. When the data is collected and not used the consequences can be costly to morale and profits.

Whether your plant has two employees, 200 or 2,000, each individual choice or decision made by an employee creates a result. And these results become an input in the next process step. This has a direct impact on the final products produced in your plant.

Most manufacturing plants will have processes and process controls that limit the number of decisions required by the employee. As-



2013 MEPTEC SEMICONDUCTOR ROADMAPS SYMPOSIUM

A Collaborative Update from Standards Bodies, Industry Groups, and Large OEMS

September 24, 2013 • Biltmore Hotel, Santa Clara, CA

In the spirit of collaboration, this event will consist entirely of panel discussions, rather than traditional presentations. This will allow for more interaction among the speakers and attendees, so that the synergies, gaps, and differences of opinion can be explored more thoroughly. A day full of panel discussions will also allow representatives of more companies, including device manufacturers and large OEMs, and industry and standards organizations, to present their views. Join us for this first-of-a-kind collaborative event!

Over the years, MEPTEC's popular Roadmaps events have been attended by high level managers, CEOs, and CTOs, looking for validation and insight into technology and business directions for their companies, for their suppliers and, in some cases even their customers. At past events they, and their competitors who were presenting their own roadmaps, were looking for strategic help and metrics of progress.

During its long and successful existence, MEPTEC has recognized the need for one essential ingredient above all others in achieving success with any semiconductor industry roadmaps: collaboration.

First, collaboration among trade associations, standards groups, OEMs, providers of analytic and design software, sub-contract service providers, and suppliers throughout the supply chain is increasingly critical to success. Second, as distinctions among semiconductor processing, packaging and assembly technologies, and design/testing protocols are disappearing manufacturers have greater need for collaboration.

The MEPTEC Roadmap event will bring together standards groups, industry groups and consortia, industry experts, device manufactures, and representatives of the large OEMS to update their roadmaps and development activities, which may include 2.5D/3D as well as other driving factors pertinent to their business segments. Join us for this first-of-a-kind collaborative event! ◆

The Biltmore Hotel is conveniently located at 2151 Laurelwood Road in Santa Clara, CA in close proximity to the San Jose Airport.

Symposium Topics will include:

- **Market Drivers –** the current and future products that continue to drive semiconductor packaging down the road of "smaller, faster, and cheaper" – logic, memory, power, other (including MEMs and sensors)
- **Packaging needs** expressed by the major device manufacturers (ODMs), the end customers (OEMs), and the assembly and test suppliers (OSATs and EMS) Non-mechanical performance needs including interconnections, transmission speeds, switching protocols, new reliability requirements.
- **Non-mechanical performance needs** including interconnections, transmission speeds, switching protocols, new reliability requirements.
- **Status of efforts** of various Consortiums, Standards groups and trade organizations to support their members and to help establish infrastructure.

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DECIDING BY THE NUMBERS *continues*

suming employees follow these processes and documented procedures, the impact of poor decisions can be mitigated. The reality is that most manufacturing processes are complex and documenting every scenario is next to impossible.

Throughout a typical eight-hour shift, an employee may make multiple decisions. For example, if each employee makes even 10 decisions, a simple math calculation shows that this equates to 20-20,000 decisions made in a plant in just one shift.

The goal of manufacturing leadership is to reduce variability in an effort to achieve strategic objectives that include providing quality products on time and at the best cost. This many decisions made in just one shift can create much variability. This variability is significantly reduced when a culture of metric or data based decision making is created.

Creating the Right Culture

With intention, senior management can create and cultivate a culture of using the data for decisions. It starts with defining expectations and casting vision for what the culture will look like. Keeping it simple and easy to duplicate is the way to go.

Once the expectations are communicated to the company, everyone will be on high alert to see if behavior matches what was stated by senior management. Acknowledging progress and not perfection will go far to creating a sustainable culture.

Managers can set the example by asking questions that require data, by asking for evidence to support decisions, by acknowledging all data-based decisions, and by avoiding any appearance of "flying by the seat of their pants."

Middle managers and employees will emulate what they are shown by their leaders. Leaders working with teams to solve problems can ask specific questions that require use of data that has been collected. For example, an inspector who states that there is a "problem with a line producing defective products all the time" may be asked "in how many of the last eight weeks was the quality below the company target?" and "how far below the target was the quality each of the eight weeks?" This requires the inspector to have the required data rather than solely an opinion or feeling that the results are unsatisfactory.

Area leaders also want their teams to emulate their behavior by providing evidential data to support pending and prior decisions. A production supervisor who authorizes overtime should be able to show data that the cost of overtime for completion of a project is a better decision than adding new team, rather than simply responding to an emergency situation and using overtime to cover other issues. Or imagine your joy when a materials lead provides data showing the root cause of a late shipment, along with a new procedure correcting this issue. Simply acknowledging teams for using accurate data (and for not using inaccurate data) will go far in cultivating a culture of accountability through metric-based decisions. This is not about praise or correction. By acknowledging with a simple statement of fact, the leader lets the team know they are noticed and reinforces expectations for data use. Acknowledgement is highly motivating and increases the vitality of employees.

A production supervisor who authorizes overtime should be able to show data that the cost of overtime for completion of a project is a better decision than adding new team, rather than simply responding to an emergency situation and using overtime to cover other issues.

Leaders who repeatedly make hurried or random decisions are not cultivating a culture of data-based decisions. But neither are leaders who sit ondata and never make a decision. Finding the right balance of analysis and action is extremely important. In most instances, cultivation of the right culture trumps the specific decisions and related consequences. It is worth

taking the time to ask a few key questions to get the data and avoid a "fly by the seat of your pants" culture.

When the data is collected and used consistently and continually and when major decisions are made with the data, a culture of accountability is created. In this type of culture, there is an effect on minor decisions too. Employees at all levels of the company realize the impact of their decisions and activity. This recognition of their impact increases their morale, the quality of their decisions, and therefore the results.

Data Collection Methods

There are many methods of data collection. Typically, the best approach for deciding which method to use is to start with the end in mind. What problem will the data be used to solve? What questions need to be answered? With this information you will have more of an idea of the best method to use.

Another important consideration is the length of time the data collection will cover. If the situation is temporary then the data collection method will be less formal or systematic. If the situation is more ongoing then the method of data collection may start less formally and ultimately become automated. Automation is great but not always required. Benefits of automation must be weighed against the costs.

Manual tracking, spreadsheet tracking, and database tracking are common methods for collecting data. Extensive data tracking systems have also been developed in house or proprietary systems purchased. These systems have an initially high cost. However, the savings achieved with fewer production issues often outweigh the initial costs.

Including the end user and the data collection team in these discussions is beneficial as they can each provide insight that will make the data collection method selected more effective.

"Another important consideration is the length of time the data collection will cover. If the situation is temporary then the data collection method will be less formal or systematic. If the situation is more ongoing then the method of data collection may start less formally and ultimately become automated."

Course Corrections

For each data collection topic, you will undoubtedly have a specific target or goal you are trying to reach. As your team moves toward the desired result, the data will help to assess performance and to take corrective action as needed. This only works if you are looking at the data often enough to make course corrections. The frequency of review will depend on the data, method of collection, and result being tracked.

Data review and course correction responsibility can be defined so that the appropriate actions can be taken in a timely fashion. Having a culture of acceptance of course correction is vital also. Course correction is not necessarily in response to a problem.

Using data-based decision making in manufacturing is like an airplane journey. From Brian Tracy's book Flight Plan—The Real Secret of Success, all airplanes are off course 99% of the time. He explains that the pilot and avionics are continually bringing the plane back on course.

Your purpose as a leader and as an employee is to move your organization to its strategic destination. Wherever you find yourself culturally and operationally as an organization, take steps today to move toward by the numbers and reap the rewards you have sown. **SMT**

Karla Osorno is business development officer for EE Technologies, Inc., an EMS provider delivering complete engineering and manufacturing services with locations in Nevada and Mexico. To read past columns or to contact Osorno, click here.

TOP TEN

News Highlights from SMTonline this Month

1 Sanmina Q3 Profit Improves

"I am pleased with our third quarter results. We continue to benefit from improved efficiencies and favorable business mix. Our outlook for the fourth quarter is modest growth with further improvements in our operating model," stated Jure Sola, chairman and CEO.

2 Top Electronics Execs Plan Gathering in September

IPC announces its IPC Management Meetings, a forum for company leaders to gain a high-level perspective on technology, market trends, and management issues, will be held September 24, 2013 in Chicago and open to senior executives.

3 Lead-Free Soldering Technology Symposium at SMTAI

The SMTA will hold the Lead-Free Soldering Technology Symposium October 17, 2013 as a focused symposium at SMTAI. The focus is on the findings of three industry consortia related to the advancement of lead-free technology.

4 Kitron Overcomes Challenging Markets; Revenue Up 3.3%

Kitron's revenue for second quarter amounted to NOK 430.3 million, a 3.3% increase compared with the same period last year. EBIT was reduced from NOK10.6 million to NOK 9.3 million for the second quarter.

5 IEC's Revenue Remains Negative in Fiscal Q3

For the quarter ended June 28, 2013, the company reported revenue of $35,154,000, and net income of $382,000 or $0.04 per diluted share. W. Barry Gilbert, chairman of the board and CEO, stated, "While revenue and earnings are down from the same quarter last year, we made quite a bit of progress from the $1.1 million loss in the second quarter."

6 NBS Moves to New Facility; Boosts Operations by 50%

"Our latest move is a significant sign that our having extolled 'Made in the USA' beginning in 2010 was much more than a slogan," explained Michael Maslana, president and CEO. "It is now widely recognized as an attractive attribute and in the context of ongoing industry discussion about re-shoring, our expansion demonstrates both a timely and meaningful continued commitment."

7 SMTA Offers Online SMT Processes Re-Certification Program

The goal of the re-certification program is to present new materials which have been added to the certification curriculum since the initial sessions in 2003 and test that engineers have a competent understanding of the updated information. Eligible engineers have up to one year to complete the online program.

8 CTS EMS Q2 Revenue Down on Market Weakness

CTS CEO Kieran O'Sullivan, stated, "We improved earnings and have taken steps to simplify our manufacturing footprint while improving operating margins. We are focused on the challenges in our EMS business…"

9 PartnerTech Reports 2.5% Sales Increase in Q2

"Second quarter sales were 2.5% higher for comparable units and in local currencies than the same period of 2012. Operating profit of SEK 3 million was lower than the second quarter of 2012, while both cash flow and operating capital turnover improved," said Leif Thorwaldsson, president and CEO.

10 Kimball's Nanjing, China Facility Earns ISO 13485 Certification

"We are proud to now have ISO 13485 certification in all of our manufacturing facilities. The addition of this certification will allow us to support our medical customers' needs in the rapidly expanding healthcare market in China," stated Tom Ferris, group director of medical business development.

EVENTS

For the IPC's Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar, click here.

For a complete listing, check out *SMT Magazine's* full events calendar here.

NEXTGEN AHEAD
September 9–11, 2013
Washington, D.C., USA

International Test Conference 2013
September 10–12, 2013
Anaheim, California, USA

Capital Expo & Tech Forum
September 10, 2013
Laurel, Maryland, USA

2013 MEPTEC
September 17–18, 2013
Tempe, Arizona, USA

Failure Analysis of Electronics Short Course
September 17–20, 2013
University of Maryland, Maryland, USA

Electronics Operating in Harsh Environments Workshop
September 17, 2013
Cork, Ireland

IESF 2013: Integrated Electrical Solutions Forum
September 19, 2013
Dearborn, Michigan, USA

MRO EUROPE 2013
September 24–26, 2013
London, UK

PCB West 2013
September 24–26, 2013
Santa Clara, California USA

ID WORLD Rio de Janeiro 2013
September 26–27, 2013
Rio de Janeiro, Brazil

SAE 2013 Counterfeit Parts Avoidance Symposium
September 27, 2013
Montreal, Quebec, Canada

2013 SMART Group European Conference
October 2–3, 2013
Oxfordshire, UK

RFID in High-Tech
October 2–3, 2013
Santa Clara, California, USA

Long Island SMTA Expo and Technical Forum
October 9, 2013
Islandia, New York, USA

IEEE SMC 2013
October 13–16, 2013
Manchester, UK

electronicAsia
October 13–16, 2013
Hong Kong, China

SMTA International
October 13–17, 2013
Fort Worth, Texas, USA

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Next Month in *SMT Magazine:*

Lead-free Developments

It's been more than seven years since RoHS became the law of the land in Europe. But many OEMs and EMS companies still find themselves facing increasing challenges related to lead-free processes. In October, *SMT Magazine* shines a light on the often murky world of lead-free assembly.

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