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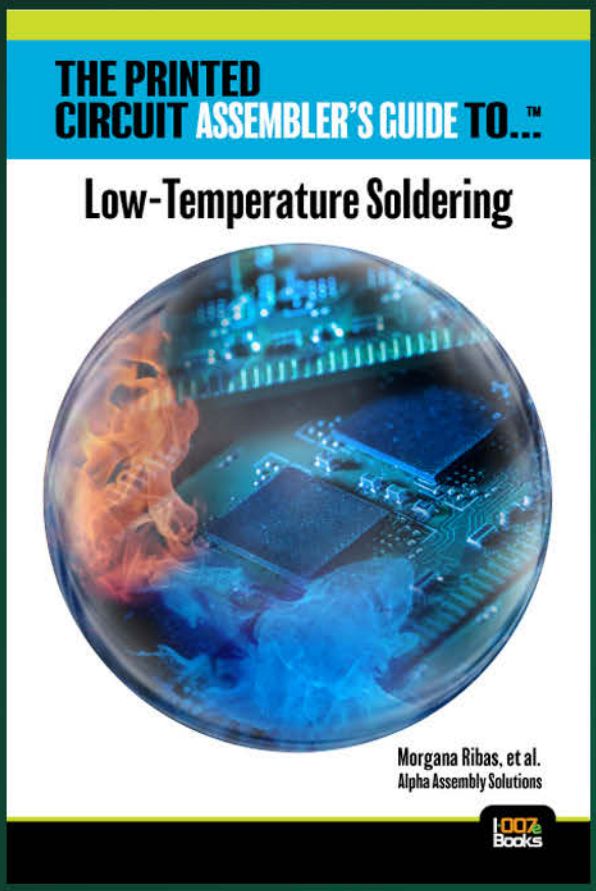

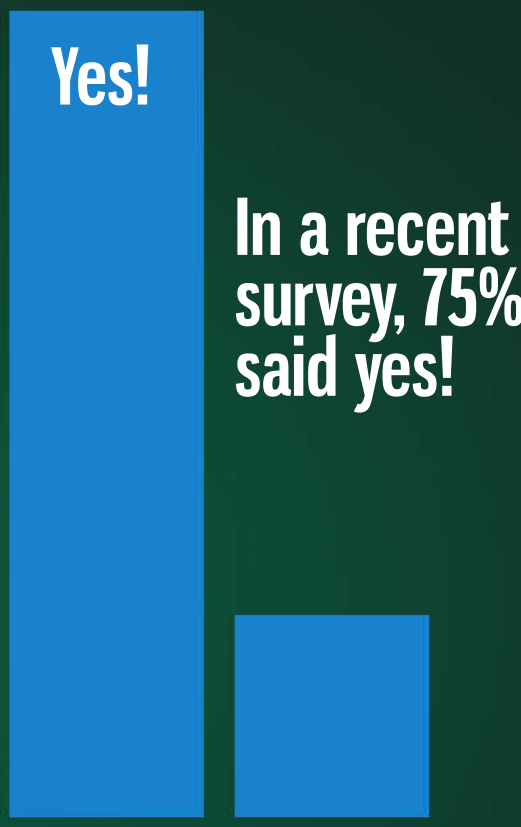

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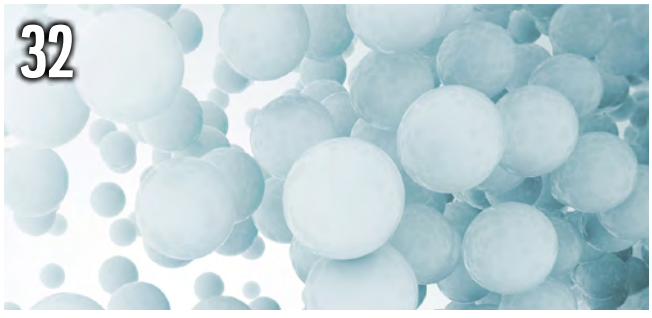
Reliability vs. Failure

It should come as no surprise that solder and solder joints are often at the center of attention in electronics assembly when discussing failures and reliability. This issue includes articles and columns from industry experts as well as insightful technical papers on the cutting-edge of failure and reliability research.



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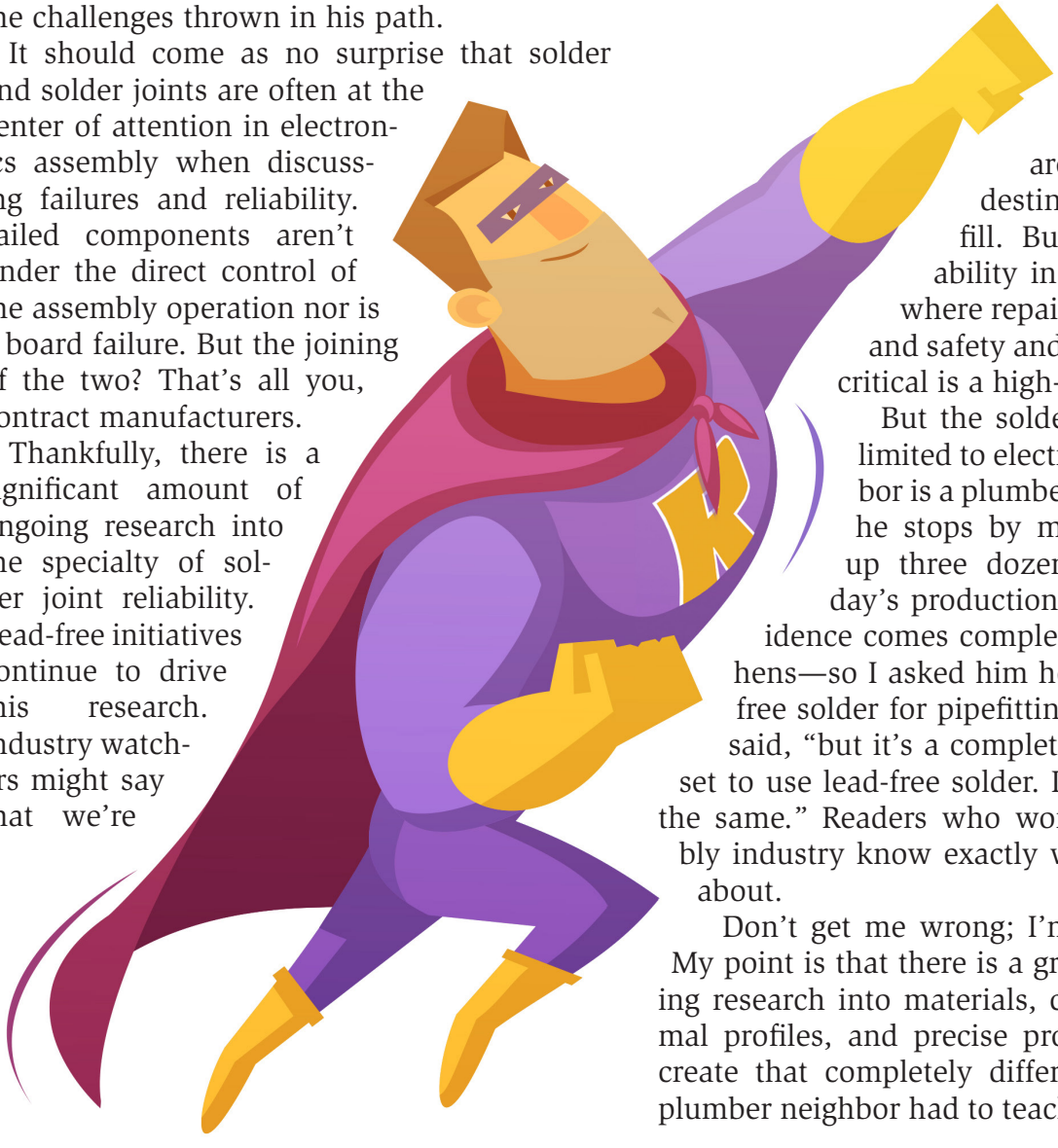
Reliability vs. Failure

Nolan's Notes
by Nolan Johnson, I-CONNECT007

Summer is officially underway here in the Northern Hemisphere, and just like the temperatures, we're turning up the heat in this issue and getting technical. Enter "Reliability Man," the hero who must persevere against all the challenges thrown in his path.

It should come as no surprise that solder and solder joints are often at the center of attention in electronics assembly when discussing failures and reliability. Failed components aren't under the direct control of the assembly operation nor is a board failure. But the joining of the two? That's all you, contract manufacturers.



Thankfully, there is a significant amount of ongoing research into the specialty of solder joint reliability. Lead-free initiatives continue to drive this research. Industry watchers might say that we're just now beginning to understand a few of the long-term effects of removing lead from solder. Some space and mil-aero applications continue to specify tin-lead solder only. For these applications, one can argue that environmental impact is simply not a high-priority concern; their products are not generally destined for the landfill. But long-term reliability in an environment where repair is not an option and safety and survivability are critical is a high-priority concern.

But the solder evolution isn't limited to electronics. My neighbor is a plumber. Every Monday, he stops by my house to pick up three dozen eggs—about a day's production when one's residence comes complete with 50 laying hens—so I asked him how he likes lead-free solder for pipefitting. "It works," he said, "but it's a completely different skill set to use lead-free solder. It doesn't behave the same." Readers who work in the assembly industry know exactly what he's talking about.

Don't get me wrong; I'm not anti-RoHS. My point is that there is a great deal of ongoing research into materials, chemistries, thermal profiles, and precise process controls to create that completely different skill set my plumber neighbor had to teach himself. This is

a time of great change and innovation for solders and conformal coatings.

As we put this issue together, it became clear that we needed technical papers on the cutting-edge of failure and reliability research. Not everyone dives deeply into the technical papers, but for those of us whose job it is to reliably deliver failure-free products, we should be aware of the latest findings. This issue brings you some of the most insightful technical research from IPC APEX EXPO 2019.

Dr. Jennie Hwang kicks the issue off with a piece titled "Learn From the Wise." And Nihon Superior's Keith Sweatman brings us his work on solder paste volume optimization for low-temperature BGA reflow. Ray Prasad follows with his column, asking, "Would You Prefer Shorts or Opens in Your Products?".

Tony Lentz addresses solder powder size in his paper, "Size Matters: The Effects of Solder Powder Size on Solder Paste Performance." Then, Eric Camden's column discusses "The F Word"—failure. Following right behind is Rusty Osgood, et al., and their paper on "Low-temperature SMT Solder Evaluation."

Treating the surface of aluminum for low-temperature soldering is the topic of discussion in Divyakant Kadiwala's paper. Next, Chris Ellis looks at "Common Machine Errors and How to Avoid Them."

Thermaltronics' Michael Gouldsmith and Zen Lee consider "Failures and Reliability in Soldering" at the tip of the soldering iron. Then, Young Song, et al., share their findings in overcoming nodules and scratches on wire bondable plating.

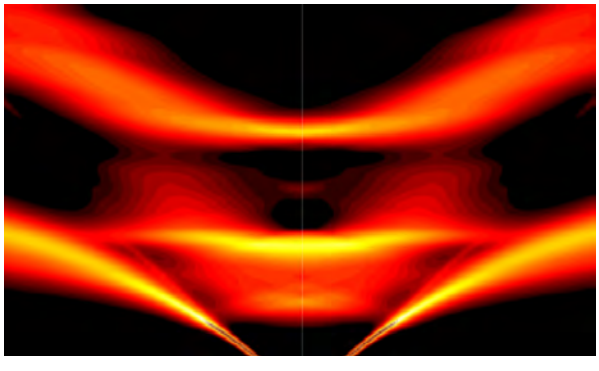
Ranjan Chatterjee and Dan Gamota bring us the iNEMI Smart Manufacturing Roadmap discussion on "Data Flow Considerations for the Electronics Manufacturing Industry." Then, Bob Wettermann discusses BGA and PCB warpage, and Alfred Macha continues his series on becoming a preferred supplier. This time, he goes into detail on "The Six Pillars."

So, put on your heat-resistant gloves; this issue is going to be as hot as an Arizona parking lot in July. Enjoy! **SMT007**

Nolan Johnson is managing editor of *SMT007 Magazine*. Nolan brings 30 years of career experience focused almost entirely on electronics design and manufacturing. To contact Johnson, click here.

Engineering Heat Transport

Scientists have discovered a way to alter heat transport in thermoelectric materials—a finding that may ultimately improve energy efficiency as the materials convert heat flow into electricity. Caltech theorists simulating the thermoelectric material lead selenide saw something surprising—a thermal wave that did not propagate. They determined the trick to potentially increasing energy efficiency in this material was to stop heat-carrying vibrational waves without thwarting electricity-bearing electrons.



To verify the discovery, they called on experimentalists to probe a real crystal. "Vibrational waves stop propagating in a perfect crystal because of nonlinear interactions between phonons," said Michael Manley of Oak Ridge National Laboratory (ORNL).

The experiment used neutron scattering at ORNL's Spallation Neutron Source and the National Institute of Standards and Technology's Center for Neutron Research and X-ray Scattering at Argonne National Laboratory's Advanced Photon Source.

The discovery improves understanding of thermoelectric performance and may enable unconventional heat transport in future materials. The research was published in *Nature Communications*.

(Source: Oak Ridge National Laboratory)

Learn From the Wise

SMT Prospects & Perspectives

by Dr. Jennie S. Hwang, CEO, H-TECHNOLOGIES GROUP

How can we get ahead in this digital world inundated with a gargantuan amount of information available to all? More sustainably, how can we stay ahead of the curve? Knowledge and wisdom are the fuel to propel us ahead; learning from the wise is the speedier path to acquire the fuel.

Warren Buffett

Business magnate Warren Buffett—one of the most successful investors in the world—holds a wealth of knowledge and wisdom. I wanted to attend the Berkshire Hathaway annual shareholders meeting regularly, but work schedule commitments persistently trumped my desire to attend regularly over the last 25 years. Nonetheless, I do make a point to read and study his iconic annual letter to shareholders, which I've found to be enlightening and thought-provoking.

Finally, I decided to make in-person attendance a priority in my work, scheduling way in advance. Last month, I had the pleasure to attend the wisdom-rich event. During the two days of the event, I absorbed or gained a bounty of observations, new ideas, renewed points, and verified thinking paths. I felt intellectually enhanced and reassured.

There were reportedly more than 40,000 in-person attendees from all over the world and millions watching the livestream of the event remotely. The cross-section of attendees is as wide as can be, from a nine-year-old to senior citizens, spanning all walks of life.

What has attracted so many people? Why are there so many fans and admirers of Buffett and his business partner Charles Munger? Perhaps the simple (overly simplistic) answer is the search for "wisdom" in investments. But more importantly, it is the wisdom above and beyond investment for how to live a long, wholesome, successful life.

Both the Oracle of Omaha, 88-year-old Warren Buffet, and his six-decade-plus business partner, 95-year-old Charlie Munger, devoted almost an entire day to addressing a variety of questions. They shared their wisdom during this meeting and covered topics ranging

Charles "Charlie" Munger

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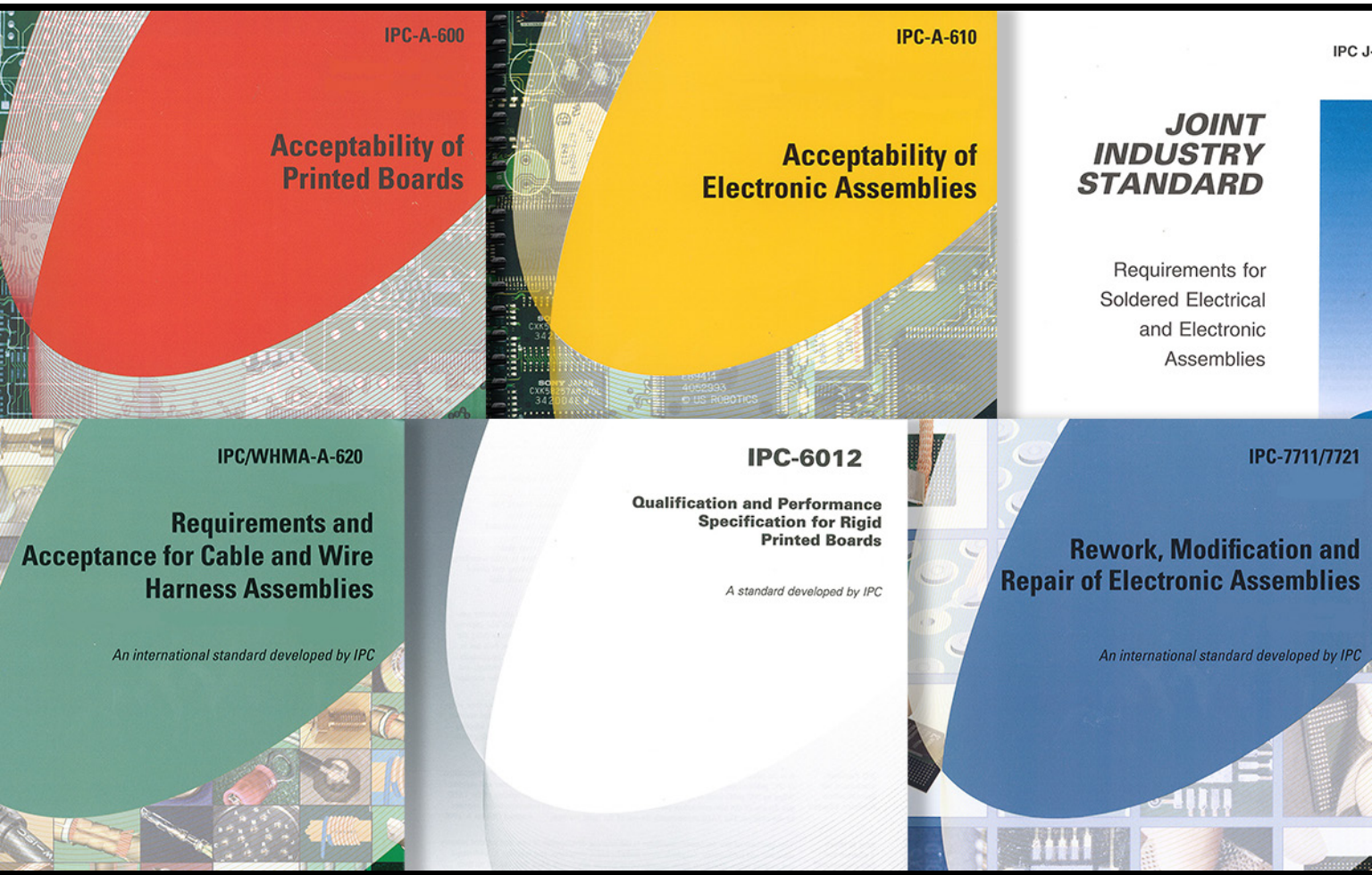

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from corporate governance and shareholder relations to human behavior and life lessons, acquisitions, and stock buyback. This wider interest than investment vividly manifested through a variety of questions and discussions, making the event even more intriguing and enriching.

This shareholders meeting is profoundly unique by any measure and in a way that is absent at many corporations, organizations, and institutions around the world. My attendance in-person this time provided me a distinctively deeper appreciation of alternative perspectives in a variety of areas.

Among many intriguing and striking observations, I want to share with our industry a select few that tugged at my heartstrings:

- The attendance of pre-teen kids (ages 9–13) brought by their parents was striking
- A 10-year-old girl asked, "What is your best personal investment?"
- An 11-year-old boy from China asked, "You said you know human nature and behavior better. How does knowing human nature and behavior help investment?"
- A 9-year old girl attending for the third time asked about investing in leading technologies was humored by Buffett, saying, "You should be rich now."
- A 13-year-old boy asked Buffett's thoughts on delayed gratification. Buffett's response was quite educational: "Saving is a necessary thing to do in life, the delayed gratification may not be a qualifier for all individuals or families in all circumstances, but I spend only 2–3 cents on every dollar."
- A 27-year old asked, "I'm young and have a lot to learn. I want to be a successful investment manager. How and when will I know I am ready to successfully manage other people's money?"
- A young woman literally kangarooed with a baby as a first-time attendee who won the "lottery" to ask a question
- Foreign country college students arrived at 3:00 a.m. on the meeting day
- When Mr. Buffett was asked: "What do you value the life most?" he responded, "Time, and I have been able to control my time, and a job that is not limited by physical abilities."
- Mr. Munger was asked, "You have worked with Buffett for more than six decades. Why is he much richer than you?" He answered with his signature touch of humor, "For a lot of reasons. Maybe he is smarter or works harder, but Albert Einstein was not rich."
- Mr. Munger said, "No idea is good enough at any price," which is a superb business acumen
- Mr. Buffett stated, "We always carefully measure ourselves on what we do." Discipline is the key!
- Mr. Munger said, "Warren is a learning machine. He reads a lot"; Buffett added, "Charlie reads more books in a week than I do in a month." This truly coincides with the following famed Buffett quotes, which I couldn't appreciate or agree with more!
  - "I think you should read everything you can. In my case, by the age of 10, I'd read every book in the Omaha public library about investing, some twice. You need to fill your mind with various competing thoughts and decide which make sense."
  - "Read 500 pages every day. That's how knowledge works. It builds up like compound interest."

On investments, corporate governance, financials, and capital allocation, I felt a deeper sense for the concepts used in measuring a company's performance by operating earnings rather than EBITDA. Mr. Buffett has been championing this approach for some time. I equally understood better the rationale behind the Buffett's stock buyback. I can also see more clearly why Mr. Buffett prefers equity investment to bonds. Not surprisingly, on Buffett's experience in corporate governance, to paraphrase his remarks, " I have served on more than 25 corporate boards. So-called independent directors are not independent at all." How true!

Other learning advice is well reflected by an interview by the *Wall Street Journal* from May of this year, Munger stated, "Part of the reason I've been a little more successful than most people is I'm good at destroying my own best-loved ideas. I knew early in life that would be a useful knack, and I have honed it all these years, so I'm pleased when I can destroy an idea that I have worked very hard on over a long period of time. And most people aren't." How pragmatic! Indeed, objectivity is the engine for building up one's wisdom.

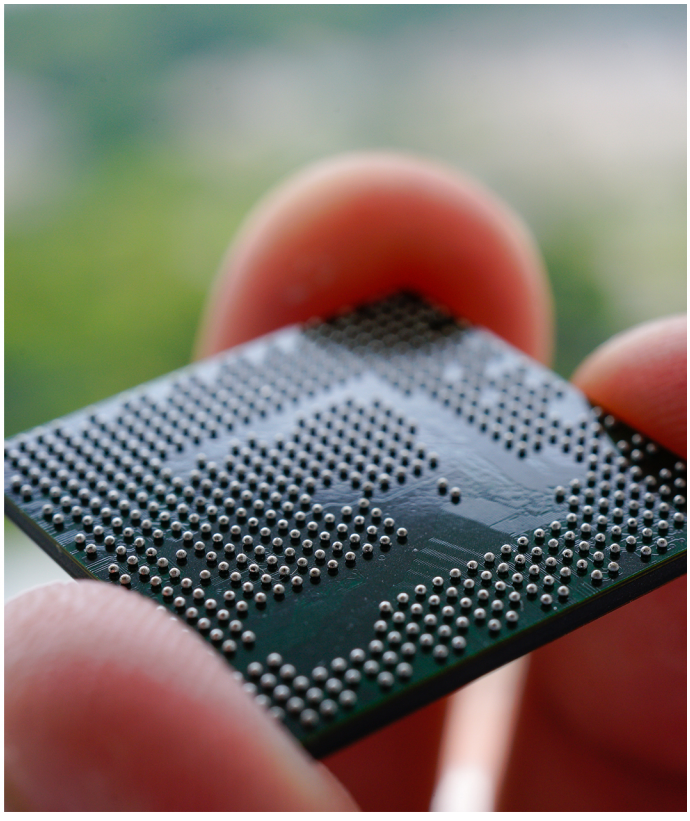
Overall, my takeaway thoughts go to the following inferred and inducted points:

1. The Buffett/Munger duo create an intellectual synergy. What a fortunate partnership. Good partnership is power!
2. There are profound reasons for the overwhelming reverence and admiration for the two
3. Pre-teen attendance points to the next generation's high aspiration
4. Pre-teen grasp of high-level knowledge demonstrates ever-increasing competitiveness in future generations
5. Learning from the wise is a speedier way to get ahead
6. Mr. Munger's advice, "No idea is good enough at any price," speaks volumes for astute business decision-making
7. A company's healthy and sustainable performance correlates so well with level-headed leadership, including the board and management. This applies to any organization.
8. Further appreciation of Buffet's iconic concepts and practices:
   - "The best investment you can make is an investment in yourself. The more you learn, the more you'll earn."
   - "We don't have to be smarter than the rest. We have to be more disciplined than the rest."
   - "If you want to soar like an eagle in life, you can't be flocking with the turkeys."
   - "Always associate yourself with people who are better than you."
   - "Someone is sitting in the shade today because someone planted a tree a long time ago."
   - "Outstanding long-term results are produced primarily by avoiding dumb decisions rather than by making brilliant ones."
   - "It's good to learn from your mistakes. It's better to learn from other people's mistakes.

How can we get ahead—and stay ahead—of the curve? Speed is the key. Among the fundamental traits, continually and consistently learning from the wise is the speedier path to acquire the fuel to propel us forward. **SMT007**

Dr. Jennie S. Hwang—an international businesswoman and speaker, and business and technology advisor—is a pioneer and long-standing contributor to electronics hardware manufacturing as well as to the environment-friendly lead-free electronics implementation. Among her many awards and honors, she was inducted to the International Hall of Fame–Women in Technology, elected to the National Academy of Engineering, an R&D-Stars-to-Watch, and YWCA Achievement Award. Having held senior executive positions with Lockheed Martin Corp., Sherwin Williams Co., SCM Corp, and CEO of International Electronic Materials Corp., she is currently CEO of H-Technologies Group providing business, technology and manufacturing solutions. She is the Chairman of Assessment Board of DoD Army Research Laboratory, serving on Commerce Department's Export Council, National Materials and Manufacturing Board, Army Science and Technology Board, various national panels/committees, international leadership positions, and the board of Fortune-500 NYSE companies and civic and university boards. She is the author of 500+ publications and several books, and a speaker and author on trade, business, education, and social issues. Her formal education includes four academic degrees as well as the Harvard Business School Executive Program and Columbia University Corporate Governance Program. For more information, please visit www.JennieHwang.com. To read past columns or contact Hwang, click here.

Optimizing Solder Paste Volume for Low-temperature Reflow of BGA Packages



Feature by Keith Sweatman
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Abstract

The need to minimize thermal damage to components and laminates, reduce warpage-induced defects to BGA packages, and save energy is driving the electronics industry towards lower process temperatures. For soldering processes, the only way that temperatures can be substantially reduced is by using solders with lower melting points. Because of constraints of toxicity, cost, and performance, the number of alloys that can be used for electronics assembly is limited, and the best prospects appear to be those based around the eutectic in the Bi-Sn system, which has a melting point of about 139°C.

Experience so far indicates that such Bi-Sn alloys do not have the mechanical properties and microstructural stability necessary to deliver the reliability required for the mounting of BGA packages. Options for improving mechanical properties with alloying additions that do not also push the process temperature back over 200°C are limited. An alternative approach that maintains a low process temperature is to form a hybrid joint with a conventional solder ball reflowed with a Bi-Sn alloy paste. During reflow, there is mixing of the ball and paste alloys. But it has been found that to achieve the best reliability, a proportion of the ball alloy has to be retained in the joint, particularly in the part of the joint that is subjected to maximum shear stress in service—which is usually the area near component side. The challenge is then to find a reproducible method for controlling the fraction of the joint thickness that remains as the original solder ball alloy.

Empirical evidence indicates that, for a particular combination of ball and paste alloys and reflow temperature, the extent to which the ball alloy is consumed by mixing with the paste alloy depends on the volume of paste deposited on the pad. If this promising method of achieving lower process temperatures is to be implemented in mass production without compromising reliability, it would be necessary to have a method of ensuring the optimum proportion of ball alloy left in the joint after reflow can be consistently maintained.

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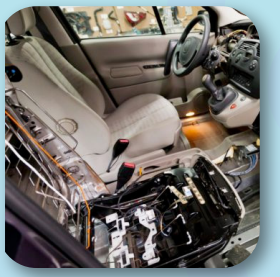

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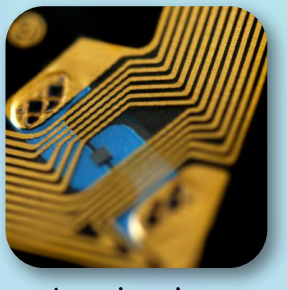

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In this article, the author explains how the volume of low-melting-point alloy paste that delivers the optimum proportion of retained ball alloy for a particular reflow temperature can be determined by reference to the phase diagrams of the ball and paste alloys. The example presented is based on the equilibrium phase diagram of the binary Bi-Sn system, but the method could be applied to any combination of ball and paste alloys for which at least a partial phase diagram is available or could be easily determined.

Introduction

The dependence of the electronics industry on solder to provide the reliable connections necessary to turn a collection of individual components into a functional circuit has created an ongoing dilemma that has challenged the industry since its inception. The main consideration in the design of electronic components is functionality; whether it be to provide a specific resistance, capacitance, or inductance in passive components; logical processing in integrated circuits; and responsiveness in sensors or just electrical connectivity. A need to survive the thermal profile required to form a joint with a molten metal has been an annoying complication.

The industry has had a fairly easy start with the Sn-Pb eutectic that has a relatively low melting point of 183°C and mechanical properties and microstructural stability that have been considered to be the benchmark for reliability in service. Because of the need to maximize heat transfer into the joint to get the substrates to wetting temperature, process temperatures (e.g., soldering tool tip temperature, wave solder bath temperature, reflow oven peak temperature) had to be substantially higher than that 183°C melting point. However, with proper process control, the temperature/time profile to which the most sensitive parts of the component were exposed could be kept within a safe limit.

The move to Pb-free solder brought a renewed challenge because the alloy endorsed by IPC as "the Pb-free alloy of choice for the electronics industry"—Sn-3.0Ag-0.5Cu (SAC305)—does not start to melt until 217°C, which is 34°C higher than the melting point of the Sn-37Pb it was replacing. However, as long as the higher process temperatures could be accommodated by the use of resins and polymers that could survive the higher thermal profiles, the electronics industry was able to adapt to this new alloy.

When the problem with higher process temperatures was not just thermal degradation of materials but gross deformation of component packages the challenge moved to a new level. Integrated circuit packages have evolved into complex stacks of a wide range of materials with very different coefficients of thermal expansion so that as the package heats the differential expansion of bonded layers results in warpage of the package. The problem is exacerbated by the temperature gradients that develop within the package as a result of variations in thermal conductivity and thermal mass. The extent of warpage can mean that at its peak the warpage in area array packages is sufficient to cause complete separation of joints at their extreme edges (Figure 1).

Depending on the temperature at which that peak separation is reached for a particular component, the separation can take different forms:

1. Unreflowed solder paste can be split with some adhering to the solder ball and some to the pad
2. Unreflowed solder paste adheres only to the solder ball and is lifted off the pad
3. Unreflowed solder paste adheres only to the pad with the solder ball detaching from the solder paste

Depending on how the warpage changes as a function of temperature, the solder paste might reflow while separation is at its peak. When, later in the reflow profile, the component returns to its original shape, there is no certainty that the separate and now molten solder will coalesce as the activity of the flux, which facilitates wetting and coalescence might have been exhausted. In the case of Type 1 separation, the result is a defect known as head-

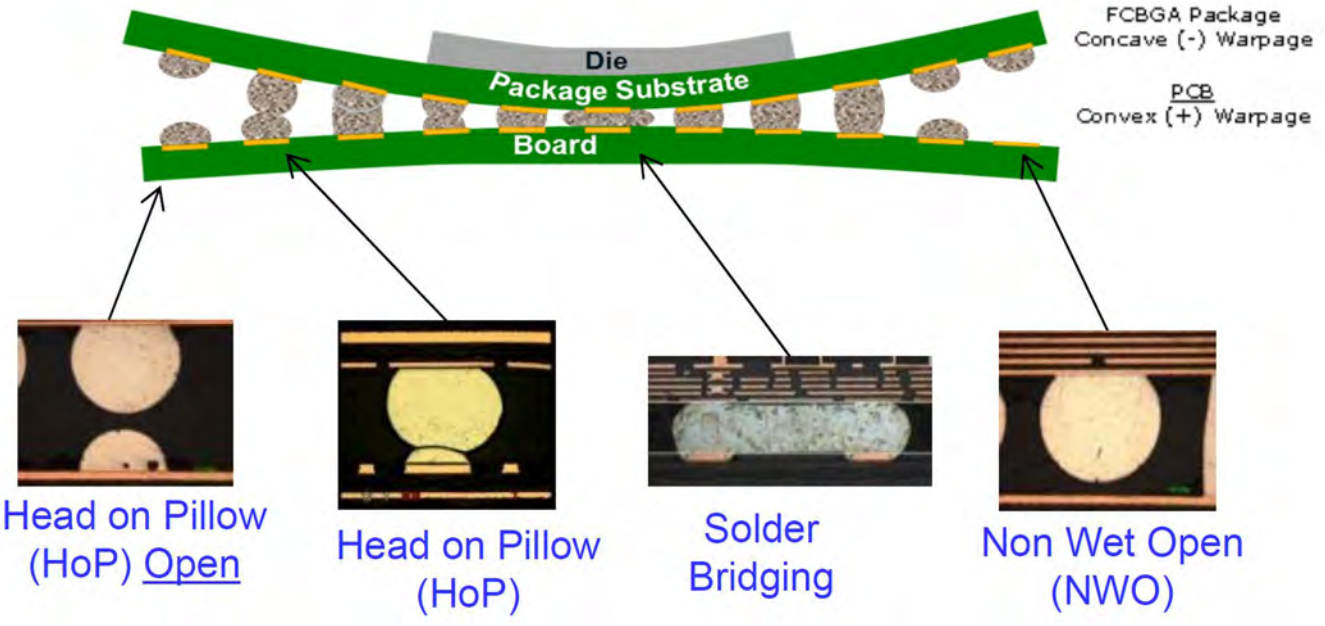

Figure 1: Defects caused by dynamic warpage of FCBGA components during reflow soldering [1].

in-pillow (HIP). In the case of Type 2 and 3 separation, the result is a defect known as a non-wet open (NWO).

Because the design of the layers of the package and the selection of materials is determined by many complex considerations that cannot be compromised by a need to minimize warpage at the peak process temperature, ways of reducing process temperature have had to be sought. For many years, the electronics industry has been aware of—and made limited use of—solders based around the Sn-57Bi eutectic that has a melting point of 139°C. With that melting point, the peak process temperature could be kept below 200°C, at which the component warpage is low enough that the risk of separation defects is significantly reduced. However, this alloy is brittle and cannot deliver the reliability required in joints to area array packages. The reliability of Sn-Bi alloys can be improved by reducing the bismuth content and adding small amounts of elements, such as silver or lead, but the alloy still cannot match the reliability of the higher melting point alloys. And as the composition moves further away from the Sn-Bi eutectic, the liquidus temperature increases, necessitating high process temperature.

A solution that the industry is now evaluating is to continue to use a conventional SAC alloy for the BGA ball but to reflow solder the package to the substrate with a low-melting-point alloy based around the Sn-57Bi eutectic. With this technique, it is possible to securely attach a BGA package to a substrate with a peak process temperature under 200°C. The result of this process is a joint such as that in Figure 2 [2].

Reliability testing of these mixed alloy or hybrid joints indicates that as long as a sub-

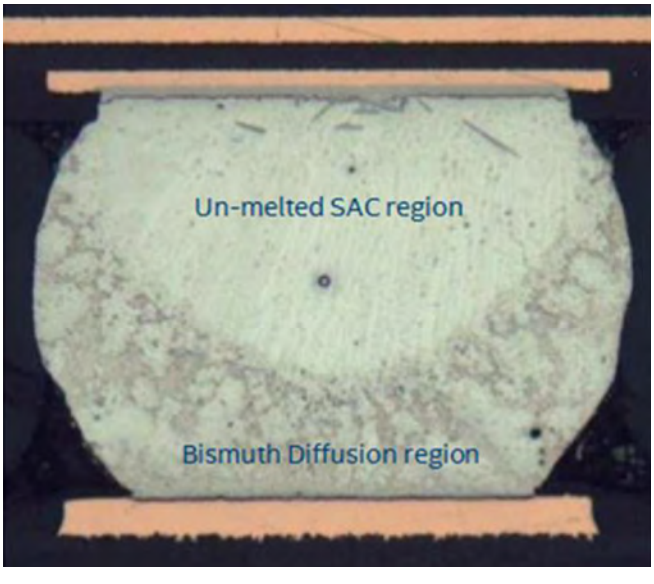

Figure 2: Typical joint formed by reflow of an Sn-Ag-Cu solder ball with an Sn-Bi low-melting-point solder.

stantial part of the SAC ball alloy remains after the soldering process, the joints have adequate reliability. The distribution of strain in a typical assembly means that it tends to be concentrated in the outer areas of solder close to the interface with the component package. If the solder in that area is an alloy that is known to deliver the required service life under the expected conditions, then the reliability of the mixed alloy joint is comparable with that of a joint that is reflowed with the same alloy as the BGA ball.

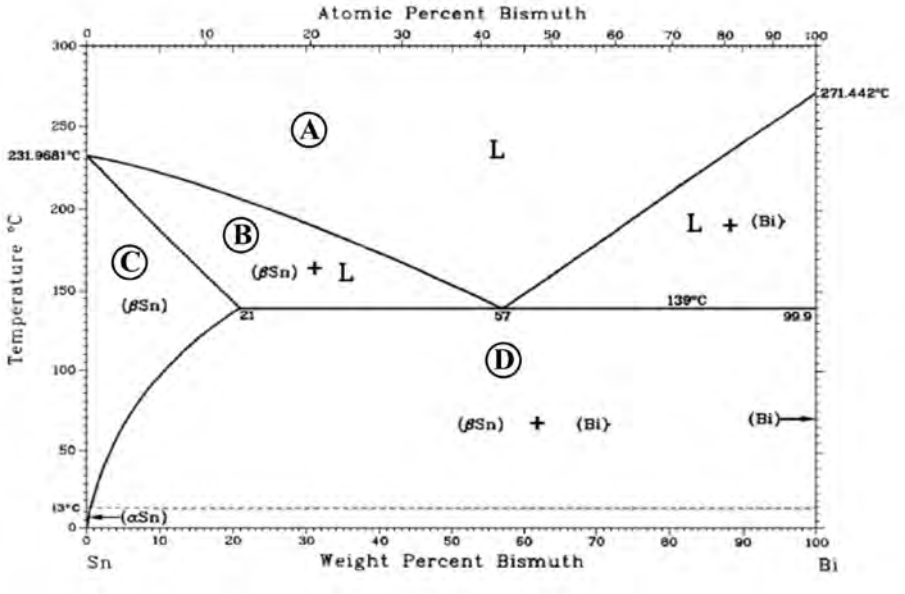

Figure 3: The Sn-Bi equilibrium phase diagram.

The challenge with this technique has been determining how to complete the mixed alloy reflow soldering process with sufficient of the original ball alloy remaining on the component that an adequate level of reliability can be achieved.

While there has been much discussion about "Bi diffusion" from the low-melting-point solder into the SAC alloy, the purpose of this article is to explain that the extent to which the BGA ball is lost to the mixed alloy is determined by the thermodynamics of the alloy system made up of the solder ball and the solder paste. Those thermodynamics are neatly summarized in one of the basic tools of the material scientist—the equilibrium phase diagram.

The Equilibrium Phase Diagram

The equilibrium phase diagram can be considered a map of the location of phases—liquid or solid—in space defined by the dimensions of composition and temperature. Where vapor pressures are significant, a third dimension is pressure. But in the case being considered here, at the process temperatures being used, the alloy constituents have relatively low vapor pressures so that dimension need not be considered.

For a particular composition at a specific temperature, an equilibrium phase diagram will show what phases are present and their composition. With the application of the "lever rule," the relative proportions of the phases present at any such point can be calculated. For a binary system (i.e., in the case of an alloy, a mixture of two metals), the phase diagram is two-dimensional. The phase equilibria for three elements can be presented in a three-dimensional diagram, or if the level of one element is fixed, as a two-dimensional pseudo-binary plot. For more than three elements the level of one or more of the elements has to be fixed to reduce the number of dimensions to three or two.

Figure 3 is the equilibrium phase diagram for the binary Sn-Bi system on which the low-melting-point alloys used in mixed alloy reflow are currently based. An alloy with the composition and temperature at Point A would be entirely liquid. An alloy with the composition and temperature at Point B would be a roughly 50/50 mixture of liquid and solid Sn-Bi alloy with about 10wt% Bi in solid solution. An alloy with the composition and temperature Point C would be completely solid with about 5wt% Bi in solid solution. An alloy at the composition and temperature Point D would be completely solid with a roughly 50/50 mix of nearly pure Bi and Sn with about 15% Bi in solid solution.

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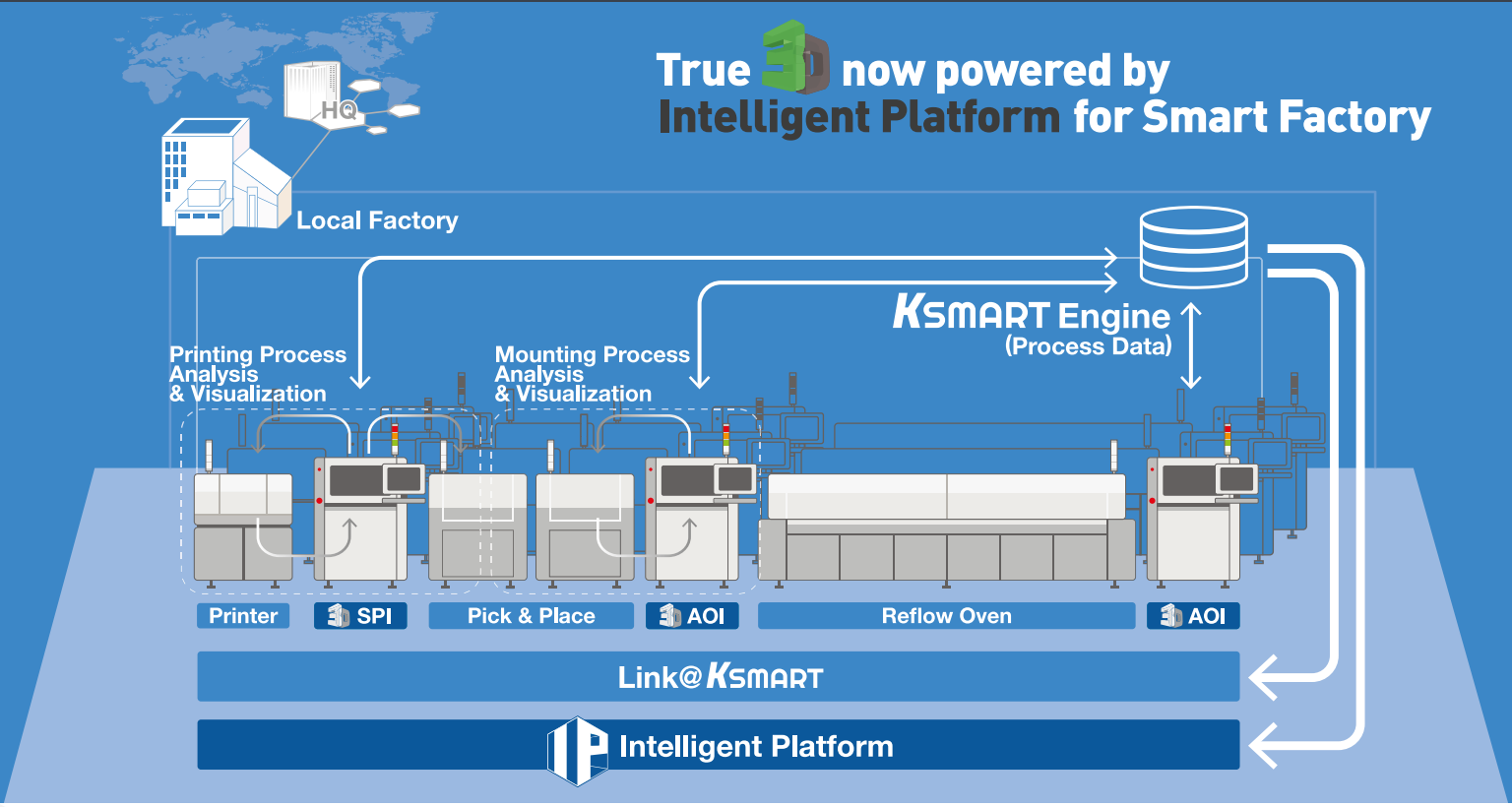

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The Model

A solder ball and the solder in the deposit of solder paste on which it is mounted can be considered as an isolated system in that all the materials that will form the final solder joint are already present. In that regard, it is different from a joint being wave soldered in which there is a virtually unlimited supply of solder on which the joint substrates can draw to form a fillet.

To the extent that during the soldering process, there can be some reaction between the copper or nickel substrates, those substrates should also be considered as part of the system; whether those reactions need to be taken into account depends on the size of the solder ball. In some very small joints, the Sn from the solder and the solder ball consumed in the reaction with the substrates to form the intermetallic compounds Cu_6Sn_5 or Ni_3Sn_4 could be a significant fraction of the total amount of Sn available in the solder ball/solder paste system. However, for the purposes of explaining the method of calculating the extent to which the solder ball is consumed in the process of reflow with a low-temperature solder, that effect will be neglected. Where reactions with substrates are significant, they can be factored into the calculations.

For the purpose of explaining the method, the system will be simplified to a solder ball and the solder in the solder paste. In a solder paste, the solder itself accounts for about 50% of the paste volume. The remainder is the flux medium that determines the printing characteristics and tackiness of the paste, provides the fluxing action required to facilitate coalescence of the powder particles into a single mass of solder and the wetting of the joint substrates, and controls the surface tension of the liquid solder that determines the joint profile. However, once the solder ball has been wetted, the flux medium plays no role in the process that determines how much of the BGA ball is lost to the mixed alloy.

To further simplify the explanation of the method, it will be presumed that the solder ball is pure Sn and the low-melting-point solder a simple binary Sn-Bi alloy. For the low-Ag SAC alloys often preferred for BGA spheres because their greater compliance reduces the incidence of pad cratering in drop impact, the alloy is already about 98.5wt% Sn (with the remainder typically being 1wt% Ag and 0.5wt% Cu). Even SAC305 is 96.5wt% Sn (with the remain-der 3wt% Ag and 0.5wt% Cu).

The process that determines the extent of penetration of the LMP alloy into the ball involves only the Sn. The Ag is present only as the Ag_3Sn intermetallic compound and the Cu as the intermetallic compound Cu_6Sn_5—both of which remain in fairly stable equilibrium with the Sn phase over the likely temperature range of the mixed alloy reflow process. Therefore, they would play no role in the interactions that occur in the reflow process. With the likely tolerances on the quantities of the materials in the system, the difference in the outcome with a pure Sn ball should not be very different from that with SAC alloy balls. However, with the basic principle established, allowance can be made for the presence of Ag and Cu in the BGA ball alloy.

Commercial Bi-Sn alloys usually contain a small alloying addition to improve their properties—typically 0.5wt% of Ag or Sb. Over the temperature range of the mixed alloy reflow process, the Ag has no solubility in Bi and would be expected to be present in the low-melting-point solder as the Ag_3Sn intermetallic compound. Sb is completely soluble in Bi and Sn and could play a role in the determination of the final equilibrium, but its effect would be small and will not be taken into account in the proposed model. Again, allowance could be made for its effect once the basic model is recognized.

If the interaction between the solder ball and solder from the solder paste is allowed to proceed to equilibrium, the factors that ultimately determine the extent to which the solder ball alloy is replaced by mixed alloy are:

- The location of the solidus line on the Sn-rich side of the Sn-Bi phase diagram
- The composition of the low-melting-point alloy
- The peak reflow temperature

If the time that the system is held at reflow temperature is limited, then the system might not reach thermodynamic equilibrium. In that case, another factor determining the extent the solder ball is replaced by the mixed alloy will be the time at reflow temperature.

The Process

The process that occurs during reflow can be described as follows:

1. The solder powder in the paste melts and coalesces into a single mass of molten solder
2. The molten solder wets the substrate pad and the lower part of the solder ball
3. The flux medium—having done its job of facilitating reflow and wetting—is displaced from the solder mass but largely remains as a coating on the molten solder, contributing to heat transfer and protecting the molten solder and the lower part of the solder ball from oxidation
4. Sn from the BGA ball starts to dissolve in the molten LMP alloy, increasing the Sn content of the molten solder
5. Dissolution of Sn from the solder ball continues until the Sn content of the molten solder moves into the two-phase region of the phase diagram when a solid phase—an Sn-Bi solid solution—starts to freeze out of the melt
6. Dissolution of Sn from the BGA ball into the molten solder continues until the composition reaches the solidus composition at the reflow temperature at which point dissolution of Sn stops
7. With the system then completely solid, the only mechanism by which further intermixing of the LMP alloy and the BGA ball can continue is by solid-state diffusion; during the time available in a commercial reflow, the profile would be negligible

If at this point the temperature is increased, some of the mixed alloy will melt, and there will be an opportunity for more Sn to dissolve from the BGA ball until the composition reaches the solidus at that higher temperature. This process is illustrated schematically in Figure 4 for a low-melting-point alloy that is 50wt% Bi/50wt% Sn and a reflow temperature of 165°C. At the end of Stage 3, the Sn-Bi alloy is fully molten (Figure 4, Point A). If the flux has done its job, the solder will have fully wetted the solder ball as well as the substrate. Sn from the ball would be starting to dissolve in the molten solder, and the Sn content of the molten increases.

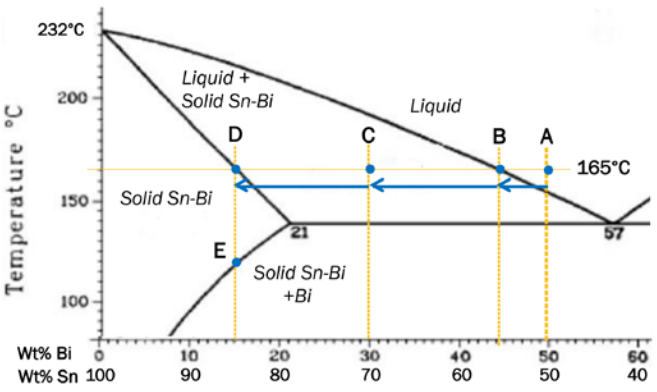

Figure 4: The process of a pure Sn BGA ball dissolving into Sn-50Bi solder at 165°C.

At Point B, the Sn content of the molten Sn-Bi alloy has reached saturation (approximately 58wt%Sn). As more Sn dissolves in the remaining liquid, a solid phase starts to freeze out. That phase is a solid solution of Bi in Sn with a composition of approximately 86% Sn. By the time the system reaches Point C (approximately 70wt% Sn), the wt% solid Sn-Bi in the semi-molten solder mix can be calculated by the lever rule as:

$$\frac{BC}{BD} \times 100\% \Rightarrow \frac{(42-30)}{(42-14)} \times 100\% \Rightarrow \frac{12}{28} \times 100\% \approx 43\%$$

Sn from the solder ball continues to dissolve until it reaches a level of approximately 86wt% (Point D) when the mix of low-melting-point alloy and Sn is completely solid. While the temperature remains no higher than 165°C, the system remains solid with solid-state diffusion the only mechanism as the Bi can migrate further into the solder ball.

The only other change in the system predicted by the phase diagram is that as the system cools the mixed alloy phase will cross the solvus line at about 130°C (Point E), which means that the Bi level has reached its saturation limit at that temperature and Bi will start to precipitate out of the Sn-Bi alloy.

Effect of Bi Level in Low-Melting-Point Alloy

In the example described in the previous section, the length of the line AD provides an indication of the amount of Sn that will dissolve from the ball alloy before the melting point of the Sn-Bi alloy reaches the reflow temperature and the mixing process stops. If the starting alloy were 60% Bi rather than 50%, then more Sn would have to dissolve from the ball alloy before Sn content of the alloy mixture reaches the solvus limit at that temperature. In reality, for a particular reflow temperature, the location of the liquidus line on the Bi-rich side of the eutectic sets an upper limit on the Bi content of the solder that is usable at a particular target reflow temperature.

Effect of Reflow Temperature

As the temperature increases, the amount of Bi that can be held in solid solution decreases. Put another way, as the Bi content of the alloy increases, when the temperature at which the alloy starts to melt, solidus decreases. In the phase diagram, that trend is reflected in the slope of the solidus line that runs from the melting point of Sn to the limit of Bi solubility in Sn at the eutectic temperature. That means that as the reflow temperature increases, the amount of Sn that will dissolve from the solder ball before the solidus line is crossed and the mixed alloy is completely frozen.

Calculating Actual Sn Dissolved

For a given volume of low-melting-point solder, the amount of Sn that will be dissolved from the solder ball at a particular temperature before the composition of the resulting mixed alloy reaches the solvus can be calculated from the slope of the solidus line.

In geometric terms, the solidus line on the Sn-rich side of the Sn-Bi equilibrium phase diagram in Figure 5 can be described by Equation 1:

$$wt\%Sn_S = 79+(T_R-139) \times (100-79)$$

Where $\%Sn_S$ is the minimum Sn content of the Sn-rich Sn-Bi alloy that is solid at the chosen reflow temperature T_R. The maximum wt%Sn at the eutectic temperature of 139°C is 79 (Figure 5). When T_R is set as the melting point of pure Sn (232°C), the equation calculates the wt%Sn at 100% Sn (allowing for rounding errors).

For a given quantity of a low-melting-point Sn-Bi alloy with a chosen Sn content and the chosen reflow temperature, this equation can be used to calculate how much Sn will dissolve from the solder ball before the mixing process is brought to a halt by the composition of the resulting alloy crossing the solidus line. If the objective is that a significant proportion of the original solder ball remains at the completion of the reflow profile, then the volume of solder paste and its initial Sn content would have to be carefully calculated, accounting for the size of the solder ball and the Sn content of its alloy.

Calculating Paste Volume for Reliable BGA Joints

For the purpose of demonstrating the application of this approach to the design of reliable mixed alloy reflow, the reflow of a 500-µm sol-

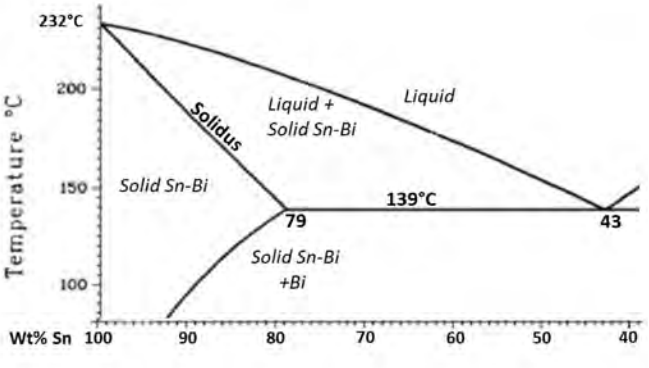

Figure 5: Phase diagram used for expressing the slope of the solidus line as a function of Sn content and temperature.

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der ball will be used as an example. A number of other simplifying assumptions are made in constructing this model, but in its practical application to the selection of assembly parameters, actual data would be used.

As in the earlier example, the paste alloy will be a 50wt% Sn Sn-Bi solder. This alloy is slightly hypereutectic with respect to Sn but still has a relatively low liquidus temperature of around 155°C (Figure 4).

Because of the large difference in density between the solder and flux medium, a stencil-printable solder paste is typically about 50% solder by volume. The density of a 50wt% Bi Sn-Bi solder can be estimated by calculation at about 8.4g/cm^3.

For simplicity, the paste deposit will be assumed to be circular so that the volume of paste is can be calculated as Equation 2:

$$\frac{\pi d^2}{4} x\ t$$

Where d is the diameter of the paste deposit and t the thickness. With the chosen volume fraction of solder in the paste deposit and the estimated density of the low-melting-point alloy, the weight of solder can be estimated as a function of the thickness and/or diameter of the deposit.

For a reflow temperature of 165°C, the wt% Sn at which the mixed alloy will reach its solidus composition can be calculated by Equation 1 as around 84.5wt%. The amount of Sn required to raise the Sn level in the molten solder can be calculated on the basis of the weight of solder in the paste deposit. It is the dissolution of that Sn that will determine how much of the original solder ball will be lost to the mixed alloy phase in the final joint. A complication is that, in calculating the amount of Sn that will be dissolved from the solder ball to reach the solidus composition at the reflow temperature, allowance has to be made for the diluting effect of the increase in the volume of the molten phase. The calculations made on this basis for a range of paste deposit thicknesses are set out in Table 1.

Paste Thickness cm	Paste Volume cm^3	Solder Volume cm^3	Solder Weight (g)	Wt of Sn (g)	Wt of Sn from Ball (g)	Volume of Sn from Ball cm^3
0.0010	1.9635E-06	9.81748E-07	8.2467E-06	4.1233E-06	1.8459E-05	0.000003
0.0020	3.92699E-06	1.9635E-06	1.6493E-05	8.2467E-06	3.6918E-05	0.000005
0.0030	5.89049E-06	2.94524E-06	2.4740E-05	1.2370E-05	5.5377E-05	0.000008
0.0040	7.85398E-06	3.92699E-06	3.2987E-05	1.6493E-05	7.3836E-05	0.000010
0.0050	9.81748E-06	4.90874E-06	4.1233E-05	2.0617E-05	9.2294E-05	0.000013
0.0060	1.1781E-05	5.89049E-06	4.9480E-05	2.4740E-05	1.1075E-04	0.000015
0.0070	1.37445E-05	6.87223E-06	5.7727E-05	2.8863E-05	1.2921E-04	0.000018
0.0080	1.5708E-05	7.85398E-06	6.5973E-05	3.2987E-05	1.4767E-04	0.000020
0.0090	1.76715E-05	8.83573E-06	7.4220E-05	3.7110E-05	1.6613E-04	0.000023
0.0100	1.9635E-05	9.81748E-06	8.2467E-05	4.1233E-05	1.8459E-04	0.000025
0.0110	2.15984E-05	1.07992E-05	9.0713E-05	4.5357E-05	2.0305E-04	0.000028
0.0120	2.35619E-05	1.1781E-05	9.8960E-05	4.9480E-05	2.2151E-04	0.000030
0.0130	2.55254E-05	1.27627E-05	1.0721E-04	5.3603E-05	2.3997E-04	0.000033
0.0140	2.74889E-05	1.37445E-05	1.1545E-04	5.7727E-05	2.5842E-04	0.000035
0.0150	2.94524E-05	1.47262E-05	1.2370E-04	6.1850E-05	2.7688E-04	0.000038
0.0160	3.14159E-05	1.5708E-05	1.3195E-04	6.5973E-05	2.9534E-04	0.000040
0.0170	3.33794E-05	1.66897E-05	1.4019E-04	7.0097E-05	3.1380E-04	0.000043
0.0180	3.53429E-05	1.76715E-05	1.4844E-04	7.4220E-05	3.3226E-04	0.000046
0.0190	3.73064E-05	1.86532E-05	1.5669E-04	7.8343E-05	3.5072E-04	0.000048
0.0200	3.92699E-05	1.9635E-05	1.6493E-04	8.2467E-05	3.6918E-04	0.000051
0.0210	4.12334E-05	2.06167E-05	1.7318E-04	8.6590E-05	3.8764E-04	0.000053
0.0220	4.31969E-05	2.15984E-05	1.8143E-04	9.0713E-05	4.0610E-04	0.000056
0.0230	4.51604E-05	2.25802E-05	1.8967E-04	9.4837E-05	4.2455E-04	0.000058
0.0240	4.71239E-05	2.35619E-05	1.9792E-04	9.8960E-05	4.4301E-04	0.000061
0.0250	4.90874E-05	2.45437E-05	2.0617E-04	1.0308E-04	4.6147E-04	0.000063

Table 1: Calculation of dissolution of Sn from solder ball as a function of the thickness of the solder paste deposit.

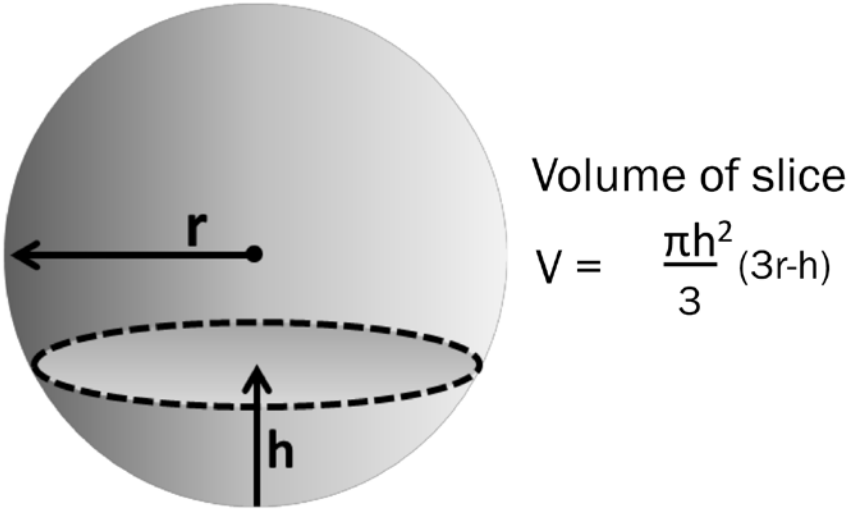

Figure 6: Equation from which the distance h of penetration of the mixed alloy into a solder ball can be estimated.

To interpret the volume of Sn that dissolves in the low-melting-point paste in terms of the extent to which the mixed alloy penetrates into the ball, the volume of a slice of a sphere is used as an approximation (Figure 6).

Because of the difficulty of solving the equation in Figure 6 to calculate h when V is known, a graphical solution is used (Figure 7).

In the example illustrated in Figure 7, a 100-µm thickness, 500-µm print of Sn-50wt%Bi solder paste reflowed at 165°C would result in the formation of a zone of mixed solder that would penetrate about 220 µm into a 500-m pure Sn solder ball.

Conclusions

In practice, as indicated in Figure 2, the interface between the mixed alloy and the remaining solder ball is not planar, but since it is determined by temperature, follow the thermal gradients. However, the point of this exercise is not to make an accurate prediction but to demonstrate the underlying principle that the extent of penetration of the mixed alloy phase into solder can be calculated on the basis of the following:

- The location of the solvus line in the relevant equilibrium phase diagram
- The composition of the low-melting-point solder
- The volume of low-melting-point solder in the solder paste deposit
- The peak reflow temperature

How far the mixed alloy penetrates into the solder ball will depend on the volume of the solder ball.

If a limit is to be set on the amount of original ball alloy that has to be retained to ensure the reliability of the joint than the paste alloy,

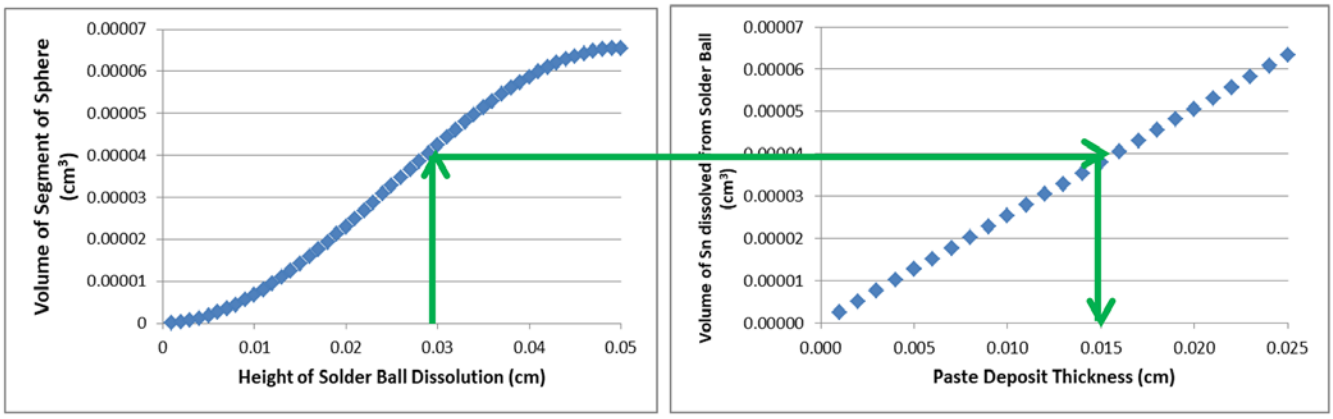

Figure 7: The plot on the right is the volume of Sn dissolved in the low-melting-point solder as a function of the thickness of a 500-µm diameter paste deposit, and the plot on the left is the height of a slice of a 500-µm diameter solder ball as a function of the volume of the slice.

the paste volume and the reflow temperature have to be set so that the volume of the ball alloy that will have to dissolve to bring the mixed alloy to its solidus composition at that temperature is no greater than the loss of original alloy volume that can be tolerated. SMT007

References

1. S. Mokler, R. Aspandiar, K. Byrd, O. Chen, S. Walwadkar, K.K. Tang, M. Renavikar, & S. Sane, "The Application of Bi-Based Solders for Low-Temperature Reflow to Reduce Cost While Improving SMT Yields in Client Computing Systems," Proceedings of the SMTA International Conference, September 2016.

2. H. Fu, R. Aspandiar, J. Chen, S. Cheng, Q. Chen, R. Coyle, S. Feng, B. Hardin, M. Krmpotich, S. Mokler, J. Radhakrishnan, M. Ribas, B. Sandy-Smith, K.K. Tang, G. Wu, A. Zhang, & W. Zhen, "iNEMI Project on Process Development of BiSn-Based Low-Temperature Solder Pastes–Part II: Characterization of Mixed Alloy BGA Solder Joints," Proceedings of Pan Pacific Microelectronics Conference, 2018.

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Flexible Generators Turn Movement Into Energy

Wearable devices that harvest energy from movement are not a new idea, but a material created at Rice University may make them more practical.

The Rice lab of chemist James Tour has adapted laser-induced graphene (LIG) into small, metal-free devices that generate electricity. Like rubbing a balloon on hair, putting LIG composites in contact with other surfaces produces static electricity that can be used to power devices. For that, thank the triboelectric effect, by which materials gather a charge through contact. When they are put together and then pulled apart, surface charges build up that can be channeled toward power generation.

"This could be a way to recharge small devices just by using the excess energy of heel strikes during walking, or swinging arm movements against the torso," Tour said.

In experiments, the researchers connected a folded strip of LIG to a string of light-emitting diodes and found that tapping the strip produced enough energy to make them flash. A larger piece of LIG embedded within a flip-flop let a wearer generate energy with every step as the graphene composite's repeated contact with skin produced a current to charge a small capacitor.

"The nanogenerator embedded within a flip-flop was able to store 0.22 millijoules of electrical energy on a capacitor after a 1-kilometer walk," said Rice postdoctoral researcher Michael Stanford, lead author of the paper. "This rate of energy storage is enough to power wearable sensors and electronics with human movement."

(Source: Rice University)

Electronics Industry News and Market Highlights

Revenues for NAND Flash Brands 1Q Fall by 23.8% QoQ While Prices Fall Non-stop in 2Q ▶

Besides the effects from the traditional off-season first quarter this year, the weakening demand in the fourth quarter of last year has pushed smartphone and server OEMs to begin adjusting their inventories, according to DRAMeXchange.

Mobile Services Market in APAC to Increase Focus on B2B and B2B2C Segments ▶

The mobile services market in Asia-Pacific (APAC) is expected to focus more on business models for the business-to-business (B2B) or business-to-business-to-consumer (B2B2C) segments as a result of declining revenue from traditional services.

NB-IoT Device Shipments Reached 53 Million Units in 2018 ▶

According to a new research report from IoT analyst firm Berg Insight, global shipments of NB-IoT devices reached 53 million units in 2018, and are expected to almost triple to 142 million units in 2019.

Global Solar Photovoltaic Services Market 2019-2023 ▶

The global solar photovoltaic services market is expected to post a CAGR of more than 16% during the period 2019-2023, according to the latest market research report by Technavio.

Commercial Aircraft Production to Hit Record High With Renewed Competition Between Airbus and Boeing ▶

The revival of competition between Boeing and Airbus is expected to result in record delivery of the highly popular narrow-body platforms and a 9.4% year-on-year growth in production.

Medical Device Contract Manufacturing Market to Reach $93.1B by 2024 ▶

The medical device contract manufacturing market is expected to reach $91.3 billion by 2024, up from an estimated $55 billion in 2019 at a CAGR of 10.6% over the forecast period.

India PC Market Declines YoY for the Third Consecutive Quarter in 1Q19 ▶

The India traditional personal computing (PC) market declined for the third consecutive quarter in the first quarter of 2019, according to IDC's Asia/Pacific Quarterly Personal Computing Device Tracker.

EMEA PC Market Will Approach Stability in 2019 ▶

Shipments of traditional PCs—a combination of desktops, notebooks, and workstations—in the EMEA region will total 71.3 million in 2019, nearly flat year-on-year.

Global Space Electronics Market Report ▶

The global space electronics industry analysis highlights that the market generated $1.27 billion in 2018 and is expected to grow at a CAGR of 5.22% during 2019–2024.

Smart Manufacturing Platform Market Worth $10.8 Billion by 2024 ▶

The smart manufacturing platform market is projected to grow from $4.4 billion in 2019 to $10.8 billion by 2024; it is expected to record a CAGR of 19.7% over the forecast period.

Would You Prefer Shorts or Opens in Your Products?

SMT Solver
Feature Column by Ray Prasad, RAY PRASAD CONSULTANCY GROUP

In my last column, I discussed realistic goals to aim for regarding defect levels. I also mentioned, but it is worth repeating, that it may be unrealistic to have zero defect in products right after reflow, but we want zero defect in products we ship to the customer. That is why we spend so much time and money on inspection, test, and repair even though they are non-value added process steps, but they are necessary steps since you don't want the customers to discover those defects.

As to the question raised in this column, would I prefer shorts or opens in my products? Neither, thank you. But if I do have to choose, I would choose a more desirable defect, if there is such a thing. But what is a desirable defect? A defect that would never escape inspection and test and would be caught before shipping the product to the customer. Before I answer this question, let me briefly review industry standards on defects and major types of defects that really matter in the functioning of a product.

Industry Standards and Major Types of Defects

There are three major types of standards in our industry: IPC, EIA, and J-STD. Each one has a different focus, reasoning, and target audience. Having been deeply involved with various standards, chairing many of them over the years, and still chairing many others, let us save this topic for future columns. For now, I will focus on two standards that deal with acceptance criteria for defects.

IPC-610 is a thick and widely purchased IPC standard that specifies acceptance criteria for all types of defects with color photos and very little text. It is easy to read and follow and is primarily targeted at inspectors and operators working on the SMT line.

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The main standard for acceptance criteria of defects in electronics assemblies is J-STD-001. IPC-610 provides a visual representation of the acceptance requirements established in J-STD-001. This standard (J-STD-001) has very few photos and is full of text and tables targeted at quality and process engineers.

If you go through these standards, there are hundreds of different types of defects. There are week-long classes and certification programs for these standards. However, if you think about it, there are only two types of defects that matter for the functioning of electronic assemblies: shorts or bridges between adjacent leads or opens in solder joints. All of the test methods, such as in-circuit test (ICT) and functional tests only look for shorts and opens because other types of defects can-not be detected by these tests and they don't affect the functionality of the boards. Thus, it goes without saying that we can simplify IPC-610 and J-STD-001, but don't hold your breath.

What Defect Should You Aim For?

As I just mentioned, ICT and functional tests can only find opens and shorts; they are not looking for any other types of defects because they cannot find them. If the defects that you see don't fall into open or short category, you can safely classify them as "others." Examples of "others" are insufficient, tombstoning, drawbridge, part movement, etc.

Bridge is the most objective type of defect. No two people will disagree if you show them a bridge. Meanwhile, opens, especially if hidden, can easily escape even ICT and functional tests because they are most likely to make intermittent connections due to pressures exerted during bed of nail testing or ICT.

There is another type of open called insufficient solder joint. Many people will disagree with me calling insufficient joint an open joint, but we all agree that insufficient solder joint is not a total open today but will most likely become an open tomorrow or months later. Therefore, we might as well call it an open. Unlike bridges, insufficient solder joint is the most subjective defect you can find. It is very likely that two well-trained inspectors will disagree whether an insufficient solder joint is acceptable or not. To be on the safe side, you might as well consider it an open.

Pitch	PPM
16 mils (0.4 mm)	13,088
20 mils (0.5 mm)	18,78
25 mils	950
50 mils	650

Table 1: QFP defect levels vs. pitch.

Industry Findings: Which Defect Is More Prevalent?

In my last column, I quoted a paper by Stig Oresjo [1] and Table 1, which shows the level of defects depending on the pitch of a gull-wing device.

Based on Table 1, it is obvious that lower pitches will result in much higher defects because lower pitch devices increase the com-plexity of the manufacturing processes, such as handling, printing, placing, and soldering.

The same paper by Oresjo also analyzed the types of defects for all the components:

- Opens: 46%
- Shorts: 22%
- Insufficient: 17%

As I noted earlier, an insufficient solder joint is an open about to happen in the near future. So, if we combine open and insufficient, almost two-thirds of defects (63%) are opens, 22% are shorts, and the remainder are 15%. This is the average of all types of components in Orse-jo's paper.

The results in the paper on gull-wing devices were even more significant:

- Opens: 65%
- Insufficient: 11%
- Shorts: 16%
- Others: 8%

If you combine opens and insufficient, the number is alarming: 76%. Shorts are only 16% of the total.

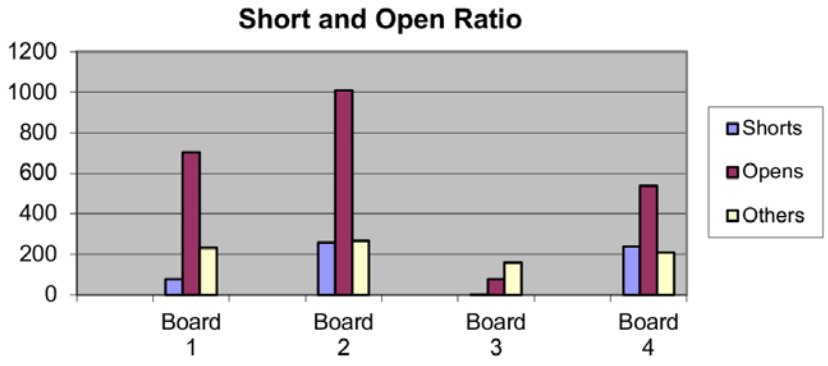


Figure 1: Shorts, opens, and others at a medical company.

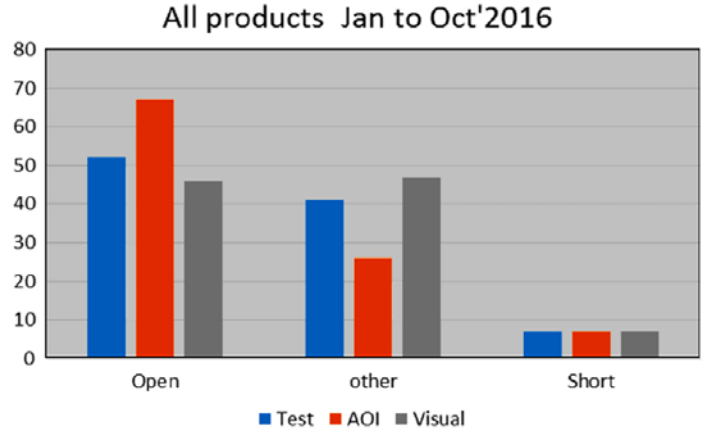


Figure 2: Shorts, opens, and others at an automotive company.

My Findings: Which Defect Is More Prevalent?

This next section details my own findings at two major companies during my consulting assignments—one at a U.S. medical company and the other at a major Japanese electronics company that supplies to the global automotive company (Figures 1 and 2).

Recommendations

An assignment for you is to look at your own data for some of your higher volume products. Put them in three categories: shorts, opens, and others. Put insufficient, tombstoning, drawbridge, part movement, etc., into the open category. For the ones that you cannot put into short or open, call them "others."

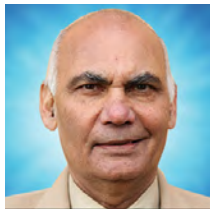
I bet that your findings will be no different than what I quoted from Orsejo's paper or my findings. I am sure of it since I have looked at the data at many companies over the years. If I'm wrong, I will buy you a drink (nonalcoholic) if we end up meeting at any industry events, such as SMTAI or IPC APEX EXPO.

My recommendation is to have six to eight times more shorts than opens, but let me be clear that I am not saying have lots of shorts and opens; I am talking about the ratio of shorts to opens. You always want to work for the total to be on a declining trend, but the total should have more shorts than opens. Why? Shorts will never escape your inspection and test steps, but opens may escape no matter how rigorous your inspection and test regimes are. Opens will be discovered eventually either at a customer site, or even worse, in the field when it is too late and too expensive to fix.

The best part of my recommendation is that it's very easy to achieve. All you need to do to achieve more shorts than opens is to design land patterns and stencils correctly. I may talk about those subjects in future columns. **SMT007**

References

1. Oresjo, S. "Year 1999 Defect Level and Fault Spectrum Study," SMTAI Proceedings, 2000.



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Size Matters:
The Effects of Solder Powder Size on Solder Paste Performance

Feature by Tony Lentz
FCT ASSEMBLY

Abstract

Solder powder size is a popular topic in the electronics industry due to the continuing trend of miniaturization of electronics. The question commonly asked is, "When should we switch from Type 3 to a smaller solder powder?" Solder powder size is usually chosen based on the printing requirements for the solder paste. It is common practice to use IPC Type 4 or 5 solder powders for stencil designs that include area ratios below the recommended IPC limit of 0.66. The effects of solder powder size on the printability of solder paste have been well documented.

The size of the solder powder affects the performance of the solder paste in other ways. Shelf life, stencil life, reflow performance, voiding behavior, and reactivity/stability are all affected by solder powder size. Testing was conducted to measure each of these solder paste performance attributes for IPC Type 3, 4, 5, and 6 SAC305 solder powders in both water-soluble and no-clean solder pastes. The performance data for each size of solder powder in each solder paste flux was quantified and summarized. Guidance for choosing the optimal size of solder powder is given based on the results of this study.

Keywords: Solder powder size, solder paste performance, solder paste printing, reflow, voiding, solder paste stability

Introduction

Size matters. That simple statement is true for many things in life. Small hands are better for speed texting. Large people are better at playing offensive or defensive line in the national football league. Antibodies are microscopically small but they play a key role in our health and well-being. Who doesn't want a large cup of coffee (Figure 1)?

Figure 1: Size matters.

Size also matters in the world of solder paste. The size of the solder powder used in a solder paste has

IPC Type	Less Than 0.5% Larger Than (µm)	10% Max. Between (µm)	80% Min. Between (µm)	10% Max. Less Than (µm)
3	60	45–60	25–45	25
4	50	38–50	20–38	20
5	40	25–40	15–25	15
6	25	15–25	5–15	5

Table 1: Solder powder size (adapted from Table 3-2 of IPC J-STD-005A).

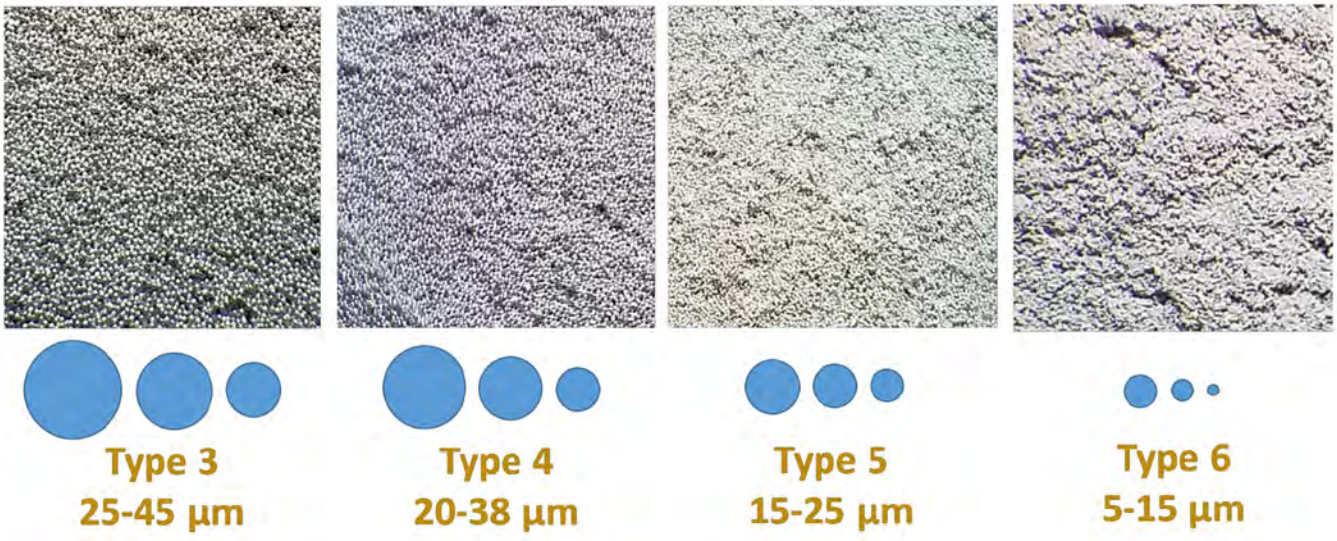

Figure 2: IPC Type 3, 4, 5, and 6 solder powders.

an effect on solder paste performance. Solder powder sizes are classified by type in the IPC standard J-STD-005 (requirements for soldering pastes) [1]. Table 3-2 details the solder powder size ranges for each type, and an excerpt is shown in Table 1.

The main particle size range is normally associated with the type. For example, Type 3 solder powder mainly falls within the 25–45 µm size range; therefore, Type 3 solder paste may be labeled as "Type 3 (25–45 µm)." Figure 2 shows Type 3, 4, 5, and 6 sizes of solder powder.

Why use Type 4, 5, or 6 solder powder rather than Type 3? The main reason to use smaller solder powders in solder paste is to improve the printability for miniature components. As solder powder size decreases, the solder pastes can be printed through smaller stencil apertures. If the "5-ball" rule is followed from the IPC-7525 stencil design guidelines standard [2], then the minimum aperture size through which printing can occur can be calculated for each solder powder size [3]. These calculations for minimum aperture size were performed using five times the maximum solder powder size of the main range (Table 2).

Generally speaking, Type 3 solder paste can be used for components ranging down to the 0402 imperial package size. Most solder paste users prefer Type 4 solder paste for 0201 imperial, micro BGAs, and similar components. Type 5 solder paste is used for even smaller soldering applications like 01005 imperial components [4] or when Type 4 solder paste does not print adequately. Type 5 and 6 solder pastes

IPC Type	Size Range (µm)	Size Range (mil)	Minimum Aperture Size (mil)
T3	25–45	1.0–1.8	9
T4	20–38	0.8–1.5	7.5
T5	15–25	0.6–1.0	5
T6	5–15	0.2–0.6	3

Table 2: Solder powder size and minimum stencil aperture size for printing using the 5-ball rule.

are used for dispensing applications, such as jet printing. Type 6 solder paste is also used for other ultra-fine-feature applications [5 & 6].

Aside from the printing capabilities given by smaller solder powders [7], other performance changes occur when smaller solder powders are used. Stencil and shelf life of the solder pastes may be shortened when using smaller solder powders. Smaller solder powders have a higher potential for random solder balling and graping. Voiding behavior can also be affected by a change in solder powder size. The goal of this study is to quantify the performance for IPC Type 3, 4, 5, and 6 SAC305 (Sn / Ag 3.0% / Cu 0.5%) solder powders in both water-soluble and no-clean solder pastes. Experimental data for each solder paste is compared and contrasted, and recommendations for the optimal use of each solder paste are given.

Methodology

Surface Area of Solder Powder and Reactivity

As the solder powder size decreases, the surface area of solder powder increases for a given mass (Table 3) [8]. These surface areas were calculated using the middle value in the main particle size range.

The surface area of the solder powder is important because it plays a role in the reactivity of the solder powder. As the surface area increases, the rate of reaction increases. Imagine trying to dissolve a cube of sugar in a cup of water. It takes time and a lot of stirring for the sugar to dissolve completely. If the same mass of granular sugar is mixed into a cup of water, it dissolves much more quickly (Figure 3).

IPC Type	Middle Surface Area of 1 Kg (m^2)	Normalized Area	Amount of Surface Area Over T3 (%)
T3	22.9	1.00	—
T4	27.7	1.21	21
T5	40.2	1.75	75
T6	80.3	3.50	350

Table 3: Solder powder size and surface area for a 1 Kg mass.

After one minute of mixing, the granulated sugar dissolved completely while the cube of sugar was partially dissolved. The granulated sugar has a higher surface area than the cube of sugar, which enables the granulated sugar to dissolve more quickly.

The same principle is true with solder powder. The higher surface area of smaller solder powder types causes the rate of reaction to be higher than the larger solder powder types. Therefore, smaller solder powder types are more susceptible to oxidation when exposed to air [9]. The chemical reactions for oxidation of tin (Sn) are as follows:

$$Sn_{(s)} + \tfrac{1}{2} O_{2\,(g)} = SnO_{(s)}$$

$$Sn_{(s)} + O_{2\,(g)} = SnO_{2\,(s)}$$

As oxygen reacts with the solder powder, metal oxides are created. The primary oxide that forms on SAC305 alloy is SnO [10]. The solder paste flux removes the metal oxides and helps to slow further oxidation [8]. Oxidation of the solder powder can continue, albeit slowly, as long as the solder paste is exposed to air. Mixing and increased temperature accelerate this process. This reaction process

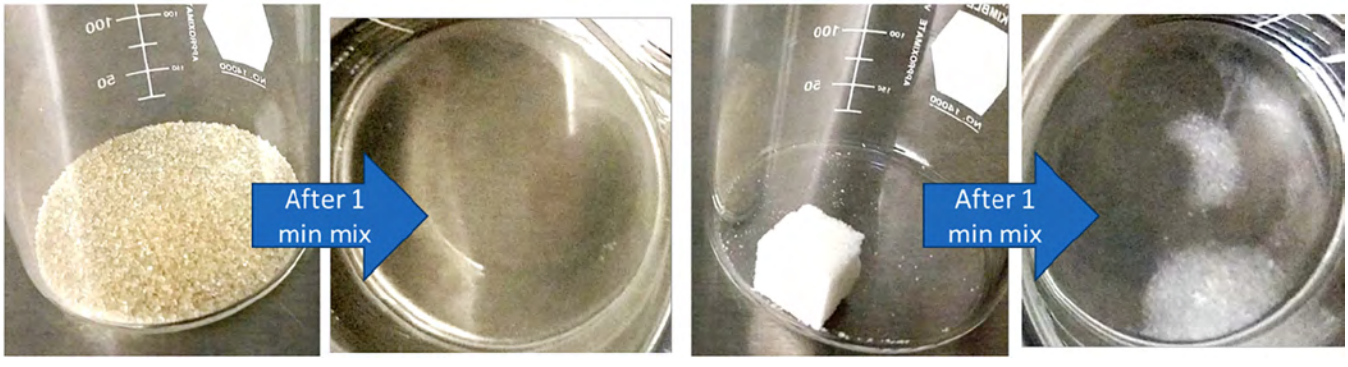

Figure 3: Granular sugar (L) versus cubed sugar (R) dissolved in water with a 1-minute mix time.

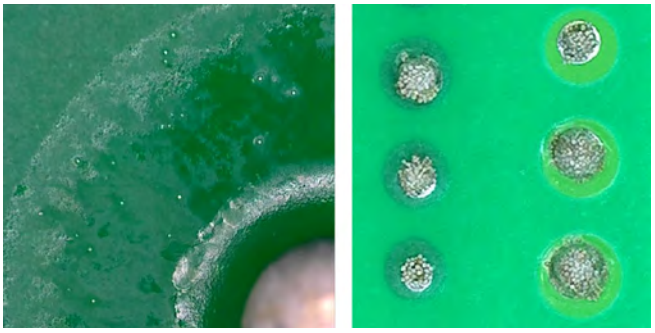

Figure 4: Random solder balling (L) and graping (R).

of solder powder oxidation and oxide removal by the flux tends to thicken the solder paste. Over time, this can lead to clogged stencil apertures and cause the solder paste to stick to the squeegee blades. The usable stencil life of the solder paste may be shortened by the smaller solder powders. The good news is that solder paste fluxes are made with ingredients to protect the solder powder, which significantly slows this oxidation process.

Oxidation of the solder powder also occurs during reflow. The solder paste flux reacts with and removes the oxides from the solder powder during reflow. As the solder powder size decreases, more flux is required to deal with these oxides. When reflowing solder pastes made with smaller solder powder sizes, the flux may run out of activity; then, oxides are left on the solder powder which interferes with the proper coalescence of the solder. Solder pastes made with smaller solder powders are susceptible to potential issues like random solder balling and graping (Figure 4).

The shelf life for solder pastes made with smaller solder powders may also be shorter than solder pastes made with larger solder powders. During storage, the flux can react with the solder metal, creating metal salts. The flux activity is depleted through this reaction over time, and this reaction is faster for smaller solder powder sizes. As more reactive solder pastes age, the solder paste may thicken and a change from a smooth and creamy appearance to more of a dull grainy appearance (Figure 5).

Print and reflow characteristics may degrade over time if the solder paste is too reactive. Solder pastes are formulated to prevent or slow this process. Storing the solder paste in a refrigerator also helps to slow this process and preserve the intended performance characteristics. Proper storage is especially important to prolong the shelf life of solder pastes made with smaller solder powder sizes.

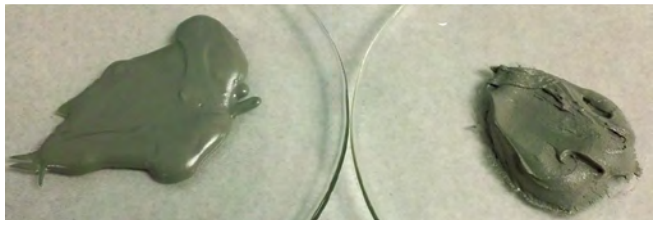

Figure 5: Fresh solder paste (L) versus aged solder paste (R).

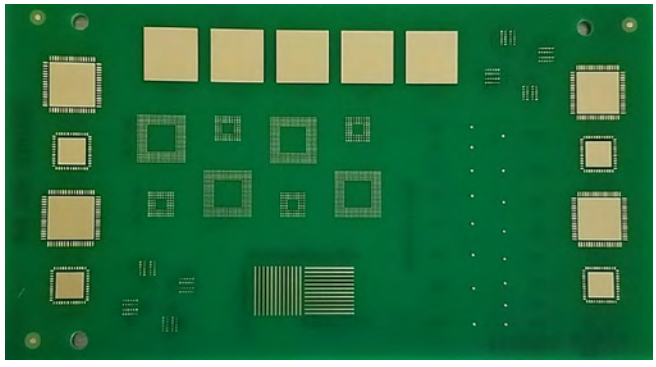

Figure 6: Print and reflow test circuit board.

Materials and Test Methods

The circuit board used for this experimentation is shown in Figure 1. This circuit board is made of FR-4 and is 0.062 inches thick with etched copper pads and electroless nickel immersion gold (ENIG) surface finish.

This print and reflow test board has patterns used to quantify printed solder paste volume, wetting or spread, random solder balling, graping, and voiding (Figure 7).

Solder Pastes

Eight solder pastes were made for this study, including four water-soluble solder pastes and four no-clean solder pastes. The no-clean flux has an IPC J-STD-004 classification of ROL0, and the water-soluble flux is classified as ORH1. The solder alloy chosen was SAC305 (Sn/Ag 3.0%/Cu 0.5%). The solder paste metal concentrations were varied based on solder powder size (Table 4).

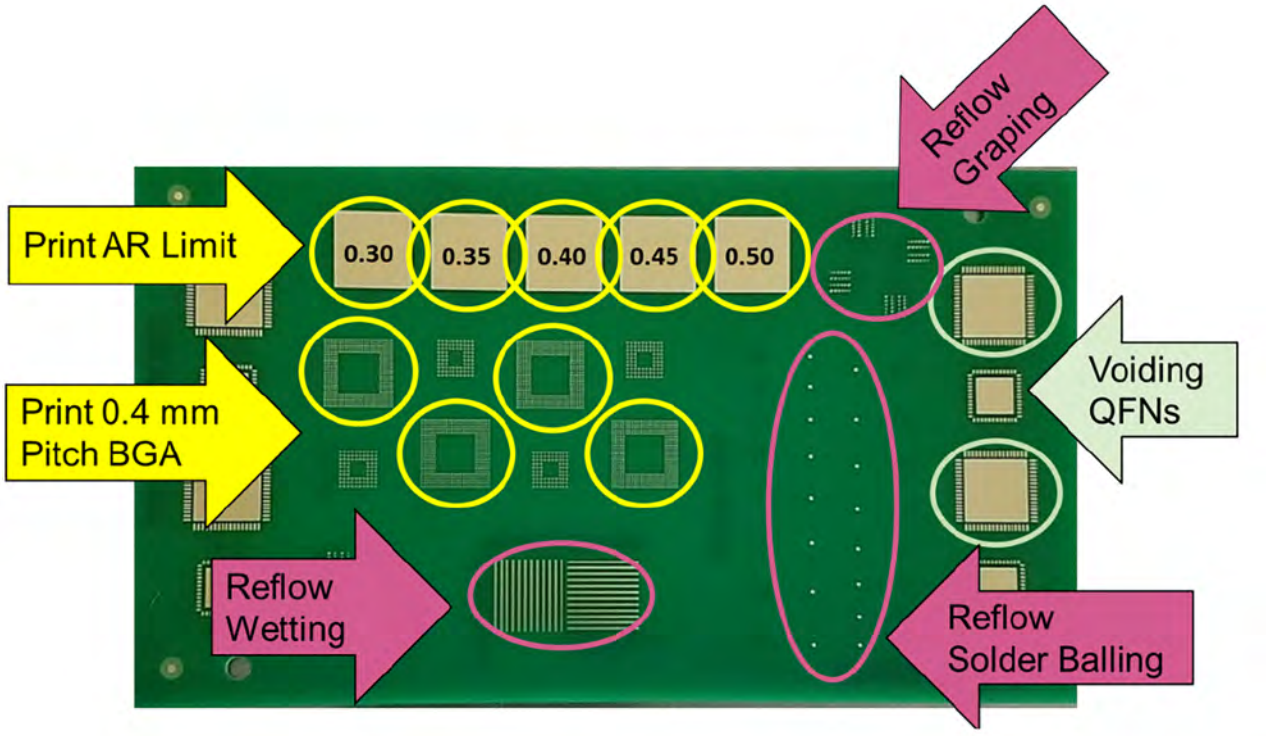

Figure 7: PR test board patterns for quantifying print, reflow, and voiding performance.

IPC Type	No-Clean Metal Content (% wt)	Water-Soluble Metal Content (% wt)
T3	88.5	88.5
T4	88.3	88.3
T5	88.0	88.0
T6	87.5	87.5

Table 4: Solder paste metal concentrations.

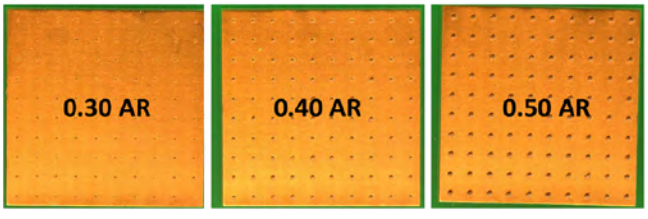

Figure 8: Printed solder paste in the area ratio (AR) limit patterns.

Print Performance

Print performance was measured using area ratio limit patterns, which have stencil aperture area ratios ranging from 0.30 up to 0.50 in 0.05 AR steps. The stencil is made of 5-mil (127 microns), fine-grain (2–5 µm) stainless steel without nano-coatings. The aperture sizes range from 6–10 mils in the area ratio limit patterns. These small area ratios show the printing limit of the solder paste (Figure 8).

Print performance was also measured using 0.4-mm pitch ball grid arrays (BGAs), which have a stencil aperture area ratio of 0.50. The apertures are 10 mils square with 2-mil radiused corners ("squircles"). Solder paste volumes were measured in the area ratio limit, and 0.4-mm BGA patterns using a solder paste inspection system (SPI) and statistical analysis performed to compare solder paste performance. Lower limits of area ratios are suggested for each solder paste.

Stencil Life and Response to Pause

A print-and-pause test was conducted on each solder paste to measure stencil life and response to pause. The process used is shown in Figure 9.

The solder paste volume data for the area ratio limit patterns and the 0.4-mm BGA patterns was compared for each time. During this test, significant drops in solder paste volume indicate that thickening or drying of the solder paste has occurred. This data is used to give a suggested stencil life for each solder paste.

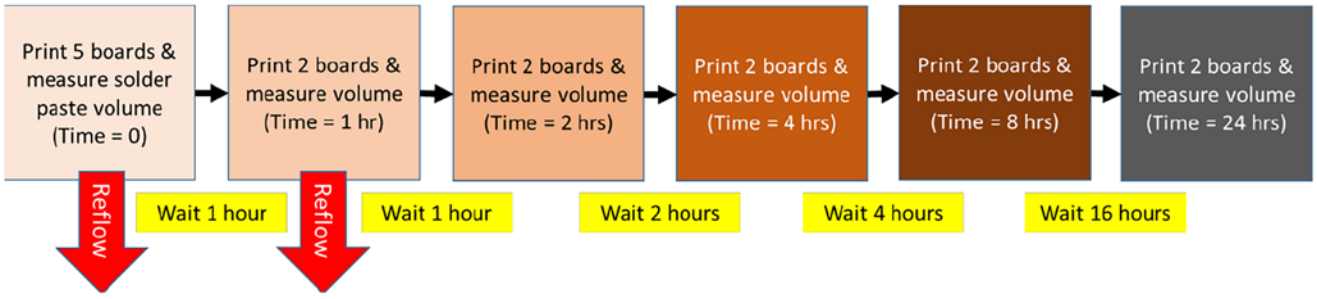

Figure 9: Print-and-pause test method.

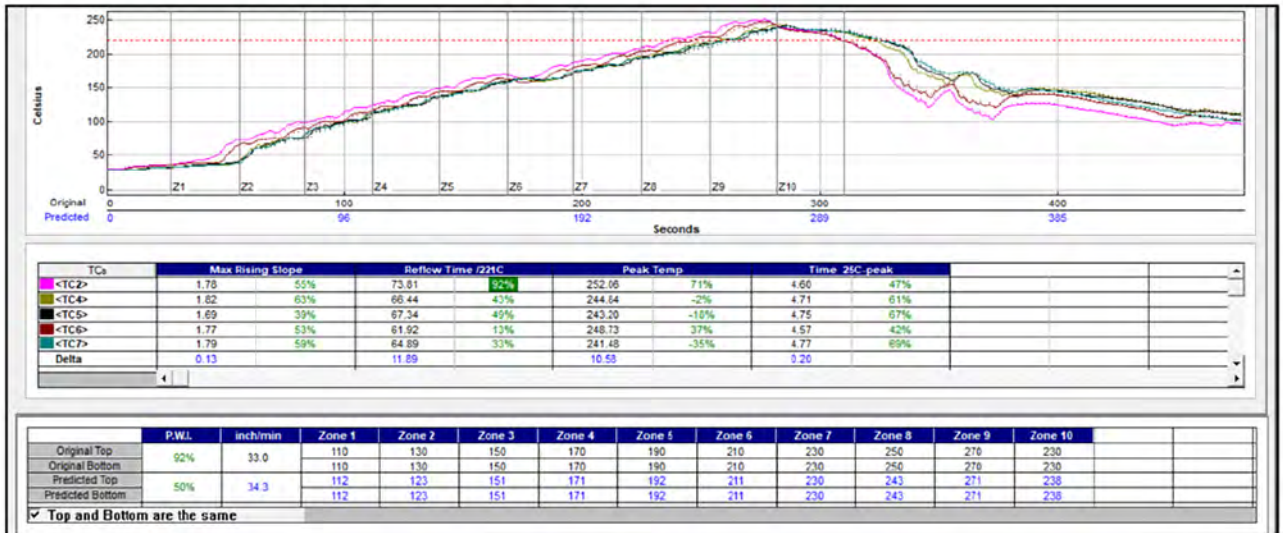

Figure 10: Linear ramp to spike (RTS) reflow profile.

The first five circuit boards from the print-and-pause test were used for reflow performance and voiding measurement. The next two circuit boards from the print-and-pause test were placed on a counter and left open to the air overnight. They were reflowed the following day (after 24 hours) and reflow performance was measured.

Reflow Profile and Performance

Reflow was done in a 10-zone convection reflow oven. A linear ramp-to-spike (RTS) type profile was used (Figure 10).

The parameters for the profile are summarized in Table 5.

Wetting, solder balling, and graping were measured for each solder paste. This was done with freshly printed solder paste and again with circuit boards that sat open to the air for 24 hours. Figure 11 shows the wetting pattern on the PR test board.

Setting	RTS Profile
Ramp rate	1.7–1.8°C/sec
Reflow time (>220°C)	61–67 sec
Peak temperature	241–248 °C
Profile length (25°C to peak)	4.70 minutes

Table 5: Reflow profile parameters.

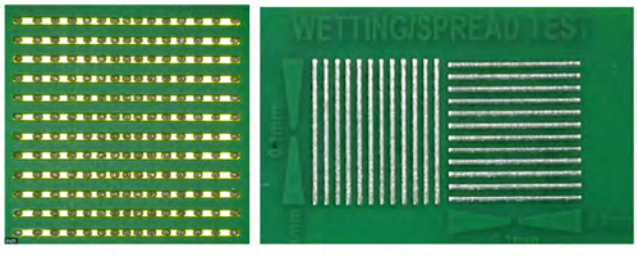

Figure 11: PR test board wetting pattern before (L) and after reflow (R).

This pattern includes 12 vertical and 12 horizontal parallel lines with 15 solder paste bricks printed down each line. The solder paste bricks

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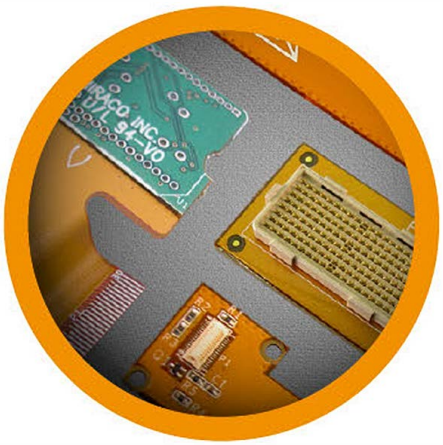
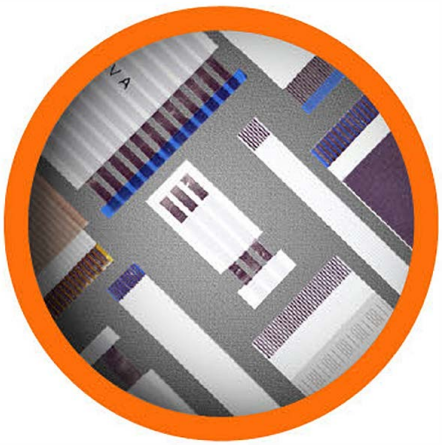


Flexible Printed Circuits



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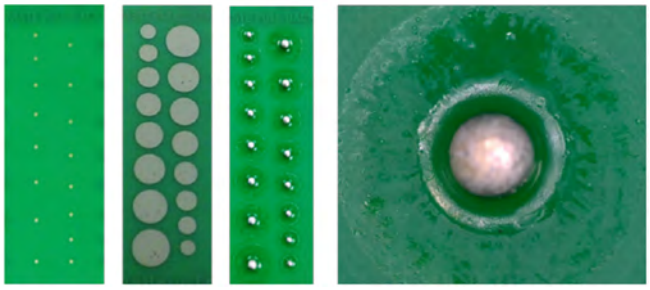


Figure 12: PR test board solder balling/pullback patterns.

are 0.4 mm wide (15.7 mils) and spacing ranges from 0.1–0.4 mm (3.9–15.7 mils). During reflow, the solder paste bricks spread together down each line. A wetting or spread percentage is calculated by counting the number of solder paste bricks that bridged together and dividing by the total possible number of bricks. Ideal solder paste performance is 100% wetting.

Solder balling is measured using solder balling/pullback patterns. The solder paste is overprinted onto the solder mask. When the solder paste reflows, it pulls back into a central sphere of solder. Random solder balls are left behind in the flux pools (Figure 12).

The overprint percentages range from 500–1,250% over the pad size. Solder balling is evaluated by the largest overprint percentage that has: zero solder balls, less than five solder balls, and less than 10 solder balls. Ideal solder paste performance is 1,250% overprint in each category.

Graping is measured using graping patterns. These patterns include square and circular, solder mask defined and non-solder mask defined pads. The pad sizes range from 0.18

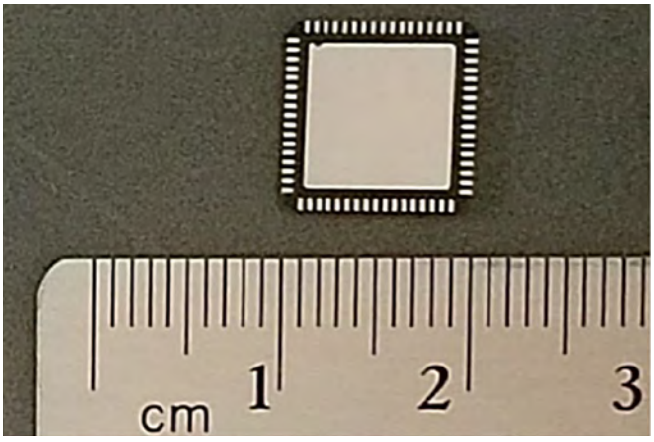


Figure 14: QFN (MLF68) dummy component.

mm (7 mils) to 0.30 mm (12 mils), and the corresponding stencil aperture area ratios range from 0.35–0.60 respectively (Figure 13).

After reflow, the solder deposits are evaluated for graping. Graping typically occurs at the smaller solder paste deposits (Figure 13). A graping percentage is calculated by dividing the total number of solder deposits with graping by the total possible. Ideal solder paste performance is 0% graping.

Voiding

The larger quad-flat no-lead (QFN) thermal pads were used for void measurements. The QFN components have 68 perimeter leads on a 0.5-mm pitch, 10-mm body size, and matte tin finish (Figure 14).

The stencil design was identical for each QFN location (Figure 15). In each case, the solder paste coverage was approximately 65% of the thermal pad area.

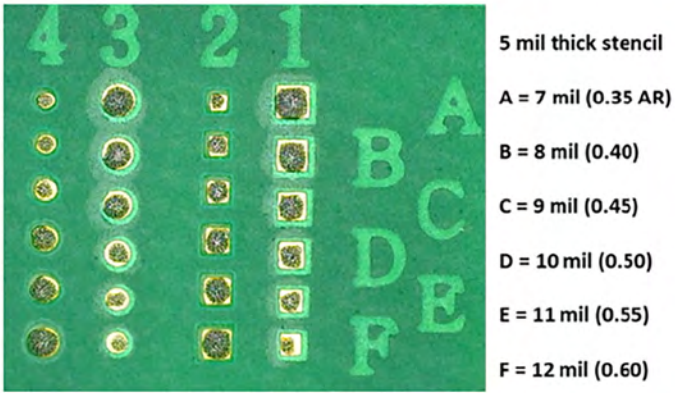
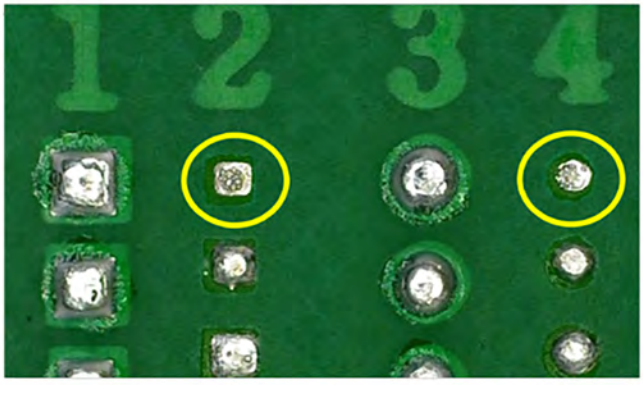


Figure 13: PR test board graping patterns.



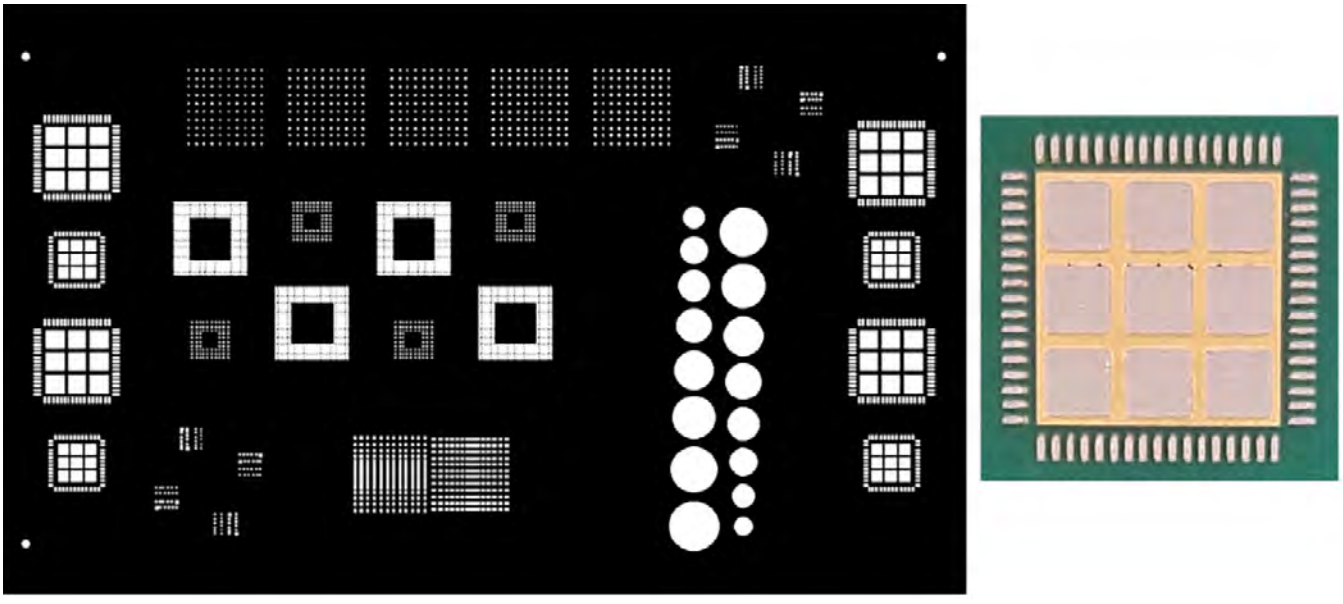


Figure 15: Stencil design for QFN thermal pads.

The QFN thermal pad stencil design was a window-pane type with nine panes. The web width of the QFN window panes was 0.51 mm (20 mils). Four QFN components were placed on each of five circuit boards for a total of 20 QFNs and 20 void area measurements per solder paste. Statistical analysis was used to compare voiding performance for each solder paste.

Standard Solder Paste Tests

Several industry standard solder paste tests were run to compare and contrast the performance of the solder pastes. Viscosity using both T-bar spindle and spiral pump, slump, and solder balling were all run per J-STD-005 [1]. The data from these industry standard tests was compared and contrasted for each solder paste, mainly to illustrate basic differences in the solder pastes.

Stability: Tack Force

Tack force testing was run per JIS Z 3284 [11] on freshly prepared coupons. Additional tack force coupons were printed and placed in a controlled environment at 21–24°C (70–75°F) and 50–55% relative humidity. The tack force coupons were stored, and tack force was measured after hold times of 24, 48, and 72 hours. Changes in tack force over time give some information about reactivity or stability of the solder paste. Ideal performance is no change in tack force over 72 hours.

Stability: Heat Aging

The solder pastes were placed in sealed jars in an oven at 50–55°C (122–131°F) for 72 hours. This temperature is much higher than recommended for solder paste storage. The normal recommended storage temperature for most solder pastes is 5–10°C (40–50°F). Elevated temperatures tend to speed potential reactions within the solder paste. This may result in a loss of activity, thickening of the solder paste, and overall degradation in performance.

After heat aging, the solder pastes were printed on the PR test board and reflowed. Viscosity, solder balling, and tack force measurements were taken. These results were compared to the results from the fresh solder pastes (before heat aging). Stable solder pastes tend to show very little change in performance while more reactive solder pastes tend to show drops performance.

Statistical Analysis

Tukey-Kramer honest significant difference (HSD) testing was done on the voiding data sets to compare and contrast the data. Tukey-Kramer HSD analysis determines whether multiple data sets are significantly different or

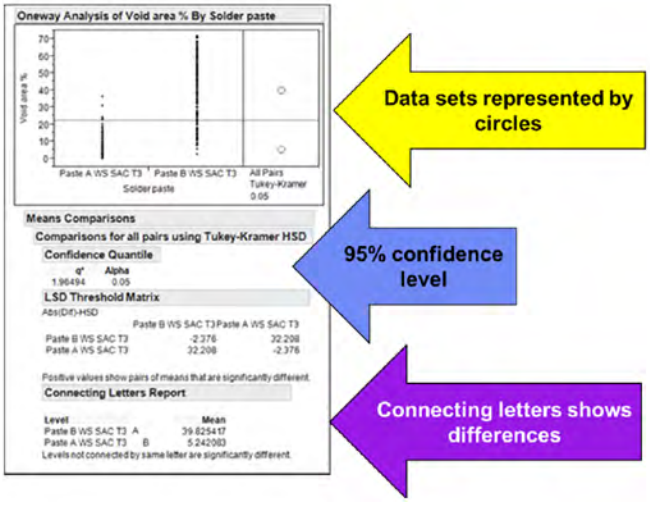


Figure 16: Explanation of Tukey-Kramer HSD report.

statistically similar. This test is similar to Student's t-test used to compare means. The output of the Tukey-Kramer HSD test is a chart that shows the data sets and several data calculations and reports (Figure 16).

The Tukey-Kramer HSD analysis shows whether the data sets under comparison are significantly different. This analysis is used to draw general conclusions and show trends in performance.

Results and Discussion

Standard Solder Paste Tests

The viscosity of each solder paste was measured using the T-bar spindle and spiral pump methods from J-STD-005 [1]. Figure 17 shows the results.

The viscosity of the no-clean solder paste increased with decreasing solder powder size for both the T-bar spindle and spiral pump methods. The viscosity of the water-soluble solder paste was more stable with respect to solder powder size regardless of the method used. The T-bar spindle method gave a higher viscosity for the no-clean SAC Type 5 and 6 solder pastes than for the water-soluble solder pastes while this was not true for the spiral pump method.

The slump of each solder paste was measured according to IPC-J-STD-005 methods. Table 6 shows the pass and fail results.

All solder pastes passed cold (25°C) slump, but there were some failures with hot slump (180°C). The no-clean Type 6 and the water-soluble Type 5 and 6 solder pastes failed hot slump. These solder pastes were formulated originally for use with Type 3 and 4 solder powders and are not necessarily optimized for the smaller solder powders.

The IPC J-STD-005 solder balling test was run using frosted glass slides and a hot plate set to 245–250°C. Table 7 shows the results.

	No-Clean		Water-Soluble	
	Cold Slump	Hot Slump	Cold Slump	Hot Slump
SAC T3	Pass	Pass	Pass	Pass
SAC T4	Pass	Pass	Pass	Pass
SAC T5	Pass	Pass	Pass	Fail
SAC T6	Pass	Fail	Pass	Fail

Table 6: IPC slump pass and fail results for each solder paste.

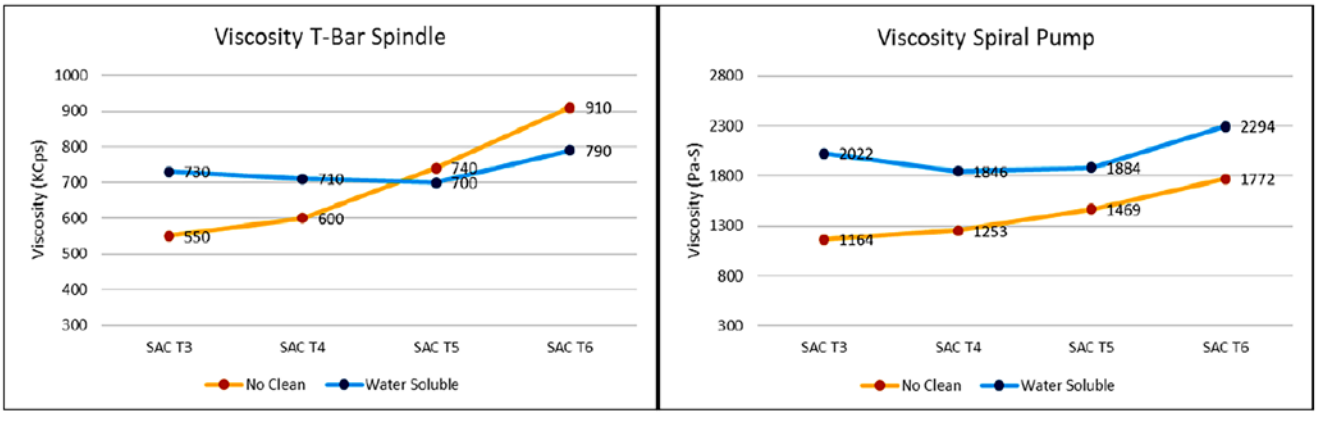


Figure 17: Viscosity of each solder paste using both T-bar spindle (L) and spiral pump methods (R).

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	No-Clean		Water-Soluble	
	Initial	After 4 Hrs.	Initial	After 4 Hrs.
T3	Acceptable	Acceptable	Acceptable	Acceptable
T4	Acceptable	Acceptable	Acceptable	Acceptable
T5	Acceptable	Ac - UnAc	Acceptable	Acceptable
T6	Unacceptable	Unacceptable	Unacceptable	Unacceptable

Table 7: IPC solder balling results for each solder paste.

All Type 3, 4, and 5 solder pastes gave acceptable solder balling results. The no-clean Type 5 solder paste gave borderline acceptable/unacceptable results. All Type 6 solder pastes gave unacceptable results showing rings of solder balls and clumps of solder balls (Figure 18).

Printing Area Ratio Limits

The printing patterns on the PR test circuit board are challenging for solder pastes. The aperture sizes in the print patterns range from 6 mils (0.152 mm) up to 10 mils (0.254 mm) and the stencil is 5 mils (127 µm). This corresponds to aspect ratios of 1.2 up to 2.0 and area ratios of 0.30 up to 0.50 respectively. The guidelines given in IPC-7525 [2] for acceptable solder paste printing are aspect ratios above 1.50 and area ratios above 0.66. The 0.30 and 0.35 area ratio apertures have aspect ratios of 1.2 and 1.4 respectively, which are below the recommended guideline of 1.50. All of the area ratios are below the industry guideline of 0.66.

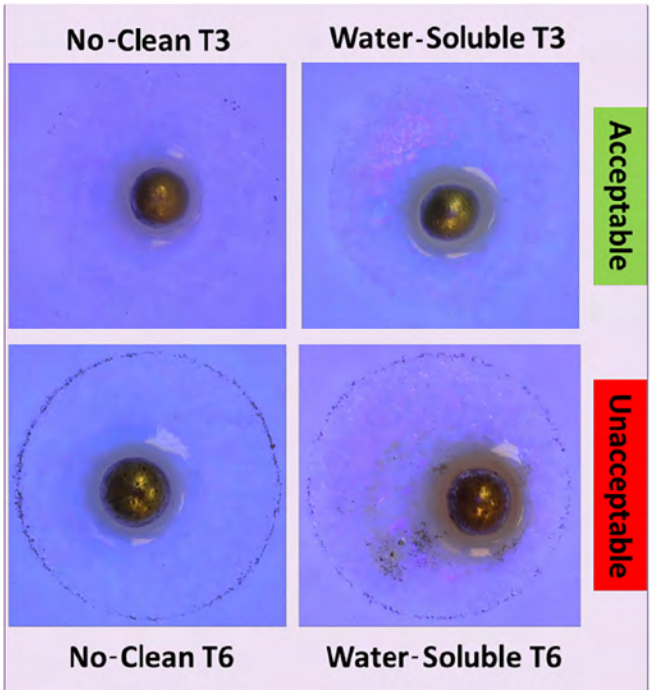

Figure 18: IPC J-STD-005 solder balling pictures of acceptable and unacceptable results.

The printed solder paste transfer efficiency (TE%) values for these patterns typically range from 5% up to 60%. Figure 19 shows the transfer efficiencies for the printed solder paste broken out by area ratio.

These transfer efficiency numbers are well below the generally accepted industry limit of 80%, which is normal for this stencil design.

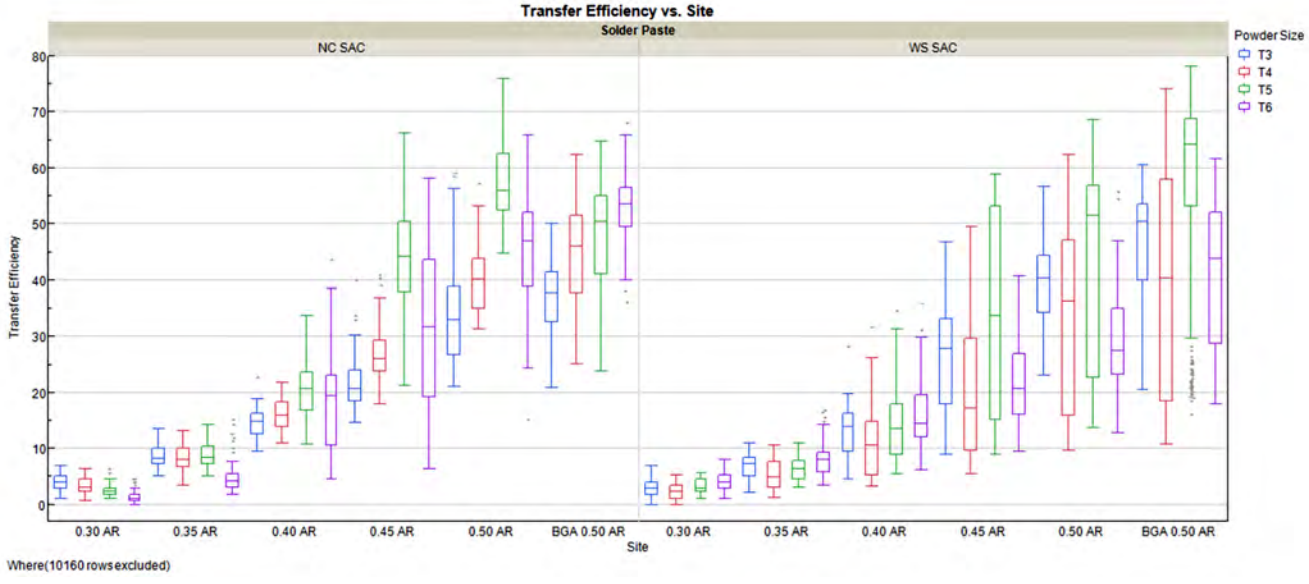

Figure 19: Transfer efficiency box plots for each solder paste by area ratio.

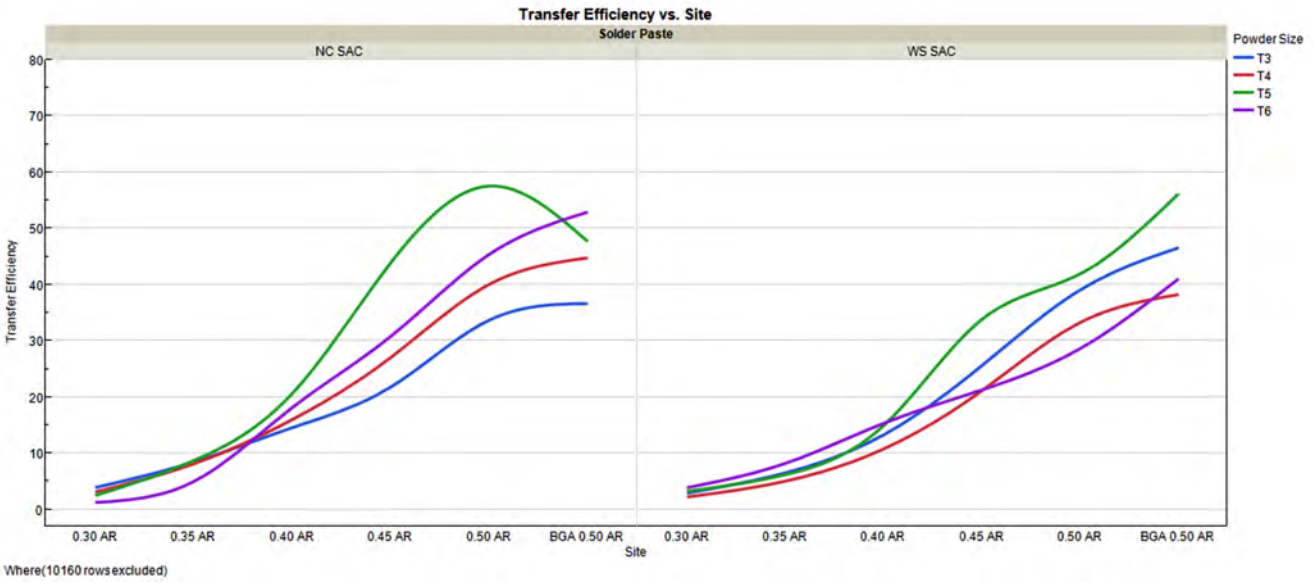

Figure 20: Transfer efficiency curves for each solder paste by area ratio.

Generally speaking, the transfer efficiencies increase with decreasing solder powder size. There are some anomalies in this data that do not follow that trend. The no-clean Type 6 solder paste gave lower transfer efficiencies for the 0.30 and 0.35 area ratios than the other solder powder sizes. This was an unexpected result. This same data set is shown as smooth curves in Figure 20.

The transfer efficiency of Type 5 solder pastes was generally higher than all of the other solder powder sizes. This was an unexpected result. Type 6 solder paste was expected to give higher transfer efficiencies than the other solder powder sizes. The water-soluble Type 6 solder paste gave some of the lowest TE% values.

If we use a rule of 0.60 area ratio for Type 3 solder pastes, then the minimum area ratios for the other solder paste types can be estimated based on the TE differences in this study. Table 8 lists these minimum area ratios by solder paste.

These minimum area ratio rules are guidelines based on the print patterns used in this evaluation. More work is needed to evaluate the print performance of Type 6 solder pastes. These rules do not take into account solder joint quality or reliability. Solder joint quality and reliability should be verified before using these rules in a production environment.

Solder Powder Size	Minimum Area Ratio No-Clean	Minimum Area Ratio Water-Soluble
Type 3	0.60	0.60
Type 4	0.55	0.60
Type 5	0.50	0.55
Type 6	More work needed	More work needed

Table 8: Minimum area ratios for each solder paste and solder powder size.

Print-and-Pause Results and Stencil Life

Print-and-pause testing is one way to determine the stability of solder pastes as they sit open to the air in the printer. Drops in transfer efficiency over time are a way to estimate stencil life. Figure 21 shows the transfer efficiency over time for each solder paste.

The no-clean solder pastes each showed similar performance in print-and-pause testing. The transfer efficiency was stable at time zero hours, one hour, two hours, four hours, and eight hours. At a time of 24 hours, there was a significant drop in transfer efficiency. The smaller solder powder sizes showed larger drops in transfer efficiency. The water-soluble solder pastes showed similar performance. There was a significant drop in TE% at a time of 24 hours. Table 9 summarizes the TE% drops from the eight-hour time to the 24-hour time.

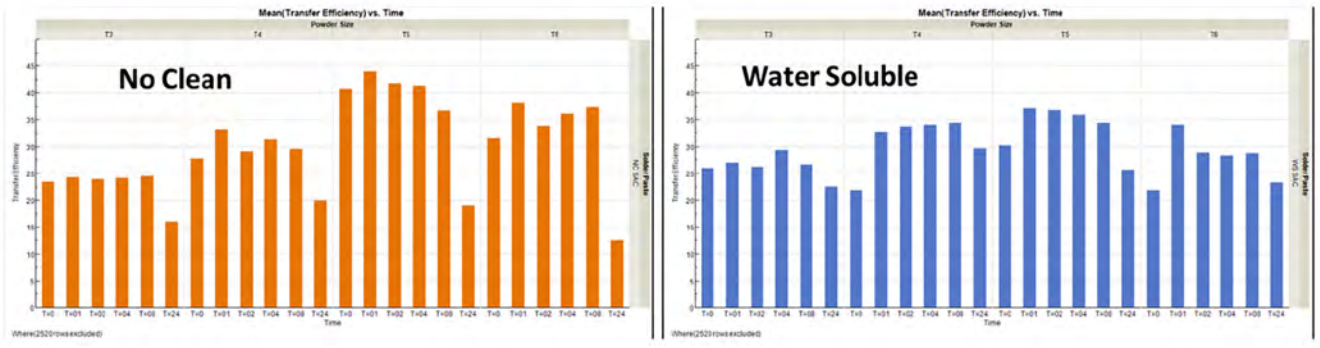

Figure 21: Print-and-pause results for each solder paste. No-clean (L) and water-soluble (R).

Solder Powder Size	Drop in TE% No-Clean	Drop in TE% Water-Soluble
Type 3	8	5
Type 4	10	5
Type 5	18	8
Type 6	25	6

Table 9: Transfer efficiency % drop from time = eight hours to 24 hours.

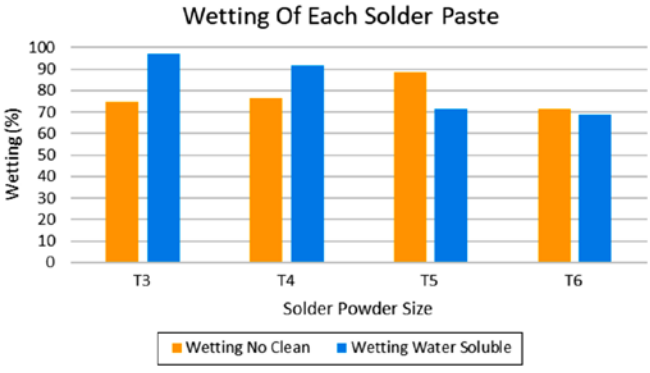

Figure 22: Wetting or spread of the solder pastes.

Type 3 and 4 solder powders give a similar drop in transfer efficiency over time for each solder paste. Type 5 and 6 solder powder sizes show a larger drop in transfer efficiency over time for each solder paste. The no-clean solder pastes are less stable with respect to decreasing solder powder size than the water-soluble solder pastes. The no-clean solder pastes tend to dry out more while sitting on the stencil, especially with the smaller solder powder sizes.

Reflow Performance of the Solder Pastes

Wetting or spread percentage of each solder paste was measured using the PR test circuit board with ENIG surface finish. Figure 22 shows the results for wetting.

The no-clean solder pastes showed fairly stable wetting of about 70–75% regardless of solder powder size. The only anomaly in this trend is the wetting percentage for no-clean Type 5 solder paste, which was near 90%. The water-soluble solder paste shows a trend in decreasing wetting as the solder powder size decreases. The wetting for the water-soluble Type 3 solder paste was 97% and this decreased to under 70% for Type 6 solder paste (Figure 23).

Solder balling was measured using the pull-back patterns on the PR test board. The largest overprint percentages that gave zero solder balls, less than five solder balls, and less than 10 solder balls were recorded for each solder paste. The maximum overprint percentage in each category is 1,250%. Table 10 shows the results for the solder pastes that were measurable with this criteria.

The solder balling was greater than 10 on all patterns for the solder pastes that are not

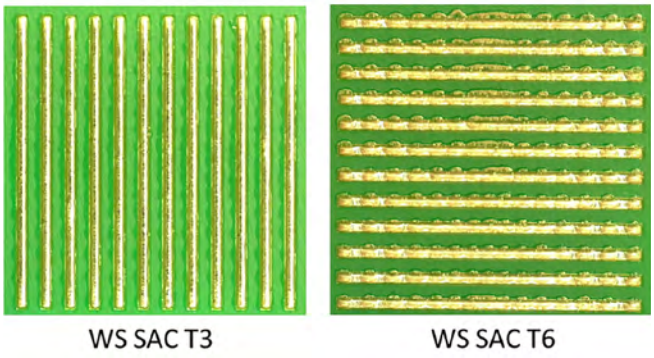

Figure 23: Wetting for WS SAC Type 3 and 6 solder pastes.

Solder Paste	Overprint With Zero Solder Balls	Overprint With <5 Solder Balls	Overprint With <10 Solder Balls
No-Clean Type 3	750%	1,200%	1,200%
Water-Soluble Type 3	None	1,200%	1,250%
Water-Soluble Type 4	None	500%	1,200%

Table 10: Solder balling performance of solder pastes that fell within the measurement criteria.

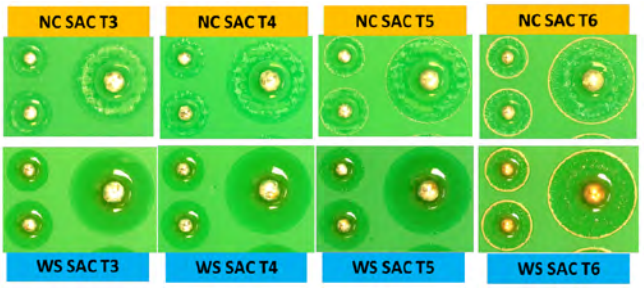

Figure 24: Solder balling in the overprint patterns.

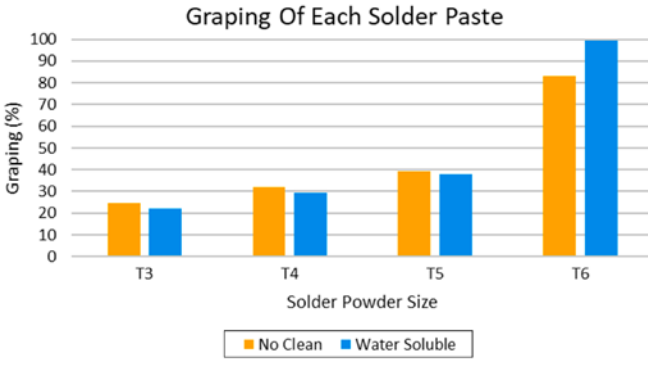

Figure 25: Graping for each solder paste.

shown in Table 10. Representative pictures of the solder balling in the overprint patterns are shown in Figure 24.

These overprint levels are fairly extreme and would not normally be used in typical surface-mount technology (SMT) designs. The solder balling generated by Type 3 and 4 solder pastes was low and would be considered acceptable on most electronic assemblies. It is evident from these images that Type 5 and 6 solder powders create excessive solder balling with the no-clean solder paste. The water-soluble Type 5 solder paste gave better solder balling than the no-clean Type 5. This is likely due to the relative activity levels of these solder pastes. The water-soluble solder paste has a higher activity level than the no-clean solder paste; therefore, the water-soluble solder paste gives less solder balling with the smaller solder powder sizes. Both the no-clean and water-soluble Type 6 solder pastes gave excessive solder balling.

The graping levels of the solder pastes vary with solder powder size (Figure 25).

The graping levels for the no-clean and water-soluble solder pastes were very similar for Type 3, 4, and 5 solder powders. Overall, the graping was very high for Type 6 solder pastes. The water-soluble solder paste gave higher graping than the no-clean solder paste with Type 6 powder.

Voiding was measured for each solder paste using the QFN thermal pads. Figure 26 shows the voiding data.

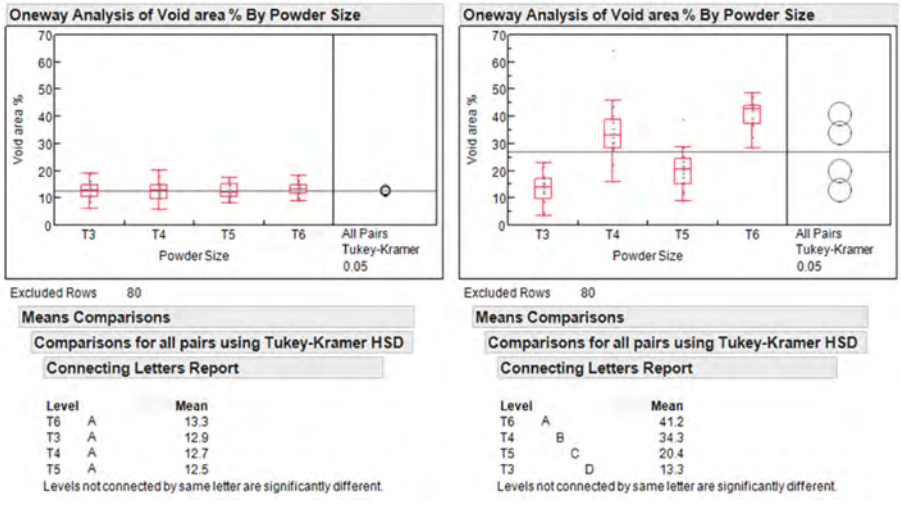

Figure 26: Voiding for each solder paste in the QFN thermal pads; no-clean (L) and water-soluble (R).

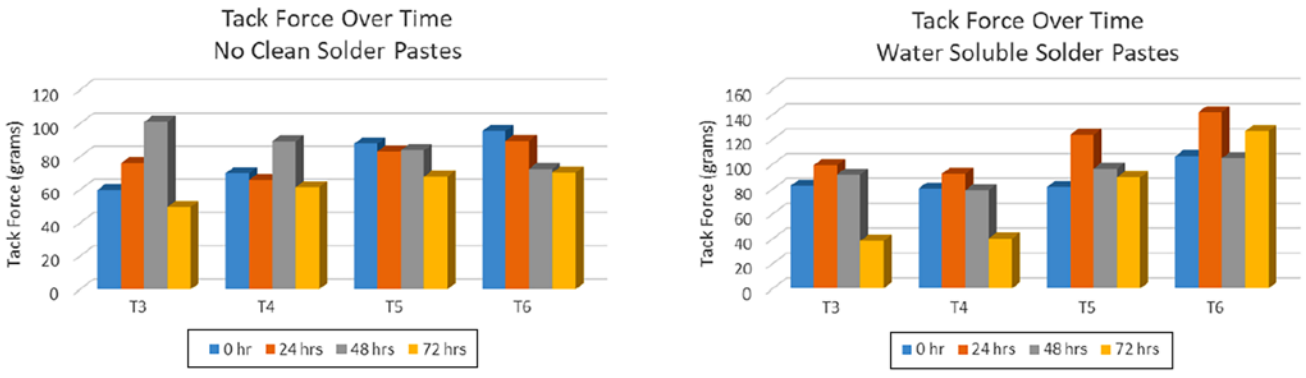

Figure 27: Tack force of no-clean (L) and water-soluble (R) solder pastes over time.

The no-clean solder paste showed statistically identical voiding behavior for each solder powder size. The water-soluble solder paste showed some differences in voiding by solder powder size. The largest solder powder (Type 3) gave the lowest voiding while the highest voiding was generated by the no-clean Type 6 solder paste. One possible explanation for this is the difference in rosin content of the no-clean and water-soluble solder pastes. The no-clean solder paste contains rosins, which help to protect the solder powder from oxidation during reflow. It is theorized that the byproducts of the reaction of the flux with the solder oxides can lead to voiding. With the added protection that rosins give, the amount of oxide generated during reflow is much lower for the no-clean than for the water-soluble solder paste. This may explain the voiding behavior observed in this work.

Stability of the Solder Pastes: Tack Force Over Time

The tack force was measured for each solder paste using the JIS method [11]. The tack force coupons were printed and stored in a chamber at room temperature and 50–55% relative humidity over a 72-hour period. Tack force was measured with the freshly printed solder paste after 24, 48, and 72 hours (Figure 27).

In general, the tack force decreases over time for each type of solder paste and each solder powder size. The tack force drops significantly at 72 hours for most of the solder pastes. This is not true for the water-soluble Type 5 and 6 solder pastes. The water-soluble Type 5 solder paste showed relatively stable tack force over the 72-hour time period. The water-soluble Type 6 solder paste showed an increase in tack force at the 72-hour time. This difference in the water-soluble paste performance is likely related to the increased flux content for the smaller solder powder types.

Stability of the Solder Pastes: Reflow Performance After a 24-hour Hold Time

The reflow performance of each solder paste was measured with freshly printed PR test boards and again with test boards that were printed and stored open to the air for 24 hours. Storing the printed solder paste open to the air can increase the solder oxide levels and deplete the activity of the solder paste. This test is one way to show the stability of the solder paste and to determine if that stability is lessened with smaller solder powders. Figure 28 shows the wetting results.

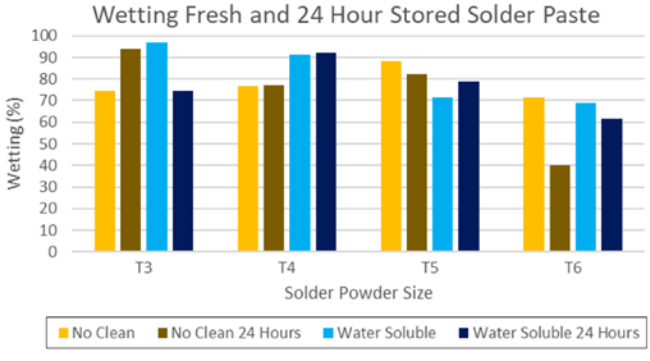

Figure 28: Wetting results of solder pastes before and after 24-hour storage.

Solder Paste	Overprint with <5 Solder Balls	Overprint with <10 Solder Balls	Overprint with <5 Solder Balls After 24 hours	Overprint with <10 Solder Balls After 24 Hours
No-Clean Type 3	1200%	1200%	600%	1000%
Water-Soluble Type 3	1200%	1250%	1150%	1250%
Water-Soluble Type 4	500%	1200%	None	500%

Table 11: Solder balling performance of solder pastes before and after 24-hour storage.

The wetting for the freshly printed no-clean solder pastes and the no-clean solder pastes stored for 24 hours were similar for every solder powder size except Type 6. The no-clean Type 6 solder paste showed a decrease in wetting when stored open to the air for 24 hours. The water-soluble pastes showed similar wetting when fresh and after 24 hours except for Type 3 solder paste, which showed a drop in wetting with storage.

Solder balling was measured using the overprint patterns in the PR test board with freshly printed solder paste and again with printed boards stored for 24 hours (Table 11).

The overprint percentages decreased as the printed solder pastes were stored over 24 hours. This indicates a general increase in random solder balling with storage. The increase in random solder balling was worse for the smaller solder powder sizes. Representative pictures of the solder balling before and after the 24-hour storage are shown in Figure 29.

The graping percentages were measured before and after 24-hour storage (Figure 30).

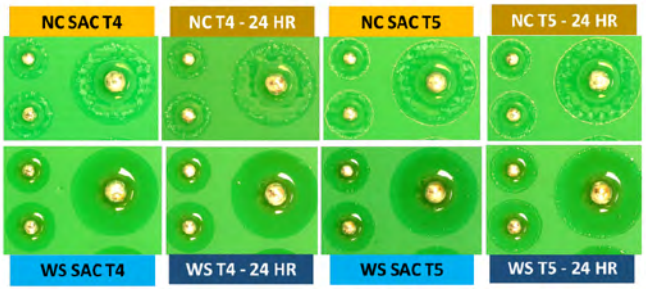

Figure 29: Solder balling of solder pastes before and after 24-hour storage.

The no-clean solder paste showed increases in graping for Type 3, 4, and 6 solder powder sizes when stored for 24 hours. The increases in graping were 6% for Type 3, 16% for Type 4, and 13% for Type 6. Type 5 solder pastes were unaffected by 24-hour storage. The water-soluble solder paste showed the same levels of graping before and after the 24-hour hold time. The graping with the no-clean solder paste shows increased sensitivity to hold times with the smaller solder powder sizes.

Stability of the Solder Pastes: Heat Aging

The solder pastes were sealed in their containers and heat aged in an oven at 50°C (122°F) for three days. After heat aging viscosity, IPC solder balling, tack force, and print and reflow performance were measured. These results were compared to the results from the fresh solder pastes. Figure 31 shows the viscosity results before and after heat aging.

The viscosity of the water-soluble solder pastes increased dramatically with heat aging.

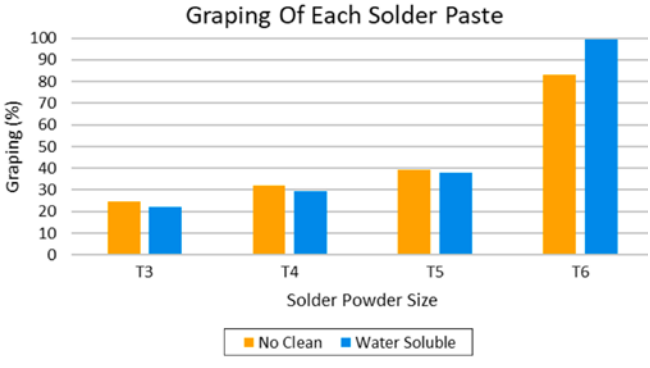

Figure 30: Graping results of solder pastes before and after 24-hour storage.

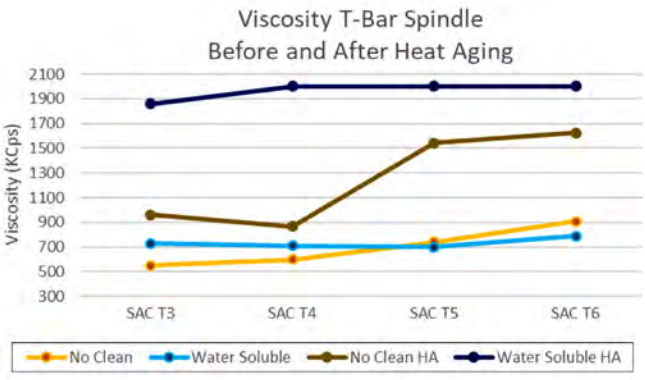

Figure 31: Viscosity T-bar spindle results before and after heat aging.

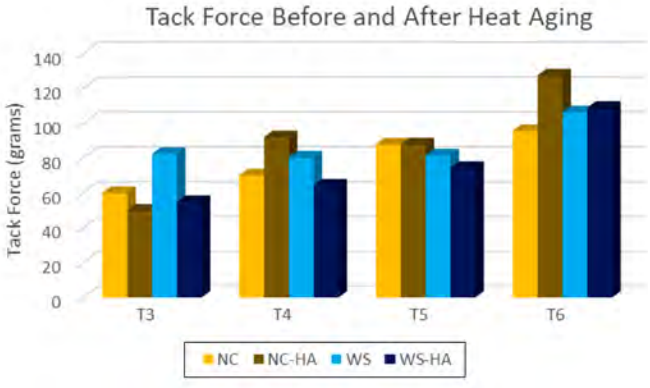

Figure 32: JIS tack force before and after heat aging.

The water-soluble solder pastes all reacted to the point of being unusable. The no-clean solder pastes showed some stability in this test. The no-clean Type 3 and 4 solder pastes increased in viscosity roughly 40–70% but were still usable. The no-clean Type 5 and 6 solder pastes increased in viscosity by more than 100%. These solder pastes were thick but printable with an increase in blade pressure.

The IPC solder balling test was run on the heat aged solder pastes and the results are shown in Table 12.

Initially, the fresh solder pastes gave acceptable solder balling for all solder powder sizes except Type 6, which was unacceptable. After heat aging, the solder on Type 5 and 6 no-clean solder pastes gave unacceptable results. Type 4, 5, and 6 water-soluble solder pastes gave unacceptable results. It is clear from this testing that the smaller solder powder sizes are more susceptible to reaction over time, which may lead to shorter usable shelf life.

The JIS tack force was measured on the heat aged solder pastes. Figure 32 shows the tack force data for the fresh and heat aged solder pastes.

The no-clean Type 3 solder paste decreased slightly in tack force after heat aging. Type 4 and 6 no-clean solder pastes increased in tack force with heat aging. The tack force of Type 5 solder pastes was stable with respect to heat aging. The water-soluble Type 3 and 4 solder pastes showed a decrease in tack force with heat aging. The water-soluble Type 5 and 6 solder pastes showed very little change in tack force with heat aging. This shows that tack force is not necessarily affected by heat aging and may not change through the shelf life.

Print performance was measured before and after heat aging. The water-soluble solder pastes were too viscous to print, so the data in Figure 33 is only for the no-clean solder pastes.

	No-Clean		Water-Soluble	
	Initial	After 4 Hrs.	Initial	After 4 Hrs.
T3	Acceptable	Acceptable	Acceptable	Acceptable
T4	Acceptable	Acceptable	Acceptable	Unacceptable
T5	Acceptable	Unacceptable	Acceptable	Unacceptable
T6	Unacceptable	Unacceptable	Unacceptable	Unacceptable

Table 12: IPC solder balling performance of solder pastes after heat aging.

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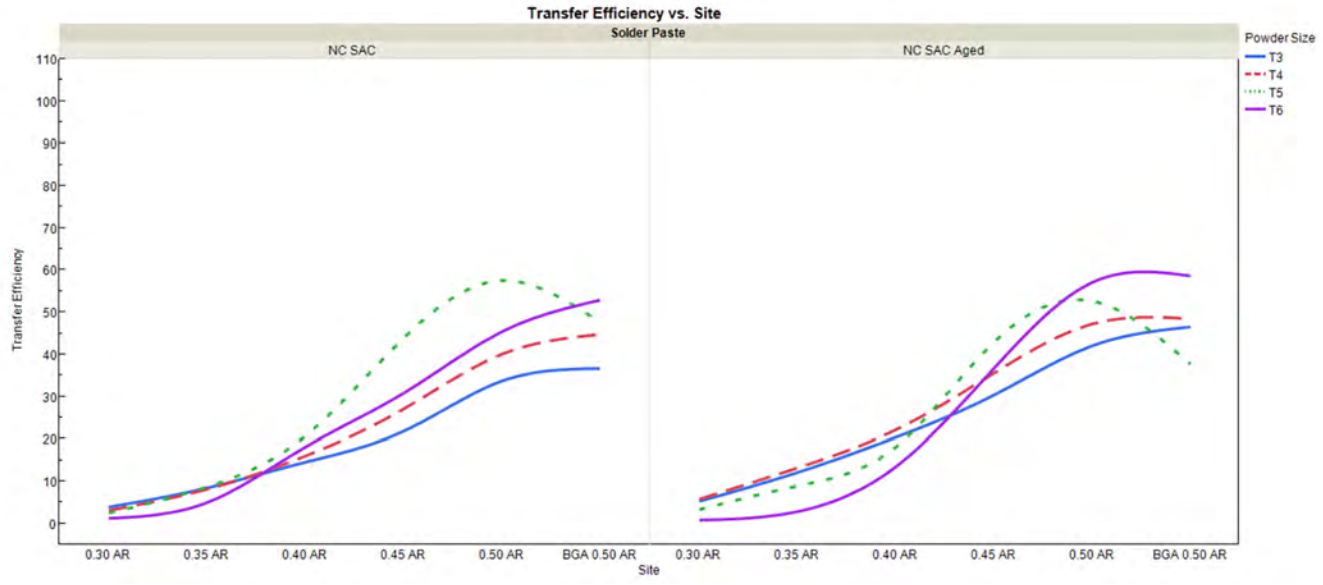

Figure 33: Print performance for the no-clean solder pastes before and after heat aging.

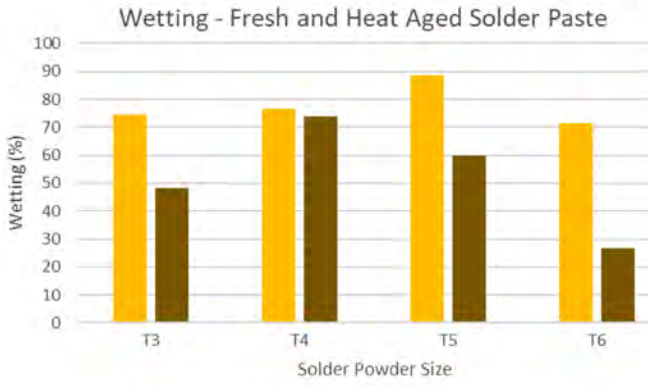

Figure 34: Wetting for the no-clean solder pastes before and after heat aging.

These transfer efficiency values are statistically the same before and after heat aging. Heat aging increased the viscosity of the no-clean solder pastes but did not affect the printability. By comparison, heat aging increased the viscosities of the water-soluble solder pastes to the point where they were not printable.

The reflow performance of the no-clean heat-aged solder pastes was measured using the PR test board and compared to the fresh no-clean solder pastes. Figure 34 shows the wetting data.

Wetting performance decreased with heat aging for each of the no-clean solder pastes. The largest decreases were with Type 5 and 6 solder pastes. Table 13 shows solder balling performance with respect to heat aging.

The no-clean solder pastes with Type 4, 5, and 6 solder powders were not measurable with these criteria and therefore are not shown in this table. The solder balling performance did not change significantly with heat aging of the no-clean solder pastes. Representative solder balling pictures are shown in Figure 35.

The graping percentages were measured after heat aging and compared to the fresh no-clean solder pastes (Figure 36).

The graping percentages were similar for the fresh and heat-aged Type 3, 4, and 5 no-clean

Solder Paste	Overprint With <5 Solder Balls	Overprint With <10 Solder Balls	Overprint With <5 Solder Balls After Heat Aging	Overprint With <10 Solder Balls After Heat Aging
No-Clean Type 3	1,200%	1,200%	1,100%	1,250%

Table 13: Solder balling performance of solder pastes before and after heat aging.

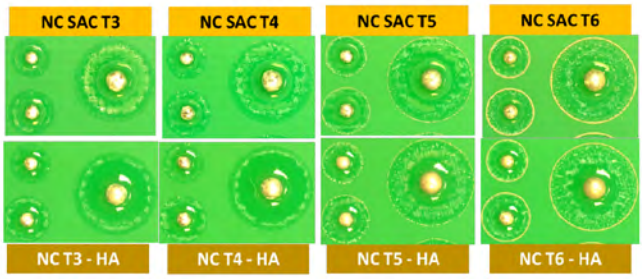

Figure 35: Solder balling of the no-clean solder pastes before and after heat aging.

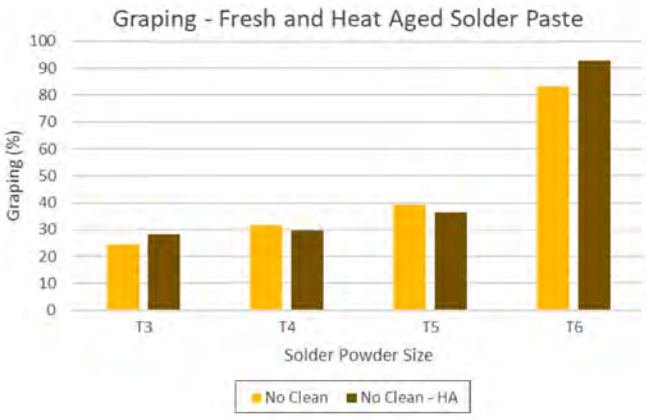

Figure 36: Graping of the no-clean solder pastes before and after heat aging.

solder pastes. Type 6 no-clean solder paste showed a slight increase in graping due to heat aging.

The decrease in wetting and graping performance with heat aging shows that the solder pastes with the smaller solder powder sizes lose activity more quickly than the larger solder powder sizes. The shelf life may be shortened for solder pastes made with smaller solder powder sizes.

Conclusions and Recommendations

Solder powder size certainly has an effect on solder paste performance. It is well understood that one cannot use every solder powder size with a particular solder paste. The solder paste must be formulated to work properly with the desired solder powder size. Here are recommendations for the optimal use of each solder paste and solder powder size based on performance in this work.

Slump (IPC)

All of the solder pastes performed well in the IPC slump test except for the no-clean Type 6 and the water-soluble Type 5 and 6 solder pastes, which failed the hot slump test. The flux concentration of these solder pastes was significantly higher with the smaller solder powder sizes, which changes the rheology of the solder pastes. This indicates that the smaller solder powder sizes may increase the potential for bridging during reflow.

Solder Balling (IPC)

Type 3, 4, and 5 water-soluble and no-clean solder pastes gave acceptable solder balling in the IPC test. Both the no-clean and water-soluble Type 6 solder pastes failed the IPC solder balling test. Type 6 solder powders have a relatively large oxide content compared to the other solder powder sizes. Type 6 solder pastes are more susceptible to solder balling than the other solder pastes.

Printing Minimum Area Ratio

In general, printed solder paste volume increased with decreasing solder powder size. The transfer efficiencies increased by roughly 5% for each decrease in solder powder size, which corresponded to a 0.05 change in area ratio. Here are the recommendations for minimum area ratio for each type of solder paste:

- Type 3 no-clean solder paste: 0.60 AR
- Type 4 no-clean solder paste: 0.55 AR
- Type 5 no-clean solder paste: 0.50 AR
- Type 3 and 4 water-soluble solder paste: 0.60 AR
- Type 5 water-soluble solder paste: 0.55 AR

Please keep in mind that the print parameters, stencil technology, and design will affect the printability and these minimum area ratios.

Pauses in Printing and Stencil Life

The no-clean Type 5 and 6 solder pastes showed the largest drop in transfer efficiency after a pause of 16 hours on the stencil. The water-soluble Type 5 and 6 solder

pastes showed a smaller drop in transfer efficiency after a pause of 16 hours on the stencil. It is not recommended to print solder paste after a 16-hour pause and 24 hours total time on the stencil. All of the solder pastes tested responded well to pauses in the printing of one, two, and four hours, and showed good printability through eight hours on the stencil. Based on this work, the recommended stencil life for all of the solder pastes tested would be eight hours. Environmental conditions, an additional rate of fresh solder paste, and other factors will affect this stencil life.

Reflow Performance (PR Test Board)

The wetting or spread of the no-clean solder pastes was consistent regardless of solder powder size. The wetting or spread of the water-soluble solder pastes decreased with decreasing solder powder size but was higher overall than the no-clean solder pastes. The solder balling performance for the no-clean and water-soluble Type 3, 4, and 5 solder pastes was acceptable for most electronic assemblies. The solder balling performance for the no-clean and water-soluble Type 6 solder pastes was excessive, as was seen in the IPC solder balling test. The graping performance for the no-clean and water-soluble Type 3, 4, and 5 solder pastes was very good. The graping was unacceptable for both of Type 6 solder pastes. Use of Type 6 solder powder in a solder paste may lead to excessive solder balling and graping.

Voiding Performance

All of the no-clean solder pastes showed identical low voiding behavior. The water-soluble solder pastes showed increasing voiding as the solder powder size decreased. Voiding is affected by solder powder particle size and a host of other factors. Voiding behavior may change with a change in solder powder size, and the process may require adjustments to minimize voiding.

Stability of the Solder Pastes

The tack force of all of the solder pastes was stable through 48 hours but dropped over 72 hours. The stability of the tack force is well beyond a normal amount of time between printing and reflow. The reflow performance after a 24-hour hold was stable for Type 3, 4, and 5 solder pastes. Type 6 solder pastes gave questionable reflow performance both before and after the 24-hour hold. A 24-hour hold prior to reflow is not recommended but shows that Type 3, 4, and 5 solder pastes were environmentally stable. More extreme environmental conditions will change the stability of the solder pastes.

Heat Aging of the Solder Pastes

The viscosity of the no-clean Type 3 and 4 solder pastes increased with heat aging, but they were easily printable. The viscosity of Type 5 and 6 no-clean solder pastes increased significantly but they were printable by adjusting the print parameters. The viscosity of all of the water-soluble solder pastes increased dramatically with heat aging and the pastes were not printable. The print performance of the no-clean solder pastes was essentially unchanged with heat aging. Heat aging caused failures in the IPC solder balling results for the no-clean Type 5 and 6 solder pastes, and the water-soluble Type 4, 5, and 6 solder pastes.

The tack force was stable before and after heat aging for all of the solder pastes. Only the no-clean solder pastes were printed and reflowed after heat aging. Heat aging caused the wetting performance to decrease for all of the no-clean solder pastes. Solder balling performance for the no-clean solder pastes worsened a little with heat aging. Graping performance was unchanged through heat aging of the no-clean solder pastes.

These results show that the reactivity of the solder pastes increases as the solder powder size decreases. This indicates that the shelf life is shorter for solder pastes made with the smaller solder powder sizes, especially Type 5 and 6 solder powders.

Summary

This work shows major differences in solder paste performance for no-clean and water-soluble solder pastes using SAC305 Type 3, 4, 5, and 6 solder powders. When solder pastes with

smaller solder powder sizes are used, the users should be aware of these performance differences so that the SMT process can be tuned accordingly.

Solder paste manufacturers are looking ahead to the future needs of the electronics industry. Smaller solder powder sizes are becoming increasingly common for miniaturized electronic applications. Solder paste manufacturers are formulating products for use with the smaller solder powder sizes to address these needs. **SMT007**

References

1. Solder Paste Task Group (5-24b), "Requirements for Soldering Pastes," J-STD-005A, February 2012.
2. Stencil Design Task Group (5-21e), "Stencil Design Guidelines," IPC-7525B, October 2011.
3. T. O'Neill, C. Tafoya, G. Ramirez, "The Impact of Reduced Solder Alloy Powder Size on Solder Paste Print Performance," *Proceedings of IPC APEX EXPO,* 2016.
4. R. Gray, "Development of a Robust 03015 Process," *Proceedings of IPC APEX EXPO,* 2015.
5. B. Roggeman, B. Keser, "Improved SMT and BLR of 0.35-mm Pitch Wafer Level Packages," *Proceedings of SMTA International,* 2015.
6. S. Harter, J. Franke, C. Lantzsch, "Evaluation of the Stencil Printing for Highly Miniaturized SMT Components with 03015 mm in Size," *Proceedings of SMTA International,* 2015.
7. Nobari, S. St-Laurent, "Solder Powder Characteristics and Their Effect on Fine Pitch Printing of Solder Paste," *Proceedings of SMTA International,* 2017.
8. E. Bastow, "Does Solder Particle Size Impact the Electrical Reliability of a No-Clean Solder Paste Flux Residue?" *Proceedings of IPC APEX EXPO,* 2016.
9. Nobari, S. St-Laurent, "Effect of Fine and Ultra-Fine Lead-Free Solder Powder Characteristics on The Reflow Property of Pastes," *Proceedings of SMTA International,* 2016.
10. Nobari, S. St-Laurent, "Investigation of Characteristics of Lead-Free Powders for Solder Paste Application," *Proceedings of IPC APEX EXPO,* 2017.
11. Japanese Standards Association, "Japanese Industrial Standard Solder Paste," JIS Z 3284, 1994.

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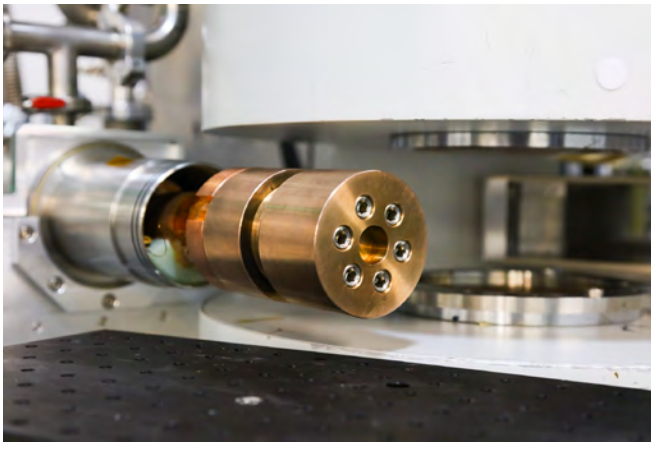
Mastering Magnetism

Researchers have pioneered a new technique using pressure to manipulate magnetism in thin-film materials used to enhance performance in electronic devices. They used neutron scattering at Oak Ridge National Laboratory's Spallation Neutron Source to explore the spatial density of atoms and observe how magnetism in a lanthanum-cobalt-oxide film changed with applied pressure.



"We developed a novel method to identify the critical role that strain has on the magnetism of films and their interfaces," said ORNL's Michael R. Fitzsimmons. "This allows us to study magnetism in thin films without having to compare a lot of differently grown samples."

The new technique, described in *Physical Review Letters,* will enable novel studies into complex correlations between magnetism and pressure involving a broad class of thin films in a wide range of applications. The thin-film materials were developed at ORNL, and complementary measurements were made at Argonne National Laboratory's Advanced Photon Source.

(Source: Oak Ridge National Laboratory)

The F Word

Quest for Reliability

Feature Column by Eric Camden, FORESITE INC.

This month's topic is failures and reliability, and I can't think of two words as diametrically opposed as these two. The word "failure" is as nasty as it gets in our world. It goes against everything we thought we knew. All contract manufacturing facilities strive to build a reliable product, or at least they all should. The problem is too many companies hope they are building reliable products without doing the work required to ensure they are. This is not uncommon, nor is it specific to the electronics industry, but as consumers, we sure know when a company didn't take the time to do reliability testing. Some companies simply don't care about reliability because even though their product isn't necessary for us to live, we simply can't live without it (I'm looking at you, Comcast).

In our industry, reliability is a must for almost all companies, so testing is normally written into drawings and contracts, but is that enough? Or is it just checking a few historical boxes without any thought? We often see legacy products that have been updated as older parts have become obsolete, or as a result of design changes, but the testing requirements haven't been updated since we found out who shot J.R.

Looking at today's electronics with package miniaturization and more complex circuitry, you may need to go beyond what you've always done. While we are on that topic, "That is how we've always done it," should be removed from your company's vocabulary. Historical testing does not necessarily mean it's still relevant or applicable to what you are building today. You need to assess the end-use environment and power demands to determine what testing should be carried out to ensure reliability. Obviously, safety-critical and life-dependent hardware must go through more rigorous testing than a PC, so there is no one-size-fits-all suite of testing. Many times, the only verification testing I see being done on bare boards is dimensional measurements. This is a good

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test and should continue. At a minimum, the next test should be an analysis of the stackup using cross-section. Many PC fabrication shops will send a cross-section puck sample with each lot. However, most of the time, I see them tucked away in a drawer in a bag stapled to a CofC, but they have not been examined by the customer. Believe it or not, a file cabinet does not take any measurements. One of the main issues with simply filing away a CofC and a puck is building product under the assumption that what the PC fabrication shop sent aligns with the print requirement. Only when a failure is detected does anyone go back and examine what was sent. Plenty of CMs do the work and examine the puck, but I can also say it certainly isn't all of them. You know who you are.

Many times, the only verification testing I see being done on bare boards is dimensional measurements.

Another very important test for bare boards is cleanliness testing of some sort with historical data or objective evidence to back up your acceptance criteria. This process is now clearly defined in the IPC J-STD-001 Amendment 1. This is especially important if your product is built with no-clean flux as there is not an end-of-assembly wash process to make up for sins upstream. If you start with a dirty bare board, you may experience issues related to electrical leakage or electrochemical migration that have nothing to do with your assembly process, so it's best to know up front if you're fighting an uphill battle.

There are many other tests you can perform on bare panels, which can be found in the IPC 4000 and 6000 series documents with IPC-A-600 as a visual reference guide. Depending on the end-use environment, there may be a much larger suite of test you need to perform. This needs to be discussed with the PCB supplier and customer.

Once you are satisfied that you are getting what you asked for regarding the bare boards, it's time to move on to your assembly. Material selections are often done using test coupons and some sort of elevated heat and humidity testing, which is a great idea. Surface insulation resistance (SIR) testing per IPC TM-650 2.3.6.7 has become a go-to test for determining how well your equipment can process the fluxes and what effect elevated heat and humidity will have, The idea is to either leave behind residues that are near benign or fully removed in the case of water-soluble flux types. There are also material compatibility tests for conformal coating, potting, adhesives, underfill, etc. It's important to know what effect different materials will have on the product. Not all materials play well together, so if you plan to coat or use some other type of surface encapsulation, these tests can be very useful and eliminate a potential issue before it manifests in a failure.

After all of the materials have been selected, it is time to move on to building your PCBAs and even more testing to see what your reliability risk is based on all of the choices and testing done up to this point. Of course, there's more testing; there's always more testing if you care about reliability. Again, you can look to IPC for a myriad of testing and need to consider the end-use environment when determining exactly what test you need, but I will cover a few of what we consider to be the most important tests are. The IPC documents you need to review are J-STD-001 and the companion IPC-A-610 for visual acceptance. These documents are a great reference tool if you have any questions about the assembly process. And no, I don't work for IPC, but I do spend time in task group meetings making a small contribution to help make the decisions that ultimately go into the assembly documents.

One of the first tests I recommend is ion chromatography to determine the level of cleanliness after assembly. IC will tell you the exact type and amount of ionic contamination, which is crucial when determining the risk for

failures related to electrical leakage or electrochemical migration. There are many ways to perform extractions for IC analysis, but one of the most important things to remember is that contamination is not evenly distributed across the entire surface of the assembly.

Historical testing using resistivity of solvent extract (ROSE) as well as standard IC extractions will show a result as if the contamination is indeed the same over each square inch. Each soldering process will introduce its own chemical signature into the final level of cleanliness, and only by looking at much smaller areas of the board will you know for sure what each process brings to the table. There are many ways to do localized extractions, and each has a unique set of benefits and drawbacks, so each method should be examined to determine which is right for your specific application. When you know just how much residue each process is adding, you can then directly address that part of the process to optimize and reduce the amount of active contamination. Excessive active residues will easily absorb atmospheric moisture and facilitate electrical leakage.

The next test I always recommend is thermal, humidity, and bias (or THB) testing. This process involves placing fully assembled product into an environmental chamber at elevated heat and humidity with a fixture that supplies nominal power to the samples and some expected output is measured over the course of 500 or 1,000 hours to get the best possible idea of what to expect in a normal field service environment. This is as close to the rubber meeting the road as you can get because this is 100% representative of your full process. All of the testing you've done to this point should give you an idea of what to expect from this type of testing. If you've made good decisions up to THB, you should see very good results.

These are the basic blocks of testing that I recommend at a minimum to cover, assess, and increase reliability. Of course, this doesn't cover every test you might need to consider. If your product is an under-hood application, you may need to add a vibration test. If it's going into a harsh environment, you may consider a mixed flow gas test. The list of applicable tests might grow, or you might be good with some of the basics I have mentioned here, but testing everything on the way to your final product is always a better strategy for reliability than having to react to the F word. **SMT007**

Eric Camden is a lead investigator at Foresite Inc. To read past columns or contact Camden, click here.

Goepel electronic Solutions, Webinar Series, and Trends

Goepel electronic offers test and inspection solutions for electronics production in automotive suppliers and automotive companies. The company specializes in automated optical inspection (AOI), automated X-ray inspection (AXI), and solder paste inspection (SPI) systems for electronics production as well as JTAG/boundary scan and end-of-line test systems.

In this interview, Barry Matties catches up with Matthias Müller to talk about Goepel electronic's overall business, the trends that he is seeing in the electronics manufacturing industry, and the informative webinar series produced by the company to help further educate their customer base and promote technical discussion on a number of topics.

To read the interview, click here.

Low-temperature SMT Solder Evaluation

Feature by Howard "Rusty" Osgood, David Geiger, Robert Pennings, Christian Biederman, Jie Jiang, and Jon Bernal
FLEX INC.

Abstract

The electronics industry could benefit greatly from using a reliable, manufacturable, reduced-temperature, SMT solder material (alloy composition), which is cost competitive with traditional Sn3Ag0.5Cu (SAC305) solder. The many possible advantages and some disadvantages or challenges are discussed.

Until recently, the use of Sn/Bi-based materials has been investigated with negative consequences for high strain rate (drop-shock) applications; thus, these alloys have been avoided. Recent advances in alloy "doping" have opened the door to revisit Sn/Bi alloys as a possible alternative to SAC-305 for many applications.

We tested the manufacturability and reliability of three low-temperature and one SAC-305 (used as a control) solder paste materials. Two of these materials are doped Sn/Bi/Ag, and one is just Sn/Bi/Ag1%.

We will discuss the tests and related results. Lastly, we will discuss the prospects, applications, and possible implications (based on this evaluation) of these materials together with future actions.

Introduction

A typical SAC305 reflow profile will have peak temperatures in the range of 235–245°C. Tin/bismuth or tin/bismuth/silver solder alloys may use a peak temperature in the range of 165–195°C. This represents a peak temperature delta of more than 50°C. Aside from the obvious energy cost savings, there are many other benefits to using a low-temperature solder (LTS) material, and they will be discussed later in this article. We also discuss some of the known and unknown risks as well.

Tin/bismuth and tin/bismuth/silver alloys are well-known to the industry and have been used routinely in consumer products that are not likely to be subjected to shock, drop, vibra-

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tion, or high temperatures, such as TVs and some appliances. These alloys are more brittle than SAC-305 and more creep resistant. This makes them well-suited for low strain rate stresses (temperature changes) but not well-suited for high strain rate stresses (shock, drop, vibration, bend, etc.).

Some solder material suppliers have been working for several years to develop a version of this (low-temperature) alloy, which is comparable to SAC-305 in terms of higher strain rate reliability.

Historically, they had come close, but only recently have they hit the mark using "secret" recipes that include trace amounts of "dopant" materials to make the alloy more ductile and crack resistant. Other papers [1 & 2] discuss the dopant effects on lattice and grain structures by adding trace amounts of elements, such as copper, nickel, manganese, and antimony. We will not go into that detail here, but the main point is that some suppliers seem to have found an appropriate recipe that maintains the bulk alloy (and hence low melting point) but alters its properties in a sufficiently beneficial way.

Another key factor in our consideration was that there had to be more than just one supplier of these types of materials before we performed any serious evaluations. We tended to avoid embracing proprietary processes or materials, which are only available from a single source.

Advantages

Some of the possible advantages of LTS include:

- Reduced board and component warp
- Reduced head-in-pillow
- Lower residual stress
- Reduced pad cratering
- Reduced CTE geometrical effects (scale factor)
  - Allows for smaller land pads/footprints
- Less expensive materials
  - PCBs
  - Components
- Less thermal exposure
  - Thermally sensitive components
  - Semiconductors
- Lower energy and maintenance costs
  - Estimated 20–25% lower energy cost depending on the profile
  - Lower maintenance cost on oven moving parts
- Possible hybrid assembly
  - SAC-305 on one side and low temp on the other
- Reduced voiding
  - ~50% void reductions observed

Disadvantages

As with any new material, there are unknown risks that may not come to light until the material is in use for some time. Some of the known risks include:

- Package warp—hot tearing
  - Large BGA packages that were previously designed to flatten out at over 210°C can cause "hot tearing" in the solder joint because the package never completely flattens and remains warped throughout the reflow cycle. One remedy for this is to use more solder paste to make up for the gap difference. The lower-temperature alloys did not tend to wet as aggressively (discussed in more detail later) and therefore can allow more solder per unit area without bridging. If the industry moves towards accepting these alloys on a large scale, it is likely the packaging vendors will adjust accordingly and may offer "LTS" versions of these packages
- Rework
  - Solder wire: Very limited (only one known source and it is not commercially available yet) and it is brittle
  - Cracked solder pots: Bismuth expands when it cools, so it can cause some solder pots (wave solder) to crack
- Wide liquidus/solidus range
  - We observed that a very rapid cooling was necessary to guarantee that the assembly was below 138°C exiting the conveyor reflow oven
- Flux residue

– We observed a considerable amount of flux residue after reflow. In time, these solder pastes may evolve to improve this

- More slump and less wetting
  – Our tests indicate a bit more slump (hot and cold) than our controlled material, but again, this is more likely to do with the maturity of the paste. However, the alloy itself does not wet as aggressively as SAC-305, which can be an issue in certain circumstances, although we still found it to be acceptable. In some cases, less wetting can be an advantage as well, such as for paste in hole

Experimental and Results

Materials Tested

Figure 1 shows the materials tested.

Material	Basic Composition - Descriptions
A - Control	SAC305 (96.5% tin, 3% silver, and 0.5% copper)
B	Sn + 47% to 51% Bi +2% other "dopants" including Ag
C	57Bi 42Sn 1Ag - No dopants
D	48% Bi, 50% Sn, 2% Ag with some dopants

Figure 1: Materials tested.

Material A is the control material. Materials B and D are the "doped" alloys, and Material C has no dopants added.

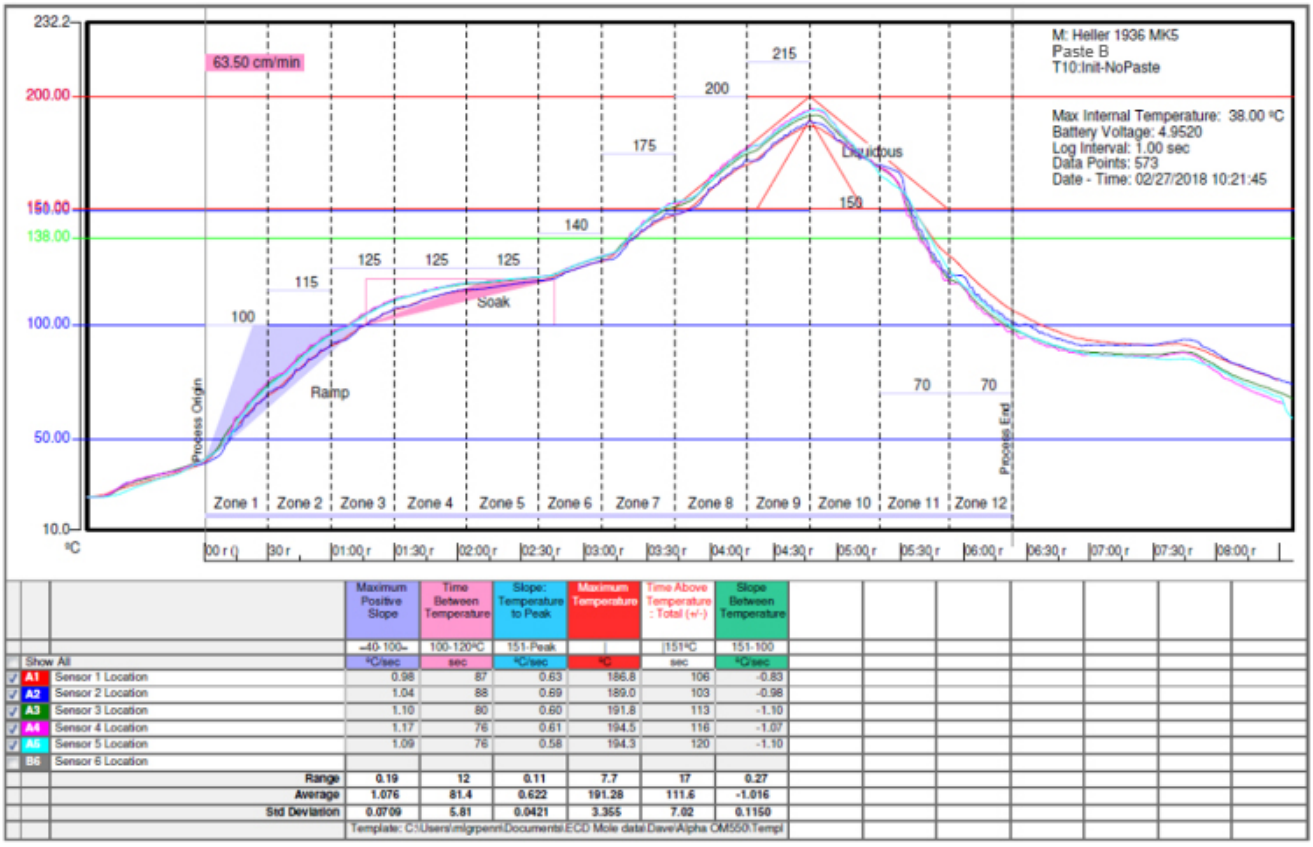
Assembly Conditions

All test boards were baked, inspected, and labeled before solder screen print. Solder paste inspection (SPI) was performed as well as SMT assembly and reflow.

Reflow Profile for LTS

Although peak temperatures as low as 165°C can be used (and should be used when appropriate), a higher temperature of 190°C was used to drive mixing on the SAC-305 BGAs (Figure 2). The solder paste and BGA ball interface experiences a sufficient phase change at these temperatures to drive diffusion and hence mixing of the BGA ball with the solder paste.

Mixing of the BGA with the SnBi paste shown in Figure 3 was approximately 50%. This is comparable to Time 0 as well as a characteristic of all the solder joints we observed, which fell into the 40–60% mixing range.



		Maximum Positive Slope	Time Between Temperature	Slope: Temperature to Peak	Maximum Temperature	Time Above Temperature : Total (+/-)	Slope Between Temperature
		-40-100-	100-120°C	151-Peak		151°C	151-100
Show All		°C/sec	sec	°C/sec	°C	sec	°C/sec
A1	Sensor 1 Location	0.98	87	0.63	186.8	106	-0.83
A2	Sensor 2 Location	1.04	88	0.69	189.0	103	-0.98
A3	Sensor 3 Location	1.10	80	0.60	191.8	113	-1.10
A4	Sensor 4 Location	1.17	76	0.61	194.5	116	-1.07
A5	Sensor 5 Location	1.09	76	0.58	194.3	120	-1.10
B6	Sensor 6 Location						
	Range	0.19	12	0.11	7.7	17	0.27
	Average	1.076	81.4	0.622	191.28	111.6	-1.016
	Std Deviation	0.0709	5.81	0.0421	3.355	7.02	0.1150
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Figure 2: Reflow profile for the LTS.

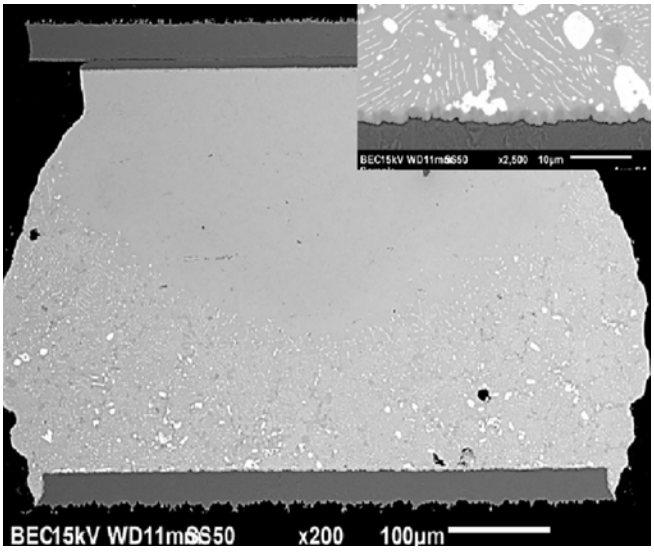

Figure 3: Cross-section of a BGA ball after 1,800 temperature cycles.

Testing Methodology

Two types of testing were performed: manufacturability and reliability.

Manufacturability:

- Solder paste volume
- Missing print
- Hot slump, cold slump
- Solder ball and two wetting tests
- X-ray and visual inspection

Reliability:

- Accelerated temp cycle (0–100°C)—JEDEC 9701
- Four-point monotonic bend test—JEDEC 9702

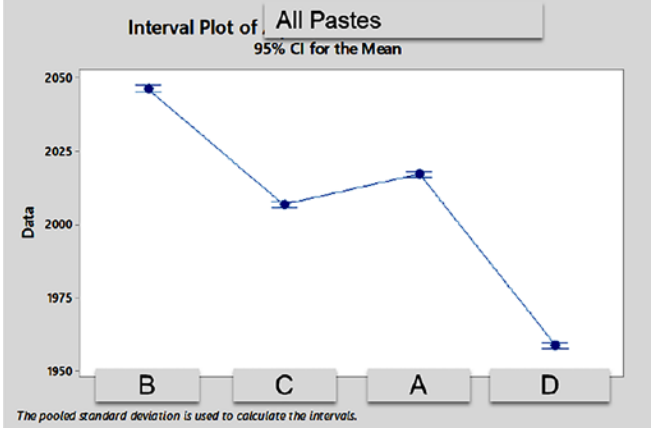

Figure 4: Solder volume box plots for the 22-mil (0.56-mm) aperture with an area ratio of 1.1. Material A is the control.

Manufacturability: Solder Paste Volume

We measured and analyzed the solder paste volume across six different aperture ratios ranging from 0.4–1.1. The apertures ranged from 8–22 mils (0.20–0.56 mm) using a 5-mil (0.13-mm) stencil.

From Figure 4, Material D has somewhat less (although sufficient) volume consistently. All materials passed our internal company specifications.

From Figure 5, Material D has somewhat less (although sufficient) volume consistently. All materials passed our internal specifications.

From Figure 6, Material D has somewhat less (although sufficient) volume consistently. All materials passed our internal specifications.

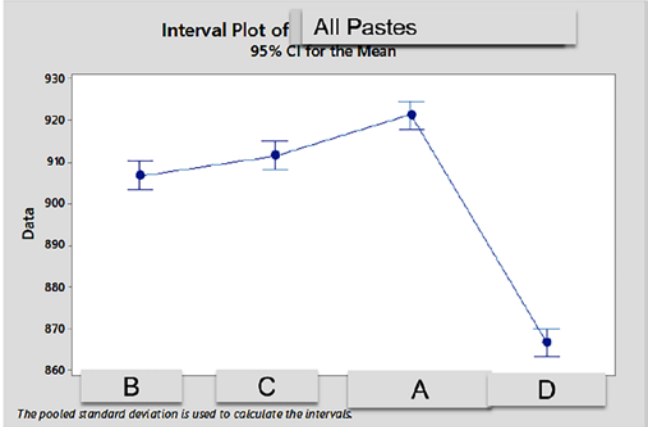

Figure 5: Solder volume box plots for the 16-mil (0.40-mm) aperture with an area ratio of 0.8. Material A is the control.

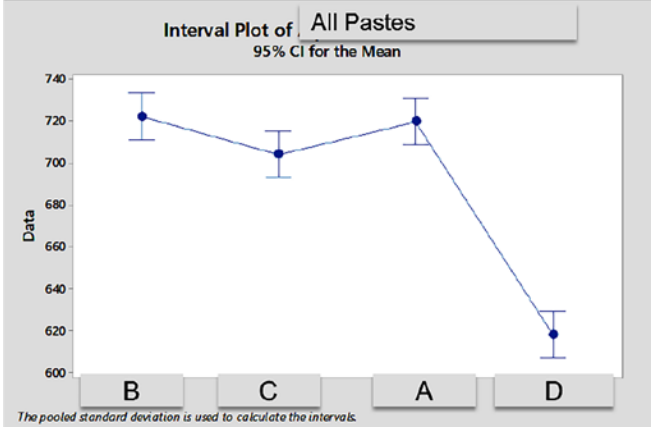

Figure 6: Solder volume box plots for the 14-mil (0.36-mm) aperture with an area ratio of 0.7. Material A is the control.

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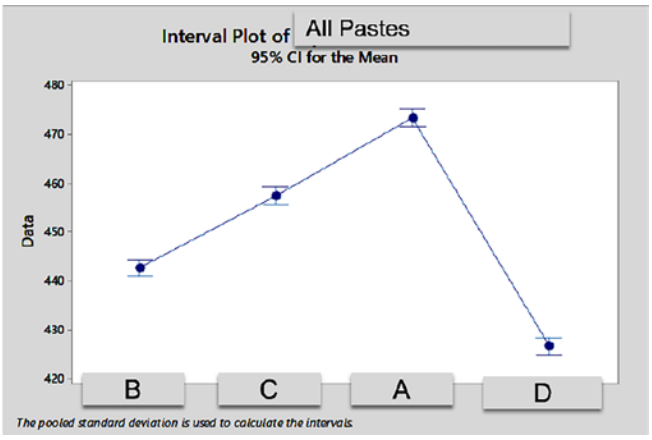

Figure 7: Solder volume box plots for the 12-mil (0.30-mm) aperture with an area ratio of 1.1. Material A is the control.

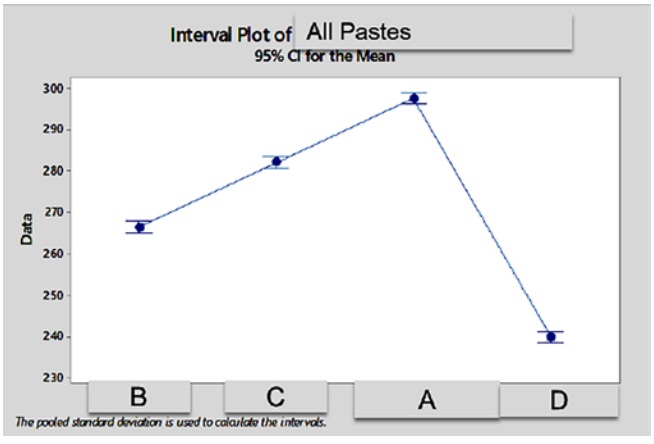

Figure 8: Solder volume box plots for the 10-mil (0.25-mm) aperture with an area ratio of 0.5. Material A is the control.

From Figure 7, Material D has somewhat less (although sufficient) volume consistently. All materials passed our internal specifications.

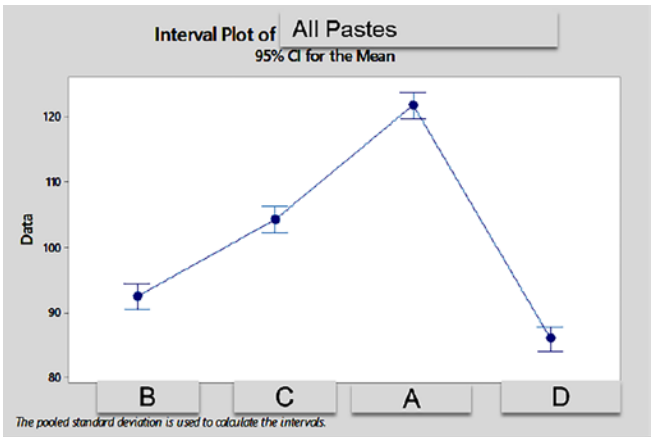

Figure 9: Solder volume box plots for the 8-mil (0.20-mm) aperture with an area ratio of 0.4. Material A is the control.

From Figure 8, Material D has somewhat less (although sufficient) volume consistently. All materials passed our internal specifications.

From Figure 9, Material D has somewhat less (although sufficient) volume consistently. All materials passed our internal specifications.

Manufacturability Testing: Missing Print

In this test, circular apertures 6–16-mils (0.15–0.40-mm) diameter are printed in three locations on the test board and inspected for missing print locations (Figure 10). The number of missing prints for each aperture are counted. We do not expect the 6-mil (0.15-mm) apertures to print at all. There were no missing prints on any of the apertures from 8 mils (0.20 mm) to 16 mils (0.40 mm), so all materials pass (Figure 11).

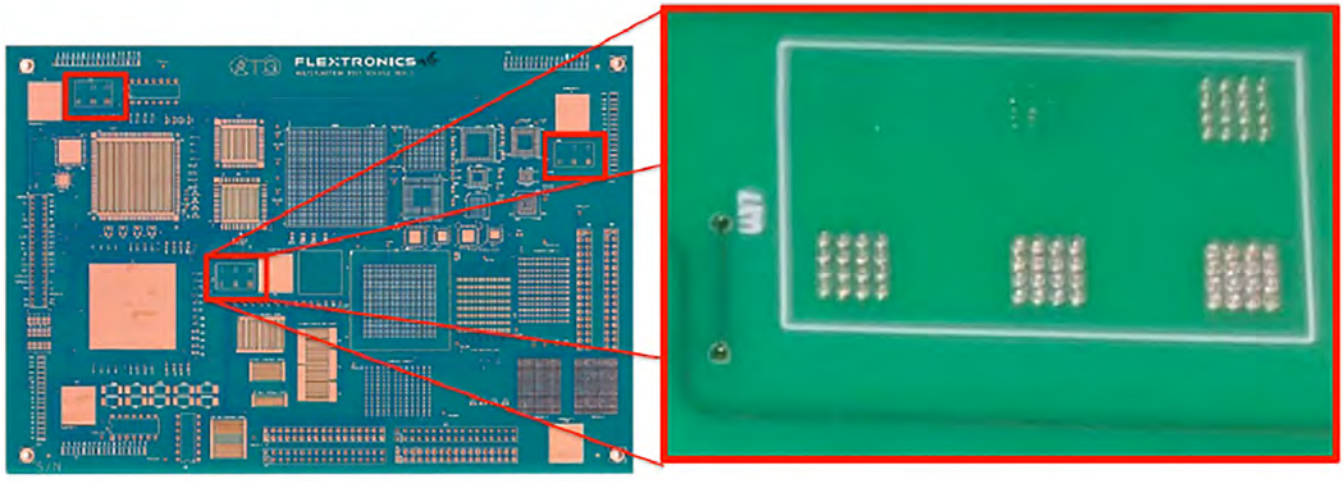

Figure 10: Missing print test pattern.

	C			B			A			D		
Ratio	U302	U301	U37	U302	U301	U37	U302	U301	U37	U302	U301	U37
6 Mils	4	0	7	1	41	14	21	0	0	9	0	0
8 Mils	0	0	0	0	0	0	0	0	0	0	0	0
10 Mils	0	0	0	0	0	0	0	0	0	0	0	0
12 Mils	0	0	0	0	0	0	0	0	0	0	0	0
14 Mils	0	0	0	0	0	0	0	0	0	0	0	0
16 Mils	0	0	0	0	0	0	0	0	0	0	0	0
Location Totals	4	0	7	1	41	14	21	0	0	9	0	0
Grand Total	11			56			21			9		
Rank	2			4			3			1		

Figure 11: Missing print test data and rank. All materials passed.

- Wetting Test 1
  - Print solder paste and measure solder spread after reflow.

Figure 12: Wetting Test 1 sample.

Material	C	B	D	A
Min	6.35	6.52	5.88	6.51
Max	6.53	6.58	6.59	6.58
Std Dev	0.03	0.02	0.27	0.02
Average	6.48	6.54	6.26	6.55
Rank	3	2	4	1

Figure 13: Wetting Test 1 results.

Manufacturability: Wetting Test 1

In this test, we printed a circle of paste on an oversized copper pad and measured the diameter after reflow (Figures 12 and 13). There is no specific pass-fail criteria for this test in terms of diameter. It is used, as with Wetting Test 2, to gauge the wetting properties of the material. The lower-temperature solders do not wet as well as the control material. This can be an advantage in paste-in-hole (PIH) applications.

Manufacturability: Wetting Test 2

In this test, we deposited the paste on rectangular pads at 5% intervals from 90–120% of the pad length. We then looked for the smallest percentage to completely cover the pad (Figures 14 and 15).

As expected in Figure 15, the low-temperature materials do not wet as well as the Sn3Ag0.5Cu control paste material.

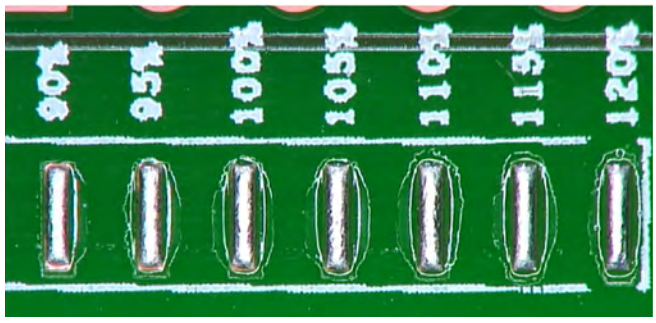

Figure 14: Wetting Test 2 sample. In this sample case, the result is 105%.

Ranking				
Wetting Test - 2A				
Wetting %	C	B	D	A
Count of 105%	1	9	11	15
Count of 110%	9	15	16	14
Count of 115%	13	5	3	0
Count of 120%	7	0	0	0
Ranking	**4**	**3**	**2**	**1**

Figure 15: Results of Wetting Test 2.

Manufacturability: Cold Slump

In this test, we printed multiple lines spaced from 0.075 mm (3 mils) to 0.300 mm (12 mils) and counted the bridged lines at each spacing (Figures 16 and 17). The paste all performed similarly, but the low-temperature materials did slump a little more. The overall ranking is as follows:

- Rank 1: Material D (120 avg. bridges 3 boards)
- Rank 2: Material A (125 avg. bridges 3 boards)
- Rank 3: Material B (185 avg. bridges 3 boards)
- Rank 4: Material C (196 avg. bridges 3 boards)

Manufacturability: BGA Voids

We observed approximately between 1% and 10% voiding on the BGA balls across all solder pastes tested with no significant performance difference between materials. Since we are not fully melting the BGA ball, we are not

Figure 16: Cold slump test sample.

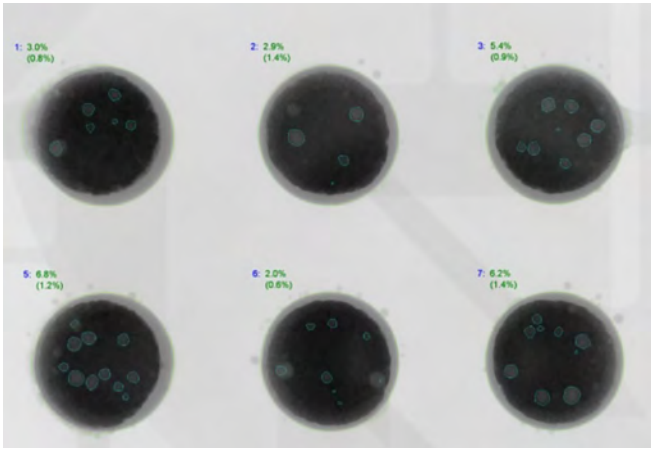

Figure 18: A typical X-ray inspection result of the 35x35 BGA with SAC305 balls.

significantly altering the "as-received" condition (Figure 18).

Manufacturability: QFN Voids

One surprising result was how well the lower-temperature paste materials performed under the QFN/BTC component. While voiding in our control SAC305 paste materials averaged 9.9%, the lower-temperature materials averaged between 1.8% for Paste C, 5.9% for Paste B, and 8.4% for Paste D. These results are shown in Figures 19–22.

Reliability: Four-point Monotonic Bend Test

We followed JEDEC 9702 recommended procedures to perform four-point monotonic bend testing on four boards of each paste type. We mounted a single 35x35 daisy-chained BGA to each four-layer test board with a thickness of 62 mils (1.6 mm). The strain rates were driven

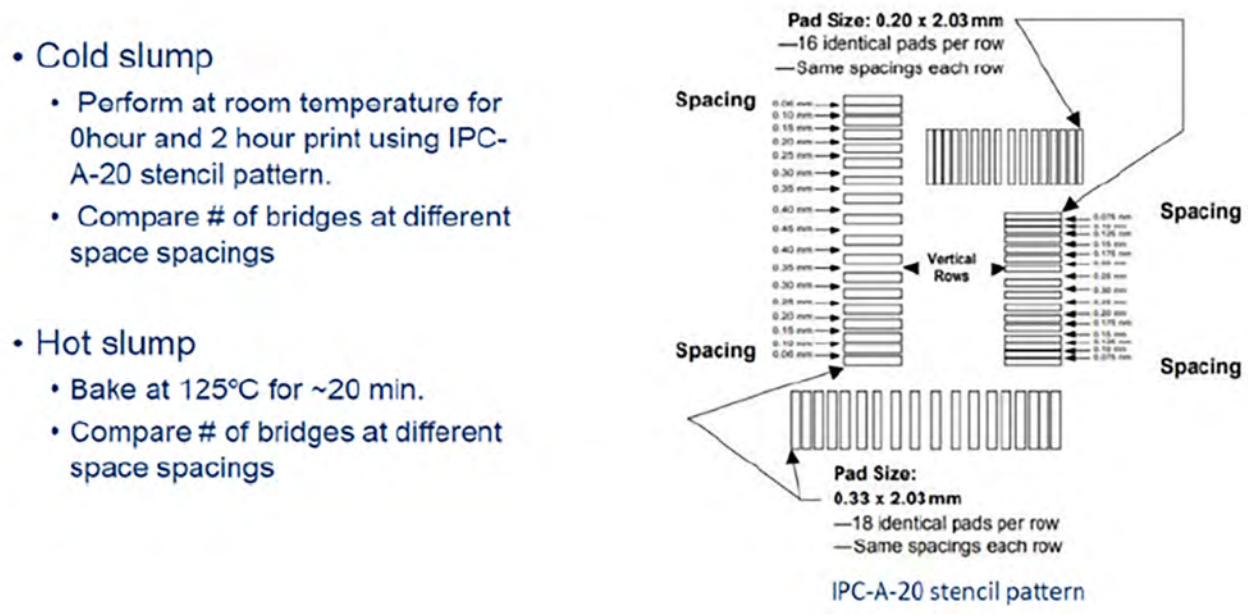

Figure 17: Description of both the hot and cold slump test.

Figure 19: Typical QFN voiding for Sn3Ag0.5Cu Paste A.

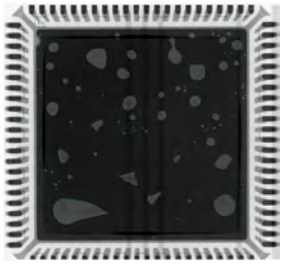

Figure 20: Typical QFN voiding for Paste D.

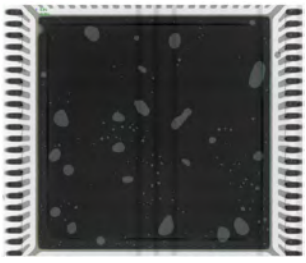

Figure 21: Typical QFN voiding for Paste B.

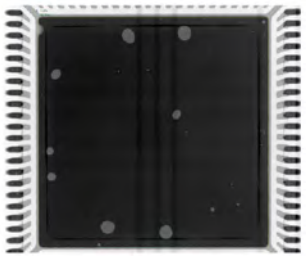

Figure 22: Typical QFN voiding for Paste C.

at a constant target head speed of 4 mm/second, which resulted in a strain response of between 5k με/sec (microstrains per second) and 8k με/sec.

One material (Material D) had a couple of anomalous readings where the daisy chain went open ahead of the bulk material failure. This is likely a weakened or compromised solder joint on the periphery of the package. This small sample set was to get an early first-level approximation.

Subsequent testing is currently underway. We will be testing eight boards at three times the strain rate (15K με/sec). In addition, we will be doing drop testing on all materials as well. The differences between the pastes were less than the differences within the pastes but we were still able to rank the performance. The doped Material B slightly outperformed the Sn3Ag05Cu control, and the other materials were comparable or slightly lower than the control. Material D had the widest range.

In the stress and continuity response curves (Figures 23–26), the solid lines are the strain measurement (inverse because the sensors were placed on the bottom) and the dotted lines (colors commensurate with each board) are the daisy chains. The dotted lines (daisy chains) rapidly go open when the circuit fails. Signal sampling is at four times the specified rate of 500 per second (measured at 2K per second).

From Figure 23, two of the four boards tested failed before the bulk material. This material had the highest as well as the lowest response range (9311με and 7313με respectively). Further evaluation would be needed to understand the early failures.

From Figure 24, one board (black line) had a slightly early failure (before the bulk failure).

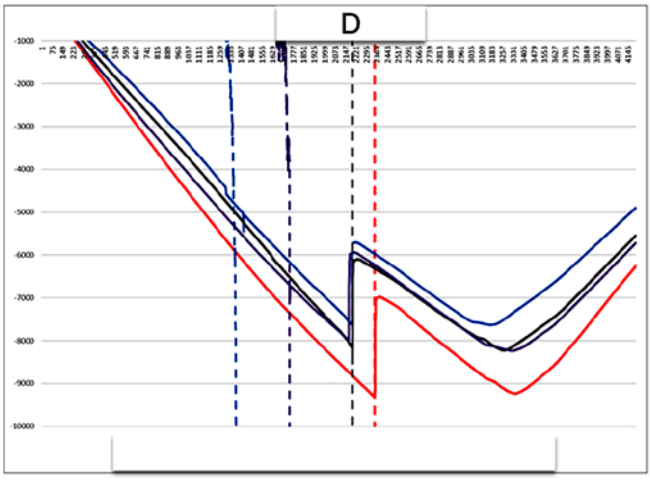

Figure 23: Strain and daisy-chain response for four Sample D boards.

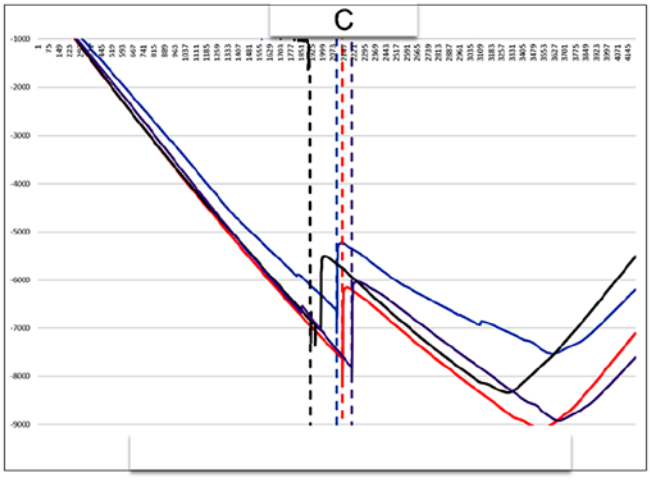

Figure 24: Strain and daisy-chain response for four Sample C boards.

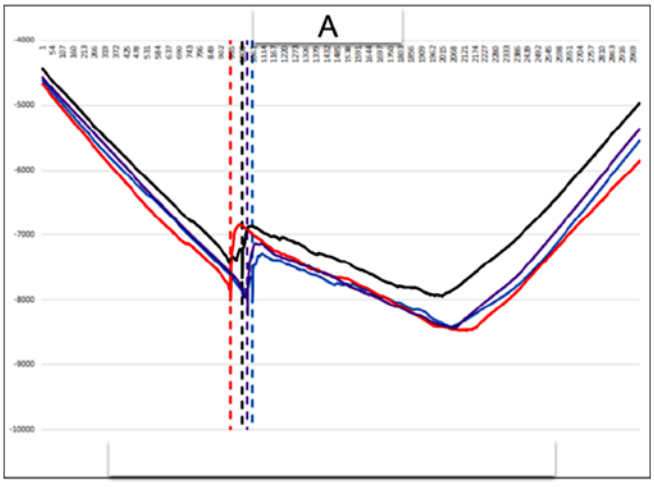

Figure 25: Strain and daisy-chain response for four Sample A (control) boards.

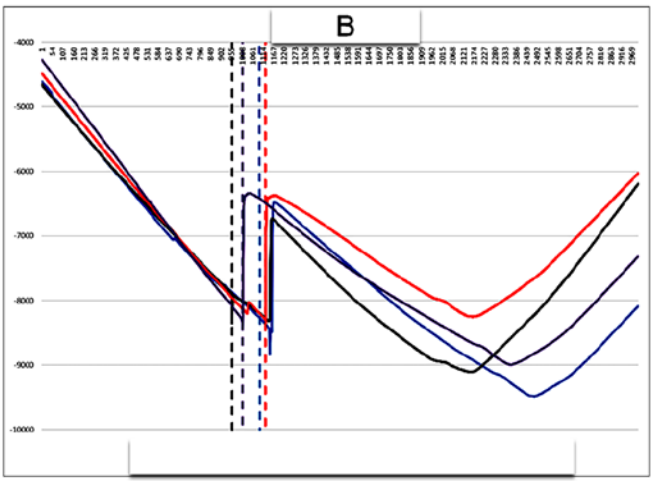

Figure 26: Strain and daisy-chain response for four Sample B boards.

4 Point Bend 35mm BGA 4.5 mm/Sec head speed - Monotonic Bend to Failure Sample Freq: 2K/Sec			
Material	Average Microstrains Over 4 Measurements	Maximum Microstrains Over 4 Measurements	Minimum Microstrains Over 4 Measurements
A -Control	7703	7963	7306
B	8172	8334	7890
C	7235	7811	6644
D	7313	9311	5031

Figure 27: Summary of strain and daisy-chain response ranges for the four paste sample boards.

These may be compromised solder joints. They may also indicate slight variance in the solder composition. More information would be needed to determine the reason for the slightly early failure.

From Figure 25, the continuity failures corresponded directly with the bulk failures for all boards tested. Interestingly, although these boards mostly failed at the board land pad-to-board interface, this material did not have the strongest response.

From Figure 26, Sample B boards had similar behavior to the control material but one board (blue line) had an open very slightly ahead of the bulk solder failure.

From Figure 27, the differences between the materials are less than the differences within each material. This indicates that there is little or no statistical difference. The slope and range of Material D needs to be studied further to determine if this is typical or an anomaly. Additional testing is underway.

From Figure 28, Material B performed the best while Material D the worst.

The failure modes were analyzed after dye and pry and cross-sectioning, and there were two primary failure modes. The control Sn3Ag0.5Cu material mostly failed below the

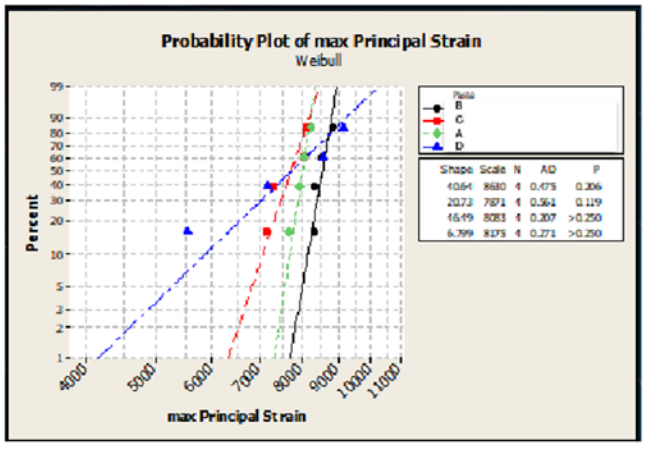

Figure 28: Results after bending four boards of each paste type to failure.

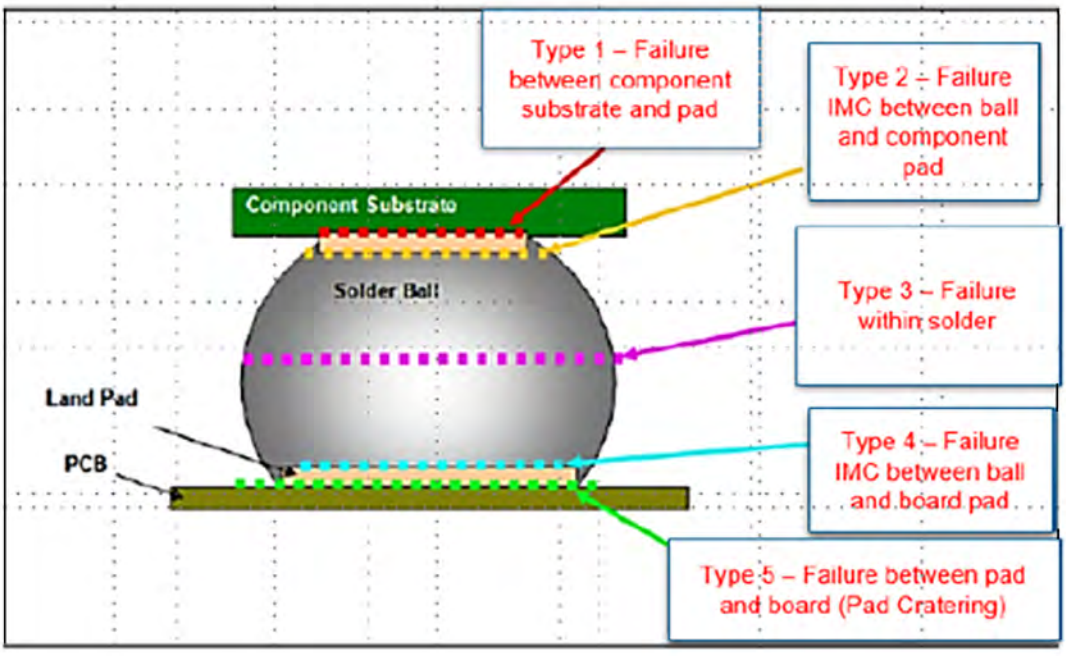

Figure 29: Failure mode descriptions. A Type 5 failure mode is between the board land pad and the board while a Type 4 failure is in the IMC on the board side.

board land pad (shown as Type 5 failure mode in Figure 29) and many pulled some board material (similar to pad cratering) while the low-temperature materials tended to break through the IMC (intermetallic) boundary in the bulk of the solder joint on the board side, shown as Type 4 failure mode in Figure 29.

Interestingly, the strongest point has historically been the bond between the board land pad and the board. In this (limited) test, the control material did not have the strongest response (Figure 30). This may indicate that the higher process temperatures of the SAC-305 reflow profile have an effect on the pad-to-board strength.

Board ID	Type 2	Type 4	Type 5	No solder joint failure
Board 1 – Control Paste	0	0	~65%	~35%
Board 2 – Control Paste	0	0	~60%	~40%
Board 14 – Paste A	0	~75%	0	~25%
Board 16 – Paste A	0	~75%	0	~25%
Board 7 – Paste B	~15%	~45%	~5%	~35%
Board 10 – Paste B	0	~60%	0	~40%
Board 3 – Paste C	~15%	~45%	~10%	~30%
Board 6 – Paste C	0	~60%	0	~40%

Figure 30: Results of the dye and pry and cross-section post-strain (solder joint) fracture failure mode analysis. The control paste mostly failed between the pad and the board while the other materials mostly failed at the IMC.

Reliability: Accelerated Temperature Cycle Testing

We followed JEDEC 9701 recommended procedures to perform accelerated temperature cycle testing. We mounted multiple daisy-chained and 0-ohm components to a four-layer PCB. The board was 62 mils (1.6 mm) with 18–20 boards used for each solder material. The boards were subjected to 0–100°C 40-minute temperature cycles with 10-minute ramps and dwells. We measured electrical continu-

ity at 200 cycle intervals for the following four components (Figure 31):

- 1196 PBGA, 35x35 mm, 1.0-mm pitch, SAC 305 (u309)
- 196 PBGA, 15x15 mm, 1.0-mm pitch SAC 305 (u1)
- 64 CBGA, 9x9 mm, 0.8-mm pitch, SAC 305 (u300)
- 2512 thin-film ceramic zero-ohm resistors (R350)

As of the time of this writing, we had reached 4,200 cycles with very few failures on any components other than the (expected) 2512 thin-film ceramic zero-ohm Resistors. Paste D boards were not assembled at the same time as the other pasteboards, so it had only completed 1,000 temperature cycles as of the time of this article without any failures (Figure 32).

As expected in Figure 33, the low-temperature (bismuth-containing) alloys slightly outperformed the control Material A during this relatively low strain rate testing.

Environmental Impact and Potential Cost Savings

With a greater than 50-degree peak temperature delta and a lower-temperature profile overall, it should be clear that the energy con-

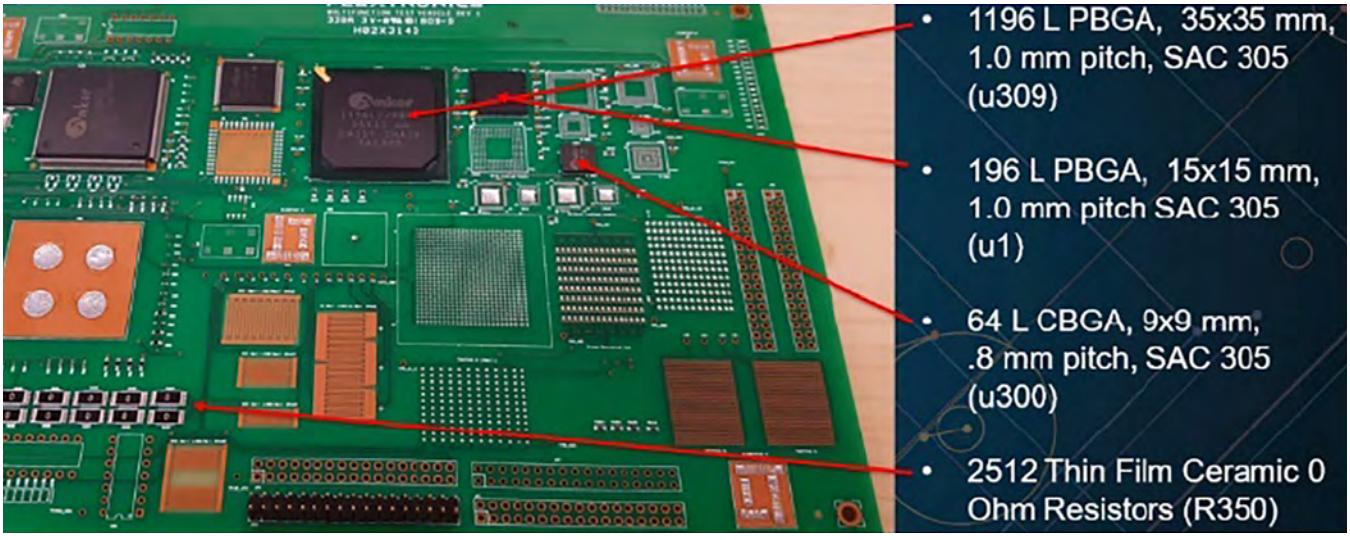

Figure 31: The test vehicle arrangement and the locations of the four monitored components.

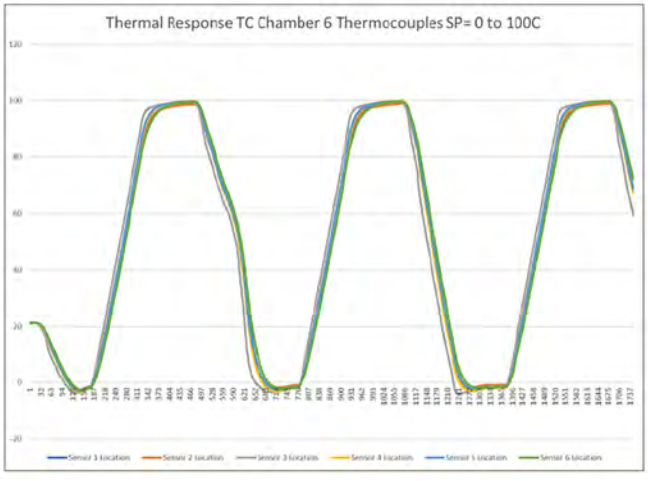

Figure 32: Temperature cycle chamber characterization response (0-100°C, 10-minute ramps and dwells).

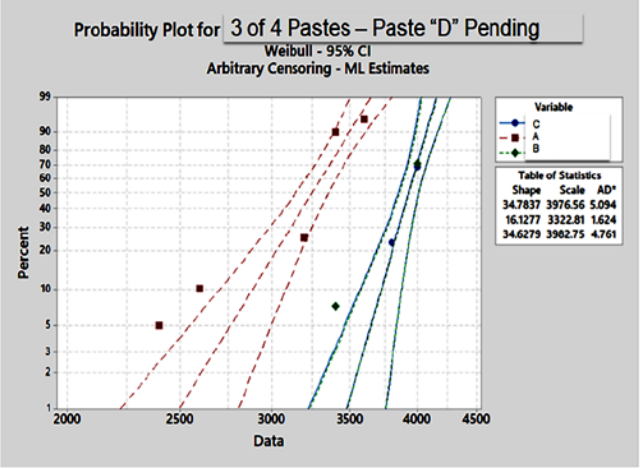

Figure 33: Weibull failure plots for the three materials (Pastes A, B, and C) on the 2512 capacitors.

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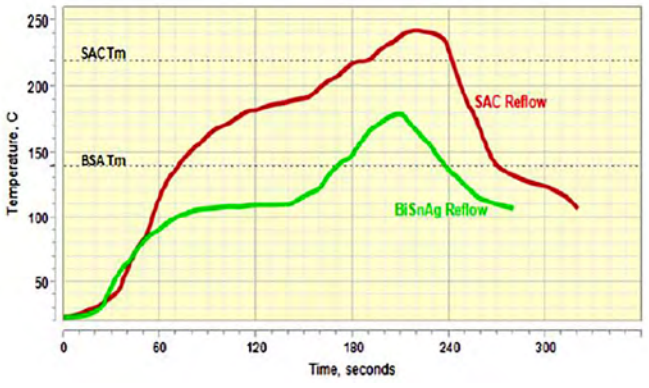

Figure 34: Comparison of the typical reflow profiles for both SAC-305 (red) and the low-temperature solder (green) [1].

sumption is significantly reduced during the reflow process (Figure 34). These low-temperature solders are estimated to save 20–25% in (reflow) energy cost over SAC-305.

It is also estimated that using these low-temperature solders would also reduce the CO_2 emissions by 1.1 metric tons per week [1]. This is roughly equivalent to 10 average gasoline vehicles (driven in the U.S.) per year.

Conclusions

Preliminary results investigating the low-temperature paste alloys against the Sn3Ag0.5Cu paste alloy look promising. Limited internal testing to date, combined with limited external testing data, indicates that these newer, doped, lower-temperature solders perform as well or better than Sn3AgCu (SAC305).

Further testing and evaluation is needed and is underway. We are proceeding with drop/shock and higher strain rate monotonic bend testing, which is where we expect to see a differentiation between the doped and non-doped solders under investigation.

Future Work

If the materials continue to make it past the tests previously mentioned, additional qualification testing will include SIR, cleanliness, and application-specific scenarios, such as large BGA assembly, high-mix assembly, paste-in-hole assembly, and rework.

Finally, to fully understand the manufacturing process window for reflow, a DOE will be conducted to define the range of peak temperatures and their effect on mixed alloy reliability across a multitude of alloys (i.e., when used to attach SAC-305 or low silver containing SAC125 BGAs. **SMT007**

References

1. S. Sahasrabudhe, S. Mokler, M. Renavikar, S. Sane, K. Byrd, E. Brigham, O. Jin, Pubudu, Goonetilleke, N. Badwe, S. Parupalli, "Low-Temperature Solder: A Breakthrough Technology for Surface-Mounted Devices," IEEE 68th Electronic Components and Technology Conference, 2018.

2. R. Aspandiar, "Characterization of Mixed Alloy SAC-BiSn BGA Solder Joints: Part II of Report on iNEMI Project on Process Development of Bi-Sn-Based Low-Temperature Solder Pastes," Pan Pacific SMTA.

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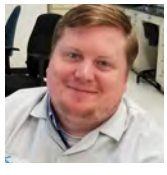

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Jon Bernal is an engineering technologist in the Advanced Manufacturing Engineering Group.

Robert Pennings and **Jie Jiang** are no longer with the company.

Supplier Highlights

Knocking Down the Bone Pile: Straightening Out Those Corners ▶

A PCB can be dropped, dinged, or mishandled as it is placed into a board carrier in the PCB assembly operations area. When the laminated material is damaged in this manner, can it be repaired? The answer, like most engineering answers, is that it depends.

Synergy Between Smart Manufacturing and the Secure Supply Chain (Part 1) ▶

As MRP and ERP functions follow computing trends and start to migrate into the cloud, a fundamental question is being raised as to whether these are still the right tools to use in today's modern Industry 4.0 driven factory, or whether these need to evolve, be enhanced, or even replaced to meet the more extreme requirements of operational flexibility as well as cope with volatile material availability in the market.

Laserssel Brings High-speed Soldering to New Application Areas ▶

Denis Barbini, general manager of Laserssel, talks about the company's new laser-selective reflow solution aimed at reducing a typical reflow oven's 10-minute cycle down to just 10 seconds as well as the overall benefits manufacturers could see from streamlining this process.

Co-owner Philip Kazmierowicz on New Role as KIC President ▶

On March 25, 2019, KIC—one of the leaders in reflow and thermal process control and smart oven technologies—announced that Philip Kazmierowicz, company co-owner, would take on the position of president. Nolan Johnson took that opportunity to sit down with Kazmierowicz to discuss KIC's history and his plans for the future of the company.

Smart Factory Transitions Are Attainable—With a Plan ▶

In a white paper, Zac Elliott, technical marketing engineer at Mentor, a Siemens Business, outlines a structured organization for smart factory implementation. In this interview, Elliott discusses how things have proceeded since the paper was published and talks about strategies for smaller firms and brownfield companies.

The Effectiveness of 75% IPA / 25% DI Extraction Solution on No-clean Flux Residues ▶

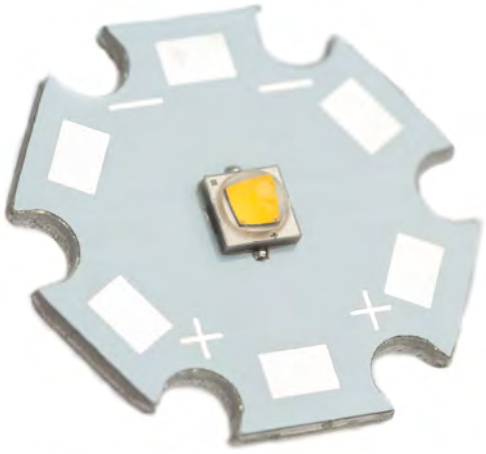
The continuous challenge in the electronics industry is to keep up with the demand for smaller, faster, and more reliable electronics. When it comes to cleaning, this rapid development of manufacturing and reliability challenges is juxtaposed with the slow pace of new test method development.

Yamaha Unveils Manufacturing Solutions at SMT Connect 2019 ▶

At the recent SMTConnect 2019 event in Nuremberg, Yamaha Motor Europe SMT Section revealed more details of new surface-mount equipment and software tools joining the Yamaha Total Line Solution to boost productivity and quality.

ITW EAE Launches PCB Temp Monitoring for Prodigy Dispenser ▶

ITW EAE is introducing a patent-pending option for the Camalot Prodigy dispenser that was developed to ensure process stability and increase yields for underfill applications.



Surface Treatment Enabling Low-temperature Soldering to Aluminum

Feature by Divyakant Kadiwala
AVERATEK CORPORATION

Abstract

The majority of flexible circuits are made by patterning copper metal that is laminated to a flexible substrate, which is usually polyimide film of varying thicknesses. An increasingly popular method to meet the need for lower cost circuitry is the use of aluminum on polyester (Al-PET) substrates. This material is gaining popularity and has found wide use in RFID tags, low-cost LED lighting, and other single-layer circuits. However, both aluminum and PET have their own constraints and require special processing to make finished circuits. Aluminum is not easy to solder components to at low temperatures, and PET cannot withstand high temperatures. Soldering to these materials requires either an additional surface treatment or the use of conductive epoxy to attach components. Surface treatment of aluminum includes the likes of electroless nickel immersion gold plating (ENIG), which is extensive wet chemistry and cost-prohibitive for mass adoption.

Conductive adhesives, including anisotropic conductive paste (ACP), are another alternative to soldering components. These result in component-substrate interfaces that are inferior to conventional solders in terms of performance and reliability. An advanced surface treatment technology will be presented that addresses all these constraints. Once applied on aluminum surfaces using conventional printing techniques such as screen, stencil, etc., it is thermally cured in a convection oven at low temperatures. This surface treatment is non-conductive. To attach a component, a solder bump on the component or solder printed on the treated pad is needed before placing the component. The aluminum circuit will pass through a reflow oven, as is commonly done in PCB assembly. This allows for the formation of a true metal-to-metal bond between the solder and the aluminum on the pads. This process paves the way for large-scale, low-cost manufacturing of Al-PET circuits.

Introduction

Aluminum is the most abundant metal in the earth's crust. Its alloys have found wide use as

alpha

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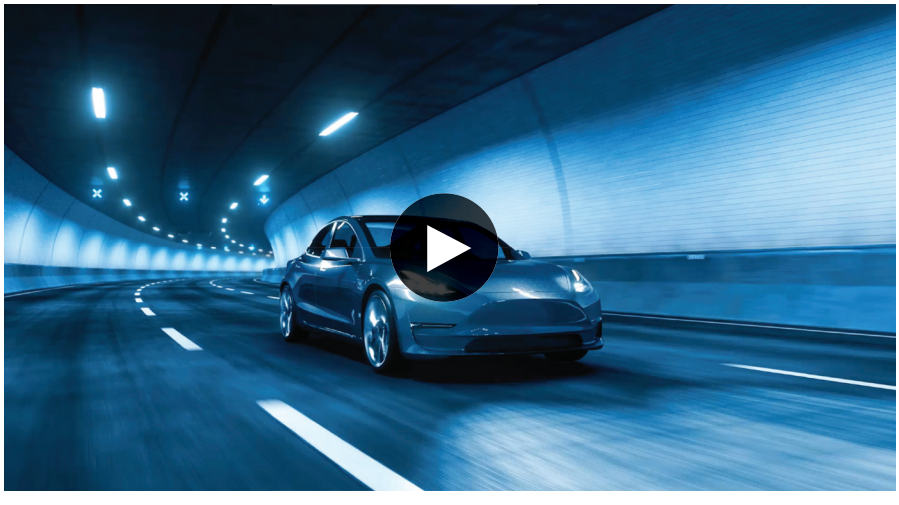

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a building material in the construction of automobiles, aircraft, bicycles, building frames, etc. Other uses range from electrical connectors, packaging cans and foils, and household utensils. While it is a material of choice in the above fields, it is second to copper in the field of flexible circuits.

This is despite the various advantages that aluminum has over copper. Aluminum is more than three times lighter than copper. The density of aluminum is 2.7 gm/cm^3 while that of copper is 8.92 gm/cm^3. Its electrical resistivity is 26.5 nΩ·m (at 20°C) while that of copper is 16.78 nΩ·m (at 20°C). Also, its thermal conductivity is 237 W/(m·K) while that of copper is 401 W/(m·K) [1].

Although it is not as good an electrical and thermal conductor as copper, it can radiate heat better than copper due to its lower density. Overall, aluminum has 68% of the conductivity of copper but has only 30% of the weight of copper. This means that a bare wire of aluminum weighs half as much as a bare wire of copper that has the same electrical resistance [2]. This will be similar for aluminum traces in the case of flexible circuits.

Also, aluminum is generally less expensive when compared to copper conductors. A recent check indicated the price of aluminum was 35% less than that of copper [1]. It is three times less expensive than copper on an equal weight basis and six times less expensive on an actual usage basis. This is the biggest advantage that aluminum has over copper. Table 1 lists the comparative properties of the two metals relevant to flexible circuits.

Flexible Circuits and Al-PET Substrates

The majority of flexible circuits are made using copper on polyimide (Cu-PI) substrates. These consist of copper foil laminated onto polyimide film. Varying the thickness of copper and polyimide gives rise to various combinations of thicknesses of Cu-PI to suit the conductivity and dielectric requirements of the end applications. Traces are formed using photolithography followed by a print-and-etch process. Components are soldered on to make the finished circuits. A reasonable selection of solders is available that can easily bond to copper traces without the need for any special surface treatment.

Property	Aluminum	Copper
Density	2.702 gm/cm3	8.92 gm/cm3
Electrical resistivity	26.5 nΩ·m (at 20°C)	16.78 nΩ·m (at 20°C)
Thermal conductivity	237 W/(m·K)	401 W/(m·K)

Table 1: Properties of aluminum and copper [3].

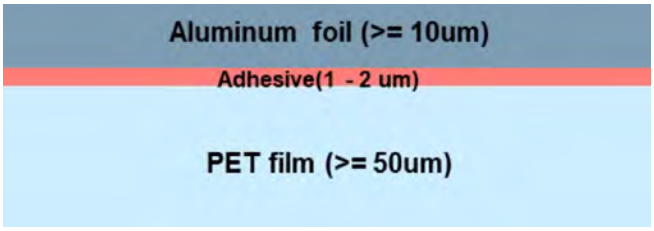

Figure 1: Typical laminated construction of Al-PET substrates.

An increasingly popular method to make flexible circuits is by using aluminum on PET (polyethylene terephthalate) or Al-PET substrates. These are available in varying thickness of aluminum foil laminated onto PET film (Figure 1).

While aluminum is less expensive than copper, PET is also significantly cheaper than polyimide film. Hence, lower material cost is a major driver for the increasing use of Al-PET substrates, but their use has been limited because of processing challenges.

The process to generate the traces on aluminum substrates is similar to that of copper. A dry-film or liquid resist is used for photolithography, which is then followed by chemical print-and-etch to form aluminum traces. But attaching the components onto aluminum is a challenge. Unlike copper, it is not easy to solder to aluminum. Soldering to aluminum is difficult because of the presence of a thin layer of aluminum oxide. This layer forms naturally when the bare metal is exposed to air. Since most flexible circuit manufacturing is done under atmospheric conditions, all aluminum surfaces will have an oxide layer. While the formation of this natural oxide is self-limiting, its presence cannot be overcome by the

flux used in existing solder pastes. If harsher fluxes are used within solder pastes to address the aluminum oxide problem, they will cause corrosion of the very thin aluminum layers and thus reliability problems.

There are two methods currently used to attach components to Al-PET substrates: one is the zincate and plating process while the second is using conductive epoxy.

Al-PET Circuits Using Zincate and Plating Finish

Special processing can be done on the aluminum pads to remove and prevent the formation of aluminum oxide. These include ENIG, nickel-palladium, or nickel-silver plating. These processes require surface preparation called the zincate process [4]. The purpose of zincation is to clean the aluminum surface for plating of the nickel or other metal. Figure 2 shows an example of a zincate process.

As can be seen in Figure 2, the zincate process involves extensive wet chemistry. The dwell time, which can vary per the alloy of aluminum, ranges from 5–17 minutes. In addition, a plating finish must follow zincation before components can be attached. These add extra costs that make it difficult for large scale adoption of Al-PET substrates in the field of flexible circuits.

Al-PET circuits Using Conductive Epoxies

Al-PET substrates are widely used to manufacture radio-frequency identification (RFID) tags, smart tags, and low-end LED lighting. These are patterned using a roll-to-roll process for print and etch. Components are attached roll-to-roll or in panels, using silver-based conductive epoxies, including anisotropic conductive paste (ACP). The assembly process begins with the application of conductive epoxy on the pad or chip. The chip is then flipped onto or placed on the pad followed by heat and pressure. This cures the epoxy and the chip is attached. While they are used in very small amounts in regular RFID tags, they are a big part of the total expense in making smart tags. These tags are larger than RFID tags and have a lot more components that demand more conductive epoxy per smart tag.

Conductive epoxies have their own challenges. They are made of adhesive epoxy filled with conductive metal particles—usually silver. They are typically syringe applied, require longer cure times, have pot-life issues, and are electrically inferior to conventional solders. In addition, they must be stored at low temperatures in special freezers to control the polymerization of the epoxy. Overall, they are very expensive and limit the use of Al-PET substrates [5].

Al-PET Circuits Using Advanced Surface Treatment

An advanced surface treatment chemistry has been developed as a new alternative. It enables soldering to aluminum without zincate and plating. It can be printed directly on

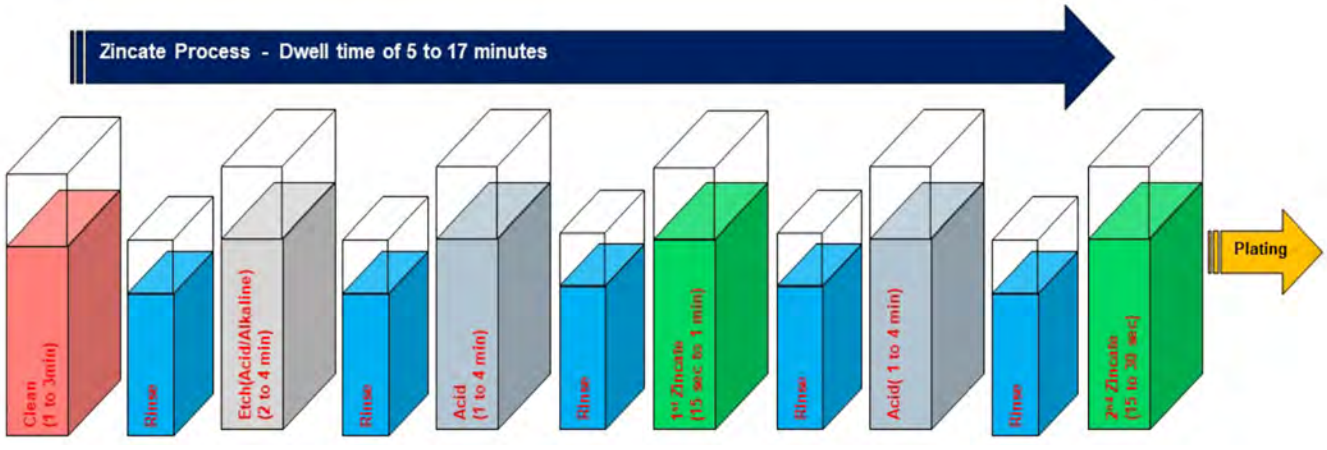

Figure 2: Zincate process used to prepare the aluminum surface for plating.

the aluminum pads where components need to be assembled. The print thickness depends on the application. Any of the conventional printing techniques can be used, including screen, stencil, etc. The aluminum surface does not need any surface cleaning or preparation. Once this treatment compound is printed, it must be thermally cured to leave the pad surface treated, active, and ready to accept solder. Cured treatment compound is non-conductive and makes room for easy print registration.

To attach a component, it needs solder—via printing or plated bumps—placed on the activated pad and then passed through a reflow oven. The compound overcomes the aluminum oxide layer and allows the formation of a true metal-to-metal bond between the solder and the aluminum on the pads. Thus, both the electrical properties and the bond strength are far superior to silver epoxies. In addition, it can be stored at room temperature and reused multiple times [5]. Figure 3 shows an overview of the process to use the surface treatment.

Surface Treatment Cure Temperature: PET Constraints and Solders

The surface treatment requires a low-temperature cure of less than 100°C. The required dwell time ranges from a few seconds to a minute depending on the oven type and air flow. Conveyor-based reflow ovens in PCB assembly houses can cure the printed surface treatment. A variety of solders can be used to attach to aluminum using a surface treatment. However, the type of solders that can be used on Al-PET substrates is limited by the PET film. Table 2 lists key properties common to heat-stabilized PET films.

Property	Value	Units
Glass Transition Temperature	78	°C
Thermal Contraction (150°C, 30 min.)	<= 0.3 MD, <= 0.1 TD	%
Upper Temperature for Processing	150	°C
Melting Point	250–260	°C
Dielectric Constant	3.1	
Dielectric Strength	3000	Volts/25 µm

Table 2: General properties of heat-stabilized polyethylene terephthalate film (PET film) [6 & 7].

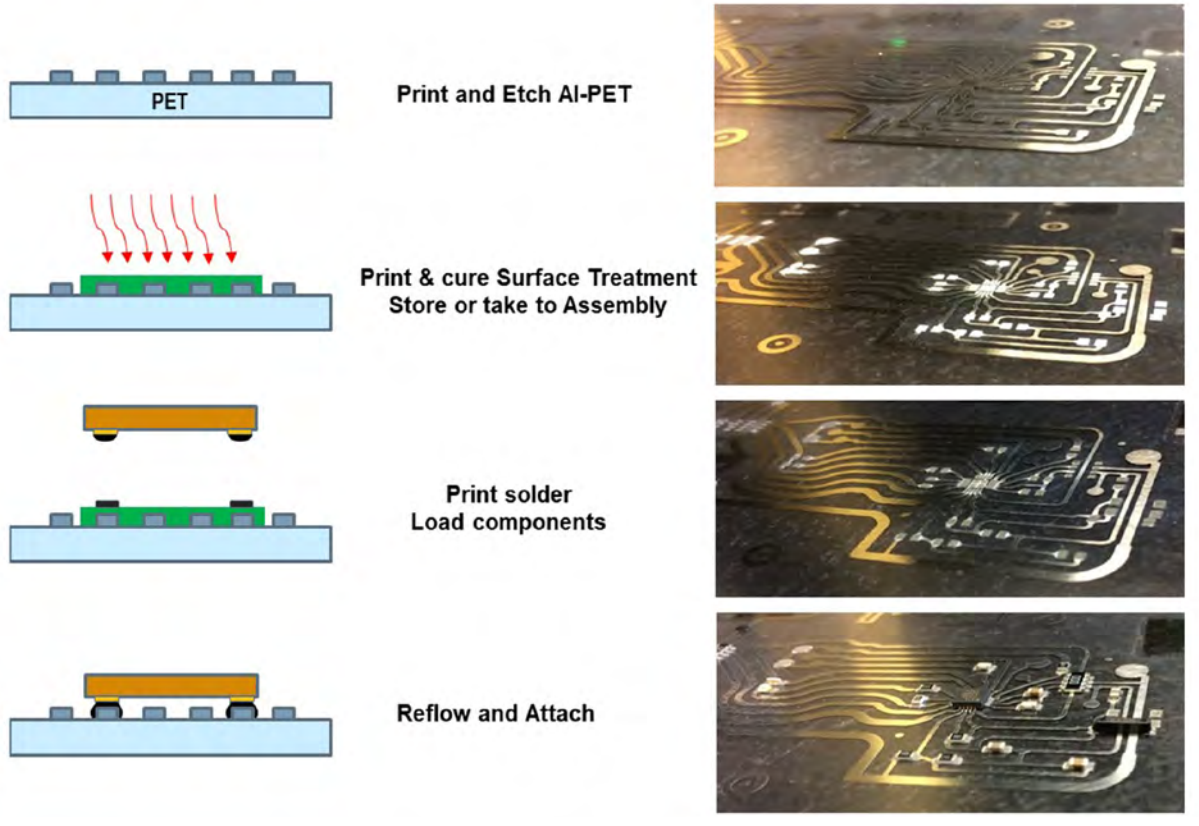

Figure 3: Overview of the process using surface treatment to solder to aluminum.

Per Table 2, the working temperature of PET films is limited to about 150°C. This is the temperature that they can be subjected to for an extended period and rules out the use of most solders that have a higher melting point. But PET films can withstand higher temperatures for a brief period. This opens the door for using a variety of low-temperature solders for assembly of components to Al-PET substrates. Most of the solders are made up of tin (41–42%), bismuth (57–57.6%) and silver (0.4–2%) in various flux systems with a melting point of ~138°C. The highest temperature during reflow is about 185°C but only for a very short time.

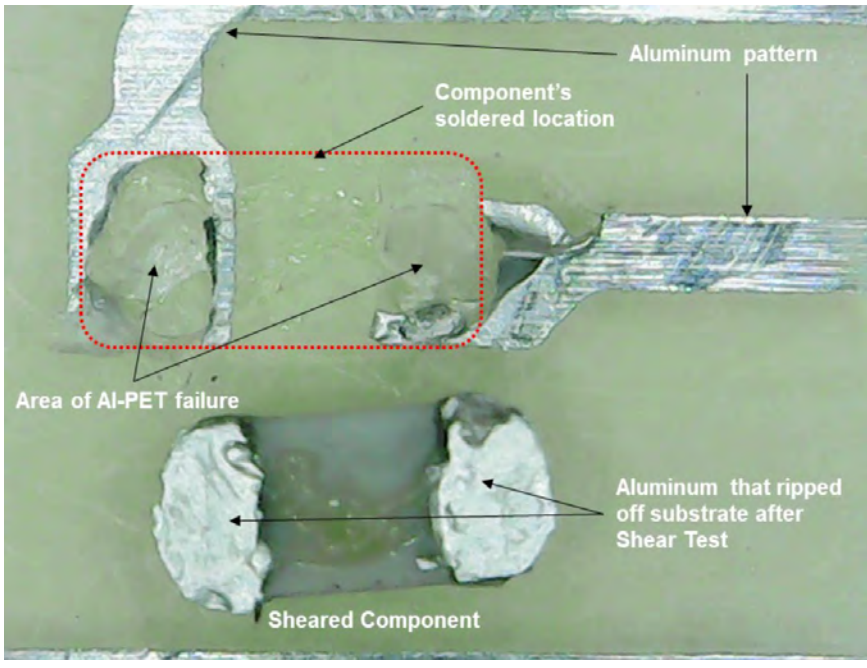

Figure 5: Shear test results showing failure between aluminum and PET substrate (package: capacitor 0805, shear value: 22N/mm²).

Assembly Trials Made Using Surface Treatment and Related Observations

Boards were made with 10-mm aluminum foil laminated onto 125-mm film of PET. The etched design was a smart tag that had components including resistors, capacitors, LEDs, QFNs, battery holders, and RFID chips. The surface finishes of these components were typically plated with Ni, Pd, Au, or Sn. Special fixtures were designed to hold the boards during processing. Figure 4 shows a partial view of the smart tag design used.

The trials were done at a local PCB assembly house and consisted of two steps. The first step was to mount etched aluminum panels on the fixture and print surface treatment compound using a stencil made of stainless steel, 737 x 737 mm, 50 mm. A conveyor-based reflow oven was used to cure the surface treatment compound at 85°C. The second step was to use the same fixtures to hold the panels during stencil printing of solder, pick-and-place loading of components, and reflow oven processing. The stencil used for the solder paste was stainless steel, 737 x 737 mm, 100 mm. The solder used was commercially available, lead-free, low-temperature, no-clean Sn/Bi/Ag with a melting point of 138°C. The reflow cycle used was as recommended by the manufacturer of the solder paste.

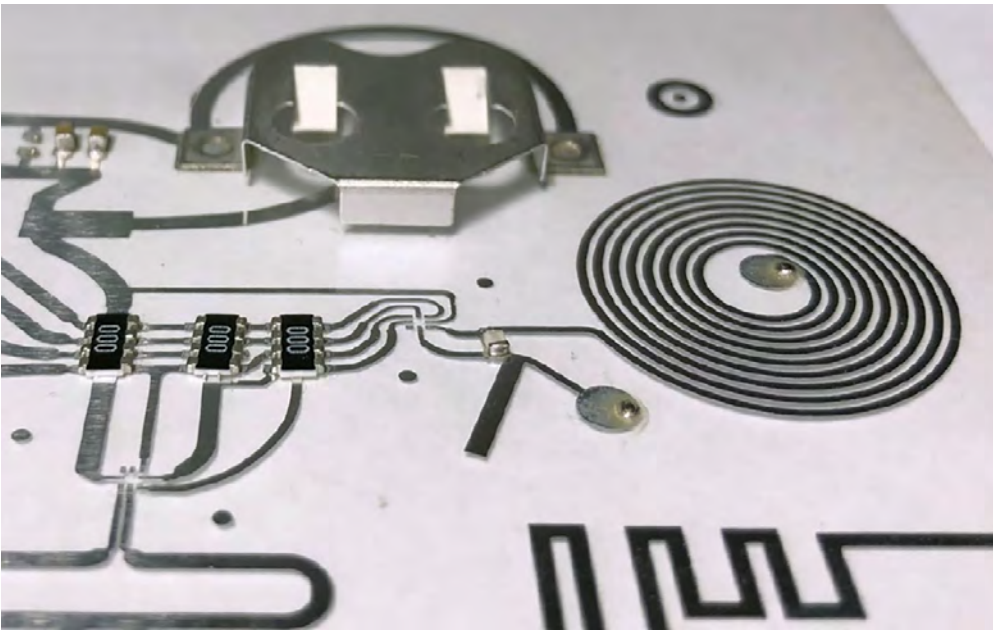

Figure 4: Smart tag design used to test surface treatment.

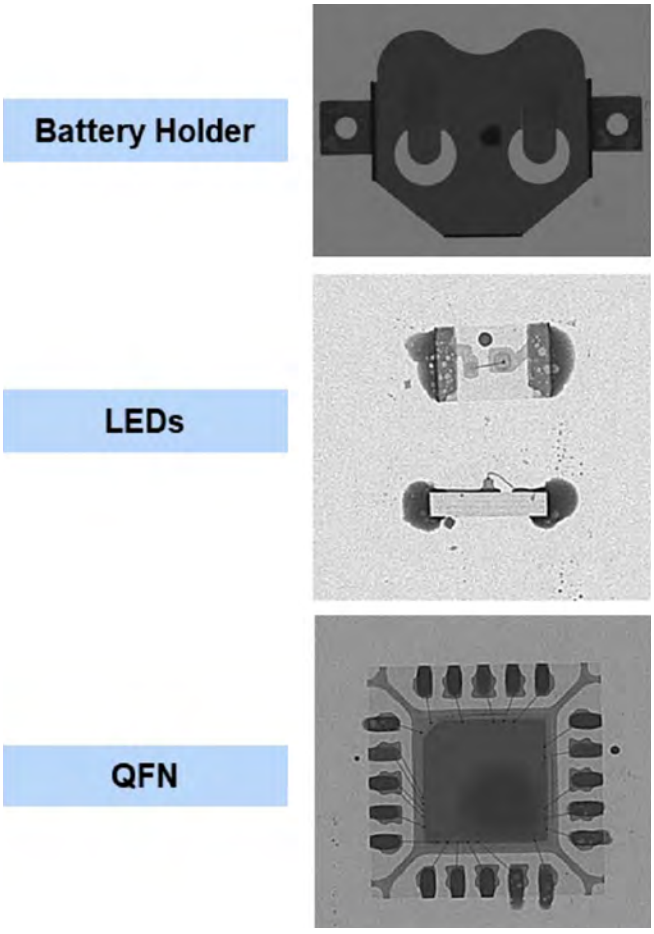

Figure 6: X-ray images of components showed good solder joints.

The resultant bond was characterized by shear tests, X-rays, and cross-sectional analyses of the intermetallic formed with the aluminum.

Shear tests were done to gauge the strength of the bond. They were also done on various components: resistors, capacitors, and chips. The tests were done using a production force gauge. The shear test values were greater than 15 N/mm^2. The solder-aluminum bond was so strong that failure was often between the aluminum and PET. Figure 5 depicts such failures.

The assembled boards were also inspected using X-ray. This was done to get a better understanding of the wetting of the solder. When examined under X-ray, the components showed good solder joints and voids were within an acceptable limit of less than 30% of the solder joint area. The key process parameters were the thickness of surface treatment, thickness of solder, and reflow profile of the solder. Figure 6 shows X-ray images of the components.

Cross-sections were done on various components, including capacitors, battery holders, and QFN chips. These give a better view of the wetting of the solder, and the intermetal-

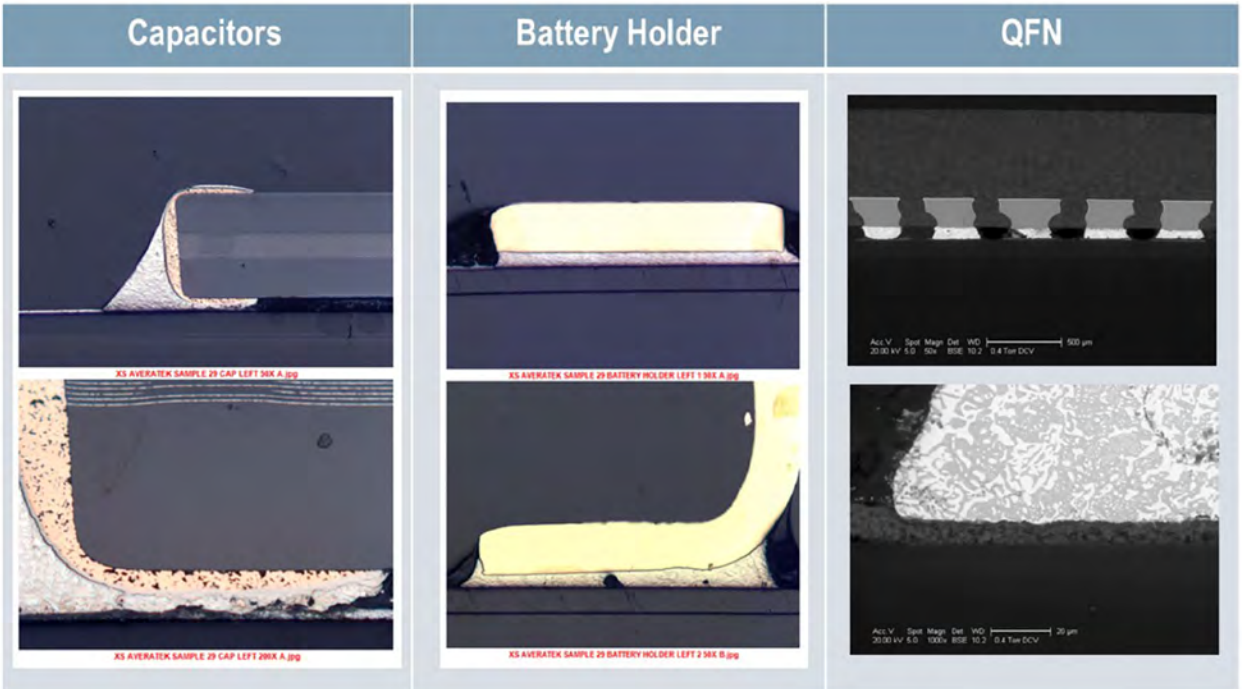

Figure 7: Cross-sections of capacitor, battery holder, and QFN/BTC soldered using surface treatment.

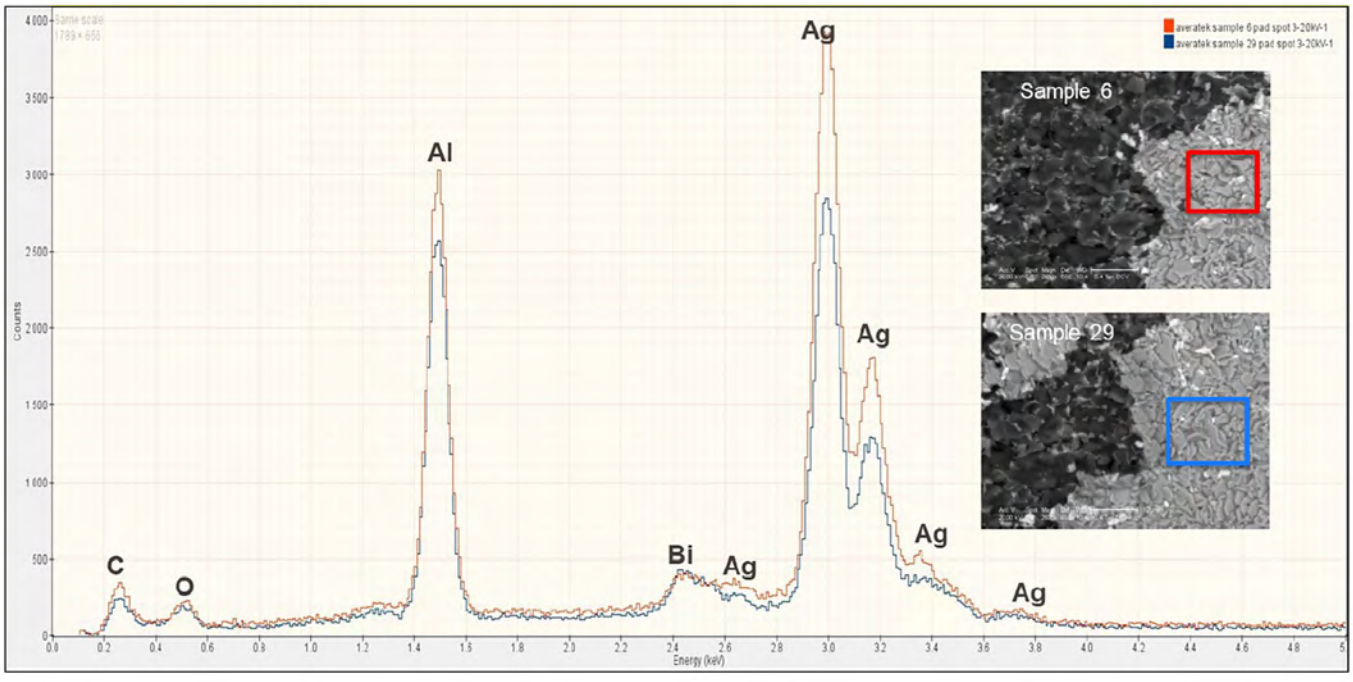

Figure 8: EDS spectra from the pad side after pulling resistor from pad showing Ag-Al intermetallic.

lic formed with the aluminum. Figure 7 shows some cross-sections.

As can be seen, while the solder wet and bonded well to the aluminum in most areas, voids were within the acceptable limit and are seen under the capacitor and battery holder's pad. These were further examined by doing an energy dispersive X-ray spectroscopy (EDS). Figure 8 shows an EDS of one such resistor pad.

As can be seen in the EDS, there is evidence that the surface treatment results in the formation of a silver-aluminum (Ag-Al) intermetallic with some presence of bismuth.

Conclusions

The surface treatment was shown to enable soldering to aluminum. Since solders vary in metal composition and flux, they each will have specific reflow profiles. Additional work may be needed to fine-tune reflow parameters for specific applications to get consistent wetting and good solder joints. Most new soldering applications would require such process development. Overall, this surface treatment has the potential to open the path for large scale use of Al-PET substrates. This could revolutionize the manufacturing of smart tags, RFID tags, and single-layer aluminum circuits. **SMT007**

References

1. Weast, R.C. *Handbook of Chemistry and Physics: 66th Edition,* CRC Press, 1985.

2. Anixter Inc. "Copper vs. Aluminum Conductors."

3. Based on price listing on Market Insider in September 2018. Actual prices will vary on a daily basis.

4. MacDermid. "Metex 6811 Cyanide Free Liquid Zincate Datasheet."

5. Averatek. "Mina: Facile Soldering to Aluminum for RFIDs."

6. "Dielectric Constants at 20°C."

7. Omnexus. "Glass Transition Temperature Values of Several Plastics."

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Common Machine Errors and How to Avoid Them

The Mannifest
Feature Column by Chris Ellis, MANNCORP INC.

When it comes to the quality of SMT boards you produce, it can be difficult to know where to begin and what features various PCBA machines offer are most important. To avoid common errors that could compromise the boards you're looking to produce, be sure to keep an eye out on these key features before assembling your line.

The first thing to keep in mind when putting together your SMT assembly area is that every step of the process is equally important. Printing, placing, and reflow are all essential stages that need to be considered with equal amounts of care and attention.

Consider how involved the stencil printing process will be for your boards. While simpler board configurations can easily get by with manual or semi-automatic printing processes, more complex boards that use 01005 chips, micro BGAs, or fine-pitch components should make use of a printer with vision alignment, programmable squeegee pressure, and programmable squeegee speed. This will ensure consistent results and minimize the possibility of error that could occur during the printing process. Without these features, you run the risk of costly defects, such as bridging or insufficient or excessive solder.

When choosing your pick-and-place machine, accuracy is your key concern. You should make certain your pick-and-place has the capability to position parts with no component more than 25% off the pad before the reflow process. This is only a minimum requirement, of course, and an even high degree of accuracy is preferable. For the reflow process itself, you should ensure that the oven has the capability to run separate unique profiles per

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board. Today, ovens are available with predictive profiling features that can cut down on guessing and testing, and many profiling software options have become better at providing you with an accurate, workable profile on the first try.

One option you may want to consider is automating your hand soldering process by use of selective solders or wave soldering machines. Wave solder machines are generally considered a better option for single-sided boards; otherwise, pallets or masking will be required unless you've decided to use glue or adhesive to hold down resistors and chips to solder them on the wave. With wave soldering, you'll experience a more consistent solder joint than hand soldering. Selective solders, on the other hand, are a great choice for complex double-sided board configurations and eliminating hand soldering in general.

While it's important to take care when assembling your SMT line, errors in the assembly process are nearly impossible to 100% eliminate. This is where an inspection station and functional testing can come in handy. An automatic optical inspection (AOI) option can allow you to identify possible issues with your board as they occur. This also means that you'll be aware of possible complications in your line before they become even more of an issue by making their way into the field or compromising multiple boards, multiplying the cost of repairs.

Should the use of an AOI or functional test detect any defects in your boards, a rework station can make remedying those defects go smoothly. Any rework station that simulates a reflow oven and has automatic removal and placement capabilities eliminates any problems related to operators hand-removing parts, lifting pads, and possibly causing damage to boards.

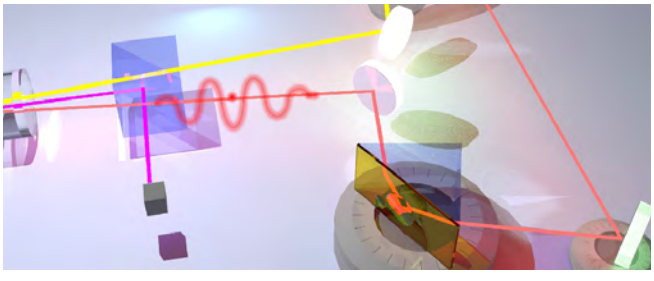
There are a number of factors to consider when beginning in-house SMT production, no matter the application of your boards. Taking care to make the right choice for accomplishing each step in the process at the outset can save you a number of headaches down the road. Whatever the final implementation of your boards, you want to make certain that your assembly process is as accurate as possible. **SMT007**

Chris Ellis is a sales manager/engineer for Manncorp Inc. To read past columns or contact Ellis, click here.

Quantum-squeezed Light Cuts Noise

Oak Ridge National Laboratory physicists studying quantum sensing, which could impact a wide range of potential applications from airport security scanning to gravitational wave measurements, have outlined in *ACS Photonics* the dramatic advances in the field.

"Quantum-enhanced microscopes are particularly exciting," ORNL's Ben Lawrie said. "These quantum sensors can 'squeeze' the uncertainty in optical measurements, reducing the uncertainty in one variable while increasing the uncertainty elsewhere."



Squeezed light refers to a quantum state where the statistical noise that occurs in ordinary light is greatly reduced. Squeezed atomic force microscopes (AFMs) could operate hundreds of times faster than current microscopes while providing a nanoscale description of high-speed electronic interactions in materials. This enhancement is enabled by removing a requirement in most AFMs that the microscope operates at a single frequency.

Future sensing technologies that harness quantum properties could be deployed as new quantum-enabled devices or as "plug-ins" for existing sensors.

(Source: Oak Ridge National Laboratory)

MilAero007 Highlights

NASA Awards Artemis Contract for Lunar Gateway Power, Propulsion ▶

In one of the first steps of the agency's Artemis lunar exploration plans, NASA announced the selection of Maxar Technologies—formerly SSL—to develop and demonstrate power, propulsion and communications capabilities for NASA's lunar Gateway.

Army Project Develops Agile Scouting Robots ▶

In a research project for the U.S. Army, researchers at the University of California, Berkeley developed an agile robot called Salto that looks like a Star Wars Imperial walker in miniature and may be able to aid in scouting and search-and-rescue operations.

Sikorsky HH-60W Combat Rescue Helicopter Achieves First Flight ▶

The Sikorsky HH-60W Combat Rescue Helicopter achieved first flight at Sikorsky's West Palm Beach, Florida site—an important step toward bringing this all-new aircraft to service members to perform critical search and rescue operations.

Lockheed Martin's Sikorsky Receives Contract to Build 12 CH-53K Heavy Lift Helicopters ▶

Sikorsky, a Lockheed Martin company, will build 12 production CH-53K King Stallion helicopters under a new $1.13 billion contract from the U.S. Navy.

Nano Dimension and Harris Receive Grant for ISS Project ▶

Nano Dimension Ltd. has received grant approval from the Israel Innovation Authority for developing hardware, in cooperation with Harris Corp., that will fly on the International Space Station (ISS) and communicate with Harris' ground-based satellite tracking station in Florida.

BAE Systems' Joint Strike Fighter Underpins Advanced Manufacturing Growth in South Australia ▶

BAE Systems Australia celebrated the production of the 15,000th titanium part produced at Edinburgh Parks in South Australia for the world's largest defense program—the F-35 Joint Strike Fighter.

Plexus Expands Darmstadt Design Center ▶

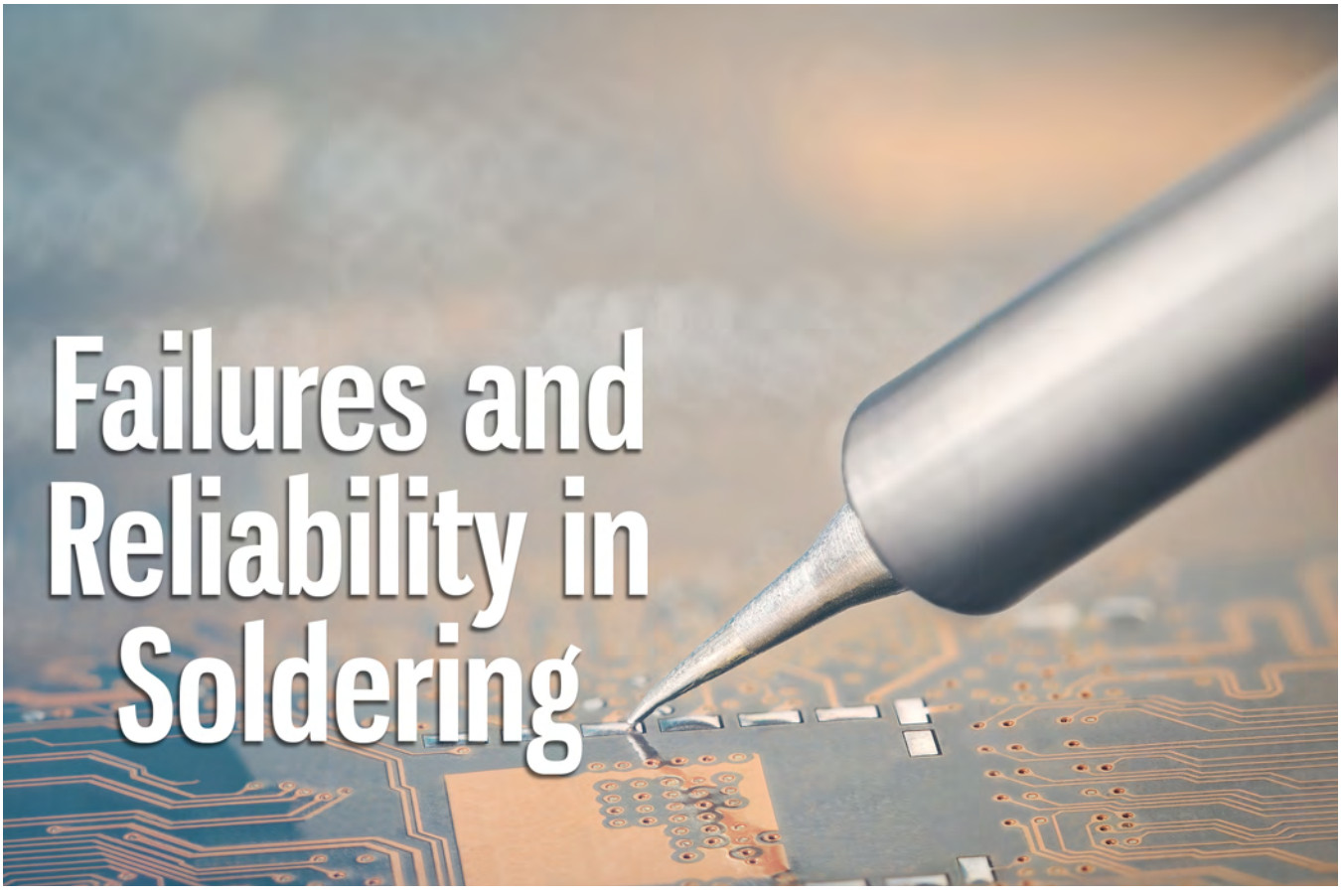
Plexus Corp. recently opened its expanded design center in Darmstadt, doubling its engineering capacity in Germany.

NASA's Juno Finds Changes in Jupiter's Magnetic Field ▶

NASA's Juno mission to Jupiter made the first definitive detection beyond our world of an internal magnetic field that changes over time—a phenomenon called secular variation.

NextFlex Launches $10.5M Funding Round for Anti-Counterfeiting, Flex Batteries, and Hypersonics Innovation ▶

The PC 5.0 total project value is expected to exceed $10.5 million (project value/investment figures include cost-sharing), bringing the total anticipated investment in advancing flexible hybrid electronics since NextFlex's formation to over $83.5 million.



Failures and Reliability in Soldering

Feature by Michael Gouldsmith and Zen Lee
THERMALTRONICS

The definition of failure is "the lack of success in doing or achieving something, especially in relation to a particular activity." If the activity is concerning a soldering process, such a failure can have a downstream impact far beyond the actual solder joint. In this regard, it is first necessary to understand what constitutes a good solder joint because appearance is too often deemed a success.

These challenges to solder joint reliability were exemplified when, in July 2006, the RoHS directive came into effect, and the higher thermal demands of lead-free solders forced all manufacturers of soldering irons to focus on improved heat transfer. This requirement was further complicated by the ongoing decrease in component sizes and the fact that many PCBs are becoming more like heat sinks due to multiple layers and other factors. The importance, therefore, is for soldering irons to provide:

- A fast response (speed)
- No overshoot (control)

Certainly, most systems today offer good or even excellent performance in thermal energy capability, but difficulties emerge in those systems using conventional ceramic heater technology, especially concerning:

- Tip-to-ground resistance (difficult to maintain)
- Tip-to-ground voltage leakage (difficult to maintain)
- Thermal transfer efficiency
- The potential for solder splatter (due to temperature overshoot)
- A requirement for calibration of the thermocouple

In this article, we will explore the considerations necessary to achieve good solder joints and offer some practical rules for good solder joints and how to achieve them reliably. We will also discuss other thermal energy factors to keep in mind.

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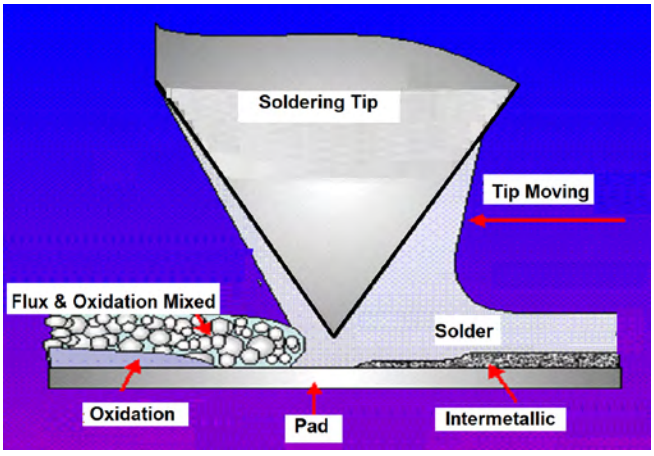


Figure 1: Components of a good solder joint and their relative placement during the creation of a solder joint.

The considerations necessary to achieve good solder joints are (Figure 1):

- The formation of an intermetallic layer
- Solder joint structure
- Joint temperature (military standard)
- Tip temperature vs. joint temperature
- Maintenance of the soldering profile (similar to that found in a reflow oven)

When copper comes in contact with molten solder, it forms two distinct intermetallics between the copper and the tin contained in the solder (Figure 2):

- Layer of "e-phase" (Cu3Sn) next to copper
- Layer of "h-phase" (Cu6Sn5) a thicker layer above

Tin is depleted by the formation of intermetallics, so in tin-lead solders, there will be a resultant lead-rich region.

A thin, intermetallic layer is necessary to produce wetting; however, thicker intermetallic layers may alter the appearance of the joint and have an adverse effect on its integrity. Some of the reasons are:

- Intermetallics are frequently brittle, and differences in CTE (coefficient of thermal expansion) between intermetallic and solder can contribute to internal stress
- Depletion of one element of the surface may impair solderability

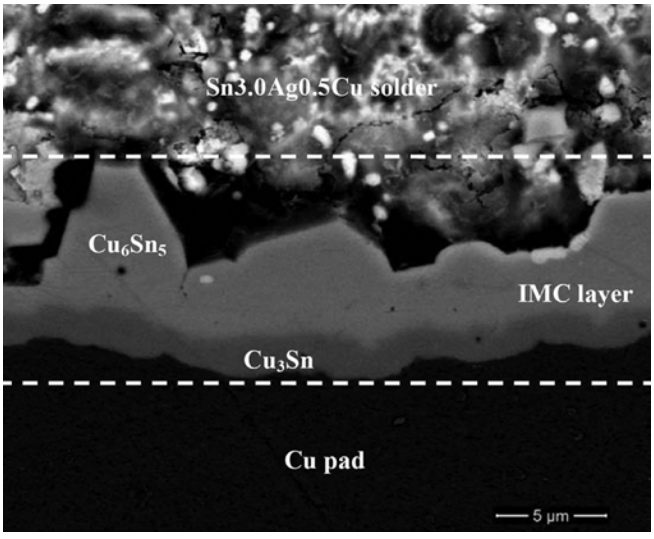


Figure 2: Cross-section showing the two distinct intermetallics between the copper and tin.

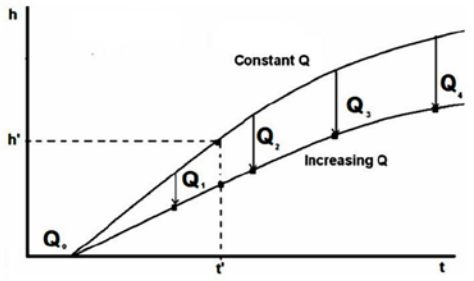
Nevertheless, without an intermetallic layer, there is no valid soldering joint, and once created, the layer grows at any temperature and accelerates exponentially as temperatures increase. This growth continues until the intermetallic compounds (the base metal) occupy the entire joint, and/or the solder is exhausted.

The rules for good solder joints are:

- Solder as quickly as possible
- Use the lowest possible soldering temperature that yields acceptable joints
- Avoid repeated soldering to improve the appearance of the joint since added exposure to high temperatures only increase the intermetallic layer. The joint may look pretty but is weaker or stressed
- Remember that the intermetallic layer grows at any temperature but accelerates exponentially at elevated temperature levels. Rates of dissolution of various metals also will rise with increases in temperature (Figures 3 and 4)

Reliable Solder Technique

Having established what considerations are necessary to form a reliable solder joint, the next step is to understand how to achieve this and what processes should be followed. While much of the focus in soldering is placed on the



Activation Energy is growing as thickness is growing, $Q_0 < Q_1 < Q_2 < Q...$

Figure 3: Activation energy increases in relation to the thickness.

- **Common Practice**
- Joint temperature is the solder melting temperature plus 40°C
- Solder tip touches joint – typically 2-5 seconds

Solder	Temp +40°C
60/40	183°C
Sn 3.8Ag 0.7Cu	217°C
Sn0.7Cu	227°C

Figure 5: Tracking solder joint temperature is preferred over soldering tip temperature.

tip idle temperature, solder joint temperature is more relevant than of the "no-load" tip idle temperature (Figure 5).

As noted in Figure 5, the recommended approach to reliable soldering is to focus on joint temperature rather than just tip temperature, since the correct formation of the solder joint is especially reliant on the right amount thermal energy being applied. In these circumstances, a soldering iron providing better thermal transfer is capable of using a lower tip temperature to deliver enough thermal energy to form a reliable solder joint.

Soldering irons with less efficient thermal transfer properties generally require higher temperatures to achieve the same result. However, the risk is the formation of a thicker intermetallic layer, which may be stressed and the likelihood of potential damage to components and the pad.

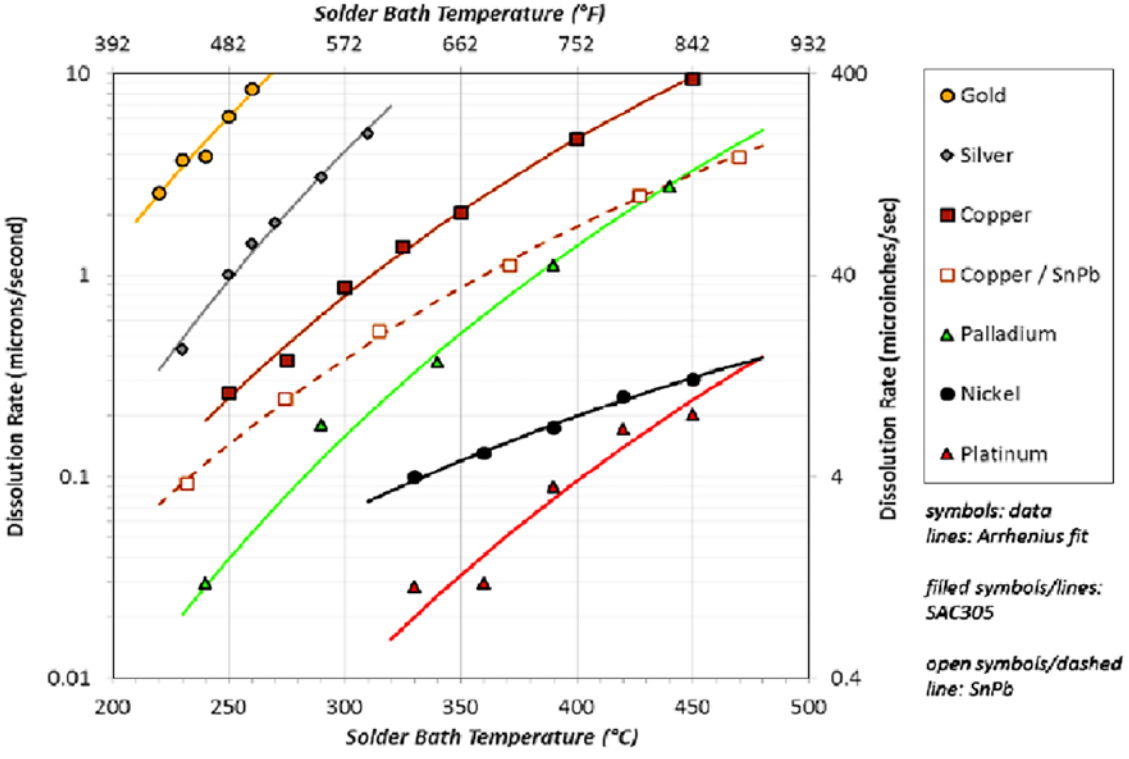


Figure 4. Rate of dissolution.

Using a reflow oven as an example of a typical lead-free solder profile, it can be noted from Figures 6 and 7 that the process involves, preheat—ramp up—reflow, and cool down with the actual reflow period in the range of 5–10 seconds maximum.

In hand soldering, the same reflow profile should be evident and is a process where thermal energy is transferred from the heater through the solder tip to the joint. This takes place as follows (Figure 8):

1. When the solder tip touches the pad with solder, stored energy in the copper tip will transfer to the joint (note that the stored energy is not controllable once it touches the joint)

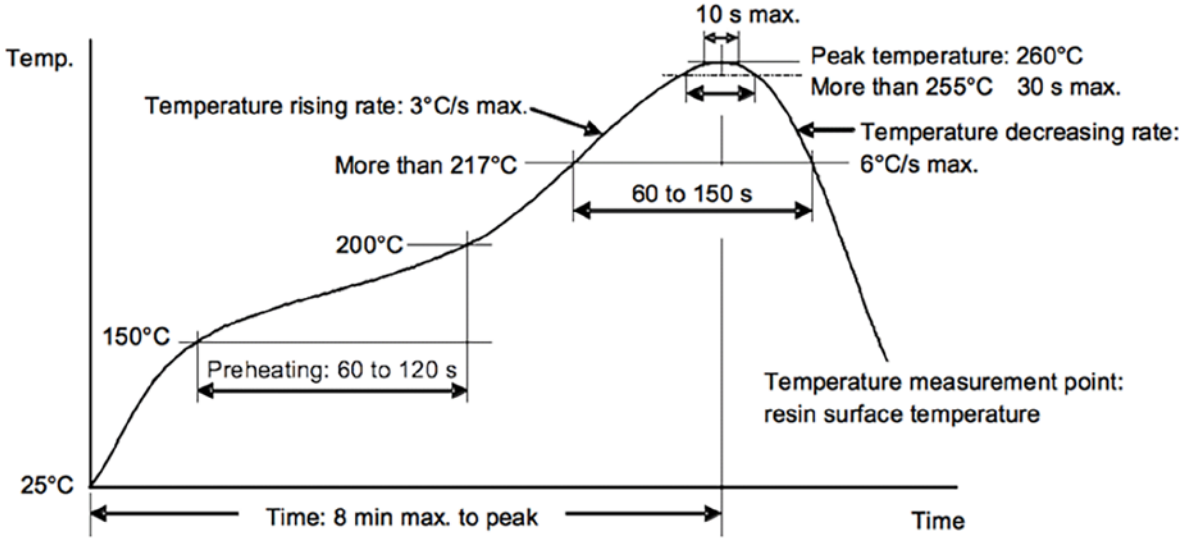


Figure 6: Reflow oven temperature profile for delivering the correct amount of thermal energy.

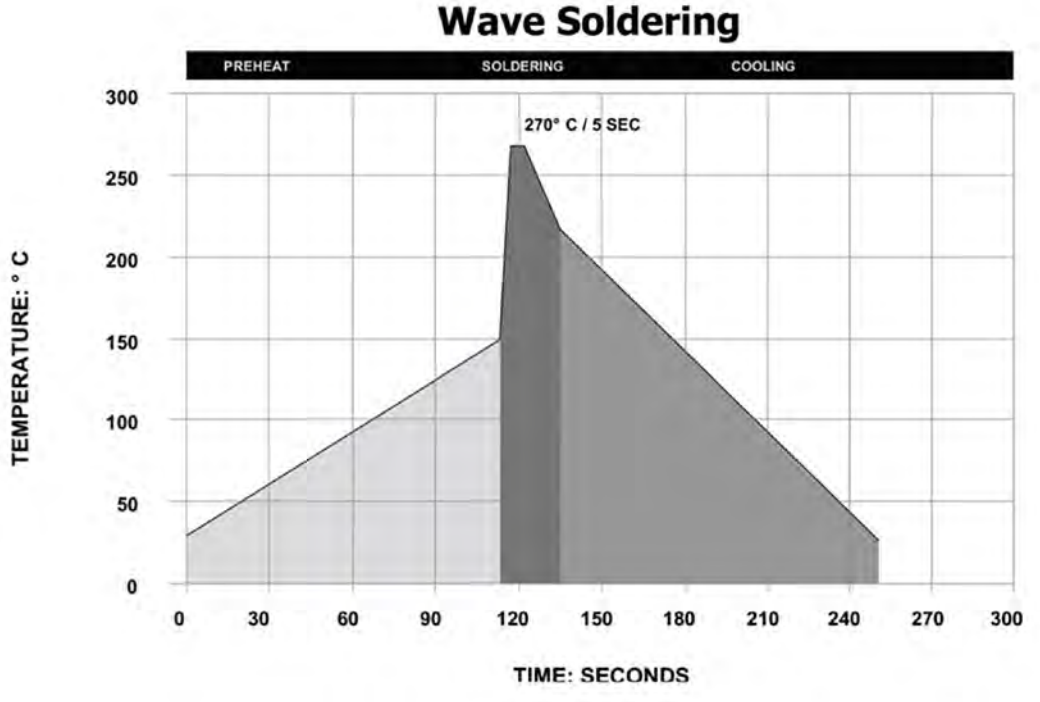


Figure 7: Wave soldering profile to deliver the correct amount of thermal energy.

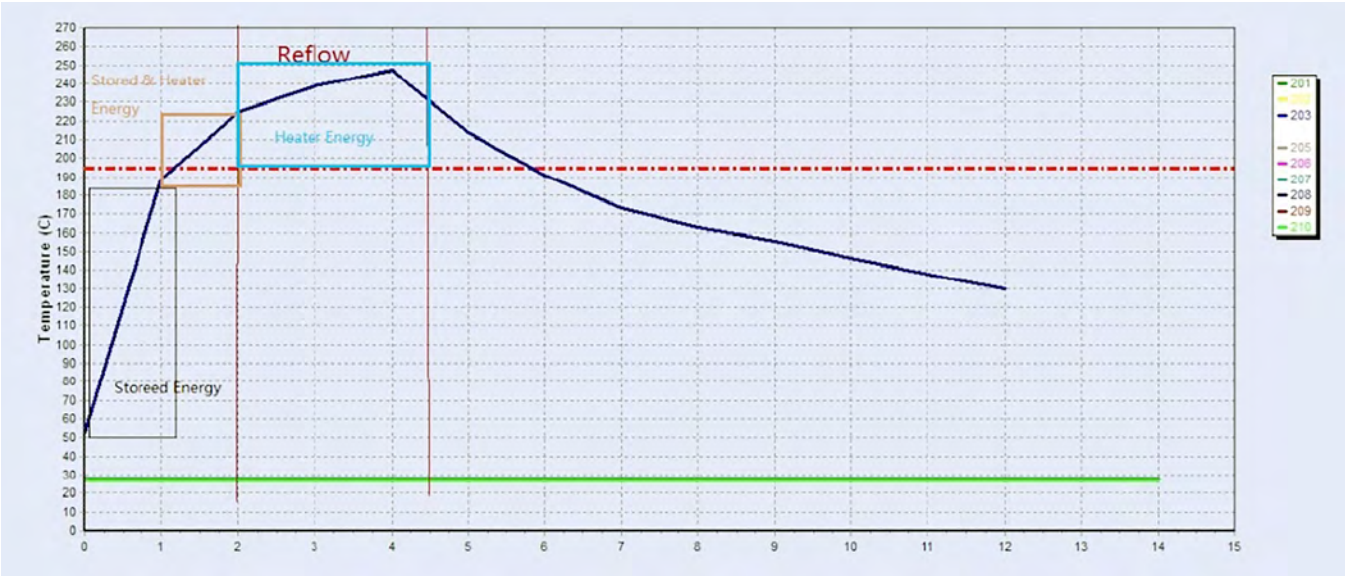


Figure 8: Hand soldering profile showing energy phases and transitions.

2. Thermal energy—which passes through the tip, pad, and joint—activates the flux and depletes the oxidization from the pad and joint (thermal energy at this phase is a mixture of stored and heater energy)
3. Any loss in thermal energy due to the joint is compensated by the heater energy that provides the reflow necessary to form a reliable solder joint. The ideal joint temperature should be solder melt temperature plus 40°C to form a good intermetallic bond. In this phase, it is critical that the heater provides the correct level of response and does not overshoot
4. The final phase is the cool-down period, which takes place 2–5 seconds after the joint is formed

It should also be noted that while tip idle temperature is often referred to as a measure of potential solder joint reliability, it can only indicate that the tip temperature is in range (e.g., ± 5°C). It does not indicate what happens upon contact with the load (joint). Basically, it is only there as a part of the standard, and the absence of proper joint testing is a simple method of checking tip temperature. So, what is the best way to achieve a reliable solder joint?

Other Thermal Energy Factors

The achievement of reliable solder joints does not just depend on the tip idle temperature but requires consideration of other thermal energy factors:

1. Tip mass (energy is stored in mass)
2. Heater power and control
3. Tip-to-pad contact area
4. Thermal energy bridge (heater → copper tip → joint)
5. Tip geometry
6. Plating thickness on the tip
7. Tip idle temperature
8. Operator skill

To overcome the potential problems associated with conventional heater technology (Figure 9) and to ensure a more reliable solder connection, it is recommended that soldering systems with the Curie Heat Technology (CHT) principle be used wherever possible.*

The use of CHT ensures (Figure 10):

- Tip-to-ground resistance is maintained
- Tip-to-ground voltage leakage will not occur
- Thermal transfer will be efficient
- No calibration is necessary
- No overshoot of temperature

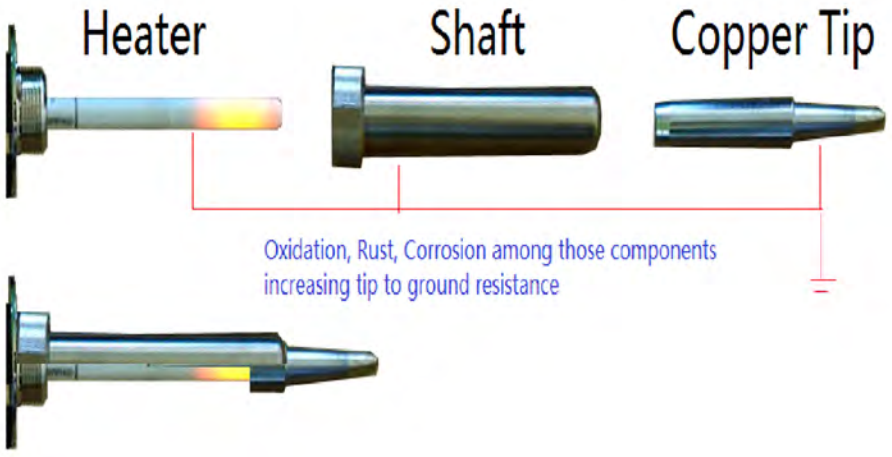


Figure 9: Conventional solder tip heater technology.

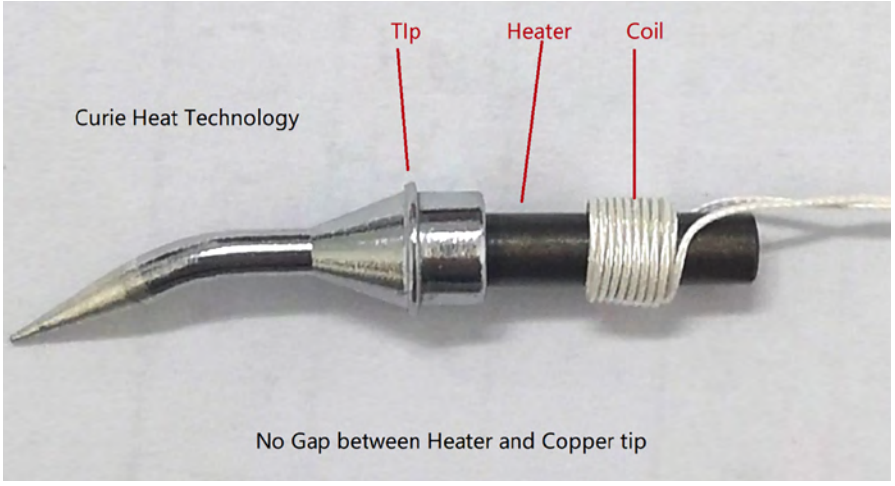


Figure 10: CHT tip/cartridge.

Conclusion

Overall, there are several factors that ensure a reliable solder joint:

- The selection of the correct tip profile for the tip-to-pad contact area
- A power supply system that can provide enough thermal energy to meet the temperature requirements with no overshoot
- The ability of the heater/tip to form an efficient energy bridge within a defined time frame
- Good-quality solder wire
- Operator skill

Above all, it is the skill of the operator that becomes the overriding factor, since even the best tools will not perform well in the hands of unskilled or poorly trained personnel. **SMT007**

References

1. P. Roubaud, G. Ng, G. Henshall, R. Bulwith, R. Herber, S. Prasad, F. Carson, S. Kamath, A. Garcia, "Impact of Intermetallic Growth on the Mechanical Strength of Pb-Free BGA Assemblies," IPC APEX EXPO Technical Proceedings, 2001.

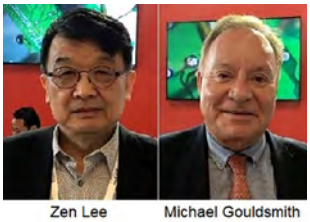
2. T. An, F. Qin, G. Xia, "Analytical Solutions and a Numerical Approach for Diffusion-Induced Stresses in Intermetallic Compound Layers of Solder Joints," *Journal of Electronic Packaging* 136(1), 011001, March 2014.

3. J. Servin, "Method to Measure Intermetallic Layer Thickness and Its Application to Develop a New Equation to Predict Its Growth," IPC APEX EXPO Technical Proceedings, 2013.

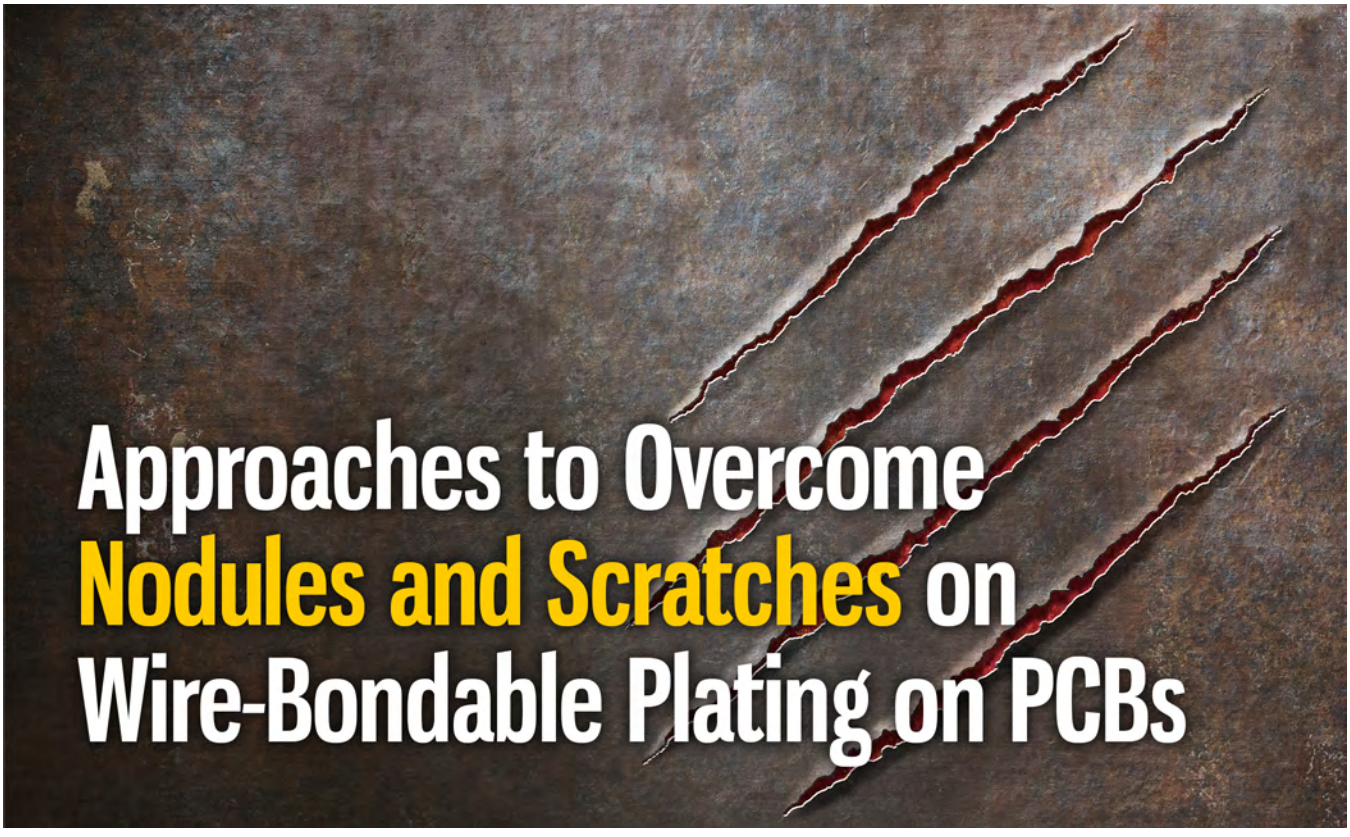
4. D. Hillman, R. Wilcoxon, T. Pearson, P. McKenna, "Dissolution Rate of Specific Elements in SAC305 Solder," SMTA International Technical Proceedings, 2018.

5. Soldering recommendation by Halo Electronics Inc. USA.

**In physics and materials science, the Curie temperature or Curie point is the temperature above which certain materials lose their permanent magnetic properties to be replaced by induced magnetism. The Curie temperature is named after Pierre Curie who showed that magnetism was lost at a critical temperature.*



For more information, contact **Michael Gouldsmith** and **Zen Lee,** co-directors at Thermaltronics USA Inc., Great Neck, New York; www.thermaltronics.com.



Approaches to Overcome Nodules and Scratches on Wire-Bondable Plating on PCBs

Feature by Young K. Song and Vanja Bukva,
TELEDYNE DALSA INC.,
and Ryan Wong,
FTG CIRCUITS

Abstract

Initially adopted internal specifications for acceptance of printed circuit boards (PCBs) used for wire bonding was that there were no nodules or scratches allowed on the wire-bond pads when inspected under 20X magnification. The nodules and scratches were not defined by measurable dimensions and were considered to be unacceptable if there was any sign of a visual blemish on wire-bondable features. Analysis of the yield at a PCB manufacturer monitored monthly for over two years indicated that the target yield could not be achieved, and the main reasons for yield loss were due to nodules and scratches on the wire-bonding pads.

The PCB manufacturer attempted to eliminate nodules and scratches. First, a light-scrubbing step was added after electroless copper plating to remove any co-deposited fine particles that acted as a seed for nodules at the time of copper plating. Then, the electrolytic copper plating tank was emptied, fully cleaned, and filtered to eliminate the possibility of co-deposited particles in the electroplating process. Both actions greatly reduced the density of the nodules but did not fully eliminate them. Even though there was only one nodule on any wire-bonding pad, the board was still considered a reject. To reduce scratches on wire-bonding pads, the PCB manufacturer utilized foam trays after routing the boards so that they did not make direct contact with other boards. This action significantly reduced the scratches on wire-bonding pads, even though some isolated scratches still appeared from time to time, which caused the boards to be rejected. Even with these significant improvements, the target yield remained unachievable.

Another approach was then taken to consider if wire bonding could be successfully performed over nodules and scratches and if there was a dimensional threshold where wire bonding could be successful. A gold ball bonding process called either stand-off-stitch bonding (SSB) or ball-stitch-on-ball bonding (BSOB) was used to determine the effects of nodules and scratches on

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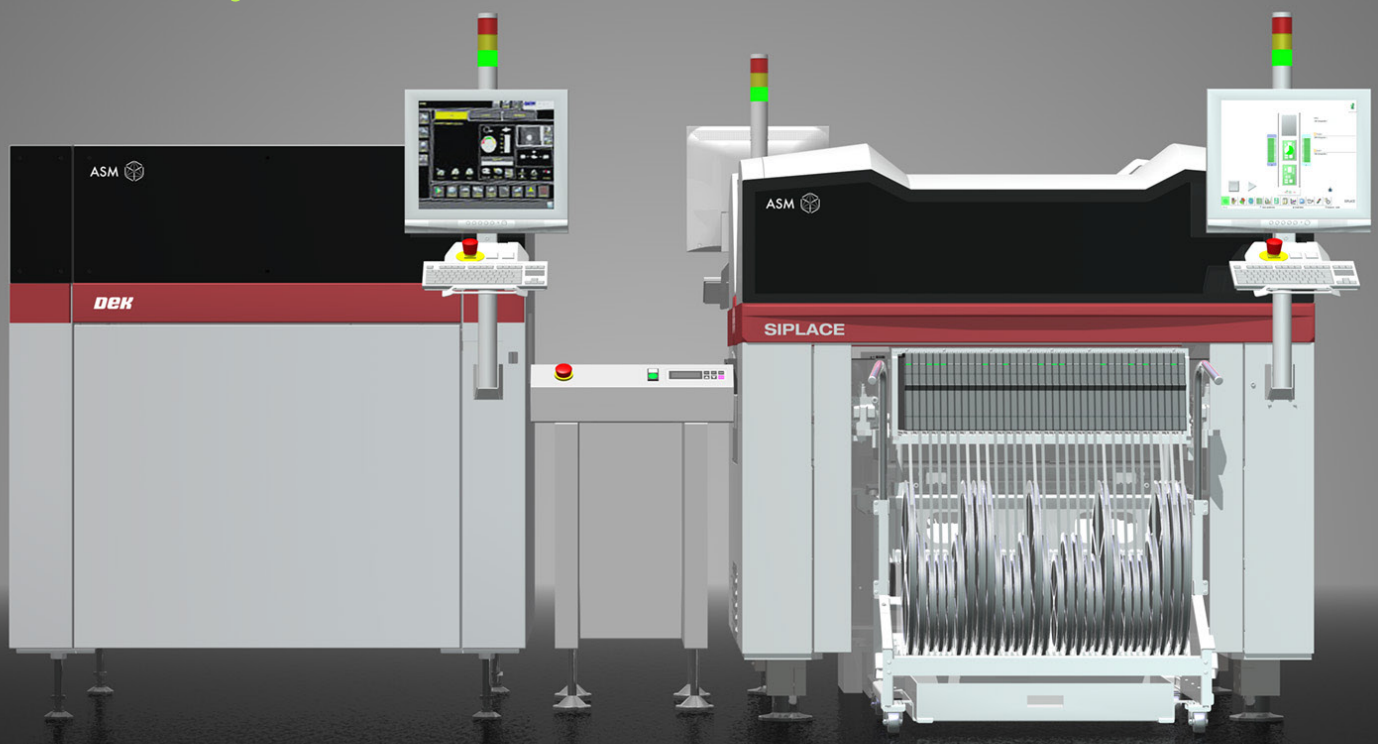

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wire bonds. The dimension of nodules, including height, and the size of scratches, including width, were measured before wire bonding. Wire bonding was then performed directly on various sizes of nodules and scratches on the bonding pad, and the evaluation of wire bonds was conducted using wire pull tests before and after reliability testing. Based on the results of the wire-bonding evaluation, the internal specification for nodules and scratches for wire-bondable PCBs was modified to allow nodules and scratches with a certain height and a width limitation compared to initially adopted internal specifications of no nodules and no scratches. Such an approach resulted in improved yield at the PCB manufacturer.

Introduction

The development of the chip-on-board (COB) type of image sensors has significantly increased in the last few years to accommodate an increasing demand for low-cost, high-performance industrial inspection cameras. Wire bonding is the most commonly used technology for making the electrical interconnection between a silicon image sensor and its substrate during image sensor fabrication. Therefore, wire bonding directly on the PCB surface is inevitable for COB-type image sensor fabrication.

IPC-A-600J section 2.7.1.3—surface plating, wire-bond pads [1]—states, "Wire-bond pads are free of surface nodules, roughness, electrical test witness marks or scratches that exceed 0.8 mm (32 min) RMS (root-mean-square) in the pristine area in accordance with an applicable test method AABUS." Since the tolerance of surface nodules (< 0.8 mm RMS) in IPC-A-600J for wire bonding pads is not easily measurable and may not properly reflect single nodules and shallow scratches, the initially adopted specification for wire bonding pads as a user was defined to be free of surface nodules and scratches. Therefore, a board was considered a reject if a nodule or a scratch was visible in the pristine area of the wire-bond at 20X magnification. If in any doubt, one could use 40X magnification for inspection to clarify pass/fail. However, in reality, it was difficult to achieve a wire-bonding surface in specification without nodules or scratches, resulting in low yield at the PCB manufacturer. In particular, PCB products designed with a center cut-out slot close to bonding pads were prone to significant yield loss due to nodules.

Yield review with the manufacturer and the analysis of causes for rejects using Pareto charts pointed out that two main reasons for PCB rejects were due to nodules and scratches on the wire-bonding surface. Yield had been reviewed on a monthly basis for 28 months, and the major yield losses continued to be due to nodules and scratches on the wire-bonding surface during the period. Figure 1 shows the

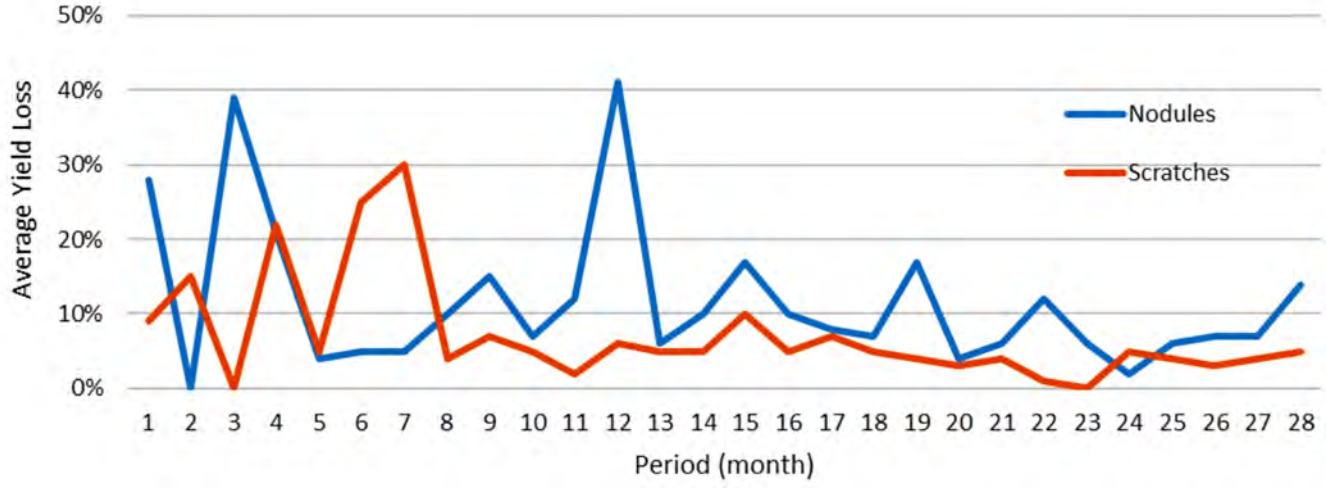

Figure 1: Average yield loss from multiple wire-bonding PCB products.

average yield loss per month for wire-bonding boards due to nodules and scratches. The average yield losses from multiple PCB products due to nodules and scratches for wire bonding boards were in the range of 4–41% and 2–30%, respectively, during the period.

It is worth noting that the data in Figure 1 may not necessarily provide the picture of actual average yield loss due to nodules and scratches. When any defect—either nodule or scratch—was first found during an inspection of a board, the reason for rejection was recorded and further inspection of that board was not pursued since the board was already determined to be a reject. For example, the manufacturer recorded a 39% yield loss for nodules and none for scratches in Period 3. However, it may not mean that there were o scratches on those rejected boards since those boards had not been inspected further for scratches after nodules were first observed.

Figure 2 shows the maximum yield loss for nodules and scratches. The maximum yield loss was recorded from one of the PCB products that showed the lowest yield at the period or in the month. Unacceptable yield loss over the period of many months initiated a discussion with the manufacturer to identify the root cause and conduct corrective actions to improve on nodules and scratches.

Corrective Actions at the Manufacturer

The PCB Manufacturing Process

One of the PCB manufacturers who had experience producing bare boards had considerable data that suggested that nodules and scratches were likely the main reasons for yield loss. The specification initially defined by the user required inspection at a 20X starting magnification, which was beyond the IPC specification of 1.75X magnification. Since there were inspection escapes, the manufacturer decided to start at 40X magnification as a preventative measure. This, combined with the criteria for absolutely no nodules or any surface imperfection, resulted in many rejected boards that may have actually been wire-bondable and reliable. The manufacturer initiated root cause analysis to determine the source of the nodules and scratches to define an action plan to reduce or eliminate the defects.

Nodules

Nodules are surface imperfections on the plated surface that can originate and grow in the copper plating process or originate from processes preceding copper plating (i.e., electroless copper) and grow in the copper plating process. Electroless copper plating is used as a metallization process that deposits a thin layer of copper onto non-conductive surfaces, such

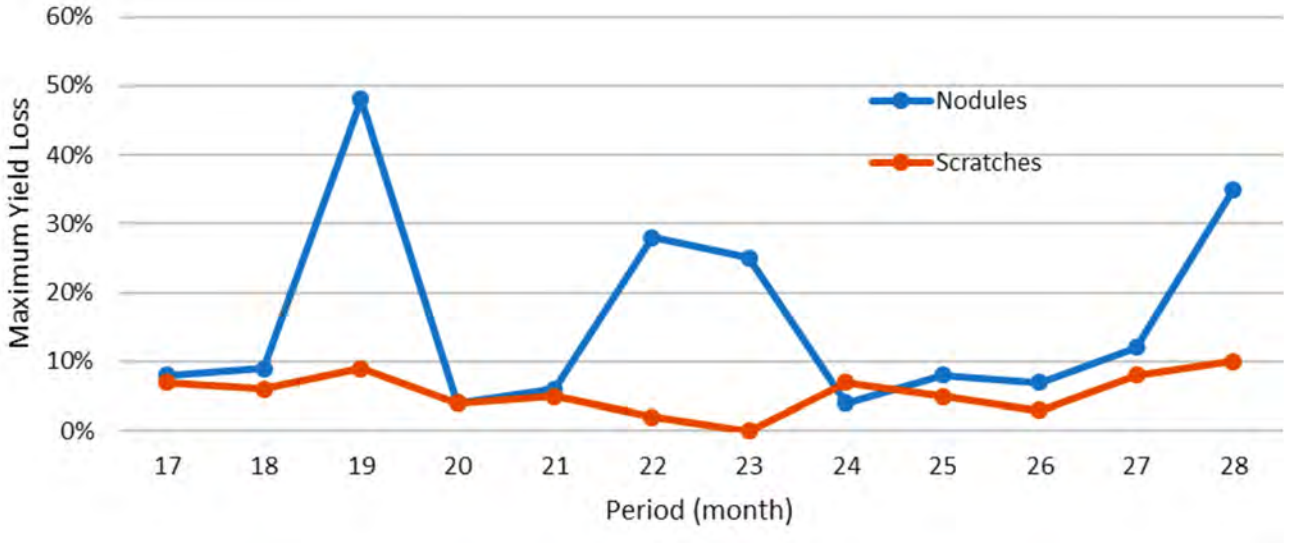

Figure 2: Maximum yield loss from a PCB product with the lowest yield.

as the hole wall of a drilled panel. This creates electrical connectivity through the plated holes. Then, the electrolytic copper plating process uses an electrical current to electrodeposit copper from a copper sulfate solution onto the copper-clad production panel. Electroplating inherently prefers to plate onto protruding features, edges, or corners; therefore, the slightest surface protrusion on the base copper foil or a minor imperfection co-deposited during the electroless copper process will attract more copper plating and grow in size to become a visually detectable nodule after electroplating.

Nodules that were observed optically under 40X magnification were cross-sectioned in an attempt to determine the process at which the nodule began to form. Given the small size of the nodules and knowing that the nodule starts with an even smaller surface imperfection that grows through electroplating, cross-sectioning down to the absolute center of the nodule was difficult to achieve and objective evidence of the nodule's origin could not be found all the time. Figure 3 shows an example of a cross-sectioned nodule. In this case, it seemed to be clear that the nodule was formed before the Ni/Pd/Au plating process, and, therefore, nodule formation would have likely happened during electroless or electrolytic copper plating.

Using a fishbone diagram to define potential root causes of the nodules, a short list of potential root causes was identified: copper foil imperfections, electroless copper co-deposited particles, and electroplated copper co-deposited particles. Each potential root cause was explored in-depth to prove or disprove that it was the source of—or contributed to—the formation of nodules.

Figure 3: Cross-sectioned view of a nodule as an example.

A random sample of copper foil was visually inspected under 100X magnification and no significant signs of imperfections were found. Using a controlled production lot, a light mechanical scrubbing process was performed on the laminated foil through a horizontal conveyorized machine, but the number of boards that were rejected for nodules remained close to the average from previous production lots. Consequently, this potential root cause was eliminated early into the investigation. The same mechanical scrubbing process was performed on panels that had been processed through electroless copper. In this case, the results were noticeable. The density of nodule occurrences was reduced but there were still boards being rejected for single nodules located at wirebond locations. And in some production lots, the frequency of the single nodules was excessive enough to still have a significant impact on yield. However, an overall improvement had been made, and this mechanical scrubbing process became a standard process.

After an extended period of processing boards with the mechanical scrubbing process after electroless copper, an opportunity to test the electrolytic copper plating process arose when an annual preventative maintenance procedure was completed on one of the three plating tanks on the automated plating line. The procedure involves:

- A complete carbon treatment of the copper sulfate based chemistry to remove organic molecules that have leached out from the dry-film photoresist
- Emptying and cleaning all copper anode baskets to remove copper sludge
- Replacing all of the anode bags
- Dummy plating after chemical additions to form a uniform copper oxide film over the anodes

Panels were plated in the new tank and a normal tank, and the number of nodules was significantly reduced on the panels plated in

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the new tank. This test was repeated a couple more times with the same results. As an interim action, all wire-bond technology boards were plated in the new tank, which limited the number of nodules to a consistent value for each lot. Subsequently, the remaining two plating tanks underwent the annual preventative maintenance procedure, and all tanks were able to plate wire-bond boards consistently.

Although the process improvements significantly reduced the number of nodules and made the process more consistent, a percentage of boards were still being rejected at final inspection for small nodules. It was important to understand the impact that these small nodules have on wire bonding—in particular, at which size does a nodule begin to negatively impact the wire-bonding process.

Scratches

Scratches refer to a surface imperfection with any depth or a discernible non-uniform contrasting marking. Scratches can originate over the base copper, over the plated copper, or over the final finish plating.

When scratches are over the base copper, the plated copper is capable of filling in minor scratches to a certain degree, but significant depths will have plated copper conforming to the surface topography. Likewise, the final finish—which, in this case, is typically ENIG or ENEPIG—also conforms to the surface topography. Although there is a depth at the scratch, the conductive feature is fully plated with a solderable and wire-bondable surface finish. This is the same situation when scratches are over the plated copper.

When scratches are over the final finish, the results can vary depending on the magnitude of the scratch. Deep scratches could potentially break through the final finish and expose copper, which would oxidize and would not be solderable or wire-bondable at that location. Surface scratches could expose the nickel, which would also oxidize rapidly and cause solderability and wire-bonding challenges. Light scratches that only abrade the gold, but do not remove the gold entirely, would still function as a normal solderable and wire-bondable feature.

In general, it was found that the majority of boards being rejected for scratches were being scratched after the final finish had been applied. An audit of the process flow of the panels after the final finish was conducted, which discovered that the scratches were occurring after depanelization of the boards in the routing process. After routing, the boards are washed off and stacked in trays in preparation for electrical testing. Boards were making direct contact with each other resulting in light scratches and surface scratches.

Corrective action was taken to produce foam trays with slots for individual boards so that the boards would not make contact with each other after depanelization. After the corrective action was implemented, the number of scratches on the boards was significantly reduced—but there was still a small number of boards being rejected for minor scratches. As was the case with nodules, it was apparent that scratches needed to be characterized to determine their effect on the wire-bonding process.

Internal Corrective Actions

Wire Bonding on Nodules and Scratches

Despite significantly reducing the occurrences of nodules and scratches, they were not completely eliminated. Even if there was only one small nodule or scratch on any wire-bonding pad, the board was still considered a reject, and therefore, the target yield remained unachievable. This was the reason for further investigation on the effect of nodules and scratches on the wire-bonding process.

The type of plating applied to PCBs used for this study was electroless nickel/electroless palladium/immersion gold (ENEPIG) with plating thickness specifications as follows; 3.0–6.0-mm Ni, 0.15–0.3-mm Pd, and 0.03–0.06-mm Au. PCBs rejected due to nodules and scratches were received from the PCB manufacturer. Nodules and scratches on rejected PCBs were inspected under a high magnification optical microscope with image analysis software that was capable of creating 3D images and profiles. The height of the nodules was measured on 3D profile images.

PCB Product	Plating Type	Nodules	Scratches
Product I	ENEPIG	Nodules with type A, B, and C	Shallow scratches
Product II	ENEPIG	Nodules with type A only	No scratches

Table 1: PCBs rejected due to nodules and scratches.

PCBs rejected due to nodules were from two different PCB products (i.e., two different PCB designs with different part numbers, called Product I and Product II hereafter) while PCBs rejected due to scratches were from only one of products—Product I. Product I had three different types of nodules that could be formed by different mechanisms or at different PCB manufacturing process steps based on the appearance of the nodules while Product II had only one type of nodule. Nodules observed from Product I and Product II were arbitrarily divided into three types based on the appearance in this study, and designated as Type A, B, and C. In this study, the effect of nodules on the wire-bonding process was only focused on isolated nodules or small nodules formed along a small mechanical defect so that a wire bond was only interrupted by a single nodule rather than by multiple nodules. The PCB samples rejected by the manufacturer due to nodules and scratches are summarized in Table 1.

The three different types of nodules observed from Product I are shown in Figures 4–6. Type A nodules, as shown in Figure 4, were most commonly observed. Type A nodules are relatively circular in shape when it is viewed from the top and has a grain structure on the nodule surface. The cross-sectioned view in Figure 3 appears to be this type of nodule. The diameter of nodules is mostly in the range of 30–50 mm. The 3D optical microscope image is on the left, and the matching 3D profile view with nodule height is on the right of the figure. Type B nodules, as shown in Figure 5, are not circular (or not symmetrical) in shape, and the surface of the nodule looks very smooth without any grain structure. Type C nodules, as shown in Figure 6, are formed along with any mechanical defect such as a nick. Any protrusions on the surface in the plating steps seems to turn into a nodule. An example of a Type A nodule observed from Product II is shown in Figure 7. Only Type A nodules were observed from Product II.

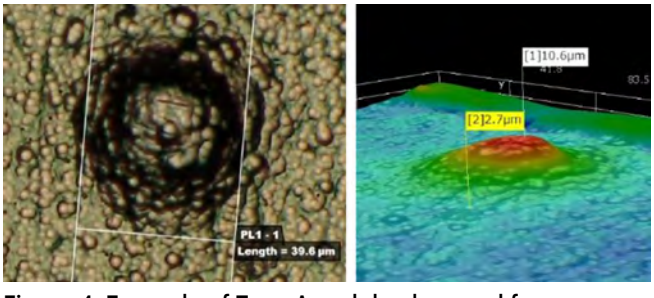

Figure 4: Example of Type A nodule observed from Product I.

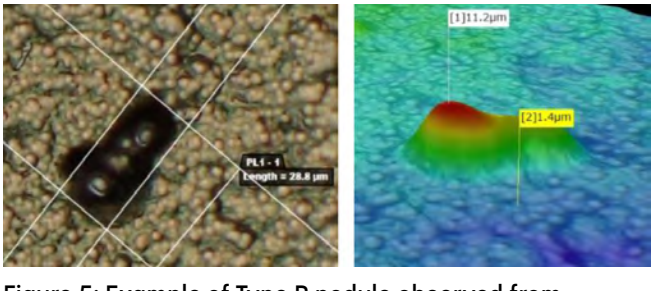

Figure 5: Example of Type B nodule observed from Product I.

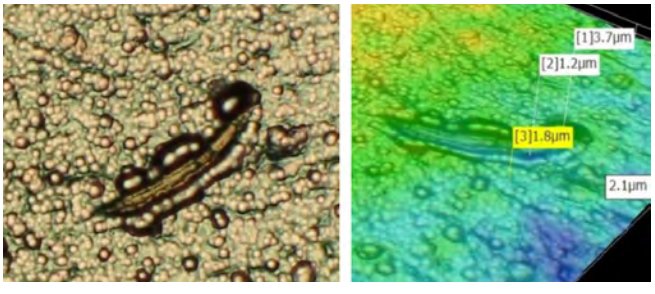

Figure 6: Example of Type C nodule observed from Product I.

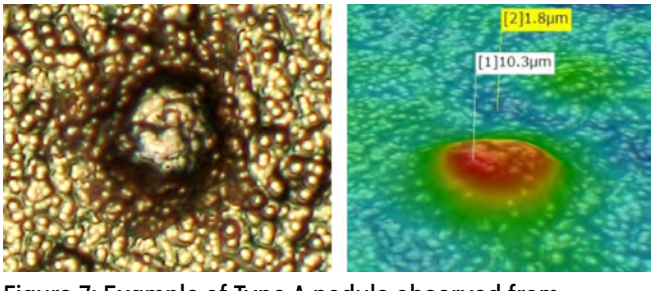

Figure 7: Example of Type A nodule observed from Product II.

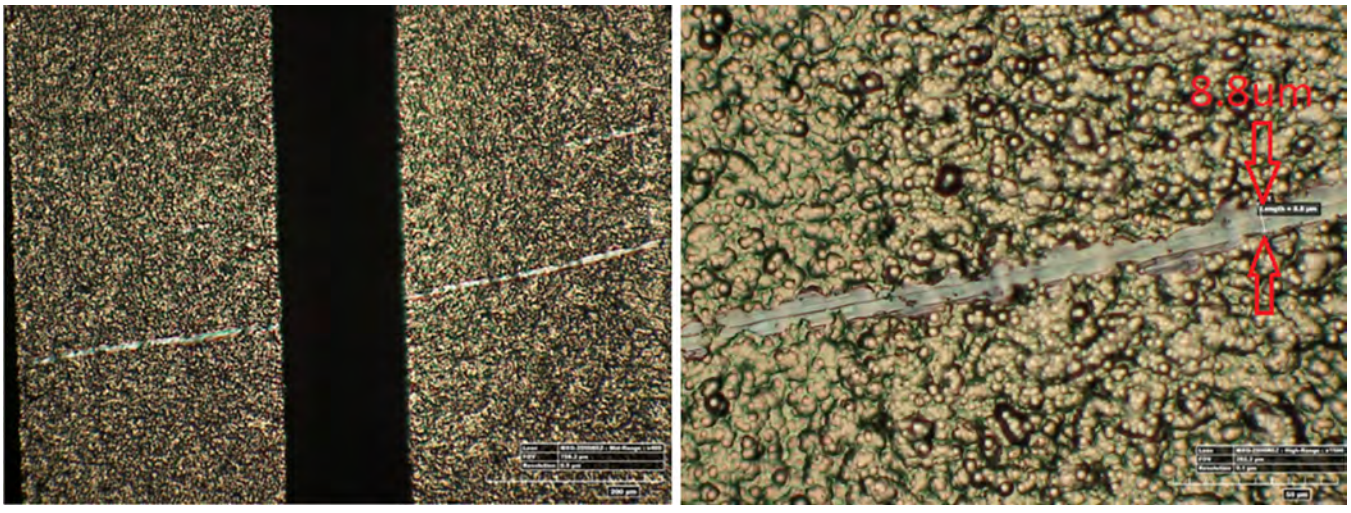

Figure 8: Scratches observed on wire-bonding track on rejected PCBs at low magnification (L) and high magnification on the (R).

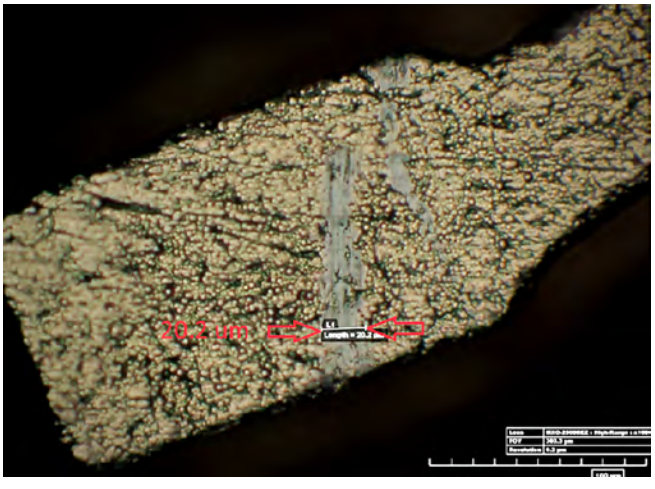

Figure 9: Scratch observed on individually defined wire-bonding pad on rejected PCB.

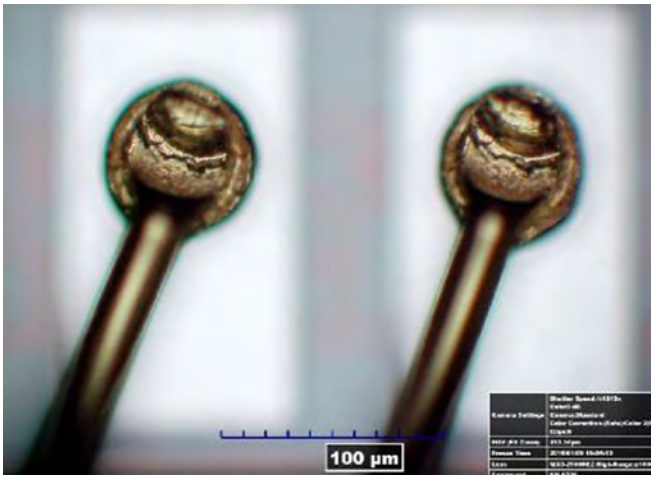

Figure 10: Bonds on die for SSB process.

Figures 8 and 9 show examples of scratches on the wire-bonding surface on rejected PCBs of Product I from the manufacturer. Those scratches seem to be made after the final surface finish step since the gold layer looks damaged due to the scratch. The widths of the scratches were about 9 mm and 20 mm (Figures 8 and 9).

The wire-bonding process used in this study is a specialized gold ball bonding process called either stand-off-stitch bonding (SSB) or ball-stitch-on-ball (BSOB) in the industry. The diameter of the bonding wire used was 25 mm. Figures 10 and 11 show an example of the SSB process in which ball bonds (or bump bonds)

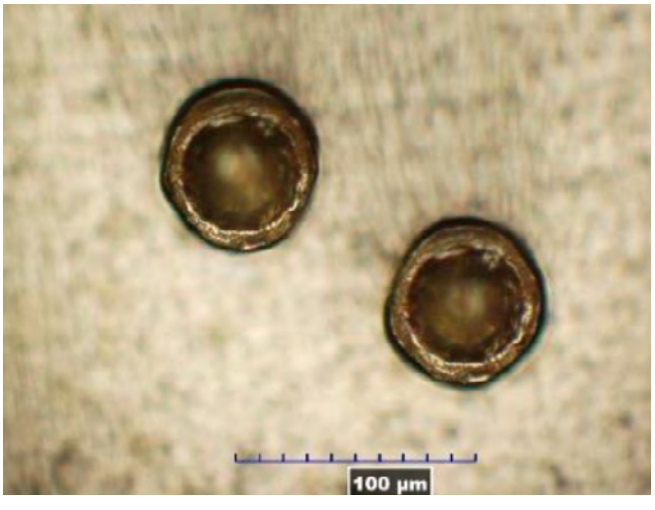

Figure 11: Bonds on PCB for SSB process.

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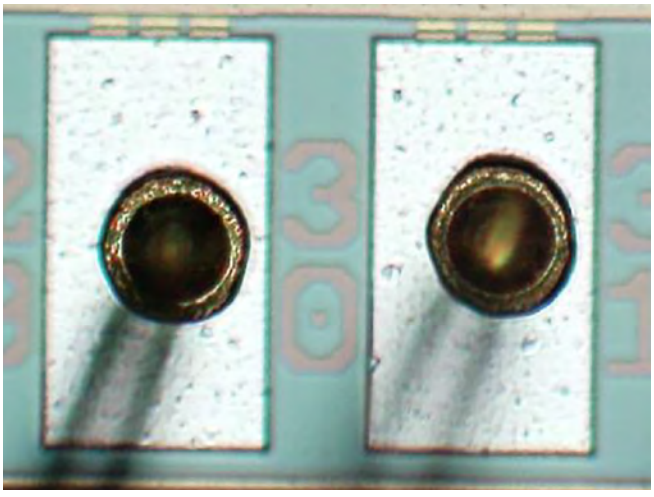

Figure 12: Bonds on die for standard ball bonding process.

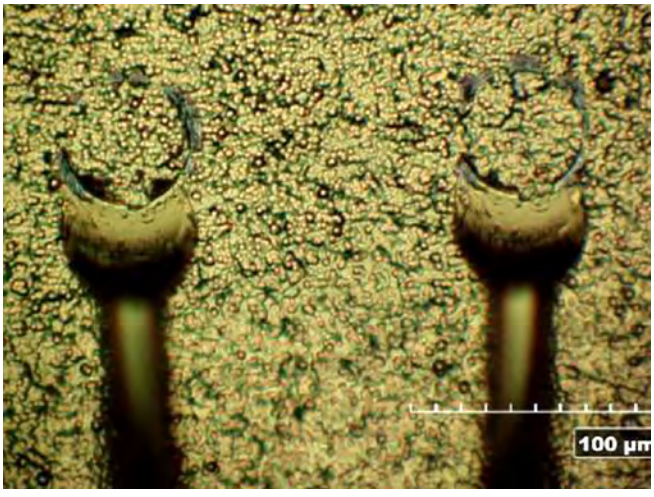

Figure 13: Bonds on PCB for standard ball bonding process.

are made on PCB bonding pads as well as on the die bonding pads—unlike the standard gold ball bonding process shown in Figures 12 and 13 [2]. For the standard gold ball bonding process, ball bonds are expected on die bonding pads, and stitch bonds are expected on PCB bonding pads. For the standard gold ball bonding process, the wire-bonding tool is directly in contact with PCB bonding pads during the stitch bonding process. One can see the circular tool mark on the bonding pad in Figure 13. For the SSB process, the bonding tool is not directly in contact with PCB bonding pads but sits on top of ball bonds on PCB bonding pads.

The height (or thickness) and the diameter of ball bonds made using the SSB process on PCB bonding pads are around 13 mm and 63 mm for Product I, and 15 mm and 62 mm for Product II. The dimension of ball bonds on PCB bonding pads would be considered a critical factor for a wire-bonding experiment on nodules and scratches. The height of ball bonds directly indicates the height of the bonding tool from the bonding pad at the time of wire bonding since the bonding tool sits on the ball bond. In theory, ball bonds might not be squashed as much as programmed if the wire-bonding tool touches a tall nodule before the ball bond is squashed as much as programmed. Therefore, it is likely that the acceptable nodule height might be related to the height of the bonding tool from the bonding surface at the time of wire bonding. In addition, ball bonding on an uneven surface due to nodules would be a factor for the integrity of wire bonds, and the height (or thickness) of ball bonds would be the amount of buffer that can conform with the shape of the nodules. In this aspect, the SSB process compared to the standard ball bonding process would be much more beneficial on wire bonding on nodules. The diameter of ball bonds is also directly related to the wire-bond contact area on PCB bonding pads. Therefore, when wire bonds are made on surface imperfections such as nodules and scratches, the percentage of the wire-bond area made intact on the bonding pad without any surface imperfections is determined by the ball bond diameter (i.e., area).

The integrity of wire bonds was measured by wire pull tests before and after reliability testing. Wire bonds were made directly on nodules and scratches even though the alignment of wire bonds on nodules and scratches varied slightly so that some bonds were aligned slightly better than the others. There were only a couple of PCBs rejected by the manufacturer due to scratches, and therefore, there were not enough scratches with varying widths to make wire bonds to determine the maximum allowable scratch width. For this reason, scratches with various widths were artificially created on PCB bonding pads by using a sharp knife blade for PCB Product I. However, the depth of artificially created scratches, as well as that

of scratches on rejected PCBs by the manufacturer, could not be controlled.

Most artificially created scratches were intentionally made deeper and wider than those on PCBs rejected by the manufacturer, as was shown in Figures 8 and 9. The integrity and reliability of wire bonds made on artificially-created scratches were considered a worst-case condition compared to those made on relatively shallow scratches on PCBs rejected by the manufacturer. Figures 14 and 15 show examples of scanning electron microscope (SEM) images of scratches with elemental analysis using energy dispersive spectroscopy (EDS).

Figure 14 shows an example of scratches on a PCB rejected by the manufacturer during the PCB manufacturing process, and Figure 15 shows an example of scratches created intentionally for this study. The amount of gold detected on the surface of the scratched area is significantly reduced compared to that on the surface without scratches, particularly for Figure 15. Meanwhile, the amount of palladium and nickel detected on the scratched area was significantly increased since palladium and nickel were exposed to the surface. Nickel was detected significantly in some isolated areas indicated as Area 3 in Figures 14 and 15.

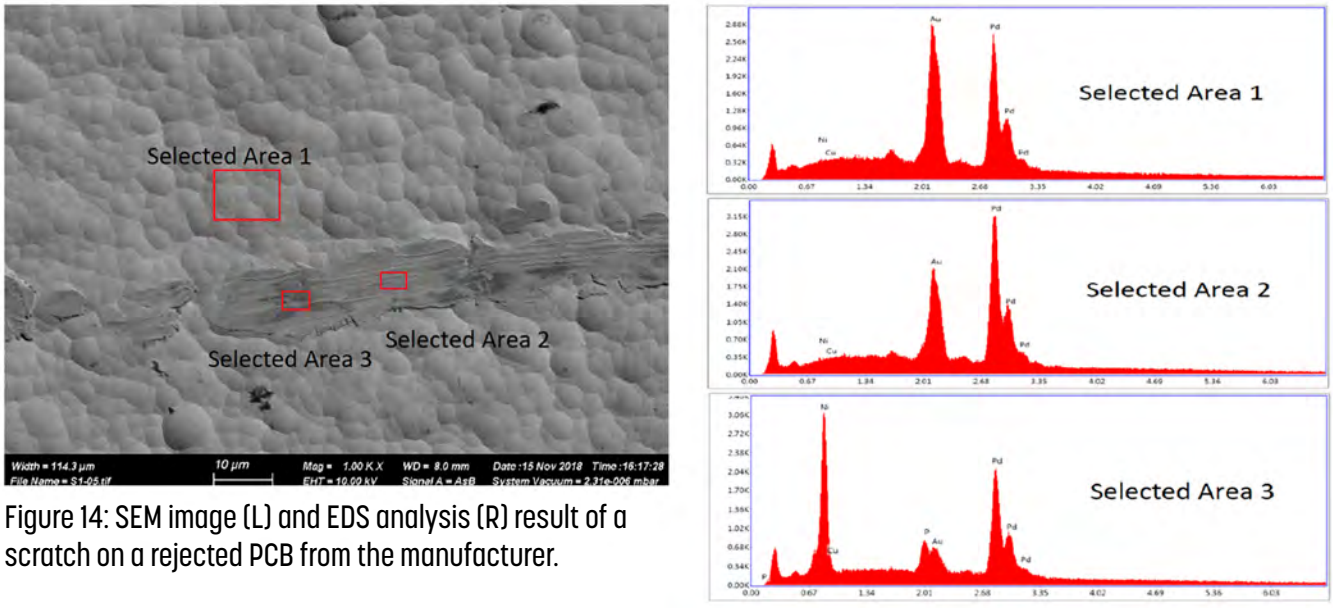

Figure 14: SEM image (L) and EDS analysis (R) result of a scratch on a rejected PCB from the manufacturer.

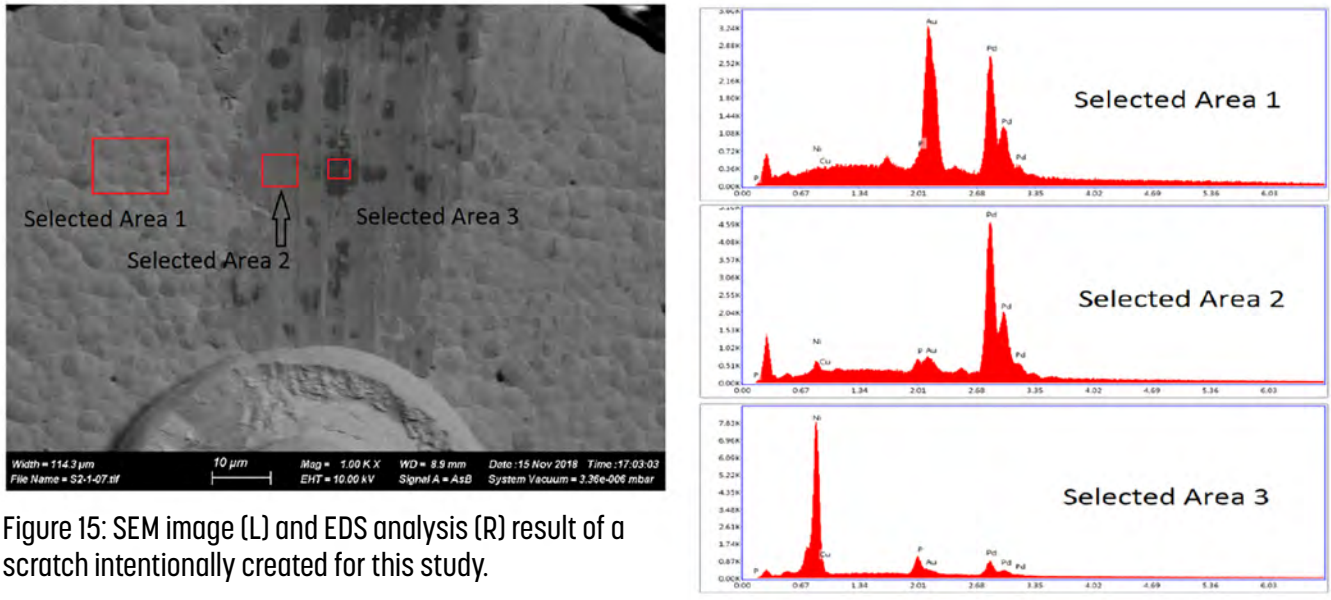

Figure 15: SEM image (L) and EDS analysis (R) result of a scratch intentionally created for this study.

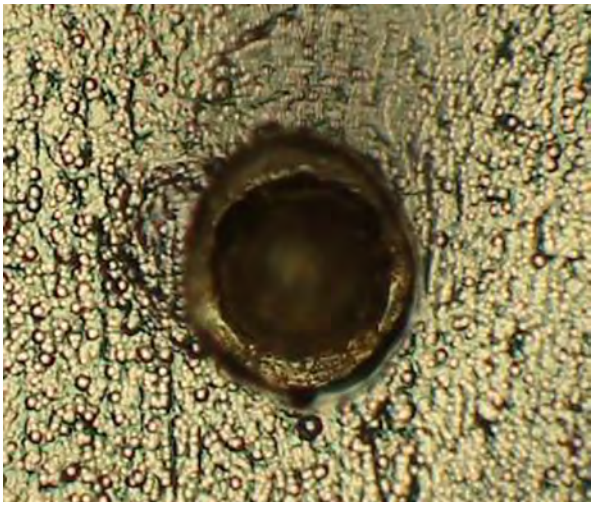

Figure 16: Wire bond made on nodule.

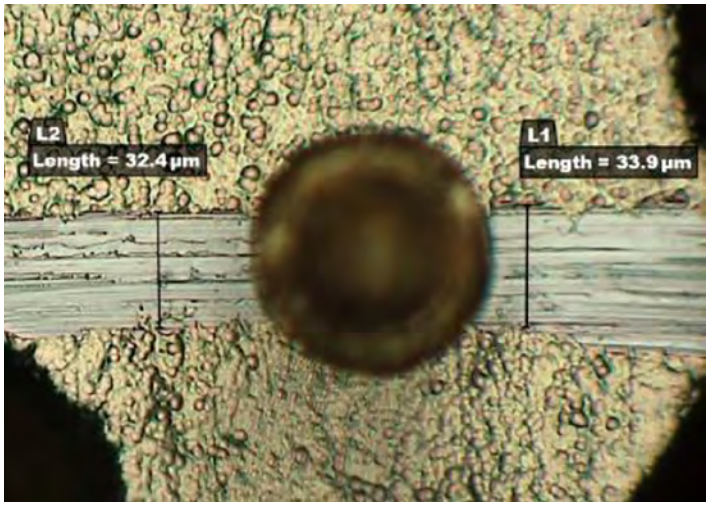

Figure 17: Wire bond made on scratch.

There was not a way to create nodules artificially; therefore, only PCBs rejected by the manufacturer due to nodules were used. Figures 16 and 17 show examples of wire bonds made on nodules and scratches, respectively. Most nodules were almost completely covered with wire bonds so that it was not clear if nodules were under the wire bonds.

Results and Discussion of Wire-bonding Experiment

Pull test results of wire bonds made on nodules before reliability testing are shown in Table 2. These test results are from Product I. All of the wire bonds pull-tested before reliability testing showed a neck break failure mode with acceptable wire pull strength (greater than 4.0 g). A neck break failure mode means that the wire bond was broken above the ball bond on the PCB bonding pad. Variation in neck break strength in Table 2 was due to the difference in wire-bond length and loop height. An unacceptable failure mode would be lifted wire bonds on the PCB bonding pads instead of broken wire bonds during wire pull testing.

Table 3 shows pull test results of wire bonds made on scratches before reliability testing. Wire bonds were made on scratches on PCBs rejected by the manufacturer. Pull test results showed a neck break failure mode with acceptable pull strength.

PCB Product	Nodule #	Type of Nodule	Nodule Height (µm)	Nodule Diameter (µm)	Pull Test Failure Mode	Pull Strength (g)
Product I	N1	A	10.1	49	Neck break	>4.0*
	N2	A	11.5	38	Neck break	>4.0*
	N3	A	13.1	54	Neck break	>4.0*
	N4	A	13.0	45	Neck break	9.7
	N5	B	16.2	31	Neck break	6.2
	N6	A	12.6	47	Neck break	6.1

**Pull strength was not recorded, but it was higher than the internal pull strength specification of a minimum of 4.0 g.*

Table 2: Pull test results of wire bonds made on nodules before reliability tests.

PCB Product	Scratch #	Scratch Width (μm)	Pull Test Failure Mode	Pull Strength (g)
Product I	S1	9	Neck break	9.4
	S2	9	Neck break	5.9
	S3	20	Neck break	7.4

Table 3: Pull test results of wire bonds made on scratches before reliability tests.

Reliability tests conducted for this study were temperature and humidity testing at 85°C/85% RH for 300 hours, and thermal cycling test for 300 cycles in the temperature range of -40–85°C. Tables 4 and 5 show the pull test results of wire bonds made on nodules after temperature and humidity testing and thermal cycling test, respectively. Note that wire bonds made in this study were using the SSB process. Test results in this study would likely be different if a standard gold bonding process or aluminum wedge bonding process had been used.

PCB Product	Nodule #	Type of Nodule	Nodule Height (μm)	Nodule Diameter (μm)	Pull Test Failure Mode	Pull Strength (g)
Product I	N7	A	8.3	50	Neck break	6.8
	N8	B	9.8	29x13	Neck break	6.9
	N9	A	8.7	35	Neck break	7.4
	N10	C	2.5	56x21*	Neck break	5.7
Product II	N1	A	7.8	31	Neck break	8.2
	N2	A	7.5	27	Neck break	10.6
	N3	A	8.0	28	Neck break	8.1
	N4	A	7.3	30	Neck break	8.6
	N5	A	6.5	24	Neck break	7.5
	N6	A	5.8	27	Neck break	7.1
	N7	A	6.4	29	Neck break	10.5
	N8	A	6.9	31	Neck break	6.4

**Including the size of the nick.*

Table 4: Pull test results of wire bonds made on nodules after temperature/humidity test.

PCB Product	Nodule #	Type of Nodule	Nodule Height (μm)	Nodule Diameter (μm)	Pull Test Failure Mode	Pull Strength (g)
Product I	N11	A	7.9	44	Neck break	7.6
	N12	A	7.5	54	Stitch break	11.3
	N13	A	6.5	31	Neck break	7.5
	N14	A	4.6	35	Neck break	7.2
	N15	C	3.3	27	Neck break	8.0
Product II	N9	A	8.9	28x45	Stitch break	NA*
	N10	A	8.5	25	Neck break	NA*
	N11	A	8.7	25	Stitch break	NA*
	N12	A	7.9	32	Neck break	NA*
	N13	A	7.7	33	Neck break	NA*
	N14	A	5.6	28	Neck break	NA*

**All of the wire bonds were broken at either the neck or stitch during the removal of the frame, which is part of the product design to create a cavity to protect wire bonds and image sensors. Therefore, wire pull tests could not be performed. However, all the wire bonds were observed broken rather than lifted.*

Table 5: Pull test results of wire bonds made on nodules after thermal cycling test.

PCB Product	Scratch Width (µm)	Number of Bonds Pulled	Pull Test Failure Mode	Pull Strength (g)
Product I	19-20	1	All neck break (0 lifted bond)	Avg. 7.3 Min. 5.8 Max. 9.0 STDEV 1.1
	20-25	4		
	25-30	5		
	30-31	2		

Table 6: Pull Test results of wire bonds made on scratches after temperature/humidity test.

PCB Product	Scratch Width (µm)	Number of Bonds Pulled	Pull Test Failure Mode	Pull Strength (g)
Product I	17-20	4	All neck break (0 lifted bond)	Avg. 8.0 Min. 5.7 Max. 9.4 STDEV 1.0
	20-25	6		
	25-30	6		
	30-33	2		

Table 7: Pull test results of wire bonds made on scratches after thermal cycling test.

Tables 6 and 7 show the pull test results of wire bonds made on scratches after reliability testing. The information about the width of the scratches is also included in the tables. The range of observed scratch widths in Tables 6 and 7 was from 17–33 mm. The widest scratch is slightly more than half of the diameter of the wire bond; however, wire pull tests after reliability testing did not show failures. In MIL-STD-883H METHOD 2010.12 [3], wire bonds made outside of the bonding pads are considered acceptable if >75% of the wire bond is within the bonding pad, which means that a maximum of 25% of the wire bond could be on a non-bondable surface. However, the area occupied by the scratch under the wire bond in this study is much more than 25%. By rough calculation, a scratch with 12.3-mm width would take about 25% of wire-bond area of the wire bond with 63-mm diameter if the scratch is aligned about in the middle of the circular wire-bond area. For a scratch with 33-mm width, the scratched area occupied under the wire bond would be about 65% of the total wire-bond area.

One of the reasons that wide scratches could be tolerable for the wire-bonding process in this study could be that scratches did not negatively affect the surface finish wire-bonding capability, as shown by the EDS results in Figures 14 and 15. Even though the gold layer was significantly damaged and removed, the pallidum layer—considered the wire-bondable surface—was not completely removed. In other words, an entire scratched area may not necessarily be a non-bondable surface. This could be considered a benefit of using an ENEPIG finished surface over using an ENIG finished surface for wire bonding.

Yield Analysis After Specification Update

Based on the successfully performed experiments, changes were made to the internal specification. Magnification used for inspection was reduced from 20X to 10X. Additionally, the specification was changed to allow for the presence of isolated nodules and scratches as per the criteria in the following paragraph and Table 8.

When inspected under 10X magnification, individual nodules, such as the most commonly observed Type A and C nodules, and shallow scratches with no exposed nickel or copper in the wire-bond area are considered acceptable. In some cases, process variations during PCB manufacturing, or any nodules formed from random particles that form Type B nodules, may create unusual deviations resulting in exceptional nodules and scratches. In these cases, the following specification referred by Table 8 can be used.

Type of defects	Considerations	Proposed specification
Nodules	Height	Accept ≤15 µm
Scratches	Width and depth where Ni or Cu are exposed	Accept ≤13 µm width regardless of depth

Table 8: Specification for nodules and scratches.

Since this new specification has been applied, the yield loss at the PCB manufacturer due to nodules and scratches has shown a significant decrease over 10 months. Figure 18 shows the average yield loss due to nodules and scratches since

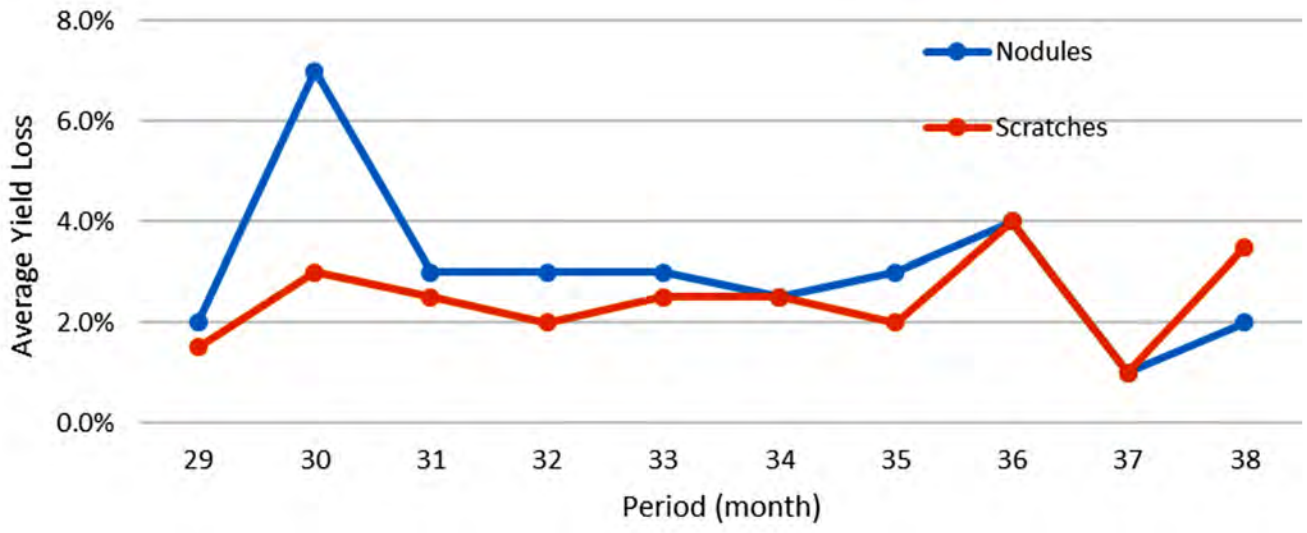

Figure 18: Average yield loss with new specification.

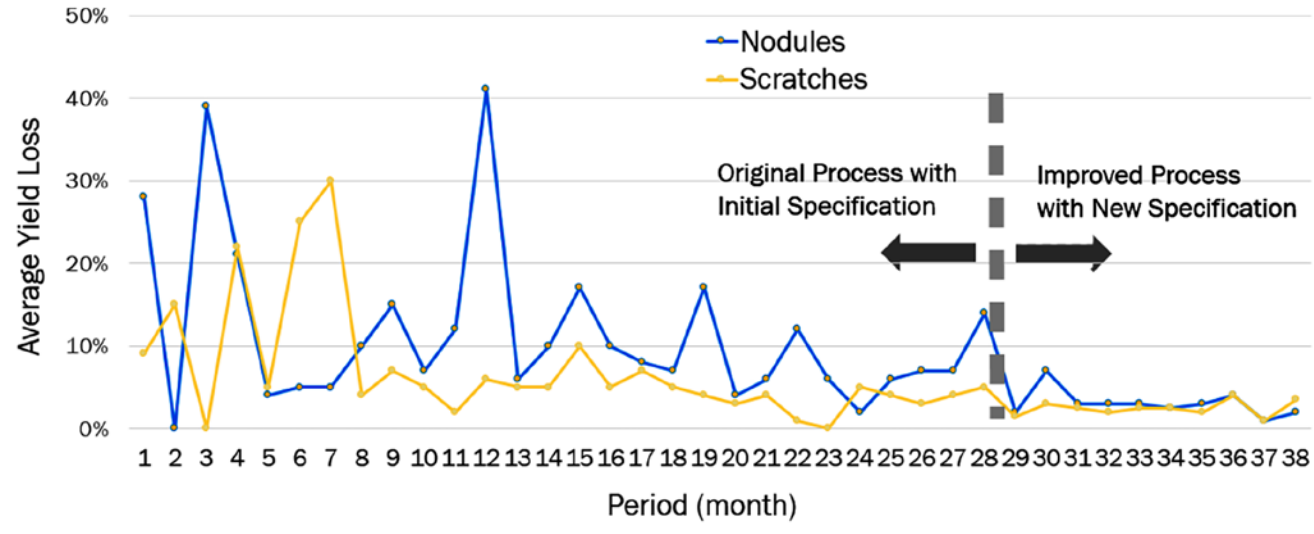

Figure 19: Overview of improvement in average yield loss before and after process improvement and specification modification.

the new specification was applied. Figure 19 shows the overview of the improvement in the average yield loss due to nodules and scratches before and after the process improvement and specification modification.

Summary

To resolve significant yield loss during PCB manufacturing caused by nodules and scratches on wire-bondable features, the PCB manufacturing process was improved to minimize the occurrence of nodules and scratches and wire bonds were evaluated to determine the allowable size of nodules and scratches on bonding pads for the gold wire-bonding process called SSB. Based on the wire-bonding test results, the initially adopted specification—which did not allow for any nodules and scratches on any wire-bondable surface—was changed to accept certain nodules and scratches based on size and the effect on the surface finish. A summary of improvements made to the PCB manufacturing processes, the wire-bonding test results on nodules and scratches using the SSB pro-

cess, and the improved yield after updating the internal specification is as follows:

PCB Manufacturing Process

1. Mechanical scrubbing after electroless copper plating for nodules was initially implemented and slightly improved yields, but later, it was found that the electrolytic copper plating tank cleanliness had a more significant impact on yields
2. The cleanliness of the electrolytic copper plating tanks has been maintained through a preventative maintenance schedule to significantly reduce the occurrence of nodules
3. Foam trays with slots were implemented to transport the boards after profile routing to reduce the number of scratches

Wire Bonding on Nodules and Scratches

1. Type A nodules were the most commonly observed nodules with a height range normally below 10 mm even though the height of two of them were about 13 mm
2. Scratches created intentionally for this study were deeper and wider (as wide as 33 mm) than those inflicted during PCB manufacturing. EDS analysis results showed that the gold layer was mostly removed, but the wire-bondable palladium layer was only partially removed, resulting in the nickel layer only exposed sporadically
3. All of the wire bonds made using the SSB process on nodules and scratches used in this study passed wire-bond pull tests before and after reliability tests of temperature and humidity testing and thermal cycling

Yield Loss Due to Nodules and Scratches

1. The internal specification was updated to address nodules and scratches on wire-bond surfaces based on the improvements made in PCB manufacturing and the results of this study. Nodules under a specific height and scratches with a certain width depending on the depth of the scratches are allowed in the new specification compared to the original specification, which had a zero tolerance for nodules and scratches
2. The average yield loss of multiple PCB products due to nodules or scratches was significantly reduced to a maximum of approximately 7% from a maximum of approximately 41%

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References

1. IPC-A-600, Revision J, "Acceptability of Printed Boards," IPC, 2010.
2. Y. K. Song, V. Bukva, "Challenges on ENEPIG Finished PCBs: Gold Ball Bonding and Pad Metal Lift," IPC APEX EXPO Technical Conference, 2016.
3. MIL-STD-883H, METHOD 2010.12, 2010.

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Smart Manufacturing Roadmap:

Data Flow Considerations for the Electronics Manufacturing Industry

Article by Ranjan Chatterjee and Dan Gamota

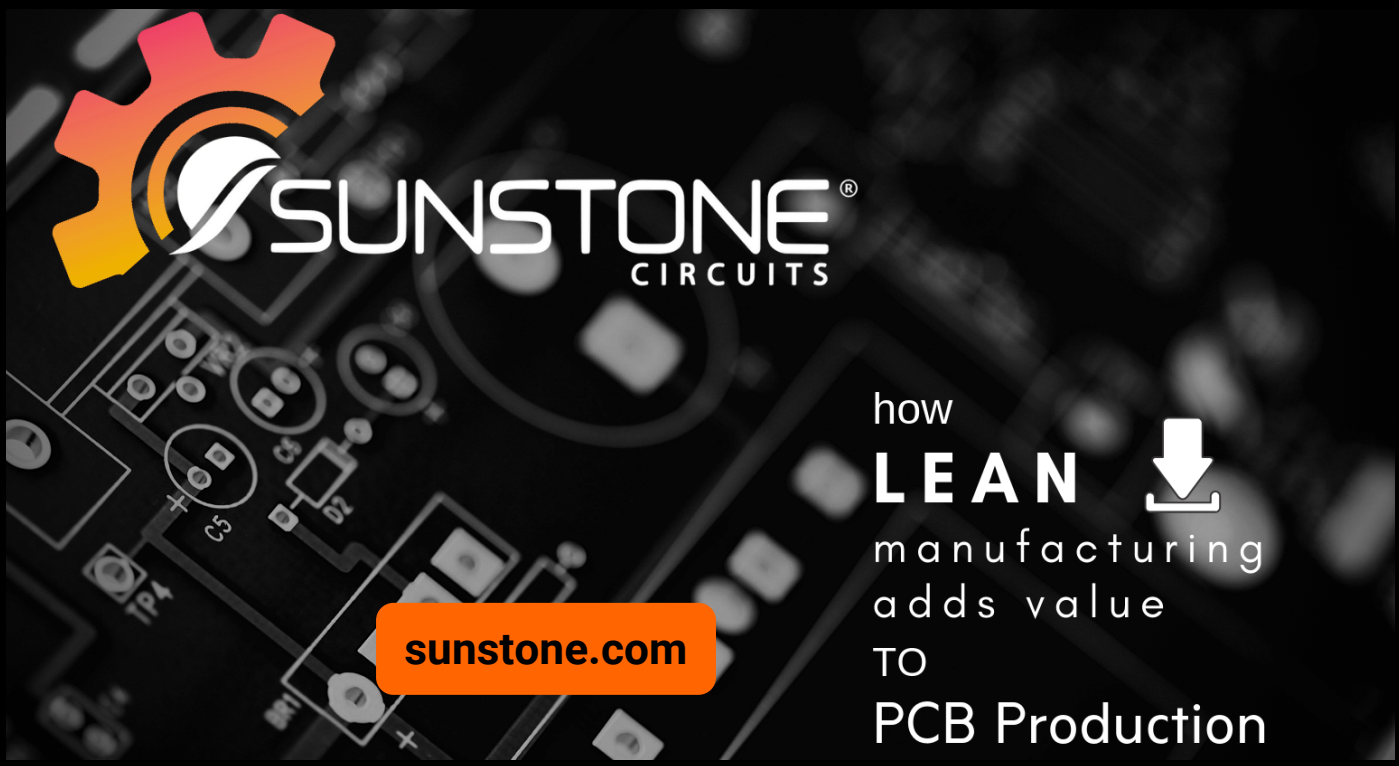
The 2019 iNEMI Roadmap features a new chapter on smart manufacturing. The chapter identifies key technology gaps and needs and offers recommendations to guide the electronics manufacturing industry in realizing the benefits of smart manufacturing. This article is based on information excerpted from the chapter.

The future of the electronics manufacturing industry depends on its ability to develop and deploy suites of technology platforms to realize the benefits of smart manufacturing and Industry 4.0. Smart manufacturing technologies will improve efficiency, safety, and productivity by incorporating more data collection and analysis systems to create a virtual business model covering all aspects from supply chain to manufacturing to customer experience. The increased use of big data analytics and artificial intelligence (AI) enables more efficient collection and analysis of large volumes of data.

Several industry reports predict that manufacturers will realize tens of billions of dollars in gains by 2022 after deploying smart manufacturing solutions. R&D programs around the world are developing technologies that will improve traceability and visualization, enable real-time analytics for predictive process and machine control, and build flexible, modular manufacturing equipment platforms for high-mix, low-volume product assembly.

The vertical segments of the electronics manufacturing industry—semiconductor devices, outsourced semiconductor assembly and test (OSAT), and printed circuit board assembly (PCBA)—are converging, and service offerings are being consolidated, driven by common/shared challenges, such as:

- Responding to rapidly changing, complex business requirements
- Managing increasing factory complexity
- Achieving financial growth targets while margins are declining
- Meeting factory and equipment reliability, capability, productivity, and cost requirements
- Leveraging factory integration technologies across industry segment boundaries
- Meeting the flexibility, extendibility, and scalability needs of a leading-edge factory
- Increasing global restrictions on environmental issues



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As the supply chain continues to evolve and converge, shifts in the traditional flow of materials will drive the need to adopt technologies that seamlessly interconnect all facets of manufacturing operations.

The smart manufacturing chapter of the 2019 iNEMI Roadmap looks at enabling technologies that span industry segments, identifying key gaps and needs that must be addressed, and how these enablers are integrated. The technologies considered most important to build a strong, agile, and scalable foundation are:

- Materials flow and conversion
- Data flow architecture
- Digital building blocks (artificial intelligence, machine learning, digital twin)
- Security

This article focuses on the data flow architecture of smart manufacturing, the foundations of which are:

- Factory information and control systems
- Big data
- Edge, fog, and cloud computing

It highlights the roadmap's integration of these elements across factory operations and facilities, digital building blocks, and security for semiconductor, OSAT, and PCBA manufacturing.

Situation Analysis

General factory operations and manufacturing technologies (i.e., process, test, and inspection) and the supporting hardware and software are evolving quickly while the ability to transmit and store an increasing volume of data for analytics—such as AI, machine learning (ML), and predictive (versus reactive) operations—is accelerating.

The advent, and subsequent growth, of big data is occurring faster than originally anticipated. This trend will continue, highlighting existing challenges and introducing new gaps that were not considered previously. The roadmap identifies several key considerations for data flow. It should be noted that while there are common elements across the three electronics manufacturing vertical segments (semiconductor, OSAT, and PCBA), there are also unique situations specific to each manufacturing environment. In all cases, standardized communication interfaces between the segments are critical.

Semiconductor and OSAT

For semiconductor device manufacturing and back-end assembly and test, accelerating the development of big data technologies will enable the deployment of solutions to realize benefits from increases in data generation, storage, and use. These capabilities, which deliver higher data volumes at real-time and

Figure 1: Connectivity architecture providing smart manufacturing functionality.

near-real-time rates, will increase the availability of equipment parameter data to positively impact yield and quality. There are several challenges and potential solutions associated with these changes, including:

- Connectivity architecture providing smart manufacturing functionality (Figure 1)
- Data flow between manufacturing execution systems (MES)—fog or cloud—and machine interfaces (edge)
- Security of information transmitted between and across the cloud to remote access points
- Standardization/guidelines for data formats between edge devices (e.g., machine-to-machine (M2M) communication)
- Preferred options for real-time monitoring and response time (e.g., M2M versus machine-to-MES, edge to fog)

Printed Circuit Board Assembly (PCBA)

The PCBA segment is in alignment with the semiconductor and OSAT verticals. The primary topics to address are data quality and incorporating subject-matter expertise in analytics to realize effective online manufacturing solutions.

The emergence of big data in electronics manufacturing operations should be discussed in terms of the "5Vs Framework," which is as follows and shown in Figure 2:

1. Volume
2. Velocity
3. Variety (data merging)
4. Veracity (data quality)
5. Value (application of analytics)

The majority of subject-matter experts (semiconductor, OSAT, and PCBA) stress that robust and redundant architectures for data flow must be established to benefit from the 5Vs attributes.

Data volumes in factories are growing at exponential rates. Pervasive data velocities measured as the data collection rates from equipment increased from less than 1 Hz in the

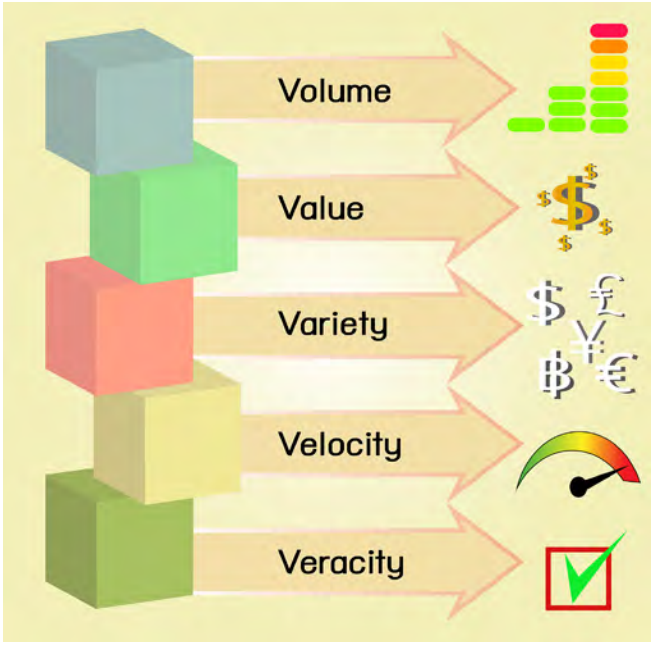


Figure 2: "5Vs Framework" for big data.

1990s to 10 Hz today, and are projected to be at 100 Hz in a few years. Data from equipment, maintenance, yield, inventory management, MES, and enterprise resource planning (ERP) existed for several years; however, analytics tools have evolved to leverage and merge multiple data sources to explore relationships, detect anomalies, and predict events. The 5Vs are foundational to appreciate widespread adoption of big data analytics in the electronics industry. It is critical to address the identified gaps—such as accuracy, completeness, context richness, availability, and archival length—to improve data quality to support advanced analytics for the electronics manufacturing industry [1].

Quantified Key Attribute Needs

The development of a scalable architecture that provides flexibility to expand; connect across the edge, fog, and cloud; and integrate a variety of devices and systems generating data flow streams is critical. Different industries seeking to deploy smart manufacturing technologies should leverage architectures that provide the desired attributes, and data flow architecture is generally considered a prime candidate for leveraging and cross-industry collaboration to identify the optimum solution.

	Semiconductor, OSAT, and PCBA Data Flow Elements			
		Edge	**Fog**	**Cloud**
Factory Operations and Facilities		Sensors	Data synchronizers/analytics	Operational analysis/optimization
Materials Flow & Conversion	*Production equipment*	Sensors, alarms, recipe manipulation; real-time excursion detection solutions	Business rules	Data store/MES
	Material handling systems	Positional & environmental sensors	Dispatching systems & stations; send & receive pull requests from equipment or operators	Lot prioritization & sequencing management for scheduling
Data Flow Architecture	*Factory information & control systems*	Equipment control systems & station controllers	Factory middleware	Back-end systems, such as databases, MES, & scheduling
Digital Building Blocks	*Digital twin, design, manufacturing, & end-product performance*	Impact under consideration	Impact under consideration	Process models for equipment process control & anomaly detection
	Artificial intelligence & machine learning	Execution clients	Data aggregators	Machine learning training solutions
	Augmented & mixed reality	Smart glasses & other assistance devices	Impact under consideration	Data systems connected to augmented reality

Table 1a: Key attribute needs, data flow considerations within and between electronics industry manufacturing segments.

	Within Segments (Semiconductor/OSAT/PCB)	**Between Segments (Semiconductor-OSAT/OSAT-PCBA)**
Security	Edge: Antivirus software, network segregation Fog: Firewalls, intrusion detection Cloud: Security for inter- and intra-company communication	Cloud: Secure communication channels for information exchange

Table 1b: Key attribute needs, security data flow considerations within and between electronics industry manufacturing segments.

Semiconductor

The development and deployment of technologies for data flow are accelerating while data analytics and data retention protocols are increasing at a faster rate than first anticipated. It is critical to collect the crucial data as well as establish guidelines to perform intelligent analysis and exercise the appropriate algorithms to specify data-driven decisions. Several topics related to data are under consideration:

- **General Protocols**

1. "All" versus "anomaly" data retention practices
2. Optimization of data storage volumes
3. Data format guidelines for analytics to drive reactive and predictive technologies
4. Data quality protocols enabling improvements in time synchronization, compression/uncompression, and blending/merging
5. Guidelines to optimize data collecting, transferring, storing, and analyzing

- **Data Considerations for Equipment**

1. Defining context data sets for equipment visibility
2. Improving data accessibility to support functions, such as advanced process control
3. Data-enabled transition from reactive to predictive functionality
4. Data visibility of equipment information (state, health, etc.)

Outsourced Semiconductor Assembly and Test (OSAT)

The key attribute needs for data flow being considered by OSATs include:

- Are the requirements for data flow within the OSAT vertical different from those required between the verticals (semiconductor-to-OSAT or OSAT-to-PCBA)?
- Are security requirements for vertical data flow and horizontal data flow similar or different?
- Are the requirements for data flow between being dependent on edge, fog, and cloud on security requirements?
- Are the data flow needs different for an OSAT managing high product mix that are competitive in nature versus an OSAT managing low product mix?
- What are the criteria to determine the value of the cloud at different levels of data flow architecture maturity/deployment?
- If there is a high level of cloud adoption for the ERP, does this drive adoption at machine-level data flow to the cloud?

Printed Circuit Board Assembly (PCBA)

Subject matter experts agree that access to data will be ubiquitous, cross-platform, and on-demand. Data flow will leverage technologies like augmented reality to help survey production floors for imminent issues, and machine communications will proactively identify and diagnose issues before an instance. The management of the type of data and assurance that the recipients receive the "appropriate" volume of data is critical.

Collaborative Efforts

The smart manufacturing chapter identified several critical gaps that must be addressed to realize the benefits of smart manufacturing and Industry 4.0. Based on the information gathered during the preparation of the chapter, iNEMI is organizing an initial smart manufacturing collaborative project to address back-end electronic packaging commonality. This project plans to address the cost and inefficiency of unique customization requirements across the packaging back-end, seeking to demonstrate the benefits of back-end commonality by defining key cases/examples (e.g., tray carriers) to address both physical and digital (information) commonality. This project plans to analyze and quantify the benefits of improved cycle time, utilization, yield, costs, etc., in a smart manufacturing environment. For additional information, contact info-help@inemi.org.

About iNEMI

The International Electronics Manufacturing Initiative (iNEMI) is a not-for-profit, highly efficient R&D consortium of approximately

90 leading electronics manufacturers, suppliers, associations, government agencies, and universities. iNEMI is hosting a meeting at SEMICON West July 9 from 10:00 a.m. to noon at the Moscone Convention Center (San Francisco). This meeting will highlight iNEMI's Roadmap and include a brainstorming session on potential new projects in the areas of backend commonality (packaging, inspection, test, and more). Brainstorming topics to include advanced packaging, media, tools optimization, data analytics, etc. Confirmed attendees include Intel, AMD, Rudolph, KNS, Cimetrix, Jabil, ASM, SEMI, and others. **SMT007**

References

1. Moyne, J., & Iskandar, J. "Big Data Analytics for Smart Manufacturing: Case Studies in Semiconductor Manufacturing," *Processes Journal,* Vol. 5, No. 3, July 2017.


Chatterjee


Gamota

Ranjan Chatterjee is vice president and general manager, smart factory solutions, for Cimetrix, and **Dan Gamota** is vice president, manufacturing technology and innovation, for Jabil. They are co-chairs of the new smart manufacturing chapter of the 2019 iNEMI Roadmap, which will go on sale this summer.

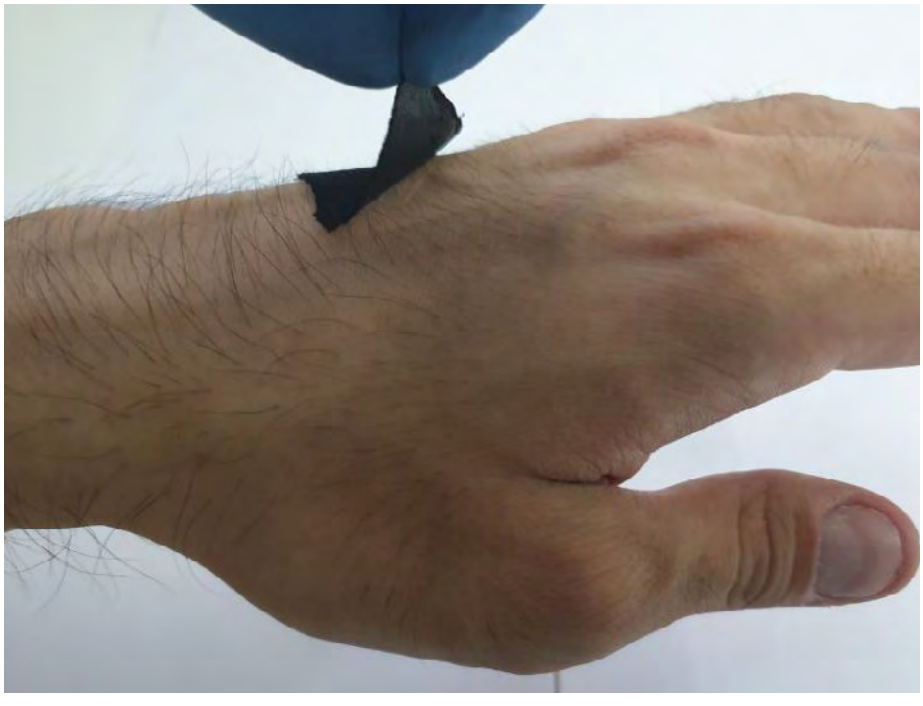
Octopus-inspired Wearable Sensor

Finding the best way to stick wearable electronics to the body has been a challenge. But a team of researchers has developed a graphene-based adhesive biosensor inspired by octopus "suckers."

For a wearable sensor to be truly effective, it must be flexible and adhere fully to both wet and dry skin but still remain comfortable for the user. Thus, the choice of substrate–the material that the sensing compounds rest upon–is crucial. Woven yarn is a popular substrate, but it sometimes doesn't fully contact the skin, especially if that skin is hairy. Typical yarns and threads are also vulnerable to wet environments.

To overcome these challenges, Changhyun Pang, Changsoon Choi, and colleagues worked to develop a low-cost, graphene-based sensor with a yarn-like substrate that uses octopus-like suckers to adhere to the skin.

The researchers coated an elastic polyurethane and polyester fabric with graphene oxide and soaked in L-ascorbic acid to aid in conductivity while still retaining its strength and stretch. From there, they added a coating of a graphene and poly(dimethylsiloxane) (PDMS) film to form a conductive path from the fabric to the skin. Finally, they etched tiny, octopus-like patterns on the film. The sensor could detect a wide range of pressures and motions in both wet and dry environments. The device also could monitor an array of human activities—including electrocardiogram signals, pulse, and speech patterns—demonstrating its potential use in medical applications, the researchers say.



The research is published in *ACS Applied Materials & Interfaces.*

(Source: ACS Applied Materials & Interfaces)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BGA and PCB Warpage: What to Do

Knocking Down the Bone Pile

by Bob Wettermann, BEST INC.

Warpage of BGA packages or PCBs can occur when any heating and subsequent cooling cycle is gone through. This may leave the package to either bow in the middle. Pushing the corners up or downward will show up in bridging (caught on X-ray) or cause opens that would show up on endoscopic or visual inspection. If the PCB warps, then opens or shorts on a variety of other component areas may result.

Reasons for Problems

BGA and PCB warpage is a problem of material coefficient of thermal expansion (CTE) mismatch between the various packaging component materials, such as the substrate, silicon die, and EMC. The rate at which there are temperature increases can affect the temperature uniformity across the component during placement and removal, so this rate is indirectly correlated with warpage differences (Figure 1).

Also, the larger the package, the greater chance of this warping phenomena with all other things being equal. Certainly, the type of rework heating method (hot air rework system, IR, hot air reflow oven, vapor phase oven, etc.) also has an impact. Using low-CTE thermal materials, it is possible to tailor CTE, partially or fully eliminating this problem.

Some plastic bodied ball grid arrays (PBGAs) include a heat spreader, which causes the top of the BGA package to expand at a faster rate than the bottom of the BGA; this can pull the

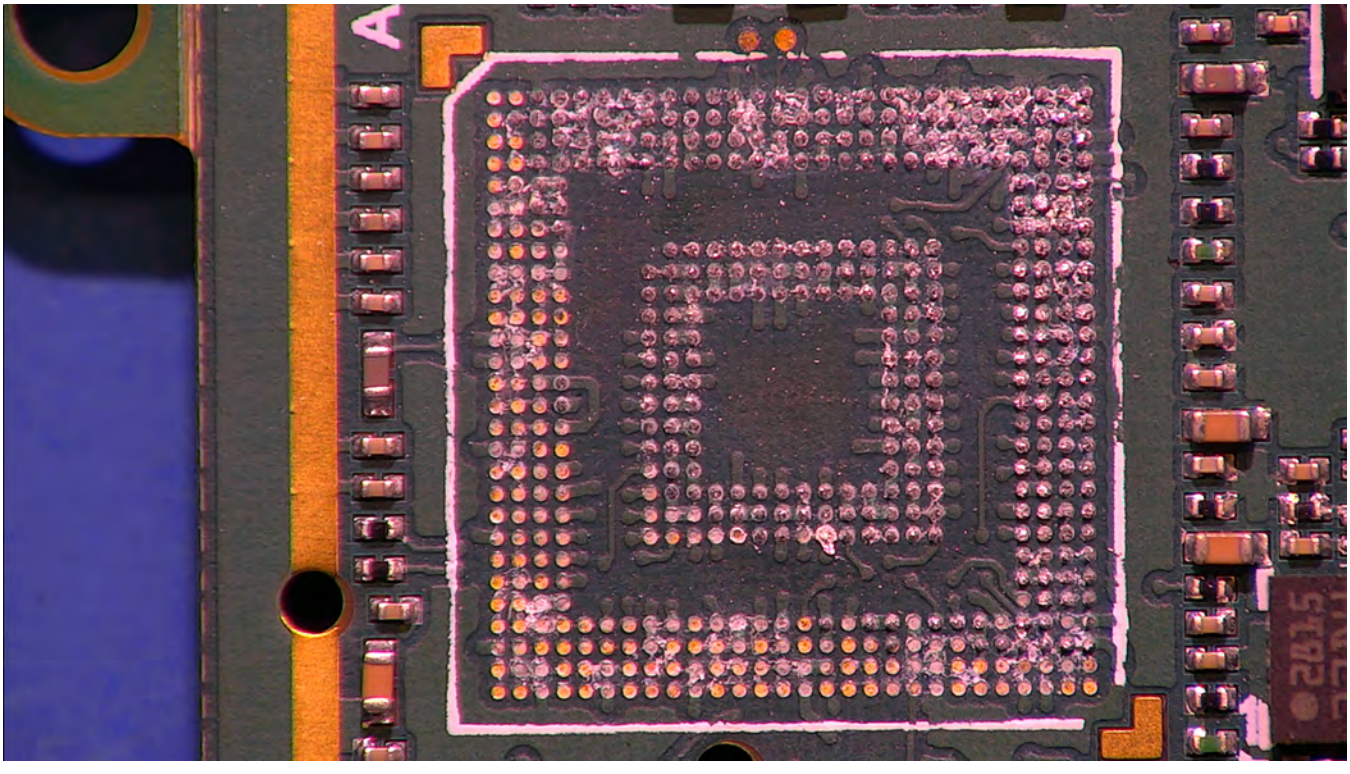

Figure 1: Opens due to BGA warpage.

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corners of the BGA down. Moisture in the BGA may also contribute to warpage as the component wants to spread in the middle. In these cases, the corners may curl upwards.

Through a series of design of experiments, you may want to confirm which part of the equation—the BGA or the PCB—is warping. Isolating which surface is doing the pulling and pushing will be useful in determining how to fix the problem.

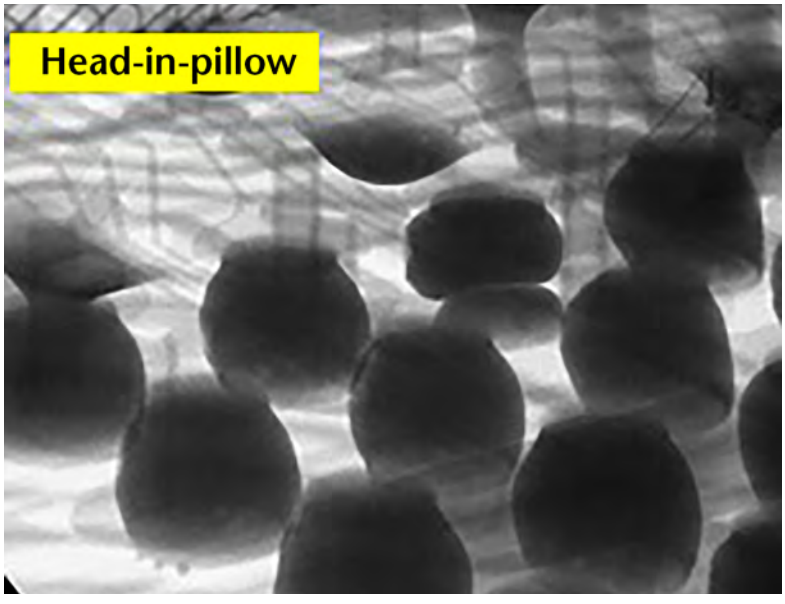


Figure 2: Head-in-pillow defect.

How to Mitigate

For BGA warping, the corners will see the largest displacement, which can cause numerous opens and bridges to occur. Similarly, the circuit board can warp up or down and push into the solder paste, causing bridges or opens. These are caught either in visual or X-ray inspection.

One of the methods to minimize warpage is to slow down your heating and cooling processes. You ramp up during your preheat section and cool down during your cooling section. Now, of course, in cooldown, you don't want to go too slow because you don't want to create a coarse-grained structure. As with many things in electronics manufacturing, it's a trade-off.

Controlling MSD devices—including the boards and components—is another way to help mitigate the impact of warpage. The J-STD-0033 and JEDEC guidelines for moisture handling will be the best place to refer to for proper MSD handling. Prebaking of boards and components followed by keeping them in a dry environment will mitigate the problems if they are associated with moisture absorption. Limiting the exposure time and understanding the MSD level of the board and components will also go a long way to mitigating the warpage associated with moisture absorption.

By using a solder paste that is formulated to reduce head-in-pillow and allows for the proper coalescing of the solder paste, solder ball warpage impacts will be limited as well (Figure 2).

Through properly engineering the volume of solder paste deposited at each pad location, some of the problems related to PCB and device warpage can be limited. In some cases, overprinting some of the pads—while in other

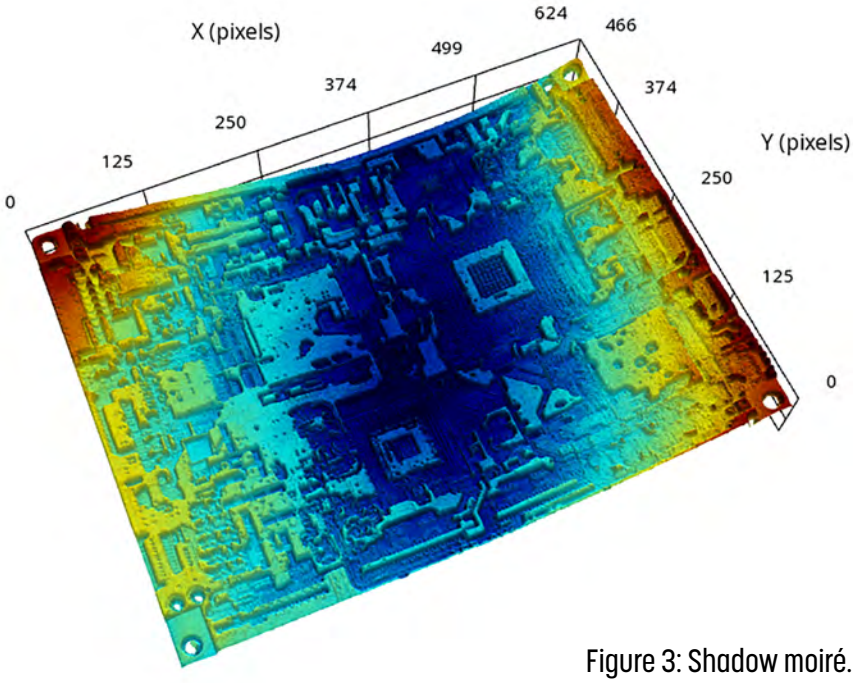


Figure 3: Shadow moiré.

cases, underprinting other pads—may help compensate for the warpage impact. For example, where the BGA is bent inwards toward the PCB, there may be evidence of shorting. In those areas, the print volume may need to be minimized. Conversely, in areas where the BGA bends "away" from the board, a larger print volume may be the best solution.

If the board is warping (IPC-TM-650 2.4.22 test method for measuring bow and twist), then you may need to use other approaches to reduce the impact of device or board warpage (Figure 3). Besides the previously-mentioned approaches, you may need to re-design the board to make sure the copper in the board is more evenly distributed. Low thermal mass (i.e., lower copper content) areas of the board will heat at different rates than higher thermal mass areas. In addition, very thin boards (0.020 inches) may need to laid out using a thicker board. Finally, different materials with closely matched CTEs may need to be used in the board or device construction. **SMT007**

Bob Wettermann is the principal of BEST Inc., a contract rework and repair facility in Chicago. For more information, contact info@solder.net. To read past columns or contact Wettermann, click here.

Scientists Create New Class of Two-dimensional Materials

In a paper published in *Nature,* researchers unveil a new process for producing oxide perovskite crystals in exquisitely flexible, free-standing layers.

A two-dimensional rendition of this substance is intriguing to scientists and engineers because 2D materials have been shown to possess remarkable electronic properties, including high-temperature superconductivity. Such compounds are potential building blocks in multifunctional high-tech devices for energy and quantum computing.

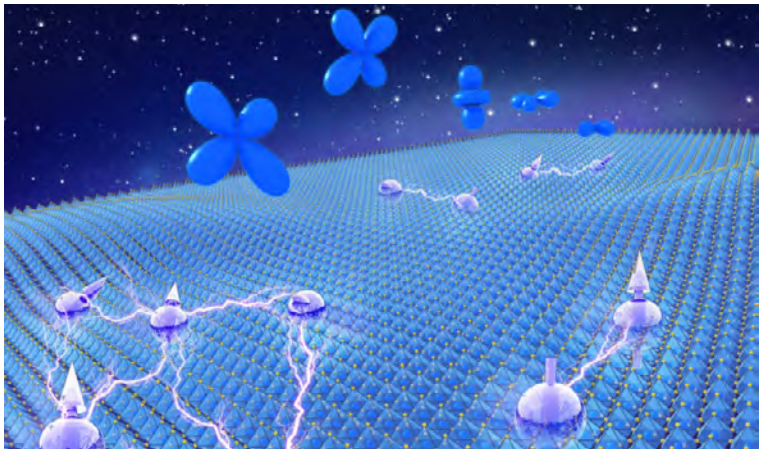
"Through our successful fabrication of ultrathin perovskite oxides down to the monolayer limit, we've created a new class of two-dimensional materials," said co-author Xiaoqing Pan, professor of materials science and engineering and Henry Samueli Endowed Chair in Engineering at the University of California, Irvine (UCI). "Since these crystals have strongly correlated effects, we anticipate they will exhibit qualities similar to graphene that will be foundational to next-generation energy and information technologies."

Pan's cross-disciplinary group of researchers applied a technique called molecular beam epitaxy to grow the thin oxide films layer by layer on a template with a water-dissolvable buffer followed by etching and transfer. His research team was able to review its work at atomic resolution using aberration-corrected transmission electron microscopy (TEM), which allowed the team to directly observe novel phenomena, including the crystal symmetry breaking and unexpected polarization enhancement under the reduced dimension.

"Given the outstanding physical and chemical properties of oxide perovskites and novel phenomena emergent at the monolayer limit, this work opens new possibilities in the exploration of quantum behaviors in strongly correlated two-dimensional materials," Pan said.

Pan and his team were joined by collaborators at China's Nanjing University and the University of Nebraska.

(Source: University of California, Irvine)



Becoming the Preferred Supplier, Phase 2: The Six Pillars

In Search of Operational Excellence

by Alfred Macha, AMT PARTNERS

Last month's column introduced the first phase of the roadmap in becoming a preferred supplier, which initial phase consisted of transforming your company's culture with a Lean Six Sigma approach. Takeaways included creating a culture that embraces continuous improvement by creating the right mindset of ownership, empowerment, agility, and accountability. Your Lean Six Sigma program needs to be rightly sized to your organization's structure for it to be sustainable. The second phase involves establishing the six pillars of operational effectiveness.

Attaining quality systems certification to a base standard of ISO 9001 or industry-specific QMS standard for medical devices (ISO 13485), automotive (TS 16949), telecommunications (TL 9000), or aerospace (AS9100D) will provide you a solid foundation to your operations. The next step is to build on that quality systems foundation and take your factory to a higher level of performance by establish-

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Figure 1: Operational excellence.

ing six pillars to achieve operational effectiveness (Figure 1):

1. Data integrity
2. Visual factory
3. Right metrics
4. Change control
5. Process monitoring
6. Learning culture

1. Data Integrity

Remember that decisions are made from data captured from your process. Get the data right! This sounds basic, but many organizations fail to consistently retrieve accurate data from their manufacturing floor. Technological advancements in scanning, automated measurements, and inspection allow for accurate data collection. However, many manufacturing processes still require manual data entry data inputs into their ERP, MES, or paper logs in the production floor to capture process or product data.

Make sure that you have configured your data collection system with the right instructions and verification steps to ensure data is collected accurately. A best practice in a manufacturing environment is to have visual guides or pictures that clearly describe a process condition or product defect with a reference code that can be used in your ERP or data collection system. Train your workforce to these visual references and establish a simple audit plan to verify data accuracy on a regular basis. At the end of the day, the credibility of your operations starts with the confidence your team has in making decisions based on the right data.

2. Visual Factory

The year was 2001, and I was a quality manager for a large PCB company in Arizona that had a 24/7 operation. The factory had a footprint of 250,000 square feet and a workforce of 1,500 employees. The executive team was determined to transform the factory into a top performer in the industry, and one initiative was to reduce process variation by having visual work instructions. We had to convert over 300 technical procedures across the factory into practical visual work instructions. The effort required the involvement of over 50 employees from across the factory.

The project resulted in higher product yields, fewer customer complaints, and high employee engagement and customers took notice. We became a preferred PCB supplier in the industry. Now, manufacturing companies have cost-effective options to create not only visual work instructions but also a complete visual factory with the use of electronic visual displays, tablets, smartphones, and customized software to support this initiative.

The benefits of implementing an effective visual factory can be quantified. A software

development organization, VKS, that specializes in visual factory solutions has research data collected via CMP AMS Ltd. and reports a quality improvement of 93% reduction of internal defects from the implementation of smart work instructions (Figure 2).

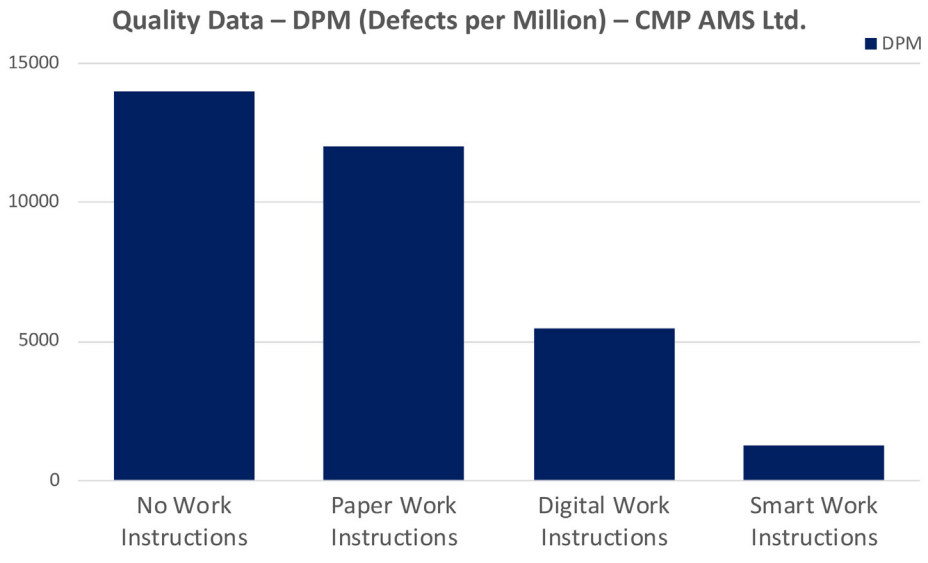

Figure 2: Defect reduction with smart work instructions.

3. Right Metrics

Measurements drive behaviors. There is so much truth in that statement, and having the right metrics in your operations can make the difference in how the workforce performs in the factory. Top companies create metrics or key performance indicators (KPIs) with the focus to bring value to their employees. Philosophically, remind your team that it's not the quantity of metrics but the quality of metrics that matter. Fewer is better.

Here are five questions you can ask as you define the right metrics:

- What is your organization's value proposition?
- What behaviors do you want to instill in the workforce that supports your value proposition?
- Are you collecting the right data to measure outputs that drives those behaviors?
- How frequently will you be communicating the metrics to your employees?
- What action plans will you take to address trends or outliers shown in your metrics?

Once you have documented a procedure that answers these questions, then select a handful of metrics and make them part of your culture's DNA.

4. Change Control

Change is inevitable, and how we control change is challenging. Hundreds of books and methods on change management exist with valuable theoretical guidance. However, the secret recipe of change control is not creating the perfect procedure based on theory; instead, it's about creating a practical procedure based on risk levels when a change occurs.

I highly recommend funneling all changes that affect manufacturing into one common change control system. One system allows for standardization, consistency, and traceability of records. Figure 3 provides a simple flowchart of how this system can be set up based on risk levels.

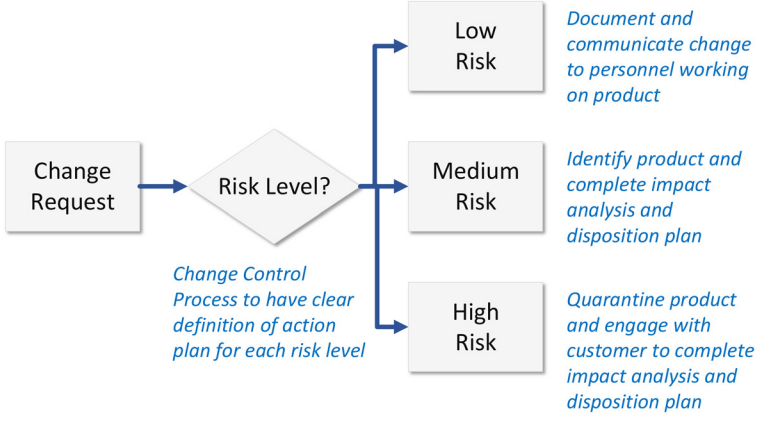

Figure 3: Example of change control that affects products.

5. Process Monitoring

The challenge that every manufacturing company faces is uncontrolled variation. While it's inevitable that the parameters of your operation are going to change in some ways from time to time, it's important to ensure that those variations are controlled and predictable. Ensure that you're always one step ahead of the game.

Evaluating your process(es) to determine what factors have a higher impact on variation is a must. Once you identify those factors that can induce higher levels of process variation, then you need to closely monitor the outputs of those factors. This is where process monitoring becomes a vital component of your operations. Process monitoring can be carried out in many forms. Here are common methods for process monitoring that have proven to be effective in many organizations:

- Identify critical parameters for your operation and monitor these parameters via statistical process control. Not every parameter is critical so you will need to keep the list of critical parameters to a manageable number
- Allocate adequate funding to invest in proper automated process monitoring systems when possible
- Implement a process audit/monitoring program where qualified personnel can spot check critical operations constantly
- Change the mindset on the production floor. Process monitoring should never be viewed as a method to blame the operator for errors; rather, it should be viewed as a tool to help operations personnel achieve success

6. Learning Culture

Traditional training programs require periodic refresher training of procedures or work instructions with a certification exam at the end to demonstrate competency in the subject content presented. This approach brings value to organizations in reaching adequate levels of operator knowledge and compliance but does not create the level of learning that great organizations foster.

Achieving operational effectiveness requires a new level of engagement with employees by creating a learning culture. The first step in creating a culture of learning in your workplace begins with your leaders. Since they are reinforcing training initiatives, they should be supportive of a learning environment. All employees need to be empowered to reach their potential by continuously gaining new skills and knowledge via in-house mentoring or coaching or external professional development courses.

Here are a set of practical guidelines that you can start implementing in your organizations to create a learning culture.

- Offer leadership sessions to all employees. Everyone in the organization should be prepared to lead a team, project, or activity as opportunities present themselves
- Encourage employees to make decisions based on the knowledge they have gained. Challenge employees to apply newly learned knowledge in their current positions
- Give feedback on employees' performance after they have learned new skills. New knowledge won't be retained unless it's applied in an employee's work function
- Recognize learning. Employees who have successfully learned new skills and abilities should be recognized, and encourage others to follow suit **SMT007**

Alfred Macha is the president of AMT Partners. He can be reached at Alfred@amt-partners.com. To read past columns or contact Macha, click here.

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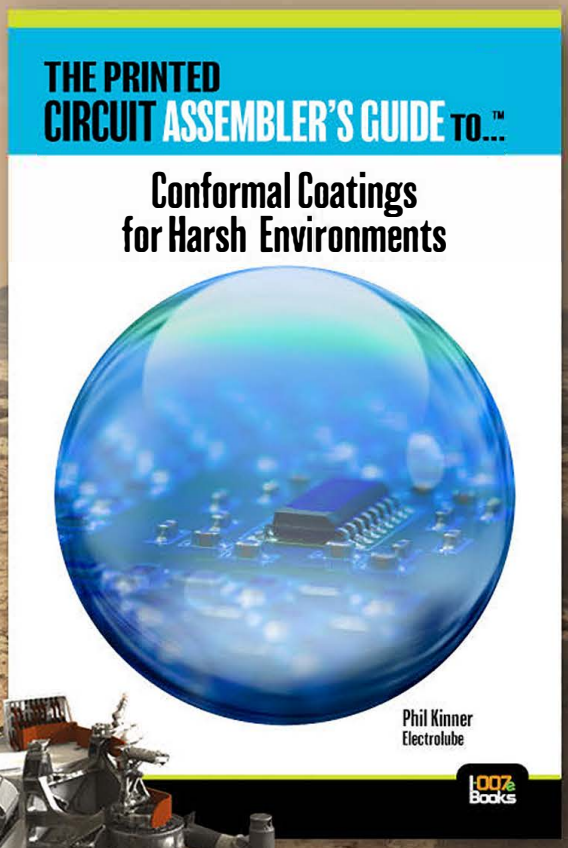

I·007e Books

1 The Government Circuit: Team IPC Working on North American Trade, EPA Regulations, EU Policy, and More ▶

In one of the highlights of IPC's work every year, top executives from electronics companies from across the U.S. came together in Washington, D.C., recently to call for policies that will drive the electronics industry's success. Attendees met with leading policymakers to discuss the U.S.-Mexico-Canada Agreement (USMCA), the electronics supply chain, EPA regulations, and workforce education.

2 Punching Out! Delegate and You Shall Be Set Free ▶


Tom Kastner

It is good for owners/CEOs to step back a few times a year and think about what they do well, what they like to do, and what others can do better. Delegating simple tasks, like sweeping floors, is easy, but delegating sales management or quality control might be tougher.

3 Operational Excellence: Process Validation Can Lead to Higher Performance Levels ▶


Alfred Macha

In this first column from Alfred Macha, the author provides a practical guideline on how to effectively implement a sustainable process validation program for contract manufacturers.

4 Zulki's PCB Nuggets: Avoid PCB Wire-bond Loop Failures ▶


Zulki Khan

Today, hybrid PCB manufacturing is making greater inroads into our industry, which is the marriage of traditional SMT manufacturing together with microelectronics and wire bonding. In many cases, the OEM working with EMS providers doesn't fully understand the nuances of effective wire bonding and related failures.

5 Communication and Information: Two Keys to Success ▶


Duane Benson

Nolan Johnson and Duane Benson, an I-Connect007 columnist and a representative from Milwaukee Electronics, discuss how assemblers can help their customers through submitting and maintaining accurate information, and engaging in open communication early and often about the highly important bill of materials.

6 Green Circuits' Three Tips to Be a Well-prepared Customer ▶


Joe Garcia

Nolan Johnson speaks with Joe Garcia, VP of sales and marketing at Green Circuits, about how they can help on both the front and back end of the process, their hidden gem—design services—as well as three tips to be a well-prepared customer.

7 Collaboratively Creating Wearable Medical Products ▶

Patty Goldman, Barry Matties, and Happy Holden recently spoke with David Moody and Rich Clemente of Lenthor Engineering along with Anthony Flattery and Amit Rushi—their customers at GraftWorx. They discussed a recent project and how they worked together to solve a difficult problem by designing a rigidized flex circuit for their product.

8 IEC Electronics to Build $22M Manufacturing Facility in New York ▶


Gov. Andrew M. Cuomo

Governor Andrew M. Cuomo recently announced the groundbreaking of IEC Electronics Corp.'s new, state-of-the-art facility in Newark, Wayne County.

9 Whizz Systems on Knowing Your Strengths and Building Customer Relationships ▶


Muhammed Irfan

Located in the heart of the Silicon Valley, Whizz Systems Inc. provides electronics product design, development, and manufacturing services. Muhammed Irfan, president of the company, speaks with Nolan Johnson about knowing your strengths, engaging start-ups, and building strong customer relationships through education and preparation.

10 IPC: N.A. EMS Growth Is Slowing, but Opportunities Remain ▶

The North American EMS industry continued to enjoy positive year-to-date growth in the first quarter of 2019, but growth rates for both sales and orders are slowing, according to IPC's first-quarter 2019 North American EMS Market Report.

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Analyst Programmer, Hong Kong

We believe in caring about our people because they are our greatest asset. CML works with multicultural stakeholders daily to achieve more and bring them the best solutions. That's why we continuously invest in optimizing our culture and focus on providing our team with opportunities to develop their skills (e.g., through professional coaching to achieve their highest potential).

The analyst programmer will assist the IT and ERP manager in Hong Kong to support the company's BI systems, ERP systems, and other related IT-landscape applications.

In addition, this post will participate in system development projects and provide support including, but not limited to, user requirement collection and analysis, user training, system documentation, system support and maintenance, enhancement, and programming.

- Develop and enhance related IT systems and applications
- Prepare functional specifications
- Transfer the relevant business and interface processes into IT systems and other applications to get a maximum automation degree and prepare all required business reports
- Conduct function testing and prepare documentation
- Manage help desk/hotline service

CML is a leading provider of printed circuit boards. We develop tailor-made sourcing and manufacturing solutions for our customers worldwide with strong partnerships and reliable connections.

apply now

APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

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Career Opportunities

Field Service Engineer: Multiple U.S. Locations

Reporting to a regional service manager, these customer-focused engineers will uphold the Koh Young culture while delivering professional technical services for our award-winning portfolio of inspection solutions. The role will enthusiastically visit our growing list of customers for installations, training, and evaluations, as well as technical support and maintenance.

We are looking for candidates with a technical degree or equivalent plus three or more years in a production environment with relevant experience. Given our growing customer base, the position will require extensive travel, including some internationally, as well as a collaborative attitude that drives success.

Koh Young is the leading 3D measurement-based inspection equipment and solutions provider. We perform quality control and process optimization across a growing set of industries including PCBA, machining, final assembly, process manufacturing, and semiconductors. In addition to our corporate office in Seoul, our international sales and support offices help us maintain a close relationship with our customers and provide access to a vast network of inspection experts.

Join the industry's leading provider of true 3D inspection solutions. Forward your resume to Michelle.Hayes@KohYoung.com.

apply now

Vision and Machine Learning R&D Engineer

Atlanta, GA or San Diego, CA

At Koh Young, we are focused on developing the future and continue to bolster our newly established R&D center near San Diego, California, with top talent focused on vision engineering and machine learning for electronics and medical applications. Currently, we are collaborating with top medical universities and hospitals across the U.S., Korea, and Japan to develop innovative neurosurgical robotic systems. With core technologies developed in-house, we expect to deliver neurosurgical breakthroughs.

The role will develop practical, scalable 3D machine learning solutions to solve complex challenges that detect, recognize, classify, and track medical imagery. Additional focus on the design, implementation, and deployment of full-stack computer vision and machine learning solutions.

The ideal candidates will hold a master's (doctorate preferred) in computer science or electrical engineering with at least three years of relevant experience. We desire a strong understanding of machine learning and computer vision algorithm application within embedded systems, plus significant vision expertise in multi-view geometry, 3D vision, SFM/SAM, and activity recognition.

Koh Young is the leading 3D measurement-based inspection solutions provider. We perform quality control and process optimization across a growing set of industries including electronics, final assembly, semiconductors, and most recently, medical imagery.

Join the 3D inspection leader as we expand. Forward your resume to Michelle.Hayes@KohYoung.com.

apply now

Career Opportunities

TAIYO AMERICA

Technical Sales Engineer

San Jose, CA, USA

The technical sales engineer will perform technical audits and help customers troubleshoot and optimize their solder mask process, prepare and deliver technical presentations explaining products or services to customers and prospective customers, collaborate with sales teams to understand customer requirements and provide sales support, secure and renew orders and arrange delivery, and help in researching and developing new products.

Required Education/Experience:
Applicants must have good "hands-on" knowledge of the printed circuit board (PCB) industry and the liquid photo imageable (LPI) solder mask process. Candidates must be self-motivated, capable of managing key accounts and developing new business opportunities that generate new sales.

- College degree preferred with solid knowledge of chemistry
- 3-5 years of work experience in a technical role within the PCB industry
- 3-5 years of work experience in a sales role
- Computer knowledge, Microsoft Office environment
- Good interpersonal relationship skills
- Good English verbal and written skills are necessary

Working Conditions:
Occasional weekend or overtime work. Travel may be 25-50% or greater.

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INDIUM CORPORATION®

Multiple Positions Available

The Indium Corporation believes that materials science changes the world. As leaders in the electronics assembly industry we are seeking thought leaders that are well-qualified to join our dynamic global team.

Indium Corporation offers a diverse range of career opportunities, including:

- Maintenance and skilled trades
- Engineering
- Marketing and sales
- Finance and accounting
- Machine operators and production
- Research and development
- Operations

For full job description and other immediate openings in a number of departments:

www.indium.com/jobs

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Career Opportunities

THERMAL SYSTEMS

Service Engineer Reflow Soldering Systems (m/f)

To strengthen our service team at Rehm Thermal Systems LLC. in Roswell, Georgia, we are seeking candidates to fill the position of Service Engineer—Reflow Soldering Systems.

Your area of responsibility:

- Installation of Rehm reflow soldering systems at the customers' site
- Maintenance and repair work as well as technical service for our customers in the USA and Mexico
- Execution of machine training

Your profile:

- Completed education studies as an engineer in the field of electrical engineering/mechatronics or comparable education (m/f)
- Basic and specialist knowledge in the field of electronics and electrical engineering/mechatronics
- High willingness to travel and have flexible employment
- Service-oriented and like to work independently

We offer:

- Performance-oriented, attractive compensation
- Comprehensive training
- A safe workplace in one successful group of companies
- Self-responsibility and leeway

Please send application documents online to Natalie Werner at n.werner@rehm-group.com.

apply now

Manncorp™

SMT Field Technician
Huntingdon Valley, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:

- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:

- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
- Ability to arrange and schedule service trips

We Offer:

- Health and dental insurance
- Retirement fund matching
- Continuing training as the industry develops

apply now

Career Opportunities

Sales Personnel, Japan

The Gardien Group is looking to expand the sales team in Tokyo, Japan, and seeking highly motivated team players with a positive attitude. Prior experience in the PCB industry is an advantage but not necessary for the right candidate.

The role involves working closely with the customer to identify their needs and deliver the right solution. The candidate should be able to offer a high level of customer satisfaction to ensure ongoing sales.

Training will be provided along with a competitive benefits package, excellent growth opportunities, and periodic bonuses.

Interested candidates, please contact us at careers.jp@gardien.com with your resume.

Kindly note only shortlisted candidates will be notified.

apply now

Sales Representatives (Specific Territories)

Escondido-based printed circuit fabricator U.S. Circuit is looking to hire sales representatives in the following territories:

- Florida
- Denver
- Washington
- Los Angeles

Experience:

- Candidates must have previous PCB sales experience.

Compensation:

- 7% commission

Contact Mike Fariba for more information.

mfariba@uscircuit.com

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Career Opportunities

ELECTROLUBE
THE SOLUTIONS PEOPLE

We Are Recruiting!

A fantastic opportunity has arisen within Electrolube, a progressive global electro-chemicals manufacturer. This prestigious new role is for a sales development manager with a strong technical sales background (electro-chemicals industry desirable) and great commercial awareness. The key focus of this role is to increase profitable sales of the Electrolube brand within the Midwest area of the United States; this is to be achieved via a strategic program of major account development and progression of new accounts/projects. Monitoring of competitor activity and recognition of new opportunities are also integral to this challenging role. Full product training to be provided.

The successful candidate will benefit from a generous package and report directly to the U.S. general manager.

Applicants should apply with their CV to
melanie.latham@hkw.co.uk
(agencies welcome)

apply now

ZENTECH

Zentech Manufacturing: Hiring Multiple Positions

Are you looking to excel in your career and grow professionally in a thriving business? Zentech, established in Baltimore, Maryland, in 1998, has proven to be one of the premier electronics contract manufacturers in the U.S.

Zentech is rapidly growing and seeking to add Manufacturing Engineers, Program Managers, and Sr. Test Technicians. Offering an excellent benefit package including health/dental insurance and an employer-matched 401k program, Zentech holds the ultimate set of certifications relating to the manufacture of mission-critical printed circuit card assemblies, including: ISO:9001, AS9100, DD2345, and ISO 13485.

Zentech is an IPC Trusted Source QML and ITAR registered. U.S. citizens only need apply.

Please email resume below.

apply now

Career Opportunities

BLACKFOX
Premier Training & Certification

IPC Master Instructor

Join the world's premier electronics manufacturing training and certification firm. This position is responsible for IPC and electronics skill-based instruction and certification at the Arizona training center as well as training events as assigned by the company's sales/operations vice president. This position is either as a contractor or full-time. Candidate must have IPC training experience and several years of hands-on experience in electronics manufacturing. Current IPC certification is a definite plus! This position will require some travel to clients, facilities and other training centers.

For more information, click below.

apply now

YOUR JOB AD HERE

For information, please contact:
BARB HOCKADAY
barb@iconnect007.com
+1 916.608.0660 (-7 GMT)

I·Connect007
GOOD FOR THE INDUSTRY

Identity Branding

What do you stand for?

I don't know who you are

I don't know your values

I don't know what you stand for

I don't know your reputation

Now, what is it you want to sell me?

This may seem extreme, but don't assume your prospects already know or remember this about you...

In fact, they may know something quite the contrary if you leave it up to your competitor to educate them about you.

At I-Connect007 we can help you build and strengthen your brand.

Learn how we can help you!

I·Connect007

GOOD FOR THE INDUSTRY

Events Calendar

SMTA Ohio Expo & Tech Forum ▶
August 8, 2019
Strongsville, Ohio, USA

The 20th International Conference on Electronic Packaging Technology ▶
August 11–15, 2019
Hong Kong

NEPCON South China 2019 ▶
August 28–30, 2019
Shenzhen, China

SMTA International 2019 ▶
September 22–26, 2019
Rosemont, Illinois, USA

productronica India 2019 ▶
September 25–27, 2019
Delhi NCR, India

electronica India 2019 ▶
September 25–27, 2019
Delhi NCR, India

52nd International Symposium on Microelectronics ▶
September 29–October 3, 2019
Boston, Massachusetts, USA

productronica 2019 ▶
November 12–15, 2019
Munich, Germany

Additional Event Calendars

Coming Soon to *SMT007 Magazine:*

AUGUST: Coatings
Much of the environmental durability of electronics—and some of their overall manufacturability—comes from the finishes and coatings. We explore the menu of options and benefits in finishes and coatings.

SEPTEMBER: Standards
We report on recent developments in current and emerging standards and take a step back to discuss some of the inherent strengths and weaknesses of standards processes.

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