

February 2012

- 12** Latest on Lead-Free Capable Materials *by Yash Sutariya*
- 24** Circuit Materials and High-Frequency Losses of PCBs *by John Coonrod*
- 36** Thermal Management Substrates *by Ian Mayoh & Mark Goodwin*
- 78** DuPont Talks Development Trends and Highlights in PCB Materials Industry *by Richard Ayes*

the **pcb** magazine

AN  I-CONNECT 007 PUBLICATION



2012 PREVIEW

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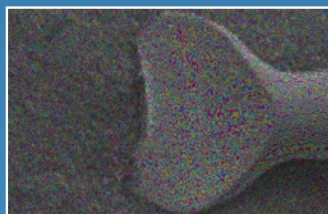
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Final Finishing

Universal Finish SolderBond (ENEPIG and ENEP) for Soldering, Au-Wire and Cu-Wire Bonding



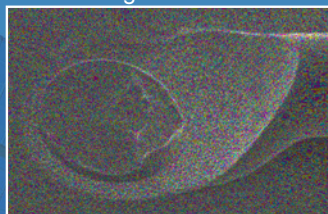
Soldering



Au-wire wedge

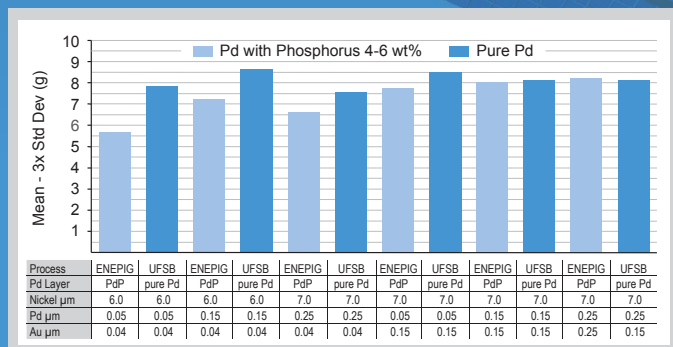


Al-wire wedge



Cu-wire wedge

Gold Wire Bond Pull Test



Universal Finish SolderBond provides also with low Au-thickness excellent results, as pure Pd is 50% softer than Palladium-Phosphor (4-6wt%).

NiPdAu (ENEPIG)		NiPd (ENEP)
Deposit Structure		
Electroless Nickel	4.0 μm - 6.0 μm	4.0 μm - 6.0 μm
Electroless Palladium	0.05 μm - 0.3 μm	0.2 μm - 0.3 μm
Immersion Au	0.02 μm - 0.06 μm	--
Functionality		
Soldering		
Eutectic Sn/Pb	Good	Good
Sn-Ag-Cu Alloy	Excellent	Excellent
Contact Switching	Yes	--
Al Wire Bonding	Yes	--
Au Wire Bonding	Yes	--
Cu Wire Bonding	--	Yes

Process Flow



Pure Pd

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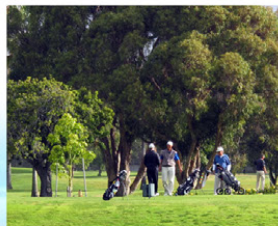
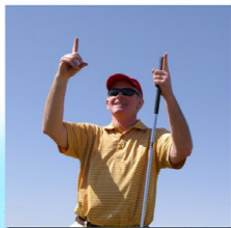
Gold Wire Bond Finish

Copper Wire Bond Finish

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the pcb magazine

AN I-CONNECT007 PUBLICATION

MATERIALS

It is a material world – and this month The PCB Magazine proves it!

Printed circuit materials have to satisfy many masters — physical, mechanical, thermal and electrical to name just a few. From laminates options and the bewildering catalogue of material properties and characteristics, how are the right materials chosen? What are the latest advances in technology and how can they help the designer achieve required performance levels? This month we've got the answers, with feature articles from Saturn Electronics, Dupont, Ventec Europe Limited and more!

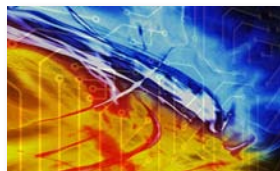
- 12 Latest on Lead-Free Capable Materials**
by Yash Sutariya



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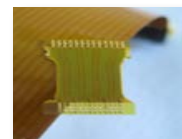
- 36 Thermal Management Substrates**
by Ian Mayoh and Mark Goodwin



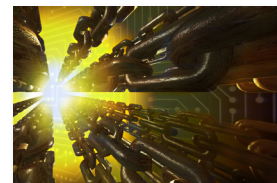
- 70 Conductive Anodic Filaments: The Role of Epoxy-Glass Adhesion**
by Seth Binfield, Dr. Craig Hillman, Thomas Johnston, and Dr. Nathan Blattau



- 78 DuPont Talks Development Trends and Highlights in PCB Materials Industry**
by Richard Ayes



- 90 Overview: Technological Developments and the Materials Supply Chain in the PCB Industry**
by Mike Devine



IPC APEX EXPO 2012 Special Section

- 46 IPC APEX EXPO 2012 Show Schedule**



- 48 FREE Keynote Presentations**

- 49 Technical Conferences**

- 51 Standards Development Meetings**

- 52 Professional Development Courses**



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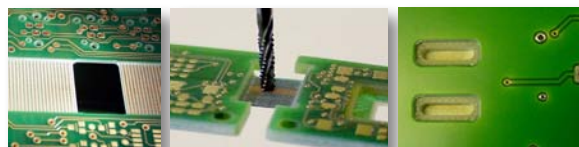
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AN I-CONNECT007 PUBLICATION

MATERIALS

ARTICLES

- 58 Advanced Routing Technology —
Depth Routing**
by Volker Feyerabend



- 100 Flexible Circuit
Solutions Continue
to Evolve and
Expand Their
Range of Capability**
by Joseph Fjelstad



VIDEO INTERVIEWS

- 18 IPC: How Environmental
Regs Affect your Business**
- 45 Ventec Celebrates Five Years**
- 103 Productronica's Unsung Hero**



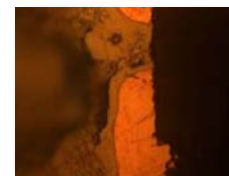
NEWS HIGHLIGHTS

- 30 Flex007 Highlights**
- 56 MilAero007 Highlights**
- 81 PCBDesign007 Highlights**
- 102 Supplier/New Product Highlights**
- 104 Top Ten Most-Read News Highlights
from PCB007 This Month**



COLUMNS

- 8 7 Billion**
by Ray Rasmussen
- 20 Advances in Copper Plating, Part A**
by Karl Dietz
- 32 Let Your Feelings DAM Go:
Be a Horrible Manager Like Steve Jobs**
by Gray McQuarrie
- 66 Case Study: PTH Voids**
by Michael Carano
- 74 A Cautionary Tale**
by Steve Williams
- 82 Board-Level Simulation and the Design
Process: Plan B — Post Layout Simulation**
by Barry Olney
- 96 Rigid-flex Manufacturing Part II: Materials**
by Dale Smith
- 106 It's Show Time!**
by Barry Matties



SHORTS

- 94 Intercept Technology, Inc. to Release
New User Interface Pantheon 7 at
IPC APEX EXPO**
- 103 Taiyo America to Unveil Liquid Photo-
imaging Solder Mask at IPC APEX EXPO**

EXTRAS

- 108 Events Calendar**
- 109 Advertisers Index & Masthead**





Electronic Chemicals, LLC

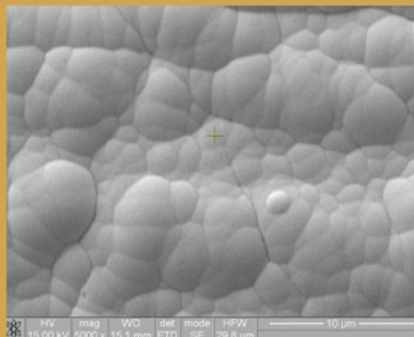
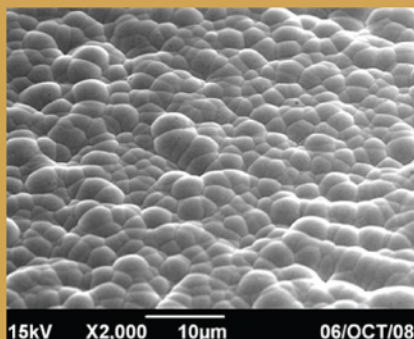
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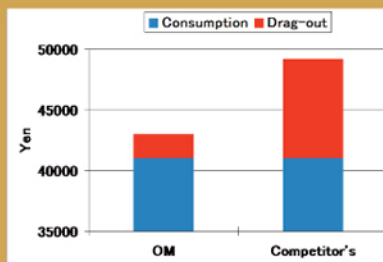
OM doesn't attack Ni surface under low Au content.

Au bath	Conventional IG	Conventional IG	OM	OM
Au content	2g/L	1g/L	1g/L	0.5g/L
N bath	Conventional Ni	Conventional Ni	930	930
SEM				

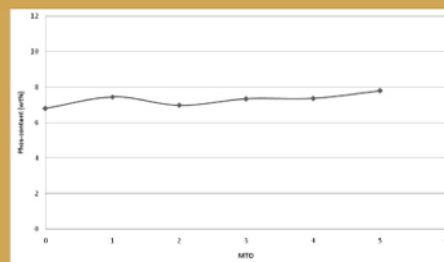
Ni attack is heavier in low Au

Ni attack not observed at 1g/L

New Combination OM/OMG 930 can Further decrease



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7 Billion

by Ray Rasmussen

I-CONNECT007

SUMMARY — *With nearly a billion people being added to the planet every decade, the U.N. predicts a worldwide population of nine billion as soon as 2050. In addition to the societal ramifications this number presents, what's in store for our industry in terms of added consumers of electronic products?*

Officially, as of October 31, 2011, more than seven billion people are crammed into this world — this little speck of dirt floating in space that we all call home. (It's a bit scary that just 12 years ago we passed the six billion mark, on October 12, 1999.) For some perspective, the one billion mark was achieved in 1804, a little over 200 years ago. We're now adding about a billion people every decade. Crazy! The U.N. pegs the peak of global population growth at around nine billion, which we'll hit in 2050. It goes up by a couple hundred million after that but then settles back down to a little less than nine billion. If you're so inclined, here's the link to the [U.N. report](#). What's interesting is that the nine billion mark seems to be where we'll settle for the foresee-

able future. In 2300, it is forecast that the population will still be around the same. That must be Mother Earth's sweet spot, or maybe it's all she can handle.

I see this in a couple ways. First, it's frightening. That's a lot of people. What are we going to do with them all? How are we going to feed and house and educate them? Where are they going to work? The problems seem almost insurmountable. We're already doing a horrible job at taking care of the ones we have now. Add another 50% on top and things get ridiculous.

The world will certainly be challenged in the years ahead as we adjust to the weight of our children and grandchildren to come.

For most of us in North America and Europe, we'll be spared from the direct repercussions of huge increases in population.

Most of the struggles will be on the ground in Asia (an additional 1.5 billion) and Africa (an additional one billion), the two areas where most of the increases will take place. In the West, and the rest of the developed world, ours will be a moral obligation. Mostly. We'll have to do our part, I suspect, one way or another.

Africa will be the winner, if you can call it that, with the fastest



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Cost

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growth rates coming during the next 40 years. Latin America also adds to the total, somewhat, with its population growing from about 520 to 768 million by 2050. Asia, as you might have suspected, will add the most people.

Developing Economies Plus Growing Populations

Today, from a business perspective, in much of the developing world, we have a double-whammy happening. This is where developing countries expand their middle classes by adding more consumers to the mix. In addition, many of these developing countries have very high growth rates, which are compounding the number of new (potential) consumers in the market. I would guess we have 20 or more years of these combined factors ahead of us until we start to see growth rates slow somewhere around 2030. After growth rates start slowing, we'll still have a continual increase in the number of new consumers entering the market each year, which will drive industry growth and expand markets for electronics, but we won't have those numbers compounded by high rates of population growth. I would expect the former condition to continue for at least 100 years with the rate declining over time as economies move from developing to developed-nation status. With Asia (China, India and South Asia) already on the road to developed status, we may see much of this growth peter out by 2050, leaving Africa mainly to provide that combination of developing nations with huge population growth.

A Few Nuggets

I did gather a few nuggets out of my study on global populations and emerging markets. Some of this information might be useful to us in the short-term, at least for those of us who still plan to be working in the industry for the next 10-20 years.

First, while China's population will grow around 9% over the next 40 years, India's will grow 51%! I expect that India will be forced in the coming years to make major adjustments to its industrial policies. They have to do something. They already have a critical need for more jobs. We have seen some efforts at improving infrastructure along with business-friendly industrial policies recently, but there's

still a long way to go. We'll have to see some big moves by India in the coming decades in order to get on top of their huge population. Of course, China won't roll over too easily if India starts to adopt similar industrial strategies, but it seems almost certain that China's factory to the world status will have to be shared with the rest of Asia and Africa. Africa's population, for instance, will double in size by 2050 and will



require tons of jobs. What's interesting is that while China and India's growth begins to wane, Africa's keeps growing in the second half of this century at almost the same rate as the first half, with their population increasing to about 2.3 billion people by 2100. And, although we'll see a lot of folks enter the middle class in South and Central America, which will drive markets, population growth won't be much of a factor over the next 40 years, likely subduing interest from global manufacturers somewhat. I'm sure



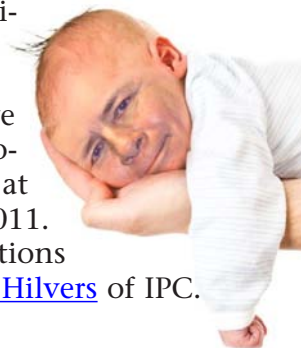
they'll get plenty of attention, but it won't be as hot a market as Africa and West Asia.

On the Other Hand...

If you just think about the burden of this huge population on the planet, it's quite daunting; on the other hand, what an opportunity it presents! Billions of new consumers will enter the market. Considering those born from 1999-2011, the oldest are 12 — that's about a billion more potential consumers — and those yet to come, another two billion; that's three billion people who will need and want the technologies and services that electronics can provide. Moreover, that's on top of what we already have! If we have three billion electronics consumers today, over the next 50 years we'll likely get to as high as six billion, or twice the current market. Keep in mind that electronics will provide solutions to many of the problems we have in the world today and to those coming in the future. Most people on the planet by 2050 will have some types of electronic products in their lives. It may be as simple as an LED light or simple communications device (notice I didn't say cell phone?). I suspect that electronics will be everywhere by then, connecting the world,

connecting governments to their citizens. Education, transportation, health, food, you name it, will be controlled, managed and enhanced with electronics. By then Apple could be the first trillion-dollar company: Who knows?

Well, I hope you've enjoyed this glimpse into the future. I have one more thing to share with you. I'd say it's a bit of a scoop since none of our competitors picked up this one. If you're wondering who the 7 billionth baby was, we have an exclusive photo of Anthony Hilvers III. He was born at 12:00:01 on October 31, 2011. Please send your congratulations to the proud grandpa, [Tony Hilvers](#) of IPC. Congrats, Tony! **PCB**



Ray Rasmussen is the publisher and chief editor for I-Connect007 publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *Circuitree Magazine*. Ray can be contacted at: ray@iconnect007.com



LEAD-FREE

Latest on Lead-Free Capable Materials

by Yash Sutariya

SATURN ELECTRONICS CORPORATION
SATURN FLEX SYSTEMS

SUMMARY — *Advancements in lead-free materials are not necessarily restricted to the materials themselves; they often develop in our knowledge base of the characteristics and performance criteria of the already available library of materials in the marketplace. This is truly the low-hanging fruit.*

Advancements in Materials... or in the Way We Think?

It's been over five years since RoHS compliance took hold. Initially, the topic dominated industry conversation as it seemed everyone had an opinion on properly transitioning to compliance. Apparently, this topic ran out of gas — at least from a copper-clad laminate standpoint.

It's time to fire up that engine again and examine some new materials in development as well as a few existing ones that were neglected from the outset — at least from the North American standpoint.

According to Steve Jobs, "You can't connect the dots looking forward; you can only connect them looking backwards." This article will review learned experiences, interpret current methods and analyze developing laminates.

How We Specify Lead-free Capable Laminates

Referencing the IPC-4101 PCB materials standard is the most efficient way to specify raw materials. This automatically aligns your fabrication notes to the latest version of this standard. Below is a summary of the most common lead-free capable laminates, from the IPC-4101 standpoint.

There are six distinct silos here, but I consider there to be three distinct categories. The only thing that distinguishes one material from its corresponding pair is the presence of fillers.

If you've read some of my past pieces, I'm probably going to sound like a broken record. You're actually right, but only because I see the same mistakes being made continually. It's almost as if designers are copying and pasting fab notes from past revisions to current designs, but that's just crazy talk. No one does that...

Initially, most customers reflexively specify "best" materials rather than performance-appropriate ones. After addressing more pressing matters, such as component libraries and new line administrations, they would return to evaluating other grades of materials to enjoy cost savings.

The original goals have been accomplished;

“ Initially, most customers reflexively specify “best” materials rather than performance-appropriate ones. ”

	/99, /124	/101, /121	/126, /129
Resin System			
Primary	Epoxy	Difunctional Epoxy	Epoxy
Secondary 1	Multifunctional Epoxy	Multifunctional Epoxy	Multifunctional Epoxy
Secondary 2	Modified/Non-epoxy (max 5%)	Modified/Non-epoxy (max 5%)	Modified/Non-epoxy (max 5%)
Fillers	99: Inorganic; 124: n/a	101: Inorganic; 121: n/a	126: Inorganic; 129: n/a
T_g	150 C min.	110 C min.	170 C min.
T_d	325 C min.	310 C min.	340 C min.
T260_(min)	30 min	30 min	30 min
T288_(min)	5 min	5 min	15 min
T300_(min)	ABBUS	ABBUS	2 min

Due to fillers, IPC designates 6 distinct silos but we've trimmed it down to three by conflating corresponding materials.

Figure 1: IPC 4101.

poor Larry the Lead-Free Laminate Specification, on the other hand, was abandoned faster than the Microsoft Zune.

I'm annoyed when reading articles in which the author's opinion either outweighs or completely lacks factual evidence (maybe another thing that no one does?), so let's review some user polls we took on this topic.

Materials are specified in a variety of ways. Only Td addresses the material's lead-free assembly capabilities; the rest do not. Since this poll was taken a few years ago, we do see more

notes calling out the IPC-4101/126 or /129 reference, but there's still work to be done.

Delaminate Already

The industry needs to deal with delamination. While phenolic materials have great thermal properties ($T_g > 170^\circ\text{C}$ and $T_d > 340^\circ\text{C}$, when conforming to IPC-4101/126 or 129), most are extremely weak in the fundamental areas of moisture absorption and copper-to-laminate adhesion.

Moisture Absorption

Standard 130Tg FR-4 materials typically have a moisture absorption rate of 0.20% when measured using a 0.028" thickness core material. Using the same test vehicle, phenolic materials often measure moisture absorption up to 0.45%. These results no longer appear on data sheets, however, as test vehicles have been altered to 0.059" thickness.

Copper to Laminate Adhesion

Standard 130Tg FR-4 materials generate peel strength results of 8-10 lbs. Holding all parameters equal, phenolic materials generate peel strength results of 3-4 lbs.

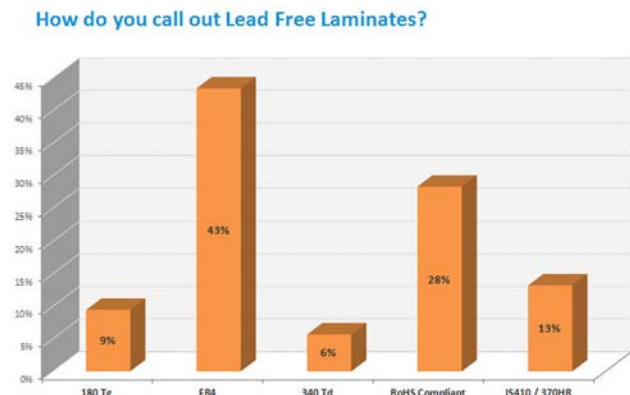


Figure 2: Laminate poll.

Vapor Escape

Material characteristics exacerbate lead-free assembly parameters. Absorbed moisture remains trapped in the PCB until escaping the dielectric from the weakest point in the board, which is typically plated via holes. During standard SnPb assembly at 200°C, the vapor pressure is 225 psi. At lead-free assembly temperatures (250°C), however, the vapor pressure increases to 575 psi.

The Perfect Storm

Combining the increased vapor pressure with phenolic material characteristics of increased moisture absorption and lower adhesion strength creates a perfect storm capable of ruining entire production runs. In fact, the forces here are so strong that often, instead of just blowing vias, entire layers separate from each other forming delamination areas of 1 square inch or greater.

SEC Solution

Mid-Grade Materials

We advocate using mid-grade materials found under IPC 4101/99 and /124. While thermal properties (150°C T_g and 325°C T_d) are lower than /126 or /129, the mechanical characteristics more than compensate (demonstrated in lab tests below). Further, I have yet to find one person in the industry who can give me a formula showing the extra benefits of a 5 or 10 degrees T_d increase. For more detailed information, please view our [Lead-Free Cost Reduction webinar](#).

Test data on IPC-4101/99 and /124 materials:

In the final analysis, standardized lab tests and assembly simulation demonstrated that IPC-4101/99 and /124 materials not only outperform /126 and /129 materials regarding moisture absorption and peel strength, but also pass (without a single failure) 6x lead-free reflow at 260°C peak temperature.

Now, Let Me Blow Your Mind...

Commercially, the lead-free transition immediately increased the bare board's cost. For

Test Group	Results
Condition	Condition A
Peel Strength Side 1:	11.73 lbs/in.
Peel Strength Side 2:	10.95 lbs/in

Figure 3

Test Group	Results
Percent Weight Loss:	0.20%
Start Temperature:	0 degrees C°
Stop Temperature:	0 degrees C°
Comments:	Moisture Method
Weight Loss % by TGA	% Weight Loss = 0.1717%

Figure 4

Conditioning	As Received
Board Number	14573-1
Material	IS400
Conveyor Speed (cm/min)	48
TC Temp Range	3.4
Time above 217	101
Passes to Fail	6x Pass

Figure 5

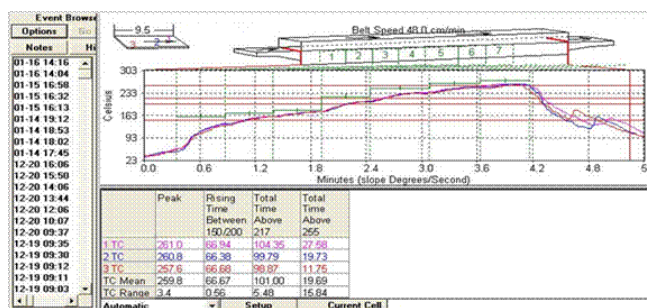


Figure 6

the most part, this cost was magnified in low-tech, low layer-count boards.

In general, the lower the layer count and technology, the higher the percentage cost increase that was incurred on behalf of the

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185HR - Laminate Properties

Property	Units	FR406	Competitive Phenolic FR-4s	185HR
Tg, DSC	°C	170	>170	>170
Td, 5% (TGA-ASTM)	°C	300	340	340
CTEz-axis (50-260C)	%	4.0	2.7 - 3.5	2.7
T-260	Min.	10	>30	60
T-288	Min.	>2	>10	>15
Dk, 100 MHz	-	3.91	-	4.19
Dk, 1 GHz	-	3.86	-	4.07
Dk, 2 GHz (Bereskin)	-	3.83	4.0 - 4.8	4.04
Dk, 5 GHz (Bereskin)	-	3.81	3.9 - 4.8	3.92
Dk, 10 GHz (Bereskin)	-	3.81	3.9 - 4.7	3.92
Df, 100 MHz	-	0.0134	-	0.0155
Df, 1GHz	-	0.0171	-	0.0188
Df, 2 GHz (Bereskin)	-	0.0177	0.019 - 0.025	0.0195
Df, 5 GHz (Bereskin)	-	0.0182	0.021 - 0.26	0.0229
Df, 10 GHz (Bereskin)	-	0.0182	0.022 - 0.027	0.0230
UL	-	FR-4	FR-4	FR-4, Family with 370HR

Dk Df data at 54 % resin

185HR Product Attributes

- Tg >170 C
- Td 340 C
- CTE z-axis 50 to 260 C - 2.7 %
- Lead Free Assembly compatible
- IPC 4101 C Slash Sheets / 21 / 24 / 26 / 98 / 99 / 101 / 126
- UL Family with 370HR
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- Stocked material in NA for Quick Turn requirements



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user. This has a great impact since, by volume, 2-8-layer boards account for a high percentage of mainstream PCB purchases.

As an illustration, let's consider a simple 4-layer board priced at domestic high volume.

Characteristic	SnPb Cost	Pb-Free
Base Board Price (10" x 6")	\$12.00	\$12.00
Final Finish	SnPb HASL: \$0	ENIG: \$ 4.50
Laminate	/21 FR4: \$0	/129 FR4: \$ 2.00
Total Cost	\$12.00	\$16.50
% Increase	0.0% - baseline	54%

Figure 7

Proposing a lead-free alternative buildup with less than 10% net cost added may evoke skepticism; however, here is such a proposal:

Characteristic	SnPb Cost	Pb-Free
Base Board Price (10" x 6")	\$12.00	\$12.00
Final Finish	SnPb HASL: \$0	SN100CL: \$ 0.50
Laminate	/21 FR4: \$0	/101 or /121 FR4: \$ 0.40
Total Cost	\$12.00	\$12.90
% Increase	0.0% - baseline	7.50%

Figure 8

IPC-4101/101 and /121 laminates have been largely ignored in the North American market, perhaps because they are viewed as too risky for such an extreme process as lead-free assembly.

We commissioned 1000-hour thermal cycling testing between -40°C to +125°C based on the following ramp and dwell rates:

1000-Hr Thermal Cycling Test	
-40°C to +125°C	5 minutes
Time @ +125°C	25 minutes
+125°C to -40°C	5 minutes
Time @ -40°C	25 minutes

Figure 9

The total time for each cycle is one hour, with 1,000 such cycles comprising the total test.

The test vehicle is an 8-layer daisy chain coupon with the following hole-size characteristics:

Drilled Hole Size	Finished Hole Size
8 Mils	6 Mils
10 Mils	8 Mils
12 Mils	10 Mils
14 Mils	12 Mils
16 Mils	14 Mils

Figure 10

The test vehicle was conditioned by processing three times through a lead-free reflow profile and then submitted for thermal cycling. Following is a chart displaying the number of failures by finished via diameter at each measurement interval. Failure is established if the resistance between endpoints of a specific via diameter daisy chain increases more than 10%.

Test Vehicle Failures (marked endpoint)					
FHS	0 hr	336 hr	612 hr	750 Hr	1008 Hr
0.006	0	10	11	11	11
0.008	0	0	2	4	7
0.01	0	0	0	0	0
0.012	0	0	0	0	0
0.014	0	0	0	0	0

Figure 11

Note that the test vehicle was fabricated with little pre-engineering with regard to drilling and desmear parameters. Based on this and the test results, we can easily establish that this material has a wide processing window and that there should be little concern to use this material type down to a 10-mil finished via size for high-reliability applications. The test parameters used were for on-engine applications.

OEMs can determine what cycling temperatures and number of cycles best fit their applications, which may increase or decrease the applicability window of this particular class of materials.

Regardless of the work involved in qualifying this third grouping of materials, the cost

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savings could be well worth the added effort of reopening the book of lead-free capable materials in most organizations.

Conclusion

Advancements in lead-free materials are not necessarily restricted to the materials themselves. Rather, they often develop in our knowledge base of the characteristics and performance criteria of the already available library of materials in the marketplace. This is truly the low-hanging fruit. **PCB**



Yash Sutariya is vice president of corporate strategy at Saturn Electronics Corporation (SEC) and owner/president of Saturn Flex Systems, Inc. (SFS). SEC is a high-mix, medium-to-high volume diversified supplier offering a wide range of manufacturing capabilities that serve the industrial controls, telecommunications, aerospace and power supply industries.

IPC: How Environmental Regs Affect your Business

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IPC's Tony Hilvers reflects on the 10-year partnership between IPC and HKPCA, and discusses the effect of non-technical aspects of RoHS, REACH and conflict metals on our businesses.



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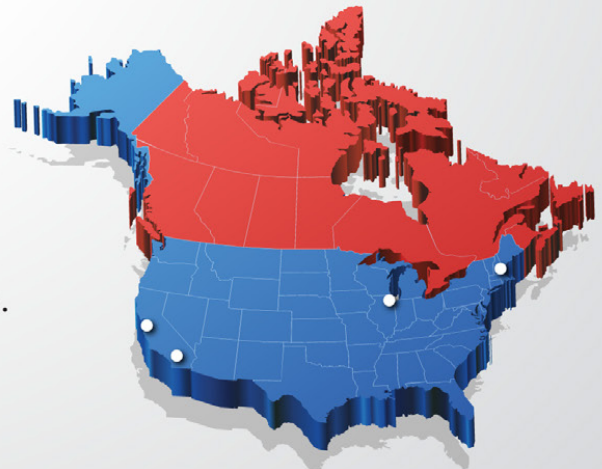
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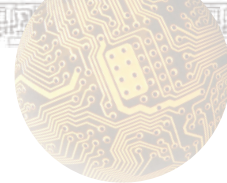


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Advances in Copper Plating, Part A

By Karl Dietz

KARL DIETZ CONSULTING, LLC

Summary — Acid copper (electroplating) for electronic applications has seen many advances over the decades. The next few Tech Talk columns will cover more recent innovations and evolutionary improvements.

Acid copper (electroplating) for electronic applications has seen many advances over the decades, which include the introduction of the high through bath with lower copper and higher acid concentration, the development of proprietary organic additives for improved leveling, grain refining and ductility, improved bath control methods such as CVS and more. The next few Tech Talk columns will cover more recent innovations and evolutionary improvements. The order in which they are presented is somewhat arbitrary and is not meant to suggest order of importance.

Inert Anodes

Copper plating involves the formation of metallic copper at the cathode through electrochemical reduction of cupric ions, i.e., the addition of electrons to the metal cations. Metallic copper that serves as a source of such copper ions and also provides a source of electrons, has traditionally functioned as soluble anodes in acid copper plating baths. Soluble in this context means that copper metal dissolves

as it is electrochemically oxidized. Herein lie inherent disadvantages associated with soluble anodes:

- As copper dissolves, shape, size and specific surface area of the anode change, affecting the current density and current distribution and thus the uniformity of the copper deposit. For good current distribution, the soluble anode should have a flat surface that is positioned parallel to the board (cathode) and has about the same size as the cathode. Even

if copper is often replenished, e.g., in the form of nuggets in a titanium basket, these ideal conditions are never quite achieved.

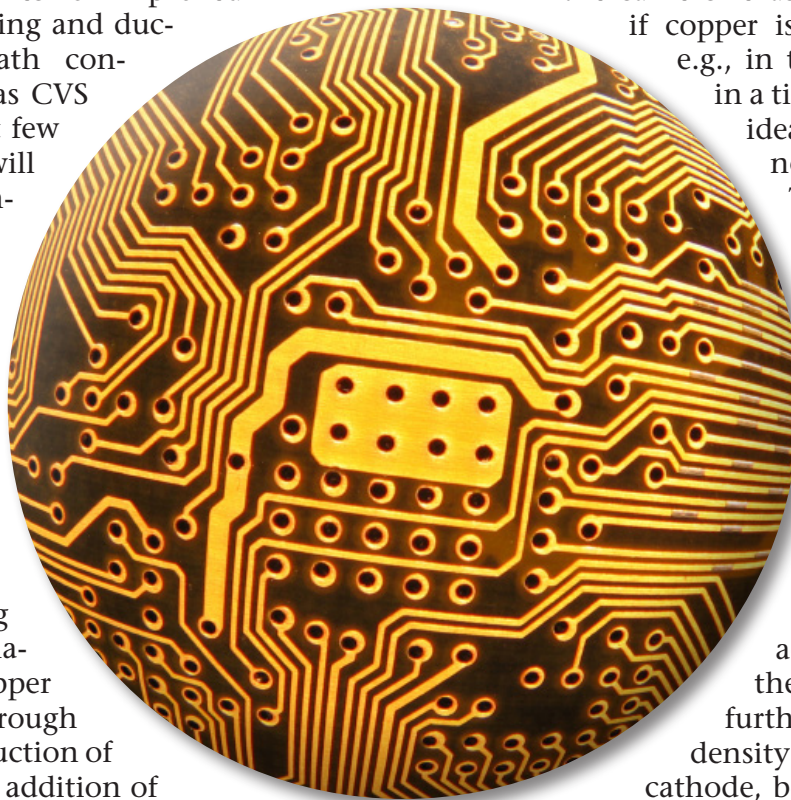
To improve the effective current distribution at the cathode surface and to smooth out localized field strength differences, the anode is typically spaced at a good distance from the cathode.

This, of course, adds to the size of the plating line. To

further improve current density uniformity at the cathode, boards can be moved

horizontally or vertically during

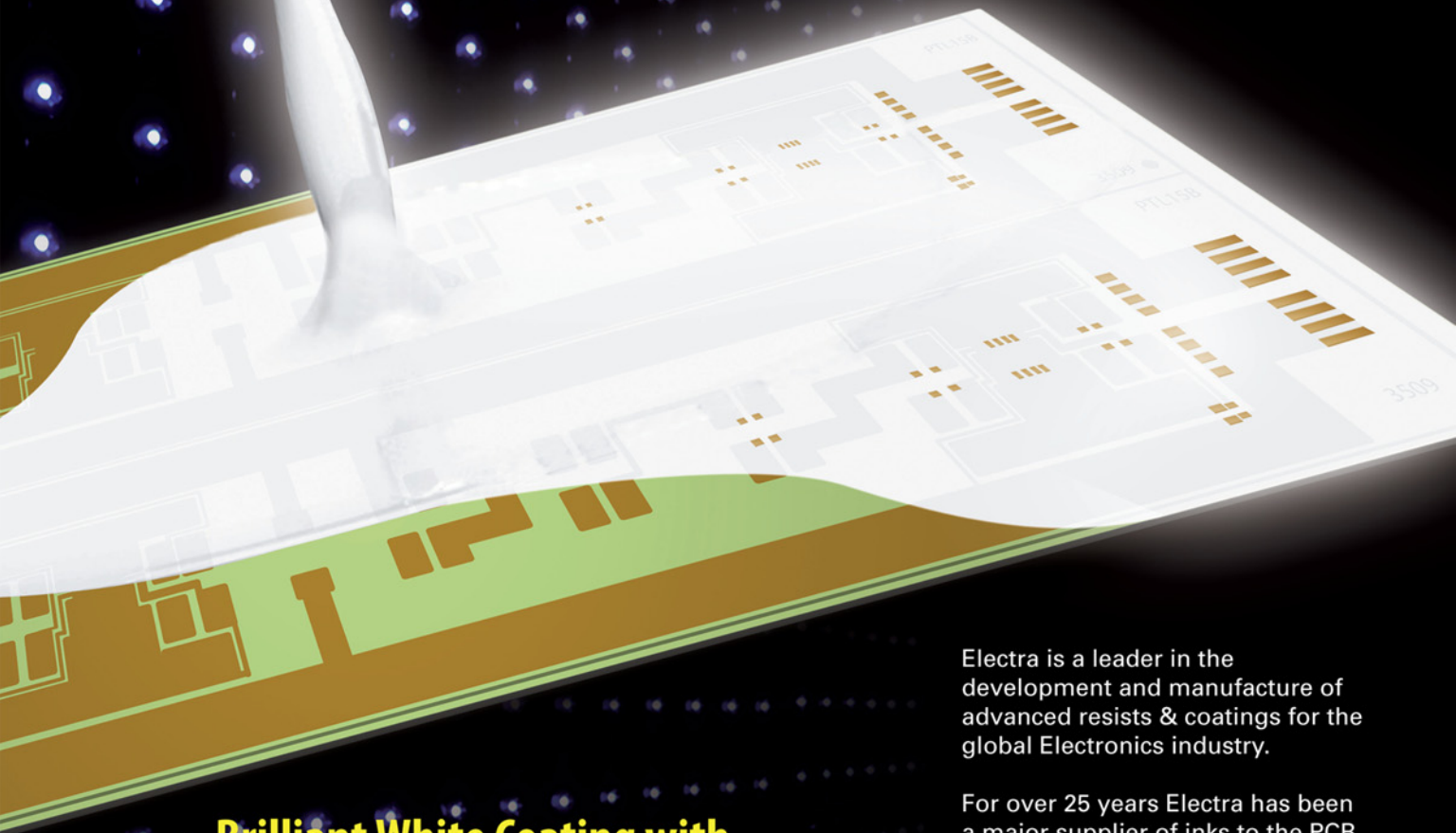
the plating process through different plating cells or plating segments of the line. This movement will average out any anode shadowing, i.e., a pattern of uneven copper deposition due to the fixed position of the board relative to



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the anode's imperfect primary current distribution.

- To dissolve anodic copper, one has to plate at anode current densities of less than 30A/ft² (about 3.3A/dm²) which affects productivity. At higher current densities, anode polarization increases and surface oxides form, causing passivation. While the anode surface begins to passivate, the current shifts to anode areas that are less passivated, making it difficult to maintain good current density distribution.

- To facilitate the dissolution of the copper and to avoid a high polarization potential and ultimate passivation of the anode surface, a special grade of "phosphorized" copper is being used, adding to the cost. In addition, a certain level of chloride ions (typically about 50ppm) in the plating solution needs to be maintained to assist the process. Dissolution of the copper creates residues (sludge) that need to be contained in anode bags to avoid contamination of the plating solution that can lead to plating nodules. These anode bags need to be pre-treated to remove potential bath contaminants and the bags need to be periodically replaced.

- By using insoluble anodes, one avoids the above-mentioned problems associated with soluble anodes, but other potential problems loom which need to be addressed. Basically, the insoluble anode supplies electrons as oxygen is formed from water. Copper ions need to be replenished in a separate step, in a module that is connected to the plating chamber. Insoluble anodes are typically made of a titanium mesh that is coated with mixed metal oxides (MMOs). For copper plating, one uses iridium oxide and tantalum oxide; ruthenium oxide and titanium oxide are found in non-copper applications. The MMO coating may deteriorate after long use, in which case it is removed and the titanium mesh is re-coated.

Plating Blind Microvias and Through-holes Shut (filling microvias from the bottom up and filling through-holes from the center)

The benefits of filling vias can be summarized as follows:

Via fill processes can be used to create stacked vias in HDI boards and IC substrates. Added advantages include improved planarity, better thermal conductivity of the vias and the ability to place solder bumps directly on top of a microvia connection. This via fill technology can not only be applied to blind microvias, but also for filling through-holes (Ref.: Blind Micro Via and Through Hole Filling for Thin Core and Flexible Base Materials, Stephen Kenny, The Board Authority, 2006, pg. 35). Figure 1 shows the early stage of plating a through-hole by a via fill process.

There are several parameters that affect the via fill performance of a plating process:

- agitation
- copper/ acid ratio
- current density
- microvia aspect ratio and diameter
- organic additive system

Regarding agitation, impingement jetting of the plating solution is preferred over air sparging. Changing to a higher copper/acid ratio, compared to a standard high-through bath, yields improvements. Going to lower current densities, as expected, improves performance. Smaller diameter and higher aspect ratio microvias give better fill ratios than lower aspect ratio, large diameter vias. This result is somewhat counterintuitive, but can be explained by looking at the specially formulated organic additive systems for the via fill process (see discussion below).

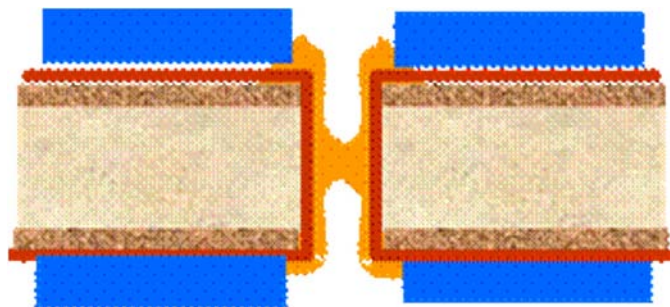
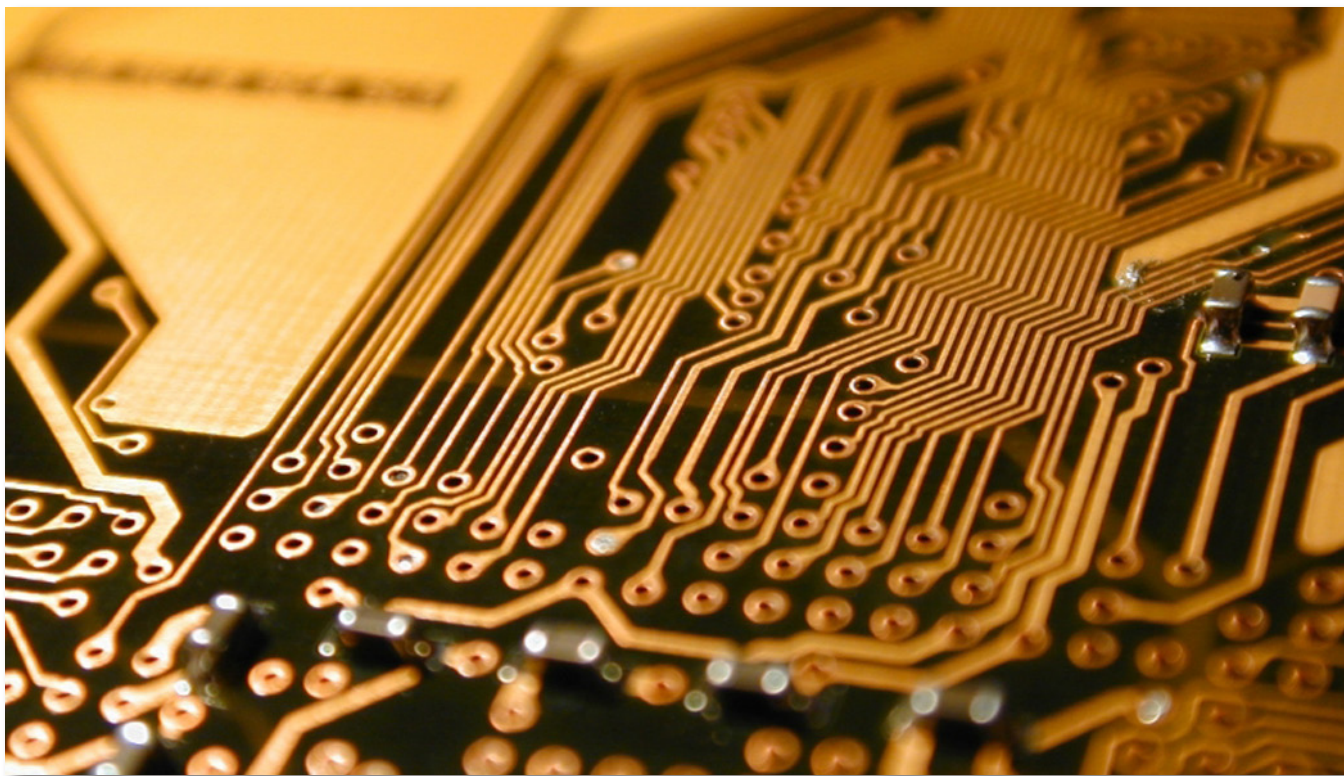


Figure 1: Plating a through-hole by a via fill process.



The functions of plating additives are fairly well understood. Polyglycols, such as polyethyleneglycol (PEG), act as inhibitors and small amounts of chloride enhance the inhibiting effect of PEG. Bis-(3-sulfopropyl)-disodium-sulfonate (SPS), other disulfides, thiourea and thiocarbamates act as accelerators. Quaternary nitrogen compounds act as levelers.

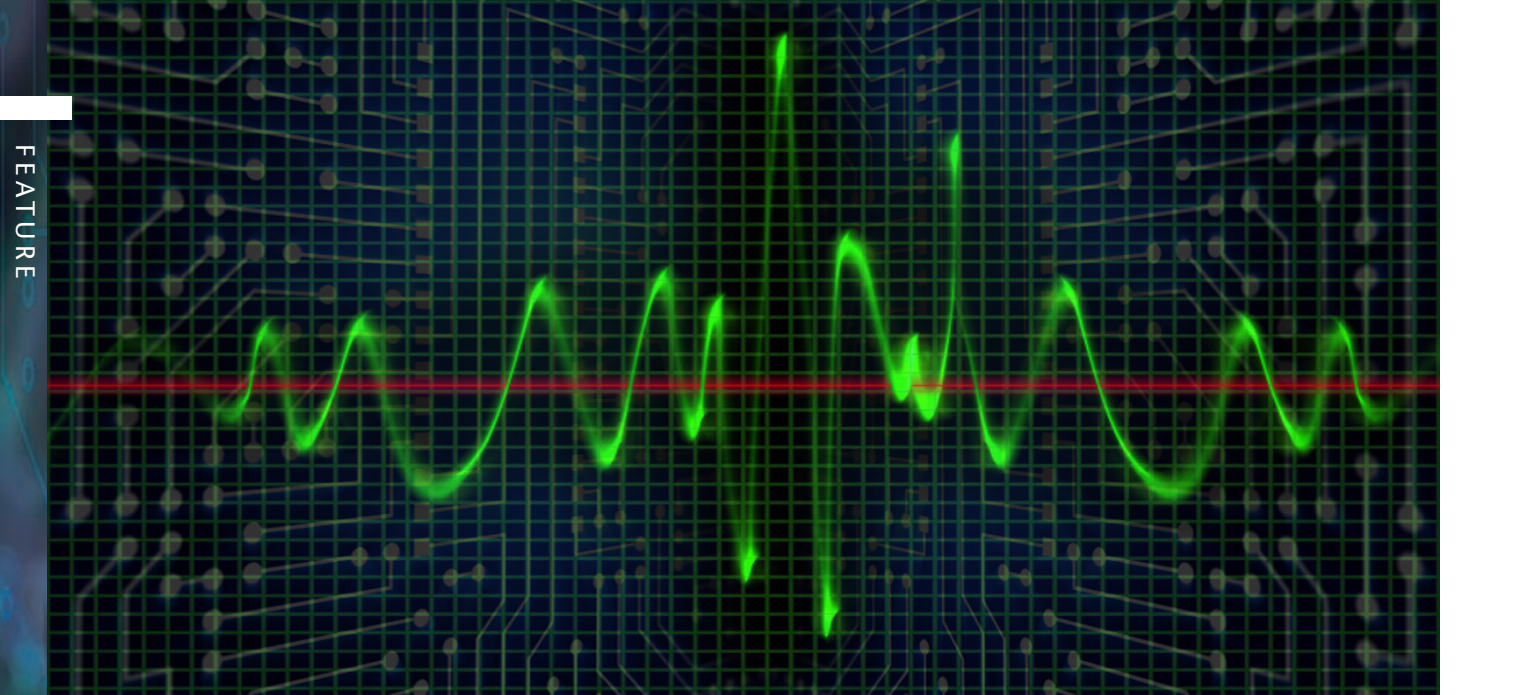
Landau studied in particular the role of PEG and SPS in the bottom-up via fill process. He points out that at the beginning of the plating process there are hardly any additives in the via hole to be adsorbed on the hole wall and hole bottom surfaces because of the low liquid volume to surface area ratio in the via. PEG adsorbs faster than SPS, but there is very little PEG to cover the hole walls and bottom.

However, on the surface, the PEG supply is plentiful and the fast adsorbing PEG inhibits plating on the surface. In contrast, practically all additives that end up on the hole surfaces have to diffuse into the hole. Since SPS diffuses faster than PEG, it reaches the bottom of the hole first and once adsorbed, forms a barrier against PEG adsorption. The slower-diffusing PEG slowly builds up on the upper part of the

hole wall near the surface, acting as a plating inhibitor while the dominant SPS at the bottom of the hole accelerates plating. Landau found that the relative concentrations of PEG and SPS have an influence on how well the bottom-up plating performs. His findings also explain the effect of via diameter and aspect ratio on the bottom-up plating performance. Wider via diameters mean a less favorable volume to area ratio in the hole which means there is more PEG initially available to adsorb on the via bottom. A high-aspect-ratio via results in a greater concentration gradient in the hole cylinder between a slowly diffusing additive such as PEG and a faster diffusing additive such as SPS, thus favoring bottom-up plating. **PCB**



Karl Dietz is president of Karl Dietz Consulting LLC. He is offering consulting services and tutorials in the field of circuit board and substrate fabrication technology. Contact Dietz by e-mail at kardietz@earthlink.net or phone (001)- 919 870 6230.



Circuit Materials and High-Frequency Losses of PCBs

by John Coonrod

ROGERS CORPORATION

ADVANCED CIRCUIT MATERIALS DIVISION

SUMMARY — *As PCB technology advances, concerns for high-frequency electrical losses are becoming prevalent. There are many aspects to consider regarding losses with circuit design, fabrication and configuration. There are also many issues to consider, with circuit materials playing a critical role.*

The PCB industry is diverse, from dynamic flexible circuitry that is as thin as a human hair, to multilayer backplanes which could be used as a diving board. Although that comparison is a little extreme, great diversity exists in the PCB industry regarding experience with electrical losses as well. The sector of the PCB industry that caters to microwave applications is accustomed to loss issues. Many other sectors of the industry probably have a mix of experience on this topic.

Recently, there have been more requirements for PCBs to have loss testing performed as an outgoing quality check. This is similar to what has been done in the past with controlled impedance boards requiring testing to ensure

the circuit is within an impedance tolerance prior to shipping the product. However, there are vast differences between testing for impedance and loss testing. Additionally, materials and circuit fabrication issues regarding losses are significantly different than impedance concerns.

In general, impedance issues are related to the dielectric constant (Dk) of the material, the precision of the conductor-etched features and the thickness of the PCB in electrically critical layers. There are more issues to consider with losses. These include dissipation factor (Df) of the material, copper surface roughness, precision of the conductor etched features, conductor length and impedance mismatches. The impedance mismatch concern refers back to the issues for impedance control; therefore loss issues have their own list combined with impedance issues. Additionally, and depending on the circuit construction, the plated finish and/or solder mask applied to the conductors can also have an impact on losses.

Electrical losses for a PCB design become important when the circuit is no longer acting like a simple interconnect, but is actually a transmission line. This is defined as the circuit conductor length being longer than one-fourth the wavelength and for a 3GHz signal that is about

“ Electrical losses for a PCB design become important when the circuit is no longer acting like a simple interconnect, but is actually a transmission line. ”

a 2-inch length, subject to the Dk of the materials and circuit construction. Actually, a better rule of thumb would be to assume the circuit is acting like a transmission line when the length is 1/10 of the wavelength. In terms of high-speed digital, the same definition applies, but it is typically related to the conductor length in terms of propagation delay and with regard to rise time.

Insertion loss is the term generally used to refer to total loss of a RF system. When looking at the PCB only, the insertion loss is comprised of four components of loss which include dielectric, conductor, leakage and radiation. Radiation loss is not going to be discussed; however, it can be an issue for some microstrip configurations. Leakage loss is generally not an issue with most PCB applications, where the substrate has very high resistivity values. Dielectric loss is mostly related to the Df of the material; however, some anomalies in the circuit fabrication process can have an impact on this subject. Conductor loss has several components of interest regarding materials and PCB fabrication, which will be expanded on in the remainder of this article.

Assuming radiation and leakage losses are not concerns, the two components making up insertion loss are dielectric loss and conductor loss. The ratio of dielectric loss to conductor loss can be important to understand for a particular construction, as it can vary based on construction and frequency. To illustrate this concept, several models were run on a common circuit construction as well as circuits tested for loss. The circuit construction was a simple microstrip transmission line and the software model used was MWI-2010 [1]. The microstrip circuit is a double-sided, non-plated through-hole using RO4350B™ copper clad laminate with ½ ounce ED copper. Three different substrate thicknesses were chosen to show the difference in total loss and their components. Additionally, circuits were tested for insertion loss and that data is shown in Figure 1.

The information shown in Figure 1 tells quite a bit about insertion loss. To begin with, it can be seen that the measured data (purple) compares relatively well to the total loss (green) of the model. The model has the ability to break

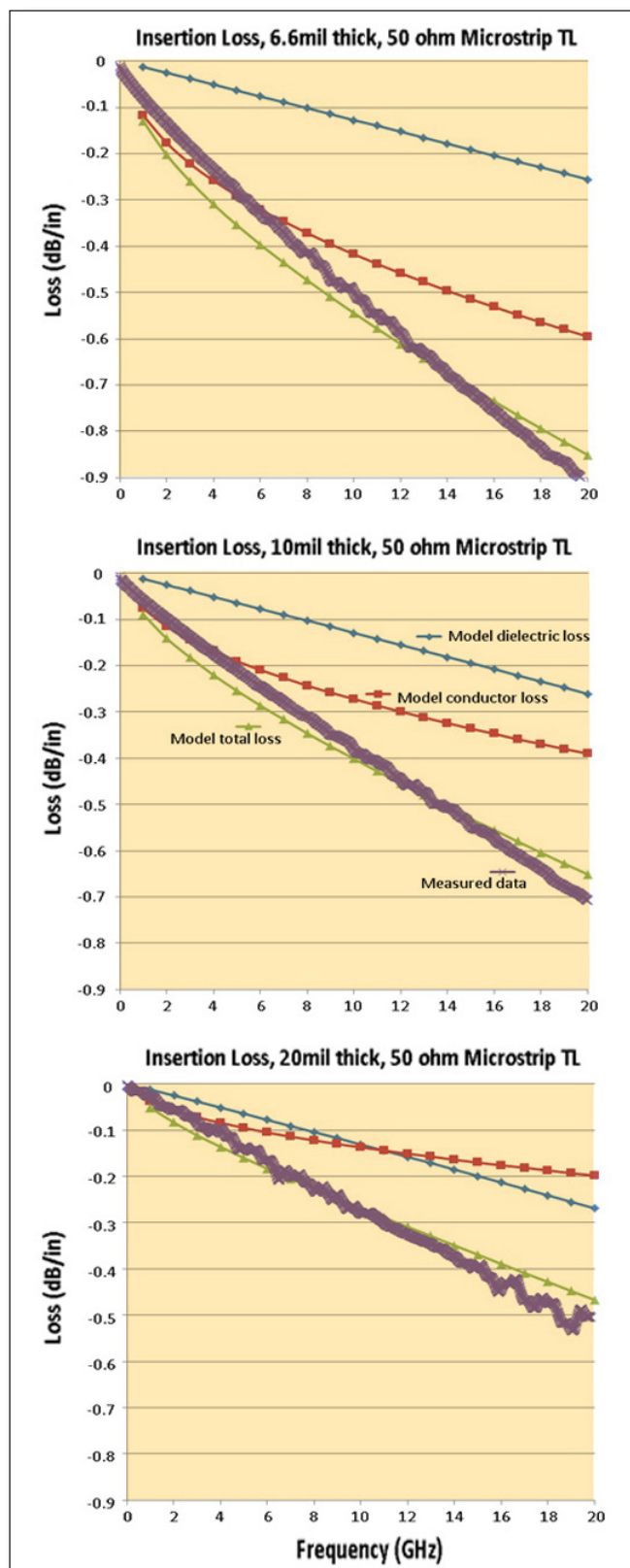
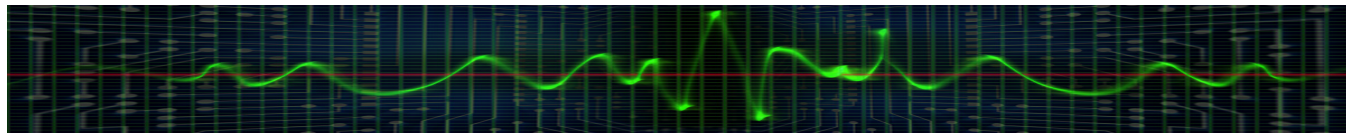


Figure 1: Insertion loss comparisons of microstrip transmission line circuits using different substrate thickness.



out dielectric (blue) and conductor loss (red) separately. Looking at the ratio of conductor and dielectric loss at 10 GHz on the 20mil circuit, there is about a 1:1 relationship. The dielectric and conductor loss are both about -0.14 dB/in at 10GHz, and added together, this gives us the total loss. The 10mil circuit shows that the conductor loss is about double the dielectric loss and at 10GHz they are -0.27 dB/in and -0.13 dB/in, respectively. The 6.6mil circuit shows that the conductor loss is dominating the overall insertion loss and at 10 GHz, it is about -0.42 dB/in and the dielectric loss is -0.13 dB/in.

When comparing circuits of different thicknesses, it is obvious that the trend of thinner circuits brings more insertion loss. That is correct for several reasons, one of which is controlled impedance. All of these circuits were 50 ohm transmission lines; when

a thinner substrate is used, a narrower conductor must be used to maintain the 50 ohm structure. The narrower conductor will have higher conductor losses and overall insertion loss. The RO4350B circuit material that was used here is considered a low-loss material with a Df of 0.0037. It can be seen in Figure 1 that the dielectric loss is relatively unchanged with the thickness variation of the circuits. In reality, there are some small changes in dielectric losses with these circuits, but it does show that the effects of conductor loss are important when using a thinner substrate. The copper clad laminate in this study used a high profile copper and it is known [2] that a rough copper surface will increase conductor losses.

To illustrate the effects of the copper surface roughness, circuits were made with the same substrate, but varying the copper type, which has a different surface roughness. The 10mil

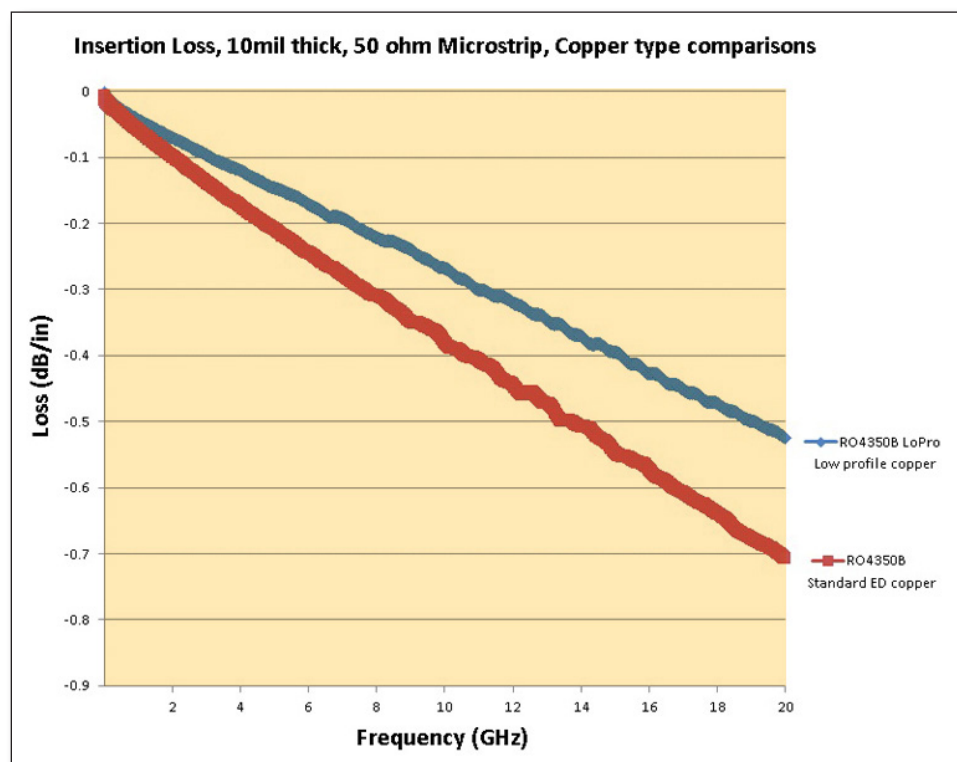


Figure 2: Insertion loss comparison of 10mil thick microstrip transmission line circuits using the same substrate, but with different copper.

circuit was used where the conductor losses are about double the dielectric losses (Figure 1). The curves in Figure 2 show the results of insertion loss on circuits using the same substrate, but with the copper having a significantly different surface roughness.

As shown in Figure 2, the circuits using the material with smoother copper, RO4350B LoPro™ laminate have much lower insertion loss. This is mostly due to the smoother copper surface of the LoPro technology. The LoPro technology also yields a copper clad panel with slightly lower Dk than the standard RO4350B laminate, allow-

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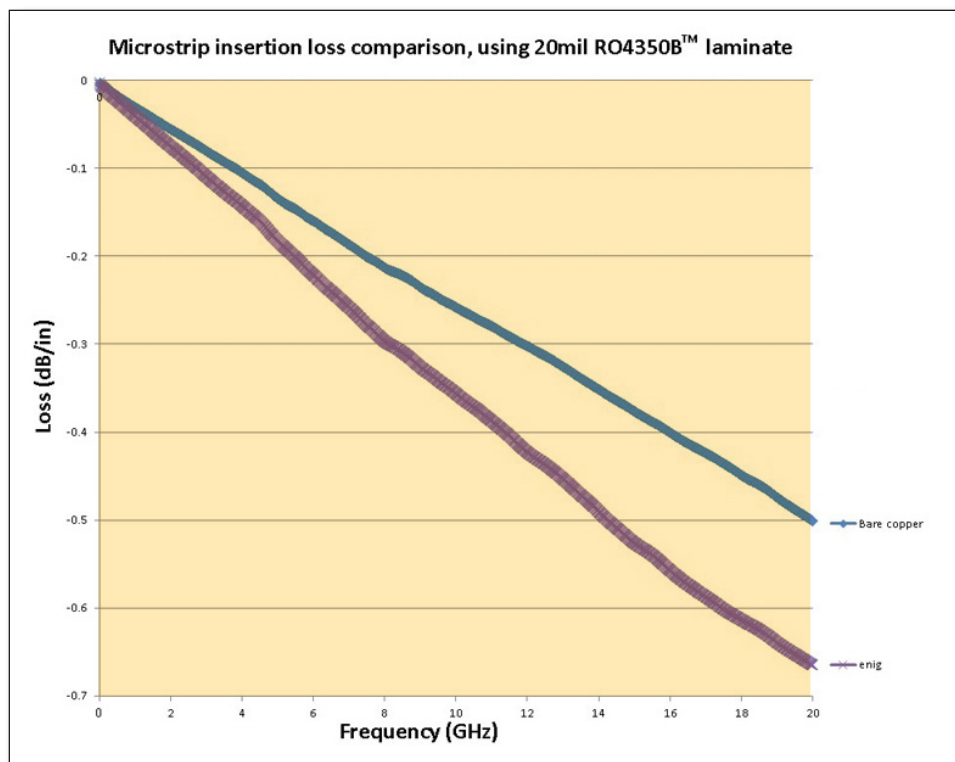


Figure 3: Insertion loss comparison of 20mil microstrip transmission line circuits using standard RO4350B laminate and comparing performance of bare copper to ENIG finish.

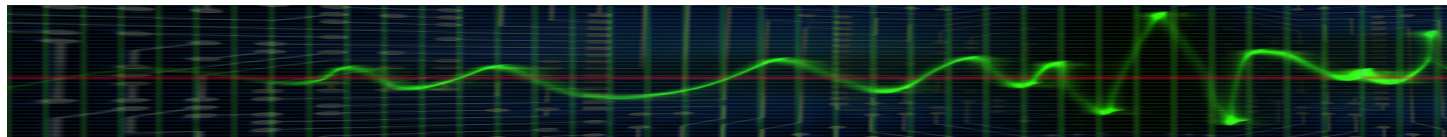
ing a somewhat wider conductor to maintain 50 ohms. The copper surface roughness used for these two laminates are 2.8 microns for the standard RO4350B laminate and 0.6microns for RO4350B LoPro circuit materials; the roughness measurements are in terms of RMS (root mean square) .

Besides copper surface roughness, there are other issues which can impact conductor losses. For microstrip or coplanar transmission line circuits, the addition of some plated finish can cause more losses. ENIG (electroless nickel immersion gold) is a common finish with many proven good attributes; however, it can cause more conductor losses. The losses due to ENIG can be difficult to quantify for many reasons. There are several different ENIG processes and each has their unique properties. Some of the

ENIG processes appear to have less impact on conductor losses than others. Additionally, the losses due to ENIG are frequency-dependent, in the sense that nickel is much less conductive than copper and at the right frequencies much of the nickel could be used by the RF current. At higher frequencies, less of the conductor is used and if the skin depth current is mostly using the nickel layer, the conductor losses will increase. To compound this issue, the nickel layer has some natural thickness variation. As an example, two exact PCB constructions can have significantly different loss performance due to the variation of

the nickel. Figure 3 shows a comparison using the 20mil circuit from Figure 1, with and without ENIG. Insertion losses are shown.

As previously mentioned, dielectric losses are mostly due to the Df of the substrate. It has already been shown that when the laminate is thinner, the dielectric losses are less significant, however that data has been shown with a low-loss substrate. A higher-loss substrate such as FR-4 will certainly have higher losses and as frequency increases the losses will increase significantly more than the low-loss material shown here. The RO4000® circuit materials have been formulated to be very stable over a wide range of microwave frequencies and that is why the dielectric losses do not change much on the different thickness circuits shown in Figure 1. In contrast, if a high-loss material such as FR-4 is used, that will show much higher losses and the



losses will likely increase with frequency in a non-linear manner.

As a summary illustration, an insertion loss comparison is shown in Figure 4, displaying results of several 20mil microstrip transmission line circuits using very different substrates. The RO4000 circuit materials discussed thus far will be shown along with a high Tg FR-4 and a ceramic filled PTFE substrate (RO3035™ circuit materials).

It can be seen from the data that insertion loss can be influenced by several different aspects. A thinner circuit will have more conductor losses and the choice of copper is more important. The plated finish can also have an impact on losses. For an application where minimizing losses is critical, then typically a very low-loss substrate would be used in combination with a very smooth copper. This was shown in Figure 4 with the RO3035 laminate using a rolled annealed copper. **PCB**

[1] MWI-2010 software is a free download from Rogers Corporation, Technology Hub. This software performs simple impedance and loss predictions using the Hammerstad and Jensen models: E. Hammerstad and O. Jensen, "Accurate models of microstrip computer aided design", 1980 MTT-S Int. Microwave Symp. Dig., May 1980, pp. 407-409. The copper roughness model in this software is limited to frequency and is from Morgan: S. P. Morgan, "Effect of surface roughness on eddy current losses at

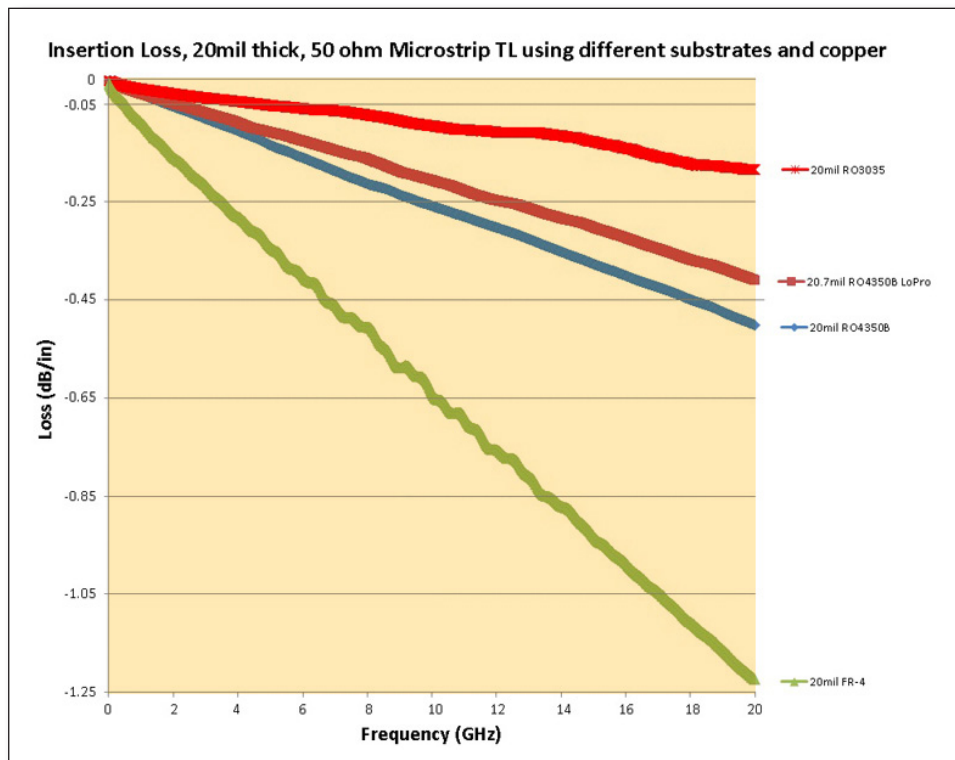


Figure 4: Insertion loss comparison using several different substrates for 20mil thick microstrip transmission line circuits.

microwave frequencies," J. Applied Physics, p. 352, v. 20, 1949.

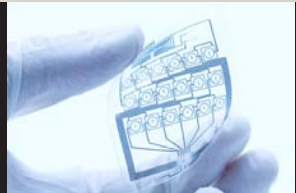
[2] J.W. Reynolds, P.A. LaFrance, J.C. Rautio & A.F. Horn III, "Effect of conductor profile on the insertion loss, propagation constant, and dispersion in thin high-frequency transmission lines", DesignCon 2010.

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John Coonrod is a market development engineer for Rogers Corporation, Advanced Circuit Materials Division. About half of his 24 years of professional experience has been spent in the flexible PCB industry doing circuit design, applications, processing and materials engineering. Coonrod's regular column, Lightning Speed Laminates appears bi-monthly in The PCB Magazine.

Top Ten Most-Read Flex007 Highlights This Month



New Path to Flex and Stretch Electronics

Imprinting electronic circuitry on flexible and stretchable backplanes promises to revolutionize a number of industries and make "smart devices" nearly ubiquitous. From solar cells to pacemakers, the list of smart applications for plastic electronics is both flexible and stretchable. First, however, suitable backplanes must be mass-produced in a cost-effective way.

Flex Technology Trends with All Flex

Dave Becker, Director of Sales and Marketing for All Flex, sits down with Editor Andy Shaughnessy to show the new types of flex his company has been developing. He also discusses the overall business climate in the flex industry.

Circuits, LLC Achieves UL 94V-0 Certification

Circuits, LLC announced that the company has received official notification from Underwriters Laboratories (UL) that it has been awarded 94V-0 certification for Type 3 and Type 4 multilayer flex and rigid-flex PCBs manufactured at the site.

MFLEX Beats Expectations for Preliminary Fiscal 2012 Sales

"We expect our net sales results to exceed the high end of our previous guidance range as the supply chain shortages from the flooding in Thailand improved throughout the quarter. We also saw an increase in shipments to our largest key customer," said Reza Meshgin, CEO of MFLEX.

Top 10 Countdown: Most-Read Flex Stories of 2011

As 2011 came to a close, I-Connect007 editors took a look back at the year's top stories. Here's our "Top 10 Countdown" of the most-read items from the Flex007 and the Flex007 Weekly Newsletter, including reports of significant growth in the flex circuit market in 2011. IPC forecasts the flex boom to continue — reaching \$12 billion in global annual sales by 2015.

Taiwan Flex PCB Makers Post December Revenues

Flexible PCB makers Career Technology and Flexium Interconnect had December consolidated revenues of NT \$1.035 billion (U.S. \$34.2 million), increasing 4.8% on month, and NT \$927 million, up 13%, while fellow maker Zhen Ding Technology Holding suffered a sequential drop of 3.5%.

Ichia to Ramp-Up Flex PCB Capacity this Year

Ichia Technologies plans to expand its production capacity by 50% for flexible PCBs used in smartphones, tablets and other consumer technology products this year.

Smaller, Smarter Electronics Using Flex Assemblies

Jay Desai of MFLEX explains how effective hardware design optimization using flex assemblies and supply chain reduction with a modularization approach can lead to superior 3D packaging solutions enabling thinner, smaller and lighter devices.

Amphenol Reports Strong Q4 Results

Amphenol President and CEO R. Adam Norwitt stated, "We are pleased to report strong performance in a very challenging environment in the quarter with fourth quarter sales of \$949 million, operating income margin of 18.5% and earnings per share of \$.73."

Flexible PCB Production Value in Taiwan to Rise

Taiwan-based flexible PCB makers' combined production value as a percentage of global total is expected to reach 15-20% in 2012, up from 10-15% currently, according to industry sources.

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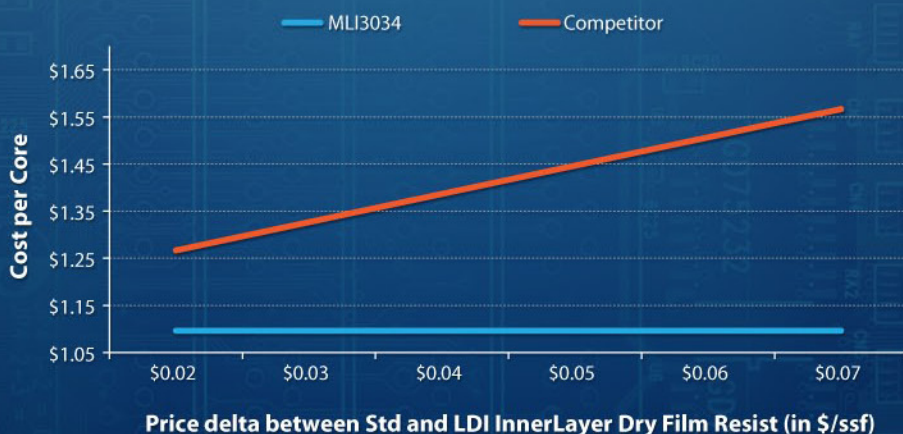
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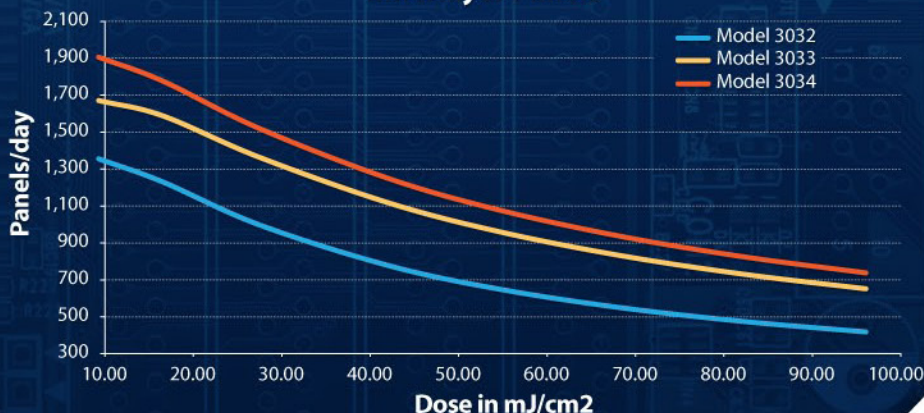
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Comparative Throughput for 18" x 24" Innerlayer Panels



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by **Gray McQuarrie**
GRAYROCK & ASSOCIATES



SUMMARY — *Are your engineers making your company's products great? If not, you have a DAM problem. In order to break this DAM you need to learn what Steve Jobs learned: You might not have a horrible manager out of control, but a true management genius that few people understand even today.*

Your work is crap! Could you imagine saying this to your engineers face to face? According to Walter Isaacson, who wrote the recently released biography Steve Jobs, Jobs said this very thing many times to his brilliant engineers working on the first Mac. It has been written that in the early days of Apple, Steve Jobs was such a horrible manager that he had to be fired. When he came back to Apple he was a much better manager.

I don't agree with this proposition. My contention has always been that behaviors drive results. The quality of the output by the original Mac team is undeniable. So, if it is true that behaviors lead to results, then it must be true that

Jobs' behavior wasn't bad, but actually good. Does this mean you should start telling your engineers that their work is crap? Not necessarily, and not before you understand what Jobs was doing.

Many of my columns have covered technical problems, but technical mastery will never be enough to solve a DAM problem. What is a DAM problem? Observe your engineers. Are you getting the work you need out of them? Sure, your engineers are working, but not on anything that will generate much growth or change. It is likely they are just maintaining the status quo. For example, they may be helping an operator with a process, or calling up a vendor about returning product, or looking up a machine cost, thinking the company will never pay for it. Your company is stuck. Being stuck like this is what I define as a DAM problem. DAMs block flow. How do you get rid of the DAM? You have to understand how and why the DAM is there before you can wreck it.

Too many engineers have at least three DAMs: the ego DAM, when they don't ask for help; the learning DAM, when they think they know it all, but don't; and, the My Precious DAM, when they are extremely territorial and demand to work in total isolation when, in fact, just the opposite is required. When you have all three of these DAMs operating, you are dealing with a self-righteous, perfectionist jerk. The DAM problems this creates are blocked productivity, discovery and growth.

Jobs knew engineers were difficult to manage and he had to shoot a cannonball in order to wreck these DAMs. That cannonball he used was, "Your work is crap." Jobs used a process to manage his engineers. Few people understand process like the author of *The Hero's Journey*, Joseph Campbell, who said, "Out of perfection





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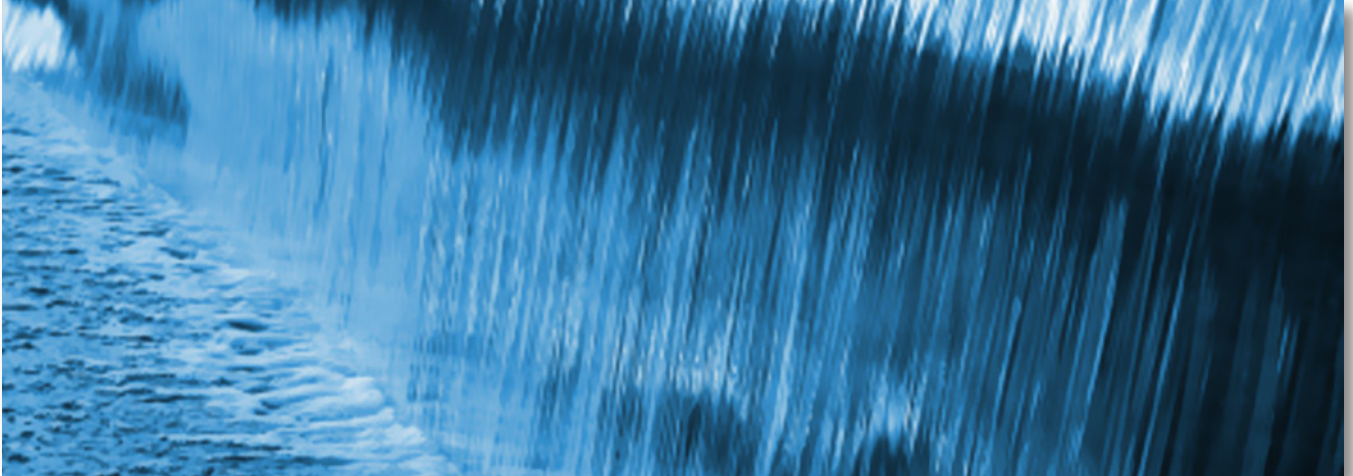
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nothing can be made. Every process involves breaking something up.”

Jobs could not launch his cannonball if he had a “feelings DAM.” If you have a feelings DAM, because you want to be liked, then you have blocked purpose. Jobs had very strong feelings about making great products. However, the feelings of his engineers were not his concern. If they were mad at him for being demanding and telling them their work was crap, so be it. If personnel came knocking on his door and said, “You can’t treat people this way,” he would say, “You’re right,” and continue telling his engineers their work was crap. He wanted a great product and he was going to get it. Jobs refused to deviate from his purpose.

Many people have said Jobs was a great visionary, but it is really tough to find anyone who would say he was a great manager or a great leader. Yet, I don’t think Jobs was a great visionary. Others brought great ideas to him. What made him great was his ability to motivate his engineers to make the vision a reality. After all, the graphical user interface was created by Xerox. They just couldn’t implement the vision. Saying “Your work is crap” was Jobs’ way of motivating his engineers to make the vision a reality. So, what was his process for managing his engineers?

First, Jobs burned the boats. Hernando Cortez burned the boats when his conquistadors stepped foot in Mexico. Jobs burned the boats by renouncing the Apple II. The Mac would be different in every way, shape and form. He

burned the boats by making sure everyone understood their careers were intimately tied to the success of the Mac. They worked on nothing else but the Mac. If the Mac didn’t make it, they wouldn’t make it.

Second, Jobs created transparency. You never knew when he was going to step into your work area and ask what you were doing. There was absolutely no possibility of hiding or creating fluff and getting away with it.

Third, Jobs placed everyone in very close physical proximity. He could not guide the team if they were scattered. With everyone close by, everyone heard everything and everyone heard Jobs, regardless of whom he was talking to. This allowed them to work together when they chose to; with Jobs, they knew they had to.

Fourth, Jobs set a very high standard. Because he had such high standards and expectations, the engineers had to help each other and work together. They had to drop their ego DAM and ask for help. As a result, they all became much more productive. They couldn’t pretend they knew what to do, because what Jobs was asking for had never been done before. Consequently, their learning DAM broke and their minds were open, which created new discoveries. Because of the high standard Jobs set, his engineers had to allow others into their thoughts and share their ideas and knowledge. This wrecked their My

Precious DAMs, which accelerated everyone's growth.

Fifth, Jobs was the GPS and knew how to motivate people. He knew exactly where he was headed. Think of a kid who hides something while another kid keeps his eyes shut. The kid who had his eyes closed now opens them and has to find the hidden object by listening to the words, hot or cold. Jobs knew that it was painful for any engineer to hear that their work was crap. When he said "This is great," Jobs would generate so much pleasure that the entire team wanted to please him again. Jobs was charismatic, but it wasn't his charisma that drove the engineers. It was what he understood about people. Jobs understood that people run from pain and run toward pleasure. Jobs absolutely was a great motivator.

Sixth, Jobs created a strong tribe. Because he was often a threat with his "Your work is crap" statement, everyone learned to circle the wagons when Jobs appeared. This threat created the need for a strong tribe. A tribe protects its members and makes everyone more secure. This is what Jobs knew he needed. Much has been said about his telling an engineer that his idea was crap and coming back the next day and presenting this very same idea as his own. It sounds like he was a bit of a jerk; however, I believe the reason he did this was because he didn't want the engineers to slip back into their own individual silos. He didn't want them distracted by who did what and who deserved to get credit and who was most important. All of this is DAM thinking. All of this creates waste. Everything belonged to the tribe and the tribe existed to satisfy the product owner, Steve Jobs.

Seventh, he was the undisputed product owner. There was absolutely no ambiguity about what they were building and why. He met with his team all of the time. He communicated with the team all of the time. He evaluated their work all of the time. He took full accountability that his engineers would absolutely understand what he wanted and what he demanded.

Eighth, Jobs created a common enemy.

The common enemy for the Mac tribe was the Apple Lisa. Nothing would be more painful for the tribe than for the Lisa project to finish before the Mac. Every person's pride, significance and value were at stake. They would do anything not to be beaten. They absolutely knew Jobs was 100% committed to beating the Lisa team.

Ninth, Jobs created a transcendent purpose that went well beyond the walls of their building or Apple itself. They all wanted to be part of something great — something that would put a ding in the universe. Jobs relentlessly articulated this. Their work would leave a lasting legacy and they all wanted a piece of it. If you want to know what really motivates an engineer, look to the pyramids of Egypt.

If you want your engineers to make your products great, you shouldn't follow these nine items as a methodology, but rather as a construct. Moreover, you shouldn't try to copy Steve Jobs literally and tell your engineers that "Your work is crap." Take the ideas and experiment and then figure out what works for you. You will find that when you work closely with your engineers, all of you will come out the other side very different people because of the growth you all experienced. After all, "Every process involves breaking something else up."

For more information on how to motivate engineers, read *Change Your DAM Thinking*, as well as Ray Immelman's book, *Great Boss, Dead Boss*. **PCB**



Gray McQuarrie is president of Grayrock & Associates, a team of experts dedicated to building collaborative team environments that make companies maximally effective. McQuarrie is the primary inventor of the patent, Compensation Model and Registration Simulation Apparatus for Manufacturing PCBs. He has worked for AlliedSignal, Shipley, Photocircuits, Monsanto and others. For more information, e-mail McQuarrie at gray@grayrock.net.

Thermal Management Substrates

by Ian Mayoh and Mark Goodwin
VENTEC EUROPE LIMITED

SUMMARY — *The mechanical, thermal performance and cost considerations should be considered when selecting an appropriate insulated metal substrate material for a particular application.*

Over the last few years, there has been increasing interest in cost-effective thermal management of component-level electronic devices and substrates and, increasingly, thermally conductive printed circuits are becoming a solution of choice.

It is the intention of this paper to review the current status of thermally conductive printed circuit substrate options, in terms of performance, construction and processing, and future developments. With particular reference to insulated metal substrates, the paper will explore the mechanical, thermal performance and cost considerations to be taken into account when selecting an appropriate IMS material for a particular application. Furthermore, questions will be raised in terms of suitability for purpose and reliability considerations.

Firstly, consider the 10 essential trends that are providing the driving force for more effective thermal management:

- Miniaturization of MLB
- High performance
- HDI
- Embedded technology, within MLB
- Flexible circuits
- Lead-free
- Halogen free
- Light-emitting diodes (LEDs)
- Optoelectronics
- Printed electronics

The need to dissipate heat from electronic modules and assemblies has, over the years, become increasingly important; this is not only as a consequence of the inevitable “smaller, faster, cheaper” trend for microelectronics to operate at higher frequencies and higher-performance levels. In the field of automotive engineering, an increasing number of functions, previously accomplished mechanically, are now solved electronically: braking and power steering are two examples. Elsewhere in power electronics, thermal management becomes a critical consideration in the design of DC power supplies, inverters, power controllers and motor drivers. However, it is the global and exponential growth in general and automotive, LED technologies that are creating huge market demand for efficient, reliable, low-cost thermal management solutions. Keeping heat generating components (LEDs/embedded components) cooler is what increases component life, which in turn increases product life and long term reliability. The move to increased usage of insulated metal substrates is primarily

“ The life expectancy of an LED is closely related to operating temperature. ”

driven by the need to reduce system costs through, in the main, reduction in size of or elimination of costly and bulky cooling fans and heat-sinks.

LED — Key Applications:

- Back light unit
- General lighting
- Street safety
- Automotive

Recent advances in high-brightness (HB) LED technology have alleviated concerns about excessive costs and led to an increasing number of local authorities across the world installing eco-friendly LED lighting; additionally, its adoption in domestic, industrial and automotive applications is rapidly and exponentially accelerating.

Putting things into perspective, a standard FR-4 has a thermal conductivity coefficient of around 0.25W/mK; thermally conductive prepregs, laminates and insulated metal substrates offer thermal conductivity coefficients of up to 8W/mK. Estimates suggest that LED

technology will capture 46% of the global lighting market by 2020, which alone provides a huge market potential for thermally conductive printed circuits.

Considering LEDs: Good thermal management is required to achieve a bright light, whilst maintaining the colour spectrum, without overheating the junction or the LED unit. The life expectancy of an LED is closely related to operating temperature. For example, 10°C reductions in temperature approximately will double the life expectancy of the LED.

How should heat be dispersed — by conduction, convection or radiation cooling? Probably, the most efficient mode of heat transfer is conduction through the substrate. Many power-electronics and under-bonnet automotive devices are built using direct bonded copper (DBC) substrates on ceramics with good thermal conductivity, particularly materials such as beryllia, silicon nitride or aluminium nitride, which are significantly better heat conductors than alumina, although at a significantly higher cost.

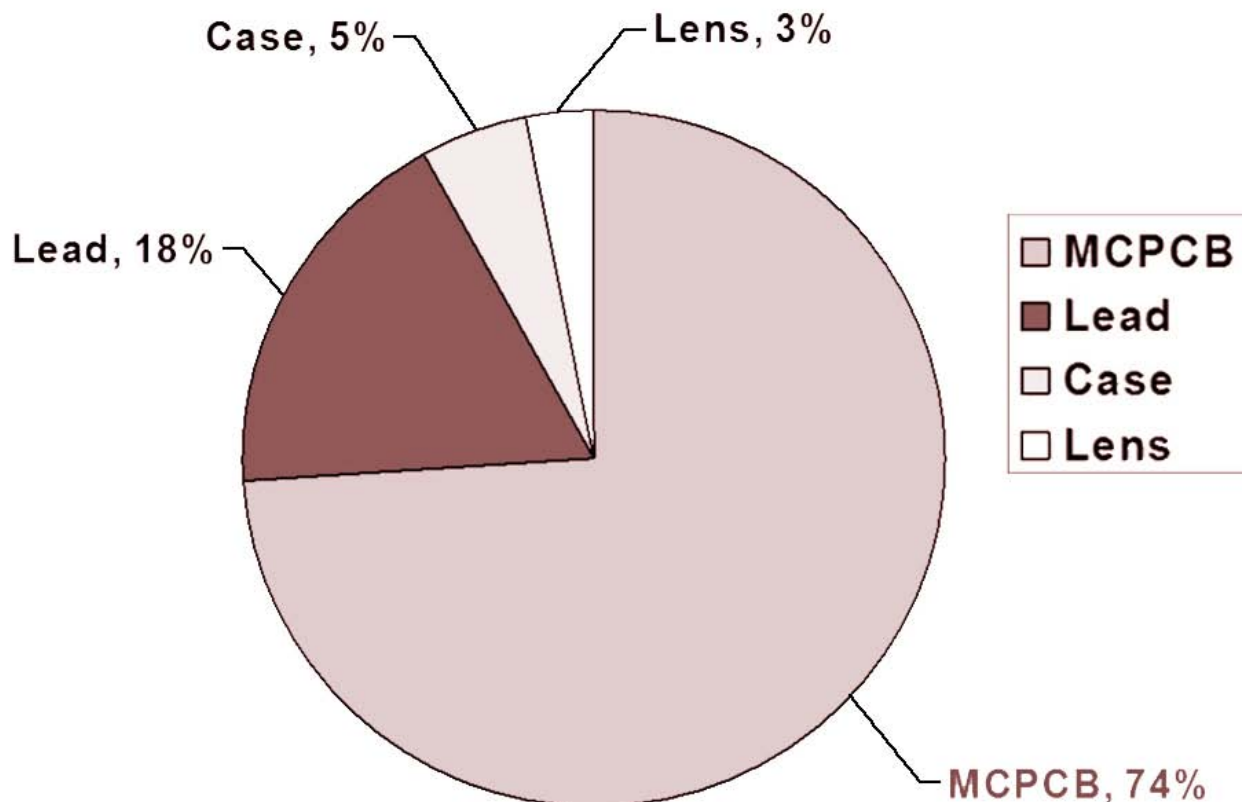


Figure 1: Thermal dissipation of a typical LED build.

The Four Main LED Substrate Types:

- **Metal Cored PCBs/IMS** — insulated metal substrates
- **Conventional PCB** — mid and high Tg FR-4
- **DBC** — direct bonded copper
- **LTCC** — low-temperature, co-fired ceramic (LTCC)

These are monolithic, ceramic microelectronic devices. In this context, co-fired ceramic means that the ceramic support structure and any conductive, resistive and dielectric materials are fired in a kiln at the same time. Low temperature means that the sintering temperature is less than 1000°C. LTCC devices include capacitors, inductors, resistors, transformers and hybrid circuits.

LED manufacturers have been adopting packaging technologies from the power-electronics field with the result that they can offer efficient thermal coupling from the semiconductor to the interconnecting substrate upon which the device is mounted. However, although common printed circuit materials have good electrical insulation properties, they generally provide excellent thermal insulation

as well. Heat dissipation has traditionally been promoted by the incorporation of internal or external heat sinks: heavy copper inner layers with thermal via holes or bonded aluminium heat ladders.

A family of thermally conductive printed circuit laminates known as insulated metal substrates (IMS) have now become widely established as a preferred base material for the manufacture of circuits for HB-LED applications and offer cost effective performance with straightforward fabrication, good mechanical stability and a range of thermal conductivities to suit particular configurations.

IMS materials generally consist of a thermally conductive dielectric layer, heavily loaded with ceramic filler, sandwiched between a copper foil and an aluminium plate. The dielectric may be unreinforced or woven-glass reinforced. Due to its superior mechanical properties, aluminium remains the most preferred backing substrate; however, alternatives include copper and steel plate.

The choice of filler is always a balance between thermal conductivity, cost and electrical insulation properties. You can see from the above chart that aluminium nitride and boron nitride give the best thermal conductivity with

Filler Type	Thermal Conductivity (W/m*K)	Breakdown Voltage (Based on 70%Filler)
Al ₂ O ₃	25~40	++
MgO	25~50	+
SiO ₂	9.6	+
Si ₃ N ₄	50	-
BeO	270	-
SiC	25~100	--
AlN	120~220	+
BN	100~250	+

++ Better + Good - Bad -- Worse

Table 1: Effect of filler on thermal conductivity and breakdown voltage.

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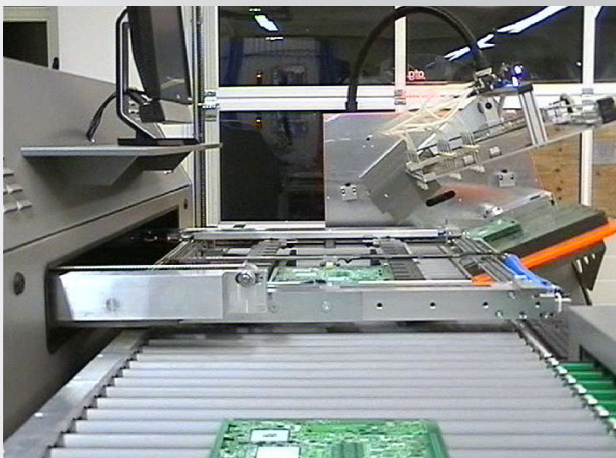


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Item	Reinforcement	Un-reinforcement (Unsupported)
Breakdown Voltage	++	+
Cost	+	-
Thickness evenness	++	+
Thermal Conductivity	+	++

Table 2: Comparison of woven-glass reinforced and non-reinforced IMS.

good breakdown voltage, while alumina gives a higher breakdown voltage, but with lower thermal conductivity.

Conventional PCB substrates are designed to have good electrical insulation, but due to the glass component they also tend to be good thermal insulators as well. The increased thermal conductivity of conventional glass style prepreps is achieved by loading the resin with thermally conductive ceramic fillers. These materials can be used to build multilayer PCB structures which can then be bonded to a heat-dissipating base.

Insulated metal substrates (IMS) are commercially available, and they offer cost effective performance with straightforward fabrication, good mechanical stability and a range of thermal conductivities to suit particular configurations. IMS is not a new concept. These materials have been available since the 1960s, but only recently has the volume demand driven the development of new and improved versions and warranted volume production.

Functions of the dielectric layer:

- Thermal conduction
- Electrical insulation
- Adhesion promotion — bonding to copper and aluminium

It also provides the choice of woven-glass reinforced or non-reinforced dielectric.

The dielectric serves a number of functions, including thermal conduction, insulation and promotion of good bonding. Generally, the di-

electric is a laminating resin loaded with a thermal conductive ceramic filler, designed to give a good bond to the copper foil, the base laminate and to the metal substrate, if it is a pure IMS. It may be glass-reinforced or unreinforced.

Conventional FR-4 glass-reinforced dielectrics create a thermally resistive, as well as an electrically resistive barrier. At this stage, thermally conductive glass reinforced dielectrics currently allow in excess of 12x more heat transfer than standard FR-4; the use of non-reinforced dielectrics is significantly increasing this figure.

As can be seen above, the choice between reinforced and un-reinforced dielectric is a trade-off; glass reinforced material offer better thickness uniformity and higher breakdown voltage (obviously the two are linked) and the cost is lower. The trade-off is that the ultimate thermal conductivity of the glass-reinforced material is less, because there's not as much room in the cross-section to accommodate as much thermally-conductive filler, and glass is a thermal, as well electrical insulator. However, that's not necessarily a disadvantage. It's all about applications engineering and choosing the most appropriate material for the job.

For a given application, the choice of dielectric is determined by the need to achieve a balance between thermal conductivity, dielectric strength, reliability and price. In general, the reinforced dielectrics have lower thermal conductivity, but higher breakdown voltage and superior thickness uniformity. The cost of glass-reinforced dielectrics is generally lower than the non-reinforced grades, which demand extreme-

Dielectric Thickness	Thermal Conductivity 1.6W/mK	Thermal Conductivity 2.2W/mK	Thermal Conductivity 3.0W/mK
75um	0.074	0.054	0.040
100um	0.099	0.072	0.053
125um	0.123	0.089	0.067
150um	0.148	0.107	0.080

Table 3: Variation of thermal impedance ($^{\circ}\text{C.in}^2/\text{W}$) with dielectric thickness, for different W/mK values of thermal conductivity.

ly critical manufacturing control to ensure uniformity of filler dispersion and the absence of traces of particulate foreign material that could lead to premature dielectric breakdown. Also, due to thickness distribution considerations, most manufacturers can only laminate non-reinforced materials in small panel sizes — increasing unit cost and potentially limiting applications.

Typical characteristics of IMS laminates are: Aluminium from 0.5mm to 3.0mm thick, available in different grades to suit mechanical requirements; copper from 18um to 410um and dielectric thickness from 75um to 150um. Printed circuit fabrication is by conventional print-and-etch techniques. The aluminium is protected during etching by a peelable film. Single-layer technology is suitable for most applications, but multilayer constructions are feasible by sequential lamination using thermally conductive prepregs and thin laminates constructed from thermally conductive prepregs.

Watt per Metre-Kelvin (W/mK)

W/mK is the commonly quoted unit of thermal conductivity, which is the measure of the ability of a substance to conduct heat, sometimes shortened to just conductivity.

Also known as the coefficient of heat conductivity because it's a coefficient, it needs to be

considered in conjunction with thickness. The reciprocal, thermal impedance, is proportional to the ratio of thickness to CTE and is probably a more practical parameter.

Thermal Impedance

Variation of thermal impedance ($^{\circ}\text{C.in}^2/\text{W}$) with dielectric thickness, for different W/mK values of thermal conductivity (Table 3).

To reduce the thermal impedance by half, double the thermal conductivity or halve the thickness of the dielectric.

So, rather than just demand a high W/mK value, consider whether a lower W/mK at a lower dielectric thickness will give the same thermal impedance, at lower cost, provided that the dielectric strength is sufficient. It's really only at high operating voltages that this becomes a serious consideration. Therefore, for most LED and low voltage applications, the lower W/mK materials are perfectly adequate.

IMS materials are currently available with thermal conductivity values from approximately 1W/mK suitable for low-power LED applications, up to about 8W/mK for power electronics. For reference, copper is 380W/mK, aluminium 200W/mK and FR-4 laminate around 0.4W/mK. It is important to systematically evaluate and characterise an IMS material for a particular application, rather than rely on data-sheet

information, which may overstate certain critical parameters or, at the very least, be difficult to use comparatively due to a variety of different test methods being used to generate critical datasheet values, such as thermal conductivity and electrical breakdown strength.

Insulated metal substrates are generally compatible with lead-free soldering processes; however, construction has a considerable influence on reliability. Woven glass reinforcement of the dielectric reduces its coefficient of thermal expansion both in the X-Y plane and, to a lesser extent, in the Z-axis, such that the CTE mismatch between copper, dielectric and aluminium is significantly less than for traditional unreinforced dielectrics. Resin chemistry determines characteristics, such as Tg (glass transition temperature) and Td (decomposition temperature), which, likewise, affect reliability under thermal stress and thermal shock conditions.

In typical LED street lighting applications, the main reliability issue for insulated metal substrates is not dielectric breakdown, since operating voltages are relatively low, but the effect of shear stress resulting from CTE differences between copper, dielectric and aluminium during the severe thermal cycling between power-

on and power-off, together with day-night and seasonal ambient temperature and humidity variations.

Key points in Selecting Dielectric Type and Thickness for IMS

- Understand the thermal, electrical and mechanical performance requirements of the design
 - There is a performance/reliability/cost trade off
- Thermal Conductivity of the Dielectric
 - Lower thermal conductivity — thinner dielectric required?
 - Higher thermal conductivity — thicker dielectric possible?
- Copper Thickness
 - Heavy coppers have a larger treatment profile
 - Consider the peak-to-peak dielectric separation between copper treatment and the treated surface of the aluminium/copper/steel backing
 - Directly influences electrical breakdown performance & reliability

$\leq 105\mu\text{m}$ copper — 75-100 μm dielectric
 $\geq 140\mu\text{m}$ copper — 100-150 μm dielectric

Item	Unit	Glass Reinforced (100 μm)	Unsupported Dielectric (100 μm)	PI Film (20 μm)	Ceramic Substrate (AlN)
Thermal Conductivity	W/m-K	3.0	3.0	0.8	170
Thermal Impedance	$^{\circ}\text{C}\cdot\text{in}^2/\text{W}$	0.08	0.08	0.06	0.001
Breakdown Voltage	VDC	2000	1500	2000	5000
Water Absorption	%	0.5~0.8	0.8~1.0	1.0~1.5	0.08
Tg	$^{\circ}\text{C}$	130	130	230	-
Peel Strength	Kgf/cm	1.4~1.6	1.2~1.4	1.0~1.2	
Price	-	Low	medium	Expensive	Very Expensive

Table 4: Dielectric comparison.

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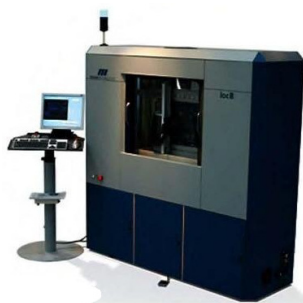
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If you really need a thinner dielectric with a heavy copper you can consider the use of RTF foil, but peel strength will be reduced.

Beware of Data Sheet Values

There is a tendency for some suppliers to quote figures based on in-house test methods; even thermal conductivity data is significantly overstated against recognised test methods by some producers.

Until the IMS market matures and a universally accepted set of test methods emerges, there are going to be some anomalies making direct correlation of data sheet values difficult.

Results of dielectric breakdown and dielectric withstand values depend on the design of the test coupon for some commonly used test methods. Best advice is to only use data sheet values as a guide:

- Don't rely on the accuracy of figures where the exact test method is not stated
- When a recognised test method is stated, don't take the results too literally
- To quote from ASTM D149, Standard Test Method for Dielectric Breakdown Voltage and Dielectric Strength of Solid Electrical Insulating Materials at Commercial Power Frequencies:

"Results obtained by this test method can seldom be used directly to determine the dielec-

tric behaviour of a material in an actual application. In most cases it is necessary that these results be evaluated by comparison with results obtained from other functional tests or from tests on other materials, or both, in order to estimate their significance for a particular material."

As for international standards for production of IMS and metal backed circuits, part of the problem is that there are no concrete standards at the moment. Committees are in place to develop standards for IMS and conductive substrates; we, along with a number of manufacturers and LEADING end users are involved. Until this is resolved, buyer beware and, in regard to data sheet values, it is important to check, check and re-check.

PCB Fabrication Considerations

Thermal prepregs ML lamination:

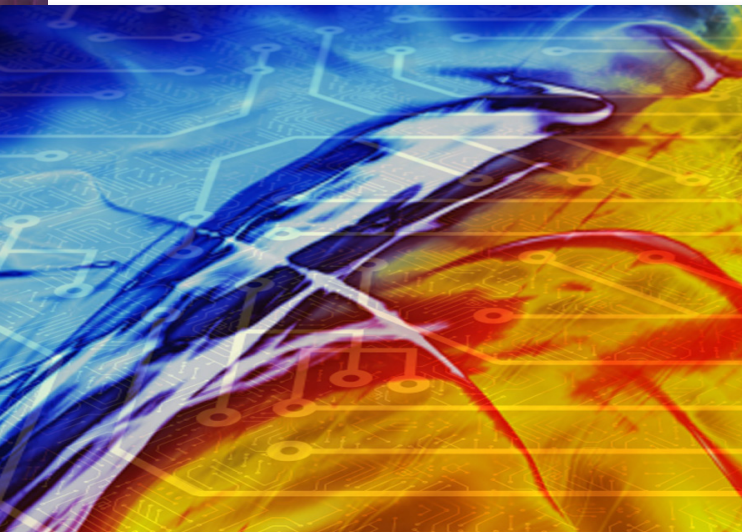
- The heavy loading of these materials, with filler, leads to low-flow prepreg characteristics; therefore, there is a need for rapid temperature rise and early application of lamination pressure.
- It is possible to encapsulate 2-oz copper tracks; however, heavier copper weights will present some challenges.

Machining:

- Due to the type and content of filler in IMS, there is a tendency to rapid tool wear.
- Undercut, diamond coated Drill bits are preferred, spindle speed will be around 80% of that used for FR-4.
- Two-flute end mills give best finish on aluminium, and adjust cutter depth at 50% tool life to compensate for local abrasion by filler.

Lead-free soldering and thermal cycling:

- Insulated metal substrates are generally compatible with lead-free soldering processes; however, construction has a significant influence on reliability. Woven glass reinforcement of the dielectric reduces its coefficient of thermal expansion both in the XY plane, and, to a lesser extent, the Z-axis
- Resin chemistry determines characteristics, such as Tg (glass transition temperature) and Td (decomposition temperature) which,



likewise, affect reliability under thermal stress and thermal shock conditions

- Surface treatment of aluminium prior to bonding is critical, both to achieve high bond strength and to avoid high-resistance shorts from metallic debris.

Summary

There continues to be increasing interest in cost-effective thermal management of electronic devices and PCBs and thermally conductive printed circuit substrates, or IMS, are becoming the solution of choice. When specifying or pre-selecting materials, think in terms of actual thermal impedance of an IMS material, rather than judging everything on WmK. Finally, choose your materials to suit the application and most importantly, do your own qualification tests and don't take data sheet values too literally.

More information may be obtained by clicking [here](#). **PCB**



Ian Mayoh has more than 27 years of experience in PCB manufacturing, and has held positions with Hoechst AG, LeaRonal, Elga Europe Ltd and Invotec Circuits. Mayoh joined Ventec Europe in January 2011 as technical support manager covering the European, Middle Eastern and African markets. Mayoh may be reached at ian.mayoh@ventec-europe.com.



Mark Goodwin is the managing director of Ventec Europe Ltd., and has been in the PCB manufacturing supply chain industry for more than 28 years, including 15 years at Isola UK. In 2007, Goodwin joined GVL Ltd, a joint venture company with Ventec Electronics (Suzhou) China and Global Laminates USA, which evolved into Ventec Europe Ltd., a majority owned subsidiary of the Ventec International Group.

Ventec Celebrates Five Years

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Mark Goodwin, general manager for Ventec's European operations, reflects upon the company's growth as it approaches its fifth anniversary.



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SAN DIEGO 2012



IPC APEX EXPO 2012 — Special Coverage Section

This year's IPC APEX EXPO is gearing up to be a good one, with new offerings as well as plenty of valuable programs, exhibitions and demos on a wide range of industry topics. Our special coverage section is just a sampling of what you'll find at this year's show — like the New Product Zone, where you can get a sneak preview of the equipment, materials and services that are breaking new ground in our industry.

For a complete listing of exhibitors, programs and events, or to simply find out more about it, [click here](#). Hope to see you at the show!

2012 Show Schedule

Exhibits Open

Tuesday, February 28: 10:00 a.m.-6:00 p.m.
Wednesday, February 29: 10:00 a.m.-6:00 p.m.
Thursday, March 1: 10:00 a.m.-2:00 p.m.

Saturday, February 25

- 8:00 a.m.-5:00 p.m.
IPC Standards Development Committee Meetings

Sunday, February 26

- 8:00 a.m.-6:00 p.m.
IPC Standards Development Committee Meetings
- 9:00 a.m.-12:00 p.m.
Professional Development Courses
- 10:00 a.m.-7:00 p.m.
IPC APEX EXPO Golf Tournament followed by Reception
- 2:00-5:00 p.m.
Professional Development Courses

Monday, February 27

- 7:30 a.m.-9:00 p.m.
IPC PCB Executive Management Meeting & Dinner
- 7:30 a.m.-9:00 p.m.
IPC EMS Management Council Meeting & Dinner
- 7:30 a.m.-1:30 p.m.
IPC Designers Forum
- 8:00 a.m.-5:00 p.m.
IPC Standards Development Committee Meetings
- 9:00 a.m.-12:00 p.m.
Professional Development Courses
- 12:00-1:30 p.m.
Event Awards Luncheon
- 2:00-5:00 p.m.
Professional Development Courses
- 5:30-6:30 p.m.
International Reception

Tuesday, February 28

- 7:30-8:30 a.m.
FREE! IPC First-Timers' Welcome Breakfast
- 8:30-9:30 a.m.
FREE! Opening Keynote Session
- 9:40-10:00 a.m.
Ribbon Cutting Ceremony
- 10:00 a.m.-5:00 p.m.
IPC Standards Development Committee Meetings
- 10:00 a.m.-6:00 p.m.
Exhibits Open
- 12:00-1:30 p.m.
Event Luncheon & IPC Annual Meeting
- 1:30-4:45 p.m.
FREE! BUZZ Sessions
- 1:30-5:00 p.m.
Technical Conference Sessions
- 6:00 p.m.
Exhibitor Networking Functions

Wednesday, February 29

- 7:30-8:30 a.m.
FREE! Women in Electronics Networking Meeting
- 8:00-9:30 a.m.
FREE! Keynote Session
- 8:00 a.m.-5:00 p.m.
IPC Standards Development Committee Meetings
- 9:00-11:45 a.m.
Technical Conference Sessions
- 9:00-11:45 a.m.
FREE! BUZZ Sessions
- 10:00 a.m.-6:00 p.m.
Exhibits Open
- 12:00-1:30 p.m.
Event Awards Luncheon
- 1:30-3:30 p.m.
Technical Conference Sessions
- 1:30-3:30 p.m.
FREE! BUZZ Sessions
- 3:30-4:30 p.m.
Technical Poster Presentations by Authors
- 4:00-6:00 p.m.
Show Floor Reception

Thursday, March 1

- 8:00 a.m.-12:00 p.m.
IPC Standards Development Committee Meetings

- 8:30-11:45 a.m.
FREE! BUZZ Sessions
- 9:00-11:45 a.m.
Technical Conference Sessions
- 9:00 a.m.-12:00 p.m.
Professional Development Courses
- 10:00 a.m.-2:00 p.m.
Exhibits Open
- 2:00-5:00 p.m.
Professional Development Courses

Certification Programs:

Friday, February 24

- 8:30 a.m.-5:00 p.m. — **PCB Designer Certification (CID) Workshop**
- 8:30 a.m.-5:00 p.m. — **PCB Advanced Designer Certification (CID+) Workshop**

Saturday, February 25

- 8:30 a.m.-5:00 p.m. — **PCB Designer Certification (CID) Workshop**
- 8:30 a.m.-5:00 p.m. — **PCB Advanced Designer Certification (CID+) Workshop**

Sunday, February 26

- 8:30 a.m.-3:00 p.m. — **PCB Designer Certification (CID) Exam**
- 8:30 a.m.-3:00 p.m. — **PCB Advanced Designer Certification (CID+) Exam**

Monday, February 27

- 8:00 a.m.-5:00 p.m. — **Intro to the EMS Industry and Program Management**

Tuesday, February 28

- 8:00 a.m.-1:00 p.m. — **Intro to the EMS Industry and Program Management**

Thursday, March 1

- 8:00 a.m.-5:00 p.m. — **EMS Program Manager Training and Certification II**
- 8:00 a.m.-5:00 p.m. — **EMS Leadership Training**

Friday, March 2

- 8:00 a.m.-5:00 p.m. — **EMS Program Manager Training and Certification II**
- 8:00 a.m.-5:00 p.m. — **EMS Leadership Training**

Saturday, March 3

- 8:00 a.m.-5:00 p.m. — **EMS Program Manager Training and Certification Exam**

SAN DIEGO 2012



FREE Keynote Presentations

Opening Keynote:

Tuesday, February 28: 8:30-9:30 a.m.

Captain's Log — boldly going where no man has gone before...

William Shatner

One of Hollywood's most recognizable figures, William Shatner has cultivated a career spanning more than 50 years as an award-winning actor, director, producer, writer, recording artist, horseman and a major philanthropist. Perhaps best recognized for his role as Captain James T. Kirk, Shatner's accomplishments in television, film, and stage are numerous, including Emmys, Golden Globes and SAG award nods. Ironically enough, his true mission has had him exploring "strange new worlds" and seeking out "new life."

There are many sides to Bill beyond his portrayals of Captain Kirk, Denny Crane (The Practice and Boston Legal) and Priceline's infamous negotiator. Even at the tender age of 80, he, like his horses, does not like to stand still.

Off the screen and broadcast waves, Shatner has authored nearly 30 best-sellers in both the fiction and nonfiction genres. His autobiography, *Up Till Now*, was a New York Times best-seller. Shatner's newest book, *Shatner Rules: Your Guide to Understanding the Shatnerverse and the World at Large* was released in October 2011. While he admits that many of the rules are tongue-in-cheek, he stands by the fact that, "in their amusement, there is a truth."

William Shatner Book Signing

Tuesday, February 28 • 10:00 a.m.

Sails Pavilion (upper level exhibit hall)

Beam on up to the Sails Pavilion and meet William Shatner in person. He'll be signing

copies of his latest book, *Shatner Rules: Your Guide to Understanding the Shatnerverse and the World at Large*. Copies will be available for purchase on-site.

Day Two Keynote:

Wednesday, February 29: 8:00-9:30 a.m.

Gazing into the Crystal Ball

Panelists: Phil Plonski, Managing Partner, Prismark Partners; Peter Irvine, President, PCM, DuPont and Cary Wood, President and CEO, Sparton

The Wednesday morning keynote promises to shake things up a bit. What will be the game-changers for the PCB and electronics assembly industries?

Is it printed electronics, nanotechnology, environmental regulations or new quality and reliability drivers? Industry experts will look into the future and predict the shocks to our industry — and opportunities.

The presentations will be short — approximately 15 minutes — allowing plenty of time for questions and answers. There will be no PowerPoint presentations — no proceedings — just the ancient method of speech to communicate exciting new trends via the power of the word.



Technical Conferences

We've done a little groundwork for you and put together just a sampling of e PCB-related technical conferences that you'll find at this year's show. Don't see what you're looking for? Click [here](#) for a complete, searchable database of what's happening and whom you can expect to see at the 2012 IPC APEX EXPO.

Technical Conference Sessions on this year's emphasis, *printed electronics*

Leaders from the printed electronics industry will present the latest technical information on materials, processes, and equipment on Wednesday, February 29. The sessions will feature presentations discussing not only the printed electronics standards IPC is developing, but also new materials and processes for printed electronics — from inks to flexible substrates to roll-to-roll manufacturing.

Topic/Track: Printed Electronics

Technical Drivers for Printed Electronics

Wed, Feb 29, 2012

9:00 - 10:00 a.m.

Presenter/Committee Chair:

- **Daniel Gamota**, President, Printovate Technologies, Inc.

The adoption of standards can facilitate the growth of the printed electronics field and reduce the burden placed on individual companies to invest significant resources in the development of company specific compliance documentation. This session will highlight the various opportunities for standards development along the printed electronics supply chain as well as the progress of the four IPC-initiated standards activities: 1) base material, 2) additive material standard, 3) standard design guideline, and 4) final assembly standard.

Advanced Materials for Printed Electronics

Wed, Feb 29, 2012

10:15 - 11:45 a.m.

Presenters/Committee Chairs:

- **Scott Gordon**, Marketing Manager, DuPont
- **Daniel Gamota**, President, Printovate Technologies, Inc. (moderator)
- **Neil Bolding**, Technical Manager, MacDermid Autotype Inc.
- *Performance Requirements for Substrates for Printed Electronics, Neil Bolding*
- *Advances in Conductive Inks Across Multiple Deposition Platforms, Scott Gordon*

An often overlooked design parameter for printed electronics based products is the selection of an appropriate substrate. During this session, subject matter experts will provide an overview of key substrate material properties (e.g. mechanical, electrical, thermal, and optical) that determine high yield manufacturing as well as in-field product performance. Also, presenters will highlight advanced substrate development efforts underway to meet the needs of designers in the final stages of new product introduction programs.

Technical Conferences — *continues***Emerging Technologies and Manufacturing Processes for Printed Electronics**

Wed, Feb 29, 2012
1:30 - 3:30 p.m.

Presenters/Committee Chairs:

- **Voya Markovich**, Sr. VP and CTO, Endicott Interconnect Technologies, Inc.
- **Don Banfield**, Product Manager, Conductive Compounds
- **Mark Poliks Ph.D.**, Director, Research and Development, Endicott Interconnect Technologies Inc.
- **Steve Tomas**, Director, Flexible Electronics, Flexcon Company
- **Frank Egitto**, R&D Manager, Endicott Interconnect Technologies Inc.

- *New and Emerging Technologies in Printed Electronics*, Don Banfield
- *Roll-to-Roll Manufacturing of Printed Interconnect Systems*, Frank Egitto, Voya Markovich, Mark Poliks Ph.D.

Printed electronics applications using advanced functional printing techniques and new ink technology continue to expand worldwide. Learn how to leverage the technical capabilities and experience of your suppliers as well as customers in order to stay abreast of the rapid changes and new opportunities that are available in printed electronics.

Topic/Track: Quality, Reliability and Test**Environmental Compliance**

Tue, Feb 28, 2012: 1:30-3:00 p.m.

Presenter/Committee Chair(s):

- **Beverley Christian Ph.D.**, Dir. Materials Intercon., Research In Motion Limited
- **Susan Landry**, Advisor, Fire Safety & Advocacy, Albemarle Corporation
- **Peter Robinson**, Vice President, Total Parts Plus
- **Jorgen Vos**, Product Management Director, PTC

In the environmental area it is always good to know: a) what the regulatory bodies want from you, b) what you can do early in your product development process to "green" your products, and c) what real environmental burden is posed by your electronic products or electronic products in general. In this session industry experts will step through the regulatory status, the design process to achieve compliance and the reality of regulatory compliance issues in

the electronics industry. Get an in-depth look at the real issues in environmental compliance today.

- *Environmental Compliance Reporting — Mastering a Moving Target*, Peter Robinson
- *New Techniques to Scale the Use of LCA in Product Development*, Jorgen Vos
- *Elemental Compositions of Over Two Dozen Cell Phones*, Beverley Christian Ph.D.

Solder Joint Testing and Performance

Wed, Feb 29, 2012: 1:30 - 3:30 p.m.

Presenter/Committee Chair(s):

- **Ning-Cheng Lee Ph.D.**, Vice President of Technology, Indium Corporation of America
- **Christopher Hunt Ph.D.**, Principal Research Scientist, National Physical Laboratory

Technical Conferences — *continues*

- **Jasbir Bath**, Christopher Associates Inc.
- **Ronald Lasky Ph.D.**, Senior Technologist, Indium Corporation of America
- **Daniel Cavin**, Principal Member of the Technical Staff, Advanced Micro Devices — AMD

What are your choices for lead-free solder alloys? How can you tell what is best for your needs? In the long term, how can you be sure the alloy you choose is reliable? The papers in this session consider the hows and whys of alloy choice, process requirements and reliability testing for lead-free solders. Improve your range of options by joining this session as industry experts give you the latest information on developments in lead-free assembly, testing and performance.

- *Choosing a Low-Cost Alternative to SAC Alloys for PCB*, Ronald Lasky Ph.D.
- *Drop Test Performance of BGA Assembly Using Sac 105ti Solder Sphere*, Ning-Cheng Lee Ph.D.
- *Low-Cycle Fatigue Behavior of Multi-Joint Sample in Mechanical Testing*, Christopher Hunt Ph.D.
- *The Influence of Copper on Second Level Interconnect Reliability of Pb-Free BGA Assemblies*, Daniel Cavin

Design for Test (DFT)

Thu, Mar 1, 2012 - 9:00 - 10:00 a.m.

Presenter/Committee Chair(s):

- **Lars-Olof Wallin**, IPC European Representative, IPC European Representative Office

Failing to plan is often described as “planning to fail.” For test, planning means using good design for test (DFT) rules. In this session, test design techniques for boundary scan of assemblies and chips will be discussed in light of the latest developments in test standardization. Learn how better to plan your test strategy by using boundary scan and the latest test standards.

- *Testing DDR Memory — How On-Chip DFT Helps*, John Pendlebury
- *Virtual Access Technique Augments Test Coverage on Limited Access PCB Assemblies*, Anthony Suto

Standards Development Meetings**Sunday – Thursday,**

February 26 through March 1

Contribute to the industry standards and guidelines that your company, customers, suppliers and competitors rely on by attending IPC standards development meetings. Newcomers and industry veterans are welcome. Participate and learn more about these critical industry documents.

New This Year — Be part of historic meetings that will begin to establish industry requirements for printed electronics in the areas of design, base materials/substrates, functional materials and final assembly (D-61, D-62, D-63 and D-64). These sessions are open to all registered attendees.

For a complete listing of Standards Development Meetings in all categories, and registration details, click [here](#).

Professional Development Courses

Sunday, Monday and Thursday

February 26-27 and March 1

Below are the courses being offered in just two topic areas at IPC APEX EXPO 2012: PCB Fab and Materials, and Quality, Reliability and Test. For a complete listing of all topic areas/courses and registration details, click [here](#).

Topic:

PCB Fabrication and Materials

PD07: PCB Fabrication Basics: Process and Specification (Part 1)

Sun, Feb 26, 2012 – 9 a.m. to noon

Level: Basic

Presenter/Committee Chair(s):

- **Jim Vanden Hogen**, Sr PCB Commodity Spclst, Plexus Corporation
- **Don Schmieder III**, PCB Commodity Manager, Plexus Electronic Assembly Corporation

What You Will Learn

- Step-by-step PCB fabrication process
- PCB types and industry specs
- Laminate types and properties
- Stack-ups, via metrics and aspect ratios

For maximum benefit, registering for both this session and Part II (PD02) in the afternoon is highly recommended.

PD50: Flexible and Rigid-Flex Circuit Design Principles and Fabrication

Sun, Feb 26, 2012 - 9 a.m. to noon

Level: Basic

Presenter/Committee Chair(s):

- **Vern Solberg**, Senior Consultant, Solberg Technical Consulting

What You Will Learn

- Applications - commercial, industrial, automotive, aerospace
- Designing single-sided, double-sided and rigid-flex circuits
- Substrate material selection and metallization technologies
- Specifying base material and applicable standards
- Fabrication methodologies
- Subtractive (etched circuit) process
- Semi-additive circuit plating
- Flex and rigid-flex fabrication

For maximum benefit, registering for both this session and Part II (PD35) in the afternoon is highly recommended.

PD02: PCB Fabrication Basics: Process and Specification (Part 2)

Sun, Feb 26, 2012 - 2-5 p.m.

Level: Basic

Presenter/Committee Chair(s):

- **Jim Vanden Hogen**, Sr PCB Commodity Spclst, Plexus Corporation
- **Don Schmieder III**, PCB Commodity Manager, Plexus Electronic Assembly Corporation

What You Will Learn

- Step-by-step PCB fabrication process (continued)
- Surface finish choices
- Array design and optimal material utilization
- Fabrication specification

For maximum benefit, registering for both this session and Part I (PD07) in the morning is highly recommended.

Professional Development Courses — *continues***PD10: Final Finishes — Compatibility with Lead-Free Assembly**

Sun, Feb 26, 2012 – 2-5 p.m.

*Level: Intermediate**Presenter/Committee Chair(s):*

- **Michael Carano**, VP of Technical Operations for Electronic Chemicals, OMG Electronic Chemicals, LLC

What You Will Learn

- Solderability overview
- Metallic coatings: electroplated nickel-gold, electroless nickel-immersion gold, palladium, immersion tin, immersion silver
- Thin versus thick organic coatings
- Compatibility of lead free surface finishes with lead free solders
- Paste spreadability studies
- Through-hole fill studies
- Joint strength testing
- Effects of aging and multiple thermal cycles on solderability
- Process control: solderability checks, deposit integrity
- Cost implications of lead-free finishes

PD35: Design for Flexible and Rigid-flex Circuits-Part II

Sun, Feb 26, 2012 – 2-5 p.m.

*Level: Intermediate**Presenter/Committee Chair(s):*

- **Vern Solberg**, Senior Consultant, Solberg Technical Consulting

What You Will Learn

- Design guidelines for complex flexible and rigid-flex circuits
- Requirements for flip chip on flex
- Preparing for volume SMT assembly
- Flex and rigid-flex assembly processing
- Quality assessment for SMT assemblies

For maximum benefit, registering for both this session and Part I (PD50) in the morning is highly recommended.

PD34: HDI: Introduction to Processes and Products

Mon, Feb 27, 2012 – 2-5 p.m.

*Level: Basic**Presenter/Committee Chair(s):*

- **Christopher Ryder**, Global Manager — Customer Quality, AT&S Austria Technologie & Systemtechnik AG

What You Will Learn

- HDI stack-up nomenclature
- Basic HDI PCB manufacturing process flow
- Common base materials employed in HDI
- Quality control tests and methods
- Common process defects
- Laser via process, including general industry variations

PD45: Front-End Engineering Perspective on Design Issues

Thu, Mar 1, 2012 – 9 a.m. to noon

*Level: Basic**Presenter/Committee Chair(s):*

- **Mike Tucker**, Director of Engineering, Colonial Circuits Inc.

What You Will Learn

- Data required from designers for fabrication
- What CAM departments do with your data
- Design recommendations
- Rules-of-thumb DFM guidelines
- Top reasons why jobs go on hold at fabrication

Professional Development Courses — *continues*

Topic:
Quality, Reliability and Test

PD01: Building Long-Term Reliability in PCBs: Materials, Plating Processes and Innerlayer Treatments for Lead-Free Assembly Requirements

Sun, Feb 26, 2012 – 9 a.m. to noon

Level: Intermediate

Presenter/Committee Chair(s):

- **Michael Carano**, VP of Technical Operations for Electronic Chemicals, OMG Electronic Chemicals, LLC

What You Will Learn

- Alternatives to conventional FR-4A
- Factors that influence lamination of multilayers, including multilayer stack-ups and tooling considerations
- How plating operations influence long-term reliability
- Key materials properties such as Tg, CTE, Td, Dk, Df and moisture sensitivities
- Operating parameters for use of oxide and oxide alternatives for inner layer lamination
- Materials - multifunctional, polyimide and non-woven strong
- Filled versus unfilled materials
- Glass styles
- PTH drilling parameters
- Circuit density
- Use of reverse treat foil versus standard foil
- PTH and blind via aspect ratios — limiting factors
- Assembly reflow profile optimization
- Conductive anode filament formation (CAF)

PD19: Controlling Moisture Content in Boards: Best Practices

Sun, Feb 26, 2012 – 2-5 p.m.

Level: Intermediate

Presenter/Committee Chair(s):

- **Bhanu Sood Ph.D.**, Director Test Services & Failure Analysis, University of Maryland

What You Will Learn

- Moisture transport mechanisms
- Governing models and dependent variables of the moisture diffusion process
- Effects of moisture on susceptible components (organic matrix, fillers, interfaces, vias, traces, solder masks etc.) and associated failure modes and mechanisms
- PCB material handling and storage guidelines: classified based on distinct steps of the PCB manufacturing and assembly process

PD42: Tin Whiskers: Origin, Propensity, Mitigation

Sun, Feb 26, 2012 – 2-5 p.m.

Level: Intermediate

Presenter/Committee Chair(s):

- **David Pinsky**, Principal Engineer, Raytheon Company
Topic/Track: Quality, Reliability and Test
Event Type: Professional Development

What You Will Learn

- Properties of coating materials
- Mechanisms for whisker formation
- Effect of environmental exposure acceleration on whisker propagation
- Whisker risk assessment
- Recommendations for whisker mitigation

Professional Development Courses — *continues***PD23: Failure Analysis:
Lessons Learned**

Mon, Feb 27, 2012 – 9 a.m. to noon

*Level: Intermediate**Presenter/Committee Chair(s):*

- **Martin Anselm**, Process Research Engineer, Universal Instruments Corporation

What You Will Learn

- Major difficulties in lead-free reliability testing
- Mixed alloy assembly best practices
- ENEPIG intermetallic formation morphologies
- PCB plating considerations
- Analytical testing techniques
- Root causes of production failures
- Failure analysis studies - fine-pitch printing, PoP, 01005 defects, and high Tg laminate failures

**PD27: Optimizing X-Ray
Inspection: Equipment,
Processes and Procedures**

Mon, Feb 27, 2012 – 9 a.m. to noon

*Level: Intermediate**Presenter/Committee Chair(s):*

- **Bob Klenke**, Principal Consultant, ITM Consulting Inc.

What You Will Learn:

- Fundamentals of X-ray inspection: geometric and system magnification, image quality; oblique viewing, tilting sample vs. moving detector
- Inspection strategies and bridging techniques
- Detection techniques for defects: BGA micro-cracks, interfacial voids and process voiding; head-on-pillow, and automated HoP inspection routine
- Inspection of QFP, QFN and discrete SMT components
- Specific application requirements:

automatic BGA void percentage calculation, infrared microscopy, XRF and X-ray counterfeit component detection techniques

- Imaging of microvias within BGA substrates
- Correlation of BGA solder ball diameter and bridging effects of popcorning
- Computerized tomography: image acquisition, computational geometric processing and 3-D modeling, 3-D imaging of multi-level wire bonding and flip-chip solder bumps
- Inspection of advanced 3-D packaging and stacked die devices
- Non-semiconductor applications, including high-temperature automotive electronics
- Optimizing the X-ray inspection process: proper selection of tilt and rotation angles and X-ray parameters, including kV and W, retaining sub-micron feature recognition and high resolution images
- Compensating X-ray tube parameters for lead-free material properties

**PD49: Testability Strategies:
Optimizing the Mix**

Mon, Feb 27, 2012 - 9:00 a.m. to noon

*Level: Intermediate**Presenter/Committee Chair(s):*

- **Louis Ungar**, President, A.T.E. (Advanced Test Engineering)

What You Will Learn

- Test strategies
- Automated inspection (AOI, AXI)
- Automatic testing and ATE
- Design for testability, including JTAG/IEEE-1149.x
- Built-In Self-Test (BIST)
- Test economics

Most-Read MilAero007 News Highlights This Month



Top 10 Countdown:

Most-Read Mil/Aero Articles of 2011

As the lights went down on 2011, the editors at I-Connect007 took a look back at the year's top stories. Like a team of analysts toiling in the Pentagon's basement, we compiled our own "Top 10 Countdown" of the most-read items from MILAERO007 and MILAERO007 Weekly Newsletter. If this list is any indication, ITAR compliance is a very important issue for many of you.

IPC Comments on Proposed U.S. Changes to Export Control

IPC has filed comments with the U.S. Department of State's Directorate of Defense Trade Controls (DDTC) urging them to protect the security of U.S. defense equipment by ensuring export control protection of design information for PCBs for defense equipment.

UK Aerospace Industry to Reach \$50 Billion by 2016

Increasing passenger air travel and the continued development of new programs such as the Airbus A380, Boeing 787 Dreamliner, Eurofighter Typhoon, F-35 Lightning III, and the Bombardier C series are expected to support steady growth. The major drivers for the UK's defense sector are tied to budgetary increases, resulting in an increased level of defense aircraft procurement.

China's Aerospace & Defense to Hit \$187 Billion by 2015

The performance of the market is forecast to decelerate, with an anticipated CAGR of 11.9% for the five-year period 2010-2015, which is expected to drive the market to a value of \$187 billion by the end of 2015.

Aerospace & Defense Industry in India to See CAGR of 13.2%

With an anticipated CAGR of 13.2% for the five-year period 2010-2015, the market is forecast to decelerate. The defense segment was the market's most lucrative in 2010, with total revenue of \$17.7 billion, equivalent to 73.5% of the market's overall value.

Military Components Spending to Increase in China, APAC

With the reduced global expenses on new platforms in North America and Europe as troops continue to withdraw from Afghanistan and Iraq, there will be more spending on upgrades and retrofit programs. Sales in North America, Europe and Japan will be modest, while those in China will substantially increase.

U.S. Military Airborne Comm Market to See Significant Growth

Forecast International projects that defense departments throughout the world will spend about \$4.25 billion on 13 military airborne communications development and acquisition programs within the U.S. market over the next ten years.



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When Reliability Counts.

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Features

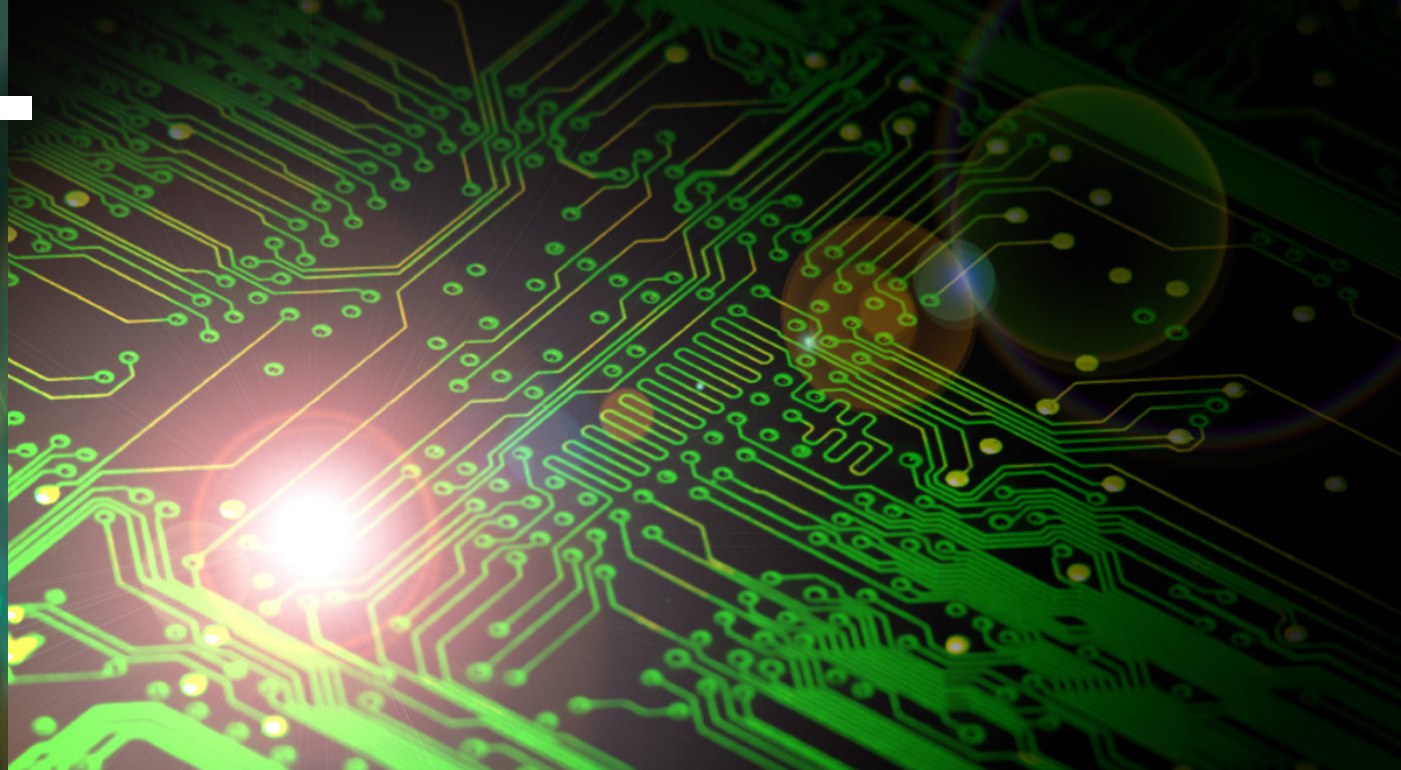
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RT/duroid® 6202PR	Reduced planar resistor variation	Lower manufacturing costs due to decreased tuning
	Low thermal coefficient of dielectric constant	Stable electrical performance versus temperature
	Low coefficient of thermal expansion	High reliability in complex multilayer designs
RT/duroid® 5880LZ	Dielectric constant of 1.96	Lowest dielectric constant microwave PCB material
	Low z-axis coefficient of thermal expansion	Plated through hole capable
	Light weight	Advantage for airborne applications
RT/duroid® 6035HTC	Highest thermal conductivity (1.44 W/mk) for 3.5Dk printed circuit board laminates	Excellent power handling capability
	Low loss 0.0013	Excellent high frequency performance
	Low profile, thermally stable copper options	Lower insertion loss, and performance reliability in high temperature applications

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Advanced Circuit Materials



ADVANCED ROUTING TECHNOLOGY — DEPTH ROUTING

by **Volker Feyerabend**

APROS INT. CONSULTING & SERVICES

SUMMARY — *The market's demands for finer structures have grown considerably over the years. Aside from smaller components, PCB dimensions for rigid and flex circuits have become increasingly smaller and lighter. As miniaturization trends continue, this course will make technological improvement and design creativity in the PCB production process indispensable.*

The market's demands for finer structures have grown considerably over the years. Aside from smaller components, PCB dimensions for rigid and flex circuits have become increasingly smaller and lighter. Therefore, the products have been made smaller and at a faster rate. In effect, one technology has been a driver for the other. As miniaturization trends continue, this course will make technological improvement and design creativity in the PCB production process indispensable.

Increases in component packaging density and the demand for more functionality have continued to drive design rules toward achieving an increasingly higher interconnection density. With newly designed circuit boards, one

must deal with increased complexity and smaller tolerances. Therefore, the need for accuracy has reached a new level as designers and manufacturers are faced with smaller tracks and vias.

In the context of drilling and routing, laser technology has enjoyed a fair share of publicity. For a long time, some considered laser technology to be the replacement for traditional mechanical processing. Lasers might play a leading role in current and future market demands, but there are still many questions to be answered and a long way to go in terms of productivity and flexibility.

The new market specifications for precision and tolerance can be supported by mechanical processes. Therefore, interest in mechanical drilling and routing processes remains on the radar. During the last years, improvements in drilling machine capabilities have been achieved. Drilling productivity is no longer an issue today with the current generation of drilling machines and new technologies in place like dual-spindle technology. Linear motors allow substantially improved path accuracy in routing, even during routing of complex forms. Precise definition of microvias, hole geometry, excellent hole-wall condition and accurate depth control allow for further options beside standard drilling.

“ With newly designed circuit boards, one must deal with increased complexity and smaller tolerances. ”

Mechanical circuit board processes, however, have some advantages, like easy adjustments or lower costs. Over the years, mechanical drilling and routing have been developed quite significantly. There is a new generation of demand in the market for system capabilities, tolerances and applications. The market shows a trend toward flex and flex-rigid boards. Certain microwave designs where relatively large surface areas have to be crossed pose a special challenge for routing and controlled-depth milling. All of this displays a clear trend towards multiplicity and flexibility which needs to be offered by equipment manufacturers.

The Swiss machine analyzed below allows depth routing with an accuracy of $\pm 15.0 \mu\text{m}$. Until now, this seemed impossible with the focus being only on laser technology. However, the strength of a drilling machine is still accuracy-based performance. The depth routing option allows for very complex designs, bended boards and structures processed with fine precision.

A customer evaluation project for the advanced depth routing use of a routing system has been performed. Below are the results.

Depth Routing Technology: Applications

To offer a structure, I will differentiate three areas of applications for the use of depth routing.

Option 1: Routing the top of the surface

Pocket routing for components is used on rigid-flex PCBs. The top surface will be milled away (taking the height of the chip and board into account). Considering a larger area must be traversed, the detection of the real surface structure is a key element. With non-conductive top surfaces a second measuring system is needed.

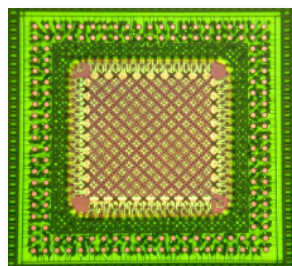


Figure 1: Sinked chip.

Different detection and calculation methods (see below) can be used. An accuracy of $\pm 40 \mu\text{m}$ is achievable with non-conductive surfaces and $\pm 15 \mu\text{m}$ on conductive spots. Pocket routing is mainly used if you need smaller

boards and a lower board thickness for buried processors or resistors.

Option 2: Routing down to the inner layers

In some applications a board must be designed with grounded inner layers and free contact surfaces on an inner layer, which will be connected to a chip. Designs should avoid tracks around the hole and above the chip. A nearby contact could falsely report the system as a closed loop and cause a false measurement, guiding the spindle to an undesired position. Customers currently use up to 12 layers in standard practice and production. The main reason for OEMs to use this kind of design is space, speed (shorter tracks) and EMC requirements. Technology-wise, there are no limitations in layer count. As more layers are added, it becomes more difficult for the system to detect the right target layer and to measure the depth.

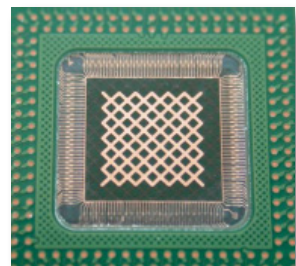


Figure 2: Buried chip.

This type of depth routing technology allows designers to sink in a chip below the board surface and design a second chip above it. Routing leaves a square donut in between the connections of the two chips. Accuracy is within $\pm 15 \mu\text{m}$.

This advanced design causes fewer EMC problems due to the symmetry and the short distance between the components instead of using long tracks to connect them. However, the real challenge is to evacuate the heat from in between the two components. This issue can be addressed by implementing an air channel and integrating the heat pipes.

Option 3: Routing semi-flexible FR4 and rigid-flexible PCBs

Depth routing for semi-flexible FR-4 and rigid-flexible boards will be used if your board designer

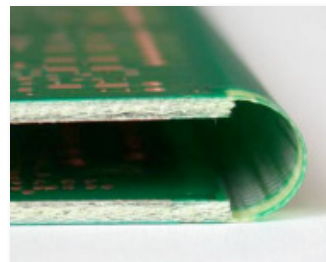


Figure 3: Bended board.

Application	Top surface		Innerlayer	Table
PCB construction	Conductive top surface	Non conductive top surface	Grounded innerlayers	Non conductive top surface
Machine equipment	Blind hole	2 nd measuring system	Blind hole + grounding	Blind hole + template
Accuracy (Posalux specification)	±15 µm	±40 µm	±15 µm	±20 µm
Routing possibilities	Single contact		Single contact	Remaining thickness
	Mean level		Mean level	
	Following		Following	

Figure 4: Routing table overview.

requests a bended board (which can be folded once). A part of the board will be milled away with an accuracy of +/- 20 µm. As a result, the board can be bended, less space is needed and the product therefore can be smaller. Because there is no conductive area in which to measure, the table of the drilling/routing machine will be used to detect the depth (for detection methods, see Figure 4).

Detection Methods to Control Depth

In all of these applications the special challenge has to do with depth-controlled drilling and milling. CO₂ laser systems automatically stop cutting when contact has been made with the copper on the inner layer. Mechanical systems require very precise measurements and feedback to achieve exact depth control. With the different available applications and products available, various measurement types are possible and necessary.

Contact Drill and Routing with Single Contact Measurement

With contact drill, each hole is individually measured. With this method, the desired result (through mechanical microvia drill-

ing) can be achieved. The drilling tool is electrically connected and makes contact with the copper foil surface. A known zero reference determines the hole depth. Base material warp is compensated and the consistent hole depths are ensured.

This becomes more difficult when we talk about routing. With a single contact measurement, surface determination will be done at the tool

entry location. The only reference point is the entry point and therefore, the depth remains constant during the entire routing process. The milled depth depends directly on the uniformity of material thickness. For relatively small boards and well defined top surfaces, traditional one point/single contact depth measurements may suffice. Note: Seldom is single contact routing used in the industry.

With thinner laminate layers and larger areas, it becomes more important to take the real differences of the substrate surface and thickness into account. Continuous monitoring and measurement or mean calculation become necessary.

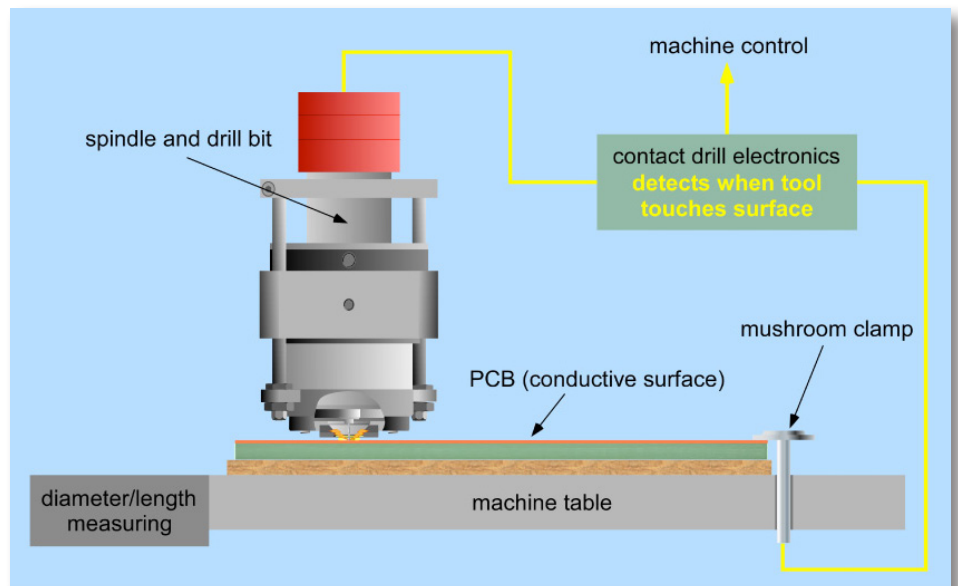
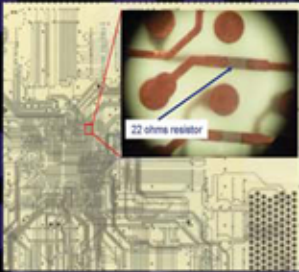


Figure 5: Closed loop.

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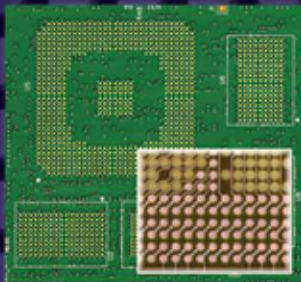


2010's

ORBIT®
Built-In-Trace
HDI resistor



Globalstar Satellite

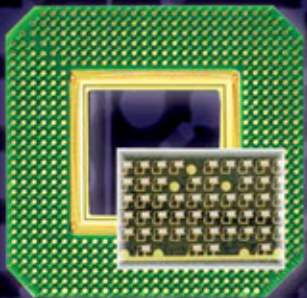


2000's

Series termination
under BGA device

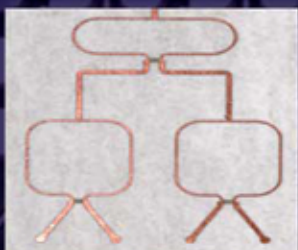


Mars Express Lander



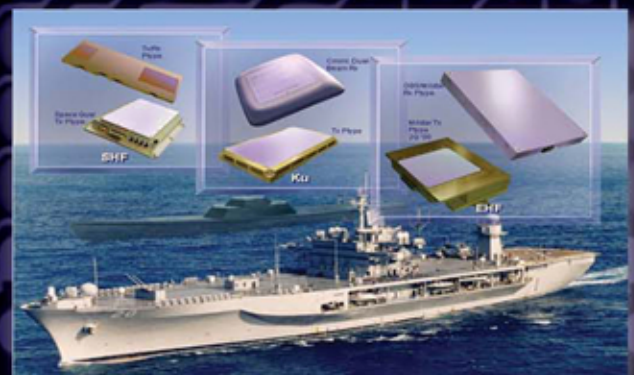
1990's

Parallel termination
of interposer board

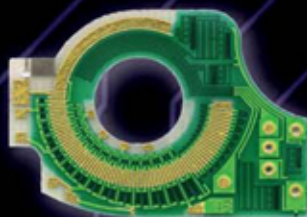


1980's

Power divider
RF application



Phased Array Antenna



1970's

Potentiometer
surface resistor

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Contact Drill and Routing with Mean Level Measurement

With mean level measurement, the surface level is measured at several locations. Several points with an electrical loop will be used. With the measured points and the received data, a mean contact level is calculated by interpolation. The routed depth is kept constant by the second measuring system (also called floating). The system allows for a depth-control accuracy of ± 15 microns throughout the operation.

Routing with Second Measuring Systems

Surface detection with a second measuring system does not need a conductive surface. Routing is accurately controlled by a z-axis servo. There are two measuring systems per spindle. The first determines the exact height of the tool at the point of entry. The reading head is fixed on the drilling head. The second measuring system is linked to the z-axis controller and controls the z-axis cutting depth and continuously compensates for surface topography. The linear scale is mounted on the pressure foot.

As soon as the pressure pad touches, the reading head starts to count. At first the difference between the tool and the pressure foot is measured. Then, the routing process begins (with the calculated depth). This measurement

method is less accurate (± 40 μm) than using a contact loop. Therefore, a workaround for BGAs is sometimes used. A single-sided copper foil on the backside of the chip can be integrated and a measurement can be done from there.

The pressure foot is also necessary because of the real board topography. The pressure foot will be used to achieve better results for applications with the flatness deviation of $> 0,4-0,5$ mm. The foot eliminates board lifting by providing downward pressure. This allows you to mill, route and drill without boards lifting from the table during the entire process.

Additionally, a single-spindle machine can feature optical registration and monitoring with a CCD camera. The routing picture will be aligned to the printed image. The camera recognizes the fiducials and will correct measurement calculations and apply them to the routing system.

Second Measuring System Routing with the Following Method

The most advanced method to measure depth is the following method, in which the spindle runs twice. First, it runs to find the conductive surfaces and then it begins to route. The copper's thickness must be at least 15 μm . The major disadvantage of the following method is speed. The method is approximately 200 - 250% slower than the mean method.

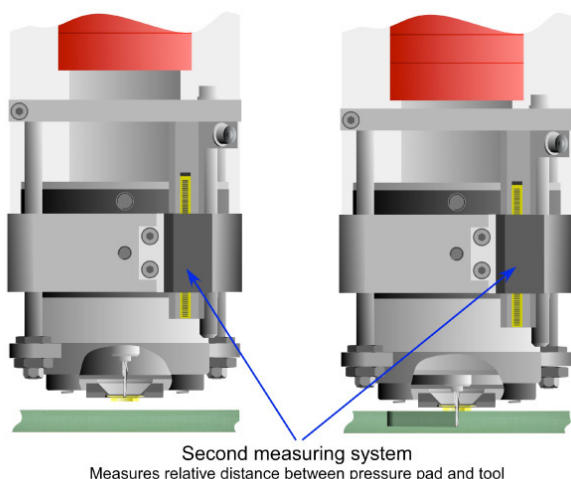


Figure 6: Second measuring system.

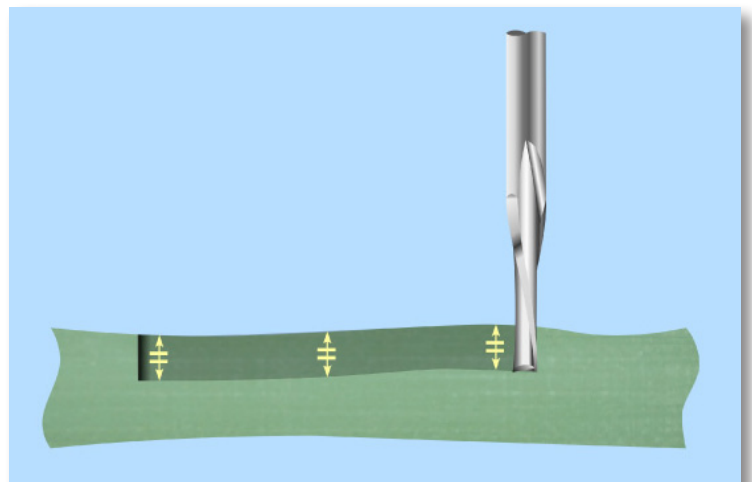


Figure 7: Following method.

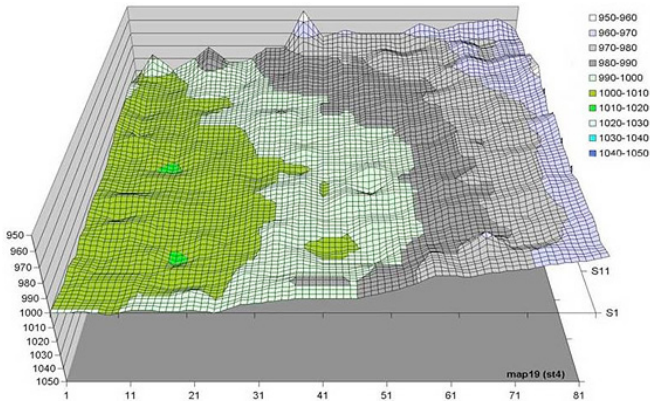


Figure 8: Mapped template data.

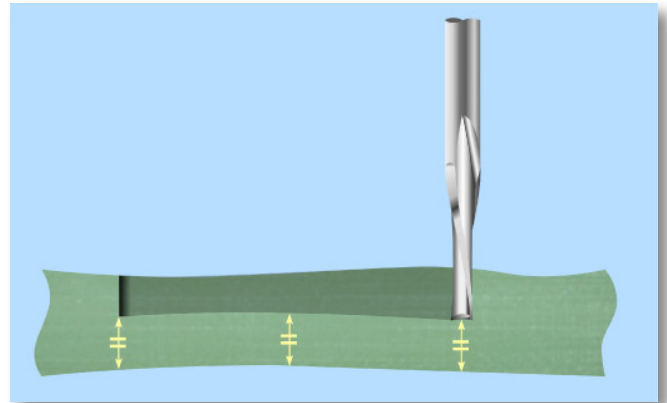


Figure 9: Measurement points.

Bottom of Panel Referenced Routing

With non-conductive top surfaces, the bottom of a PCB will be used as a reference to calculate the depth. This routing type is mainly used for rigid-flex FR-4 boards. The automotive industry, with applications like dashboards and ABS systems, and the telecommunication industry, with mobile phones, drive this technology in the main. The contact drill method is used to map an aluminium template. This mapped template data is used during routing to correct routing depth. This type of method is also used to separate the rigid-flex board.

Figures 10, 11 and 12 represent application examples.

Herbert Kläy, Director of the PCB division of the Swiss Equipment manufacturer Posalux, shared his views about the process and the future of the technology: "Today's customers'

needs for productivity and accuracy (with the miniaturization and the new set of products) can be handled with the above mentioned methods and technologies. Even aluminium backed PCBs for LEDs and the automotive industry can be processed. In our developmental strategy it is expected that more R+D developments and improvements will be made over the next coming years."

The development of CO₂ lasers should also be watched closely; however, as of today, lasers are no real alternative for depth routing. If one has to deal with large areas and larger material volumes on boards, productivity is the main challenge and R&D departments have only started to experiment with the technology for depth routing. When it comes to larger boards heating up, limited flexibility and scanning processes become additional problems. There-

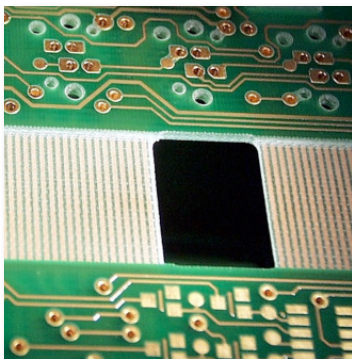


Figure 10: Slot routing.

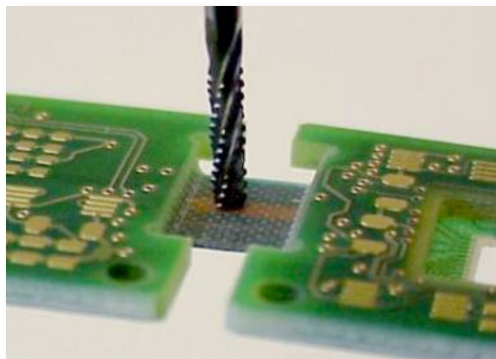


Figure 11: Volume routing (at bended boards).

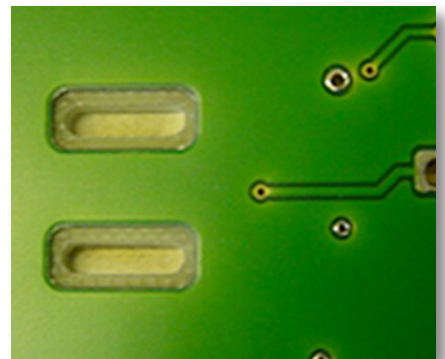


Figure 12: Special contours/ applications.

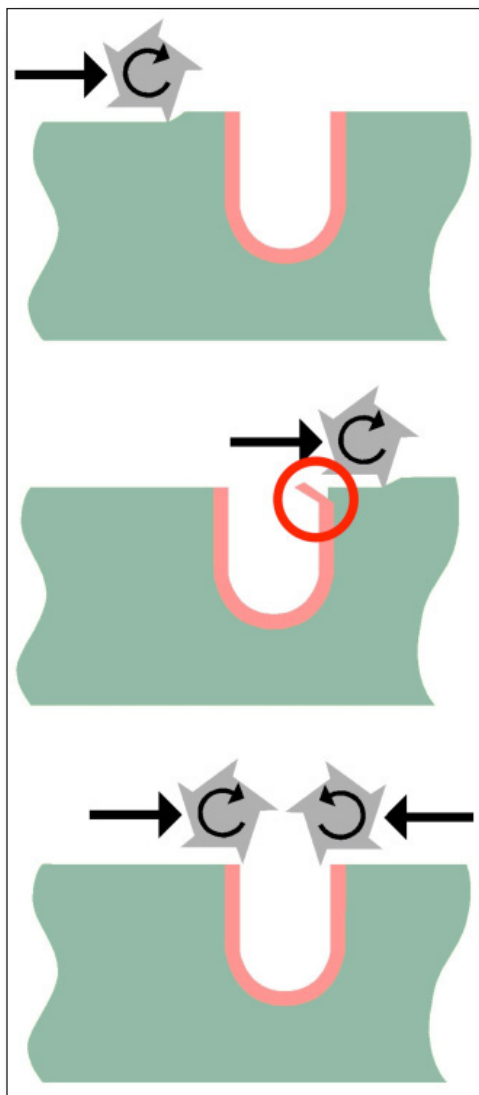


Figure 13: Inversed routing.

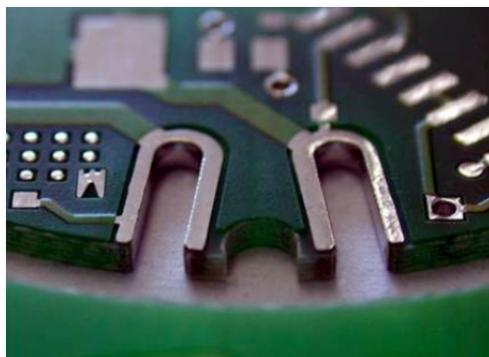


Figure 14: Inversed routing automotive application example.

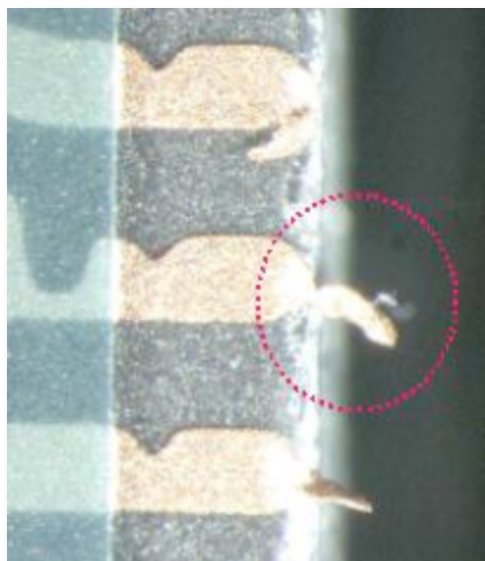


Figure 15: Burr A (example of a metal burr issue).



Figure 16: Burr B (electrical short problem).

fore laser technology has not been fully adopted in the market yet, although short-term laser depth routing may be an alternative for small boards or build-up technologies on substrates. In a couple of years it will be apparent whether or not the laser technology path will be cost-effective. Laser machines can cost up to 1-2 times more than single drilling machines. The productivity benefit may also be visible if there are many blind holes on the products. Most laser drill systems using a single laser source limit speed and productivity. Many laser systems are using $> 4 \text{ J/cm}^2$ for opening the Cu surface.

With organic materials like polyimide or epoxy resins, only 100 mJ/cm^2 is needed. This is a wide spectrum and the laser system demands a very advanced energy control to handle the various types of drilling steps.

The system's flexibility is also limited due to the fact that you must first decide which wavelength is best, keeping ablation performance, materials and absorption ratio in mind. The laser spot size (70 um with CO_2 lasers) is an additional challenge in drilling microvias. Another constraint is the mechanical board design, which might not deliver the same qual-

ity and repeatability in the micrometer range. Therefore, there is still sufficient scope for the use of mechanical drilling and routing.

The Swiss drilling and routing machine can be configured with asynchronous drilling and routing spindles, which have a rotation speed ranging from 15,000 – 125,000 rpm and a tool diameter range of 0.1 - 6.35 mm. If larger diameters and standard PCBs are used, synchronous routing spindles with a high torque at low speed and a speed range of 5,000 - 60,000 rpm can be used. In this case maintenance is lower and spare parts are relatively easy to find.

Conclusion

Mechanical routing technology is ideal for PCB manufacturers who target high-tech markets and prepare themselves for the customer's demands of today and tomorrow. Depth routing technology supports a high-end market with the need for accuracy, miniaturization, process stability and the need for productivity.

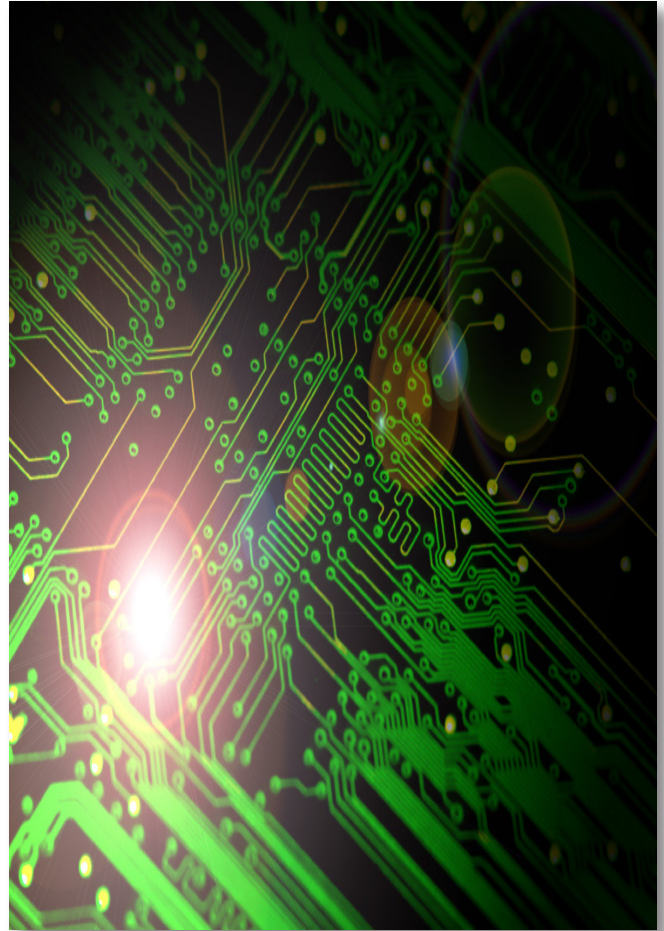
Key markets for routing technology include telecommunications, automotive and niche markets such as aerospace.

A significant advantage of the mechanical routing process is flexibility. Mechanical routing processes can offer a wide range of applications and the use of organic and non-organic materials like polyimide or epoxy resins, copper and brass PCBs with ceramic insulation layer and alloys (aerospace products). Routing with oil mist for non-ferrous materials is also available.

Automatic tool changes and spindle direction turns (reversed rotation) offer accuracy and productivity. Due to this fact, burr issues will be reduced by routing from both sides. The different applications and detection methods to control depth offer a wide range of products which can be utilised.

The Swiss equipment manufacturer developed a sophisticated interpolation algorithm which improves the accuracy and productivity while routing complex contours. This method also considerably reduces the tool wear and increases the lifetime of the routing tool.

To use the described design options, some depth routing manufacturing know-how and the right equipment is necessary. Therefore, a



close relationship between designers and PCB manufacturers has proven to be helpful.

Moreover, in various markets there is a rising demand for this kind of high-end technology. PCB shops and markets might stand a better chance of differentiating themselves from their competitors by adopting depth routing technology. **PCB**



Volker Feyerabend is president of APROS Int. Consulting and Services. He has a degree in engineering and economics and has worked for Hewlett Packard, Agilent Technologies and Groz-Beckert in various international senior management positions. Feyerabend also headed a European outsourcing organization with a focus on EMS/ PCB companies. Contact him at Info@APROS-Consulting.com.

Case Study: PTH Voids

by **Michael Carano**
OMG ELECTRONIC CHEMICALS

Summary — Troubleshooting means getting to the root cause of a defect in order to minimize yield loss and make significant process improvements. This edition of Trouble in Your Tank presents an actual case study that allows the reader to apply his or her knowledge gained from past columns.

Troubleshooting means getting to the root cause of the defect or defects so that one can minimize yield loss and make significant process improvements. This edition of Trouble in Your Tank presents an actual case study that allows the reader to apply his or her knowledge gained from past columns.

For this first case study, the fabricator is experiencing a serious PTH voiding problem. This problem did not appear until the fabricator began building part numbers with a different resin system (at the customer's request). Interestingly, the fabricator was able to build the same part number with a different resin material (lower Tg) without issue. The engineers focused on the desmear and electroless copper processes in order to gain a better understanding of the root cause of the voids. Through a process of brainstorming and testing, the team identified the root cause of the voiding and as a result, made significant improvements in the metallization process.

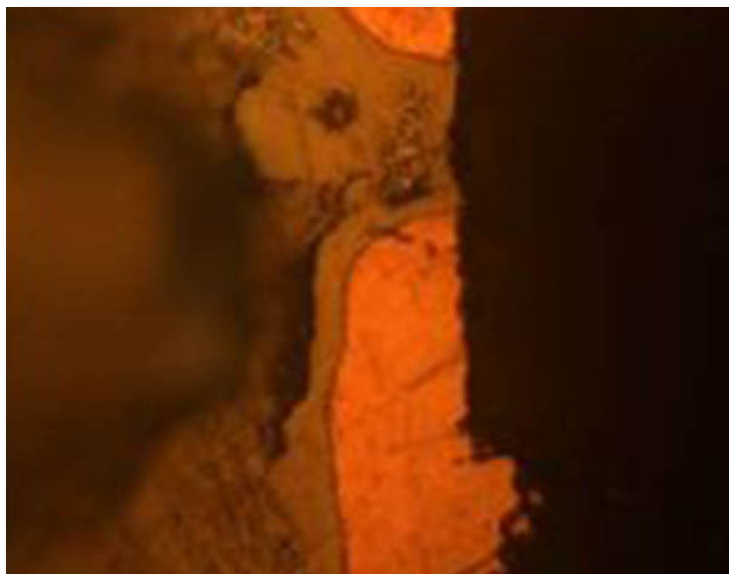


Figure 1: Classic PTH void.

Introduction

You have now had the opportunity to read several of these columns dedicated to presenting and solving PCB issues related to quality and reliability. For this month's column, the author would like to present a case study of an actual situation that occurred in a PCB facility. No names or organizations will be identified. This case study is used to simply build on many of the topics presented in this series. The case studies will test your knowledge of the process and hopefully stimulate your critical thinking skills as to the identification, root cause and corrective actions needed to restore quality and reliability. I encourage you to respond to mike.carano@omgi.com or [www.twitter.com/mike-carano1](https://twitter.com/mike-carano1) to make your own suggestions or further the discussion. In all cases, your comments

will not be retweeted or published without your expressed written permission.

Presentation of a Technical Issue It is an all-too-familiar story. A PCB fabricator is clicking on all cylinders. Processes are under control. The company feels confident to take on some additional work for a large and loyal customer. The end-user needs some new designs and requires a

different material set to be used in the build. The board design itself is not overly complex. The board thickness for the new design was 3.0



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John Martin
Electronics Lab Manager
Badger Meter, Inc.

...and of course the customer is always right!

mm and the smallest hole size is 0.3 mm. A similar design has been fabricated (and continues to be) in the past with a different material set. There have been no issues of PTH voids. However, with the new material set, the incidence of voiding has increased significantly. A typical void found on a microsection is shown in Figure 1.

What is the thought process? First, as a troubleshooter, are you certain this is related to the electroless copper process only and not something else? Are there other factors that could be contributing to the cause of the defect? As one examines the micro-sections, the shape or characteristic of the voided area yields some very important clues. Notice the tapered ends of the plated copper. In Figure 2, one sees the beginning of the pin-hole void. Again, notice the taper in the electroplated copper. What does this indicate?

One thing that is obvious with the taper is that the void was not caused by any issues with etch-outs (after tin strip and etch) or air bubbles in the acidic copper electroplating step. The taper indicates propagations voids — meaning that there was no electroless copper in this area prior to electroplating. While it may be possible that the micro-etch prior to pattern plating may be the root cause (did you think of that?), the troubleshooting team reviewed etch rate panels from the various in process checks imposed by engineering. Satisfied that the cross-check

on the micro-etch prior to pattern plating indicated that etch rates were in spec, the team decided to build test panels to determine the root cause of the pin-hole voiding issue.

The team decided to build identical panels. One set would be built with a standard FR-4 material, the other set with the new material. As a matter of clarity, the second material set is described as a 175°C Tg, high-elastic modulus, low-CTE FR-5 equivalent. Twelve panels of each set were designed as daisy chain panels for easy analysis. Each panel (3.0-mm thick) contained 30,000 drilled holes, each hole being 0.3 mm in diameter.

The two sets of panels were processed through the permanganate desmear line, electroless copper, then imaged and sent to pattern plating. After pattern plating, the photoresist was stripped, then panels were etched and tin resist stripper was then sent to electrical test. It was clear from the first run that the second material (higher Tg) set showed a significantly higher incidence of voids. So, what would be your next step? First, the engineers should have examined the condition of the hole-wall immediately after desmear. Upon examination, there is a distinct difference between the standard material and the FR-5 (Figure 3).

Normal-Tg materials are much easier to be roughened by desmear than high-Tg materials. The rougher hole wall surface provides a better environment for electroless plating. In contrast, high-Tg materials are difficult to roughen by desmear as these materials are more chemically resistant. The smooth hole wall surface makes it more difficult for the palladium catalyst to adhere. This influences catalyst adsorption which in turn affects the deposition of the copper. Lower catalyst adsorption on the resin will lead to lower copper plating thicknesses and voids.

Now what? Change materials? Sorry, the end-user requires this particular material for reasons that cannot be disclosed here. So, when this author was asked to look at the situation, the idea was to look closely at a few areas that were not previously disclosed. What do you think that entailed?

Well, the first step was to walk the line to again look for anything that seemed out of the

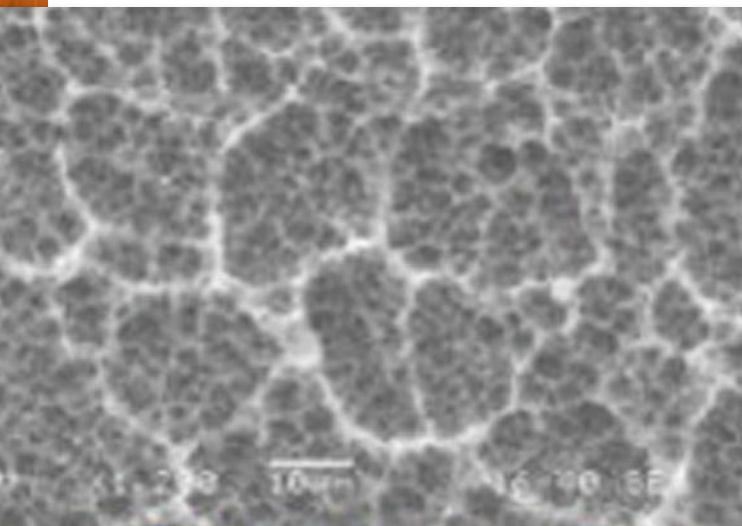


Figure 2: Beginning of pin-hole void.

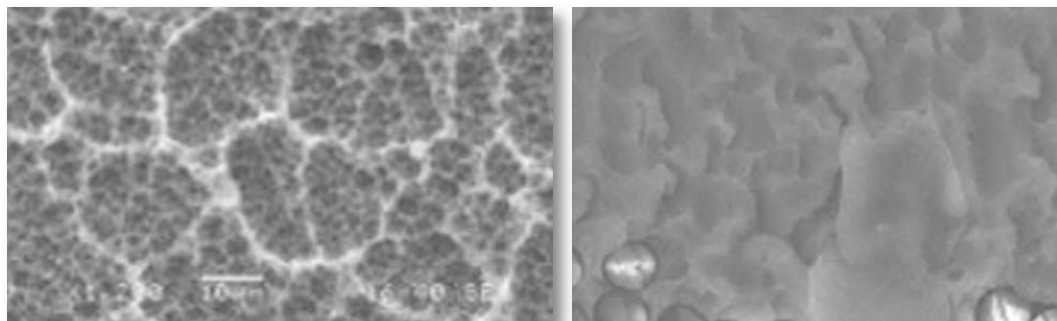


Figure 3: Standard FR-4 (left) and FR-5 (right).

ordinary. The chemistry was in spec according to the supplier recommendations. However, the author did notice air agitation in the rinse waters after catalyst and in the catalyst process tank itself. There was also a lack of vibration in the electroless copper tank. This raised concern. First, using vibration on the plating racks in the electroless copper tank and the catalyst tank is a proven process modification known to reduce the incidence of voids, particularly in small-diameter vias. Secondly, air agitation is not ideal, especially in the catalyst tank. Air agitation can impact the catalytic activity of the palladium. When this occurs, voids are the end result.

It was recommended to set up a second test run. This time, the plating would include trial runs with the air agitation as described above, turned off to provide a direct comparison. Twenty-four test panels (daisy chain) were built — this time twelve panels with the FR-4 material and twelve with the FR-5 material. These two sets were split into two. One set would be processed with air agitation in the catalyst and catalyst rinse and the second set of each material set processed with the agitation off. After completing the plating and remaining fabrication steps, the test panels were electrically tested to measure the extent of opens (voids in the vias).

The results showed that:

- Air agitation in the catalyst and catalyst rinse tank were a main cause of voids
- The best way to avoid pin-hole voids is to turn off the agitation due to the effect on the palladium catalyst
- The type of resin material has an effect on voids as discussed previously

electroless copper tank set-up and vibration parameters.

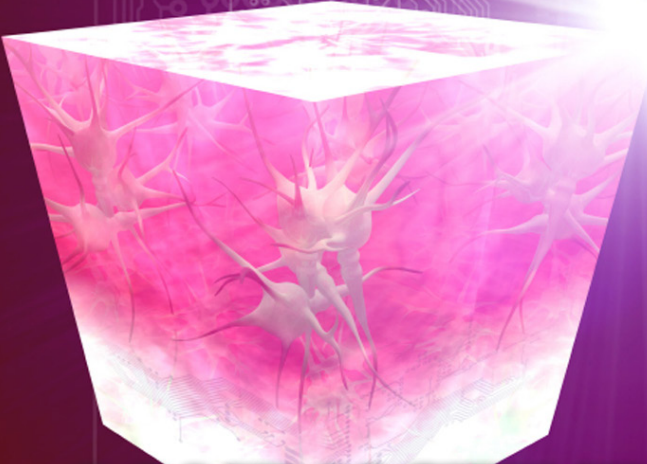
Summary

PTH voiding can originate from many sources. In this case study, resin material used in the fabrication of the circuit boards appeared to be the root cause of the voids. In addition, other process improvements were required. As an example, care must be taken to not introduce air in the palladium catalyst process step due to concerns about oxidation. In addition, certain resin materials, depending on the chemical make-up, may have greater tendency to void than other materials. Ensuring effective catalyst adsorption through improved solution movement will help in preventing voids. Installing vibration in the catalyst and electroless copper plating tanks (in order to help improve solution movement in the PTH) has a positive effect in reducing PTH voids.

In the next edition of *Trouble in Your Tank*, additional information on different laminate materials will be presented. In particular, the focus will be on optimizing the desmear process to ensure a void-free copper deposit. **PCB**



Michael Carano is with OMG Electronic Chemicals (formerly Electrochemicals), a developer and provider of processes and materials for the electronics industry supply chain. He has been involved in the PWB, general metal finishing photovoltaic industries for over 29 years. Carano holds nine U.S. patents in topics including plating, metallization processes and PWB fabrication techniques.



CONDUCTIVE ANODIC FILAMENTS:

The Role of Epoxy-Glass Adhesion

by Seth Binfield, Dr. Craig Hillman,
Thomas Johnston, and Dr. Nathan Blattau
DfR SOLUTIONS

SUMMARY — *Glass fibers used in glass ply have a chemical coating, or size, applied for lubrication which prevents fractures and for adhesion between the fibers and resin. In this co-authored article by DfR Solutions, the role of epoxy-glass adhesion in conductive anodic filament formation is explored.*

All glass fibers used in glass ply production have some form of sizing applied before the weaving process to ensure sufficient lubrication and prevent fracture. In conventional glass production, fibers are drawn from molten glass and a starch-oil sizing is applied. This sizing provides mechanical integrity and lubrication for subsequent processing. Warp yarns, corresponding to the grain direction in the laminate, are then coated with a second sizing for additional protection. The sizing applied to the glass fibers is subsequently removed by a thermal decomposition process and the fabric is coated with a silane finish to provide a chemical coupling and ensure bonding between the glass surface and the resin matrix.

Depending on the laminate manufacturer, the silane finish may be applied by the glass fabric supplier or in-house. The silane finish is often applied before the impregnation of the epoxy resin. There are several factors that drive the effectiveness of silane in retarding or preventing CAF events, including degree of coverage, density of coverage and ratio of bound to unbound siloxanes.

Bonding Process

The precise nature of the mechanism in which silane increases adhesion is not entirely understood. Silane coupling agents modify the interface between organic resin surfaces and non-resins to improve adhesion. It is thought that the silane coupling agents form bonds with the glass surfaces and resin matrix through the silane functional group. Hydrolyzed silanes condense to oligomeric siloxanols and eventually form rigid cross-linked structures. The bonding to a polymer matrix may take various different forms. Bonding may be covalent, where the siloxanol is compatible with the liquid matrix resin. The solutions might also form an interpenetrating polymer network as the siloxanols and the resins separately cure with only limited copolymerization.

The interfacial region between the glass fiber and epoxy resin varies from tightly bound siloxanes at the fiber wall to unbound siloxanes blending into the epoxy matrix. Unbound siloxanes permit penetration of the epoxy resin into the interface region and strengthen the ep-

“ Silane coupling agents modify the interface between organic resin surfaces and non-resins to improve adhesion. ”

oxy-glass bond, while tightly bound siloxanes restrict moisture absorption. The proper ratio of bound to unbound siloxanes results in the optimum interface.

A further optimization process involves balancing the degree of residual stress present at the interface. As an example, a method of increasing adhesion is to improve the reactivity of surface treating agents with the epoxy resin by varying the number and kinds of the organic functional groups on the silane coupling agents. However, the improved reactivity with resins can result in a thin, rigid layer on the interfaces that can induce residual stress at the interface. The use of surface treating agents together with long chain polysiloxanes will reduce the residual stress, but will tend to decrease intrinsic interfacial adhesion because:

- The reactivity of surface treating agents with long chain polysiloxanes is poor under usual treating conditions.
- Long chain polysiloxanes have no alkoxyl groups reactive to base materials.
- The hydrophobic groups, such as methyl groups, on long chain polysiloxanes disturb the impregnation of base materials with the long chain polysiloxanes.

Silane Chemistry

The choice of silane chemistry and other finish additives is often driven by compatibility with the epoxy resin formulation and is considered highly proprietary by most laminate manufacturers. These coupling agents will influence fiber-resin interaction through changes in surface properties such as surface energy and bonding site availability. The coverage of the silane will be driven by the weave, surface preparation of the glass and the application process. The amount and composition of silane also depends on process factors, such as pH and cure conditions. Combined, material selection and manufacturing parameters will drive the final quality of the interfacial bond.

There are numerous types of silanes available for laminate production. Some older examples are shown in Table 1. More recent formulations include epoxysilane coupling agents, such as γ -glycidoxypropyltrimethoxysilane, aminosilane coupling agents, such as N- β -(N-vinylbenzylaminoethyl)- γ -aminopropyltrimethoxysilane, hydrochloride, cationic silane coupling agents, vinylsilane coupling agents, acrylsilane coupling agents, and mercaptosilane coupling agents. These may be used individually or in a combination of two or more in desired ratios. Hexcel-Schwebel and

Mechanical Strengths of Epoxy Laminates (MPa), (G-10 Formulation with Style 7678 Glass Cloth)

Finish on glass	Initial		2-H boil		200-H boil	
	flex	comp	flex	comp	flex	comp
None	448	290	—	—	—	—
Chrome complex (Volan® A)	503	345	421	282	227	138
$\equiv \text{SiCH}_2\text{CH}_2\text{CH}_2\text{Cl}$	586	324	503	310	345	241
$\equiv \text{SiCH}_2\text{CH}_2\text{CH}_2\text{NH}_2$	544	338	482	303	353	234
$\equiv \text{Si}(\text{CH}_2)_3\text{NHCH}_2\text{CH}_2\text{NHCH}_2\text{C}_6\text{H}_5$ HCl HCl	586	365	455	338	324	320
$\equiv \text{Si}(\text{CH}_2)_3\text{NHCN}_2\text{CH}_2\text{NHCH}_2\text{C}_6\text{H}_4\text{—CH=CH}_2$	586	358	550	310	413	310
$\equiv (\text{CH}_2)_3\text{OCH}_2\text{CH}(\text{O})\text{CH}_2$	509	339	457	332	322	221

Table 1: Examples of some common silane coupling agents used in FR-4 epoxy laminates.

Dow Corning currently have a significant share of the silane marketplace for glass ply production, with Dow Corning's Z-6032, vinylbenzylaminoethylaminopropyltrimethoxysilane [C₆H₄-CH₂-NHC₂H₄NHC₃H₆-Si(OCH₃)₃] especially popular due to its high water resistance and status as a universal coupling agent that is successful with various epoxies.

However, changes in silane selection are ongoing as epoxy chemistry is constantly modified, fillers are added to FR-4 formulations, and cost is the dominant driver in material selection within the electronics supply chain. As an example, Z-6032 tends to have a higher price due to some rare raw materials and product instability that requires cooling during transportation and storage.

Glass/Epoxy Interfacial Characterization and Control

After the impregnation of the glass fabric with the epoxy resin, direct characterization of the interfacial chemistry is difficult and often not performed. As such, reverse engineering of interfacial chemistry is not a practical enterprise. However, the laminate manufacturer should have processes and procedures in place to characterize the silane finish and its compatibility with the epoxy resin blends.

If silane finishes are applied by a supplier, the laminate manufacturer should have controls in place to confirm the silane finish. If multiple finishes are used, there should be a process in place to identify each finish. Resin can also be crucial and evidence of systems to ensure adequate control is also necessary. These include resin lot conformance checks for content, molecular weight and impurities.

Qualification Requirements

The primary process for ensuring good bonding at the glass/epoxy interface, outside of CAF testing, is the use of the test method IPC TM-650 2.6.16 *Pressure Vessel Method for Glass Epoxy Laminate*. This test method requires exposing laminate coupons to pressure cooker conditions (121°C, 100%RH, 15 psi) for 30 minutes and then immersing the coupons in a solder pot heated to either 260°C or 288°C.

The pressure vessel test method is called out in IPC-4101B *Specifications for Base Materials for Rigid and Multilayer Printed Boards* as an optional test as agreed upon between user and supplier. If the test is incorporated, IPC-4101B recommends that it be used for both conformance and qualification testing, with testing performed on every lot. The test method provides a grading system of 1 to 5, with laminates graded 4 to 5 often rejected by the PCB supply chain. **PCB**



Craig Hillman, Ph.D. is CEO and managing member of DfR Solutions. Dr. Hillman's specific expertise includes best practices in design for reliability (DfR), execution and implementation of strategies for managing environmentally-friendly electronics, qualification of new technologies and market acceptance and successful product development processes.



Dr. Nathan Blattau is senior vice president of DfR Solutions and has been involved in the packaging and reliability of electronic equipment for more than ten years. His specialties include best practices in design for reliability, robustness of Pb-free, failure analysis, accelerated test plan development, nonlinear finite element analysis, solder joint reliability, fracture and fatigue mechanics of materials.



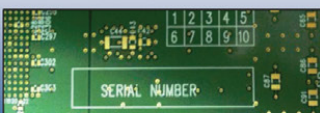
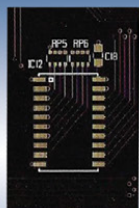
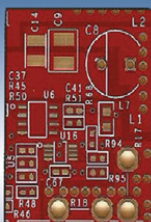
Seth Binfield has been a technical staff member at DfR Solutions for more than five years. His areas of expertise include analytical chemistry methods and equipment, and their application to the materials in, as well as contamination and cleanliness of electronic products. Binfield may be reached at sbinfield@dfrsolutions.com.



Thomas Johnston
As of presstime, no bio was available.

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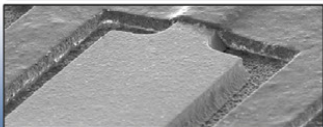
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Recommended Reading:
***"Why Inkjet for PCB has become
a Reality"*** by Guy Alon and
Ron Ellenbogen of Orbotech

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A Cautionary Tale

by Steve Williams

Summary — As we all look to improve our manufacturing organizations in 2012 and become leaner and meaner, the fictitious canoe story is a reminder to focus on the right things and concentrate on activities that will improve the bottom line.

Once Upon A Time...

A very large American manufacturer and its equally large Japanese competitor decided to hold an annual canoe race between the two companies, with the winner securing bragging rights for the following year. Both teams were given 30 days to develop their strategy and prepare their teams to reach peak performance before the race.

On the big day, Team Japan won by a mile.

Team America, very discouraged and disappointed, decided to investigate the reason for the crushing defeat. A canoe steering committee of senior managers was formed to investigate the root cause and recommend appropriate action. After months of meetings, action items and strategic analysis, their conclusion was that Team Japan had eight people rowing and one person steering, while Team America had eight people steering and one person rowing.

Unsatisfied with the internal conclusions and feeling that a deeper study was in order, Team America's management hired the prestigious Williams Consulting firm and paid them a large amount of money for a second opinion. After considerable time and great expense, Williams Consulting advised, of course, that too many people were steering the canoe, while not enough people were rowing. Not sure how to utilize that information, but wanting to prevent

another loss to Team Japan, the rowing team organizational structure was re-aligned into:

- 4 Steering Supervisors
- 2 Area Steering Managers
- 2 Steering Directors
- 1 Rower

They also implemented a new pay-for-performance program that would give the one person rowing the canoe greater incentive to work harder. The program was launched with much fanfare and named "Team High Incentive Canoe Kickoff" (THICK), with meetings, dinners and free pens for the rower. There was discussion of getting new-technology paddles, canoes and other equipment, extra vacation days for practices, and bonuses.

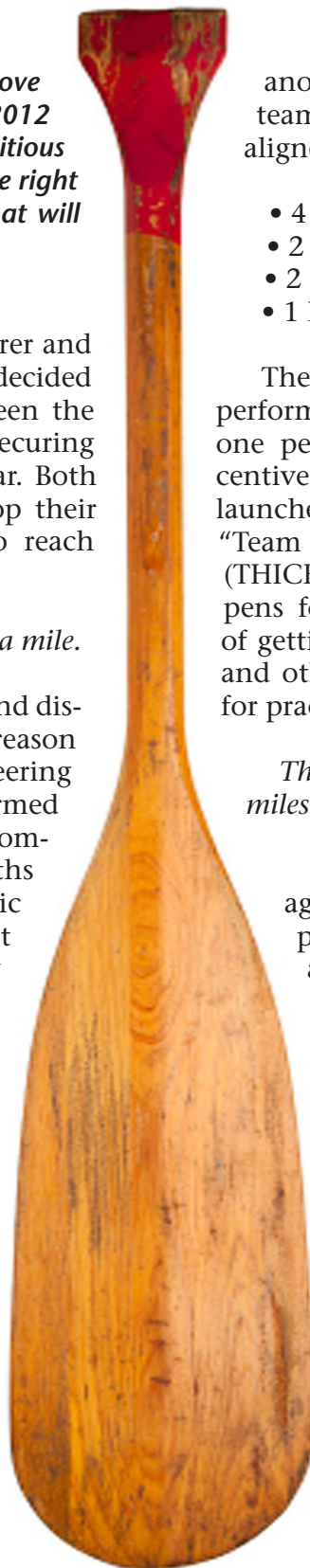
The next year, Team Japan won by two miles.

Humiliated, Team America's management laid off the rower for poor performance, halted development of a new canoe, sold the equipment and canceled all capital expenditures for new technology. The money saved was distributed to the senior executives as bonuses. The following year the racing team was outsourced to India.

Steve's moral of the story: If Team America doesn't start working smarter in the manufacturing sector, we will be destined to remain a service nation.

Art Imitates Life

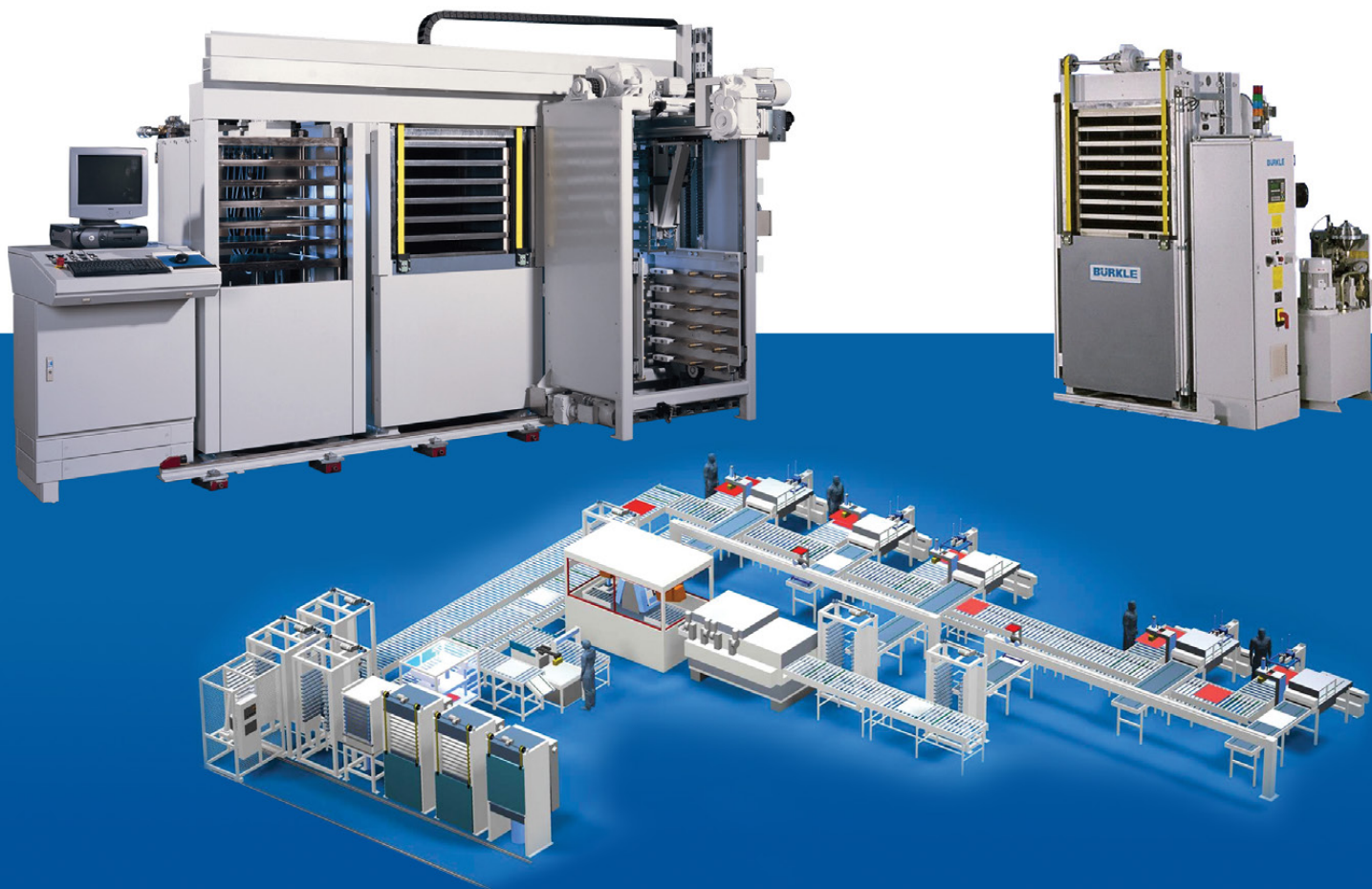
Is this story so far-fetched? I would suggest that a quick look through recent headlines of any



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major newspaper would provide ample examples that it is not. While the excesses of high-profile companies such as Tyco, WorldCom, Enron and Solyndra have been well publicized, corporate irresponsibility can be found at every level in the business world. Examples abound of senior executives that have been incentivized for short-term performance at the expense of long-term corporate health. The award of multi-million dollar golden parachutes to CEOs that are fired for underperformance is commonplace. Personal agendas trump stakeholder value. Has the whole world gone crazy?

Decades ago it began in the automotive industry; everyone remembers the big push to “buy American” when Asia’s automotive companies began to penetrate the U.S. market in a big way. This finally fizzled out when people began to notice (at that time) that these automobiles were not only less expensive, but were also built better. There is a reason some of these companies began offering 10-year, 100,000 mile warranties when most U.S. automakers were still offering 3-year, 36,000 mile warranties. They know that, statistically, the risk of having to pay-out on this warranty is within an acceptable number because of the product’s quality.

Author’s note: As 3/36 warranties are still common, I would like to know what these people are smoking who are telling us the average person drives only 12,000 miles per year. The average 36,000 mile warranty is realistically only about 1½ - 2 years of coverage. Considering that an automobile is generally the second most expensive purchase for

the average consumer, this warranty is not only embarrassing, but totally unacceptable.

Take a Lesson

I have to give credit where credit is due; the U.S. automotive industry has made great strides recently in the areas of product quality, reliability and warranty. However, to fully appreciate this we must examine the motivation behind this improvement. Did the folks in Detroit determine that the American consumer deserved a better quality automobile out of the goodness of their hearts? Hell no, they did it because their foreign competition was kicking their collective butts, stealing market share and seriously threatening to put them out of business.

As we look to retrench our operations during 2012, be sure to remain focused on the right things for the long-term sustainability of not only our organizations, but our industry. Heed the caution of this tale and don’t get caught being one of the companies with eight people steering and only one person rowing. **PCB**



Steven Williams is a 35-year veteran in the electronics industry and an authority on manufacturing and management. He is currently the commodity manager for a large global EMS provider, a distinguished faculty member at several universities and author of the book *Survival Is Not Mandatory: 10 Things Every CEO Should Know About Lean* (www.survivalisnotmandatory.com).

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– Eric Anderson, Electrical Engineer
Beijer Electronics Inc.



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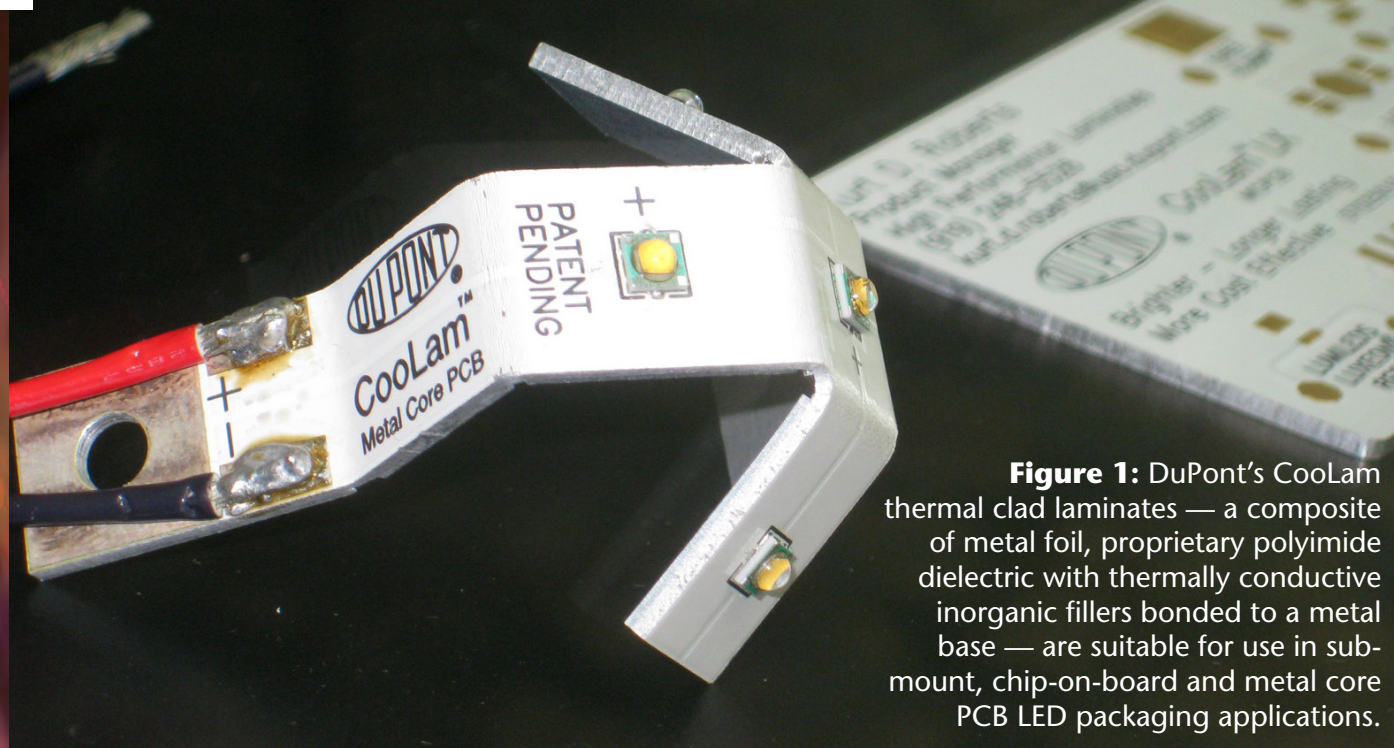


Figure 1: DuPont's CoolLam thermal clad laminates — a composite of metal foil, proprietary polyimide dielectric with thermally conductive inorganic fillers bonded to a metal base — are suitable for use in sub-mount, chip-on-board and metal core PCB LED packaging applications.

DuPont Talks Development Trends and Highlights in PCB Materials Industry

by **Richard Ayes**
I-CONNECT007

SUMMARY — *In the last few years, the growth in mobile electronics has been driving the trend toward PCB materials that are thinner, lighter and more capable. DuPont Global Business Manager Peter A. Irvine shares his view of the PCB materials industry for 2012.*

In an interview with I-Connect007, Peter A. Irvine, global business manager, DuPont Circuit and Packaging Materials, discusses the latest developments and supply chain issues in the world of PCB materials during the past year, as well as some of the growth drivers for 2012. He also shares his outlook for the industry this year, and points out a few challenges that companies will continue to face.

How did the PCB materials industry perform in 2011?

After a strong first half of 2011, the second

half of the year was softer than normal; but overall, the PCB materials industry was up in value slightly in 2011 versus the previous year. There was value for high-performing materials. The global economic uncertainty made customers more conservative about inventory management and order placement, at all levels of the supply chain. Toward the year-end, forecast availability seemed to decline as customers seemed disinclined to commit, absent confirmed order placement from their customers.

What were some of the key developments in PCB materials last year?

Most active developments were for high-speed and thermal substrates. New applications are moving to flex or rigid-flex for assembly due to space and weight considerations. The speed of rapid prototyping has increased even as technical requirements grew in complexity. Customers continued to move to laser direct imaging (LDI) to meet many of these prototype requirements.

“ Most active developments were for high-speed and thermal substrates. ”

In terms of regulations, and with the increasing move towards green manufacturing, were there any significant standardizations during the past 12 months that significantly affect the materials suppliers? What about the challenges of lead-free processing?

We saw no major regulatory changes in 2011. DuPont has a strong commitment to product stewardship and sustainability as it continues to reduce waste, conserve energy and increase efficiencies wherever possible, and help its customers do the same. Meanwhile, the industry continues to develop laminate material with higher Tg and less propensity for warp. In flexible laminates, we see the continued migration towards adhesiveless polyimides.

Did you encounter any major supply issues last year?

Yes. Major global supply issues stemmed from the earthquake and tsunami in Japan in the first half of the year, and then the flooding in Thailand in the second half. Both events caused participants in the entire PCB supply chain to recheck their suppliers, both to evaluate the immediate impact of these disasters as well as to evaluate ongoing risks. Also in the second half, the economic uncertainty has, in some cases, made it more challenging for material suppliers to plan and serve customer needs due to limited forecast availability.

How has the PCB materials industry evolved over the past three to five years?

The key trend in the industry over the last three to five years has been primarily driven by the growth in mobile electronics, which has pushed the industry toward materials that are thinner, lighter and more capable. Customization of materials to achieve end-user specific needs has also been on the increase. For fabricators, there has been continued emphasis on finer lines and spaces, greater density on holes and pads, and faster lead times, all at higher yields and lower cost. There has also been a heavy focus for DuPont on addressing design challenges at the OEM level, with higher speed and frequency materials, thinner profiles and even more specialty materials to address aesthetic as well as performance properties.

How is 2012 shaping up for the company?

Overall, DuPont expects between 12 and 17% growth in 2012, with sales in the range of \$40-42 billion. Electronics is a key growth area for the company and DuPont continues to expand its portfolio for circuit and packaging materials, with new product developments focused on high-speed and high-frequency to meet increasing demand in consumer electronics, especially in tablets and smartphones.

What major challenges will materials providers face in the coming year?

Uncertainty in the global economy will make forecasting a challenge. The industry continues to need quicker response times all the way through the value chain for prototyping and mass production, even for customized materials. Accelerating innovations to accommodate consumer demands is another key challenge we expect to see. Helping fabricators quickly integrate new high-performance offerings in a way that will achieve high-yield, low-cost and reduce waste remains a priority to overcome these challenges. We're working in close collaboration with our customers to ensure their success.

On a global basis, in which regions do you see growing demand for the PCB materials?

Demand will be strongest in Brazil, Russia, India, China and other emerging economies as the desire for high-end, high-value electronics is accelerating at a greater rate than mature markets. The regions supplying these markets will be predictably impacted. Demand for PCB materials for the smartphone, tablet and ultra-microcomputer segments will grow at a greater rate than materials for slower growing end uses.

What are the latest material technologies on the anvil at DuPont?

DuPont leverages its expertise and experience with a core set of technologies, including high temperature/high performance polymers, photochemistries, fluoropolymer technologies, fine particle dispersions, and multilayer films and coatings to deliver innovations that drive improvements in a range of areas for consumer electronics, high reliability and industrial markets. For consumer electronics, developments

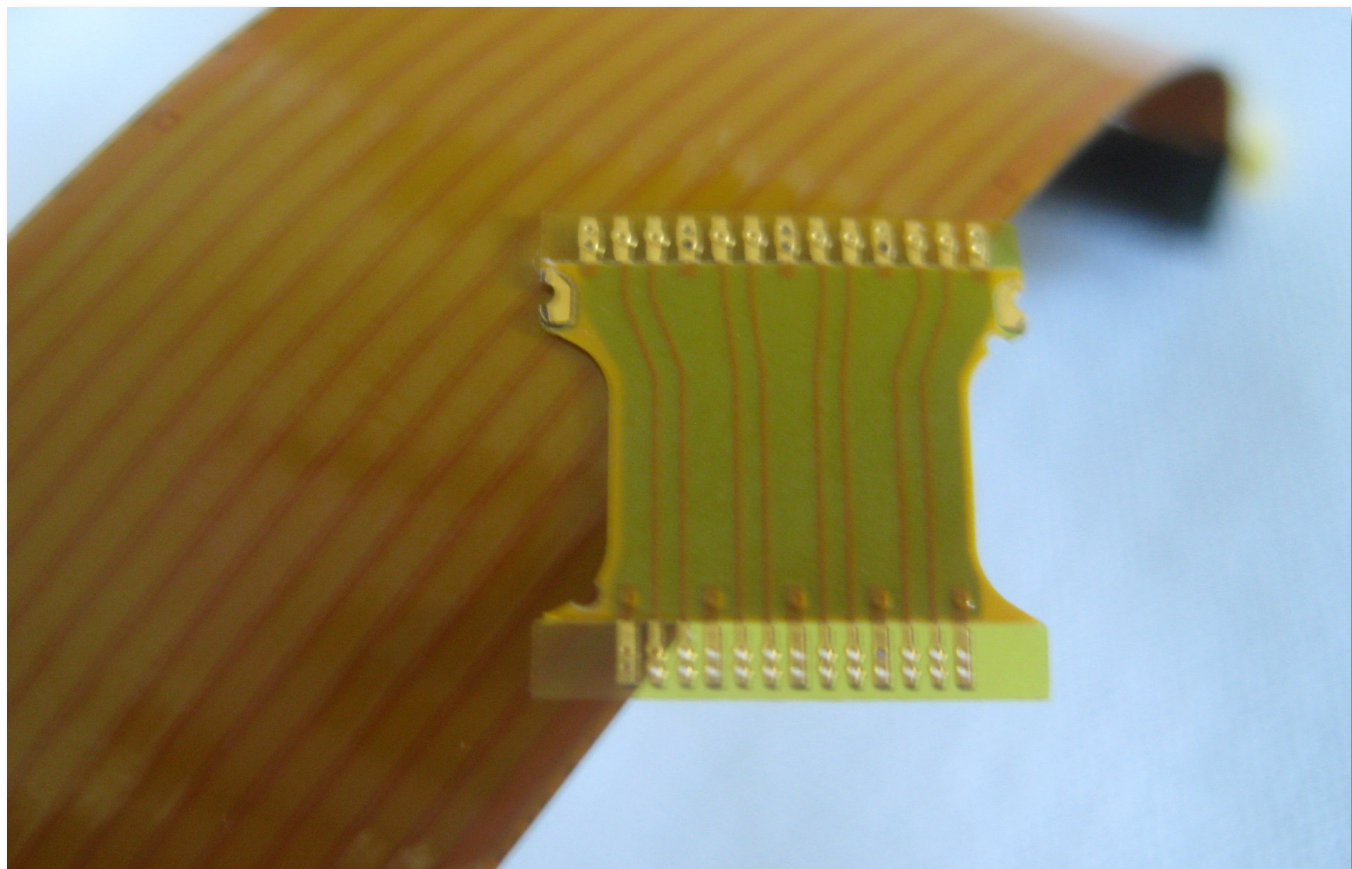


Figure 2: The Pyralux TK flexible circuit material is a copper-clad laminate specifically formulated with DuPont Teflon fluoropolymer film and Kapton polyimide film for high-speed digital and high-frequency flexible circuit applications.

focus on materials for smart phones and tablets with thinner and smaller form factors that can handle large and high-speed data rates. Ensuring high-reliability devices with signal integrity, low loss, controlled impedance, and temperature tolerance are continued drivers in high reliability markets. Other industrial applications focus on new energy and transportation needs, such as high-speed trains, photovoltaics and wind power, and thermal management for LED lighting.

Please enlighten us on some of the company's business initiatives in the coming year.

Across the corporation, DuPont will continue to focus on sustainable growth by meeting our customers' needs for advanced materials.

What is your view of the materials industry for the year ahead?

In the first quarter, we will be watching for positive indicators that the conservative orientation of customers in the fourth quarter of 2011 is beginning to lift. With growth trends expected to stay steady in the consumer electronics market, we hope to see a return to the growth curve that projects 5 to 7% at some point in 2012. **PCB**



Dr. Peter A. Irvine is global business director for DuPont Circuit and Packaging Materials, part of the DuPont Electronics and Communications business. Dr. Irvine has more than 25 years with DuPont and has held a range of leadership positions in sales, marketing, technology and business management within electronics.

Most-Read PCBDesign007 News Highlights This Month



Frontline's InSolver Enables Accurate Impedance Modeling

Powered by Mentor Graphics HyperLynx technology, Frontline's InSolver is a cost-effective PCB impedance field solver that enables fast and accurate stackup and impedance modeling for a wide range of PCB structures.

Bay Area Circuits Introduces Tools, Conversion Guide

To help PCB design engineers create and verify their PCB Designs, Bay Area Circuits has introduced a PCB array calculator, a free desktop Gerber Viewer, and a DXF/DFG-to-Gerber Conversion Guide.

PCB Designers Love This Book

We've heard it all before: There just aren't that many sources for PCB design information geared toward flexible circuits — until now. *Flexible Circuit Technology, 4th Edition* was published last fall, and PCB designers have been downloading it like crazy.

Zuken Names Chidester Head of International Marketing

Steve Chidester has been appointed head of international marketing, a strategic role that will draw on Chidester's 30-year experience in the electronic design industry. In this role, Chidester will oversee all marketing activities for Zuken in Europe and North America.

Mentor Graphics Appoints Three Executives

Mentor Graphics has appointed three new executives. John Lenyo has become vice president and general manager of the company's Design Verification Technology Division; Joseph Reinhart

has been appointed vice president of Corporate Development and Investor Relations; and Richard Trebing has been named corporate controller and chief accounting officer.

Zuken Releases New Version of Board Modeler Lite

Zuken has released a new version of Board Modeler Lite that offers significant productivity enhancements during board layout design. Board Modeler Lite 6.1, available now with CADSTAR 13.0, bridges the process between MCAD and ECAD design flows by offering a common platform to communicate between the two disciplines.

EDA Consortium Posts 18% Revenue Increase for Q3

The EDA Consortium (EDAC) Market Statistics Service (MSS) announced that the Electronic Design Automation (EDA) industry revenue increased 18.1% for Q3 2011 to \$1543.9 million, compared to \$1307.0 million in Q3 2010.

Top 10 Countdown: Most-Read Design Articles of 2011

It's been quite a year in PCB design. In 2011, stories about HDI or microvias usually drew a big audience and a column series on DDR design techniques went through the roof. Without further ado, we present the Top 10 most-read PCB design articles.

Board-Level Simulation and the Design Process: Plan B — Post Layout Simulation

by Barry Olney

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Summary — *Post-layout simulation covers batch mode simulation, which automatically scans nets on an entire PCB, flagging signal integrity, crosstalk and EMC hot spots. While post-layout simulation can be used for disaster recovery, ideally this process is completed during the design process.*

As with the film *Star Wars*, we are going to start this saga toward the end to see how the Imperial Empire has destroyed our system and then go back to the beginning to step through a methodology that will hopefully save us from this final painful and time-consuming step.

Unfortunately, board-level simulation is engaged too often towards the end of the design cycle. Ideally the simulation should be done during the design process to ensure design integrity. By following this year's series of columns on *Board-Level Simulation and the Design Process*, designers can be up-to-date on the best methodology to follow.

Plan B is basically disaster recovery. If, for instance, on the third iteration your product still does not meet specifications and management is pushing to have the project completed, then you need an alternative plan. However, if

the simulation is done during the design process, these re-spins can be avoided.

First, the post-layout board-level simulation requires the translation of the design files so that they can be read into the simulator. The simulation software interfaces to all major electronic design automation (EDA) PCB design packages. However, when there are issues with the translation of PCB databases, there is always another way via Spectra DSN or another PCB package.

The I/O Buffer Interface Specification (IBIS) models are required for all the major devices. Because IBIS models do not reveal the proprietary internal process or architecture information, semiconductor vendor's support of IBIS continues to grow and these days most models are available for download from the vendor's Web site. The IBIS format has proven to give reliable and accurate board-level simulation information.

A preliminary batch mode simulation is initially completed on the design. Default IC characteristics, crosstalk of 150mV maximum and EMC to FCC, CISPR Class A and B are set up in the simulator. The batch mode simulation au-

UNITS: MIL		ICD STACKUP PLANNER – www.icd.com.au							9/27/2011		Total Board Thickness: 61.2		
		Differential Pairs >				USB	DDR2	SATA	ETHERNET	LVDS			
Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled		
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description	
1	Top	Dielectric	3.3	0.5								Soldermask	
		Conductive			1.4	8	4	0.31	53.53	99.99		Signal	
2	GND	Dielectric	4.3	3								Prepreg	
		Conductive			1.4							Plane	
3	Inner 3	Dielectric	4.3	8								Core	
		Conductive			1.4	8	4	0.31	62.39	99.59		Signal	
4	VCC	Dielectric	4.3	12								Prepreg	
		Conductive			1.4							Plane	
5	GND	Dielectric	4.3	4								Core	
		Conductive			1.4							Plane	
6	Inner 6	Dielectric	4.3	12								Prepreg	
		Conductive			1.4	12	6	0.42	54.11	91.56		Signal	
7	GND	Dielectric	4.3	8								Core	
		Conductive			1.4							Plane	
8	Bottom	Dielectric	4.3	3								Prepreg	
		Conductive			1.4	4	4	0.31	53.53	89.98		Signal	
		Dielectric	3.3	0.5								Soldermask	

Figure 1: The perfect stackup for high-speed design.

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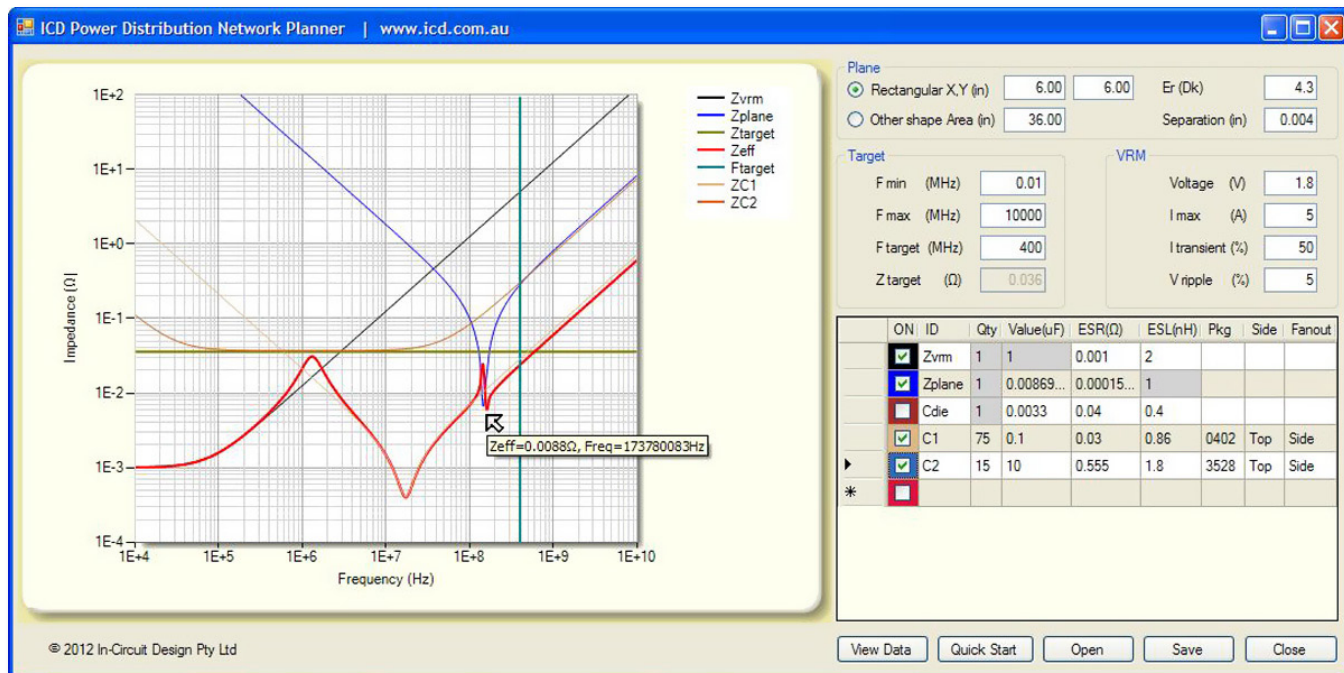


Figure 2: The ICD power distribution network planner illustrates the decoupling scheme.

tomatically scans large numbers of nets on an entire PCB, flagging signal integrity, crosstalk and EMC hot spots.

The post-layout simulation analysis can then be prepared using supplied specifications. This is an extensive interactive board-level simulation which takes the analysis to the next level — simulating trouble spots identified by the batch analysis in order to further resolve the issues with greater accuracy.

As part of the design for manufacturability (DFM) check, the board stackup is analyzed to ensure that both single-ended and differential impedances conform to the technology requirements. For example, USB differential pairs must be 90 ohms and the DDR2 clocks have to be routed to 100 ohms differential impedance; thus, the variables need to be adjusted to achieve this. However, the basic structure of the substrate remains the same — the dielectric thickness, copper thickness, etc.

Figure 1 illustrates the perfect stackup for high-speed design. This is calculated by the ICD Stackup Planner (download from www.icd.com.au). Good interplane capacitance can be achieved by using 4-MIL plane spacing, in the center, resulting in 241 pF/in² capacitance. This

reduces the power distribution network (PDN) impedance at high frequencies. Also, the stackup should be symmetrical about the center to ensure that the board does not warp during the PCB fabrication or reflow process.

The stackup should be checked for split planes; analog and digital sections should be examined, keeping the current return paths in mind. I generally use route fences to direct routes rather than splitting the planes, which can be disastrous. High-speed signals should not cross over analog areas.

Stitching vias should be used to connect all ground planes to provide a direct return path for signal currents. If the return current needs to cross over from a ground plane to a power plane (which can also be used as a reference plane) then a 100-nF capacitor should be placed next to the signal via, between the planes to provide this path.

Decoupling capacitors (DCAPs) supply instantaneous current (at different frequencies) to the drivers until the power supply can respond. In other words, it takes a finite time for current to flow from the power supply circuit (whether on-board or remote) due to the inductance of the trace and/or leads to the drivers.

Every decoupling capacitor has a finite series inductance which causes its impedance to increase at high frequencies. In order to reduce this inductance, as much as possible, a number of DCAPs should be placed in parallel, as close as possible to each power pin, using a thick, short trace. For example, if the vias are 20/8 MIL (pad/hole) then a 20-MIL trace should be used on the DCAPs.

The specifications, number and placement of all DCAPs should be reviewed. Figure 2 illustrates how the ICD PDN Planner is used to calculate the value and number of 10uF tantalums and 100-nF ceramic X7R capacitors required to keep the PDN impedance below the target impedance up to 400 MHz. The target impedance is determined by the switch mode voltage regulator characteristics and the allowable voltage ripple. The red line represents the effective impedance.

In this example, there are two anti-resonance peaks. The first, at 1.4 MHz, is formed

by the switched mode voltage regulator module and the 100-nF capacitors suppressed slightly by the tantalums. The second peak is around 173 MHz, which in this case happens to be the resonant frequency of the plane reacting with the 100-nF capacitors. These peaks are associated with the circuit formed after one capacitor (or regulator plane) has gone inductive and another capacitor is still capacitive — the classic parallel LC tank circuit. The most effective way to reduce the height of the anti-resonance is to minimize inductance.

This is, however, a trial-and-error process and you should keep in mind that every different value capacitor added creates another anti-resonance peak. And, even small-value DCAPs do not have much affect above 1 GHz, so in order to minimize the impedance at higher frequencies you may have to reduce the plane-to-plane spacing or use embedded plane capacitance if using high-frequency, fast rise-time devices.

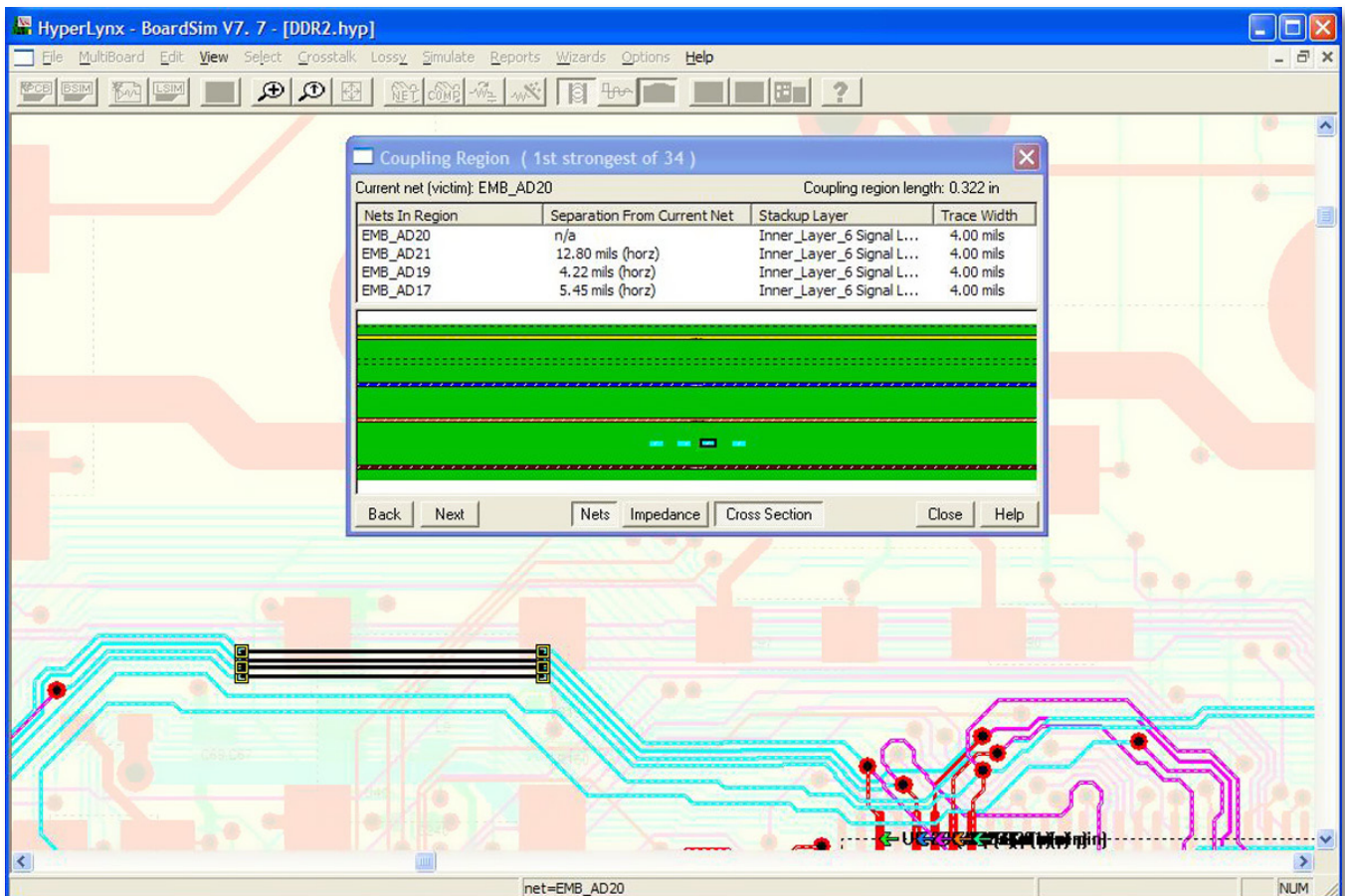


Figure3: Crosstalk on long parallel trace segments.

The inductance of the capacitor mounting has not been considered in this example. This inductance will increase the impedance and can be reduced by placing the power and ground planes closer to the capacitor mounting surface which reduces the loop area. The optimum mounting inductance of 0.5 nH is obtained when an 0402 capacitor is mounted using the via-on-side scheme with wide connecting traces to the vias. To further reduce the mounting inductance, two vias per capacitor land can be used in parallel.

As mentioned previously, the batch mode simulation produces a report of possible SI, crosstalk and EMC violations. Interactive simulation is then used to further analyze these potential issues.

Example:

Maximum allowed crosstalk: 150 mV pea
NET = EMB_AD20

AGGRESSOR NETS (Estimated peak crosstalk)

EMB_AD17: 175 mV

EMB_AD21: 65 mV

EMB_AD19: 102 mV

Sum of the two strongest aggressors: 277mV

Crosstalk is typically picked up on long parallel trace segments. These can be on the same layer, as in Figure 3, but may also be broadside coupled from the adjacent layer. It is for this reason that orthogonal routing is recommended on adjacent layers (between planes) to minimize the coupling area. This will not occur with the stackup illustrated in Figure 1, because there is only one signal layer between the planes — so this is very safe as far as broadside crosstalk is concerned, plus it allows a clear return path for signal current.

When interactive routing, one tends to group signals for aesthetic reasons — this is the artistic side of the PCB designer showing through. But, although it looks nice and neat, it may not perform so well. It is recommended that, in the above case, trace segments should be spaced by three times the trace thickness where possible or alternatively the trace-to-plane height can be reduced in the stackup.

Synchronous buses, as typically used in

DDR designs, benefit from an extraordinary immunity to crosstalk. Crosstalk only occurs when the signals are being switched and this crosstalk only has an effect within a small window around the moment of the clocking. So, providing the receiver waits sufficiently long enough for the crosstalk to settle before sampling the bus, the crosstalk has no effect on the signal quality at the receiver.

Apart from the issues of EMC, signal integrity and crosstalk problems can cause intermittent operation due to timing glitches and interference dramatically reducing your product's reliability.

Series terminators are typically used in high-speed design to slow the rise time, prevent ringing and hence EMI. These need to be manually checked for correct value or they can be determined by the simulator:

$$\text{transmission line impedance} - \text{driver impedance} = \text{series terminator (ohms)}$$

Flight times of the critical signals are then examined. One could compare the matched lengths of each signal, but delay will vary depending on the meander pattern. Also, the trace either side of a series terminator needs to be added to obtain the total length. Instead, it is best to compare the skew between, for example in Figure 4, the DDR2 MDQ0 (data) and MDQS0 (strobe) to ensure the flight times are correct. In

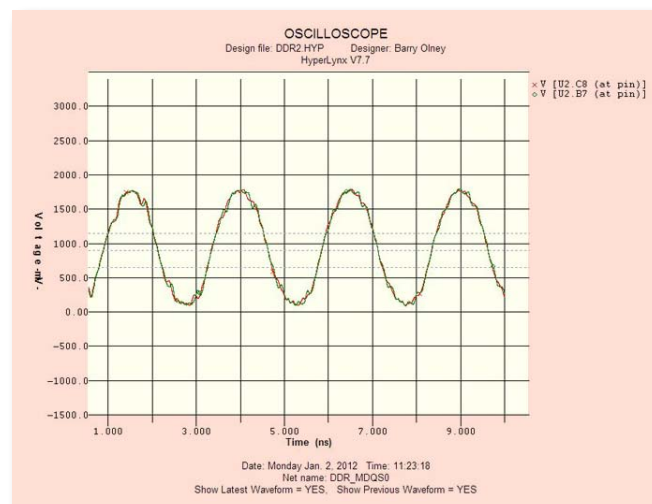


Figure 4: Flight times of DDR2 MDQ0 compared to MDQS0.

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this case there is 10pS difference, well within the specification.

Also, firmware can be used to adjust the drive strength in most FPGAs. I typically use the mid-strength drive current (8 - 12 mA) unless there are multiple loads in which case a high drive current may be required. High drive strength normally distorts the waveforms. If this occurs, back it off a little and check the waveforms again.

The signal groups to compare for DDR2 devices are:

Data: MDQ, MDQS & MDM
Address: MA, MBA, MRAS, MCAS, MWE
Control: MCS, MCLKE, MODT
Clock: MCLK, MCLK#

The DDR2 signals should be referenced to the VDD (1.8V) power plane or ground plane. The clock is used to capture the address and command data whilst the data is captured by the strobes rather than the clock. Therefore, the signals in the groups above should be compared to each other. For example: MDQ0 compared to MDQS0 and MDM.

The timing of the differential clocks should also be checked and the eye needs to be wide open. Figure 5 shows the DDR2 clock signal at the pins of each memory chip.

Since all products must comply with strict electromagnetic compliancy regulations, all

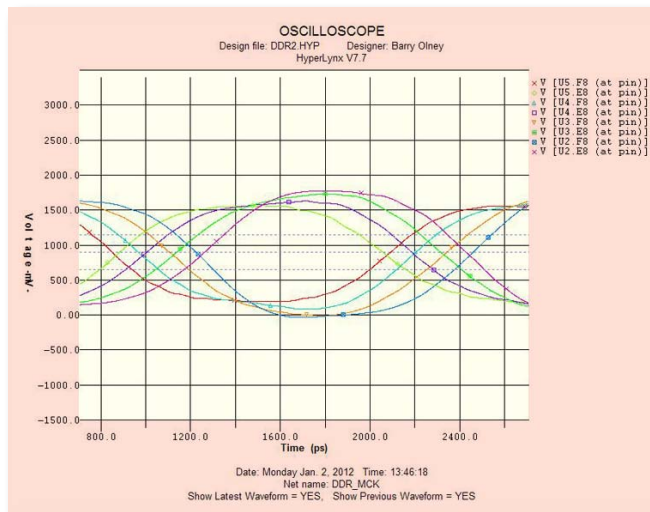


Figure 5: The differential clock at each of the DDR2 chips and the 100-ohm end terminator.

critical high-speed signals should be simulated to determine the amount of expected radiation. The EMC standards, for Class B, limit the radiation to 54 dB average with a peak of 74 dB (at a 3 m distance) above 1 GHz. However, harmonics can still cause unforeseeable problems. Generally these issues are caused by routing traces on the outer (microstrip) layers where radiation is much higher than that of the inner (stripline) layers. Routing these signals between the planes can reduce the EMI by more than 10 dB.

The FCC (US Standard is the blue horizontal lines
The CISPR (Euro standard) is the red horizontal lines
The Class B limit is the lowest pair of lines.

In this case, the radiation for a DDR2 clock of 400MHz is:

34.54 dB @ 380.95 MHz (fundamental)
29.9 dB @ 1.19 GHz (3rd harmonic)
37.29 dB @ 2 GHz (5th harmonic)
54.95 dB @ 5.19 GHz
51.23 dB @ 10 GHz

If the maximum clock frequency is 108 – 500 MHz, then emissions have to be measured between 30 MHz – 2 GHz. For a 500 MHz – 1 GHz clock, the measurement is between 30

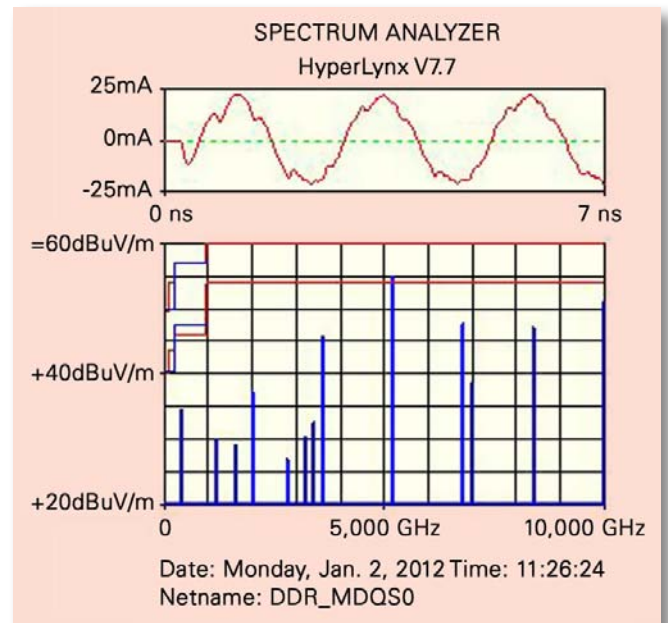


Figure 6: Electromagnetic radiation from MDQS0 strobe.

MHz – 5 GHz. The radiation in Figure 6, up to 2 GHz, is well below the Class B limit; however, we need to ensure that the anti-resonance peaks of the PDN are not at the frequencies of the odd harmonics. A large noise voltage spike can result on the power rail if there is a high transient current at these peaks.

On completion of the interactive simulation, an extensive post-layout simulation report is then compiled highlighting all the issues that need to be addressed by the engineer and/or designer. Once modified, the board is then re-simulated to ensure integrity.

We all know that simulation tools are expensive. Then there is the learning curve associated with complex software, not to mention the fact that the engineer needs to have years of experience analyzing high-speed designs.

By utilizing a PCB board-level simulation service, you can be assured that your PCB will be reliable and manufacturable, will conform to specifications and pass the relevant compliancy tests, which will save you time, money and frustration for a fraction of the cost of board iterations and multiple compliancy testing. Plus, the simulation can be done before the design is finalized (before Gerber output or even earlier in the design process, as recommended) to further reduce production time and costs.

Points to Remember:

1. Ensure that both single-ended and differential impedances conform to the technology requirements. Adjust the stackup if required.
2. The stackup should be symmetrical about the center.
3. Stitching vias should be used to connect ground planes or DCAPs between power and ground planes to provide return current paths.
4. DCAPs should be placed in parallel, as close as possible to each power pin using a thick, short trace.
5. The impedance of the PDN should be kept to a minimum (target impedance) up to the target frequency.
6. The inductance of the capacitor mounting can be reduced by taking the via fanout to the side of the land pattern.
7. Crosstalk is typically picked up on long parallel trace segments. Traces should be spaced

by three times the trace thickness where possible.

8. Series terminators should be used on critical signals and need to be checked for correct value.

9. Flight times of the critical signals should be within specification. This may be different for matched lengths. Check data to strobes and address/command to clocks.

10. Make sure that the anti-resonance peaks of the PDN are not at the odd harmonic frequencies of the clock.

11. Ideally, the board-level simulation should be done during the design process to ensure design integrity.

12. The post-layout board-level simulation can be used for disaster recovery: Plan B.

Stay tuned for Part 1 of the new series, Board-Level Simulation and the Design Process. Now that we have seen what happens when you don't follow a proven design process, I will walk you through the entire methodology to get it right the first time. **PCB**

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6. The Perfect Stackup — Barry Olney
7. Controlling the Beast — Barry Olney
8. High-Speed Signal Propagation — H.

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The ICD Stackup Planner and the new ICD PDN Planner can be downloaded from www.icd.com.au



Barry Olney is Managing Director of In-Circuit Design Pty Ltd. (ICD), Australia, a PCB Design Service Bureau and Board Level Simulation Specialist. Among others through the years, ICD was awarded "Top 2005 Asian Distributor Marketing" and "Top 2005 Worldwide Distributor Marketing" by Mentor Graphics, Board System Division. For more information, contact Barry Olney at +61 4123 14441 or email at b.olney@icd.com.au.

Overview: Technological Developments and the Materials Supply Chain in the PCB Industry

by Mike Devine

eXception GROUP

SUMMARY — *The subject of technology and materials supply is clearly vast and compounded by ever-increasing challenges. Since the dawn of the electronics age, the quest for capability, combined with commercial competitiveness and ease of manufacturability, has sustained many careers.*

Today, the boundaries between exotics (i.e., polyamide, PTFE, ceramic, and thin/thick film polymer materials) and standard FR-4 derivatives are narrow, but critical to today's existing technologies — satisfying the majority of needs for product design where once the requirement was deemed to be leading edge for signal integrity/speed/loss and thermal applications.

Understanding the markets, the clients, and technology roadmaps of the future of electronics interest is essential to success. Take, for example, the automotive market. For many years automotive PCB manufacturing has been led by fabricators in Germany and Asia supporting traditional, single-sided and double-sided PCBs in high volumes, with strict legislation. The legislation remains due to safety-critical applications, but the technology has evolved to embrace alternative manufacturing techniques and materials.

Any hardware designer involved in an application deemed hazardous or safety-critical has little choice but to specify materials with absolute known performance characteristics that have been proven through actual field use throughout years of life.

Frequently, software and hardware engineers and their PCB fabrication partners are asked about their manufacturing methodologies and material choices. One continuing trend is the increased use of high-speed signals in various applications, including encrypted communications and networks. Driven by silicon development from all the leading manufacturers (e.g., Intel, Texas Instruments, STMicroelectronics



and Xilinx), the adoption of high-speed/low-loss materials utilized in designs is widespread across all applications. Silicon development itself has led to increased pin count FPBGA (fine-

pitch ball grid arrays) in order to facilitate the increased interconnect required to support the additional functionality. Three years ago, the standard pitch for BGAs was 1mm-0.5mm, with the emergence of 0.4mm and 0.3mm beginning to show. Today's challenge as seen by many PCB fabricators is the ability to support their loyal customer base with technical advice and support and to manufacture boards at a yield that is acceptable and within cost constraints to the program and business.

Medical Case Study

eXception PCB Solutions and their Internal Design Services (IDS) department has worked closely recently with a medical OEM to provide a PCB with HDI technology (sub 50um track and gaps) which has replaced the need for the application of a silicon component by using 0.25mm BGA construction.

This type of technology can only be produced using HDI technology, by PCB manufacturers that can combine local technical support with investment in the latest manufacturing equipment capable of handling thin laminates, processing fine geometries, superior registration and multiple lamination cycles. Additionally, this type of service is common throughout Europe and North America, and in Southeast Asia, though only through specialist vendors. Interesting to note, however, is that OEMs who are using Asia are seeing and feeling additional pain. The increased threats of force majeure are having a major impact on the supply chain, with regard to raw materials and/or the supply of key components to complete the assembly cycle. Examples seen in 2011 include the supply of Nelco laminates from Japan and hard disc drives from Thailand, plus the increased costs associated with local inflation throughout China. This has resulted in more

complex PCB designs being sourced from the Western world at higher cost.

Supporting this trend are the raw material vendors who are evaluating and consistently launching new base laminates and dielectrics that will be part of the future. Advanced applications are being sourced by vendors such as Rogers Advanced Circuits, which has introduced a range of high-performance thermoplastic laminates (XT/RT Duroid) that are regarded as highly reliable, halogen-free, flame-retardant and thermally and chemically robust, with melting points higher than PTFE materials. This makes them well suited to rugged applications including airborne lightning strike protection, phased array antennas and unmanned aerial vehicles (UAVs).

PCBs require higher technology and more stable substrates to perform alongside the exotic laminates (Arlon, Rogers, DuPont, Bergquist, etc.) currently in the marketplace. With the current advance of semiconductor and PCB technologies, laminate suppliers are responding to customer needs by developing the optimum materials for the next generation. These include thermosetting resin design and compound material design technology.

The operating temperature of PCBs today can easily exceed 125°C. Placement of PCBs within the end application will push temperatures even higher, and power dissipation from the device may result in operating temperatures higher than 150°C. Use of external cooling fans can restrict placement, so internal heat planes (CIC, Cu cores) and through-hole copper filling can dissipate heat away from components. PCBs have evolved to survive harsh operating environments and materials currently available are capable of withstanding extremes in temperature, humidity and vibration.

“
Any hardware designer involved in an application deemed hazardous or safety-critical has little choice but to specify materials with absolute known performance characteristics that have been proven through actual field use throughout years of life.
”

How can the industry move forward cost-effectively? High-performance PCB base materials can enable maximum operating temperatures around 200°C, with low Z-axis expansion and resistance to delamination and chemical attack.

The first requirement for engineering low coefficient of thermal expansion (CTE) PCBs is to understand the physics behind the properties of CTE. One must know what creates problems and how to engineer methods to minimize the CTE effect on printed circuits.

CTE simply means that every material expands or contracts as its temperature changes. The expansion is expressed in ppm/°C or parts per million per °C. For example, FR-4 typically has a CTE of 45 ppm/°C or 0.000045 inches expansion per °C. Most printed circuits will have materials with different CTEs sandwiched together with components of different CTEs soldered on board. When temperature excursions occur, due to changes in either ambient conditions or the power dissipated by the circuit, these materials will expand differently, leading to the creation of stresses. The CTE of copper is 16 ppm/°C or 0.000016, which is about 3x less than the expansion of a typical laminate.

In severe cases, warping of an entire board or a solder joint fracture of the components may be evident.

CTE is very important in circuits that mount large BGA chip packages due to the shearing of the solder balls. The stresses created as the circuit board expands at a different rate than the ceramic BGA package can literally tear off a chip package. Laminate construction (weave) has a profound impact on the Er/loss tangent value of the dielectric in the local vicinity of placing signal traces. The nature of the construction presents an irregular material profile to the signal traces that become more apparent in the thinner dielectrics. Ultimately this highlights the limitations of epoxy/fiberglass laminates. The traditional FR-4 materials are rapidly gaining ground on the higher cost/performance laminates. Thermally and electrically-enhanced FR-408HR (Isola), and VT461 (Global Ventec) can provide a migration path to support higher layer count and heavy copper designs.

How can fabricators support designers' requirements?

The advancement in FR-4 substrate has reduced the gap between the need for higher cost, improved performance and exotic laminates. With the increasing need for higher signal integrity speeds for today's Wi-Fi, GPS and communications applications, stable and robust material performance is essential. However, this is aligned to the physical constraints of the mechanics as well. Higher layer counts are an option, but increasingly, this means much thinner laminate dielectrics ($\Rightarrow$ 75 μ m) and use of single ply 106 (circa 55 μ m) or 104 (circa 45 μ m); this can impact on the fabricator's capabilities to manufacture repeatedly and keep yields high and costs lower.

Alternative technology

One option is to migrate toward embedded technology by moving surface mounted electronics into the substrate. Improved EMC shielding can be achieved, together with higher miniaturization and improvement reliability, through advanced thermal management. Embedded component technology has evolved since the early 1990s. In the early years, special



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cavities in the prepreg were used as a separator between the layers of a multilayer PCB, which enabled the fabricator to use standard PCB manufacturing technologies and equipment without damaging sensitive components during multilayer lamination and pressing.

Today, with the evolution of laser ablation technology, this can be performed by using polymer resistor/capacitor paste and laser trimming to achieve the desired resistance.

The advancements in standard materials, combined with a myriad of proven, well-documented and safe field applications across numerous and diverse product projects, provide a compelling attraction for the most risk-averse engineers.

The development and continuous improvement in performance and specification from the exotic supplier camp continues unabated; however, with truly outstanding material solutions available from a global supply base, it can be reported that the boundaries remain, albeit

not at the same median points as in previous times.

As ever, the Darwinian principle of evolution by natural selection is perhaps the dominant force in play, with the obsolescence of defunct elements and compound growth where interest and take-up is high.

The future of our industry will be exciting. **PCB**



Mike Devine joined eXception Group in 2005. After a successful early career in all aspects of manufacturing, Devine moved into process engineering management and then became a CAM engineering manager. Eventually, he joined the external technical sales team and was instrumental in setting up a new department that led to formalising Internal Design Services (IDS), of which he is now Technical Director.

Intercept Technology, Inc. to Release New User Interface Pantheon 7 at IPC APEX EXPO

Intercept Technology, Inc., will be unveiling its PCB/Hybrid/RF layout design software, Pantheon 7, at IPC APEX EXPO later this month. Pantheon 7, with an advanced PCB, Hybrid and RF design application user interface has been redesigned from the ground up, offering greater ease of use and improved productivity for all designers.

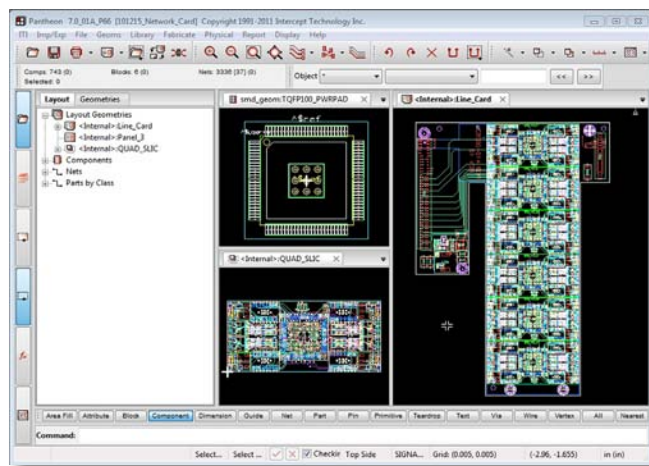
This software release takes the last 15 years of Pantheon's development as an advanced PCB/Hybrid/RF design application and overlays a modern user flow that greatly increases productivity and provides a scalable solution for designs of all sizes and complexities. Most importantly, the redesign makes no changes to the database; all existing customers will be able to upgrade or run mixed-version environments without any incompatibility issues.

Pantheon 7's Intercept-standard user interface features include:

- Multi-window support for real-time edit and update of geometries on the board

- Project Explorer with quick access to board, block, component, net, and part references
- Quick Search Toolbar for quick entry and select of design objects
- Undocked Toolbars for maximized edit window space, greater ease of use
- Window Control Toolbar to open/close windows and maximize edit window space
- Redesigned menu structure for faster and more intuitive user flow

For more information visit www.intercept.com.



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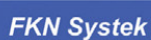
This three-day event will be packed with informative workshops, exhibits and a comprehensive technical conference that will provide all attendees with a competitive edge in eastern Europe's fast-growing electronics interconnect market.

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Rigid-flex Manufacturing Part II: Materials

by Dale Smith

DAS FLEX CIRCUIT CONSULTANTS, LLC

Summary — The combination of rigid and flex materials cause stress in interconnects, which in turn can cause reliability issues when the product is exposed to thermal excursions during solder, component assembly or end-use environmental conditions. It is extremely important to use proper materials for rigid-flex fabrication.

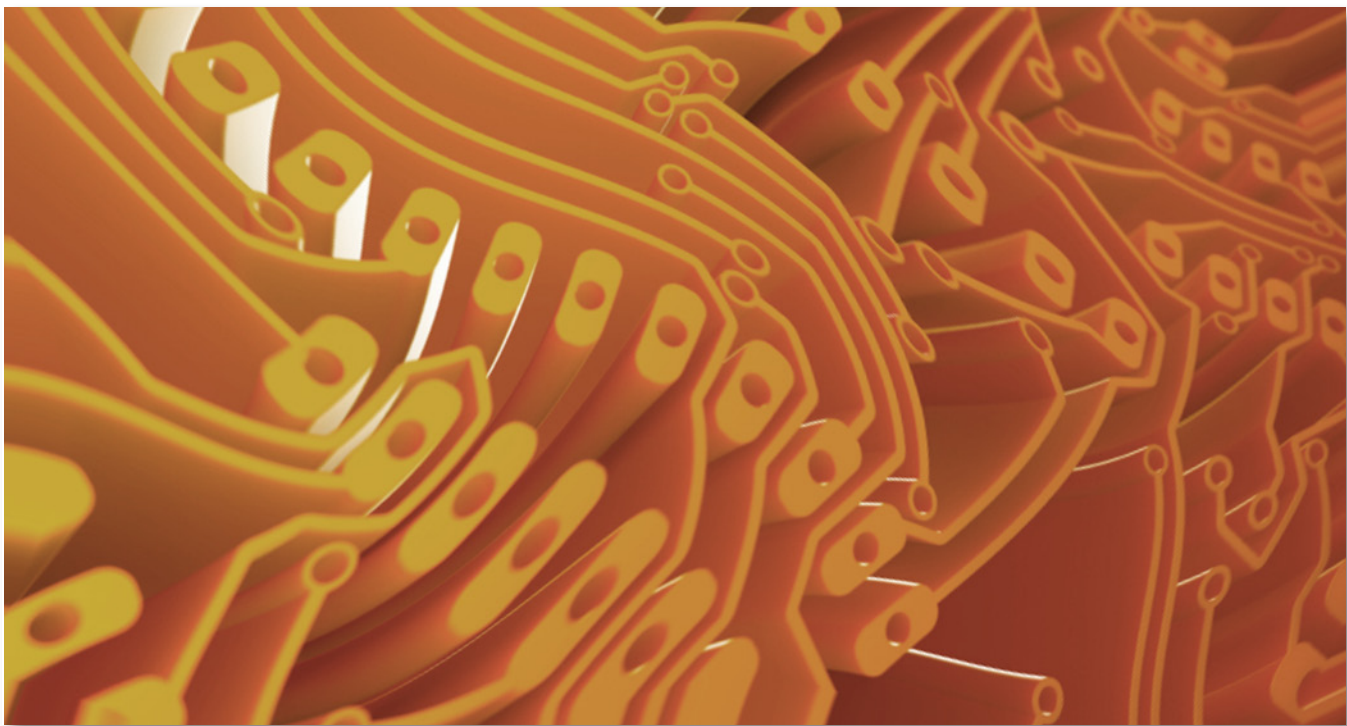
Materials: Overview

It is extremely important that proper materials are utilized for rigid-flex fabrication. The combination of rigid and flex materials cause stress in the plated through-hole interconnects. These stresses can cause reliability issues especially when the product is exposed to thermal excursions during solder, component assembly or end-use environmental conditions. Typically, high-performance materials are selected to avoid having process issues during manufacturing and yield long-term reliability in stressful environments.

High Performance Materials

What determines a high-performance material? Typically, it will be the material's thermal, electrical and physical properties that will determine how well it will perform. The following are material properties to consider when selecting materials for rigid-flex processing and its end-use service:

- Tg = glass transition temperature
- Td = thermal decomposition temperature
- CTE (X, Y, Z) = coefficient of thermal expansion; emphasis on Z axis
- Bond strength (at ambient and elevated temperatures)
- Solder resistance (solder float)
- Dimensional stability
- Flexible endurance
- Electrical (dielectric strength/breakdown and constant)
- Chemical and moisture resistance



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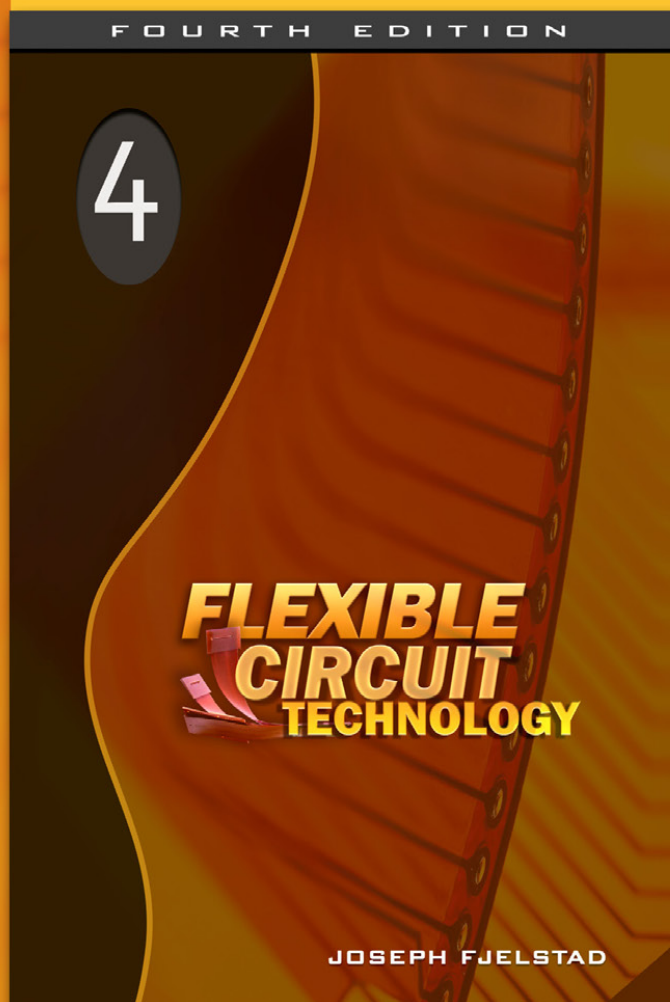


Table of Contents

Acknowledgements.....	8
Foreword.....	12
Chapter 1 Flexible Circuit Technology Overview	14
Chapter 2 Flex Circuit Technology—Past, Present & Future	26
Chapter 3 Flex Circuit Drivers, Benefits & Applications	48
Chapter 4 Process Challenges and System Applications in Flex ...	94
Chapter 5 Flexible Circuit Materials	126
Chapter 6 Implementing Flexible Circuit Technology	168
Chapter 7 Practical Design Guidelines for Flex	184
Chapter 8 Guide to Reliable Static and Dynamic Flexing	262
Chapter 9 Flex Circuit Manufacturing Process	280
Chapter 10 Flexible Circuit Assembly	354
Chapter 11 Printed Electronics	380
Chapter 12 Solderless Assembly Processes for Flexible Circuits ...	448
Chapter 13 Stretchable Circuits	478
Chapter 14 Inspection and Test of Flex Circuits	514
Chapter 15 Plated Through-Hole Reliability	542
Chapter 16 Documentation Needs for Flexible Circuits	572
Chapter 17 Flexible Circuit Standards and Environmental/ Regulatory Requirements	586
References.....	608

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In rigid-flex construction, we need to select many materials:

- Flexible metal clad laminates for the flexible layers
- Adhesive-coated dielectric film (covercoat for the flexible metal layers)
- Rigid metal clad laminates for the rigid layers
- No-flow prepreg (glue to bond all layers together)

Flexible Metal-Clad Laminates

The preferred choice is an adhesive-less laminate (i.e., DuPont Pyralux AP product) per IPC-4204/11. This is an all-polyimide material that has a proven track record (almost 20 years) for performing extremely well in rigid-flex applications; not only in processing but also for long-term reliability in harsh environments. This is due to its desirable thermal, electrical and physical properties:

- High Tg = >220oC
- High Td = >500oC
- Easily passes 10 second solder float at 288oC (will pass 60 seconds)
- Low CTE = 40 ppm/oC
- High bond strength = copper to polyimide >10 lbs./in. (maintains value after solder)
- Good dimensional stability = .04 to .08% per IPC TM 650 Method 2.2.4
- Good flexing endurance capability
 - Passes MIL-P-50884 qualification of 100,000 cycles
- Excellent electrical properties
 - Dielectric strength of >6000 volts/mil
 - Dielectric constant = 3.4
- Good chemical resistance
 - Most PCB chemicals have negligible effect on the material
- Low moisture absorption
 - Less than 1.0% per IPC TM-650 Method 2.6.2

Copper Foil Type

The preferred copper foil for flex circuits is a wrought rolled annealed (typically referred to in IPC-4562 as type W7). This copper has excellent ductility and elongation properties and offers:

- High resistance to cracking during flexing
- High resistance to foil fractures in PTHs during thermal exposure.

Note: Some of the ultra-thin copper foils (i.e., 9-micron copper) are only available in electrodeposited form.

Covercoat

A preferred choice with a proven history would be DuPont Pyralux LF. Acrylic adhesive is coated onto a polyimide dielectric film (DuPont Kapton) in a B-stage form. For rigid-flex manufacturing and long-term service life, the material has the following desirable properties:

- High bond strength to treated copper surfaces
 - 9-10 lbs./in. (maintains value after solder)
- Good electrical properties
 - Dielectric strength >3000 volts/mil
 - Dielectric constant = 3.5
- Good thermal properties
 - Passes 10-second solder float at 288oC
- Good flex endurance capability
 - Passes MIL-P-50884 qualification of 100,000 cycles
- Good chemical resistance
 - Most PCB chemicals have negligible effect on material

Note: Unfortunately, there is no all-polyimide covercoat material available today. The covercoat adhesives have poor thermal properties (low Tg and high Z axis CTE). Their presence in the plated through-hole can cause barrel fractures in the electrodeposited copper plating. Therefore the covercoat material should only cover the flexible areas. We will discuss this in more detail in a later column.

Rigid Metal Clad Laminates

Generally, two resin systems (epoxy and polyimide) are used for rigid copper clad laminates. These materials are generally referred to as:

- For epoxy resin systems (most common): IPC-4101/21, /24, /26, /28
- For polyimide resin systems: IPC-4101/40, /41, /42 (/41 preferred)

There are many manufacturers of rigid materials. Some rigid materials I've had success with for long-term thermal reliability are:

- Isola FR406® for epoxy resin system
- Isola P95 for polyimide resin system

Polyimide costs more, but is recommended over epoxy due to higher Tg and Td. The Z-axis CTE is about the same for both materials below the Tg. However, above Tg, the Z-axis expansion increases dramatically. Therefore, using polyimide, we may not experience excessive Z-axis expansion because we will not reach its Tg during thermal exposure.

Some key material properties are:

	Epoxy	Polyimide
1. Tg	170oC	260oC
2. Td	300oC	400oC
3. Solder Float		
288oC 10 sec.	Pass	Pass
4. CTE (Z)*	60 ppm/oC	55 ppm/oC
5. Bond Strength	7-9 lbs/in.	6-7 lbs/in.
6. Electrical	>1000 volts/mil	>1000 volts/mil
7. Dielectric		
Constant	4.0	4.0

Note: Property values are for comparison only and may vary depending upon material manufacturer and material construction.

*CTE will dramatically increase above material's Tg rating.

Some Notes:

1. Core thicknesses range from .0025" to .031". Thinner cores are generally used due to overall thickness constraints and will have higher CTE.

2. Minimum of two (2) glass ply is recommended to avoid electrical issues.

3. Thinner cores will use finer glass (higher resin to glass ratio). Conversely, thicker cores will use coarser glass (higher glass to resin ratio) and may have more glass plies.

4. Thicker cores will have better dimensional stability.

5. Material is available in double- or single-copper clad. For single-clad, it is preferred to purchase double-clad and etch copper off one side. Result will be a rougher surface topography yielding higher prepreg bond strength.

Copper Foil Type

Preferred is an electrodeposited HTE (high-temperature elongation) copper foil referred to in IPC-4562 as type 3. This type is highly resistant to foil fractures in PTHs during thermal exposure.

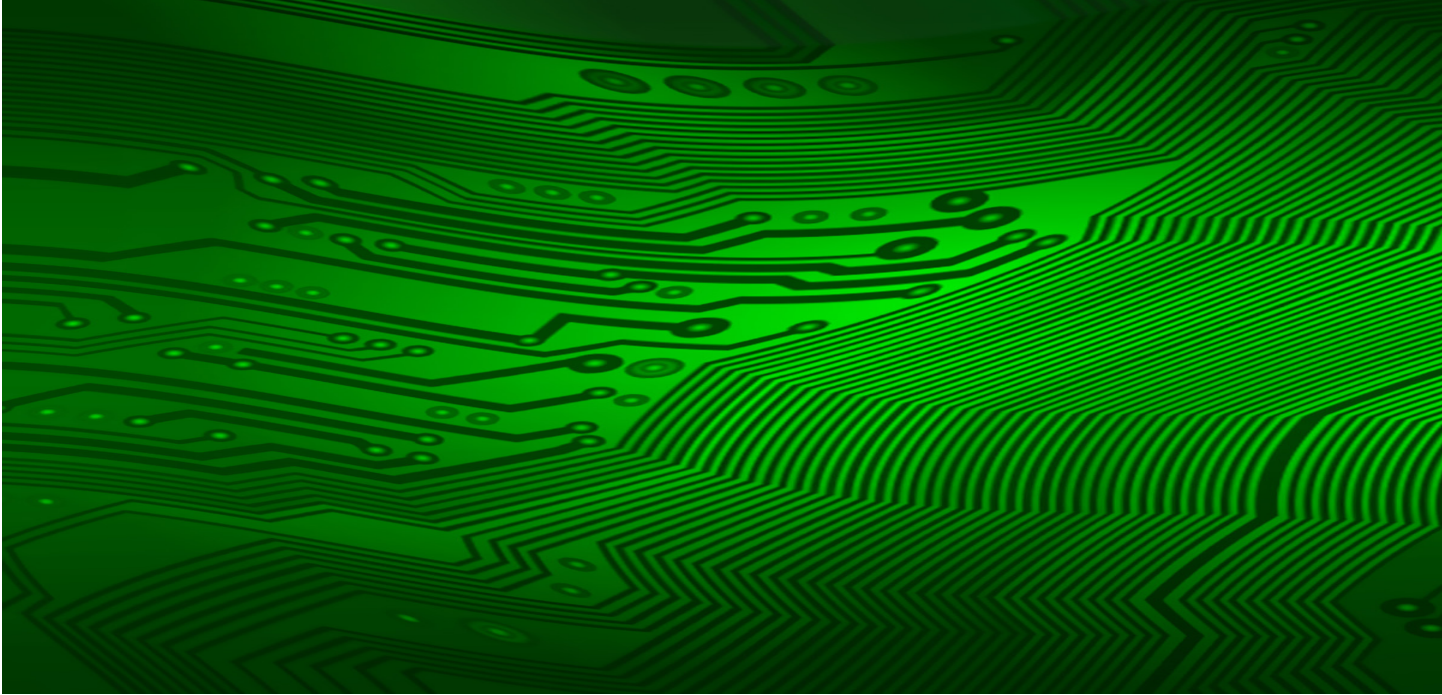
No Flow Prepreg

This material is utilized to laminate all the flexible layers and rigid layers together to form a rigid-flex panel. It is the same B-stage material as conventional prepreg, except the resin chemistry has been altered to dramatically reduce flow. This is critical to minimize resin flow-out into the flexible areas. Material will become C-stage rigid material when fully cured and will add rigidity to the rigid section. Similar to rigid metal clad laminate material, we desire high-performance thermal, electrical and physical properties.

In my next column (Rigid-Flex Manufacturing, Part 3), I will discuss Z-axis expansion and how it affects rigid-flex through-hole interconnect reliability. **PCB**



Dale A. Smith is President of DAS Flex Circuit Consultant and has more 30 years experience in the printed circuit industry. He specializes in rigid/flex high reliability manufacturing and Lean Manufacturing implementation into PCB shops. Reach Smith at 267-424-0690 or by e-mail at dale.smith68@verizon.net.



Flexible Circuit Solutions Continue to Evolve and Expand Their Range of Capability

by **Joseph Fjelstad**
VERDANT ELECTRONICS

SUMMARY — *Though now arguably more than 100 years old, flexible circuit technology continues to evolve and find new habitats where it can grow and thrive. In fact, flexible circuit technology is a technology that can not only adapt, but also has some real staying power.*

Flexible circuits are arguably the oldest of structured interconnection, based on the findings of gifted researcher, innovator and self-described technology generalist Dr. Ken Gilleo. The roots of flexible circuits, at least as determined by patent literature Gilleo uncovered, date back more than 100 years to a 1903 British patent issued to Albert Hansen of Germany, entitled "Improvements in, or Connected with, Electric Cables and the Joining of Same." Hansen was an amazingly prescient inventor who not only appears to have anticipated the flexible interconnections the industry relies so heavily on, but also in a later disclosure something that looks very much like a multilayer circuit of sorts.

In the beginning, the flexibility of the circuit enabled the user to utilize all three dimensions of space to accomplish their design for interconnection needs and this is still all that

is required for the vast majority of electronic products, which take advantage of flexible circuit technology. The early stages of the technology also served to inspire an early innovator named Arthur Berry to create a resistive heater on a flexible base film in 1913, a product idea that continues to be used in many applications that, unfortunately, are often unseen and unappreciated by the user.

As time progressed, the potential to use a flexible circuit in a dynamic fashion caught the attention of electrical product engineers and the application opportunity horizon for flexible circuits grew at an increased rate, spurred on by printers, disc drives and hinged/foldable electronic products.

Because the base film was flexible, it was observed that circuits could be processed in roll-to-roll (or reel-to-reel in the case of narrower, sprocketed films) fashion much like products of the print media. While panel processing of flexible materials to create circuits remains of prime importance for reasons related to production versatility, roll-to-roll processing technologies helped keep costs down for volume production of high-run products. The reel-to-reel process variant of unwind/process/rewind flexible circuit processing in a continuous fashion became (and still is) an important processing method for the manufacture of TAB (tape automated bond-



ing) products. Though invented in the 1960s, TAB became of high interest in the late 1970s for making fine-pitch, low-profile packages for integrated circuits including microprocessors. Today, display driver circuits appear to be the most widely targeted application for the technology. Given all of the display of every imaginable size, it comes with little surprise that TAB will likely be around for some time to come and may get future opportunities as newer generations of engineers come to understand and appreciate its capabilities.

The marriage of flexible and rigid circuits was another important evolutionary step for flexible circuits and rigid-flex circuits are now widely used in a range of product applications, having stepped beyond their military/aerospace origins in the 1960s. These products are often highly engineered and those involved in their design and manufacture are normally among the most seasoned of flex circuit professionals.

Today, flexible circuit technology continues its evolutionary path into areas that are opening doors to new types of products. One of the evolutionary new forms of flex is the stretchable circuit, a circuit that is not only flexible, but which can also be resiliently stretched. Products based on the technology are redefining mobile vital sign monitoring both for medicine and in sports as the circuit and sensors which are in contact with the skin, expand and contract with the users muscles.

A final evolutionary type of flex circuit for this discussion is one wherein active circuit elements are embedded into the flex circuit mate-

rial itself. Much of this activity has been spearheaded in Europe at Fraunhofer Institute. The die are thinned down to as low as 25 microns, at which point the normally brittle circuit can actually be bent. Variations on the theme of embedding that can be manufactured using more standard and widely accessible technologies are discussed in the newly released [4th edition Flexible Circuit Technology](#) in the chapter of solderless assembly of flexible circuits.

In summary, though now arguably more than 100 years old, flexible circuit technology continues to evolve and find new habitats where it can grow and thrive. The older versions of the technology have not suffered extinction, but continue to serve the electronics industry and its product designers. Obviously, flexible circuit technology is a technology that can not only adapt, but also has some real staying power. **PCB**



Verdant Electronics Founder and President Joseph (Joe) Fjelstad is a four-decade veteran of the electronics industry and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 250 U.S. and international patents issued or pending. He is the author of *Flexible Circuit Technology* and author, co-author or editor of several other books and more than 300 technical papers, articles and columns.

Most-Read Supplier/New Product Highlights This Month



Top 10 New Products of 2011

It took some time, but we did it. After scanning the sizable catalogue of products launched this year, here are our choices for the PCB007 Top 10 New Products of 2011.

The Pulse: Roller Coaster Year

Throughout 2011, "The Pulse" explored a range of PCB topics from a signal integrity standpoint. Columnist Martyn Gaudion takes a look back to see how these issues have played out over the course of this crazy year.

Atotech Expands Facility in Podnart, Slovenia

The new production facility of Atotech Slovenia covers a total area of approximately 3,200 square meters, and hosts 29 mixing vessels for an annual production capacity of 15,000 tons, which can be further expanded to 20,000 tons/year.

AccuKraft Employs D.B. Management Group L.L.C.

Becky Hanson, president of AccuKraft, announced this week that her company has engaged the services of D.B. Management Group, L.L.C. to help with their national expansion.

Rogers Lowers Q4 Guidance

Bruce D. Hoechner, president and CEO commented, "As we had anticipated in October, demand across many of our markets continued to weaken through the fourth quarter, adversely affecting the sales and earnings of many of our business segments."

Orbotech Earns Viasystems' Supplier Appreciation Award

Orbotech was selected for the prestigious award in recognition of its exceptional service at Viasystems' PCB production plants in Asia Pacific and its top performance in providing the solutions required to support the company's continued success.

Court Dismisses Administrative Suit Against Isola Patent

Isola has announced that the Taiwanese Intellectual Property Court confirmed the validity of Isola's Taiwan patent no. 413659 (Fillers for Improved Epoxy Laminates) by dismissing an administrative suit filed by Taiwan Union Technology that challenged Isola's patent.

Lloyd Doyle to Celebrate 30 Years

Founded in 1982 by Roy Lloyd and Dr. Keith Doyle to develop industrial automation products, the company has earned a global reputation for its unique connectivity-referenced, automated optical fault detection systems for PCBs.

Zuken Releases New Version of Board Modeler Lite

Zuken has released a new version of Board Modeler Lite that offers significant productivity enhancements during board layout design. Board Modeler Lite 6.1, available now with CADSTAR 13.0, bridges the process between MCAD and ECAD design flows by offering a common communication platform.

GCT Unveils New Diamond-Coated Tools

GCT GmbH introduces two new diamond-coated tools: end-mill-type 1328 with two flutes and centre cutting, and chamfering cutter-type 138x with single flute.

Productronica's Unsung Hero

by Real Time with...productronica 2011



Videographer Kirk Wallace, the unsung hero of the Real-Time with... team, offers his tips for transporting expensive camera equipment by air. Not to be missed if you are traveling to IPC APEX EXPO!



realtimewith.com

Taiyo America to Unveil Liquid Photoimagable Solder Mask at IPC APEX EXPO

Taiyo America will introduce the PSR-4000 PRSM, a totally new Liquid Photoimagable Solder Mask. Incorporated are all the outstanding properties of PSR-4000 BN, PSR-4000 GP01EU and PSR-4000 HFX — in one new product. Taiyo's most environmentally friendly product to date has already been tested in North America and Europe and has a commercial release date of March 2012.

PSR-4000 PRSM Highlights:

- Environmentally friendly
- Screen print or spray application
- Available in black, blue, clear, green, orange, purple, red, white and yellow
- Excellent small hole clearing
- Wide processing window
- Fine dam resolution
- Two-year shelf life
- Halogen free
- RoHS compliant
- Meets Aerospace Outgassing Requirements
- Compatible with Lead-Free Processing
- Withstands ENIG & Immersion Tin



PSR-4000 PRSM Cross Section – 50 micron dam

TOP TEN

PCB007
News

Most-Read News Highlights from PCB007 this Month

① **Express Circuits Unveils Secrets to Five-Year Stretch**

In a conversation with Pete Starkey, Vin Makwana, technical manager at Express Circuits, discusses the technology that the company has recently been pursuing: stretchable circuits. Express has been working with military and medical customers to develop stretchable circuits, materials, and processes.

② **Epec Marks 60th Anniversary; Proud to be America's Oldest**

As the oldest production PCB company in North America, perhaps in the world, the 60-year story of Epec is strongly connected to the development of the PCB industry.

③ **DDi Corp. to Relocate Headquarters and Anaheim Facility**

DDi Corporation has entered into an agreement to purchase a \$7.5 million building in Anaheim, California that will become its corporate headquarters and Anaheim manufacturing operations.

④ **Enigma Divests PCB Fabrication Business**

Dorigo Systems Ltd. founder Mark Pillon, P. Eng., has acquired the business assets and operations of Enigma's Burnaby PCB fabrication facility. Administrative operations have already resumed under a new company name, Enigma Interconnect (2012) Corporation.

⑤ IPC Adjusts Roadmap Direction; Expands Coverage

IPC is adjusting its roadmap to make it more useful, covering more types of technology and adding emulators. This expansion meets the needs of manufacturers, and focuses on the specific requirements of their customers and their product platforms.

⑥ Webinar Highlights Electronics Industry Prospects for 2012

"2012 will not be a year where you can sit on your tail and grow," said Walt Custer, president of Custer Consulting. "Growth will have to come from your competitors." Custer was one of three analysts focused on the electronic interconnect supply chain in a recent IPC webinar entitled, "Business Outlook for 2012."

⑦ Aspocomp Oulu, Cibo-Print Sign Purchase Agreement

Aspocomp Oulu Oy and Cibo-Print Oy have signed a business purchase agreement in relation to the business operations of a factory in Teuva. The agreement includes the PCB trading operations of Cibo-Print Oy.

⑧ 2011 HKPCA & IPC Show Reaches New Heights of Success

This year's show, jointly organized by HKPCA, IPC and the China Council for the Promotion of International Trade Guangzhou Sub-council, marked the event's 10th anniversary as the flagship trade show in Southern China for the PCB and EA industry.

⑨ Top 10 Most-Read PCB007 Articles of 2011

The top articles from 2011 include a little bit of everything, from processes to printed electronics. So, without further ado, here are the Top 10 Most-Read PCB007 articles of last year.

⑩ German PCB Market Normalizing

According to ZVEI, cumulative revenue for the year represents one of the highest values for the past 10 years, reflecting normalization in the industry.



PCB007.COM

It's Show Time!

by Barry Matties

I-CONNECT007

SUMMARY — *This year's IPC APEX EXPO in San Diego is nearly here...have you made the necessary arrangements? Another word of advice: The key to a successful show is you. Are you ready?*

Here we are just days away from another IPC APEX EXPO. This year's event, as you probably know by now, takes place in San Diego, California. It's interesting that as an industry, we go to these events each year, doing the same things, basically. Aside from a few new, cool innovations from year to year, not much else seems to be too fresh. As an industry reaches a level of maturity, things tend to become routine. The same speakers speak, the same exhibitors exhibit and for the most part, the same people attend. Some exhibitors say they participate out of fear — fear that someone will notice that they aren't there and assume the worst.

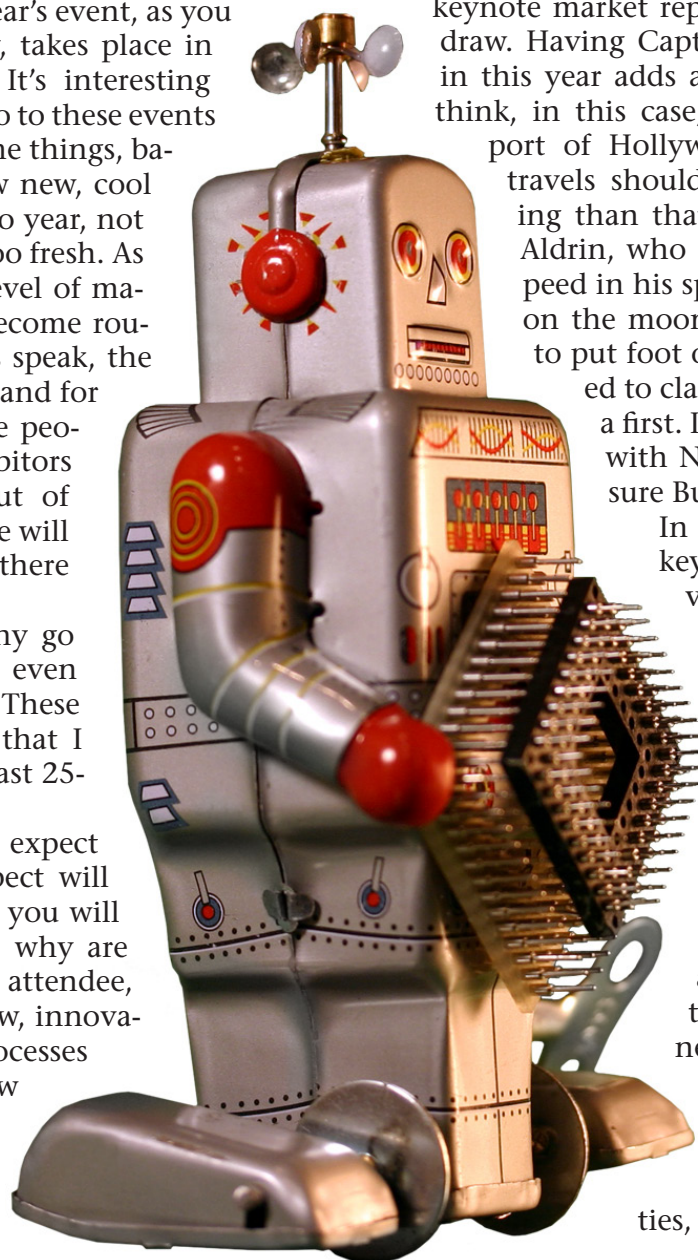
So why exhibit? Why go year after year? Why even have an annual show? These are all valid questions that I have heard during the last 25-plus years.

As an exhibitor, you expect that a new, solid prospect will land in your booth and you will close a sale. Otherwise, why are you exhibiting? As an attendee, you're hoping to see new, innovative equipment or processes unveiled on the show floor that will help you improve your business. As a show organizer, you hope for

strong traffic and that all of the above actually happens. To hedge the traffic bet, you plan a strong conference program, with professional development classes, poster sessions, and a few great keynotes to kick things off.

Certainly Walt Custer's and Sharon Starr's keynote market reports are always a good draw. Having Captain Kirk beam himself in this year adds a level of excitement. I think, in this case, William Shatner's report of Hollywood's imagined space travels should be far more interesting than that of past keynote Buzz Aldrin, who shared with us that he peed in his spacesuit while standing on the moon. Since he was second to put foot on the moon, he decided to claim that achievement as a first. I guess we have to check with Neil Armstrong to make sure Buzz truly was the first.

In any case, a special keynote guest is only a very small part of what keeps the show fresh. The evening reception is also a nice way to bring people to the show floor, but I don't think free popcorn and a special guest speaker lead people to spend their valuable time at a trade show. They attend to learn something new, check out the latest equipment, meet the teams behind the products, find new business opportunities, stay in touch with the



**“ I don’t recommend just showing up and expecting miracles.
It’s still business and you have to treat it as such. ”**

pulse of the industry and reconnect with old friends.

As an exhibitor, you should help keep the show fresh and relevant. You do this by bringing your latest equipment offering and your people — your “A” game, if you will. One thing you must do is to make sure you share with the industry, in advance, why they should come see you. I don’t recommend just showing up and expecting miracles. It’s still business and you have to treat it as such. Put real thought into the message that you present — before, during and after the show. If you are investing in being there, don’t fall short on your investment. Make sure you present yourself in a way that allows prospects to both notice and remember you. By the way, it’s not a promotional back scratcher or a ballpoint pen for which you will be remembered. You will be remembered for standing out and for offering innovative technology and real solutions that will help the industry — your customers — become more competitive.

As for the show organizers, they should be making sure that they do everything possible to present an extremely productive business environment; an industry is at stake, after all. When you compare a U.S. trade show to a Chinese show, there is a difference of night and day. It is clear that China’s shows are strong, whereas the U.S. seems to be in a holding pattern at best.

How does a trade show help the industry? It can’t. Only you can. The trade show is only the place where the industry’s players come together to support each other. Therefore, make the best of it by helping your customers become more competitive. Focus on bringing solutions to the show that will help them reduce cost through improved efficiencies, increased first-pass yields, removal of pain points in the manufacturing process, and any other way you can contribute to their success.

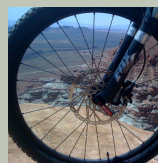
If I organized the event, it would be a show focused on solutions designed to help the attendees become more competitive in their business. The value of the show should be so strong that all companies would require their people attend, and not just for the structured technical programs, but also to hear and learn from the exhibitors. Again, the creation of a great show is not just up to the organizers; it takes all in-



involved. The exhibitors play such an important role. If you are an exhibitor you should take this role seriously. As an attendee, be sure to look at the exhibitors’ offerings, as these are the companies dedicated to serving you.

One last thing: There is no reason we can’t have some fun along the way. IPC and the Los Angeles and Orange County Chapter of the SMTA are hosting a golf tournament on Sunday, and this is a great way to kick off the event. More info can be found [by clicking here](#).

See you in San Diego! **PCB**



Barry Matties started in PCB manufacturing in the early 1980s and in 1987, co-founded *CircuiTree Magazine*, which sold in 1999 as the leading industry publication.

In the early 2000s, he and business partner Ray Rasmussen acquired PCB007, followed by *SMT Magazine* in July 2010. With his many years of business leadership skills, Matties now produces this column, relating 25 years of successful business leadership, marketing and selling strategies that really work. Contact Matties at barry@iconnect007.com.

EVENTS

- [IPC Calendar of Events](#)
- [SMTA Calendar of Events](#)
- [iNEMI Calendar](#)
- [PCB007 Online Events](#)



[11th annual Flexible Electronics and Displays Conference and Exhibition](#)

February 6-9, 2012
Phoenix, Arizona

[Dallas Expo & Tech Forum](#)

February 7, 2012
Richardson (Dallas), Texas

[International Exhibition with Workshops on Electromagnetic Compatibility](#)

February 7-9, 2012
Düsseldorf, Germany

[Houston Expo & Tech Forum](#)

February 9, 2012
Stafford, Texas

[Pan Pacific Microelectronics Symposium](#)

February 14-16, 2012
Sheraton Poipu Resort, Kauai, Hawaii

[Electronics For You Expo 2012](#)

February 16-18, 2012
Pragati Maidan, New Delhi, India

[Southern Manufacturing 2012](#)

February 15-16, 2012
FIVE, Farnborough, Hampshire, UK

[IPC APEX Expo](#)

February 28-March 1, 2012
San Diego Convention Center,
San Diego, California

[PV SYSTEM EXPO 2012](#)

February 29-March 2, 2012
Tokyo Big Sight, Japan

[SIAF Guangzhou](#)

March 7-9, 2012
Guangzhou, China



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ADVERTISER INDEX

atg Luther & Maelzer GmbH.....	39
Atotech.....	2
Burkle North America.....	75
CA Picard.....	17
Electra Polymers.....	21
Fein-Line Assoc.....	87
Integral Technology.....	27
I-Connect007.....	3, 93, 97
IPC.....	77, 95
Isola.....	15
Maskless Lithography.....	31
Meptec.....	83
Microcraft.....	19
Ohmega Technologies, Inc.....	61
OMG Electronic Chemicals.....	7
Prototron Circuits.....	67
Rogers Corp.....	57
Semblant.....	5
Taiyo-America.....	73
Technica USA.....	33
Ventec.....	9
Viking Test.....	43

Standards, Specifications, Approvals, Oh My! It's the March Issue of The PCB Magazine!

Standards and specifications are fundamental to the PCB industry both locally and internationally. Standards harmonize fabrication processes and safety requirements and define reproducible levels of product quality and reliability, but which standards are relevant to PCBs? Who is responsible for writing and enforcing them? Our March issue navigates the maze of standards with articles from IPC, American National Standards Institute, Intercept Technology, Inc., and more.

Don't miss our regular columns, offering everything from common sense management ideas, to market reports and expert technical guidance. Not a subscriber? Click [here](#) to get The PCB Magazine delivered to your inbox every month.