PCB007 PRESENTS

January 2013

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12 HDI Use in Optical Waveguides
by Happy Holden

34 Built Board Tough: Budget DC Copper Plating for High-Reliability and Increased Capabilities
by Yash Sutariya

44 Addressing PCB Reliability—Technologies and Strategies
by Richard Ayes

56 High-Reliability PCBs in Mil/Aero Applications
by Zulki Khan

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JANUARY FEATURED CONTENT

HIGH RELIABILITY

This month, our authors scrutinize high-reliability PCB applications, where failure is absolutely unacceptable and the potential cost consequences of failure are enormous. What factors influence reliability, and how is PCB reliability measured? Find out this month!

12 HDI Use in Optical Waveguides
by Happy Holden

34 Built Board Tough: Budget DC Copper Plating for High-Reliability and Increased Capabilities
by Yash Sutariya

44 Eltek Addresses PCB Reliability—Technologies and Strategies
by Richard Ayes

50 Heavy and Extreme Copper for Maximum Reliability in PCB Design and Fabrication
Compiled by Epec Engineered Technologies

56 High-Reliability PCBs in Mil/Aero Applications
by Zulki Khan

FEATURED SHORT:

32 Contamination and Moisture Effects on PCB Reliability
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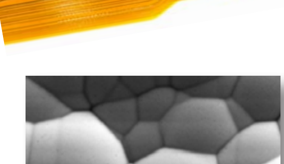
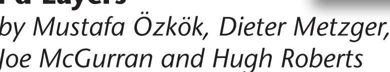
CONTENTS

ARTICLES

68 **The Problem with UL Approval of Rigid-flex Circuits**
by Bob Burns



80 **Wire Bonding and Soldering on ENEPIG and ENEP Surface Finishes with Pure Pd-Layers**
by Mustafa Özkök, Dieter Metzger, Joe McGurran and Hugh Roberts



VIDEO INTERVIEWS

48 **Multek Around the World**

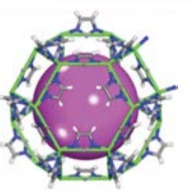
67 **Airtech Shows Staying Power in China**

SHORTS

11 **Flexible, Light Solar Cells Open Opportunities**

67 **New Nano Trap Protects Environment**

72 **Sandia Aims to Create Exascale Computing Operating System**



EXTRAS

102 **Events Calendar**

103 **Advertisers Index & Masthead**

COLUMNS

8 **PE: The Glass is Half-Full**
by Ray Rasmussen

64 **Global Competitiveness**
by Steve Williams

76 **Screen Printing Applications in Electronics—Part A**
by Karl Dietz

86 **Those Problematic Soldermask Issues—a Case Study**
by Mike Carano

92 **RF/Microwave: A Series of Unfortunate Events**
by Judy Warner

96 **How Can You Predict Your Company's DAM Future?**
by Gray McQuarrie

NEWS HIGHLIGHTS

62 **Flex007**

74 **Market**

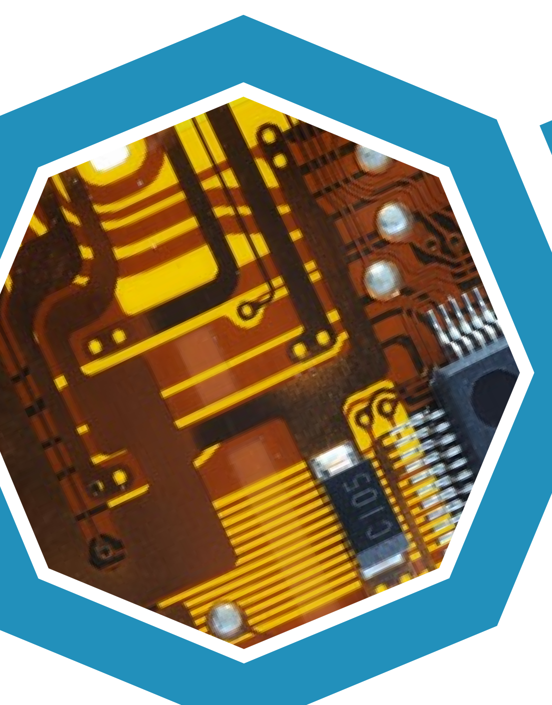
85 **PCBDesign007**

90 **Supplier/New Products**

95 **Mil/Aero007**

100 **Top Ten Most-Read PCB007 News Highlights This Month**

Standard FR4 Material · High Reliability · Lead Free Assembly
Signal Integrity · Halogen Free · Special Applications · Thermal Management
Flex-Rigid & Heat Sink Bonding



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PE: The Glass is Half-Full

by Ray Rasmussen
I-CONNECT007

SUMMARY: With IPC jumping into the PE standards game last year and with most OEMs and their suppliers paying closer attention to the opportunities printed electronics provides—and when you see all the dollars flowing into development—it's not a matter of if PE will take a bite out of the PCB apple, but when.

Not to overstate the implications, but I believe, as those who've been reading my columns already know, that printed electronics (PE) will take a bigger and bigger bite out of the PCB apple each year as the material sets mature and PE products move into mainstream electronics. With IPC jumping into the PE standards game last year and with most OEMs and their suppliers paying closer attention to the opportunities PE provides—and when you see all the dollars flowing into development—it's not a matter of if, but when.

Figure 1: From left to right: Nilesh Naik, Eagle Circuits; Joe Fjelstad, Verdant Electronics; and, Mike Dubois, Caledon Controls.

It's been frustrating for me over the years to watch the progression of this emerging circuit technology and realize that our industry was nowhere to be seen. A few folks could see the potential, but most had their collective heads in the sand. In a good year, I might see one fabricator walking the floor at Printed Electronics USA, held this year in Santa Clara, California. But instead of seeing just one fabricator, I actually ran into three or four and heard that a few more (including Viasystems) were in attendance. Still, the numbers of the missing are troubling.

I had a chance to spend time with Rocky Catt (see sidebar) of Sunstone Circuits and Nilesh Naik of Eagle Circuits this year. Both were attending the show for the first time. For Naik, it was both frightening and exciting. The potential to displace the PCB as we know it was certainly evident along with the opportunities of new markets and possibilities for fabricators.

Two obvious and immediate applications for PE technologies were being exhibited on the show floor. The first is flex. Plenty of flex circuits are already being made by the billions (literally). Over a billion RFID tags were sold in 2012. Single-sided, roll-to-roll systems for antennas, RFID tags, along with other simple circuits, comprise most of the market today. One exhibitor alluded to the fact that some of their PE circuits were being evaluated for an upcoming Apple product. They're dramatically cheaper and significantly lighter (when grams matter).

The second application was for QTA prototypes. Being able to test a board design in hours by sending the file either to your in-house system or to a service center down the street should have great appeal

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to those building tomorrow's products. Shaving days off the development time is worth a lot to these guys. In this case, you'd send the file and have to wait for approximately 10 to 20 minutes, depending on whether you wanted an eight-layer or 16-layer board. I'm sure there are still some kinks to work out with substrates and inks before systems like these will be mainstream, but they're close now.

Some of the systems we were looking at ran from $300,000 to 500,000, but a few companies were selling print heads for inkjet printers, which would allow companies to experiment with some of the PE technologies for just a few thousand dollars. Screen printing is another way to dabble without investing too much. I really encourage companies to start playing around with these simple PE systems to get a feel for what's possible.

What struck me at this year's show was the number of universities and research organizations in attendance or being represented. From PARC to Cal Poly, from Clemson to Georgia Tech, these institutions were peddling their latest and greatest innovations. I don't remember seeing them at previous shows.

As in years past, the folks at IDTechEx produced a solid conference with speakers from a variety of companies producing PE or looking for PE opportunities within their sectors or specifically for their companies' products. Presentations from military contractors like United Technologies and Boeing discussed the need to reduce weight and enhance capabilities while consumer product companies like P&G were looking for smarter, more enticing packaging solutions.

Years ago, I came across an article quoting a guy from Motorola about how they were looking to use the inside of their cell phone casings to apply the circuits, eliminating at least one of the PCBs. At this conference I heard it again in a talk by United Technologies. It's an obvious opportunity for product designers looking to reduce the size and weight of their products. Jetting a circuit onto a 3D surface is doable in the PE world. Component assembly systems are being adapted to support these configurations, as well. As soon as they get the reliability they're looking for, it'll be a done deal. It seems like they're almost at that point.

Figure 2: Rocky Catt (right) of Sunstone Circuits.

At the show this year, the organizers ran a concurrent conference and show on graphene, an amazing new material discovered in 2004. If you're not aware, here a few of the properties that have plenty of folks really excited: Nano-ribbons of graphene are 100x more conductive than copper; graphene has high thermal conductivity and is the strongest material ever measured. It's 200 times stronger than structural steel.

One of the offshoots of graphene is carbon nanotubes, which brings us back to printed electronics. There are carbon nanotube inks on the market today, with more on the drawing board. And to really make things interesting, one research group has figured how to align the tubes to make them even more conductive. It's pretty cool stuff. This wonder material will find its way into more and more electronic products in the coming years. Everyone's working on this. It's a game-changer and it's now closely linked to printed electronics.

PE: Not for Everyone

Well, yes and no. PE technologies have some distance to go before they'll take a big bite out of our industry, but it's coming. Make no mistake. Watch for hybrid PCB, PE systems in the near future, as more and more fabricators look for ways to differentiate their offerings to their customers. Staying on top of the progress of printed electronics will open the door to more opportunities for our industry. Certainly, the glass if half-full.

In response to my request for his impressions of the show, Sunstone's Rocky Catt had this to say:

To summarize, here are my thoughts.

To a degree, I felt like a bit of an outsider at first because most attendees and exhibitors were already connected to the industry. They know the products, processes, and terminology, and have specific applications in mind. To me, the obvious question is not only

what this means to the PCB fabrication industry, but specifically to Sunstone, which I describe as a low-volume (<100 pcs.), high-mix organization.

It was also clear, to which most of the exhibitors attested, that the industry is following many paths, and not one process has emerged as the leader. However, due to the variety of production processes, coupled with endless applications for the final product, this might be acceptable, perhaps expected. It's easy to see the differences in requirements between printed panels for a car's dashboard versus a cell phone versus a throw-away medical patch. They are all different with varying performance and price requirements.

The real question for Sunstone is: Can we satisfy customers' (current and future) needs as we all move into the near future? Will we satisfy those needs by ourselves or partner with someone?

The real take-away for me was that there are potential solutions. I started to feel more a part of the process when I realized that we can approach this from different levels, or progress through the levels:

- *Level I: For approximately $2,000, prototype kits using a standard desktop inkjet printer are available.*
- *Level II: For approximately $7,000, you can get a desktop graphics printer with software.*
- *Level III: For $25,000+, you can get an inkjet printer, or a screen printer.*
- *Level IV: For $60,000+ you can get an aerosol jet printer.*
- *Level V: The sky is the limit for specialized lines.*

Throughout these levels, services are available to assist.

Obviously, these solutions are probably not for those already directly involved in the industry, but do provide an avenue to test something or learn more about the processes. Also, different inks are to be considered, some needing a secondary process (sintering) and some that that do not.

Aside from our first exposure (the meetings in Irvine, California last year), this was Sunstone's first glimpse at process equipment and materials. It was an excellent introduction to exploring the possibilities. While events like this lead to more questions rather than solutions, it is keeping us on the path, and that's what's exciting.

Thanks again for the introductions—much appreciated.

We'll be in touch,
Rocky **PCB**

Ray Rasmussen is the publisher and chief editor for I-Connect007 publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuiTree Magazine.* Contact Rasmussen here.

Flexible, Light Solar Cells Open Opportunities

MIT researchers have produced a new kind of photovoltaic cell based on sheets of flexible graphene coated with a layer of nanowires. The approach could lead to low-cost, transparent and flexible solar cells that could be deployed on windows, roofs or other surfaces.

The new approach is detailed in a report published in the journal Nano Letters, co-authored by MIT post-docs Hyesung Park and Sehoon Chang, associate professor of materials science and engineering Silvija Grade ak, and eight other MIT researchers.

The new material, Grade ak says, may be an alternative to ITO. In addition to its lower cost, it provides other advantages, including flexibility, low weight, mechanical strength and chemical robustness.

HDI Use in Optical Waveguides

by Happy Holden
GENTEX CORPORATION

SUMMARY: Happy Holden presents the issues, materials and current processes being researched to create an integrated optoelectronic circuit board by European, Japanese and North American organizations.

Introduction

High-density interconnect (HDI) printed circuits play an important role for optical PCBs, and the challenge of optoelectronics and integration of photonics into the printed circuit. By 2012, expectations are that photonic PCBs will grow to a $2.5 billion industry. In this paper, I looked at the issues, materials and current processes being researched to create this integrated optoelectronic circuit board by European, Japanese and North American organizations. In addition to reviewing the global players in polymer photonics, the paper reviews the current programs of three of the eight groups globally[1]:

- EOBC-OptoFoil (Univ. of Ulm, Fraunhafer Inst, Daimler-Chrysler, Siemens)
- Truemode™ (Terahertz-UK)
- PolyGuide (Dupont, HP)
- OptoBump (NTT, Japan)
- TOPCat (NIST, 3M, Goodyear)
- JIEP (Japan)
- Electrical-Optical Circuit Board (UK)
- Terabus Program (IBM, Agilent)

Photonics and Electrical Performance

The performance of the conventional electrical interconnection technology is limited through the underlying physical properties. The most important disadvantages and problems respectively are that flowing electrons create a magnetic field; this introduces a myriad of problems at high frequency that makes up signal integrity and power integrity. These are major hindrances to the three growing challenges in advancing electronics:

- Bandwidth of the Internet for "packets" and the growing volume of data
- Challenge of the future for 'massively parallel computing cores' needing to communicate
- Many cores on the silicon chips needing connections.

The popularity of wireless devices and increasing applications that demand high bandwidth has placed an enormous burden on the Internet. Take, for example, the per-lane data rates of the PCIExpress interface that has increased from 2.5 Gbps for Gen 1.0, to 8.0 Gbps for the current Gen 3.0, and is expected to increase to 16 Gbps by Gen 4.0.

To accomplish these higher speeds above 10 Gbps, optical connections seem to be the solution. Figure 3 shows the growth of optical interconnect cabling for IBM supercomputers, growing from 5,000 fiber cables in 2006 to more

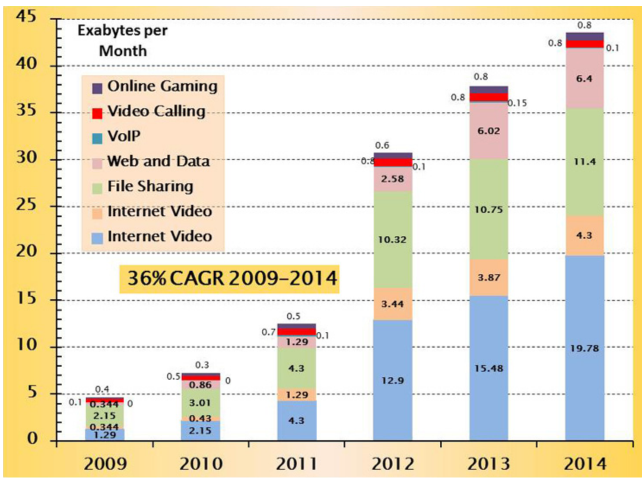


Figure 1: Internet bandwidth and IP traffic trends place a greater load on communication infrastructures, especially from 2012 on. Current popularity of 4G wireless devices, as well as internet video and file sharing are the chief demands. (Source: CISCO VNI, 2010)

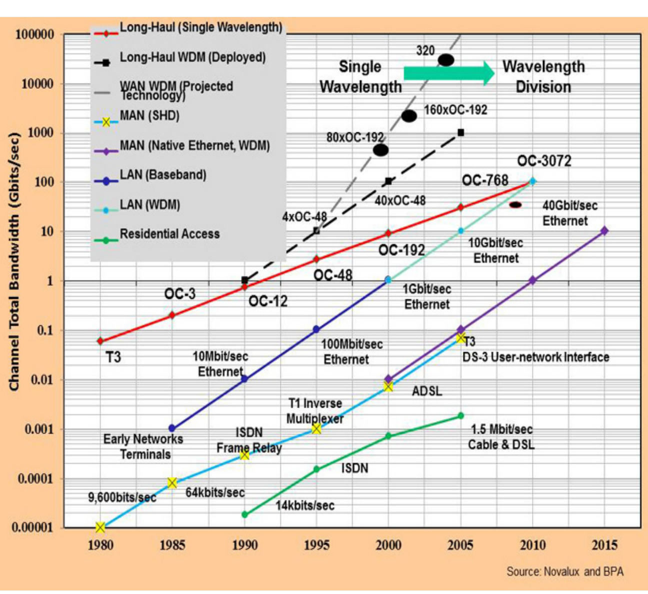


Figure 2: ITRS projected high-speed I/O data bandwidth trends for popular communication standards. (Source: ITRS)

Figure 3: In 2006, IBM introduced the Mare Nostrum supercomputer with 27 Tflops.

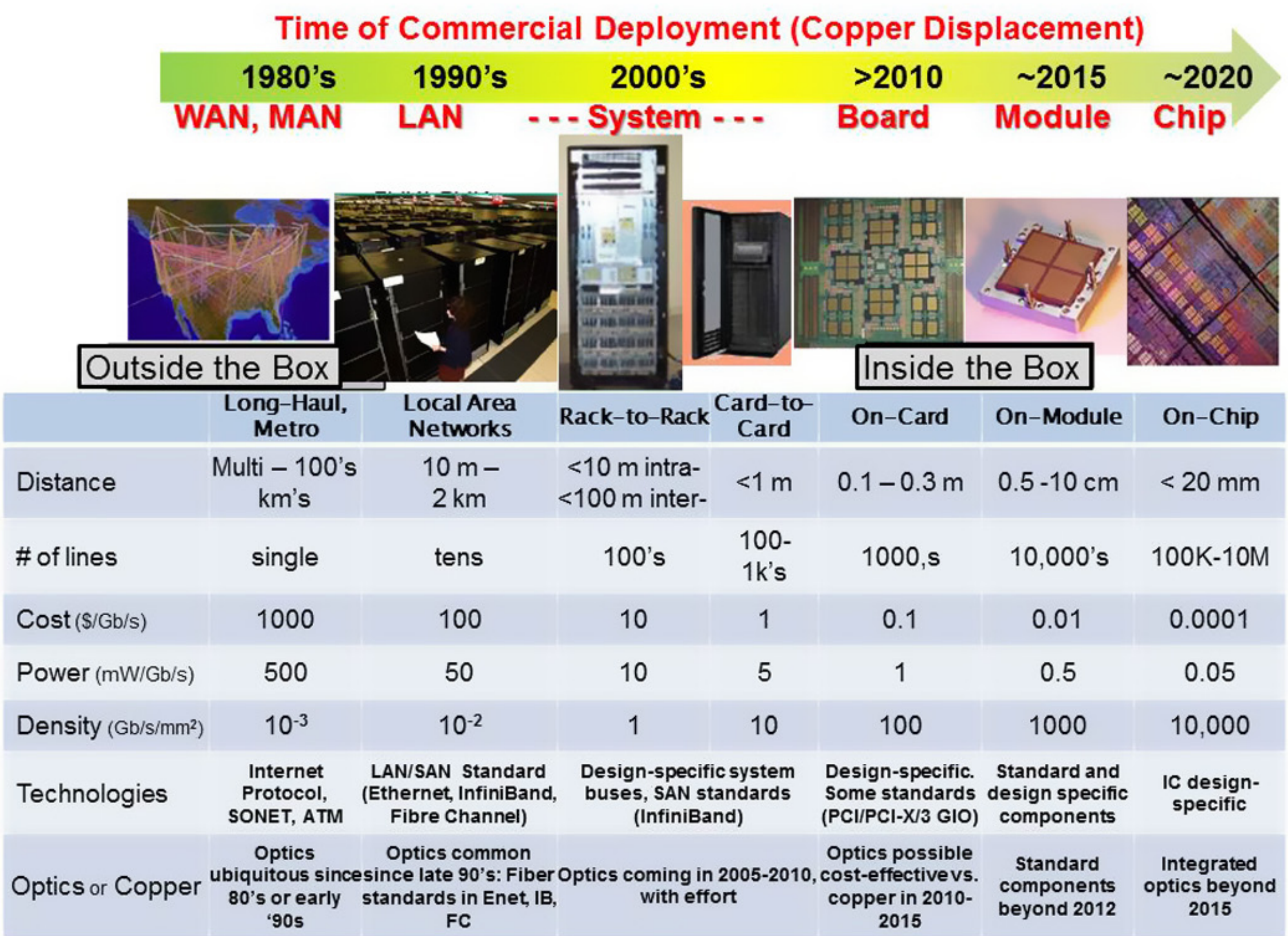
than 540,000 for the P775 in 2011. The next machine, Blue Water, will have over five million fiber-optic cables[2]. In these last two, instead of the fiber terminating at the PCB card edge, the Agilent and Avago MicroPOD optical connector actually extends onto the central processor module (Figure 3). The competition between electrons and photons (copper versus waveguide) is now down to the last 100 meters! As seen in Figure 4, a roadmap from the Terabus program[3], the number of optical lines is increasing, along with the density of those lines, correspondingly, the cost and power is coming down as well. Currently, the focus is on board-to-board channels of <1 meter, and for the "intra-system" of <10 m, and the "inter-system" of <100 m.

Electrons vs. Photons

Why the focus on photonics? Probably because Gene Roddenberry told us that was the technology for *Star Trek* back in 1966! But aside from science fiction, the photon has inherent advantages over the electron. First, it does not generate magnetic fields, nor is it affected by magnetic fields, which is a big advantage in noise reduction.

The second advantage is its density! As seen in Figure 5, a-d, a photon is much smaller and more compact than an electrical cable.

Thirdly, individual tracks (waveguides) and connectors can be packed closer together without generating noise or crosstalk. Figure 5a compares a one meter electrical and optical cable; a full rack of these cables (b); a 17.5 mm x 13.5



	Long–Haul, Metro	Local Area Networks	Rack–to–Rack	Card–to–Card	On–Card	On–Module	On–Chip
Distance	Multi – 100's km's	10 m – 2 km	<10 m intra- <100 m inter-	<1 m	0.1 – 0.3 m	0.5 -10 cm	< 20 mm
# of lines	single	tens	100's	100-1k's	1000,s	10,000's	100K-10M
Cost ($/Gb/s)	1000	100	10	1	0.1	0.01	0.0001
Power (mW/Gb/s)	500	50	10	5	1	0.5	0.05
Density (Gb/s/mm²)	10^{-3}	10^{-2}	1	10	100	1000	10,000
Technologies	Internet Protocol, SONET, ATM	LAN/SAN Standard (Ethernet, InfiniBand, Fibre Channel)	Design-specific system buses, SAN standards (InfiniBand)		Design-specific. Some standards (PCI/PCI-X/3 GIO)	Standard and design specific components	IC design-specific
Optics or Copper	Optics ubiquitous since 80's or early '90s	Optics common since late 90's: Fiber standards in Enet, IB, FC	Optics coming in 2005-2010, with effort		Optics possible cost-effective vs. copper in 2010-2015	Standard components beyond 2012	Integrated optics beyond 2015

Figure 4: Evolution of optical interconnects from long-haul fiber, wide-area networks to systems, boards and then modules and chips. (Source: IBM[3])

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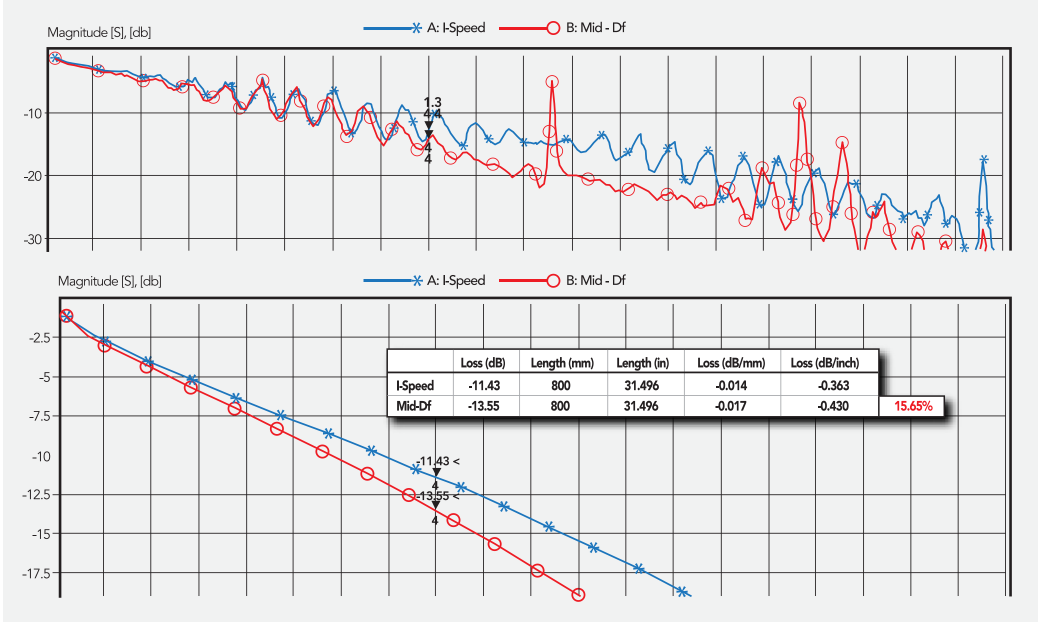

	Loss (dB)	Length (mm)	Length (in)	Loss (dB/mm)	Loss (dB/inch)	
I-Speed	-11.43	800	31.496	-0.014	-0.363	
Mid-Df	-13.55	800	31.496	-0.017	-0.430	15.65%

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Figure 5: Possible polymer waveguide materials, of which PDMS and haloacrylates are the most promising have their lowest loss in the 840-900 nm wavelengths while optical silica-glass used in fiber-optics-cables is lowest at 1550 nm. This is why the optical connections are 8x to 22x more productive than the older electrical connection.

mm cross-section of an optical connector has 144 10+ Gbps interconnects while the same size for controlled impedance electrical connectors has only 21 (c); electrical traces on PCBs have only two differential pairs while the same size of optical waveguides contains 16[4] (d).

These advantages are expressed by IBM's Optical Roadmap (Figure 6)[4]. In 2006, their supercomputers used a single optical cable at the card edge only. By 2011, as in the P775 computer, they had multiple optical fibers to the card edge and across the board to individual connectors at the processors (Figure 3, lower right). In research now, but deployed by 2015 will be the integrated optical waveguides on the card and backplane with optical connectors and sockets. By around 2020, it is predicted that the optical interconnections will be on the chip and between cores and memory, as well as board and backplane.

For the foreseeable future, systems will be a mixture of electrical circuits with high-speed optical and slower electrical data busses (Figure 7)[5]. In the far future, the actual circuit elements may be photonic computing, memory, encryption and analysis as well as data distribution, effectively realizing the predictions of science fiction writers.

Photonics and Waveguides

It is difficult in this short article to expose fully all the progress and details in optical board developments since 2003. A very good summary is found in the e-Book, *Handbook of Fiber Op-*

tic Data Communication: A Practical Guide to Optical Networking, Chapter 26: Optical Backplanes, Board and Chips Interconnects, which contains a very good summary of the technology up to 2008, with 43 excellent references[6].

Optical Waveguide Materials

Five materials are mentioned in literature from five commercial companies:

- PDMS (polydimenthylsiloxane) from Wacker
- PDMS from Chamie and Dow Corning- OE4140
- Photodefinable acrylate from Exxelis-Truemode
- Photodefinable epoxy from MicroChem-NanoSU-8-50
- Photobleached acrylate film from Hitachi Chemical and NIPPON Paint

There are a number of candidate polymer materials for waveguides, as seen in Figure 8[1]. Two waveguide materials seem to predominate: PDMS (polydimenthylsiloxane) and halo-acrylates. The fabrication processes can be summarized in Figure 9.

PDMS Polymers and Photodefinable Polyacrylate

The PDMS polymers are a popular choice. The reported waveguide losses at 850 nm are only 0.05 dB/cm and had high thermal stability (>230C). The acrylate waveguide polymers have been available in two forms, liquid and film. The liquid polymer is now distributed by Exxelis as Truemode. It has been the central material used in the UK Engineering and Physical Science Research Council's (EPSRC) Innovative Electronics Manufacturing Research Centre (IeMRC), and Integrated Optical and Electronic

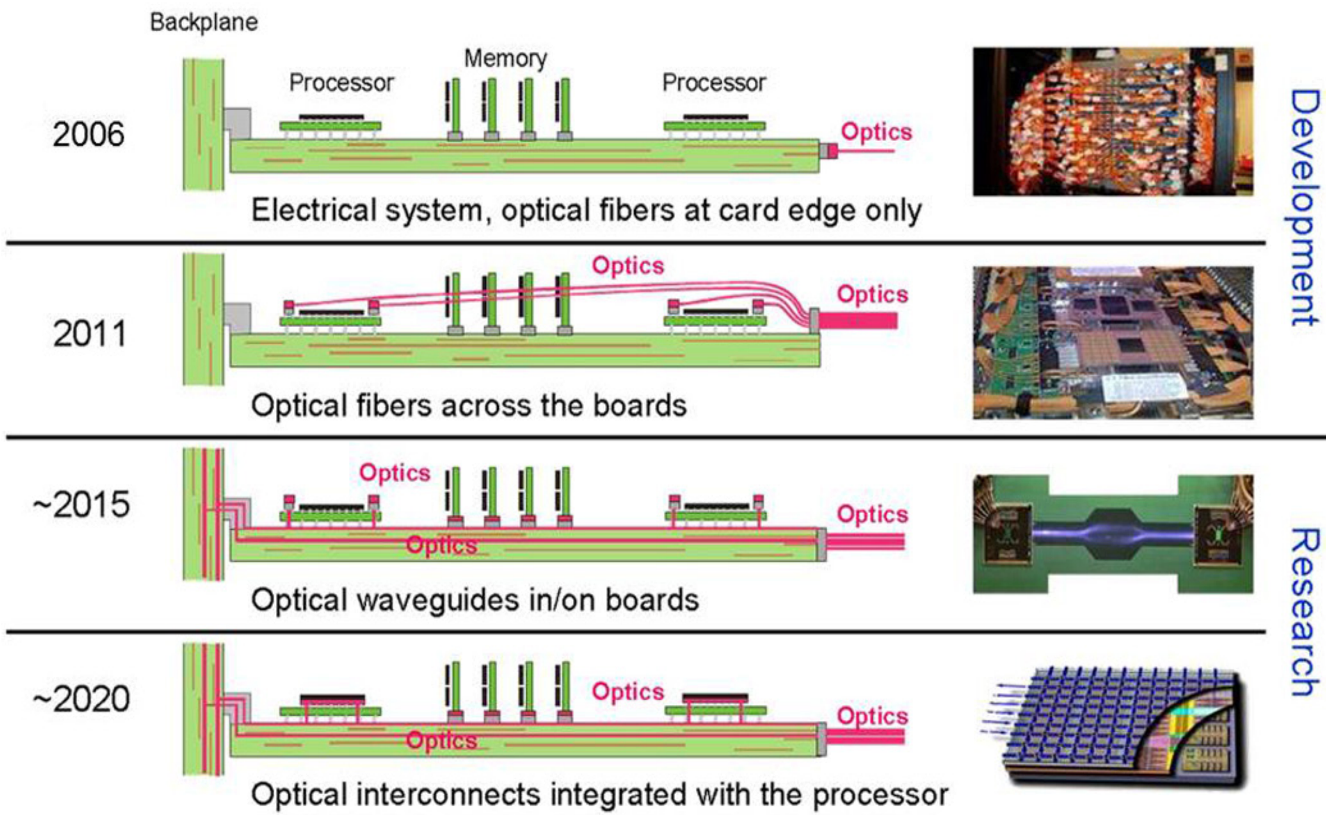

Figure 6: Proposed evolution of optical interconnections from 2006 until 2020, from single fiber, to multiple fibers, to integrated optical waveguides and eventually to optics integrated on the ICs[4]. (Source: IBM-Zurich)

Interconnect Printed Circuit Boards' (OPCB) landmark program at Loughborough University. This included 10 industrial companies and four universities in the UK.

A key objective of the various OPCB projects in the UK was the investigation of varied waveguide fabrication techniques and materials. A 10-layer board was designed by IBM-Zurich. It had eight conventional copper-clad layers and two optical layers on the outside, (Figure 9). The design rules for the 10 Gb/s optical channels was no less than 125 um with a vertical separation of no more than 250 um of the 70x70 um waveguides. When this is compared to a similar high-speed channel in copper, the separation grows to 1500 um, or a 36-fold increase in channel capacity (Figure 10[8]).

In experiments on the inkjet deposition of polymer waveguide structures focusing principally on the structuring of the core layer on top of the lower cladding (Figure 11). It was found that the UV cure optical polymer materials, photo-patternable polysiloxane and acrylates, and could be inkjet printed by controlling the viscosity and developing correct inkjet printhead waveforms. Using this technique, lines of optical polymer were initially deposited and then cured in a separate UV exposure unit. However, a key issue was preventing the spread of the material before curing, such that structures with a good height-to-width ratio (aspect ratio) were formed[6].

3D Waveguide Fabrication Techniques

Three ongoing programs seem to have the most publications, one from each major electronics infrastructure: Germany, the United States and the United Kingdom. However, many are studying the problem and government laboratories, institutes and universities from Austria, Australia, Finland, Canada, Korea, Japan and China have published on many of the topics brought up in this paper.

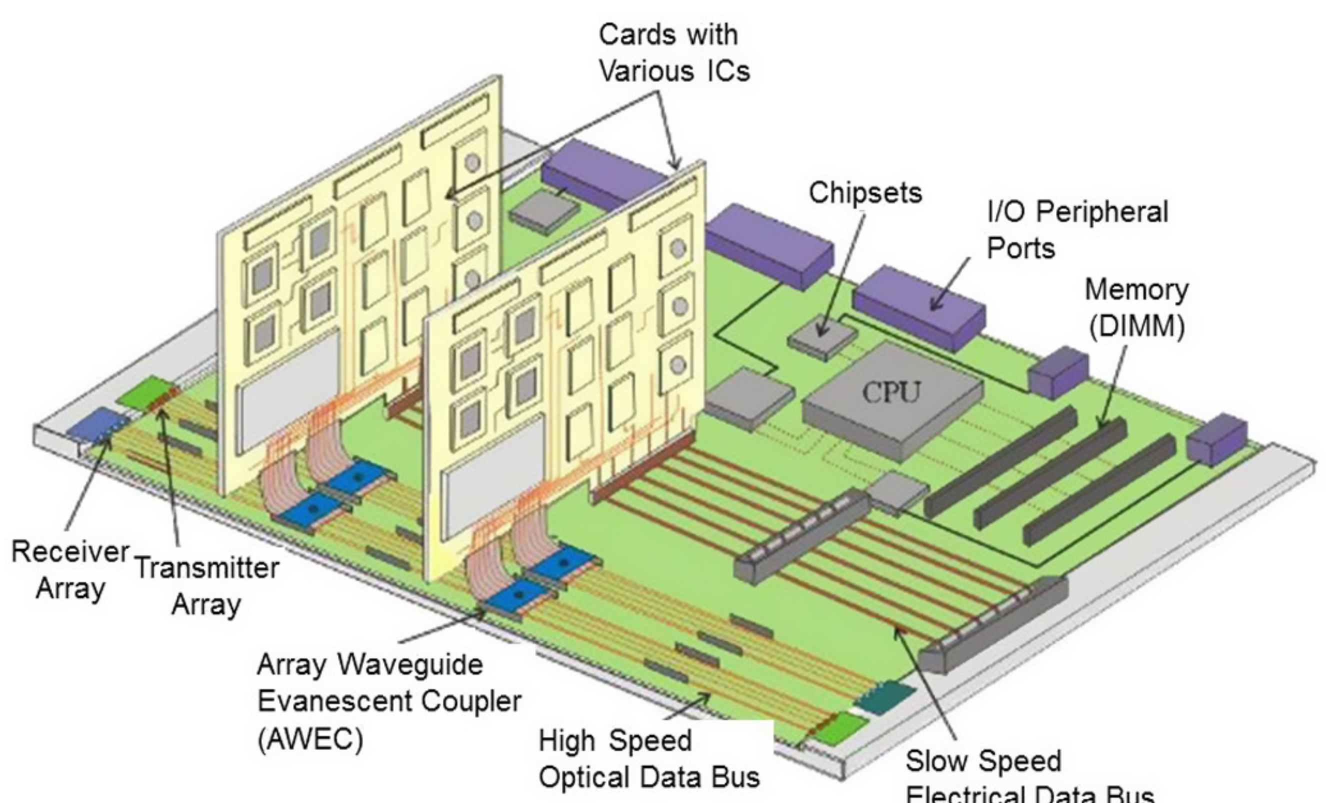

Figure 7: A schematic of the proposed array waveguide evanescent couplers (AWEC) technique and its use for multicard backplane with electrical and optical busses[5].

Figure 8: Six processes for defining polymer optical waveguides.

EOCB

This work is part of the German projects "Electrical/Optical Circuit Board" and "OptoSys," which are supported by the German government's Department of Education and Research (BMBF) under grants 16SV802/6 and 01BP801/01. (Dortmund, Ulm and the Fraunhafer Institute for Applied Solid-State-Physics in Freiburg are participating on a suborder basis.)

The progress in Germany is typical of that in the UK and USA, moving from the laboratory at universities to industrial companies building prototypes and the infrastructure. The Electrical Optical Circuit Board (EOCB) typified by C-Lab of Siemens in the last update is now replaced by commercial firms like Vario-Optics AG of Villingen, Switzerland (spin-off of Varioprint AG

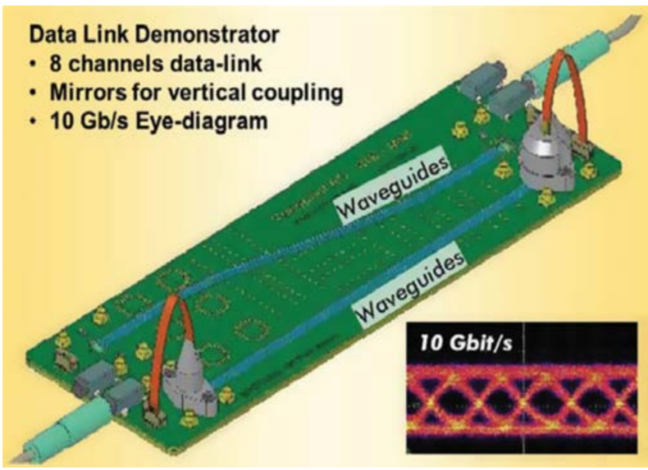

Figure 9: EOCB 10 Gb/s Data Demonstrator fabricated by Varioprint and demonstrating the PDMS polymer for waveguides[10].

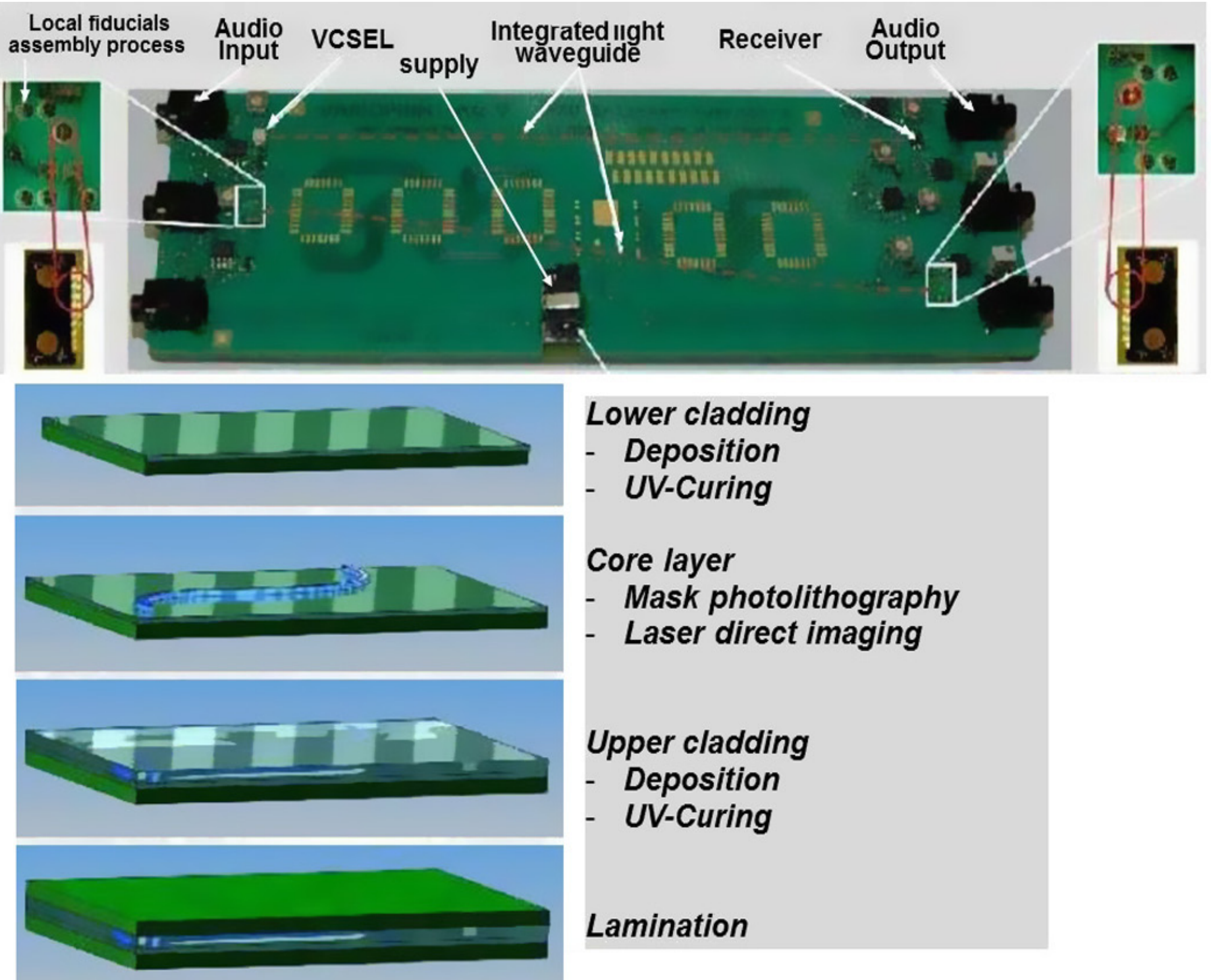

Figure 10, a and b: Data link demonstrator daughter board (a); waveguide fabrication process (b)[10].

of Heiden, Switzerland), and tested/qualified by Microtec GmbH laboratories[Pusch-2006]. Microtec tested and reported on the EOCB performance along with failure mechanisms and failure predictions[11]. This provided new information for standards and pre-qualification actions.

Vario-Optics participated in a number of demonstration test vehicles. One is seen in Figure 9, an 8-channel, 10 Gb/s data link with damping rates of 0.05 dB/cm @ 850nm and coupling losses <1.2 dB per interface[10]. A second is shown in Figure 10a, and the fabrication process is shown in Figure 10b with waveguides of 50 x 50 µm.

Integrated Optical and Electronic Interconnect PCB Manufacturing

In the UK, a large team of university and industrial companies collaborated under EPSRC's leMRC, and OPCB: University College London, (UCL) Instigator, Principal Investigator and Technical Project Leader; the School of Engineering and Physical Sciences, Heriot-Watt University, Edinburgh; and the Wolfson School of Mechanical and Manufacturing Engineering, Loughborough University—together with eight companies: Xyratex Technology (project manager and manufacturer of petabyte data storage systems), BAE Systems, Renishaw, Dow Corning USA, Exxelis (polymer supplier), Stevenage

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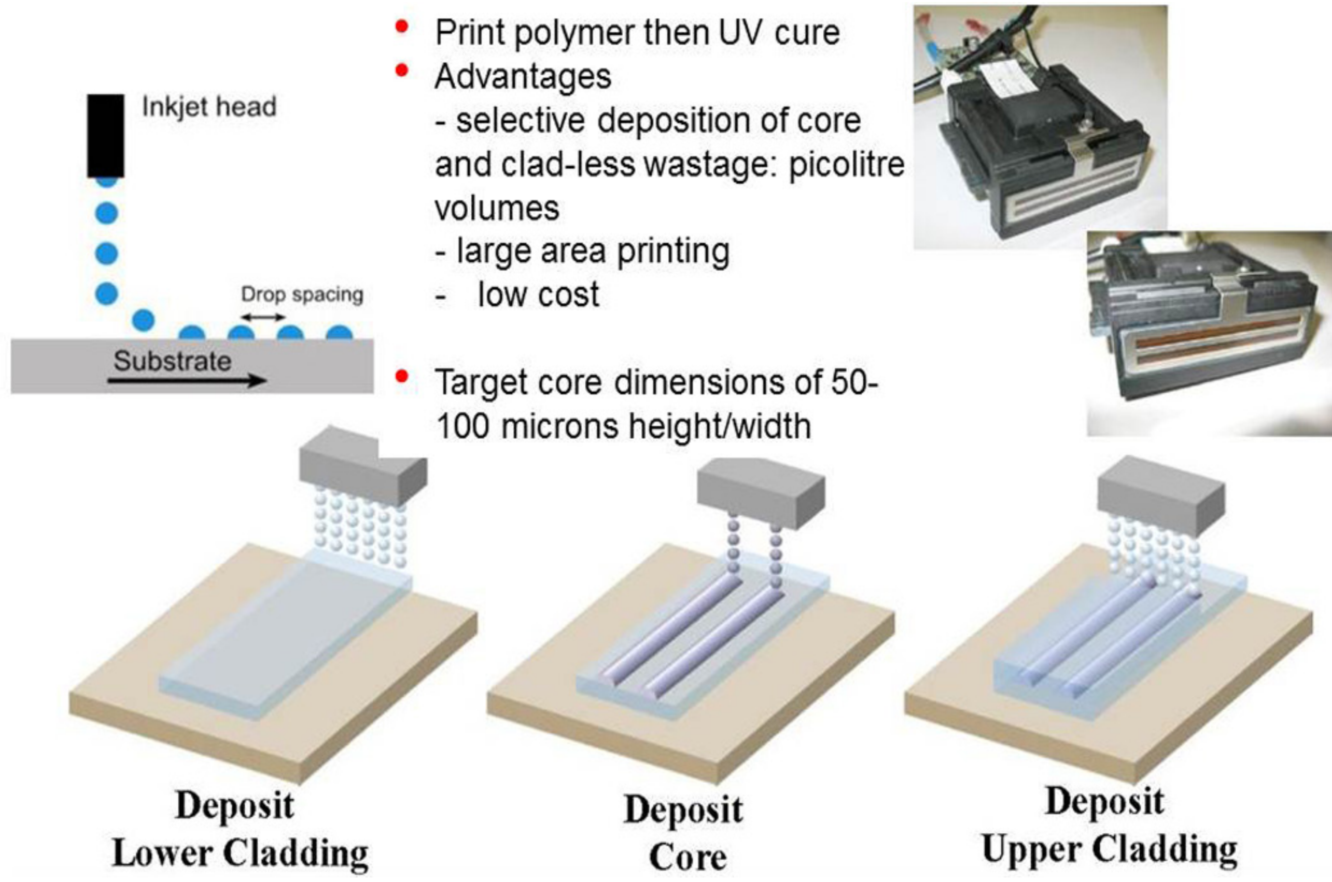

Figure 11: Inkjet printing of waveguides was conducted at Loughborough University for both poly-acrylate and polysiloxane using a Microfab Jetlab 4 with a Xaar 760 printhead. Various temperatures, viscosity and substrate pre-treatment were tested[14,15].

Circuits, Cadence Design Systems, and National Physical Laboratory.

The simple research in polymer waveguides that started in 1998 at Heriot-Watt University is now a very large program involving four UK universities and 10 industrial firms. The current reference [OPCB-12] has no less than 35 references published from 2005 to 2010. The purpose of this program is to develop manufacturing techniques for integrated optical and electrical interconnects in standard FR-4 PCBs. In particular, the purposes are:

• To establish waveguide design rules for several different manufacturing techniques and to incorporate them into commercial design rule checker and constraint manager layout software. PCB designers can easily incorporate optical connection layers without detailed knowledge of the optics involved in their designs (Figure 11)

• To investigate and understand the effect of waveguide wall roughness and cross sectional shape on the behavior of light and the effect on waveguide loss

• To develop low-cost manufacturing techniques for OPCBs. To develop and to compare the commercial and technological benefits of several optical PCB manufacturing technologies—photolithography, direct laserwriting, laser ablation, embossing, extrusion and ink-jet printing—for high-data rate, small and large (19”), rigid and flexible PCBs so that it will be clear which technology is best for each type of PCB

• To characterize the behavior of optical waveguide backplane systems in real-world con-

ditions, including temperature cycling, high humidity and vibration

- To design a commercial, low-cost, optical connector (dismountable, passive, self-aligning and mid-board) as the next stage from the prototype demonstrated in the earlier Storlite Project

Loughborough University is developing and testing polymer waveguide fabrication methods including direct laser write, laser ablation, and inkjet printing[14,15]. This culminated with the building of a hybrid integrated optical and electrical interconnected test system backplane incorporating multiple layers of copper tracks and polymer waveguides to demonstrate bi-directional, error-free interconnections using 10 Gb/s ethernet digital traffic, as seen in Figure 12.

Terabus Project (IBM's Optocard)

IBM Research has invested heavily in the past five years in optical printed circuit board technology based on multi-mode polymer waveguides. This is now referred to as optocard. This research was partially funded by the U.S. government as the Terabus Program[3,12]. IBM believes this technology will be needed to provide the bandwidth for future server generations (clouds), allowing highly integrated electrical-optical links of waveguides, flex and fiber between systems, modules, boards and chips.

A typical high-performance computer (HPC) has a "chip-module-board" structure seen in Figure 13a. The bandwidth limits are characterized in Figure 13b. The electrical packaging technology is mature and there is not enough

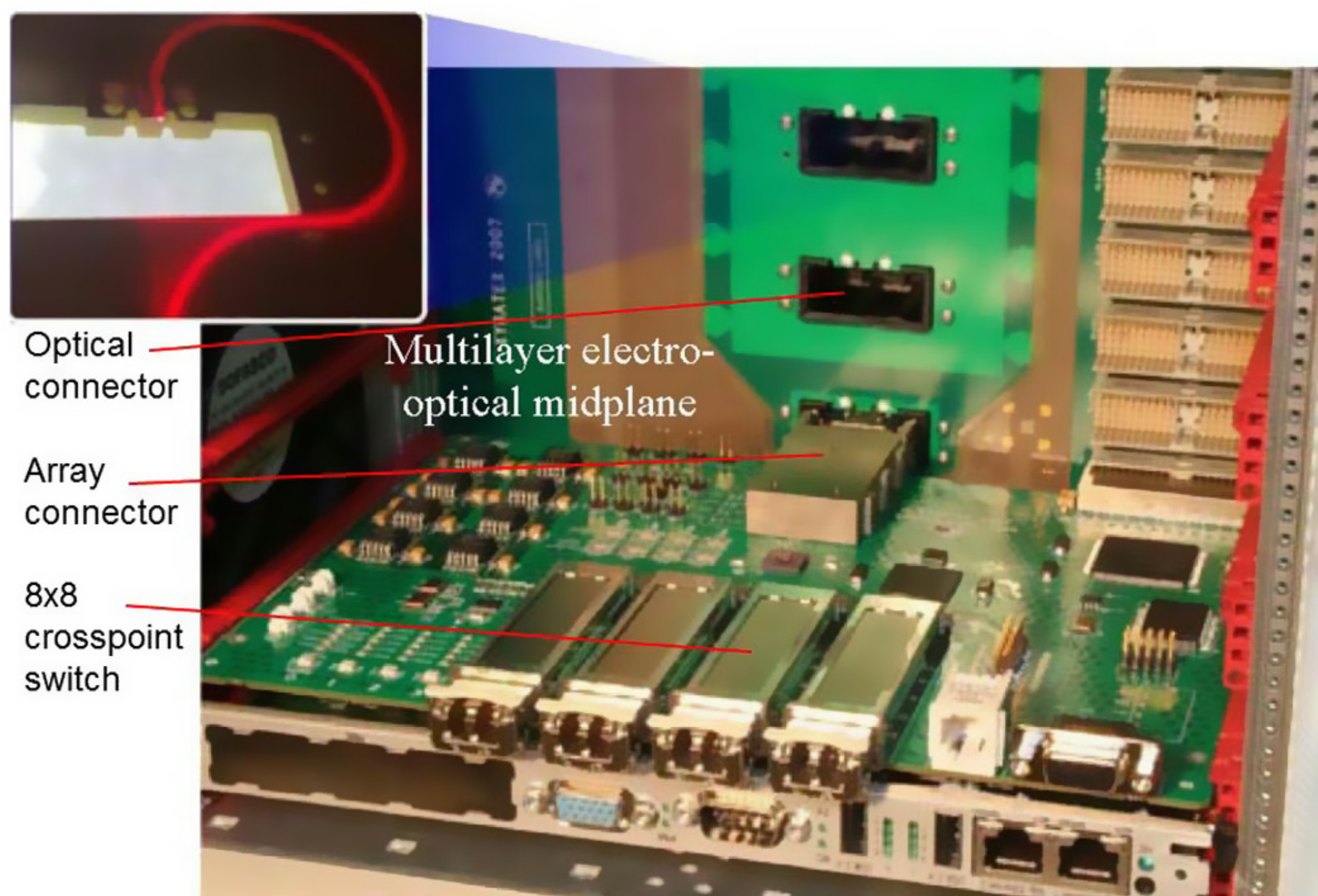

Figure 12: Hybrid integrated optical and electrical interconnected test system backplane incorporating multiple layers of copper tracks and polymer waveguides to demonstrate bi-directional error-free interconnections using 10 Gb/s Ethernet digital traffic[10].

space or pins (including per-pin BW) to get past the chokepoint at the module-to-circuit board interface, which is only 12.6 Tb/s. What is needed is a more miniaturized structure proposed in Figure 13c, using optical TX and Rx along with waveguides (OE modules) and optical bussing on the PCBs. This raises the bandwidth to 76.8 Tb/s. The organic OE module is seen in Figure 13d[11]. IBM's OE module progression is detailed in Figure 14. The goal is exabit computing (10^{15} bytes/sec) and in the short-term from 2008 to 2012, the progress for the optochip from 240 Gb/s to 480 Gb/s. The second step uses the O-PCB with the polymer waveguides and the third step includes direct optical connections to the OE Module.

Back to Today

Figure 15 shows the current architecture of the P775 supercomputer. The optical interconnects go directly to the processor module and use a 48-channel x 4 (48x4) operating at 12.5 Gb/s. These are supplied by Avago and soon, others. This allows the nearly 540,000 optical channel connections required for the system. Remember, Blue Water will require more than five million optical connections.

The optical connections and cables are seen in Figure 16. This 192-channel flexible waveguide is an optical backplane operating at 850nm and 12.5 Gb/s. The flex material is polyimide with 12 WGs per tail with 250 mm pitch. The fabrication of the Optocard flex cables and

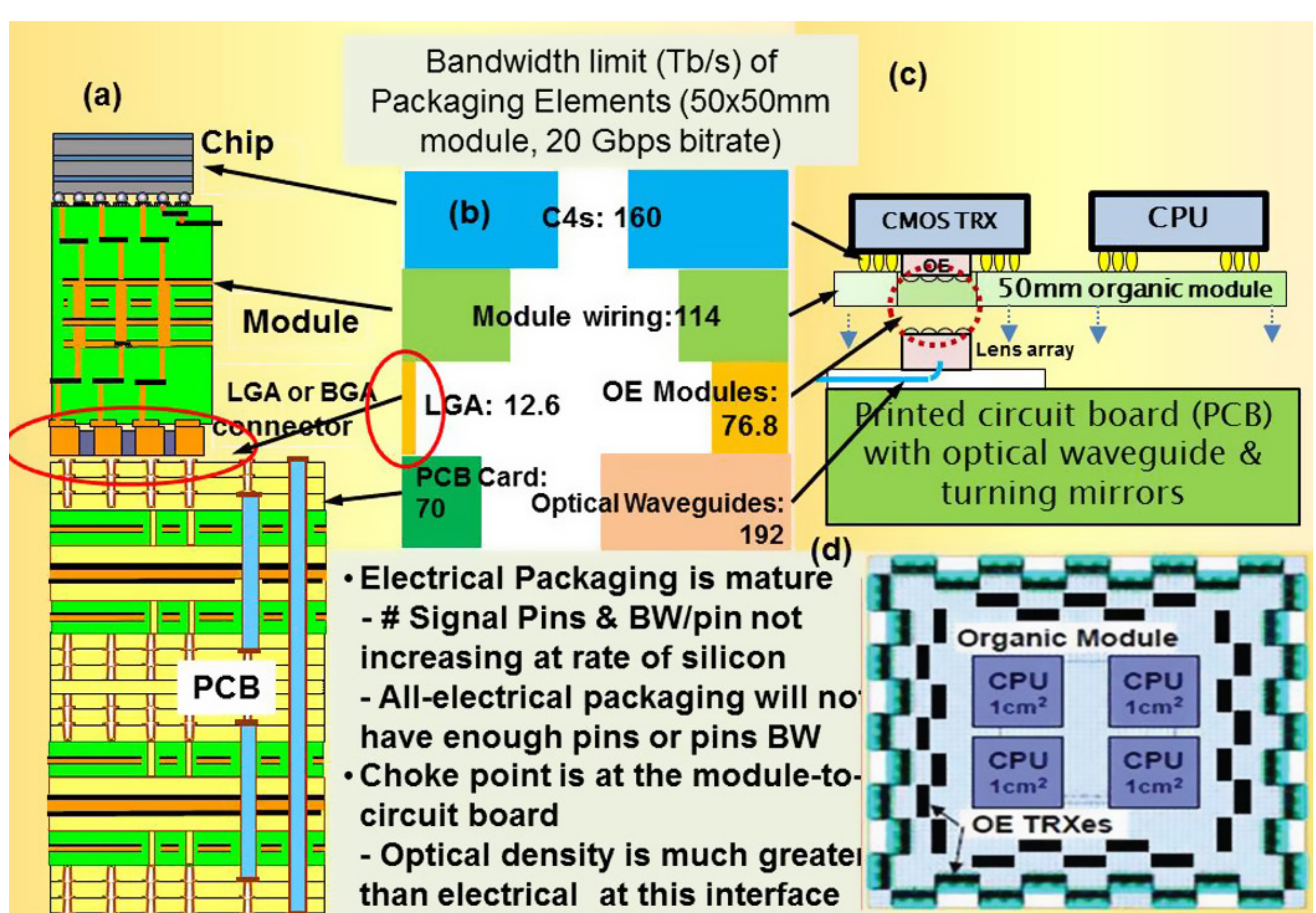

Figure 13, a-d: Structure (a) and performance (b) (bandwidth limits) of a "chip-module-board" structure, which is only 12.6 Tb/s for today's structure. What is needed is a more miniaturized structure proposed in (c), using optical TX and Rx along with waveguides (OE modules) and optical bussing on the PCBs. This raises the bandwidth to 76.8 Tb/s. The organic OE module (d).

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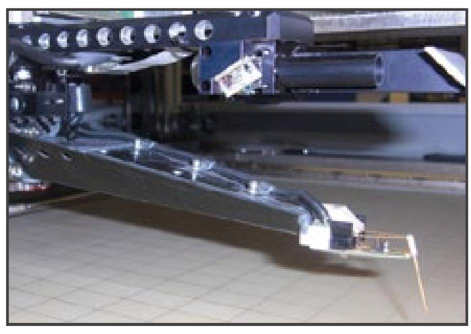

Basic specification	8 test probes, 4 XGA color cameras
Test area	610 mm x 510 mm
Smallest test point	35 μm (*with micro needle probes)
Repeatable accuracy	+/- 4 μm
Test voltage	up to 1000 Volts
4-wire Kelvin measurement	0,25 mΩ - 1 kΩ (± 0,1 mΩ ± 2 %)

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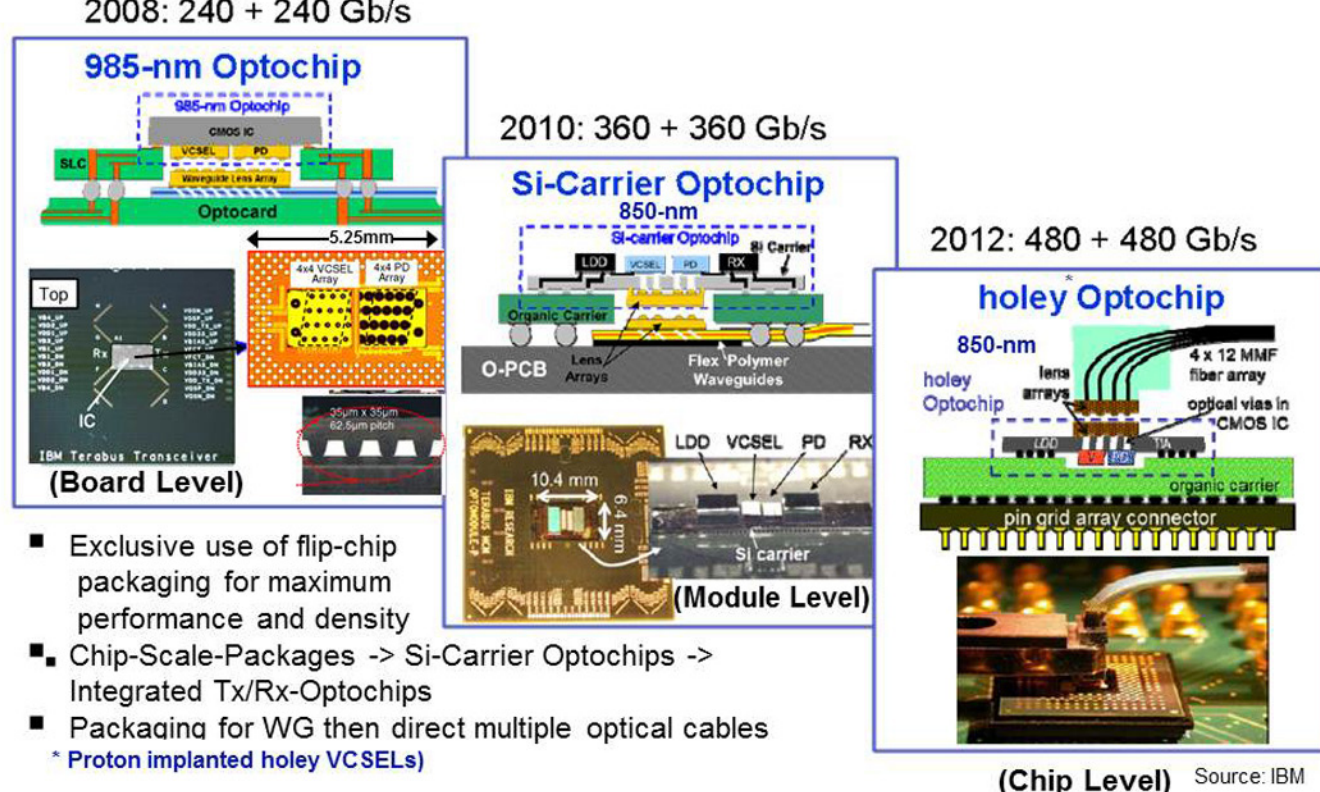

Figure 14: IBM's pathway to exabit computing, optical data paths from board level to module level to chip level with increasing bandwidth and number of channels at each step[16].

rigid waveguides was conducted by Endicott Interconnect Technologies (EIT) of Binghampton, NY[12]. These were fabricated by direct deposition of the waveguide material (Dow Chemical XP-5202A) onto a hybrid PCB substrate of Upilex polyimide with a layer of resin coated copper (RCC) laminated on both sides and to a frame.

The Terabus project's objective is to create a dense, hybrid packaging structure made up of optochips, optomodules connected with flexible waveguides to create the optocard with additional waveguides in a backplane between optocards. This is shown in Figure 17. The future vision is for an optically-enabled MCM as seen in Figure 6c, with performance projected in Figure 13c to the 2014 to 2016 era[9]. Other flex-optical cabling is ThunderBolt from Apple. Similar to Intel's LightPeak, Thunderbolt is a combined electrical/optical connection standard.

Figures 18a-g show these flex polymer waveguides in the optocard. A frame is employed to address the need of flat working surfaces that are required during optical fabrication, as seen in Figure 17a. The flex assembly is aligned to the optomodule and Pyralux and is used to laminate them together. The entire assembly is then baked under pressure to cure the Pyralux. The fully assembled structure is shown in Figure 17b. The attachment process is repeated at the other end of the waveguide flex to complete the optocard, as seen in Figure 14c. EIT also employed inkjet printing of the waveguides successfully[4].

The Terabus structure consists of the optomodule connected to the HDI PCB (Figure18a), with integral or flex waveguides (Figure 18b), patterned by the process (Figure 18c) and showing its cross-section (Figure 18d, e, f, g). The optomodule is an organic HDI chip carrier (known in IBM as SLC) with the optochip containing optical VCSEL and PD chips aligned by optochip lens array to waveguide lens array on the optoboard.

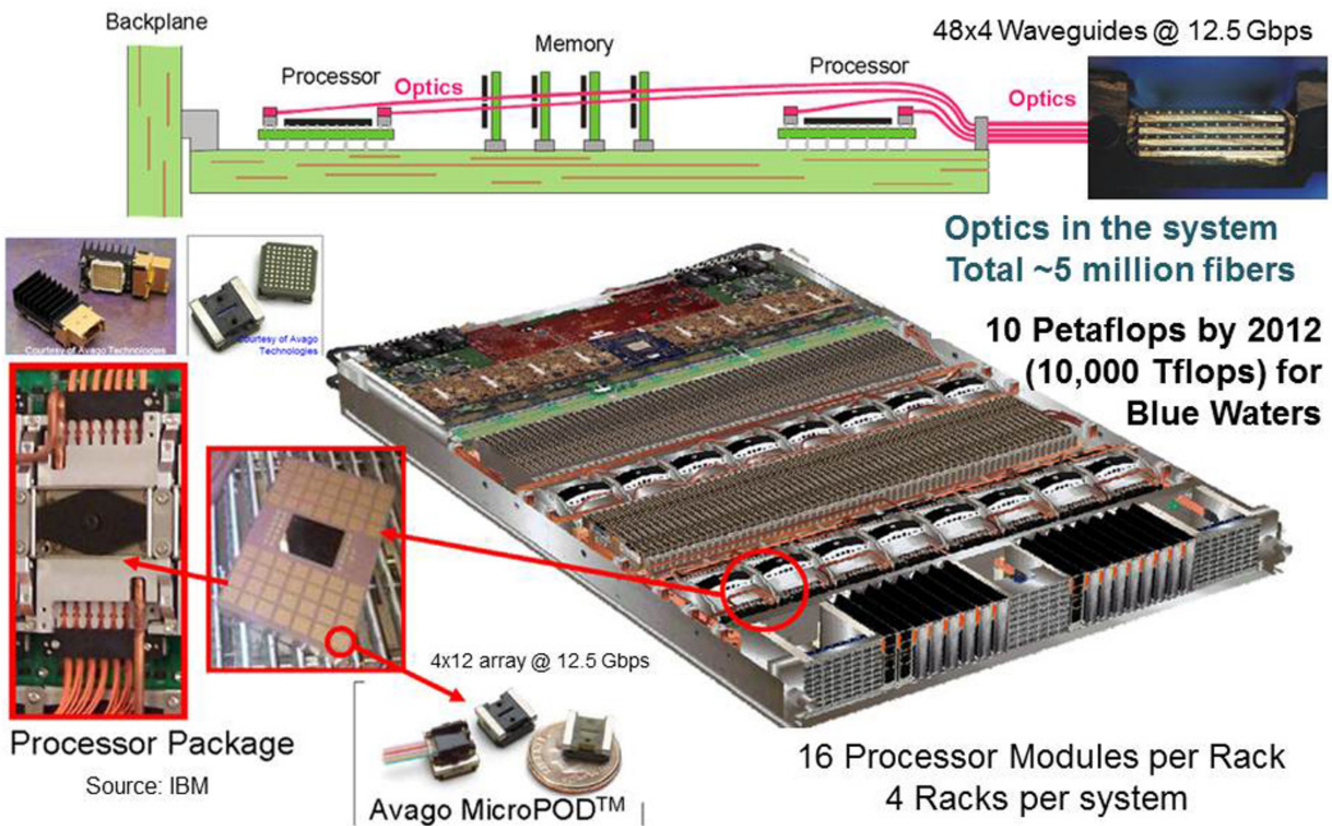

Figure 15: IBM opto packaging strategy (a); 2011 strategy of grouped waveguide cables to CPU modules (b); CPUs processor package and module that individual MicroPOD optical connectors (c); rack with 16 processor modules: four racks per system. (Source: IBM[17])

Figure 19 shows a close-up of a possible silicon chip carrier containing all the optochip elements in addition to the organic chip carrier[20]. The next step is the ongoing work to integrate all of the optical TX (VCSEL) and Rx (photodetectors) into the CMOS processors chips.

Conclusion

Embedded optical waveguides in printed circuits have progressed aggressively in the last few years due to cooperation between university and industrial partners. There are now several polymer materials available, several successful methods of fabrication for the waveguide in a PCB, as well as design tools and test facilities, reliability data and assembly techniques. A number of successful optical demonstration boards were fabricated by industrial firms capable of building these boards in production. The 12.5 Gb/s threshold per channel has been achieved and now the 16 Gb/s and 25 Gb/s are in progress. Soon, the 40 Gb/s channel will also be achieved. Hopefully culminating by 2020 with optical interconnects integrated into the processors and system performance in the 1,000 petaflop/sec range or an exaflop![21, 22, 23, 24, 25]. **PCB**

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Optical L-Links

Optical D-Links

4 connectors, 48 waveguides each

- Miltilayer waveguide optical connector
- Based on passive alignment
- Basic building block for optical backplane technology

24 WG channels at 850 nm
12.5 Gb/s/ch per flex sheet

Waveguide cross-section
35 µm
35 µm

Light incoupling

48 WGs with 62.5 ?m pitch

12 WGs with 250 ?m pitch

Source: IBM

Figure 16: The details of the optical cabling and backplane consisting of 192 waveguides, fabricated as eight flex conductor sheets of 24 WGs, divided into four connectors with 48 waveguides each; the L-links and the D-links operating at 850 nm and 12.5 Gb/sec[20].

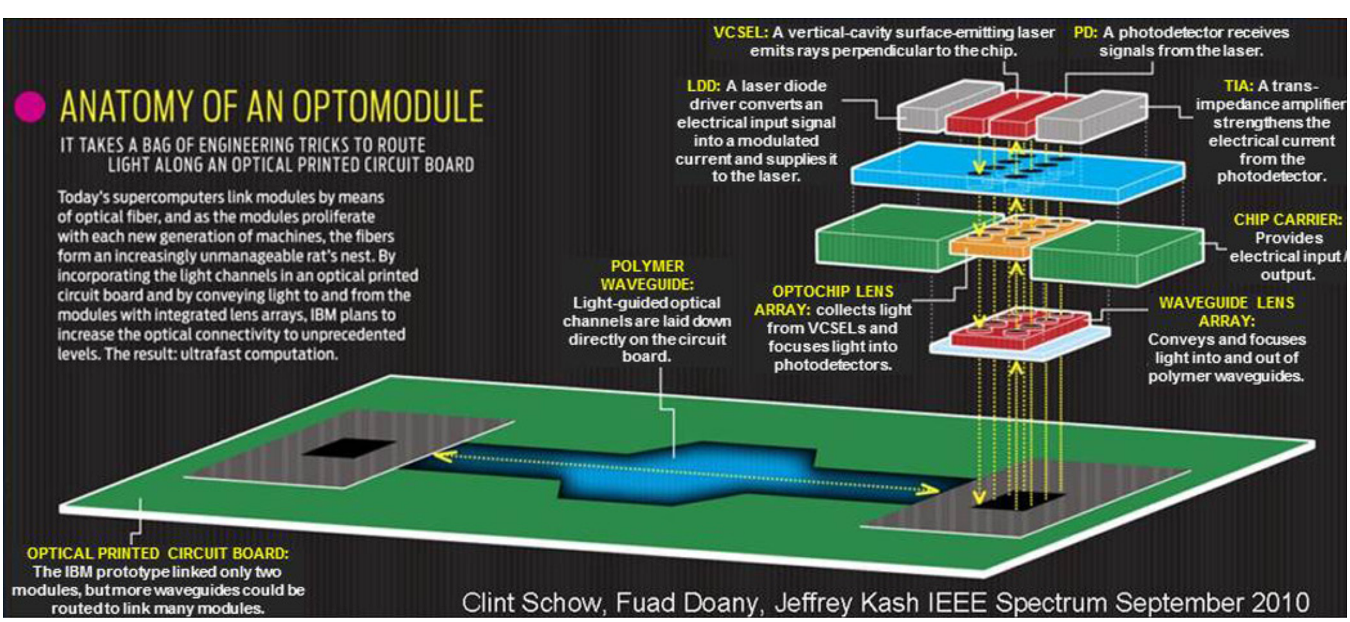

Figure 17: The details of IBM's optical system: optochip, optomodule and optocard connected by the polymer waveguides[20].

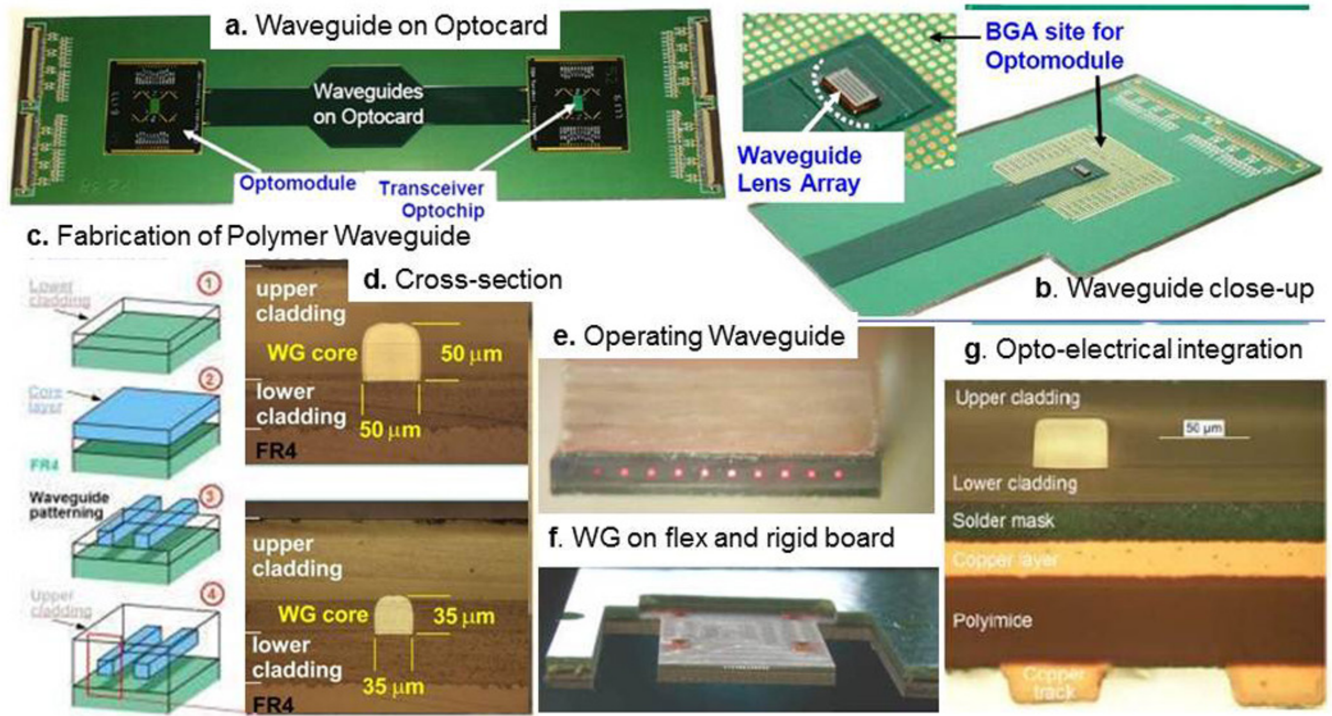

Figure 18a-g: Optocard with flex waveguide attached (a); flex waveguide close-up (b); waveguide fabrication process (c); design rules and cross-sections (d); operating waveguides (e); laminated to optomodule (f) ; completed optocard integration with the polymer waveguide (g)[10].

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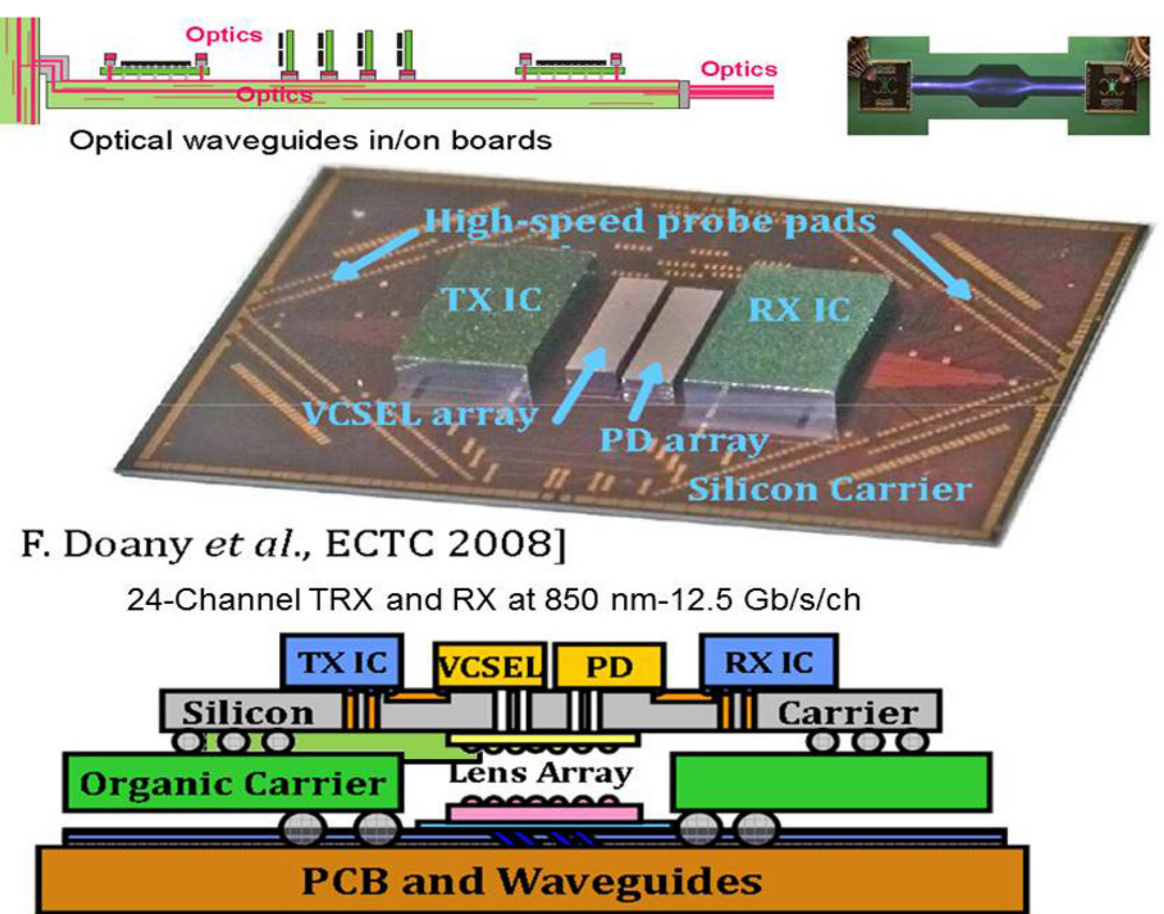

Figure 19: The Terabus project optical waveguide interconnects and related work using a silicon carrier in addition to the organic SLC carrier with future vision and performance of 2014-2016[9].

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Happy Holden is the director of electronics technologies at GENTEX Corporation in Zeeland, Michigan. Contact Holden at happy.holden@gentex.com

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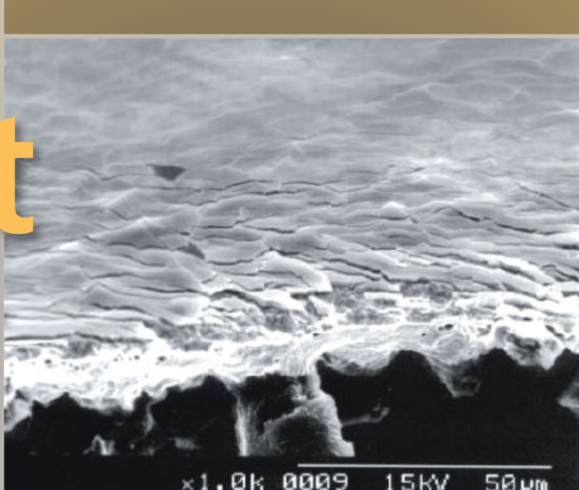

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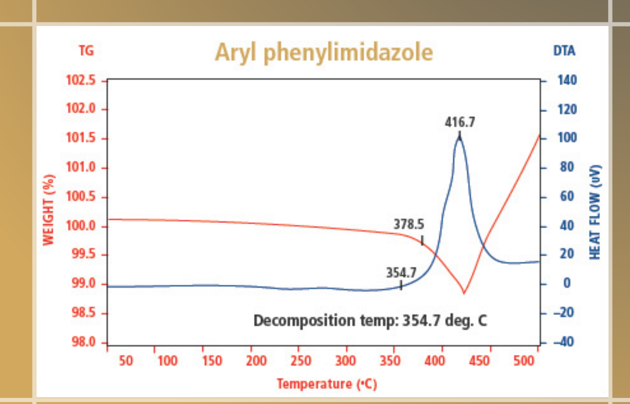

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Cascade Tap
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Contamination and Moisture Effects on PCB Reliability

Courtesy of ERA Technology Ltd.

Printed circuit boards can suffer from a variety of problems if the surface is contaminated with electrically conducting materials. Combined with moisture, the result is a lowering of resistance between tracks and pads, which can lead to corrosion of metals. It can also result in the formation of metal filaments that grow between pads or tracks on rigid or flexible circuits and between oppositely charged metal terminations of components, such as MLCCs, or between the pins of connectors.

The essential conditions required for this are a combination of ionic contamination, moisture and an applied voltage. The process is electrochemical with metal dissolving at one electrode—the anode, and being electrodeposited at the opposite electrode—the cathode. The electrodeposited metal normally takes the form of dendrites such as those shown in Figure 1.

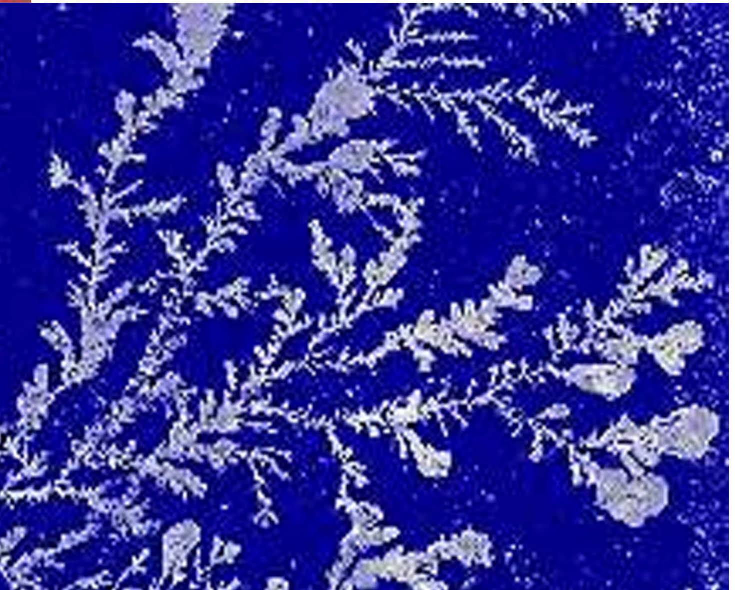

Figure 1: Silver dendrites growing on a flexible circuit between silver conducting tracks.

Dendrites can be silver, copper, tin, lead or a combination of metals and cause failures in electrical equipment by short circuits. Dendrite growth can be very rapid; failures have been known to occur in less than 30 minutes but can take several months or more. The rate of growth is dependent on the applied voltage, the quantity of contamination, and surface moisture. The amount of contamination required for silver dendrites can be extremely small.

Ionic contamination can arise from fluxes used during soldering processes, from handling (fingerprints) and other materials such as dust and dirt. Standard test procedures have been developed to measure the level of contamination which essentially involves washing the whole PCB in a solvent and measurement of the ionic conductivity. The severity of the washing procedures vary from simply removing surface soluble ions to extracting materials that has been adsorbed within the PCB laminate.

The ionic contamination level is calculated from the ionic conductivity of the wash solution and the total board area. The result is an average value across the whole surface. The development of standards of cleanliness and standard test methods date back to the early 1970s in the U.S., culminating in the publication of the original American MIL standards. It was from this work that the original pass/fail criteria of 10µg NaCl equivalence per square inch or 1.56µg per cm^2 were first proposed.

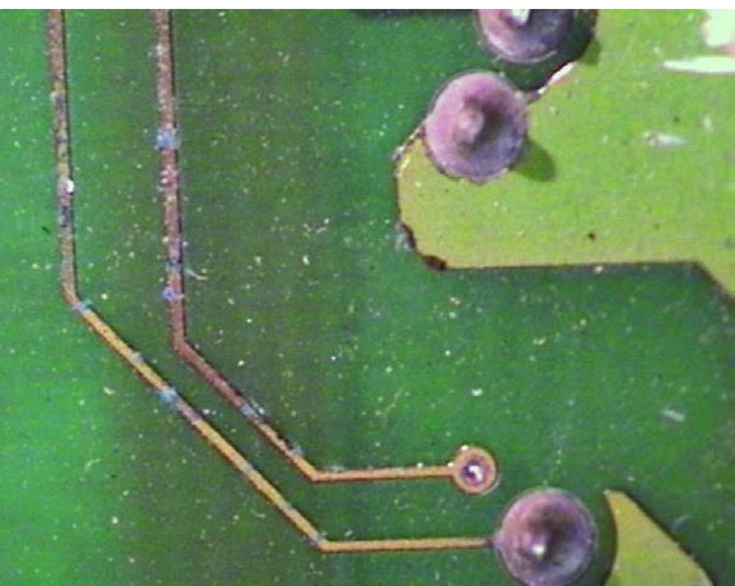

Figure 2: Corrosion of copper circuitry on PCB.

Cleanliness testing is now a routine procedure and manufacturers of both bare and populated boards are commonly asked to ensure their products meet contamination specifications based on this limit.

Equipment used under very dry conditions should not suffer from these problems unless there are large temperature fluctuations that result in condensation occurring on the surface of the circuitry or if the contaminants are hygroscopic and adsorb enough moisture to provide a liquid layer on the surface. However, very dry conditions are not recommended for delicate electrical equipment due to the increased risk from static discharge.

The ideal situation is constant temperature and a relative humidity of 40-50%. At relative humidities above 50%, there is an increasing likelihood that water condensation will occur on the surface of circuitry with changes in air temperature. Where the PCB surface is at a lower temperature than the ambient air, this cools the air adjacent to the surface, resulting in an increase in the local relative humidity. Condensation occurs when the temperature reaches the dewpoint. At the dewpoint temperature, the relative humidity reaches 100% and water is formed.

At high relative humidity values, but less than 100%, a thin moisture layer will be present on the surface which may be enough to decrease surface insulation resistance, cause corrosion or form metallic dendrites. The higher the humidity, the thicker the moisture layer and the faster corrosion or dendrite growth can occur.

Dendrites cause short circuits when they bridge across tracks or between pads and in some cases this has resulted in arcing and fires. Corrosion leads to open circuits especially with very fine pitch circuitry. Water is essential for both of these processes and the wetter the surface, the worse these can be. However, electrical equipment used at high humidity but less than 100%RH will have a thin moisture layer on the surface, which can be sufficient for damage to delicate circuitry. For this reason, particularly sensitive equipment is used in environments where both temperature and humidity are closely controlled. If the equipment is used in locations where this is not possible then an option is to use conformal coatings or potting, but these can lead to a wide range of other technical problems if not used correctly. **PCB**

Figure 3: Burnt PCB resulting from arcing, initially caused by dendrites.

Built Board Tough

Budget DC Copper Plating for High-Reliability and Increased Capabilities

by Yash Sutariya
SATURN ELECTRONICS CORPORATION
SATURN FLEX SYSTEMS, INC.

SUMMARY: Converting your old DC copper plating setup to one that produces high-reliability and higher aspect ratio copper plating for vias isn't difficult; some old jeans and a little resourcefulness can produce world-class plating capabilities in a small hand-plating line.

In last year's reliability issue for PCB Magazine, we touched on three "backbone" processes that are critical in yielding high-reliability PCBs. I'm going to focus on the copper plating portion of that article in this issue.

Remember the conversion kits that made a Fiero look like a Ferrari with new outer skins and decals? While nice on the outside, they still performed like the 4-cylinder roadster they were made to be. Or, for you baseball comedy fans, who can forget Willie Mays Hayes' Rolls Royce Beetle from *Major League?*

Well, we're going to discuss a project with quite the opposite outcome: converting your old DC copper plating setup to a setup that produces high-reliability as well as higher aspect ratio copper plating for vias.

Since I started in this industry, my dad has impressed upon me the importance of a proper copper plating line setup. In fact, back in the good old days he designed his own line to optimize all parameters related to copper plating—and had it built in-house. Our suppliers called it a $1 million R&D project as some of the features were not commonly used in the industry. Thankfully, it worked out and he was still able to pay my tuition and other (bar) bills.

When I acquired Saturn Flex in 2010, I inherited a classic type of plating setup: a basic three-rack line with a single rectifier. Like every teenaged 35-year-old, I didn't listen to what my dad was preaching and left the line as is, to focus on other aspects of turning around this company. Of course, the first higher-technolo-

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gy order we received saw us scrapping out more than half of the pieces due to copper plating issues. At that moment, we began a total conversion of our copper plating line to optimize all plating parameters with the goal of building extremely high-reliability and high-technology PCBs, which I will describe in this article.

Rectification

First and foremost is rectification. The most common setup is a single rectifier that provides power for multiple plating racks. While common, it is the least optimal setup. The ideal setup would be for each plating rack to have two rectifiers (one for each side), which allows for optimization of the amps applied to each side of the panels based on specific design characteristics—including aspect ratio and exposed copper area. This, in turn, allows you to hold a set number of amps per square foot (ASF)—no matter the degree of design imbalance of the PCB from one side to the other. This is critical on higher density designs as it will ensure that you meet minimum plating requirements in the hole, while avoiding over-plating the surface copper. Overplating the surface copper can result in plating resist entrapment between fine circuitry, which prevents etching of the underlying copper, thereby causing short circuits in your design that may not be able to be repaired.

Next we have to address the type of rectifier. My preference is going with a newer style rectifier that has solid state controls, less than 0.5% ripple effect, and is rack-mountable for ease of operation. It boggles my mind to see that folks are still using older, variable-frequency manual-control rectifiers due to the cost of newer rectifiers (or that they don't know the benefits of newer rectifiers). In researching rectifiers, I benefited from the fact that unlike most of the other equipment we use to build PCBs, rectifiers are not PCB industry specific and can be found through multiple sources. Coincidentally, I bought mine on eBay, of all places. I chose Sorenson DC8-75 rectifiers, meaning they were capable of outputting 75 amps at eight volts. Lower voltage is required for PCB copper plating as it allows you to plate at a slower rate for a longer period of time. This results in a much lower ripple effect. Ripple effect is AC current mixing in with the DC current output of the rectifier. The more AC that leaks into the DC current, the more chance you have for quality issues that include step-plating and increased additive consumption. Increased additive consumption can result in reduced uniformity and poor grain structure refinement, both of which can lead to long-term reliability issues.

For my three-rack plating line I needed six rectifiers, which I purchased for about $400 each. In addition we spent another $1,000 on 3/0 AWG welding cable to connect the rectifiers to the anode and cathode bars. All in all, not a huge investment and one that most shops can make—and one that is easy to pay off in as little as one higher technology quick-turn order. For the connections to be safe, we found all copper fittings which we then coated with plastisol to prevent oxidation that would inhibit current flow.

Agitation

Simply put, agitation is the movement of the plating racks to which the production panels are mounted in a back and forth motion

so that the copper plating chemistry is forced against the face of the panel. While it seems like a simple concept, it's surprising how many plating lines I have seen at smaller shops that have their plating racks fixed in place. That was also the case at my shop when I bought it.

By not agitating the plating racks, you are relying on only the chemical side of the copper plating process to plate your through-holes. This can result in severe "dog-boning" of the plated through-hole, meaning that the knees of the hole will plate much thicker than the middle of the hole. Not only does this setup require a much longer cycle time to meet minimum plating thickness requirements, but in the case of higher aspect ratio vias it can result in not achieving the minimum required plating thickness in the middle of the hole. Personally, I don't think meeting IPC Class III requirements on aspect ratios of 6:1 or higher is possible in a production environment without adequate agitation of the plating rack.

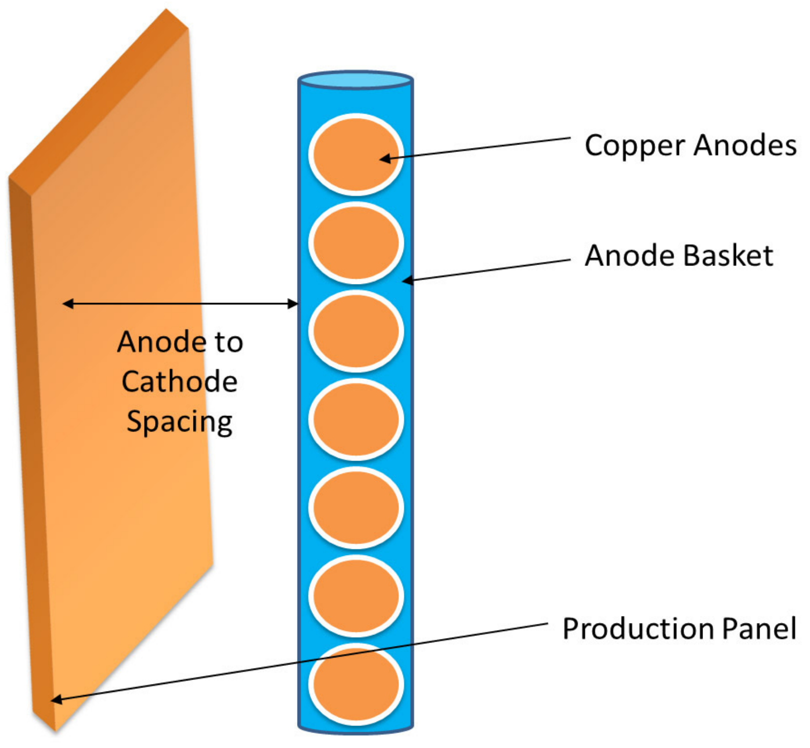
Agitation provides local solution flow through the holes, which not only enhances copper plating by replenishing depleted chemistry, but also removes air from the holes as a byproduct of the process.

A retrofit to an existing plating line is pretty easy. The first step is to bolt or weld on a mount for the agitation motor, which needs to be low RPM with high torque. We chose a ¼ H.P. motor from Marathon Electric (model# 5kh33gn-c140a) for a cost of about $200.

The next step is to build an agitation ladder. Once again, the materials and skills involved are not PCB-industry specific. We purchased a 1.5" square stainless steel rod and then contracted a local welder to put it all together (make sure you qualify that the welder has experience and the equipment necessary to weld stainless steel as it's not the same as normal steel). Another item to be aware of is to make sure that the agitation rack is insulated from the copper flight bars that hold the anodes and plating racks. We learned this the hard way, so you don't have to. The cost for the materials and labor was about $400.

We then purchased nylon wheels that the rack rolls on to reduce friction during movement. This reduces resistance to the agitation motor—increasing its life. You can use PVC saddles that the agitation rack slides along as well (we have this setup here in the Detroit shop),

but there will be resistance to the motor. If you're starting from scratch and have the height allowance, I'd recommend going with the wheels.



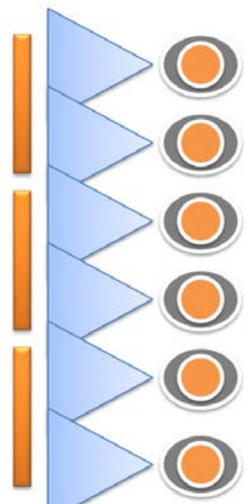
Spacing

The anode-to-cathode (panel) spacing within the plating cell is a very critical characteristic that I'm sure gets addressed when plating lines are initially designed. However, as time goes on and lines get sold, reinstalled, and/or modified, there is a chance that these requirements are superseded for capacity improvements or reductions. This happened to our affiliate in Chicago and after increasing capacity and making room for an education system, their anode-to-cathode spacing was a mere four inches.

The optimum anode-to-cathode distance is 10 inches. The optimal agitation stroke is two inches, meaning that the anode-to-cathode span will be eight to 12 inches, with a mean of 10 inches. The idea is to capture enough plating radius to cover your entire panel surface, while not being too far away such that the plating effect is weakened.

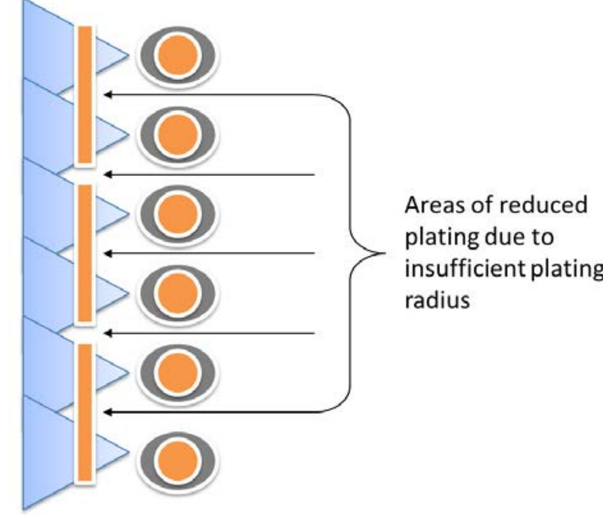
Copper Plating Setup

Top View w/ Optimal Anode to Cathode Spacing



Copper Plating Setup

Top View w/ Insufficient Anode to Cathode Spacing



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Plating Racks

Plating racks are one of those items in a PCB shop that make an owner really pucker up at the thought of spending money on. The reason is that these are treated as a secondary contributor towards copper plating—"it's only there to hold the panel in place." Not true. Plating racks not only lend mechanical stability to the copper plating process, but also serve as a conduit for electrical conduction.

My primary point of contention is that the panel is only making contact with the rack along one side. This means that the panel will have more current at the point of contact than it does at the other sides, resulting in a higher copper plating thickness variation. High variation increases the likelihood of PCBs with insufficient copper plating thickness in the vias to make it to the customer and into the field. Additionally, from a risk-management standpoint, the more contacts you have, the less impact a single poor

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contact will have on the overall quality of the panel.

Our solution to this problem was to make racks that allow for clamping the production panel on both the top and the bottom. If you don't want to custom-design your own rack, M&B Plating has a flexible design that allows for clamping on both sides of the production panel. Regardless of which sides the clamping occurs on, the main benefit is that you now have multiple opposing points of electrical contact for the current you apply during copper plating.

Another benefit to having this type of clamping setup is the added mechanical stability it provides. In a standard manual plating rack the panels will sway back and forth in a bath that has adequate agitation. This reduces the resistance that the panel gives against the copper plating chemistry, thereby reducing the volume of solution flow through the holes on the unsupported sides of the panel. The result will be added plating variation between one end of the panel and the other. Further, higher aspect ratio holes will be afforded much less solution flow on the end of the panel farthest from the clamp point, which translates into reduced copper plating thickness that may violate customer requirements, or result in all out failure at electrical test. These style racks can be purchased new for about $500-$800 each, depending upon the size, # and style of clamps, and types of material used.

Vibration

One common failure mode for open vias is air bubbles entrapped in the hole during copper plating. The air bubble prevents copper plating solution from traveling through the hole. Most air entrapment can be resolved through the use of agitation during copper plating. However, higher aspect ratio and smaller vias may need an extra kick to really make sure they are cleared out in the beginning of the plating cycle. This will ensure that solution is flowing through the holes for sufficient time to achieve the minimum desired plating thickness.

We purchased our vibrators from Cougar, model #ATU-42V1 for about $200 each, $600 total for our three-cell system. These are extremely simple to install since they typically run on compressed air. Also, they are mechanically attached to the cathode bars with nuts and bolts, so no welding is necessary. Make sure you fabricate a solid platform that will allow for optimal vibration transfer from the platform to the cathode bar. Before you run out and buy a bunch of vibrators, you need to consult with your chemistry and equipment suppliers to size them properly for your particular plating setup.

> ***"Before you run out and buy a bunch of vibrators, you need to consult with your chemistry and equipment suppliers to size them properly for your particular plating setup."***

Depending upon the method of chemical agitation, you may not even need to run them during the entire plating cycle. You would just run the vibration during the first five to 10 minutes of the plating cycles. The reason for this is that most air is entrapped in vias during the initial movement of dropping the panels into the plating bath. Once the air is out, there is little risk of re-introducing air back into the via unless you have a problem with your air system for chemical agitation…which leads us to our final topic of conversation.

Chemical Agitation

Chemical agitation is most often achieved using an air bubbling system. The air bubbles agitate the chemistry as they move from the bottom of the tank (where they are introduced) to the top. The size of the bubbles typically makes them too large to enter into vias, but there is always a chance that plastic fibers or other errant materials in the lines can cause them to break up into sizes small enough to create an issue.

Chemical eductor systems address this issue. Instead of using air to create chemical agitation, they use fluid pumps. Typically, copper plating chemistry is pumped out of the tank from one

end, and reintroduced at a high velocity at the other end across the surface of the panels. Individual chemistry suppliers tend to have their own feelings of what is an optimal setup so it's best to consult with them prior to designing and installing a full chemical eductor system. Between the plumbing, labor, and pumps, you could expect to spend upwards of $1,000 for a small three-cell setup; however, once it's done, it's done. These pumps typically last for a long time, but I would still use a union to hook them up instead of hard plumbing.

Conclusion

While converting a copper plating line isn't as exciting or fun as buying and installing a brand new drilling machine with 225k spindles, linear X, Y, and Z motion, vision, it's still an equally valuable improvement to your process.

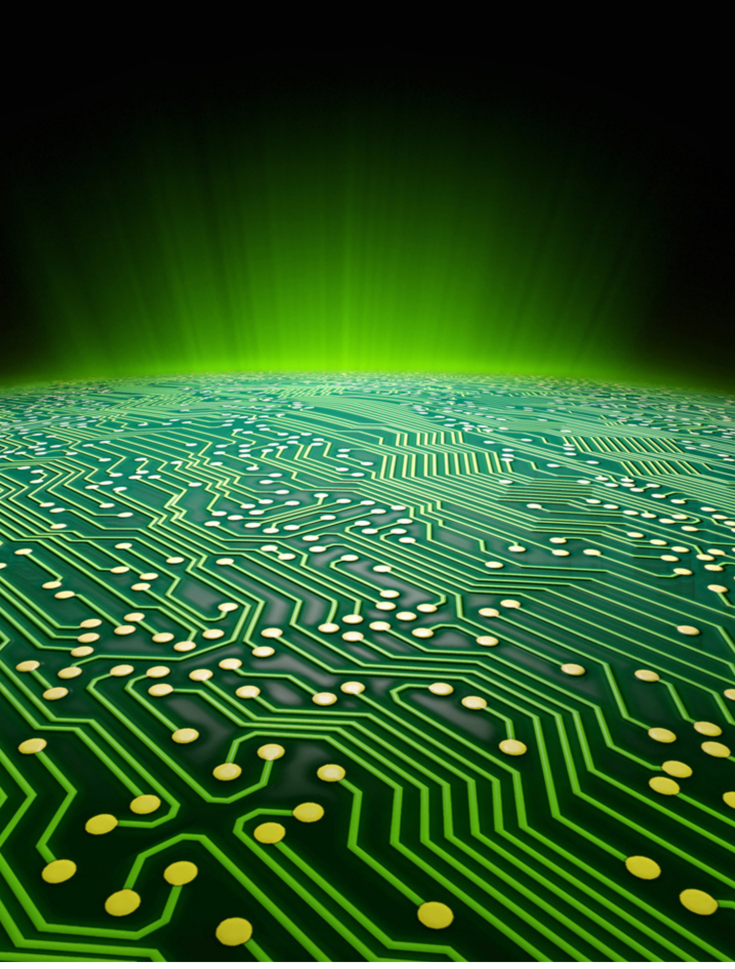
Further, this isn't a zero-sum solution in that you need to implement all of the improvements in order to benefit. Every one of these ideas offers an incremental quality and capability improvement so even doing one at a time, over time, will garner benefit. In total, after spending less than $8k and having four pairs of jeans eaten through by chemicals, we now have world-class plating capabilities in a small hand-plating line. Basically it's like a Ford Fiesta with hot rod engine.

There's nothing stopping you from doing the same. Just wear polyester Dickies during your install—you'll save a couple of bucks. **PCB**

Yash Sutariya is vice president of corporate strategy at Saturn Electronics Corporation and owner/president of Saturn Flex Systems. Contact Sutariya at ysutariya@saturnelectronics.com.

FEATURE

Addressing PCB Reliability—*Technologies and Strategies*



by Richard Ayes
I-CONNECT007

SUMMARY: I-Connect007's Richard Ayes and Roberto Tulman, vice president of technologies and CTO of Eltek Ltd, an Israel-based manufacturer of rigid and rigid-flex printed circuit boards, discuss some of the technological issues involved in reliability of PCBs for military, aerospace, medical and industrial equipment applications.

How was business last year, and how do you see this year shaping up for the company?

Last year has been a very challenging one for the industry, but Eltek managed to keep its revenues stable. The industry within the Western countries has been shrinking, and the east has also been suffering from decreasing orders. China started to serve not only mass quantities, but is also biting into our classical markets. We saw the market's pull for cutting-edge technologies with more complex designs, multiple laminations with mixed materials, smaller vias and narrower lines and spaces.

Eltek invested $2 million in equipment last year. We plan to invest much more in the coming years to enhance our capabilities. The R&D and engineering teams are actively and intensively looking for solutions and new techniques to provide our customers more options and solutions. We have several machine development projects with equipment manufacturers to adjust the equipment to Eltek's needs. The coming year will find us in the middle of an equipment upgrade in the main production lines, with new challenging projects to manufacture more demanding and functional boards.

The defense and aerospace markets account for nearly half of your market share. From a PCB manufacturer's point of view, how has the defense and aerospace electronics industry changed over the past five to 10 years? What are some of the key technology developments, and how did they affect your PCB business?

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Those markets were characterized for generations as the most conservative ones. They wouldn't change a component's shape or the design's rules for any reason. You could easily recognize a defense board just by looking at it. About 10 years ago, something started to change. I believe the factors could be the unavailability of the traditional components, the need for higher frequencies, and of course, the drive to fulfill the required functionality.

Today, the boards for the defense and aerospace markets specify very complex stack-ups, blind and buried vias, via-in-pad designs, high-frequency materials and mixed technologies. The tier 1 customers became very sophisticated and their requirements usually include intensive audits of our plant, meticulous testing of the finished boards, reliability testing for new designs, external laboratory use, and more. These markets, as well as others, learned to exploit the flex-rigid boards' design to a maximum; although those boards are usually more expensive, they provide excellent solutions for reliability and weight and space savings. Another important fact is they learned to bring the new designs to Eltek's technology team in the preliminary phase. This non-intermediate communication between Eltek and the customer in the early stages can increase success and lead to better designs, better manufacturability and lower price.

The medical equipment segment, meanwhile, is your second biggest market. Similar to the above question, how has your business evolved to cater to the technology requirements happening in the medical equipment sector? What key drivers have led to these changes in your manufacturing strategies?

The medical market, which we are proud to serve and be part of the effort of improving health and saving lives, has changed dramatically over the past 10 years. The market has been driven from standard boards to the most complex boards possible to manufacture in the high-reliability world. The healthcare sector has developed, in the last year, invasive and non-invasive systems capable of replacing expensive surgery. These systems include body-implantable devices and surgery-replacement apparatuses, which require very high reliability in order to perform well and deliver.

To gain the capabilities needed to cater to these market requirements, Eltek improved and changed its equipment and technologies to be able to manufacture reliable flex-rigid boards with multiple flex layers. Today, these boards include very dense circuitry, sequential laminations, cavities, and different types of connectors in both the flex and rigid layers with very accurate dimensions. We needed to manage and improve our registration tools and test, and use lightweight materials and mix between different types of resins.

All these advances are implemented along with intensive R&D work to maintain reliability. All-layer-vias boards are being manufactured for body-implantable devices, flex-rigid boards for CT and MRI machines, special boards for medical pills, endoscopy boards, and more. Another major change being seen in this market is the final finish of the boards. Many of the boards, which have soldered and wire-bonded components, demand different types of final plating. While in the past we used to perform selective plating in the different areas of the boards, now we need to migrate to other technologies like nickel, palladium or gold, for example, because of the high density of the circuitry.

What were the biggest technological challenges that you've faced in both sectors?

Although those sectors (medical and mil/aero) were exempted from the lead-free regulations, the lack of leaded components has driven manufacturers to higher temperature assembly, thus affecting the long-term reliability of the boards. The customers understood the change, and started looking for ways of measuring it. This change carries with it several others, like the types of raw materials to be used, the copper quality, etc.

But, the biggest technological challenge for both sectors has been the immense growth in the number of sequential laminations in their boards. The complexity of the boards has grown exponentially over the past few years, having a mixture of several types of blind and

buried vias, in both rigid and flex-rigid boards. The need for controlled impedances in the boards has grown as well, requiring better control of the production processes, thicknesses of dielectrics and width of the conductors. All of these, together with the constant reduction in via pad diameter and line/space widths became the main driving factor of the defense and the medical equipment market.

At present, both industries have increasingly demanding applications where PCB failure is absolutely unacceptable and the potential cost consequences of failure are enormous. Now more than ever, board reliabilities have been one of the key focus of the industry. From your experience, what are some of these reliability risks, and what factors influence the reliability of your products targeted at the said markets?

Failure of these systems would be too costly in lives and money. Many of the major OEMs understand the risk and they manage it. I would say one of the major risks is related to the purchasing process more than with the production process. Although, assuring reliability costs more, many of the jobs are transferred to subcontractors who are not always aware of the mission-profile and all the problems that can arise with the boards. The OEMs should make sure the subcontractors will not compromise the quality and reliability of the boards at any stage.

Another major risk factor relies on the design process. The design of the product is critical to the long-term reliability. Choosing the right stack-up and the right design rules for specific boards can impart more robustness and durability than any manufacturing process can.

The manufacturing factors influencing reliability start with choosing the right base materials, the right coppers, managing registration and materials flow, and the monitoring of the production process itself. But, the most important factor within the board shops is the stability of the manufacturing process and the reproducibility they can get from batch to batch. The industries should account for getting the same results from batch to batch, and that is not simple nowadays. The raw materials change; sometimes without notice. Raw material fabricators are using different suppliers, and therefore deliver different qualities. Monitoring and controlling the production process is not only done in the chemistry lab and the temperature and pressure of the press, but also making sure the raw materials you use are tested and have not changed; training your work force to deliver the same results; and developing new production techniques to allow less human error.

How do you measure and quantify PCB reliability?

Many years ago, when boards were built of only a few layers and a couple of hundreds of vias, we used to cross-section the coupons, thermal stress them and that was all. The reliability was not actually measured and quantified, but was only qualitatively tested. Nowadays, boards include several lamination cycles, different types of vias—sometimes stacked microvias—thousands of holes and narrow lines; qualitative tests are not enough anymore. In addition to that, the lead-free assembly temperatures, the new materials and processes, the profile of use of the circuit, and other factors also affect the reliability of the boards.

In order to measure and quantify, we decided to make use of newly developed quantitative techniques like IST (interconnect stress test developed by PWB Interconnect) and HATS (highly accelerated thermal shock developed by IRTS, Inc.). Those techniques—with their respective differences—allow us to develop new manufacturing processes, test existing ones, compare between different kinds and sources of raw materials, and choose the right ones for the different applications. The tests are done on hundreds of vias, thus being more representative of the quality of the boards. Manufacturers using those tests will be able to maintain more stable processes and reproducible results. Eltek has adopted both techniques to test all new processes and materials and to maintain the quality of our production.

The possibility we have today of quantifying reliability and of comparing results allow us

to better understand the mechanisms of failure and to focus on the processes or materials responsible for these issues. Any issues or problems are seriously addressed to understand the failure, the reason and mechanism, and to see how it affects the different designs. Any corrective action taken is measured and tested to see its effect on other parameters or processes used for the board. The performance of the boards is tested under harsher conditions than the real ones. The boards are submitted to six reflow simulations and tested at higher temperatures with very high transitions to accelerate the possible failures. Close collaboration with the designers at early stages of the projects minimizes the number of problems. The key word should be prevention.

Finally, from your observation, what key technology developments have happened in the PCB manufacturing industry this year, and what issues have driven these trends?

The PCB technologies are driven by the components developers and the needs of the market. We see new less-expensive direct imaging systems based on LED technology emerging. These machines avoid the use of artworks and allow better accuracy in the photolithographic process. A lot of effort is being placed in the direct imaging of solder mask, which is becoming more and more problematic in the fine-pitch world. We also see the development and introduction of new final finishes-palladium, gold, and Teflon based finishes have been released lately. New base materials are being introduced all the time by almost all the major manufacturers, in order to serve the higher frequency boards and the thermal reliability requests. However, it is important to mention that any new technique or material introduced in the process of manufacturing high-reliability boards should be thoroughly tested and approved beforehand. Failing to do so can compromise reliability. **PCB**

VIDEO INTERVIEW

Multek Around the World

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Heavy and Extreme Copper for Maximum Reliability in PCB Design and Fabrication

Compiled by
Epec Engineered Technologies

SUMMARY: Understanding the heavy copper circuit's basic construction allows full appreciation of its capabilities and potential applications.

Various power electronics products are being designed every day for a range of applications. Increasingly, these projects are taking advantage of a growing trend in the printed circuit board industry: heavy copper and extreme copper PCBs.

What defines a heavy copper circuit? Most commercially available PCBs are manufactured for low-voltage/low-power applications, with copper traces/planes made up of copper weights ranging from ½-oz/ft² to 3-oz/ft². A heavy copper circuit is manufactured with copper weights anywhere between 4-oz/ft² to 20-oz/ft². Copper weights above 20-oz/ft² and up to 200-oz/ft² are also possible and are referred to as extreme copper. For the purposes of this discussion, we will focus primarily on heavy copper. The increased copper weight combined with a suitable substrate and thicker plating in the through-holes transforms the once unreliable, weak circuit board into a durable and reliable wiring platform.

The construction of a heavy copper circuit endows a board with benefits such as:

- Increased endurance to thermal strains
- Increased current carrying capacity
- Increased mechanical strength at connector sites and in PTH holes
- Exotic materials used to their full potential (i.e., high temperature) without circuit failure
- Reduced product size by incorporating multiple copper weights on the same layer of circuitry (Figure 1)
- Heavy copper plated vias carry higher current through the board and help to transfer heat to an external heatsink
- On-board heatsinks directly plated onto the board surface using up to 120-oz copper planes
- On-board high-power-density planar transformers

Figure 1: Sample featuring 2-oz, 10-oz, 20-oz, and 30-oz copper features on the same layer.

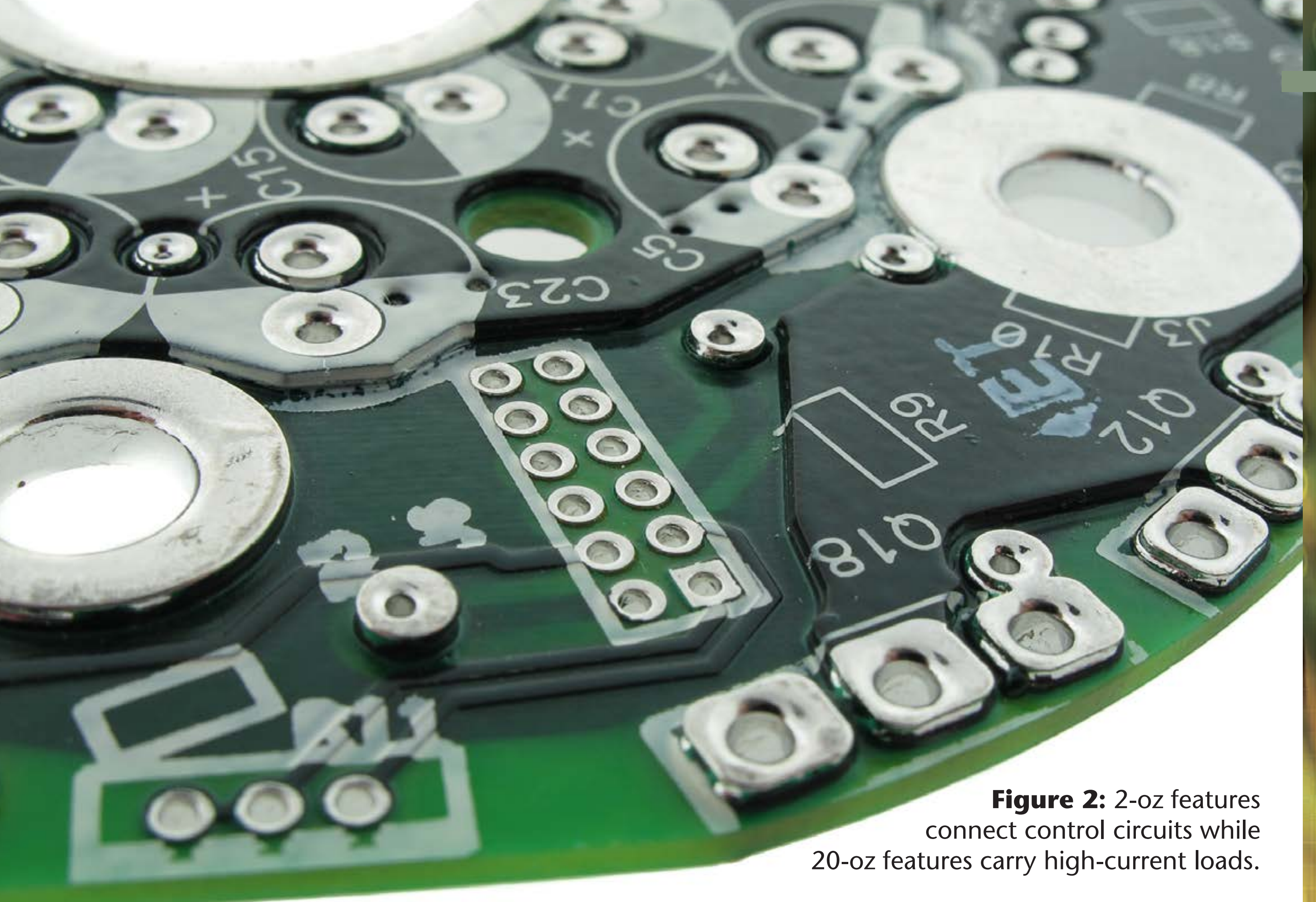


Figure 2: 2-oz features connect control circuits while 20-oz features carry high-current loads.

Although the disadvantages are few, it's important to understand the heavy copper circuit's basic construction to fully appreciate its capabilities and potential applications.

Heavy Copper Circuit Construction

Standard PCBs, whether double-sided or multilayer, are manufactured using a combination of copper etching and plating processes. Circuit layers start as thin sheets of copper foil (generally 0.5-oz/ft^2 to 2-oz/ft^2) that are etched to remove unwanted copper, and plated to add copper thickness to planes, traces, pads and plated through-holes. All of the circuit layers are laminated into a complete package using an epoxy-based substrate, such as FR-4 or polyimide.

Boards incorporating heavy copper circuits are produced in exactly the same way, albeit with specialized etching and plating techniques, such as high-speed/step plating and differential etching. Historically, heavy copper features were formed entirely by etching thick copper-clad laminated board material, causing uneven trace sidewalls and unacceptable undercutting. Advances in plating technology have allowed heavy copper features to be formed with a combination of plating and etching, resulting in straight sidewalls and negligible undercut.

Plating of a heavy copper circuit enables the board fabricator to increase the amount of copper thickness in plated holes and via sidewalls. It's now possible to mix heavy copper with standard features on a single board. Advantages include reduced layer count, low impedance power distribution, smaller footprints and potential cost savings. Normally, high-current/high-power circuits and their control circuits were produced separately on separate boards. Heavy copper plating makes it possible to integrate high-current circuits and control circuits to realize a highly dense, yet simple board structure.

The heavy copper features can be seamlessly connected to standard circuits. Heavy copper and standard features can be placed with minimal restriction provided the designer and fabricator discuss manufacturing tolerances and abilities prior to final design (Figure 2).

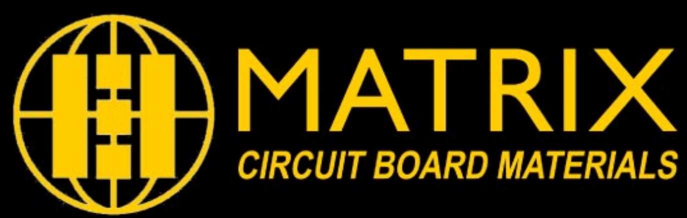
Current Carrying Capacity and Temperature Rise

How much current can a copper circuit safely carry? This is a question often voiced by designers who wish to incorporate heavy copper circuits into their project. This question is usually answered with another question: How much heat rise can your project withstand? This question is posed because heat rise and current flow go hand in hand. Let's try to answer both of these questions together.

When current flows along a trace, there is an I^2R (power loss) that results in localized heating. The trace cools by conduction (into neighboring materials) and convection (into the environment). Therefore, to find the maximum current a trace can safely carry, we must find a way to estimate the heat rise associated with the applied current. An ideal situation would be to reach a stable operating temperature where the rate of heating equals the rate of cooling. Fortunately, we have an IPC formula we can use to model this event.

		Track Width (inch)								
Cu weight (oz/ft2)	Thickness (inch)	0.0625	0.1250	0.2500	0.5000	1.0000	2.0000	4.0000	8.0000	16.0000
1	0.0014	4.6	7.6	12.5	20.7	34.2	56.6	93.6	154.7	255.6
2	0.0028	7.6	12.5	20.7	34.2	56.6	93.6	154.7	255.6	422.5
4	0.0056	12.5	20.7	34.2	56.6	93.6	154.7	255.6	422.5	698.4
6	0.0084	16.8	27.8	46.0	76.0	125.5	207.5	343.0	566.9	937.1
8	0.0112	20.7	34.2	56.6	93.6	154.7	255.6	422.5	698.4	1154.4
10	0.0140	24.4	40.3	66.5	110.0	181.8	300.5	496.7	821.1	1357.1
12	0.0168	27.8	46.0	76.0	125.5	207.5	343.0	566.9	937.1	1548.9
14	0.0196	31.1	51.4	84.9	140.4	232.0	383.6	634.0	1047.9	1732.1
16	0.0224	34.2	56.6	93.6	154.7	255.6	422.5	698.4	1154.4	1908.1
18	0.0252	37.3	61.7	101.9	168.4	278.4	460.2	760.7	1257.3	2078.2
20	0.0280	40.3	66.5	110.0	181.8	300.5	496.7	821.1	1357.1	2243.2
24	0.0336	46.0	76.0	125.5	207.5	343.0	566.9	937.1	1548.9	2560.2
28	0.0392	51.4	84.9	140.4	232.0	383.6	634.0	1047.9	1732.1	2863.0
32	0.0448	56.6	93.6	154.7	255.6	422.5	698.4	1154.4	1908.1	3154.0
36	0.0504	61.7	101.9	168.4	278.4	460.2	760.7	1257.3	2078.2	3435.1
40	0.0560	66.5	110.0	181.8	300.5	496.7	821.1	1357.1	2243.2	3707.8
45	0.0630	72.5	119.8	198.0	327.3	541.0	894.3	1478.1	2443.2	4038.3
50	0.0700	78.2	129.3	213.7	353.3	584.0	965.2	1595.5	2637.1	4358.9
55	0.0770	83.8	138.6	229.0	378.6	625.7	1034.3	1709.6	2825.8	4670.8
60	0.0840		147.6	244.0	403.2	666.5	1101.7	1820.9	3009.8	4974.9
70	0.0980		165.0	272.8	450.9	745.3	1231.9	2036.2	3365.7	5563.1
80	0.1120		181.8	300.5	496.7	821.1	1357.1	2243.2	3707.8	6128.6
90	0.1260		198.0	327.3	541.0	894.3	1478.1	2443.2	4038.3	6675.0
100	0.1400		213.7	353.3	584.0	965.2	1595.5	2637.1	4358.9	7204.8
120	0.1680			403.2	666.5	1101.7	1820.9	3009.8	4974.9	8223.0
140	0.1960			450.9	745.3	1231.9	2036.2	3365.7	5563.1	9195.3
160	0.2240			496.7	821.1	1357.1	2243.2	3707.8	6128.6	10130.0
180	0.2520			541.0	894.3	1478.1	2443.2	4038.3	6675.0	11033.1
200	0.2800			584.0	965.2	1595.5	2637.1	4358.9	7204.8	11908.9

Figure 3: Approximate current for given track dimensions (20˚C temp rise).



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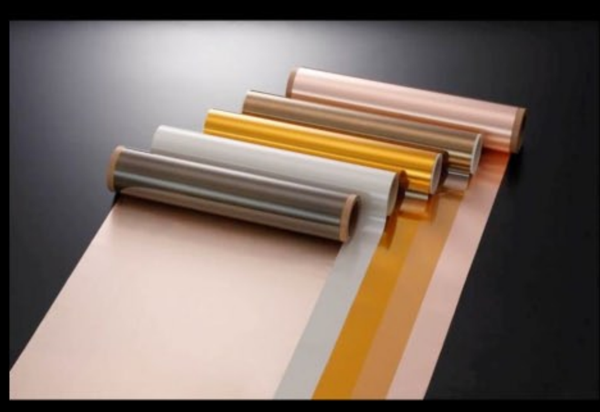

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TYPE	FCCL	12.5μm 1/2 mil	14μm	18μm	20μm 4/5 mil	25μm 1 mil	50μm 2 mil	75μm 3 mil	100μm 4 mil
Standard	R-F775/770	-	-	-	✓	✓	✓	✓	✓
Low Elasticity	R-F785/780	✓	✓	✓	-	✓	-	-	-
High Heat Resistance	R-F786/781	✓	-	✓	-	✓	✓	-	-

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		Adhesive	Polyimide	Adhesive
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	MCL 210	50μm	25μm	-
BOND PLY	MBP 111	25μm	25μm	25μm
	MBP 212	50μm	25μm	50μm

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IPC-2221A: calculation for current capacity of an external track[1]:

$$I = .048 * DT^{(.44)} * (W * Th)^{(.725)}$$

Where I is current (amps), DT is temperature rise (°C), W is width of the trace (mil) and Th is thickness of the trace (mil). Internal traces should be derated by 50% (estimate) for the same degree of heating. Using the IPC formula we generated Figure 3, showing the current-carrying capacity of several traces of differing cross-sectional areas with a 30°C temperature rise.

What constitutes an acceptable amount of heat rise will differ from project to project. Most circuit board dielectric materials can withstand temperatures of 100°C above ambient, although this amount of temperature change would be unacceptable in most situations.

Circuit Board Strength and Survivability

Circuit board manufacturers and designers can choose from a variety of dielectric materials, from standard FR-4 (operating temp. 130°C) to high-temperature polyimide (operating temp. 250°C). A high-temperature or extreme environment situation may call for an exotic material, but if the circuit traces and plated vias are standard 1-oz/ft^2, will they survive the extreme conditions? The circuit board industry has developed a test method for determining the thermal integrity of a finished circuit product. Thermal strains come from various board fabrication, assembly and repair processes, where the differences between the coefficient of thermal expansion (CTE) of Cu and the PWB laminate provide the driving force for crack nucleation and growth to failure of the circuit. Thermal cycle testing (TCT) checks for an increase in resistance of a circuit as it undergoes air-to-air thermal cycling from 25°C to 260°C.

An increase in resistance indicates a breakdown in electrical integrity via cracks in the copper circuit. A standard coupon design for this test utilizes a chain of 32 plated through-holes, which has long been considered to be the weakest point in a circuit when subjected to thermal stress.

An increase in resistance indicates a breakdown in electrical integrity via cracks in the copper circuit.

Thermal cycle studies done on standard FR-4 boards with 0.8-mil to 1.2-mil copper plating have shown that 32% of circuits fail after eight cycles (a 20% increase in resistance is considered a failure). Thermal cycle studies done on exotic materials show significant improvements to this failure rate (3% after eight cycles for cyanate ester), but are prohibitively expensive (five to 10 times material cost) and difficult to process. An average surface-mount technology assembly sees a minimum of four thermal cycles before shipment, and could see an additional two thermal cycles for each component repair.

It's not unreasonable for a SMOBC board that has gone through a repair and replacement cycle to reach a total of nine or 10 thermal cycles. The TCT results clearly show that the failure rate, no matter what the board material, can become unacceptable. Printed circuit board manufacturers know that copper electroplating isn't an exact science—changes in current densities across a board and through numerous hole/via sizes result in copper thickness variations of up to 25% or more. Most areas of "thin copper" are on plated-hole walls—the TCT results clearly show this to be the case.

Using heavy copper circuits would reduce or eliminate these failures altogether. Plating of 2-oz/ft^2 of copper to a hole wall reduces the failure rate to almost zero (TCT results show a 0.57% failure rate after eight cycles for standard FR-4 with a minimum of 2.5-mil copper plating). In effect, the copper circuit becomes impervious to the mechanical stresses placed on it by the thermal cycling.

Thermal Management

As designers strive to obtain maximum value and performance from their projects, printed circuits are becoming more complex

and are driven to higher power densities. Miniaturization, use of power components, extreme environmental conditions and high-current requirements increase the importance of thermal management. The higher losses in the form of heat, that's often generated in the operation of electronics, has to be dissipated from its source and radiated to the environment; otherwise, the components could overheat and failures may result. However, heavy copper circuits can help by reducing the I^2R losses and by conducting heat away from valuable components, reducing failure rates dramatically.

In order to achieve proper heat dissipation from heat sources in and on the surface of a circuit board, heatsinks are employed. The purpose of any heatsink is to dissipate heat away from the source of generation by conduction and emit this heat by convection to the environment. The heat source on one side of the board (or internal heat sources) is connected by copper vias (sometimes called "heat vias") to a large bare copper area on the other side of the board.

Generally, classical heatsinks are bonded to this bare copper surface by means of a thermally conductive adhesive or in some cases, are riveted or bolted. Most heatsinks are made of either copper or aluminum. The assembly process required for classical heatsinks consists of three labor-intensive and costly steps.

To begin, the metal serving as the heatsink must be punched or cut to the required shape. The adhesive layer must also be cut or stamped for a precision fit between the circuit board and the heatsink. Last but not least, the heatsink must be properly positioned on the PCB and the entire package has to be coated for electrical and/or corrosion resistance with a suitable lacquer or cover coat.

Normally, the above process can't be automated and must be done by hand. The time and work required to complete this process is significant, and the results are inferior to a mechanically automated process. In contrast, built-in heatsinks are created during the PCB manufacturing process and require no additional assembly. Heavy copper circuit technology makes this possible. This technology allows the addition of thick copper heatsinks virtually anywhere on the outer surfaces of a board. The heatsinks are electroplated on the surface and thus connected to the heat conducting vias without any interfaces that impede thermal conductivity.

Another benefit is the added copper plating in the heat vias, which reduces the thermal resistance of the board design, realizing that they can expect the same degree of accuracy and repeatability inherent in PCB manufacturing. Because planar windings are actually flat conductive traces formed on copper clad laminate, they improve the overall current density compared to cylindrical wire conductors. This benefit is due to minimization of skin effect and higher current-carrying efficiency.

On-board planars achieve excellent primary-to-secondary and secondary-to-secondary dielectric isolation because the same dielectric material is used between all layers, ensuring complete encapsulation of all windings. In addition, primary windings can be spilt so that the secondary windings are sandwiched between the primaries, achieving low leakage inductance. Standard PCB lamination techniques, using a choice of a variety of epoxy resins, can safely sandwich up to 50 layers of copper windings as thick as 10-oz/ft^2.

During the manufacture of heavy copper circuits, we are usually dealing with significant plating thicknesses; therefore, allowances must be made in defining trace separations and pad sizes. For this reason, designers are advised to have the board fabricator on board early in the design process.

Power electronics products using heavy copper circuitry have been in use for many years in the military and aerospace industry and are gaining momentum as a technology of choice in industrial applications. It's believed that market requirements will extend the application of this type of product in the near future. **PCB**

References

1. IPC -2221A

Epec Engineered Technologies provides customized, built-to-print PCBs for all sectors of the electronics industry.

High-Reliability PCBs in Mil/Aero Applications

By Zulki Khan
NEXLOGIC TECHNOLOGIES, INC.

SUMMARY: Experienced EMS providers and contract manufacturers apply special steps and techniques at layout, fab, and assembly to build-in product reliability, and these steps and techniques must be implemented at various design and manufacturing stages to ensure high quality and reliability in mil/aero applications.

PCB design, fabrication, and assembly for mil/aero, medical, and other high-reliability applications demand considerably more than the routine processes and procedures being used for commercial applications. That's because these special breeds of PCBs require the highest available quality, reliability, and consistency to comply with stringent and rugged environmental requirements.

Experienced EMS providers and contract manufacturers (CMs) know to apply special steps and techniques at layout, fab, and assembly to build in product reliability, and these steps and techniques must be implemented at various design and manufacturing stages to ensure high quality and reliability.

At Layout

During PCB design layout, a number of different techniques can be implemented—too many to describe here. However, the following are some of the more salient ones. Foremost is the use of mil-spec components with tolerances of 1 - 2% versus commercial ones, which have 10% tolerances. While they are more expensive, they are considerably more reliable with gold finish terminations rather than tin lead finishes on the leads.

Also worth noting is this next technique, which may sound amateurish and unnecessary to some industry observers. But having an extra set of eyes review the accuracy of the parts library after it has been created is a great idea. The importance of applying two or more sets of eyes (e.g., a designer's and a checker's) on the parts library, footprints, and pad stacks helps to prevent mistakes. One designer can make the pad stacks, for instance, and another can perform verification to ensure accuracy. If pad stacks are not made correctly, internal shorts on power and ground planes may result.

Here, it's important to pay close attention to tolerances, as multiple suppliers may manufacture the same component. Those different manufacturers may have varying mechanical, electrical, footprint and temperature tolerances, some of which can adversely affect a placement of the component if they are not taken into consideration during the design layout phase.

This is especially true for BGA, CSP, QFN, and flip-chip packages because room for error is considerably smaller and limited. These components cannot be seen via the naked eye; X-rays or other devices must be used to clearly view those components. But if the wrong footprint or pad stack is created, there is no recourse but to perform costly rework, which in some extreme cases may not even be possible.

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Brady L. Boyd, C.P.M.
Materials Supervisor
SelfCharge Inc.

I received the 150+ boards yesterday afternoon. Thank you once again for your excellent service and quality. Be sure to thank the people in your factory for me as well. When I order from you, I know I don't have to worry about getting bad boards and going through the purchase cycle again. Let alone the embarrassment of explaining it all to my boss and his boss.

Warmest regards,

Richard Diehl
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Pay special attention to detail when creating fabrication and assembly notes. An EMS provider should be required to comprehensively detail IPC or mil-spec standards along with their respective classes, (e.g., adding a note specifying that the PCB must comply with MIL-PRF-31032). There should not be any question or ambiguity, and notes should clearly state the required standard and its class. Also, as shown in Figure 1, datum points and definitions must be properly noted in fabrication and assembly drawings to avoid confusion. A datum point is the center from which all dimensions are calculated; it is important for it to be precise and clear.

Blind or buried vias should be avoided wherever possible in aerospace PCB applications, because they limit the number of manufacturers that can fabricate these bare boards with utmost accuracy. On the other hand, through-hole vias with a lot of plating wall are considerably more reliable than the smaller blind or buried via.

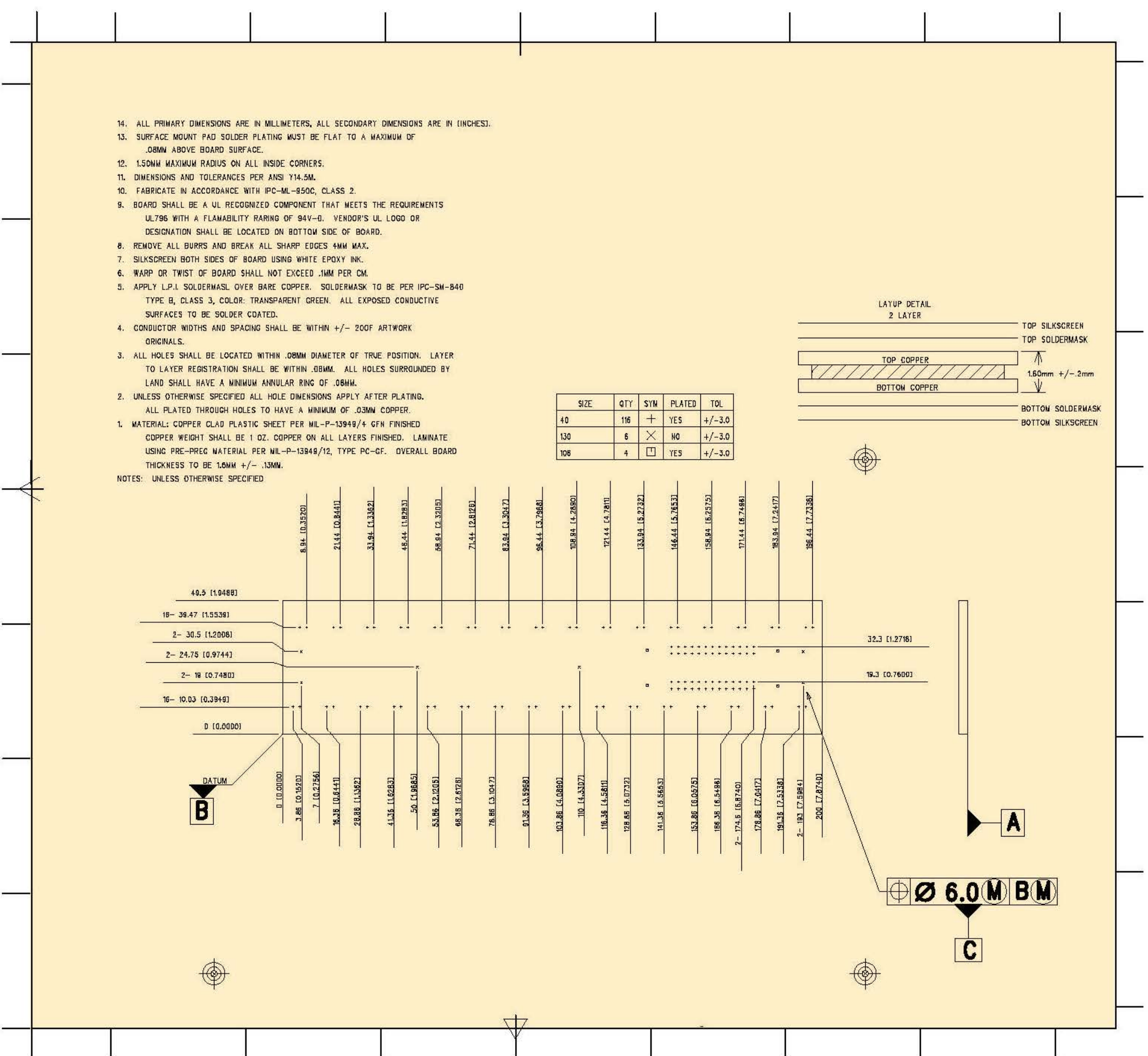


Figure 1: Datum points must be properly noted in fabrication and assembly drawings.

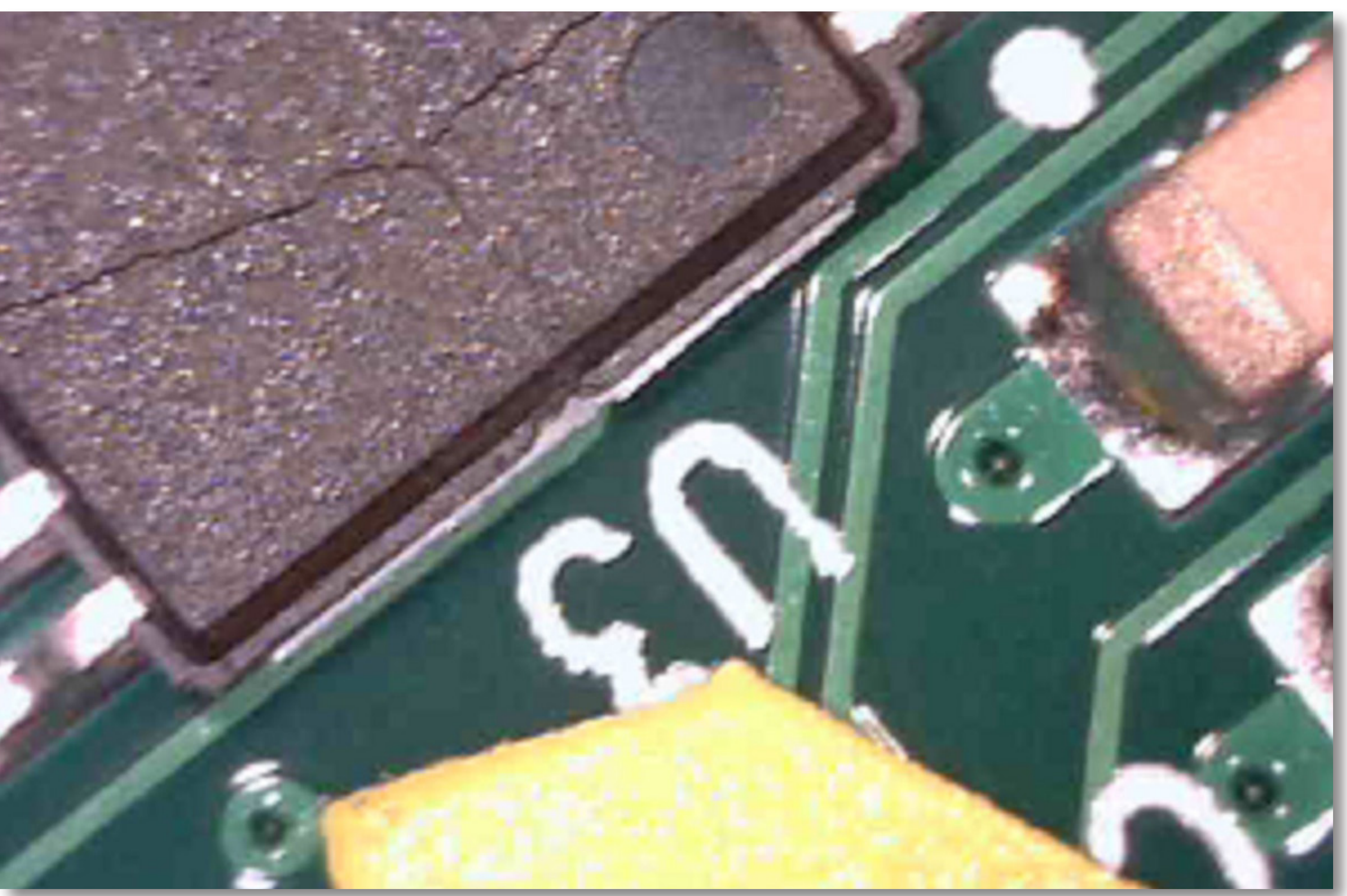


Figure 2: Fractured component due to overheating.

In some cases, it's well worth going the extra mile during layout. For example, the electrical engineer's function is to create the schematic and select the right components. However, at layout, the PCB designer can spend a little extra time verifying that a particular component does in fact comply with its associated temperature, electrical and power ratings. This added step makes sure the component operates correctly and effectively in extreme temperature conditions in rugged aerospace applications.

Safe and continuous operating temperatures must be maintained for components and PCB material, alike. This means keeping a sharp eye on coefficient of thermal expansion while the layout is being performed. In this regard, the aerospace PCB designer must constantly be aware of thermal matching. When through-hole, glass-based components are used together with surface mount, ceramic-based components, there will be different coefficients of thermal expansions. The differences or mismatches in thermal expansion can create a fractured joint in extreme thermal conditions. Care should be taken to review and verify these mismatches and efforts made to reduce them, when and if it happens. Failing to do so can result in fracturing components.

Also, a major requirement for maintaining a coefficient of thermal expansion is to ensure thermal relief is properly designed in. The goal is to greatly reduce thermal stresses to improve component and product reliability. One heat dissipation technique is to have a gap between the PCB and component. That can be implemented by using a clamp or thermal mounting plate, which increases conductivity area for dissipating the heat.

At times, depending on the aerospace application, an experienced EMS provider can provide indirect cooling such as air or liquid-based cooling. Also, for the more traditional PCB design, applying heat sinks on external planes is vital to dissipate heat generated by circuitry to

Figure 3: Assembly notes must include instructions to clean residue from under vertical heat sinks and associated devices.

Figure 4: Thermal grease is used to dissipate heat.

ambient atmosphere. Special heat sink fixtures play a part in thermal relief, as well. At times, they are connected to the metal frames. Another associated design consideration deals with heat sink mounting and specific board areas from where heat is to be dissipated. This step involves hardware and ensuring heat sink soldering at proper locations.

In some cases, residues of processing agents or solutions can remain under a heat sink and components such as BGAs or CSPs. Therefore, it is important to include special instructions in assembly notes to make sure cleaning is performed under devices such as vertical heat sinks (Figure 3). Sometimes it's a good idea to dissipate the heat using a thermal transfer medium such as thermal grease or boron nitride (Figure 4). These solutions can be used to make the heat flow from one segment of the circuitry generating more heat towards the cooler part of the circuitry and eventually into the atmosphere.

At Fabrication

Well documented fabrication notes are essential for detailing all the specifications and ensuring that a PCB is correctly fabricated to comply with aerospace specifications. This includes PCB surface finish considerations. Normally, HASL or gold are recommended for long-term reliability and not necessarily silver or OSP. Silver is to be avoided due to short shelf-life and the possibility of corrosion.

Avoiding warpage is an important factor in some aerospace applications. When temperatures are extreme, and copper distribution is not balanced on the board's surface, the board can warp. So the limit for warpage can be made even tighter, say by 20%, especially for boards less than 62 mils thick. If the board warps, the integrity of components' connection solderability is at risk. Poorly soldered joints cause mechanical stress, and eventually, the joint cracks, compromising the joint assembly.

At Assembly

Aerospace applications demand consideration of multiple factors at the assembly stage. Up front, the PCB application has to be clearly defined either as a J Standard or IPC Class III. There may be slight differences, and depending on the application within aerospace circles, some applications would suffice as Class III versus others as J Standard. So it is important to define the PCB based on the application.

At times, in aerospace applications, non-standard parts and components are used. Availability can be an issue. But an even more important issue is the testability of that part after assembly has been performed. If non-standard parts are used, it is important there exists some historical data available for testing that part and assuring it will have longevity. Gathering that historical data can be challenging at times.

Always check to see if the assembly drawing requires components to be fastened or tied down.

Figure 5: Inspection of complex BGA, QFN, and flip chip packaging demands the use of sophisticated X-ray machines.

At this point, assurances are made for properly defining a complete bill of materials, including hardware fastening material, thermal grease, epoxies, spacers, and other ancillary items that are part of the complete product build. It's important to review these details at the beginning of the assembly stage in order to ensure acceptable and repeatable assembly on a consistent basis.

Tall components, fixtures, complex packages, and conformal coatings are special factors, and they require extra attention. Tall components will likely require tie-downs so that they remain sturdy and withstand mechanical stresses. Moreover, they will need special handling during flying probe or ICT testing, since tester probe movement could be restricted due to component placements. The use of fixtures is a good idea for aerospace applications because they support consistency, speed, and reliability. Fixtures to be considered should be used for wave solder, pick and place, and AOI.

Proper and reliable inspection of such complex packages as BGA, QFN, and flip-chip commands the use of advanced X-ray machines with acceptable tolerance limits defined (Figure 5). For example, when a void is detected, what kinds of void calculations are specified? What are the acceptable limits? When BGAs are inspected, void calculations must be tightened to acceptable limits for the aerospace applications.

Conformal coatings, also known as potting, are used for protecting the boards from agents such as moisture, dust, chemicals, and extreme temperatures. There are different kinds of conformal coating techniques, including brush, spray, and dipping. These techniques are based on cure time, substrate type, and type of drying agents to be used. The type of coating to be used depends on the particular aerospace application. And, there are acceptable criteria for conformal coating from different agencies like IPC, UL, and ASTM. These agencies provide the definitions and criteria for usage, which depends on the type of material used for conformal coating, shelf life, viscosity, appearance, flammability requirements, moisture, and insulation resistance.

Testing

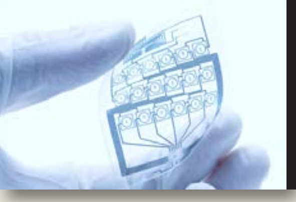
Here, the focus is on implementing design-for-test (DFT) techniques, which originates with layout of the PCB for an aerospace application. At this stage, different nets are being probed with test coverage being as close to 100% as possible. Temperature cycling for an aerospace PCB is considerably different than that for a commercial one, which goes through a normal temperature cycle.

However, for aerospace PCBs, extreme temperature cycling is essential. Thus, procedures for temperature cycling must be defined. The same is true for power cycling; an aerospace PCB has to be exposed to different power levels for optimal performance under extreme conditions.

As for aging testing, different test labs can age boards by running them through various kinds of stress testing, such as mechanical vibration, and temperature power cycling. It is a good idea to expose an aerospace PCB to ensure all critical steps and techniques have been implemented to attain high-quality and reliability goals prior to production. **PCB**

Zulki Khan is president and founder of NexLogic Technologies, Inc., in San Jose, California. He may be reached at zulki@nexlogic.com.

Most-Read Flex007 News Highlights This Month



Flexible, Low-Voltage Circuits Using Nanocrystals

Electronic circuits are typically integrated in rigid silicon wafers, but flexibility opens up a wide range of applications. In a world where electronics are becoming more pervasive, flexibility is a highly desirable trait, but finding materials with the right mix of performance and manufacturing cost remains a challenge.

Eltek Suffers 10% On-Year Revenue Drop in Q3

Revenues for the quarter ended September 30, 2012 were $10.8 million compared with revenues of $12.0 million recorded in the third quarter of 2011. Gross profit for the third quarter of 2012 was $1.7 million (16.1% of revenues) compared with gross profit of $2.4 million (20.0% of revenues) in the third quarter of 2011.

All Flex Sales Growth Prompts Additional Facility

All Flex, manufacturer of flexible circuits and heaters, has obtained an additional facility to support continued increase in sales in 2012 and an optimistic forecast that requires more manufacturing space. Indirect office staff is transitioning to another facility that will allow for a 10% increase in manufacturing space in the current building which serves as company headquarters in Northfield, Minnesota.

A Flexible and Transparent Supercapacitor

In a recently published article, colleagues from Northeastern and Rice University presented their design of a flexible and transparent supercapacitor, a device that stores energy as an electrical field instead of a chemical reaction, as batteries do. As such, it is a prime energy storage candidate for the thin, flexible devices of the future.

Flexium's Revenue Hits Record High in November

Flexible PCB maker Flexium Interconnect saw its revenues hit a new high for the third consecutive month at NT $1.44 billion (USD $49.52 million) in November. The monthly figures represented an increase of 21.9% sequentially and 75.2% on year.

Smartphones Drive Rigid-Flex PCB Demand in 2013

PCB makers Unimicron Technology, Unitech Printed Circuit Board, and Compeq Manufacturing all expect demand for rigid-flex PCBs, particularly from the smartphone sector, will gain further momentum in 2013.

IBIDEN Strengthens Foundation, Celebrates 100 Years

Hiroki Takenaka, president and CEO of IBIDEN, held a commemorative party at Ogaki Forum Hotel to celebrate the company's 100th anniversary. The event was attended by Gifu Prefecture Governor, Hajime Yoshida, with whom the company has enjoyed a long-standing relationship.

IPC: N.A. October Flex Shipments Rose, Bookings Fell YOY

Flexible circuit shipments in October 2012 were up 15.6%, and bookings were down 18.9% compared to October 2011. Year to date, flexible circuit shipments decreased 4% and bookings decreased 10.5%. Compared to the previous month, flexible circuit shipments decreased 10.3% and flex bookings were down 0.5%.The North American flexible circuit book-to-bill ratio remained low at 0.74.

MFLEX Plans to Repurchase Common Stock

Norman Ip, chairman of WBL Corporation Limited, said, "Once declared effective by the SEC, the shelf registration will provide WBL an avenue to monetize our holdings, whether in whole or in part, of MFLEX common stock, as we execute our strategic options for our technology businesses to enhance shareholder value."

Innovative Circuits Upgrades Soldermask Operations

Flex maker Innovative Circuits recently completed an upgrade of its soldermask operations with the acquisition of four pieces of new equipment. "The new ovens will provide top-level curing and drying through the use of cross-flow air ventilation systems," said Mitch Sprinkle, operations manager for ICI.

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	Low coefficient of thermal expansion	High reliability in complex multilayer designs
RT/duroid® 5880LZ	Dielectric constant of 1.96	Lowest dielectric constant microwave PCB material
	Low z-axis coefficient of thermal expansion	Plated through hole capable
	Light weight	Advantage for airborne applications
RT/duroid® 6035HTC	Highest thermal conductivity (1.44 W/mk) for 3.5Dk printed circuit board laminates	Excellent power handling capability
	Low loss 0.0013	Excellent high frequency performance
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Global Competitiveness

by Steve Williams

SUMMARY: Once upon a time, most PCB companies were merely concerned with being competitive with the neighbor down the street, or perhaps within a limited regional footprint. Today's global economy brings a new set of pricing pressures to an already complicated pricing model.

Pricing Model

In the not-too-distant past, discussions on pricing were a much simpler matter that could be reduced to square-inch terms without much consequence. A quick calculation could be estimated with only the knowledge of the number of holes, layers and form-factor size. Fast forward to today, where one would be hard-pressed to develop a workable square-inch pricing matrix for the complexity of current PCB technology. The sheer multitude of laminate configurations provide virtually unlimited permutations of T_g, Dk, GHz with epoxy, PTFE, and ceramic substrates that would make any standard pricing model impossible. Throw in laser microvias, sequential lamination, multiple surface finishes, and hybrid constructions and it becomes clear that any attempt to compare PCB pricing across the board (no pun intended) would be unreliable, at best.

Global Economy

Although the term "global economy" has been overused and much maligned, the PCB industry has seen this truly become a reality in this millennium. Even the most diehard pro-American domestic PCB manufacturers have realized that the best cost countries (BCCs) are not going away, and that they are producing high-quality PCBs delivered within domestic lead-times, at significantly lower prices. The

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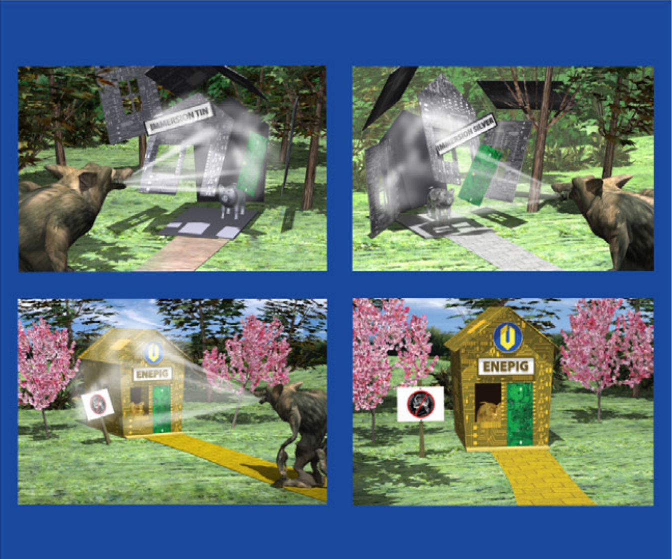

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current U.S. recession that continues to cripple our board industry has accelerated the move of business out of the U.S. As U.S. printed circuit board manufacturers have shuttered billions of dollars of capacity, PCB expansions in emerging BCCs are occurring at a rapid pace.

As OEMs and contract manufacturers continue to try to drive costs out of their products, they are looking outside the U.S. for cost reductions at an unprecedented pace. Reservations about sending advanced technology to BCCs are quickly disintegrating as PCB manufacturers continue to expand technology and capabilities. Asia, in particular, has changed the rules drastically by significantly reducing minimum order quantities (MOQ) and supporting the high-mix, low-volume (HMLV) manufacturing model many U.S. customers must use to remain flexible and competitive. In addition to Asia, European manufacturers have always had the technology, and they are now becoming extremely cost-competitive in the Eastern region. This has led to the rapidly accelerating trend of U.S. PCB manufacturers forming alliances with BCC partners. This not only provides their customers with a low-cost alternative, but also provides a means for them to stay in the game. Most of the medium-to-large (>$300 million) PCB manufacturers either have such alliances or own facilities in BCCs. This model is not only being quickly adopted by small companies, but also by quick-turn service facilities looking to add a "total-solution" capability to their customer offerings.

World-Class Pricing

This is another buzzword that means different things to different people, often without much substance behind it. My definition of world-class pricing is a globally competitive price, by technology, from a source that is capable of producing the product. While this may sound self-evident, closer examination typically proves that it is not. Pricing is deceptive, especially in today's economic environment as companies are trying to stay alive by attempting to provide technology or services that have never been part of their strategy or core competency.

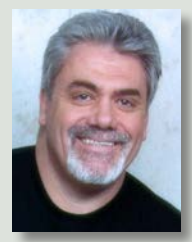
Any company can undercut your current price on any single piece of business, but do you really want them building your product? In most cases, you probably do not. Frequently, companies publish and advertise that they can produce X technology, but when you get into the facility and evaluate their capability and mix, you find out that they may have built this technology once. They have neither the equipment nor the skill set to consider it a core competency.

World-class pricing means that whether the product is a 4-layer or 40-layer board, customers expect to pay a price that is competitive anywhere around the globe. This may mean Oshkosh, Wisconsin, or Guangdong, China, or anywhere in between.

Another customer expectation is that a supplier presents the best available price the first time. When told they have lost a piece of business due to a noncompetitive price, many suppliers still ask, "Why didn't we get a chance to sharpen our pencil?" Gone are the days when we all had time to negotiate every job to arrive at the best available price. In today's constantly compressing time-to-market environment, there simply is not time to haggle over price; customers want your best effort up front. The bottom-line message is that customers have taken a global approach to pricing and business will be won by world-class competitiveness.

Stay in the Game

The best-cost country phenomenon is a constantly evolving dynamic. First, it was Japan, then Taiwan; today it is China, and tomorrow it will be some other developing nation. One thing is certain: The evolution will continue as a new BCC emerges and the cycle continues. To stay in the game, U.S. manufacturers need to reshape, realign, and refocus to remain competitive in the global economy. **PCB**



Steven Williams is the commodity manager for a large global EMS provider and author of the book Survival Is Not Mandatory: 10 Things Every CEO Should Know About Lean.

Airtech Shows Staying Power in China

by Real Time with...HKPCA & IPC 2012

VIDEO INTERVIEW

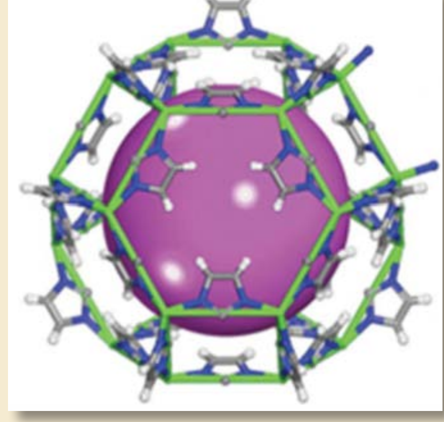
Jim Hegeduis, PCB business development manager for Airtech, has been coming to the HKPCA show for 10 years, and he's watched the show and the region grow and develop. He discusses Airtech's strong commitment to technology and their equally strong commitment to Chinese PCB manufacturing.

realtimewith.com

New Nano Trap Protects Environment

A new type of nanoscale molecular trap makes it possible for industry to store large amounts of hydrogen in small fuel cells or capture, compact and remove volatile radioactive gas from spent nuclear fuel in an affordable, easily commercialized way.

The ability to adjust the size of the trap openings to select for specific molecules or to alter how molecules are released at industrially accessible pressures makes the trap uniquely versatile. The trap is constructed of commercially available material and made possible through collaborative work at Argonne and Sandia national laboratories.



"This introduces a new class of materials to nuclear waste remediation," said Tina Nenoff, a chemist at Sandia National Laboratories. "This design can capture and retain about five times more iodine that current material technologies."

Organic molecules linked together with metal ions in a molecular-scale Tinker Toy-like lattice called a metal-organic-framework, or MOF, form the trap. Molecules of radioactive iodine or carbon dioxide or even hydrogen for use as fuel can enter through windows in the framework.

Once pressure is applied, these windows are distorted, preventing the molecules from leaving. This creates a cage and a way of selecting what to trap based on the molecule's shape and size.

The compression also turns the MOF from a fluffy molecular sponge that takes up a lot of space into a compact pellet. The ability to compress large amounts of gas into small volumes is a crucial step to developing hydrogen gas as an alternative fuel for engines.

ARTICLE

The Problem with UL Approval of Rigid-flex Circuits

by Bob Burns
PRINTED CIRCUITS, INC.

Introduction

In the early 1980s, the first rigid-flex circuit board concepts came into use. We use the word concept, because they were developmental efforts at marrying flex circuit boards and rigid circuit boards to eliminate connectors, improve reliability, or achieve connectivity and density in a small space. They were very similar to flex with stiffeners, except that the stiffeners had circuits as well, and through-holes provided connection between the two formats.

These early attempts were for military and space applications. The military had its own PWB specifications and had a history of electronics built with both rigid boards and flexible boards—so they had a good basis for understanding how to design and specify these hybrid products.

In the 1990s, DuPont introduced its line of adhesiveless flexible laminate called AP, for Adhesiveless Pyralux. Eliminating the adhesive in the flexible laminate provided for greater reliability, by reducing Z-axis CTE forces on vias, caused by the high Z-axis CTE values of acrylic adhesive used to laminate the copper to the Kapton base material. The new materials improved the reliability of flexible circuit designs, but were particularly valuable in the manufacture of higher layer count rigid-flex. Specifications were developed and rigid-flex quickly became an accepted packaging medium whenever designers were looking for higher reliability and/or increased connection density.

The use of rigid-flex in military, avionics and aerospace applications has grown steadily since then, and it is particularly valuable in high-stress, high-vibration, or thermal excursion environments that would disrupt connectivity in traditional rigid boards with flex/connector junctions.

Rigid-flex also found acceptance in high-reliability medical applications in implantable devices, and dynamic flex applications that require never fail reliability. It has also proven invaluable in packaging a lot of functionality in very small spaces, such as digital cameras, video cameras and miniaturized medical electronics.

Rigid-flex has continued to expand into the commercial markets, consumer electronics and industrial applications for many of the same reasons. Although more expensive than traditional packaging methods, it provides unmatched reliability that often provides OEMs and designers with product differentiation and greater reliability, particularly in environmental stress applications.

The Problem

The growth and acceptance of rigid-flex in the commercial sector, has created a unique problem. The difficulty lies in getting a UL rating on rigid-flex constructions due to the overwhelming number of configurations that must be represented in the test vehicles.

Many electronics designers and manufacturers are required to have their products recognized and rated by UL, usually mandated by their insurance carriers. This rating signifies that the product can sustain a certain level of exposure to a flame, without igniting. Products that meet this requirement have much lower chances of starting a fire, and thus reduce chances of product liability claims.

To meet this requirement, PWB fabricators manufacture and submit samples of their boards to UL for a rating approval. The most popular approval rating for manufacturers of PWBs is 94 V-0. Most fabricators have a file with UL that designates what constructions they may put their UL logo on, to designate that a board has met UL's 94 V-0 test requirements.

The sample requirements call out dielectric thicknesses, copper thicknesses, circuitry dimensions, etc., in order to encompass as broad a range as possible, so that the fabricator can apply their UL logo to as many parts as possible for their customers. Compliance is verified by UL auditors that visit fabricators, looking for violations. UL letters of recognition specifically state that any violations can lead to immediate revocation of the fabricator's UL recognition.

For a fabricator to obtain UL recognition, he will typically start with one supplier's materials and build a test sample base from there. A typical test submission might be 10 to 20 test coupons, $10,000 to $14,000, and take 12 to 16 weeks for testing and approval. UL recognition gives the fabricator the ability to put his UL logo on PWBs manufactured with that supplier's material, as long as it falls within the parameters represented in the coupons they originally submitted.

Once approved, the fabricator must use the same materials that were submitted in the original sample. To use another supplier's laminate or prepreg within a PWB, and apply his UL logo, would be a violation. It would also be a violation even if the fabricator had UL recognition on the other supplier's material. The fabricator cannot mix and match (even if both materials were approved by UL separately) two material suppliers without specifically achieving a recognition from UL by submitting mix-and-match samples.

Mix-and-match approvals are obtained whenever a fabricator wants the flexibility to mix-and-match materials within its UL qualification. Those approvals can get large and expensive due to the larger sample sets required. UL needs to verify that regardless of material combinations, thicknesses, or copper constructions that all combinations will pass their flame rating tests. The sample set increases exponentially, as does the cost and the timeline for building, submitting and testing the sample set. Mix and match qualifications are not attempted very often because it is hard to recoup the investment in the original qualification.

> ***"Mix and match qualifications are not attempted very often because it is hard to recoup the investment in the original qualification."***

These same constraints are true for both rigid board fabricators as well as flexible circuit fabricators. However, with rigid-flex things get much more difficult.

Rigid-flex fabricators use materials that are similar to rigid board fabricators, and materials that are similar to flex fabricators. When you combine the two material sets in making a rigid-flex, you create a combined material library that is so large it is hard to adequately cover all of the possible material combinations. It would be somewhat similar to attempting a UL recognition on a mix and match build, but instead of using two suppliers, you would be attempting a mix and match on three suppliers with complete interchangeability. And

that would be to get just one material qualification, such as an FR-4 rigid-flex qualification. If you wished to add polyimide rigid materials, that doubles the material library again.

Rigid-flex manufacturers build their product with rigid laminate, flex laminate, prepreg, flexible coverlayer and bondply—in all the thickness variations and copper configurations. A basic UL qualification now requires well over 100 sample coupons, months of building and submitting for testing, and an exponential increase in cost. The cost alone is difficult to ever recoup, let alone the manufacturing time and expense of building the samples. Thus, fabricators have little incentive to undertake the task.

Previous Options

The difficulty of certifying PWBs to UL 94 V-0 hasn't deterred designers from increasingly incorporating rigid-flex designs into medical and commercial applications. Its viability as a robust packaging medium continues to bring value to electronics designers and users.

The problem arises when the requirement is communicated to the board fabricator. The requirement generally elicits one of three responses.

1 Many rigid-flex fabricators offer to submit their customer's constructions to get UL recognition one material set at a time. The samples submitted represent only one construction—any change in materials, even adding a sheet of prepreg, automatically disqualify the part from UL recognition and the new build must be resubmitted. The problem with this approach is that it is still expensive in its own right, is still a lengthy process to get qualified, and in the end it is very limited in scope. Few board designers/buyers want to pay the cost to get UL recognition on their parts at all, let alone on a board-by-board basis.

"**Some fabricators think that if they have UL recognition on a rigid-flex submission, then they are qualified to build all rigid-flex boards with that material set. That is also erroneous.**"

2 Some designers have worked around the requirement by specifying that the board be built with materials that are recognized by UL to 94 V-0. This eliminates the sampling and testing requirement, and the associated costs. However, it does not represent UL certification of the board, and would not be in compliance with insurance carrier agreements for product liability. It leaves the board buyer exposed to claims, should anything occur with its end product.

3 The final attempt to fix the problem is not much of a solution. Many board fabricators, particularly the less informed and/or offshore manufacturers, have little or no understanding of the testing requirements for UL recognition. Often, they assume that if they have recognition of flexible circuit constructions, and separately rigid board constructions, then they are legitimately allowed to mix and match. This is erroneous and UL's letter of recognition states directly:

"Products that bear the UL Mark shall be identical to those that were evaluated by UL and found to comply with UL's requirements. If changes in construction are discovered, appropriate action will be taken for products not in conformance with UL's requirements and continued use of the UL Mark may be withdrawn."

Some fabricators think that if they have UL recognition on a rigid-flex submission, then they are qualified to build all rigid-flex boards with that material set. That is also erroneous. The error, if discovered by an auditor, leaves the board fabricator vulnerable to losing their UL recognition, and leaves the board buyer exposed to product liability claims should something go wrong.

In 2004, Printed Circuits, Inc. looked at the problem from its customers' perspective. PCi

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*Boucher, Michelle. 2010. "Why Printed Circuit Board Design Matters to the Executive." Aberdeen Group

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has specialized in the manufacture of rigid-flex boards since 1997, and had been building rigid-flex since 1982, and saw that many of their customers were coming to rigid-flex from either a hard board or flex background and could not accept the cost, testing requirements or limited applicability of UL recognition by individual constructions.

Implementation

PCi undertook a two-year project to build, submit and qualify a set of rigid-flex samples that would represent over 90% of the designs then on the market. The project required 138 samples that took a year and a half to build, and six months of testing to build the largest UL 94 V-0 qualification of rigid-flex in the world.

Interestingly, in the first round of testing a couple of the samples failed, even though they were manufactured with UL 94 V-0 approved materials. This serves to validate UL's requirement that each construction must be tested before UL certification is awarded, and that specifying and using 94 V-0 materials alone is not enough.

After receiving the UL qualification, PCi also added color-coded travelers for all manufacturing lots that required UL certification, which allow the UL auditor to easily verify which lots require UL certification, and to quickly determine compliance to their qualification listing.

As the demand for rigid-flex enters the mainstream electronics packaging arena, designers and buyers will increasingly require UL 94 V-0 rating on their components to maintain their own UL compliance. **PCB**

Bob Burns is the national sales and marketing manager at Printed Circuits, Inc., in Minneapolis, Minnesota.

Sandia Aims to Create Exascale Computing Operating System

In the stratosphere of high-performance supercomputing, a team led by Sandia National Laboratories is designing an operating system that can handle the million trillion mathematical operations per second of future exascale computers, and then create prototypes of several programming components.

The XPRESS project (eXascale Programming Environment and System Software) team includes Indiana University and Louisiana University; the universities of North Carolina, Oregon and Houston; and Oak Ridge and Lawrence Berkeley national laboratories. Work began Sept. 1.

"The project's goal is to devise an innovative operating system and associated components that will enable exascale computing by 2020, making contributions along the way to improve current petaflop (a million billion operations a second) systems," said Sandia program lead Ron Brightwell.

Scientists in industry and in research institutions believe that exascale computing speeds will more accurately simulate the most complex reactions in such fields as nuclear weapons, atmospheric science and chemistry and biology, but enormous preparation is necessary before the next generation of supercomputers can achieve such speeds.

"System software on today's parallel-processing computers is largely based on ideas and technologies developed more than twenty years ago, before processors with hundreds of computing cores were even imagined," said Brightwell. "The XPRESS project aims to provide a system software foundation designed to maximize the performance and scalability of future large-scale parallel computers, as well as enable a new approach to the science and engineering applications that run on them."

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Most-Read PCB007 Market News Highlights This Month

Windows 8 to Miss Expected Users

A recent survey showed that while 96% of consumers own a Windows-based PC, only 39% of these are likely to upgrade to Windows 8. The survey also revealed that Windows 7 is a clear favourite, with 28% selecting this version as their preferred choice and 14% selecting Windows 8.

Smartphones to Take Larger Share of Flash Memory Usage

Approximately 792 million flash memory units, including both NOR and NAND varieties, will ship in 2013 to smartphones, compared to 703 million units for feature phones, according to an IHS iSuppli Memory On the Move Market Brief from information and analytics provider IHS.

Global Economy to Make Hesitant and Uneven Recovery

"The world economy is far from being out of the woods," OECD Secretary-General Angel Gurría said during the Economic Outlook launch in Paris. "The US 'fiscal cliff,' if it materialises, could tip an already weak economy into recession, while failure to solve the euro area crisis could lead to a major financial shock and global downturn..." Mr. Gurría said.

China's GDP Increase to Fuel Demand for Consumer Goods

The recently concluded 18th China Communist Party Congress, which saw outgoing President Hu Jintao deliver a report on China's economy and a roadmap for the next decade, will jump-start key industries including the information and communications technology (ICT) sector.

Global Display Market to Hit $164.24B by 2017

According to a new market research report, "Global Display Market 2012 - 2017 by Technology [E-Paper, OLED, LED, LCD, DLP, LCoS, Plasma], Type [Conventional, Flexible, Transparent, 3D], Applications [Consumer Appliances, Home Appliances, Automotive, Industrial, Healthcare, Others] & Geography, " published by Markets and Markets, the total global display market is expected to reach $164.24 billion by 2017.

Semiconductor Equipment Sales to Hit $38.2B in 2012

After a 151% market increase in 2010 and a 9% increase in 2011, the equipment market is expected to contract by 12.2% in 2012. Growth is expected in just two regions in 2012—Taiwan (12.7% increase over 2011) and South Korea (10.7%).

Industrial Electronics Semiconductor Market Outlook Dims

Revenue for industrial semiconductors—used in a wide array of application markets from home automation to aeronautics and military purposes—is projected to finish the year at $31.4 billion, up 3% from $30.5 billion in 2011. This year's meager expansion contrasts with the solid 9% increase of last year and the exuberant surge of 35% in 2010, immediately after the recession.

Home Automation Services Market Sees Strong Growth

"Home automation adoption is moving into the mainstream as a combination of home connectivity, standardization, and a range of new sensors and devices bring an ever expanding number of players into the market," says Jonathan Collins, principal analyst, ABI Research.

Medical Electronics Market Poised to Hit $4.1B by FY 2012

The medical electronics market remains a steady source of revenue growth in semiconductors and is expected to reach nearly $4.1 billion in global revenue for the FY 2012. Over the next few years sales will accelerate at a steady rate of 9 percent on average thanks to rapidly aging populations and a greater emphasis on preventative care.

Competitive Tablet Segment Alters Supply Chain Strategies

"With the changes taking place in the mobile PC segment, existing supply chain relationships could be disrupted due to competitive conflicts," noted Jeff Lin, of NPD DisplaySearch. "For example, Samsung Display plans to improve its mobile PC customer portfolio by reducing its share in Apple and increasing support to captive brands and other external customers, like Amazon and Barnes & Noble."

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Screen Printing Applications in Electronics—Part A

by Karl Dietz
KARL DIETZ CONSULTING, LLC

SUMMARY: This column reviews several screen printing applications that are used in the fabrication and assembly of printed circuit boards and electronic packages and devices.

There are several screen printing applications that are used in the fabrication and assembly of printed circuit boards and electronic packages and devices. They include:

- Screen printing of non-photoimageable, UV-curable or thermo-curable ink through a screen that has been patterned with a photosensitive emulsion. The ink can be screened onto single-sided copper-clad laminate for print and etch circuitization or as a plating resist for double-sided and multilayer boards, or as a soldermask
- Screen printing of photoimageable liquid soldermask onto finished circuit boards. This operation can be double-sided in a vertical mode, or single-sided in a horizontal mode
- Application of "legend print," typically by screen printing, but more recently by inkjetting, after soldermask application, so called "legend print" is applied. This white lettering on top of the usually green soldermask coating may contain information regarding lot numbers, date of manufacture, position markings for component mounting, component type, etc.
- Application of solder paste by screen or stencil printing in assembly, i.e., the mounting of active and passive components onto the board through solder joint connections
- B²it process, which includes multiple screen printing steps forming cone-shaped bumps with silver paste that serve as Z-axis interconnects in a coreless microvia HDI package
- Screen printing of conductors and via fill with thick film conductive pastes on LTCCs (low temperature co-fired ceramics)
- Screen or stencil printing of conductive or non-conductive via fills in PCBs
- Screen printing of silver paste conductors on solar cells
- Screen printing of embedded capacitor and resistor structures in PCBs, modules and substrates

All of these printing steps have to be able to handle the customary board formats, with the exception of solder paste printing, which may be done after the board has been broken up into smaller patterns that were possibly repeated

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two, four, or six times ("2-up", "4-up", and "6-up" format) on the board. This process is called singulation. Thus, for solder paste printing, the original board size is the largest that is handled. More often, solder paste printing is done after singulation with half-size, one-quarter-size or one-sixth-size formats.

The smallest board size is typically 12x12 inch. The reason some boards are processed in such small formats has to do with the difficulty of achieving good registration and fine line resolution on larger formats. Other common formats are 12x18, 18x24, and 20x24 inch, whereby 18x24 inch is by far the most common. Boards typically travel through the various processing modules with the longer size in machine direction (and the smaller side in transverse direction), which means that for an 18x24 inch board the squeegee stroke length of a screen printer would be 24 inches.

Term	Definition
Mesh Count	Number of wires per linear inch/cm in a screen mesh
Mesh Angle	Orientation or "bias" of wire mesh relative to the screen frame
Mesh Tension	Level of tightness in screen or resistance to deflection (Newtons/cm)
Emulsion	Polymer coating in the mesh that defines and gaskets print
Squeegee	Polymer blade used to move ink across and through mesh
Durometer	Hardness or flexibility of squeegee or emulsion (Shore A units)
Squeegee Pressure	Amount of effective, downward force applied by the squeegee
Squeegee Travel	Mechanical limit to horizontal squeegee travel across screen
Downstop	Mechanical limit to vertical squeegee travel to the substrate
Attack Angle	Forward printing angle of squeegee (affects hydraulic forces)
Snap Off	Distance between underside of screen and substrate surface
Flood	Coats mesh surface with fresh ink in preparation for next print
Print/Flood	Printing in one direction with a flood coat in the opposite direction
Print/Print	Printing substrate w/two passes of ink, one in each direction
Print/Alternate	Printing substrate w/one pass of ink, in alternating directions
Scavenging	Squeegee edge scrapes some ink from mesh openings after transfer
Viscosity	Internal resistance of a fluid relative to motion under external shear
Rheology	Characterization of viscous flow relative to shear forces and/or time

Table 1: A glossary of terms used in screen printing (source: DuPont).

The screen is typically patterned with a polyvinyl acetate or polyvinyl alcohol-based photosensitive emulsion. The emulsion is coated onto the screen mesh, dried, exposed through a phototool, and developed. Alternatively, the emulsion pattern can be formed on a support sheet and subsequently transferred to the screen.

The substrate is placed under the screen frame, ink is applied on top of the patterned screen, and a squeegee then pushes the ink through the openings of the screen. Several types of squeegee profiles and materials are in use, and the proper selection will depend on the application. A diamond-cut profile squeegee is fairly rigid and is sensitive to the screen printer settings, especially the required "parallelism." This type of squeegee is used for high resolution patterns in small formats. A rectangular or flexible squeegee is less sensitive to printer settings and is used for high-speed printing of large patterns. A dual or triple composite durometer squeegee is a reasonable compromise to pattern large areas with good resolution. The harder durometer composite backs up the softer layer, or in the case of triple composite, is sandwiched between two softer layers.

Next month's Tech Talk, "Screen Printing Application in Electronics—Part B" will look at a few of these applications in more detail. **PCB**

Karl Dietz is president of Karl Dietz Consulting LLC, offering consulting services and tutorials in the field of circuit board and substrate fabrication technology. Dietz can be reached by e-mail at karldietz@earthlink.net or phone (001) 919 870 6230.

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Wire Bonding and Soldering on ENEPIG and ENEP Surface Finishes with Pure Pd-Layers

By Mustafa Özkök and Dieter Metzger
ATOTECH DEUTSCHLAND GMBH
and Joe McGurran and Hugh Roberts
ATOTECH USA INC.

This article was presented at IPC APEX EXPO 2012 in San Diego, CA.

Abstract

As a surface finish, electroless nickel/electroless palladium/immersion gold (ENEPIG) has received increased attention for both packaging/IC-substrate and PWB applications. With a lower gold thickness than conventional electroless nickel/immersion gold (ENIG) the ENEPIG finish offers the potential for higher reliability, better performance and reduced cost [1,2].

This paper shows the benefits of using a pure palladium layer in the ENEPIG and ENEP (electroless nickel, electroless palladium) surface finishes in terms of physical properties and gold wire bonding test results.

Introduction

The ENEPIG surface finish originated in the mid-1990s as a modification of the conventional ENIG finish. During development of ENEPIG, it was recognized that the addition of a palladium (Pd) layer between the nickel and gold enabled both gold and aluminum wire bonding operations, in addition to the normal soldering application. In addition, the Pd layer was found to limit the corrosion of the nickel by an overly aggressive immersion gold process. An electrolytic nickel/gold finish was typically the process of record (POR) for such wire bonding needs.

Comparison of Properties of Pure Palladium vs Palladium-Phosphorus (PdP) Deposits

One subtle difference in the ENEPIG processes available in the market pertains to the deposition of electroless palladium. The electroless palladium layer in ENEPIG can be deposited either as a palladium-phosphorous alloy (PdP) or as "pure" palladium. The deposition mechanism may be similar, because both can be deposited in an autocatalytic (electroless) manner. However, the physical properties of the two deposits are quite unique, resulting in differences for the assembly steps of soldering and wire bonding.

Hardness of Electroless Deposited Palladium

One key difference between the two types of palladium layers relates to the hardness of PdP and pure Pd deposits. Increasing the phosphorus content also increases the hardness of the palladium deposits, as shown in Figure 1.

The hardness of autocatalytically deposited pure Pd is 250 HV, whereas the hardness of PdP (with 4-6% phosphorus content) is approximately twice that value. The lower hard-

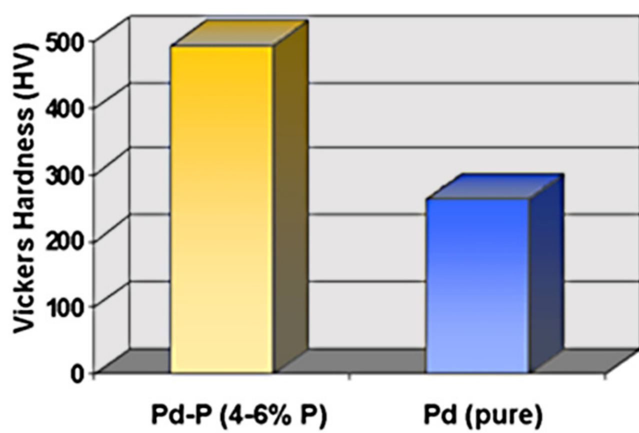


Figure 1: Hardness comparison of palladium-phosphorus and pure palladium autocatalytic deposits.

Pd Type	Stress Type	Value
Pd-P (4-6 w%P)	Tensile	3800 N/mm²
Pure Pd	Tensile	2100 N/mm²

Table 1: Comparison of internal stress of PdP and pure Pd deposits.

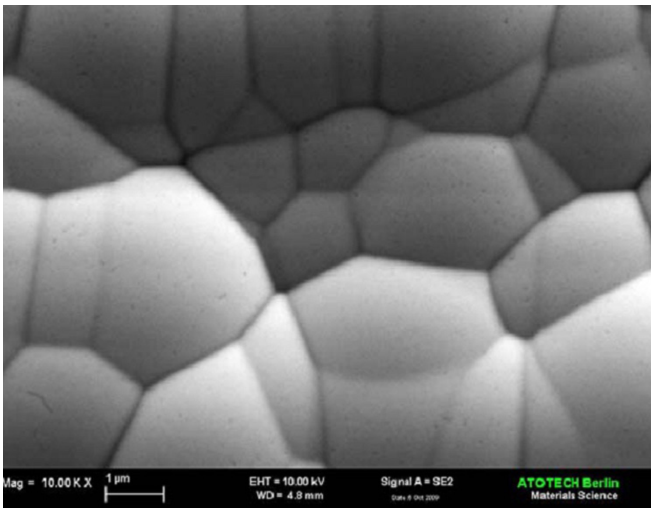


Figure 2: PdP deposition (0.15 μm) over nickel, showing a relatively even and smooth surface.

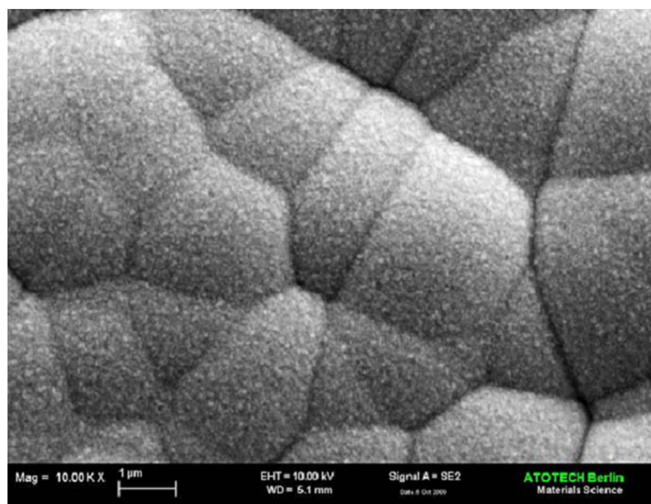


Figure 3: Pure Pd deposition (0.15 μm) over nickel, showing some nano-roughness on the surface.

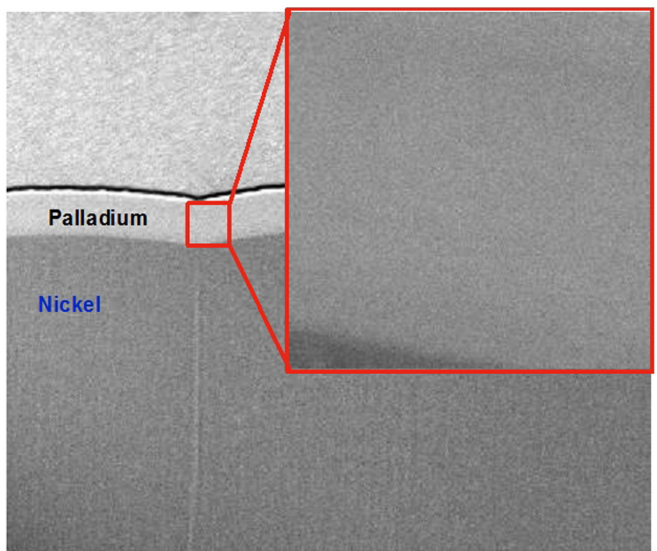


Figure 4: PdP deposition (0.30 μm) shows an amorphous structure.

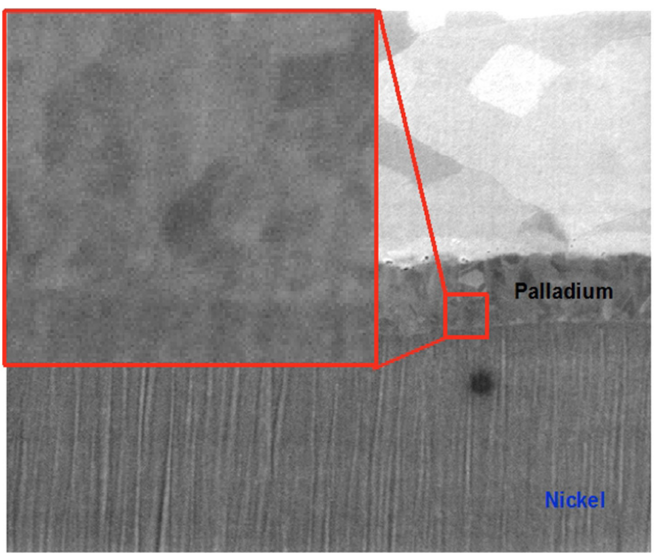


Figure 5: Pure Pd deposition (0.15 μm) on nickel shows a fine crystalline structure.

ness of pure Pd is regarded as one explanation for the better wire bonding performance of ENEPIG with pure Pd in comparison to ENEPIG with PdP.

Internal Stress in Deposited Pd Layer

The value of internal stress is an indicator of the amount of mechanical energy captured within the layer after the electroless deposition. The Pd crystal structure and the type of electroless deposition influence this value. Lower internal stress is clearly shown for pure Pd. The reason for this difference is presumed to be the different crystal structures of pure Pd and PdP.

Topography of Electroless Palladium

When comparing the surfaces of pure Pd and PdP depositions, some difference in the topography is apparent. As shown in Figures 2 and 3, the PdP surface shows an even and smooth topography within the individual grains, whereas pure Pd exhibits a form of nano-roughness. The larger grains reflect the known structure of the underlying nickel layer.

Crystal Structure

As illustrated in Figures 4 and 5, cross-sections show that the crystal structure of PdP is amorphous, whereas pure Pd is characterized by a fine crystalline structure.

Test Conditions for Gold Wire Bond Investigation

The following wire bond test conditions were used for the further wire bond investigations (see Figures 6-8 and Table 2).

To assess the wire bond performance of ENEPIG finishes with pure Pd in comparison to PdP, investigations were conducted with varying thicknesses of gold, palladium and nickel. As shown in Figures 7 and 8, almost no difference exists between the two finishes in terms of either wire pull force or failure mode for samples with a thicker gold deposit (0.15 µm). However, in the case of lower gold thickness (0.04 µm) the ENEPIG finish with pure Pd exhibits significantly greater pull strength results and a higher incidence of the preferred wire bond failure mode.

Sample Overview

Wire bonding test vehicle

Au wire bonds placed on 125 µm bond finger

Figure 6: Test layout for wire bonding.

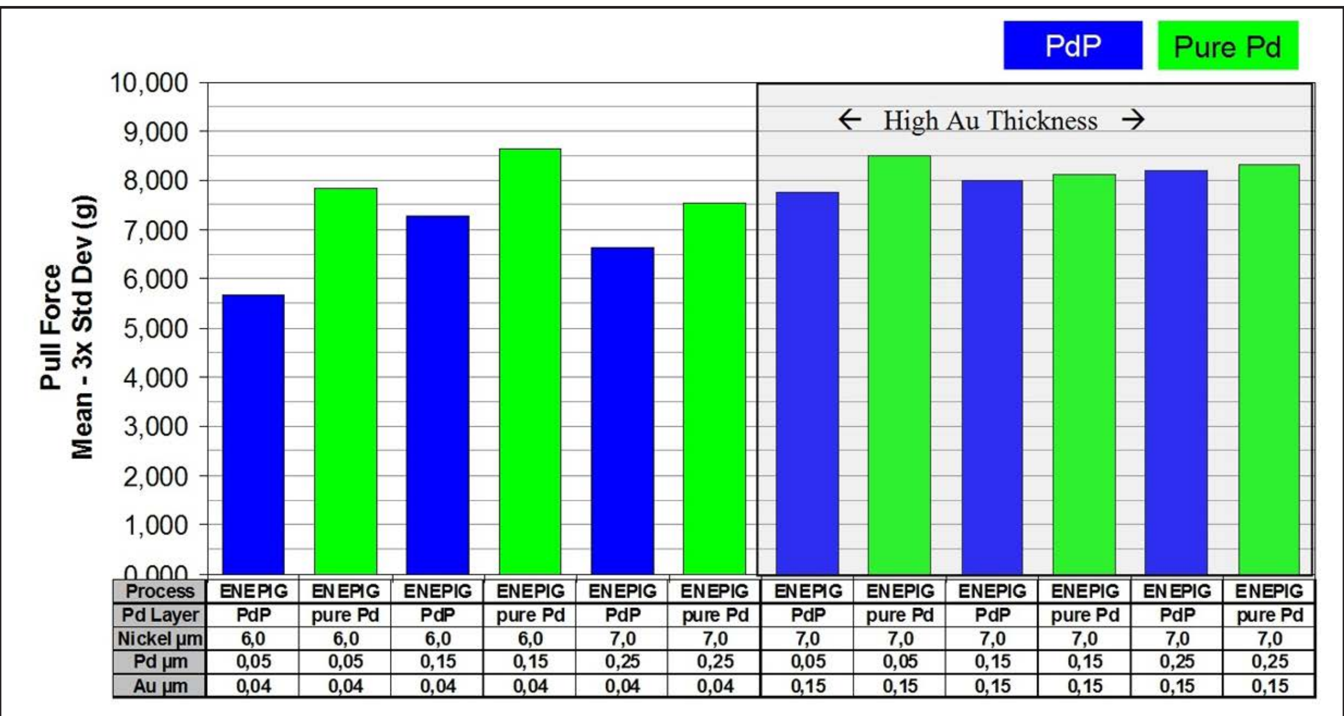
Bond Parameter	
Wedge US	0.68
Wedge Force (g)	24
Time (ms)	20
Temperature* (°C)	165

Equipment Details	
Bonder	Delvotek 5410
Bond capillary	41488-3823-R35
Company	Kulicke & Soffa
Au Wire	Type GMH
Ø	23 µm
Company	Tanaka

Sample Details	
Sample	WBTV
Surface Finish	Universal ASF II
Aging	4h 150°C

Pull Test Conditions	
Pull Tester	Dage 4000
Pull Speed (µm/s)	500

Table 2: Wire bonding and sample parameters.



Process	ENEPIG	ENEPIG	ENEPIG	ENEPIG	ENEPIG	ENEPIG	ENEPIG	ENEPIG	ENEPIG	ENEPIG	ENEPIG	ENEPIG
Pd Layer	PdP	pure Pd	PdP	pure Pd	PdP	pure Pd	PdP	pure Pd	PdP	pure Pd	PdP	pure Pd
Nickel µm	6,0	6,0	6,0	6,0	7,0	7,0	7,0	7,0	7,0	7,0	7,0	7,0
Pd µm	0,05	0,05	0,15	0,15	0,25	0,25	0,05	0,05	0,15	0,15	0,25	0,25
Au µm	0,04	0,04	0,04	0,04	0,04	0,04	0,15	0,15	0,15	0,15	0,15	0,15

Figure 7: Comparison of gold wire bond pull test results for ENEPIG (with PdP) vs. ENEPIG (with pure Pd) with varying thickness of Ni, Pd and Au.

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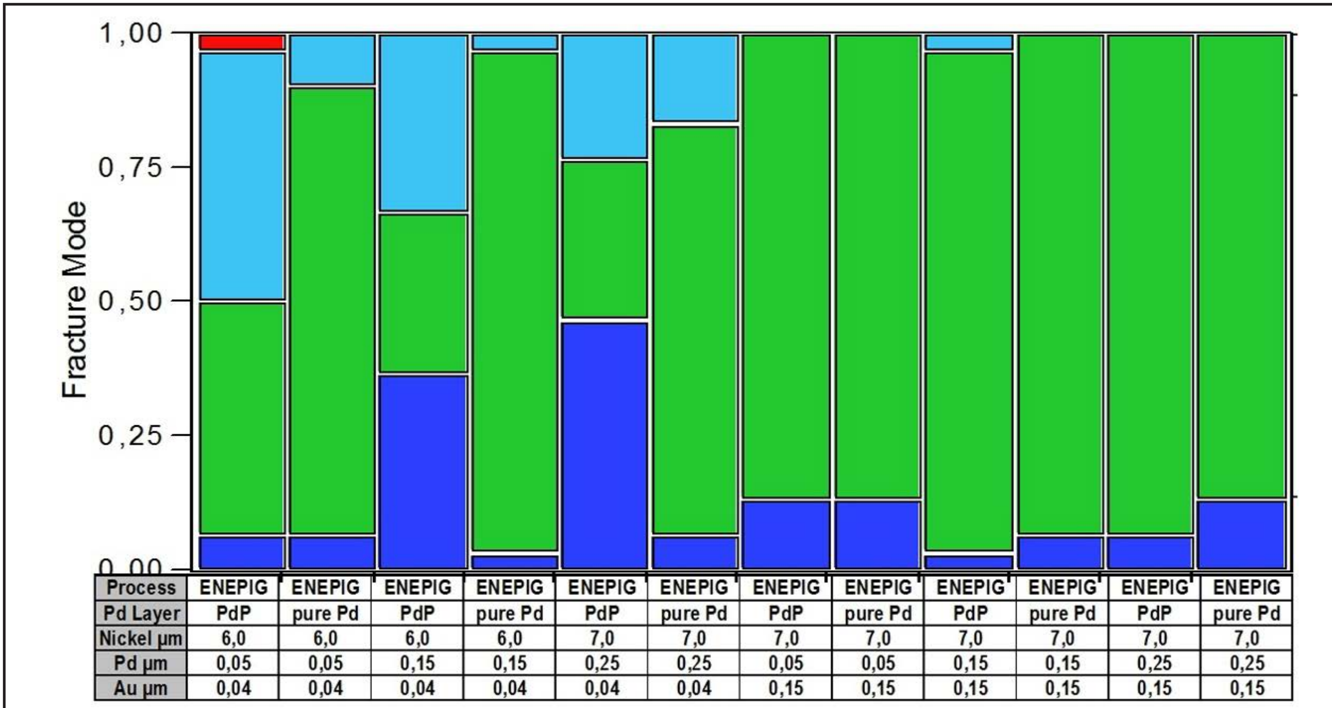

Process	ENEPIG	ENEPIG	ENEPIG	ENEPIG	ENEPIG	ENEPIG	ENEPIG	ENEPIG	ENEPIG	ENEPIG	ENEPIG	ENEPIG
Pd Layer	PdP	pure Pd	PdP	pure Pd	PdP	pure Pd	PdP	pure Pd	PdP	pure Pd	PdP	pure Pd
Nickel µm	6,0	6,0	6,0	6,0	7,0	7,0	7,0	7,0	7,0	7,0	7,0	7,0
Pd µm	0,05	0,05	0,15	0,15	0,25	0,25	0,05	0,05	0,15	0,15	0,25	0,25
Au µm	0,04	0,04	0,04	0,04	0,04	0,04	0,15	0,15	0,15	0,15	0,15	0,15

Figure 8: Comparison of gold wire bond failure mode results for ENEPIG (with PdP) vs. ENEPIG (with pure Pd) with varying thickness of Ni, Pd and Au.

It is theorized that reducing the gold thickness increases the effect of the palladium hardness on the wire bonding process. Furthermore, it is assumed that a softer Pd layer is beneficial for the wire bonding process. As known from electrolytic deposited Ni/Au (i.e., "soft" gold), the hardness does have a significant influence on gold wire bonding. Conversely, electrolytic deposited hard gold is not used for wire bonding in the market. As such, ENEPIG with pure Pd can operate with a wider operating window for gold wire bonding, but more importantly, it can operate with lower gold thickness and still achieve similar results.

Copper Wire Bonding Capability of ENEP Surface Finish

With respect to the ENEP surface finish, the use of pure Pd does provide a further significant benefit. Recent investigations have shown that copper wire bonding is possible for IC substrate and PWB applications when performed on ENEP surface finishes having a pure Pd layer. For semiconductor applications, copper wire bonding on pure Pd ENEP is already established [4, 5, 6].

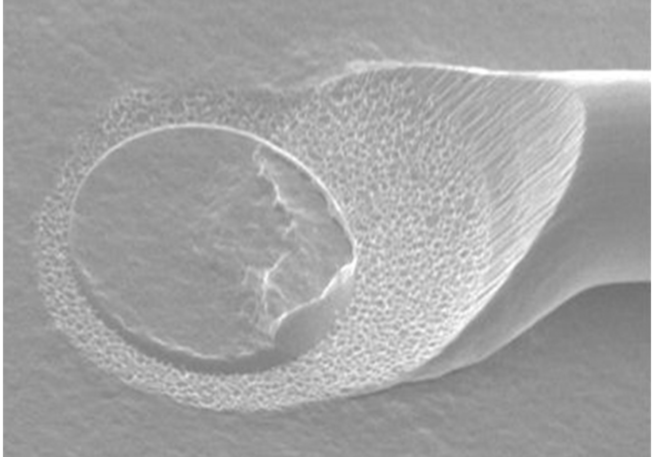

Figure 9: Typical copper wire wedge bond.

Summary

These investigations show that using electroless pure Pd depositions (without co-deposited phosphorus) can enhance the performance of ENEPIG surface finish. In the case of ENEPIG, the use of pure Pd widens the process window for gold wire bonding and, as demonstrated, allows a reduction in the gold thickness, thus enabling an increase in yield on the assembly side

Most-Read PCBDesign007 News Highlights This Month

NEWS

"Father of the Gridless Router" Alan Finch Dead

Few people in the electronics industry can honestly claim responsibility for a quantum leap in technology. Alan C. Finch was one of those people. Finch, the "father of the gridless autorouter," passed away this weekend in the UK. I was fortunate enough to talk with him by phone years ago, and found him very unimpressed with his "rock star" status in the EDA world.

Agilent Releases ADS 2012

ADS 2012 features new capabilities that improve productivity and efficiency for all applications the system supports and breakthrough technologies applicable to GaAs, GaN and silicon RF power-amplifier multichip module design.

Probe Manufacturing Receives Recognition for Growth

Kam Mahdi, Chairman and CEO, said, "We are honored and excited to have been recognized by the Orange County Business Journal for our robust growth over the past two years, which ultimately ranked Probe as the 9th fastest growing company in Orange County."

Mentor Graphics Debuts New Thermal Testing Method

Mentor Graphics Corporation today announced the new T3Ster DynTIM tester, the industry's cutting-edge method of measuring thermal characteristics of thermal interface materials (TIM).

Ventec AS9100C Approval Fully Certified

Ventec Europe is proud to announce that its parent company, Ventec Electronics Suzhou Co. Ltd., is now fully certified to AS9100 Revision C, the quality management standard specifically written for the aerospace and defence industry, in accordance with the Aerospace Supplier Quality System Certification Scheme EN9101:2009, EN9104-001 edition January 2012 and SR002.

Zuken CADSTAR Distributor Quadra Solutions Expands

Zuken has announced enhanced support for its Scandinavian CADSTAR users as UK-based distributor Quadra Solutions expands. Scandinavia is an increasingly important region for Zuken. Sales in Scandinavia of CADSTAR—Zuken's desktop PCB design solution—has seen consistent growth.

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as well as a possible cost reduction. In addition the ENEP surface finish with pure Pd is offering the associated cost reduction by avoiding the expenses for the gold bath and ENEP with pure Pd enables next generation interconnection techniques, namely copper wire bonding. PCB

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4. "Nickel-Palladium Bond Pads for Copper and Gold Wire Bonding," Horst Clauberg, Asaf Hashmonai, Tom Thieme, Jamin Ling and Bob Chylak

5. "Next Generation Nickel-Based Bond Pads Enable Copper Wire Bonding," Bob Chylak, Jamin Ling, Horst Clauberg, and Tom Thieme

6. "Nickel-Palladium Bond Pads for Copper Wire Bonding," Horst Clauberg, Petra Backus and Bob Chylak

Those Problematic Soldermask Issues—a Case Study

By Mike Carano
OMG ELECTRONIC CHEMICALS

SUMMARY: There are multiple reasons why soldermask lifts and peels from the board surface. In this actual case study, test your troubleshooting skills by zeroing in on the root cause of the defect.

Introduction

I am sure you have heard the words, "It's not rocket science." Apologies to the rocket scientists. Sometimes PCB fabrication just makes it look that way. This month's Trouble in Your Tank approaches the subject of soldermask adhesion using an actual case study. As the reader will note, I recommend using sound troubleshooting methodology to zero in on the root cause of the problem.

Problem Statement

A medium-sized U.S.-based PCB fabricator had started to experience adhesion failures of liquid photoimageable soldermask on select part numbers. The company utilizes a double-sided screen printing machine to apply the solder mask.

The fabricator claims that "nothing has changed" (I love that one). Figure 1 shows an example of the defect.

The fabricator noted that these peeling issues were only evident after going through hot air solder leveling (HASL) and on occasion the electroless nickel immersion gold process (ENIG). From a troubleshooting standpoint, it is critical to first get a baseline measurement of the problem. Tech service personnel on the scene performed some basic tape peeling tests on soldermask boards prior that had yet to be processed either in ENIG or HASL. The results of the tape testing revealed sporadic but definite mask peel from edges and the tops of traces even prior to subjecting the boards to HASL and ENIG. Thus, one first should rule out the final finish processes (at least in this case) as the root cause of soldermask peeling.

Brainstorming the possible root cause(s) yielded the following:

- Poor surface preparation of the bare copper prior to mask
- Contaminants on copper surface preventing adhesion of mask
- Excessive mask thickness
- Inadequate mask thickness leading to stress points on edge of traces
- Insufficient tack dry of mask prior to exposure
- Under or over curing of the mask

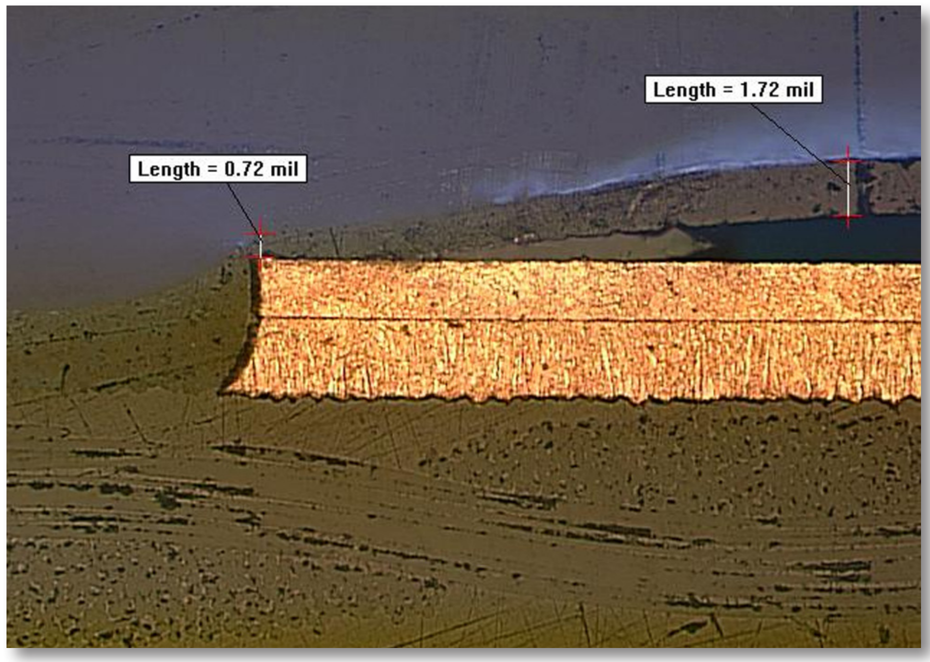

Figure 1: Cross-section of soldermask peeling.

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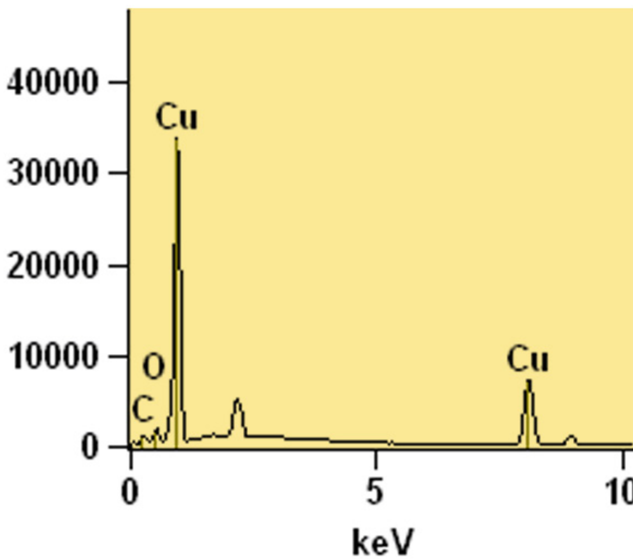

Figure 2: EDAX scan of copper surface under the peeled or blistered mask.

First, the tech service engineer reviewed and audited the pre-cleaning (surface prep) of the bare boards prior to mask application. The fabricator employed a mechanical surface prep system that utilized pumice. This is a very effective means to ensure sufficient surface topography of the copper surface by allowing bonding sites for the mask.

The second concern was that there were residues or contaminants on the copper surface that were negatively impacting adhesion. EDAX was performed on several areas of the copper surfaces where the mask had peeled (Figure 2). The analysis showed that the copper surfaces (eight tests in all) were not impacted by any type of contamination.

The next areas of concern were related to over-dry mask thickness (either too thin or too thick). Mask that is too thin leads to stress points that can easily be attacked by final finish chemicals or exhibit poor adhesion in general due to the thin mask deposit. Alternatively, excessively thick masks and possible reasons for this will be presented later.

In summation:

- Excessive soldermask thickness will cause incomplete drying of the mask, excessive artwork marking, and potential soldermask peel due to solvent entrapment
- Mask thickness should be controlled between 2-2.5mils wet
  - Wet mil thickness of 2-2.5mils equates to 5.7-6.5 grams/ssf of wet mask
  - Boards with less than 2 oz. total copper should be ran between 5.7-6.0 grams/ssf

A random check of several circuit boards showed mask thickness in many cases between 3.0-4.2 mils thick when dry. That is after tack dry and solvent evacuation. This is clearly unacceptable. To further underscore this point, the tech team again took several finished PCBs and immersed those parts in methylene chloride. The results can be seen in Figure 3.

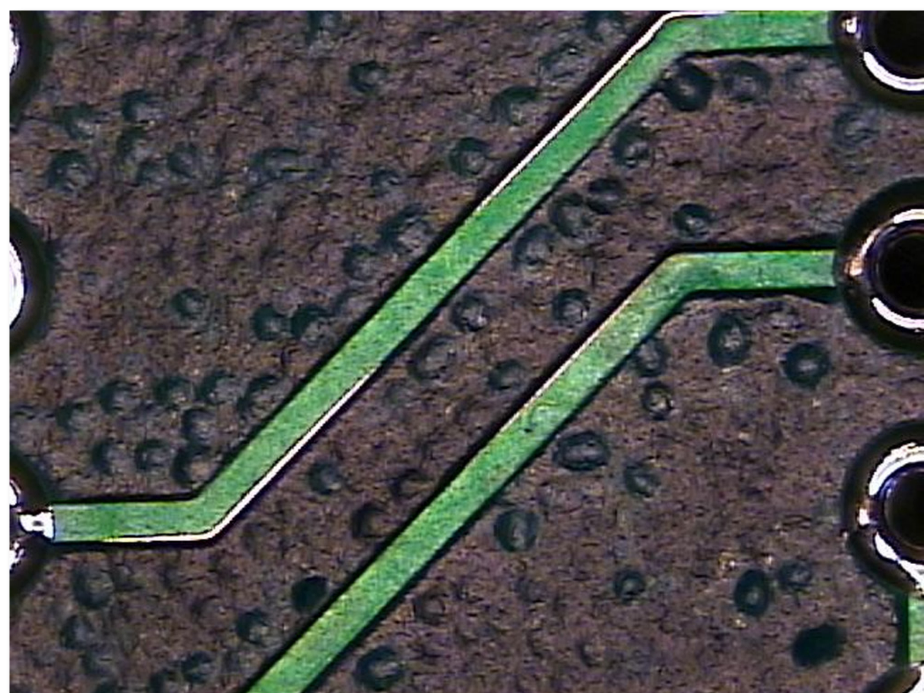

Figure 3: Evidence of blisters in mask after methylene chloride soak test.

The tech team then audited the tack dry process including temperatures and dwell times. The good news was that the process was indeed within specification for the soldermask being used. However, the issue remained that the wet thickness was over the specification and needed to be corrected.

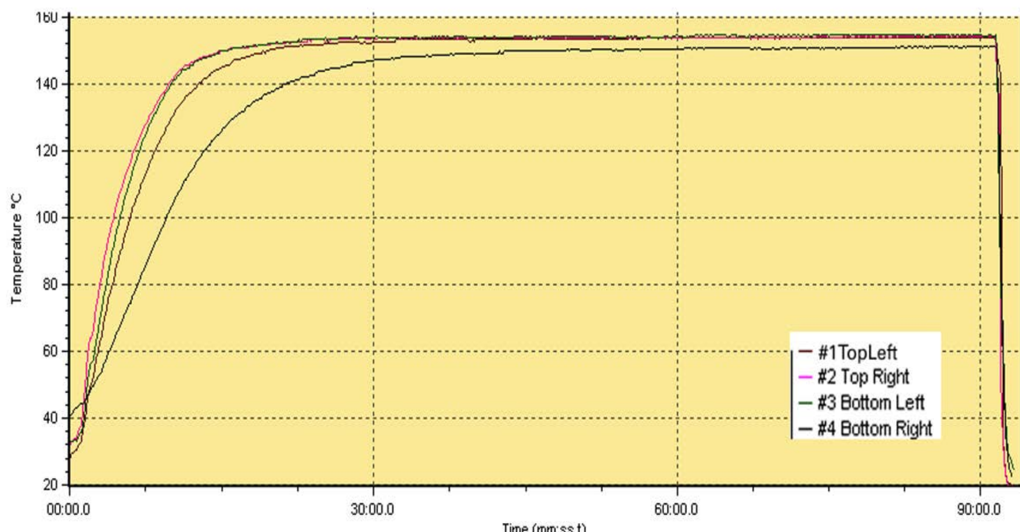

Figure 4: Temperature profile of the thermal curing oven for the soldermask.

Interestingly, further analysis showed that even some of the "in specification" thickness solder mask features were showing evidence of blistering and peeling. This necessitated a thorough review of the soldermask final curing process.

Fully cured and properly tack dried soldermask will pass a 30-minute methylene chloride soak cycle without exhibiting signs of blistering or peel. The soldermask in this case failed the soak test for blistering and peeling indicating solvent retention in the mask prior to exposure and potentially an under-cure issue.

The process control document for the soldermask in question required a final cure temperature of 150°C for 60 minutes. That means curing temperature must be maintained for the entire time, exclusive of ramp-up time. This also means the surface of the circuit board must "see" that temperature for the entire time. The review of the profile indicated that the final cure temperature was only reached and held for 42-45 minutes, which indicates insufficient final curing. This can easily cause the mask to peel and blister.

Corrective Action

In order to bring this process within specification, two items were addressed. First, the thickness of the mask had to be adjusted back to the 2-2.5 mils of wet thickness. This was achieved by educating the operators on proper viscosity adjustment for the solder mask in use. It was determined that operators were not properly adding solvent to the primary mask material resulting in a wet material that was essentially too high in both solids content and viscosity. This resulted in higher wet weight thicknesses further compounding tack dry and final cure. The second item marked for corrective action was to bring the final cure process within specification.

The results of the profiles indicated that there were not only failures to reach the proper cure temperatures, but there were variations within the thermal oven itself. Tech service engineers discovered an air vent that was completely open. This prevented the bottom left of the thermal oven from reaching the desired temperature/dwell time. Adjusting the vent to halfway open reduced the temperature variation in the oven and all locations met requirements. Secondly, the engineer adjusted the peak temperature in the oven to 155°C, which further ensured that the surface of the board achieved the desired final cure temperature. **PCB**

Michael Carano is with OMG Electronic Chemicals, a developer and provider of processes and materials for the electronics industry supply chain.

Most-Read PCB007 Supplier/ New Product Highlights This Month

Robert Burkle Names New Company Managers

The company management of Robert Bürkle GmbH, represented by Hans-Joachim Bender and Ralf Spindler, has been completed by Renato Luck and Jürgen Brenner. Luck will be responsible for the technology sector and manage product innovation, development and project management. Brenner will be responsible for the production sectors of the German locations in Freudenstadt, Paderborn and Mastholte.

Maskless Wins Multi-System Purchase Order for N.A.

Maskless CEO Bill Elder commented, "We are very pleased to be working with Frank and his team at Technica USA. Their professionalism and technical understanding of our system's assets allows them to be able to present our products in such a way that shows our customers and potential customers the advantages of buying our system."

DuPont MCM Debuts New Low Cost Conductive Inks for PE

DuPont Microcircuit Materials (MCM) is introducing a new series of screen printed conductive ink materials for the printed electronics market, designed to offset the rising cost of silver.

LPKF Board Welcomes Christian Bieniek

In early December, Dr. Christian Bieniek became the fourth member of the LPKF Board of Managing Directors. Bieniek, in his capacity as COO, will head the management, control, and organization of operational processes, as well as operational performance of the specialist mechanical engineering company.

New Tech Promises to Overcome IC Packaging Obstacles

As for the next-generation IC packaging industry, an undeniable need exists to satisfy the demands for finer lines and space on conductors. The new NEAP is one of the technologies that will overcome obstacles the IC packaging industry currently faces in trying to meet requirements for future MPU architecture.

Dow Unveils Commercial-Ready Tech for PCB Mfg

Dow Electronic Materials, a business unit of The Dow Chemical Company, has announced two key commercial-ready technologies for leading-edge PCB manufacturing. Dow brings to market two new MICROFILL™ copper plating products that enhance the performance of high-density interconnect (HDI) and IC substrate PCBs.

Plasma Etch Offers New Green Plasma Etching System

The company has developed a technology called the Magna Series that eliminates the need of CF4 gas presently used daily by PCB manufacturers throughout the world with the use of plasma etching systems for desmear and etchback processing applications.

MOOG Components Secures Zeta Certification

Integral Technology, Inc., a manufacturer and distributor of HDI electronic materials for the PCB industry, has announced that PCB/flex/rigid-flex manufacturer Moog Components Group based in Galax, Virginia, has received Zeta® Certification allowing them to produce circuit boards using Integral's dielectric films.

PPG Fiber Glass JV: Fourth Furnace in Kunshan, China

"This furnace features innovative, state-of-the-art technology," said Terry Fry, PPG general manager of global electronics and the company's regional fiber glass business. "The technological advancements of its manufacturing operation enable us to maximize process efficiency while saving energy and reducing emissions."

Gardien Helps Hüco Implement Integrated Test

As a global solution provider, the Gardien Group draws on the expertise and long-standing experience of their teams to support customers with tailored solutions. Through this tailored approach Gardien has been working closely with Hüco to identify the best ways to support their new department.

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RF/Microwave: A Series of Unfortunate Events

by Judy Warner

I repeatedly hear two unfortunate stories from our RF and microwave PCB customers.

Story one includes the following plot points:

1. RF engineer creates schematic
2. RF engineer passes on to PCB layout person and oversees critical design areas
3. PCB layout person or engineering manager quotes for PCB prototype build with reputable source
4. Reputable PCB source scraps the boards a couple of times before giving up altogether
5. PCB layout or engineering manager is now in big trouble with their schedule and/or their customer
6. New supplier is chosen
7. Repeat steps 3-6

Story two looks like this:

1. RF engineer creates schematic
2. RF engineer lays out his own board because the layout department has been eliminated, and they didn't like having to look over the shoulder of the layout person anyway—this way is just faster
3. RF engineer doesn't realize that their uber-powerful software allows them to do things that are neither practical nor ideal for manufacturing
4. RF engineer/manager quotes prototype boards at a reputable supplier
5. Board supplier reports the board will be very expensive or not buildable because of manufacturability issues
6. RF engineer goes back to the drawing board, or pays too much money for an unnecessarily complex board
7. Reputable PCB supplier scraps the boards and finally concedes they can't make the board
8. Repeat steps 5-6 from story one

All parties from both stories above are blameless. Generally, they are well educated and adept at their given profession. Why, then, do I repeatedly hear these tragic tales? I've given this a lot of thought and asked many questions of colleagues and industry peers. Here is what I have learned.

First of all, due to economic constraints, companies are often asking their RF engineers to wear two hats, one as engineer, and the other as PCB designer. Because of the complex performance needs of these boards, a layout person often needs oversight in order to avoid violating areas that would impact critical performance. By taking the layout person out of the equation, some redundancy is eliminated. However, what are lost are the unique skills of the layout person who is at all times mindful of manufacturing practices and limitations. To exacerbate the

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Strengthening & Advancing Electronics Manufacturing Globally

matter, current layout software, while very flexible and powerful, does not necessarily raise a red flag if a design is not practical or feasible to manufacture.

The end result is a board that is either very expensive to manufacture or completely impossible to make. So while saving money by eliminating an area of potential redundancy, costs are driven up by poor PCB designs, or the need for redesigns. In this case, RF engineers can't possibly know what they don't know! For this reason, I contend that RF engineers are innocents in these sad tales of woe.

Now, let's take a look at the role of the board supplier. Notice that I said that the person buying the prototypes chose reputable suppliers. We are talking about well-established, quality circuit board manufacturers here. From what I can best understand, it appears to me that many board suppliers are not fully aware that they don't really know how to make RF/microwave boards. They make boards with astronomical layer counts, superfine lines, buried and blind vias—the whole gamut. So when they get a quote for some boards using Rogers 6000 series material that is only four to six layers, it appears to be an easy job. They may have made a few products on Rogers 4350, and from there they make one large, highly flawed assumption—that these materials are the same, or at least similar. So they take the job and start processing the materials, which become unruly. The registration is off, the impedance measurements are off, and plating is a mess. Try as they may, they cannot make the board and don't realize it until they have lost money and have placed their customers in hot water. Again, they don't know what they don't know! That is why I also hold board suppliers relatively harmless in my sad stories.

So much time, money, effort and pain are expended as this cycle continues to repeat itself. Sometimes in the effort to cut costs, we inadvertently increase them while putting our customer relationships at stake. RF and microwave applications require both board design and manufacturing expertise. These products require special processing procedures during fabrication, in particular.

If I could wave a magic wand I would write a new story that goes like this:

1. RF engineer creates schematics
2. RF engineer passes the schematic on to a PCB layout professional who specializes in RF and microwave design—a designer with an eye toward performance as well as the best manufacturing practices, and who needs little to no oversight
3. RF engr/mgr/layout person quotes and has the boards built by a board supplier who specializes in making RF/microwave boards
4. Board supplier gets it right the first time
5. Everybody lives happily ever after… and saves money and headaches along the way!
6. Repeat

Just as RF/MW engineering is a specialty within the general discipline of engineering, RF/MW PCB fabrication is a specialty within the general discipline of board manufacturing. It is absolutely critical that you do your homework and find out if your fabricator is a capable RF/MW specialist. One simple way is to ask what percentage of their work is RF and microwave boards. The length of time that they have been making RF/MW boards is also a helpful indicator. A list of current RF/MW customers and perhaps some references would be useful as well.

RF/MW boards are not always complex, but they are always difficult! Following the advice above will greatly increase your chances of getting your boards made right—the first time.

I hope this will help you to stop writing stories that depict "A Series of Unfortunate Events" and get you writing stories that end with a "happily ever after" for you and your company! **PCB**

Judy Warner is the director of sales and marketing for Transline Technology in Anaheim, California, a PCB manufacturer specializing in RF and microwave applications.

Most-Read Mil/Aero007 News Highlights This Month

NEWS

U.S. State Dept Lists PCBs in ITAR Draft Rulemakings

Calling the State Department's decision a "step in the right direction," IPC President John Mitchell said, "IPC appreciates that the State Department shares our view that ITAR's regulation of printed boards should be clearer." But IPC is still troubled by the inclusion of the term "specially designed" in reference to PCBs.

IPC ITAR Workshop to Raise Awareness

"Domestic printed board manufacturers have sounded an alarm that defense industry confusion over ITAR's treatment of printed boards is undermining national security," said IPC President and CEO John Mitchell. "IPC is grateful for the opportunity to partner with federal officials in workshops like this to clarify current and proposed export control regulations."

FTG Undergoes Organizational Changes

Firan Technology Group Corporation (FTG) has appointed Claude Bougie as president of FTG Aerospace Tianjin. Claude brings with him a wealth of experience in the Aerospace industry and will use this knowledge and experience to ensure the rapid growth of FTG's business in Tianjin. Kaiyan Gu will continue as general manager at FTG Aerospace, Tianjin and will report directly to Claude.

Basic Electronics Touts High-Quality Service, Personnel

Basic Electronics Inc. achieved excellent marks in its AS9100 audit report. As per the audit results from NQA, Basic was noted to have zero nonconformities, with mention of its continued customer satisfaction in delivering quality product with an emphasis on cost improvement.

Call for 21st Century Defense Strategy

The changing global security landscape and worsening fiscal outlook demand significant adjustments to national security strategy and budgeting, according to an extensive, year-long study released today by The Stimson Center: A New U.S. Defense Strategy for a New Era.

MEMS in Military & Aerospace to Reach $283.6M in 2012

Revenue for pressure sensors in both military and civil aerospace applications will reach $35.7 million by year-end, up 20% from $29.7 million last year, according to an IHS iSuppli MEMS Market Brief from information and analytics provider IHS.

Report: Global Military Aviation MRO Market 2012-2022

This report provides readers with a comprehensive analysis of the military aviation MRO market through 2012-2022, including highlights of the demand drivers and growth stimulators for military aviation MRO. It also provides an insight on the spending pattern and modernization pattern in regions around the world.

Air Cargo Security & Screening Systems Market $486.5M in 2013

Visiongain's analysis indicates that the global air cargo security and screening systems market will reach a value of $486.5M in 2013, as airports and air freight companies acquire new screening systems and update existing security systems in order to meet the requirements set aside by relevant government authorities.

DARPA Unveils PIXNET Technology

PIXNET aims to develop helmet-mounted and clip-on camera systems that combine visible, near-infrared, and infrared sensors into one system and aggregate the outputs. This technology would ingest the most useful data points from each component sensor and fuse them into a common, information-rich image that can be viewed on the warfighter's heads-up display.

How Can You Predict Your Company's DAM Future?

by Gray McQuarrie
Grayrock & Associates

***SUMMARY:** If you really want to steer your company in the right direction, then you better take a look inside your soul and examine your own DAM behaviors. The solution to all of your DAM problems is much closer than you think.*

Would you like to look into a crystal ball and know if you are headed in the right direction or the wrong direction with your company? Would you like to know if your company is going to prosper or plummet? Silly and rhetorical I know, but hear me out. You already possess this ability and likely don't even know it. Permit me to be the first to encourage you to change your DAM thinking and use your sensory skills! Malcolm Gladwell's book Blink gets at this innate skill we all possess, so read this book if this article isn't enough for you. Confused? Hang on and let me explain.

How do you feel when you enter the lobby of a supplier or a customer? Do you feel welcome or unwelcome? Does it appear as though they are making lots of money or struggling? Do you get the sense that they are running a tight ship and anticipating, or do you feel they are disorganized and probably just reacting to situations? Do you see any evidence that points to the accuracy of the best supplier award hanging on the wall, or the mission statement which states that people in this company are treated with respect?

How you feel in the lobby and how you are treated in the lobby during the first five minutes tells you a lot about the business you are visiting. But we are trained to take these intuitions and feelings and put them on the back burner with the dial in our brain set to ignore. Yet what you are sensing, right off the bat, and what you will likely continue to sense during your visit, is the culture of the business enterprise.

This is a skill not to be ignored and left to fallow, but to develop and use deliberately to make your company better. In fact, this isn't a luxury; it is a necessity. According to Louis Gerstner, who turned IBM around from the brink of disaster, "If you do not manage culture, it manages you, and you many not even be aware of the extent to which this is happening." Why should you care? Because if you don't do this, if you do not manage your company's culture, you will have DAM problems by the bushel load.

Thinking DAMs, the true source of any DAM problem, are what I described in my first book, Change Your DAM Thinking. To illustrate, let me explain two thinking DAMs: the ego DAM and the learning DAM. If you have someone in your company who you would describe as a perfectionist jerk, who seems to feel that he or she can do no wrong, and treats others as inferior, then you know what I am talking about. The learning DAM described here is the know-it-all, and the ego dam is I am better than you. You can't teach know-it-alls anything new, because they are perfect, so discovery is blocked. Furthermore, you can't work with superior beings, because they are jerks, and productivity is blocked.

Let me give you an example about how debilitating perfectionist jerk behavior can be. Remember back in the 1980s and early 1990s, as layer counts were growing and cores were getting thinner? Well, registration scrap was growing and becoming an increasingly worrisome problem for the entire industry. Everyone believed strongly the problem was the fault of the laminate supplier who could not make a stable core material. During the 1990s, AlliedSignal's Chandler, AZ lamination plant (where I was based) would bake all of the core material in an attempt to stabilize it. And we would do a huge amount of destructive testing using ovens to

simulate our customer's multilayer lamination cycle. Then, we collected data to see if in fact the core was unstable. All of this extra work was really expensive and time-consuming. Moreover, all of this work made our customer relationship worse, not better, because our data used in our test showed the core was stable, but their data used in our core, in their process, showed the core was unstable. There was fear, mistrust, and crisis, especially when a major customer would jump ship in favor of our competitor, who promised a more stable core; of course, this proved not to be the case. We were at a loss as to what to do. It was like we were searching for the Holy Grail. This was a serious DAM problem!

When all of this work and switching lamination suppliers failed to solve the core material instability, which was the believed to be the source of registration scrap, the arguments from know-it-all experts became increasingly fantastical. It was the poor quality of American glass, and Japanese glass was the cure. It was the resin suppliers that the laminators used; they needed to be looking at the control charts of their suppliers' reactors.

All of this fantastical, dogmatic thinking (yes, DAM thinking) got our entire industry further and further away from the real truth. If you challenged anyone who believed in this dogma you might as well prepare yourself for crucifixion. I was one of the few who didn't believe, and I will never forget how my boss went on and on with his face turning all shades of red and the veins popping out of his head, telling me I was insane to pursue the effort: an effort to organize a team to once and for all understand why the core material moved so unpredictably in our customers' processes.

By combining a good pair of ear plugs, an unyielding faith in the scientific method and collaboration with some outstanding people at Continental Circuits, we were able to find (using a Fein Focus machine and doing design of experiments) that it was the interaction of prepreg style (as well as resin content of the prepreg and not the core) in conjunction with the amount of copper left on the core material after etching that was driving the movement and not some sort of unpredictable instability in the core created by exotic issues pertaining to the glass and the resin. In truth, the movement of the core (without any extra baking) was remarkably consistent for a given multilayer construction. One of the ways this is handled today is by having neural net software train itself on movement data from a production population containing a variety of multilayer constructions to come up with reasonably accurate image compensation values.

This wasn't a tough technical problem to understand and solve. What made this problem so impossibly slow to resolve was the perfectionist jerk behaviors of too many well-meaning people, who proved to be obstructing the truth. This happens way too much in our industry. This is why it is important not to ignore this behavior, but identify it and get it out of your company's culture. You can call it "The No Asshole Rule" as Bob Sutton did in his book with the same title, or something more polite, but the question is, what are you going to do about it? Are you going to put up a sign that says "Perfectionist jerks need not apply and if you work for us already, don't be surprised if you are fired?" Check out this YouTube video with Bob Sutton for more ideas about why your company culture is so important.

What do companies like Apple do? Steve Jobs said in an interview: "One of the keys to Apple is that Apple is an incredibly collaborative company… And there is a tremendous amount of teamwork at the top of the company, which filters down to tremendous teamwork throughout the company. And teamwork is trusting the other folks to come through with their part without watching them all of the time." Here is the two-minute interview excerpt with Steve Jobs.

When it became clear that the person in charge of iOS, Scott Forstall, whose team apparently wasn't dealing with Siri issues effectively, and who wasn't collaborating very well with his peers for some DAM reason, would not apologize for Apple Maps, he was fired. All of this had to do with his behavior going against the grain of maintaining Apple's collaborative culture that at its heart was based on trust. Was this a good business decision to let Forstall go, thus preserving the collaborative company culture? Time will tell.

	Question (often or yes = 1, some or maybe = 0, none or no = -1)	
	DAM Thinking (Y-axis)—Are you able to deal with the reality of being DAMmed?	
1	Key people think the company can't perform any better (it's as good as it gets)?	0
2	"Others are to blame and it isn't my fault," is a common theme?	1
3	The biggest obstructionist in the company can't be fired (he or she is indispensible)?	1
4	People feel that the fix to a "problem" is outside of their control and influence?	1
5	Technical skills trump people skills (individual effort trumps collaborative effort)?	0
	The DAMs (X-axis)—What behaviors are DAMming up progress?	
6	Ego DAM: people are out to prove who is the best?	1
7	Learning DAM: People like to demonstrate how much they know?	1
8	My Precious DAM: People protect their turf?	1
9	Trust DAM: People don't trust others to share information?	1
10	Feelings DAM: People don't think they are treated fairly and feel entitled to more?	0

Table 1: Portion of self-assessment test for determining your company culture.

Dysfunction Quadrant: A company is in a rut. Everything is slow. Change is impossible. Margins are declining. Company has slow to no growth.	**Hyper Growth:** Super growth spawned from market disruptive business and product development. Teamwork, operations, logistics, and great execution.
Crisis Quadrant: People fear for their job and don't trust one another. There is little focus. Everyone is distracted and stressed. Meetings are a waste of time. It's survival everyday.	**Development Quadrant:** Teamwork and collaboration! People love work. Focus is on new business systems and market disruptive technology and products.

Table 2.

Where is your company culture? What does it portend for you? Where do you need to go? What is your compass and what is your map? To find out the answer to these questions, visit businessagilitysolutions.com and take the self-assessment test to help you understand your company's culture (Table 1).

Table 2 is a brief description of the type of behaviors you will see and things to watch out for in each of the quadrant categories.

Figure 1 shows the four categories your company can experience: crisis, dysfunction, hyper-growth, or development.

In Figure 1, the X-axis score is determined by how much DAM thinking you have going on in your company (as seen by an increasingly negative score) or how much FLOW thinking (lack of DAM thinking) you have going on in your company (as seen by an increasingly positive score). The Y-axis measures your company focus, which can be reality based or fantasy based. For example, when you have DAM thinking going on, are you dealing with immediate reality or pretending problems don't exist? If you are pretending problems don't exist, then your company is in trouble.

For example, let's say that you believe that you can get away with not knowing the organic levels and/or the age of your plating tank chemistries, and you are not going to get copper stringers. Or, you think you can get away with not having a service contract for your laser direct imaging machine, or not maintaining the accuracy of your laser drills by allowing the temperature and humidity of the room they are in to fluctuate wildly. I have seen all of these things happen in our industry and the resulting crisis scenarios. DAM thinking and pretending we can make shortcuts and get away with it puts us in the crisis quadrant.

When your company has a FLOW thinking culture, then we can have fantasies about how great we could be. For example, at some point William Morean, co-founder and chairman of Jabil Circuits, must have had a far-fetched fantasy about his company being one of the most significant contract manufacturers in the world. And today it is just that and Morean is one of the wealthiest people on the planet. This is a

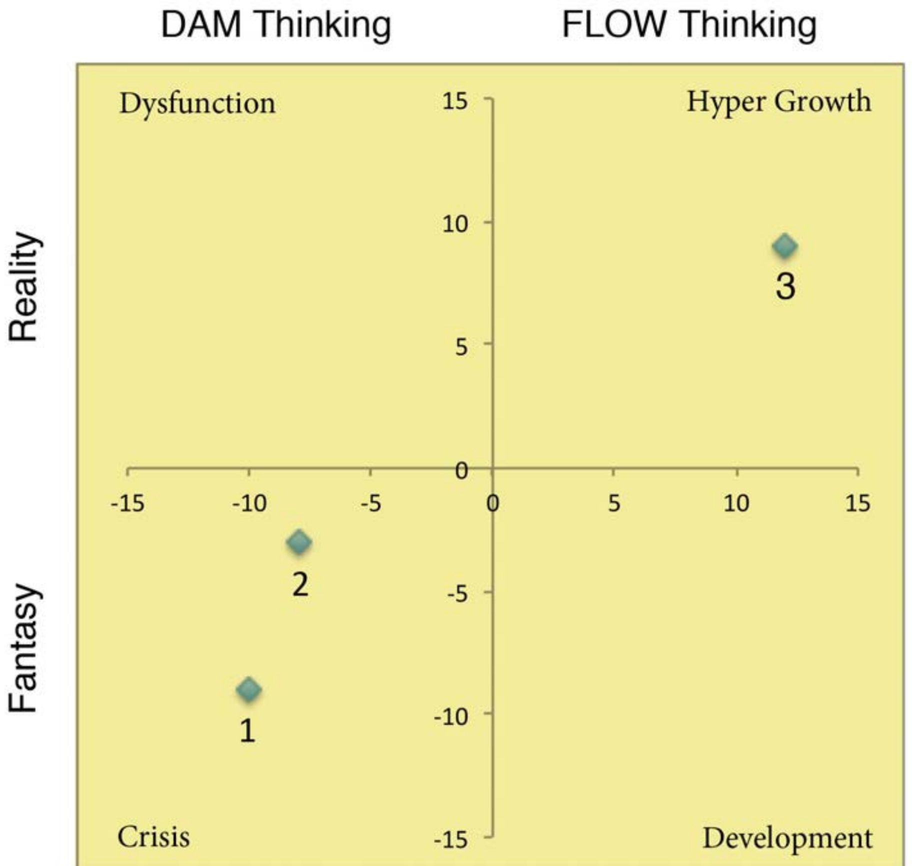

Figure 1: The four culture categories that a company can experience.

company I discussed in my November 2012 column, "Is Kaizen Required to Make Those DAM iPhones?" that does tens of thousands of Kaizens a year. This should tell you something about the importance of collaboration at Jabil.

Probably about as far-fetched as Morean was Earl Bakken, when he ran a ten-employee company called Medtronic and asked my grandfather, who at that time owned a venture capital company called Community Investment Enterprises (CIE) for some money to keep going. My grandfather told Earl he had to dream big, and Earl did dream big, and eventually Medtronic became the biggest medical device company in the world. The point here is that when you have the right culture in your company, dreams can manifest as reality. When you don't have the right culture and dream big, you will accelerate your company's demise. Behaviors lead results. Culture matters—a lot.

If you take the assessment test and find yourself in the dysfunction quadrant, do not despair. How many of us took a "How to Create a Great Company Culture Class," in which we were told what to do? We all have been trained to compete against each other and to be wary and even not trust each other, and pretend that we know it all. It's a hard habit to break.

When people read my first book, they told me, "The book caused me to think a great deal, but you didn't tell me what I was supposed to do." The first step to solving any problem is to be aware of it and observe it not only in others, but more importantly, within yourself. For example, when you see the ego DAM in yourself, understand that you have the power to change it. The next time you are confronted with a challenge, instead of showing everyone how you can do it all yourself, show your company how you can organize others and get them to do it themselves in their own way, where they get full credit. If you can do this seemingly simple thing, you are well on your way to making your company the next Apple, Jabil Circuits, or Medtronic. Your behavior at work, the spirit you think about and conduct your work, will predict your own success and your company's success too. After all, there is only one way to solve your DAM problems and that is to change your DAM thinking. **PCB**

Gray McQuarrie is president of Grayrock & Associates, a team of experts dedicated to building collaborative team environments that make companies maximally effective. Contact McQuarrie at gray@grayrock.net.

TOP TEN

Most-Read PCB007 News Highlights This Month

1 Sunstone Circuits Opens New Oregon Office

The new building, which houses customer service, finance, marketing, human resources and executive management, represents Sunstone's continued growth and commitment to serving customers 24/7/365.

2 IPC APEX EXPO 2013 Highlights 35 Technical Sessions

Over three days, 35 technical sessions with nearly 100 research papers will address additional topics such as military electronics, advanced packaging, fluxes and paste, embedded devices, high-frequency electronics, and ESD. In addition, the areas of rework/repair, cleaning, assembly reliability, solder and alloy reliability, printing and PE will have multiple sessions.

3 IPC: N.A. PCB Shipments, Bookings Down in October

Rigid PCB shipments were down 1.1% in October 2012 from October 2011, and bookings decreased 9.2% year over year. Year to date, rigid PCB shipments grew 4.4% and bookings decreased 0.2%. Compared to the previous month, rigid PCB shipments were down 12.4% and rigid bookings fell 14.3%.

4 Stickleback Acquires D.E.B. Electronics

PCB manufacturer D.E.B. Electronics, established more than 50 years ago, has enjoyed success with a wide customer base. Recently, the company suffered the effects of one of its largest customers moving its business to China. The family-run manufacturer was not able to recover from the loss and closed in the first week of December 2012.

5 Thomas Edman Appointed President of TTM Technologies

TTM Technologies Inc. has announced that Thomas Edman has been appointed as president of TTM Technologies Inc., effective January 7, 2013. Edman will report to Kent Alder, TTM's chief executive officer. Edman brings more than 20 years of executive experience and extensive electronics industry experience in the U.S. and Asia to his new role.

6 IPC/JPCA-4591: Guidelines to Build Printed Circuits

The concept of printing conductors onto a range of substrates has been around a long time, but it's only now beginning to see burgeoning acceptance. IPC is accelerating this growth with standards that will make it easier to specify and build printed electronic circuitry.

7 Spirit Circuits Sees 20% Growth in November

Hampshire, UK-based Spirit Circuits is reporting a 20% growth as they finish the year with a record month. November is the year-end for the PCB manufacturer and their records show they have achieved both the highest ever production output and their highest ever sales intake.

8 Bare PCB Industry's Revenue Hits $5.1 Billion in 2011

The industry's revenue for the year 2011 was reported at $5.1 billion, with an estimated gross profit of 16.39%. Import was valued at $1.9 billion from 78 countries. The industry also exported $1.7 billion USD worth of merchandise to 127 countries.

For the latest PCB news and information, visit: PCB007.com

9 K&F Electronics Joins SPF Premier Partner Program

Semblant announces that industry-leading PCB fabricator K&F Electronics has joined its Semblant Plasma Finish (SPF) Premier Partner Program. K&F Electronics joined the program to address growing OEM demand for PCB surface finish advancements.

10 Becker & Müller Invests in New Blackhole Production Unit

To better meet increasing market demands, PCB manufacturer Becker and Müller has invested in a new PILL unit for the Blackhole HT direct metallization process. This new production line enables the company to fulfill client requests at an even higher level of quality.

EVENTS

- IPC Complete Calendar of Events
- SMTA Calendar of Events
- iNEMI Calendar
- PCB007 Online Events

2013 International CES
January 8-11, 2013
Las Vegas, Nevada, USA

42nd Internepcon Japan
January 16-18, 2013
Tokyo Big Sight, Japan

18th Annual Pan Pacific Microelectronics Symposium
January 22-24, 2013
Maui, Hawaii, USA

DesignCon 2013
January 28-31, 2012
Santa Clara, California

43rd Annual Collaborative Electronic Warfare Symposium
January 29-31, 2013
Pt. Mugu, California, USA

SEMICON Korea 2013
January 30-February 1, 2013
Seoul, Korea

SPIE Photonics West 2013
February 2-7, 2013
San Francisco, California, USA

6th Annual Mobile Deployable Communications
February 7-8, 2013
Amsterdam, Netherlands

Medical Design & Manufacturing
February 11-14, 2013
Anaheim, California, USA

Electronics Manufacturing Korea 2013
February 13-15, 2013
Seoul, Korea

IPC APEX EXPO® Conference & Exhibition 2013
February 19-21, 2013
San Diego, California, USA

CMSE—Components for Mil & Space
February 20-21, 2013
Los Angeles, California, USA

Embedded World
February 26-28, 2013
Nurnberg, Germany

MEDTEC Europe
February 26-28, 2013
Stuttgart, Germany

IEEE CPMT Advanced Pkg Material
February 27-Mar 1, 2013
Irvine, California, USA

Medical Devices Summit
February 28-March 1, 2013
Boston, Massachusetts, USA

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MASTHEAD

PCB007 Presents

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ADVERTISER INDEX

atg Luther & Maelzer GmbH........................ 25
Burkle North America.................................. 41
CA Picard... 3
Electra Polymers.. 39
Fein-line Associates...................................... 91
Gardien... 35
IPC.. 83, 93
Isola.. 15
Maskless Lithography.................................. 21
Matrix USA.. 53
Mentor Graphics............................ 71, 73, 75
OMG Electronic Chemicals.......................... 31
Panasonic... 9
The PCB List.. 2
Prototron Circuits... 57
Rogers... 63
Semblant... 5
Stebgo... 49
Taiyo America.. 79
Technica USA.. 45
Troostwijk... 87
Uyemura... 65
Ventec... 7
Viking Test.. 77

Next Month in *The PCB Magazine:* HDI

Advances in component packaging continue to drive the demand for PCBs with interconnection densities far higher than can be achieved by traditional technologies, and HDI PCBs with microvia interconnects have become established as an enabler for a new generation of mobile devices and high-tech electronics. The February issue of *The PCB Magazine* will explore the latest HDI developments with experts from around the world.