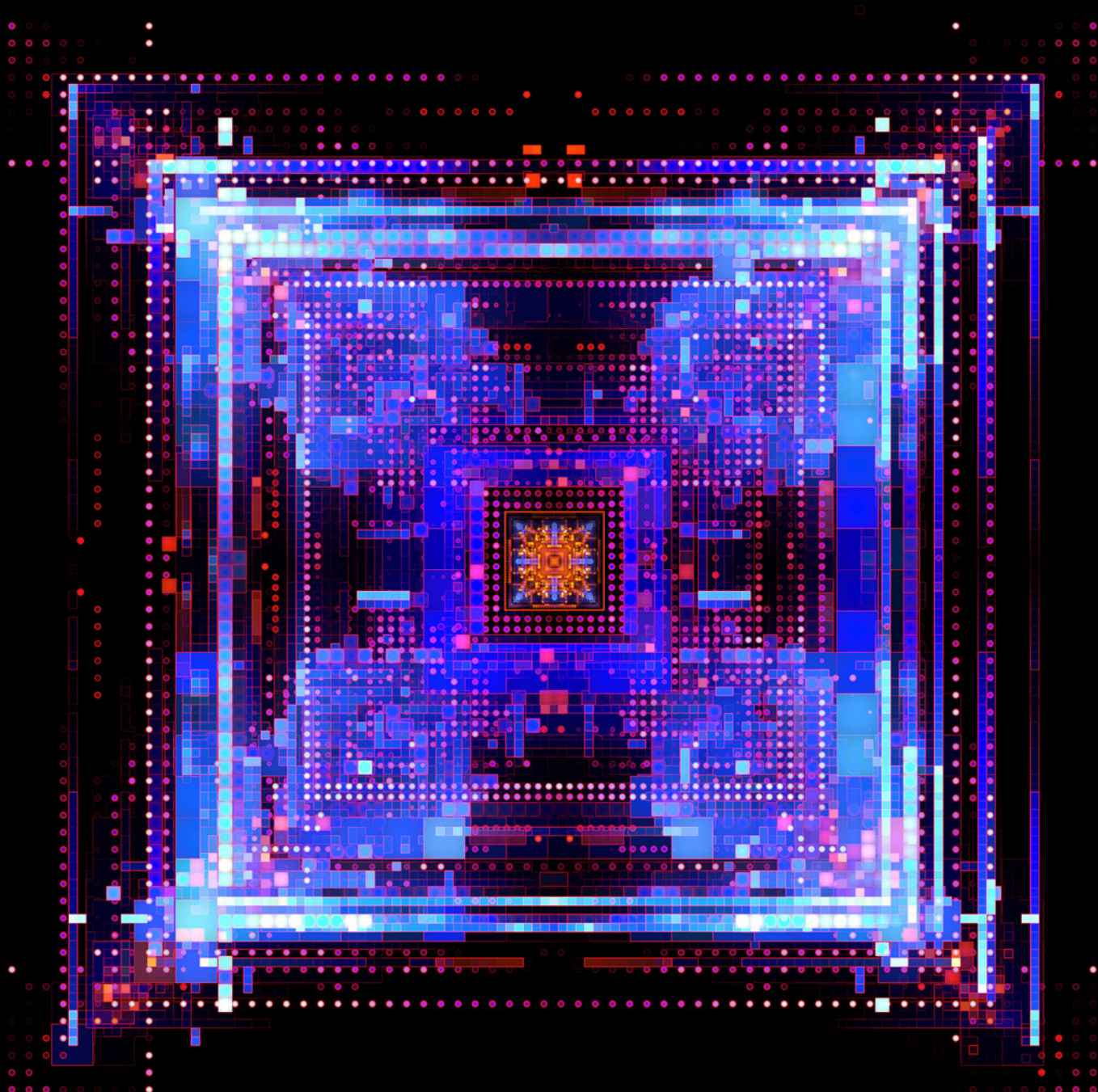


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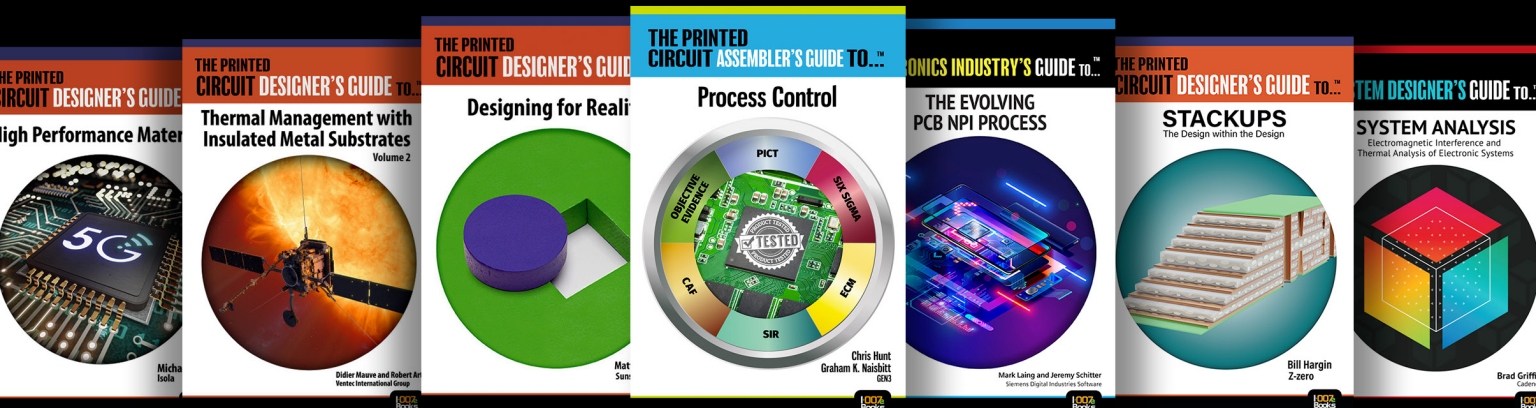
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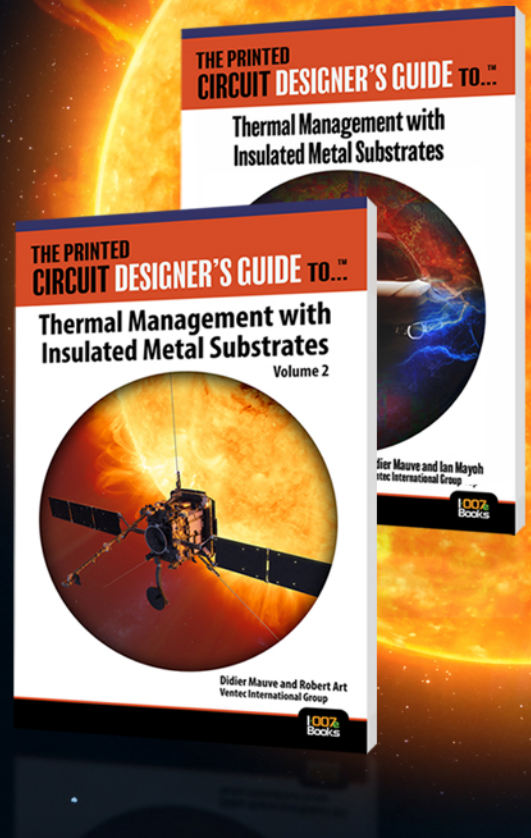


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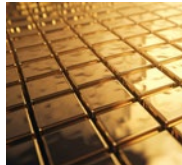
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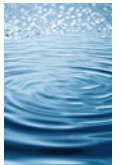
Advanced, Complex, and Emerging Strategies

This month, our contributors focus on designing PCBs with advanced, complex and emerging technologies. We investigate design strategies for boards that are on the cutting edge of technology, or crazily complex, or so new that designers are still writing the rules as they go, like Wyatt Earp and his brothers taming a lawless cow town.

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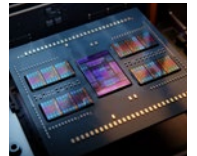
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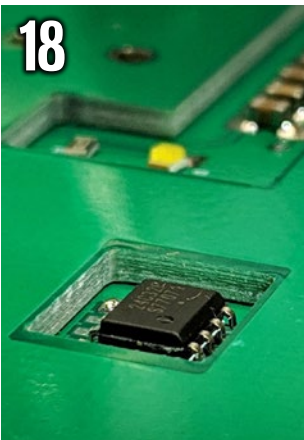
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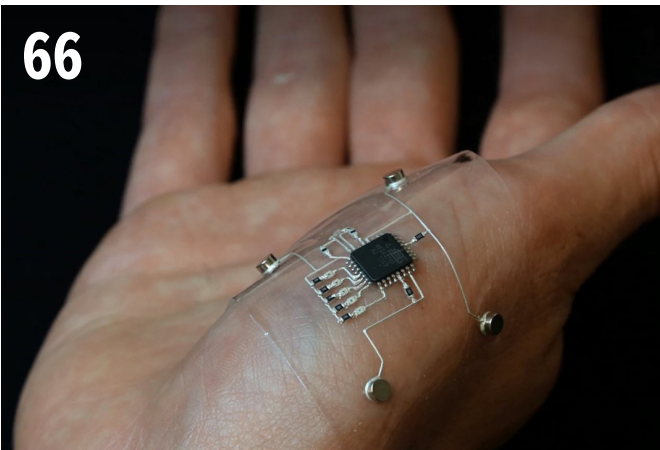
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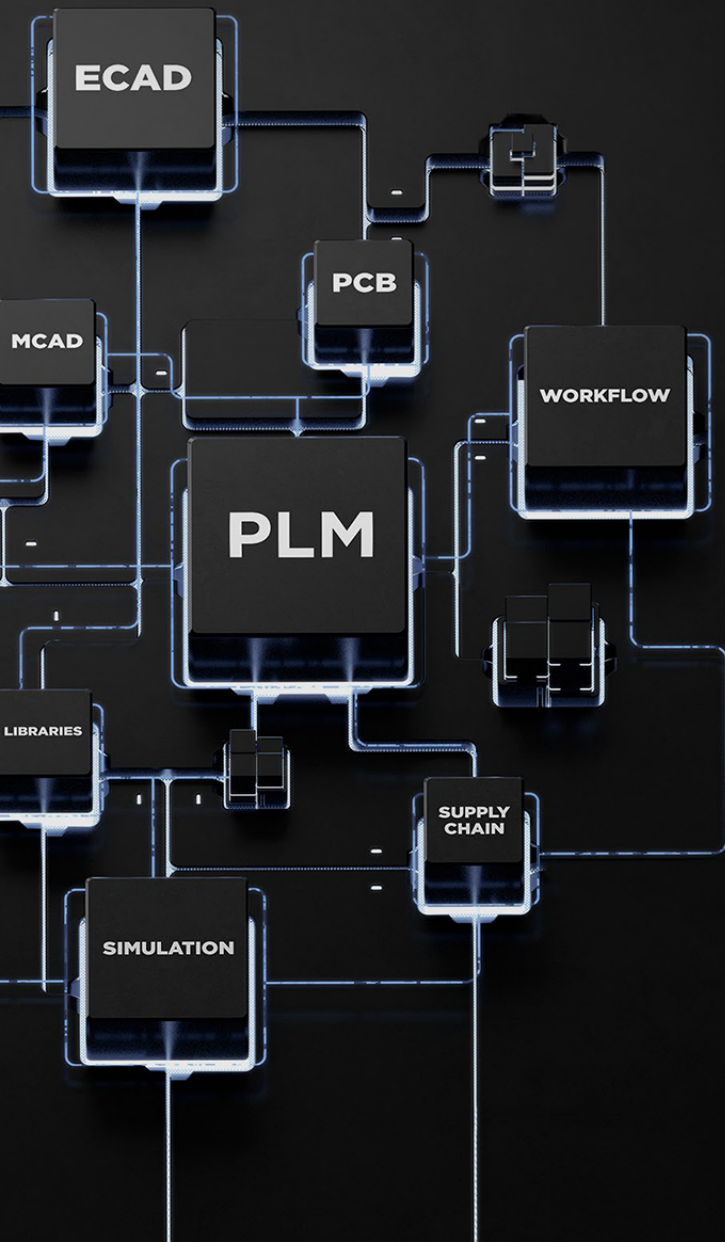


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Advanced, Complex, and Emerging Design Strategies

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

I've spent 24 years writing about PCB design, and there's been one constant this entire time: Designers are an off-grid group of people. I know several people who live in RVs, and they're all PCB designers.

Designers are all a little unconventional. In fact, being off grid may be a requirement for success as a PCB designer. Some designers are really "out there." They like to push the limits of

their design abilities. They don't like the status quo; they enjoy the challenges inherent in this job. They don't shy away from new ideas, new materials, and new techniques. These designers look for ways to bend the laws of physics to meet their needs.

If I've just described you, you're in luck. This month, we focus on designing PCBs with advanced, complex, and emerging technolo-



gies. We'll talk about design strategies for boards that are on the cutting edge of technology, crazily complex, or so new that designers are still writing the rules as they go—like Wyatt Earp and his brothers taming a lawless cow town.

Albert Gaines kicks off this issue with a discussion about RF techniques and his work designing fragmented aperture antennas. Next, John Watson shares some of his strategies for designing tiny PCBs, which can bring, if not huge challenges, at least some trade-offs.

Kris Moyer points out that sometimes cavities aren't a bad thing, especially when there's a need to reduce board skyline. As the industry moves toward smoother copper, Martyn Gaudion focuses on modeling the effects of surface roughness on transmission lines. Vern Solberg explains how designers can take advantage of heterogeneous chiplet packaging. Barry Olney takes cavity design to the next level; he discusses methods for taming the electromagnetic energy that emanates outward in all directions from multilayer plane cavities. Tim Haag explains how he learned to design advanced circuit boards and he offers advice to inexperienced designers facing bleeding edge technology. Rick Ramos shares his strategies for designing and manufacturing wearable biosensors.

We also have columns from Joe Fjelstad and Jamin Wilson (a new contributor from Sunstone Circuits), and the third installment of a flex series by Mike Morando.

I hope you all are having a good summer. I'll see you on the road soon enough. **DESIGN007**



Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 23 years. To read past columns, [click here](#).



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RF Antenna Design on the **Bleeding Edge**

Feature Interview by Andy Shaughnessy

I-CONNECT007

At SMTA Atlanta Tech Expo and Forum, I met with PCB designer Albert Gaines, owner of HiGain Design Services. Albert has been working on some really interesting, fragmented aperture antenna designs, and some of this stuff is really pushing the limits.

Al and I discussed his work with RF, the differences between COTS and custom antennas, and his efforts to educate engineers about what they can and can't do.

Hi, Albert. Good to see you. I understand you're doing some pretty interesting antenna design work. Tell us about it.

We're doing some really fancy designs, compared to what we used to do; we're doing the

sequential lay-up up of board layers with Rogers and other types of high-frequency laminates. They are actually back drilling, filling, and planarizing blind vias on internal layers, and then stacking materials as we need them for the dielectrics we need. Instead of depending on this particular core, we're actually using a single layer of double layer cores, stacking up sometimes two or three layers of special prepreg.

Then it gets pretty interesting. This is all about trying to get away from having a large parabolic antenna. You have a flat circuit board with all these receivers or transmit elements all over it, and we basically create a grid. It's like the dot matrix of your LED TV—they get



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Albert Gaines

signals from each one of those combined and through software and then get an antenna. The largest one so far has a 242-transmitter array on one side and a 242-receiver array on the other side.

Who are the typical customers for this sort of thing?

As you can expect, there are some big players in this market. There is still a great push to get satellite access more transportable and smaller. Some customers are looking at it from a commercial standpoint, like the trucking or the airline industry. It's just a portable antenna for wherever you might need it; you can open up a case, lay it on the ground or just take it out, mount it on a truck or whatever. The whole antenna structure is about 40" x 30". They are also developing smaller arrays for specific applications.

It's interesting when you start working with 4-mil spaces and other small features. I always tell everybody that my favorite button is Zoom, but it's relative to whatever space you have to work with, and when you see a board that's 40" x 30"—wow, that's a pretty big element.

But it's been very interesting, and the technology has really changed. We have some good board shops that we're working with, and they're willing to push the envelope in a niche market. It has opened my eyes over the last couple of years about what can be done in a circuit board environment, as opposed to limitations you are put on by an average board shop.

We're not even looking at multiples of two layers of boards. Some of these are 11-layer and 15-layer boards. We're using a lot of special materials. As I was saying, we just finished one module that's about the size of a cellphone. It has low-noise amplifier stages with printed filters and combiners on internal layers. We just basically kept stitching back and forth while adding layers until we got all the elements we needed and came out the other end. It's more a matter of what you need, and not the limitations of a normal board.

You mentioned that you're doing more of this RF work than ever before.

Yes. I worked for 20 years for Scientific Atlanta, a leader of satellite communication, doing a lot of RF front ends, couplers, filters, and other printed elements; that was what I did. I've been self-employed now for almost 22 years and I was primarily doing digital, power supplies, etc. Somebody reached out to me a while ago and said, "Hey, can you do this?" I said, "Yes, I can."

So, I started working with them, and then their board shop turned me on to a couple of others. Now probably 70% of my current work is high-frequency antenna microwave circuits. My clients are really pushing the envelope, if there actually is one.

How do you determine whether you should design your own antenna or buy a COTS antenna? Where do you draw the line?

From what I know, the thing with COTS is that they're generally made for a specific application frequency range and have integration limitations. If you're trying to pinpoint your appli-

cation and want to have controls, you can get somebody to develop that.

Can you get me a photo of this antenna?

No. I wish I could share with you what the elements looks like. It's basically a bunch of copper squares; one of them almost looks like the screen of a Space Invaders game—very pixelated. A lot of it is way above my head. Most of these engineers or PhD guys know how to run the software and come up with the models. My job is to put the reins on them and say, "You can't do this, but you can do this." But I've learned some things that we can do that I thought we couldn't do.

This has become a big part of my job as I get older. I'm spending a lot of time training people: "You can do this, but you can't do that. You can't have a 2-mil annular ring here." I feel like that's part of what us older guys are here for—to share our knowledge. I tell people that I'm training PhDs every day.

That makes you at least an adjunct professor.

I guess that's why they call it leading-edge technology, and it's good to be in that world. I'm doing something different, something new, and it may be the next wave of the future.

It sounds like it's some pretty advanced stuff, but you're having fun with it.

Yes, you try to have fun with it, but it makes for a lot of late nights and strenuous days. It's always good to push the limits and learn along the way. In today's world, if you are not learning, you are losing.

Is there anything else you want to add?

I really appreciate your magazine. I look forward to every issue that comes out, and I suggest that other designers should pick it up.

It's been great catching up with you, Albert. Thanks.

Thank you, Andy. DESIGN007



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Honey, I Shrunk the PCBs

Elementary, Mr. Watson

Feature Column by John Watson, CID, ALTIUM

In 1989, the family-friendly science fiction adventure film, “Honey, I Shrunk the Kids,” was released. This movie, with a grammatically incorrect title, follows the misadventures of inventor Wayne Szalinski, played by Rick Moranis, who accidentally shrinks his children and their friends down to a minuscule size with his experimental shrinking machine.

Through a series of unfortunate events, the children end up stranded in their backyard, and because of their size, it becomes a treacherous and gargantuan wilderness. As they try to navigate their way home, the kids encounter a series of larger-than-life obstacles. Things that generally would not be a problem now pose a huge challenge: the lawn turned into a vast jungle and everyday objects became life-threatening. They face menacing insects, unpredictable

weather conditions, and are forced to sleep inside a LEGO brick.

As an industry, we live in our own version of “Honey, I Shrunk the Kids.” PCB designs are shrinking smaller and smaller with each design spin. Our industry demands

the latest and greatest, where

innovations coming off the

line must be smaller and

sleeker and have all

the latest new func-

tions, which, as we

know, determines

the fit and form. Miniaturization

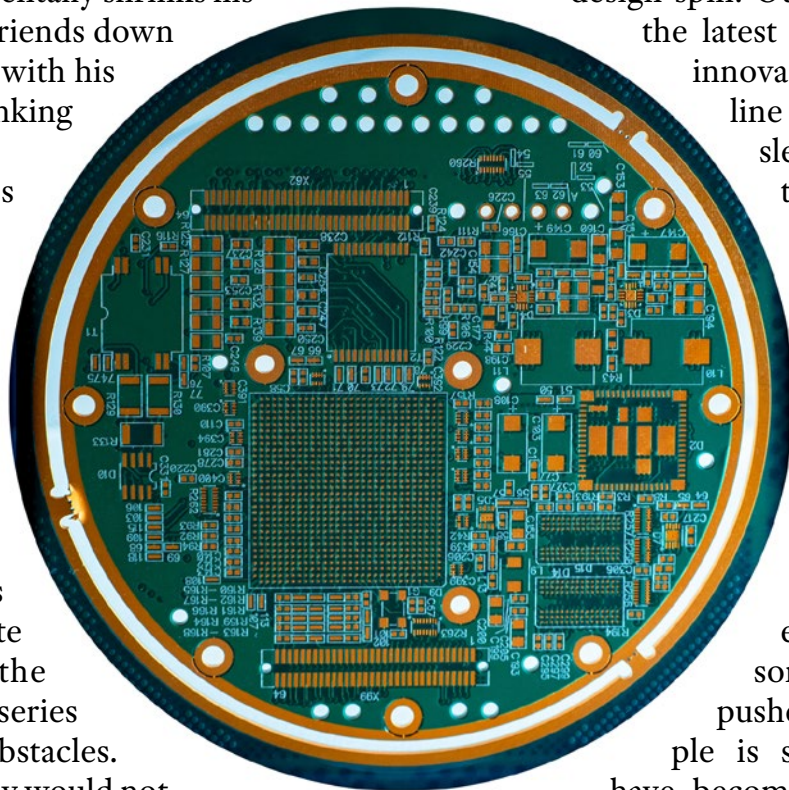
and integration is a growing trend

with electronics.

Manufacturers have pushed that

trend to the very edge of the envelope; some would say they’ve pushed too far. One example is smartphones, which

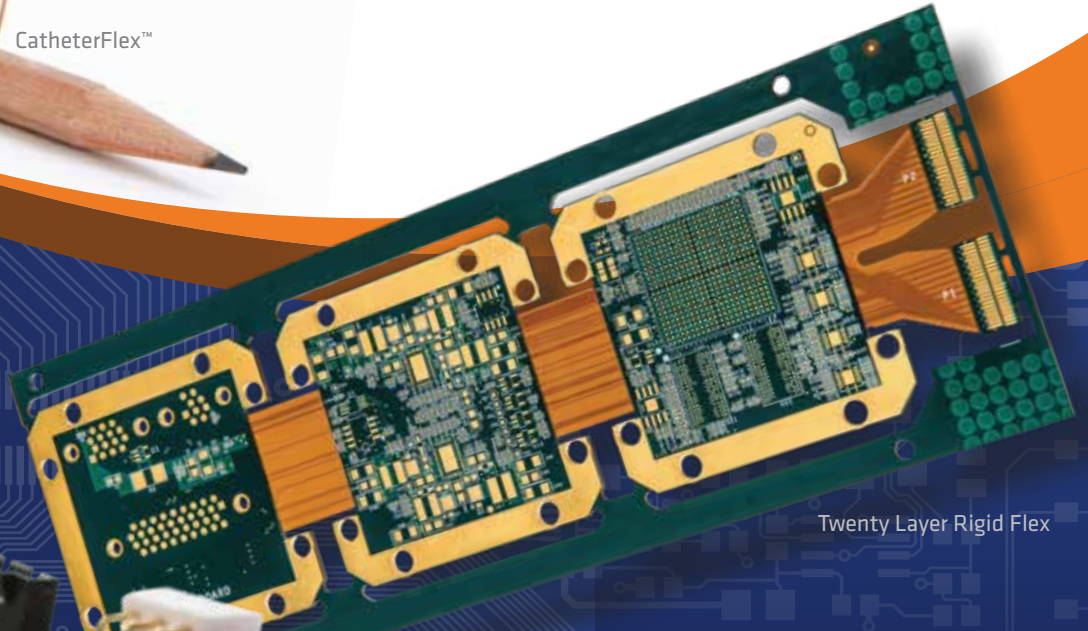
have become increasingly compact, resulting in smaller screen sizes and, consequently, smaller virtual keyboards. This is a problem for me, because I suffer from a common condition called Fat Finger Syn-



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drome, better known as FFS. Many users with FFS have expressed frustration with the diminishing size of smartphone keyboards, making typing more challenging and prone to errors. The reduced surface area of the keyboard often leads to unintentional typos, making it difficult for people (such as myself) to type accurately.

Nowhere is the tinier tech trend happening faster than with wearables and medical devices. The future market size and revenue growth of such a wearable technology market is expected to experience significant growth. Statista said the wearable devices' market size was around \$27 billion in 2020¹, and it is projected to reach over \$74 billion by 2026. You see them everywhere: fitness trackers, smart watches, glasses, rings, jewelry, clothing, and even shoes with embedded sensors monitoring every feasible detail about your life. It's today's version of the mood ring. (The younger generation may have to Google that one.)

Such devices come with unique engineering challenges, but the bigger problem is that wearable devices collect and transmit personal data. This is all done wirelessly by uploading your health metrics, location information, and even personal habits into the cloud. There lies the risk that this data could be intercepted or misused, compromising an individual's privacy. These wearable devices are vulnerable to security breaches and hacking. If not properly secured, personal information or sensitive data stored on the device could be accessed by unauthorized individuals.

Design Challenges and Considerations

As we saw in "Honey, I Shrunk the Kids," size matters; the same goes for our PCBs. Things that were not typically a concern with a larger

PCB design become significant problems when you reduce the board size. It is the equivalence of the backyard becoming the vast jungle.

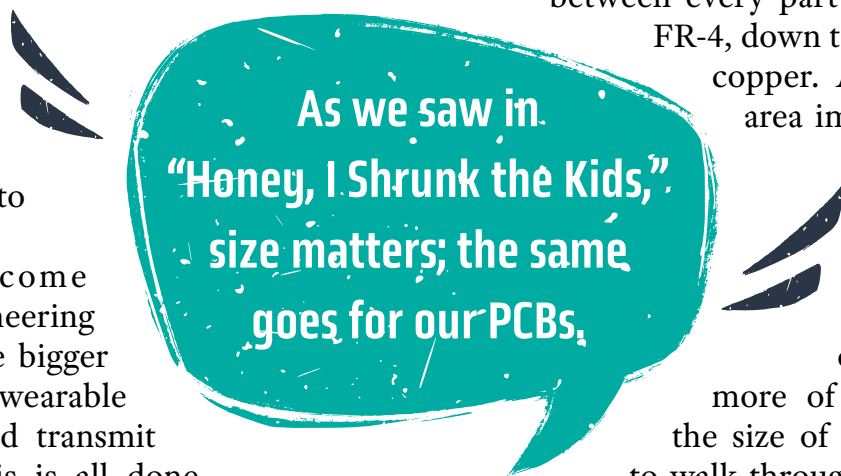
Serendipity refers to the occurrence of unexpected and fortunate events or discoveries by chance, often while searching for something unrelated. But a principle known as "designed serendipity" refers to the deliberate creation of conditions or environments that increase the likelihood of serendipitous discoveries or opportunities.

That, in its basic form, is a PCB. We are creating an environment where the forces of energy are controlled in a specific way. Over the years, I have changed how I look at PCB design. It's not just "connecting the dots." Instead, there is a fascinating interconnection of the various parts of the design. There's an intricate balance between every part of the PCB, the FR-4, down to the grain on the copper. A change in one area impacts others differently. Like dominoes, the other areas are impacted when one is tipped over. Nothing has more of an impact than the size of the PCB. I want to walk through a scenario that explains what happens when we reduce the PCB size.

Form, Fit, and Function

As we know, wearable medical devices often need to be compact, lightweight, and comfortable. That requires designing PCBs that fit within the limited space available and conform to the shape of the wearable device.

Getting everything into a device requires using unique solutions and miniaturization techniques, much like the old joke about squeezing 10 pounds of "stuff" into a five-pound bag. First, just using smaller components like 1005s for your discretes will not cut it. You



will need what I refer to as the “all of the above” approach. You will most likely use advanced packaging components, system-on-chip (SoC) integration, microcontrollers, sensors, integrated circuits, or even ultra HDI, giving more functionality in a smaller package. These components occupy less space on the PCB, allowing for a more compact design.



We have seen that a smaller area means smaller components and overall PCB space; trace routing is our next challenge.

PCB Considerations

With wearable electronics, size matters, and the dominoes begin to fall. Using a conventional 0.062” PCB is probably out of the question, and FR-4 is not an option, strictly due to space requirements. This is why one of the fastest growing areas in the PCB industry is flex and rigid-flex. Flex and rigid-flex are often the only solution to meet the complexity of some of these devices. There is a direct correlation between the rise in wearable/medical devices and the increase in rigid-flex circuits. It’s not a matter of if you will ever do a flex design, but when.

We have seen that a smaller area means smaller components and overall PCB space; trace routing is our next challenge. Designers must use smaller trace widths and spacings to accommodate more routing channels, and inner layers for routing to maximize the routing density. That requires using microvias to create additional routing layers. With that, another domino falls, and smaller traces have higher resistance. That can lead to increased voltage drops and power losses, affecting signal quality and power delivery. This will introduce higher impedances, making controlled impedances more difficult.

Reducing the size of the PCB impacts the entire design: component sizes and routing impact the signal integrity and EMC/EMI. Power management is another consideration since these are battery-operated devices. Efficient power management is essential to maximize battery life while providing adequate power to the various components. That involves designing power-efficient circuits, implementing low-power modes, and optimizing the power supply network.

How small can we go?

A Canadian company, Precision NanoSystems, is answering that question with the creation of nano-



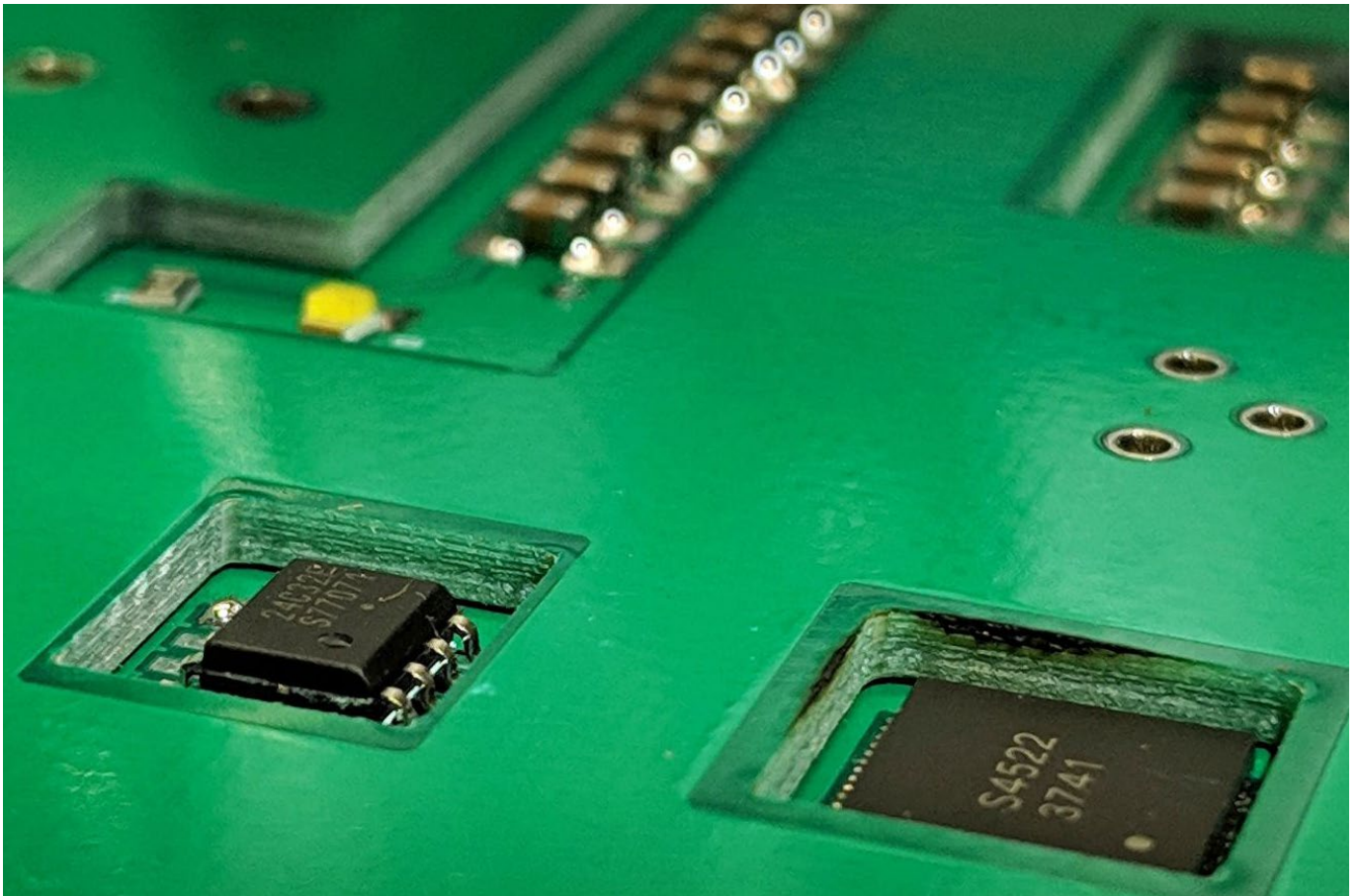
technology directly out of another sci-fi movie, “Fantastic Voyage,” released in 1966.

To save a scientist, a submarine is shrunk to microscopic size and injected into his bloodstream with a small crew. That is now nearly a reality, with nanotechnology that can navigate the human body—injecting medicine directly into a tumor, for example.

Honestly, where can this technology go? In my opinion, anywhere our imaginations will take it. **DESIGN007**



John Watson, CID, is a customer success manager at Altium. To read past columns, [click here](#).



Designing Cavities to Reduce Skyline

Feature Article by Kris Moyer

IPC

With the increasing shrinkage of modern electronics in both board size and product volume, it's becoming more difficult to mount components to the PCB surface and still meet volumetric requirements. To avoid chip-on-board (COB) processing, board cavities can help mitigate the Z-axis skyline volumetric issues and allow for components that would otherwise not fit within the skyline to be used.

As the name implies, a cavity is the removal of some of the board material to expose traces and contact pads on inner layers of the PCB. This is done to allow attachment of the component to these exposed pads rather than pads on the surface of the PCB (Figure 1). To form

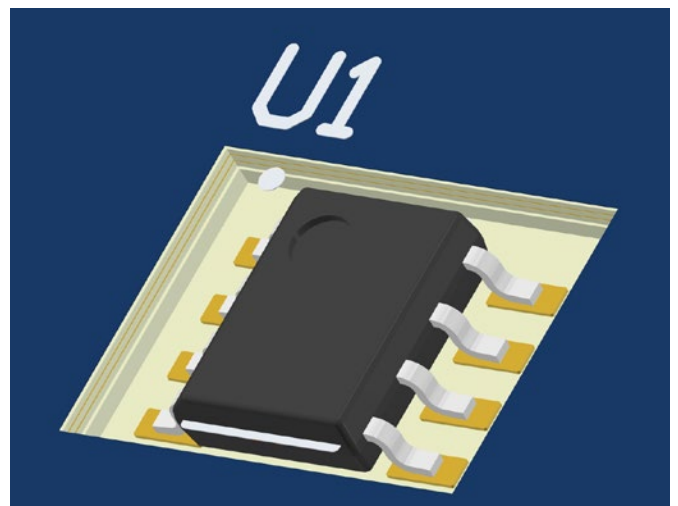


Figure 1: A typical cavity as it appears in an ECAD software tool.



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One long-standing sustainability slogan is “think globally, act locally.” Siemens predictive analytics expert, Jonathan Fromm, introduces us to the “eight R’s” of sustainability in the sixth, and final, episode of this series from *On the Line with...* brought to you by I-Connect007.



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cavities, several special processes need to be considered. Among these are inner layer plating, particularly the effects of plating and surface finish on inner layer impedance for signal integrity; sequential lamination; surface finish on exposed inner layer pads; and the use of controlled depth milling to form the cavity, just to name a few.

One of the first items of concern is the effect of plating and surface finish on impedance of the inner layers. When cavities are formed without sequential lamination, the plating and surface finish needed to support the soldering process will add conductive material thickness to the exposed areas of the inner layer. This in turn will cause an impedance discontinuity due to these different thicknesses of the traces.

Additionally, the removal of the reference planes from one side of the conductor changes the structure of the transmission line from a stripline on inner layer to a microstrip in the cavity. Most ECAD and SI tools do not support different transmission line structures on the same layer of the board. There are some solutions to this conundrum: Rather than relying on the built-in transmission line structures of ECAD tools, the designer can manually calculate the controlled impedance trace widths for the stripline and microstrip sections and then use area constraint rules to define the widths both in the cavity and on the remainder of the layer.

One possible way around this issue is to use sequential lamination to allow plating on the entire layer. But sequential lamination poses its own problems. First, it is a more costly and time-consuming process. Second, it adds fabrication allowances. It may also require the use of blind and/or buried vias to make the connections between layers. The multiple plating cycles needed for sequential lamination can cause other fabrication issues. It is recommended that the fabricator be consulted on any sequential lamination PCB design.

Other design challenges exist in the formation of the cavity using milling methods. One of these is the need for a large radius on the

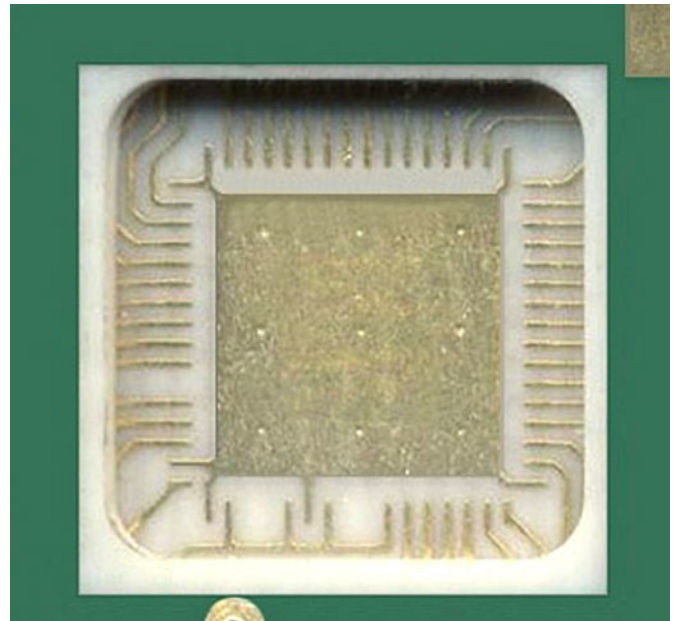


Figure 2: A view of a cavity showing radiused corners from milling process. (Image credit: Saturn Electronics)

inside corners of the cavity. In Figure 1, you can see a simplistic view of the cavity from the design tool. In Figure 2, you can see what the cavity will need to look like with the radiused corners from the milling operation. Design tools can define these inside radii; however, the fab shop should be consulted to determine what the appropriate radius needs to be for cavity formation. One way to avoid completely milling out the area of the cavity is to pre-form the prepregs, cores, and copper foils. Figure 3 shows an example of what the pre-formed

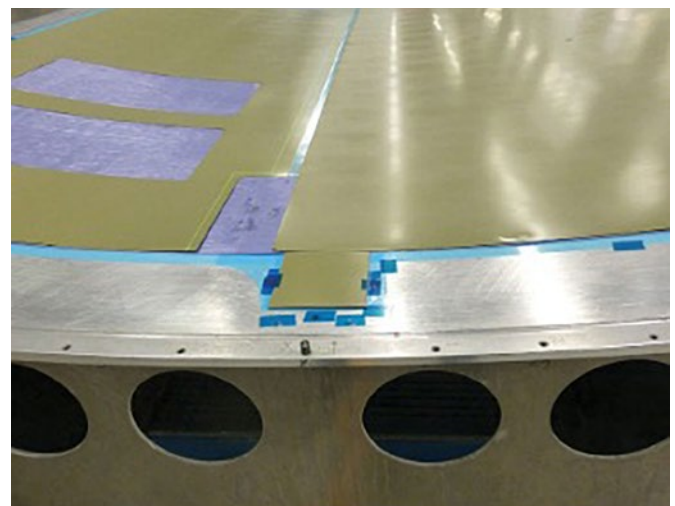


Figure 3: Cavity created with pre-formed prepreg.

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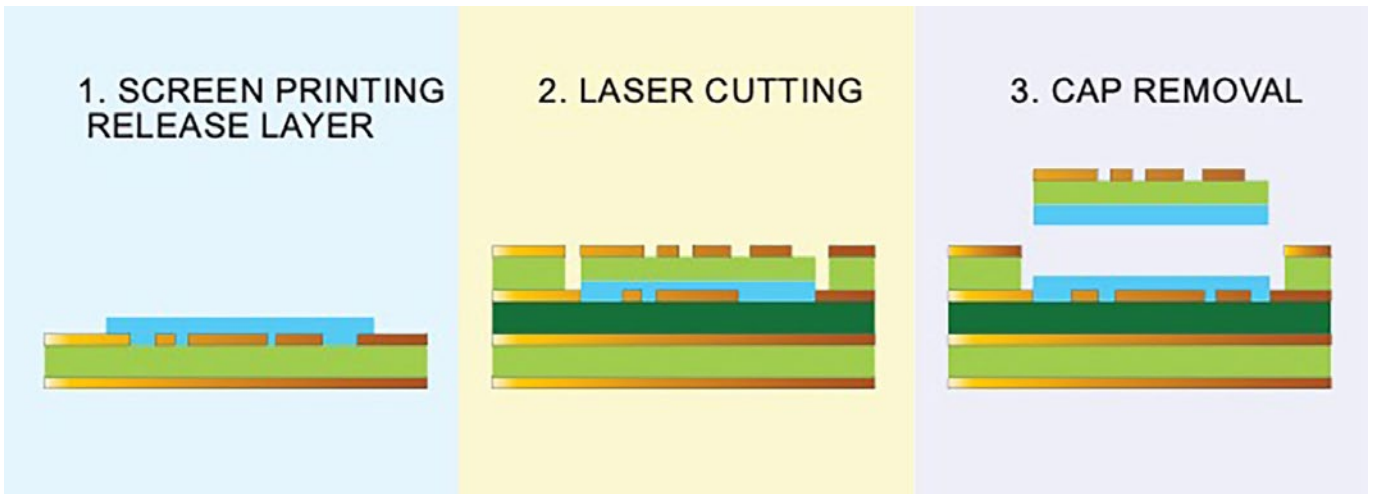


Figure 4: The steps for creating a cavity by using laser drilling to remove a plug of material from the board.

pregreg might look like. This technique will require more careful layer alignment during fabrication but will require only minor milling or cleanup of the cavity edges rather than complete material removal.

A newer technique has been developed for the formation of a cavity in the PCB. This technique involves the use of a release film being applied to the area of the inner layer where the cavity is to be formed. The board is then fabricated in the usual single lamination process. After lamination, laser drilling methods are used to define the perimeter of the cavity. Finally, the plug of material is removed from the board and the cavity is cleaned to remove any residue from the release film before surface finish is applied. This technique requires careful alignment of the layer and release film.

Additionally, accurate alignment of the laser cutting of the plug is necessary to assure no release film is left in the board that might cause issues like delamination or moisture ingress, but also close enough to the release film to allow plug removal without fracture or other damage to the remaining board material. Figure 4 shows an example of this process.

The final area of concern with cavities is in the assembly process. The placement heads in pick-and-place machines in modern assembly lines feature controlled depth travel. For cavi-

ties, this depth needs to be altered to ensure that the part is fully inserted into the cavity and not released at the regular board surface and allowed to fall into the cavity. This will require more complex and careful programming of the pick-and-place equipment and may need additional fiducials or other alignment methods to ensure proper placement.

Another area of difficulty in the assembly of cavity parts is the application of solder paste. Due to the depth of the cavity, the use of traditional paste screens for the cavity is not possible. This will require the use of direct paste printing or manual paste application in the cavity.

While there are several challenges to the use of cavities, with careful planning and consideration cavity can be an excellent solution to packaging challenges in modern electronic designs. **DESIGN007**



Kris Moyer, CID+, is a certified master designer and an IPC instructor.

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Playing the ISO ‘Game’ for Better Quality

Connect the Dots

by Jamin Wilson, SUNSTONE CIRCUITS

If someone asks at your next backyard barbecue, “How is work going?” it might not be gripping to say, “I am improving processes to realize efficiencies based on the ISO 9001 framework.” Unless, like me, they are also an ISO nerd. While that’s what I’m doing at work, perhaps a more engaging answer would be,

“We have turned quality improvement into a game that everyone on the production team can participate in.”

Our ISO game turns every production order into a gaming token. Each token generates scores of “on time” and “quality” for every system it passes through.



Figure 1: Our ISO “game” turns every production order into a gaming token.

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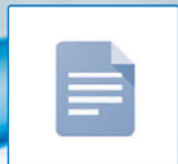
Verify

Ensure that manufacturing data is accurate for PCB construction.



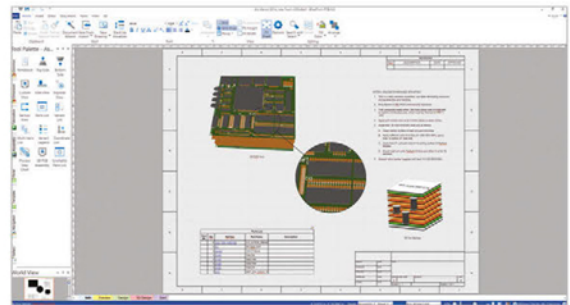
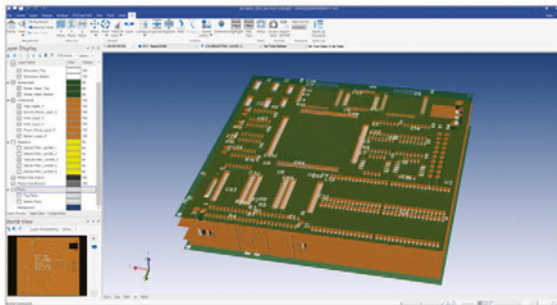
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The sum of the scores from each department is tallied at the end of production to calculate a combined score. Each department, shift, and participant are continually challenged to find ways to increase token scores. Our game complements the competitive elements of human nature, whether between different shifts or neighboring departments. The ultimate goal is to improve the system itself, providing everyone with a common goal, and allowing for a friendlier environment, while at the same time improving on-time deliveries and producing higher quality boards.

That's right. We have been gamifying our ISO initiative. Gamification is an extremely useful methodology for companies needing to train new knowledge and skills. It is also used successfully for career development, early group learning, and continuing education. It makes the work more fun and, I believe, makes our business more efficient and our products higher quality.

After 20 years as a lab technician, I moved into administering the quality management systems (QMS). That meant I became the ISO point person. My job is to continue the ongoing

improvement that has been integral to our company's success with ISO.

Commitment to ISO Leads to Improved Results

ISO and QMS should be more than a badge on the company website. ISO certification tells the marketplace that your company has created a system that drives continuous improvement of production output.

Even when the QMS functions well and there exists a quality-focused culture, that does not mean it is time to turn on the autopilot. Use the ISO framework to pursue truly continuous improvement. As Jeff Bezos said about developing a space program, we intend to work "step-by-step, ferociously."

Step-by-step is a great model for our work in building custom PCBs for clients. It is a step-by-step process; a PCB board build goes through multiple systems on our factory floor, from masking and plating to drilling and shipping.

ISO 9001 is a lens to look at the work. Each step costs in time and expense. Each team works in a specific area, taking in a job from

Annual Corrective Action Reports

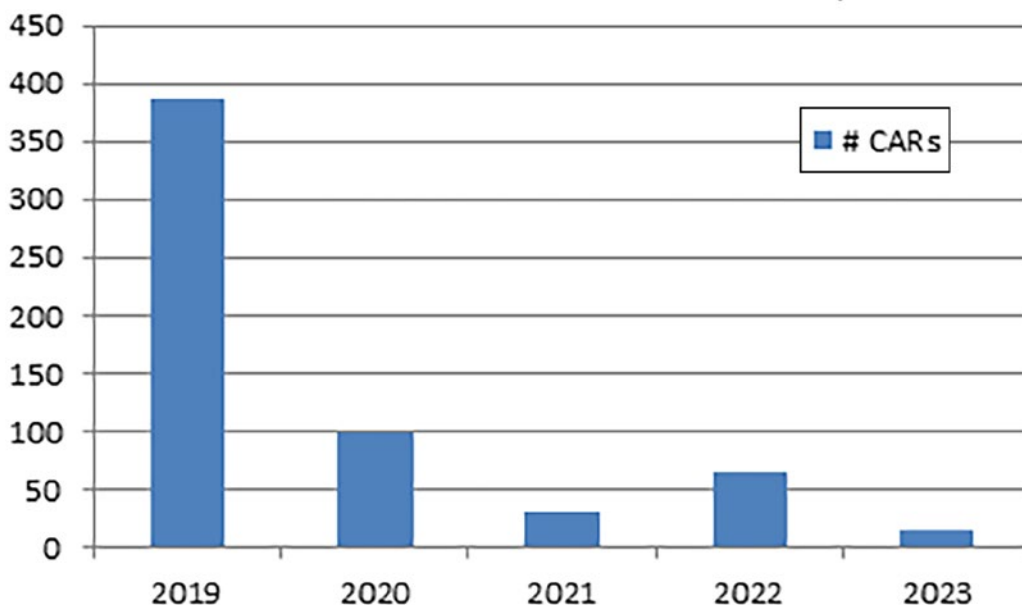


Figure 2: Annual report showing how ISO 9001 adoption led to a reduction in corrective actions. Corrective Action Requests (CARs) are a root cause analysis of a production problem that has occurred.

the previous stage and performing their task, then handing it off to the next.

With ISO, No Cheat Codes

Once we have the systems set up and scored, we bring in the experts. Not outside experts, but the people who work every day on the factory floor on these questions. The teams that operate each process are our experts and have developed all the innovations of our QMS. They are far more familiar with their process than I am. The game helps to train them in ISO and practice in a more engaging way, which helps us as a team consider how changes would affect the process.

For instance, quality checks are a necessary part of manufacture, but they have a high cost. It is expensive to do constant quality checks and does not add value to a functioning board. However, the sooner a failure or error is identified, the less wasted work—tokens—we will spend on that board. Using the game, we can visualize what happens when we move a quality check. The game helps us ask, “Does the increase in time and expense pencil out to more efficiency and better quality?”

When it comes to generics, there is even more potential for variance.

Visualize, Discuss, and Improve

The game is a way for us to look at our system and see how their expertise can find ways to improve. Are quality checks in the optimal place? Is there redundancy? Could we reduce some of the steps?

Any organization that has been successful with ISO will tell you that this is the key: bringing the team together to visualize and refine their work. The game makes that easier and more fun so we get our creative juices flowing. Not only that, but we can also see the results in a measurable way: more tokens.

We have only been using the game for a



Figure 3: An example of our game “tokens.”

short while. It has created more interest and increased momentum in our ISO work. It gives people the buy-in and a global vision of how their work impacts the other aspects of our business. We have animated discussions about maintenance, the supply chain, and the other wraparound efforts that impact the business with the same abstraction of tokens expended. It gives flight to our collective purpose. The accumulated wisdom of the team captured with the game then forces action by leadership. The measure of tokens makes it easy to communicate the impact of proposed changes.

ISO initiatives are ripe for gamification, and we are really happy with how it has energized our initiatives. Maybe soon team members will be working to get on a leaderboard of tokens saved. **DESIGN007**



Jamin Wilson is quality systems administrator at Sunstone Circuits.

Standing Waves in Multilayer PCB Plane Cavities

Beyond Design

Feature Column by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Plane cavities in multilayer PCBs are essentially unterminated radial transmission lines. They form a transmission line that propagates electromagnetic (EM) energy within a plane cavity emanating from a feed point within the plane and outward in all directions. Like all transmission lines, it will reflect if not terminated. This creates standing waves—ringing. The bigger the mismatch, the bigger the standing waves, and the more the impedance will be location-dependent. As frequency and edge rates continue to increase, the impact

of intrinsic electrical characteristics becomes more pronounced. AC switching currents in the power/ground planes can be very large. Under these circumstances, a plane pair acts more like a radial transmission line rather than a distributed planar capacitor.

A parallel plate capacitor (or a planar pair) has two conductors separated by a dielectric layer. Most of the electromagnetic energy in the structure is concentrated directly between the plates. However, some of the energy radiates into the area outside the plates. The elec-



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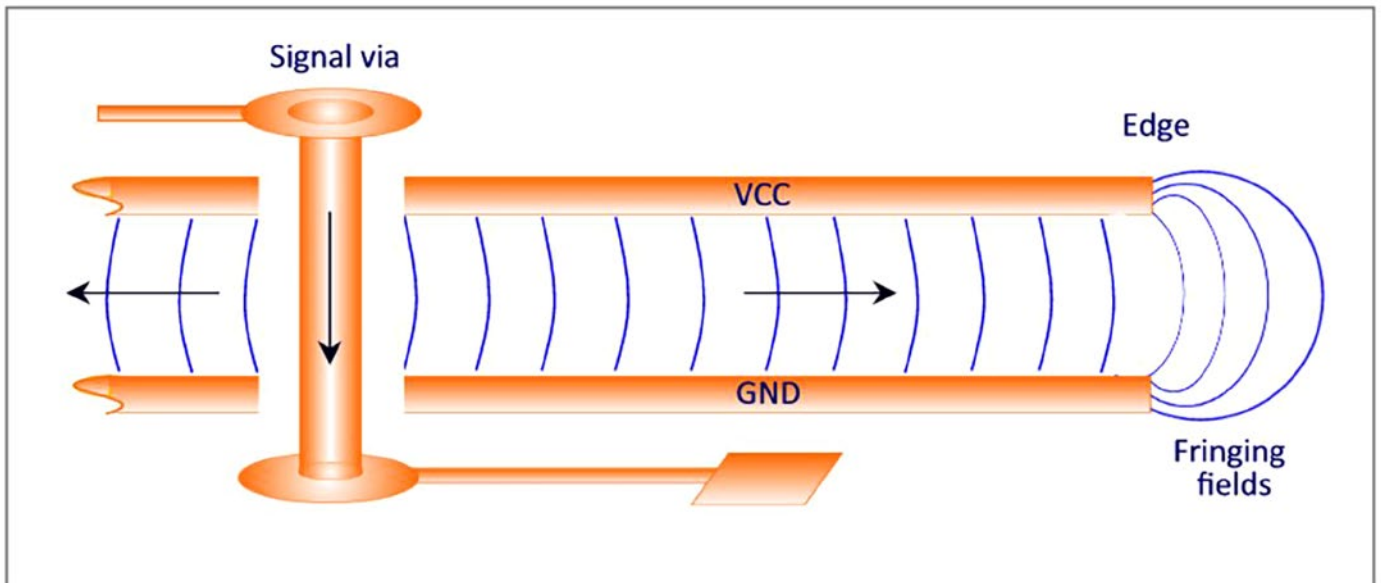


Figure 1: Signals passing through a plane cavity intensify fringing fields.

tric field lines associated with this effect are called fringing fields (Figure 1).

When displacement current flows through the impedance of a cavity between two planes, it generates voltage. Although quite small (typically in the order of 5 mV), the accumulated noise from simultaneous switching devices can become significant. This voltage, emanating from the vicinity of the signal via, injects a propagating wave into the cavity, which can excite the cavity resonances or any other parallel structure (for instance, between copper pours and planes). Other signal vias also passing through this cavity can pick up this transient voltage as crosstalk. When the wave meets the PCB edge, the two reference planes form a slot antenna that will radiate noise with the potential to generate electromagnetic interference (EMI) to nearby equipment.

The more switching signals that pass through the cavity, the more noise is induced into other signals. It impacts vias all over the cavity, not just the ones in proximity to the aggressor signal vias. This cavity noise propagates as standing waves spreading across the entire plane pair. This is the primary mechanism by which high-frequency noise is injected into cavities: by signals transitioning through cavities, using each plane successively as the signal return path.

Cavity resonance also affects the power/signal return layers at the edges of the PCB. Edge effects can be particularly problematic since it is the board edges that are in such proximity to the chassis and, hence, the radiation fields can induce currents into the chassis frame.

When the cavity has open-end boundary conditions, resonances arise when a multiple of half wavelengths can fit between the ends of the cavity. If the clock or data harmonics overlap with the cavity resonant frequencies, there is the potential for long-range coupling between any signals that run through the cavity. This is one reason why all return planes should be GND layers, so that stitching vias between GND planes can be placed adjacent to each signal via transition to minimize the possibility of exciting the cavity resonance. Figure 2 shows a standing wave produced by the superposition of two harmonic waves of equal amplitude, frequency, and wavelength moving in opposite directions.

A region under a large BGA densely populated with vias also appears as a discontinuity due to the large array of anti-pads eating a hole in the plane. A discontinuity reflects propagating energy because it represents a mismatch with the characteristic impedance of the transmission line.

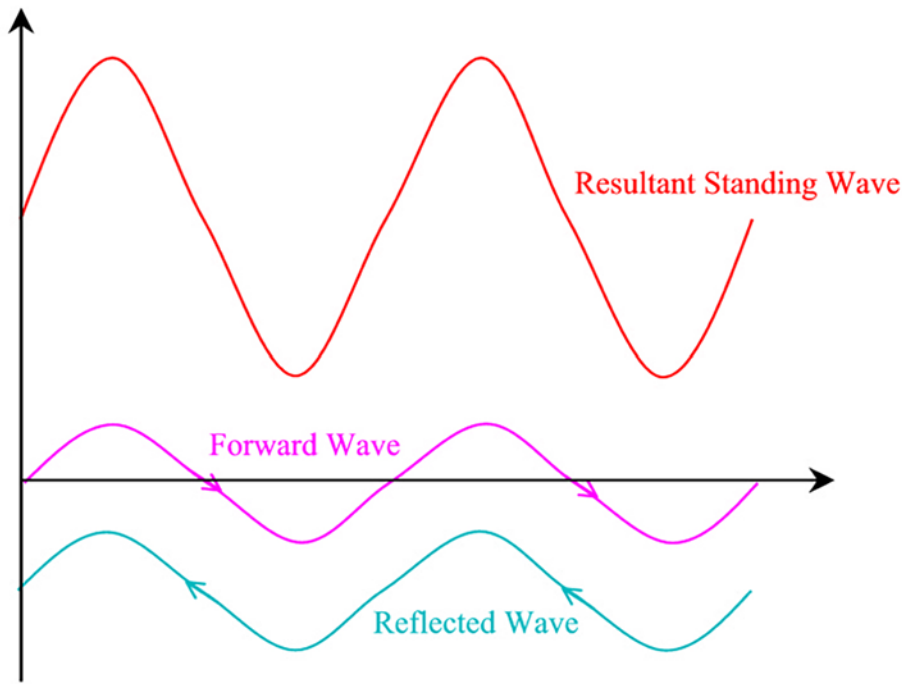


Figure 2: Standing wave is the superposition of two harmonic waves.

The edges of the board cause the greatest amount of reflection since an edge is a totally abrupt open circuit surrounding the board. Reflected energy is accompanied by phase reversals in its components, and combined reflections from the open circuit at the edge of the board can cause a phenomenon known as voltage doubling, creating a standing wave. The standing wave appears to be vibrating vertically without traveling horizontally.

There are various approaches to reducing radiation edge effects from the PCB. In many cases, energy can be reflected, possibly creating additional internal cavity resonance effects and coupling to internal vias, and resulting in increased radiation. When plane pairs resonate, their emissions come from the fringing fields at the board edges. With ground/power plane pairs, edge-fired emissions can be reduced by reducing the plane separation and lowering the AC impedance. Alternatively, make the power planes slightly smaller (~200 mil) than the GND plane. This modifies the pattern of the fringing fields, pulling them back from the edge, and may help reduce emissions to some extent.

Edge plating, as the name suggests, is the process of plating the edges around the PCB. This is an elegant (but expensive) solution to prevent emissions from extremely high-speed SerDes signals on terabit routers, etc., but is an over-kill for a typical high-speed design.

Another way to mitigate this problem is to create a via fence, stitched to ground around the perimeter of the PCB. If the spacing between the stitching vias is less than or equal to $1/12$ th of a wavelength, the via fencing will appear as a short circuit,

causing the propagating wave to be reflected back to the source rather than being launched from the PCB edge. Unfortunately, most of the above techniques create reflections and possibly exasperate the issue.

Parallel planes in multilayer PCBs exhibit multiple resonances, which increase the impedance and the EM radiation. A typical FR-4 laminate of 4-mil thickness produces a characteristic impedance of about 3 to 5Ω for adjacent planes. The larger the plane area, the lower the impedance.

The best solution to dampen the plane resonance is to terminate the transmission line with an impedance-matching resistive element along the board edges. But in practice, this means approximating a continuous structure with resistors spaced around the perimeter. Obviously, multiple low-value resistors cannot be placed directly between the power supply and ground as it would needlessly dissipate a huge amount of DC power. To prevent this, they should be AC coupled with a ceramic capacitor of sufficient capacitance to allow the resulting impedance to appear predominately resistive at and above the lowest frequency of

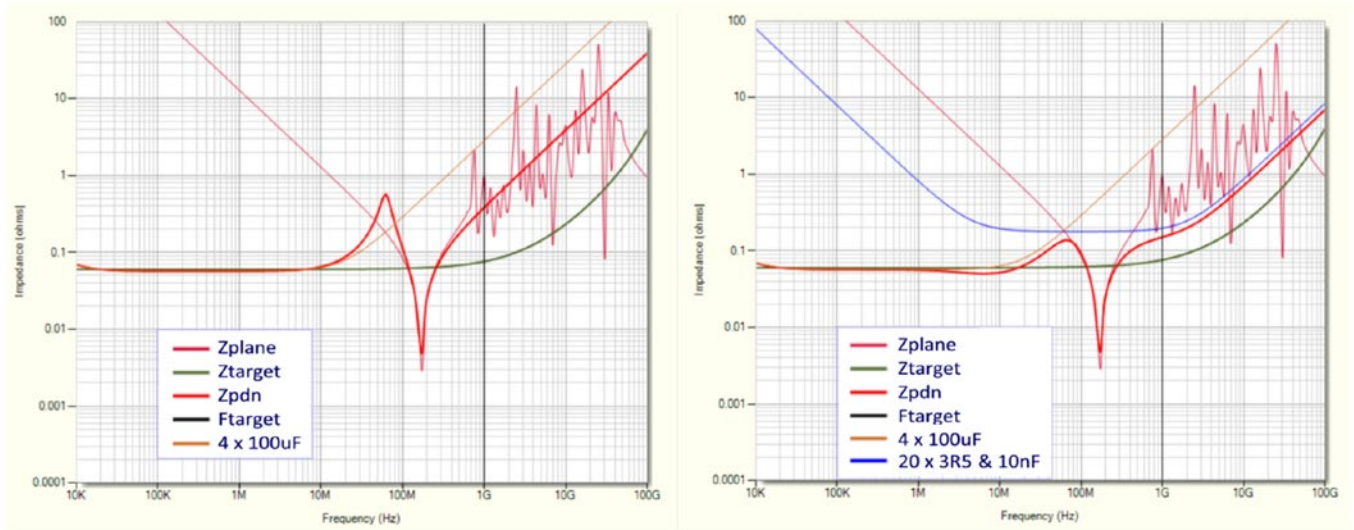


Figure 3: a) Zpdn with 4x100uF; b) Zpdn with added RC damping. (Source: iCD PDN Planner)

interest. A 10nF, X7R ceramic capacitor is a typical value. The addition of loss to dampen modal resonances is more important than the exact termination value and distribution. Notice how the 20-series RC terminations of 3R5Ω and 10nF (blue) dampen the plane resonance, pushing the effective PDN impedance (Zpdn) down below the resonance, above 200MHz (Figure 3b).

A standing wave can be generated at switching locations within the interior of the PCB. Therefore, there may be hot spots within that cavity that would benefit from the placement of an additional AC-coupled load at or near the source.

Reflections occur in a transmission line only when there is a discontinuity. If the edge of the board is terminated in the characteristic impedance of the radial transmission line, then the EM energy will be absorbed and there will be no reflections. This will not eliminate the initial transient but does, however, prevent it from being compounded. Termination elements inhibit standing waves from developing between the planes and protect peripheral signals and electronics from radiation.

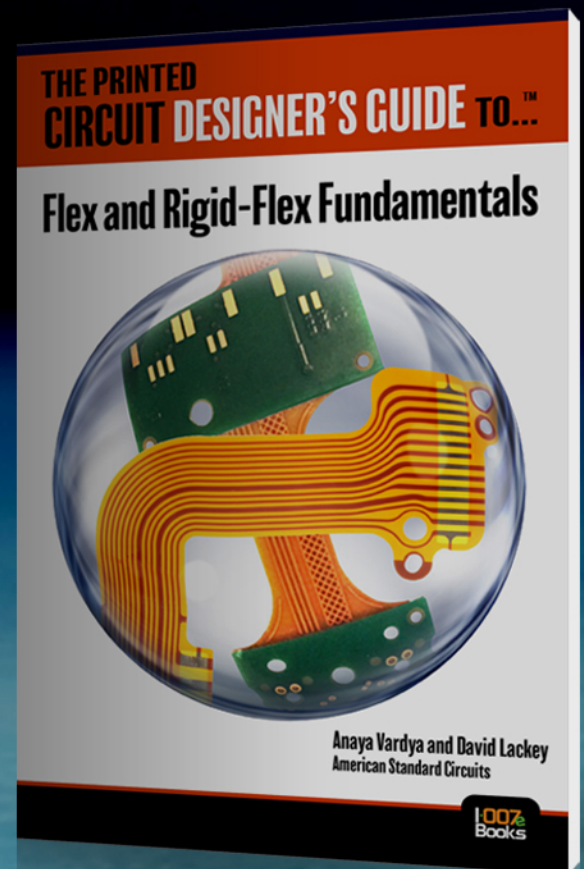
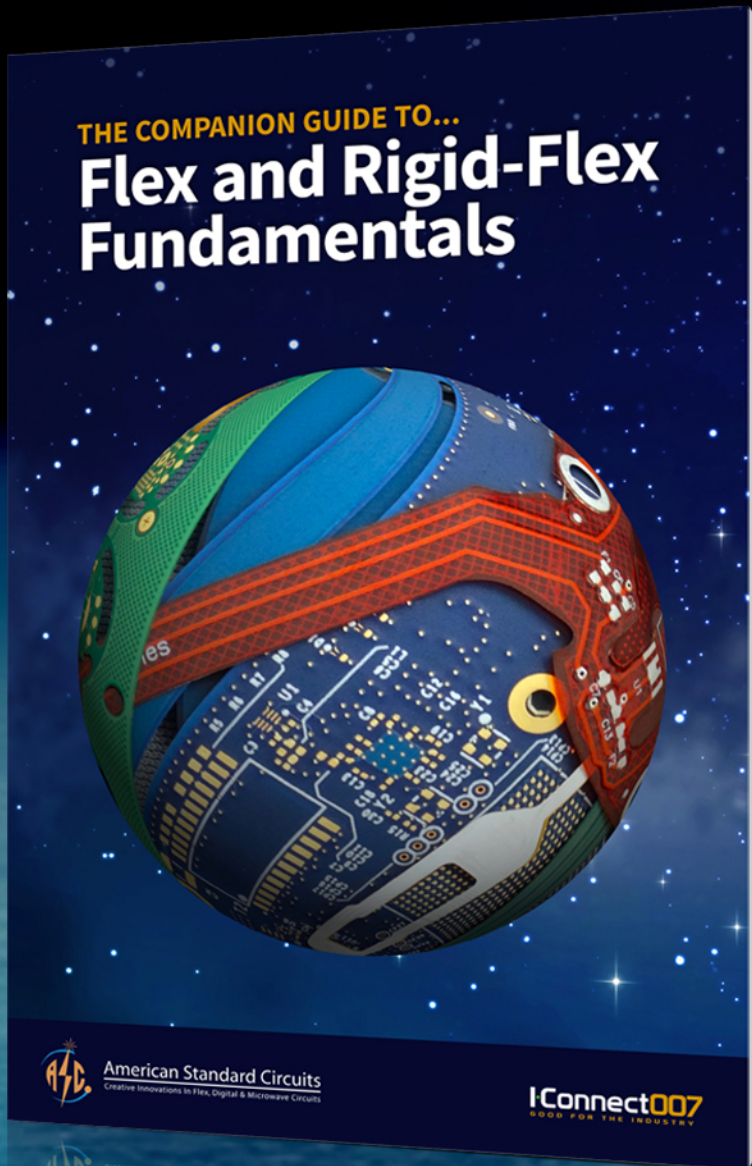
Key Points

- Plane cavities in multilayer PCBs are essentially unterminated radial transmission lines that will reflect if not terminated.

- The energy that radiates from the edges of the plane pair is called a fringing field.
- When displacement current flows through the impedance of a cavity between two planes it generates voltage.
- Signal vias passing through a plane cavity can pick up the transient voltage as crosstalk.
- A standing wave is produced by the superposition of two harmonic waves of equal amplitude, frequency, and wavelength moving in opposite directions.
- Standing waves impact vias all over the cavity, not just the ones in proximity to the aggressor signal vias.
- All return planes should be GND layers, so that stitching vias between GND planes can be placed adjacent to each signal via transition to minimize the possibility of exciting the cavity resonance.
- A region under a large BGA densely populated with vias also appears as a discontinuity due to the large array of anti-pads eating a hole in the plane.
- The edges of the board cause the greatest amount of reflection since an edge is a totally abrupt open circuit surrounding the board.
- The standing wave appears to be vibrating vertically without traveling horizontally.

Take your flex game to the next level

This guide provides additional insights and best practices for those who design or utilize flex and/or rigid-flex circuit boards.



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Books

- Parallel planes in multilayer PCBs exhibit multiple resonances, which increase the impedance and the EM radiation.
- The best solution to dampen the plane resonance is to terminate the transmission line with an impedance-matching resistive element, along the board edges. **DESIGN007**

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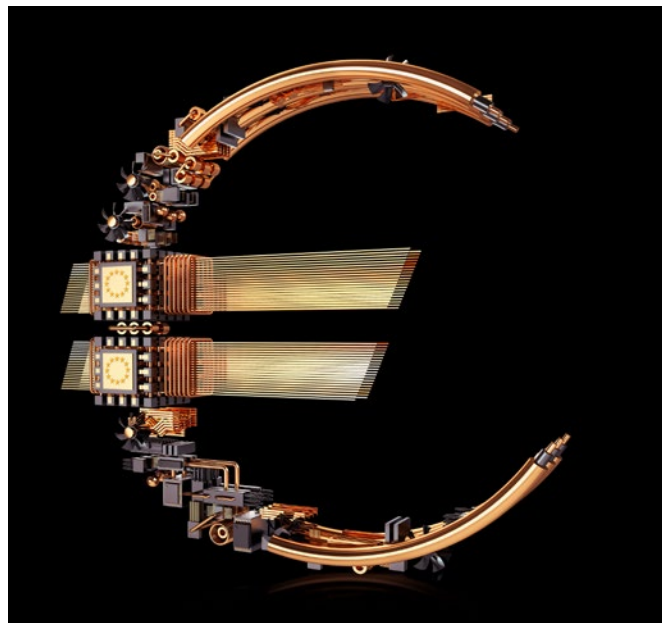


Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns, [click here](#).

Toward a European Chips Act

By **Alison James**, IPC senior director, European government relations

While the U.S. government has begun to implement its CHIPS and Science Act, the European Union is deliberately moving to issue its own legislation. Rising geopolitical tensions and the supply chain vulnerabilities exposed during the height of the COVID pandemic, followed by the Russian invasion of Ukraine, accelerated a move in the European Union now happening throughout all



global regions: taking stock of strategic assets and vulnerabilities.

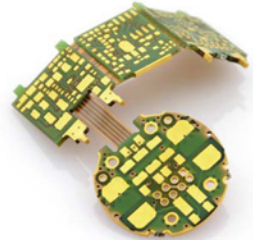
Electronics and data, it seems, are the “oil” of the 21st century, and the high strategic importance of both elements focuses efforts to secure supply by building regional bases for high value-added activities and intensifying cooperation with strategic trading partners.

The European Union’s proposal for legislation regarding semiconductors was issued in February 2022 against the backdrop of global chip shortages, a global “subsidy race” in the world’s main producing regions, and a renewed EU industrial policy aiming to deliver on the bloc’s ambitious digital and green transition. It is part of the region’s evolving “strategic autonomy” agenda: reducing the continent’s vulnerability to supply chain disruptions and geopolitical risks. At this time, the proposed legislation is in the final months of negotiation in the inter-institutional process under which European legislation is formed.

With announcements of confirmed and rumored investments by well-known chip companies, it’s clear that a leading intention behind the European Chips Act is to attract high-end semiconductor manufacturing to produce the most advanced chips.

To read the rest of this article, which appeared in the Spring 2023 issue of *IPC Community*, [click here](#).

Focused on Flex

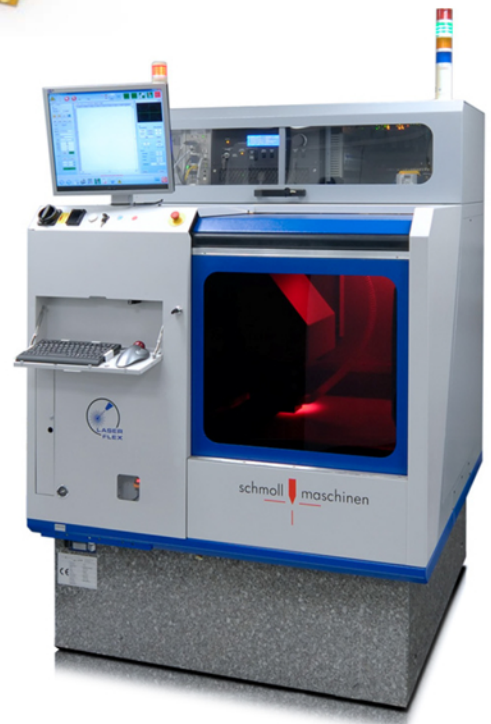


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Rough Roughness

Reasoning

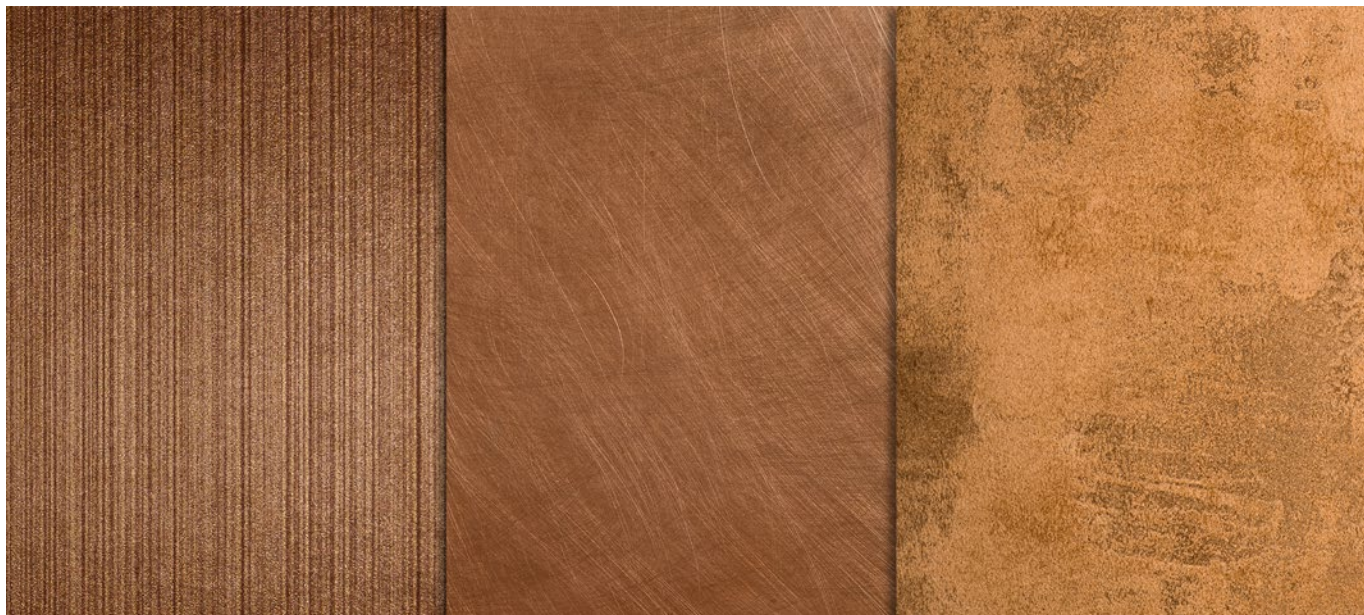
The Pulse

Feature Column by Martyn Gaudion, POLAR INSTRUMENTS

Reliable bonding reduces the risk of delamination through thermal stresses. The tried-and-tested way of achieving a good, reliable bond is to ensure that the copper is sufficiently rough to promote adhesion to the epoxy resin in the prepreg material. As materials and bonding technology improves, the copper surfaces can be made increasingly flatter and still achieve the desired reliability. In the future, new bonding methods—some already here but still on the high-priced side of the equation— may allow extremely flat copper to bond reliably. Meanwhile, as the industry is heading down the road of “smoother” copper, there is still a need to model the effects of a rough surface on signal transmission.

Models and Methods

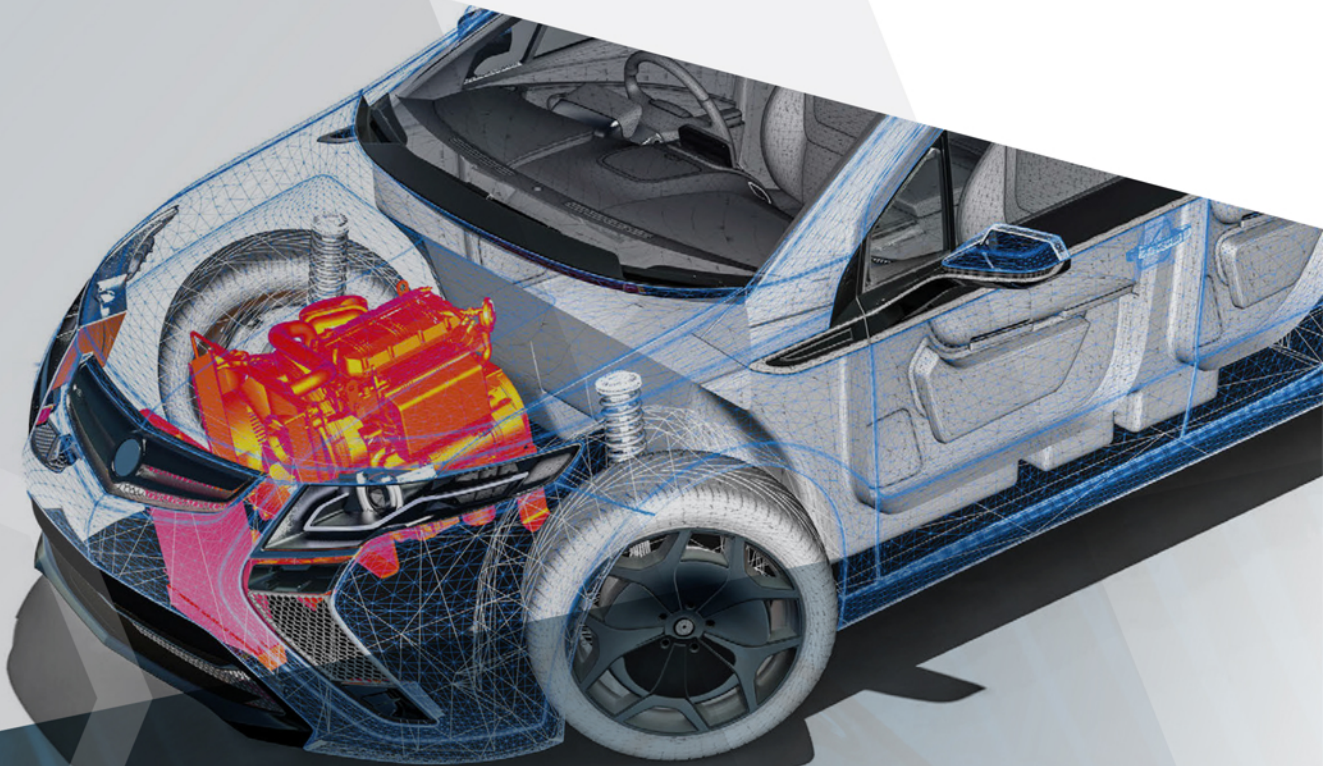
There are four or five primary methods for modelling signal losses owing to roughness, depending on how you interpret them. Hammerstad and Grosse are legacy methods, but still valid at the low GHz range. Hammerstad was developed around World War II to calculate the losses caused by machining grooves in early radar systems. Grosse extends the frequency capability a little higher. But if you are pushing into the high GHz, then these legacy models soon start to saturate, and they will both underpredict the contribution that surface roughness makes to loss. Newer methods (of the last decade or two) perform to much higher frequencies and correlate well with measurement systems.





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Huray modelling describes the dendritic surface of the copper as small pyramids of copper balls. Using a scanning electron microscope (SEM), the SI engineer can enter the ball count, area, and number of balls in area to prime the Huray model. If this seems a little tedious and only for academics with time on their hands, there is a welcome answer. Bert Simonovich of Lamsim Enterprises has a paper which describes a preprocessor which takes the matte and drum side's Rz roughness measurement and, as if by magic, generates a set of Huray parameters. This saves us a lot of time and effort with analysing SEM images.

The second relatively recent method for modelling is the gradient method. Its authors propose that rather than model the detail of the surface, that the interface between the copper and the dielectric be treated as a gradient where the characteristics blend from pure conductor to pure dielectric over the RMS

(Rq) roughness of the surface. Papers on the gradient method propose that not only does this model help the effects of roughness on loss but also takes quite good care of the effects of roughness on phase.

Are You a Snowball or a Ski Slope?

The two modern methods take a different approach to roughness modelling with Huray comparing and modelling the surface topology as small stacks of snowballs (further simplified by Bert Simonovich with his Cannonball Huray method). The gradient method offers a "ski slope" down from the pure conductivity of copper, through a blended zone of decreasing conductivity, until the rough surface ends in pure dielectric material. Huray takes data analysed from an SEM to model the roughness. The Cannonball method uses commonly available Rz roughness data, and the gradient method uses RMS (Rq) roughness data.

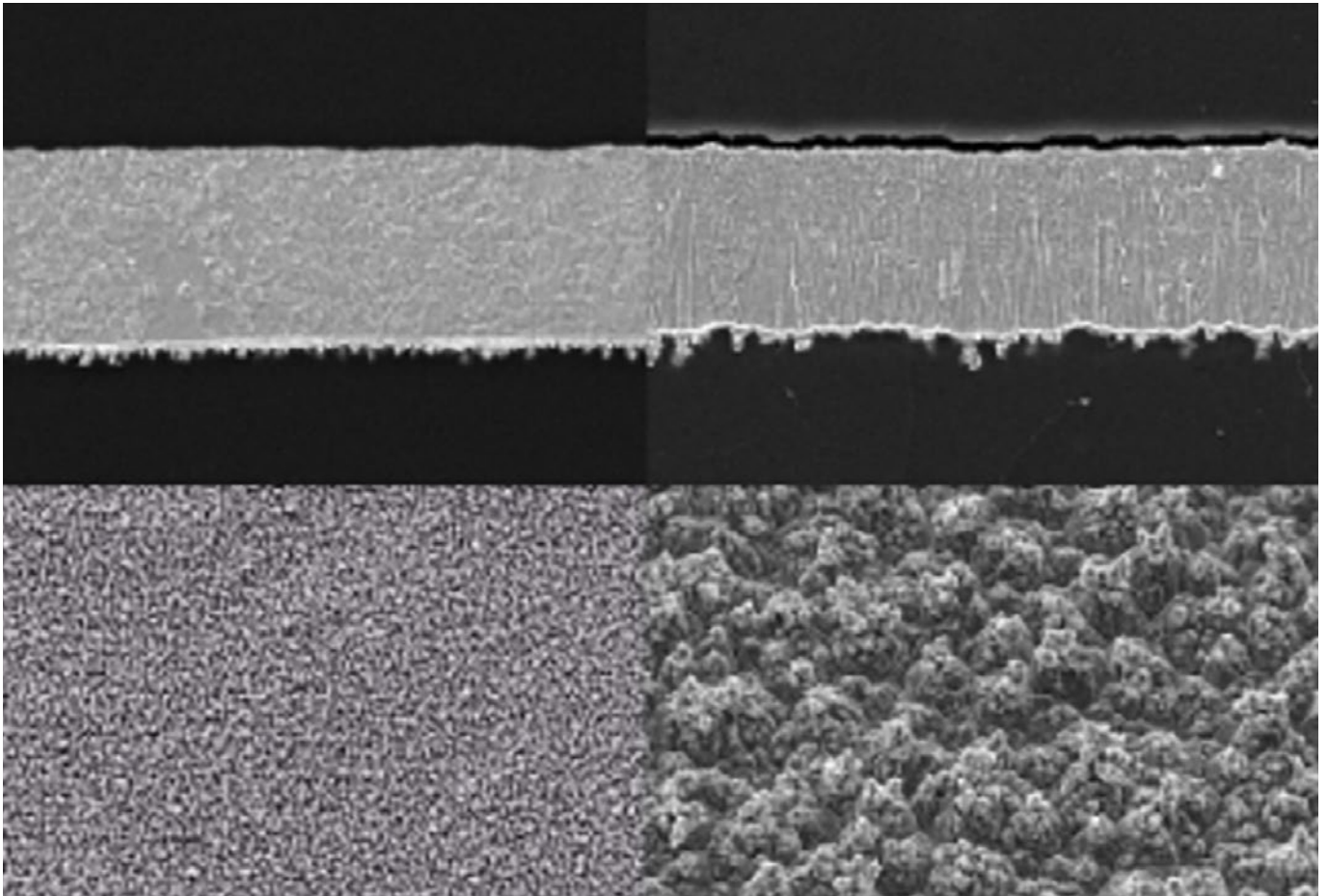


Figure 1: Smooth and rough copper. (Source: Circuit Foil)

Roughness Not Just a Number

RMS Rq Rz Rz (ISO), Rz(DIN), Rz(JIS), and a myriad other roughness metrics reveal a minefield of complexity to the SI engineer who may just ask, “How many microns of Cu is the roughness on this foil?” What is important is that the methods mentioned are modelled using specific roughness metrology, and there is no trustworthy conversion from one to the other. You may find some articles that say something like, “In a limited number of circumstances a conversion is possible,” but it is prone to error and pitfalls. So, the bottom line is to use the gradient method; you need to use RMS (sometimes called Rq) roughness. For the Cannonball Huray, use Rz (DIN or JIS). There is good reason for the variety, as in mechanical engineering you may be looking at a certain roughness to hold lubricant on a bearing or cylinder surface, or the measurement may simply be one of process control.

The OEM Rules

Regardless of the method you would like to use, or you feel is best for your application, if an OEM is specifying a particular model then you had best stick to that. It's fine to compare with other methods, but for product qualification, if the OEM is using roughness model “A,” then that's the choice made for you.

Future Directions

You may have noticed earlier in the article that with improvements in resin systems and copper surface pretreatments, that profiles are getting smoother. Over time (and we are not there yet), the need for roughness modelling will ease.

A Little Knowledge is...

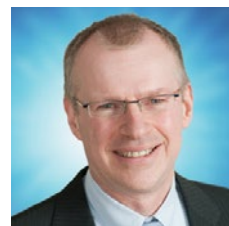
...a dangerous thing, as the saying goes. Whilst roughness data may be readily available from your foil or laminate supplier, remember that depending on where the material is in the stack, it is likely to undergo further treatment or plating on drill end layers. Not only do you need to have material data, but also stackup information on how the fabricator further treats it before bonding is valuable to form a complete picture.

Conclusion

Whilst at first sight roughness modelling may seem fearsomely complex, roughness is only part of the loss budget. Getting a reasonable figure in for roughness and choosing the correct model will enhance your prediction of insertion loss compared with solvers that simply model smooth surfaces. **DESIGN007**

Resources

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Martyn Gaudion is managing director of Polar Instruments Ltd. To read past columns, [click here](#). Martyn is the author of *The Printed Circuit Designer's Guide to... Secrets of High-Speed PCBs, Part 1 and Part 2.*

When it comes to generics, there is even more potential for variance.

PCB Designer's Guide to Heterogeneous Chiplet Packaging

Designers Notebook

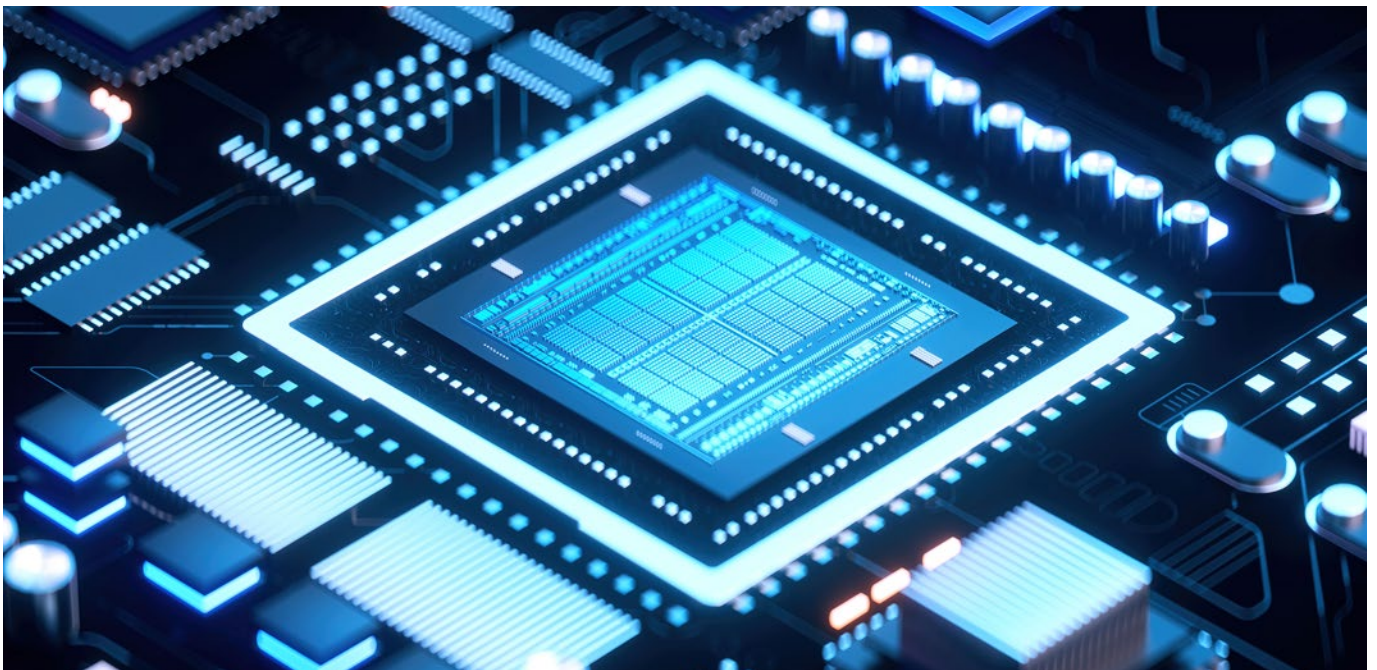
Feature Column by Vern Solberg, CONSULTANT

Integrating multiple chiplet elements on a single interposer or package substrate may be referred to as a multi-chip module, a hybrid IC, a 2.5D package, or simply an advanced package. Implementing chiplet technology will provide several advantages over the traditional, system-on-chip alternative. Each chiplet element is designed to be a building block with a specific function that is often common for multiple system-level products. Chiplet elements can also be sourced from multiple providers, even though they may be using alternative fabrication processes.

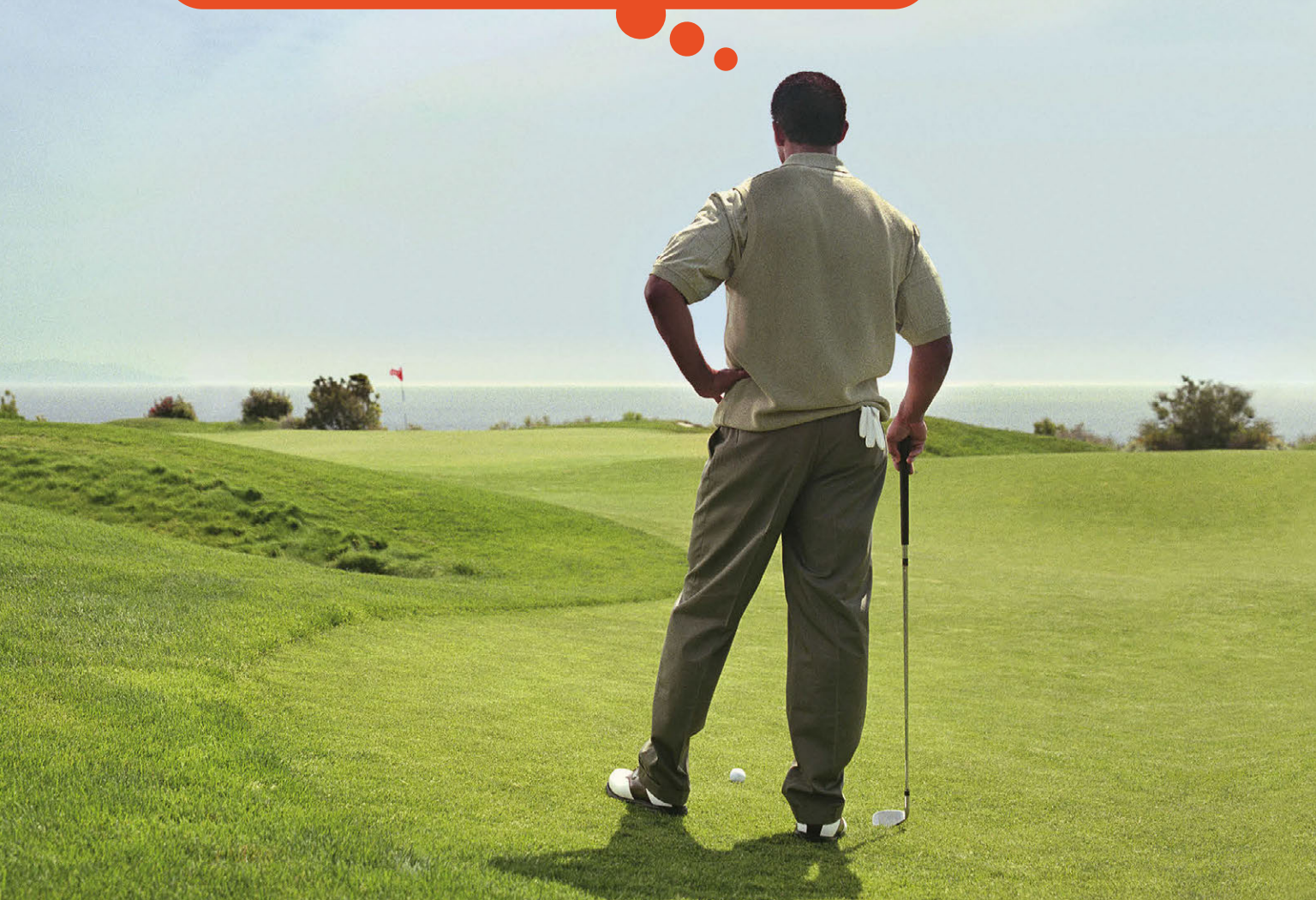
Common goals that product developers strive to achieve are improving performance, simplifying assembly processing, and for the companies that are producing hand-held, portable, and wearable electronics, minimizing product size. Achieving these objectives has

been made possible through advances in semiconductor fabrication methods and innovative packaging technology. Until recently, the alternative to arranging and interconnecting individual semiconductor functions relied on integration, a process for combining multiple functions into a single “monolithic” die element. Developers found that by combining the CPU with all primary logic support utilities, a true heterogeneous system-on-chip (SoC) product was achievable. Technically, the SoC package accomplished two goals: Processing speed increased and it scaled down the overall circuit board area by integrating several supporting functions within a single package outline.

As the basic SoC morphed into the newer multiple core processor variations, the semiconductor developers realized that they would



Hmm, what is recommended
**minimum distance for
copper to board edge?**



PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

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need a more efficient solution to support current and future generations of advanced computing products. Merging all the peripheral functions onto the same piece of silicon as that supporting the larger multi-core processor functions has resulted in an excessive increase in silicon area and, for some, unacceptable wafer processing defects. Here's the thing: Defects in the CPU portion of the die are not uncommon. It happens, but when defects occur in any of the peripheral supporting functions, the whole element must be scrapped, even though the multi-core CPU is functioning perfectly.

High-Density Semiconductor Packaging Innovation

Breaking up the traditional SoC model, several developers have adopted a heterogeneous packaging solution using chiplets, which isn't a package type but part of a packaging architecture. With chiplets, individual die elements can be broken down into smaller pieces and mixed and matched as needed to emulate the multiple function monolithic SoC die. A chiplet is simply a small outline, silicon-based integrated circuit (IC) that contains a specific subset of functionality. The chiplet elements are designed to function in unison with other chiplets, sharing a common platform

because the chiplet elements, typical of those illustrated in Figure 1, can be placed very close to one another, minimizing signal path lengths. The shorter path connecting the chiplet elements ultimately leads to enhancing the end product's performance potential.

A primary benefit of adopting chiplets is that the cost of wafer fabrication is much lower than the monolithic multiple function die, delivers a higher yield than the single monolithic die variations, and each element can be pre-tested. The flexibility offered by chiplets also provides important design and development benefits. Because they can be customized and upgraded easily, chiplets allow manufacturers to rapidly adapt to changing market conditions or new technological developments. They also simplify the production process by reducing the time and steps required to design and manufacture complex, application-specific SoCs.

So, where does the circuit board designer fit into this emerging package technology swing?

Many challenges come with interconnecting chiplets, especially in the context of commercial applications and scalability. On the other hand, they offer a promising solution to some of today's most pressing chip design issues. Much like the traditional printed circuit board as the basic interconnect method for electronic products, the heart of the system-in-chip (SiP)

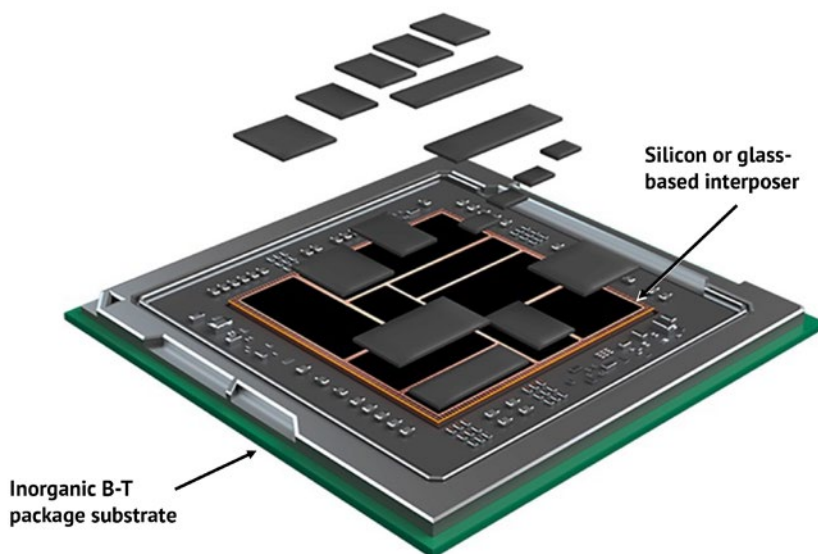


Figure 1: Heterogeneous chiplet package assembly example. (Source: Cadence¹)

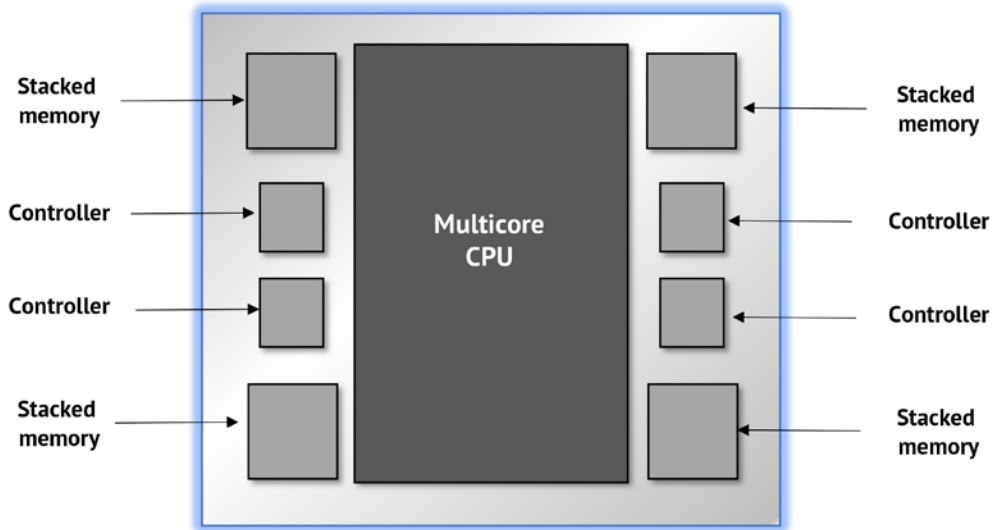


Figure 2: Multicore CPU with memory chiplet set on a silicon interposer.

variation is the interposer-substrate, the silicon or glass-based platform that glues everything together (Figure 2).

Circuit interconnect and land pattern geometry for the processors and chiplet elements are defined in millimeters and micro-meters (or microns), significantly smaller than the traditional surface mount configured circuit board; CAD tools to support interposer development are already in place.

Although silicon wafers or glass panels will be the preferred base platform for the highest density applications, there are inorganic materials that will accommodate the merging of chiplet die elements with a more relaxed density. In any case, it's simply a matter of scaling.

Status of Standards for Chiplet Elements

The industry chiplet standards are still being ironed out, but there are two major proponents: the Universal Chiplet Interconnect Express (UCIe) Consortium and the Joint Electronic Device Engineering Council (JEDEC). Activities within the JEDEC JC-11 subcommittee's scope include all aspects of the mechanical design, integration, interoperability, and standardization of all semiconductor devices. The organization's responsibilities include generating design guidelines, standardized measuring methods for mechanical

features, and mechanical outlines for commercial microelectronic packages and assemblies. The member-supported working groups also develop mechanical, environmental, and ergonomic performance specifications, recommend land pattern geometry, and establish the designators for identifying semiconductor device packages.

While several semiconductor developers have already established their own procedures for integrating their proprietary chiplet families, JEDEC member companies have initially targeted standards development for high-capacity memory, standards for stacked DRAM, as well as open compute platform (OCP) as part of their open domain-specific architecture initiative. These standards will guide the chiplet builders in developing an electronically standardized chiplet part description to make it easier to create a chiplet-configured system-in-package (SiP) design. By using chiplets, the ultimate goal is to reduce product development times and eliminate wafer process deficiencies by integrating pre-developed and electrically certified (KGD) dies onto an interposer.

Chiplet standards development activity is well underway, although the idea of a LEGOS brick format, with the same size die and a universal terminal pattern for interface (that some

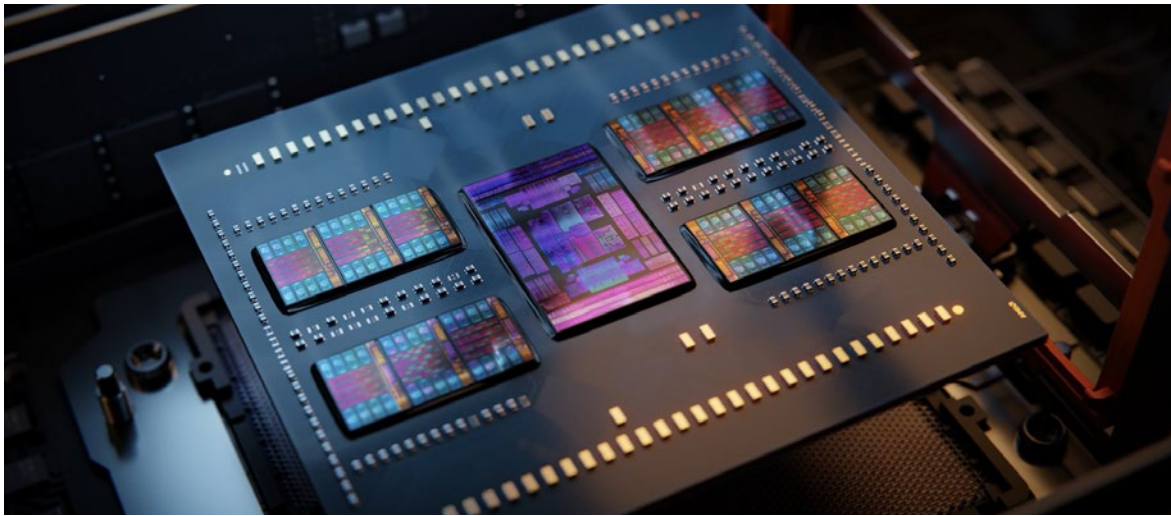


Figure 3: Multicore CPU with 12 DDR5-4800 memory chiplet elements. (Source: AMD)

predicted during the early stages of development), will not be practical.

So, a chip maker may have a menu of modular dies, or chiplets, in a library similar to the traditional plastic-encased, pre-packaged semiconductors. Using an uncased die, the designer is able to mix-and-match the chiplets and connect them using an ultra-high-density, die-to-die interconnect scheme only possible with silicon and glass interposers. To ensure that chiplets supplied from different manufacturers can work together, significant issues must be defined. Standards will need to describe the physical connectivity required between chiplet elements, and define compatible signal levels, operating voltages, and data transfer rates as well as digital compatibility aspects. Also required: the number of lanes in a bus, the coding sublayer for error correction, and how individual devices will know to automatically connect and exchange data with one another.

Change in Semiconductor Package Strategies

The industry front runners agree that as the electronics industry moves forward, more and more products will reflect this chiplet building-block approach for highly complex semiconductor packaging applications. Every major foundry has a technology roadmap addressing the interconnect densities for both


the 2.5D and 3D integration. These roadmaps will also forecast the progression of both logic and memory stacking and logic element stacking. While many challenges come with implementing chiplet elements, especially in the context of commercial applications and scalability, they offer a promising solution to some of today's most pressing chip design issues.

With chiplet technology gaining momentum, it's only natural that many big players in the industry are starting to get involved. Global Foundries and Samsung, for example, are two major companies at the forefront of this trend, each working on their own solutions to the chiplet challenge while Intel Corporation, AMD, Qualcomm, ARM, TSMC, and Samsung are working together on defining new standards for chiplet-based CPUs.

Major Participants in Chiplet Packaging Innovation

Intel already has the pieces in place to develop these chiplet-based products. Key criteria, known-good dies, EDA tool refinement, die-to-die interconnect technologies, and a sustainable manufacturing strategy.

AMD is also actively researching and developing chiplet technology. The company has already released processors that use chiplet-based architectures (Figure 3).

A person in a yellow shirt is sitting on a suspension bridge that spans across a deep valley. The bridge is made of wooden planks and is supported by cables. Below the bridge is a calm lake that reflects the surrounding mountains. The mountains are covered in snow and are very high. The sky is a mix of blue and orange, suggesting a sunset or sunrise. The overall scene is peaceful and scenic.

Hmm, what is the recommended **minimum solder mask** width to be able to get a solder mask bridge **between two copper pads**?

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IBM is a leading provider of advanced semiconductor technologies and is actively working on chiplet technology. The company has developed a chiplet-based architecture for its power processors and is also researching the use of chiplets in other applications.

TSMC is a contract semiconductor manufacturer and is actively researching and developing chiplet technology. The company has announced plans to use chiplet-based architectures in its future processors.

Samsung is actively researching and developing chiplet technology. The company has already released processors that use chiplet-based architectures.

GlobalFoundries is a contract semiconductor manufacturer and is actively researching and developing chiplet technology. The company has announced plans to use chiplet-based architectures in its future processors.

SK Hynix is a major provider of memory and storage solutions and is also actively researching and developing chiplet technology.

Micron is a leading provider of memory and storage solutions and is actively researching and developing chiplet technology.

Qualcomm is active in the mobile chip market and is researching and developing chiplet technology. The company has announced

plans to use chiplet-based architectures in its future processors.

Huawei is a leading provider of telecommunications equipment and is also actively researching and developing chiplet technology. The company has announced plans to use chiplet-based architectures in its future processors.

Xilinx specializes in the design and development of FPGAs (field programmable gate arrays) and other types of programmable logic devices.

With continued development and innovation, the electronics industry can expect to see more widespread use of chiplet concepts sooner than later. **DESIGN007**

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1. "Chiplets and Heterogeneous Packaging Are Changing Design and Analysis," a white paper by John Park, Cadence Design Systems, 2020.



Vern Solberg is an independent technical consultant, specializing in SMT and microelectronics design and manufacturing technology. To read past columns, [click here](#).

Despite Export Ban on Equipment, China's Semiconductor Expansion in Mature Processes Remains Strong

On June 30, the Netherlands introduced new export restrictions on advanced semiconductor manufacturing equipment. Despite facing export controls from the US, Japan, and the Netherlands, TrendForce anticipates the market share of Chinese foundries in terms of 12-inch wafer production capacity will likely increase from 24% in 2022 to an estimated 26% in 2026. Moreover, if the exports of 40/28nm equipment eventually receive approval, there's a chance that this market share could expand even further, possibly reaching 28% by 2026. This growth potential should not be dismissed.

Several manufacturing processes including photolithography, deposition, and epitaxy will be subject to these recent export restrictions.

The U.S. Export Administration Regulations (EAR) is primarily aimed at limiting China's growth in advanced process, rather than mature ones. Although export regulations from the U.S., Japan, and the Netherlands cover equipment used across both mature and advanced process generations, it's namely equipment used in 45nm to more advanced processes which will require inspection.



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How I Learned Advanced Design Strategies

Tim's Takeaways

Feature Column by Tim Haag, FIRST PAGE SAGE

If there's one thing that helped my career in printed circuit board design more than anything else, it would be my time working at a service bureau. Don't get me wrong, I'm delighted with the different captive shops I've worked for in larger companies throughout my career. Over the years, these organizations have provided the opportunity to lay out boards for computer systems, test equipment, display hardware, and much more. But in all those captive shops, the board types have usually been pretty much the same, which stands to reason when you consider the type and range of products sold by each parent corporation. The service bureau, however, was a different story.

Back in the Day

It is important to note: Working at the service bureau was a long time ago. CAD systems were in their adolescent phase, and designers were transitioning from light tables, X-Acto knives, dollies, and tape. At the same time, new types of electronics were growing at an accelerated rate, which went hand-in-hand with all the new CAD tools and designers—like me. On any given day, you would find yourself working on a standard board type for a garden-variety computer, and then switch over to a one-off power control board for an industrial application. While at the service bureau, I worked on boards ranging from an inch square to over three feet. I saw everything from single-sided



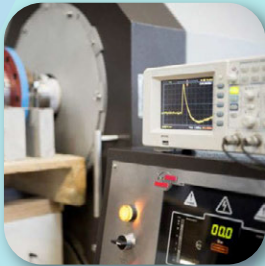


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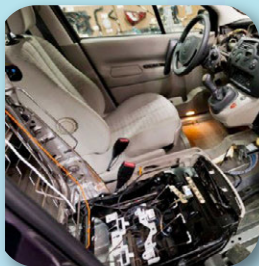
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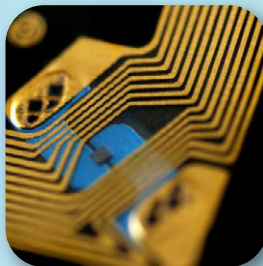
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boards to 16 layers, which wasn't nearly as commonplace then as it is now.

Learning as you go was the name of the game, and there was a lot to learn. The technology wasn't nearly as demanding as it is now, but for the CAD and manufacturing technologies available at the time, it was fairly tight. There were other boards, like the power control board I mentioned earlier, that had "traces" several inches wide to absorb huge amounts of energy, if necessary. We ended up using dumb graphics to design portions of that one because the CAD systems we were using couldn't handle the width requirements.

I rarely worked with the same board shape twice except for the standard computer cards we would do from time to time; some of the outlines given to me were really bizarre. I remember one that had the shape of a skull, and we actually had a lot of fun with it until it was time to settle down and get to work. The parts placement and routing could be just as wild, and I worked on some boards with radial placement and routing. Due to the limitations of the CAD system, I would have to use a 1-mil grid for parts placement with a series of drawn circles on a graphics layer behind the parts serving as a placement guide.

Beyond PCB Design

Interestingly enough, circuit board types and technologies weren't the only unusual variations in work that the service bureau introduced me to. I got to know different sorts of people too. Some folks would drop off their data and trust us to design the board just as you would expect. However, others would stay with us and monitor the layout throughout the entire process. There's nothing more "helpful" than having a backseat driver while you are

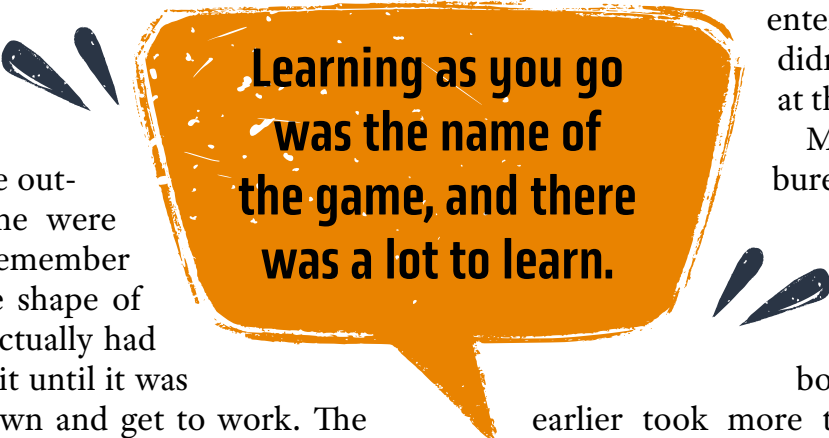
laying out a circuit board (and some of you will know exactly what I mean). One guy sitting behind me would try to "steer" while I routed his board, making a clicking noise whenever I changed directions or dropped a via. I can still hear him in my nightmares: "That should go left... *click*, ah that's good... no I wouldn't do that... *click*, straight down now... good... *click!*" To be fair, though, others made it all worthwhile. One of my backseat drivers bought me dinner while "we" were working. The next night he mentioned dinner again, and my boss joined us in hopes of a free meal, only to have the guy give my boss the bill instead. To this day, I can still see the sour expression on my

boss's face. Dinner and entertainment; life just didn't get much better at the service bureau.

My time at the service bureau also exposed me to some other unique situations. For example, that little one-inch board I mentioned

earlier took more than two weeks to design, even though it only had two connectors and maybe 75 connections. They took their time getting us the information we needed, then needed several days to examine my work. After some design changes, we had to drive out to their facility for a large-scale design review. Really? For a one-inch board? Meanwhile, back at the shop, I had laid out a standard computer card while waiting for them. That engineer had all his data neatly organized and packaged, and the design went like clockwork

Then there was the time a group of guys from a large aerospace corporation commandeered our conference room for a month while we designed a series of PCBs for their project. I don't think that any of us spoke more than a dozen words to them; it was all very mysterious. White shirts, red power ties,



**Learning as you go
was the name of
the game, and there
was a lot to learn.**

and copious amounts of coffee, only then to emerge from their isolation to ask a question, request a correction, or grab another pot of coffee. It was pretty creepy in a “Scooby-Doo vs. the CIA” way.

New Technologies to Explore

One of the most fascinating things about working at the service bureau was learning about the new technologies in the projects we were designing for our customers. I’ve already mentioned some of them, like the power board that could take a lightning strike. Of course, there were plenty of computer cards and other standard electronics applications, but there were also some really interesting ones too. I worked on some projects where I wasn’t allowed to know their purpose. One engineer even hinted at a military application, which seemed unlikely since none of us had any security clearances at the time. But hey, it was the ’90s, so I guess anything is possible. I also worked on one of the first touchscreen systems designed for a CRT (I never knew if it ever worked) and a biosensor wristwatch before anyone had even considered the catchphrases “human interfaces” and “wearable technology.”

While this month’s contributors will have plenty to say on how to approach unique design

situations, my intent was to highlight how starting out with all of these unusual design scenarios helped me be better prepared for the bulk of the work I encountered later on. Certainly, I learned how to coax the most out of a CAD system while being educated by some of the most talented designers I’ve ever known. Learning about many different board shapes, sizes, and technologies was invaluable later on, as was the exposure to multiple manufacturing processes, dimensioning etiquette, and design standards. I know things have changed over the years, and maybe my experience isn’t as easy to replicate anymore. It’s been a while since I’ve poked my nose into a service bureau, and it would be interesting to see what’s different and what hasn’t changed.

At any rate, if you ever get a chance to be part of a fast-moving, take-your-breath-away business like a service bureau, I recommend embracing the opportunity. You will be amazed at the education that you will come away with. Until next time, my friends, keep on designing. **DESIGN007**



Tim Haag writes technical, thought-leadership content for First Page Sage on his longtime career as a PCB designer and EDA technologist. To read past columns, [click here](#).





MilAero007 Highlights



NASA Funds Small Business to Advance Tech for Space, Earth ▶

A new slate of funding from NASA will help small businesses develop technologies to advance space exploration, climate research, and more. In mid-April, NASA selected 112 proposals from 92 U.S. small businesses across 28 states to receive Phase II funding from the Small Business Innovation Research program, totaling approximately \$98 million.

American Made Advocacy: Taking the Fight to Capitol Hill ▶

If you're not at the table, you're on the menu. That's one of the reasons, in his State of the Union address, President Biden's praise for an emerging manufacturing renaissance was so welcome. He said, "If we invent it here, we should also make it in America." He sounded a lot like a microelectronics CEO.

Carol Handwerker Appointed to NIST Advisory Committee ▶

We often hear words and phrases that naturally go together: Salt and pepper, touch and go, trace and space. When it comes to the work of IPC member Carol Handwerker, however, the collocations are much more nuanced, and have greater significance. You're more likely to think of phrases such as standards and technology, lead-free and solder, or advanced packaging and heterogeneous integration.

Viasat Completes Acquisition of Inmarsat ▶

Viasat Inc., a global communications company, announced the completion of its acquisition of Inmarsat.

EWPT 2023: A Review by Happy Holden ▶

While IPC was hosting its annual SummerCom mid-year standards event, WHMA was hosting its own "wire show," co-located in Milwaukee, Wisconsin. During IPC SummerCom 2023, more than 90 meetings from May 13–18 were conducted.

Raytheon to Deliver Full Rate Production for TCTS Increment II Air Combat Training System for U.S. Navy ▶

Collins Aerospace, a Raytheon Technologies business, announced it will deliver on the full rate production contract awarded by the U.S. Navy for Tactical Combat Training System–Increment II (TCTS II), Air Combat Training System (ACMI) for the U.S. Navy.

Lockheed Martin to Collaborate With U.S. Army to Improve Space-Enabled Defense Systems ▶

Lockheed Martin signed a Cooperative Research and Development Agreement with the U.S. Army Combat Capabilities Development Command's Aviation and Missile Center to advance Beyond Line of Sight connectivity. Under this CRADA, Lockheed Martin and AvMC will jointly develop and demonstrate space-enabled defense systems.

Boeing, Indonesia Partner to Explore Air Traffic Management Improvements ▶

Boeing has signed an agreement with AirNav Indonesia to explore initiatives to further enhance the safety and efficiency of Indonesia's national air traffic management system.

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Designing and Manufacturing Wearable Biosensors

Feature Article by Rick Ramos

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As wearable electronic devices continue to be more prevalent, it's an ever-greater challenge for companies that manufacture them to keep their competitive edge. It is vitally important that each device is effective, cost-efficient, and of the highest quality available.

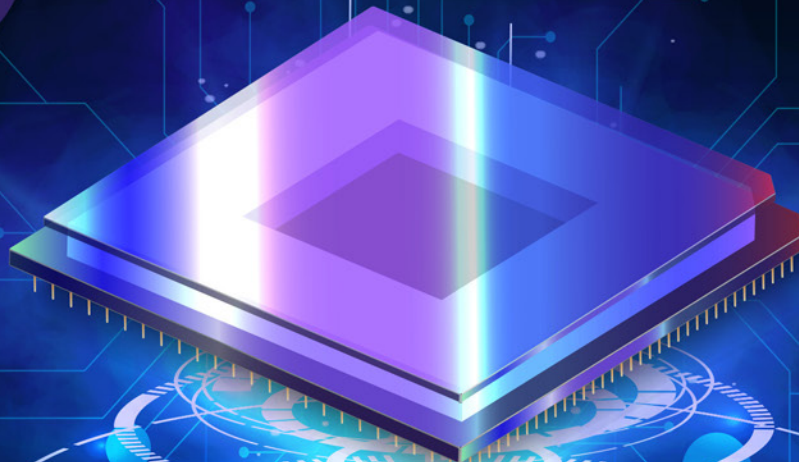
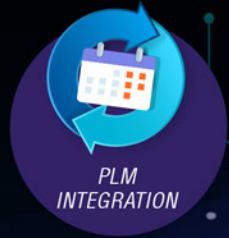
To cost-effectively mass produce wearable biosensors, vertical integration of manufacturing and assembly operations is key. This involves printing conductive inks on flexible substrates and successfully performing converting operations (such as lamination of medical-grade hydrocolloids, adhesives, non-woven and foam layers, hydrogel dispensing and/or placement and final packaging) in surface-mount technology (SMT) components. Any connections must be made on the “non-patient” side of the patch to ensure patient

comfort. We have been successful with 0.010” via print filling in order to have continuity between skin contact and a communication device.

Vertical integration for wearable biosensor manufacturing includes:

- DFM engineering abilities for tooling, test equipment, and packaging
- Screen-printing of silver, silver/silver chloride, carbon, dielectric, and graphic ink
- Sheet-fed and roll-to-roll printing
- SMT processes with flexible circuits. With screen-printed polyester, etched polyimide and rigid PCBs may be required for hybrid patches
- Screen printed through-holes on flexible substrates

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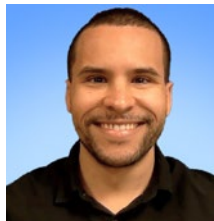
Technologies Used to Manufacture Biosensors

The process for manufacturing biosensors employs screen printing, laser cutting, lamination, and adhesives. Screen printing of various conductive inks uses, but is not limited to, silver, silver/silver-chloride, carbon, zinc, gold, dielectric, and more. In addition, the SMT process is used if components are required. There are several key conversion processes, including die-cutting and lamination of medical grade foams and adhesives, as well as the dispensing and placement of medical grade hydrogels and final packaging. Through-holes allow for connections between the top and bottom layer printed circuits and up to six layers per side.

In most applications, biosensor manufacturing involves a supply chain of companies since few companies possess all the necessary capabilities. These capabilities include:

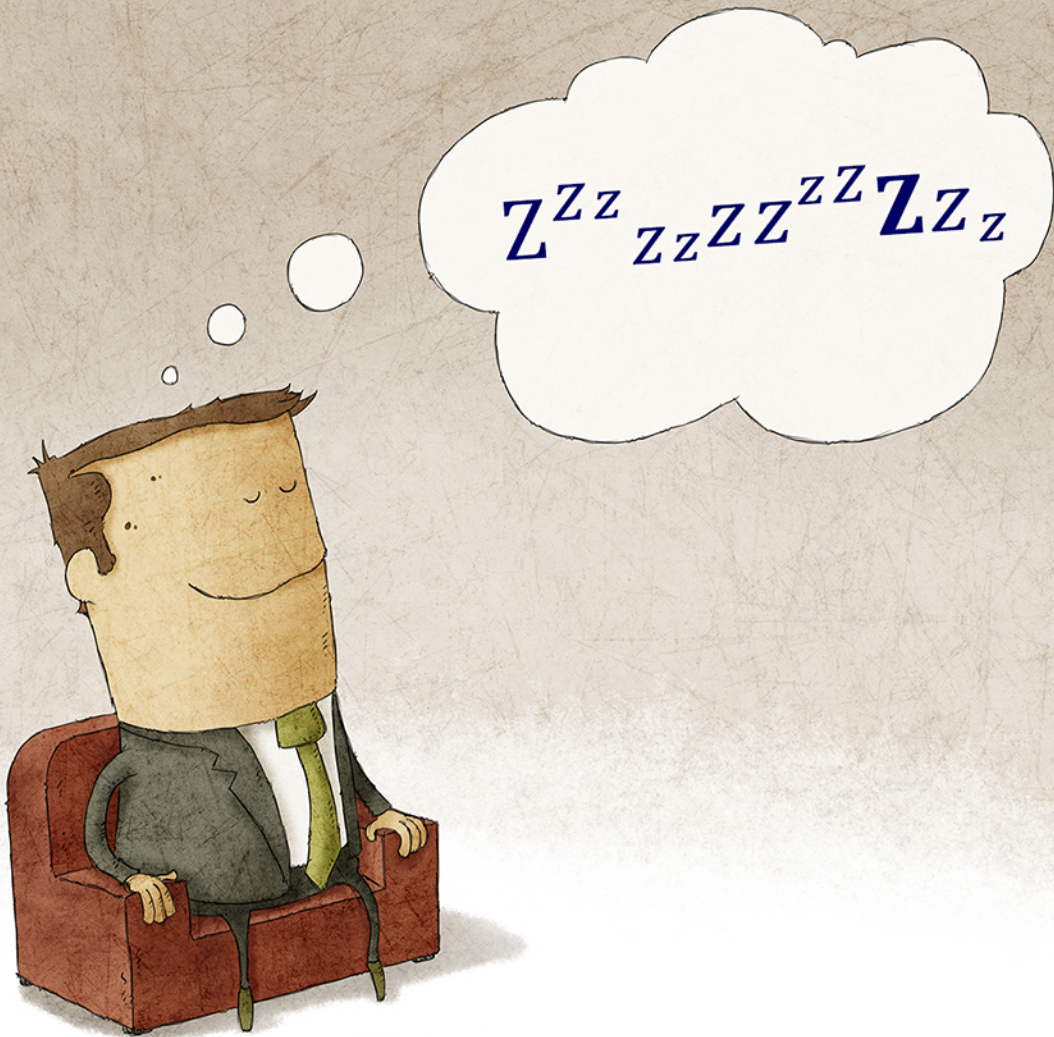
- Circuit/electrode printing
 - › Sheet or roll-to-roll
 - › Typically, 2-5 print passes
 - › Oven drying or UV curing after each print pass
 - › Oven dwell typically ≤ 10 minutes at $\leq 140^\circ\text{C}$
 - › Slip sheet or interleaf may be required to prevent ink rub-off since carbon inks tend to be soft and transfer to backside of substrate when stacked or wound in rolls
 - › Routine in-process measurements to confirm conformance to agreed dimensional, ink thickness, and electrical specifications
- Patterning of spacer/adhesive layer
 - › One or combination of SRD, rotary, match metal, and/or laser
- Patterning of lid or top layer
 - › Same as spacer/adhesive

- Dispensing and drying/conditioning of functional material
 - › This is where most of the IP resides, and this step is often performed by the OEM. This is changing as more medical converters are adding dispense capability in an effort to add value.
- Laminating
 - › Cold with pressure sensitive adhesive (PSA) or heated (hot melt)
 - › Performed by OEM or converter
- Option: Cartridge or cassette type configuration
 - › Application may skip lamination process and instead die cut individual sensor circuits and install them into an injection molded plastic microfluidic cartridge or cassette.
- Sheet/roll to cards
 - › Large format cut down to rectangular card format (sensors nested 1 row x TBD across) for compatibility with commercially available strip singulation equipment.
- Singulation
 - › Individual sensors are typically slit from cards into individual test strips
- Packaging
 - › Singulated test strips placed in plastic vials, often with inside walls lined with a desiccant. A screw or snap cap is installed, followed by application of label. **DESIGN007**



Rick Ramos is a marketing and inside sales engineer for Eastprint Inc.

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Flex007 Highlights



Insulectro Announces New Partnership With Laminate Suppliers Arlon Electronics Materials and EMC ▶

Insulectro has announced it will become the exclusive distributor for North America of Arlon copper clad laminates beginning September 4, 2023. Arlon is also the master distributor for Elite Materials Company (EMC), based in Taiwan, bringing both product lines to Insulectro.

Rigid-flex, Rigidized Flex, or Hybrid Flex? ▶

In a recent interview with Design007 Magazine managing editor Andy Shaughnessy, he asked me about rigid-flex and its new popularity. This seems like a perfect opportunity to dig into the topic and discuss the differentiation between rigid-flex, rigidized flex, and what I am calling a hybrid flex.

Challenges of DFM Analysis for Flex and Rigid-Flex Design, Part 3 ▶

DFM analysis tools for the last several decades have focused on a typical rigid PCB or some variant. While many standard DFM constraints are applicable, flex has many unique requirements that cannot be addressed with typical DFM analysis. Flex and rigid-flex DFM must be targeted toward the unique materials and processes used to produce flex and rigid-flex designs.

Toyochem Develops Highly Flexible EMI Shielding Films for Smart Devices ▶

Toyochem Co., Ltd. has rolled out the new LIOTELAN line of highly flexible conductive and insulating sheet films for the protection of

electrical and electronic equipment. The new sheet films exhibit high water-resistance and are highly flexible with a high elongation of 500%. LIOTELAN shielding films can be hot-press molded on to the electromagnetic interference (EMI) noise source on the PCB.

Flexible Circuits Acquires Third CBT/MLI DI System from Technica USA ▶

Technica USA reported that Flexible Circuits purchased their third CBT/MLI direct imaging (DI) system for their plant expansion.

New OE-A Roadmap Unveils Exciting Printed Electronics Industry Prospects ▶

The highly anticipated OE-A Roadmap offers valuable insights into the present state and prospects of flexible, organic, and printed electronics. The whitepaper delves into key markets such as automotive, consumer electronics, healthcare, printing and packaging, smart building, and Internet of Things, providing comprehensive analyses and forecasts for each sector.

Worldwide Wearables Market Is Forecast to Rebound in 2023 with Continued Growth Thereafter ▶

After declining for the first time ever in 2022, worldwide shipments of wearable devices are forecast to rebound in 2023, reaching a total of 504.1 million units, according to new data from the International Data Corporation (IDC) Worldwide Quarterly Wearable Device Tracker.

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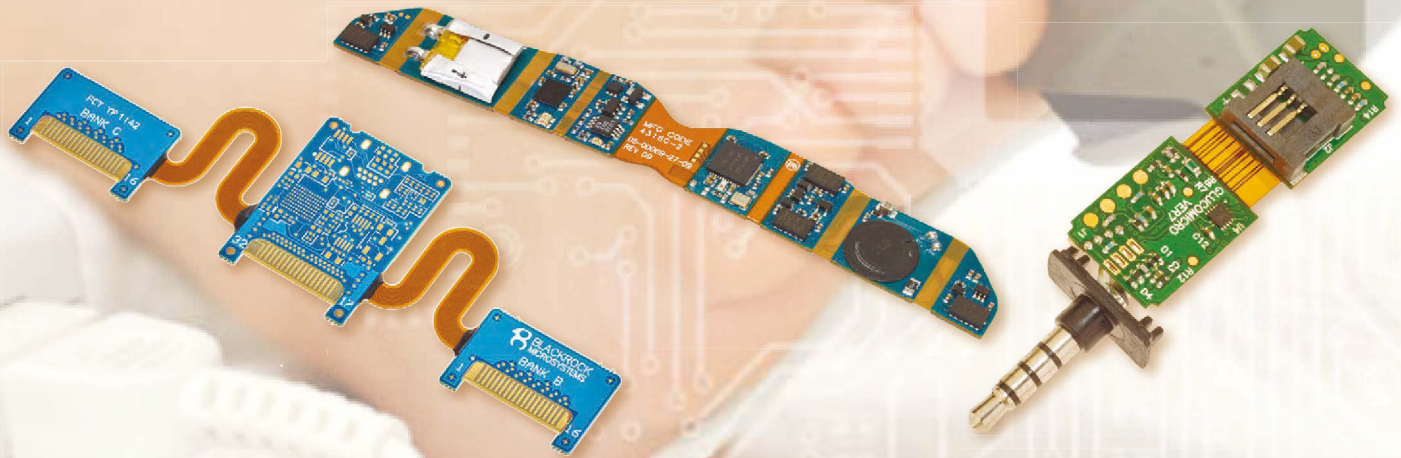
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Stiffeners for Flex Circuits

Article by Mike Morando
PFC FLEXIBLE CIRCUITS

One of the most recent topics in the flex world has been the evaluation of materials required to build a rigid-flex or flex circuit. Discussions around flex and materials include variations of polyimide and copper. Here I will discuss another material that plays a very important role in the world of flex circuits: stiffeners. These are critical components to a flex circuit because they broaden its scope and potential applications.

A “stiffener” in the flex circuit world is a generic term used to identify a material that prevents a flex circuit from bending and flexing. In all these instances, we will not be talking about rigid-flex—just flex circuits only. Stiffeners are, in most cases, a non-electrical component/addition to a flex circuit and function as a mechanical support.

Stiffeners are attached in a secondary operation by either thermal bonding, pressure sensitive adhesives (PSAs), or epoxy. Stiffeners

require a secondary operation in the manufacturing process, so it is a cost adder.

Materials we have used to add stiffeners include FR-4, polyimide, aluminum, alumina, steel, and ceramic. As technology progresses and flex is used in more and different applications, a variety of materials are being used to support and create flex stiffeners.

Reasons to include stiffeners into your flex circuit design include:

- The SMT process and component support
- Through-hole component mounting
- Flatness requirements
- Mechanical infrastructure and design support
- Increased material thickness requirements
- ZIF connector interface
- Heat dissipation
- Wire bond pads

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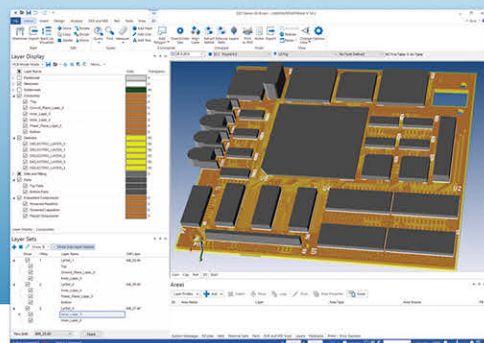
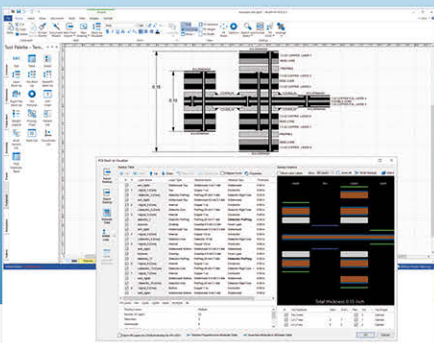
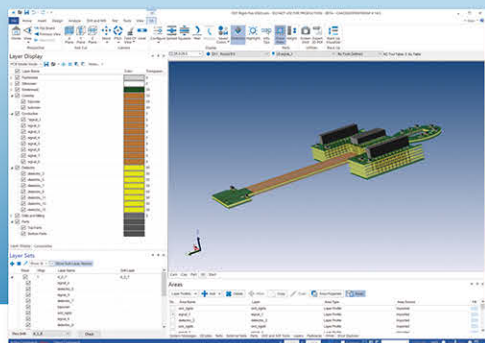


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Figure 1: Mechanical support for SMT connector.

FR-4 and polyimide stiffeners can be placed in panel form on top of the flex panel. The material is drilled, routed, and pressed onto the flex panel. The flex with the stiffeners, now attached and in place, get routed or lasered and removed from the panel.

Manufacturers will always try to attach stiffeners in panel form; it is the most cost-effective solution to adding stiffeners to flex. In some instances, there is a need to hand place the stiffeners, requiring a separate lamination process. This adds cost. Your manufacturer should help you to design the lowest cost solution.

SMT Component Support

The most common use of a stiffener tends to be SMT component support. For SMT support, a stiffener—usually FR-4 material—is attached underneath an area where SMT components will be placed. The addition of the stiff-

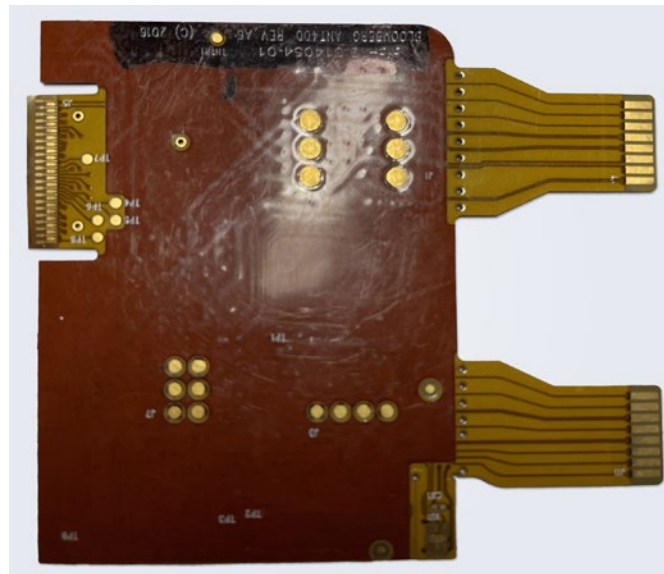


Figure 2: Polyimide stiffener supporting SMT.

ener serves a few purposes during assembly: The stiffener creates a flat surface for precise component mounting, provides a “hard surface” for the actual placement—preventing the flex from bouncing during the placement process—and will support the assembly through the reflow oven. After assembly is complete, the stiffener protects the solder joints by not allowing the flex to bend in the assembled area.

Through-hole Components

For through-hole assembly, FR-4 is the most common use, but it depends on the application. The use of the stiffener supports the component as it is attached to the flex, protecting the solder joints and the flex from bending awkwardly and cracking traces.

Flatness

In most cases, it works to use FR-4 to create a flat, stiff surface. In some instances, however, there is a need to create a perfectly flat surface (minimal tolerances across an area). FR-4 material and the adhesive process can provide tolerances that may not be acceptable.

As an example, we once needed to create a perfectly flat surface to mount a large BGA component: 360+ balls on a five-layer flex. Our assembly and inspection group shuddered, as the need to keep both the flex and component flat to make perfect contact across all the balls

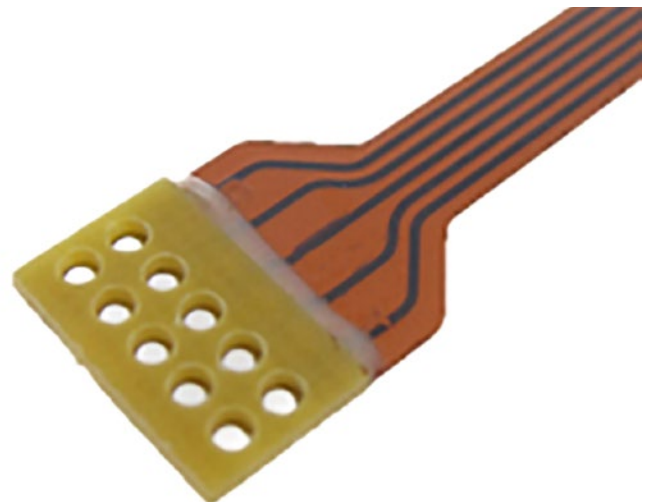


Figure 3: Through-hole stiffener.



Figure 4: Stainless stiffener for flatness.

would be super difficult. The tolerances were mils across inches of area.

First, we had a call with the component provider to understand the tolerances they could hold. Once we had agreement and thought the tolerances were doable, we manufactured a machined stainless-steel stiffener that held very tight tolerances. The stainless material provided not only the flatness required, but the strength to hold a five-layer flex flat. The stiffener was pressed onto the flex and the BGA component was placed using SMT. Inspection was done using X-ray to confirm all balls were seated. Success!

Mechanical Support

We use stiffener material on flex to assist with mechanical requirements of the design. While the use of flex does provide “flexibility” of the circuit, there may be a need to mount, bend, attach, or support the flex in an application.

This could include connector mounting holes, strain relief for bend areas, connector gripping for mating and unmating, any flex mounting requirements, or wire bonding

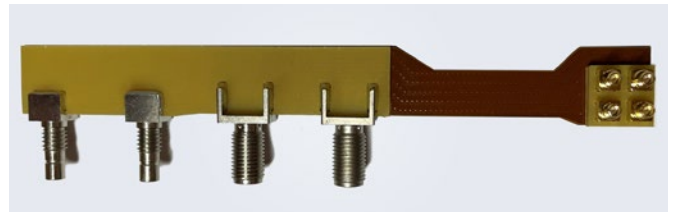


Figure 5: FR-4 stiffener mechanically supporting TNC connectors.



Figure 6: Stiffener supporting display.



Figure 7: Stiffeners supporting SMT connectors and wire bond area.

support. The use of a stiffener depends on the outline and shape of the design. The material used in these applications tends to be FR-4 and polyimide.

Figures 5–7 demonstrate a few applications where a stiffener is supporting the flex.

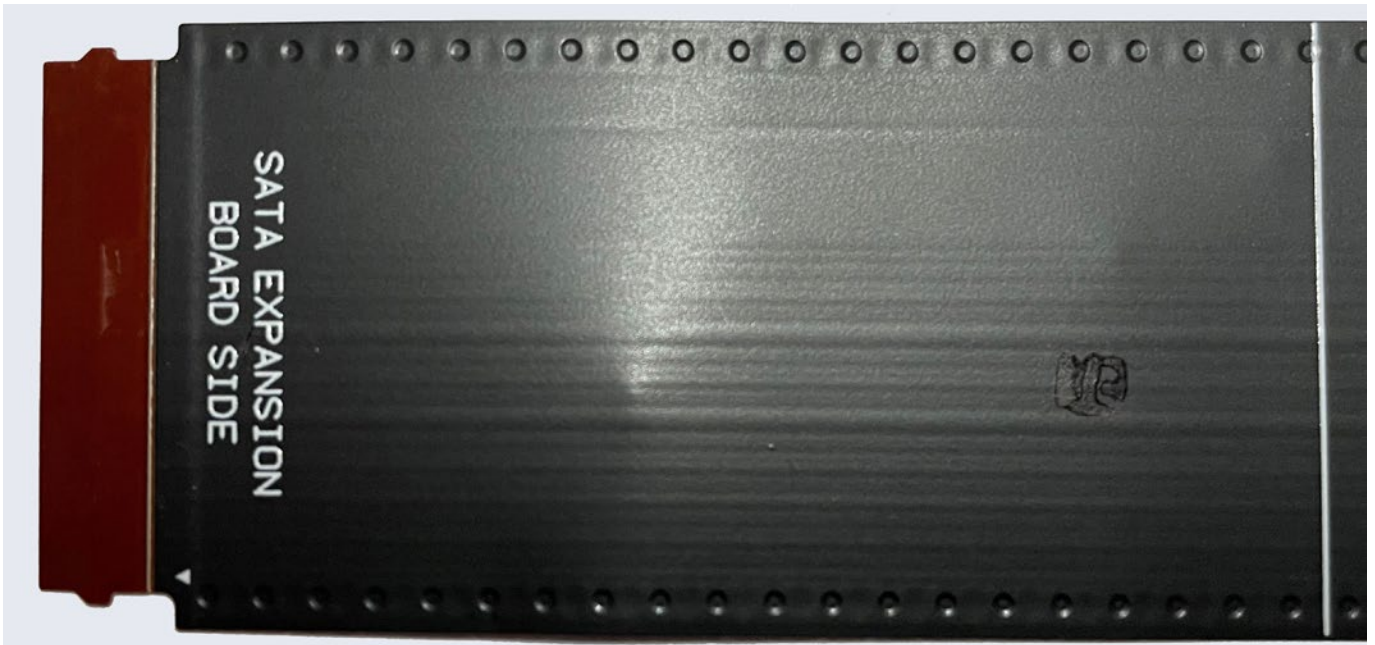


Figure 8: Polyimide stiffener for shielded ZIF application.

Heat Dissipation

As we add more resistors, capacitors, semiconductors, and LEDs to flex, there becomes a need for the flex to assist in heat dissipation. In addition, where the flex circuit is creating heat—like a flex heater—there is a need to spread the heat.

For heat dissipation, aluminum and ceramic stiffeners have worked well. Common medical applications for us have been small cameras and an LED side by side. The LED gives off a fair amount of heat and can disrupt the image sensor (camera). Using an aluminum stiffener supports the SMT placement, protects the components after assembly, and most importantly, dissipates the heat enough to not disrupt the other components in the area.

Alumina has been used for heat spreading. Applications requiring a flex heater and consistent temperatures across areas could use aluminum, alumina, or ceramic. Check with your manufacturer as these are highly custom.

Zero Insertion Force Connectors

Zero Insertion Force connectors (ZIF), commonly used in flex circuit applications, have

specific thickness requirements for attachment. Manufacturers' height requirements vary. FR-4 is too thick. In order to meet the flex height requirement of the connector interface, flex shops will use additional layers of polyimide. Polyimide adds height and stiffens the circuit at the interface.

Stiffeners on flex circuits provide mechanical support and strength, circuit flatness, thickness, heat spreading and dissipation, and the protection of solder joints. Your flex manufacturer will be familiar with the materials and the process. Adding stiffeners to your flex circuit is part of the design process and should be considered carefully.

Stiffeners enable and broaden the scope of flex applications. **DESIGN007**



Mike Morando is director of sales and marketing for PFC Flexible Circuits, a subsidiary of OSI Electronics.

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Stretching Conductors— and Design Possibilities

Flexible Thinking

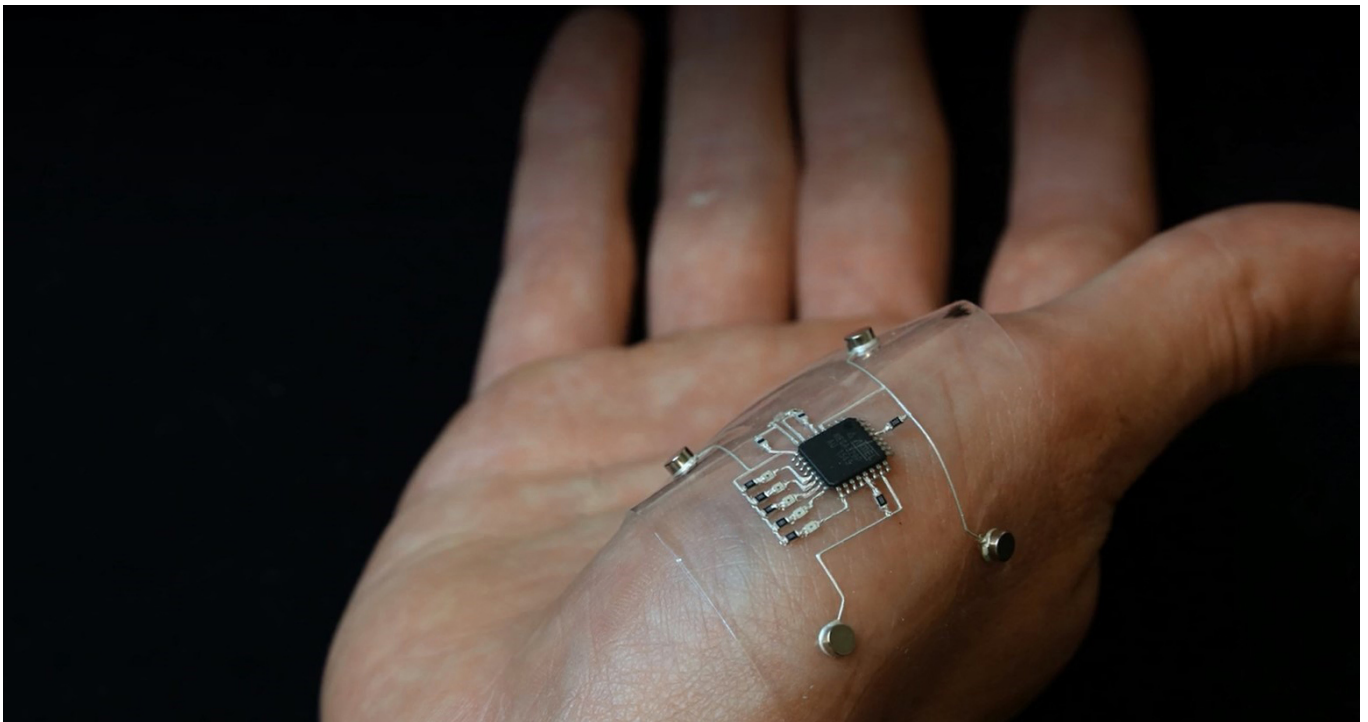
by Joe Fjelstad, VERDANT ELECTRONICS

Stretchable circuits, also referred to as elastic circuits or even “elastronics,” are a subset of the venerable flexible circuits that have enabled countless numbers of today’s electronics products, from toys to smartphones to the International Space Station. This most recent “member” of the interconnection family—stretchable circuits—has been designed and engineered to be resiliently bent, twisted, and/or stretched in support of the end product’s need without negatively affecting its electrical function.

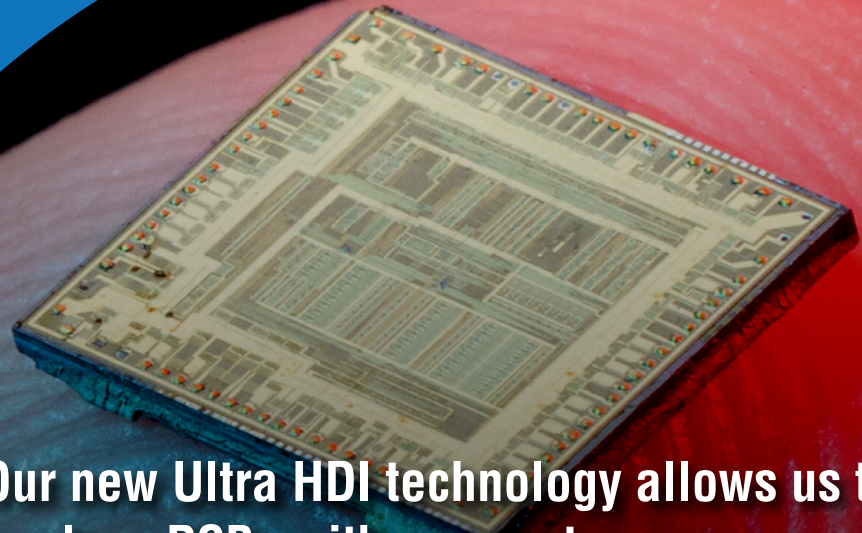
The idea of creating an interconnecting circuit that can be stretched and resiliently (or forcibly) returned to its original position has been around for many years. Ones that caught

my attention when the industry first began to “pile on” the concept by creating circuits on elastomeric base films were those where the circuit was formed in an accordion-like fashion. This was used to allow access to electronics housed in file cabinet-like drawers since at least the 1970s and, on a much larger scale, the jetways used to get passengers on and off passenger planes. You can see the undulating cables hanging beneath the jetways.

However, the pursuit of using elastomeric substrates for creating stretchable circuits arguably began in earnest in Europe, funded by the European Union’s shared scientific funding called Project STELLA, which ran from February 2006 to January 2010. I was for-



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tunate enough to give a keynote address at the first conference on flexible and stretchable circuits in Gent, Belgium in 2008.

There were many excellent papers given at the inaugural conference, which described research on how to design and fabricate the circuits, typically using copper, and mitigating the mechanical damage inevitably caused by repeated stretching. Solutions were both in-plane (using undulating traces) and out-of-plane (using humped circuits that flattened when stretched). There were also examinations of stretchable conductors comprised of elastomers loaded with conductive metals.

Most interesting at the time were the applications that were shared, especially wearable electronics products. At the time, fashion apparel was most alluring. Affixing rows or arrays of LEDs to clothing was eye catching and became somewhat of a poster child for the nascent technology.

However, it was the fact that stretchable circuits could conform to irregular contours of the human body, thus allowing for comfortable and unobtrusive integration into clothing, accessories, or directly on the skin; this opened the doors to the new interconnection option. They soon found their way into many new products, including a variety of health monitoring, fitness tracking features, and smart textiles which integrated electronic functionality into clothing.

Stretchable circuits were also deemed to have significant potential in healthcare. They are currently used in novel medical devices, including electronic skin patches, which can monitor vital signs, like blood pressure; measure blood chemistry, such as sugar levels; and deliver drugs such as insulin to correct the levels. They can also provide real time feedback during physical rehabilitation sessions. Some

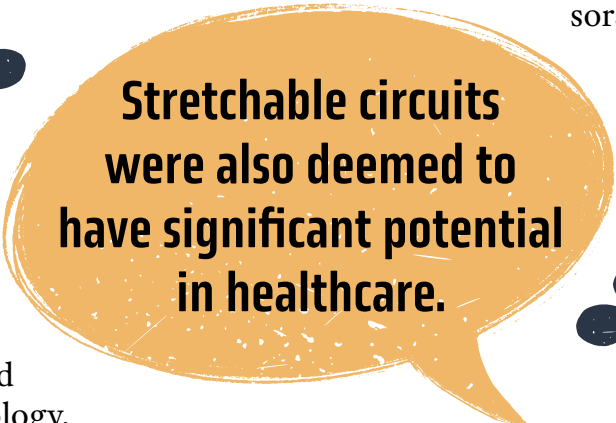
researchers have been looking into using stretchable circuit technology for implantable applications that would enable seamless integration with soft tissues, providing the potential to restore use of paralyzed limbs and mobility to accident victims. In this regard, stretchable circuits show promise in the manufacture of prosthetics to restore limbs of amputees, many the victims of wars. Stretchable circuits integrated into such products allow for more natural movement and allow wearers to move back into society with the anonymity they enjoyed before they lost their limbs. All appendages are subject to development, and it

can be expected they will have sensors integrated into them that allow the wearer to sense touch, pressure, and temperature; perform delicate tasks; and experience again the joy of holding their loved ones or a newborn child.

Not surprisingly, stretchable circuits are being employed to create smart and flexible sensor systems for all manner of products from automobiles and appliances to household furniture, pet monitoring, and security systems—all connected to the internet and monitored by computers. Getting sleepy at the wheel? Your car will direct you safely off the road.

Of course, stretchable circuits will, without question, be employed in the design of increasing numbers of consumer electronics, from video gaming appliances and virtual reality headsets to exercise and relaxation devices as well as an unimaginable range of devices locked—only for this moment in time—inside the minds of the countless present and future inventors, who will bring them to the public to improve everyday lives.

In summary, while stretchable circuits are still a relatively new kid on the block, we can



**Stretchable circuits
were also deemed to
have significant potential
in healthcare.**

expect to see much more use of the technology in the future. I am doing my part. In my most recent Occam/SAFE technology patent, I described a way to make such products without dealing with the inherent instability that stretchable materials present to manufacturing. I hope to soon get the opportunity to build a demonstration circuit as envisioned and open doors to even more applications for this wonderful new member of the flexible circuit family. **DESIGN007**



Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185 patents issued

or pending. To read past columns or contact Fjelstad, [click here](#). Download your copy of Fjelstad's book *Flexible Circuit Technology*, 4th Edition, and watch his in-depth workshop series "Flexible Circuit Technology."

Altium 365 GovCloud Offers Increased Security

Altium recently launched Altium 365 GovCloud, a dedicated platform accessible only to—and managed solely by—U.S. persons. The company says that GovCloud can help customers to be in compliance with ITAR, EAR, and other requirements.

I-Connect007 spoke with Bruno Blasigh, Director of Cloud Security for Altium 365, about the new platform, how it functions, and how GovCloud can help to keep foreign entities from accessing your data.

Bruno, how are you doing? Give us a little background about yourself.

I'm the director of cloud security for Altium 365. Ultimately Altium 365 is an electronics product design platform, allowing people to bring together all the aspects of PCB design, as well as helping organizations to build better products faster.

Altium recently launched Altium 365 GovCloud. Tell us about this and how it's different from the standard platform.

Sure. GovCloud allows us to be more specialized with secure workloads, allowing us to work together with companies that deal with what we call CUI, which is controlled unclassified information, as well as ITAR and other requirements. So, Altium 365 GovCloud offers more compliance measures and certifications tailored to meet these government requirements.

That's where this secure workload started coming in with the cloud service providers, which many SaaS companies like Altium are utilizing to meet those infrastructure requirements. This allows

us to build a more secure platform locking down systems to meet those requirements. I think one of the biggest struggles with the cloud in general is its openness and aspects with open sources, right? So Altium 365 GovCloud gives us a better measure to let us know that the underlying infrastructure, which is critical for storing the data and all the other information, does meet those high standards.

[***Click to read the rest of this article.***](#)



Bruno Blasigh



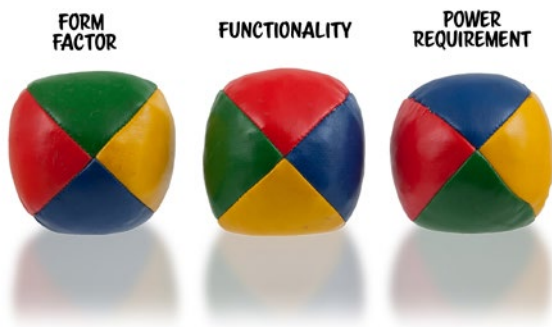
John Watson

Elementary, Mr. Watson: Where Have All the PCB Designers Gone?

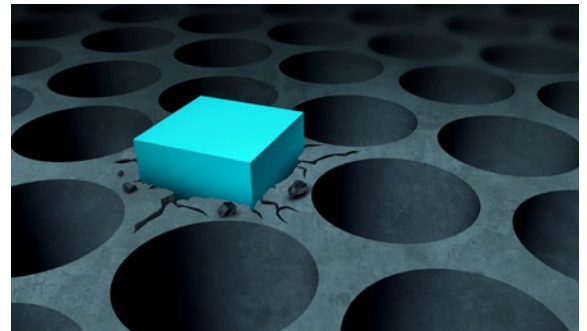
What are the biggest challenges in PCB design? Now, that's a loaded question, but one that I'd like to talk about. Before I do so, I think it's helpful to talk about challenges themselves, how we view them, how they affect us, and what we do about them. What one person perceives as a challenge may not be a challenge for another person.

Beyond Design: Balancing Trade-offs for Optimal PCB Design

As multilayer PCBs become more complex, PCB designers face the challenge of cramming more components and connections onto a limited board area without compromising performance or quality. Increasing the number of signal layers can help to accommodate more signal routing and reduce crosstalk, but there are inevitable bottlenecks in the breakout of high pin-count devices.



Connect the Dots: Avoiding Five Common Pitfalls of Parts



Ill-fitting parts can frequently cause delays and cost overruns, and undermine PCB performance, durability, and overall quality of the board. These poor results can be avoided. Here are five methods designers can implement to avoid common, parts-related manufacturability pitfalls.

Design Problems: From the Designers' Viewpoint

It seems like everyone has something to say about PCB designers and the way they do their jobs. Everyone involved in the process likes to chime in with advice for the front-end folks. But what do designers think about their segment of the industry? This month, we asked PCB designers and design engineers to discuss their biggest pain points.



Siemens Brings Real-time Supply Chain Intelligence to Siemens Xcelerator and the Digital Twin

Siemens Digital Industries Software announced that it is integrating the Supplyframe Design-to-Source Intelligence platform with its Siemens Xcelerator portfolio of software and services to bring robust real-time supply chain intelligence to the world's most comprehensive digital twin technology.

IEEE IMS Show: A High-Speed Designer's Paradise



For a PCB designer or design engineer, virtually all the sources for board raw materials were present on the IMS show floor: semiconductors, board material suppliers, fabricators, design bureaus, design tool vendors, EMS equipment manufacturers, solder, and more. Given that this is a microwave symposium, nearly all the exhibitors had a high-speed, RF story to share. RF and high-speed design challenges are in the forefront of everyone's thinking this week.

DFM 101: Cost Driver Summary

One of the biggest challenges facing PCB designers is in not understanding the cost drivers in the PCB manufacturing process. We will wrap up this DFM series with a summary of cost drivers that impact delivery, quality, and reliability. It is categorized by low-, medium-, and high-cost adders.



PCB Design Challenges—From the Fabricator's Viewpoint

If you're a fabricator, chances are you have a few things to say about at least a few of the PCB designs that make their way through your shop. I guarantee that you have several well-worn stories about designs that made you scratch your head and think, "Hmmm." So, in this section, we asked PCB fabrication experts to share their thoughts about challenges that PCB designers need to understand more thoroughly.

An Exclusive Review of the Institute of Circuit Technology's Annual Symposium

After a long crawl through heavy traffic on the M42 motorway, it was a great relief to exit at Junction 6 and arrive at the National Conference Centre for the 2023 Annual Symposium of the Institute of Circuit Technology on June 6. The conference center is co-located with the historic National Motorcycle Museum and situated in the heart of the UK midlands, a stone's throw from Birmingham International Airport.



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- Various Manufacturing

All interested candidates should contact Arlon's HR department at 909-987-9533 or email resumes to careers.ranch@arlonemd.com.

Arlon is a major manufacturer of specialty high-performance laminate and prepreg materials for use in a wide variety of printed circuit board applications. Arlon specializes in thermoset resin technology, including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, High Density Interconnect (HDI) and microvia PCBs (i.e., in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity, allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001: 2015 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customers' requirements.

For additional information, please visit our website at www.arlonemd.com

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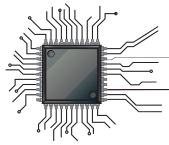
Are You Our Next Superstar?!

Insulectro, the largest national distributor of printed circuit board materials, is looking to add superstars to our dynamic technical and sales teams. We are always looking for good talent to enhance our service level to our customers and drive our purpose to enable our customers to build better boards faster. Our nationwide network provides many opportunities for a rewarding career within our company.

We are looking for talent with solid background in the PCB or PE industry and proven sales experience with a drive and attitude that match our company culture. This is a great opportunity to join an industry leader in the PCB and PE world and work with a terrific team driven to be vital in the design and manufacture of future circuits.

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Career Opportunities



MivaTek

Global

Field Service Technician

MivaTek Global is focused on providing a quality customer service experience to our current and future customers in the printed circuit board and microelectronic industries. We are looking for bright and talented people who share that mindset and are energized by hard work who are looking to be part of our continued growth.

Do you enjoy diagnosing machines and processes to determine how to solve our customers' challenges? Your 5 years working with direct imaging machinery, capital equipment, or PCBs will be leveraged as you support our customers in the field and from your home office. Each day is different; you may be:

- Installing a direct imaging machine
- Diagnosing customer issues from both your home office and customer site
- Upgrading a used machine
- Performing preventive maintenance
- Providing virtual and on-site training
- Updating documentation

Do you have 3 years' experience working with direct imaging or capital equipment? Enjoy travel? Want to make a difference to our customers? Send your resume to N.Hogan@MivaTek.Global for consideration.

More About Us

MivaTek Global is a distributor of Miva Technologies' imaging systems. We currently have 55 installations in the Americas and have machine installations in China, Singapore, Korea, and India.

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eptac

TRAIN. WORK SMARTER. SUCCEED.

Become a Certified IPC Master Instructor

Opportunities are available in Canada, New England, California, and Chicago. If you love teaching people, choosing the classes and times you want to work, and basically being your own boss, this may be the career for you. EPTAC Corporation is the leading provider of electronics training and IPC certification and we are looking for instructors that have a passion for working with people to develop their skills and knowledge. If you have a background in electronics manufacturing and enthusiasm for education, drop us a line or send us your resume. We would love to chat with you. Ability to travel required. IPC-7711/7721 or IPC-A-620 CIT certification a big plus.

Qualifications and skills

- A love of teaching and enthusiasm to help others learn
- Background in electronics manufacturing
- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

Benefits

- Ability to operate from home. No required in-office schedule
- Flexible schedule. Control your own schedule
- IRA retirement matching contributions after one year of service
- Training and certifications provided and maintained by EPTAC

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Career Opportunities



American Standard Circuits

Creative Innovations In Flex, Digital & Microwave Circuits

CAD/CAM Engineer

Summary of Functions

The CAD/CAM engineer is responsible for reviewing customer supplied data and drawings, performing design rule checks and creating manufacturing data, programs, and tools required for the manufacture of PCB.

Essential Duties and Responsibilities

- Import customer data into various CAM systems.
- Perform design rule checks and edit data to comply with manufacturing guidelines.
- Create array configurations, route, and test programs, panelization and output data for production use.
- Work with process engineers to evaluate and provide strategy for advanced processing as needed.
- Itemize and correspond to design issues with customers.
- Other duties as assigned.

Organizational Relationship

Reports to the engineering manager. Coordinates activities with all departments, especially manufacturing.

Qualifications

- A college degree or 5 years' experience is required.
- Good communication skills and the ability to work well with people is essential.
- Printed circuit board manufacturing knowledge.
- Experience using CAM tooling software, Orbotech GenFlex®.

Physical Demands

Ability to communicate verbally with management and coworkers is crucial. Regular use of the telephone and e-mail for communication is essential. Sitting for extended periods is common. Hearing and vision within normal ranges is helpful for normal conversations, to receive ordinary information and to prepare documents.

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APCT
Passion | Commitment | Trust

APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

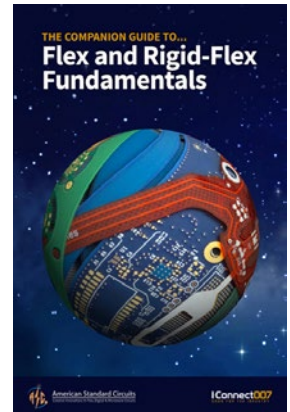
Thank you, and we look forward to hearing from you soon.

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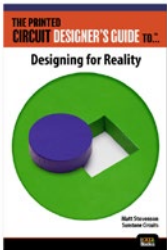
NEW!

THE COMPANION GUIDE TO... FLEX AND RIGID FLEX FUNDAMENTALS

I-Connect007 and American Standard Circuits are proud to announce the launch of the companion guide to the immensely popular *The Printed Circuit Designer's Guide to... Flex and Rigid-flex Fundamentals*. This short guide, written by topic experts at American Standard Circuits, is designed to provide additional insights and best practices for those who design or utilize flexible and/or rigid-flex circuit boards. Topics covered include trace routing options, guidelines for process optimization, dynamic flexing applications, rigid-to-flex transition and more. Visit I-007ebooks.com to download your copy.



I-007eBooks The Printed Circuit Designer's Guide to...



Designing for Reality

by Matt Stevenson, Sunstone Circuits

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by Michael Gay, Isola

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by Bill Hargin, Z-zero

Finally, a book about stackups! From material selection and understanding laminate data-sheets, to impedance planning, glass weave skew and rigid-flex materials, topic expert Bill Hargin has written a unique book on PCB stackups. [Download your copy today!](#)

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