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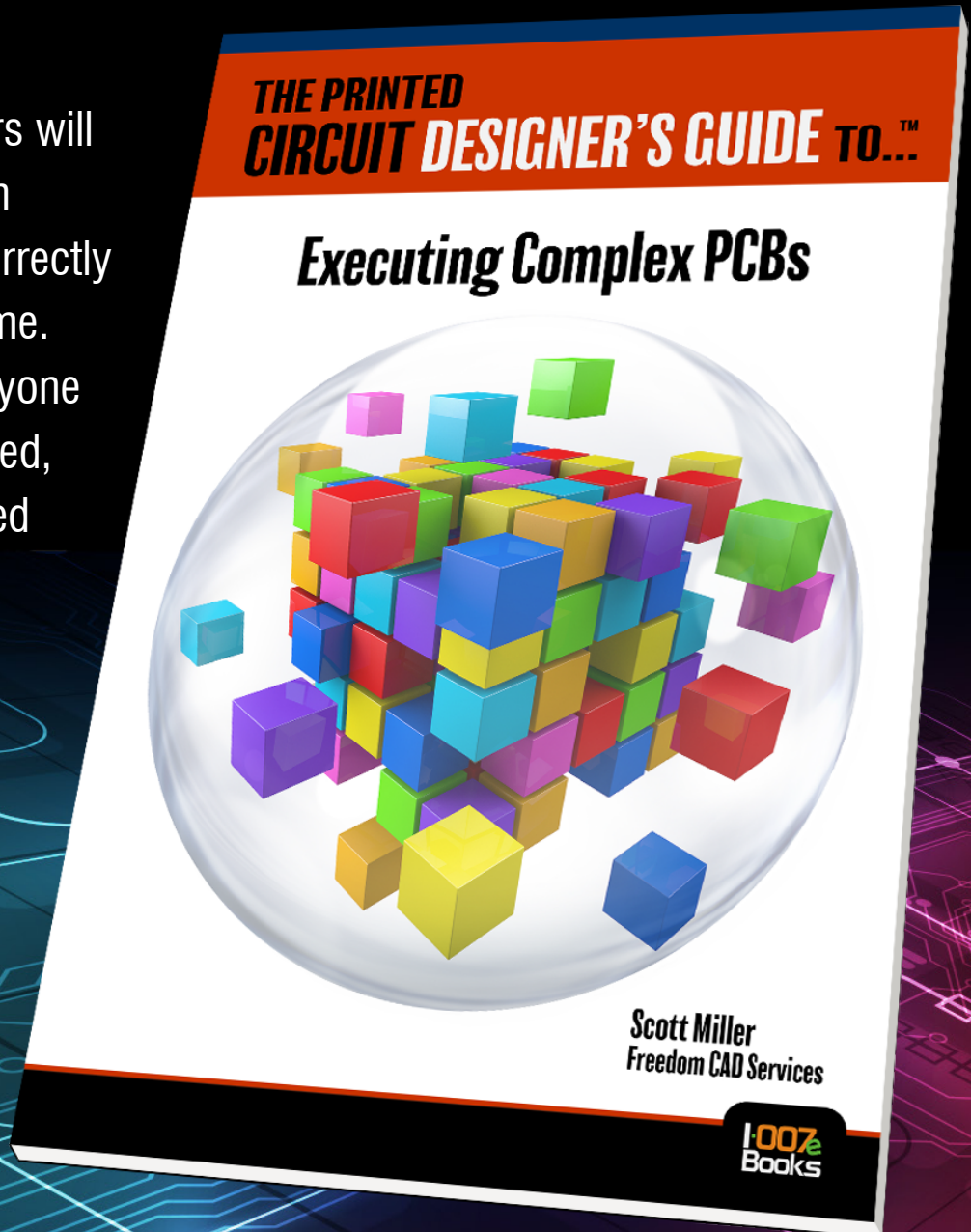


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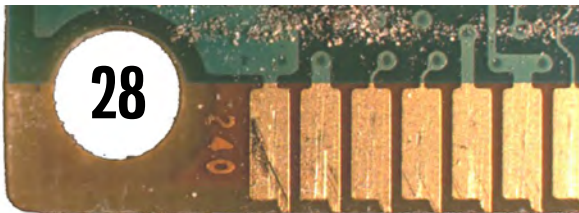
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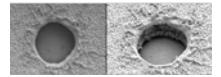
Our industry is embarking on a new age of technical development to achieve the reliability now required of the devices we fabricate. Reliability will be crucial to both our success and safety. We look at the latest developments in reliability improvement for PCB fabrication.



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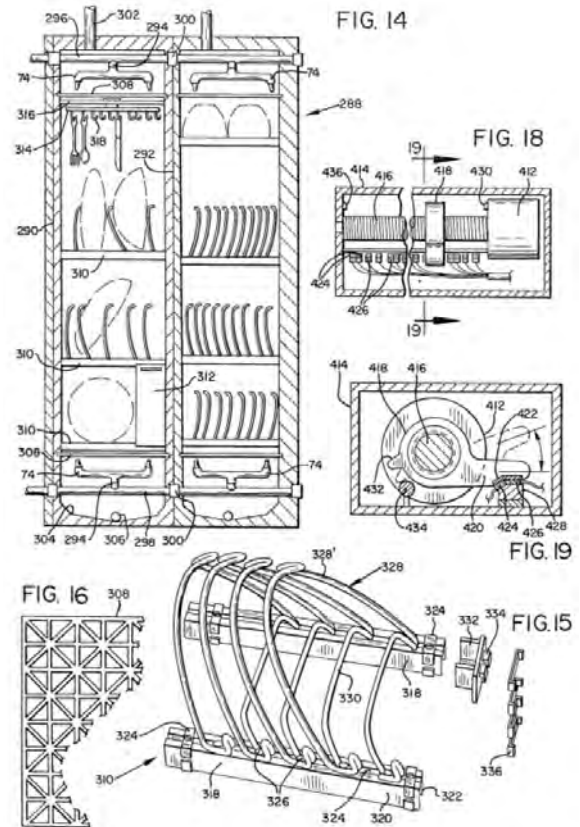
It All Comes Down to the Landing

Nolan's Notes
by Nolan Johnson, I-CONNECT007

My grandmother, Frances, was something. Some thought she was brilliant, and others were convinced she was full-blown crazy. She certainly was creative, though; nobody could argue that point. She spent almost 50 years designing and building a prototype self-cleaning house. She did not have an engineering degree; she was entirely self-taught. Over the years, she worked out all sorts of mechanical solutions and developed water-repellent materials and fabrics of her own formulation so that



Grandma Frances in her self-cleaning kitchen in 2002.



Detail of self-cleaning cupboard, a patented design held by Frances Gabe.

her home could simply shower itself clean. She lived in that prototype for 40+ years.

However, I have to say that when one detail started to go wrong, everything cascaded out of control very quickly. At one point, Frances made the dish cupboard do double-duty as the dishwasher; just put the dirty dishes back with the clean ones and wash them all, every time. If the cupboard malfunctioned, then a couple of dirty dishes would end up making a mess of everything. Later on, she just kept the dishes on a rack on the wall. To wash the dishes, you had to spray down the whole kitchen. Need-

less to say, most of the time, the house was like a rainforest. While some of her implementations may have been a bit impractical overall, her self-cleaning house was a reliable solution to her housecleaning problem in that it worked and she didn't have to.

And that's our theme for this issue—reliability in the products that we turn out for use in the world. Of course, to talk about reliability, we also have to talk about the failures we're trying to avoid. Grandma Frances had a pacemaker that served her well for many years, triggering a heartbeat something like 800 million times while keeping her alive—and creative—longer.

A demonstration of a very different level of reliability is illustrated on this month's cover. Falcon Heavy's reusable side boosters are shown landing in unison at Cape Canaveral Landing Zones 1 and 2 following a SpaceX test flight in February 2018.

Our industry is embarking on a new age of technical development to achieve much higher levels of overall reliability that will be required of the devices we fabricate. Medical devices will be relied upon to keep us living in many more situations. Autonomous vehicles will need to be failure-free to keep riders and pedestrians alike safe in the world. IoT will bring opportunities to put smart electronics in new places, performing in unthought-of ways. Reliability will be crucial to both our success and safety.

Right now, it's hard to avoid the conversation. Recently, IPC hosted the IPC High-Reliability Forum and Microvia Summit in Baltimore, Maryland—two full days of discussion on how to increase reliability. I-Connect007 sent Design007 Managing Editor Andy Shaughnessy to cover the event.

"The conference in Baltimore was solid with attendance up from last year," said Shaughnessy. "The big topic at the conference was mil/aero microvia failure and the investigations by Motorola and other members of the IPC V-TSL-MVIA subcommittee. By the way, that committee would love to have more input from the industry if you're able to share your company's data on microvia failures."

Thus, we look to those conversations for this issue. We start with Jerry Magera and J.R. Strickland who set the tone with their technical article titled "Microvias: Links of Faith Are Not Created Equally." Right on their heels is research from Paul Wang, et al., into "Interconnect Reliability With System Design and Transportation Stress." Completing the technical hat trick, Mike Konrad discusses "How Changing Cleaning Technologies Affect Reliability" with Andy Shaughnessy.

Columnist Todd Kolmodin changes up the pace with his column, "What Do You Mean 'Passed' Isn't Enough?" NCAB's Jeff Beauchamp brings us "A Guide to High-reliability PCBs From Design to Specification," and Mike Carano's column moves into part four on "Moving Into Microvias."

In another interview, Andy Shaughnessy talks with Terry Munson about avoiding CAF failures. And columnist Steve Williams files an interview with Prototron's Van Chiem on the topic of reliability. Tara Dunn continues the theme with "When You Do Everything Right and Something Still Goes Wrong."

Gardien's Todd Kolmodin (in addition to his column in this month's issue) goes deeper into the feedback loop between post-fab test and ongoing design optimization in his article, "How to Feed Test Data Back to Engineering for Process Improvement." And Didrik Bech discusses how to "Avoid Failures in PCB Production with Compliance Control." Finally, Marc Ladle holds onto his column's anchor position with a visit to and a discussion of Huawei's influence on the community of Dongguan, China.

My grandmother's self-cleaning house may have been reliable for her, but it was never ready to take over the world. However, the products we build for our customers (SpaceX included) will. So, dive into this issue with us and we'll all stick the landing. **PCB007**



Nolan Johnson is managing editor of *PCB007 Magazine*. Nolan brings 30 years of career experience focused almost entirely on electronics design and manufacturing. To contact Johnson, [click here](#).



Microvias: Links of Faith Are Not Created Equally

Feature by Jerry Magera and J.R. Strickland
MOTOROLA SOLUTIONS INC.

Abstract

Microvias connect adjacent copper layers to complete electrical paths. Copper-filled microvias can be stacked to form connections beyond adjacent copper layers. Staggered microvias stitch adjacent copper layers with paths that meander on the layers between the microvias. Both microvia configurations are formed by essentially the same sequential operations of laser drill, metallization, and patterning, using various chemical, mechanical, and thermal treatments to form each layer, one over the other. Stacked microvias must be filled while staggered microvias do not. Process specifics differ from manufacturer to manufacturer. Stacked microvias fracture during reflow assembly while staggered microvias do not. Assembly reflow subjects the printed wiring board (PWB) to the greatest temperature excursion. Stacked microvias with a weak interface fracture during assembly reflow and are a hidden reliability threat. This phenomenon

was reported in IPC-WP-023 ^[1] in May of 2018. IPC-TM-650 Method 2.6.27A is a performance-based PWB acceptance test that detects fractured microvias. SEM pictures are presented to initiate discussions in the search for the root cause. Included are cross-section images of completed microvia structures, SEMs after laser drill, and after electroless copper. Not all stacked microvias fail. To learn why, microvia samples were collected from different PWB suppliers. Microvias drilled by UV lasers are compared to microvias drilled by other laser configurations. The images show that microvia structure was influenced by laser type. This article discusses the various laser-drilled microvias and presents SEM photographs to begin the search for the root cause of weak copper interface.

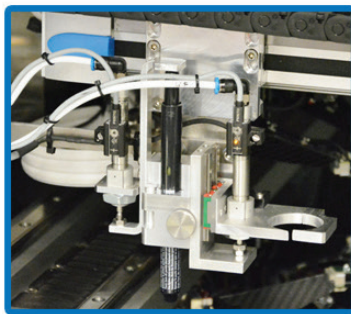
Introduction

The search for root cause in this article focuses on laser drill. Not all stacked microvias fail. To learn why, microvia samples drilled by UV lasers were visually compared to microvias drilled by other laser configurations. Samples

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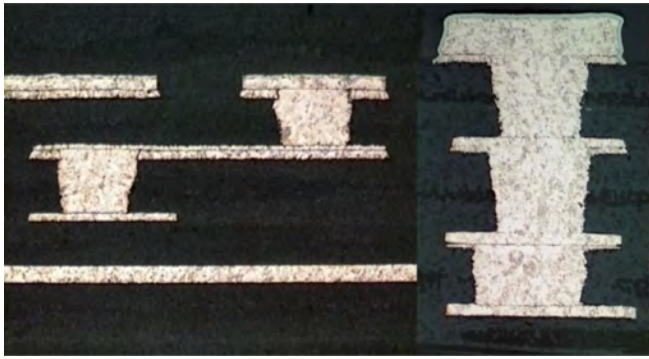


Figure 1: Cross-section of layer 1 to layer 3 staggered copper filled microvia and layer 1 to layer 4 stacked copper filled microvia. Cross-sections were polished and microetched to reveal copper structure.

were extracted after laser drill and after electroless copper. SEM analysis provided high-resolution views for comparison. The SEM pictures revealed that microvia structure was influenced by laser type.

Figure 1 shows a two-level staggered microvia and a three-level stacked microvia. Both configurations are used in PWBs; however, when both were used on same PWB, the stacked microvia failed during reflow assembly while the staggered microvia did not. The microvias were formed with a UV-CO₂ combo laser UV clean followed by desmear, electroless copper, and electrolytic copper fill.

Both stacked and staggered microvias must survive reflow assembly. A cross-section of a failed three-stack microvia shown in Figure 2 revealed a separation between the target pad and plated copper fill at both layers 2 and 4. The microvias were drilled with a UV laser followed by desmear, electroless copper, a copper strike, then copper fill. The UV laser ablation parameter was set to dig into the copper target

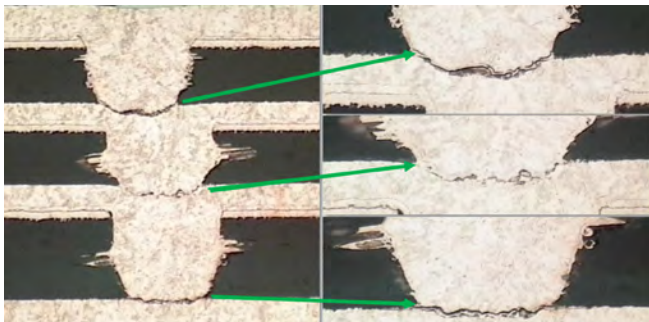


Figure 2: Cross-section of a three-stack microvia failure.

pad. The UV-drilled microvia failed during reflow assembly.

Figure 3 is SEM photograph of a UV laser-drilled, copper-filled microvia cross-section before assembly reflow. The copper-fill to target pad interface as shown is a complex structure that meanders into the layer 2 plated copper. Arrow (a) points to a UV laser-formed copper burr at the knee of the copper foil. Arrow (b) points to a thin demarcation that follows the copper fill to copper strike interface. Arrow (d) points to the electroless layer between the copper foil and electroplated copper. Arrows (c) and (e) point to interface features that are darker and coarser than the plated copper. The electroplated copper strike to electroless copper to target pad interfaces were obscured by the features created by the UV laser ablation.

UV laser-drilled stacked microvias failed reflow assembly more frequently compared to microvias drilled by other laser types. The difference was related to the UV laser created features present between the copper fill and target pad as shown in Figure 3. The features, only observed in UV laser-drilled microvias formed as copper melted and recast in the presence of air, coincide with the weak points that fracture

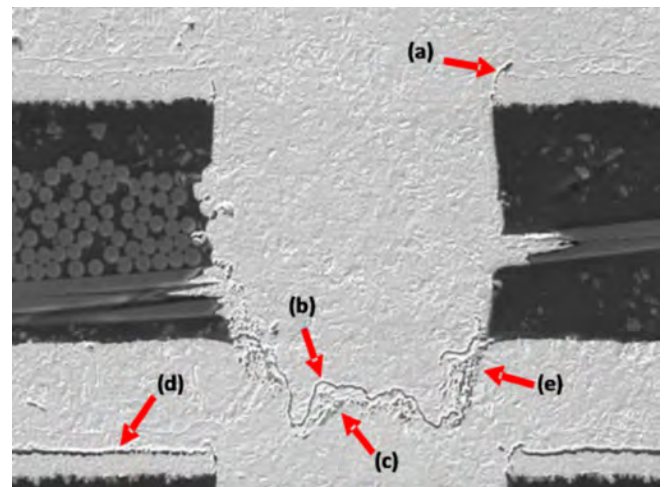


Figure 3: UV-only laser-drilled copper-filled microvia: (a) UV-laser-induced burr formed on copper foil; (b) Demarcation between copper fill and copper strike; (c) Feature with different texture compared to the plated copper; (d) Electroless copper layer between copper foil and electroplated copper; (e) Feature with texture different compared to the plated copper.

when thermally stressed during reflow assembly. The rest of this article presents SEM photographs of microvias after laser drill and after electroless copper to show the condition of the copper surface of the target pad produced by the commonly practiced laser processes.

Results and Discussion

The PWB manufacturing base uses different laser types, plating chemistries, and laminate materials in the manufacture of PWBs with microvias. A reliable stacked microvia depends on the condition of the target pad after the laser process. Laser drilling is the accepted method of forming microvias. UV Nd:YAG and CO₂ lasers were developed to drill microvias and are commercially available in four different configurations to the PWB industry.

1. UV Nd:YAG Laser

The UV laser can micro-machine a variety of materials, including copper and glass-reinforced dielectric laminate to produce unique features. The ability to ablate copper can potentially damage copper surfaces, such as the target pad of a microvia. SEM photographs of target pads touched by the UV beam show evidence of melted copper and copper particles that were explosively ejected from the melted copper surface. Copper flow patterns were visible on the target pad along with porosity and inclusions that were characteristic of the sputtering and recasting of molten copper. Molten copper flow patterns were visible over the surface of the target pad and the rim of the outer layer copper foil surrounding the microvia opening—basically any copper surface the UV beam contacted. Constructions require surface copper thickness thinner than target copper thickness to prevent the UV beam from piercing the target pad copper. In most constructions, UV copper ablation requires entry copper to be less than 0.5-oz. copper weight.

2. UV-CO₂ Laser

Referred to as a combination laser drill machine, it consists of a UV laser and a CO₂ laser. The UV laser first creates a window through the copper foil and slightly bites into the glass-

reinforced dielectric material. After the UV laser opens the copper window, the CO₂ laser then removes the remaining laminate material to expose the target pad. The copper target pad reflects the CO₂ laser beam, and the reflected photons collide with the incident photons at the copper surface. The photon interaction and reflection leaves a very thin resinous skin^[2] on the copper surface of the target pad that must be removed before the microvia is plated for a reliable connection.

Many manufacturers today add a UV target pad cleaning step to remove the residual film. The intensity of the UV laser cleaning step may adversely modify the target pad copper surface. It was observed that melted and recast copper features were produced around the rim and edge of the copper foil at the outer layer of the microvia, but this damage did not produce reflow-induced failures. The entry copper thickness is typically less than 0.5-oz. copper.

3. CO₂ with Chemically Etched Copper Window

A low-power CO₂ laser beam cannot ablate through reflective copper but can ablate glass-reinforced dielectric material. An opening must first be created in the copper foil to allow the CO₂ laser beam to drill a microvia. The window is created by imaging and etching the copper foil. The diameter of the copper window may be either less than or greater than the CO₂ beam diameter. The process practiced depends on the ability to register the CO₂ beam within the copper window and target pad, taking into account cumulative registration tolerance for material stretch and shrink. The CO₂ beam reflects off the target pad and leaves the characteristic resinous film that must be removed. Since copper windows are formed by a print-and-etch process, there is no restriction on entry copper thickness. The low-power CO₂ laser does not melt or recast target pad copper.

There are two etched window processes practiced. The conformal etched copper window process consists of an etched copper window diameter that is less than the CO₂ beam diameter, so the copper window defines the microvia diameter. The oversized etch copper

window process consists of an etched copper window diameter that is greater than the CO₂ beam diameter, so the CO₂ laser beam diameter defines the microvia diameter.

4. Laser Direct Drill With CO₂

The laser direct drill (LDD) process uses a high-power CO₂ laser to drill through thin, specially coated copper foil and through glass-reinforced dielectric. After piercing the entry copper, the CO₂ laser parameters are adjusted to reflect off the target pad; therefore, it does not melt or recast the copper surface of the target pad. The cut through the thin treated copper does leave the characteristic melted and recast copper feature around the rim of the outer layer copper foil. The entry copper foil must be less than 9- μ m thickness and treated to absorb the CO₂ beam.

After laser drill, a series of chemical operations remove the residue from the target pad left by the CO₂ laser. These operations will be covered in future papers.

Reflow-induced failures were observed to follow demarcations between the copper fill and target pad. Demarcations in microvias visually vary for different laser processes. Fig-

ures 4–6 provide examples produced by different laser processes. Figure 4 is a UV-CO₂-UV cleaned microvia stack, which failed in six reflow cycles. Figure 5, a UV-formed stack, failed in the first reflow cycle. Figure 6, an LDD CO₂ laser-drilled stack, survived 30 lead-free reflow passes with a peak temperature of 245°C.

Figures 7 and 8 are SEMs of a 0.003"-diameter microvia at 30° tilt and 1000x magnification. Figure 7 is after UV laser drill, and Figure 8 after electroless copper. The microvia was UV laser drilled in 0.5-oz. outer layer copper foil and 106 prepreg. Figure 7 shows the target pad condition after UV laser ablation. The copper surface of the target pad was modified. Also visible is a copper burr and scalloping on the rim of the outer layer copper. Spherical copper particles are attached to the microvia sidewall. Figure 8 is a picture taken after 40 μ m of electroless copper was deposited. An agglomeration of small spherical copper particles was trapped inside the microvia. Cracks are visible in the 40 μ m copper deposit. Features outside the target pad are interesting, but because failures were observed between the plated copper fill and the target pad, this investigation focused on the condition of the target pad im-

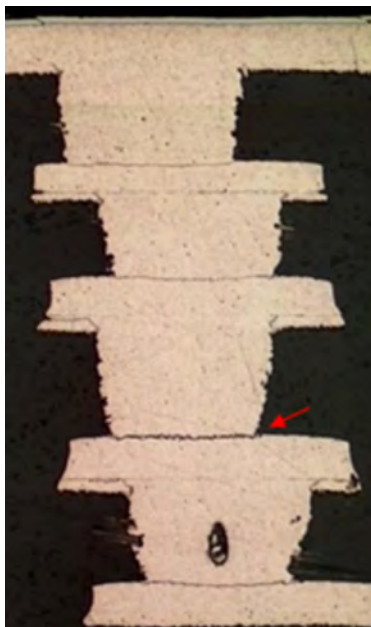


Figure 4: UV-CO₂-UV laser-drilled microvia stack that failed in six reflow cycles. Red arrow points to failure.

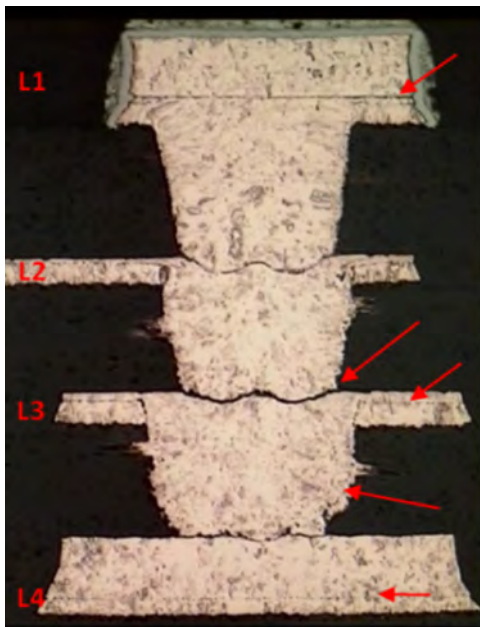


Figure 5: UV laser-drilled microvia stack that failed first reflow cycle. Red arrow at layer 3 points to failure.

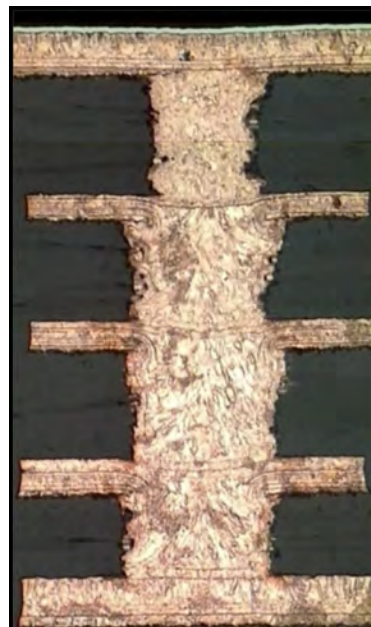


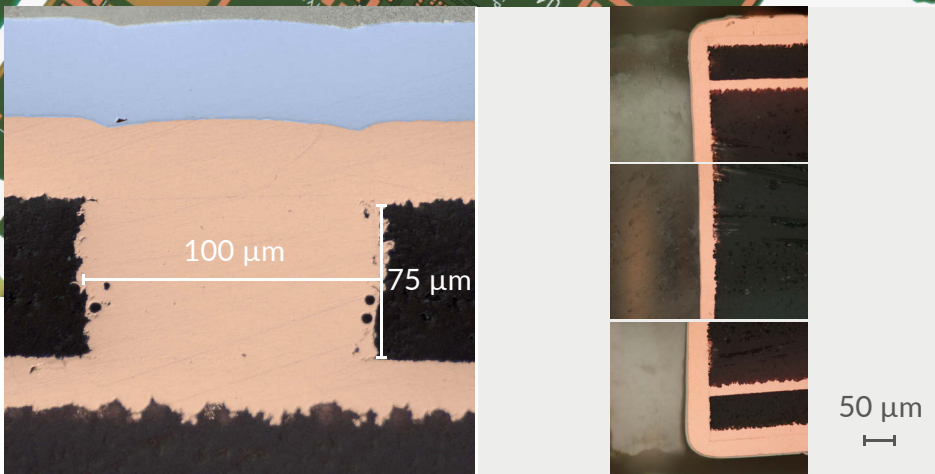
Figure 6: CO₂ laser direct drill microvia stack survived 30 lead-free reflow cycles.

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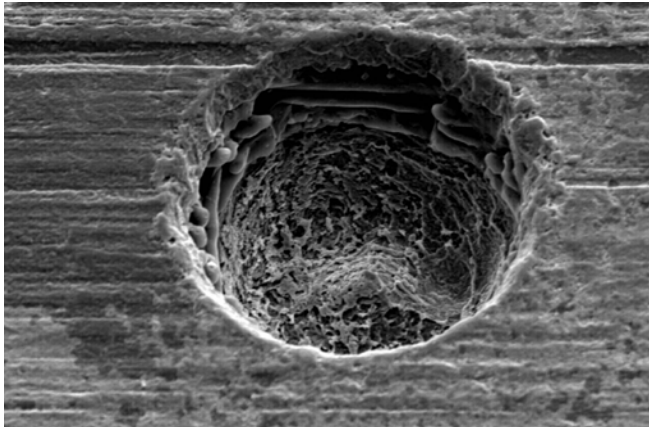


Figure 7: UV laser-drilled 3-mil diameter microvia at 30° tilt, 1000x magnification.

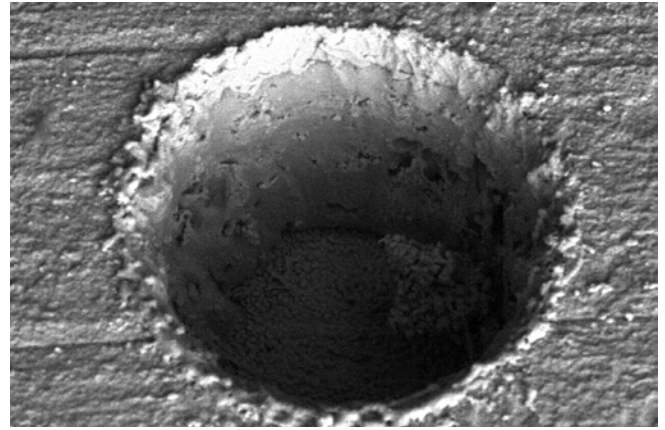


Figure 8: UV laser-drilled 3-mil diameter microvia after electroless copper at 30° tilt, 1000x magnification.

mediately after laser drill. As shown in Figure 7, a significant portion of the copper target pad was ablated away and left roughened by the UV beam. The manufacturer's UV laser process intentionally drilled into the copper surface to remove perceived contaminants before further processing.

UV laser parameters are selected by drilling test arrays of microvias that are assessed and judged by how visually clean the target pads appeared as viewed by optical microscopy. The diameter and copper appearance of the exposed target pad were compared to the microvia entry diameter and outer layer copper. The test array contained enough microvias to establish parameters aggressive enough to account for the variation in laminate glass content. Figure 9 shows examples of typical glass fabric yarn density. A 0.006"-diameter microvia drawn as a red circle is provided for reference. Glass density was greatest at fabric knuckle locations where warp and weft yarns overlapped, and least in the weave openings between the glass yarns. The variation in glass density in the beam path required parameters set aggressive enough to completely clear all the microvias and to accommodate localized material thickness variations typically encountered in multilayer panel fabrication. Material considerations ensure that some microvias receive too much laser energy.

The UV ablation of copper produced a visually modified copper target pad surface that failed frequently when used in stacked micro-

vias. SEM views of the ablated copper surface of the target pad revealed structures that looked like melted copper, copper flow patterns, sputtered copper, and recast copper [3]. The structures present in UV-ablated copper target pads are not present on target pads following CO₂ laser ablation. UV-ablated copper filled microvias were more fragile than those formed by other laser processes.

Figures 10 and 11 show two different UV-ablated microvias that compare different UV beam parameter settings and their effect on the target pad. In Figure 10, the UV beam settings produced a smoother target pad surface compared to the UV parameters used in Figure 11. In Figure 10, a concentric circular structure

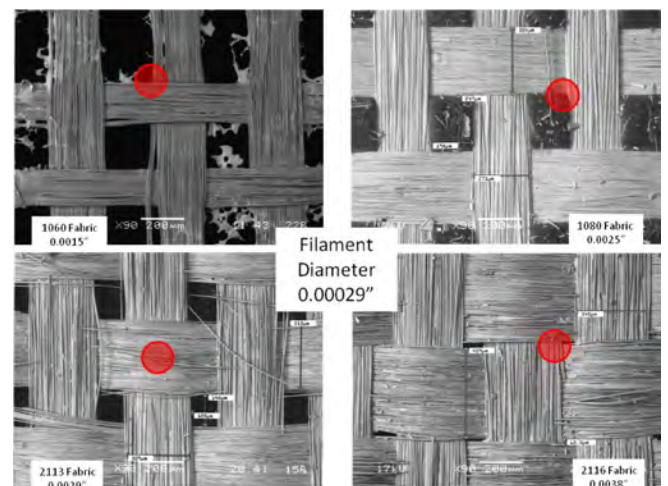


Figure 9: Typical glass fabric yarn styles used in microvia construction. The red circle represents a 6-mil diameter microvia for reference.

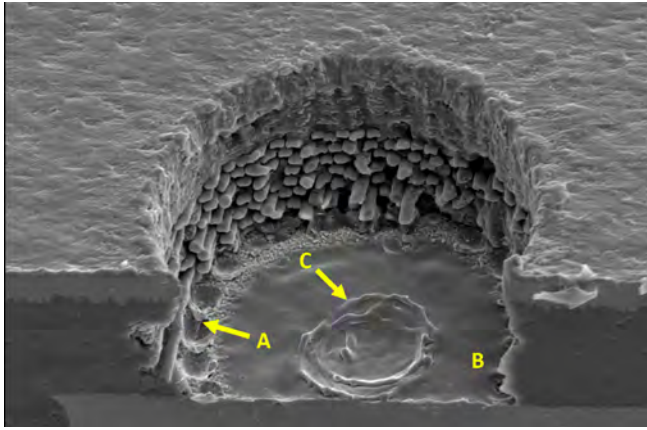


Figure 10: SEM SE (secondary electron) view of UV laser-drilled microvia with gentle UV ablation parameters.

is visible at location C that looks like copper waves propagating from the smoother copper B region. These features were produced by the action of the UV beam repeatedly trepanning in pulses over the copper target pad. Copper waves propagated from the center of the target pad as the beam repeatedly punched the central region. A chain of copper craters at arrow A located at the perimeter of the target pad follows the UV beam pitch pattern. Both pictures show that copper melted, flowed, and solidified to form these patterns. Similar copper melt structures were also present on the rim around the copper edge of the outer layer copper around the entrance of the microvia. The change in copper morphology by the action of the UV laser beam shown in the SEM pictures are the unusual features seen at the demarcation of Figure 3 associated with fractures. These features were only present on the target pads of microvias touched by the UV laser beam.

SEM analysis revealed more detail than optical microscopy. Additional SEM photographs were taken of samples fabricated by the UV-CO₂ laser, the CO₂ laser used in the etched oversized window and conformal mask processes, the CO₂ laser used in LDD, and the UV laser. The pictures are provided to inspire further discussion. Figures 12 shows views of UV-CO₂ laser-drilled microvias at 0° and 30° tilt. The UV laser initially opens a window in the copper foil and ablates a little bit into the epoxy glass (Figure 13).

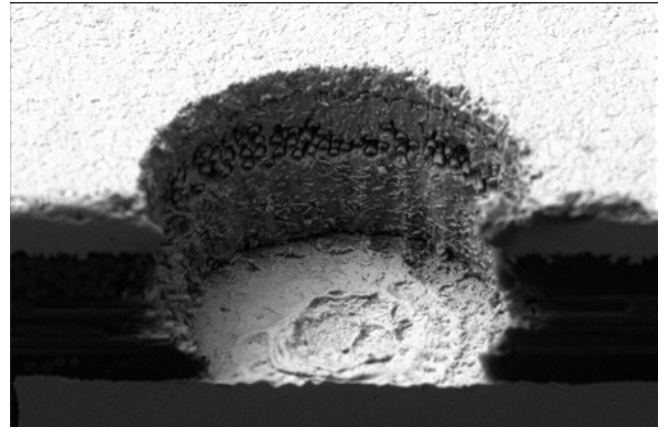


Figure 11: SEM BSE (backscattered electron) view of UV laser-drilled microvia with aggressive UV ablation parameters.

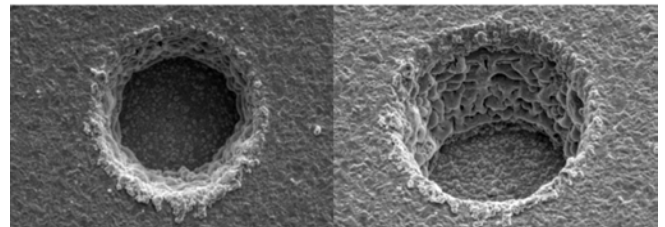


Figure 12: SEM SE view of UV-CO₂ laser-drilled microvia at 0° tilt (L) and 30° tilt (R).

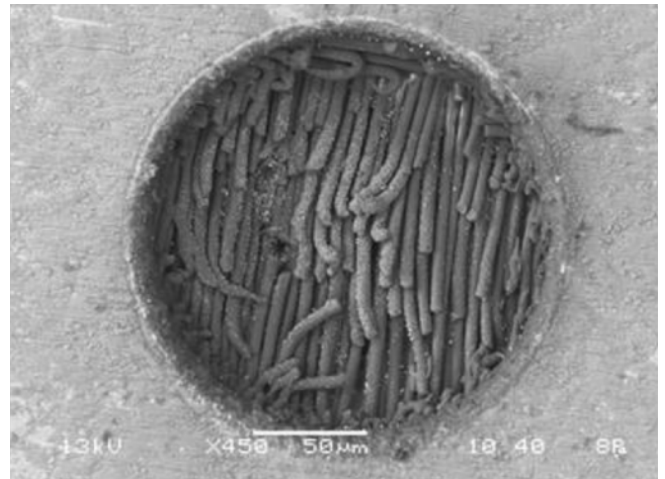


Figure 13: SEM SE view at 0° tilt of UV-CO₂ laser-drilled microvia after the UV laser drill step opened a window in the copper foil and before the CO₂ laser completes the microvia ablation to the target pad.

The CO₂ laser then removes the remaining epoxy glass material and leaves a very thin resinous film as it reflects off the copper target pad [2]. The initial UV laser step leaves a copper burr of melted and recast copper as it clears

the foil copper. A burn mark is visible on the outer layer copper foil surrounding the microvia. Copper droplets and spheres were also scattered on and around the microvia. Some of the tips of the glass fibers were melted and fused together. The target pad was undisturbed because the UV laser never touched the target pad.

Figure 14 shows views after desmear and electroless process of a microvia from the same manufacturer. The process did not remove the melted and recast copper burr from the rim of the microvia opening. After desmear, the glass fibers protruded more from the microvia sidewall. The glass fabric influenced the texture of the sidewall because of the localized glass fiber density. No visual copper anomalies were seen on the target pad.

Figure 15 shows microvias from a manufacturer that etched a 245- μm oversized copper window in the copper foil and then drilled the microvia with a 100- μm diameter CO_2 laser. The oversized window exposed the laminate to allow the CO_2 laser to drill the microvia. The 245- μm copper window was slightly smaller than the 250- μm capture pad that eventually capped the filled microvia. The copper surface and rim of the chemically etched copper foil were clean and well defined since no UV laser

was used. This process exposed a substantial amount of bare laminate around the microvia. There was some discoloration visible on the target pad, but no melted and recast copper damage. The discolorization was due to a thin residual film that remained on the target pad surface. This phenomenon occurs in all CO_2 laser processes.

Shown in Figure 16 are views of the oversized window with the CO_2 laser-drilled microvia after desmear and electroless copper.

Desmear removed the thin resin film from the target pad, caused the glass fibers to protrude more from the microvia sidewall and increased the resin texture exposed in the copper window. Electroless copper plated directly over the bare laminate inside of the window. Most of the capture pad formed over the bare laminate with only a small portion overlapping the copper foil. Chemically deposited copper-to-laminate adhesion is less than the adhesion of laminated copper foil. The diameter of the window was selected to accommodate the cumulative alignment tolerance necessary to make sure the CO_2 laser-drilled the microvia within the window. No target pad melting and recast of copper was visible.

Figure 17 shows views of a CO_2 laser-drilled microvia through a conformal copper mask. The copper etched window diameter in this process was the same or slightly smaller than the CO_2 beam diameter. No laminate surface was exposed. The window masked the oversized CO_2 laser beam and therefore defined the microvia diameter. The edge and surface of the copper foil were clean and well-formed since copper was not melted and recast. No target pad melted and recast copper was visible.

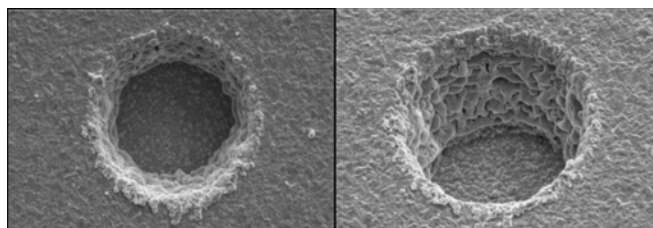


Figure 14: SEMs SE view at 0° tilt of UV- CO_2 laser-drilled microvia after desmear and electroless process at 0° tilt (L) and 30° tilt (R).

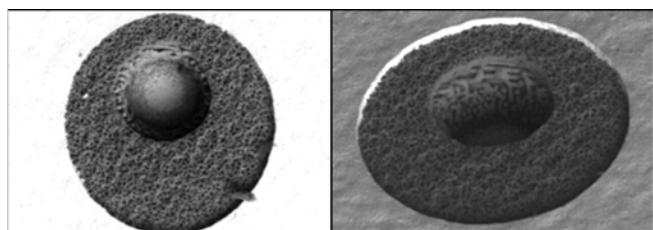


Figure 15: SEM view of CO_2 laser-drilled microvia inside chemically etched oversized copper window at 0° tilt (L) and 45° tilt (R).

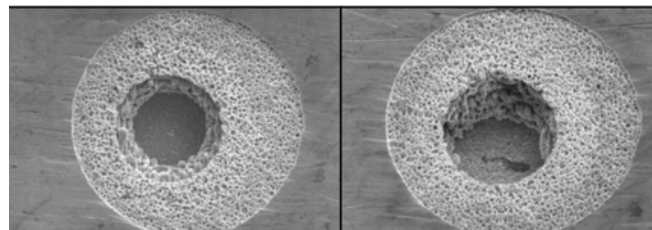


Figure 16: SEM view of CO_2 laser-drilled microvia inside chemically etched oversized copper window after desmear and electroless copper at 0° tilt (L) and 30° tilt (R).

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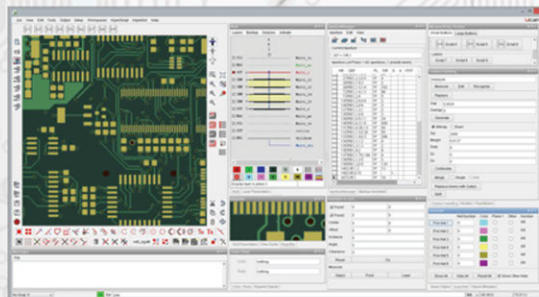
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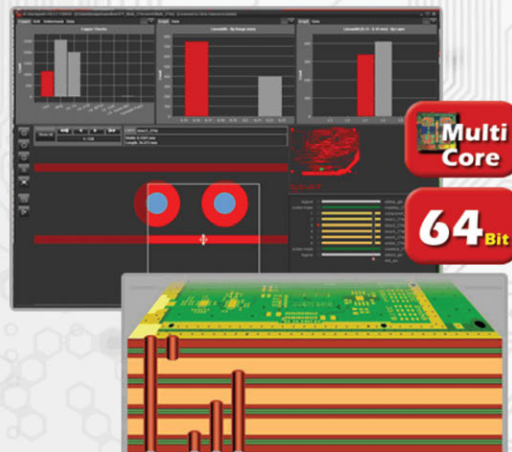
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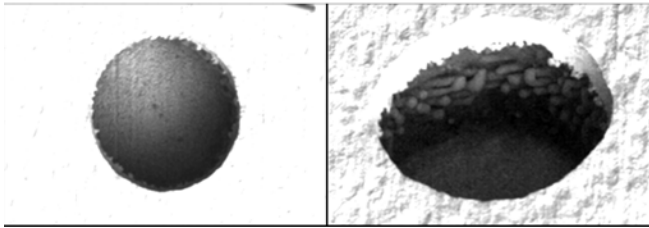


Figure 17: SEM view of CO₂ laser-drilled microvia aligned to a chemically etched conformal copper window at 0° tilt (L) and Figure 17. SEM view of CO₂ laser-drilled microvia aligned to a chemically etched conformal copper window at 0° tilt (L) and 45° tilt (R).

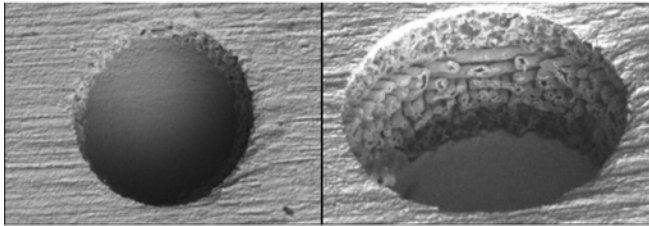


Figure 18: SEM view of CO₂ laser-drilled microvia aligned to a chemically etched conformal copper window after desmear and electroless copper at 0° tilt (L) and 45° tilt (R).

Figure 18 shows views of the CO₂ laser-drilled microvia through the conformal mask process following desmear and electroless copper metallization. After desmear, the glass fibers appeared to protrude more from the microvia sidewall. The electroless copper deposit peeled from the melted tips of the glass fibers. No laser-induced copper target pad modification was visible.

Figure 19 shows views of the CO₂ LDD microvia process. The microvia was formed by direct CO₂ laser ablation through oxide treated 9 micron thick copper foil. The microvia diameter and roundness depended on the CO₂ beam diameter and quality. In this case, the outer layer copper foil showed melted and recast copper surrounding the microvia opening, but no CO₂ laser-induced melting and recast of copper on the target pad.

Figure 20 shows the CO₂ LDD microvias after mechanical brush scrub, desmear, and electroless copper metallization. The brushing operation was completed after laser drill and was necessary to remove the surface oxide before the next process to prevent contamination of equipment and chemistry. Brushing was also the best

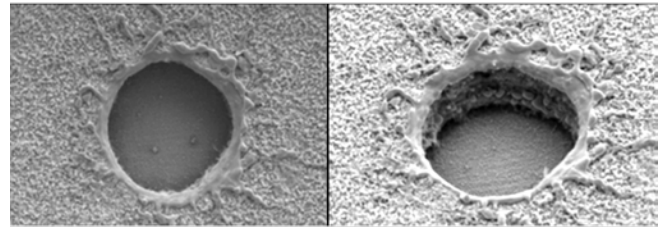


Figure 19: SEM view of CO₂ laser direct-drilled microvia through oxidized 9-mm copper foil at 0° tilt (L) and 45° tilt (R).

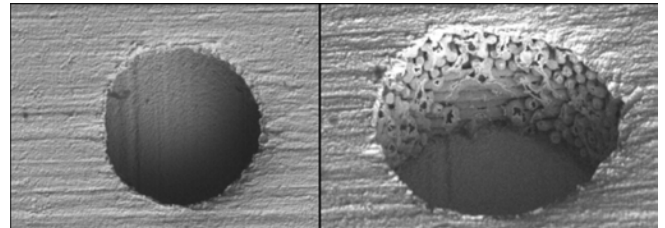


Figure 20: SEM view of CO₂ laser direct-drilled microvia through oxidized 9-mm copper foil after mechanical brush scrub, desmear, and electroless copper at 0° tilt (L) and 45° tilt (R).

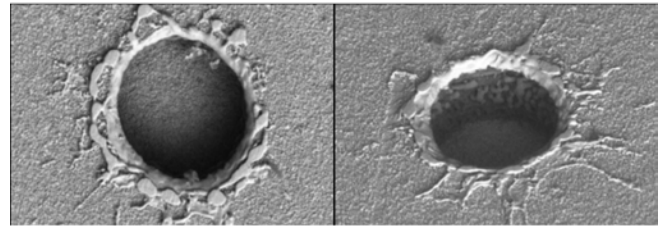


Figure 21: SEM view of CO₂ laser direct drilled microvia through oxidized 9-mm copper foil from another supplier illustrating variation in beam quality at 0° tilt (L) and 45° tilt (R).

practical method to remove the melted and re-cast copper that surrounded the microvia. The brushing process left directional brush marks in the copper foil. Brush marks visible on the target pad were created before the current layer was laminated. No other CO₂ laser-induced copper target pad modification was visible.

Figure 21 shows views of a CO₂ LDD laser-drilled microvia from another supplier. A similar process was used to oxide the copper foil. The roundness of the microvia was directly related to the roundness and uniformity of the CO₂ laser beam. A substantial amount of ablated outer layer copper was melted and recast around the rim of the outer layer of the mi-

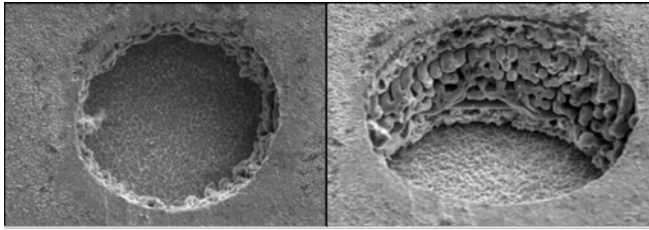


Figure 22: SEM view of CO₂ laser direct-drilled microvia through oxidized 9-mm copper foil after mechanical brush scrub, desmear, and electroless copper at 0° tilt (L) and 45° tilt (R).

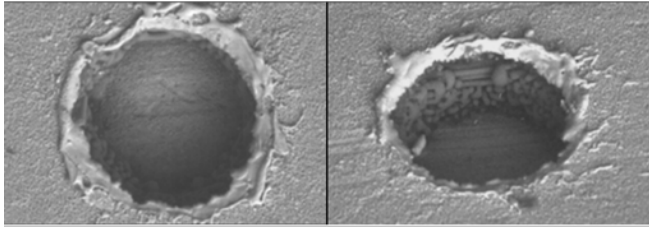


Figure 23: SEM view of CO₂ laser direct-drilled microvia through oxidized 9-mm copper foil from another supplier illustrating better beam quality at 0° tilt (L) and 45° tilt (R).

crovia. No CO₂ laser-related melted and recast copper was visible on the target pad.

Shown in Figure 22 are images of the CO₂ LDD drilled microvia after desmear and electroless metallization. No copper foil brush marks were visible from the deburr process used to remove the surface oxide and the laser formed copper burr.

Figure 23 shows a microvia from another supplier's CO₂ LDD microvia process. The outer layer copper foil was oxidized before LDD ablation. The microvia roundness was better than the CO₂ beam quality of the previous supplier's LDD formed microvia. Melted and recast copper were formed around the rim of the outer layer copper.

Figure 24 shows the CO₂ LDD drilled microvia after desmear and electroless copper. No brush marks were visible following the deburr process used to remove the oxide and recast copper burr. However some of the copper foil around the rim was damaged, which changed roundness of the microvia. No melted and recast copper anomalies were formed on the target pad.

Figure 25 shows CO₂ LDD microvias from another supplier. A substantial amount of melted

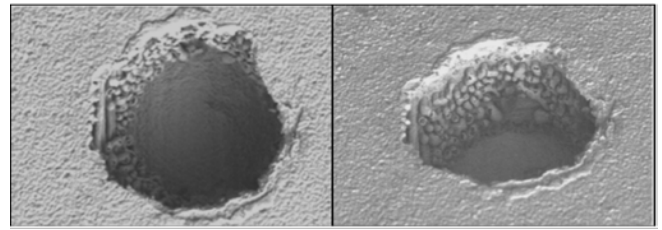


Figure 24: SEM view of CO₂ laser direct-drilled microvia through oxidized 9-mm copper foil after mechanical brush scrub, desmear, and electroless copper at 0° tilt (L) and 45° tilt (R) showing copper foil damage.

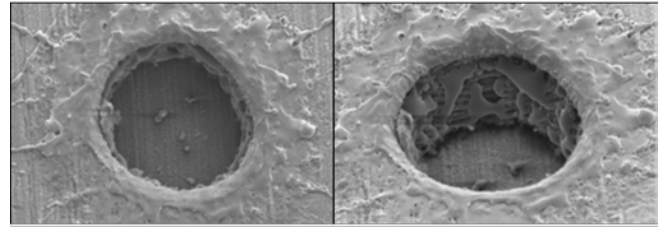


Figure 25: SEM view of CO₂ laser direct-drilled microvia through oxidized 9-mm copper foil from another supplier showing variation in degree of laser-induced surface copper recast at 0° tilt (L) and 45° tilt (R).

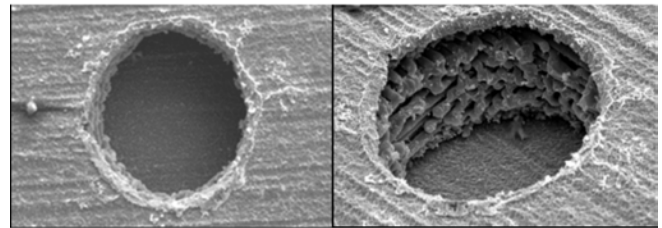


Figure 26: SEM view of CO₂ laser direct-drilled microvia through oxidized 9-mm copper foil after mechanical brush scrub, desmear, and electroless copper at 0° tilt (L) and 45° tilt (R) showing brush marks on the copper foil.

and recast copper was spread on the outer layer around the microvia.

The roundness of the microvia matched the CO₂ beam quality. The microvia sidewall shows melted and fused tips of glass fibers—a condition typically present with CO₂ laser ablation of glass-reinforced dielectric material. Brush striations can be seen on both the outer layer copper foil and target pad. No melted or recast copper was visible on the target pad.

Figure 26 shows SEMs of the CO₂ LDD microvia after desmear and electroless copper metallization. Brush marks were still visible.

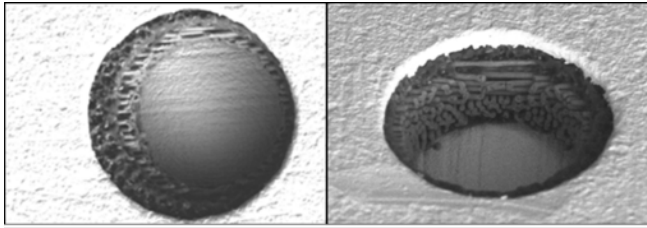


Figure 27: SEM view of CO₂ laser-drilled microvia inside slightly oversized chemically etched copper window illustrating degree of alignment at 0° tilt (L) and 45° tilt (R).

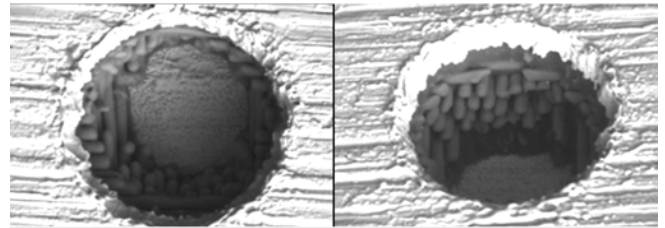


Figure 29: SEM view of UV laser-drilled microvia with parameters minimizing target pad damage at 0° tilt (L) and 45° tilt (R).

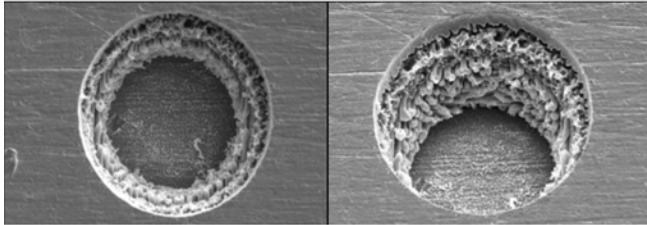


Figure 28: SEM view of CO₂ laser-drilled microvia inside slightly oversized chemically etched copper window after desmear and electroless copper at 0° tilt (L) and 45° tilt (R).

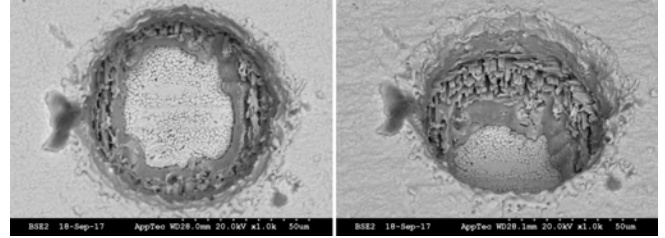


Figure 30: SEM view of UV laser-drilled microvia after desmear and electroless copper at 0° tilt (L) and 45° tilt (R). Example of microvia formed in location crossing glass yarns.

Figure 27 shows SEMs of a microvia that was CO₂ drilled within a slightly oversized copper etched window. In this process, the CO₂ beam diameter was only slightly smaller than the copper window diameter therefore the CO₂ beam defined the microvia diameter. The window diameter was smaller than the window diameter used in the process shown in Figure 15. Less laminate was exposed therefore a greater portion of the capture pad was formed over the copper foil, which provided a better anchor into the laminate. The chemically etched windows in copper foil did not require a deburr process. No melted or recast copper was produced on the target pad.

Figure 28 shows the oversized window and CO₂ laser-drilled microvia after desmear and electroless copper.

Figure 29 are SEMs of a UV laser-drilled microvia. The UV beam parameters were selected to minimize target pad damage. Just a small amount of UV-induced melted and recast copper was visible at 12:00 on the target pad in Figure 45. Substantial brush stroke striations were visible on the outer layer copper foil.

A small amount of melted and recast copper was visible around the rim of the microvia. No visible glass fibers were melted or fused together. Figure 30 shows the UV laser-drilled microvia after desmear and electroless copper metallization. Melted and recast copper was visible around the rim of the microvia. The desmear operation included a glass etch step that etched away a substantial amount of the glass fibers. No glass fibers were observed protruding from the microvia sidewall. Small cracks were visible in the electroless copper deposit on the microvia sidewall.

The gentler UV laser parameter left less melted and recast copper on the target pad and produced a greater microvia sidewall taper that substantially reduced the microvia contact area to the target pad. The UV laser parameters were set aggressively enough to account for the heaviest glass content and thickest dielectric variation across the laminate to make sure the microvia was fully formed. Microvia target pads located in the openings between the glass yarns and in thinner dielectric region received too much UV ablation.

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The SEMs in Figure 31 are of the UV laser-drilled microvia from another supplier. The images show a significant amount of melted and recast copper on the target pad. The rim of the outer layer copper foil was melted and recast. The laser beam pitch was visible on the rim and sidewall of the microvia.

Figure 32 shows the UV laser-drilled microvia after desmear and electroless copper. Some melted and recast copper is visible around the rim of the microvia. Also visible is the extent of melted and recast copper on the target pad.

Figure 33 shows pictures of a UV-CO₂ laser-drilled microvia. Melted and recast copper was visible around the rim of the outer layer copper foil and at the target pad. The tips of the glass fibers were melted and some were fused together.

Figure 34 shows the UV-CO₂ laser-drilled microvia after desmear and electroless copper. The UV laser did not drill a perfect circle. Also, there was some misregistration between the UV and CO₂ laser beams. The electroless copper deposit appeared to be cracking and flaking off the glass fibers.

Some melted and recast copper was visible on the target pad, which suggested either very aggressive initial UV parameters were used that allowed the UV beam to pierce the dielectric and hit the target pad, or a UV clean-up process was used after CO₂ ablation.

Figure 35 shows a UV-CO₂ laser-drilled microvia from another supplier. A melted and recast copper burr was formed around the rim of the microvia, but no melted or recast copper was observed on the target pad.

Figure 36 shows the UV-CO₂ laser-drilled after desmear and electroless copper. Electroless copper cracked and peeled off the melted tips and fused glass fibers.

The SEMs show that copper target pad surface structure is different for UV and CO₂ lasers. The UV laser leaves melted and recast copper on the target pad, but the CO₂ does not. The high-power CO₂ LDD laser does this only on the entry copper that is not the source of failures that form during reflow assembly.

Reflow-tested samples compared UV-CO₂ (supplier A) and UV (supplier B) laser-drilled

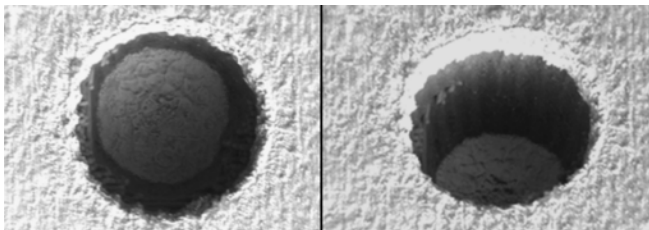


Figure 31: SEM view of UV laser-drilled microvia from another supplier with parameters that modified the morphology of target pad 0° tilt (L) and 15° tilt (R).

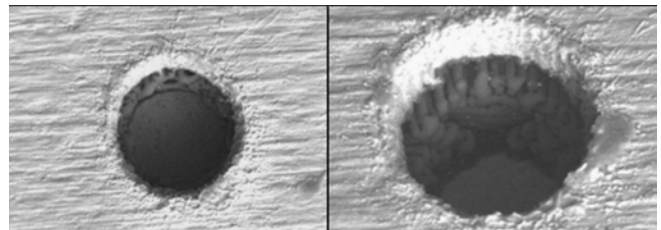


Figure 33: SEM view of UV-CO₂ laser-drilled microvia at 0° tilt (L) and 45° tilt (R) with recast copper around the rim of the UV-formed copper window.

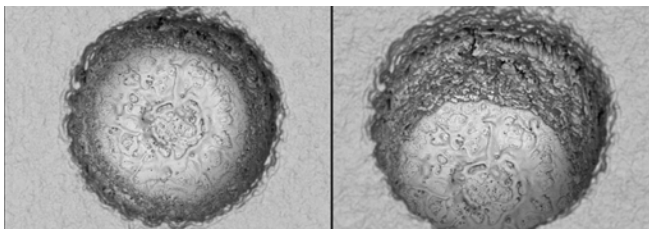


Figure 32: SEM view of UV laser-drilled microvia from another supplier after desmear and electroless copper at 0° tilt (L) and 15° tilt (R). UV parameter modified the morphology of the target pad.

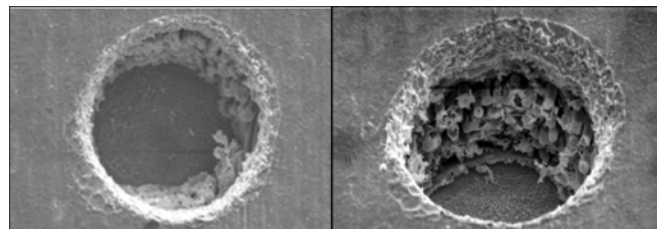


Figure 34: SEM view of UV-CO₂ laser-drilled microvia after desmear and electroless copper at 0° tilt (L) and 45° tilt (R). Example of slight misregistration between UV and CO₂ beams.

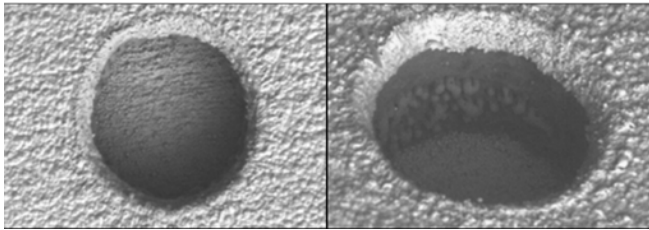


Figure 35: SEM view of UV-CO₂ laser-drilled microvia from another supplier at 0° tilt (L) and 45° tilt (R) with a recast copper burr around the rim of the UV-formed copper window.

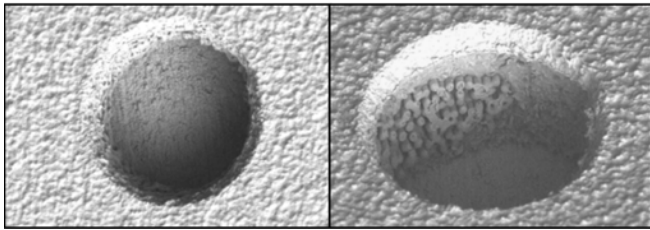


Figure 36: SEM view of UV-CO₂ laser-drilled microvia after desmear and electroless copper at 0° tilt (L) and 45° tilt (R).

microvias. Figure 37 shows probability plots comparing the two different laser-drilled microvia responses to reflow assembly thermal stress. Samples were subjected to 30 lead-free reflow cycles with peak temperature to 245°C. The Tg of the laminate was 175°C. The probability plot of temperature (L) recorded the temperature when an open was detected. The probability plot of reflows (R) plotted reflow cycles to failure. Both the mean failure temperature and cycles to failure for UV-drilled microvias failure were lower than means for UV-CO₂ laser-drilled microvias. These results suggest that UV laser-modified copper surfaces produced weaker microvia interfaces. This finding is important because many microvias formed by UV-CO₂ laser processes today add a UV laser cleaning step [4]. Unknown is the extent of change in copper morphology by the UV copper surface cleaning step and its effect on reflow survivability.

Conclusions

Stacked microvias solve PWB circuit congestion driven by increased silicon content, density of input/output paths to accommodate functionality, and smaller footprints. It was observed that fabricators’ ability to produce reliable stacked microvias varied. Stacked microvias fracture during the reflow assembly process. Stacked microvia fractures were observed at interfaces between the copper fill and target pad. Staggered microvias, however, did not fail.

Presented material focused on the visual condition of the copper surface of the target pad immediately after laser drill. There is significant variation in the final surface morphology of the target pad after laser drill among the different techniques used by PWB fabricators. UV lasers created visible copper morphology changes not observed with the various CO₂ laser processes. UV laser-modified

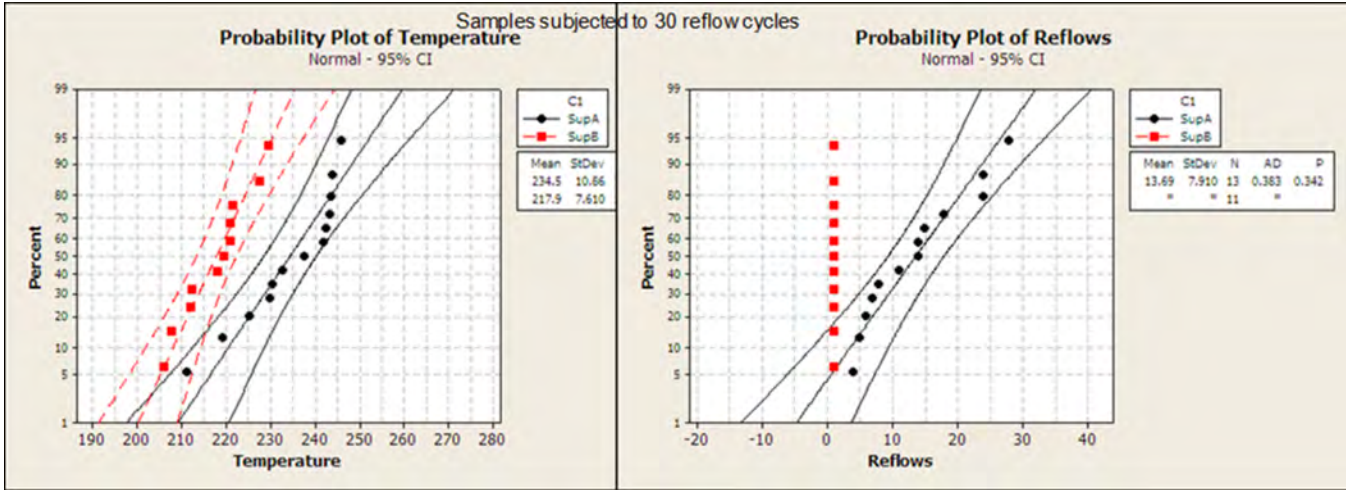


Figure 35: SEM view of UV-CO₂ laser-drilled microvia from another supplier at 0° tilt (L) and 45° tilt (R) with a recast copper burr around the rim of the UV-formed copper window.

copper morphology was reported to increase copper hardness and decrease ductility [3]. The features—those identified in the cross-sections and SEM photographs through which fractures formed and propagated during assembly reflow thermal stress—coincided with failures. Chemical species analysis at the copper surface of the target pad of an actual microvia after laser drill was not possible due to microvia sidewall, outer layer copper, and sample preparation interference. Further investigations are encouraged.

Probability plots of UV-CO₂ and UV laser-drilled microvias indicate the UV laser-drilled ones frequently fail during the first reflow pass while stacked microvias formed by CO₂ laser processes survived up to 30 reflow assembly cycles. This suggests the UV modified copper surface of the target pad results in a weak interface that fractures during reflow assembly.

Until the root cause of stacked microvia failures is determined and problem solved, staggered microvias must be used for mission critical and high-hazard environments. The window for staggered microvias is closing as the reduction in pitch and increased circuit density forces the use of stacked microvia constructions. **PCB007**

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A Tribute to Greg Beck

Recently, our industry lost one of its veterans—Greg Beck, owner of Beck's Light Gauge Aluminum Company. He passed away unexpectedly in Lake Zurich, Illinois, on May 2, 2019. He was a passionate and committed executive who built a successful business around thin-gauge steel and aluminum processing for high-technology applications.



The company was founded by George Beck, Greg's father, who was also very prominent in the industry. Last year, Greg and his company joined the Insulectro family of companies through acquisition. Greg's pioneering work with

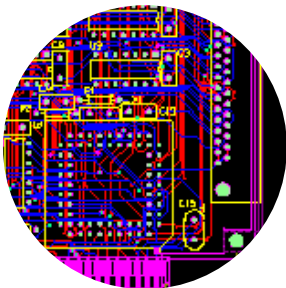
American-sourced aluminum was a perfect fit for Insulectro's line of business. We appreciated Greg's enthusiasm for the blending of the businesses and his guidance and direction as he stayed on to continue his extraordinary work.

"On behalf of all my fellow teammates, we celebrate Greg's life. We salute the successes Greg accomplished for our industry, and we pay tribute to his visionary legacy which will remain a guiding light in our business. Insulectro will name its light-gauge metal processing line in both our Chicago-area and our Orange County, California, facilities in honor of Greg," Insulectro President and CEO Patrick Redfern commented. "Our thoughts and prayers continue to be with Greg's family and friends, and the business colleagues who knew him and worked with him and recognized his genius." (Source: Insulectro)

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Interconnect Reliability Correlation With System Design and Transportation Stress



**Feature by Dr. Paul Wang, Vincent Weng,
and Dr. Kim Sang Chim**
MITAC INTERNATIONAL INC.

Abstract

Interconnect reliability—especially in BGA solder joints and compliant pins, which are subjected to design parameters—is very critical to ensure product performance at predefined shipping conditions and user environments. Plating thickness of the compliant pin and the damping mechanism of electronic system design are key success factors for this purpose. In addition, transportation and material handling process of a computer server system will be affected by shock under certain conditions. Many accessory devices in the server computer system tend to become loose, resulting in poor contact or solder intermittent interconnect problems due to the shock load from the transportation and material handling processes.

In this article, design variables—such as pin hard gold plating thickness, motherboard locking mechanism, and damping structure design—are experimented and reviewed. Also,

a shock measurement device is used to real-time monitor the acceleration, duration, and direction of shock in large stationary or moving systems in transportation and transferring process. There were two transportation routes from Fushan, China, to Sezimovo, Czech Republic, through the China and Russia border by train and returned by sea cargo through the Mediterranean, Arabic, and South China Seas in which a product package was embedded with a shock measurement device. The collected force data of g-force can be used to calculate the shock energy level, ΔV . The comparison between the value of ΔV and shock energy tested in the lab can be used to judge whether a system design can sustain and cause contact interconnect problems in the transportation and transferring process. These design variables and stresses can be evaluated by drop test or vibration test to ensure system functional integrity is achieved.

Introduction

Reliability of BGA solder joints and compliant pin interconnects is critical to ensure product performance is maintained at predefined



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Figure 1: Example of partial loose contact of a daughter card from a press-fit connector.

shipping conditions and user environments. Many electronic devices—such as network cards HDDs in the server system—tend to become loose, resulting in poor contact problems due to the severe shock from the transportation and material handling processes. Different design variables—such as hard gold plating thickness on the pin, motherboard locking mechanism, and damping plate—are experimented and reviewed in this article. A shock measuring device was used to monitor in real-time the acceleration, duration, and direction of shock in large stationary or moving systems in the transportation and transferring process.

Poor contact issues happened on some models of desktop, AIO, and server computer systems. After removing the top cover of a computer system, some accessories—such as memory and NIC cards—were found to be partially disengaged from their normal interconnect positions (Figure 1). An example of a contact inter-

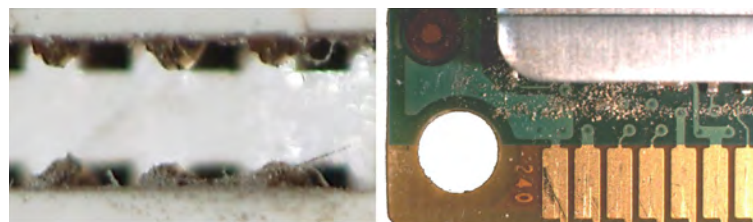


Figure 2: Dust and fiber accumulated in DIMM slot (L) and particles found near DIMM contact pads (R).

connect defect rate for a specific experimental test vehicle is shown in Table 1. In most of the cases, these contact problems may not be permanent but can be quickly resolved by double insertion of the interconnect system.

Although not the main topic of this study, another source of contact interconnect problems ^[1] is coming from particles or fibers from raw material, manufacturing, or the user environment can be observed from time to time in DIMM socket pins and circuit board contact pads. These foreign materials can create a barrier for proper contact between pad and socket (Figure 2). In one extreme case, soft white plastic particles were smeared on the contact surface, creating a risk of intermittent contact or open circuit (Figure 3). FTIR organic chemical analysis indicated that the fibers were rayon/cellulose, which is a common material from various sources—such as cloth and gloves—which are difficult to clearly implicate in a failure. However, the white particles are most likely polyethylene from plasticizer—a fatty acid that poses an interconnect concern (Table 2).

To avoid the accumulation of fibers and particles on contact pads, there are many changes required in environment control and management for sensitive interconnect devices, such

Model XXX to location Y	20xx/6 to 20xx/4	May	Jun	Jul	Aug	Defect Rate
Total tested Qty	2265	229	119	207	155	2975
HDD poor contact Qty	22(0.97%)	0	0	0	1(0.65%)	23(0.77%)
NIC/SSL poor contact Qty	8(0.35%)	0	1(0.84%)	0	0	9(0.30%)
Mem poor contact Qty	0	0	4(3.36%)	0	0	4(0.13%)
Cable poor contact Qty	1(0.04%)	0	0	0	0	1(0.03%)
Total poor contact Qty	31(1.37%)	0	5(4.2%)	0	1(0.65%)	37(1.24%)

Table 1: Defect rate of a series of computer server systems.

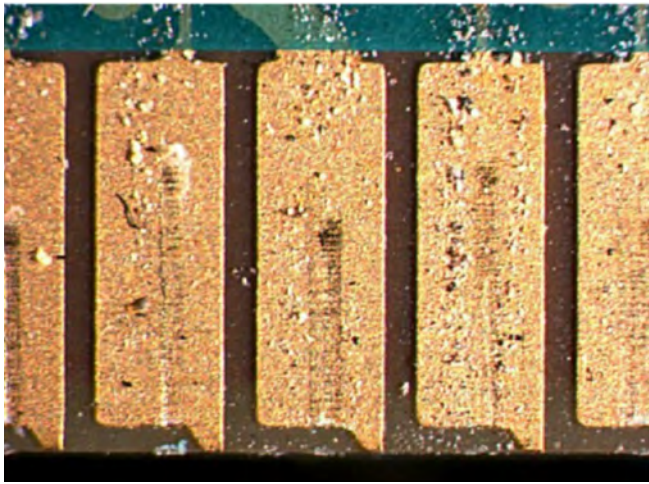


Figure 3: Close-up view of particles on DIMM contact pads.

as press-fit pins and optical modules. The use of particle counters is getting popular in particulate control on the manufacturing floor along with connector vacuuming, cleaning, and re-seating/inserting an edge card. Again, in most cases, these contact problems may not be permanent but can be quickly resolved by double insertion of the interconnect system to provide a clean contact interconnect interface.

Approach

In this study, a realistic test vehicle (Figure 4) is designed with a commercially available press-fit connector of various sources on to a motherboard with full electrical function. A riser card is plugged into the press-fit connector that serves as an interface for NIC and SSL card interconnect. The following three design variables were experimented on in addition to the pallet of test vehicles with an installed shock measurement device were shipped

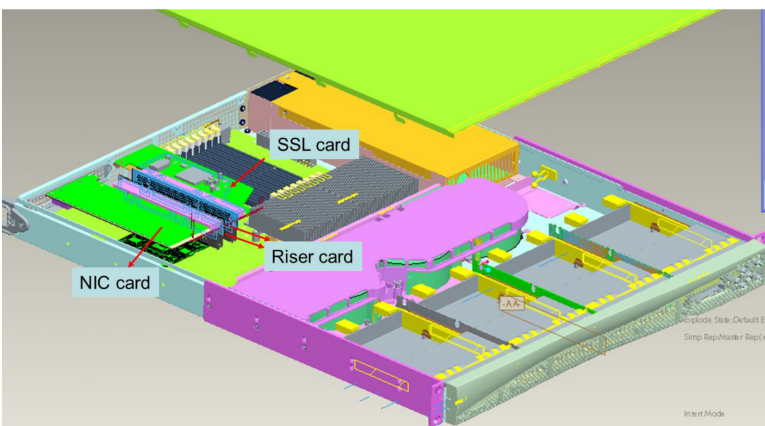


Figure 4: Test vehicle with press-fit connector and riser card interface for NIC and SSL interconnect.

through two shipping routes as train and sea cargo to see the correlation to the function failure of the test vehicle:

- Damping plate for NIC and SSL cards
- Hard gold plating thickness
- Locking mechanism for motherboard

Results and Discussion

Design Variable Change

Several design variables to improve the press-fit interconnect quality are considered to be tested in the shipping routes and during material handling. Some design changes were made specifically to solve the NIC/SSL poor contact issue.

First, the plating thickness in various press-fit connectors on the test vehicle is measured. As shown in Tables 3 and 4, the gold (Au) plating thickness on some connectors is in the 1-microinch range, and on the other, is more than

Visual Appearance	FTIR Match to Library	FTIR Attribution	Comment
Tan fiber	70%	Rayon/cellulose	Common material, multiple sources. Rarely causes a problem (at least that can be isolated.)
White particles	1. 92% 2. 91%	1. Ethyl triacontanoate 98 2. Polyethylene	1. Plasticizer, fatty acid, possible constituent of bulk; low melting point (soft), 0.86 g/cm3 2. Not common use in electronic components. Softness poses concern and is clearly engaged with contacts.

Table 2: Chemical analysis of foreign material on contact pads.

Cards	Model xxx	Plating	Model xxx	Plating	Model Y	Plating	Model X	Plating
Riser board	SN#ss(Riser PCB)	15μ"	SN#xxx-Riser PCBx8tox8	30μ"	SN#xxx Riser connector	1μ"	SN#xxx(Riser PCB)	30μ"
			SN#xxx-Riser PCB 8tox4	30μ"			SN#xxx(Riser connector)	1μ"
DIMM socket	SN#xxx	15μ"	SN#xxx	20μ"	SN#xxx	15μ"	SN#xxx	15μ"
	SN#xxx	15μ"	SN#xxx	20μ"				

Table 3: Hard gold plating thickness of various interconnect devices.

DESCRIPTION	PART	CONTACT PLATING	MODEL	SUPPLIER
TF-CON; SBU	64-BIT 184 PIN PCI-X	Gold Flash (1μ" gold min.)	A	1
	184 PIN	15μ" Gold min.	B	2
	184PIN	15μ" Gold min.	C	3
TF-CON; SBU	98 PIN PCI-X	30μ" Gold min.	D	4
	98 PIN PCI-X	30μ" Gold min.	E	5
	98 PIN PCI-X	30μ" Gold min.	F	6
TF-CON; SBU	164 PIN PCI-X	15μ" Gold min.	G	7
	164 PIN PCI-X	15μ" Gold min.	H	8
	164 PIN PCI-X	15μ" Gold min.	I	9

Table 4: Example of plating thickness of press-fit connector.

15 microinches. By comparing the Au thickness on the connector pins in Tables 2 and 3, it shows that the Au thickness on some connectors is only 1 microinch and is more than 15 microinches on other connectors. The Au thickness measured on the poor-contact NIC/SSL (Table 4) is also less than 15 microinches. It is thus seen that the probability of poor contact is much larger on connectors with 1-microinch Au plating than that on connectors with 15 microinches.

Second is the increase in damping plate area and thickness. In the original system, there were no damping plates on the riser card and NIC/SSL card. Changing the damping material from plastic to more elastic foam material helped to enhance the damping effect of the system to overcome external shock load. The new foam will continue in contact with the riser card with no gap between the foam and riser card. It can prevent the riser card from coming out of connectors under transporta-

tion stress. In the current design, the riser card was pressed by one plastic part and the NIC/SSL card were pressed by foam (Figure 5). The exact thickness of the foam damping plate is based on the following tolerance analysis.

The tolerance analysis (TA) conducted on the stack of mechanical parts indicates that there is some tolerance among different mechanical parts when the top cover is assem-

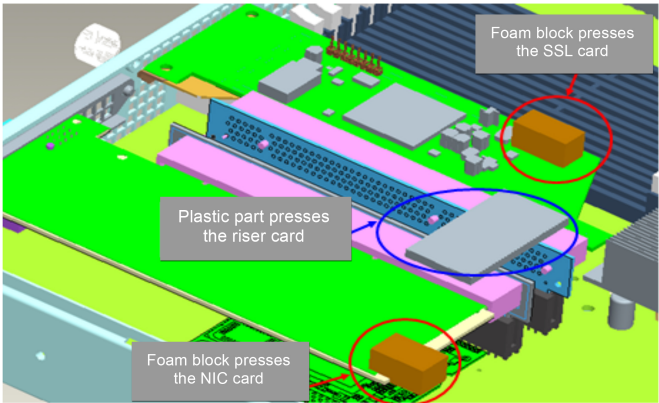


Figure 5: Foam plates added to enhance the damping effect.

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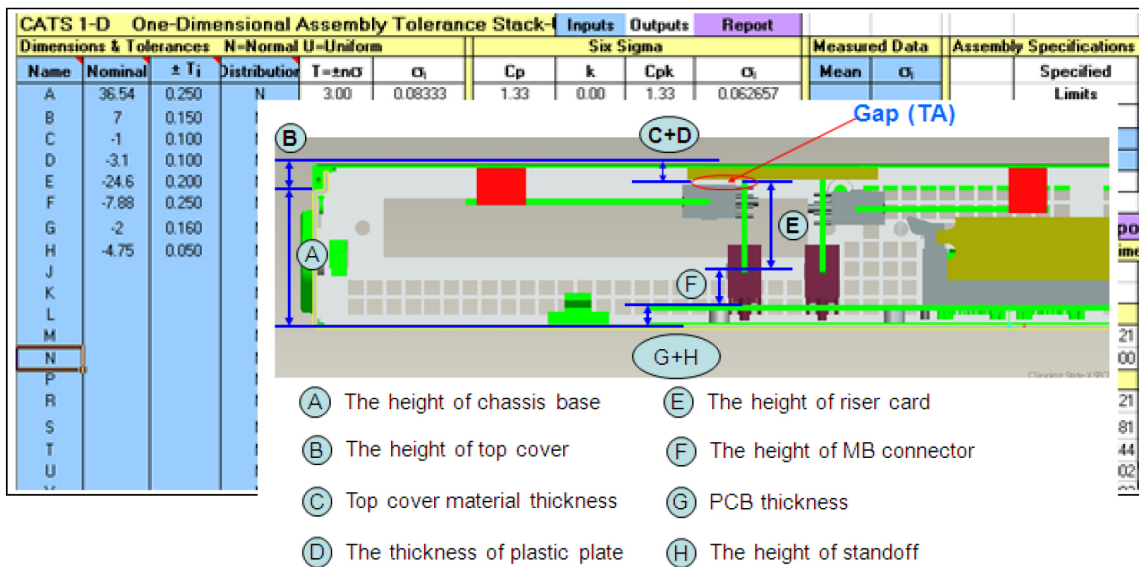


Figure 6: Tolerance analysis on a stack of mechanical parts.

bled, which results in a gap between the plastic plate and riser card. The gap is -0.277 mm minimum and 0.697 mm maximum. When the system is in shock, only one end of the riser card is pressed; the other end would lift. Based on this gap issue, the new design was adopted. In the new design, foam is used instead of the plastic sheet to press the riser card; the foam is thicker and the damping area is larger.

Figure 6 lists the difference between the current design and the new design. In the new design, the tolerance analysis shows that the gap between the foam and riser card is -1.927 mm minimum and -0.953 mm maximum. Therefore, no gap exists between the foam and riser card. The two can be firmly pressed. The foam

would be pressed tightly onto the top cover and would not lift the top cover due to its perfect elasticity with the change (Figure 7).

Third, although NIC/SSL is pressed by foam vertically, no protection is there horizontally. The jack that connects the riser card and NIC/SSL is also seated horizontally. When NIC/SSL is in shock, they may slip from the jack on the riser card, resulting in poor contact. Adding motherboard locking mechanism can help prevent the disengagement of NIC/SSL card from the riser card during the vibration of the motherboard. Figure 8 illustrates two plastic holders used to fix the NIC to prevent PCB swaying in transportation.

	Current design	New design
Detail		
Part material	Plastic	Foam
Thickness	3.1 mm	4.5 mm
Size	25*50 mm	50*110 mm

Figure 7: Damping material design and tolerance analysis.

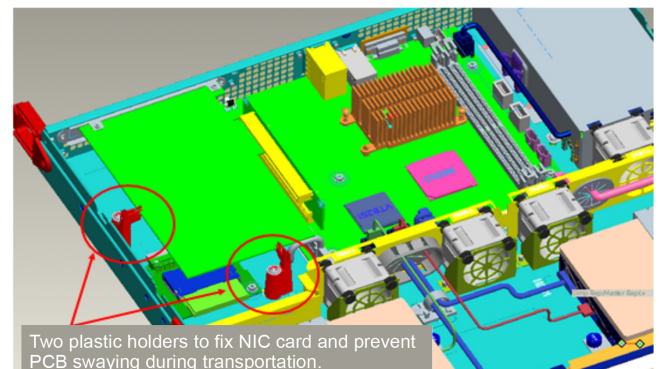


Figure 8: Board locking mechanism to restrain horizontal movement.

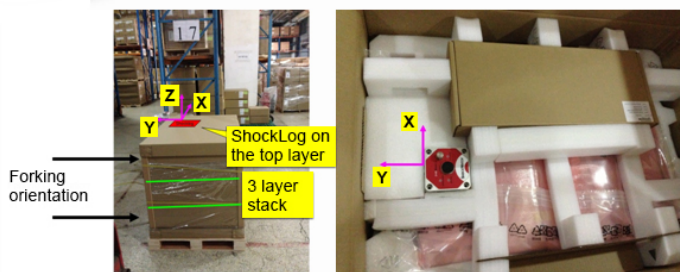


Figure 9: A shock gravitational force measurement device embedded in the shipping box.

After the implementation of the three changes in design variables, the effect to the failure rate needed to be verified in terms of whether the system can survive during the severe of shock in the transportation and handling processes. Two transportation routes were chosen: from Fushan, China, to Sezimovo, Czech Republic, through the China and Russia border by train, and a return sea trip through the Mediterranean, Arabic, and South China Seas. As shown in Figure 9, a shock gravitational force measurement device was embedded in the shipping box of the computer server to record the acceleration and direction of shock in real-time in large stationary or moving systems in transportation and transferring process.

The data collected can be used to calculate the shock energy level ΔV . The comparison between the value of ΔV and the criterion can be used to judge whether the shock can cause poor contact problems in transportation and transferring process. At the same time, the maximum temperature and humidity were measured by temperature sticker and humidity sticker to compare to the reading from the shock measuring device.

Improvement Effect Verification

A lab drop test with extreme conditions was performed on a boxed computer server system to simulate the harsh transportation process (Figure 10). The test setting included a 250-Hz filter frequency and a drop height of 610 mm for the packaged weight of 16.42 Kg. In the test, the accelerometer was installed in the box and used to record the acceleration and duration along X, Y, and Z axes when the system



1. Filter Frequency: 40 Hz (shocklog limitation)
2. Package weight: 31.224 kg
3. Drop height: 620 mm

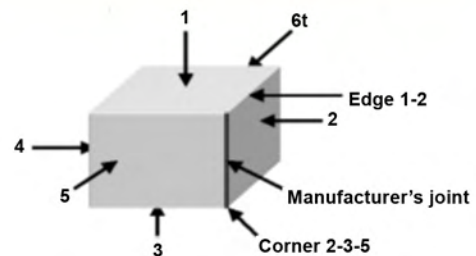


Figure 10: The 10 lab corner-edge-face multiple drop tests to emulate transportation stress.

was going through 10 multiple corner-edge-face drop tests. After the lab test and road test, the system would go through normal boot-up and inspection to see if any accessories were loosened. Then, the package box was checked, and humidity and temperature numbers on stickers were recorded.

The maximum shock energy from field measurements and lab tests were then calculated based on Equation 1 where A is the peak acceleration of nominal pulse in g and D is the duration of the nominal pulse in 1/ms^[2]. If the total energy level from the lab drop test on the product is larger than from real transportation and handling stress, then the package design

is able to protect the electronic product from shock and vibration in the shipping.

$$\Delta V = 2/\pi * A * D * 10^{-3} \qquad \text{(Equation 1)}$$

The maximum shock force level along X, Y, and Z in the drop test is recorded in Table 5. The maximum ΔV calculated from Equation 1 is 17.09 along the Z-axis, which can be used as the criteria to judge whether the shock energy level for the packaged system is out of limits in transportation and transferring processes. The data maximum g-force from those two routes by train and sea were retrieved from the shock measurement device then the same computation was done as previously for maximum energy levels ΔV. The maximum acceleration recorded by the device from the railroad route along the horizontal XY-direction was 20 g and vertical Z-direction was 35 g, which converts to 5.46 total energy. On the other hand, the maximum acceleration recorded by the device from the sea cargo route along the horizontal XY-direction was 13 g and vertical Z-direction was 11 g, which converts to 2.03 total energy. Comparing the total shock energy of railway and sea cargo to the maximum energy from the lab test indicates the package design and three design improvements were able to eliminate the contact interconnect problem and reduce the failure rate to zero.

Finally, the temperature and humidity from the stickers in the packaging box and data measurement from the shock measurement device were all within the product testing requirement for product storage and operation, +40 ~ -40°C and 30-95% RH to fulfill the product warranty mission time.

Conclusion

The contact interconnect problem of electronic accessories in the computer server system due to the severe shock in the transportation and transferring processes can be resolved through the following three approaches:

- Ensure hard Au plating thickness
- Increase the damping plate area and thickness
- Add the motherboard locking mechanism

The redesign verification approach to compare shock energy from the field through two shipping routes to the lab test indicated that the total energy level from the lab drop test on the product is much larger than from real transportation and handling stresses so that the package design is able to protect the electronic product from shock and vibration during the shipping and avoid the contact interconnect failure totally.

PRODUCT PACKAGE DROP TEST			
Corner-Edge-Face Drop Number	MaxX	MaxY	MaxZ
1	31.7	9.3	6.3
2	43.4	13.6	7.1
3	56.4	6.4	16
4	4.6	25.3	21.7
5	69.2	7.7	10.8
6	77.3	5.9	16.1
7	4.9	46.2	18
8	2.9	32.2	3
9	6.2	3.9	49.6
10	8.7	10.8	109.5
Δ Max. Value (g)	77.3	46.2	109.5
Δ V (m/s) (Assumed Value 4 ms)	1.93	1.15	2.73
Δ V (m/s) (Assumed Value 11 ms)	5.31	3.17	7.52
V (m/s) (Assumed Value 25 ms)	12.06	7.21	17.09

Table 5: Multiple corner-edge-face drop test for the product.

Future Work

One of the major drawbacks of this energy level approach derived from the fact that the maximum g-force is not able to compute the accumulated stresses so as to understand the damage from accumulated energy to the interconnect system of contact and solder joint. The research teams are looking forward to adding the lab rolling rock test to emulate the accumulation energy for railway and sea cargo routes then compare to the shock energy accumulated over time in these two routes by integration the area under the g-force time curve.

The iNEMI Board Assembly Technical Roadmap of 2017 predicts that the low-temperature soldering (LTS) usage will increase to 20% + by 2027^[3]. The drivers for this LTS technology trend are threefold: the energy and CO₂ emission reduction, overcoming the material limitation in electronic components and PCBs, and low-temperature soldering process to match with electronic miniaturization. Due to the nature of the brittleness of bismuth contained in the low-temperature solder SnBiAg, the impact-related failure rate of LTS is substantially below current SAC305, which is widely used. Potential mechanical strengthening mechanisms, such as corner or edge bonding material attached along the BGA, are being evaluated to reduce the susceptibility to mechanical shock. Since some of the BGAs still use SAC lead-free solder, there will be forward compatibility issues with LTS paste applications to the SAC component circuit interconnect system. The mixture of SAC and SnBiAg creates a complicated mixed alloy system in which bismuth tends to form a layer in bulk the form in the mixture as well as along the IMC and solder interface (Figure 11)^[4]. It is the intention of the project team to use the energy level approach to evaluate the LTS solder joint interconnect integrity when the product packages are going through the same shipping routes. PCB007

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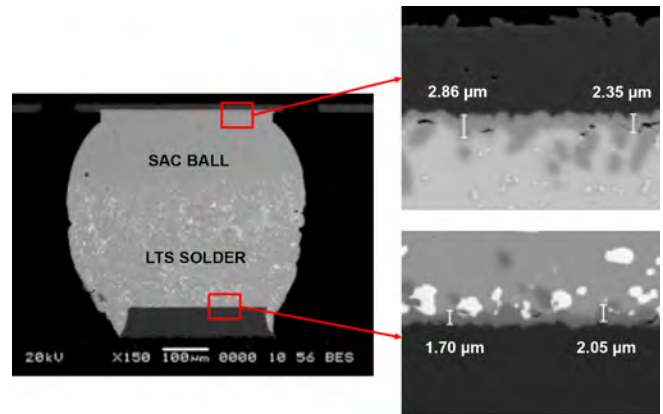


Figure 11: Microstructure of mixed alloy of SnAgCu and LTS (L) with IMC thicker at package side (upper R) and bismuth accumulation at LTS and IMC interface (lower R).

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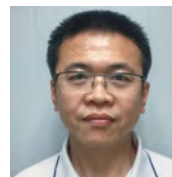
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Vincent Weng is senior engineer of reliability engineering.



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How Changing Cleaning Technologies Affect Reliability

Feature Interview by Andy Shaughnessy
I-CONNECT007

At the recent IPC High-Reliability Forum and Microvia Summit, Andy Shaughnessy spoke with Michael Konrad, founder and president of Aqueous Technologies and a speaker and panelist at the event in Baltimore, Maryland. They discussed Konrad's presentation and the recent proliferation of cleaning, from solely high-reliability products to Class 1 consumer products.

Andy Shaughnessy: Good to see you, Michael. Can you start by telling us about your upcoming presentation?

Michael Konrad: I'll be talking about the factors that influence the reduction in residue tolerance on circuit assemblies. Historically, circuit assemblies were—almost without exception—cleaned after solder and reflow. With the introduction of the Montreal Protocol and a ban on the cleaning solvents that were used to remove the containment species from the circuit assemblies, the majority of the industry switched to no-clean technologies. The hope was that this would eliminate the need for cleaning, and it largely did for a long time.



Now, due to miniaturization and very minimal—if any—gaps between the bottom of the component and the top of the board, the amount of tolerable residue has shrunk on assemblies to the point where now most assemblies are cleaned again. It's an evolution. I'll also be introducing the new IPC J-STD-001 Amendment 1 change to the cleanliness testing requirements of the J-Standard as the way the industry has responded to the sudden need for cleaning again and the consequential need to test for cleanliness.

Shaughnessy: What's the change with that standard?

Konrad: Much of the change has to do with resistivity of solvent extract (ROSE) testing, which was the predominant method of testing cleanliness for the last 30–40 years. But ROSE testing isn't going away; it's going to be used more. What is going away is the historical pass-fail limit that was associated with the ROSE test. ROSE testers were used to determine pass or fail, clean or dirty; now, they're

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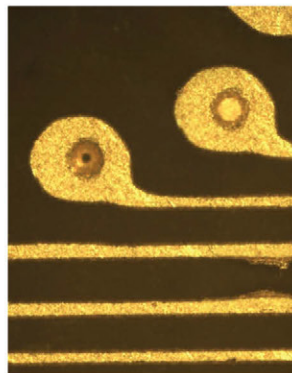
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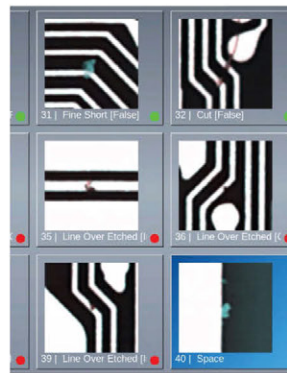
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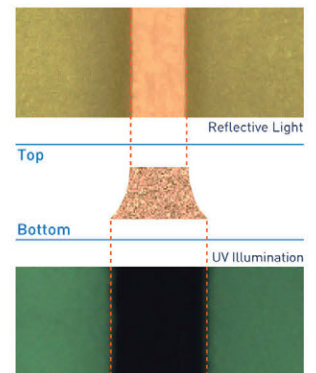
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Michael Konrad presenting at the 2019 IPC High-Reliability Forum and Microvia Summit.

going to monitor process control and provide validation. The pass-fail method was designed in the '70s when the Bee Gees were on the radio every other song. I'm glad we're not in the '70s anymore for a number of reasons, but the standard we've been using until last October was established in the '70s. Boards, of course, have changed dramatically since then.

Shaughnessy: You used IoT as an example of electronics now being in environments that are new and nontraditional. Can you talk about some of the contamination effects?

Konrad: It's not often that we are in a revolutionary moment. Usually, we're in an evolution, but now, the revolution of electronics has allowed us to largely take consumer goods and throw them into harsh environments. We're putting electronics into smart electrical meters that are in harsh environments outside of hundreds of millions of homes. We're putting electronics in toothbrushes and refrigerators and accelerometers in footballs and tennis rackets. All of these things experience harsh environmental conditions. Whenever the temperature or humidity increases, the amount of residue tolerance decreases. With what would normally be Class 1 electronics—which really have

no high expectation of reliability—we're throwing them outside and causing them to fail.

The explosion of IoT—and taking electronic components and assemblies and putting them in places where we traditionally have not had them—is creating a need to remove residues more than it would have before. Normally, we remove residues if somebody is going to die if the component or the assembly fails. That's considered a high-reliability requirement; we clean so we don't kill people. Now, a lot of consumer goods—even Class 1 consumer goods—are being cleaned because it will create a better reputation for the manufacturer. For example, the failure of an electronic

flea collar will not kill anyone; you just have an itchy dog. We're seeing a lot of things being cleaned that historically—at least in the last 30 years—were not.

Shaughnessy: Are you talking about contamination during manufacture that presents once the product is deployed?

Konrad: Yes. Ionic contamination, specifically, is not an issue unless it's merged with moisture and electrical current. Three factors work together to produce electrochemical migration, which has a number of knock-on fatal effects on an assembly: ionic residue, moisture, and electrical current. Remove any one of those three, and you solve the problem. If the power is turned off, electrochemical migration won't occur. Prevent the assembly from ever coming into contact with moisture, and we can leave residue on the assembly. In most cases, however, we really can't prevent moisture from ever contacting the assembly. And we certainly can't suggest our customers turn off their products to improve reliability, so what's left is to remove the residue.

Shaughnessy: Are you doing seminars around the country on this topic?

Konrad: Yes. We have two workshops coming up in Rockville, Maryland, and Raleigh, North Carolina. Then, we have two more in Melbourne and Tampa, Florida. It's a roadshow. And we have a number of experts from conformal coating and soldering material, to cleaning equipment, testing, and coating, speaking on subjects and how they relate to reliability.

Shaughnessy: You see a good cross-section of people coming to your events. Are you ever surprised by some of the problems attendees have?

Konrad: I've been in this business for 35 years, and just when I think the element of surprise is gone, something comes up. One of the challenges our industry, to quote a colleague, is the "silver tsunami"—the exit of highly experienced engineers from our industry, the old sages who sat in the cubicle who knew the answer to every question and where all of the "process bodies" were buried. Mostly, they've retired, and young engineers are left who are very enthusiastic, and in some cases, inexperienced.

We do these workshops—and cleaning is a common denominator in a lot of these workshops—because many people are under the impression that cleaning left us completely in the late '80s and early '90s. Folks are running their product with a jar of paste that says "no-clean" on it, and some people treat "no-clean"

almost as if it were an instruction, like "don't clean."

Now that cleaning has roared back, there's still a sense of misinformation or an absence of good information. Why are we cleaning something that says "no-clean?" There are reasons behind it. The most popular flux cleaned today is no-clean. Most of our customers are cleaning no-clean flux.

The workshops allow people to realize that if they're cleaning, that doesn't mean that they're doing something wrong; it means that their board has changed and it's no longer happy with a little bit of residue left on it. Education seems to be the best way to drive that point home.

Shaughnessy: It does sound like an order. "Do not clean."

Konrad: Right. "No clean. Yes, sir. I'm not going to clean it."

Shaughnessy: Is there anything else you want to mention?

Konrad: I'm glad you're here. It's a great event, and there are a lot of good speakers.

Shaughnessy: Thanks for speaking with me today, Mike.

Konrad: Thank you. **PCB007**

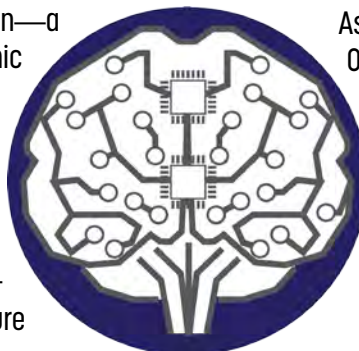
Building a Brain

Researchers at Oak Ridge National Laboratory (ORNL) are taking inspiration from neural networks to create computers that mimic the human brain—a quickly growing field known as neuromorphic computing.

By replacing traditional memory and CPUs with electronic neurons and synapses, scientists aim to create systems that solve complex problems more quickly using less power. "The computing community is starting to understand that this future

beyond the GPU-CPU environment is coming," ORNL's Catherine Schuman said.

As scientists imagine supercomputers after ORNL's Summit—the world's fastest supercomputer—and its successor—Frontier—they will look for ways to surpass power and performance limits of traditional computing. "One of those paths forward is to incorporate more novel computing architectures into the supercomputer," Schuman said. (Source: Oak Ridge National Laboratory)



What Do You Mean “Passed” Isn’t Enough?

Testing Todd

by Todd Kolmodin, GARDIEN SERVICES USA

It’s Friday afternoon, and the shipping deadline is approaching rapidly. Your high-visibility Class 3, Level C product is just about done with electrical test and should fly through FA and barely make it. You are relieved and look forward to Saturday on the lake. Just to make sure, you call the ET department and check on the yield. The lead in ET replies, “96% final.” You are quite happy with the news as you manufactured enough overage to compensate for that loss of 4%. Relieved, you head out the door pleased that the new customer delivery has been met.

Not so fast! Your cellphone rings just as you press the disarm button on your getaway car, and your quality manager is on the other end. They say, “We have a problem.” You happily retort, “We had a 96% yield! They passed ET!” But your quality manager replies, “You better come to the lab,” and you have the same feeling

as when the dealer flips a blackjack just when you’ve doubled-down. Their final comment before hanging up is, “We better not ship this order.” Feeling your boat sink before you even get it off the trailer, you reluctantly head to the lab.

So, what happened? Although you had a 96% yield, it has been discovered that, within that 4% of failures, is a defect that puts the entire order at risk. In this case, I’m talking about barrel voids. ET had detected barrel voids in the 4% of failures. The decision now must be made as to whether the “passed” product can ship as reliable or should the order hold for evaluation. Looking from the outside, the answer is fairly clear that it should hold to evaluate the type of void detected and whether it poses a potential field failure once it leaves the manufacturing facility. This decision, however, is critical, and honestly, there are many times the order doesn’t go on hold and ships instead.



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A photograph of a roll-to-roll processing machine. A wide, flat, copper-colored strip is being fed from a large roll on the right, passes through several rollers and guides, and is then cut into smaller pieces by a pair of scissors. The machine is light green and has a yellow emergency stop button. The background is dark and industrial.

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How reliable is this order in the long run without verification? It's a risk that, unfortunately, is taken due to production pressure and high revenue deliverables. Sure, in most cases, there may be no negative results from this decision, but it only takes one failure at assembly to cause a line stoppage and a costly return to the manufacturer. This also results in the OEM and/or CM possibly questioning the reliability of the manufacturer, and in today's market, reputation is key!

From a reliability standpoint, we need to quickly assess what risk we may have uncovered when faults are detected during electrical test. What are the showstoppers, and what statistically shows a low latent risk at the assembler and beyond? In most cases, isolated inner layer defects, random shorts, or surface solder tails are not statistically significant on the overall long-term reliability of the product. These are usually either reworked (if allowed) or scrapped. Many OEMs no longer even allow repairs on their product, so the latent risk is fully removed as the board is scrapped.

**From a reliability standpoint,
we need to quickly assess what
risk we may have uncovered
when faults are detected
during electrical test.**

The significant defect that requires much more scrutiny is the void. This can be even more important when microvias and blind and/or buried vias are involved. These are the defects that may hide in a "passed" board only to manifest during assembly due to thermal stress and high temperature during solder flow. Once the void is identified, it is crucial to identify its type and what substructures may be involved (in the case of sub-part stack lamination). If the void is determined to be a bubble or air entrapment type circumferential void, it could be an isolated case. This may be isolated

to a specific flight bar on a plating line, and some sampling of other board serial numbers processed on that flight bar may be indicated.

However, if a taper plate or thin copper void is determined, it may indicate a wide range of risk on the entire load that was processed. Failed bonding on a microvia can also indicate an undetermined plating issue or even an anomaly in sub-part lamination. Now, the risk on the overall long-term reliability of the product has become very high. Shipping product when defects like these are found, even in a small percentage, blows the statistical curve of ET yield. A 96% yield does not bode well when that 96% may be hiding 100% of potential field failures.

We must determine what risk is present, which requires high-resolution resistance testing of the barrels or, alternately, 4-wire Kelvin testing. In most cases, this is done on the smallest holes as the higher the aspect ratio, the greater the risk. Studies have been done to calculate the theoretical resistance that can be expected based on the copper weight and aspect ratio. With this test, you can determine if you have a risk within the remainder of the product that "passed" electrical test. We must remember that standard electrical test is measuring continuity resistance at 10 ohms and above even for Class 3, Level C product. Taper plate and thin copper will not be detected under these test conditions. The fluctuations in resistance of a good barrel versus a suspect barrel will be in the milli-ohm range. This is undetectable with standard ET, which is why we can have a 96% yield in ET with a hidden train wreck just waiting to happen.

The problem arises here that now we have an entire order that must be screened but the direct access to the barrels is not available due to solder mask and/or via plug. The best results in 4-wire Kelvin testing is the direct probing of the opposing sides of the barrel. Probing at the first opportunity from the barrel introduces more copper and thus increases the mean resistance of that given barrel. What happens is that the resistance master developed from that longer circuit now becomes too large to accurately detect the small changes in resistivity that thin copper or taper plate may cause.

Remember, the test is looking for milli-ohm changes in resistivity from a good barrel to trigger a fault. The detection guard percentage is adjustable and typically set to around 25%. If you have excess copper in the circuit, the total resistance end-to-end is 1 ohm, and the fault trigger is 25%, you would have to see a 250+ milli-ohm change in that circuit to trigger a fault. That is far too high to detect the type of fault in question.

The main solution is pre-planning with these types of product. Small hole size, high aspect ratio product requires in-process screening. Trying to perform 4-wire Kelvin test on fully masked and finished product will not identify the potential latent defect unless the barrels are accessible from both sides. This test should be performed before solder mask and after all plating processes are complete. This allows the direct probing of the high aspect ratio barrels, which will deliver the most accurate results. This can also be a sampling from each flight bar from plating to identify if there was a potential systemic issue across the entire load or just perhaps an issue with just one flight bar alone. Performing the test at this stage increases your confidence in reliability as resistance fluctuations will be detected before costly final processes are performed. If the test is fatal and caught early enough, a restart can be performed with as minimal an impact as possible on delivery.

What we have seen today is that “passed” is not always passed. We must be diligent to scrutinize the failures found during routine electrical test as a high yield in ET may not indicate high reliability. Improperly reviewing the failures, and especially overlooking the potential impact of a detected void, can turn a 96% ET yield into a 0% yield in the field. This may result in a devastating monetary hit to the manufacturer not to mention the reputation hit in this extremely competitive market. **PCB007**



Todd Kolmodin is VP of quality for Gardien Services USA and an expert in electrical test and reliability issues. To read past columns or contact Kolmodin, [click here](#).

Establishing the Ultimate Limits of Quantum Communication Networks



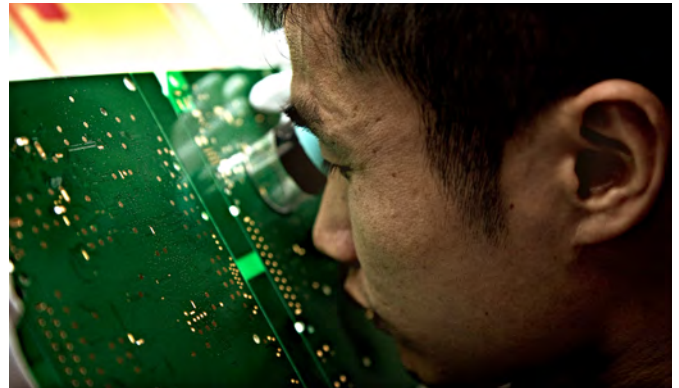
Right now, sensitive data is typically encrypted and then sent across fiber-optic cables and other channels together with the digital “keys” needed to decode the information. However, the data can be vulnerable to hackers. Quantum communication takes advantage of the laws of quantum physics to protect data. These laws allow particles—typically photons of light—to transmit the data using quantum bits, or qubits.

Multinational corporations are now building intermediate-size quantum computers with an increasing number of quantum units or qubits. Once they scaled up to larger sizes, these devices will have far-superior capabilities than current classical computers.

One challenge will be to connect quantum computers together to create a quantum-version of the Internet or “quantum internet.” However, an important but unanswered question remains: What is the ultimate rate at which one can transmit secret messages or quantum systems from one remote quantum computer to another?

“Studying quantum networks is notoriously difficult, but recent mathematical tools developed in quantum information theory have allowed us to completely simplify the analysis,” he said. “An outstanding question was to compute the maximum number of elementary quantum systems [known as qubits] that could be reliably transmitted from one user of the network to another, or similarly, the maximum number of completely secret bits that these remote users could share. This number has now a precise analytical formula.”

(Source: University of York)



A Guide to High-reliability PCBs From Design to Specification

Feature by Jeff Beauchamp
NCAB GROUP

In our daily lives, we constantly interact with electronic products, and all of these products contain a printed circuit board (PCB). Because the PCB serves as the interconnect for all the various components required for the electronic system to function reliably, it is often referred to as the key component.

Thus, it comes as no surprise that PCB reliability is a critical factor right from the start of the PCB production process. If a PCB has a reliability issue, the end product itself is at risk. The important thing is getting it right the first time. Trying to improve reliability once the product is designed and in production can lead to massively high costs for the product owner. In some cases, such as medical equipment or

motor vehicles, it could even become a matter of life or death.

Creating reliable PCBs is an outcome of considering all aspects that can affect reliability as early as possible in the design process. The further down the design process, the more expensive and risky it can be to fix. Because its design has been tailored to a specific function and application, you can't compare a PCB to other components. As a custom component, the PCB's role is critical. A good board design improves the reliability of the end product and lessens the risk of failure. Furthermore, as technology advances, design solutions become increasingly complex, which requires more comprehensive planning in terms of design and manufacturing. It follows, of course, that the more complex the function of the PCB, the more complex both construction and manufacturing becomes.



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Important Features

The following list highlights the 14 most important features for designing and producing a reliable PCB as seen by NCAB Group. Note that some of these features are not included in IPC standards, but NCAB finds these particular constraints to be critical. IPC standards are guidelines for the industry, but they are not always comprehensive in terms of producing the most robust board feasible. For high-reliability and/or high-technology circuit boards, guidelines usually need to exceed IPC standards to increase performance and lifetime.

1. 25-micron nominal hole plating per IPC Class 3
2. No track welding or open circuit repair
3. Cleanliness requirements beyond those of IPC
4. Tight control on the age of specific finishes
5. Internationally known base material types used—no local or unknown brands allowed
6. Tolerance for copper-clad laminate is IPC-4101 Class B/L
7. Defined solder mask, ensuring accordance to IPC-SM-840 class T
8. Defined tolerances for profile, holes, and other mechanical features
9. Specific solder mask thickness (IPC does not require this)
10. Defined cosmetic and repair requirements (IPC does not require this)
11. Tighter requirements for the depth of via fill (IPC requires 60%, but we require at least 70%)
12. Peters SD2955 peelable as standard
13. Specific qualification-and-release process for every purchase order
14. No X-outs accepted

At the same time, boards should be designed in a way that they can be manufactured reliably by as many factories as possible. The extra investment in thought up front gives the product better lead times overall while maintaining quality.

Applying the very latest technology required by the component manufacturers often only increases the challenge level. For example, if you can avoid BGA escape routes that use six or seven different layers of blind or buried vias and reduce it to a standard multilayer board, it's a good idea to do so. Reduced layer counts do away with all of the extra drilling and plating processes, significantly reducing costs while also improving the manufacturability of the product. By keeping manufacturing options as open as possible through smart design, this will allow easier switching from one production facility to another. Further, this reduces the design's overall supply chain risks. If one factory, for example, is underperforming or dealing with a technical issue, production could more easily move to another facility. The riskiest PCB design is one that is limited to a single factory's unique processes.

Data and Documentation

But there is more to reliability than just the manufacturing process or careful design practice. Reliability is achieved through the mindset that plans the entire process from design through delivery. Therefore, it is critical that complete and concise information, build notes, and instructions are provided to your PCB supplier and that the partner demonstrably puts quality first. Look for a partner with a seamless approach that will take the project from prototype manufacturing to production manufacturing without sacrificing quality or reliability. Design teams do their part in this reliability process by creating a complete and detailed manufacturing package.



Product specification begins at the time of quote and is continuously updated through dialogue with the customer until production begins. Our experience at NCAB shows that about 30% of all of the new articles provided to us arrive with missing data or contain ambiguous or conflicting information in describing the build. This causes engineering questions (EQs) to be raised, which take time to clarify and can easily affect delivery dates.

Some examples of missing, ambiguous, and conflicting information include:

- Outline information/data/drawings
- Unspecified plated or non-plated holes
- Unspecified surface finish
- Unspecified copper thickness
- Unspecified material to be used
- Unspecified color of solder mask/legend print
- Unspecified thickness of the finished board
- Missing Gerber or drill files
- Board thickness does not match the specified build
- Legend print included in the documentation but not to be printed
- Dimensions on the drawing do not match the Gerber outline
- Number of holes in drill drawing does not match with the number of holes detailed in the supplied drill file
- The hole sizes in the drill drawing do not match the sizes in the drill file
- Copper thickness in specification is not per IPC
- Specified impedance requirements cannot be achieved based upon the stated build
- Attached netlist contains short/opens compared to Gerber files

Recommendations

So, how does a design team avoid these data transfer pitfalls? Here are five key recommendations for preparing to transfer a design to manufacturing.

1. Include the Original Data

And if this is a move, include the working files. Providing both sets of data ensures your



design matches what you should have already been receiving and reduces the number of EQs. Tooled data is very useful when delivered alongside the original files. If this is a first-time build, it helps to provide the desired array layout, ensuring the supplier produces the correct array.

2. Include Stackups

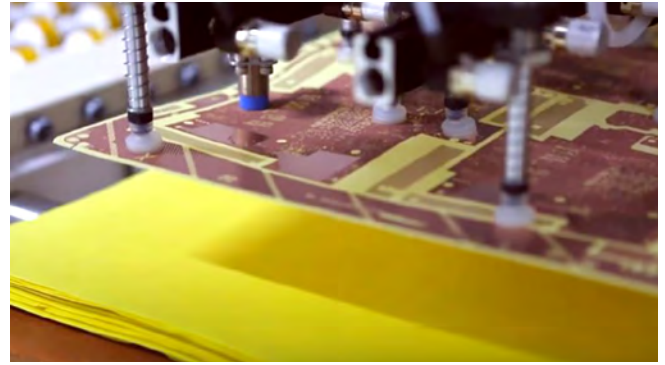
Another factor that will greatly increase the likelihood of a correct build includes stackups (previous or desired). Not specifying the stackup could yield a different end-result depending on manufacturer preferences and material choices, affecting designed impedance and other performance issues.

3. Include Any Previous EQs

Assuming the order has previously received pre-production engineering, it's helpful to include documentation on any previous EQs. Those previously answered questions will help reduce repeat questions. Some common examples of items that might trigger an EQ include:

- Unterminated traces
- Shorts (intentional or unintentional)
- Conflicting information in the fabrication documentation

If this is a first-time build, expect to receive EQs. A good supplier will ask detailed questions before building anything. If you do not receive questions, you should be suspicious of what that supplier changed without consent.



4. Create Fabrication Data That References IPC Specifications

Having requirements per IPC standards creates a clear expectation for your supplier without getting too specific. Examples of specifications to reference include:

- Material per IPC-4101
- Acceptability per IPC-600
- Manufacturer to IPC-6012 Class X
- Surface finish per IPC-4552, IPC-4553, IPC-4554, etc.

Being too specific when telling your supplier what the design requires can potentially cause unintentional costs. For example, it may seem like a good idea to specify an exact material from a precise brand to ensure adequate control. It may seem contradictory at first, but unless the design absolutely requires one specific material only, it might be safer to specify an IPC standard and benefit from a number of approved brands. With some latitude, the factory will then be free to choose the material with which they have the greatest experience and is best suited to their manufacturing processes. Forcing a specific choice on the factory can create problems since it could introduce additional yield risk upon the reliability of their processes compared to using a material the fabricator is familiar with.

5. Copper Weights

NCAB recommends specifying copper per the IPC copper table in the IPC-6012 and IPC-600 specifications. IPC does not specify copper in terms of ounces per square foot but instead

specifies in terms of finished thickness in mils and microns. A common example we frequently see is a request for 2-oz. copper on the outer layers. Most manufacturers will accomplish this with 1-oz. base copper and Class 2 plating for a finished thickness (after processing) of 47.9 μm (1.886 in.). This can affect reliability if the PCB was designed with an expectation for 70- μm (2.80-in.) copper on the outer layers.

Conclusion

Overall, it is important that your PCB supplier quote with standards and reliability in mind, not solely on price. Providing the previously mentioned documentation and details will help ensure yield reliability without incurring any unnecessary costs. IPC standards are a useful guideline with which to work but be sure to always evaluate the ultimate function of the board and adjust your design and build requirements accordingly for manufacturability.

There are many factors to consider when first designing and then transferring a board to a supplier in order to build a reliable PCB. Be prepared to answer questions to make sure the PCB performs as required. It is important to choose a supplier who values quality, takes full responsibility for production, and works with you as a partner to help produce a reliable PCB. **PCB007**



Jeff Beauchamp is a field applications engineer with NCAB Group.



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Moving Into Microvias, Part 4

Trouble in Your Tank

by Michael Carano, RBP CHEMICAL TECHNOLOGY

Copper deposit in the vias with electroless copper or alternatives, such as carbon-based direct plate processes to the vias, depends on process control, equipment design, and chemical parameters. When these are not in control, defects arise.

Introduction

In “[Moving Into Microvias, Part 3](#),” I discussed the importance of desmear, particularly as it relates to higher-performance materials. In Part 4, I will present metallization for HDI blind via processing.

There are a few points to consider first. With respect to HDI and blind vias, the chemistry must find a way into these cup-shaped vias. The chemistry must be replenished as it is depleted to maximize the diffusion of the active ingredients to the vias. Of course, these same principles apply for through-hole vias as well. Designing plating cells to ensure plating solution movement is critical to providing void-free deposits for HDI designs. I will delve into these cell design methods and other techniques in a future column. For now, let’s discuss metallization and potential issues.

HDI Via Defects

The big concern for HDI and vias is not getting a sufficient thickness of copper in the blind vias. This includes voids at the capture pad, thin or tapered plating as the via wall meets the capture pad, poor throwing power, adhesion failures, etc. Figure 1 depicts an ideal state for plating of blind vias. The plating is uniform in thickness at the capture and along the via sidewall.

However, not everything is this easy. As blind via structures become deeper (3–5 mils) and diameters shrink (from 4 mils to 3 mils or less), fluid dynamics play an increasingly critical role. Allowing for sufficient plating solution exchange in these cup-shaped vias is necessary to ensure that key addition agents—such as brighteners and leveling agents as well as copper ions—are replenished, as these are depleted during the plating operation. The same holds true for conventional electroless copper and direct metalization processes.

Secondly, starting with a quality-formed blind via plays a significant role in plating continuity and uniformity. Figure 2 depicts a poorly drilled via. Glass fibers and more of a cup-shaped via negatively impacts the plating quality.

With poorly formed vias, there is an extreme difficulty with moving plating solutions into the via. A poorly formed via will bring about mass

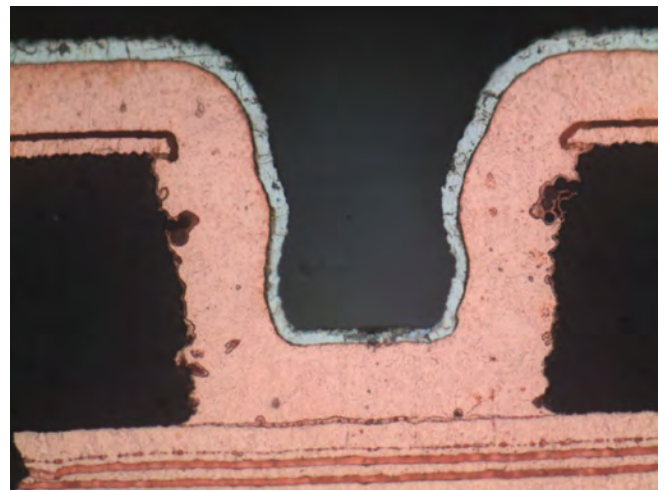
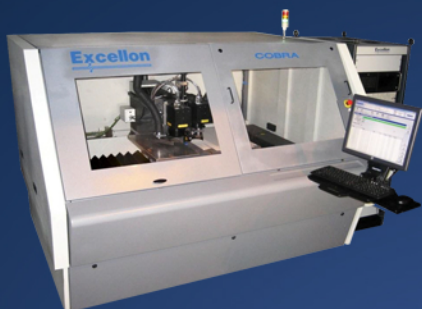


Figure 1: Ideally plated blind via.

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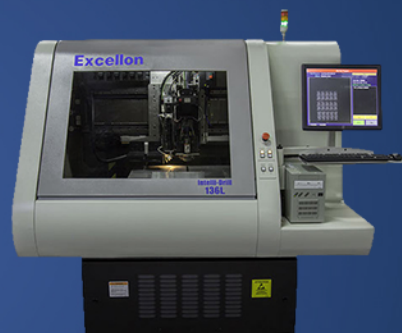
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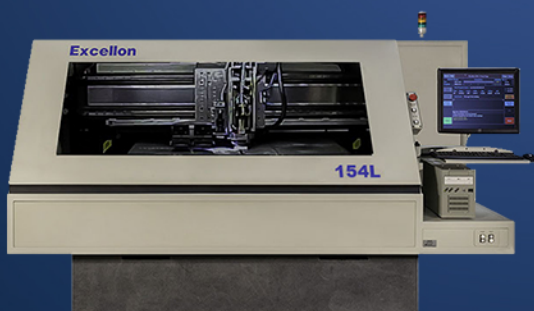
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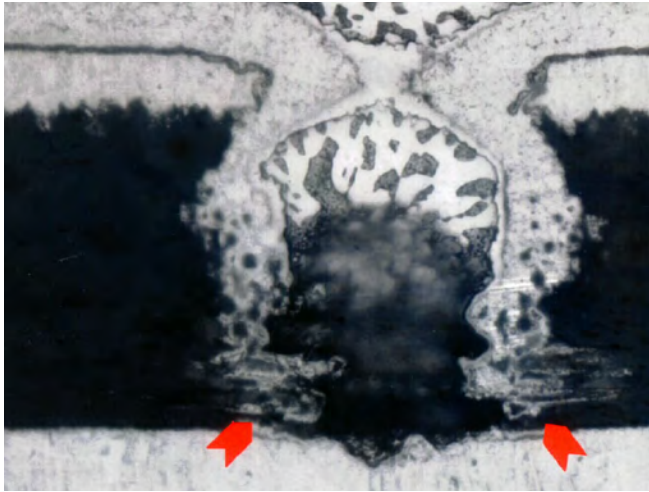


Figure 2: Glass fiber bundles protruding into the drilled via (the arrows show areas where there are apparent voids).

transport limitations. The inability to move fresh plating electrolyte into blind vias will result in thin plating near the junction of the side wall and capture pad. Thin plating thickness presents an area of weakness that can lead to separation or cracking within the copper.

In addition, laser via formation of blind vias can lead to another issue shown in Figure 3. The section shown in the image points to an area where there are voids in the blind via.

It is recommended that both front light (FL) and back light (BL) testing be included in the fabricator's routine quality control protocol. The FL technique is particularly useful because this test helps to determine the location of the voiding. Figure 4 shows an example without voids.

Further analysis of the nonconformance found in Figure 3 is shown in Figure 5.

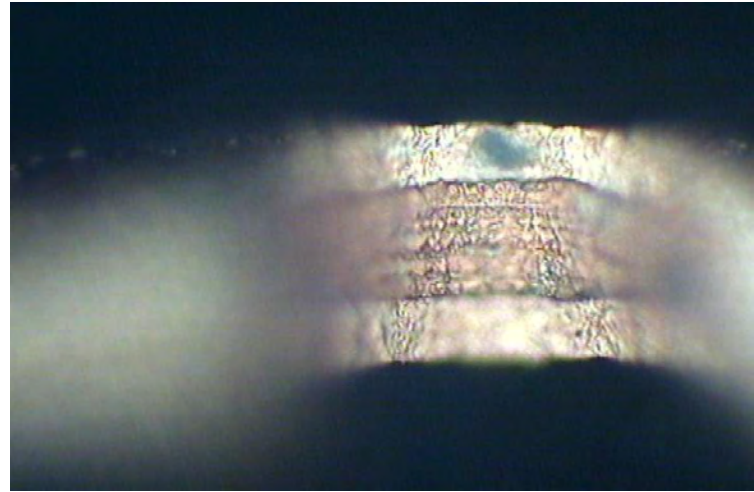


Figure 4: Front light evaluation, showing no copper voiding issue.

The gap shown in Figure 5 exacerbates the difficulty in getting plating into this gap and eliminating the voided or very thin copper plating. Fluid dynamics do play a significant role in achieving uniform plated deposits. However, when there are these gaps or wedges existing between the copper and the resin, increased solution convection may be insufficient.

Regardless of the defect shown in Figure 5, what are the potential causes of the gap or wedge seen in the previous image? There could be several causes. However, let's understand what it is not. In the real-life situation seen previously, the fabricator laid the blame on the micro-etch and the electroless copper process. There was no attempt to look either upstream or downstream in the manufacturing process.



Figure 3: Dark area indicates no copper plating. This is a front light of the blind via.



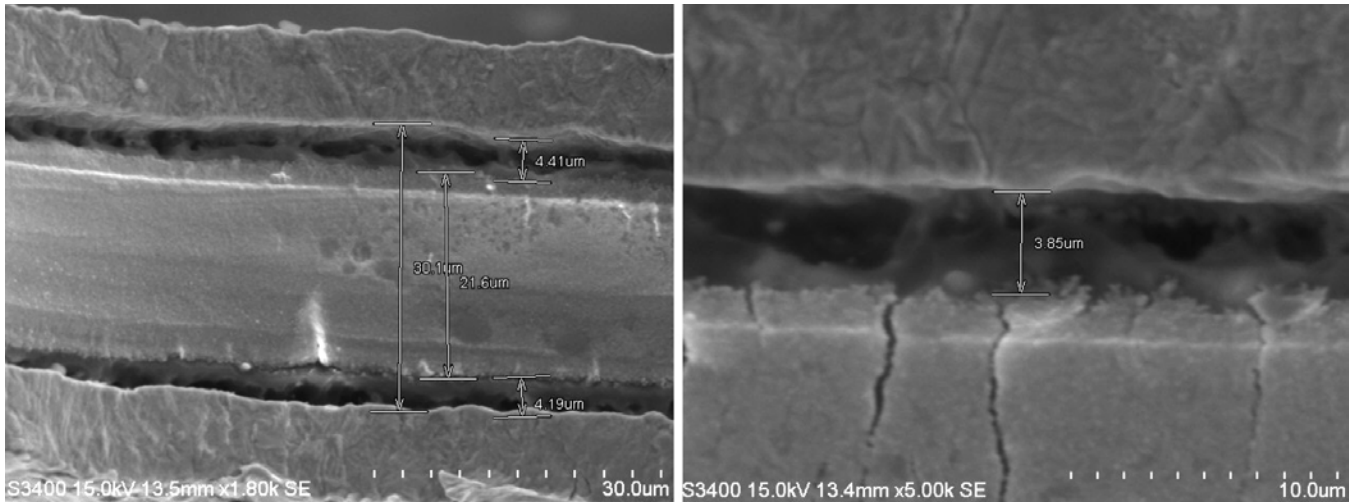


Figure 5: SEM view of the via in the flexible circuit (note the gap).

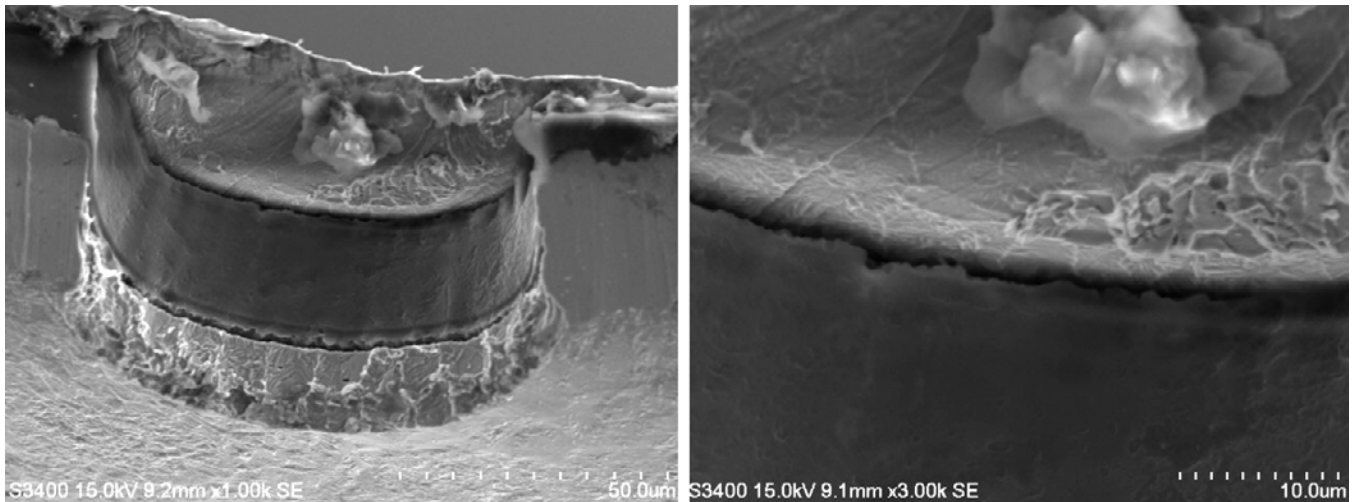


Figure 6: Two views of the gap after via formation and before any further processing.

The supplier tech team, however, performed its own investigation. The team asked for data on laser via formation used at this facility and examined materials immediately after laser via formation. As the results showed (Figure 6), the wedge or gap already existed.

Moving back further into the process, the team noted that gap existed on certain flexible materials supplied by a third party. When the chemical supplier tech team obtained flex materials from a second supplier, examination showed no gap or wedge existed either before or after chemical processing. Of course, chemicals such as those used in desmear or micro-etching, could have led to this defect. But in this situation, this was not the case.

Conclusion

Lesson learned: Don't assume it is the chemistry. Fabricators, in many instances, may not want to take any responsibilities. As a process troubleshooter, stick to your guns and conduct a thorough upstream and downstream investigation. Ensuring a quality copper deposit in the vias with electroless copper or alternatives, such as carbon-based direct plate processes to the vias, depends on process control, equipment design, and chemical parameters. When these are not in control, defects arise. **PCB007**



Michael Carano is VP of technology and business development for RBP Chemical Technology. To read past columns or contact Carano, [click here](#).

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Digital has become the most preferred medium of communication today. While it facilitates communication between two individuals, it has also opened avenues for humans to communicate with gadgets.

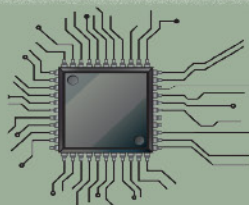
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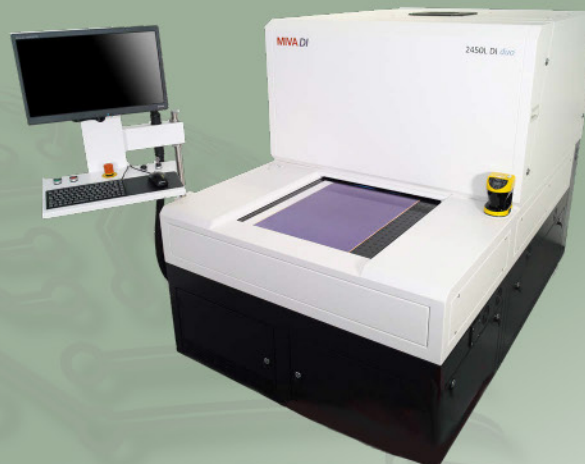
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Avoiding CAF Failures at the IPC High-reliability Forum

Feature Interview by Andy Shaughnessy
I-CONNECT007

I recently spoke with Foresite CEO Terry Munson during the IPC High-Reliability Forum and Microvia Summit in Baltimore. Terry discussed his presentation on the causes of conductive anodic filament (CAF), the dangers of resin starvation, and what advice he'd give to PCB designers to avoid those types of failures.

Andy Shaughnessy: Can you give us a rundown of your presentation?

Terry Munson: Thanks for the opportunity to share. I talked today about CAF and what's causing those types of failures. We're seeing an increase in those type of failures in automotive, medical, and even some of the server board construction. Class 2 and 3 hardware are both experiencing similar issues. And the difference between CAF and electrochemical migration boils down to this: CAF is inner layer, and the electrochemical migration is external.

Shaughnessy: I thought the dendrites and CAF were almost interchangeable.



Terry Munson

Munson: Yes, dendrites. We've seen a lot of external failures; it's harder to find those internal failures when things are shorted and when there are two vias that are shorted together or to the ground plane. Dendrites grow on the surface due to flux residues, board fabrication residues, external moisture, and micro-condensation—droplets of water sitting there. Internally, the only thing you have as a contaminant source is the etching materials for the prepreg, the desmear process, and then the plating process. In the barrel itself—if the resin flows well and there isn't any resin starvation in the weave—you have no place for that plating chemistry to go, so it just gets flushed out and is relatively clean behind the barrel.

When you have resin starvation, and fiberglass is exposed, that fiberglass bundle becomes a collector. All that low surface tension plating chemistry works right in. Now, when you plate a big copper barrel right next to that, the chemistry is going to do what chemistry is designed to do: dissociate the copper

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Figure 1: Cross-section of two vias with a measurable short showing CAF shorting in a layer of resin starved prepreg

and create a conductive opportunity. We're still figuring out how we go from the anode to the cathode without the normal pathway. You have dendrite growth that transports through the metal salt, which collects on the surface. With a CAF, you always seem to have the power effect; the dendrite is thicker on the power side. So, it is plating to that crystal area and then putting to a ground plane and finding a pathway through that weave—that structure—or at micro-separation where you have two layers that can separate.

In my presentation, I showed both of the open weave exposures, which are very visible in cross-section. Then, I showed the micro-separation at the prepreg level where the wrong material was used for low-flow or no flow resin. Because it was the wrong material, there was a gap between the two layers. The plating chemistry fit into that space between the via and the ground plane. I had beautiful dendrite photos showing that. It worked out extremely well.

We also have inner layer shorts that occur at the power trace to ground due to poor rinsing of the prepreg itself or poor control. And when we split a board apart and use a localize C3 extraction where we can still extract the surface area of the inside of the board and compare the microvias to areas where there are no microvias, we see a difference between 3 $\mu\text{g}/\text{in}^2$ of sulfate to 74 $\mu\text{g}/\text{in}^2$ sulfate where we see dendrites. Areas that have low levels of sulfate resin from the methane sulfonic acid plating have very low levels of contamination. Areas where we see dendrites growing around the microvias come from very high doses of contaminants from the trapped residue from the plating.

Now that we've split the board open, we're able to then take a look at the physical. Most people are surprised you can cleave it and look at the inner layers. It splits relatively easy, especially if there is a weak layer; then, it will split along that interface. We have created a tool to allow us to do that with a press and a special blade that we have. We can go in and cleave a board open and see any weave that has nearly no resin flow into it. We can see the impression made into the resin and confirm that it did not flow into it. We can compare that to other areas of a board where we have good resin flow and show there is no problem.

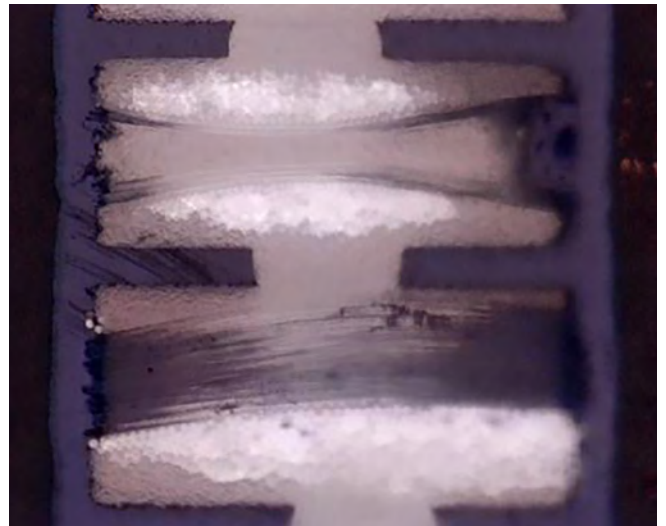


Figure 2: A back-lit close-up showing CAF shorting in a layer of resin-starved prepreg.

Shaughnessy: That was interesting. I like the part of your presentation about the resin-starved areas that were “thirsty.”

Munson: That weave had no way of getting the resin to flow into it, whether it was due to compression and density or bad resin that was overheated or had been stored out of a controlled situation.

Shaughnessy: With some of the things you showed in the presentation, do you have any advice you’d like to give to designers on any things they should or shouldn’t do?

Munson: We are going to see designers being challenged by circuit needs. We are creating blind and microvia structures, and we’re building a lot more architecture and circuitry into the board itself making it a three-dimensional structure. From a design standpoint, one of the biggest things we suggest is giving as much space between power and ground as we possibly can so we don’t have a 2-, 3-, or 4-mil separation on the inner layers where we’re creating an opportunity for a short to occur. The more space we put in there, the greater the opportunity for the resin to flow effectively and at least block parts of that pathway.

Microvias are always going to be a challenge. From a designer standpoint, microvias are the necessary connections to the rest of the whole circuit board. We need to spend more time with the fabrication process to understand what the equipment limitations are and how to help them. We think the press and the lamination process are both critical—how long to press, how hot the press is, how much to allow the resin to flow into the weave, and then how fast to cool. The faster it cools, the quicker the flow stops. It becomes a dance, and a lot of fabricators are in the process of trying to put as much product through those time-consuming processes as possible.

Pushing the fabricator to understand this process and its limitations, where the stackup limitations are, how many panels you can put

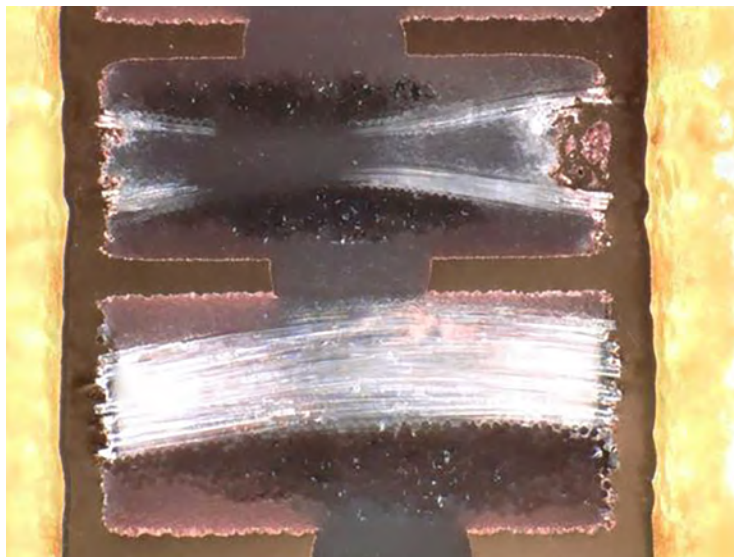


Figure 3: Close-up showing CAF shorting in a layer of resin-starved prepreg.

into it, and the differences between electric heating and oil heating are all important. All of those variables become critical, and the designers need to understand that those issues may affect 2–4% of the hardware. Some of the boards processed in the same stack might all perform extremely well, but on the same panel, there might be nine out of 16 boards, all with the inner layer weave issue on that prepreg. To me, it is not just a prepreg issue; it’s a prepreg and press issue.

Shaughnessy: What would be one or two big takeaways from your presentation that you would you want everybody to remember?

Munson: As density and circuit sensitivity continues to change, we are going to have greater opportunities to have these types of failures and risk issues. Understand what the equipment process limitations are so that we can look for those things and design them out. The second takeaway is to understand the cleanliness of your process. How clean are the inner layers of your board? How can you assess that on a normal, regular basis? That helps.

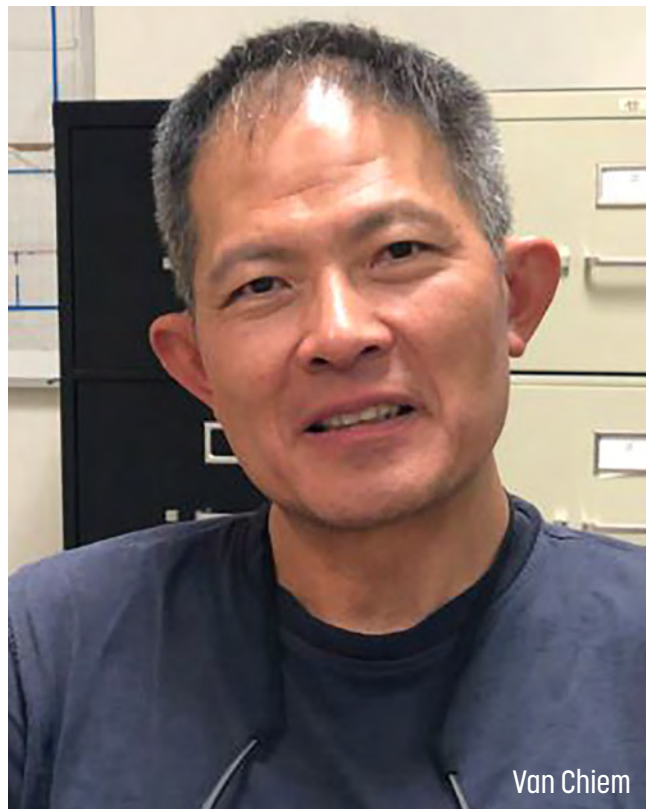
Shaughnessy: Very good. Thanks, Terry.

Munson: Thank you. PCB007

A Conversation With Prototron's Van Chiem

The Right Approach

by Steve Williams, THE RIGHT APPROACH CONSULTING



I recently spoke with Van Chiem, a process engineer with Prototron Circuits, about developing in-house flex and rigid-flex processes and capabilities at their facility in Tucson, Arizona.

Steve Williams: Van, you have a very diverse technical background in PCBs. Can you tell us a little bit about your past experience and what brought you to Prototron?

Van Chiem: I have over 25 years of experience in this field. I started as a process engineer at Unisys Corporation where we made computer chips and advanced component packaging for interconnections like wire bonding, flip chip, and tab bonding. This is my ninth job in the PCB industry. Another job I had was with Enthone in Connecticut at the time, which is now MacDermid Alpha Electronics Solutions. I was in the research group working on the formulation of solder mask to try and convert it to photodefinable dielectric material for microvia. Instead of drilling, we used a photo process to create a microvia, and then the electroless copper followed by plating the copper to form the microvia with smart circuitry. That

was my second job in the industry. I have had seven more jobs, but that might be too much to talk about.

Williams: How about we save the other seven for the next interview (laughs). So, you've seen a lot of technology changes in the last 25 years in the industry and were actually one of the original technologists.

Chiem: Well, I don't like to talk about myself, but I guess you could say that.

Williams: How long have you been at Prototron?

Chiem: About a year and a half.

Williams: And you have already accomplished quite a bit here. Prototron brought you on board for the specific purpose of upgrading their technology in a number of different areas, right?

Chiem: Yes, Kim O'Neil, the general manager here, brought me on especially to develop flex and rigid-flex processes.

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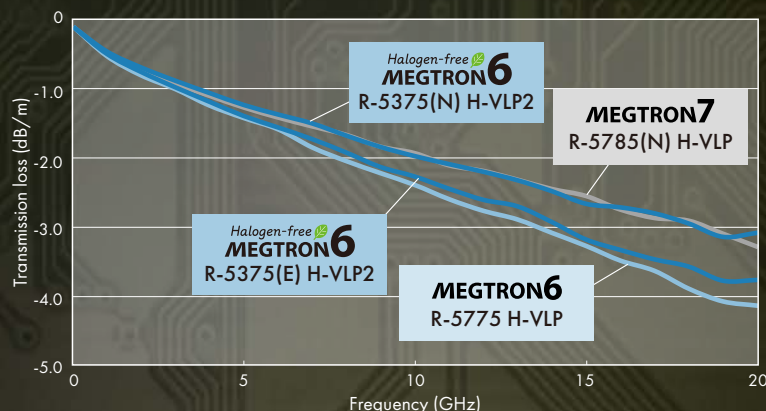
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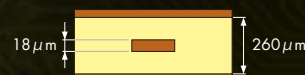
Applications

- ICT infrastructure equipment, High speed networking(High-end server/ router, Optical network, switch), High layer count PCB, etc.

Transmission Loss



Construction



Line length	200mm, 100mm
Line width	125μm
Impedance	50Ω
Inner Cu treatment	No-surface treatment
Core	0.13mm
Prepreg	#2116 56% x 1ply



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Williams: So, you were kind of the R&D lead on developing that technology and getting it to become a viable technology here in Tucson. What was that process like, and what were the challenges?

Chiem: From a technology standpoint, there weren't any major challenges, as this technology is 20–30 years old and very mature. I used to work at Honeywell back in the '90s where we built flex as a chip carrier every day and talked about 3-mil lines and spaces 20 years ago.

Williams: It may be new to Prototron, but it's old to you?

Chiem: Exactly. We were doing some crazy PCB technology 20 years ago in Costa Mesa, California.

Williams: And did you have to do anything here from an equipment set standpoint, including changes to processes, or was it just a matter of using different raw materials?

Chiem: Of course, flex and rigid-flex require a different material set, but mainly, we just needed to develop custom frames, or material handling fixtures, to process the thin materials through Prototron's standard, rigid PCB conveyorized equipment. The Tucson shop was set up for standard, rigid multilayer production, and the equipment set reflected that.

Williams: Were there any obstacles you had to overcome because the shop had never built flex here before? Did you have to re-educate the workers or develop new processes and re-train people on how to handle this type of material?

Chiem: We also had to modify our processes and procedures to adapt to flex processing. Then, it was just a matter of blending the current chemistry and equipment with the new frames to make flex a reality here at Prototron. As we've progressed, we've gained knowledge on how to develop the in-house flex capability. I also needed to train people, write speci-

fications, upgrade the procedures, and make sure everybody was familiarized with the new processes.

Williams: Are you also looking at doing rigid-flex?

Chiem: We have developed the processes and ran test orders successfully, so I am confident we can build rigid-flex here right now. It's not difficult.

Williams: I love your confidence. I understand you're currently working on another project with some very small mechanically drilled holes also.

Chiem: Correct. Kim wanted me to work on mechanically drilling 4-mil microvias using our current Schmoll drilling equipment.

Williams: And that would be controlled depth drilling of the microvias?

Chiem: Yes, 4-mil diameter by 5 mils deep.

Williams: Earlier, you mentioned that mechanically drilling 4-mil holes is not that big of a deal; it's the fluid dynamics of getting the chemistry through a blind hole of that size hole.

Chiem: Therefore, we need to put in some new, different chemistry, as the current conventional chemistry that we have right now is not meant for this application.

Williams: So, it's pretty standard microvia stuff, but you are doing it mechanically instead of laser drilling. Excellent. What else is on your to-do list for Prototron in advancing their technology levels?

Chiem: I think we are open to doing R&D collaboration with other companies on advanced technology. For instance, I am working with an organization in Toronto, Canada, to develop a very advanced PCB design. In that way, we have a mutual interest between the two

companies. We can co-develop this PCB technology and process that can be applied at both companies.

Williams: Wow! As a fellow old board rat, I find this really interesting. What do you think the timeline is?

Chiem: All I can tell you is that it is an ongoing iterative process as design adjustments are made after each batch of PCBs are built and tested until the process is perfected.

Williams: It's exciting to work with you. I know you're doing a lot of great things here, and I'm looking forward to what you come up with

next. Anyone who needs high-quality flex and rigid-flex PCBs can contact Van and the team at Prototron, and they will take care of you. Thanks for taking the time today to talk.

Chiem: Of course. I am always available to help. **PCB007**

This column appeared previously in the July 2019 issue of *Design007 Magazine*.



Steve Williams is the president of The Right Approach Consulting. To read past columns or contact Williams, [click here](#).

New Interaction Between Thin-film Magnets for Faster Memory Devices

Nowadays, we ubiquitously stream videos, download audiobooks to mobile devices, and store huge numbers of photos on our devices. Thus, the storage capacity we need is growing rapidly, and researchers are working hard to develop new data storage options. One possibility is represented by the so-called "racetrack memory device" in which data is stored in nanowires in the form of oppositely magnetized layers.

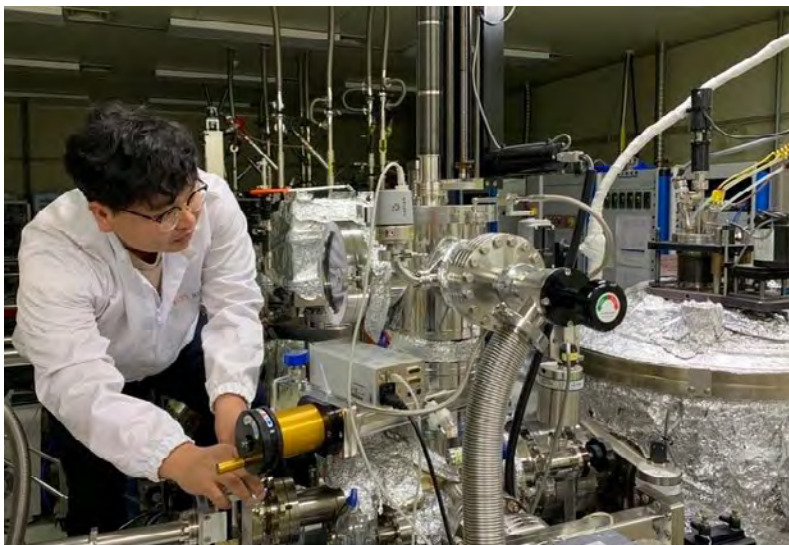
A research team from Eindhoven University of Technology, Johannes Gutenberg University (JGU), Peter Grunberg Institute (PGI), Daegu Gyeongbuk Institute of Science and Technology, and Sogang University has now made a discovery that could significantly improve these racetrack

memory devices. Instead of using individual domains, in the future, one could store the information in three-dimensional spin structures, making memories faster and more robust, and providing a larger data capacity. The results are published in *Nature Materials*.

The research team was able to demonstrate a hitherto undiscovered interaction, which occurs between two thin magnetic layers separated by a non-magnetic layer. Usually, spins align either parallel or antiparallel to each other. This would also be expected for two such separate magnetic layers. However, in this work, the researchers have been able to show that the spins in the two layers are twisted against each other. More precisely, they couple to align perpendicular at an angle of 90 degrees with one another.

Reinoud Lavrijsen, assistant professor at Applied Physics, says, "This breakthrough discovery opens up the possibility of designing various new three-dimensional spin structures, which, in the long term, could lead to new magnetic storage units. The identified interaction, however, is at this moment not strong enough for applications, but we are committed to engineer and optimize this further so that it can be used in future three-dimensional data storage and logic devices."

(Source: Eindhoven University of Technology)





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High reliability and compliance are hot topics at conferences all over the world. If you are a supplier to industries like defense, automotive, medical, and aerospace/space, high-reliability and regulatory compliance are strict demands for electronic device manufacturers.

Nano Dimension and Harris Receive Grant for ISS Project ▶

Nano Dimension Ltd. has received grant approval from the Israel Innovation Authority for developing hardware, in cooperation with Harris Corporation, that will fly on the International Space Station (ISS) and communicate with Harris' ground-based satellite tracking station in Florida.

Army Project Develops Agile Scouting Robots ▶

In a research project for the U.S. Army, researchers at the University of California, Berkeley developed an agile robot, called Salto that looks like a Star Wars Imperial walker in miniature and may be able to aid in scouting and search-and-rescue operations.

U.S. House Approves Measure to Promote Lead-Free R&D in Milaero, Automotive, Medical ▶

IPC is applauding the U.S. House of Representatives for approving a measure that would promote R&D into the performance of lead-free electronics in high-reliability sectors such as aerospace, defense, automotive, and medical equipment.

What to Do About Drones ▶

Cheap, capable quadcopter drones mean everyone from civilian air traffic controllers to front-line military commanders need new and specialized technologies to meet the threat.

NextFlex Launches \$10.5M Funding Round for Anti-Counterfeiting, Flex Batteries, and Hypersonics Innovation ▶

The PC 5.0 total project value is expected to exceed \$10.5 million (project value/investment figures include cost-sharing) bringing the total anticipated investment in advancing flexible hybrid electronics since NextFlex's formation to over \$83.5M.

Commercial Aircraft Production to Hit Record High with Renewed Competition Between Airbus and Boeing ▶

The revival of competition between Boeing and Airbus is expected to result in record delivery of the highly popular narrow-body platforms and a 9.4% year-on-year growth in production.

Growing Military Demand to Boost Security Robots Market at 8.9% CAGR Until 2025 ▶

The global security robots market is expected to be worth nearly \$3.9 billion by the end of 2025, according to a new report by the Transparency Market Research.

NASA Selects First Commercial Moon Landing Services for Artemis Program ▶

NASA has selected three commercial Moon landing service providers that will deliver science and technology payloads under Commercial Lunar Payload Services (CLPS) as part of the Artemis program.

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When You Do Everything **Right** and Something Still Goes **Wrong**

Flex Talk

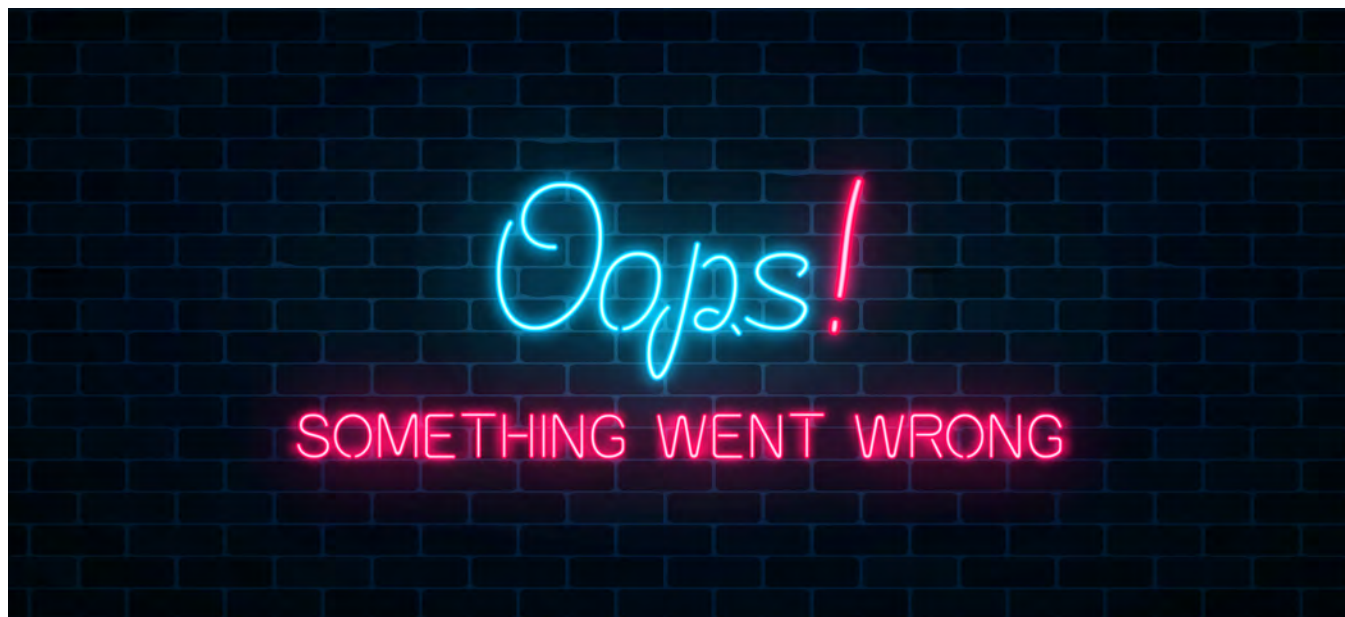
Feature Column by Tara Dunn, OMNI PCB

Our industry is full of tales describing the work and effort needed to overcome fabrication hurdles to produce a complex design. Manufacturing a custom product with 100+ processing steps can be tricky enough, but when you add in a highly complex set of design attributes, pour engineering resources into defining the process, and verify that it is repeatable and reliable, that comes with a certain sense of pride and satisfaction. Today, I want to share a case study of one of those types of designs. And while this example will be one of those stories that will be discussed for years to come, it is also a case of something going wrong even when everyone is doing things right.

This tale starts approximately three years ago when we reviewed a complex design for a medical application. The product has contact with human skin, requires FDA approval, and was expected to have multiple prototype revisions

and both test and pre-production runs before going to full production. The design itself was extremely tricky and required a very specific material set and multiple surface finishes and lamination cycles. Countless hours were spent in engineering discussions, trying to get an understanding of which elements had some flexibility and could be adjusted to make the design more manufacturable and how to overcome the challenges for the elements that had no flexibility. There were three or four revisions and subsequent engineering reviews to make adjustments after each build.

There were several small test lots of these PCBs run as the final product was going through qualification. I think everyone involved with the fabrication of that design felt a strong sense of pride and satisfaction when we moved to the pre-production phase with a process and product that was performing well





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and with a good yield given the technological hurdles involved.

Until one day, several months ago, when the company doing the PCB assembly noticed a slight color and texture difference between some of the pieces. Significant time and effort were put into review and analysis of those parts from both a PCB fabrication perspective and from an end-use perspective. The final analysis showed this to be measling acceptable per IPC standards. Good, right? The product should be usable. Unfortunately, while the parts meet the IPC specification they were built to, it was determined that this condition was not going to be acceptable for end use.

Once again, we all had to sit down together to figure out a solution to this latest hurdle. Product that was built is now being sorted at the contract manufacturer, further testing on the final product is being done, and there are discussions about a potential field recall. The engineering groups throughout all segments of the full build cycle are meeting to find the best path forward. In one recent meeting, we talked about how to have a specification written to quantify the texture issue in a way that can be inspected, and parts will now be screened before shipping to assembly. I imagine there will be additional discussions as we move toward the long-term solution.

In these situations, I think there is a natural tendency to want to place blame on something that is frustratingly causing a considerable de-

lay in product launch and comes with considerable cost to all involved. But this example really shows that even when everyone is doing everything right, something unexpected can still go wrong.

It would be satisfying to be able to finish this with a list of lessons learned from this example, but from a technical perspective, I don't think we will be able to do that. I believe the lesson learned in this case study is that strong communication and a timely response have been critical from the beginning of this project and are key ingredients to working through complex design requirements. Frank discussions during the process development phase were critical to developing a reliable and repeatable fabrication process. And when this latest issue was identified, a swift response, testing, and reporting were crucial as we worked to understand this texture anomaly that was ultimately determined to have a significant impact on the end use.

As far as a final resolution, this is still to be determined. Watch for a future column to help bring an ending to this PCB tale—one that will be used as an example for years to come. **PCB007**



Tara Dunn is the president of Omni PCB, a manufacturer's rep firm specializing in the PCB industry. To read past columns or contact Dunn, [click here](#).

Widening the Net

Scientists at Oak Ridge National Laboratory (ORNL) studying quantum communications have discovered a more practical way to share secret messages among three parties, which could ultimately lead to better cybersecurity for the electric grid and other energy assets.

Current protocols, such as quantum key distribution—a prevailing approach in cybersecurity research—are designed for only two parties, and in one instance, uses a pair of light particles called entangled photons. Securely extending quantum cryptography to three parties usually

requires the difficult step of creating a three-photon entangled state.

"In our experiment, we were able to add the laser source as a third active participant while only needing to produce one pair of photons," said ORNL's Brian Williams, lead author of the study published in *Physical Review A*. "Our method removes the need for producing a third photon, which dramatically improves operation efficiency."

This finding could inspire improved security for existing and future computer networks.

(Source: Oak Ridge National Laboratory)

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How to Feed Test Data Back to Engineering for Process Improvement



Feature by Todd Kolmodin
GARDIEN SERVICES USA

Some people think of the PCB manufacturing process as a black box: design data goes to the manufacturer (fabrication house), and magically, the finished PCB is produced. While it may have been like that in the past—such as manufacturing in the ‘80s, which now looks archaic and sometimes unbelievable—in actuality, fabricating PCBs today is quite a ballet of processes. All of the complex steps must be taken in place and in sync to deliver a successful product. The challenge is to identify and feed back as-built testing information to help optimize the design data over time.

Today, as in years past, the OEM design is sent to the manufacturer for processing. There, the design data is massaged to produce the required PCB within the fabrication modes and methods of the manufacturer while still producing the required end product. Now, however, this same design data is also used in other processes throughout the manufacturing process in addition to creating the photo-imaging data and CNC drill/route programs.

This same design data drives other quality control processes too. There are tools and software programs in the verification processes that utilize this same customer supplied data to drive the quality control feedback loop. The design data is used to verify inner layer and outer layer circuits, such as in the AOI and AVI processes (automated optical and visual Inspection). The design data also drives electrical test (ET) processes.

Now, in the PCB manufacturing arena, the ET game has changed considerably. To close the quality feedback loop, even more checks must be included with the board design’s tooling. And the new ET results data requires new presentation methods for an efficient response from the inspectors.

Getting Here From There

Back in the ‘80s, most ET was done by means of “self-learning” a board and then comparing it to the rest of the lot; there was no such thing as netlist test. The risk was extreme with this method because the testing standard relied on a “known good board” to use as the master. If there was no gold-standard board to use, then

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Dk @ 10 GHz - 3.85

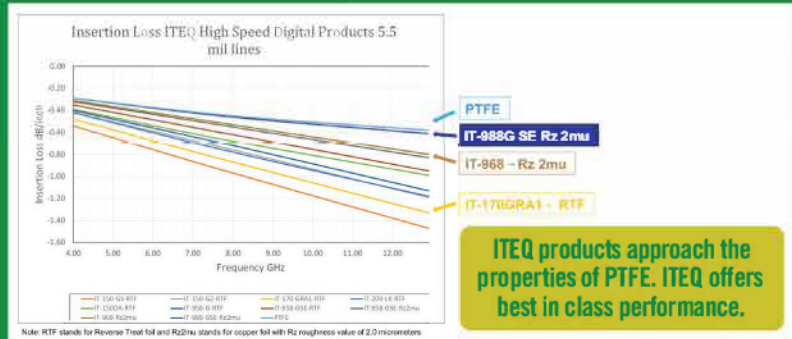
Df @ 10 GHz - 0.0043

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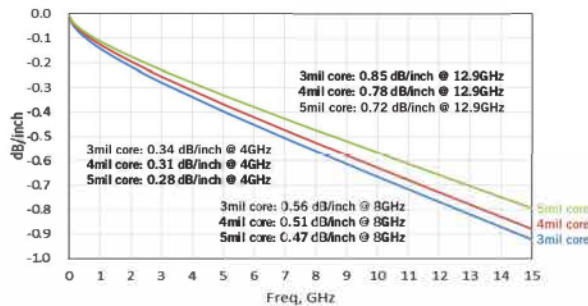
Dk @ 10 GHz - 3.30

Df @ 10 GHz - 0.0019

Insertion Loss - Measured



IT-968 Loss Performance



Industry Test Vehicle

32 layers, 0.140" thick

Four 2 oz copper internal layers

0.8 mm pitch, 9.8 mil drills

- Passed 1000 hours CAF, 10 V bias, 50 V
- 1ST - Passed 1000 cycles, 6x 260 °C precondition

- No delamination after 8x 260 °C reflow after 2 weeks at 35 °C/ 85 % RH

IT-968 SPP Comparison



Ultra Low Loss IT-968 SE

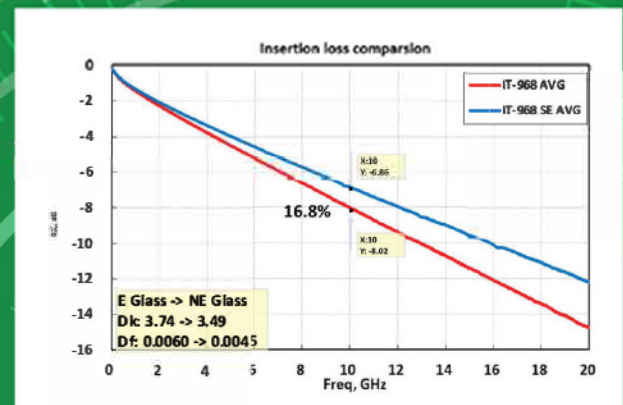
- **Features**
High Tg, low CTE, High Thermal Reliability with Ultra Low Df < .005.
Designed for High Speed Applications.

- **Applications**
Server/Storage/Switch (10G/40G/100G),
Backplane, Telecom, Base Station

Feature High Speed, 25Gbps/path Solution

Property	Test Method	IT-968	IT-968 SE
Tg (°C)	DSC	195	195
T-288 (w/ 1 Oz Cu, min)	TMA	320+	120+
Td-5%(°C)	TGA 5% loss	390+	390+
CTE (%), 50-260°C	TMA	2.2	2.2
Peel strength (lb/inch)	1 oz D-2423	6	6
Water Absorption		< 0.1	< 0.1
Dk, 1 GHz 2-10 GHz	IPC TM 650 2.5.5.9	3.4	3.4
	IPC TM 650 2.5.5.13	3.4-3.7	3.4-3.7
Df, 1 GHz 2-10 GHz	IPC TM 650 2.5.5.9	0.0032	0.0028
	IPC TM 650 2.5.5.13	0.0038-0.005	0.0031-0.004
		0	0

E-Glass vs Low Dk Glass



ITEQ

testing had to make do with a learned comparison test on a sample from the build lot. The risk that the sample board was bad was significant, setting up the age-old “two wrongs make a right” scenario. For example, if the board had a repeating film defect that affected the entire lot, the learn comparison test for ET would have been performed on a bad board. As would be expected, when a bad board is learned and tested against an entire lot of bad boards, they all “pass.” More than once, this false-premise test data resulted in catastrophic failures at the assembler and a 100% reject back to the manufacturer.

The risk that the sample board was bad was significant, setting up the age-old “two wrongs make a right” scenario.

Complicating matters in the ‘80s were the challenges of ET verification. The fixture or grid testers of the day supplied fault data in an X-Y grid coordinate system based on the test fields of the machine. The fixtures used pins that matched the footprint of the PCB and translated down to the X-Y grid where the machine learned the electrical signature of the board. When opens or shorts were detected, they were reported in the X-Y grid. This results data had to be translated by hand to identify the locations on the board where the fault was reported. This was usually done with the help of a mylar grid overlay that the inspectors placed over the board and a datum point identified on the fixture to match to the PCB. The difficulty for the inspectors was in properly identifying the locations on the PCB that the machine had reported. Multimeters or “beepers” were used to ring out the probable fault and determine whether it was an open or a short. This methodology was risky and could easily lead to misdiagnosing a fault, which would then result in an escape.

Netlist Testing

With the advent of netlist testing, it became possible to develop tools to graphically identify the reported fault locations on the board based. Electronic “to-from” lists were now available to translate the fault data from the test machine’s X-Y grid to the actual PCB design. These methods were primitive at first but got the job done with a much greater degree of accuracy than the old overlay method.

Enhancing the quality process is a significant advance in verification. Gardien’s FaultStation is a prime example. FaultStation is designed to seamlessly provide real-time fault verification based on the machine reports, either fixture/grid test or flying probe. In today’s ET arena, data is key.

In Gardien’s case, we receive the tooling data from the manufacturer. Sometimes, that tooling may be just the raw customer data, or it may be post-process tooling data from the manufacturer. But what is new at this point is that the OEM’s electronic netlist is also provided. With a netlist, ET will create the test solution from the manufacturing data and then compare the electrical signature solution to the OEM netlist. This process validates that 1) the ET program data is correct with respect to the OEM requirement, and 2) there were no errors introduced during the manufacturer tooling process.

Figure 1 depicts the Gardien design process flow. Remember, “garbage in, garbage out,” so the proper feedback and check process is essential. The Gardien ET process reviews the customer/OEM requirements as well as the industry specification(s) that may also be necessary; this includes IPC and military requirements as applicable. This also ensures the proper test methodology and test parameters are used when testing the product.

The test equipment will now log their fault data to databases for result retention. FaultStation, for example, utilizes these databases to quickly load fault data from the machines and uses the design data to visually present the faults to the verification operator. Using barcodes from the test machines, the fault report from the machine can be scanned by FaultStation. FaultStation queries the machine data-

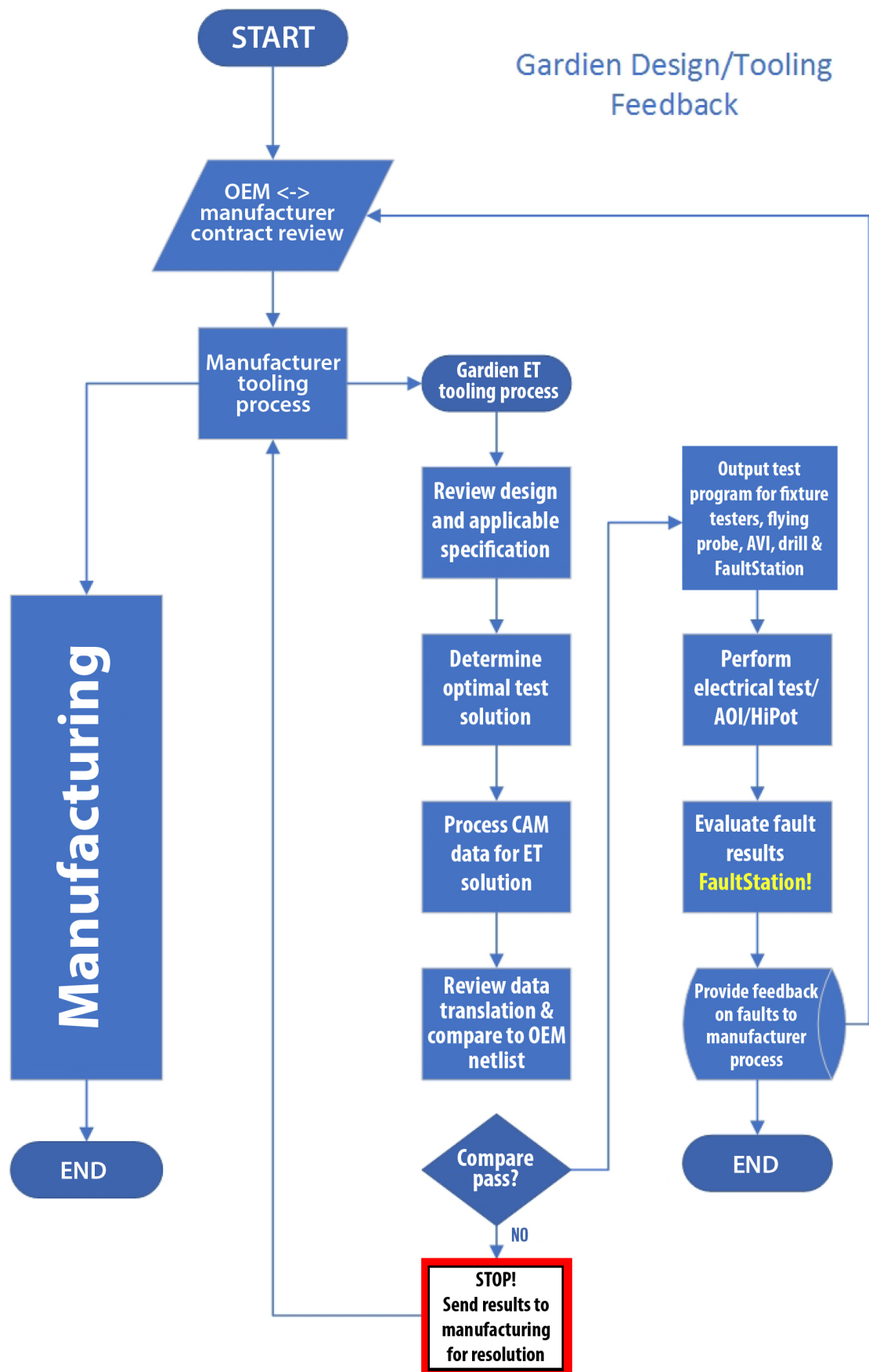


Figure 1: Design/tooling loop.



Figure 2: FaultStation GUI.

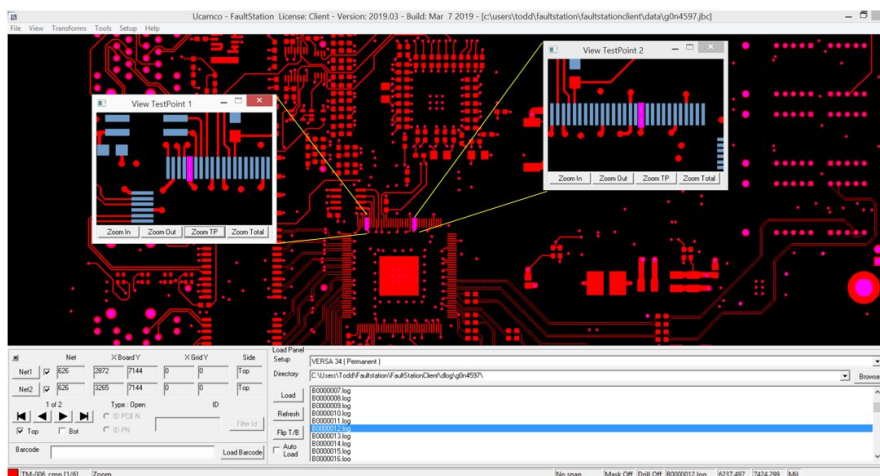


Figure 3: Fault view.

base, locates the fault record, and presents it graphically to the verification operator. Figure 2 shows the main FaultStation user interface. The operator can then step through the faults visually. The result is that the operator can then accurately troubleshoot the PCB because the fault review is based on PCB design data.

FaultStation can evaluate the PCB layout directly against the fault data and predict the probability, and in the case of a short circuit, even the location of the suspected fault. FaultStation logs this data for future reference (example in Figure 3). Based on this data, systemic

manufacturing constraints may be identified and communicated back upstream to process engineering. This can result in improved yields on future runs.

Tools, such as FaultStation, utilize the design data from the front end to create the graphical troubleshooting solution. Essentially, FaultStation uses a “living” electronic PCB developed from the design data from the OEM. This provides yet another quality feedback loop in the matrix when critical and

costly designs are being manufactured. These tools provide a crucial feedback component that can capture defects, analyze probabilities, and provide strong statistical feedback to the front end for adjustments in the process to increase yield and reduce unnecessary non-conformance. **PCB007**



Todd Kolmodin is VP of quality for Gardien Services USA and an expert in electrical test and reliability issues.

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Avoid **Failures** in PCB Production With Compliance Control

The PCB Norsemen
Feature Column by Didrik Bech, ELMATICA

Failures and reliability in the printed circuit industry are usually considered in the context of quality claims and non-conformity. This is a logical approach; however, there is a new context where these aspects are under close scrutiny, namely compliance—especially in the defense industry. Failing to understand import and export compliance for every country you deliver to and from will, at some point, result in challenges in your supply chain with potentially severe ramifications.

The Defining Factor Between Financial Success and Costly Mistakes

To be compliant or not—that is the question to ask. Saying, “Yes, we’re compliant,” is easy, but proving and documenting it is much harder. It is important to understand the challenge and recognize the importance of working diligently with all aspects of compliance. Compli-

ance management in the defense industry can be the defining factor between financial success and costly mistakes.

When procuring components, printed circuits, or materials for the defense industry, there is no such thing as assuming or relying on questionable interpretations of rules and regulations. There’s no option for shortcuts as to whether your supplier follows regulations or not. You must know the country of origin down to the component, the printed circuit or material level of your products, and the bill of materials (BOM) should encompass a country of origin for every article. If you supply to the U.S. defense market, you risk: jeopardizing the business in your entire supply chain; exclusion from delivering to the U.S market; substantial penalties, and possibly jail time if you breach U.S. FAR/DFARS and ITAR regulations. So, how do you ensure that you are compliant with U.S. regulations?



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What Questions Should You Ask?

Here are four questions to address to reduce the chance of failure and increase reliability:

1. How are we organized to meet compliance challenges?
2. What do we prioritize in our compliance work and why?
3. What policies and procedures do we need?
4. How do we train our colleagues in compliance?

A company supplying an article to a product purchased by the U.S. Department of Defense (DoD) must be aware of the strict compliance the DoD places on all exports and imports. The consequences can be severe; there are no excuses, and one cannot simply claim that one did not know; it is your responsibility to know. In other words, plausible deniability does not work.

Sounds scary and like a lot of work? It is, but not being compliant, or not taking the regulations seriously, is even scarier. Again, compliance management in the defense industry is of the utmost importance. A compliance strategy should be simple, stringent, and provide the company with an effective monitoring capability of its supply chain. This can be addressed by asking four questions:

1. Have we identified the risks?
2. Are we monitoring the risks?
3. Have we implemented elements to reduce those risks?
4. Do we have an action plan to implement if needed?

Where Do You Start?

Let's begin with six tips to get you started on your compliance strategy:

1. Stay up to date on rules and regulations. Don't think you know it all. Seek advice.
2. Make sure you have a local champion—one that has the ultimate responsibility for compliance.
3. Involve all departments in a cross-functional, multi-departmental task force, making sure all involved employees

are trained to identify and handle compliance articles.

4. Customize your procedures, systems, and methodologies to support compliance handling.
5. Restrict and control access to sensitive information. Make sure you only grant access to the minimum number of people needed to handle the task.
6. Contact and involve yourself with your customers' products. Request compliance information to ensure that all parties are aware of the risks of being non-compliant. Sharing is caring.

Offering support, knowledge, and service during your customers' product development process is the essential element to reduce the possibility of printed circuit failure and increase the reliability of your customers' products. Ensuring that vital information is shared at the right stage of the product development process will result in the selection of the correct manufacturer, design, compliance setup, regulation, standards, and technical requirements of your printed circuit. Figure 1 shows one example of a product development process and a number of different steps where one can support development to reduce risk and increase reliability.

Each step is equally important for the product and its potential success. We have experienced over and over again that early involvement is the key, and sharing information with compliant partners is the requirement.

Having sorted out all the technical aspects, one question still remains. What information is imperative to have in order to understand the compliance requirements? We have learned that there is some vital information you should have answered. These questions will create a framework for which countries and companies you can cooperate with—an internal risk analysis (Figure 2).

After completing the internal risk analysis for the product, one should consider conducting an external risk analysis (Figure 3). This is an analysis of factors prone to investigate the reclassification cost of your printed circuit. These external factors can affect your supply chain by



Figure 1: Example product development process.



Figure 2: Internal risk analysis.



Figure 3: External risk analysis.

hindering your ability to purchase, produce, or ship printed circuits. These factors should consequently be addressed to reduce the chance of failure in delivering printed circuits.

Do Not Underestimate the Need for Data Security

Finally, in this age of data and IoT, we need to address the necessity to share more and more data. This data or information is also vital to share in order to be compliant and follow laws and regulations. Data and cyber security are unavoidably becoming a pivotal concern in all

companies. “Who should have access to the data? Who is allowed to share the data? How do we save and store the data?” are only a few of the questions one must consider in order to avoid failure. Having a company compliance program combined with a cybersecurity strategy is something we all, sooner or later, will have to address to increase our reliability. **PCB007**



Didrik Bech is the CEO of Elmatica. To read past columns or contact The PCB Norsemen, [click here](#).



Supplier Highlights



Orbotech Celebrates Success of Orbotech Diamond and Discusses Future Trends ►

At the 2019 CPCA Show in Shanghai, Barry Matities caught up with Meny Gantz—VP of marketing for Orbotech’s PCB division—to talk about the drivers behind the success of Orbotech Diamond systems before turning the conversation toward the future and Industry 4.0.

Rogers’ Advanced Connectivity Solutions Adds N.A. Distributor ►

Rogers Corporation’s Advanced Connectivity Solutions (ACS) business unit announced today the introduction of a new distribution channel with the addition of International Electronic Components (IEC) to their sales and service team in the United States and Canada effective July 8, 2019.

DuPont on Materials Challenges and New Opportunities ►

John Andresakis, senior marketing technologist in the Interconnect Solutions (ICS) Group of DuPont, and Jonathan Weldon, RF applications engineer also in ICS at DuPont, spoke with the I-Connect007 editorial team about trends the company is seeing, what challenges their customers are facing with materials today, and future opportunities with new technologies, including 5G, electric cars, IoT, and more.

Creating Stability in Materials Chaos ►

Nolan Johnson and Tony Senese—manager, business development group, Panasonic EMBD—discuss the evolution of the materials marketplace over the years from a time when the market aligned for the rise of Panasonic’s MEGTRON 6 to the ever-changing materials industry of today.

Taiyo America Opens San Jose, California, Office ►

Taiyo America Inc., a subsidiary of Taiyo Holdings Co. Ltd., has opened a new office in Silicon Valley, USA.

Laminate Suppliers Face Increasing Demands From Customers ►

In an interview with Nolan Johnson, TUC North American President Alan Cochrane talks about the company’s shift toward trending areas and how strategies like the adoption of thinner glass styles have helped make it all possible.

atg’s A7-24 Provides TTM Large Format Testing Capability ►

atg Luther & Maelzer GmbH has announced the installation of its first extra-large format 24 test head flying probe system at the TTM Technologies Stafford Division.

Insulectro’s OEM Program: Time to ACT! ►

Ken Parent, Insulectro VP of sales and product management, discusses the current dynamics in the materials marketplace and how Insulectro is developing educational resources to help design teams and fabricators better understand the capabilities and features for the emerging laminate materials.

Isola on Adapting Processes to Meet Customer Needs ►

Sean Mirshafiei, chief sales and marketing officer for Isola, discusses the company’s perspective on material market trends and how they are adapting product development processes to respond to new customer needs.

5G: Higher Frequencies!

Do you have the **right** circuit materials?

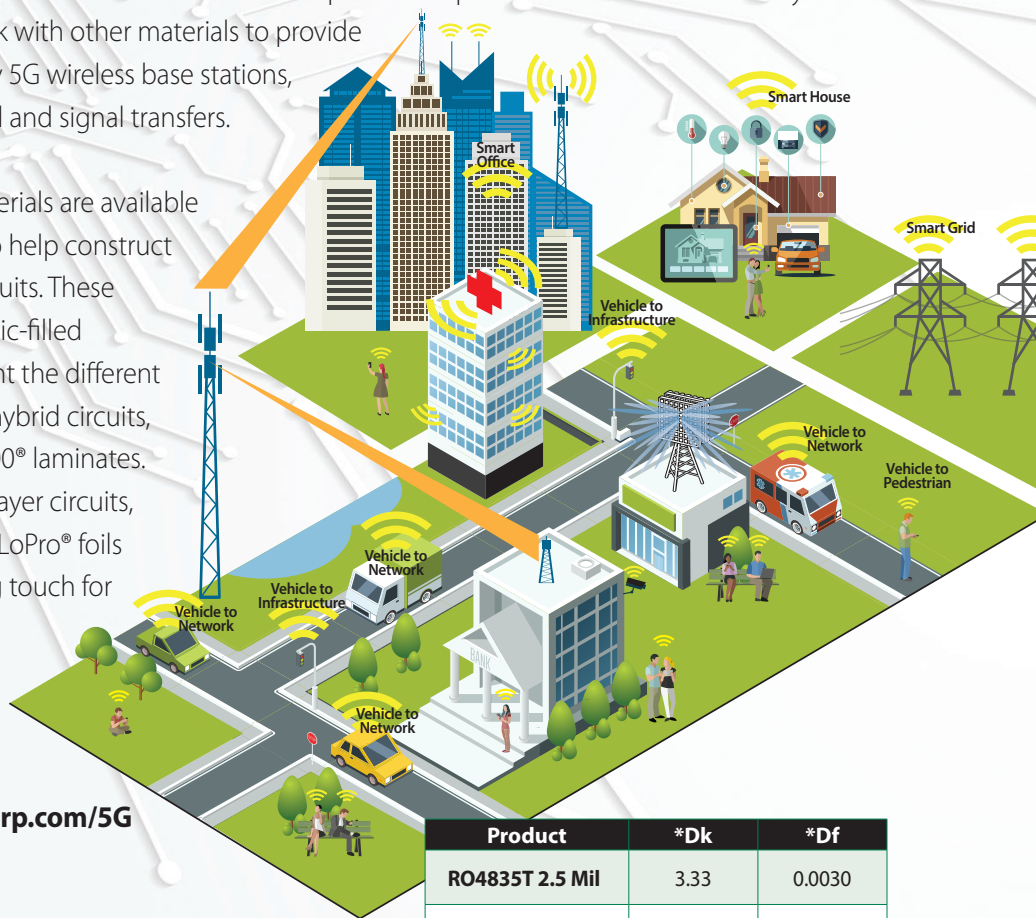
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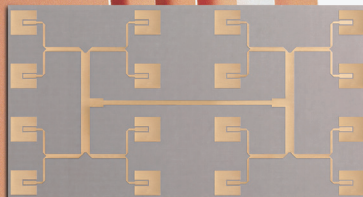
Product	*Dk	*Df
RO4835T 2.5 Mil	3.33	0.0030
RO4835T 3.0 Mil	3.33	0.0034
RO4835T 4.0 Mil	3.32	0.0036
RO4450T 3.0 Mil	3.23	0.0039
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Focusing on Surface Sensitivity for Reliability

Feature Interview by Andy Shaughnessy
I-CONNECT007

During the IPC High-Reliability Forum and Microvia Summit, I spoke with Customer Applications Scientist Elizabeth Kidd and Sales Engineer Alex Bien, both of BTG Labs, about their presentation on the challenges of working with highly sensitive surfaces, such as the risk of contamination. We also discussed the various surface characterization techniques that BTG Labs uses to identify such contaminants, and some PCB design strategies for creating a better surface—and a more reliable board.

Andy Shaughnessy: Elizabeth, it's nice to meet you. I know you're giving a presentation in a few days, but tell us about the company, and then we'll talk about your presentation.

Elizabeth Kidd: Sure. BTG labs is a materials science company specializing in surface science and adhesion technologies. We have our roots in being a research and development lab and scoping root cause analyses for people who are scratching their heads at these industrial adhesion problems. From there, we develop the technology to make manufacturing floor inspections of materials as they go through their critical surface process points.

Alex Bien: We help folks to hone in on one area—the surface—that they've never had eyes



Elizabeth Kidd and Alex Bien

on nor had a way to quickly evaluate surface chemistry in a fast, point-and-shoot manner. Our opening speaker today is addressing this lack of insight into the three nanometers that we need to control to create reliable adhesion. Thus, our focus is putting that technology to the floor in the hands of people who are making dollars-and-cents decisions every day.

Kidd: And taking the high sensitivity of R&D techniques—such as XPS, X-ray photoelectron spectroscopy, and FTIR, which is Fourier transform infrared spectroscopy—that have their eyes on the top molecular layer of a surface, and being able to scale that to a method or technique that can be taken onto the manufacturing floor.

Shaughnessy: Can you also tell us about your presentation?

Kidd: The presentation addressed what we just mentioned—controlling your surface process to better your wire bonding, die pad bonding, laminate coating adhesion, and all of those things. We even have some applications for the coupling agents that we were speaking of known as a conversion coating, and other industries use those organosilanes to increase adhesion between organic material and inorganic material.



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Shaughnessy: Are you talking about copper, FR-4, and any sort of surface?

Kidd: Yes. We'll have some applications in metals, polymers, and in composites as well.

Bien: That's a good point, though. It's particularly difficult to control surface chemistry and match surface chemistry between dissimilar materials. It's very easy to bond metal to metal, and it's pretty easy to bond composite to composite, but metal to polymer, glass to polymer, and those material interfaces are more challenging to create to promote adhesion.

It's particularly difficult to control surface chemistry and match surface chemistry between dissimilar materials.

Shaughnessy: What are the biggest takeaways from your talk?

Kidd: Namely, the sensitivity of this surface. As Alex mentioned, we have a monomolecular layer that we're trying to control, and that layer is highly sensitive to contamination events. Contact contaminants from the manufacturing process—things like upstream process aids from stamping or anything left over from any wash process from a chemical etch bath—have a huge impact. Or perhaps you've had a change in your supply chain where supplier X used chemical X, and now supplier Y is using chemical Y, and all of a sudden, you have more random failures or successes, and you don't know why.

It's drawing attention to those small changes in a process that can affect that monolayer that we're trying to adhere to. We'll mainly be talking about contamination, how to look for it, how to characterize that, using various surface characterization techniques—such as FTIR, XPS, and contact angle measurements—

and surface activation and detection of coatings. The main takeaway is to increase the awareness of the sensitivity and how you can change—negatively or positively—that surface, even unknowingly.

Shaughnessy: With one small thing having a large influence on the process.

Bien: A small change in the process creates a snowball effect downstream.

Kidd: Exactly. Think about a fingerprint. If you put a fingerprint on the surface, that's 1,000–10,000 molecules thick. If you try to stick something to it now, you're not sticking to the surface; you're sticking to the chemicals and the oil from that person's fingers. That kind of sensitivity is important.

Shaughnessy: You measure down to the angstrom level?

Kidd: Yes.

Bien: A couple of nanometers is the thickness that we want to be sensitive to.

Shaughnessy: And you get to see it on a monitor? Do you get a read-out?

Bien: It's a digital output.

Kidd: We have a couple of machines and products called the Surface Analyst that will allow inspections to be made. We have an automated solution that will deposit the droplet, analyze the droplet, and give you a read-out. It can mash all of the data together to give you a statistical output that is significant for whatever manufacturing process you are trying to look at—batch to batch and all that jazz.

Bien: We employ every surface technology that's in the marketplace. We're a process development and optimization house as well as a manufacturer of products that allow companies to measure and control their surfaces, and we see this as a hole in this industry. There's a

real need out there. Most folks don't have access to Ph.D. materials scientists. If a company is able to employ a Ph.D. in materials science, they are usually down the hallway from your manufacturing facility and not working hand-in-hand with those on the production floor. We work with those people to bring about knowledge expertise and process recommendation to gain very high reliability where stresses, temperatures, thermal cycles, and contamination events are critical, and sometimes in defense or medical device cases, have to deal with lives.

Shaughnessy: What is the threshold for the switching method for going between XPS and traditional and ion chromatography? How do you know which techniques to use?

Kidd: C3 extraction and ion chromatography take a solvent and apply a very small amount to dissolve what you have on your surface. Then, you will use an ion chromatograph to look at what kind of species or ions you're seeing from what has been dissolved on the surface. That is a measure of what your solvent can dissolve. Using an in-situ spectral technique like infrared spectroscopy or XPS is a direct measure of the surface state. You don't have to worry about having some kind of solvent medium to dissolve the material. You're looking at what's there. It's a direct measure or a direct eye on the functional groups that you have on those materials.

Bien: Solvent extraction is more of a legacy method. You would use it in cases where you don't have access to spectroscopy.

Kidd: Right, and for the C3 IC methodology, that does a good job at detecting conductive species, but it's not going to tell you if you have an organic species that has made its way onto your surface from some kind of environmental contaminant or upstream contact contamination event. It's going to tell you if you're chemical etch bath is leaving behind ions that would otherwise create a pathway to short-circuit your board. It's not going to give you evidence of oil amount or if you have silicone or something like that.

Shaughnessy: What are the biggest challenges that your customers are facing that you can help them with?

Bien: Most folks have intermittent failures where they don't have any understanding of why this is happening now versus two months before when they made 500 boards in a run, and everything was great. In terms of the organics that Elizabeth mentioned, the organic materials finding their way into processes are the reason for adhesion loss most of the time. There are three things that we need to control to get reliable adhesion: (1) the chemistry of the adhesive and the coating that we're putting down, (2) the chemistry of the surface that we're presenting to that adhesive, and (3) how we cure it in terms of temperature, pressure, environment, etc. Most people are doing steps one and three, but they're not taking a good look at step two.

In terms of what we're seeing out in the marketplace, it's a lot of things like wash processes that are dragging soaps and surfactants out of them and manufacturers not having good techniques to identify those before they send them into SMT process or conformal coating process. It's a breakdown somewhere in the chain of events that are in the manufacturer's procedural steps, from incoming component surface inspection all the way until final assembly. It could be in a wash process or plasma treatment process, but it's a failure of knowledge of how to tune the knobs.

Kidd: And to that point, people are monitoring the knobs. In the case of a parts washer, they're monitoring the concentration of cleaning agent and particulate count, temperature, and cycle time. What they're not measuring is the actual surface that's coming out of that washer. For example, you could have a washer that has been recently cleaned and is in pristine condition, passing all of your checks—including particulate count and concentration analysis. And you could have a washer that has been running for a month, has the "correct" cleaning agent concentration, and is passing the particulate amount. But if the agent you're trying to clean

is an oil, it's not going to give you eyes on how much concentration of oil you have that you have removed from previous batches. Looking at those process parameters is not enough; you have to look at the resultant surface chemistry on the back end of it.

Shaughnessy: Is there anything that PCB designers should do, or not do, to help create a better surface?

Kidd: The best thing product designers can do to create a surface that won't hinder adhesion is to build in surface quality validation checks throughout the production process. When these steps are implemented from the very beginning it puts technicians, designers, engineers, and operators all on the same page about the importance of surface quality in an adhesion process. It doesn't do any good to have all these treatment and cleaning steps if there is no way to measure and evaluate what kind of surface you're creating.

Everything that is done in the lab that affects surfaces must be able to be done in the manufacturing facility.

What they should not do is develop laboratory tests and surface evaluations that cannot be scaled to the production line. Everything that is done in the lab that affects surfaces must be able to be done in the manufacturing facility. Otherwise, the tests aren't correlating to the kinds of surfaces being created in production. Designing the process to ensure adhesion predictability through data-rich feedback controls is the best way to create and maintain consistent surfaces.

Shaughnessy: How is the company doing?

Bien: We're doing great! Elizabeth has been on-board for four years now. I was employee #17,

so we're up to 33 now. We're focused in on the electronics market. We came from a background of aerospace, and we're constantly finding new places where companies are not controlling their surface. Our top markets are aerospace, electronics, medical devices, and we do a lot of work in automotive and consumer products as well. We're growing every year. A lot of our effort is going towards automating the kind of inspections and measurements we've been talking about.

Shaughnessy: It's funny that we're seeing such an increase in the last 10 years or so in cleaning in general. Now, everybody is realizing that contaminants are a problem, and there are consequences, such as non-adhesion.

Bien: Well, today's quality is tomorrow's scrap, right (laughs)?

Shaughnessy: Right. Even if it works, it's ending up in a landfill. Is there anything else we haven't mentioned that you'd like to talk about?

Bien: If you want to understand more about surface chemistry and how it relates to your process, we have a great blog that we put out weekly, which is an awareness article per week. It comes out every Thursday. You can find that on our website at btglabs.com.

Kidd: And to drive that home, the uniqueness of BTG Labs—and one of the very attractive things that I have found that I'm learning about this company—is that we don't have somebody pay thousands of dollars for a study and then hand you a report with a bunch of squiggly lines and numbers. We're going to make sense of the information and help people to better build their surface process control or build their material system and educate them about the holistic material process that they're looking at.

Shaughnessy: That sounds good. Thank you.

Kidd: Thank you, Andy.

Bien: Thanks. PCB007

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ACCEPTING APPLICATIONS

Sunday Afternoon in Dongguan

Ladle on Manufacturing
by Marc Ladle, VIKING TEST LTD.

Every time I come to China, there is always something new to see. The skyline changes at a pace that makes most of the rest of the world appear to be asleep. But even with a reasonable amount of prior experience, I have been a little surprised by what I have seen in Dongguan today.

I really don't want to make any political comments or get involved in disagreements and negotiations between continents and countries, so I would like to make my position quite clear. I primarily regard myself as pro-human. The world will be a better place when every person on the planet has the same chance for good health, happiness, and the opportunity to achieve their potential. Employment certainly plays a part in this, and as far as I am concerned, the goalposts moved for me today.

I have made more than 30 visits to China over the past 12 years, and I have always been impressed with the governmental policies that have helped living standards improve so quickly. Advances in technology certainly move very fast over here. The policy in China is to encourage business and technology with a view of improving employment opportunities for all.

In the U.K., the national news has featured ongoing concerns over the hardware manufactured by the Chinese company Huawei. It has been mentioned often enough that most of the time, the BBC newscasters now have the pronunciation of the company name similar to how it would be pronounced in Chinese. To my ears, it sounds like "Wah Way."

I knew a little about Huawei before today, and I have previously checked out their smartphones. The current models definitely seem to keep up with other manufacturers of similar devices. Based on this, I assumed they were a decent-sized company with nice facilities.

The reason all of this appeared on my radar today was because I had a free afternoon with my wife, and I wanted to visit something new while we were in China. I have a reasonable excuse for doing this because occasionally, I need to look after a customer while they are visiting this area, and I always like to show them something they have not seen before. My good friend, Mr. Jermin Wang, has looked after me in China for more than 12 years now, and he came up with the idea of visiting Songshan Lake. I was promised beautiful views and the opportunity to cycle around the lake. While we were on the way to the lake, which was around



Figure 1: Huawei development, Songshan Lake.

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one hour from our hotel, Jermin shared that Huawei was in the process of building a new facility there.

Songshan Lake is a pretty large area. We drove for a while, admiring the views from the car and looking for a place to park. At one point, the design of the buildings changed notably to a very European style that reminded me of Germany. We drove further, and the design changed a little and became a little more French and then Tuscan. Jermin told us that all of this European-style development was owned by Huawei (Figure 1). The sheer scale of the development and the quality of the environment being created was staggering. I am not super confident about the figures I was given, but I was told that 20,000 Huawei workers have transferred to this site so far. The amount of construction currently underway suggests the final figure will be a multiple of this number.

It was impossible to guess the purpose of each building, and I am sure some of the structures are more industrial than they appear from the outside, but at a glance, we could have been in Europe. An example of this was a building that appeared to resemble a church (Figure 2).

We proceeded with our plan for a gentle cycle ride around the lake. My wife Linda is not a cyclist, and a little persuasion was needed to get her on the back of a tandem we hired from a local kiosk. I am glad the path was pretty level because there was not much added power coming from the pedals at the rear. Every wobble was accompanied by a little shriek from behind my left ear and smiles and laughs from the locals who were happy to stop and watch us make our precarious progress.

The whole area is pretty idyllic and rivals most of the parks I have visited in Europe. If I had to make a comparison, I would probably pick Bourneville, which is near Birmingham in the U.K. John Cadbury, a Quaker and philanthropist in the mid-19th century, built a “model village” to house his workers and carry out his business of confectionery manufacturing. His primary consideration was the health and well-being of his workforce. Cadbury is still a world-renowned name today after more than 100 years. This long-term success may be at least in part due to the way the company looked after their workers. There are definite parallels with the Huawei development at Songshan Lake, although the latter dwarfs the

scale of the former by a considerable amount (perhaps 50,000+ residents compared to around 1,000 in Bournville).

The Songshan development is undoubtedly a very attractive place to live and work. There were plenty of people relaxing and enjoying the fresh air and fine weather and well-maintained landscaped gardens. The landscaping and planting are quite beautiful, and the facilities look like they have been very well thought through. Fur-



Figure 2: The church.



Figure 3: Tram station.



Figure 4: Tram into town.

ther, there is a tram system extending across the whole Huawei complex with regular stations (Figures 3 and 4).

Of course, there is also a level of security that prevents the casual visitor from wandering in. At every entrance, there was a manned checkpoint with polite and friendly security guards who were happy to explain that it was possible to tour the complex but only in the company of a member of Huawei staff and with prior arrangement (Figure 5). We checked with a friend who works for Huawei in Shanghai, and he confirmed that he would have been able to show us around if he had been present.

In this case, with no available escort, we were limited to taking a look at the areas still under construction (Figure 6). Even the security points were built to fit in with the architectural plan. I would be very happy to take up residence in a building like that!

We retreated to a coffee shop for a cool drink

to consider what we had seen. It seems pretty obvious to me that Huawei is planning for the long term. This is a company that wants to attract the best staff by offering a working environment and employment conditions that are the very best possible by any standards.

I can't help wondering if some of the reason that Huawei has been singled out for close scrutiny on the international stage is because of the strength of their long-term business model



Figure 5: Security gate under construction.



Figure 6: Buildings under construction.

and ambitions, which must be quite a serious threat to the established leaders in the field, including a lot of American companies. Could there be an element of protectionism involved in some country’s current foreign policies?

If there was a public hotel amongst the complex, I would seriously consider booking my summer vacation in the new Huawei town next year. Taking a gentle wander through representations of various regions of Europe. Spending the morning sipping a coffee in a French coffee bar followed by a short tram ride to Tuscany for a lazy afternoon stroll along the lake-

side with a spot of fishing. Heading to Bavaria for the evening to enjoy a cold beer and pork knuckle meal. Of course, I am imagining what it may be like inside the campus, but if the internal arrangement is a fraction of the external facade, then it would be impossible not to be impressed. **PCB007**



Marc Ladle is a director at Viking Test Ltd. To read past columns or contact Ladle, [click here](#).



Denny Fritz: The Difference Between Quality and Reliability

Andy Shaughnessy recently spoke with industry veteran (and I-Connect007 columnist) Denny Fritz at IPC’s High-Reliability Forum and Microvia Summit in Baltimore, Maryland. Their conversation explored the relationship between quality and reliability—two terms that are unequal but often used interchangeably. Andy and Denny also discussed the current state of lead-free solders in the U.S. military and defense market and the microvia reliability issues Denny discussed during his presentation at the Forum.

[Click here](#) to read the full interview.

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Fein-Line Associates is a consulting group serving the global interconnect and EMS industries, as well as those needing contact with/information regarding the manufacture and assembly of Printed Circuit Boards. The principal of Fein-Line Associates, Dan (Baer) Feinberg, formally president of Morton Electronic Materials (Dynachem) is a 50+ year veteran of the printed circuit and electronic materials industries. Dan is a member of the IPC Hall of Fame; has authored over 150 columns, articles, interviews, and features that have appeared in a variety of magazines; and has spoken at numerous industry events. He covers major events, trade shows, and technology introductions and trends.

Mr. Feinberg and his associates specialize in:

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- merger and acquisition due diligence
- market information and market research
- expert witness assistance and seminars regarding all aspects of printed circuits
- electronic assembly manufacturing and marketing



Dan (Baer) Feinberg

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Editor Picks from PCB007

1 It's Only Common Sense: The Consultative Sale ▶

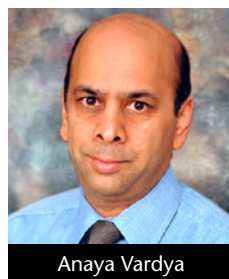
The best way to represent yourself and your company as a true expert is to produce and publish valuable content about your products through content marketing. The key word is valuable.



Dan Beaulieu

2 Standard of Excellence: Three Ways to Face the Future With Your PCB Suppliers ▶

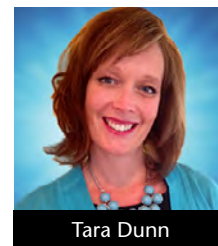
Once you have established a solid, trusting relationship with your PCB vendor, you can start working together developing new products, technologies, and in some cases, services. Here are three ways that you can work with your PCB suppliers to face the future.



Anaya Vardya

3 Flex Talk: New Materials or New to You? ▶

There are so many new processes and materials in the PCB segment that it can be a challenge to keep up with all the new developments. It is fun to start chasing the next new thing, but it is important to keep in mind that even materials and processes that have been around for a while are still new to someone.



Tara Dunn

4 ICT 45th Annual Symposium Review ▶

The Institute of Circuit Technology (ICT) held its 45th annual symposium on June 4, 2019, in Dudley at the Black Country Museum—a symbol of the spirit of innovation in engineering technology and the entrepreneurial and manufacturing skills that had established that region's supremacy in leading the original Industrial Revolution. Here's a recap of the events and presentations at the symposium.

5 AWE 2019: Go XR, Be Awesome ▶

Dan Feinberg attended and covered the recent 2019 Augmented World Expo (AWE) and conference in Santa Clara, California. The event featured the latest developments and technologies in augmented (AR), mixed (MR), virtual (VR), and extended virtual reality (many just call it all XR to make it simple). Here's a wrap-up of the event.



Dan Feinberg

6 The Right Approach: Help Wanted! How to Train New Employees in Today's Digital World ▶

In six short years, millennials will make up around 50% of the global working population. With our ever-increasing culture of information overload since the mobile revolution began, attention spans have been shrinking. While millennials seem to be the subject of much of the reporting on Digital-Age attention spans, the effect can be seen across all age ranges. How can you train anyone in this environment? Read on.



Steve Williams

7 EPTE Newsletter: JPCA Show 2019, Part 1 ▶

The three-day JPCA Show last month at Tokyo Big Sight was sold out despite the slowdown for the global printed circuit industry. The show came at a good time and gave me the opportunity to network, collaborate, and collect market data for both business and technology trends.

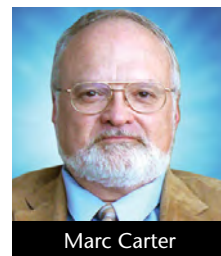
8 IPC: April 2019 Book-to-Bill Ratio Rises to 1.02 ▶

Total North American PCB shipments in April 2019 were up 6.6% compared to the same month last year. Year-to-date sales growth as of April was 14%.



9 Better to Light a Candle: Chapter Three—First-year Recap of the PCB Fabrication Course at MTU ▶

In the third installment of this column series, Marc Carter acknowledges the many organizations and individuals that willingly and freely contributed their time, materials, and support to make this first “prototype” effort a success.



Marc Carter

10 IMPACT Washington, D.C. 2019 Recap: Leaders Call for Action on USMCA Trade Deal ▶

Top executives from electronics companies across the United States were in Washington, D.C., to call on the Trump administration and Congress to support policies that will drive the electronics industry's future growth in North America and worldwide.



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Development Chemist Carson City, NV

Develop new products and modify existing products as identified by the sales staff and company management. Conduct laboratory evaluations and tests of the industry's products and processes. Prepare detailed written reports regarding chemical characteristics. The development chemist will also have supervisory responsibility for R&D technicians.

Essential Duties:

- Prepare design of experiments (DOE) to aid in the development of new products related to the solar energy industry, printed electronics, inkjet technologies, specialty coatings and additives, and nanotechnologies and applications
- Compile feasibility studies for bringing new products and emerging technologies through manufacturing to the marketplace
- Provide product and manufacturing support
- Provide product quality control and support
- Must comply with all OSHA and company workplace safety requirements at all times
- Participate in multifunctional teams

Required Education/Experience:

- Minimum 4-year college degree in engineering or chemistry
- Preferred: 5-10 years of work experience in designing 3D and inkjet materials, radiation cured chemical technologies, and polymer science
- Knowledge of advanced materials and emerging technologies, including nanotechnologies

Working Conditions:

- Chemical laboratory environment
- Occasional weekend or overtime work
- Travel may be required

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Assistant Department Manager, Operations, Carson City, NV

This is an entry-level professional management trainee position. Upon completion of a 1-2-year apprenticeship, this position will be elevated to facility/operations manager. Primary functions during training: shadow incumbent staff managers to learn and understand the operations and personnel of the operations department. This position will train and learn, develop, implement, and coordinate strategies related directly to the manufacture of Taiyo products. Additionally, this position will be learning all about the facility, environment, and health and safety functions. Eventually, this position will be responsible for the administration, security and maintenance of the facility and warehouse

Required Experience/Education:

- 4-year college degree in industrial engineering or another similar science discipline combined with work experience in ink or coatings manufacturing
- Ability to read, analyze, and interpret common scientific and technical journals, financial reports, and legal documents
- Ability to respond to inquiries or complaints from customers, regulatory agencies, or members of the business community
- Ability to develop and implement goals, objectives, and strategies
- Ability to effectively present information to top management, public groups, and/or boards of directors
- Ability to apply principles of logical or scientific thinking to a wide range of intellectual and practical problems
- Knowledge of governmental safety, environmental, transportation regulations/laws

Preferred Skills/Experience:

- Bilingual (Japanese/English)
- Toyota Production System (TPS)

Working Conditions:

- Occasional weekend or overtime work

See complete job listing for more information.

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Technical Support/Sales Engineer, U.K.

We are looking to expand our U.K. technical support team. As a technical support/sales engineer (home office/Leamington Spa), you will assist potential customers and current customers in appreciating the benefits of using—and optimizing the use of—Ventec materials in their printed circuit board manufacturing processes, enhance customer loyalty and satisfaction, spread the use of Ventec materials, and grow sales. You will provide a two-way channel of technical communication between Ventec's production facilities and U.K./European customers.

Skills and Abilities Required for the Role

- HNC, HND, degree, or equivalent in a technical/scientific discipline
- Scientific/technical educational background
- Printed circuit board industry experience an advantage
- Good written and verbal communications skills
- Ability to work in an organized proactive and enthusiastic way
- Ability to work well both in a team as well as an individual
- Good user knowledge of common Microsoft Office programs
- Full driving license essential

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Qualifications:

- A self-motivated business professional who is driven to succeed with a minimum of 3 years outside sales experience in the PCB or PE industry
- Proven sales/business development record
- Excellent communication and interpersonal skills
- OEM and electronic assembly experience is a plus

We offer:

- Competitive salary and commission plan with a comprehensive benefits package
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Analyst Programmer, Hong Kong

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The analyst programmer will assist the IT and ERP manager in Hong Kong to support the company's BI systems, ERP systems, and other related IT-landscape applications.

In addition, this post will participate in system development projects and provide support including, but not limited to, user requirement collection and analysis, user training, system documentation, system support and maintenance, enhancement, and programming.

- Develop and enhance related IT systems and applications
- Prepare functional specifications
- Transfer the relevant business and interface processes into IT systems and other applications to get a maximum automation degree and prepare all required business reports
- Conduct function testing and prepare documentation
- Manage help desk/hotline service

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APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

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Field Service Engineer: Multiple U.S. Locations

Reporting to a regional service manager, these customer-focused engineers will uphold the Koh Young culture while delivering professional technical services for our award-winning portfolio of inspection solutions. The role will enthusiastically visit our growing list of customers for installations, training, and evaluations, as well as technical support and maintenance.

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Koh Young is the leading 3D measurement-based inspection equipment and solutions provider. We perform quality control and process optimization across a growing set of industries including PCBA, machining, final assembly, process manufacturing, and semiconductors. In addition to our corporate office in Seoul, our international sales and support offices help us maintain a close relationship with our customers and provide access to a vast network of inspection experts.

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Vision and Machine Learning R&D Engineer Atlanta, GA or San Diego, CA

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The role will develop practical, scalable 3D machine learning solutions to solve complex challenges that detect, recognize, classify, and track medical imagery. Additional focus on the design, implementation, and deployment of full-stack computer vision and machine learning solutions.

The ideal candidates will hold a master's (doctorate preferred) in computer science or electrical engineering with at least three years of relevant experience. We desire a strong understanding of machine learning and computer vision algorithm application within embedded systems, plus significant vision expertise in multi-view geometry, 3D vision, SFM/SAM, and activity recognition.

Koh Young is the leading 3D measurement-based inspection solutions provider. We perform quality control and process optimization across a growing set of industries including electronics, final assembly, semiconductors, and most recently, medical imagery.

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Technical Sales Engineer San Jose, CA, USA

The technical sales engineer will perform technical audits and help customers troubleshoot and optimize their solder mask process, prepare and deliver technical presentations explaining products or services to customers and prospective customers, collaborate with sales teams to understand customer requirements and provide sales support, secure and renew orders and arrange delivery, and help in researching and developing new products.

Required Education/Experience:

Applicants must have good "hands-on" knowledge of the printed circuit board (PCB) industry and the liquid photo imageable (LPI) solder mask process. Candidates must be self-motivated, capable of managing key accounts and developing new business opportunities that generate new sales.

- College degree preferred with solid knowledge of chemistry
- 3-5 years of work experience in a technical role within the PCB industry
- 3-5 years of work experience in a sales role
- Computer knowledge, Microsoft Office environment
- Good interpersonal relationship skills
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Working Conditions:

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- Execution of machine training

Your profile:

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- High willingness to travel and have flexible employment
- Service-oriented and like to work independently

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SMT Field Technician Huntingdon Valley, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:

- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:

- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
- Ability to arrange and schedule service trips

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- Retirement fund matching
- Continuing training as the industry develops

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Sales Personnel, Japan

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Training will be provided along with a competitive benefits package, excellent growth opportunities, and periodic bonuses.

Interested candidates, please contact us at careers.jp@gardien.com with your resume.

Kindly note only shortlisted candidates will be notified.

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This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

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Events Calendar

NEPCON South China 2019 ▶

August 28–30, 2019
Shenzhen, China

C3Bio Conference on Biosensors, Bioelectronics, and Biodevices ▶

September 9–10, 2019
Bath, U.K.

C3Bio Training Workshop on Lab-on-Chip ▶

September 11–12, 2019
Bath, U.K.

EIPC PCB Pavilion @ WNIE Exhibition ▶

September 18–19, 2019
Warwickshire, U.K.

productronica India 2019 ▶

September 25–27, 2019
Delhi NCR, India

electronica India 2019 ▶

September 25–27, 2019
Delhi NCR, India

52nd International Symposium on Microelectronics ▶

September 29–October 3, 2019
Boston, Massachusetts, USA

IPC Electronics Materials Forum ▶

November 5–7, 2019
Minneapolis, Minnesota, USA

productronica 2019 ▶

November 12–15, 2019
Munich, Germany

2019 International Electronics Circuit Exhibition (Shenzhen) ▶

December 4–6, 2019
Shenzhen, China

Additional Event Calendars



Coming Soon to *PCB007 Magazine*:

AUGUST: Wet Processes

Wet processes are the core of printed circuit fabrication. What's new? Are there new offerings down the road to make your wet process capabilities sharper? Faster? Greener? Easier to operate? Find out in this issue.

SEPTEMBER: Standards

We report on recent developments in current and emerging standards and take a step back to discuss some of the inherent strengths and weaknesses of standards processes.

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