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JULY 2012

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July 2012 Featured Content

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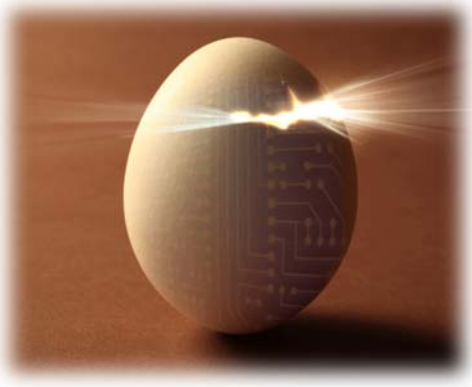
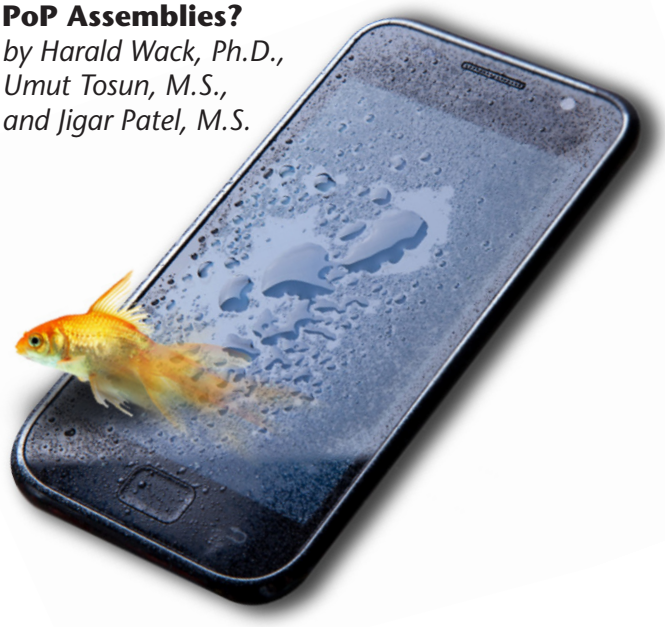
Companies are dealing more and more with advanced packages: Chip-scale packages, BGAs, stacked chips, through-silicon vias—the list goes on and on. This month, we tackle the subject with an array of articles on advanced packaging.





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THE WAY I SEE IT

Let Them Eat Cake

by Ray Rasmussen
I-CONNECT007

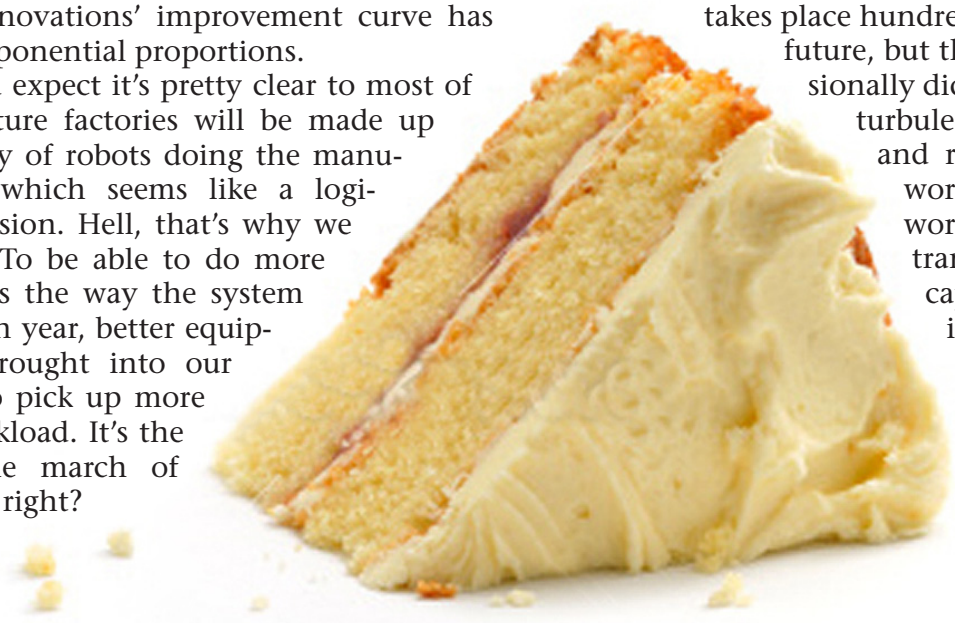
Summary: We've seen the pace of innovation increase with the industrial revolution and now, with the introduction of electronics, the pace of change has accelerated, dramatically. Leaving the linear, incremental world behind, innovations' improvement curve has reached exponential proportions.

Recently, I watched an interview with Google CEO Larry Page in which he talked about the initiatives underway at the search engine giant. That interview, along with a few other articles and recent events, got me thinking about the state of manufacturing and where we're likely headed.

Throughout history, engineers, scientists, tinkerers, and inventors have been looking for ways to do things better. New materials, new techniques, and completely new approaches to problems have led to a host of innovative new products, which have been, mostly, of great benefit to society. We've seen the pace of innovation increase with the industrial revolution and now, with the introduction of electronics, the pace of change has accelerated, dramatically. Leaving the linear, incremental world behind, innovations' improvement curve has reached exponential proportions.

I would expect it's pretty clear to most of us that future factories will be made up increasingly of robots doing the manufacturing, which seems like a logical progression. Hell, that's why we automate: To be able to do more for less. It's the way the system works. Each year, better equipment is brought into our factories to pick up more of the workload. It's the unstoppable march of progress, right? But we seem to be at a crossroads. Traditionally, we used automated equipment to replace humans for mind-numbing, repetitive daily tasks. Most of us should see the logic in that. But today, there's an eminent convergence of these evermore powerful "learning" computers (Watson from IBM) along with much more capable machines (Google's self-driving car), the implications of which are becoming a bit scary.

Of course, as we transition to this *Star Trek*-like existence where humans (highly educated) pursue more lofty ideals, going "where no man has gone before," leaving robots to grind through the daily chores, there likely will be disruptions in our social fabric. The majority of the world's population, already vastly underemployed, will be displaced (by those who have jobs or could have jobs) increasingly by these very capable surrogates for human labor. It's an interesting societal paradox: Automation reduces the costs of making goods and services accessible to more people around the planet, while, at the same time, eliminating critically needed jobs in underdeveloped countries with extremely low standards of living and high unemployment rates. Of course, *Star Trek* takes place hundreds of years in the future, but the TV show occasionally did look back at the turbulent years of war and revolution as the world supposedly worked through the transition from our capitalist economic system to that "greater good" society where the drivers aren't so much economic, but needs-based; a world where, as



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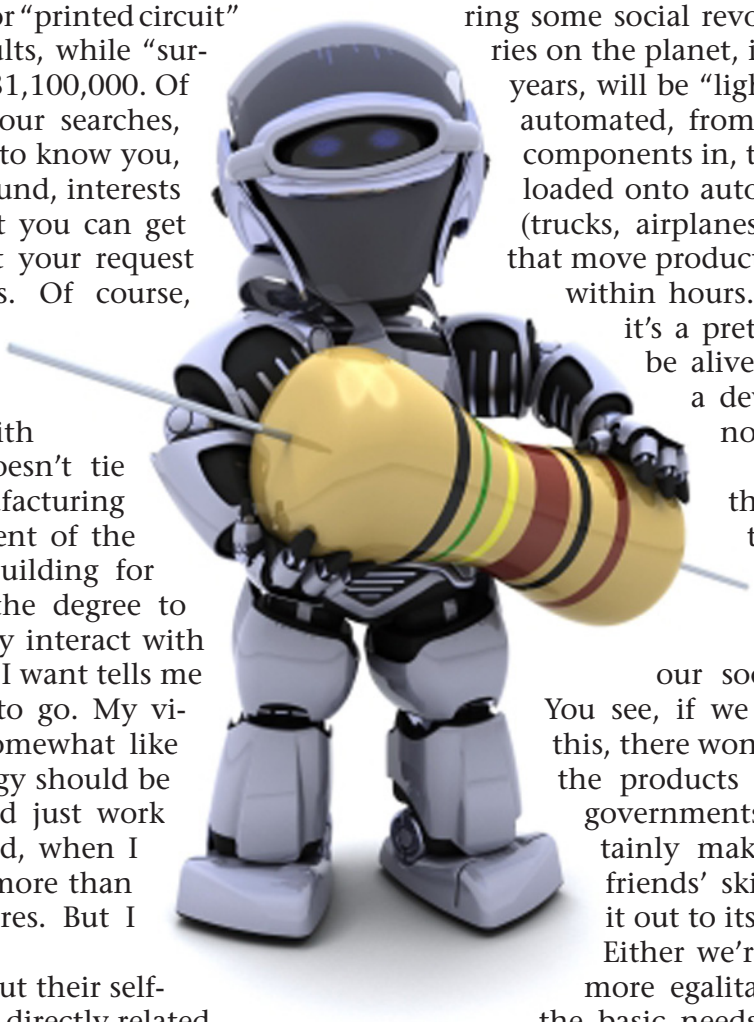
LET THEM EAT CAKE *continues*

Spock reminds us, "The needs of the many outweigh the needs of the few."

Looking a bit more at where automation is headed, what really got me thinking was that interview with Larry Page on Charlie Rose's show on PBS (U.S. public television) recently, in which Page said there is still so much to do on search, so much so, that he believes they're only about 1% of the way there. Get out! Right off the top, I didn't get it. Search is everywhere these days. I use it multiple times a day, checking news, doing research, getting a map, looking for a five-day weather forecast, etc. His point is that they still don't know what you (the consumer) want clearly enough, which is why today, when you post up a search query, you get millions of results (which I used to think was so awesome!). So many results are available that the information is almost useless.

I've been thinking the same thing for the last few years: A search for "printed circuit" gave me 3,770,000 results, while "surface mount" delivered 31,100,000. Of course, we can refine our searches, but Page wants Google to know you, including your background, interests and personality so that you can get a dozen results that fit your request perfectly, not millions. Of course, this raises all kinds of privacy issues, but that aside, you can see where we're going with this. Although this doesn't tie into robots and manufacturing directly, it's a component of the kind of world we're building for ourselves. Personally, the degree to which I have to directly interact with technology to get what I want tells me how far we still have to go. My vision for technology, somewhat like Page's, is that technology should be invisible. Things should just work and deliver what I need, when I want it, with nothing more than a few queries or gestures. But I digress.



Page also talked about their self-driving car. Now, this is directly related to us and our industry. This technology has huge implications, I believe. The company recently released a video on YouTube (of course), of their car driving a blind person around town to do a few errands and even pick up a few tacos at the Taco Bell drive-through. As Page points out, this isn't a futuristic technology. It's here, now. Check out the video here.

To tie at least some of this together, if we already have self-driving cars and sophisticated learning computers, we can certainly have autonomous factories, which will adjust to ever-changing product requirements and workflows, etc. In fact, this is very close. As reported widely by the press, we'll see millions of robots in Foxconn factories doing repetitive tasks all day long in the next few years, as promised by Terry Gou. But soon the automated systems, the robots, will become quite flexible, constantly adjusting to workflow and product variations. Barring some social revolution, most factories on the planet, in the next 20 to 50 years, will be "lights out" and totally automated, from raw materials and components in, to final product out, loaded onto autonomous transports (trucks, airplanes, trains and ships) that move products around the world within hours. On the one hand, it's a pretty exciting time to be alive if you're living in a developed country. If not, I'm not so sure.

In thinking this through a bit it seems to be a losing proposition unless we're willing to rethink the way our society is structured. You see, if we get really good at this, there won't be anyone to buy the products being built except governments, which will certainly make my conservative friends' skin crawl. But think it out to its logical conclusion. Either we're moving toward a more egalitarian society where the basic needs of all are met by

LET THEM EAT CAKE *continues*

governments, which will likely have greater control over much of the products and services offered, or we'll suffer a fate similar to that of the great societies of the past as our social systems become unglued with billions of people at the bottom of the heap, literally fighting to get their piece of the pie. Unless we take care of those who have little, we'll suffer a fate similar to that of those societies that didn't pay enough attention to the welfare of the masses. I guess if they're hungry, we could "let them eat cake."

I did a Google search on "The Fall of Rome" and came up with this from About.com:

There are adherents to single factors, but more people think a combination of such factors as Christianity, decadence, lead, monetary trouble, and military problems caused the Fall of Rome. Imperial incompetence and chance could be added to the list. Even the rise of Islam is proposed as the reason for Rome's fall, by some who think the Fall of Rome happened at Constantinople in A.D. 1453.

We have some interesting parallels with the comments above, don't you think? Religion is still divisive. Decadence is running rampant. Monetary trouble is everywhere; the military industrial complex continues to expand around the world and there is plenty of incompetence. Islam is also very much in the news these days. We certainly have a problem with lead (or lack thereof). Interesting.

Here's another article, this one from Reuters, titled, "Robots lift China's factories to new heights." It'll give you a better understanding of the drivers pushing automation forward.

I do think we'll reach a point very soon where consumers will begin to demand that products have a certain amount of "human-made" content. It won't be "made in America" so much, but "made by humans" that will become the new mantra. We need more jobs, not fewer, in this world. From a human perspective, for about half of the planet, automation seems to be taking us in the wrong direction. For the other half the benefits are quite attractive. We just have to figure out how to close the gap without coming unglued in the process. **SMT**

Ray Rasmussen is the publisher and chief editor for I-Connect007 publications. He has worked in the industry since 1978 and is the former publisher and chief editor of CircuiTree Magazine. Contact Rasmussen here.

SMT PERSPECTIVES AND PROSPECTS

100 Points on Lead-Free Performance and Reliability, Part 2

by Dr. Jennie S. Hwang, *CEO*
H-TECHNOLOGIES GROUP

Summary: In this month's column, the final of a two-part series, Dr. Hwang takes a wide, sweeping look at the history, timeline, highlights, and future projections for lead-free manufacturing.

Continuing last month's list, this column wraps up the points on lead-free properties, performance, and reliability, retrospectively and prospectively. Each of the summary points will not be discussed or elaborated. However, inquiries about any of the points for scientific base, rationale, and further discussion are welcome.

51. The SAC system has been successful in serving the intended function for most applications, but not all.

52. The SAC system encompasses compositions including: SAC405, SAC305 and in-between of 3 to 4% Ag and of 0.5 to 1.5% Cu; low-Ag content of SAC system; and all doped SAC compositions.

53. Low-Ag compositions denote the SACs containing less than 3% Ag, such as SAC105, SAC0803, etc.

54. Doped SAC compositions, in a practical sense, denote those incorporated with a non-alloying element(s) in a small dosage.

55. SnCu system has been successful in serving the intended function in wave soldering for some applications.

56. SnCu system denotes compositions of SnCu in various percentage of Cu, as well as the doped SnCu compositions.

57. Doped SnCu compositions denote those SnCu compositions incorporated with a non-alloying element(s) in a small dosage.

58. Effects of higher process temperature imposed by SAC solders should be considered in the areas of PCB bare board, components, flux chemistry, solder joints (including voids), and PCB surface finish, separately and collectively.

59. Higher process temperature contributes to PCB de-lamination, blistering, warp, PCB discoloration, large PCB sagging during reflow, Cu pad peel strength reduction, and pad-lifting.

60. Higher process temperature contributes to PCB through-hole barrel crack, Cu dissolution, PCB Z-axis thermal expansion (weakened through-hole via).

61. Higher process temperature could cause PCB intrinsic interconnect open, electroless Cu separates from the post, electrolytic Cu separates from electroless Cu, and electroless Cu cohesive failure.

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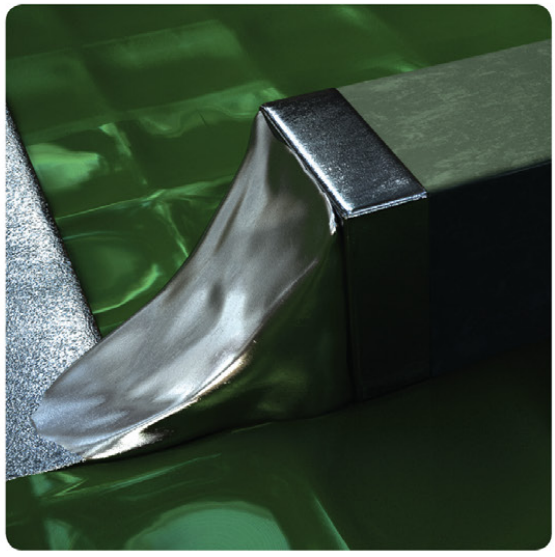

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100 POINTS ON LEAD-FREE PERFORMANCE AND RELIABILITY, PART 2 *continues*

62. Effects of higher process temperature on PCB surface finish (solderability and intermetallic compounds) should be considered.

63. Pad cratering was hardly observed in SnPb soldering.

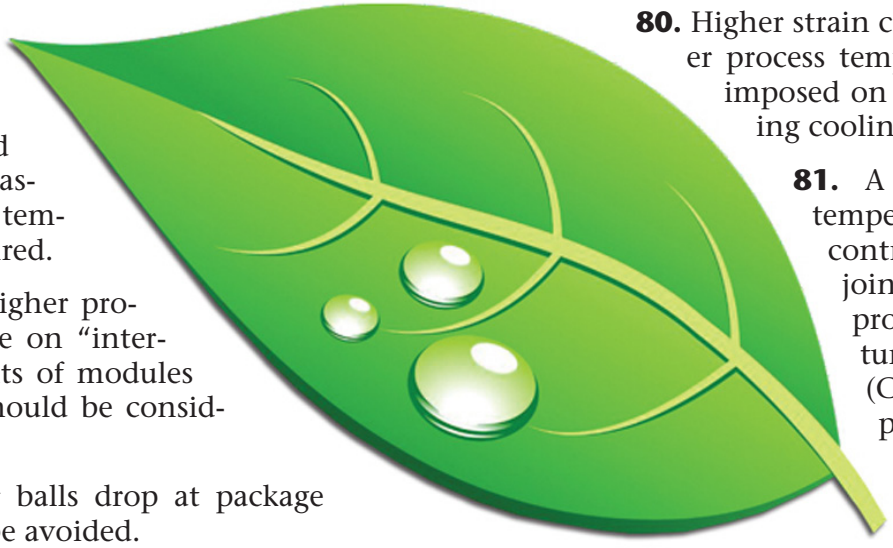
64. Pad cratering and pad lifting should be differentiated. They have different phenomena and causations.

65. Effects of higher process temperature on the probability of electro-migration issue should be taken into consideration.

66. A higher process temperature may adversely affect aluminum electrolytic capacitors.

67. Defects or damages of MLCC should be avoided.

68. Heat-sensitive components should be protected when a high assembly process temperature is required.



69. Effects of higher process temperature on "internal" solder joints of modules or subsystem should be considered.

70. BGA solder balls drop at package interface must be avoided.

71. A higher process temperature may induce BGA/CSP delamination between the layers of interposer beneath the die.

72. Effects of higher process temperature on connector plastic housing changes (dimensional, functional) should be considered.

73. A higher process temperature may increase Z-axis thermal expansion, which, in turn, may induce undue effects on components during cooling (compressive stress).

74. Higher process temperatures exert adverse effects on component co-planarity (BGA).

75. Higher process temperatures on component moisture sensitivity should not be ignored. At a higher process temperature, components may have to be dried to a lower moisture content to avoid package crack.

76. Effects of higher process temperature on flux chemistry (user) should not be underestimated.

77. Higher process temperature impacts on flux formulation (supplier).

78. For cleaning, higher process temperature affects the ability to clean flux residue.

79. A higher process temperature may contribute to potential electrochemical failure (flux contaminants adsorbed onto or absorbed into the substrate).

80. Higher strain created by a higher process temperature may be imposed on solder joint during cooling.

81. A higher process temperature may contribute to solder joint voids. A higher process temperature can promote $(CuNi)_6Sn_5$ compound at the bonding interface, resulting in additional voids.

82. Head-on-pillow open joint was hardly observed in SnPb soldering.

83. Head-on-pillow occurs with SAC system.

84. Higher process temperature causes more oxidation on solder pads after the first reflow, which particularly affects OSP surface finish.

85. Higher process temperature increases the propensity to tin whisker phenomenon when a metal coating used (such as Sn or SnCu or SnAgCu) is prone to tin whisker.

86. Higher process temperature aggravates black pad problem.

100 POINTS ON LEAD-FREE PERFORMANCE AND RELIABILITY, PART 2 *continues*

87. Higher process temperature may incur wave soldering disadvantages (dross, equipment).

88. Higher process temperature affects the reflow oven (working life, residue accumulation).

89. Higher process temperature increases residual stress.

90. Higher process temperature increases energy cost.

91. Higher process temperature imposes higher demands on rework-ability.

92. Using a marginal process temperature will result in production defects and or potential reliability mishaps.

93. Lower process temperature has to come from the lower melting temperature solder alloy.

94. A lower melting temperature solder alloy needs to resort to a quaternary system. Under the constraints of all practical factors, a quaternary system incurs higher raw material cost per unit weight.

95. Cost is part of the equation. The cost of ownership is the bottom line.

96. It is vitally important to recognize that quaternary system denoted herein is separate and distinct from a doped system.

97. For die attach and package levels, a practical system having a higher melting temperature above 275°C is yet to be established.

98. Solder joint reliability cannot outperform an alloy's intrinsic properties and mechanical behavior (interactive creep and fatigue).

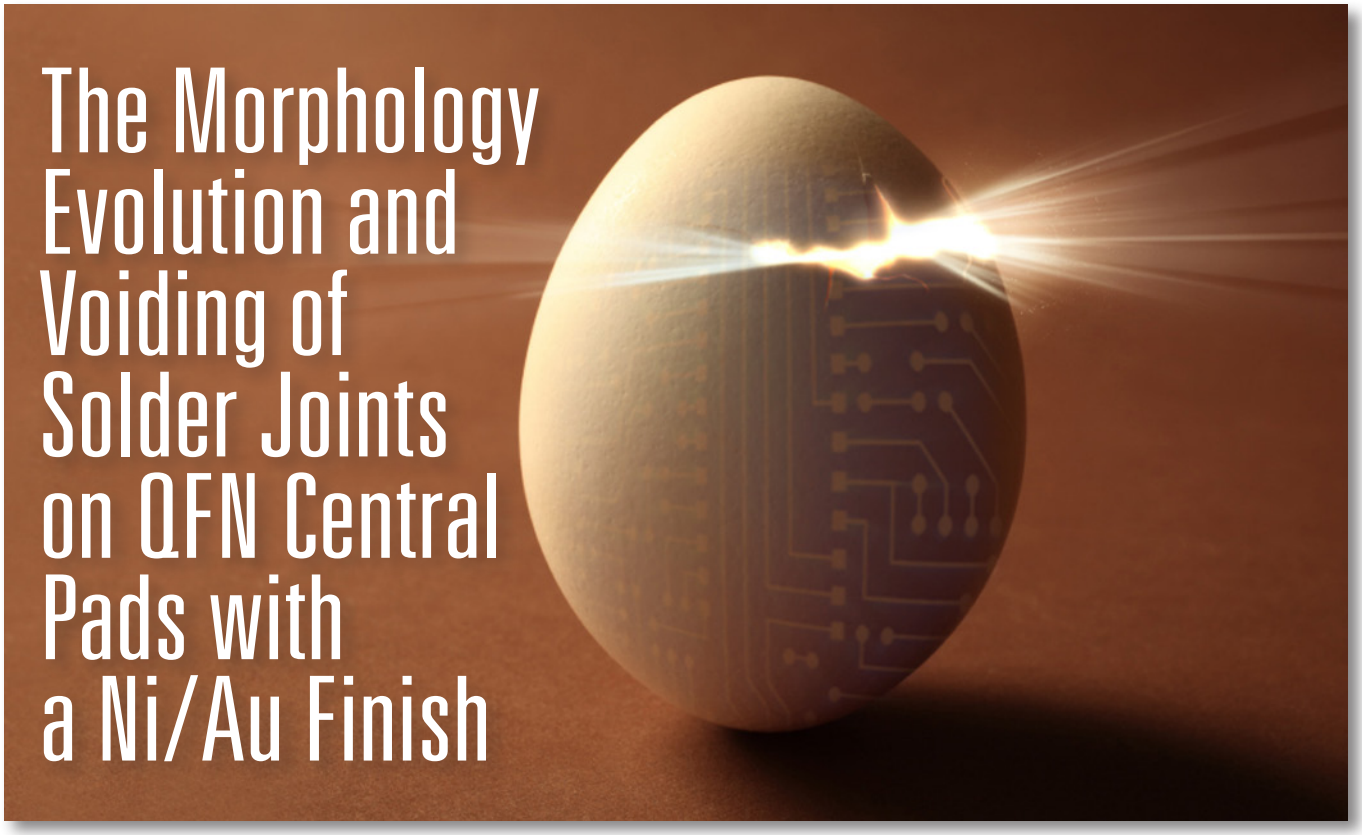
99. The development of the balanced performance was, and still is, a demanding task to deliver the performance and reliability equivalent to or better than 63Sn37Pb. It is a highly intricate use of metallurgy. Solder alloys and processes rather than SAC system need to be established to fit all applications that are currently (as of June, 2012) under RoHS exemptions.

100. Ultimate reliability calls for the establishment of a lower process temperature to ensure the integrity of PCBAs that are complex in structure and makeup and required to perform under versatile and/or harsh environments. **SMT**

Dr. Hwang will present two lectures on "Array Package Interconnection: Forward/ Backward Compatibility and Reliability" and "Preventing Production Defects and Failures" at SMTA International Conference on October 15, 2012, in Orlando, Florida.

Dr. Hwang, a pioneer and long-standing contributor to SMT manufacturing since its inception as well as to the lead-free development, has helped improve production yield and solved challenging reliability issues. Among her many awards and honors, she has been inducted into the WIT International Hall of Fame, elected to the National Academy of Engineering and named an R&D Stars to Watch. Having held senior executive positions with Lockheed Martin Corporation, Sherwin Williams Co., SCM Corporation and IEM Corporation, she is currently CEO of H-Technologies Group providing business, technology and manufacturing solutions. She is a member of the U.S. Commerce Department's Export Council, and serves on the board of Fortune 500 NYSE companies and civic and university boards. She is the author of 300+ publications and several textbooks and an international speaker and author on trade, business, education and social issues. Contact her at (216) 577-3284; e-mail JennieHwang@aol.com.

The Morphology Evolution and Voiding of Solder Joints on QFN Central Pads with a Ni/Au Finish



by Julie Silk, Jianbiao Pan, and Mike Powers
AGILENT TECHNOLOGIES

Summary: ***This paper, originally presented at IPC APEX EXPO 2012, reports on a comprehensive study regarding the morphology evolution and voiding of SnAgCu solder joints on the central pad of two different packages—QFN and an Agilent package called TOPS—on PCBs with a Ni/Au surface finish. Samples were isothermally aged and representative solder joints were cross-sectioned and analyzed using SEM and EDX spectroscopy to investigate the evolution of the solder joint morphology as a function of Au content and isothermal aging.***

Editor's Note: This paper was originally presented at IPC APEX EXPO 2012.

Introduction

The quad flat no-lead (QFN) package is increasingly popular due to its small size, easy trace routing, and good thermal and electrical performance [1]. It has a large central underbelly pad, which dissipates heat from the die inside the package through a solder connection to the printed circuit board (PCB). The short standoff distance between the QFN package and the PCB also reduces inductance thus providing excellent electrical performance. An Agilent package called TOPS has features similar to a QFN, being leadless with a large underbelly pad.

Although the QFN package and the TOPS packages offer a number of benefits, to the authors' knowledge, the evolution of morphology of the solder joint on the central underbelly pad has not been reported. In this paper, the authors report on a comprehensive study regarding the effect of Au content on the morphology of SnAgCu solder joints on the underbelly pad, assembled on PCBs with a Ni/Au surface finish. Samples were isothermally aged at the equivalent of 0, 2, 7, and 14 years' service life. Representative solder joints were cross-sectioned and analyzed using scanning electron microscopy (SEM) and energy dispersive X-ray spectroscopy (EDX) to investigate the evolution of the solder joint morphology as a function of Au content and isothermal aging.

Another issue with these leadless packages with a large underbelly pad is that excessive voiding often occurs in the solder joint on the underbelly pad. If the void area is large, thermal performance will be reduced. There are a few application notes that provide guidelines for pad pattern design, stencil design, reflow profile, and others [2-6]. To the authors' knowledge, no paper has been published on the effect of Au content on the voiding. In this paper, the effect of Au content on voiding in the underbelly solder joint is reported.

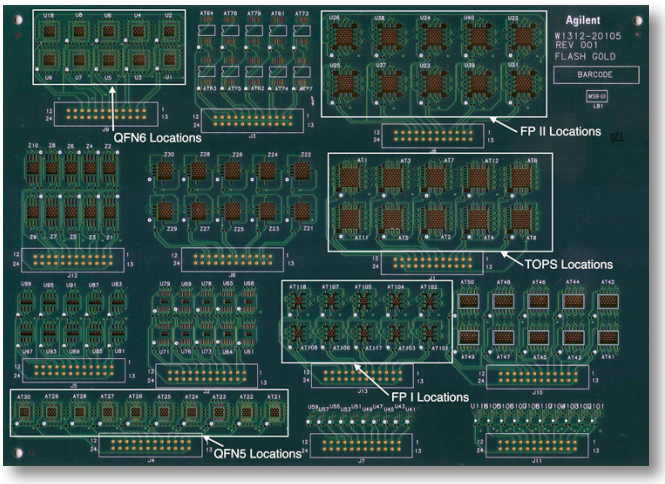


Figure 1: Test vehicle.

Experiment

Component, Test Vehicle, and Assembly Process

The test vehicle is shown in Figure 1. The board finish is electrolytic Au over Ni. There are two different Au thicknesses: A flash Au finish with 0.08 ~ 0.38 µm Au over 5 µm Ni and a thick Au finish with 2 ~ 2.54 µm Au over 5 µm Ni. Two types of leadless packages, QFNs and TOPS, were assembled on the test vehicle. Figure 2 shows these packages. The QFNs were two different sizes: QFN5 is 5 mm x 5 mm and QFN6 is 6 mm x 6 mm. The size of the TOPS package is 10 mm x 10 mm. The pad finish on the QFN5 and QFN6 is matte Sn over Cu and that on the TOPS is electrolytic Au over Ni.

The assembly process was done using a standard surface mount assembly line in a realistic production environment. The solder paste used is Sn3.0Ag0.5Cu (SAC305) Type 3 with no-clean flux and metal content of 88% by weight. The stencil used is electroformed nickel, laser cut with a foil thickness of 0.1 mm (4 mils). The solder paste coverage of the central pad for QFN5 and QFN6 is 43% and that for TOPS is 56%. Since the volume of solder paste on the central pad was not measured, the nominal solder paste volume is calculated based on the stencil aperture size and the coverage. The calculated nominal Au content of solder joint on the central pad for QFN5, QFN6, and TOPS package is shown in Table 1. For details about the reflow profile and Au content calculation, please refer to papers published by the authors [7-9].

The assembled PCBs were randomly divided into three groups. The boards in Group 1 were not subjected to thermal aging. The boards in Group 2 were subjected to isothermal aging at 125°C for 30 days. The boards in Group 3 were subjected to isothermal aging at 125°C for 56 days. The three thermal aging times represent 0, 7.8, and 14.6 years of service when the device is operated at 60°C. Activation energy of 0.8 eV

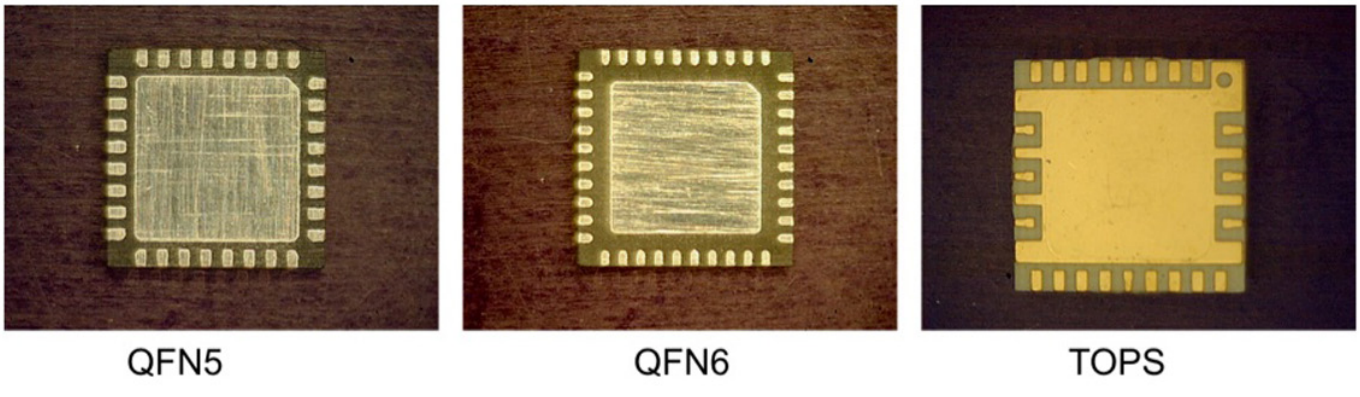


Figure 2: Packaged QFN components.

	Flash Au	Thick Au
QFN5 or QFN6	1.2%	10.9%
TOPS	4.1%	11.2%

Table 1: Nominal Au content in weight percentage in solder joints on central pad.

was used. One flash Au board and one thick Au board from each group were randomly selected for cross-sectioning and SEM/EDX analysis. An additional thick Au board was aged at 125°C for 209 hours, or 2.25 years of service when the device is operated at 60°C. Aging at 125°C for 209 hours is equivalent to 1,000 hours at 100°C. The SEM used in this study was a JEOL JSM-6390 equipped with a Thermo Scientific 6733A EDX.

Results and Discussion

Evolution of Solder Joint Morphology

The evolution of the microstructure for both QFN and TOPS solder joints on the underbelly central pad was evaluated. The substrate finish on the QFN package does not have a Ni diffusion barrier and the TOPS package includes a Ni barrier layer in the substrate finish. In both part types, the solder joint microstructure is compared as a function of isothermal aging times and relative Au content in the solder joints.

QFN and TOPS on Flash Au Board

The SEM micrograph of two as-built solder joints between the central pad of a component and a board with a flash Au finish is shown in Figure 3. The Au content in the QFN solder joint is about 1.2% by weight and the Au content in the TOPS solder joint is about 4.1%. The interfacial intermetallic compound (IMC) on the component side of the QFN solder joint is Cu_6Sn_5 while that of the TOPS solder joint is $(Ni, Cu, Au)_3Sn_4$. This is because the finish of the QFN package does not have a Ni diffusion barrier layer and allows Cu to diffuse into the joint. The TOPS package has a Ni layer. The interfacial IMC on the board side of the QFN joint is $(Ni, Cu, Au)_3Sn_4$ or $(Cu, Ni, Au)_6Sn_5$ while there are two different IMC layers that can be seen in the board side of the TOPS joint: $(Au, Ni)Sn_4$ over $(Ni, Au)_3Sn_4$ layer. The IMC in the bulk solder of the QFN joint is pebble-like $(Cu, Au)_6Sn_5$ while that of the TOPS joint is needle-like $AuSn_4$.

Figure 4 shows the SEM micrograph of two aged solder joints between the central pad of a component and a board with a flash Au finish. The joints were aged at 125°C for 30 days. For the QFN joint, there is no significant difference in the IMCs and microstructures between the aged sample and the as-built sample except that $(Cu, Au)_6Sn_5$ in the bulk solder coalesces to larger sizes. The driving force for this coarsening behavior is the energy reduction associated with a lower surface area to volume ratio. In the TOPS joints, needle-like $AuSn_4$ IMCs in the bulk solder of the as-built sample changed to stone-like $AuSn_4$ IMCs after aging. Some $AuSn_4$ IMCs in the bulk solder migrated with aging to form

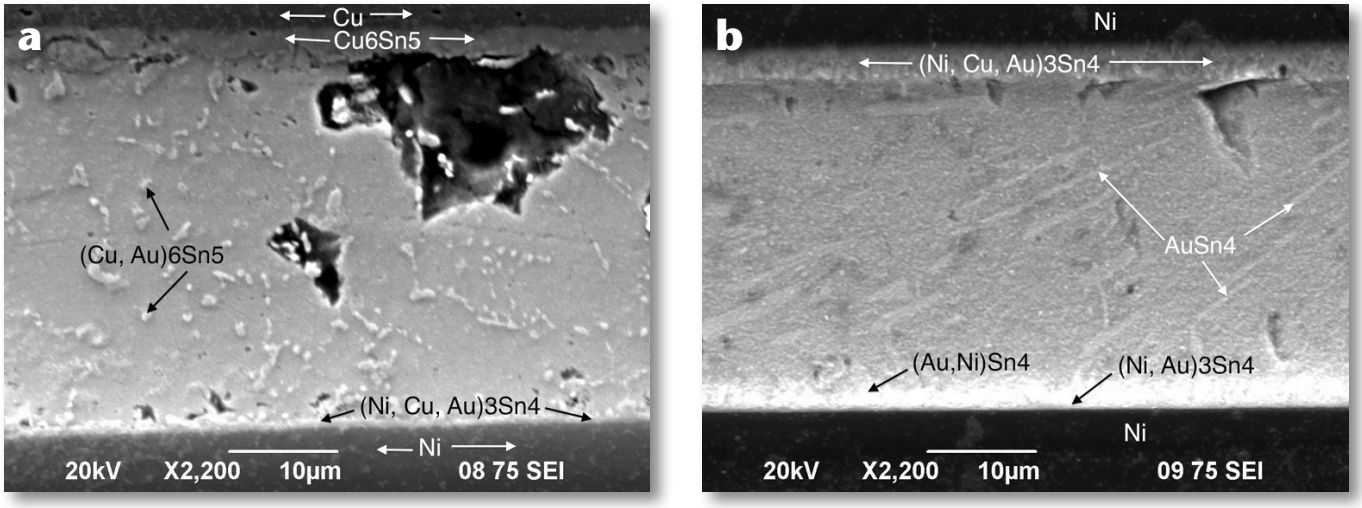


Figure 3: SEM micrograph of an as-built solder joint between the central pad and a board with flash Au finish. a) QFN. b) TOPS.

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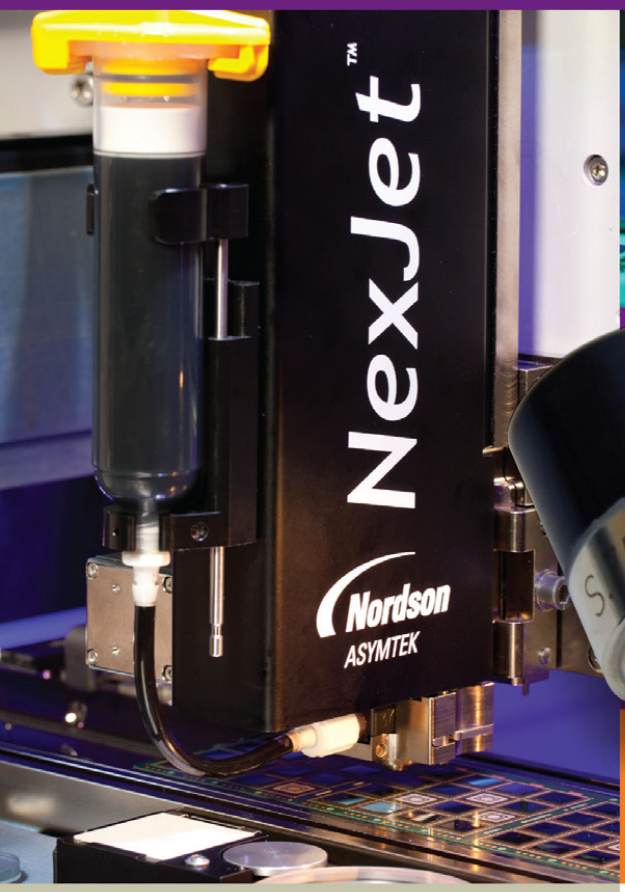

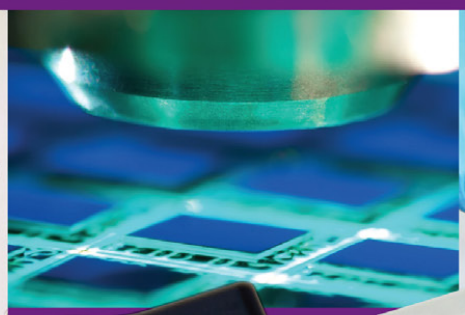

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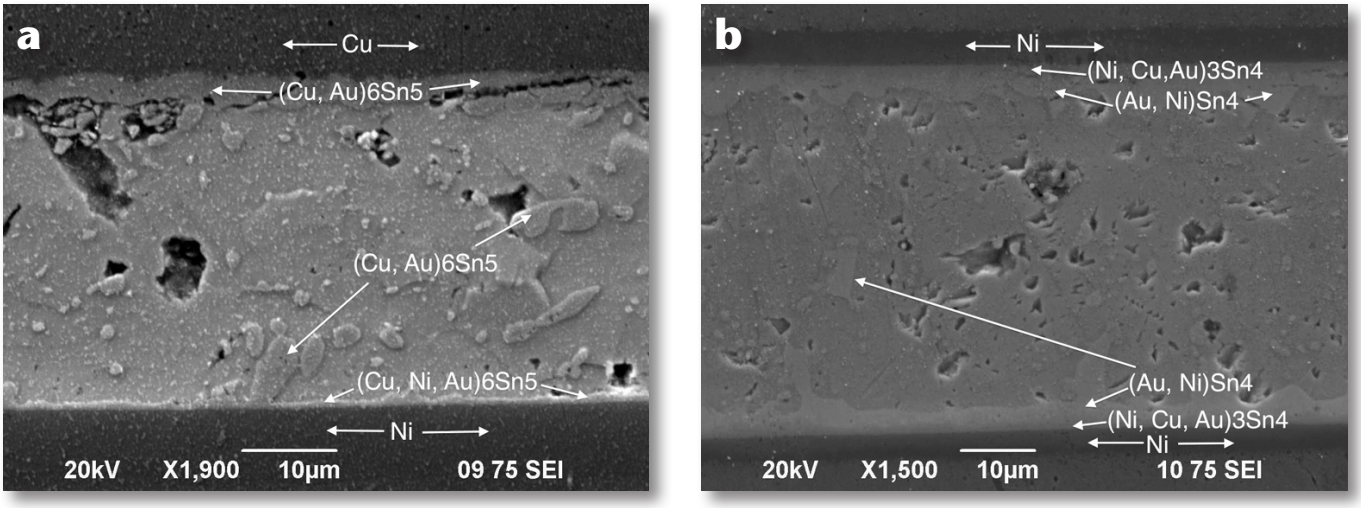

Figure 4: SEM micrograph of an aged solder joint between the central pad and a board with flash Au finish. The sample was aged at 125°C for 30 days. a) QFN. b) TOPS.

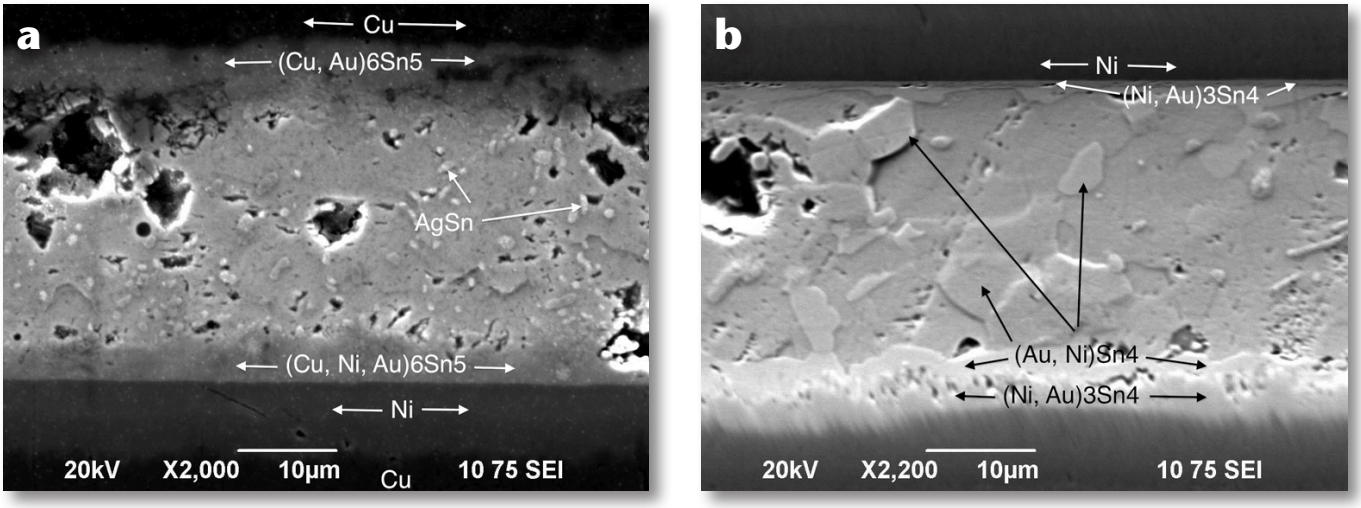

Figure 5: SEM micrograph of an aged solder joint between the central pad and a board with flash Au finish. The sample was aged at 125°C for 56 days. a) QFN. b) TOPS.

a continuous (Au, Ni)Sn_4 layer next to the (Ni, Cu, Au)$_3Sn_4$ IMC at the interface. In the QFN joints, there is not a continuous layer of detrimental (Au, Ni)Sn_4 IMC in the interface on the flash Au board.

After aging at 125°C for 56 days, one QFN solder joint and one TOPS joint on a flash Au board are shown in the SEM micrographs in Figure 5. The IMCs and microstructures are similar to that of samples aged for 30 days. However, the interfacial IMC thickness increased.

QFN and TOPS on Thick Au Board

The SEM micrograph of two as-built solder joints between the central pad of a component and a board with a thick Au finish is shown in Figure 6. The Au content in the QFN solder joint is about 10.9% by weight and the Au content in the TOPS solder joint is about 11.2%. The interfacial intermetallic compound (IMC) on the component side of the QFN solder joint is (Cu, Ni, Au)$_6Sn_5$ while that of the TOPS solder joint is (Ni, Cu, Au)$_3Sn_4$. The IMC in the bulk solder of the QFN joint is pillar-like and/or stone-like $AuSn_4$, same as that of the TOPS joint.

Figures 7 and 8 show the SEM micrographs of solder joints on thick Au boards after aging at 125°C for 30 days and 56 days, respectively. It is interesting to note that the interfacial

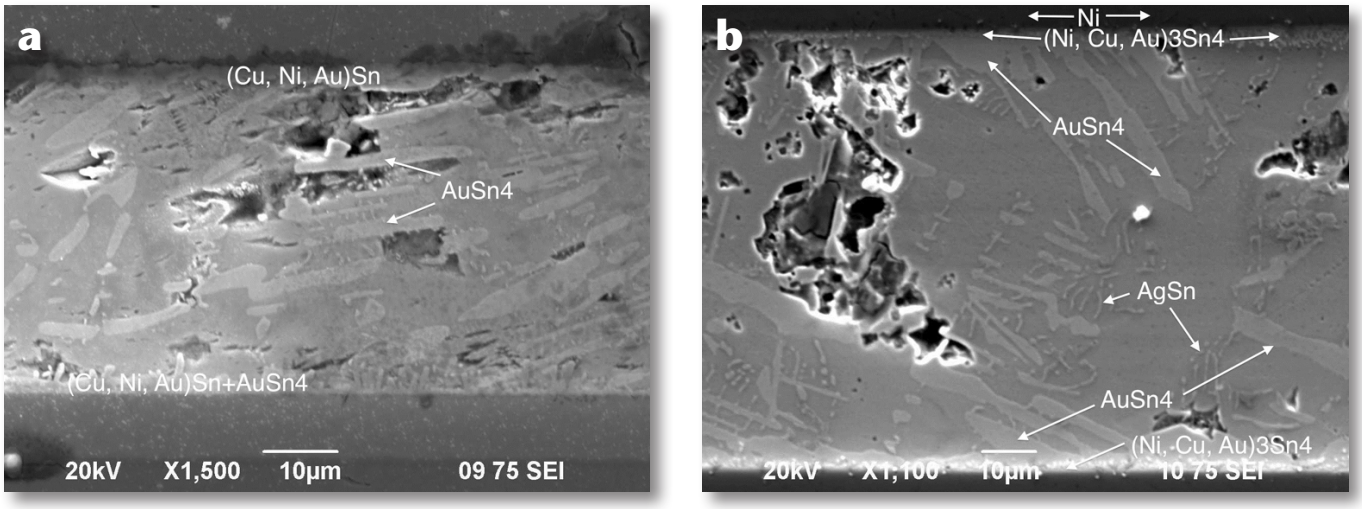

Figure 6: SEM micrograph of an as-built solder joint between the central pad and a board with thick Au finish. a) QFN. b) TOPS.

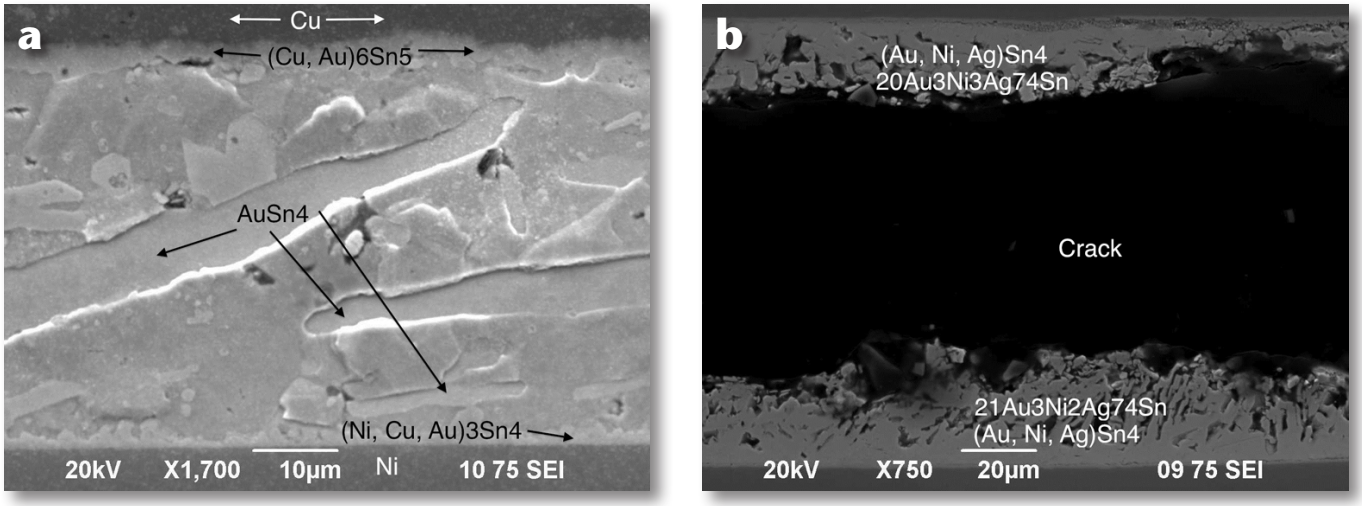

Figure 7: SEM micrograph of an aged solder joint between the central pad and a board with thick Au finish. The sample was aged at 125°C for 30 days. a) QFN. b) TOPS.

IMC of the TOPS joint on the board side is a continuous (Au, Ni)Sn_4 layer next to the (Ni, Cu, Au)$_3Sn_4$ IMC while there is no continuous layer of (Au, Ni)Sn_4 at the QFN joint. The result is significant. It is the effect of Cu on $AuSn_4$ IMC migration. When copper is available, as with the QFN, the $AuSn_4$ IMCs did not form a continuous interfacial layer. The driving force for the migration of $AuSn_4$ is a reduction of Gibbs-free energy by mixing, consequently establishing an $AuSn_4$ equilibrium between the bulk and the interface. With the fast diffusion of Cu into the IMC, there is less drive to absorb Ni and thus less migration to the Ni interface.

It was also noticed that there are large fractures in the solder joint between the central pad of a TOPS and a thick Au board as shown in Figure 9. Such fractures did not occur in solder joints between a TOPS and a flash Au board. Such fractures also did not occur on solder joints between a QFN and a thick Au board. This indicates that high Au content (over 10 wt% Au) has a more severe effect on the reliability of solder joints without Cu (Ni layer on both sides of the joint) than those with the availability of Cu. When copper is available, $AuSn_4$ IMCs are less likely to migrate to the interface and form a continuous IMC layer, thus improving the reliability.

THE MORPHOLOGY EVOLUTION AND VOIDING OF SOLDER JOINTS *continues*

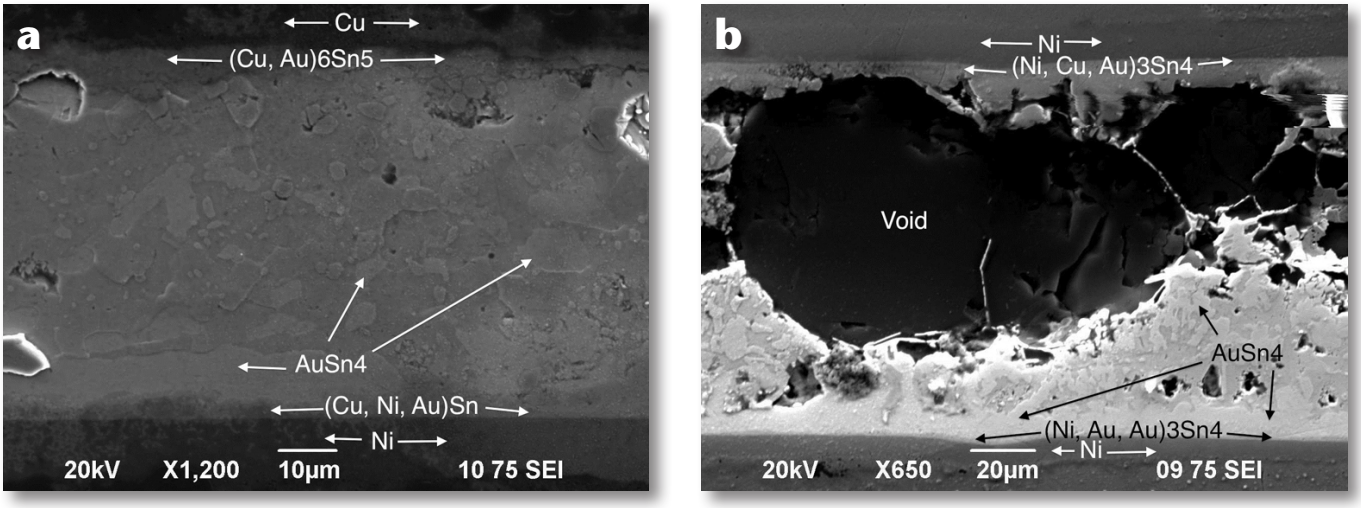

Figure 8: SEM micrograph of an aged solder joint between the central pad and a board with thick Au finish. The sample was aged at 125°C for 56 days. a) QFN. b) TOPS.

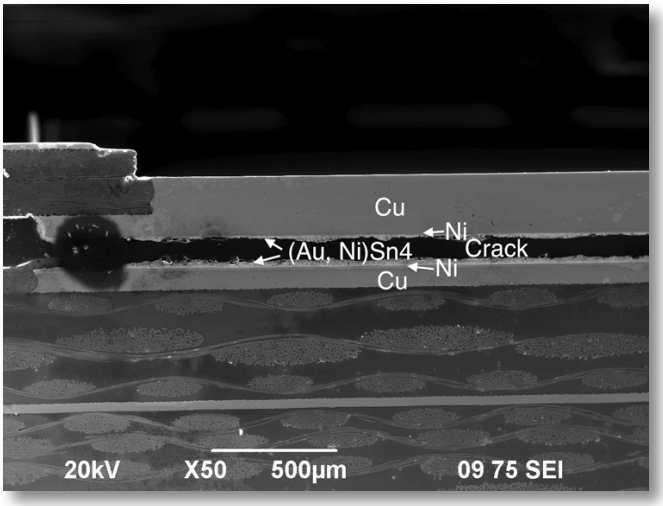

Figure 9: SEM image of the solder joint between the central pad of TOPS component and a thick Au board.

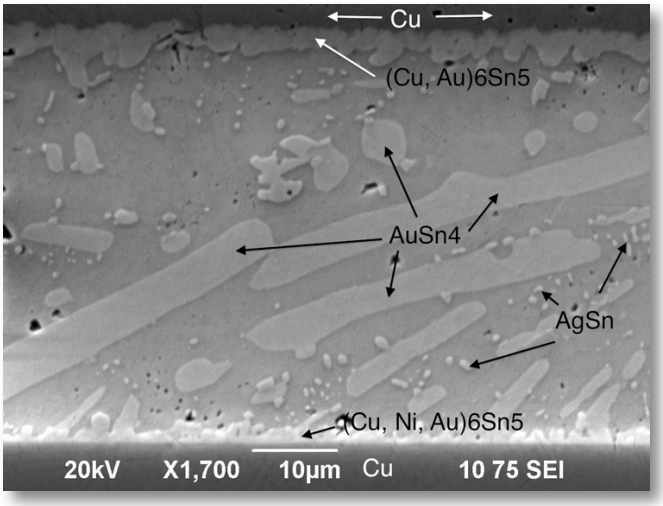

Figure 10: SEM micrograph of an aged solder joint between the central pad of a QFN and a board with thick Au finish. The sample was aged at 125°C for 209 hours.

Thermal Aging Time

It is useful to know how long is long enough for thermal aging. In this study, the authors compared the microstructure and IMC thickness of solder joints aged at 125°C for 209 hours versus 30 days and 56 days.

Figure 10 shows the SEM micrograph of a solder joint between the central pad of a QFN and a thick Au board aged at 125°C for 209 hours. Comparing with the SEM image of as-built solder joint in Figure 6 a) and the SEM image of aged solder joint in Figure 7 a), it seems the coalescence process of the $AuSn_4$ IMCs in the bulk solder has completed after aging for 209 hours. There is no significant difference in microstructure between the solder joint aged for 209 hours and the joint aged for 30 days, except that the IMC layer is thicker in the sample aged for 30 days. Figure 11 shows the SEM images of a solder joint between a perimeter lead of a TOPS and a thick board aged at 125°C for 209 hours, compared with solder joints as-built, aged for 30 days, and aged for 56 days. The same conclusion can be drawn that there is no significant difference in microstructure of the bulk solder joint between the solder joint aged for

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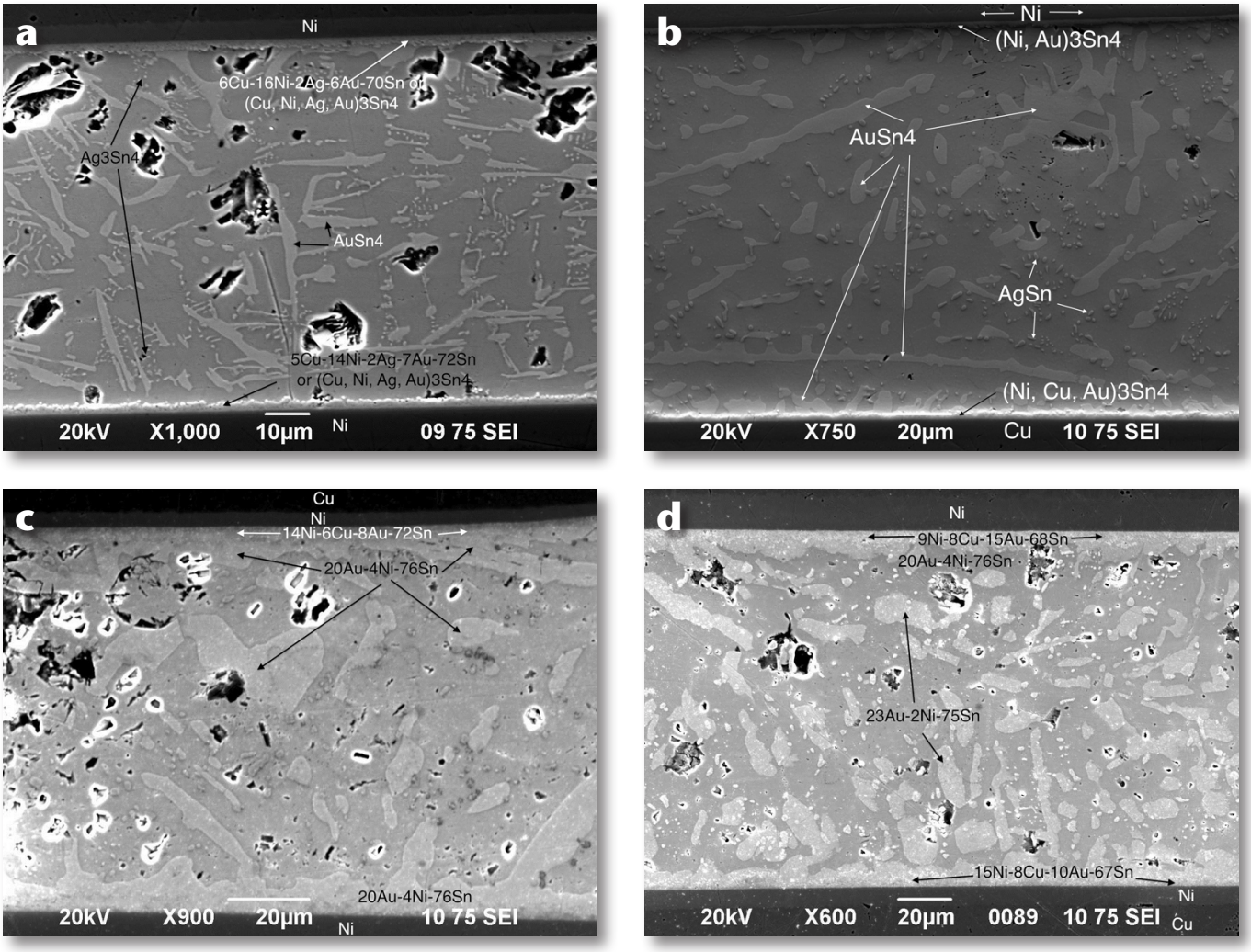

Figure 11: SEM images of solder joints of a TOPS component on a thick Au board. a) As-built. b) Aged at 125°C for 209 hours. c) Aged at 125°C for 30 days. d) Aged at 125°C for 56 days.

209 hours and the joint aged for 30 days or 56 days. However, at the interface, the migration of $AuSn_4$ to a continuous layer has not yet occurred. This indicates that the two-year equivalent aging time appears to not be sufficient to see significant migration of the $AuSn_4$ IMC.

Figures 12 and 13 show the changes in mean IMC thickness (four measurements per group) at the component and board interfaces, respectively, as a function of thermal aging time and board finish (thick versus flash Au) for the QFN platform. For the case of QFN, the IMC thickness and composition at the component and board interfaces can evolve independently, due to the difference in the surface finish stack-up. The evolution of IMC thickness as a function of thermal aging and board finish for the TOPS platform is shown in Figure 14, where the IMC thickness at both interfaces is included in the calculation of the mean thickness (four measurements per group) because composition at the two interfaces is essentially the same for the TOPS platform, owing to the presence of a Ni diffusion barrier at both interfaces. For both platforms, the mean IMC thickness increases with thermal aging time and increases at about the same rate.

However, it is interesting to note that for the QFN packages the increase in IMC thickness is higher on the flash Au boards, whereas for the TOPS packages the mean IMC thickness increase is higher for the thick Au boards. Since Cu is readily available in the QFN solder joints, migration of $AuSn_4$ type IMCs from the bulk

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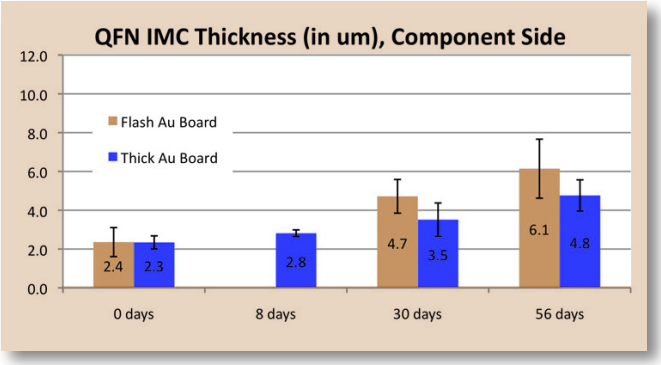

Figure 12: IMC thickness for QFN on flash and thick Au boards, component side of interface (error bars are ±1σ).

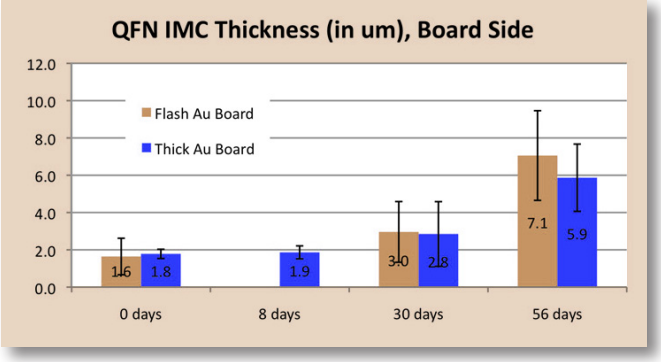

Figure 13: IMC thickness for QFN on flash and thick Au boards, board side of interface (error bars are ±1σ).

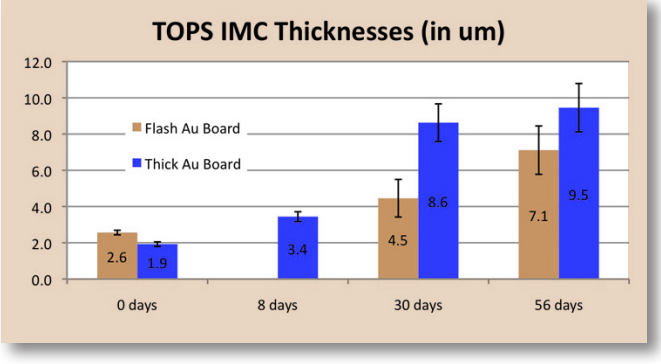

Figure 14: IMC thickness for TOPS on flash and thick Au boards (error bars are ±1σ).

to the interfaces during thermal aging is mitigated (i.e., $AuSn_4$ does not contribute to the increase in IMC thickness) and the IMC growth is dominated by formation of the $(Cu, Ni, Au)_6Sn_5$ IMC. In contrast, the presence of a Ni diffusion barrier at both interfaces for the case of the TOPS packages results in migration of (Au, Ni) Sn_4 IMC from the bulk to the interfaces during thermal aging where it contributes to the overall IMC thickness. Since more Au is available in the case of the thick Au boards, it makes sense that the contribution to overall IMC thickness is enhanced.

Voiding in the Central Underbelly Pad Solder Joint

It is well known that excessive voiding often occurs on the solder joint on the underbelly pad. In this study, a 2D X-ray image was taken on every component on every board after assembly. Figure 15 shows two X-ray images. A total of 540 images were analyzed including nine QFN5, nine QFN6, and nine TOPS components on 10 flash Au boards and 10 thick Au boards.

The analysis was done using the software ImageJ [10]. By adjusting the contrast and setting a threshold, the software is able to determine all voiding area and calculate the total voiding area. The software also shows the area of each void in the image. Voiding is characterized using void percentage, which is defined as the ratio of all voiding areas to the central pad area.

Figure 16 shows the average void percentage of each component type on the flash Au board and the thick Au board. The number for QFN is an average of 120 components and the number for TOPS is an average of 60 components. It is clear that thick Au metallization on thermal pads leads to more voiding. It was also noticed that the majority of voids cover thermal vias in the center of the pad. Note that all thermal vias in the study are un-filled, which was an error in board fabrication. The intended design was to epoxy-fill and plate over these vias, or "vippo" (via in pad plated over).

The SEM image in Figure 17 shows that voids are due to solder loss resulting from solder flowing through thermal vias. Figure 18 shows that interfacial IMCs have been formed on the void area. This indicates that solder wetted the pad on the PCB and on the component, formed IMCs, then solder flowed through thermal vias and voids are created due to the solder loss.

The standoff distance of the solder joint

THE MORPHOLOGY EVOLUTION AND VOIDING OF SOLDER JOINTS *continues*

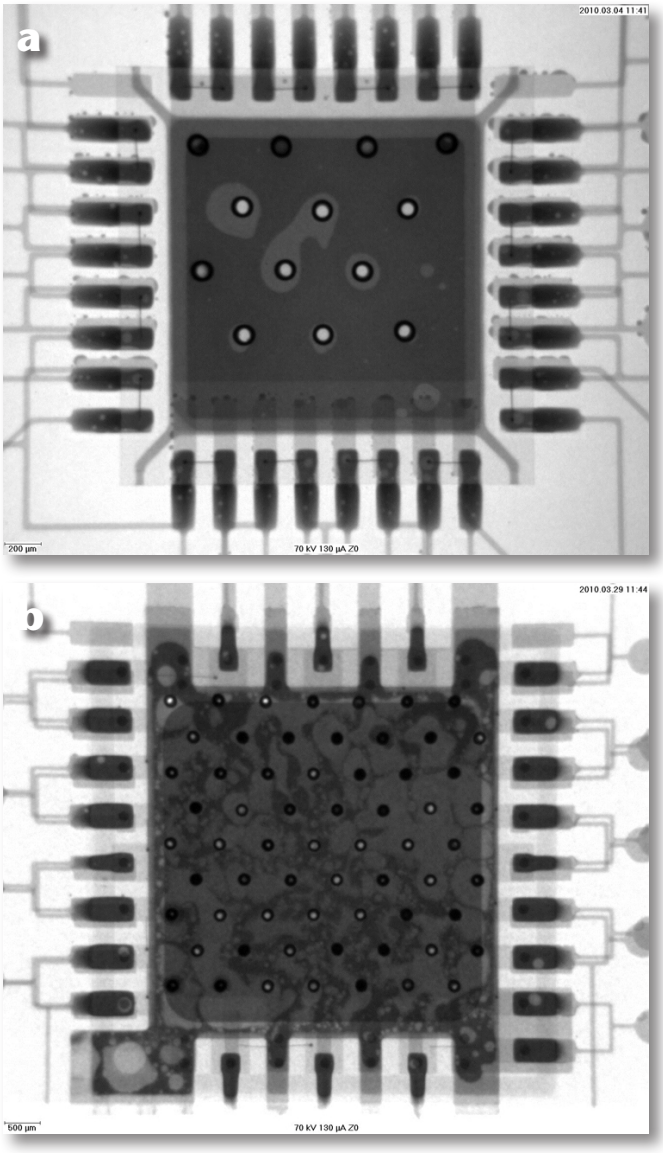

Figure 15: X-Ray images. a) A QFN component on a Flash Au board. b) A TOPS component on a thick Au board.

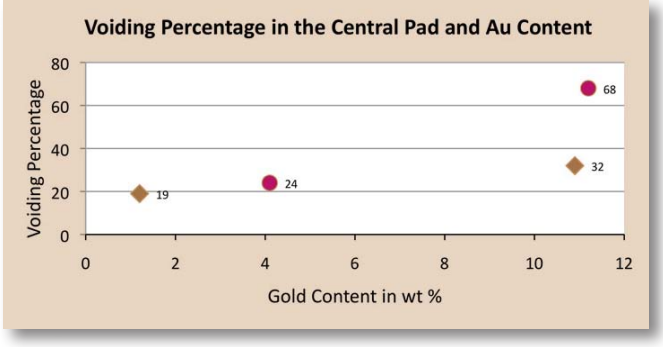

Figure 16: Graph of voiding percentage versus gold content (diamonds are QFN, circles are TOPS).

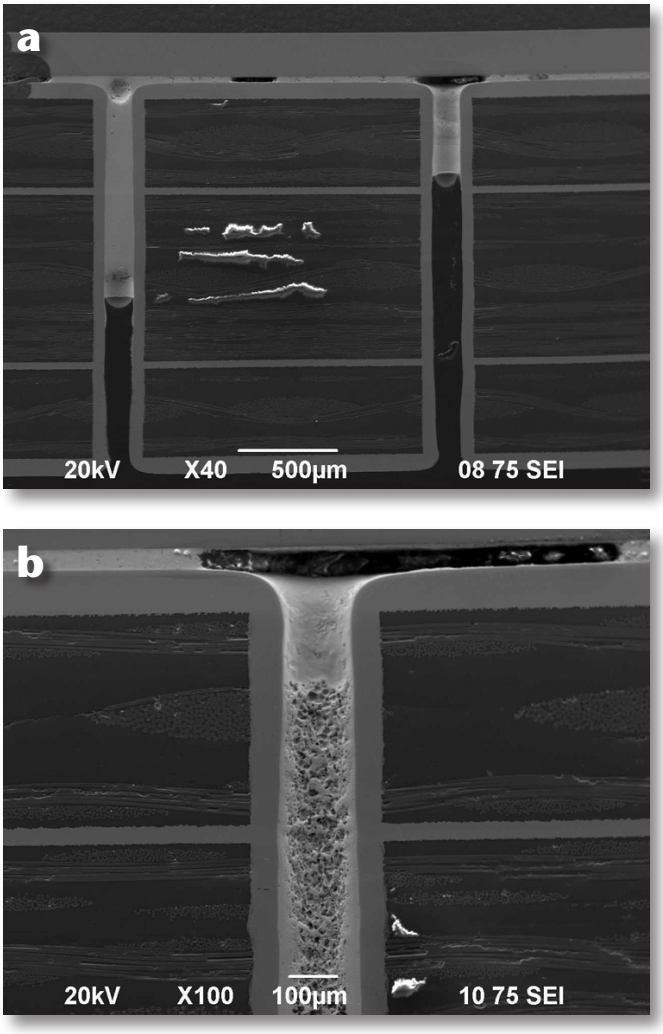

Figure 17: SEM images showing voids due to solder loss.

on the central pad was measured and reported in Table 2. Note that the stencil thickness is 100 µm (4 mils), and the solder paste coverage of the central pad for QFN5 and QFN6 is 43% and that for TOPS is 56%. If the standoff height of the solder joint were only determined by the solder paste coverage, the standoff would be 21.5 µm (or 43% of stencil thickness times 50% solder volume) for QFNs and 28 µm (or 56% of stencil thickness times 50% solder volume) for TOPS. The measured standoff is much larger than this even though there is solder loss to the thermal vias. The standoff was higher with more gold. The complete separation between the TOPS component and the thick Au board was due to high Au content

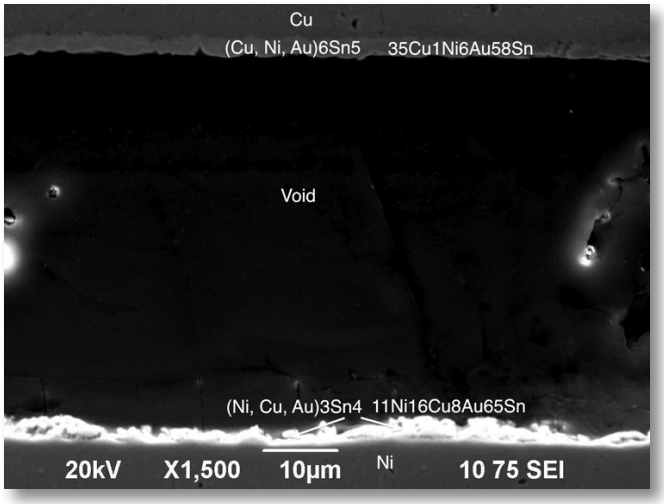

Figure 18: SEM image showing interfacial IMCs on the void of a QFN component on a flash Au board.

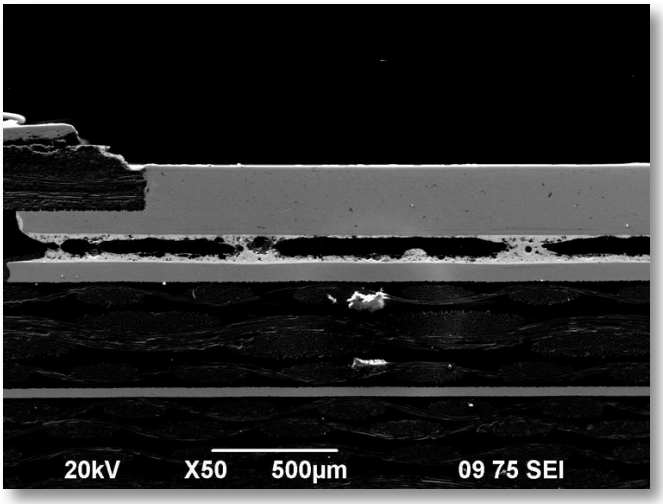

Figure 19: SEM image showing cracks/voids of a TOPS component on a thick Au board.

	Flash Au board	Thick Au board
QFN	35	51
TOPS	37	100

Table 2: Average solder standoff thickness (µm).

leading to $AuSn_4$ IMC across the whole joint as shown in Figure 19.

Conclusions

A comprehensive study has been conducted investigating the morphology evolution and voiding of SnAgCu solder joints on the central pad on PCB with a Ni/Au surface finish. The following conclusions can be drawn from this study:

- The significant result was the effect of Cu on $AuSn_4$ IMC migration. When copper is available, as with the QFN, the $AuSn_4$ IMCs did not form a continuous interfacial layer. The driving force for the migration of $AuSn_4$ is a reduction of Gibbs-free energy by mixing, consequently establishing an $AuSn_4$ equilibrium between the bulk and the interface. With the fast diffusion of Cu into the IMC, there is less drive to absorb Ni and thus less migration to the Ni interface. Thus, the availability of Cu mitigates the negative effects of $AuSn_4$ IMC.
- For both platforms, $AuSn_4$ IMCs are dispersed through the bulk solder as-built. With aging, $AuSn_4$ IMCs have coalesced decreasing the surface area to volume ratio.
- For both platforms, the mean IMC thickness increases with thermal aging time and increases at about the same rate. However, the relative thicknesses of $(Cu, Ni, Au)_6Sn_5$ IMC or $(Ni, Cu, Au)_3Sn_4$ IMC versus $(Au, Ni)Sn_4$ IMC are distinctly different. For the QFN packages the increase in IMC thickness is higher on the flash Au boards. IMC growth is dominated by formation of the $(Cu, Ni, Au)_6Sn_5$ IMC. For the TOPS packages, the mean IMC thickness increase is higher for the thick Au boards. $(Au, Ni)Sn_4$ IMCs from the bulk migrate to the interfaces during thermal aging, contributing to the overall IMC thickness. More Au is available in the case of the thick Au boards, so the contribution to overall IMC thickness is enhanced. The increase in Ni_3Sn_4 IMC is minimal.
- The microstructure of solder joints thermally aged at 125°C for 209 hours is similar to those aged for 30 days or 56 days other than the expected difference in IMC thickness. This indicates that thermal aging at 125°C for 209 hours, equivalent to 1000 hours at 100°C, is sufficiently long to have IMCs in the bulk solder coalesce. The TOPS joint did not show a continuous layer of $AuSn_4$ IMC at the interface, so 125°C for 209 hours was not long enough for this migration to occur.

• Voiding analysis showed that thick Au metallization on thermal pads leads to more voiding and larger standoff height. SMT

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Is Cleaning Critical to PoP Assemblies?

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ZESTRON AMERICA

Summary: Cleaning is a critical process in the electronics manufacturing industry. Effective cleaning improves product reliability by ensuring optimal surface resistance and preventing current leakage that can lead to PCB failure. This paper addresses the cleanliness level of package-on-package (PoP) assemblies, including underneath PoP components and in between packages.

Introduction

Package-on-package (PoP) components were introduced as an avenue for smaller assemblies to be able to house a larger amount of components, which can fulfill a multitude of functions. For example, in the consumer electronics market, cell phones have been significantly reduced in size while meeting additional consumer demands. Nowadays, they contain games, e-mail access, cameras, video cameras, radios, compasses, TVs, etc.—all in one relatively small device.

At the same time, cleaning has become a critical component of the electronics manufacturing process, particularly if long-term board reliability and functionality is a must.

The use of PoPs when designing boards requires additional considerations with regard to cleaning as the authors not only had to clean the flux residues between the bottom package and the board, but also the flux residues between the top and the bottom package. The bottom package standoff height is usually less than 1 mil, whereas the space between packages can vary. These standoff heights do not lend themselves to cleaning with water as the surface tension of 72 dynes/cm for deionized (DI) water is typically too high to penetrate these small spaces. In addition, no-clean pastes and fluxes are typically used for PoP soldering processes, which prohibit cleaning with DI water as well.

Field experience and customer feedback have shown that cleaning PoPs has become increasingly difficult and that typical process settings and equipment configurations may not

result in properly cleaned assemblies. The authors therefore designed this study to validate the effectiveness of using engineered cleaning agents and improved mechanical design features in the wash section of the inline equipment to clean PoPs. Additionally, the authors chose to reflow the test vehicles with and without nitrogen to assess any possible advantages/disadvantages for the cleaning process results.

Article Summary

This three-phase collaborative study [1] was conducted to validate new machine design options and cleaning agents for cleaning PoP assemblies. The authors used two different alkaline cleaning agents and compared their performance at various wash concentrations and belt speeds. Furthermore, the study analyzed the effect of nitrogen versus traditional reflow methodologies with regard to cleanability.

The three phases of the study are:

Phase 1: Cleaning Performance – Visual Inspection. The cleaning performance was assessed via visual inspection with an Olympus SZ 40 microscope with up to 60x magnification.

Phase 2: Cleaning Performance – Ion Chromatography. The cleaning performance was further verified via ion chromatography.

Phase 3: Cleaning Performance – Surface Insulation Resistance. The cleaning performance was also measured using third party surface insulation resistance (SIR) measurements.

Prior to performing the cleaning trials, a total of 18 PoP 14 mm test boards (Figure 1) were populated and reflowed according to the following procedure:

1. A popular HF no-clean solder paste was printed onto 18 bare PoP 14 mm test boards.
2. The accuracy of the print was inspected via microscope.
3. The bottom package was placed onto the board using a pick-and-place machine.
4. Subsequently, the top package was dipped into a HF PoP paste before placing it on top of the bottom package using a pick-and-place machine.
5. Following component placement, the boards were reflowed in a nine-zone reflow oven with nitrogen capability and according to the reflow profile outlined in Table 1. Fourteen boards were reflowed using nitrogen and four boards were reflowed without nitrogen. The same profile was used in both cases.
6. After reflow, several boards underwent X-ray inspection for bridging. No bridging was found.
7. Furthermore, an electrical test using a voltage meter was conducted on one board to ensure proper solder ball connections. The voltage was checked between each point. All boards passed.

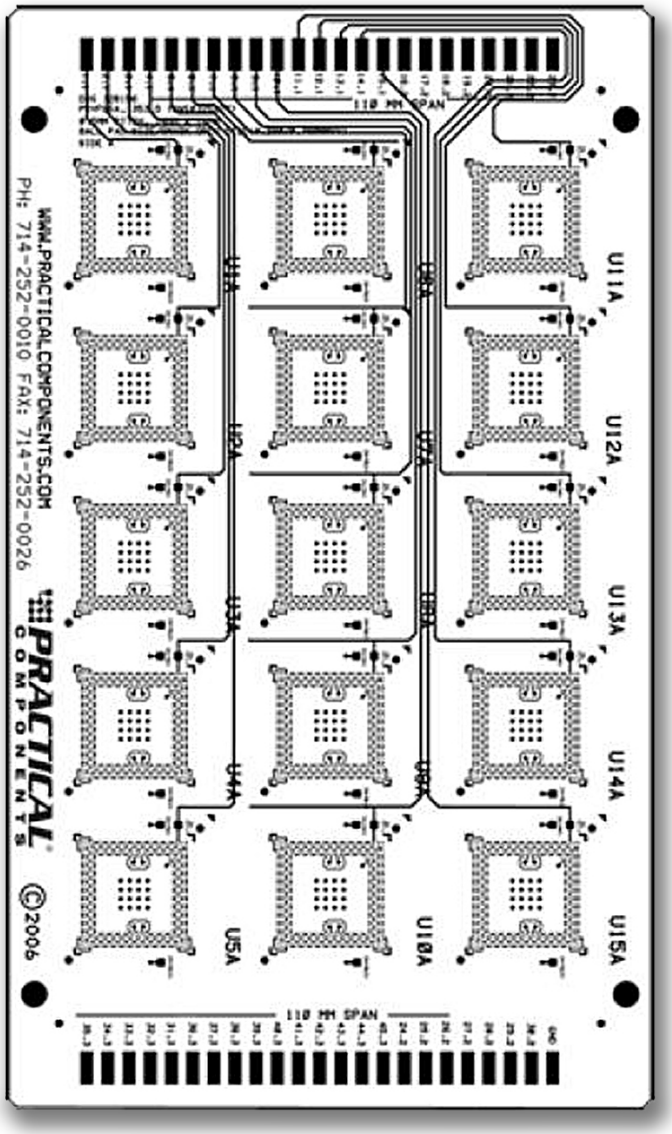

Figure 1: PoP 14 mm test board.

IS CLEANING CRITICAL TO POP ASSEMBLIES? *continues*

Zone	Temperature °C
1	100
2	120
3	150
4	180
5	190
6	210
7	225
8	245
9	265
4 Cooling Zones	
60 cm/min conveyor speed	
O_2 level <50 ppm with Nitrogen	

Table 1: Reflow profile for 18 PoP 14 mm test boards.

Following reflow, all 18 test boards were subjected to cleaning trials and analytical tests as outlined below.

Methodology Phase 1

Cleaning Performance – Visual Inspection

For the first part of the study, a total of 16 cleaning trials were conducted using a Speedline AS 200 inline cleaner. The independent process variables included the two different pastes used, the reflow with and without nitrogen, cleaning agents A and B, wash concentrations of 10% and 15%, a wash temperature of 150°F (65.5°C), belt speeds of 1 FPM an 0.5 FPM respectively, as well as a 12-bar spray configuration in the inline cleaner.

In detail, the wash spray configuration consisted of four V-jet (V), 4 JIC (J) and four deflector (D) spray bars. The spray bars were configured as follows: DVJVJDDVJVJD. This configuration was chosen based on empirical data and as recommended by the equipment manufacturer. It is important to note that typical inline machines are equipped with four spray bars. A summary of the independent process variables is provided in Table 2.

A visual inspection of the boards and component Levels 1 (between board and bottom package) and 2 (between bottom and top package) was performed via 40x magnification and the results recorded. Prior to the inspection, the components were removed and separated.

Results Phase 1

Cleaning Performance – Visual Inspection

The findings of the visual inspection show that for cleaning agent A, only Trials 1 and 2 presented problems. Both trials were conducted on boards reflowed without nitrogen at 10% concentration and belt speeds of 1 FPM (Trial 1) and 0.5 FPM (Trial 2) respectively. For Trial 1, neither Level 1 nor Level 2 passed visual inspection, i.e., flux residues were found between the first component and the board as well as in between components. For Trial 2, residues were found at Level 1 only, i.e., Level 2 was deemed clean. All remaining six trials passed visual inspection for both levels, i.e., no residues were found.

The results for cleaning agent A are summarized in Table 3.

The findings of the visual inspection show that for cleaning agent B, also only Trials 9 and

Variable	
Reflow Profile	With and Without N_2
Cleaning Agent	A and B
Belt Speed	0.5 and 1 fpm
Fixed	
Cleaning Equipment	AS 200 Inline Cleaner
Spray Bar Configuration	DVJVJDDVJVJD
Wash Temperature	150°F (65.5°C)
Solder Paste (bottom level)	HF No-Clean
PoP Paste (top level)	HF PoP Paste

Table 2: Process variables.

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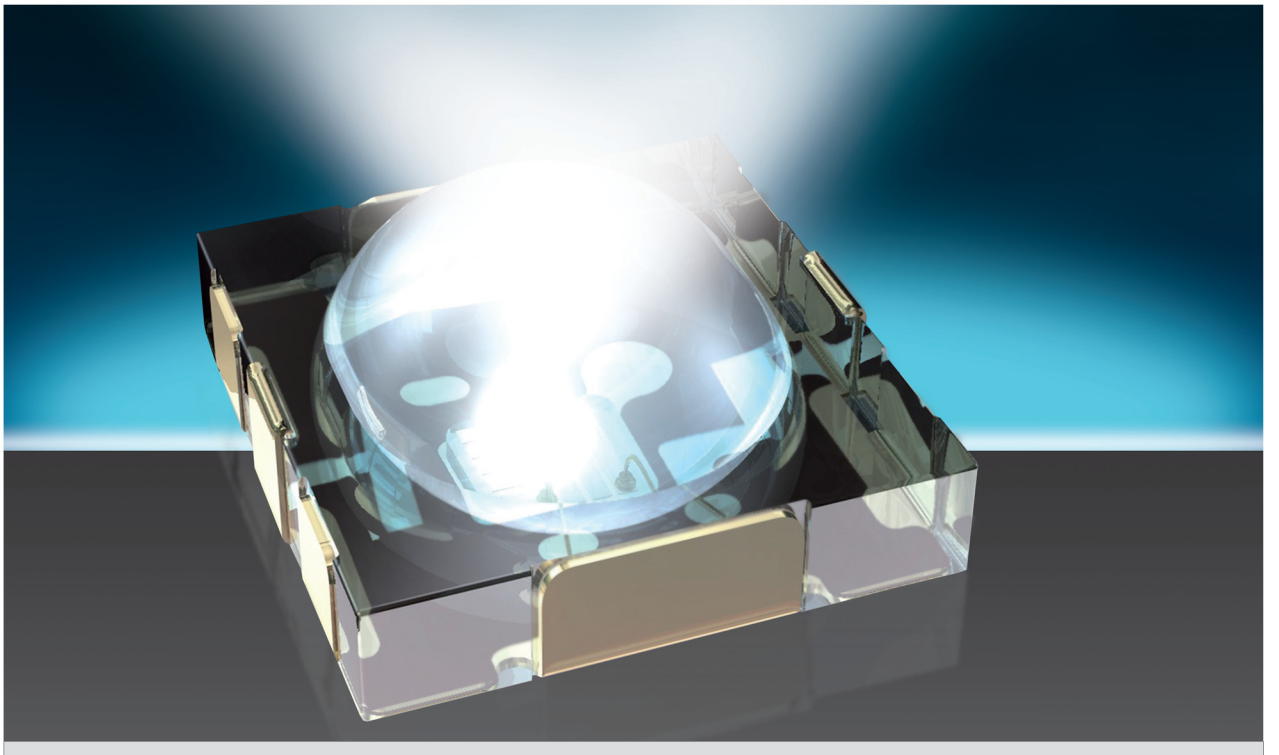

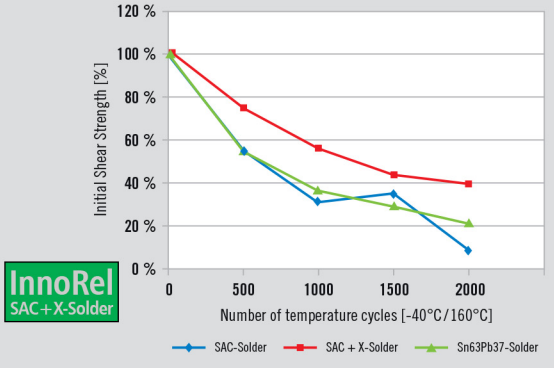

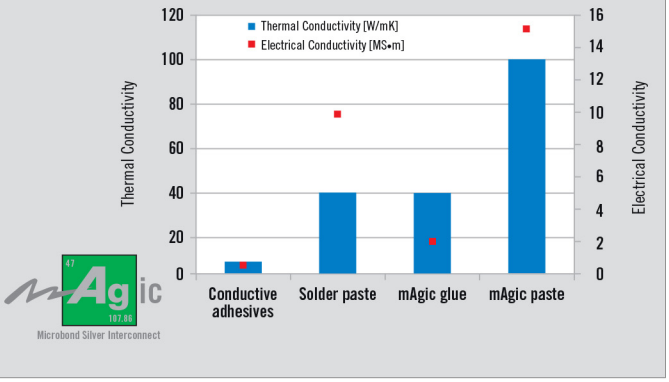

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Trial	Reflow	Concentration %	Belt Speed (fpm)	Results Level 1	Results Level 2
1	no N_2	10	1	-	-
2	no N_2	10	0.5	-	+
3	no N_2	15	1	+	+
4	no N_2	15	0.5	+	+
5	N_2	10	1	+	+
6	N_2	10	0.5	+	+
7	N_2	15	1	+	+
8	N_2	15	0.5	+	+
- not clean + clean					

Table 3: Results of visual inspection cleaning agent A (wash temperature 150°F/65.5°C).

10 presented problems. Both trials were conducted on boards reflowed without nitrogen at 10% concentration and belt speeds of 1 FPM (Trial 1) and 0.5 FPM (Trial 2) respectively. For Trial 9, neither Level 1 nor Level 2 passed visual inspection, i.e., flux residues were found between the first component and the board, as well as in between components. For Trial 10, residues were found at Level 1 only, i.e., Level 2 was deemed clean. All remaining six trials passed visual inspection for both levels, i.e., no residues were found.

The results for cleaning agent B are summarized in Table 4.

Conclusion Phase 1

Cleaning Performance – Visual Inspection

The results based on the visual inspection show that both cleaning agents performed identically and equally well. After nitrogen reflow, consistently clean substrates were found at both wash concentration levels (10% and 15%) and belt speeds (0.5 FPM and 1 FPM). When reflowing without nitrogen, however, the faster belt speed as well as the lower wash concentration impacted the cleaning results. In particular, a 10% wash concentration for both cleaning agents as well as the higher belt speed of 1 FPM resulted in assemblies that were not clean. The same concentration and slower belt speed provided partially clean assemblies. It is important to note, though, that the results were identical for both cleaning agents.

In summary, reflowing PoPs with nitrogen opens the cleaning process window, i.e., wash concentration levels and belt speeds can be adjusted to meet the needs of the manufacturer. While the wash concentration can be reduced to 10%, the belt speed can be increased to 1 FPM, which in the long run will save cleaning process costs and time. However, one should not lose sight of the fact that using nitrogen for reflow is typically much more expensive.

If a reflow process with nitrogen is not avail-

Trial	Reflow	Concentration %	Belt Speed (fpm)	Results Level 1	Results Level 2
9	no N_2	10	1	-	-
10	no N_2	10	0.5	-	+
11	no N_2	15	1	+	+
12	no N_2	15	0.5	+	+
13	N_2	10	1	+	+
14	N_2	10	0.5	+	+
15	N_2	15	1	+	+
16	N_2	15	0.5	+	+
- not clean + clean					

Table 4: Results of visual inspection cleaning agent B (wash temperature 150ºF/65.5ºC).

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able or cost prohibitive, the manufacturer has to be more selective as the cleaning process window will be narrower. Only 15% wash concentration at both belt speeds and for both chemistries provided completely clean assemblies.

The authors conclude that there are several potential reasons for these results. First, any lack of cleaning performance after oxygen reflow could be related to concentration, i.e., 10% may be too low of an effective concentration to clean these challenging components properly. Second, the results show that the higher the belt speed, the more difficult it is to clean due to a lack of exposure time to the cleaning agent, in particular after reflow without nitrogen. However, as mentioned above, reflowing with nitrogen can be cost prohibitive and may not provide the desired cost benefit. By increasing the concentration of both cleaning agents to 15%, the PoPs can be properly cleaned without using nitrogen and at lower as well as higher belt speeds.

To further quantify and qualify these findings, several additional test vehicles were chosen and cleaned with both solutions. Subsequently, this new set of boards was subjected to ion chromatography and SIR analysis to further evaluate any residues underneath the components and more precisely gauge the assemblies' cleanliness levels. Previous studies have shown that relying on visual inspections only may not always be best practice [2].

Methodology Phase 2

Cleaning Performance – Ion Chromatography

The object of performing additional ion chromatography (IC) testing according to IPC-TM-650 method 2.3.28 was to move beyond visual inspection and conduct a more detailed cleanliness analysis of both cleaning agents [3]. IC is a test for ionic cleanliness that determines if contaminants are present on electronic assemblies and bare boards. Such contaminants, when mixed with moisture and an applied voltage, often contribute to electrochemical failures [4].

Based on the assessment during the preliminary cleaning trials, four additional trials were conducted using the higher concentration level (15%) and the slower belt speed (0.5 FPM). The process parameters are outlined in Table 5.

Results Phase 2

Cleaning Performance – Ion Chromatography

The IC results indicate that all substrates passed inspection as the contamination levels found were well below the maximum allowable levels. Overall, in less than half (42%) of all possible cases a small amount of ionic contamination was detected. For anions, this constitutes 30% and for cations 62.5%. In detail, minute amounts of chloride, bromide, nitrate, ammonium, magnesium and calcium were found during all four trials. Sodium, on the other hand, was only detected in Trials 1, 2 and 3. No sodium was found in Trial 4. Furthermore, no other anions or cations were detected.

The IC test results are summarized in Tables 6 and 7.

Conclusion Phase 2

Cleaning Performance – Ion Chromatography

On average, cleaning agent A removed slightly more contamination compared to cleaning agent B. Contrary to the visual inspection results, the above numbers indicate that cleaning agent A performed better on boards reflowed without nitrogen than with nitrogen, which is somewhat surprising and

Trial #	Re-Flow	Cleaning Agent	Wash Concentration %	Wash Temp. °F	Belt Speed fpm
1	no N_2	A	15	150*	0.5
2	N_2	A	15	150*	0.5
3	no N_2	B	15	150*	0.5
4	N_2	B	15	150*	0.5
*65.5°C					

Table 5: Independent process variables – ion chromatography.

ANION SPECIES ALWAYS TESTED FOR					
Ionic Species	**Max. Contimination Levels µ/in²**	**Board # 1 µ/in²**	**Board # 2 µ/in²**	**Board # 3 µ/in²**	**Board # 4 µ/in²**
Fluoride (F^-)	**3**	n.d.	n.d.	n.d.	n.d.
Acetate ($C_2H_3O_2^-$)	**3**	n.d.	n.d.	n.d.	n.d.
Formate (CHO_2^-)	**3**	n.d.	n.d.	n.d.	n.d.
Chloride (Cl^-)	**4**	0.15	0.19	0.15	0.18
Nitrite (NO_2^-)	**3**	n.d.	n.d.	n.d.	n.d.
Bromide (Br^-)	**10**	0.09	0.21	0.16	0.12
Nitrate (NO_3^-)	**3**	0.09	0.10	0.14	0.16
Phosphate (PO_4^{2-})	**3**	n.d.	n.d.	n.d.	n.d.
Sulfate (SO_4^{2-})	**3**	n.d.	n.d.	n.d.	n.d.
WOA (Weak Organic Acid)	**25**	n.d.	n.d.	n.d.	n.d.
n.d. = non detected					

Table 6: Ion chromatography test results for anions.

contradictory to the visual inspection results. The IC testing for Boards 3 and 4, which were cleaned with cleaning agent B, on the other hand, confirmed the visual inspection results. However, one should not lose sight of the fact that all boards passed the IC testing and that the contamination levels detected were well below the maximum allowable limits for each ionic species.

Methodology Phase 3
Cleaning Performance – Surface Insulation Resistance (SIR)

The goal of performing a third-party surface insulation resistance (SIR) analysis was to further validate the cleanliness levels. SIR testing evaluates the propensity for assembly failure caused by shorts or current leakage between metal conductors. It is an electrical test that measures a change in current over time and is typically performed at elevated temperatures and humidity levels [5].

Based on the previous cleaning trial results, a total of 10 boards were populated and reflowed with nitrogen. Eight were cleaned according to the process parameters outlined in Table 8. Additionally, one bare board was used as control. The same cleaning equipment, i.e., a Speedline AS 200 inline cleaner with a 12 spray bar configuration (4 V-Jet, 4 JIC, 4 Deflector; DVJVJDDVJVJD) was used to clean the boards.

In detail, the first two boards were populated and soldered only to test the reliability of the flux. They were not washed. The second two boards were populated, soldered, cleaned,

CATION SPECIES ALWAYS TESTED FOR					
Ionic Species	**Max. Contamination Levels µ/in²**	**Board # 1 µ/in²**	**Board # 2 µ/in²**	**Board # 3 µ/in²**	**Board # 4 µ/in²**
Lithium (Li^+)	**3**	n.d.	n.d.	n.d.	n.d.
Sodium (Na^+)	**3**	0.08	0.20	0.03	n.d.
Ammonium (NH_4^+)	**3**	0.08	0.09	0.12	0.18
Potassium (K^+)	**3**	n.d.	n.d.	n.d.	n.d.
Magnesium (Mg^{2+})	**1**	0.05	0.11	0.11	0.12
Calcium (Ca^{2+})	**1**	0.31	0.45	0.48	0.34
n.d. = non detected					

Table 7: Ion chromatography test results for cations.

IS CLEANING CRITICAL TO POP ASSEMBLIES? *continues*

Trial #	Reflow	Cleaning Agent	Wash Conc. %	Wash Temp. °F	Belt Speed fpm
1	N_2	A	15	150*	0.5
*65.5°C					

Table 8: SIR process parameters.

Board #	SIR Board Preparation
1	Control Board
2 A & B	Populate + Solder + No Wash
3 A & B	Populate + Solder + Clean + Rinse + Dry
4 A & B	Populate + Solder + Clean + Rinse + Dry + Bake
5 A & B	Populate + Solder + Only Clean + Dry
6 A & B	Populate + Solder + Only Clean + Dry + Bake

Table 9: SIR board preparation.

rinsed, and dried, which constitutes standard process protocol. Another two boards were populated, soldered, cleaned, rinsed, dried, and baked to check if the drying process is efficient. The following two boards were populated, soldered, only cleaned (not rinsed), and dried. The rinse step was omitted here to simulate possible cleaning agent residues due to improper rinsing. The last two boards were populated, soldered, only cleaned (not rinsed), dried, and baked. The boards were not rinsed to simulate the potential of dried cleaning agent residues. It is important to note, that the boards were baked at 85°C for 30 minutes. The control board was not treated. The test was conducted for a total of 192 hours at 85°C and 85% relative humidity. Initial and final testing was done at ambient temperatures and humidity. Furthermore, the wires were carefully soldered with only the end of the board protruding from the bags to minimize contamination.

The SIR board preparation steps are outlined in Table 9.

To obtain the results, three data points were manually assessed, i.e., one before the test, one at 96 hours and one at the conclusion of the test. The resistance at each daisy chain was recorded for each data point. The SIR test was conducted in accordance with IPC standard IPC-TM-650 Method 2.6.3.7.

Results Phase 3 *Cleaning Performance – Surface Insulation Resistance (SIR)*

All boards subjected to SIR analysis passed the test. In particular, the in-situ measurements were about 0.6 ohms higher than the initial/final measurement, which matched quite well with the resistance temperature dependence of copper. A 0.7 ohm rise was calculated between 25°C and 85°C from the equation.

The SIR test results are graphed in Figure 2.

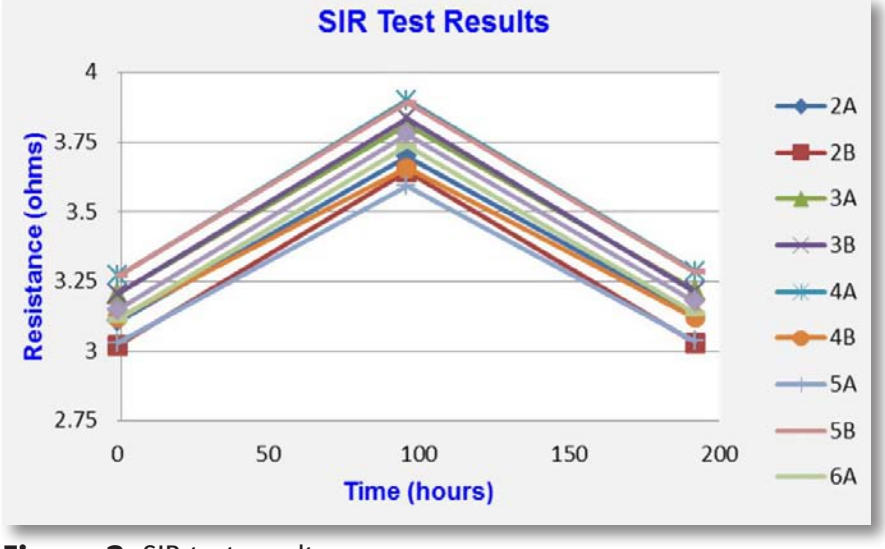

Figure 2: SIR test results.

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Conclusion Phase 3

Cleaning Performance – Surface Insulation Resistance (SIR)

The SIR results indicate that all boards, i.e., even the boards that were not cleaned, passed SIR testing. For the boards that were cleaned but not rinsed, this means that any chemistry left behind on the board may not cause any problems. For the boards that were not cleaned at all, however, the results are not necessarily an indication that PoP assemblies do not need cleaning at all. For one, not all no-clean fluxes have the same signature, i.e., some can be more corrosive than others. Any potential corrosion will more than likely not occur until the boards are deployed in the field.

Second, as the SIR testing was conducted in a very controlled environment, the test results are not necessarily an indication of any board failure potential once they are subjected to temperature and humidity fluctuations. Long-term exposure to varying environmental conditions may stress and crack the inert resin layer, which will expose flux activators to the atmosphere and can lead to electrochemical migration and dendrite growth. Ultimately, this can cause board failure.

Final Conclusions

The results of all three phases of the study show that with new-generation cleaning agents and an improved mechanical design in the wash section of an inline cleaning machine, PoP assemblies can be effectively cleaned.

As for this paper, only two package components were used on a test vehicle. ZESTRON is planning to collaborate with industry partners to develop and validate cleaning process parameters for multiple stack PoP assemblies in the future.

This research paper is part of a series written on optimizing precision cleaning processes for the electronics manufacturing industry. These studies have been presented at the industry's known conferences SMTAI and IPC APEX EXPO. Based on our findings, key market developments have been initiated, thereby addressing the current shortcomings observed in the industry. **SMT**

Acknowledgements

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Dr. Harald Wack is president of ZESTRON. He graduated with M.S. and Ph.D. in organic chemistry from Johns Hopkins University in Baltimore, Maryland, and has 17 years of global experience in the electronics manufacturing industry with five years' experience in academic research related to asymmetric catalysis. He is a current member of the IPC Cleaning & Alternatives Handbook task group and chairs the European IPC/SMTA Cleaning Symposium 2009.

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Jigar Patel, M.S. chemical engineering, is senior process engineer at ZESTRON. As an active member of various industry organizations, such as the IPC and SMTA, Patel has presented a number of technical papers at educational events concurrent with trade association conventions and expos.

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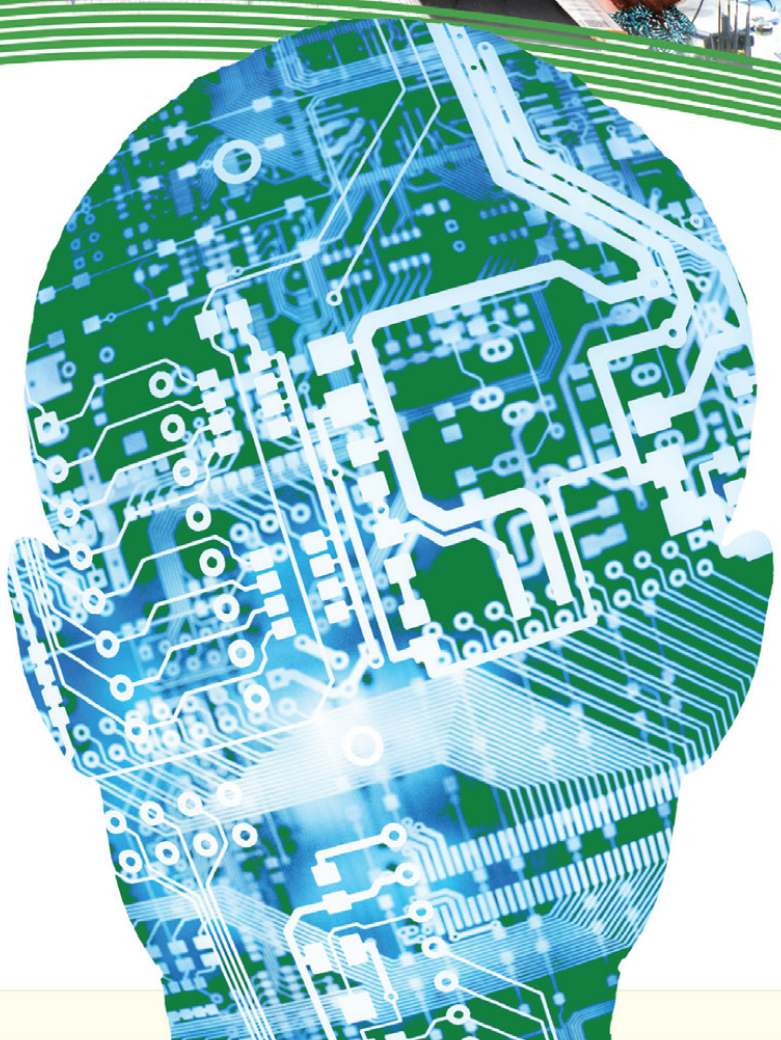

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ZESTRON launched two new flux removal products at IPC APEX EXPO 2012. Technical Marketing Manager Sal Sparacino, and Application Technology Manager Umut Tosun explain their characteristics and benefits to Technical Editor Pete Starkey.

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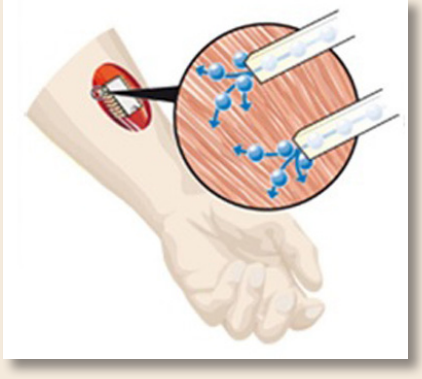
First Chemical Circuit Developed

The Organic Electronics research group at Linköping University previously developed ion transistors for transport of both positive and negative ions, as well as biomolecules. Klas Tybrandt, doctoral student in Organic Electronics, has now succeeded in combining both transistor types into complementary circuits, in a similar way to traditional silicon-based electronics.

An advantage of chemical circuits is that the charge carrier consists of chemical substances with various functions. This means that we now have new opportunities to control and regulate the signal paths of cells in the human body.

"We can, for example, send out signals to muscle synapses where the signaling system may not work for some reason. We know our chip works with common signaling substances, for example acetylcholine," says Magnus Berggren, professor of organic electronics and leader of the research group.



The development of ion transistors, which can control and transport ions and charged biomolecules, was begun three years ago by Tybrandt and Berggren, respectively a doctoral student and professor in organic electronics at the Department of Science and Technology at Linköping University. The transistors were then used by researchers at Karolinska Institutet to control the delivery of the signaling substance acetylcholine to individual cells. The results were published in the well-known interdisciplinary journal PNAS.

In conjunction with Robert Forchheimer, Professor of Information Coding at LiU, Tybrandt has now taken the next step by developing chemical chips that also contain logic gates, such as NAND gates that allow for the construction of all logical functions.

His breakthrough creates the basis for an entirely new circuit technology based on ions and molecules instead of electrons and holes.

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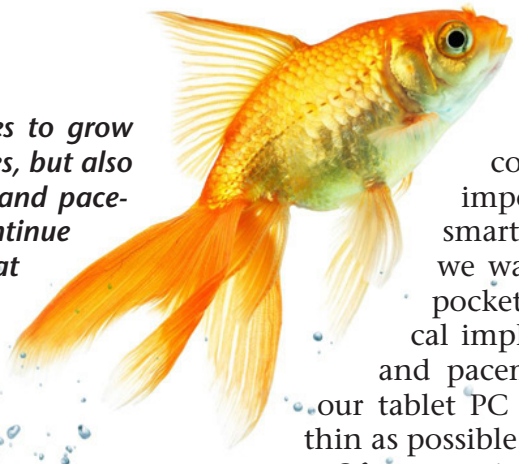
SMT TRENDS & TECHNOLOGIES

It's Getting Crowded

by Sjef van Gastel
ASSEMBLÉON NETHERLANDS B.V.

Summary: Miniaturization continues to grow in importance; not only for smart phones, but also for medical implants like hearing aids and pacemakers. Integrated circuits (ICs) will continue to integrate more devices, but the great majority of components on a PCB are passives. At board level, the next round of miniaturization will come from three key factors outlined by Sjef van Gastel.



Amazing, isn't it? For a little less than $500 you can buy a high-end smartphone that serves as an all-in-one device. Integrated communication (voice calling, e-mail, Skype, SMS, Twitter), information (PDA, radio, navigation, Internet), and entertainment (camera, gaming, media player) can all be found in a housing slightly larger than a pack of cards with the thickness of a glossy magazine.

The most important enabler is miniaturization. Miniaturization brings more functions in the same size, or the same functions in a smaller size. Take a look inside your smartphone. Teardown websites will show thin and flat subassemblies, small-sized and high-density populated substrates, and large-area thin battery packs (Figure 1).

Miniaturization continues to grow in importance, not only for smart phones (Remember, we want them to fit in our pockets!), but also for medical implants like hearing aids and pacemakers. And we want our tablet PC and LED TV to be as thin as possible.

Of course, integrated circuits (ICs) will continue to integrate more devices, but the great majority of components on a PCB are passives. At board level, the next round of miniaturization will come from the three key factors that follow.

Reducing Component and Substrate Line Interspacing

A large number of components per board area translates to minimizing component size and related interspacing. Some years ago, the smallest passive component in handheld products was the 0201 (0.6 mm x 0.3 mm). Now it is the 01005 (0.4 mm x 0.2 mm), with leading passive component manufacturers having recently introduced 0.3 mm x 0.2 mm compo-

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IT'S GETTING CROWDED *continues*

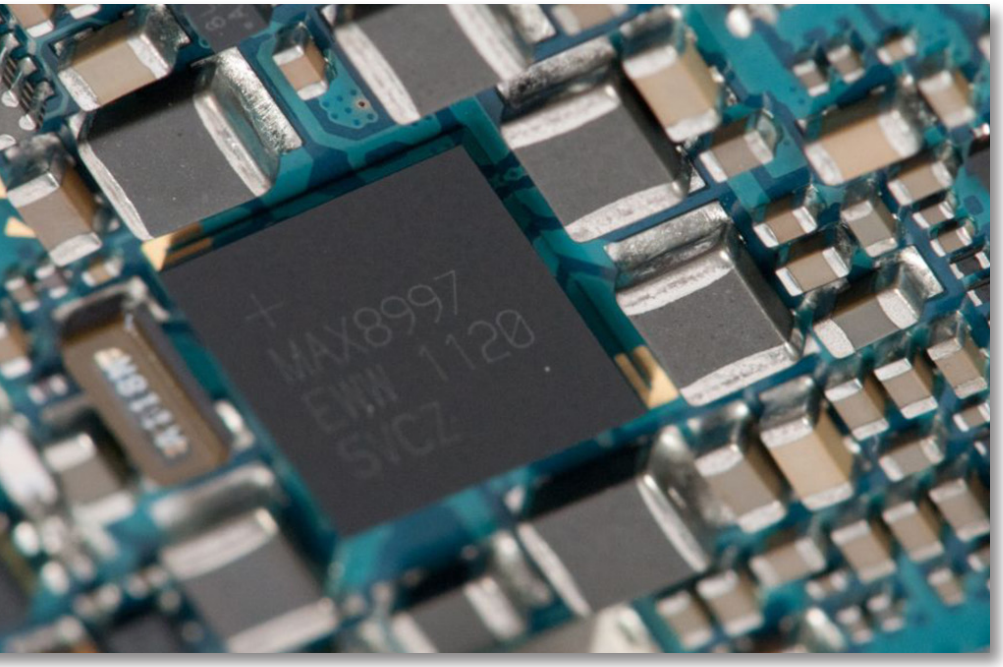


Figure 1: Example of miniaturization on a smartphone.

nents, and 0.2 mm x 0.1 mm types expected later this year.

Passive component interspacing is expected to shrink to below 60 microns. Achieving this high-density placement means shrinking related substrate line interspacing. As a result, the number of substrate layers will increase to enable line rerouting. This action has unwanted side effects, though: The signal line lengths, along with the substrate costs, will increase. To overcome these disadvantages, and also to increase smartphone design flexibility, more and more smartphone functions are becoming available as functional IC modules, mostly in ball grid arrays (BGAs) or chip scale packages (CSPs).

So, we are now seeing a shift of passive components from the main board (second-level interconnect) to functional modules (first-level interconnect). This component migration from PCBA toward semiconductor assembly and test services (SATS) will also bring new challenges for the semiconductor packaging industry: The combination of a few flip chips with multiple ultra-small passives on the first-level interconnect substrate. Most chip assembly systems offer high-accuracy placement at moderate speeds, while the need is for a combination of both high accuracy and high speed.

Embedding Components in Substrates

Further integration and miniaturization comes from placing components inside the substrate rather than only on substrate surfaces: Component embedding. Here, components are migrating from the PCBA manufacturing process toward the substrate manufacturing process.

Components may be embedded in two ways. First, passive components can be "formed" on the inner substrate using thick- or thin-film technology. Here, restrictions on electrical values and related tolerances exist. Second, components may be placed on substrate inner layers. This demands special precautions to limit warping in the thin inner layers and avoid breaking ultra-thin components (passives down to 50 microns, and active dies down to 20 microns). It also demands high placement accuracy (down to 10 microns, see Figure 2).

Embedded component technology is expected to grow in importance in the coming

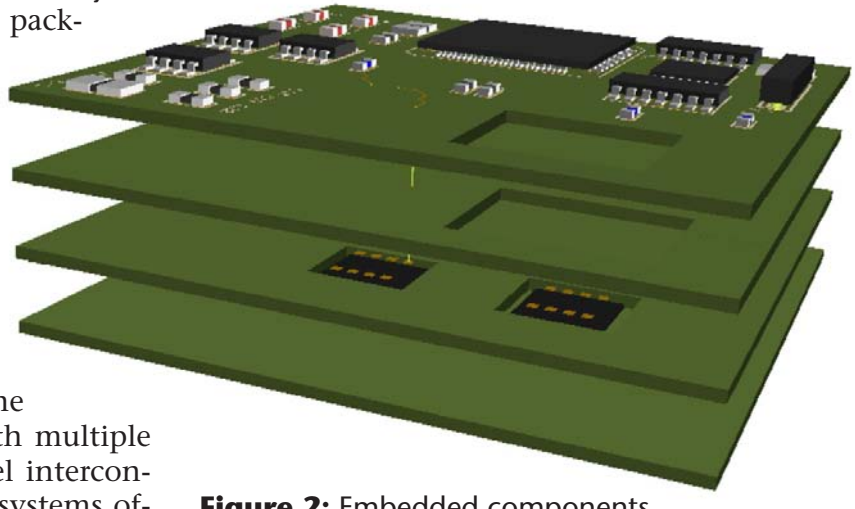


Figure 2: Embedded components.

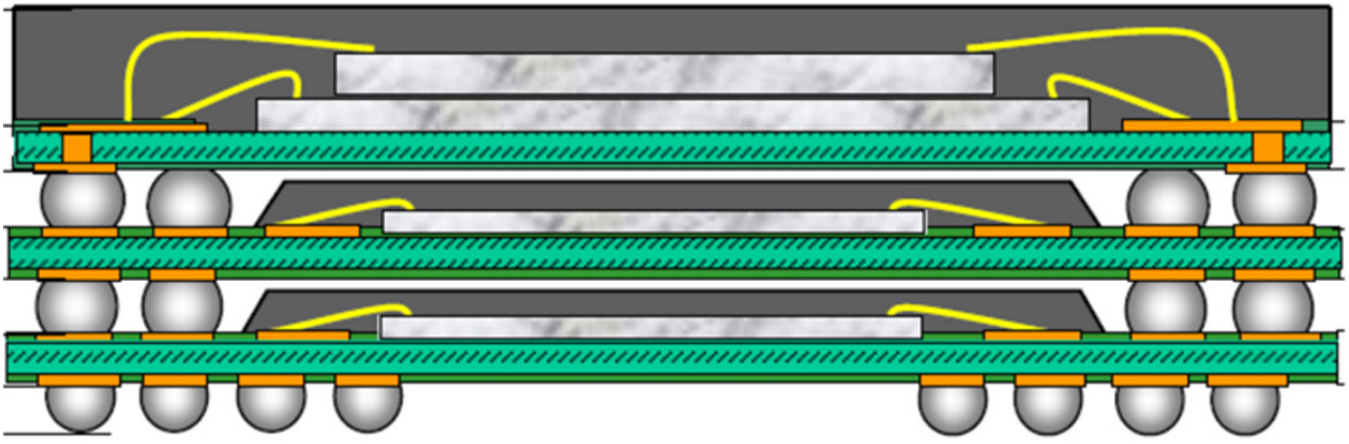


Figure 3: PoP components.

years. In addition to the advantages (improved product reliability, reduction of substrate area, and shorter interconnections), it will also bring disadvantages (rework is not possible, thickness limitations, and special SMDs needed with Cu terminations related to Cu structuring).

Stacking Components on the Increase

In addition to reducing sizes and embedding them, components may also be stacked on top of each other on substrate outer surfaces. This component stacking is called package-on-package (PoP) and is growing in popularity for smartphones. The main reason for this is flexibility in combining microprocessors with memory modules with shorter interconnections also increasing signal transfer speed. An overview of smartphone teardowns shows an average of two PoPs per smartphone. Two packages are usually stacked (CSP style); however, triple stacks are also possible (Figure 3).

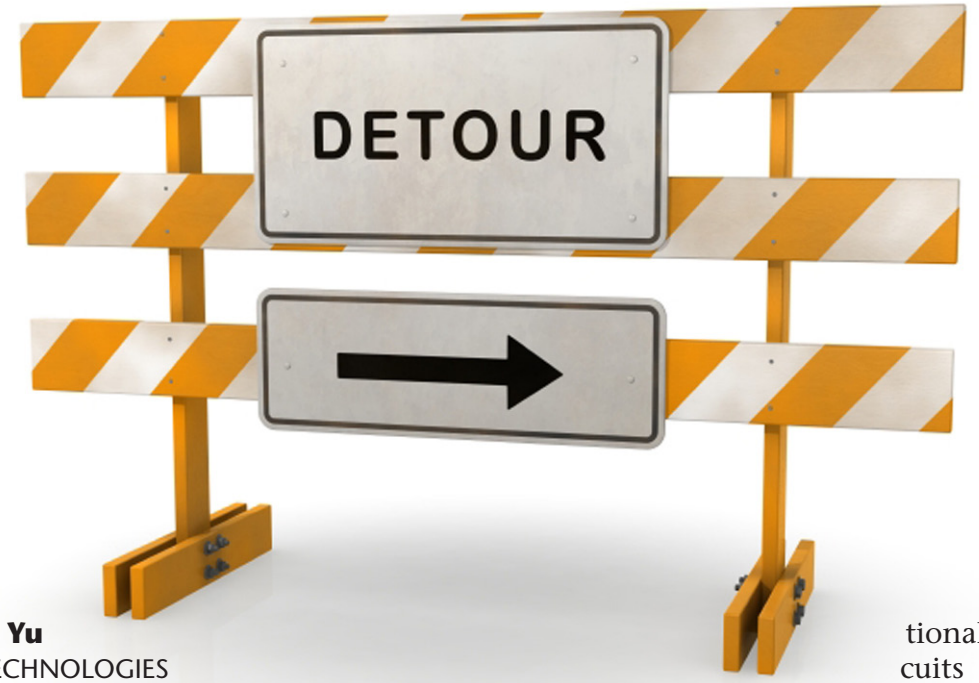
What will be next in the ongoing race for the smallest and thinnest smartphone? No one knows, but one thing is certain: SMT technology will miniaturize it. And pick-and-place machines must be able to cope.

The next generation of smartphones, which will, in turn, help drive miniaturization in the rest of the industry, will make three demands on pick-and-place machines. Placement accuracy must go down to 25 microns for CSP placement in reflow and down to 10 microns for conductive adhesives. Delicate components will need ultra-low placement force of below 1 N along with impact force control. In addition, placement quality must be below 10 defects per million to prevent production lines from turning out expensive failures.

It's getting crowded; let's shrink again. **SMT**

In addition to playing the clarinet in two bands, Assembléon's Sjef van Gastel has another passion: SMT. He has been with the company since its start-up as a Philips division in 1979. As the current Manager for Advanced Development, he combines his experience as systems architect and machine designer to explore technical and business opportunities from emerging technologies. van Gastel holds many patents and is a frequent speaker at international conferences related to SMT. He is also the author of "Fundamentals of SMD Assembly," which has become a standard piece of literature in the industry.

MEMS/SMT Hybrid PCBs Take Design/Assembly Detour



by Michael Yu
NEXLOGIC TECHNOLOGIES

Summary: ***Why place both MEMS and SMT technology on the same subassembly? The answer can be found in the considerable performance gains achieved within an extremely small system. Size, weight, and power (SWaP) consumption most often drive the OEM to use this combination of MEMS and SMT devices on a PCB.***

The main thrust of microelectronics, since their inception, has been continual miniaturization to make chips, PCBs, and systems smaller, faster, increasingly functional, and more reliable. Subsequently, microelectromechanical systems (MEMS) came into the electronics industry limelight with significant benefits. Today, hybrid MEMS/surface mount technology (SMT) subsystems on PCBs are making greater inroads into OEM markets.

When you put these two technologies together, it's important to first know the difference between them. In simple terms, conventional integrated circuits (ICs) as we've known them over the last few decades are SMT devices generating and conducting electronic signals without the need for moving mechanical parts. Those are regarded as solid-state silicon devices. On the other hand, MEMS components add the extra dimension of moving mechanical parts, in most cases, on to the same silicon chip that populates the integrated microelectronics. Silicon-based MEMS components can range from simple devices with few to no moving parts to highly complex devices with considerable numbers of moving parts.

But the all-consuming question is: Why place these two technologies on the same subassembly? The answer can be found in the considerable performance gains achieved within an extremely small system. Size, weight, and power (SWaP) consumption most often drive the OEM to use this combination of MEMS and SMT devices on a PCB.

For example, a navigation system can be squeezed into a small PCB along with other

functions (Figure 1). The normal size of a three-axis gyroscope navigation system is 2,500 mm x 1,400 mm x 2,100 mm. But the dimension of MEMS/SMT three-axis gyroscope navigation IC is 4 mm x 4 mm x 1.1 mm, which is dramatically smaller.

Also, an unmanned driving system can be shrunk down into small boards for missile, unmanned aerial vehicle/unmanned ground vehicle/unmanned undersea vehicle (UAV/UGV/UUV). In addition, micro-satellites can acquire a huge performance improvement when you compare them with more expensive traditional satellites characterized by long development cycles. Plus, all these microsystems feature power savings, dimension reduction, cost savings, and greater application flexibility.

So, it's not too far-fetched for MEMS/SMT hybrid PCB applications to trigger such futuristic electronic gadgets as portable robotic smartphones that'll help drive our cars, fly airplanes, automate battlefield and sea warfare attacks, and safeguard our troops in skirmishes, all while furthering today's drone technology. But, on a more humane side, MEMS/SMT hybrid PCB technology can be the basis for intelligent surgery robotics that can perform intricate operations to remove deadly body tissues like cancer.

But the fact still remains: These two technology giants, MEMS and SMT components, have completely different system integration requirements. In effect, MEMS assembly deals with a high-level integration of dissimilar functions, while traditional microelectronics assembly is low-level integration of electronic components.

Examples of two different types of MEMS devices populating MEMS/SMT hybrid PCBs today are an absolute pressure sensor and gyroscope (Figures 2 and 3). The MEMS gyroscope has inertial motion detecting sensors in a three-axis accelerometer for detecting acceleration as well as a data-processing integrated circuit. The absolute pressure sensor MEMS has a precision atmospheric pressure sensor and data calculation capability to detect and process the measuring results.

The PCB is the system carrier to combine the different functional blocks into a complex system and provides the communication channels for those blocks, as well as the power supply path and resource sharing infrastructure.

As the chart shows, there are key differences in assembly when you compare MEMS with conventional SMT PCBs. For conventional

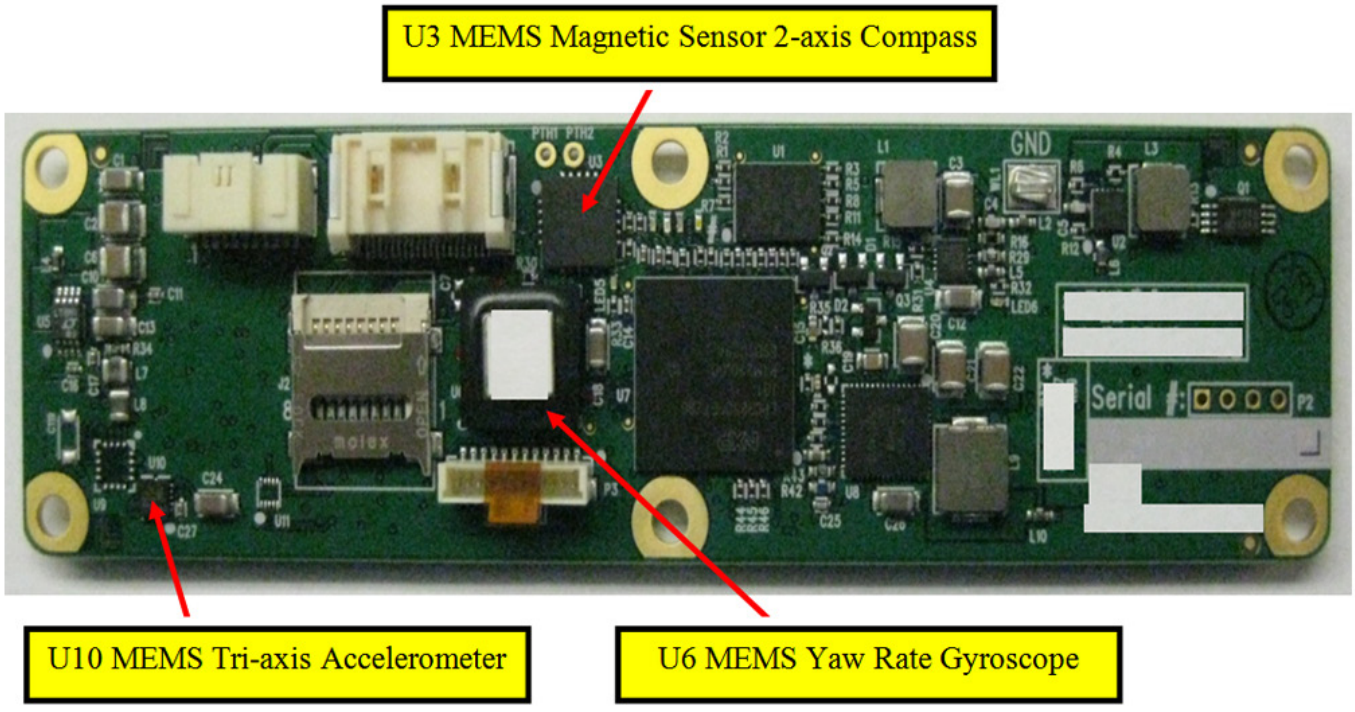


Figure 1: A MEMS navigation system is squeezed into a small PCB along with other functions.

MEMS/SMT HYBRID PCBS TAKE DESIGN/ASSEMBLY DETOUR *continues*

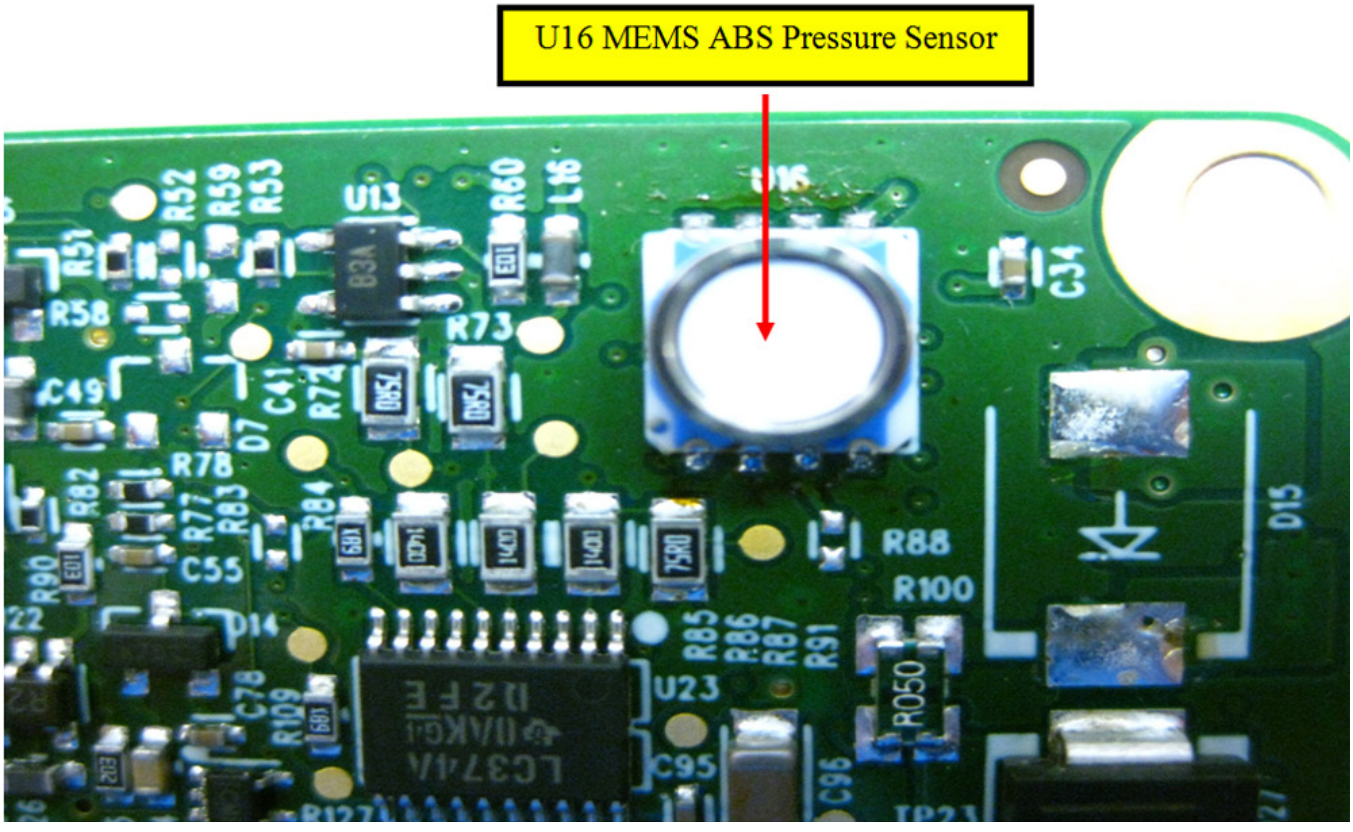


Figure 2: MEMS absolute pressure sensor (U16).

SMT microelectronics assembly, the traditional system integration requirements focus on the solder joint's electrical connection. The major assembly steps are solder paste printing, pick-and-place, and reflow with the latter being the most important step.

As far as MEMS assembly is concerned, the key requirement involves the combination of mechanical performance and electrical connection. From a broad perspective, the major issues are assembly stress control, minimizing such mechanical problems as stress-related MEMS damages and thermal damage, and electrical connection performance. Hence, the most crucial step is combining the IP-protected MEMS assembly process and modified SMT process.

Challenging Assembly

Several problematic areas arise when you try to mix MEMS assembly with conventional PCB assembly. And, by the way, there are currently no IPC standards covering hybrid MEMS/PCB assembly design-for-manufacturing and quality control (QC) inspection. Consequently, the experienced PCB assembly house must forge together an assembly strategy to effectively produce these hybrid PCBs. On top of this, no standard mass-production assembly equipment is tailored for hybrid MEMS and conventional PCB assembly. So, the savvy CM or EMS provider is left to his own ingenuity and brainpower to create such a line.

The conventional PCB assembly process introduced a high level of shock and stress that has the highest probability of damaging a MEMS element. Damages incurred during the PCB separation and ultrasonic cleaning processes significantly reduce product final test yield and long-term reliability. Add to that PCB bowing and twisting after solder reflow—even the second-pass reflow after finishing bottom-side reflow. The top-side reflow process and the stress on the fab pad structure damages the bottom side MEMS pad structure, solder joints, and the MEMS devices themselves.

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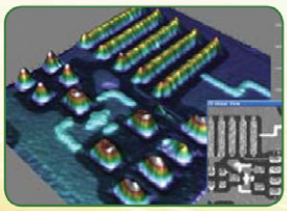

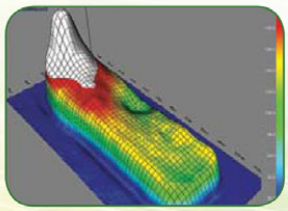

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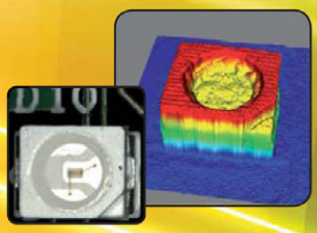

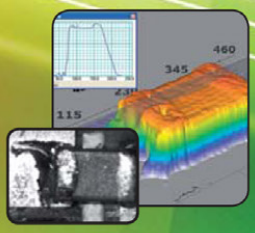

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MEMS/SMT HYBRID PCBS TAKE DESIGN/ASSEMBLY DETOUR *continues*

based MEMS devices have limited thermal life. They cannot withstand reflow temperature twice. However, due to certain aerospace engineering limitations, small PCBs cannot allow all MEMS components on one side or the top side. Therefore PCB design engineers must place some MEMS components on the bottom-side of a double-sided assembly.

MEMS components have extremely high placement and orientation accuracy requirements simply because their applications demand them. Here is where major problematic areas arise since standard SMT pick-and-place machines, solder-paste thickness, and reflow movement cannot meet those high requirements. Along this same line, some MEMS components might require a high level of clean room cleanliness and a low-light exposure environment for the component manufacturing process and system assembly.

While this hybrid offers major system advantages, assembling MEMS and SMT components on the same PCB poses difficult challenges. MEMS components are completely different from SMT components. Some MEMS can only withstand one reflow cycle. Take, for example, the MEMS absolute pressure sensor, which is used to measure an aviation vehicle's altitude. This MEMS device is made of silicone gel material that can only withstand a maximum temperature of 240°C for 10 to 20 seconds. With this limitation, it cannot undergo a second lead-free reflow process if the system designer intentionally or inadvertently places this MEMS device on the secondary board side. Therefore the design must be performed thoughtfully to assure this MEMS device is on the primary board side to avoid the second reflow cycle.

On the other hand, SMT components can withstand three or more reflow cycles. Also, the MEMS thermal tolerance is much lower than with SMT components. Standard SMT components, like micro-BGA packaged FPGAs or ultra-low-pitch CSP devices, have a fairly large

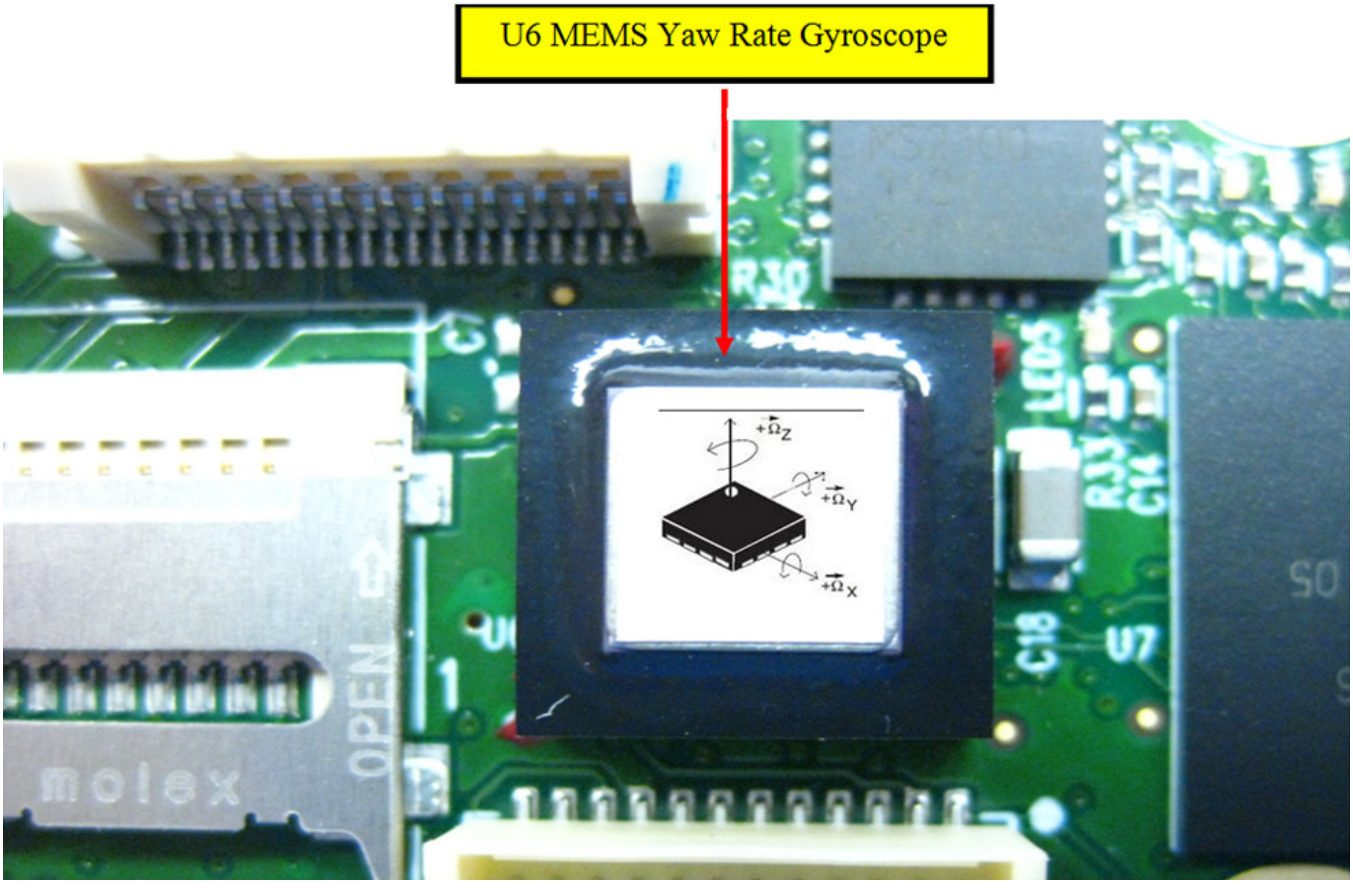

Figure 3: MEMS gyroscope.

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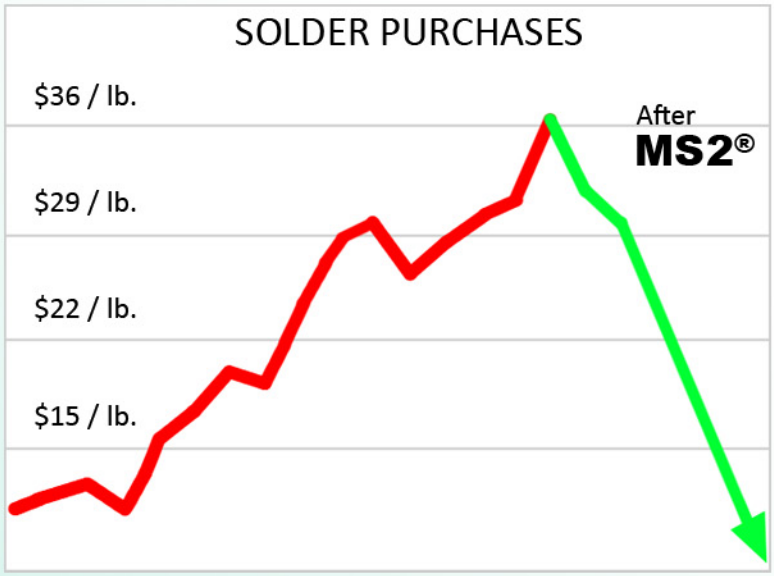

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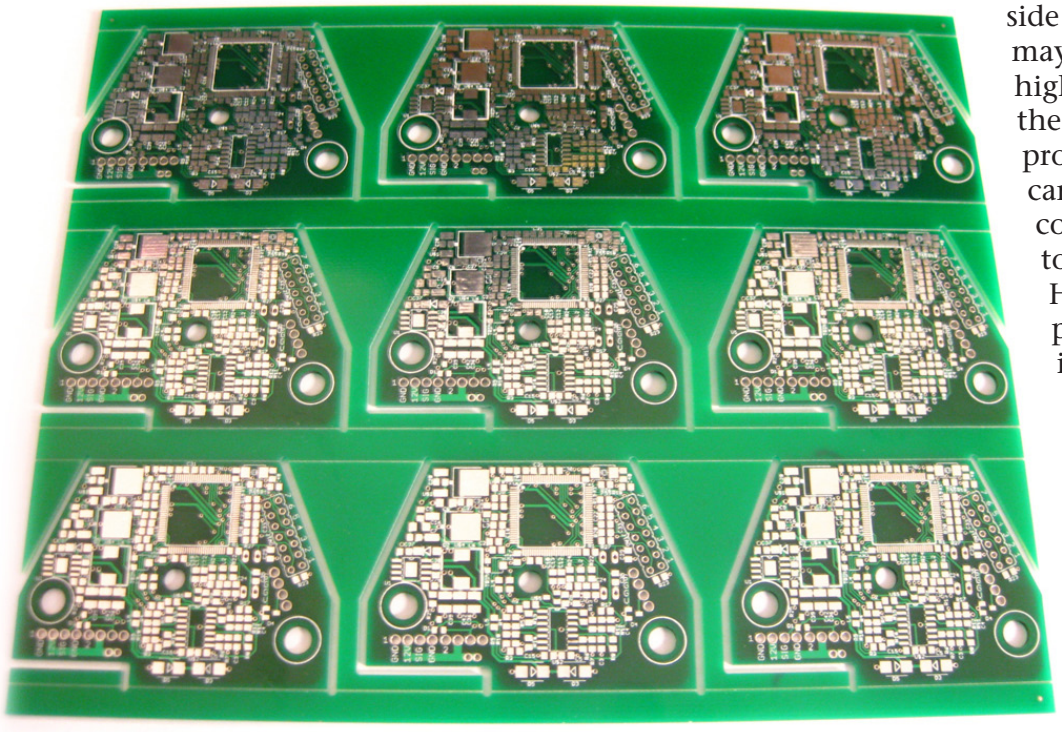

Figure 4: A panelized PCB.

thermal tolerance because they consist of a solid-state silicon die without other low-melting-temperature materials.

But the MEMS components consist of different materials such as silicon structures, polymers, metals, or oxidized metals. The use of these materials provide better than silicon die mechanical properties and high degree of reliability. When multiple materials are bonded to become a highly-accurate structure their thermal tolerance is much less than the solid-state single-material silicon die.

Moreover, due to the limitation of a micromechanical system, MEMS components are extremely sensitive to assembly stress and can be easily damaged by typical PCB assembly steps, such as reflow, wave soldering, and de-panel process.

Another thing the OEM must consider is that some MEMS components, like a MEMS digital altimeter, are rather high, some extending upwards of 3 to 5 mm compared to low-profile SMD BGAs or CSPs (1 to 2 mm). When they are installed on the bottom side of the board, the standard selective wave-soldering fixture becomes too thick to achieve good wave-soldering quality. To make things worse, those bottom-side MEMS components may not withstand the high temperatures of the wave-soldering process. PCB designers cannot move all MEMS components to the top side of the board. However, a special proprietary soldering process can be applied to finish the bottom-side soldering and meet high aerospace quality requirements.

Most aerospace MEMS control and sensing boards are very small. For assembly efficiency, those small boards need to be panelized, as shown in Figure 4, and three global fiducial marks should be added on the panel-frame areas. Unfortunately, with this hybrid MEMS/SMT PCB technology still in its infancy, most EMS companies don't have sufficient experience to handle a MEMS boards de-paneling process. They usually subject those boards, as they do with standard SMT assembly boards, to the de-paneling process, resulting in low final test yield.

The breakout is performed manually, and MEMS solder joints are damaged as a consequence. The ideal process is to apply the necessary experience by selecting the proper de-panel tooling and process to minimize cutting stress to MEMS component terminations. The CM's or EMS provider's depaneling process and special tooling must assure zero damage to all MEMS solder joints and different hybrid MEMS/SMT boards. Based on these specific differences, the traditional PCB assembly process takes on considerable adjustments to produce highly-reliable hybrid MEMS/SMT component boards.

Host of Considerations

Consequently, the CM or EMS provider must take into account a host of considerations. For

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Assembly Process	SMT Assembly	MEMS Assembly
Solder Paste Printing with Stencil	Standard pads and solder-volume easily meet SMT quality requirements, based on IPC standards.	IPC Standards may not meet MEMS requirements. Need more solder volume or special joint-strength enhancement measures.
Pick-and-Placement Process	Standard placement accuracy nd fiducial alignment meet SMT quality requirements, based on IPC standards.	IPC Standards may not meet MEMS requirements. Need more placement accuracy or special enhancement for P&P capability.
Reflow Profile	Standard paste-required reflow profiles meet SMT quality requirements, based on IPC standards.	MEMS reflow may need extremely high heat-transferring efficiency for the reflow oven to handle the large MEMS body and short time above 240 degree C. Need special reflow profiles for MEMS.
Wave Soldering Process	Standard selective-wave fixture and process meet SMT quality requirements, based on IPC standards.	The bottom-side of MEMS may require special wave soldering process because some MEMS components are high.
Hand-soldering Process	Standard hand-soldering process meets SMT quality requirements, based on IPC standards.	MEMS hand-soldering may need special temperature-cycle profiling to reduce the thermal impact.
De-paneling Process	Standard de-paneling machines and process meet SMT quality requirements, based on IPC standards.	Standard de-paneling machines and process cannot meet MEMS quality requirements. They need special de-paneling process.
2nd Operation Process	Standard 2nd Operation process can meet all requirements.	MEMS may need epoxy or RTV enhancement for the high strength and high reliability requirement.
QC Inspection; X-ray Inspection; AOI	Only 100% regular X-ray inspects BGA/CSP joints. AOI may be not required. Based on IPC standards, regular visual inspection is required.	100% AOI inspection and 100% 3D X-ray inspection for all underneath joints and for any kit size. We need to change X-ray beam direction to inspect internal complex structure-covered solder joints of MEMS. Visual inspection needs new MEMS standard.

starters, both MEMS/SMT hybrid PCB layout engineering and assembly engineering must closely collaborate throughout such a project. MEMS components need extra edge clearance due to their heights and complex structure. Those extra edge clearances should be much larger than those needed for normal BGA components.

This provides enough room for quality inspection (including visual inspection and X-ray inspection) and for the touch-up and rework. MEMS assembly needs extra board stiffness and very low warpage tendency. Also, high-end PCB laminate material and a good copper balance are required for proper assembly. The heat-relieving pad layout also helps MEMS assembly quality. The PCB layout engineer must pay special attention to stress relief and heat isolation, as well as follow certain guidelines to protect the MEMS devices.

Other design guidelines can protect MEMS components and improve MEMS assembly quality. One is to provide enough edge clearance for MEMS boards, although it is sometimes physically impossible. Another is use design ingenuity to layout all MEMS on one side of the board and avoid a double-sided MEMS layout. Also, the PCB designer should use larger pads for MEMS components since small pads need joint-enhancement measures.

Further, the PCB designer must always add good board-level fiducial marks on the three corners. Also, he or she needs to avoid odd-shaped PCB boards for MEMS/SMT hybrids. Lastly, the PCB designer should avoid deep cutting or notching into the middle of a board design to prevent board warpage. Deep cutting or notching greatly reduces board stiffness and reduces PCB resistance to the thermal stress during the reflow process, resulting in a large post-reflow board warpage. As a result, board warpage increases the possibility of MEMS solder-joint cracking, causing low final testing yield.

At assembly, a substantial amount of adjusting is required to effectively process MEMS/SMT hybrid PCBs. Those adjustments and introduction of new assembly techniques are targeted at successfully resolving the process stress and avoiding process shock, as well as solving board bowing and flexing reflow problems. And you have to accomplish that while keeping in mind the fab house's limitations. That means those measures won't require the special fabrication capital equipment investment and extra longer lead time. They also won't result in extra fabrication costs.

Also needed are assembly steps to properly solve the double-sided MEMS assembly issues and prevent any thermal shock and damage or risk of it. Meeting the high MEMS device position and orientation requirements is yet another major step in assembly adjustment. Special AOI processes, for example, must be developed to successfully test and inspect MEMS/SMT hybrid products. AOI machines need multiple lighting options to light the different MEMS for inspection. Due to the great variety of MEMS, their markings are not as clear as SMD standard markings.

Aside from these adjustments, the CM or EMS provider must also develop highly specific design for manufacturing (DFM) guidelines, as well as tailored engineering and technician instructions and guidelines to ensure efficient assembly operations. Lastly, QC inspectors must be trained to understand the slightest defects in these complex MEMS/SMT hybrid PCBs. For example, they need to learn new quality criteria to identify the MEMS insufficient solder defects and micro-cracking on the MEMS terminations. For instance, in some applications, larger MEMS components need more solder to gain extra strength on the board as well as to meet aerospace requirements. **SMT**

Michael Yu is senior manufacturing engineer at NexLogic Technologies, Inc., San Jose, California, with extensive experience in process control, SMT process, and manufacturing resources management. He has been in the EMS industry for over 16 years with work experience at Bema Electronics and Pactron Electronics. He has a B.S. in Materials Engineering from Shanghai Jiao Tong University and an M.S. in Mechanical Engineering from South Dakota School of Mines & Technology.

Assembly and Rework of Lead-Free PoP Technology

by Raymond G. Clark and Joseph D. Poole
TT ELECTRONICS – IMS

Summary: *Lead-free package-on-package (PoP) technology is the latest in vertical electronics packaging integration and has become the preferred technology for mobile handheld electronics applications. TT electronics has developed the capability to assemble and rework numerous state-of-the-art packaging technologies, and this article addresses the essential engineering development activities performed to both assemble and rework PoP components.*

Abstract

Miniaturization continues to be a driving force in both integrated circuit packaging and PCB laminate technology. In addition to decreasing component pitch (lead-to-lead spacing), utilization of the vertical space by stacking packages has found wide acceptance by both designers and manufactures of electronics alike. Lead-free package-on-package (PoP) technology represents one of the latest advancements in vertical electronics packaging integration and has become the preferred technology for mobile handheld electronics applications. TT electronics in Perry, Ohio, has developed the capability to assemble and rework numerous state-of-the-art packaging technologies. This article will focus on the essential engineering development activities performed to demonstrate TT electronics' ability to both assemble and rework PoP components.

Background

For many years peripherally leaded packages were at the forefront of electronic packaging technology. In those days the main purpose of integrated circuit (IC) packaging was to protect the device inside from environmentally induced corrosion, provide mechanical protection, and provide an electrical path to the printed circuit board. This strategy proved effective until ever-increasing lead counts made the peripherally-leaded package impractical. The introduction of area array packaging technology solved this problem. In today's area array packaging, the leads are distributed across the entire surface of the package in a rectangular array fashion (Figure 1). Thus, a larger I/O count can be accommodated in a smaller area package. In fact, the area required for a peripherally leaded package increases exponentially with lead count while the area array package shows a linear dependence (Figure 2).

Figure 1: Illustrates the difference between QFP and BGA packages, showing an ultra-fine-pitch 160 lead QFP (pitch 0.3 mm) on a background consisting of the bottom side of a 1.5 mm pitch PBGA with 225 interconnection solder balls. From this picture it is easy to understand the popularity this BGA package has received among the people in the assembly business. Note that there are five QFP leads for every BGA solder sphere.

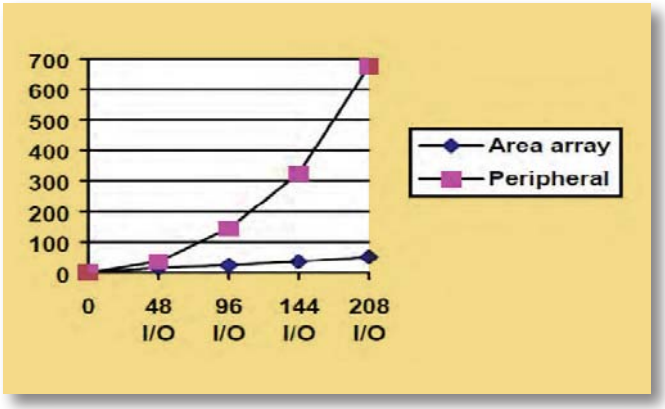

Figure 2: Peripherally leaded packages consume area at an exponential rate when compared to area array packages and the same pin count and lead pitch (0.5 mm pitch shown).

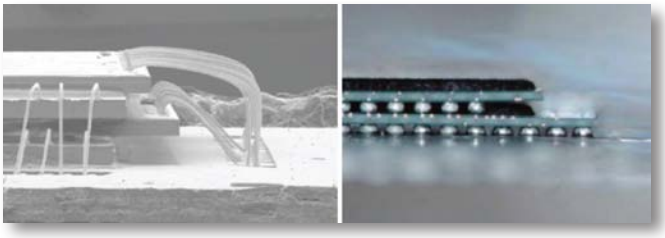

Figure 3: The stacked-die structure (left) versus the PoP structure (right).

In recent years the stacked packaging structure has found acceptance in the mobile handheld electronic market. By combining logic and memory chips into the same stacked package, designers can fit more function into a smaller and lighter form. The two predominant forms of stacked packaging structures are: the stacked die stricture and the PoP structure (Figure 3)[1].

The most obvious benefit of both PoP and the stacked-die structure is space savings; however, some other key differences make the PoP package the preferred embodiment. The main benefit of PoP structure is that the memory is decoupled from the logic device. Therefore:

1. The memory package can be tested separately from the logic package.
2. Only known good packages are used in the final assembly. Compare this to the stacked-die package where the entire package is thrown away if either the memory or logic is defective.
3. The end user controls the logistics. This means that the memory can treated as a commodity item and sourced from multiple suppliers.
4. Any mechanically mating top package can be used. Therefore, for a low-end phone, a smaller memory package can be used on the top package. For a high-end phone, more memory could be used with the same package.
5. Because memory only comes into play during final assembly, there is no need for logic suppliers to source memory.

Electrically, PoP offers benefits by minimizing track length between logic components and memory. This results in better performance of the devices since the shorter routing of interconnections between circuits results in faster signal propagation and reduction in "crosstalk" noise.

ASSEMBLY AND REWORK OF LEAD-FREE POP TECHNOLOGY *continues*

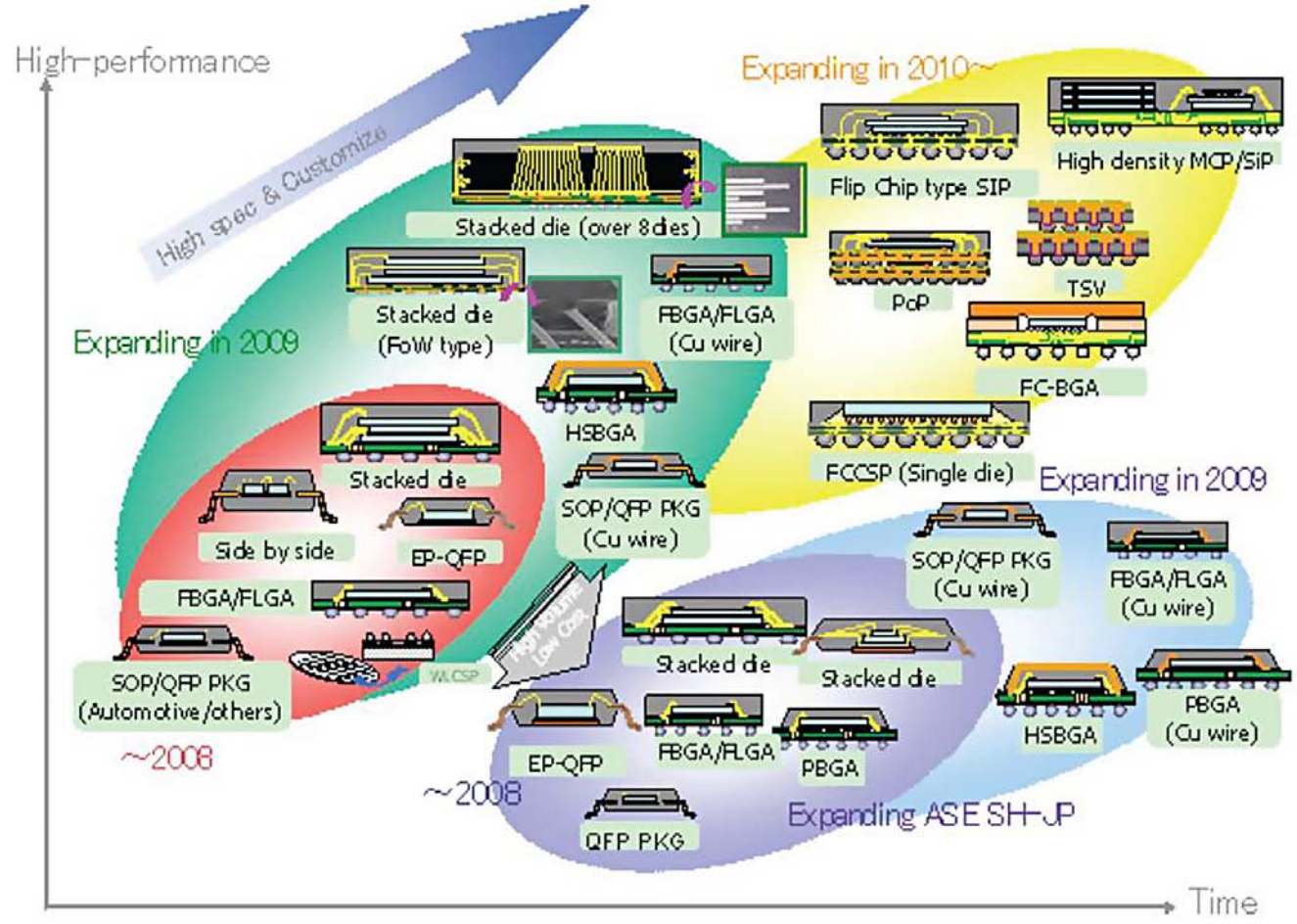

Figure 4: Trends in Integrated Circuit packaging 2009 courtesy of The Advanced Semiconductor Engineering Group of Japan.

TT Electronics has invested significant financial as well as engineering resources into the development of best-in-class assembly capability, thus aligning our assembly platform with the latest integrated circuit packaging technologies as well as those to come in the foreseeable future (Figure 4). Package-on-package technology represents one of the latest in trends in IC packaging. The use of PoP packaging technologies increases assembly complexity. To offset this added complexity, PCB assemblers must employ improved techniques of assembly and rework.

Test Vehicle and Components

The test vehicle used for this evaluation was a commercially available board with space for 15 PoP placements (Figure 5). The board size was 132 mm x 77 mm and 1.0 mm thick. Two different surface finishes were selected for this evaluation. Two different PCB surface finishes were investigated: ENIG (electroless nickel immersion gold) and OSP (organic solder preservative) [2, 3].

Figure 5: PoP test vehicle.

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Sincerely,

Lynn Hamilton
President, CEO
Custom Connections, Inc.

...and of course the customer is always right!

ASSEMBLY AND REWORK OF LEAD-FREE POP TECHNOLOGY *continues*

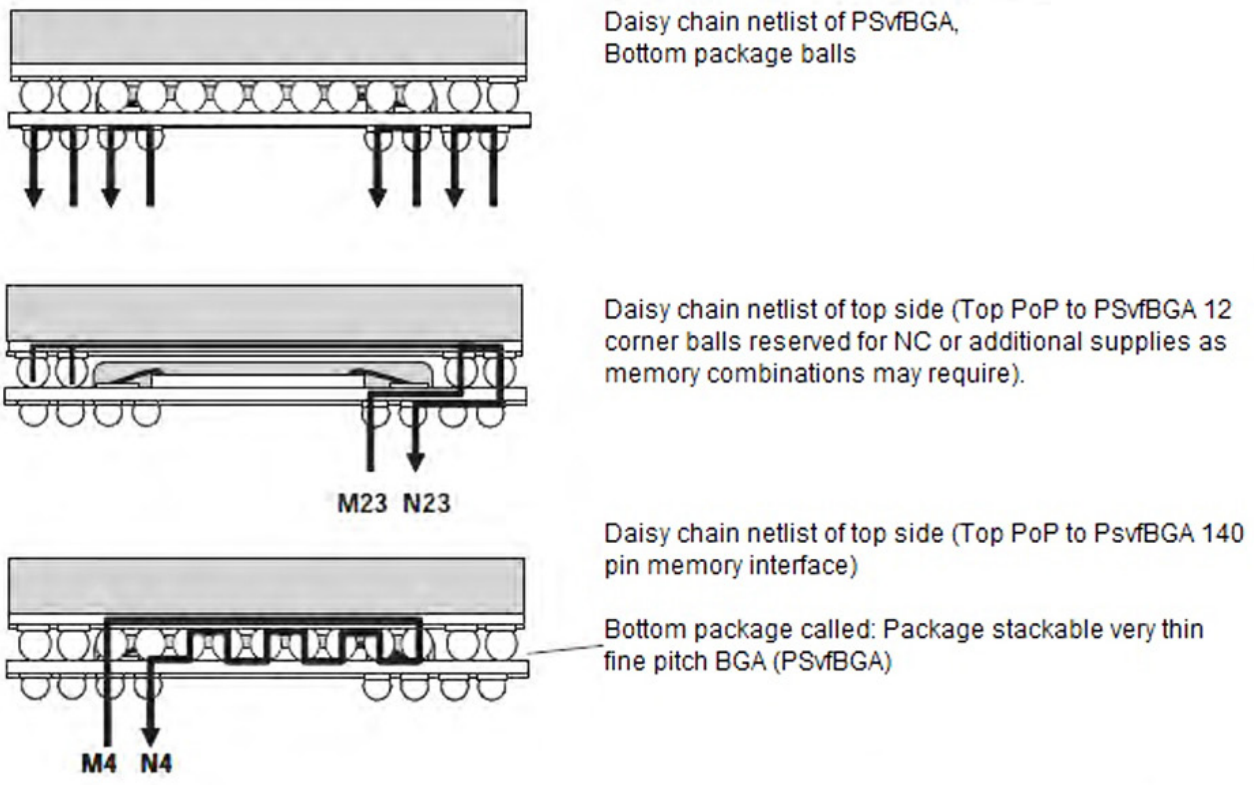

Figure 6: Electrical diagram of the three daisy chained network on each of the 15 sites of the test vehicle.

The pads on the test vehicles and the components are daisy chained together. There are a total of three networks for each populated location (Figure 6); one network for the entire bottom, one network for three leads located at each corner of the top package, and one network for the remainder of the leads on the top package.

The PoP components selected for our initial experiments were 14 mm x 14 mm. The bottom package had a four-row peripheral array of solder balls with 353 I/O on a 0.50 mm pitch (Figure 7). The top package had a two-row peripheral array with 152 I/O on a 0.65 mm pitch (Figure 8). The solder ball alloy for the top package and bottom package were SAC105 (Sn98.5/Ag1.0/Cu0.5) and SAC125 (Sn98.3/Ag1.2/Cu0.5) respectively.

PoP Assembly Considerations

The main goal of the PCB assembly test matrix was to determine the impact of several key

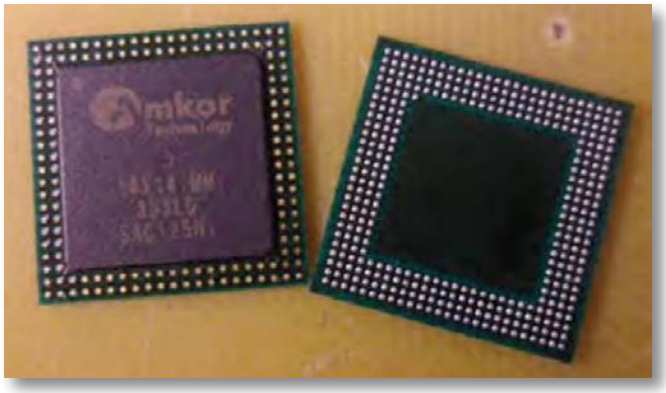

Figure 7: Bottom module.

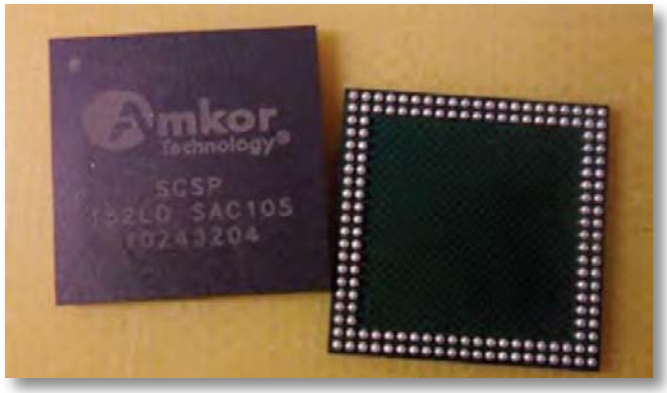

Figure 8: Bottom module.

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assembly variables on final assembly yield. An extensive literature search as well as discussions with the manufactures of PoP components and assembly material suppliers led to the following PCB assembly matrix (Table 1):

- Evaluation of the impact of two PCB surface finish options ENIG versus OSP on final assembly yield.
- Evaluation of two fluxing options (mesh V paste versus tack flux) for the top PoP package and their effect on final assembly yield.
- Development of a cost-effective method for transfer fluxing of the top PoP module.
- Development of a rework process for underfilled PoP components.

Test Vehicle Assembly

All test vehicles were assembled on a conventional surface mount technology (SMT) line. The test vehicle PCBs were all screened with a no-clean SAC 305 type III solder paste using a 5 mil thick stencil (Figure 9). The bottom packages were then placed directly on the test vehicle. The top packages were then dipped in either a flux or dippable solder paste prior to being placed on the lower package. A special fixture was developed for transfer fluxing of the top PoP package. An evaluation was conducted to determine the optimal method for transfer fluxing of the top PoP component (a transfer flux versus a "newly" developed ROLO SAC 305 transfer paste).

Once all PoP packages had been placed, the entire assembly was reflowed in a convection oven in an air environment. A reflow profile suitable for all ball metallurgies was used. The peak reflow temperature for the process ranged from 240°C to 245°C, with a time above 217°C ranging from 60 seconds to 70 seconds.

The underfill material was a reworkable epoxy based, heat cured material developed specifically for PoP applications. The underfill was a black opaque color and had a glass transition temperature (Tg) of 69°C. The coefficient of thermal expansion was 52 parts per million (ppm) below Tg and 188 ppm above Tg. The underfill was dispensed using a conventional adhesive dispenser and allowed to flow under the packages via capillary flow. Curing was accomplished using the recommended curing profile in air of 8 minutes at a temperature of 130°C.

PCB Surface Finish	Underfill	Forced Rework
ENIG	No	No
OSP	No	No
ENIG	Yes	No
ENIG	No	Yes
OSP	No	Yes
OSP	Yes	Yes
ENIG	Yes	Yes
OSP	Yes	No

Table 1: Test vehicle assembly matrix.

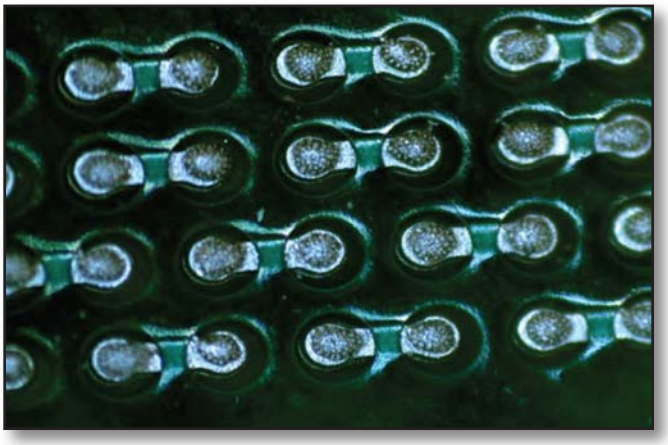

Figure 9: Solder paste print using a Type III SAC305 solder paste.

Forced Rework Process

Four cells of the test matrix were reworked. Two of the rework cells consisted of underfilled PoP packages. Rework was accomplished using a combination of infrared and hot air heating. Considerable effort was spent in developing a rework process for the underfilled components since the addition of underfill makes the rework process considerably more complex.

Transfer Fluxing Process

TT electronics engineers developed a semi-automated method for transfer fluxing the top module of the PoP package using a specially designed fluxing fixture (Figures 10a and 10b). This fixture was developed for low-volume, high-mix assembly processes. This fixture has 84 pockets machined to a depth equal to one-third the ball height of the top PoP module. Additionally, a locating mark was machined next to each pocket at a fixed distance. Using these locating marks, each location can be programmed into the placement machine for automated placement of the top module into the pocket. Care was taken to ensure that the outline of the TT Fluxing fixture was the same as a JEDEC matrix tray. In doing this, the tray can be utilized in the following manner:

- Transfer flux (or paste) is screened into the pockets.
- The fixture is then inserted into the placement machine and the top module is inserted into the pre-fluxed pocket.
- After the top module has been placed into each of the 84 pre-fluxed pockets, the tray is placed into the matrix tray handler of the placement platform.
- The pick-and-place tool is then used to place the bottom PoP module prior to placement of the pre-fluxed top module.

The TT PoP Fluxing fixture provided successful soldering results on numerous trial runs (Figures 11a and 11b). A survey of recent publications on PoP assembly revealed that the preferred method of assembly is to use a paste type transfer flux for the top module. It was determined that more consistent soldering results were obtained using the mesh V transfer paste for the assembly of the top PoP module; therefore, this material has been adopted as the process of record[4].

Rework of Underfilled PoP Packages

Reworking underfilled PoP packages represents a significant challenge for development of an effective rework process. To clarify the effect of temperature on the underfill shear strength it was determined that the shear strength of the underfill as a function of temperature needed to be quantified. It was determined that the shear strength of the laminate could best be measured using test coupons consisting of underfill sandwiched between two pieces of laminate. The test coupons were prepared using 1" square pieces of laminate with a thickness of 0.100". Thick pieces of laminate were used to ensure that no deformation of the sample occurred during shear testing. This allows for a more precise and consistent measurement of the underfill shear strength. To prepare the samples the following process was used.

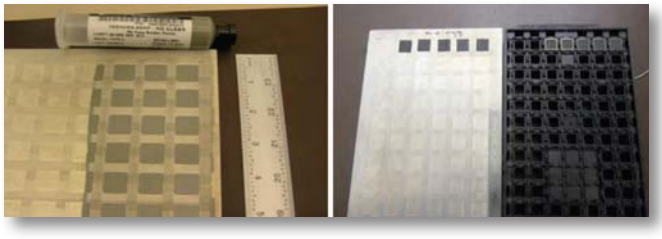

Figure 10: The PoP Transfer fluxing fixture developed by engineers at TT Electronics (left). Regular JEDEC outline matrix tray for 14mm PoP bottom and top modules (right).

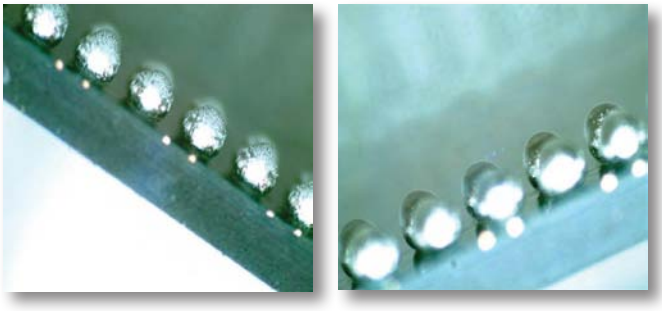

Figure 11a (left): Transfer paste (Type IV) ROLO, no-clean.

Figure 11b (right): Transfer flux, no-clean.

ASSEMBLY AND REWORK OF LEAD-FREE POP TECHNOLOGY *continues*

1. A controlled volume of underfill was then dispensed onto one of the laminate pieces. With the underfill acting as an adhesive and using temporary 0.005" shims to control the separation of the laminate pieces.

2. Two laminates were then joined together and temporally secured using clamps. The clamps ensured that there was no movement of the laminate/underfill sandwich prior to curing.

3. The samples were then cured for eight minutes as 130°C.

4. Using this technique laminate/underfill/laminate sandwiches were produced with a consistent underfill bond line thickness of 0.005". After curing the test samples were then placed into fixture which measured the shear strength of each sample.

Using this technique laminate/underfill/laminate sandwiches were produced with a consistent underfill bond line thickness of 0.005". After curing, the test samples were then placed into fixture, which measured the shear strength of each sample.

The fixture used to measure the underfill shear strength was then heated to temperatures of 230°C, 240°C and 250°C respectively. A thermocouple was used to ensure the underfill shear test samples reached the desired temperature. The samples were then sheared to failure (Figure 12) and the maximum shear strength at cohesive failure of the underfill was recorded. To ensure accurate shear strength measurements the area of the underfill deposit at the failure interface was measured and then used to determine the shear strength per unit area, (NOTE: all failures were cohesive in nature; no failures were observed at the underfill laminate interface.) A total of 10 measurements were taken at each of the three temperatures. The 10 readings in milli-Newtons per square millimeter were recorded and the data has been plotted in Figure 13. The underfill shear strength shows a consistent decrease in shear strength as a function of increasing temperature.

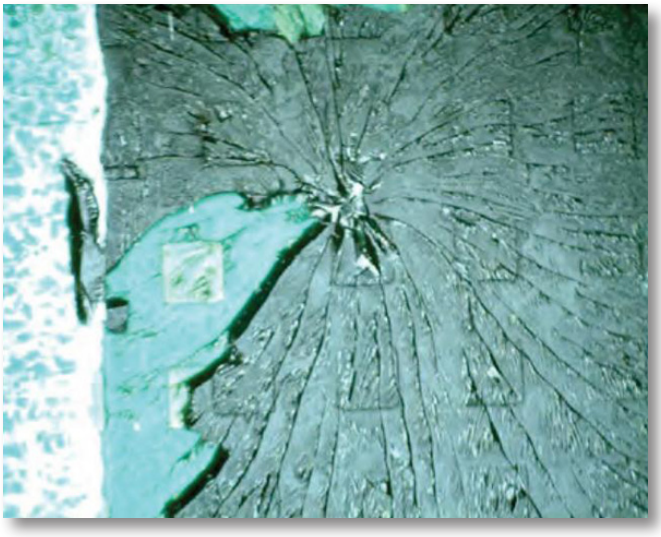

Figure 12: The cohesive failure interface of the underfill on the shear strength test coupons.

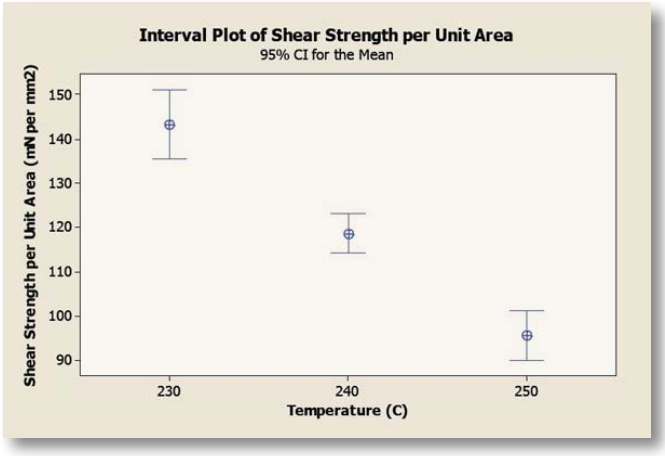

Figure 13: Plot of underfill shear strength at various temperatures of interest for SAC 305 rework.

The essential elements of successful PoP package rework involve the following steps [6, 7, 8]:

1. Heating of the PoP structure and removal of the underfill fillets from the perimeter of the package using a plastic scraping tool (taking care so as not to damage the laminate).

2. Heating of the PoP using an appropriate SAC305 profile.

3. Removal of the top and bottom PoP packages.

4. Removal of the residual underfill using flux as a solvent and heat (Figure 14).

5. Re-dressing the site using SAC305 alloy and a soldering iron.

6. Replacements of the top and bottom package followed by reflow using an appropriate profile.

7. Reapplying underfill and, finally, cure.

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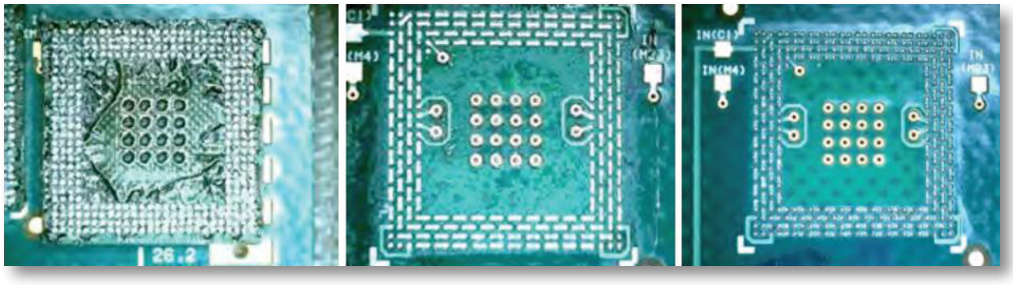

Figure 14: PoP rework site after removal of underfilled component (left); site after complete underfill removal (center); site after complete underfill removal and site redress (right).

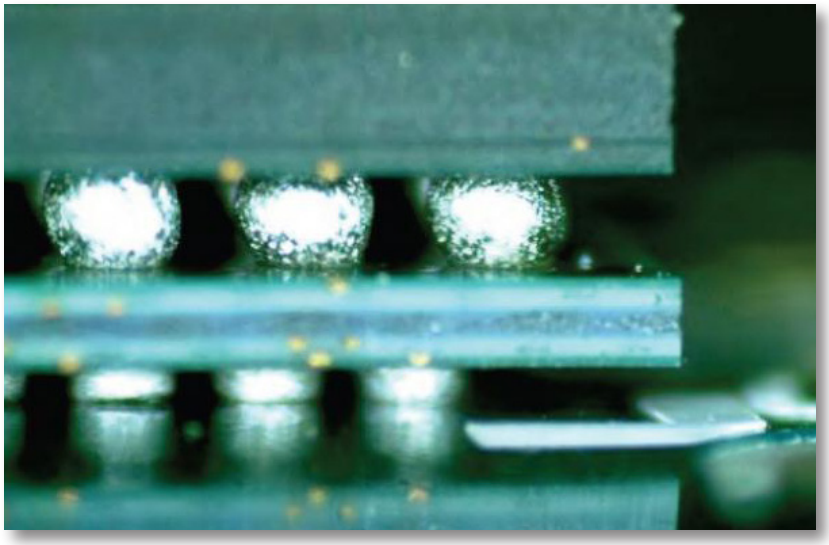

Figure 15: 45X image of OSP-reworked site.

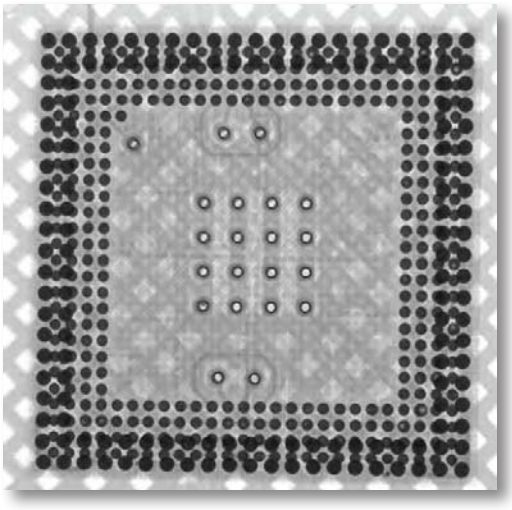

Figure 16: Transmission X-ray of ENiG forced reworked module.

Successful rework of the PoP components requires an automated rework tool with a transfer fluxing station, vacuum component handling system, split-optics for accurate placement and a real-time computer-controlled, closed-loop heating system using hot air and/or infrared heating (Figure 18).

Underfilled Options for PoP Packages

Two options are available when underfilling PoP packages. One involves underfill of the bottom PoP module only and the second involves underfilling both the top as well as the bottom PoP modules. A review of published literature reveals that the preferred method for optimal thermal cycle as well as drop test reliability involves applying underfilling of both top and bottom PoP modules. Thus, it was determined that all underfilling for the test matrix would be performed on both the top and bottom PoP modules [9, 10].

Assembly Results

Assembly Yield & Cross Sections

Following assembly, all packages were inspected using transmissive X-ray, perimeter solder joints were inspected using an ERSA scope and all modules were electrically tested using a digital multimeter. No failures were observed after assembly. Figures 15 through 20 show several images of the PoP packages after assembly and forced rework. Additionally no failures were observed in forced rework locations.

Conclusions

Work to date has established successful primary attach processes for package-on-package assembly using transfer fluxing of dippable Type V solder paste. In addition the TT PoP Fluxing fixture has shown its viability in volume manufacturing. Both combinations of PCB surface finish (ENIG and OSP) demonstrated excellent process yields. A rework process for underfilled

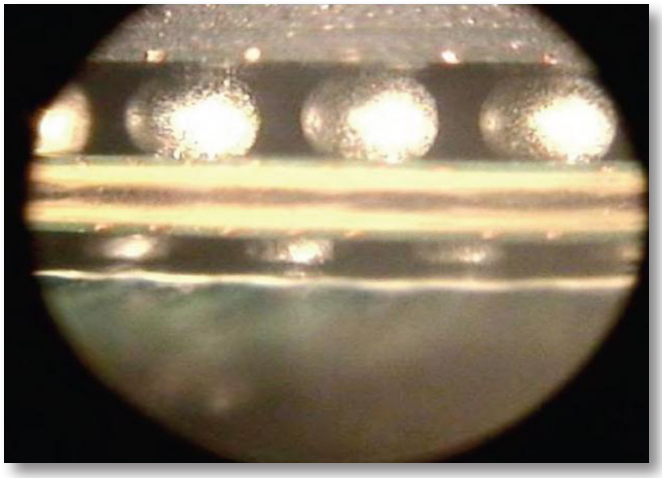

Figure 17: ERSA image of ENIG finish with forced rework.

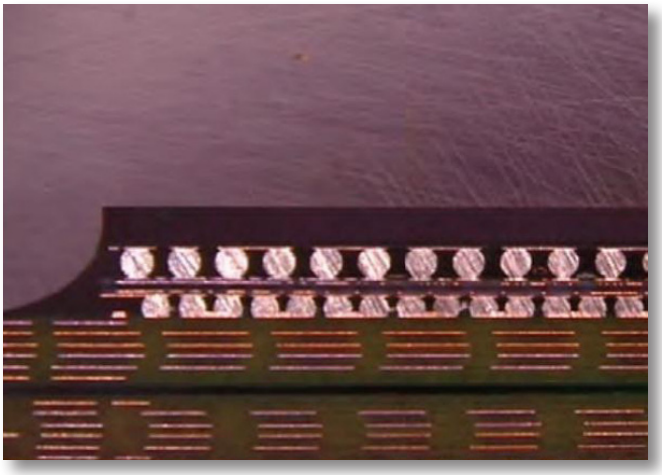

Figure 19: Cross-section of underfilled module with forced rework on ENIG finish.

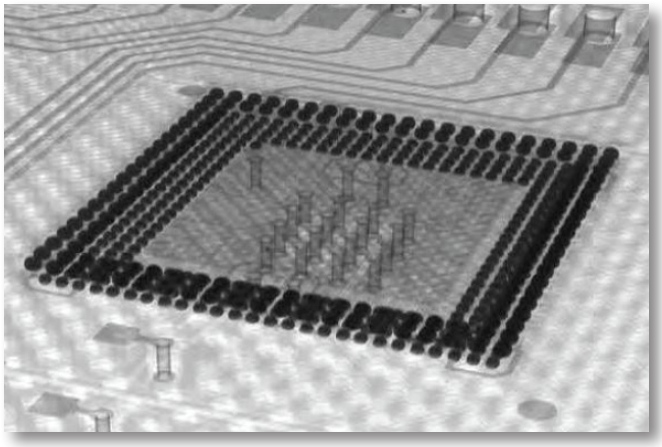

Figure 18: 3D X-ray image of PoP on PCB with ENIG finish.

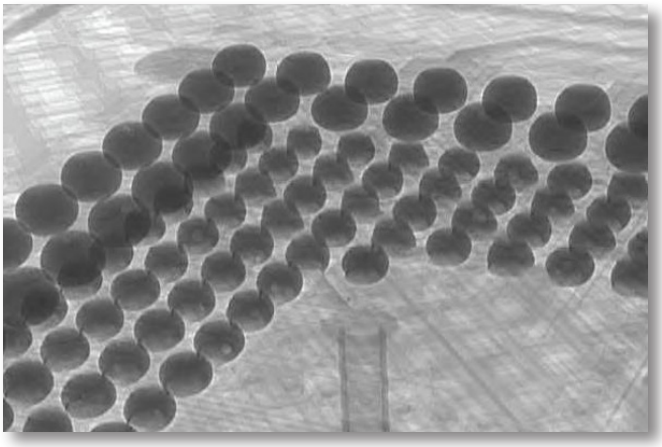

Figure 20: 3D X-ray of OSP forced reworked module.

PoP packages was developed and effectively demonstrated in a manufacturing setting. By successfully executing the build matrix with no electrical failures, TT electronics has shown its capability to effectively assemble PoP packaging technology. **SMT**

Acknowledgments

The authors would like to thank everyone that helped to make this a successful endeavor, especially David Molyneux, senior SMT production technician for his diligence in programming the Juki KE2060.

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Ray Clark began his career in TT electronics in 2006 as a senior test technician. He became a Certified IPC Trainer for the IPC-A-610 and IPC J-STD-001 in 2007. In 2008, he was given the position of senior training specialist. He regularly conducts formal training classes for the IPC A-610 Workmanship Standards Certification, IPC J-STD-001 Training and Certification, Solder Rework/Repair, and provides hands-on solder training for beginners and advanced applications and Solder Certification and Recertifications. Prior to TT electronics, Clark served in the United States Navy for 17 years as an electronics technician, where he performed various types of repair and rework of military electronics.

Joseph D. Poole is no longer with TT electronics.

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Large Diameter Wedge Bonding of Round and Ribbon Wire:

The Future for High-Power, High-Reliability Automotive Electronics

by Lee Levine
HESSE & KNIPPS GMBH

***Summary:** With automotive modules increasing in cost, field failures cannot be tolerated. Zero defects and optimum long-term reliability are essential for electronics manufacture and performance. Large diameter wire can help in reaching a zero-defect goal.*

Wedge bonding is widely used for interconnection of automotive engine control modules (ECMs) and other under-the-hood devices (see Figure 1). As vehicle electrification becomes more widespread, it will become even more prevalent. Bonding of large ribbon wire, Al, Cu, and Al-clad Cu will become a dominant technology due to the ribbon's large current-carrying capacity, excellent high-frequency conductance, and low inductance. As automotive

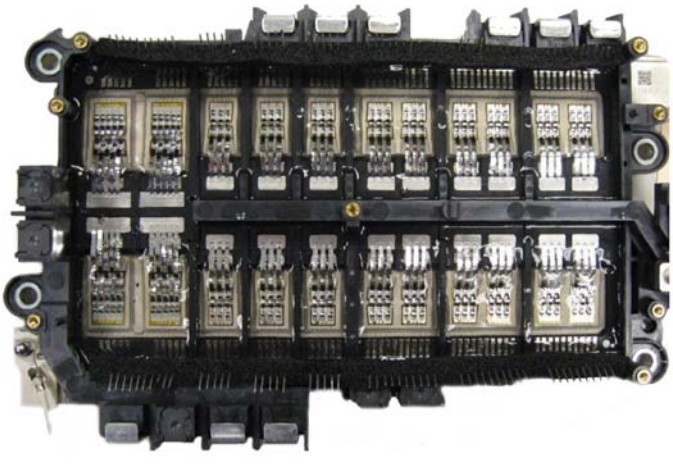

Figure 1: Prius engine control.

modules are expensive, field failures carry huge costs. Zero defects and optimum long-term reliability are essential during electronics manufacture and performance. Large diameter wire will support the goal of zero defects.

Bonding large diameter wire and ribbon requires substantially more energy than bonding fine wire. Ultrasonic generator output can be as high as 50W (Al wire) and 100W (Cu and ribbon) compared to 0.25W for fine wire bonders. Bond parameters are higher, with thicker metallization on leads or on substrates required. Soft-touch contact detection and closed-loop bond force control provide uniform bond deformation and high bond reliability.

For cantilever leads, lead shape and size must accommodate the larger forces and provide a stable surface for bonding. Lead cross-section and exposure length must be mechanically stiff to provide a stable bonding surface without resonating during bonding. If leads resonate, ultrasonic energy will be attenuated, resulting in poor bond quality.

The dynamics of loop formation with heavy wire are very different from that of fine wire. Relative stiffness (deflection under a load) for 20 mil wire is 160,000X that of 1 mil wire (stiffness is proportional to D [1]). During looping, significant forces are applied to both the first bond and to the underlying metallization while bending the wire. Loop profile and trajectory both have an important effect on minimizing those forces.

While looping motions that minimize bond stress effect bond quality, understanding bonding mechanics provides the process engineer with a big advantage in the development of optimized processes. Wedge bonders can bond both ribbon and round wire on the same platform with only a minor changeover. Heavy wire wedge bonders can bond both round bonding wire of up to 20 mils diameter and ribbon up to 80 mils width x 12 mils thick.

Heavy Wire Current-Carrying Capacity

Large diameter aluminum or copper round or ribbon wire are commonly used in electronic interconnection of ECM devices because of the high current required by these components. A 20 mil diameter, 100 mil length, 99.99% Al

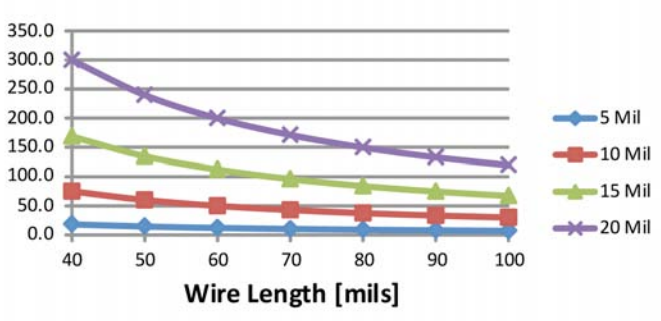

Figure 2: Safe DC current carrying capacity.

round wire can safely carry 120 amps [A]. Safe capacity is a better metric than fusing current, a metric commonly used. Fusing current is the amount of DC current that melts the wire and results in an open circuit; safe capacity is defined by its ability to produce less than a 83˚C temperature rise (in air or encapsulated). Figure 2 provides a graph showing safe DC current carrying capacity [amps] as a function of wire diameter and length for large diameter 99.99% Al wire [2]. It applies to DC current and low-frequency alternating current, as current flows through the entire cross-section of the wire for these conditions.

For short ribbons, safe current is the same as a round wire of the same cross-section (D=sqrt(4*w*t/ϖ)). As AC frequency increases, current flow moves by magnetic effects to the wire surface (skin) and is proportional to the wire perimeter (outer 0.5 µm of the surface). Ribbon wire, because the perimeter is larger than round wire of equivalent cross-sectional area, is capable of carrying more high-frequency current. In addition, ribbon wire induction is lower, enabling faster signal propagation. As a result, ribbon bonding is becoming an important alternative for automotive electronics.

As insulated gate bipolar devices (IGBT power modules) carry high currents and have very high switching rates, they are increasingly ribbon bonded. Heavy ribbon not only carries the high currents required, but also helps transfer heat out of the IGBT. Ribbon as large as 12 mils thick x 80 mils (in Al, Cu-clad, Al, and Cu) can be bonded with a heavy wire bonder. As we move toward vehicle electrification, with much higher energy demands for power storage in banks of parallel connected batteries, ribbon bonding will be the leading-edge interconnec-

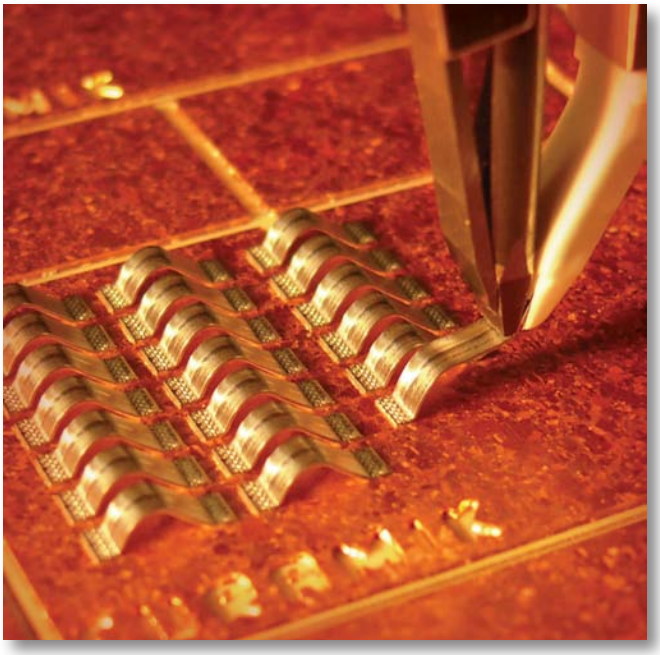

Figure 3: Copper ribbon bonds.

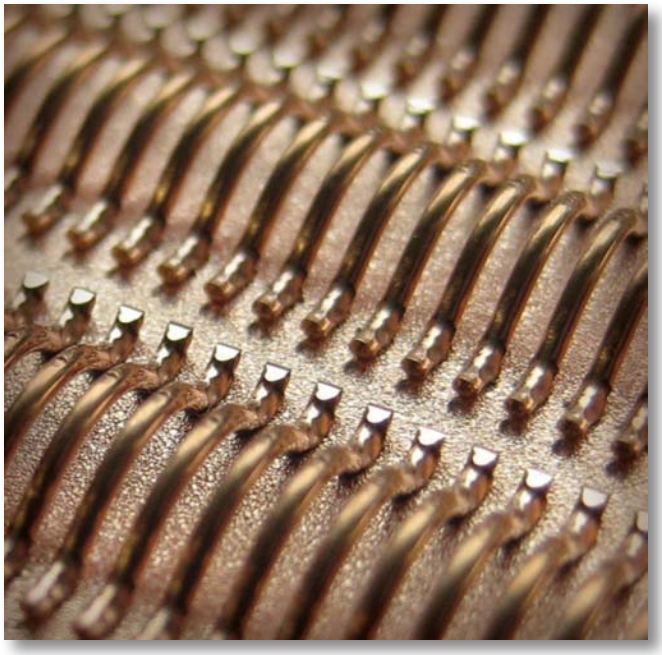

Figure 4: V groove.

tion technology. Figure 3 depicts wedge bonding with large ribbon.

Wedge and Active Cutter Configuration

Heavy wire wedge tools are configured differently than fine wire wedges because, after forming second bond, the wire is cut by the "active cutter" located behind the tool. This differs from fine wire wedge bonding where the wire is terminated by either clamp or table tear motions. The active cutter provides a precision depth cut that improves bond reliability, limits impact force, and increases cutter life expectancy. Programming both cutter speed and force provides better control than previously available. When reverse bonding (second bond on the die bond pad), the active cutter is so precise that bonding is accomplished without marking the die surface. The ability to program cut depth as a percentage of the wire diameter enables reverse bonding on sensitive structures.

Using the active cutter, the second bond heel can have a full cross-section, enabling the use of "V" and "U" groove tools (see Figure 4) that capture a large portion of the wire cross-section within the groove, without reducing the area of the second bond heel. The increased cross-section allows bonds to achieve both higher pull strength and higher shear strength than achievable with conventional shaped tools.

Fine wire wedge bonding requires a smaller cross-sectional area (more deformation) behind second bond to reliably terminate the wire.

Process Integrated Quality Control (PIQC™)

High-cost, high-reliability devices used for automotive packages require a much higher level of quality assurance than lower-cost commodity ICs. Automotive packages often carry much higher current and must operate in one of the most difficult environments. Under-the-hood operating conditions are high-stress environments. With the new government initiatives for vehicle electrification, higher currents and more difficult thermal stress will increase already difficult requirements. High long-term reliability and zero defects in manufacturing are required.

Some newer wedge bonders have real-time quality monitoring features that are unavailable on ball bonders. PIQC™ is one such bond quality measurement system that uses multi-variate analysis to determine bond quality and transmit the data to the factory computer system. Tracking of bond quality enables an exact record of each bond to be stored and eliminates bad bonds from entering the system.

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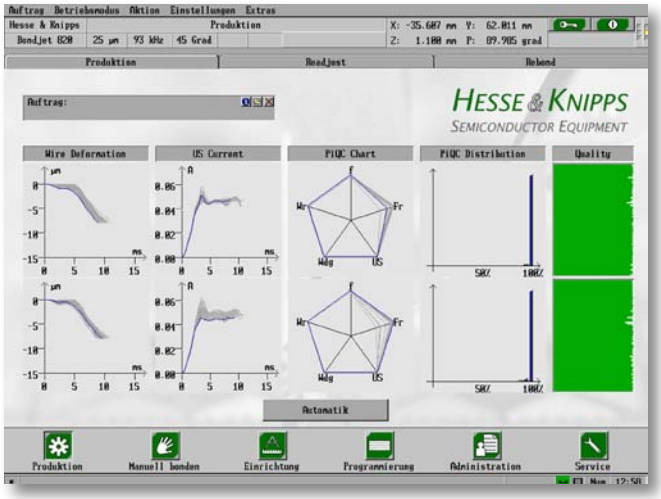

Figure 5: Screen capture of a radar chart.

PIQC™ incorporates a patented sensor, mounted directly on the ultrasonic transducer that captures real-time measurements of friction at the bond interface and amplitude of the tool tip. During bonding, the system monitors and captures both the normal ultrasonic control signals and the unique signals reflected from the bond interface to the PIQC sensor. More than five individual signals are monitored and analyzed using multi-variate analysis including: ultrasonic current, transducer impedance, ultrasonic frequency, tool displacement, and bond interface friction. Each signal is compared to a standard and graded. Different types of defects, such as scratches, contamination, and bonding off-pad, trigger different responses from the indicators. A combination of five response indicators is used to maximize quality discrimination. A quality decision algorithm determines the overall quality grade. Acceptance limits can be specified that will either flag a poorly bonded device or stop the process for operator assistance. The "radar chart" provides a graphic picture of the five signals simultaneously. Figure 5 is a screen capture of some of the quality tools demonstrating the bond uniformity and showing a radar chart.

The process engineer can monitor production operations from his desk and be assured that the process is meeting requirements. Traceability of each device bond record assures that quality is maintained throughout the system and that it is well documented.

Conclusion

Wedge bonding large diameter wire and ribbon provides a highly-flexible, high-reliability process that is widely used for automotive applications. The high volumes and high reliability required by the automotive industry are being met by new, innovative developments such as PIQC, ribbon bonding of larger size wires, copper round and ribbon bonding, and active cutting. Heavy wire wedge bonding will continue to add new capabilities that enable new automotive applications. **SMT**

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As a distinguished member of the technical staff for Hesse & Knipps, Inc., Lee Levine provides support for customers with challenging wedge bonding process requirements. In addition, he researches and presents technical papers on various aspects of wedge bonding.

A degreed expert in metallurgy, Levine has more than 30 years of semiconductor materials, manufacturing, and process development experience. The recipient of the IMAPS 1999 John A. Wagnon Technical Achievement Award, he holds four patents and has published over 70 technical papers. His major innovations include copper ball bonding, loop shapes for thin, small outline packages (TSOP and TSSOP, and CSPs) and introduction of DOE, and statistical techniques for a better understanding of the wire bond assembly process.

Levine is founder of Process Solutions Consulting, Inc.; his company currently provides process consulting, yield improvement, SEM, EDS, and metallography services to customers in the microelectronics industry. Levine is also an IMAPS Fellow and has served as IMAPS' vice president of technology. He may be reached at Levine@hesse-knipps.us.

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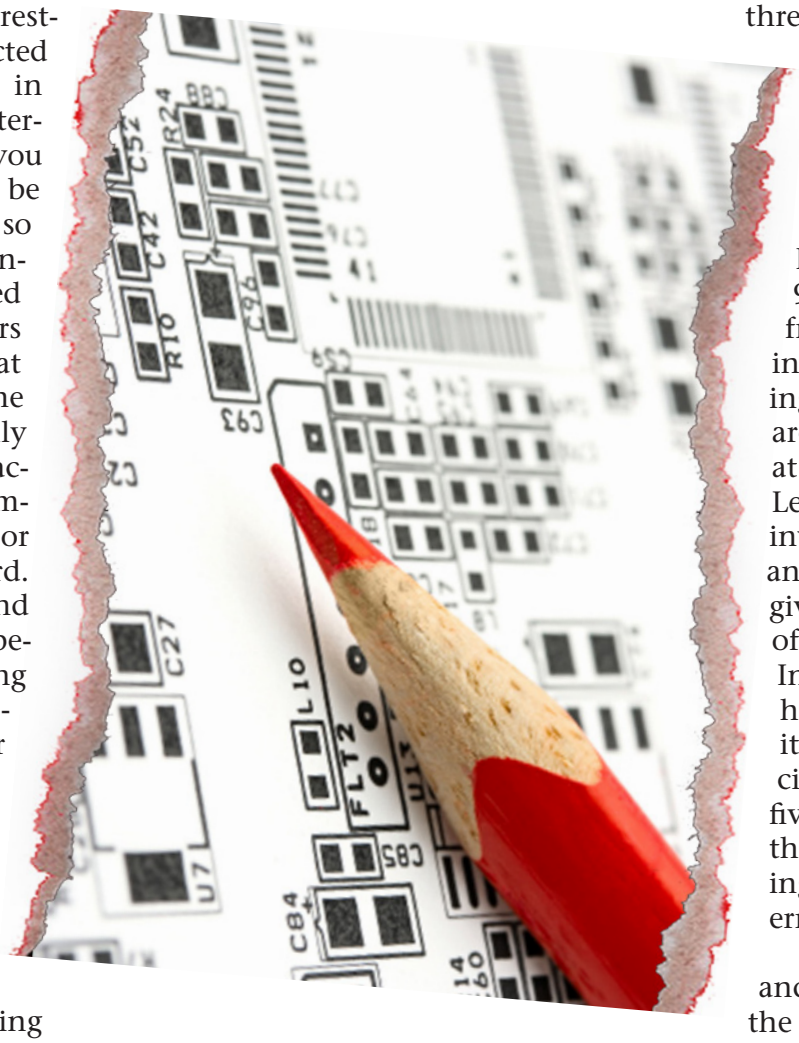
ZULKI'S PCB NUGGETS

In Praise of an Accurate Fab Drawing

by Zulki Khan
NexLogic Technologies

Summary: A highly detailed and accurate fab drawing is the linchpin for avoiding pitfalls and inadvertent errors in board fabrication. The delineation between a great product and one that's merely average is how well specifications are written, how much detail is included, and how accurate those specifications are.

The PCB fabrication drawing, also known as a fab drawing, is perhaps one of the most interesting, yet often neglected and abused areas in the industry. An interesting fact when you consider that it can be misinterpreted in so many ways. For instance, inexperienced PCB layout engineers may put in what they believe to be the right numbers only to discover their actions have led to ambiguity and a faulty or non-working board. Without practical and in-depth layout experience, a fab drawing can keep you guessing on whether or not you've made the right choice.



One thing is for sure: A highly detailed and accurate fab drawing is the linchpin for avoiding pitfalls and inadvertent errors in board fabrication. The delineation between a great product and one that's merely average is how well specifications are written, how much detail is included, and how accurate those specifications are.

A highly qualified PCB layout engineer needs to include a number of pieces of detailed information in a fab drawing to ensure a board is correctly fabricated to precisely comply with the design. Due to space limitations here, I'm not able to detail all the information required in a correct fab drawing. Rather, I'll focus on the three crucial areas that demand a PCB layout engineer's utmost attention: Stack up, material, and drill chart.

The most prevalent item missing 99% of the time from a fab drawing is information specifying how many panels are to be stacked up at the drill machine. Let's say the project involves 100 boards and no specification is given on the number of panels to stack up. In this case, the fab house takes it upon itself to make that decision and stacks up five or six panels and then performs drilling, which can cause errors.

This creates a meander, thus increasing the tolerance and reducing reliability because you should only stack up two to maybe three panels at a time. It's important to note here that

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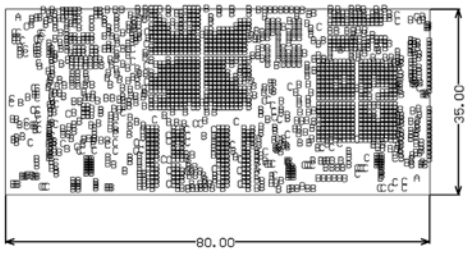
IN PRAISE OF AN ACCURATE FAB DRAWING *continues*

CAM350 V 10.5 : Wed May 30 15:23:51 2012 - (Untitled)
NOTES: UNLESS OTHERWISE SPECIFIED

1. UNLESS OTHERWISE NOTED, ALL DIMENSIONS ARE IN INCHES.
   TOLERANCE: +/- .003.
2. PCB TO BE FABRICATED PER IPC-A-600 OR MOST CURRENT VERSION.
3. SOLDERMASK TO BE PHOTO-IMAGEABLE OR DRY FILM (GREEN).
4. ALL PLATED HOLES TO HAVE MIN. WALL THICKNESS OF .001 COPPER.
   ALL HOLE DIAMETERS ARE AFTER PLATING.
   .005 MIN. ANNULAR RING PERMISSIBLE.
5. ALL EXPOSED PADS OR COPPER NEED TO BE GOLD PLATED ENIG.
   10 MICRO INCHES OF GOLD OVER 150 MICRO INCHES ELECTROLESS NICKEL
6. BOARD WARPAGE SHALL NOT EXCEED .007 PER DIAGONAL INCH OF BOARD AS PER IPC-D-300.
7. USE ROUTE AND RETAIN WITH MOUSE BITES INSTEAD OF V-SCORES.
8. SILKSCREEN TO BE NON-CONDUCTIVE EPOXY INK.
   NO SILKSCREEN ALLOWED ON EXPOSED PADS OR IN HOLES.
   MIN CLEARANCE BETWEEN SILKSCREEN LEGEND AND VIAS, PADS, OR HOLES
   TO BE .005.
9. ALL BOARDS SHALL BE FULLY TESTED FOR CONTINUITY PER SUPPLIED IPC 356 D NETLIST
   BY COMPARING WITH GERBER DATA BEFORE FAB AND NOTIFY THE RESPONSIBLE ENGINEER
   OF ANY NETLIST DISCREPANCIES.
   ALL BOARDS SHALL BE 100 ELECTRICALLY TESTED FOR OPENS/SHORTS.
   APPLY TEST STAMP IN NON-LEGEND AREA ON SOLDER SIDE OF PCB.
10. FINISHED BOARD INCLUDING ANY SOLDERMASK OR LEGENDS SHALL HAVE A UL. FLAMMABILITY RATING OF 94V-0.
    DATE CODE AND MANUFACTURERS UL SYMBOL/TYPE SHALL BE PERMANENTLY MARKED OR ETCHED ON THE BOARD.
11. PCB TO BE FABRICATED PER IPC STANDARD IPC-A-600D CLASS 2.
12. ALL UNCONNECTED PADS ON INTERNAL LAYERS MAY BE REMOVED.
13. IMPEDANCE CONTROLLED
    4.5 MILS TRACES ON LAYERS 4, 5, 7, 8, 11, 12, 14 & 15 NEED TO HAVE SINGLE ENDED IMPEDANCE OF 50 OHMS +/- 10 TOLERANCE.
    4.5 MILS TRACES ON OUTER LAYERS NEED TO HAVE SINGLE ENDED IMPEDANCE OF 50 OHMS +/- 10 TOLERANCE.
    4 MILS TRACES ON LAYERS 4, 5, 7, 8, 11, 12, 14 & 15 NEED TO HAVE DIFFERENTIAL IMPEDANCE OF 100 OHMS +/- 10 TOLERANCE.
    4 MILS TRACES ON OUTER LAYERS NEED TO HAVE DIFFERENTIAL IMPEDANCE OF 100 OHMS +/- 10 TOLERANCE.
    VENDOR CAN ADJUST TRACE WIDTHS TO ACHEIVE DESIRED IMPEDANCE.

Symbol	Hit Count	Tool Size	Plated	Hole Type
B	1733	8mil (0.2032mm)	PTH	Round
C	130	10mil (0.254mm)	PTH	Round
A	2	98.425mil (2.5mm)	PTH	Round
	1865 Total			



LAYERS	18
MIN LINE WIDTH/SPACING	4 MIL / 4 MIL
SOLDER MASK	LPI (GREEN) BOTH SIDES
SILK SCREEN	WHITE BOTH SIDES
THICKNESS	0.080 + /- 10
MATERIAL	PCL-370HR
COPPER THICKNESS	1/2 OZ.

18 LAYER STACK UP

(100 ohms)DIFFERENTIAL TRACE	(50 ohms)SIGNAL TRACE	GERBER EXTENSION	DESCRIPTION	CU WEIGHT
		.GTO	TOP SILK SCREEN	
		.GTS	TOP SOLDERMASK	
4 MILS 8 MILS 4 MILS	4.5 MILS	.GTL	L1-TOP	0.5 OZ.
		.GP1	L2-PWR PLANE	0.5 OZ.
		.GP2	L3-GND PLANE	0.5 OZ.
4 MILS 12 MILS 4 MILS	4.5 MILS	.G1	L4-SIG1	0.5 OZ.
4 MILS 12 MILS 4 MILS	4.5 MILS	.G2	L5-SIG2	0.5 OZ.
		.GP3	L6-GND PLANE	0.5 OZ.
4 MILS 12 MILS 4 MILS	4.5 MILS	.G3	L7-SIG3	0.5 OZ.
4 MILS 12 MILS 4 MILS	4.5 MILS	.G4	L8-SIG4	0.5 OZ.
		.GP4	L9-PWR PLANE	0.5 OZ.
		.GP5	L10-GND PLANE	0.5 OZ.
4 MILS 12 MILS 4 MILS	4.5 MILS	.G5	L11-SIG5	0.5 OZ.
4 MILS 12 MILS 4 MILS	4.5 MILS	.G6	L12-SIG6	0.5 OZ.
		.GP6	L13-PWR PLANE	0.5 OZ.
4 MILS 12 MILS 4 MILS	4.5 MILS	.G7	L14-SIG7	0.5 OZ.
4 MILS 12 MILS 4 MILS	4.5 MILS	.G8	L15-SIG8	0.5 OZ.
		.GP7	L16-GND PLANE	0.5 OZ.
		.GP8	L17-PWR PLANE	0.5 OZ.
4 MILS 8 MILS 4 MILS	4.5 MILS	.GBL	L18-BOTTOM	0.5 OZ.
		.GBS	BOTTOM SOLDERMASK	
		.GBO	BOTTOM SILK SCREEN	

0.080 + /- 10

the drill stack is limited by the PCB's thickness and the flute length of the drill tool. No more than two to three panels should be stacked at a time; otherwise it adversely affects the aspect ratio, which is quite often missing from the fab drawing. So what happens in the absence of this panel stack-up information? The fab house goes ahead and uses as many panels as possible on the stack up—creating trouble.

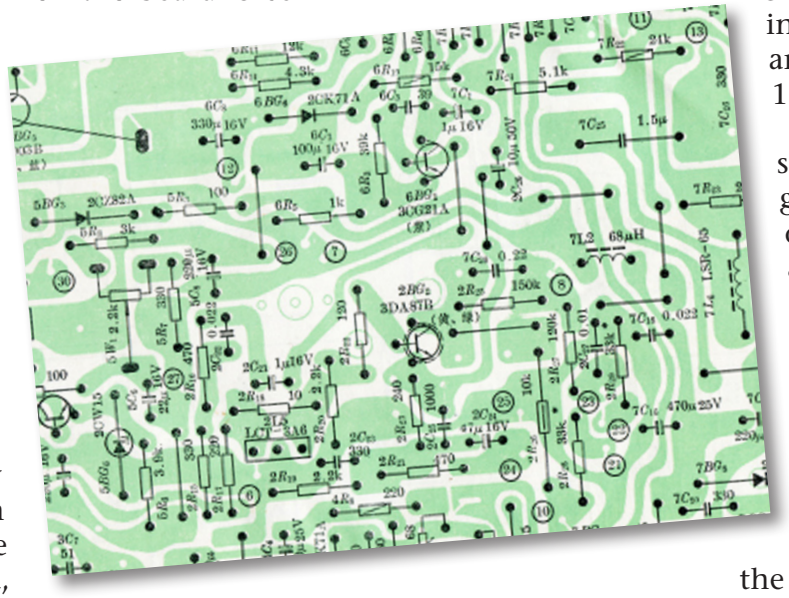
A fabrication drawing and its detailed notes should also define the board material to be used. This particular description should include the manufacturer's name, grade, thickness, and number of layers. This information is critical, and particularly so since 80 to 90% of all PCBs use FR-4 material as a default.

FR-4 comes in many grades. Some, like FR406 and FR408, are high-temperature materials and several manufacturers make products equivalent to FR-4 material. It's important, therefore, to call out one primary material. If the preferred material is not available, a specific secondary material should be spelled out instead of stating "or equivalent."

If the term "equivalent" is clearly stated in the fab note, the fab house technician is left to his or her discretion and has no other choice but to select what they consider to be the correct material. In some cases, the fab house may have a standing policy to use the least expensive "equivalent" material. Consequently, this lower-priced material could pose problems in terms of performing at higher temperatures and may even fail at those temperatures, say 180° or more. In fact, the material may only be capable of reaching 170°.

IN PRAISE OF AN ACCURATE FAB DRAWING *continues*

Material thickness must also be noted. If it's a multilayer board, the layer stack-up must be detailed. Such detail includes how the layers are stacked, pre-preg thicknesses, how far apart they are from internal layers, and whether or not the pre-preg construction is balanced. If it's not a balanced construction there may be a possibility of warping when the board is complete.



Now we come to the drill chart and slots. The drill chart is basically a nomenclature of how many and what type of drills are used on a particular board. Are they plated or non-plated? Are they round, oblong, or oval? Are they intended for certain slots? Also, if angle slots are involved, extremely precise definition of those slots is demanded using a data point from which to measure the angle. That slot should be properly defined with correct X and Y coordinates; otherwise, a board built with a wrong slot has no other place to go but the trash.

Now, let's talk a bit about the drill holes themselves. The novice PCB layout engineer (or one who doesn't have practical in-house manufacturing interaction and experience from which to draw) often erroneously creates a whole gamut of different drill holes, shapes, and sizes, thus making PCB manufacturing difficult.

Generally, these engineers are relying solely on their theoretical knowledge for making decisions and performing the layout portion dealing with drill holes. They are not familiar with manufacturing and don't know how drill machines work. Often they're unsure of the type of drill holes required. In cases like this, the usual routine is to pull a component from a component library without paying much attention to drill size or making it uniform.

At the same time, the PCB layout engineer does not stop to consider that many of the components on a given layout are similar. For example, let's say that engineer calls for three different drill holes—13, 15, and 18 mils. He or she could have minimized that number to only one by only using a 15 mil hole with a +/- 3 mil tolerance, meaning that hole could be anywhere from 12 to 18 mils.

In contrast, the savvy PCB layout engineer thinks in the opposite direction and favors minimizing drill holes so as to use as few holes as possible on a drill chart. It follows, then, that the fewer the drill holes, the easier it is to manufacture the board. When there are too many drill holes fab houses sometimes make the decision to combine some of them, which can create a major problem for assembly.

It's best for everyone concerned to limit drill holes to 15 or fewer. That number is adequate enough to accommodate the many different types of components required by the layout. **SMT**

Zulki Khan is the founder and president of NexLogic Technologies, Inc., in San Jose, California, an ISO 9001:2008 Certified Company, ISO 13485 certified for manufacturing medical devices and a RoHS-compliant EMS provider. Prior to NexLogic, Khan was General Manager for Imagineering, Inc. in Schaumburg, Illinois. He has also worked on high-speed PCB designs with signal integrity analysis. He holds a B.S. in EE from NED University in Karachi, Pakistan, and an M.B.A. from the University of Iowa. He is a frequent author of contributed articles to EMS industry publications.

Top Ten Most-Read Supplier/ New Product Highlights

IPC Updates Stencil Design Guidelines

IPC-7525B provides guidelines for the design and fabrication of stencils for solder paste and surface-mount adhesive with discussion on through-hole and mixed technology. The updated standard includes differences for tin-lead and lead-free solder paste, overprint, two-print, and step stencil designs.

Tin Whiskers Focus of UK Symposium

November 27-28, 2012, the Center of Advanced Life Cycle Engineering at the University of Maryland and Department of Materials Research at Loughborough University will hold the 6th International Symposium on Tin Whiskers at Ford College, Loughborough University, UK.

IPC Midwest to Address Challenges in Manufacturing

The two-day exhibition will feature electronics manufacturing's top suppliers to companies in advanced microelectronics, aerospace and military, automotive, medical and industrial equipment and devices, telecommunications, and other industries. Leading experts will share the latest research on manufacturing defect-free, quality electronic products as part of the technical conference.

Plexus to Build New Facility in Wisconsin

Plexus Corporation intends to construct a 410,000 square foot manufacturing facility in Neenah, Wisconsin. This facility will replace two existing leased facilities in Neenah and will consolidate approximately 1,000 employees into the new building. The facility is expected to cost approximately $50 million, with construction expected to begin in July 2012 and to be complete in fall 2013.

Tough Road Ahead for Flextronics, Jabil

The sputtering U.S. economy and stalled unemployment levels are certainly a concern and those with the majority of their operations in the U.S. could be in for an uphill battle for the remainder of the year. Waning demand out of Europe is also a concern, and the ongoing Eurozone crisis is showing no signs of letting up.

Variosystems Expands in China; Builds New Facility

The company broke ground on a future China facility in Suzhou (Wuzhong District) on March 23, 2012. The new manufacturing location will meet the growing demand of existing customers and will draw interest for customers looking at China for offshore manufacturing.

eXception Aids Apollo, Upgrades Supply Chain Process

eXception Group has worked with Apollo on a sophisticated supply chain solution that has increased service levels and reduced costs for the company. The two companies devised a lean supply chain process that significantly improved delivery and supply of eXception Group's 4.8 million circuit boards it supplies each year to Apollo.

Murrietta Receives Sandia National Laboratories Award

Andrew Murrietta, vice president sales and marketing and co-owner, announced that his company has won a Supplier Performance award from Sandia National Laboratories 10th Annual Production supplier conference for Weapons Engineering and Product Realization. The conference, with a theme of "Defying Obstacles," was held to allow Sandia to recognize their suppliers and thank them for their valuable service over the last year.

SMTC San Jose Boosts Capabilities

This expansion highlights SMTC's commitment in advancing their current manufacturing capabilities and development of new services offered to OEMs in California. The company now has advanced capabilities to offer such as dedicated prototyping lines, additional SMT capacity and state of the art testing technology. Also added to the facility is a new Class 10,000 Clean Room which will service the growing demand from medical device OEMs seeking controlled environment capabilities for final assembly and packaging services.

SigmaTron Acquires Spitfire Control

"We have a long term relationship with Spitfire and this was the next logical step. With this acquisition, SigmaTron will add two excellent manufacturing operations in locations that will augment our international footprint. We believe that Mexico will continue to grow as the manufacturing location of choice in North America and Vietnam will continue to be a relatively low cost manufacturing location in Asia," said Gary R. Fairhead, SigmaTron's president and CEO.

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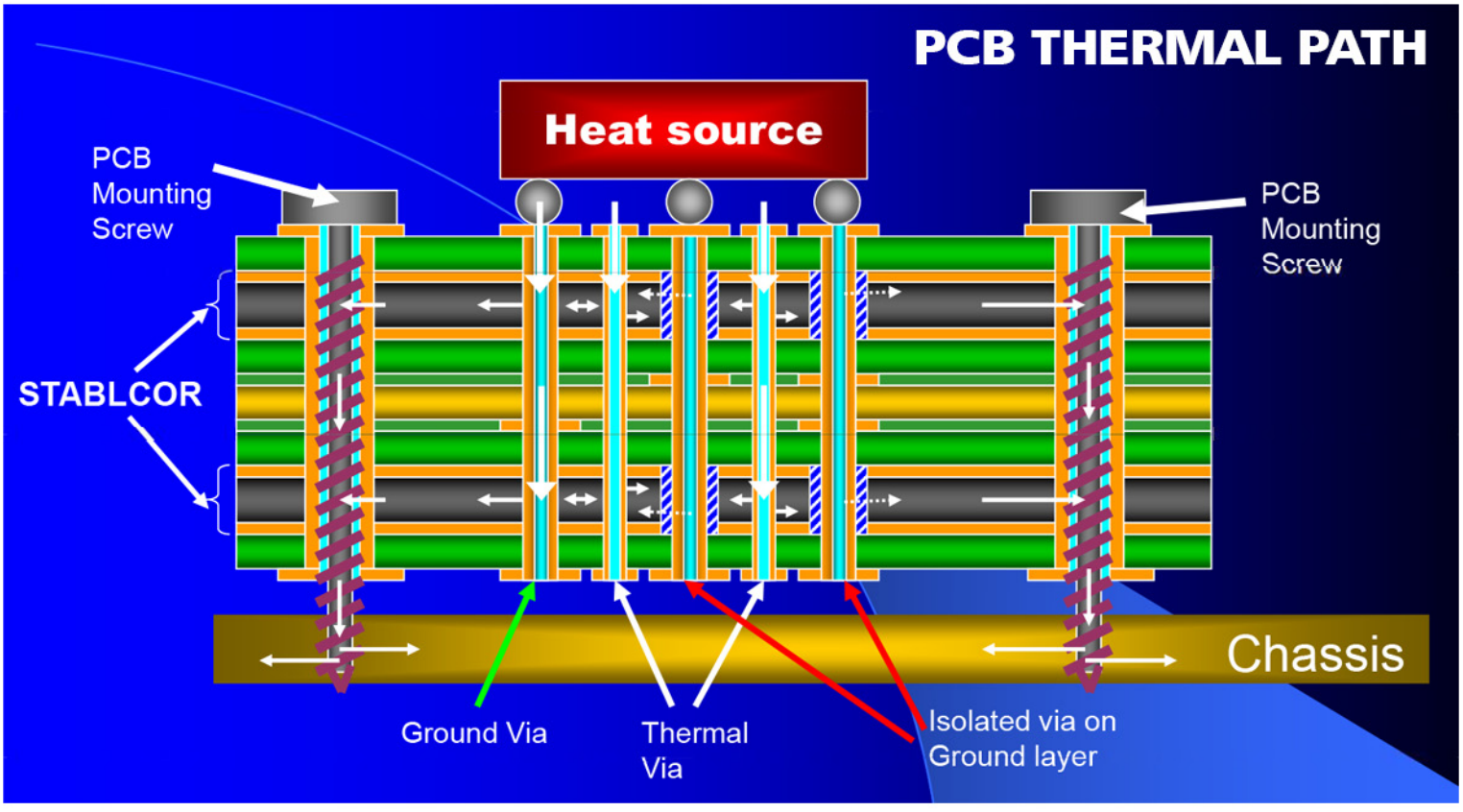

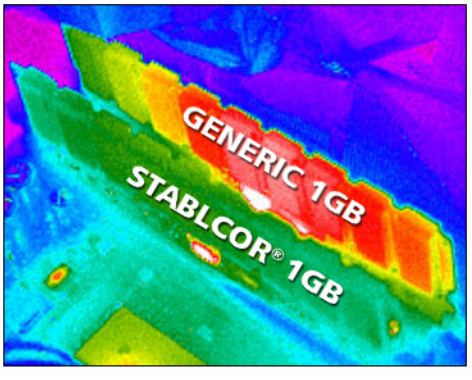

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THE SUPPLY SIDE

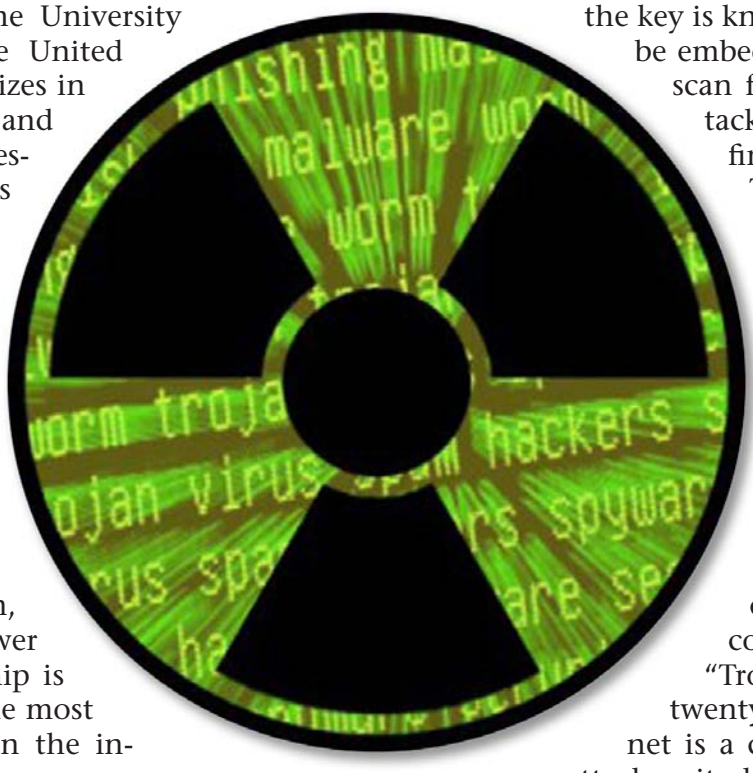
Microsemi Denies Security Issue

by Christopher Torrioni
SENSIBLE MICRO CORPORATION

Summary: Researchers have made a discovery that has left many in the industry dumbfounded. Is a "backdoor" open to Actel's ProASIC3 chip? To make matters worse, it appears this alarming feature was deliberately designed into the silicon. Chris Torrioni takes a closer look.

Security breaches and counterfeit chips seem to be dominating industry news cycles on a weekly basis; however, last week a new story broke that has left many simply scratching their heads.

Dr. Sergei Skorobogatov, a senior research associate at the University of Cambridge in the United Kingdom who specializes in attack technologies and tamper-resistant processors for Cambridge's Hardware Security Group, posted a possible "backdoor" finding into Actel's ProASIC3 chip. Actel, now owned by Microsemi, markets the chips to critical application users such as the U.S. government for weapon technology, aviation, and nuclear and power systems. The PA3 chip is marketed as one of the most highly secure chips in the industry.



The research document, drafted by Skorobogatov and Christopher Woods from Qua Vada Labs, claims to have used an innovative patented technique and was able to extract the secret access key using Pipeline Emission Analysis (PEA), ultimately activating backdoor control. According to the posted document, the backdoor is only available on the actual silicon and has not been detected in any firmware loaded onto the chip.

Traditionally, bugs or flaws in firmware are easily fixed with a patch. No fixes are available for the actual hardware of the chip or silicon which makes the group's findings even more alarming since the devices are actively deployed in the field. Skorobogatov further states, "This permits a new and disturbing possibility of a large-scale Stuxnet-type attack via a network or the Internet on the silicon itself. If the key is known, commands can be embedded into a worm to scan for JTAG, then to attack and reprogram the firmware remotely." The only known fix would be to recall all chips in use for replacement, which is highly unlikely at this point.

Stuxnet-style attacks have become the weapon of choice for those involved in cyber warfare. Discovered in 2010 and commonly labeled the "Trojan Horse" of the twenty-first century, Stuxnet is a computer worm that attaches itself deep into a computer system—usually supervisory control and data acquisition (SCADA) equipment—corrupting files and reprogramming code. These worms specifically target critical applications and industries such as military networks, industrial controls, and financial institutions.

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MICROSEMI DENIES SECURITY ISSUE *continues*

Stuxnet continues to be the largest viral threat in cyberspace today. In fact, it's what many experts believe is targeting Iran's nuclear program. Originally, most thought the Stuxnet virus was built to steal secret codes or factory formulas in Siemens automation software, enabling terrorists or malicious users to counterfeit devices. Experts now believe that is not the case. The Stuxnet worm looks specifically for Siemens software-based equipment that has the exact settings needed to inject its code and reprogram the programmable logic device (PLD) for the application. Stuxnet has also destroyed major operating systems in Indonesia and India to date.

Researchers from The University of Cambridge further concluded the Actel backdoor entry was deliberately designed into the silicon. Some are pointing the finger at China where the chips were actually manufactured; however, Skorobogatov now states that he does not believe that to be the case. This has sparked much debate in the chip community and again raises the question as to why some of our highest security electronic devices are being made in a region that is widely known for stealing intellectual property rights and leading the trend in counterfeiting devices. Even if this case isn't found to be designed with malicious intent, doesn't this keep the door wide open for that to happen in the future?

Robert Graham, an industry expert from Errata Security posted a response to the claims of deliberate backdoor intent on his blog, stating: "It could just be part of the original JTAG building-block. Actel didn't design their own, but, instead, purchased the JTAG design and placed it on their chips. They are not aware of precisely all the functionality in that JTAG block, or how it might interact with the rest of the system. I'm betting that Microsemi/Actel know about the functionality, but thought of it as a debug feature, rather than a backdoor. It's remotely possible that the Chinese manufacturer added the functionality, but highly improbable. It's prohibitively difficult to change a chip design to add functionality of this complexity."

Graham went on to say, "On the other hand, it's easy for a manufacturer to flip bits. Consider that the functionality is part of the design, but that Actel intended to disable it by flipping a bit, turning it off. A manufacturer could easily flip a bit and turn it back on again. In other words, it's extraordinarily difficult to add complex new functionality, but they may get lucky and be able to make small tweaks to accomplish their goals."

Finally, last week, a much anticipated response by Microsemi was made in a statement with regard to the security findings by the Cambridge researcher team and posted it on their website. Microsemi is denying that any "backdoor" entry in their ProASIC3 chip was deliberately designed that enables the circumvention of security. They further claim the UK Security Research Team has not contacted them with regard to their findings. **SMT**

Christopher Torrioni is president and co-founder of Sensible Micro Corporation, a professional stocking distributor and sourcing partner to hundreds of global OEM and EMS manufacturing companies. He obtained his Bachelor's Degree from the University of Central Florida and brings 11 years of industry knowledge and experience in electronic component supply, market news, procurement pitfalls and quality assurance standards. Torrioni is also a corporate sponsor to the SMTA Tampa Bay Chapter as well as the Tampa Chamber of Commerce and Tampa Bay Technology Forum.

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— Sue Knight
Surface Technology International, Ltd.

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Top Ten Most-Read Mil/Aero007 Highlights

Flextronics Earns Lockheed Supplier Excellence Award

The award was given to Flextronics in recognition for excellence in program performance in support of Lockheed Martin's Space Systems Company. The award recognizes program performance in meeting and exceeding technical, cost, and schedule objectives.

Sanmina-SCI's ISWICS Secures NSA Type 1 Certification

"Achieving this high-level certification is a critical milestone for our division where the ISWICS is designed and manufactured, and we're proud to be able to provide this important capability to ensure the success of current and future missions conducted by the Army, Navy, Air Force, or Marine Corps," said Mike Underwood, president, Defense and Aerospace Systems Division.

Counterfeits' Widespread Effects the Focus of Conference

Companies attempting to manage the growing challenge of counterfeit electronic components face a range of government- and industry-related pitfalls that make it virtually impossible to eliminate all risk associated with the plague of fake parts.

Sparton, USSI JV Secures U.S. Navy Sonobuoy Contract

Sparton Corporation and USSI, a subsidiary of Ultra Electronics Holdings plc (ULE) announce the award of subcontracts valued at $10.5 million to their ERAPSCO joint venture for the manufacture of sonobuoys for the United States Navy.

Lockheed Martin, Arrow Electronics Ink Supply Chain Deal

Lockheed Martin has signed a new strategic enterprise agreement with Arrow Electronics covering procurement of more than 22,000 electronic components used in advanced technology systems such as missiles, satellites, radar systems, tactical fighter aircraft, and unmanned surveillance systems. It represents Lockheed Martin's largest agreement with any single supplier for these commodities.

PartnerTech Expands Capability; Acquires Aerodyn AB

PartnerTech has acquired Aerodyn AB, a company focused on contract manufacturing of heavy components for ship propulsion with propeller systems or water jets. The company's estimated yearly turnover is approximately 40 MSEK and it will be consolidated into the Machining operating segment from the second quarter 2012. Aerodyn employs approximately 20 people and is based in Karlskoga, Sweden.

Northstar Completes Acquisition of Echotec Sonar

With Echotec now being the cornerstone entity of Northstar Electronics, the company plans to aggressively develop innovative, leading-edge sonar systems needed by the defense, homeland security, commercial shipping, cruise ship, and commercial fishing sectors. Echotec will pursue contract opportunities to design, develop, and build systems for projects in North America and internationally.

Navy Awards $12.9 M Contract to Sparton, USSI JV

ERAPSCO will provide production subcontracts in the amount of $4 million and $8.9 million to Sparton Electronics Florida, Inc. and USSI respectively. Production will take place at Sparton's DeLeon Springs, Florida facility as well as USSI's Columbia City, Indiana facility and is expected to be completed by January 2014.

New DARPA Program Seeks New Cooling Solutions

Recent advances of the DARPA Thermal Management Technologies program enable a paradigm shift—better thermal management. DARPA's Intrachip/Interchip Enhanced Cooling (ICECool) program seeks to crack the thermal management barrier and overcome the limitations of remote cooling. ICECool will explore "embedded" thermal management by bringing microfluidic cooling inside the substrate, chip, or package by including thermal management in the earliest stages of electronics design.

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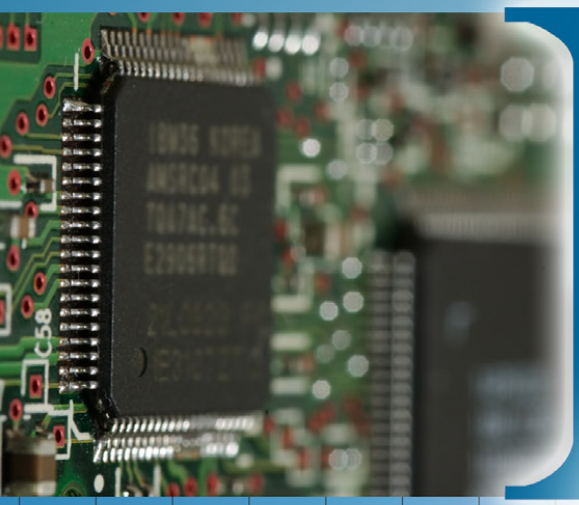

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Most-Read News Highlights from SMTonline this Month

1 Koh Young Celebrates Delivery of 3,000th SPI System

In making the announcement, Dr. Kwangill Koh, CEO, said, "We are honored to have Mack Technologies deploy our KY8030-3 systems to optimize their electronics manufacturing process. My thanks go out to the entire Koh Young family whose dedication, perseverance, and commitment to excellence and customer satisfaction have made this possible."

2 Applied Nanotech Introduces Thermally-Conductive Bonding Materials

THERCOBOND is specially designed for power electronic device packaging and dielectric coating, with an optimal combination of thermal conductivity, thermal diffusivity, thermal expansion, dielectric and insulating properties, wettability, and printability.

3 P. KAY Metal's MS2 Earns Two New Patents

P. KAY Metal, Inc. has been informed that two more important patents covering its MS2® chemical dross elimination material and process have been granted. The latest patents granted in the past week are in Japan and Singapore.

4 Pulse Electronics Introduces Pin-in-Paste RJ45 Connectors

The company introduces pin-in-paste RJ45 connectors with integrated magnetics. This method, also called pin-in-hole or intrusive reflow, is a process that allows through-hole components to be reflow soldered instead of wave soldered. This option has been added to the PulseJack™ JXR0 and JXR1 1x1 tab-down and tab-up 100BASE-T integrated connector module product families.

5 Henkel to Acquire Cytec Industries' PSA Product Range

Henkel has signed an agreement with the U.S.-based specialty chemicals company Cytec Industries Inc. to acquire its high-performance pressure sensitive adhesives product range. PSAs are specialized adhesives used in the packaging, automotive, electronic, and durable goods industries for foils and films, tapes, or labels offering high-performance adhesive characteristics.

6 Nordson ASYMTEK Debuts New Jetting System in Japan

Central to the new jetting system is the Genius™ Jet Cartridge, an innovative, one-piece jet that is quickly and easily removed without tools for cleaning or replacement, and is a significant advancement to the next step in jetting technology. The cartridge also features built-in memory to store usage data like the number of cycles and cartridge type.

7 TK, Microtek Launch New HATS Lab in Europe

Tech Knowledge (TK), in cooperation with Microtek Laboratories, is proud to announce the launching of TK Lab—the first test laboratory in Europe and the Middle East that will provide HATS thermal shock test services as well as HATS systems to the printed circuit board and electronic interconnect industries.

8 MEK Installs New AOI System at SMTC Ontario

MEK Europe BV, formerly known as Marantz Business Electronics, and its distributor, CGI Americas, recently announced the installation of the fourth AOI system within SMTC. The Toronto-headquartered EMS provider recently commissioned an iSpector HDA 650, complementing systems in operation at its San Jose, California and Chihuahua, Mexico facilities.

9 Nordson EFD Demos Latest Fluid Dispensing Tech

The company, a subsidiary of Nordson Corporation, demonstrated their latest fluid dispensing technologies for improving electronics manufacturing processes at Jisso/Protec Japan 2012, in Tokyo June 13-15, 2012. Nordson EFD products, including their EFD products, are available in Japan exclusively from Nordson K.K or their official distributor network.

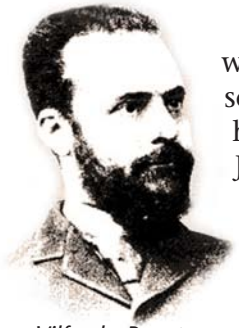
10 Essemtec Supplies SMD Tower to ABB

ABB Semiconductors in Lenzburg, Switzerland, long searched in vain for a suitable production storage system for HiPak IGBT modules production. Project Manager Prabath Lewdeni found the SMD Tower by chance. Its supplier, Essemtec, re-engineered the SMD component storage system into clean room storage for ABB.

THE SALES CYCLE

The Critical 20

by Barry Matties
I-CONNECT007


Vilfredo Pareto

The Pareto Principle, otherwise known as the 80/20 Rule, is something most in the industry have heard of, but rarely utilize. Just to clarify, the principle says that 80% of effect comes from 20% of cause. The principle was named after Vilfredo Pareto by the well-known consultant Joseph Juran back in 1906. According to some, the idea arose from an observation by Pareto in his vegetable garden. Since then, the principle expanded into all areas of business, economics, and, as it turns out, in all aspects of everyday life.

Is it really true? See for yourself: A simple audit begins with data collection from your own business or life.

Many areas can be examined and you will most likely find that 80% of the results come from 20% of the inputs:

- Sales: 80% are created from 20% of your products.
- Sales: 80% of sales are produced by 20% of your sales team.
- Manufacturing defects: 80% occur from the same 20% of reasons.
- Profits: 80% are derived from 20% of your customers.
- Problem employees: 80% of the problems come from 20% of the people.

So, if you start seeing the trend and realizing the 80/20 Rule is in effect throughout your business, then improving your business really becomes more a question of how well you can identify the critical 20% in each area and focus on that as it applies to your current mission. Such analysis will give you the greatest result and, with focus, give your entire team clarity on what they should be working on to get the greatest overall result for the organization. This process is really one of the quickest and easiest ways to improve your business.

For example, by focusing, your sales team will know exactly what to sell—they can have a strong emphasis on the products that bring in the 80% of your sales. They can then also focus on the customers that fit in the critical 20% that produces 80% of results. Meanwhile, your manufacturing team can work on the critical 20% of your manufacturing processes that will increase yields and reduce cycle time. With this tune-up alone, you can really change your profit margins.

The Pareto Principle does not say or imply that we should not perform 100% of the job or function. It merely suggests that the best use of time for the greatest result, 80%, will be found in the first critical 20% of inputs. And, in some areas, like employee problems, that may be sufficient to reduce the noise, if you will. Take process improvement—it's never done. But let's say you want to reduce your cycle time by X.

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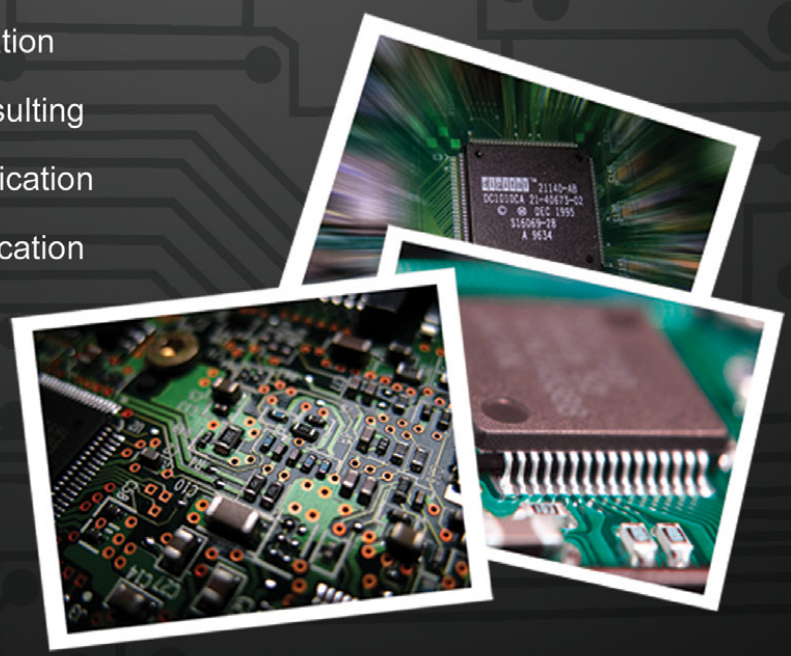

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THE CRITICAL 20 *continues*

You will achieve the first 80% of X by focusing on the inputs that represent the critical 20%. In this 20% you will quickly find your largest bottlenecks that, if removed, would substantially reduce your cycle time. The next time you perform cycle-time process improvement your overall cycle time will be less, but you will still look for the critical 20% and find the next set of bottlenecks. Finally, at some point, you will find that cycle-time reduction itself is no longer part of the critical 20% needed to achieve your current mission.

This is where good business leadership comes in. Someone or some leadership team in your company has to be clear on what the objectives are for your business. Next, they have to really be able to focus the energy of the entire company around those objectives. Of course, some companies have more resources to focus on multiple areas simultaneously, while others may only be able to focus on one or two areas. In either case, use the Pareto Principle to guide you—80% of your goals can be achieved by focusing on the critical 20%.

By the way, I think Steve Jobs was a master of focus. When he returned to Apple he reduced the huge product mix they had to the critical 20%, realizing the rest was noise and a huge distraction to becoming a great company. **SMT**

Barry Matties is the publisher of the I-Connect007 family of publications. He started in PCB manufacturing in the early 1980s and in 1987 became a founder of *CircuiTree Magazine,* which sold nearly 13 years later as the leading industry publication. In the early 2000s, Barry and longtime business partner Ray Rasmussen joined forces again and acquired PCB007 and launched the I-Connect007 family of publications. Later, in July 2010, *SMT Magazine* and SMT China was also acquired by I-Connect007. With his proven successful business development and leadership skills, Barry now produces this column relating over 25 years of successful business experience, including business, marketing and selling strategies that really work. Contact Barry here.

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EVENTS

For the IPC's Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar, click here.

For a complete listing of events, check out *SMT Magazine's* full events calendar here.

ASQED Microelectronic Olympiad
July 9, 2012
Bayan Lepas, Malaysia

Ohio Valley Expo and Tech Forum
July 12, 2012
Independence (Cleveland), Ohio

Future Horizons Semiconductor Industry Forecast Seminar
July 17, 2012
London, England

IPCA International EXPO 2012
July 25-27, 2012
Bangaluru, India

27th International Fair of the Electrical, Energy and Automation Industry
August 7-10, 2012
Expominas, Belo Horizonte – MG, Brazil

Brasil Consumer Electronic Expo
August 14-16, 2012
Sao Paulo, Brazil

IPC Midwest Conference & Exhibition
August 22-23, 2012
Schaumburg, Illinois

Capital (D.C.) Expo and Tech Forum
August 23, 2012
Laurel, Maryland

NEPCON South China 2012
August 28-30, 2012
Shenzhen, China

Webtorial: Design and Assembly Process Challenges for Bottom Terminations Components (BTCs) such as QFN, DFN and MLF in Tin-Lead and Lead-Free World
September 6 & 13, 2012

Automation 2012
September 7-10, 2012
Mumbai, India

Electronics Goes Green Conference 2012
September 9-12, 2012
Berlin, Germany

PCIM South America
September 11-13, 2012
Sao Paulo, Brazil

West Penn Expo and Tech Forum
September 13, 2012
Monroeville, Pennsylvania

EIPC Summer Conference
September 13-14, 2012
Milan, Italy

The ECOC Exhibition
September 16-20, 2012
Amsterdam, The Netherlands

Advancement in Thermal Management 2012
September 18-19, 2012
Denver, Colorado

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Next Month in SMT Magazine

Discovered in the 1940s, tin whiskers can spontaneously form on tin-based, lead-free finished surfaces even at room temperature. Because of their ability to conduct electrical current, tin whiskers can also cause electrical shorts and initiate metal vapor arcs—leading to failure. The August issue of SMT Magazine will bring a host of industry experts to address tin whisker growth, risk mitigation, detection, and failure analysis.

If you're not yet a subscriber, don't miss out! Click here to receive SMT Magazine in your inbox each month.

See you in August!